

IN THE UNITED STATES DISTRICT COURT  
FOR THE DISTRICT OF DELAWARE

SENTIENT SENSORS, LLC,

Plaintiff,

v.

CYPRESS SEMICONDUCTOR  
CORPORATION,

Defendant.

Civil Action No. 1:19-cv-01868-MN

**SECOND AMENDED JOINT CLAIM CONSTRUCTION CHART<sup>1</sup>**

Plaintiff, Sentient Sensors, LLC (“SS”), and Defendant, Cypress Semiconductor Corporation (“Cypress”), respectfully submit the following Second Amended Joint Claim Construction Chart pursuant to the Court’s recent Orders (D.I. 66; D.I. 76).

The parties have agreed to the following constructions: The parties have agreed to withdraw their competing proposals for following terms and will simply apply the plain meaning of these terms going forward:

| <b>Claim Term</b>                                                                                                                              | <b>Joint Proposed Construction</b> |
|------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|
| Original Term 3: Oscillator(s)<br>(‘177 Patent, Claims 1, 6, 10, 14, 19)                                                                       | Plain and ordinary meaning         |
| Original Term 6: “processor configured to automatically activate from totally deactivated (unpowered) state”<br>(‘177 Patent, Claims 3, 7, 12) | Plain and ordinary meaning         |
| Original Term 7: “a plurality of gates arranged in a field programmable gate array”<br>(‘177 Patent, Claims 1, 6, 10, 15)                      | Plain and ordinary meaning         |
| Original Term 8: “configured to run independent processes”<br>(‘177 Patent, Claims 1, 6, 10)                                                   | Plain and ordinary meaning         |

<sup>1</sup> While the parties present herein citations to the intrinsic record of primary relevance, they reserve the right to cite and discuss any portion of the patent or file history to respond to each other’s claim construction briefing.

The parties dispute the constructions of the following terms (including any related terms) of asserted claims in U.S. Patent No. 6,938,177 (the “’177 patent”):

| No. | Claim Term                                                           | Plaintiff’s Proposed Construction                                                                                                                      | Plaintiff’s Intrinsic Evidence                                                                                                                                                                                                                                                                     | Defendant’s Proposed Construction                                                                                                                                                                        | Defendant’s Intrinsic Evidence                                                                                                                                                                                                                        |
|-----|----------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | “An instrument controller”<br><br>(’177 Patent, Claims 1-20)         | An electronic circuit that provides “System on a Chip” control functions consistent with the performance and operation of an Integrated Circuit device | <p><b>Specification:</b><br/>Col. 3, ll. 55-60; Col. 1 l. 64 – Col. 2 l. 1.</p> <p><b>File History:</b><br/>Examiner search strategy and results 3-9-2005</p> <p>Remarks and claim amendments - Reply to Office Action date 2-25-2005</p> <p>Original claims – Application as filed 12-19-2001</p> | multi-chip module instrument controller                                                                                                                                                                  | <p><b>’177 Patent:</b><br/>Patent Title; Abstract; Figs. 1-3; 1:11-18; 1:20-2:31; 2:32-4:20; 6:6-31.</p> <p><b>File History:</b><br/>Original Claims; Applicant 2/25/05 Reply, including pp. 1-16; Office Action 12/8/04; Notice of Allowability.</p> |
| 2   | Embedded<br><br>(’177 Patent, Claims 1, 5, 6, 9, 10, 13, 15, 17, 20) | “on-chip”                                                                                                                                              | <p><b>Specification:</b><br/>Col. 3 l. 5, 17, 35 and 67 Col 4, l. 58; Col. 8 l. 45 – Col. 9 l. 6 and 17.</p> <p><b>File History:</b><br/>Remarks and claim amendments - Reply to Office Action date 2-25-2005</p>                                                                                  | Plain Meaning. Specifically, embedded means what it says, embedded within the component that is required in that part of the claim (e.g., embedded in processor, means embedded (i.e., implanted) in the | <p><b>’177 Patent:</b><br/>Figs. 1-3; 2:59-3:21; 3:60-4:5; 4:39-68; 8:45-9:6</p>                                                                                                                                                                      |

|   |                                                                                                                                                                            |                                                                    |                                                                                                                                                                                                                   |                                                                                                                                                                     |                                                                                          |
|---|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------|
|   |                                                                                                                                                                            |                                                                    | Original claims – Application as filed 12-19-2001                                                                                                                                                                 | processor; embedded within FPGA means embedded (i.e., implanted) within the FPGA).                                                                                  |                                                                                          |
| 3 | “two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations”<br><br>(‘177 Patent, Claims 1, 6, 10) | Plain and ordinary meaning                                         | <b>Specification:</b><br>Col. 4 ll. 10-19; Col. 6 l. 65 – Col. 7 l. 35; Col., 7 l. 64 - Col. 8 l. 1;<br><br><b>File History:</b><br>Original claims – Application as filed 12-19-2001                             | two independent internal oscillators coupled to the processor, for providing clock signals, one for the low-frequency and another for the high-frequency operations | <b>‘177 Patent:</b><br>Figs. 1-3; 1:31-43; 3:26-29; 4:39-55; 5:1-14; 6:65-7:30; 7:64-8:4 |
| 4 | power converter<br><br>(‘177 Patent, Claims 5, 9, 10, 13, 15, 17, 20)                                                                                                      | A converter which changes a voltage level to another voltage level | <b>Specification:</b><br>Col. 8 l. 45 – Col. 9 l. 6.<br><br><b>File History:</b><br>Remarks and claim amendments - Reply to Office Action date 2-25-2005<br><br>Original claims – Application as filed 12-19-2001 | Plain Meaning. Specifically, the required power converter converts electrical power.                                                                                | <b>‘177 Patent:</b><br>Figs. 1-3; 1:30-42; 2:59-3:11; 3:34-37; 3:61-4:5; 8:45-9:6        |

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**ECKERT SEAMANS CHERIN & MELLOTT, LLC**

By: /s/ Gary W. Lipkin  
Gary W. Lipkin (#4044)  
Alexandra D. Rogin (#6917)  
222 Delaware Ave, 7<sup>th</sup> Floor  
Wilmington, DE 19801  
Telephone: 302-574-7405  
glipkin@eckertseamans.com  
arogin@eckertseamans.com

Robert W. Morris  
10 Bank Street, Suite 700  
White Plains, NY 10606  
Telephone: 914-286-6440  
rwmorris@eckertseamans.com  
*Attorneys for Plaintiff*

Of Counsel:  
Michael Shanahan  
Scott H. Kaliko  
Kaliko & Associates, LLC  
633 Wyckoff Avenue  
Wyckoff, NJ 07481  
T: 201-739-5555  
skaliko@kalikolaw.com

**FISH & RICHARDSON P.C.**

By: /s/ Thomas L. Halkowski  
Thomas L. Halkowski (#4099)  
Grayson P. Sundermeir (#6517)  
222 Delaware Avenue, 17th Floor  
P.O. Box 1114  
Wilmington, DE 19899  
Telephone: 302-652-5070  
halkowski@fr.com  
sundermeir@fr.com

David M. Hoffman  
111 Congress Avenue, Suite 810  
Austin, TX 78701  
Telephone: (512) 472-5070  
hoffman@fr.com  
*Attorneys for Defendant*