

Petitioner's Oral Hearing Demonstratives

Xilinx, Inc., et al. (Petitioner)
v.
Sentient Sensors, LLC (Patent Owner)

Case No. IPR2023-00195
U.S. Patent No. 6,938,177

Before Hon. Christa P. Zado, Jon M. Jurgovan, and Sheila F. McShane

The '177 Patent

The '177 Patent

(12) **United States Patent**
Blemel

(10) Patent No.: **US 6,938,177 B1**
(45) Date of Patent: **Aug. 30, 2005**

(54) **MULTI-CHIP MODULE SMART CONTROLLER**

(75) Inventor: **Kenneth Blemel**, Albuquerque, NM (US)

(73) Assignee: **Sentient Sensors LLC**, Albuquerque, NM (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 673 days.

(21) Appl. No.: **10/028,556**
(22) Filed: **Dec. 19, 2001**
(51) Int. Cl.⁷ **G06F 13/04; G06F 13/12; H03K 17/693**
(52) U.S. CL. **713/500; 710/69; 716/16**
(58) Field of Search **713/500**

(56) **References Cited**
U.S. PATENT DOCUMENTS
5,892,962 A * 4/1999 Cloutier 712/16

(10) Patent No.: **US 6,938,177 B1**
(45) Date of Patent: **Aug. 30, 2005**

6,148,399 A * 11/2000 Lyke 712/10
2002/0129191 A1 * 9/2002 DaCosta 711/103
* cited by examiner

Primary Examiner—Lynne H. Browne
Assistant Examiner—Stefan Stoyanov
(74) Attorney, Agent, or Firm—Sheppard, Mullin, Richter & Hampton LLP

(57) **ABSTRACT**
A multi-chip module instrument controller having various interface and operational capabilities. The controller incorporate a microprocessor and both volatile and non-volatile memories. The controller includes variable analog-to-digital conversion bit depths, with higher bit depths for some applications. Additionally, the controller includes a separately controllable field programmable gate array that acts as a parallel processor with internal or separate external clock. The FPGA preferably includes more than thirty thousand gates (30,000) and adds a freely re-configurable and separately programmable multi-purpose digital system that can run independent of the microprocessor.

20 Claims, 3 Drawing Sheets

Ex. 1001

(57)

ABSTRACT

A multi-chip module instrument controller having various interface and operational capabilities. The controller incorporate a microprocessor and both volatile and non-volatile memories. The controller includes variable analog-to-digital conversion bit depths, with higher bit depths for some applications. Additionally, the controller includes a separately controllable field programmable gate array that acts as a parallel processor with internal or separate external clock. The FPGA preferably includes more than thirty thousand gates (30,000) and adds a freely re-configurable and separately programmable multi-purpose digital system that can run independent of the microprocessor.

The '177 Patent

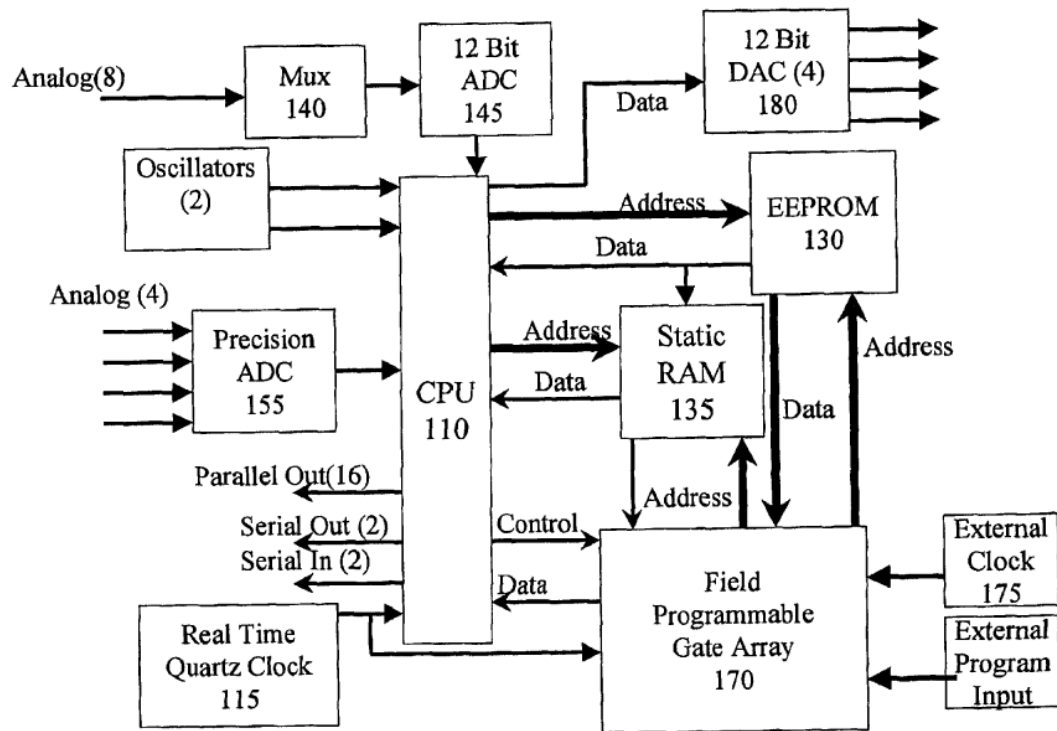


Fig. 1

Summary of Disputed Issues

Only Two Disputed Limitations

1. Ground 1

The “gate array...configured to run independent processes” limitation

- Patent Owner argues for a narrow claim construction, but the prior art provides the element **under any proposed construction** in the case

2. Ground 4

The “power converter” limitation

- Patent Owner seeks a previously rejected claim construction
- But regardless: the prior art provides the element **under either proposed construction** in the case

Outline

1. **Ground 1:** “gate array ... configured to run independent processes”
 - A. Claim construction
 1. literal proposals
 2. control and clocking
 - B. Dehkordi or Lyke provides this element under all proposals
2. **Ground 4:** “power converter”
 - A. Claim construction
 - B. Steele provides this element under both proposals
3. **Additional Issues**
 - A. Patent Owner uses the wrong definition of the POSITA
 - B. Patent Owner wrongly claims Dehkordi was “speculative”
 - C. Patent Owner incorrectly seeks to disregard prior art teachings
 - D. Patent Owner’s expert is entitled to no weight

The Ground 1 Issue

“gate array...configured to run independent processes”

Ground 1: gate array “configured to run independent processes”

Claim Language

1. An instrument controller comprising:
 - a non-volatile memory storage component for program and data storage;
 - a large volatile memory storage component for additional program and data storage;
 - a processor coupled to both the non-volatile memory storage component and the large volatile memory storage components, the processor capable of high-frequency and low-frequency operations and having an embedded memory for storing an initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory;
 - at least two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations;
 - a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and configured to run independent processes in parallel with the processor; and
 - a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing the analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing the digital inputs to the processor;
 - wherein a first portion of the gates in the field programmable gate array is configured to perform signal processing; and
 - wherein a second portion of the gates in the field programmable gate array is configured to operate as a signal distribution matrix for rerouting signals within the instrument controller.

Outline

- 1. Ground 1: “gate array ... configured to run independent processes”**
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Ground 1: gate array “configured to run independent processes”

The prior art invalidates under any proposed construction

- **Lyke** and **Dehkordi** provide a “gate array ... configured to run independent processes” if “independent process” is construed as:
 - Plain and ordinary meaning
 - Patent Owner’s “without computational assistance from another”
 - Patent Owner’s “independent of each other and the processor”
- **Dehkordi** provides the “gate array ... configured to run independent processes” element even if an independent control or clocking requirement is (wrongly) grafted into the claim language

Outline

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Ground 1: gate array “configured to run independent processes”

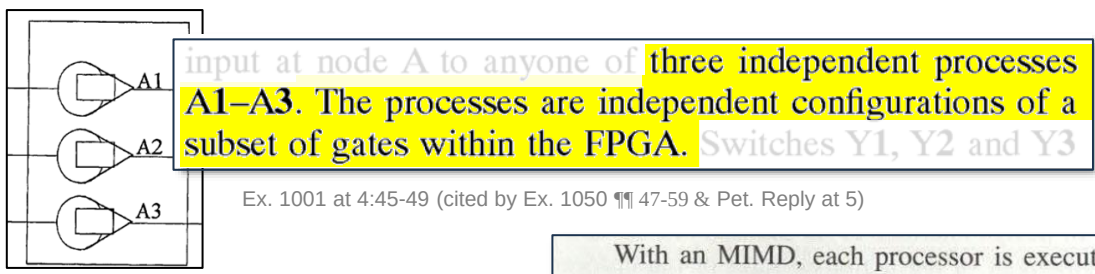
Claim Construction: “process”

	Petitioner Xilinx	Patent Owner Sentient
“process”	Plain and Ordinary Meaning: Includes “a segment of code that may be run independently” and “[a] program or part of a program; a coherent sequence of steps undertaken by a program” Reply, 5-6; Petition, 8	“a computational process programmed into the FPGA gates.’ Excludes initialization and power up sequences.” POR, 26

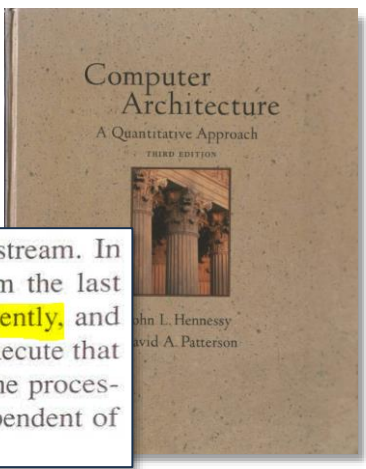
- Petitioner proposes **plain and ordinary meaning**
 - Dr. Shanfield (Petitioner’s expert) provides many examples of a POSITA’s understanding of “process”
- Patent Owner urges an **artificially limited self-referential definition**

Ground 1: gate array “configured to run independent processes”

Intrinsic/extrinsic evidence of plain meaning of “process”



Ex. 1001 at 4:45-49 (cited by Ex. 1050 ¶¶ 47-59 & Pet. Reply at 5)



With an MIMD, each processor is executing its own instruction stream. In many cases, each processor executes a different process. Recall from the last chapter that a process is a segment of code that may be run independently, and that the state of the process contains all the information necessary to execute that program on a processor. In a multiprogrammed environment, where the processors may be running independent tasks, each process is typically independent of the processes on other processors.

Ex. 3004 at 530 (cited by Ex. 1050 ¶¶ 47-59 & Pet. Reply at 5)

United States Patent [19] **5,978,260**
Trimberger et al. [45] **Date of Patent:** Nov. 2, 1999

[54] **METHOD OF TIME MULTIPLEXING A PROGRAMMABLE LOGIC DEVICE**
[57] **Inventors:** Stephen M. Trimberger, San Jose; Richard A. Carberry, Los Gatos; Robert Andrew Johnson, San Jose; Jennifer Wang, Fremont, all of Calif.
[73] **Assignee:** Xilinx, Inc., San Jose, Calif.
[21] **Appl. No.:** 09/119,534
[22] **Filed:** Jul. 20, 1998

Related U.S. Application Data
[63] Continuation of application No. 08/116,008, Aug. 18, 1995, Pat. No. 5,784,312.
[51] **Int. Cl.⁶** G11C 13/00
[52] **U.S. Cl.** 365/182; 365/180.01
[58] **Field of Search** 365/182; 189/01; 365/230.01

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(List continued on next page.)
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23-12137 10/1978 Japan
W094/2675 5/1994 WIPO
W095/2226 2/1995 WIPO
OTHER PUBLICATIONS
"The Programmable Logic Data Book" copyright 1994, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124.
"Principles of CMOS VLSI Design, A Systems Perspective", N. West & K. Eshraghian, Addison-Wesley Publishing Company, 1988, pp. 160-164.

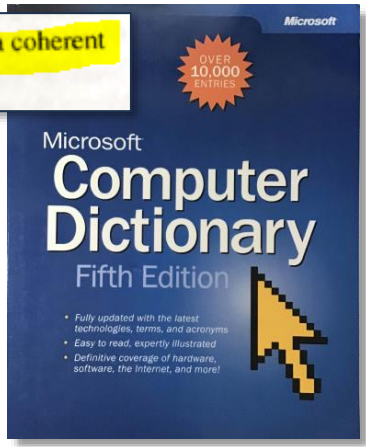
Primary Examiner—Terrell W. Fears
Attorney, Agent, or Firm—E. Eric Hoffman; Bever & Hoffman; Jeanette S. Harms

ABSTRACT
A programmable logic device (PLD) comprises at least one configurable element, and a plurality of programmable logic elements (PLEs). Alternatively, a PLD comprises an interconnect structure and a plurality of programmable logic elements for configuring the interconnect structure. In either embodiment, at least one of the programmable logic elements includes N memory cells. A predetermined one of the N memory cells forms part of a memory slice, wherein at least a portion of each slice of the programmable logic device is allocated to either configuration data or user data memory. Typically, one memory slice provides one configuration of the programmable logic device. In accordance with one embodiment, a memory access port is coupled between at least one of the N memory cells and either one configurable element or the interconnect, thereby facilitating loading of new configuration data into other memory slices during the one configuration. The new configuration data may include off-chip or on-chip data.

Configuration/Read Select (CRS)
Configuration/User Memory Data
200 201 202 203 204 205 206 207 208 209 210 211 212 213 214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255 256 257 258 259 260 261 262 263 264 265 266 267 268 269 270 271 272 273 274 275 276 277 278 279 280 281 282 283 284 285 286 287 288 289 290 291 292 293 294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322 323 324 325 326 327 328 329 330 331 332 333 334 335 336 337 338 339 340 341 342 343 344 345 346 347 348 349 350 351 352 353 354 355 356 357 358 359 360 361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 388 389 390 391 392 393 394 395 396 397 398 399 400 401 402 403 404 405 406 407 408 409 410 411 412 413 414 415 416 417 418 419 420 421 422 423 424 425 426 427 428 429 430 431 432 433 434 435 436 437 438 439 440 441 442 443 444 445 446 447 448 449 450 451 452 453 454 455 456 457 458 459 460 461 462 463 464 465 466 467 468 469 470 471 472 473 474 475 476 477 478 479 480 481 482 483 484 485 486 487 488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503 504 505 506 507 508 509 510 511 512 513 514 515 516 517 518 519 520 521 522 523 524 525 526 527 528 529 530 531 532 533 534 535 536 537 538 539 540 541 542 543 544 545 546 547 548 549 550 551 552 553 554 555 556 557 558 559 560 561 562 563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586 587 588 589 590 591 592 593 594 595 596 597 598 599 600 601 602 603 604 605 606 607 608 609 610 611 612 613 614 615 616 617 618 619 620 621 622 623 624 625 626 627 628 629 630 631 632 633 634 635 636 637 638 639 640 641 642 643 644 645 646 647 648 649 650 651 652 653 654 655 656 657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674 675 676 677 678 679 680 681 682 683 684 685 686 687 688 689 690 691 692 693 694 695 696 697 698 699 700 701 702 703 704 705 706 707 708 709 710 711 712 713 714 715 716 717 718 719 720 721 722 723 724 725 726 727 728 729 730 731 732 733 734 735 736 737 738 739 740 741 742 743 744 745 746 747 748 749 750 751 752 753 754 755 756 757 758 759 760 761 762 763 764 765 766 767 768 769 770 771 772 773 774 775 776 777 778 779 780 781 782 783 784 785 786 787 788 789 790 791 792 793 794 795 796 797 798 799 800 801 802 803 804 805 806 807 808 809 810 811 812 813 814 815 816 817 818 819 820 821 822 823 824 825 826 827 828 829 830 831 832 833 834 835 836 837 838 839 840 841 842 843 844 845 846 847 848 849 850 851 852 853 854 855 856 857 858 859 860 861 862 863 864 865 866 867 868 869 870 871 872 873 874 875 876 877 878 879 880 881 882 883 884 885 886 887 888 889 890 891 892 893 894 895 896 897 898 899 900 901 902 903 904 905 906 907 908 909 910 911 912 913 914 915 916 917 918 919 920 921 922 923 924 925 926 927 928 929 930 931 932 933 934 935 936 937 938 939 940 941 942 943 944 945 946 947 948 949 950 951 952 953 954 955 956 957 958 959 960 961 962 963 964 965 966 967 968 969 970 971 972 973 974 975 976 977 978 979 980 981 982 983 984 985 986 987 988 989 990 991 992 993 994 995 996 997 998 999 1000

Ex. 3002 at 423 (cited by Ex. 1050 ¶¶ 47-59 & Pet. Reply at 5)

process¹ n. A program or part of a program; a coherent sequence of steps undertaken by a program.



have a shared memory. However, if signals from multiple sub-networks feed the same combinational logic, a mechanism is required to allow each “process” to update the output signal of the combinational logic. Creating redundant logic

Ex. 1066 at 37:60-63 (cited by Ex. 1050 ¶¶ 47-59 & Pet. Reply at 5)

Ground 1: gate array “configured to run independent processes”

Claim Construction: “independent processes”

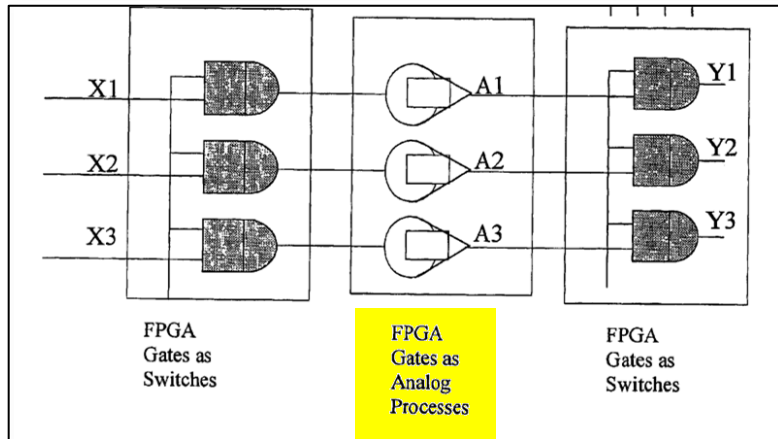
	Petitioner Xilinx	Patent Owner Sentient
“independent processes”	Plain and Ordinary Meaning: “‘independent process’ is ‘a process that runs separately from another process.’ (Independent processes is the plural form.)” Reply, 4, 6-8; Petition 8	“Plain and Ordinary Meaning: ‘without computational assistance from another.’ Independent processes are independent of each other and the processor.” POR, 26

- Petitioner proposes plain and ordinary meaning
 - Dr. Shanfield explains why the intrinsic evidence (prosecution history, specification) supports plain meaning
- Patent Owner urges a “plain meaning” that embeds hidden limitations

Ground 1: gate array “configured to run independent processes”

Intrinsic evidence of plain meaning of “independent process”

- The patent’s affirmative example of independent processes are processes that run separately from each other
 - “independent configurations of a subset of gates within the FPGA”



external inputs in order to perform parallel processes. As shown, gates X1, X2 and X3 are configured to route the input at node A to anyone of three independent processes A1–A3. The processes are independent configurations of a subset of gates within the FPGA. Switches Y1, Y2 and Y3 are configured to selectively route the outputs from these processes to the output node B. When the analog functions represented by A1–A3 are identical, then a form of functional redundancy is achieved, giving an increased fault tolerance to the signal monitoring function. When the analog functions A1–A3 differ, then different analog processing functions are selectively applied to the analog signal being monitored.

Ground 1: gate array “configured to run independent processes”

Extrinsic evidence of “independent” process in FPGA context

for caching. Space-sharing is a way of partitioning the FPGA logic resource so that each function or task obtains as much resource as it needs and executes independently of all others as if it were the sole application executing on a chip just large enough to support it.

Ex. 1058 at 2 (cited by Ex. 1050 ¶¶ 96-104 & Pet. Reply at 13 et seq.)

In multitasking systems, concurrent tasks may need to use the FPGA to perform specific (usually, independent and unrelated) algorithms in hardware so as to achieve the performance required by the corresponding applications. In some cases, an application may benefit from the speed-up granted by the FPGA execution of different independent algorithms at different points of the task itself. In other cases, it is interesting to be able to run a service algorithm in hardware for all tasks

Ex. 1060 at 3 (cited by Ex. 1050 ¶¶ 96-104 & Pet. Reply at 13 et seq.)

parts which are then executed sequentially [2]. Another possibility is to execute several algorithms, that do not require all FPGA resources, in parallel in one FPGA, i.e. true multitasking [3]. Due to the multiple usage of

Ex. 1061 at 301 (cited by Ex. 1050 ¶¶ 96-104 & Pet. Reply at 13 et seq.)

Ground 1: gate array “configured to run independent processes”

In contrast, Patent Owner’s constructions are *ipse dixit*

POR

A. Claim Construction

The proper construction of “process” is “a computational process programmed into the FPGA gates.” Robust specification support for this definition exists in multiple areas including, *e.g.*, at EX. 1001 at 8:16-32; 9:19-35. A primary purpose of the FPGA is to act as a co-processor for various analog or digital functions that compute a result. EX. 1001 4:39-50. Power up sequences do not qualify at least because they do not produce a computational result and such features have no specification support as processes. Similarly, initialization sequences also do not qualify because they also do not produce a computational result, but rather merely prepare the FPGA to perform computations and also have no specification support. EX 2020 ¶¶ 49-51.

The proper construction of “independent processes” is “without computational assistance from another” which is consistent with Patent Owner’s previous litigation definition and the specification. See, for example, EX. 1001 2:9-18; 2:48-55. The plain meaning of “independent processes” are independent of each other and the processor. This is because grammatically speaking “independent” modifies “process” which is its plain meaning, and, as the Board points out - the specification supports both. Institution Decision at 16. EX 2020 ¶52.

PO’s Expert Decl.

50. In my opinion, the proper construction of “process” is “a computational process programmed into the FPGA gates.” This definition is clear from the ‘177 specification and one of ordinary skill in the art would understand that the claimed process must be a computational process to achieve the goals of the invention. Robust specification support for this definition exists in multiple areas including, *e.g.*, at EX. 1001 at 8:16-32; 9:19-35. A primary purpose of the FPGA is to act as a co-processor for various analog or digital functions that compute a result. EX. 1001 4:39-50. Power up sequences do not qualify at least because they do not produce a computational result. Similarly, initialization sequences also do not qualify because they also do not produce a computational result, but rather merely prepare the FPGA to perform computations. . . .

52. In my opinion, the proper construction of “independent processes” is “without computational assistance from another” which is consistent with the specification and Patent’s Owner’s definition in a prior litigation involving the ‘177 patent. See, for example, EX. 1001 2:9-18; 2:48-55; EX. 1012; In my opinion, the plain meaning of “independent processes” are independent of each other and the processor. This is because grammatically speaking “independent” modifies “process” which is its plain meaning, and, as the Board correctly opines - the specification supports both. Institution Decision at 16.

Outline

- 1. Ground 1: “gate array ... configured to run independent processes”**
 - A. Claim construction
 1. literal proposals
 2. control and clocking
 - B. Dehkordi or Lyke provides this element under all proposals
- 2. Ground 4: “power converter”**
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- 3. Additional Issues**
 - A. Patent Owner uses the wrong definition of the POSITA
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Ground 1: gate array “configured to run independent processes”

What about PO’s argument re: “control and clocking”?

DESCRIPTION OF THE PRIOR ART

...

However, there are several limitations to the design in U.S. Pat. No. 6,148,399. First the AIC is not capable of performing parallel independent processes. Although the AIC does include a specialized ASIC, it is controlled and clocked by the microprocessor and cannot run independently of the microprocessor. Accordingly, independent parallel processes are not possible. Accordingly, what is needed is an MCM design capable of executing multiple parallel processes in an independent fashion.

Patent Owner’s argument is not correct. The ’177 patent...

- ...omits Lyke’s FPGA teachings
- ...focuses on Lyke’s “resistive ASIC”
- ...does not claim independent clocking or control
- ...undercuts Patent Owner’s arguments (slides 21-24)

Further, the prior art provides independent clocking and control (slides 28-29)

Ground 1: gate array “configured to run independent processes”

Patent Owner’s argument about “control” is wrong

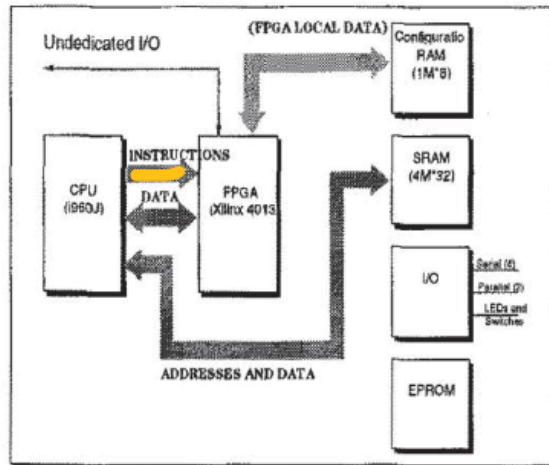


Fig. 2: Functional unit mode

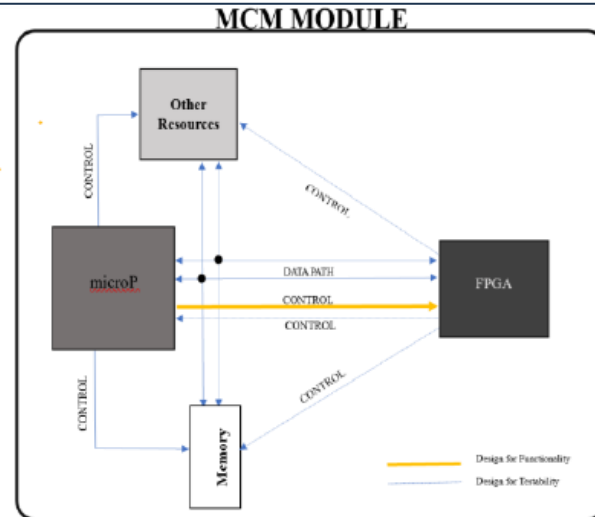


Figure 1: Designing for Testability for a Typical MCM.

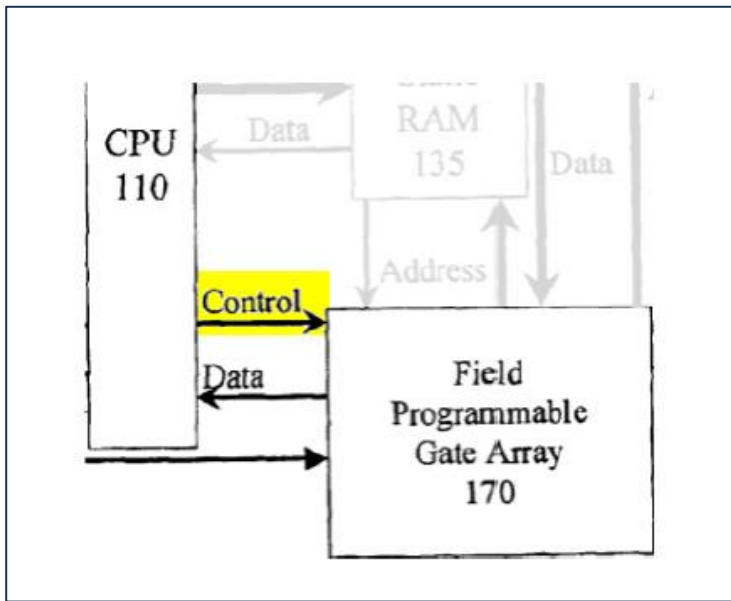
As is clearly apparent from the above, D1-D2 operates under the control of the processor, meaning that its FPGA neither operates independently or in parallel during normal operation. Thus, in light of D2, D1 is not operating independently or

POR at 41-42

Ground 1: gate array “configured to run independent processes”

The '177 patent undermines PO's “control” argument

'177 Patent (Fig. 1 extract)



Ex. 1065 (Sentient's expert)

Q. Figure 1 is an example of the multi-chip module that's claimed in the '177 patent, right?

...

A. Yes, that's correct. This is within the -- the section of detailed description of the preferred embodiments. That's correct.

Ground 1: gate array “configured to run independent processes”

Patent Owner’s argument about “clocking” is wrong

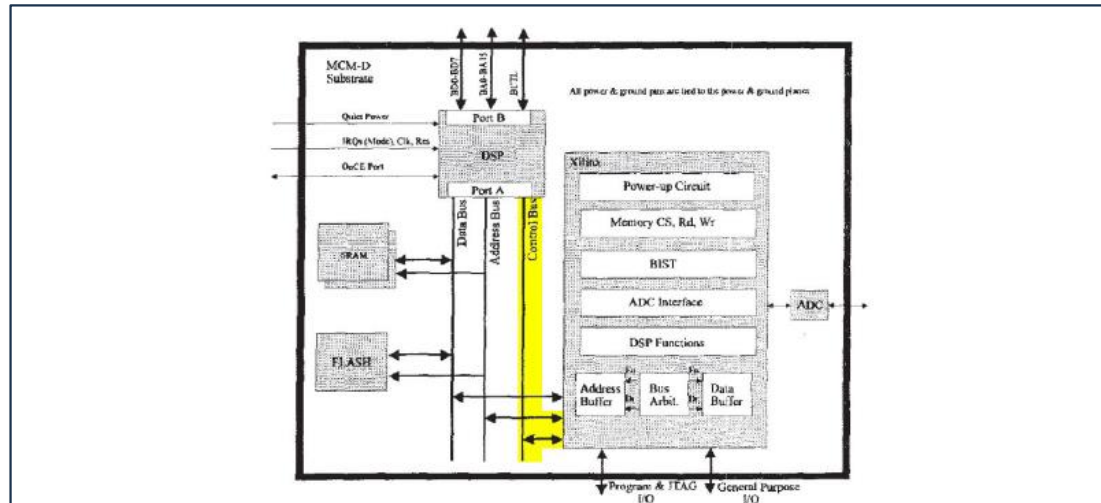
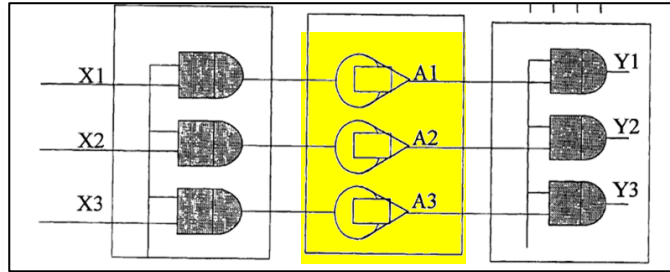


Figure 1. The Block Diagram of the DSP Sub-system.

As shown above, the DSP processor and the FPGA are connected through a control bus (highlighted in yellow) used to control the FPGA, with both components relying on the same clock, and which a POSA would understand were synchronized⁹. As such, the FPGA is dependent on the processor, and they are necessarily in a dependent configuration. Consequently, no independent processes are possible during normal operation and neither the Petition nor D1 suggest otherwise. EX. 2020

Ground 1: gate array “configured to run independent processes”

The ‘177 patent undermines PO’s “clocking” argument



external inputs in order to perform parallel processes. As shown, gates X1, X2 and X3 are configured to route the input at node A to anyone of three independent processes A1–A3. The processes are independent configurations of a subset of gates within the FPGA. Switches Y1, Y2 and Y3 are configured to selectively route the outputs from these processes to the output node B. When the analog functions represented by A1–A3 are identical, then a form of functional redundancy is achieved, giving an increased fault tolerance to the signal monitoring function. When the analog

time. As shown, the FPGA may be clocked using the same on-board VCO as the microprocessor; or it may be clocked separately via an external clock 175. Alternatively, where no clock is used, the FPGA will operate at gate speeds.

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Ground 1: gate array “configured to run independent processes”

Dehkordi is a MCM with processor, FPGA, ADC, volatile/non-volatile memory, etc.

Dehkordi:

Development of a DSP/MCM Subsystem Assessing Low-volume, Low-cost MCM Prototyping for Universities

Peyman Dehkordi, Tim Powell, Donald Bouldin
University of Tennessee¹

Abstract

This paper discusses the design and development of a general-purpose programmable DSP subsystem packaged in a multichip module. The subsystem contains a 32-bit floating-point programmable DSP processor along with 256 K-byte of SRAM, 128 K-byte of FLASH memory, 10 K-gate FPGA and a 6-channel 12-bit ADC. The complete subsystem is interconnected on a 37 mm by 37 mm MCM-D substrate and packaged in a 320-pin ceramic quad flat pack. The design has been submitted to the MIDAS brokerage service to be fabricated by Micro Module Systems. Our experience shows that low-volume MCM prototyping is achievable and somewhat affordable for universities. The design flow, electrical and thermal analyses, CAD tools, cost and lessons learned are discussed in this paper.

Introduction

Multichip module packaging has been in use by IBM and others for high-volume and/or high-cost products for many years but only recently has a low-volume and low-cost service become available to the design community. A variety of other reasons have also impeded growth including the availability of known good die (KGD) and the expense of sophisticated CAD tools optimized for this purpose. Previous work such as [1] discusses various MCM design techniques in depth; however, real-world MCM design problems are not well documented for the first-time users [2]. There has been a tremendous push from Advanced Research Project Agency (ARPA) for wide-spread usage of this technology for the past few years through their Application Specific Electronic Module (ASEM) program. As a result, MIDAS is now offering MCM services for low-cost prototyping [3]. As a part of our ARPA project, we have exercised the availability of this technology for universities. We have performed this exercise by acquiring the appropriate CAD tools and designing a subsystem using bare dies that were procured in small quantities within the required time period. The final design has been submitted to MIDAS for fabrication.

¹ This work was sponsored in part by ARPA under grant DAAH04-94-G-0004

Design Flow

We decided to implement a design representing a typical application of a MCM including a processor, memory and gate-array. It consists of a complete DSP subsystem based on the Motorola 96002 32-bit floating point DSP processor as shown in Figure 1. The module also includes 256 K-byte of SRAM, 128 K-byte of EEPROM, a 10 K-gate Xilinx 4010 FPGA and a 6-channel 12-bit ADC. The module was designed to exploit the multi-processing capability of the 96002. The FPGA is primarily a hardware pre-processor of incoming data but also provides other generic logic functions required for implementation of the entire subsystem.

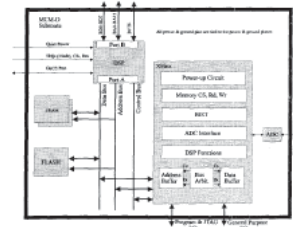
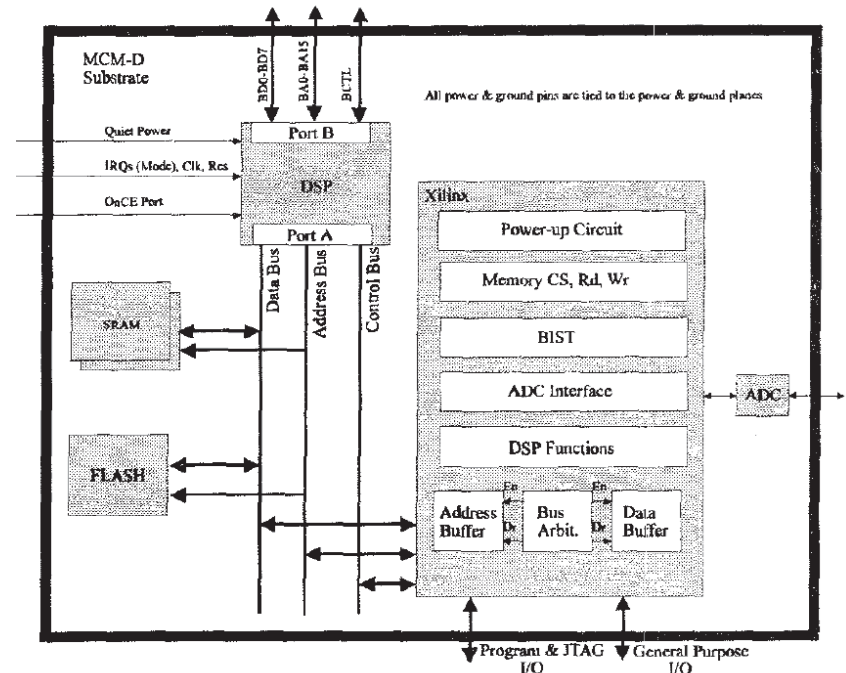


Figure 1. The Block Diagram of the DSP Sub-system.

The design flow is shown in Figure 2 along with the CAD tools used. We had to modify our original plans several times in order to be certain that all of the dies could be acquired within the desired time frame. We found out that it is a good practice to establish a good working relationship with the die supplier to reduce the design cycle as well as die cost and to take advantage of the availability of dies which have already been tested by the supplier. We performed an early analysis on the candidate design to make

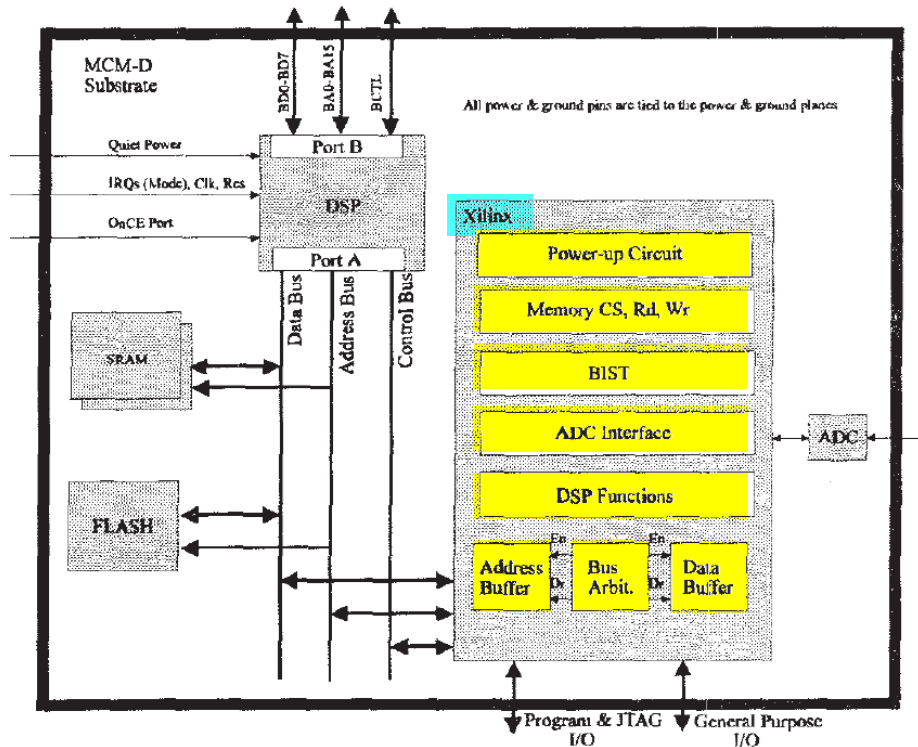


along with the FPGA TAP port for testing purposes. The FPGA has a RAM-based configuration where the configuration may come from outside the module. A portion of the FPGA is configured for multi-processing bus arbitration and is connected to the internal data and address bus on the module. The FPGA can easily be reconfigured to route these lines to the module pins for possible probing and

Ground 1: gate array “configured to run independent processes”

Dehkordi provides either side’s literal constructions

Dehkordi:



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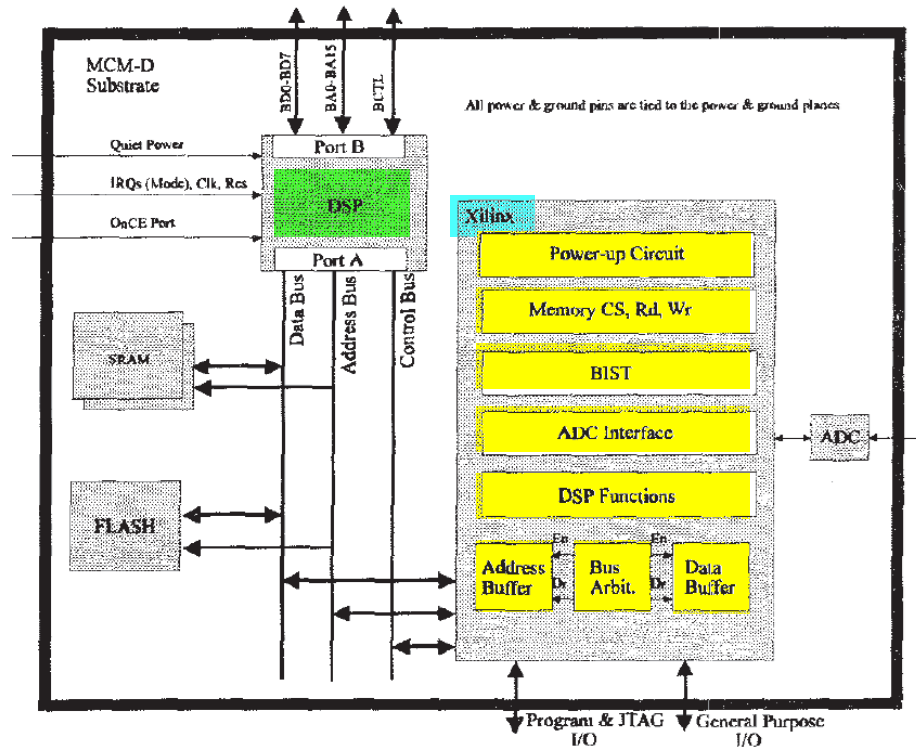
Independent processes as:

- ✓ plain meaning: run separately from other processes
- ✓ “without computational assistance from another”
- ✓ “independent of each other and the processor”

Ground 1: gate array “configured to run independent processes”

Dehkordi also provides independent control

Dehkordi:



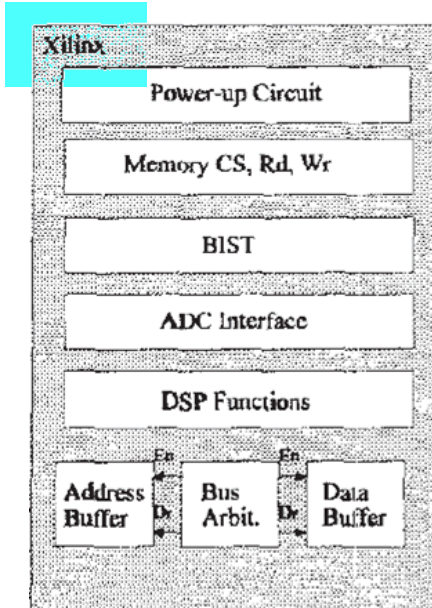
D2
(Ex. 2019 at
171-172):

Careful planning for testability, proper connectivity and configuration of the FPGA not only can allow for an emulated BSP methodology, but can also allow thorough testing of the MCM in its environment. The FPGA can be configured as a pseudo built-in logic analyzer that can monitor core dies within the MCM in real time. This allows testing of not only the hardware aspect, but also allows monitoring of software execution in a limited manner. Moreover, a FPGA

Ground 1: gate array “configured to run independent processes”

Dehkordi also provides independent clocking

Dehkordi:



Xilinx 4010 FPGA

Xilinx 4010 FPGA Manual (Ex. 1014, 23-24):

On-Chip Oscillator

XC4000 Series devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration modes. The oscillator runs at a nominal 8 MHz frequency that varies with process, Vcc, and temperature. The output frequency falls between 4 and 10 MHz.

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8 MHz clock, plus any two of 500 kHz, 16kHz, 490Hz and 15Hz (up to 10% lower for low-voltage devices). These frequencies can vary by as much as -50% or +25%.

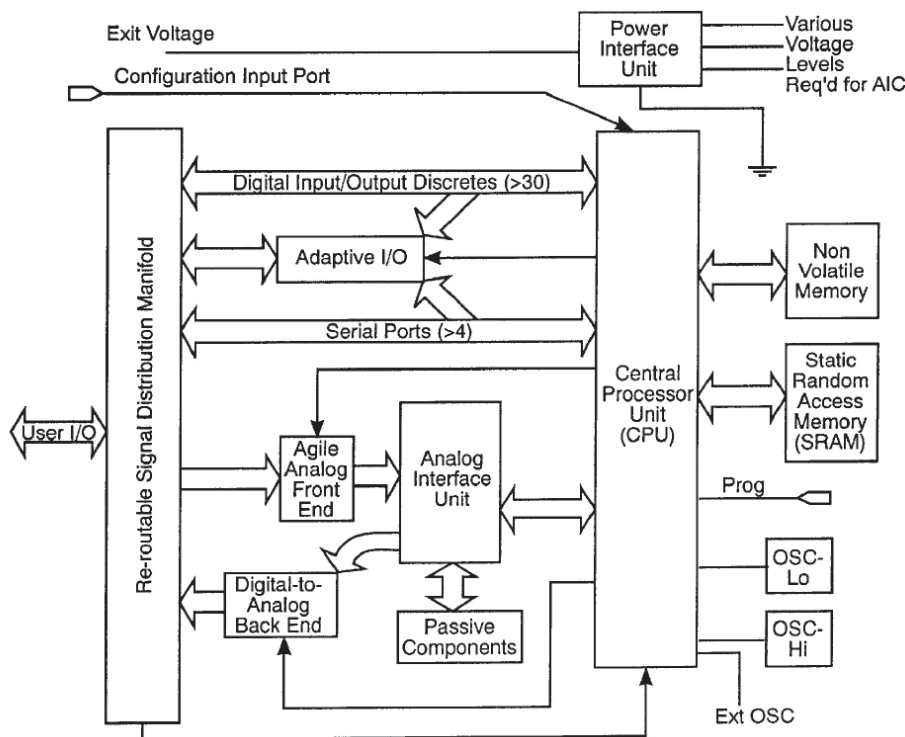
D2 (Ex. 2019, 172):

EEPROM: Since this particular FPGA has an internal system clock, it can stop operations once an error or fault is detected and notify its environment (PCB - LEDs) the probable cause of the error/fault. If the FPGA receives an incorrect address midway through the boot cycle, it can flag

Ground 1: gate array “configured to run independent processes”

Lyke is a MCM instrument controller with processor, FPGA, ADC, volatile/non-volatile memory, etc.

Lyke:



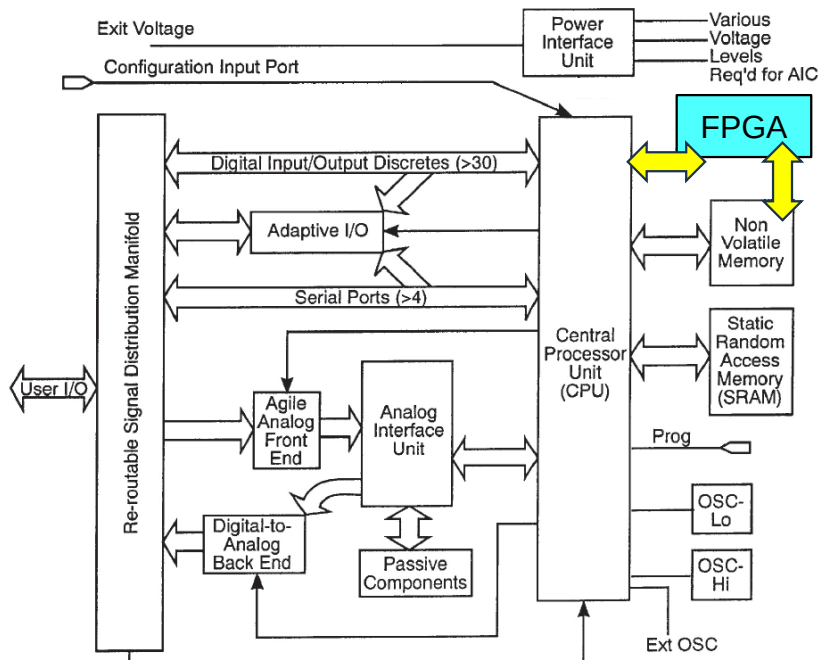
Pat. No. 6,938,177 Docket No.: 42653-0048IP1	
reconfigurable field programmable gate array (FPGA), reconfigurable interconnect devices, analog function blocks, and embedded power conversion." <i>Id.</i> , 2:66-3:5	
29. I note that the '177 patent is very similar to the Lyke prior art reference discussed in more detail below. Sections of the '177 patent are identical or nearly identical to sections of the Lyke reference. Compare EX1001 with EX1003:	
'177 Patent (EX1001)	Lyke Prior Art (EX1003)
"[T]he present invention includes an internal embedded power conversion module which greatly extends robustness of the design, particularly when a number of adjustable internal voltage references are provided. When combined with agile analog control, this capability allows the present invention to not only maintain its internally correct operating power supply under external variation, but this capability permits the present invention to maintain interface integrity." § 46-58.	"The internal embedded power conversion greatly extends AIC robustness, particularly when a number of adjustable internal voltage references are provided. When combined with agile analog, this capability allows the AIC to not only maintain its internally correct operating power supply under external variation, but this capability permits the AIC to maintain interface integrity." 6:10-19.
"The present invention uniquely combines inherent core and I/O feature[s], design methodology, and operating principles to create an electronics building block having numerous monitoring/controlling applications. Along with its increased functionality and unique circuit design, the primary characteristics of the present invention are its compact size, light weight, low power consumption, and compatibility with robust application regimes." 2:59-65.	"The AIC uniquely combines inherent core and I/O features, design methodology, and operating principles to create an electronics building block with numerous monitoring/controlling applications. The AIC's primary characteristics are small size, weight and power, versatile functionality, and compatibility with robust application regimes." 1:66-2:5.
security systems, miniature weapons computers, space probe central control	security systems, miniature weapons computers, space probe central control
last left operation (a simple form of rollback). The non-volatile storage also allows serialization, for specific	serialization, for AIC-specific calibration parameter storage
has more than 20 extremely available discrete signal channels. These channels	has more than 20 extremely available discrete signal channels 2. These are
fast-switching drivers." 7:7-25	"As described earlier, a preferred embodiment of the present invention
	"The internal embedded power conversion greatly extends AIC
	matrix." "the prior art fails to disclose or suggest 'resettable digital real-time quartz

Dr. Shanfield showed the '177 Patent's overlap with Lyke

Ground 1: gate array “configured to run independent processes”

Lyke provides either side’s literal proposals

Lyke:



only and not as a limitation. Other variations to the current design include a surface-mounted program/prototype area for MEMS-based or other sensors and components, including an AIC “personality” module plug-in socket, for extending AIC functionality without altering the AIC’s floor plan size (similar to a co-processor socket). A RAM-based field programmable gate array(s) interfaced internally within the AIC and configured automatically through a downloading mechanism involving AIC’s internal CPU and access of the non-volatile memory might also be included For a system

Ex. 1003 Fig. 1 (modified to add “FPGA” and arrows described in Lyke’s specification, that were omitted in the ’177 patent description of Lyke)

Ground 1: gate array “configured to run independent processes”

POSITA would have read Lyke knowing about FPGAs

Dr. Shanfield:

entirely. For many of the same reasons above, a POSITA would have known that one of the fundamental features of an FPGA was the ability to run separate simultaneous processes. *See, e.g.,* Diessel, EX1058, 2 (describing “partitioning the FPGA ... so that

EX1050, ¶105

for caching. Space-sharing is a way of partitioning the FPGA logic resource so that each function or task obtains as much resource as it needs and executes independently of all others as if it were the sole application executing on a chip just large enough to support it.

In multitasking systems, concurrent tasks may need to use the FPGA to perform specific (usually, independent and unrelated) algorithms in hardware so as to achieve the performance required by the corresponding applications. In some cases, an application may benefit from the speed-up

parts which are then executed sequentially [2]. Another possibility is to execute several algorithms, that do not require all FPGA resources, in parallel in one FPGA, i.e. true multitasking [3]. Due to the multiple usage of

Ground 1: Summary

- The prior art combination (through Dehkordi or Lyke) provide a “gate array ... configured to run independent processes” ...
 - ✓ ... under the plain and ordinary meaning of this term
 - ✓ ... under Patent Owner’s construction that “‘independent processes’ [means] ‘without computational assistance from another.’”
 - ✓ ... under Patent Owner’s construction “‘independent processe’ are independent of each other and the processor.”
 - ✓ ... under Patent Owner’s clocking and/or control arguments.
- The Board should adopt Petitioner’s unchallenged rationale regarding combination of prior art references and the expectation of success in making that combination. Pet., 12-18 (citing EX1002 ¶¶ 50-66).

The Ground 4 Issue

“power converter”

Outline

1. **Ground 1:** “gate array ... configured to run independent processes”
 - A. Claim construction
 1. literal proposals
 2. control and clocking
 - B. Dehkordi or Lyke provides this element under all proposals
2. **Ground 4:** “power converter”
 - A. Claim construction
 - B. Steele provides this element under all proposals
3. **Additional Issues**
 - A. Patent Owner uses the wrong definition of the POSITA
 - B. Patent Owner wrongly claims Dehkordi was “speculative”
 - C. Patent Owner incorrectly seeks to disregard prior art teachings
 - D. Patent Owner’s expert is entitled to no weight

Ground 4: “power converter”

The prior art invalidates under any proposed construction

- The Board correctly already analyzed this element in the POPR; Patent Owner largely repeats its original arguments.
- Patent Owner advocates a claim construction that was rejected by a prior district court judge in an unrelated matter.
- Patent Owner doesn't support its limited construction and there is no lexicographic definition or limitation in the patent.

Ground 4: “power converter”

Claim Language

5. The instrument controller of claim 1, wherein a third portion of the gates in the field programmable gate array is configured to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

Ground 4: “power converter”

Claim Construction: Proposals of Record

	Petitioner Xilinx	Patent Owner Sentient
“power converter”	Plain and Ordinary Meaning: (same as construction issued by a Federal District Court judge from Sentient’s unrelated prior litigation) “plain and ordinary meaning, specifically, a power converter converts power” Reply, 21; Petition, 8	(same as construction rejected by a Federal District Court judge from Sentient’s unrelated prior litigation) “a converter which changes a voltage level to another voltage level.” POR, 26

Steele provides a “power converter”

’177 Claim:

5. The instrument controller of claim 1, wherein a third portion of the gates in the field programmable gate array is configured to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

Steele:

United States Patent Steele	[19]	[11] Patent Number: 5,675,824	
		[45] Date of Patent: Oct. 7, 1997	
[54] PROGRAMMABLE LOGIC HAVING SELECTABLE OUTPUT VOLTAGES	5,223,751	6/1993	Simmons et al. 307/475
	5,260,643	11/1993	Sandhu 323/225
	5,262,705	11/1993	Hattori 318/479
[75] Inventor: Randy C. Steele, Folsom, Calif.	5,297,097	3/1994	Etoh et al. 395/226
	5,304,872	4/1994	Avraham et al. 307/475
[73] Assignee: Intel Corporation, Santa Clara, Calif.	5,325,335	6/1994	Ang et al. 365/205

Yet another object of the present invention is to provide an output signal voltage level which is derived from that signal's input power supply.

Note that even though the PLD, itself, is powered by 5 volts, a user has the ability to choose the voltage level for signals output from the CFBs. This holds true, irregardless

The PLD is powered by a 5.0 supply voltage on the V_{cc} pin. V_{ss} is ground. In addition, in the currently preferred embodiment of the present invention, there is a separate V_{cco} pin associated with each of the CFB's 200–207 (i.e., eight V_{cco} pins).

The V_{cco} pins correspond to the output supply voltage. By coupling the desired output voltage to a V_{cco} pin, a user can select the voltage level of signals being output from a particular CFB. Once a user specifies a V_{cco} voltage for a particular CFB, that whole block outputs signals at the specified voltage level. In this manner, a user can specify a plurality of different voltage levels for output signals. For example, a user could couple the V_{cco} of CFB0 to a supply voltage of 5 volts while simultaneously coupling the V_{cco} of CFB1 to a supply voltage of 3 volts. Hence, output signals from CFB0 are at a 5 volt level, which can be properly utilized by external devices operating on a 5 volt signal reference. Meanwhile, output signals generated by CFB1 are at a 3 volt level. These 3 volt output signals can then be used by those devices operating on signals at a 3 volt reference.

Ground 4: Summary

- The prior art combination (through Steele) provides the “power converter” element ...
 - ✓ ... under the plain and ordinary meaning of this term
 - ✓ ... under Patent Owner’s (previously rejected) construction that a “power converter” is “a converter which changes a voltage level to another voltage level”
- The Board should adopt Petitioner’s unchallenged rationale regarding combination of the prior art references and the expectation of success in making that combination. Pet., 22 (citing EX1002 ¶¶ 115-118).
 - Sentient’s argument that Steele is “superfluous” and “hindsight” is incorrect. Petitioner’s expert showed (with extrinsic evidence) the POSITA would have sought the space/cost savings and reliability advantages. See Petition at 46-47; Pet. Reply at 22-23.

Additional Issues

Outline

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 - A. Claim construction
 1. literal proposals
 2. control and clocking
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 - D. Patent Owner’s expert is entitled to no weight

Additional Issue #1: PO uses the wrong POSITA

But the prior art invalidates under either POSITA

Petitioner Xilinx

A person with a Bachelor's degree in Electrical Engineering or Computer Engineering, or a related field, and ... two years of experience related to the **design or development of multi-chip modules operating as instrument controllers.**"

Pet., 7 (citing Ex. 1002 ¶¶ 24-26); Reply, 1-4 (citing Ex. 1050 ¶¶ 9-19)

Patent Owner Sentient

A person with a Bachelor's degree in Electrical or Computer Engineering or an equivalent degree with at least four years of experience in FPGA and processor systems design including but not limited to **system on a chip 'SoC' and electronic vehicle sensor systems** or related technologies.

POR, 24-25; Ex. 2020 ¶ 22.

Exemplary intrinsic evidence re: POSITA

lers. This is because an **electronics instrument controller** designed in accordance with the invention includes a significant improvement in functionality and circuitry design over **prior art MCM controllers**, such as the AIC in U.S. Pat. No. 6,148,399. For example, the present invention improves

Pet. at 7 (citing Ex. 1002 ¶¶ 24-26); Pet. Reply at 1-4 (citing Ex. 1050 ¶¶ 9-19); POR at 24-25;
EX1001, 1:44-50, 2:34-44; 3:26-30

The invention in U.S. Pat. No. 6,148,399 combines controller and data acquisition functions of conventional test modules into a single, tightly coupled MCM design. Prior to the invention of the AIC, **many MCM design proposals** for space-based test devices had been proposed and/or developed; however, designs approaching the functional capabil-

FIG. 1 is a functional schematic block diagram of a preferred embodiment of the **MCM Controller** of the present invention;

Additional Issue #2: Dehkordi is not “speculative”

Development of a DSP/MCM Subsystem Assessing Low-volume, Low-cost MCM Prototyping for Universities

Cost & Testing Issues

The purpose of this section is to provide the reader with a *rather realistic* cost for this MCM. We have prototyped a total of 5 MCMs which each MCM costing about \$ 2,780.

FPGA and a 6-channel 12-bit ADC. The complete subsystem is interconnected on a 37 mm by 37 mm MCM-D substrate and packaged in a 320-pin ceramic quad flat pack. The

to be fabricated by Micro Module Systems. Our experience shows that low-volume MCM prototyping is achievable and somewhat affordable for universities. The design flow,

PO's expert at deposition:

I think a POSITA would have understood D1 and D2 and -- and how those systems operate, and I've discussed that in my declaration.

Additional Issue #3: Prior art informs the POSITA

Ex. 1025, Halverson:

United States Patent [19] [11] **Patent Number:** **5,574,930**
Halverson, Jr. et al. [45] **Date of Patent:** **Nov. 12, 1996**

[54] **COMPUTER SYSTEM AND METHOD USING FUNCTIONAL MEMORY**

[57] **ABSTRACT**

A computer system has a central processing unit and a

A processor is a functional unit within a computer that interprets and executes instructions. In serial processors, instructions are processed sequentially, one at a time, even when the result or outcome of one instruction is independent of another instruction. In systems with parallel processors, performance is improved by processing unrelated instructions simultaneously within the same interval of time.

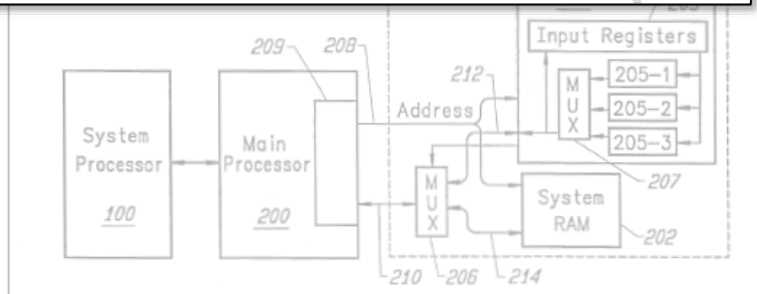
U.S. PATENT DOCUMENTS

4,502,118 2/1985 Hagenson et al. 395700

asserts a second set of memory addresses defined by the configuration data. The functional memory includes access circuitry for routing data signals from the central processing

Traditional parallel data processors execute simultaneously with a main processor instructions that are unrelated, that is, not dependent on the result of the other. Thus,

Although the concept of parallel processing and the use of field programmable gate arrays is not new, the present

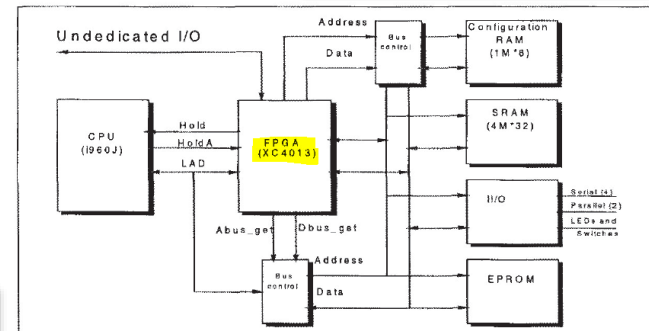


Ex. 1036, Kostranov:

A Reconfigurable Approach to Low Cost Media Processing

Igor Kostanov,

a Xilinx 4013 FPGA



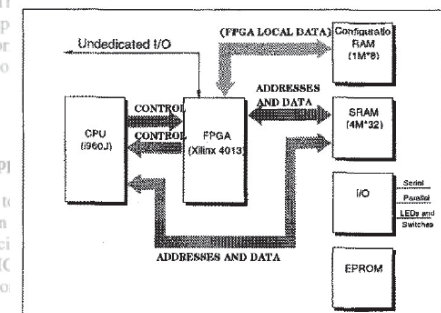
This paper first contrasts existing design approaches with the features of the CPU/FPGA approach. Ti Riley, which was develop accelerating media algor detail and finally some co

2. Background

2.1 Existing Design Ap

The various approaches to processors, augmentation (DSPs), application-speci integrated circuits (ASIC speed, time-to-market, no

2.2 CPU/FPGA Appro



In **datapath mode** the FPGA can arbitrate to become bus master. The CPU and FPGA execute as **two independent execution units** and most of the information that passes between them is control and synchronisation.

Additional Issue #4: PO's expert is entitled to no weight

POPR

subsystem that includes a Motorola 96002 DSP processor and Xilinx 4010 series FPGA shown below:

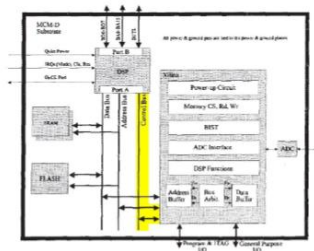


Figure 1. The Block Diagram of the DSP Sub-system.

As described above, the DSP processor and the FPGA are connected through a control bus (highlighted in yellow) used to control the processor, which a POSA would understand includes a common clock signal. As such, the FPGA is dependent on the processor, and they are necessarily in a reciprocal master/slave configuration.

Given that, no independent processes are possible during normal operation and neither the Petition nor *Dehkordi* suggest otherwise.

POR

includes a Motorola 96002 DSP processor and Xilinx 4010 series FPGA shown below. EX. 2020 ¶69.

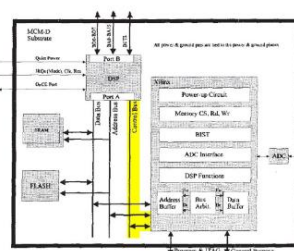


Figure 1. The Block Diagram of the DSP Sub-system.

As shown above, the DSP processor and the FPGA are connected through a control bus (highlighted in yellow) used to control the FPGA, with both components

PO's Expert Declaration

subsystem that includes a Motorola 96002 DSP processor and Xilinx 4010 series FPGA shown below:

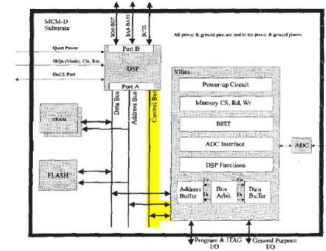


Figure 1. The Block Diagram of the DSP Sub-system.

70. As shown above, the DSP processor and the FPGA are connected through a control bus (highlighted in yellow) used to control the FPGA, with both

components relying on the same clock, and which a POSA would understand were in a dependent configuration. Consequently, no independent processes are possible during normal operation and neither the Petition nor D1 suggest

Q. All right. Let me ask: When were you engaged to start providing expert services in this IPR matter?

A. I believe it was September -- around September of 2023.

Q. And then judging by the date, September 2023, you weren't involved at all in drafting the patent owner preliminary response in this IPR matter, right?

A. That is correct.

Pet. Reply, 27; Ex. 1065 (Peck Depo Tr.) at 11:4-8 & 11:22-12:1