

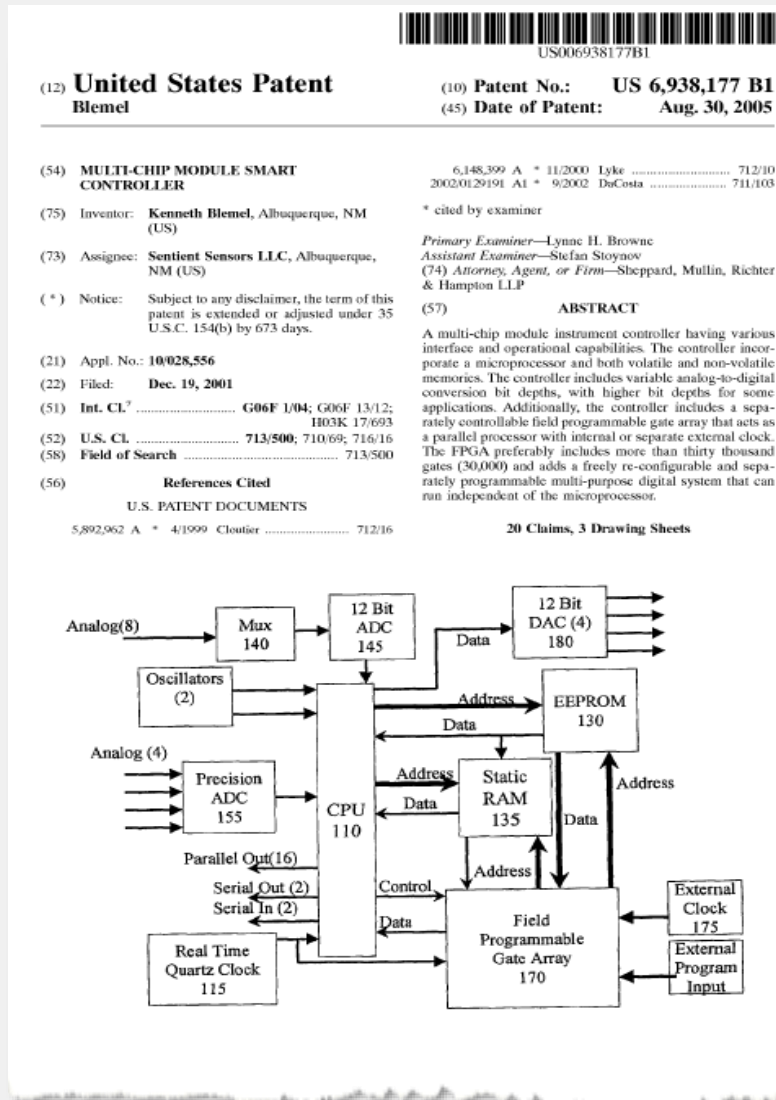
Patent Owner's Presentation

**Xilinx, Inc., *et al.* v.
Sentient Sensors LLC**

IPR2023-00195 (U.S. Pat. 6,938,177)

June 26, 2024

The '177 Patent



- Sole Inventor: Kenneth Blemel
- Developed through the Cooperative Research and Development Agreement entered into with the U.S. Government (EX1001 at 1:6-11)
- The '177 patent protects various products developed, manufactured, and sold by Mr. Blemel's small business in Albuquerque, New Mexico

Xilinx's Grounds

Ground	Basis	Claims	References Used in Challenge
Ground 1	§ 103	1, 4	Lyke, Dehkordi, Frantz, Faura
Ground 2	§ 103	2	<i>Same as Ground 1</i> + Krasner
Ground 3	§ 103	3	<i>Same as Ground 1</i> + Christian
Ground 4	§ 103	5, 10-11, 13-14, 15, 17, 19, 20	<i>Same as Ground 1</i> + Steele
Ground 5	§ 103	12, 18	<i>Same as Ground 4</i> + Christian

(Petition at 1)

Xilinx's Grounds ***do not*** include:

- The general knowledge of a POSA
- Halverson (EX1025)
- Kostranov (EX1036)

Xilinx Cannot Rewrite its Petition

As the Supreme Court has held, “in an inter partes review the petitioner is master of its complaint and normally entitled to judgment on ... the *claims it raises*, not just those the decisionmaker might wish to address.” *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1355 (2018) (emphasis added); see also *Intuitive Surgical, Inc. v. Ethicon LLC*, 25 F.4th 1035, 1041 (Fed. Cir. 2022) (“[A]s the master of its own petition, Intuitive could have made its challenges more pointed and specific....”). This holding is consistent with the statutory framework that requires a petition to identify “the grounds on which the challenge to each claim is based.” 35 U.S.C. § 312(a)(3); see also 37 C.F.R. § 42.104(b) (requiring petitioner to identify “the patents or printed publications relied upon for each ground” and “where each element of the claim is found in the prior art patents or printed publications relied upon”).

Apple Inc. v. MPH Techs. Oy, No. 2021-1355, 2022 WL 4103286, at *7 (Fed. Cir. Sept. 8, 2022)

den of proof. Given that framework, we find no support for the PTO’s position that the Board is free to adopt arguments on behalf of petitioners that could have been, but were not, raised by the petitioner during an IPR. Instead, the Board must base

F.3d 1342, 1360 (Fed. Cir. 2012)). Thus, while the PTO has broad authority to establish procedures for revisiting earlier-granted patents in IPRs, that authority is not so broad that it allows the PTO to raise, address, and decide unpatentability theories never presented by the petitioner and not supported by record evidence.

In re Magnum Oil Tools, Int’l, Ltd., 829 F.3d 1365, 1381 (Fed. Cir. 2016)

Exemplary Limitations of Challenged Claims

“Independent processes in parallel”	“Power Converter”
[1.5] a plurality of gates arranged in a field programmable gate array, <i>the gate array coupled to the processor and configured to run <u>independent processes in parallel</u> with the processor;</i> <i>See also</i> [10.5]	[10.7] wherein a portion of the gates in the field programmable gate array are configured to operate as an internal embedded <i>power converter</i> capable of receiving an input voltage level and generating each operating and reference voltage needed with the instrument controller. <i>See also</i> [13.6], [15.1], [20.1]

Proposed Claim Construction

Element	Patent Owner Proposal	Petitioner Proposal	Intrinsic Support
“process”	“a computational process programmed into the FPGA gates”		EX1001, 4:39-50; 8:16-32; 9:18-35
“independent processes”	“without computational assistance from another”; plain meaning = “independent of each other and the processor” (POR at 28)		EX1001, 2:9-18; 2:48-55
“power converter”	“a converter which changes a voltage level to another voltage level”		EX1001, 8:64-67
“independent process” (singular)		“a process that runs separately from another process”	

Proposed Claim Construction (Intrinsic Evidence)

US006938177B1

(12) **United States Patent**
Bleml

(10) Patent No.: **US 6,938,177 B1**
(45) Date of Patent: **Aug. 30, 2005**

(54) **MULTI-CHIP MODULE SMART CONTROLLER**

(75) Inventor: **Kenneth Bleml**, Albuquerque, NM (US)

(73) Assignee: **Sentient Sensors LLC**, Albuquerque, NM (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 673 days.

(21) Appl. No.: **10/028,556**
(22) Filed: **Dec. 19, 2001**
(51) Int. Cl.⁷: **G06F 1/04; G06F 13/12; H03K 17/693**
(52) U.S. Cl.: **713/500; 710/69; 716/16**
(58) Field of Search: **713/500**

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,892,962 A * 4/1999 Cloutier 712/16

20 Claims, 3 Drawing Sheets

6,148,399 A * 11/2000 Lyke 712/10
2002/0129191 A1 * 9/2002 DoCosta 711/103

* cited by examiner

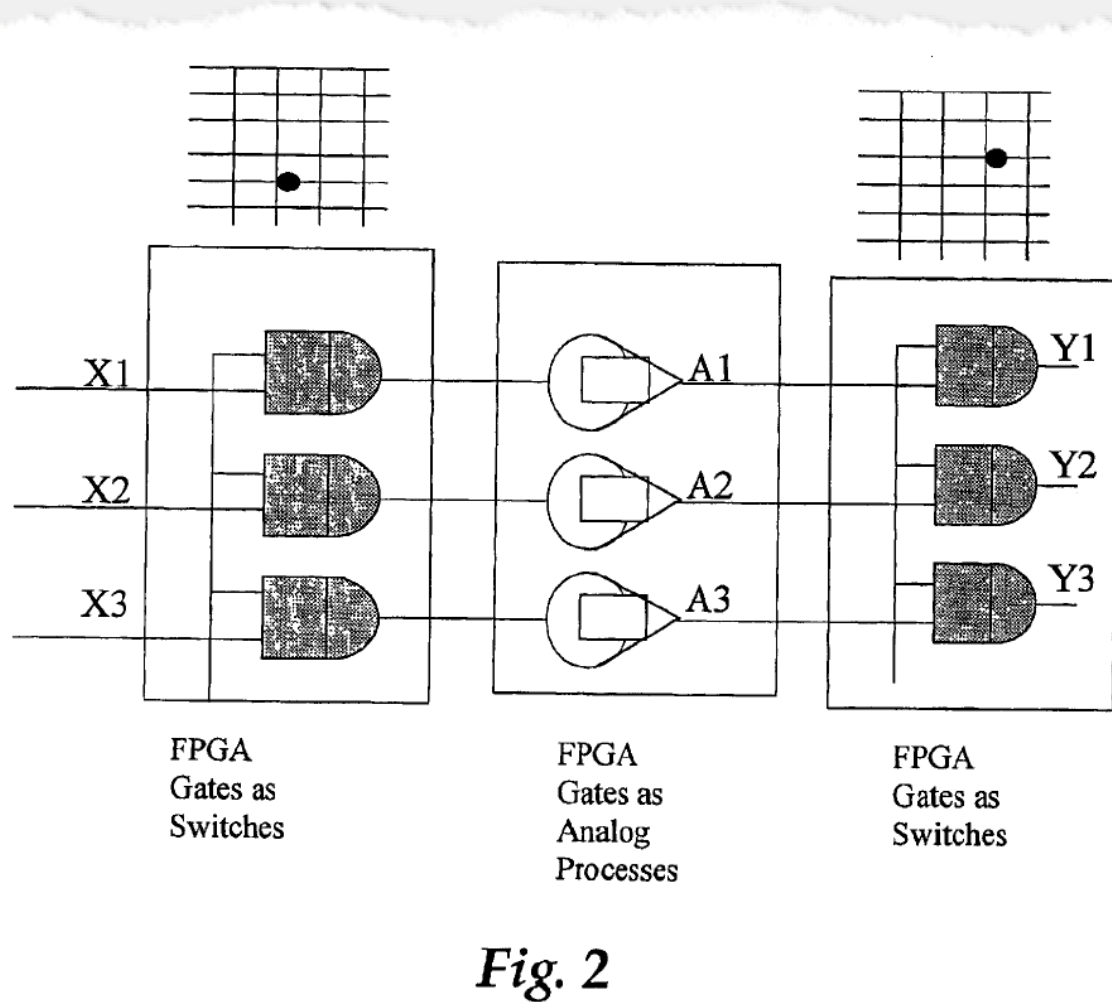
Primary Examiner—Lynne H. Browne
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(57) **ABSTRACT**

A multi-chip module instrument controller having various interface and operational capabilities. The controller incorporate a microprocessor and both volatile and non-volatile memories. The controller includes variable analog-to-digital conversion bit depths, with higher bit depths for some applications. Additionally, the controller includes a separately controllable field programmable gate array that acts as a parallel processor with internal or separate external clock. The FPGA preferably includes more than thirty thousand gates (30,000) and adds a freely re-configurable and separately programmable multi-purpose digital system that can run independent of the microprocessor.

- “... adds a freely re-configurable and separately programmable multi-purpose digital system that can run independent of the microprocessor.” (EX1001, Abstract; see also *id.* at 2:48-55; EX1010 at 43 of 167.)
- The FPGA “may operate either under control of the microprocessor (for example as a co-processor) or, may be operated independently. . . . [T]he FPGA may be clocked using the same on-board VCO as the microprocessor; or it may be clocked separately via an external clock **175**. Alternatively, where no clock is used, the FPGA will operate at gate speeds.” (EX1001, 4:39-50.)
- “As shown [in FIG. 2], gates **X1**, **X2** and **X3** are configured to route the input at node A to anyone [*sic*] of three independent processes **A1-A3**. The processes are independent configurations of a subset of gates within the FPGA.” (EX1001, 2:48-55, FIG. 2.)
- “Preferably, the FPGA can be configured in numerous gate array patterns.” (EX1001, 8:35-36.)
- “The inclusion of the FPGA in the design of the present invention provides a simultaneous parallel processing capability that can be implemented as a mathematical coprocessor and still perform as a digital signal processor (DSP) of multiple analog signals simultaneously digital by the ADC, all the while switching input lines to the ADC.” (EX1001, 9:18-23; see also *id.* at 9:24-35.)

Proposed Claim Construction



EX1001, FIG. 2

Proposed Claim Construction

With this construction, the claim language would read as: “a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and configured to run *[computation processes programmed into the FPGA, which must each be independent—i.e., occur without computational assistance—from another computational process programmed into the FPGA, and from the processor,]* in parallel with the processor.”

See PO Sur-Reply at 3-4

Proposed Claim Construction

Element	Patent Owner Proposal	Petitioner Proposal	Intrinsic Support
“independent process” (singular)		“a process that runs separately from another process”	

Xilinx’s Proposed Construction is unhelpful:

- It was not supported by Xilinx with evidence from the intrinsic record
- Ignores the actual claim language
- Ignores the language of the claim as a whole
- Does not resolve the parties’ dispute

See PO Sur-Reply at 6-7

The Shortcomings of Lyke (EX1004)

However, there are several limitations to the design in
10 U.S. Pat. No. 6,148,399. First the AIC is not capable of
performing parallel independent processes. Although the
AIC does include a specialized ASIC, it is controlled and
clocked by the microprocessor and cannot run independently
of the microprocessor. Accordingly, independent parallel
15 processes are not possible. Accordingly, what is needed is an
MCM design capable of executing multiple parallel pro-
cesses in an independent fashion.

EX1001, 2:9-17

ensure accuracy. The AIC of U.S. Pat. No. 6,148,399 uses a
constant bit depth of 10 bits for its A/D conversion so all
processes are executed at the same bit depth. Accordingly,
what is needed is an MCM design capable of performing
A/D conversion at different bit depths such that multiple
parallel processes which require different bit depths can be
executed in an independent fashion.

EX1001, 2:24-30

The Shortcomings of Lyke (EX1004)

Consistent with Patent Owner's Arguments during Prosecution

The instrument controller of the present invention offers enhanced power management and functional flexibility, more specifically, the instrument controller offers variable analog-to-digital conversion bit depths, along with higher bit depths for some applications. Also, the present invention eliminates the need for a resistive ASIC. Instead, the present invention adds a separately controllable FPGA that acts as a parallel processor with an internal clock or separate external clock. The FPGA preferably includes more than thirty thousand gates and adds a freely reconfigurable, and separately programmable, multi-purpose digital system that can run independent of the microprocessor. Also, the present invention incorporates a microprocessor with a processing speed of up to 33 MHz.

See PO Sur-Reply at 6 (citing EX1010 at 43 of 167); see also POR at 4, 8-10, 30-37

Dehkordi 1 (EX1004)

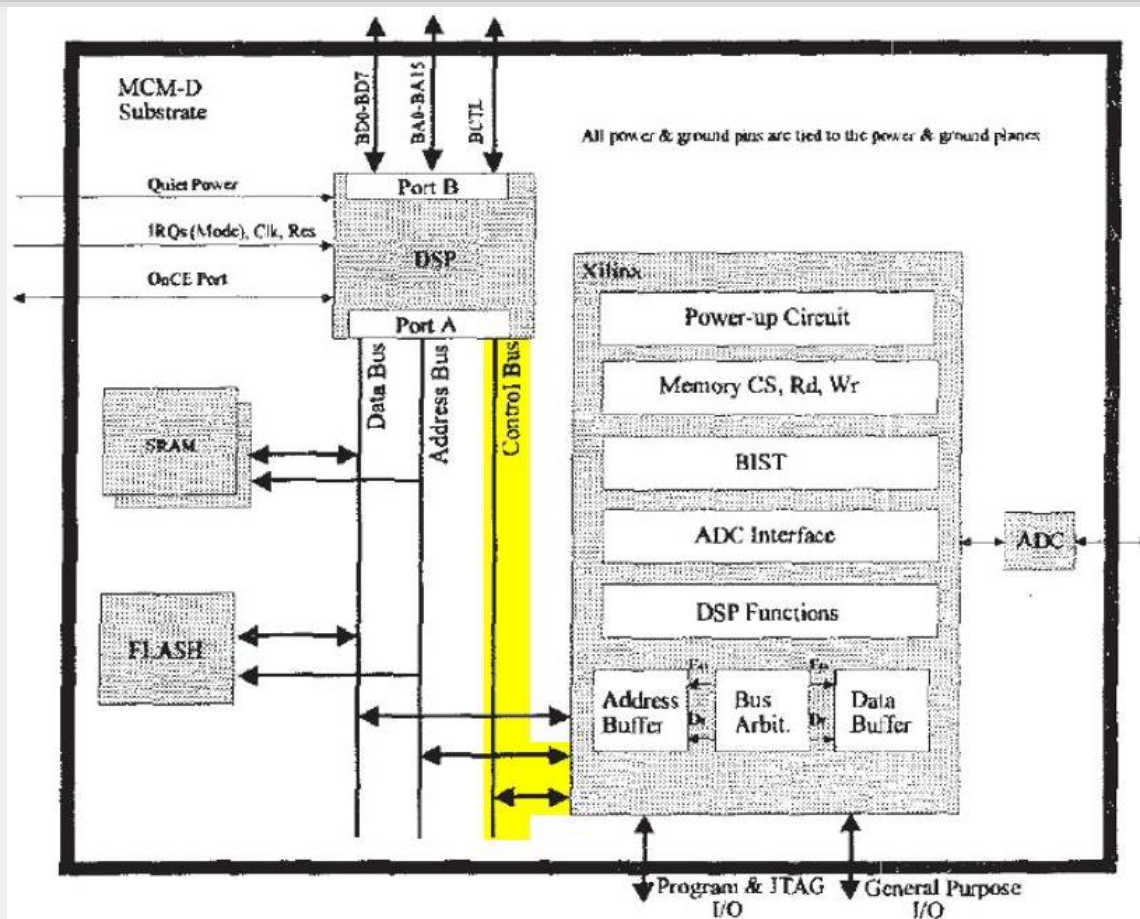
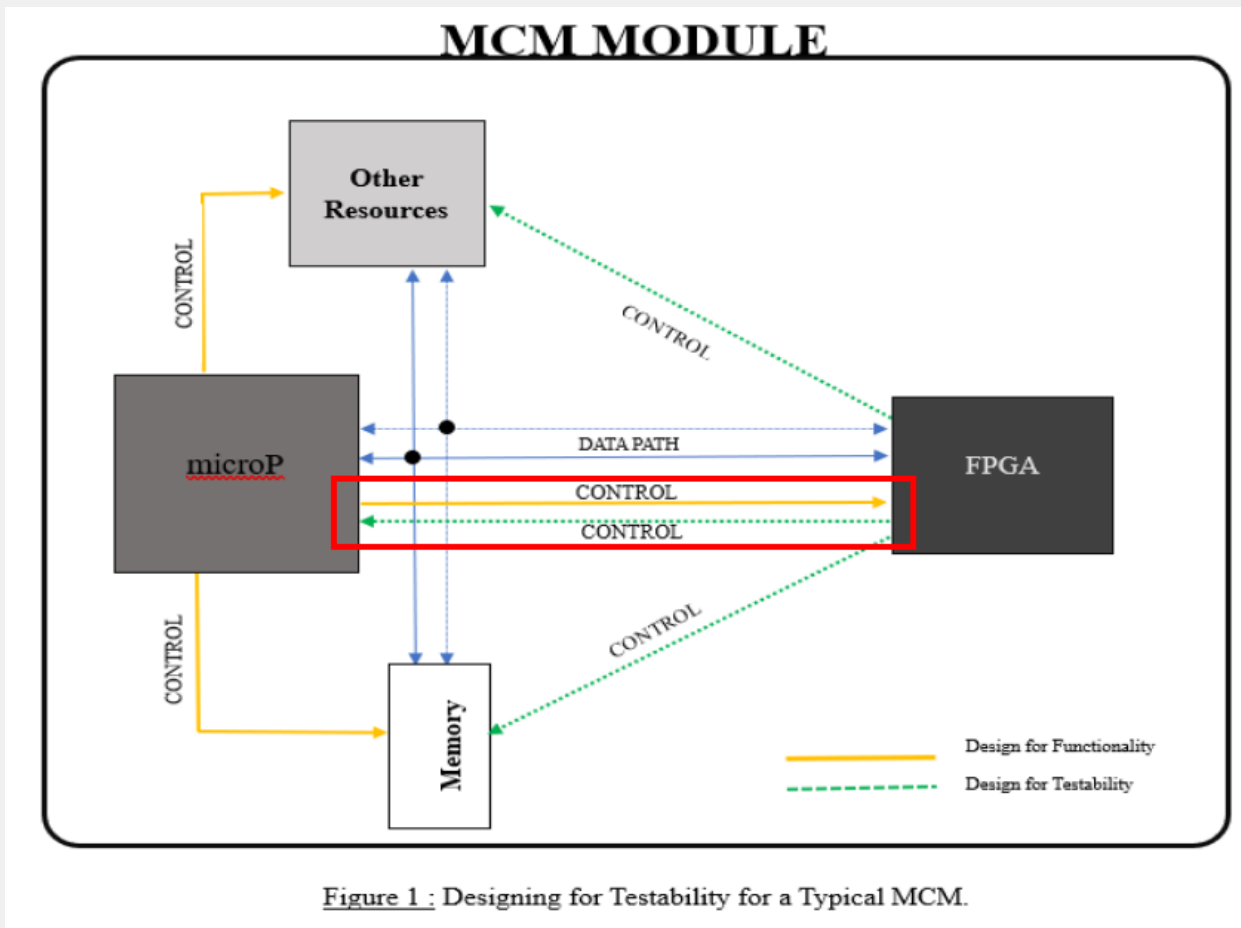


Figure 1. The Block Diagram of the DSP Sub-system.

See POPR at 11 (citing EX1004, Fig. 1 (annotated)); see also POR at 14-18, 37-52; PO Sur-Reply at 9-15)

Dehkordi 2 (EX2019)



See POR at 17 (citing EX2019, Fig. 1 (annotated); see *also* POR at 14-18, 37-52; PO Sur-Reply at 9-15)

Steele (EX1009)

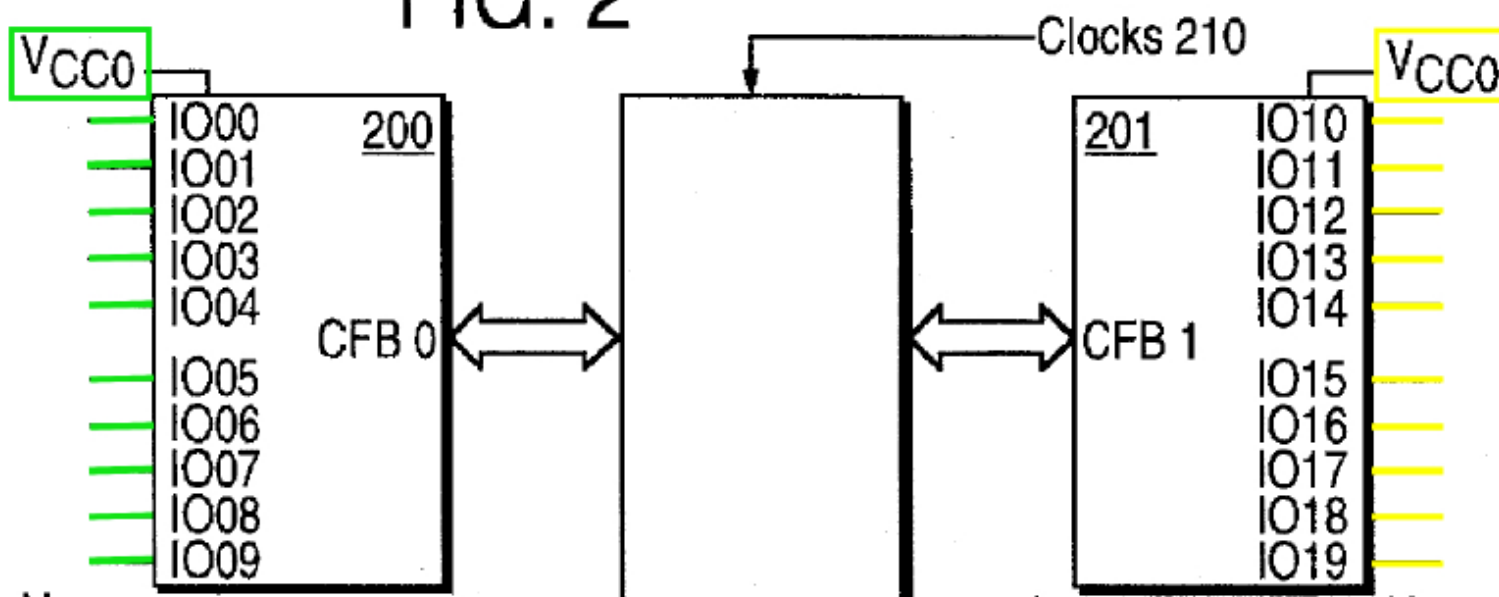
U.S. Patent

Oct. 7, 1997

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5,675,824

FIG. 2



See POR at 17 (citing EX2019, Fig. 1 (annotated)); see also POR at 52-56; PO Sur-Reply at 15-17)

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