

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC., ADVANCED MICRODEVICES, INC., AND ATI
TECHNOLOGIES ULC.,

Petitioner,

v.

SENTIENT SENSORS LLC,

Patent Owner.

Case IPR2023-00195

Patent 6,938,177 B1

Record Of Oral Hearing

Held: June 26, 2024

Before JON M. JURGOVAN, CHRISTA P. ZADO, and
SHEILA F. McSHANE, *Administrative Patent Judges*.

APPEARANCES:

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The above-entitled matter came on for hearing Monday, June 26, 2024,
commencing at 1:00 p.m. EDT, via videoconference.

P-R-O-C-E-E-D-I-N-G-S

(1:00 p.m.)

JUDGE ZADO: All right. Hi. Good morning or good afternoon, depending on which time zone you're in. This is the oral hearing in IPR 2023-00195 between Petitioners Xilinx, Incorporated; Advanced Microdevices, Incorporated; and ATI Technologies, Incorporated, and Patent Owner Sentient Sensors, LLC, involving challenged claims of U.S. Patent No. 6,938,177. I'm Judge Zado, and joining me are Judges Jurgovan and McShane.

For clarity of the transcript and for the benefit of the judges, we ask that you please identify yourself each time before you begin speaking and also that you identify any exhibits or demonstratives including by page number or slide number and/or exhibit number that you are using or referring to. And we also ask that when you are not speaking, that you please mute yourself.

And given that this is a virtual hearing, we ask that if you experience any technical difficulties during the hearing, including difficulties that impact your ability to hear what is being said, please go ahead and just speak up, even if it's not your time to argue, and let the Panel know immediately.

So, today, the parties have requested, and each party will have 45 minutes of total argument time. Petitioner will go first and present its case with regard to the instituted claims. Petitioner may reserve time for rebuttal. Thereafter, Patent Owner will argue its opposition to Petitioner's case. And if there is rebuttal from Petitioner, we will hear that after Patent Owner's argument. And Patent Owner also may reserve time for surrebuttal.

So, with these preliminaries being said, let's go ahead now and get the parties' appearances, and we'll begin with Petitioner.

1 Who is appearing on Petitioner's behalf?

2 MR. SHNEIDMAN: Thank you, Your Honor. I am
3 Jeffery Shneidman with Fish & Richardson, on behalf of Petitioner Xilinx.
4 I'm joined virtually by my colleagues David Hoffman and Craig Deutsch.

5 JUDGE ZADO: All right. And would Petitioner like to reserve time
6 for rebuttal today?

7 MR. SHNEIDMAN: Yes, Your Honor. I'd like to reserve ten
8 minutes today for rebuttal.

9 JUDGE ZADO: All right. And who is appearing on Patent Owner's
10 behalf today?

11 MR. COCHRAN: Good afternoon, Your Honor. My name is
12 Andrew Cochran of Cahill Gordon & Reindel, on behalf of Sentient Sensors.
13 I have with me in the room Gerald Flattmann, also with Cahill, and with us
14 remotely is John Stellabotte of Ellenoff Grossman & Schole.

15 JUDGE ZADO: And would Patent Owner like to reserve time for
16 surrebuttal?

17 MR. COCHRAN: Yes. Ten minutes would be fine.

18 JUDGE ZADO: So, before we begin, are there any questions or
19 issues the parties would like to raise? I'll start by directing this question to
20 Petitioner.

21 MR. SHNEIDMAN: No, Your Honor.

22 JUDGE ZADO: Same question for Patent Owner.

23 MR. COCHRAN: No, Your Honor.

24 JUDGE ZADO: Okay. We'll begin in a moment, but before we
25 begin, I just would like to note that when the hearing is over, we ask the
26 parties remain on the line with the court reporter to answer any questions or
27 provide clarifications on names and spellings and the like with the reporter.

1 So, with that, I'm going to get my timer ready, and then we can go
2 ahead and begin. So just bear with me for a moment, please.

3 All right. Petitioner, whenever you are ready, please begin.

4 PETITIONER ARGUMENT

5 MR. SHNEIDMAN: Thank you, Your Honor. So, again, my name is
6 Jeffery Shneidman with Fish & Richardson, on behalf of Petitioner Xilinx.
7 My plan for this opening discussion is to cover a subset of the slides and the
8 demonstratives unless the Board has specific questions about a particular
9 area.

10 That said, I'd welcome the opportunity to jump right into anything
11 Your Honors wish to discuss, but unless the Board wants to do so at the
12 outset, I'll set the stage for what I think is at issue in this dispute by moving
13 to slide 4 of the slide deck.

14 On slide 4, we see the '177 patent, Figure 1. It's shown here. It's a
15 combination of off-the-shelf parts put together in a known and expected
16 way. Much of the '177 patent is lifted verbatim directly from the references
17 we explained in our petition.

18 And the '177 patent is not a novel combination of items. And the
19 Patent Owner doesn't dispute that most of the claim elements are found in
20 the prior art. It may help to set the context of what the '177 says it
21 purportedly added over Lyke, column 2, at lines 9 through 31.

22 And specifically, in column 2, the '177 patent specification claims to
23 disclose an improved variable conversion A to D converter and that's been
24 validated by the prior art, including the Lyke and the Faura references, and
25 the Patent Owner doesn't challenge that fact or that ground, so I'm not
26 focusing on that today.

1 The second item is the addition of an FPGA to replace Lyke's ASICs.
2 But the combination of the FPGA, which is described in the '177 patent as a
3 novel feature, was not novel and was even disclosed in Lyke and other
4 contemporaneous references, such as Dehkordi, in the manner that I'm going
5 to discuss today.

6 So, if I move to slide 6, I'm going to talk about the two disputed issues
7 in this case. And there are no other art-related challenges. In particular,
8 there's no challenge to the motivation by the POSITA to combine the prior
9 art or the POSITA's reasonable expectation of success in making that prior
10 art combination.

11 JUDGE ZADO: Counselor, I'm going to ask you pause right there
12 because this does touch upon an area where I did have a few questions, now
13 that we're talking about the person of ordinary skill in the art.

14 Petitioner has proposed in the petition one level, and Patent Owner
15 proposes a different level. And my question is, does which level we adopt
16 change how we should decide this case?

17 MR. SHNEIDMAN: We believe no, Your Honor.

18 JUDGE ZADO: And -- I'm sorry. Were you going to continue?

19 MR. SHNEIDMAN: I was just going to say it's true that in the
20 Institution Decision, the Board invited the parties, if they disagreed, to
21 explain why they thought the person of ordinary skill difference would
22 matter. I did see the Patent Owner did present a different version of it, but
23 we don't believe it makes a material difference to patentability. We don't
24 believe it's a correct statement of the person of ordinary skill in the art, and
25 we address that in the Petitioner Reply. But I don't think it makes a
26 difference in terms of the patentability.

1 JUDGE ZADO: And along those lines, just to be sure that the Panel
2 hasn't missed anything, were there any arguments in any of Petitioner's
3 papers specifically indicating that if we adopted, say, Patent Owner's level of
4 ordinary skill in the art instead of Petitioner's, you know, how that would
5 have impacted the analysis?

6 MR. SHNEIDMAN: So the Petitioner's expert confirms that his
7 opinions are the same as to what the person of ordinary skill in the art would
8 have understood under either definition of the person of ordinary skill in the
9 art. And he does that in Exhibit 1050. I don't have it --

10 (Simultaneous speaking.)

11 JUDGE ZADO: All right. Thank you.

12 MR. SHNEIDMAN: So the claims in the '177 patent are quite broad.
13 And we showed in the petition why the applicant was not entitled to claims
14 so broadly over the prior art. As we spelled out in the petition, what the
15 applicant ended up obtaining was obvious in multiple ways.

16 And so, in this trial, the Patent Owner is focusing only on two
17 claim elements and arguing from narrowing claim construction. And I guess
18 this is an attempt to avoid the prior art and to try to amend the claims
19 through claim construction, which of course is not proper. But even under
20 those narrowed interpretations of the claim language, we showed in our
21 papers why, under every claim construction at issue presented in this case,
22 the prior art still provides each disputed element.

23 So, if I move to slide 9, first, I'm going to talk about Patent Owner's
24 challenge to Ground 1, which relates to what the element that the parties call
25 Element 1.5. We've listed here the exemplary claim language from Claim 1.
26 The Patent Owner does not contest that everything in this claim is taught in

1 the prior art except for the element of the gate array configured to run
2 independent processes in parallel with a processor.

3 And I've highlighted here, on slide 9, the portion of the element that
4 the parties have focused their briefing on, which is this gate array configured
5 to run independent processes.

6 So let's talk about this claim construction issue first and move to slide
7 11. On slide 11, the main point I'll start with, of course, is that the prior art
8 in the petition invalidates under any of the proposed constructions, either
9 literally as presented by the parties, or in the hidden, sort of embedded
10 limitations that we thought were found in the Patent Owner's arguments.

11 I say it that way because we'll see in a minute, the Patent Owner now
12 seems to be disclaiming, in the Patent Owner's Sur-reply, the arguments that
13 it made in the Patent Owner Response about the control and the clocking.
14 But those interpretations of independent are also taught in the asserted prior
15 art.

16 Now, I'll come back to this issue in just a moment, but for now, let me
17 stick to the arguments that were literally presented by the parties in the
18 papers and turn to slide 13. So slide 13 shows what each side proposed as
19 the meaning of the term process which is a component of the independent
20 (audio interference).

21 There is no lexicography or disclaimer in the file history. There's no
22 reason to redefine a process to be anything other than the plain meaning to
23 the POSITA. The Petitioner has advocated for a plain and ordinary
24 meaning. Whereas, if you look at the Patent Owner Response at page 26,
25 the Patent Owner is advocating for something narrower.

26 And on the right-hand side of this slide 13, you see the word process
27 there in black, but it's swimming in this sea of red limitations. And there's

1 really no reason to add these extra words. There's nothing in the record to
2 support the Patent Owner's limited reading that appears here on slide 13.

3 The evidence doesn't support the narrow exclusionary reading, and if
4 you move to slide 14, I'll explain what I mean by that. Slide 14 shows some
5 of the intrinsic and the extrinsic evidence that Petitioner's expert,
6 Dr. Shanfield, relied on in describing how the POSITA would understand
7 the process.

8 And notably, only the Petitioner put in supported evidence on this
9 point. Despite this, several of the items being called out in the Institution
10 Decision, Patent Owner was certainly on notice. The Patent Owner and their
11 expert doesn't cite to a single piece of extrinsic evidence to explain the
12 POSITA's view, the expert's view as to what the POSITA would have
13 understood a process, or an independent process would mean.

14 The Patent Owner chose not to depose Dr. Shanfield in this case. So,
15 while Dr. Shanfield explained at length, over two declarations, his opinions
16 with the declaration with the petition and with the Petitioner Reply, the
17 Patent Owner chose not to cross-examine Dr. Shanfield or attempt to rebut
18 that testimony. And so, as a result, the Patent Owner simply does not
19 address most of the exhibits and evidence in this case. And the expert is
20 silent. The Patent Owner's expert is silent (audio interference).

21 So, looking still at slide 14, here we have the '177 patent itself talking
22 about processes in the upper left in terms of subsets of gates within the
23 FPGA, that is the programming or the code that's being configured onto the
24 FPGA.

25 And we see the then classic and contemporaneous textbook, Patterson
26 and Hennessy, describing process as a segment of code that may be run
27 independently.

1 We see the then contemporaneous dictionary describing process as a
2 program or part of a program, coherent series of steps.

3 And we see another example of extrinsic evidence in the FPGA
4 context, patent by Steve Trimberger, a distinguished engineer at Xilinx, that
5 describes collections of combinatorial logic as a process. There is no
6 evidence supporting a departure from a plain meaning and the evidence
7 supported -- excuse me -- that's cited by the Petitioner is --

8 JUDGE ZADO: Excuse me. I'm sorry to interrupt. This is
9 Judge Zado.

10 I'm hearing some background noise, and it looks like the conference
11 room where Andrew Cochran is, is not on mute. If that's correct, could you
12 please mute your room? Thank you.

13 Go ahead.

14 MR. SHNEIDMAN: So, anyway, the point being is that the evidence
15 here that the Petitioner presents is unrebutted and well-supported.

16 If I move to slide 15, in the Institution Decision, at page 14, the
17 Board, quote, encouraged the parties to provide their interpretations of the
18 term independent process.

19 You know, and both sides responded, trying -- or saying that they
20 were using the plain and ordinary meaning, which Petitioner proposed to be,
21 quote, an independent process is a process that runs separately from another
22 process. Independent processes is the plural form.

23 And again, not to beat the dead horse here, the Board reminded the
24 parties to identify specific evidence in the intrinsic record and to support
25 with extrinsic evidence and these statements as to what the POSITA would
26 have understood this term. And only the Petitioner's expert in this case did
27 so.

1 And if you look at the intrinsic and extrinsic evidence next, it will
2 show you I think the highlights. So, on slide 16, we have really the strongest
3 statement in the '177 patent. It's really the only affirmative example of an
4 independent process, which independent processes, there, are described as
5 processes that run, in our view, separately from each other. Or in the
6 patent's words, it's independent configurations of a subset of gates within the
7 FPGA.

8 And as Dr. Shanfield explained, the way that an FPGA commonly
9 works is that separate sections of the FPGA are literally divided up to run
10 different independent processes. And that's what's being described here in
11 Figure 2 of the '177 patent. A subset of gates is running process A1. A
12 second subset of gates, literally separate real estate on the chip, is running
13 process A2. And a third subset of gates is running process A3.

14 And so it's Dr. Shanfield's view of what the POSITA's understanding
15 of independent processes would've been at the time of the '177 patent is not
16 only supported by this sort of intrinsic evidence but also the extrinsic
17 evidence as well if we turn to slide 17.

18 Slide 17 shows some of the extrinsic evidence identified and cited by
19 Dr. Shanfield. And I'll just read the first one for example, which describes
20 partitioning the FPGA logic resource so that each function or task executes
21 independently of all others, as if it were the sole application executing on the
22 chip.

23 And that's what we see going on in the '177 patent Figure 2 as well,
24 with processes A1, A2, and A3. And so, Dr. Shanfield is describing his
25 plain and ordinary meaning of an independent process extensively with
26 pieces of both intrinsic and extrinsic evidence in support.

1 And this contrasts to what we see on slide 18 where we see the Patent
2 Owner's arguments on the plain and ordinary meaning are really
3 unsupported ipse dixit. The Patent Owner literally provided one paragraph
4 on the construction of independent process, and it's the same text found in
5 the Patent Owner expert declaration, albeit with the words in my opinion
6 added.

7 And I don't mean to be beating a dead horse, but this really comes
8 down to how a person of ordinary skill in the art would have understood
9 these terms. And so, that's why this matters. So --

10 JUDGE JURGOVAN: Counsel, can I interrupt for a second? I think
11 the dispute is really not really so much focused on process and what an
12 independent process is, but what that means in the context of this claim.

13 So it says the gate array coupled to the processor and configured to
14 run independent processes in parallel with the processor. So does that -- that
15 means that, at least within the gate array, the processes that are running there
16 are independent from one another; do you agree with that?

17 MR. SHNEIDMAN: I think so. I think that's what we're seeing in
18 Figure 2 there of the patent in column 8.

19 JUDGE JURGOVAN: Okay. What about -- does that language there
20 mean that the processes that are running in the FPGA are independent of
21 what the processor is doing, the processor's operation?

22 MR. SHNEIDMAN: I don't think it's an "and," necessarily. I think
23 the broadest reading here that's reasonable is an "or." But it doesn't matter at
24 the end of the day because we showed both. The petition sort of started out
25 assuming, well, it's -- we can show, you know, by point the --

26 JUDGE JURGOVAN: I understand. I understand your view on that
27 point, but I'm just trying to understand right now what this means.

1 So, the independent processes, does that mean that the processor is
2 also running independent processes, this language in Claim 1, for example?

3 MR. SHNEIDMAN: Well, so, good question. I think it's saying the
4 gate array is configured to run independent processes. And then it goes on
5 to say in parallel with the processor. But focusing first on that first bit, it's
6 the gate array is configured to run independent processes, so it's whatever is
7 going on within the gate array.

8 (Simultaneous speaking.)

9 JUDGE JURGOVAN: These independent processes are not related to
10 a clock signal in your view?

11 MR. SHNEIDMAN: I don't think it's --

12 (Simultaneous speaking.)

13 JUDGE JURGOVAN: -- or a voltage regulation?

14 MR. SHNEIDMAN: No, I don't think so. And I can jump to a slide
15 that shows that, but I think the '177 patent undermines sort of the clock
16 regulation argument. Let me just see here. If you look at slide 24 for
17 example, the '177 patent sort of gives two pieces of information that tell us
18 it's really not about clocking.

19 The first is, it's an example of redundancy. And A1, A2, and A3 here
20 are -- imagine it's the same signal processing application. Like, maybe this
21 is outer space, and you have bit rot and radiation. And it might knock out,
22 you know, the FPGA gates that are running on the A1, so you might have
23 some bad calculations going on.

24 And so, you're performing this calculation, but in order to do the
25 redundancy, you've got to be performing this thing at the same time the data
26 is coming into the system, it's literally being clocked in, right? So you've got

1 the same clock that's driving A1, A2, and A3, and Dr. Shanfield explains
2 this in his declaration as that this is what it means: The POSITA --

3 JUDGE JURGOVAN: I understand. I think the '177 describes that
4 those processes could be the same or they could be different from what I --
5 (Simultaneous speaking.)

6 JUDGE JURGOVAN: I think you've answered my question. So, you
7 know, to the extent you need to reach other matters, please do so.

8 MR. SHNEIDMAN: Thank you, Your Honor.

9 JUDGE JURGOVAN: Thank you.

10 JUDGE ZADO: So, actually, I -- this is Judge Zado. I do have a
11 follow-up question. If we were to interpret Claim 1, Limitation 1.5 as
12 requiring that it's the processes on the FPGA that must be independent of
13 each other, where has Petitioner shown that the processes in either Lyke's
14 FPGA or a skilled artisan would have understood the processes in Lyke's
15 FPGA are independent of each other?

16 The reason I ask this question is it did seem like in the petition,
17 Petitioner was arguing that the processes on the FPGA in Lyke are
18 independent of the processes on the processor rather than arguing they're
19 independent of each other. So I just wanted to ask -- so I want to ask the
20 question, can you identify where in the petition the argument is made that
21 the processes in Lyke's FPGA were or would have been understood to be or
22 it would have been obvious for them to be independent of each other?

23 MR. SHNEIDMAN: Yes. Thank you for the question. The petition,
24 at page 28, so there's a sentence that says -- and it's talking here about the
25 arbitration process -- the portion -- this portion of the FPGA runs an
26 arbitration process to manage the flow of data throughout the remainder of

1 the MCM, independently and in parallel to whatever computation is
2 happening on the processor and other portions of the FPGA.

3 So the point there and the citing reference to Dr. Shanfield explaining
4 this more is you have a bunch of stuff going on in the FPGA, different
5 processes that are all separate. Whatever is going on in the power process is
6 different than what's going on in the ADC -- excuse me -- the analog-to-
7 digital converter process is different than what's going on in the bus
8 arbitration. And so, the point is, there's a whole series of items that are
9 running independently. It's also discussed in the -- so that's the petition. I --

10 JUDGE ZADO: So, this quote you just read, you said it's at page 28
11 of the petition?

12 MR. SHNEIDMAN: Yes.

13 JUDGE ZADO: Where does it begin? Which paragraph?

14 MR. SHNEIDMAN: Second, even beyond Lyke's teachings,
15 Dehkordi describes a gate array. Do you see that?

16 JUDGE ZADO: I do. So --

17 MR. SHNEIDMAN: And then, about halfway through the paragraph,
18 this portion -- quote, portion of the FPGA runs an arbitration process to
19 manage the flow of data, et cetera, et cetera, independently and in parallel to
20 whatever computation is happening on the processor and other portions of
21 the FPGA.

22 JUDGE ZADO: Okay. I see that. Thank you. And I believe you
23 were about to point us to somewhere else?

24 MR. SHNEIDMAN: Yes. So --

25 JUDGE JURGOVAN: Counsel, before you leave bus arbitration,
26 does bus arbitration necessarily mean the processes that are running on the

1 DSP and the FPGA are different or are independent? I mean, bus arbitration
2 is just arbitrating who -- what device has control over the bus, correct?

3 MR. SHNEIDMAN: I --

4 (Simultaneous speaking.)

5 JUDGE JURGOVAN: -- not necessarily whether the programs are --
6 they could be dependent on one another, right? I mean, the DSP might be
7 waiting for some data from the Xilinx. Xilinx arbitrates and gets control of
8 the bus and sends that to the DSP. Those are not independent programs,
9 correct?

10 MR. SHNEIDMAN: So I think that the bus arbitration process itself
11 is orthogonal and independent to however the higher level, for lack of better,
12 are using the bus, right? It's simply a communication process that's
13 managing access. And what it's -- its world is not affected. It's not -- you're
14 not getting computational assistance, for example, to use Patent Owner's
15 terms, from the processor in order to perform that arbitration process.

16 JUDGE JURGOVAN: Right as to arbitration of the bus, but it doesn't
17 mean that the programs running on the DSP and the FPGA are independent
18 from one another. They might be very dependent on one another.

19 MR. SHNEIDMAN: I think depending on what you mean by
20 dependent, which is a whole other crux, but I do think that the bus
21 arbitration process itself is independent from whatever process is running on
22 that processor.

23 JUDGE JURGOVAN: I see what you're saying. Okay. Thank you.

24 MR. SHNEIDMAN: Yeah. And so, yeah. Let's see here. What's the
25 fastest way for me to get -- I think Exhibit 1050 at paragraphs 102 through
26 104 and 111 through 112 as further examples of Dr. Shanfield explaining

1 how the processes running on the FPGA are different from each other and
2 are independent from each other.

3 JUDGE ZADO: Okay. Thank you.

4 MR. SHNEIDMAN: Of course. All right. So let's see. Maybe what
5 I'll do here is turn to slide 19. And this is the point that I was sort of
6 planning on addressing the Patent Owner's Response's arguments about
7 control and clocking. And on slides 21 and 23, we excerpt out portions of
8 that Patent Owner Response that asserted statements about control and
9 clocking.

10 But I think, the Patent Owner's Sur-reply at page 6 goes in an
11 interesting, different direction, so I want to look at that. On page 6 of the
12 Patent Owner's Sur-reply, it says, Xilinx's argument that Patent Owner is
13 allegedly embedding notions of control and clocking into the claim
14 construction is not an effective rebuttal. For one, those words do not appear
15 in Patent Owner's proposed construction. And second, Xilinx did not
16 explain how Patent Owner's proposed construction can be read to implicitly
17 include those concepts.

18 That's a curious statement as we read Patent Owner to be throwing out
19 their prior argument to try and avoid the prior art. I think the POR is pretty
20 clear that they're trying to make some linkage.

21 But to the extent that clocking or control is still in play, you know, we
22 addressed that head-on in our briefing, Petition Reply at pages 16 through
23 20; the declaration, Exhibit 1050, at paragraphs 117 through 136. I'm happy
24 to answer questions about it from the Board, but given the limited time, I do
25 want to engage briefly with the Patent Owner's Sur-reply's new pivot.

26 The Patent Owner's Sur-reply, at pages 9 through 12, does proceed in
27 a new direction as Patent Owner claims that, quote, the claim term involving

1 independent processes requires viewing the independent processes on a
2 system level instead of the sub-application level.

3 And goes on to say that, quote, one must examine other criteria at the
4 system level. And that's at pages 11 and 12.

5 JUDGE ZADO: So, Counselor, I have a question for you on this. Is
6 Petitioner contending that this, what you referred to as a pivot, this argument
7 about independence having to be at a system level instead of application
8 level, is that new argument, or is that responsive to something in Petitioner's
9 Reply?

10 MR. SHNEIDMAN: Look, I think it's new argument. I also think it's
11 easier just to dispose of the argument. I don't think it is proper. I don't think
12 that the ground rules allow for this, but let's arguendo that it's fair, right? I
13 think that there's no support for that is the point, in the '177 patent. There's
14 no support for that in the expert declaration. If you look at pages 9 through
15 12 in the POSR, there's no citation for any of this attorney argument, and so
16 it's naked. It's neither relying on intrinsic nor extrinsic evidence as to what
17 the POSITA would understand. And it's just simply unsupported.

18 But taken at face value, I think the prior art also teaches their new
19 concept of independence as well. And so, what I propose to do is to jump to
20 slide 26 and address the prior art covering this challenged element under all
21 of the proposals. And if the Board has questions about other aspects, I'm
22 certainly happy to do that too.

23 But if we move to slide 26, this is Dehkordi. And let's first talk about
24 how the prior art combination provides the disputed claim element. And I'll
25 start, again, by focusing on the language of the claim, which Your Honors
26 have already asked about, and it's at the top of the screen here, this snippet --
27 of course, it's a longer portion -- the gate array configured to run

1 independent processes. So, again, we're talking about the FPGA being
2 configured to run these independent processes.

3 And so, the first art of note is Dehkordi, which teaches this MCM
4 with all of these components, the FPGA, the processor, the analog-to-digital
5 converter, the memories. And another teaching includes that the FPGA has
6 a configuration that may come from outside the MCM. That is, it's separate
7 programming, and that the FPGA has portions of gates configured in
8 different ways. And so, one of the teachings is a portion of the FPGA gates
9 configured for multiprocessing bus arbitration as we've discussed.

10 And if we turn to slide 27, that shows the portion of the FPGA gates
11 described in the text at the bottom there, of Dehkordi's Figure 1, along with
12 other separate processes. And we see here the power-up process, the analog-
13 to-digital interface process, the DSP functions, et cetera. And I refer the
14 Board to our argument about these aspects of this in our petition at pages 28
15 and 29.

16 And as Dr. Shanfield explains, as we've already discussed, the
17 processes have nothing to do with each other. The POSITA would have
18 recognized this as the classic example of the FPGA being split up so that
19 different portions of the gates on the FPGA are performing the separate
20 functions. And we know that from the literal disclosure as well as
21 Dr. Shanfield describing this and putting this in the context of the prior art.

22 JUDGE ZADO: So, Counselor, one of Patent Owner's arguments is --
23 well, there are two that I want us to have time to discuss. The first one is
24 that Patent Owner -- and I believe this is at page 12 of the sur-reply, and I'll
25 double check on that. But in essence, Patent Owner has this argument that --
26 involving circuit A and circuit B, but I'll paraphrase that, basically, if a
27 computational process -- if the output of computational process A is input

1 into process B, then these processes are not independent of each other. And
2 the exact language is in the sur-reply I believe at 12 -- let me see where it is.

3 MR. SHNEIDMAN: I think it's page 13, Your Honor, the further, in
4 hardware design paragraph.

5 JUDGE ZADO: Thank you. Yes. This is page 13 of the sur-reply.
6 The exact language is, when circuit A performs a computation and produces
7 an output that is received as an input by circuit B and used to perform a
8 computation, this is an example of two processes that are not independent.

9 And I paraphrased that to be basically, if a process A -- if the output
10 of process A is received by process B and used by process B, these two
11 processes, A and B, are not independent of each other.

12 And so, I think what Patent Owner is saying is even if Dehkordi has
13 these processes that I guess are, at the application level, independent, it
14 seems Patent Owner's argument is that somehow these are not independent
15 because the output of one is the input to another. And so, I just -- I don't
16 know if Petitioner has a response to that.

17 MR. SHNEIDMAN: Sure. So the first thing I'll observe here is that
18 Patent Owner is talking about Dehkordi 2 in its example, with Petitioner, of
19 course, relying on Dehkordi.

20 I think that if I think of the '177 patent and its example, it's a firm
21 example of independent processes. It's describing them as independent
22 subsets of gates, and it's not putting -- like, I feel like the Patent Owner is
23 trying to move the ball of what independence means in the broadest sense in
24 order to try to avoid the prior art.

25 In fact, though, Dehkordi's bus processing process has nothing to do
26 with the ADC, has nothing to do with the power-up circuitry. It's not a case
27 where you're feeding circuit A and -- you know, you're not feeding the

1 output of circuit A into circuit B. So, the example, the straw man it's setting
2 up with respect to Dehkordi 2, isn't actually what's going on -- what we're
3 focused on in Dehkordi.

4 And again, I'd refer to paragraphs 102 to 104 and 111 through 112 of
5 Dr. Shanfield's testimony in Exhibit 1050 where these are really processes
6 that very closely logically match the kind of thing that's going on with A1
7 through A3 and its description there within the '177 patent. So I see it as a
8 bit of a red herring of an argument. I also think it's a limitation that's not
9 contemplated in the description in the '177 patent itself.

10 JUDGE ZADO: Okay. Thank you. I'd also like to note at this point
11 you have 3 minutes.

12 MR. SHNEIDMAN: All right. I appreciate that. Maybe what I will
13 do is briefly touch on -- I do want to touch on Ground 4 briefly. Let me just
14 conclude up here by moving to slide 33.

15 What I'd say is Petitioner has presented prior art in this trial that
16 invalidates this gate array element under all the potential interpretations of
17 the term, from the plain and ordinary meaning proposed by Petitioner where
18 the processes are run separate from each other, as well as all the way up to
19 this new sur-reply system-level thing, which is if you're looking -- again, I
20 guess I didn't finish that out with Dehkordi.

21 If you're looking at a system level of these processes within -- that's
22 depicted in that Figure 1 of Dehkordi, again, they're not interplaying with
23 each other. There's no computational interaction with each other, as
24 Dr. Shanfield unrebuttably testifies.

25 And so, the other aspect I guess I'd make here -- or the other point I'd
26 make is the Patent Owner doesn't engage with the more than the dozen
27 reasons that the POSITA would make the combination of prior art as well as

1 the expectation of success. And we'd ask the Board to adopt or to find that
2 that is satisfied. It's something that wasn't necessary to reach an Institution
3 Decision, but here, to go ahead and find the motivation to combine as
4 shown.

5 And I guess I'd ask that the Board find the claims challenged in
6 Ground 1 are valid not just under our claim construction, which we
7 encourage the Board to adopt, but also to find the prior art invalidates the
8 claim under any claim construction at issue in the case.

9 So, in my one minute, let me briefly touch on Ground 4 if we move to
10 slide 37. And the point I really want to start with here is we're showing on
11 slide 37 the exemplary claim language relating to the power converter
12 element. And the point I want to make first is that everything that's
13 highlighted in yellow is already literally taught in Lyke, no dispute.

14 Lyke itself disclosed, quote, an internal embedded power converter
15 means capable of generating each operating and reference voltage needed
16 within the instrument controller.

17 And I refer the Board to the petition at page 46, which cites Lyke at
18 column 5, lines 54 through column 6, line 9.

19 So the alleged novelty is doing this within a gate array. And if I go to
20 slide -- let's go to slide 39. In the upper right, we have the claim language.
21 And again, Lyke is providing everything for itself that's in yellow.

22 But Steele also provides a power converter element in an FPGA
23 programmable logic device. And Steele teaches its invention as being in an
24 FPGA. That's described column 4, lines 6 through 10. Steele's invention is
25 in a portion of gates, and Steele explicitly teaches that the user, quote, may
26 stuff in logic, unquote, into other unused parts of the FPGA. And that's
27 column 8, lines 12 through 18.

1 And then I'll just, you know, close this part by saying Steele teaches
2 that the present invention provides output signals which are derived from the
3 input power supply. And if I look at the lower-right language here, if I just
4 zoom in -- my eyes aren't so great -- but meanwhile, an output signal is
5 generated by this controller logic block 1 are at a 3-volt level. These 3-volt
6 output signals can then be used by those devices operating on signals in a 3-
7 volt reference.

8 So we feel that Steele is definitely explicit in terms of its teachings of
9 a power converter in an FPGA, Lyke teaching you everything in yellow in
10 the upper right-hand corner of five, but then also putting this within Steele
11 we think Steele teaches this as well.

12 So, slide 49, I know I'm a little over. I'll cut into my rebuttal time
13 here. I'm just focusing on the last point is that there are multiple reasons for
14 explaining the motivation to combine.

15 There's one aspect I just want to flag which is the Patent Owner makes
16 a very short argument and doesn't really dispute the motivation to combine
17 with the expectation of success, but it does make a very short argument that
18 because Lyke teaches the power converter that such a combination with
19 Steele is superfluous in hindsight. And that's not correct.

20 Dr. Shanfield explained why, in particular, in space applications, the
21 POSITA would have sought to reduce the number of elements for radiation
22 concerns and cost savings. He gave multiple pieces of extrinsic evidence,
23 including references that were contemporaneous, advocating for such a chip
24 reduction for liability and cost reasons, among other points.

25 And the Patent Owner didn't engage with any of this evidence. It
26 doesn't dispute this. It doesn't address it. And so, the evidence is
27 unrebutted.

1 And so, again, we'd ask that the Board adopt our claim construction
2 but also find that the prior art teaches these elements under either claim
3 that's advanced in the case.

4 So, unless the Board has other questions, I'll stop for now. And I
5 welcome other questions.

6 JUDGE ZADO: So I have no further questions for now. And I don't
7 whether my colleagues do.

8 (No response.)

9 JUDGE ZADO: Okay. So you've argued for 38 minutes. And so,
10 you have 7 minutes remaining for rebuttal.

11 And with that, we'll go ahead and let's now hear Patent Owner's
12 arguments. So, whenever you're ready, you may begin.

13 PATENT OWNER ARGUMENT

14 MR. COCHRAN: Thank you, Your Honors. Obviously, there's a lot
15 that we would disagree with, with what Petitioner just argued. And I'm
16 happy to start this off with answering any questions that you may have on
17 specific issues, but I'd like to start with claim construction if there are no
18 questions first.

19 JUDGE ZADO: I just ask that you please identify yourself for the
20 record before you continue.

21 MR. COCHRAN: Sure. My apologies. My name is
22 Andrew Cochran.

23 So the claim construction issues here are -- really go to one of the
24 cores of what this invention is really about. The independent processes in
25 parallel with the processor is part of an overall claim that must be taken as a
26 whole, together, not in isolation.

1 And we have a field programmable gate array configured to -- take
2 you to the claim language on slide 5 of Patent Owner's petition. A field
3 programmable gate array configured -- wait. I'm sorry. Let me back up --
4 gate array coupled to the processor and configured to run independent
5 processes, plural, in parallel with the processor.

6 And this was a big distinguishing point in the intrinsic evidence,
7 including the specification, and in the prosecution history on why this was
8 an improvement and a patentable improvement over Lyke, which the
9 Government issued to Mr. Blemel, a contract to him specifically improve
10 over Mr. Lyke's invention.

11 JUDGE ZADO: Counselor, I'm going to ask a question here because
12 what I would really like to hear -- so we have your Patent Owner's papers
13 and understand -- I believe I understand the positions about looking at the
14 claims as a whole, but what I'm trying to understand is the word
15 computational because the Patent Owner defines a process as a
16 computational process programmed into the FPGA gates.

17 So rather than saying what a process is, it appears Patent Owner has
18 inserted the word computational in front of the word process, even though
19 the word computational is not in the claim language or anywhere in the
20 specification. And then goes on with the construction of independent
21 process to say without computational assistance from another.

22 And so, what I'm grappling with here -- and then I'll say one other
23 thing. In the sur-reply, at pages 3 to 4, Patent Owner then goes even further
24 and writes the claim language, but replaces the word independent processes
25 with, quote, computation processes programmed into the FPGA, which must
26 each be independent -- i.e., occur without computational assistance -- from

1 another computational process programmed into the FPGA, and from the
2 processor.

3 I'm trying to understand what the word computational is adding here.
4 I understand, in the Patent Owner Response, there's discussion of a system
5 level versus application level. I still fail to understand what the word
6 computational has to do with any of this.

7 And so, if you could please spend time discussing why the word
8 computational is even relevant and how it even supports this argument about
9 system level versus application level because I'm just not seeing it.

10 MR. COCHRAN: Sure. So, I think, in general, the computation is
11 added to emphasize that these are independent and that other processes that
12 do not have computational assistance from -- process X doesn't have
13 computational assistance from process Y. That goes to the independence of
14 what these processes really are.

15 And it goes to what Your Honor said earlier about if process A is
16 providing input to process B, are they really dependent or independent? And
17 I think that we would argue that they are dependent on each other because
18 computational assistance is needed between them. But really --

19 JUDGE ZADO: Well, I'm going to ask you about that as well, sur-
20 reply at page 13, because I still don't understand what computation adds.

21 When I had paraphrased this argument to the Petitioner, I paraphrased
22 it as -- basically, if circuit A performs a process -- because process is the
23 language we see in the claims -- if circuit A performs a process, and if the
24 output of that process is received by circuit B, and circuit B uses that to
25 perform a process, I still don't understand why the word computation -- I still
26 don't understand what it adds because it seems like what Patent Owner's

1 argument really is, is not the word computation. It's if a process is
2 performed.

3 And this process is essentially software programming code. You
4 perform this process -- it could be software programming code or
5 programming of the FPGA gates. You perform this process, and if the
6 output of that process is used for the input of another process, these two
7 processes are linked and no longer independent of each other because the
8 output of one process is the input of the other process.

9 We also have this notion that a process is basically, you know,
10 programmed by how the FPGA gates are arranged. So I'm not
11 understanding what the word computation is adding here.

12 MR. COCHRAN: So I think your interpretation is correct. I think in
13 terms of interlinking two processes together if one provides input -- if the
14 output of one provides the input to the other, they're linked together and no
15 longer -- we would say that they're no longer independent of each other --
16 independent from each other.

17 And so, in that sense, computation, it adds to the claim construction in
18 that it gets to that example of the process A and process B being linked
19 together, but it not necessarily -- the wording itself is not necessarily --
20 because the focus is on independent. And it is -- the claim language itself is
21 independent processes in plural, which I -- so there are multiple processes
22 going on here that are independent.

23 So that's -- I think your interpretation is incorrect, except for I do have
24 some comments about your mention of software. But in that sense,
25 computation is really going to the independence.

26 JUDGE JURGOVAN: So, Counsel, let me ask the same question I
27 asked the Petitioner. And that is, here, the word independent, do you

1 interpret that to mean that the processes running on the FPGA are
2 independent from one --

3 MR. COCHRAN: Yes. There will be processes running on the
4 FPGA that are independent of each other.

5 JUDGE JURGOVAN: Okay. So we've got that much established
6 then.

7 What -- does that word independent also mean that there are processes
8 on the processor that are independent and running in parallel with these
9 independent processes on the FPGA, or does the independent processes here
10 just refer to the processes running on the FPGA?

11 MR. COCHRAN: Our interpretation, and a very high-level example,
12 is that there would be three processes. So, to answer your question directly,
13 I think it's -- there will be an independent process running on the processor,
14 and at least two independent processes running on the FPGA, all of which
15 can be independent of each other.

16 JUDGE JURGOVAN: Okay. So the word independent, does that
17 also have anything to do -- as used in this limitation, 1.5, does that have
18 anything to do with power conversion or clock signals because I think you
19 argued that it does?

20 MR. COCHRAN: So I think they're examples of what could be
21 involved, but they're not --

22 JUDGE JURGOVAN: Okay.

23 (Simultaneous speaking.)

24 JUDGE JURGOVAN: Well, let me ask this then. If the processor
25 and the FPGA are clocked by the same signal, why can't their processes be
26 independent?

1 MR. COCHRAN: Well, from my understanding, Your Honor, that if
2 they're clocked by the same signals that they're -- one is in control of the
3 other or one is in control, or the other is in control. There's no independence
4 there.

5 JUDGE JURGOVAN: Assuming that the CPU has generated the
6 clock signal, which I don't think is the case.

7 MR. COCHRAN: Correct. And forgive me if I'm -- I'm not as up on
8 my electrical engineering. I think you may have known that we've lost a
9 member of our team, but I'm doing my best to answer the electrical
10 engineering questions.

11 JUDGE JURGOVAN: Okay. I appreciate that. And then, with
12 respect to the power conversion, again, same question. I mean, just because
13 the processor and the FPGA are receiving the same power level, why
14 wouldn't the processes running on each be independent from one another?

15 MR. COCHRAN: I think there are scenarios where they would be
16 independent from each other if I'm understanding your question correctly.

17 JUDGE JURGOVAN: Okay. Thank you. You've answered my
18 questions. Appreciate it.

19 MR. COCHRAN: Yeah. And I think, ultimately, the independent
20 processes in parallel with the processor on the system level within the
21 instrument controller as a whole goes to the core of the invention and this
22 multifunctionality and flexibility when it comes to programming this for
23 different sensors and having different functionality as it's used for whatever
24 purpose it might be used for.

25 So, if I may then --

1 JUDGE McSHANE: Counsel, this is Judge McShane. Just a quick
2 one. Could you give me like a one or two-sentence description or, if you
3 will, definition of what a computational process is in your view?

4 MR. COCHRAN: Sure. I will do my best, Your Honor, with the
5 caveat that my electrical engineering is not top-notch. But I think -- so,
6 perhaps, a simple example of a sensor -- a temperature sensor that is on a
7 portion of the FPGA gates that is set to regulate a fan depending on
8 thresholds of temperature that it has sensed. So it has -- it is computing the
9 temperature as it receives the signal, and it is able to then turn the fan on or
10 off depending on the threshold that it meets. And that is an independent
11 process that does not involve the processor or any other portion of the FPGA
12 gates.

13 And there could be multiple of those depending on how many sensors
14 are programmed into it and other programs. Does that help, or did I --

15 JUDGE McSHANE: Yeah. But that's basically the code running,
16 right? The program code?

17 MR. COCHRAN: So, from my understanding -- and that's where I
18 take issue with Petitioner's claim construction for process which seems to be
19 going more towards a software-oriented definition of a process instead of
20 what the claim actually says and what the intrinsic evidence actually says,
21 which is more on the higher-level system hardware design processes. They
22 are, in my view, two different things.

23 And the intrinsic evidence supports the hardware design aspect of a
24 claim construction -- it does not support Petitioner's claim construction
25 which is more software. And I think that's clear if you look at what
26 Petitioner presented in their argument. They only had a single instance of
27 the intrinsic evidence that -- I don't actually see how it supports a software

1 reading of independent processes. They say it does. But the other evidence
2 that they presented is all intrinsic evidence that does not tie into the intrinsic
3 evidence at all.

4 And I can go to the intrinsic evidence to talk more about that unless
5 Your Honor has additional questions.

6 JUDGE McSHANE: Sure. I don't have additional questions, but you
7 know, so please continue.

8 MR. COCHRAN: So, on slide 7 of Patent Owner's demonstratives,
9 I've listed out several pieces of the intrinsic evidence here that goes toward
10 what we say is support for independent processes being the computational
11 processes that are each run separately -- or I shouldn't say separately because
12 I do take issue with that too. They're independent and do not have
13 computational assistance from other processes.

14 Because this system as a whole, what the patent explains is, it's freely
15 re-configurable and separately programmable multipurpose digital system
16 that can run independent of the microprocessor. The FPGA may operate
17 either under control of the microprocessor, for example as a coprocessor, or
18 may be operated independently.

19 And in that section, there's examples of different clock scenarios as
20 well, which is why we said in our sur-reply that our definition is clock-
21 agnostic. It goes into Figure 2, where the gates X1, X2, and X3 are
22 configured to route an input node A to any one of three independent
23 processes, A1 through 3. The processes are independent configurations of a
24 subset of gates within the FPGA.

25 And the configurations of the subset of the FPGA goes to that system-
26 level argument of these hardware design processes that have -- that are

1 different and distinct from what I would say software software-implemented
2 processes that would be running on the processor.

3 The inclusion of the FPGA in the design of the present invention
4 provides simultaneous parallel processing capability that can be
5 implemented as a mathematical coprocessor and still perform as a digital
6 signal processor of multiple analog signals simultaneously digital -- digitized
7 by the ADC, all the while switching input lines to the ADC.

8 This is a multifunctional instrument controller with a processor and an
9 FPGA. The FPGA configured to run independent processes parallel --
10 plural, in parallel with the processor. The aspect of Petitioner's separate for
11 independent does not answer or, what I said in the sur-reply was, it does not
12 resolve the dispute because something could be separate and still depend on
13 something else. So it doesn't get to the question of what independent
14 actually is in the claim language itself.

15 Lyke, if I may go to Lyke, is something that was extensively reviewed
16 and studied in the patent itself and in the prosecution history by the
17 examiner. The patent itself --

18 JUDGE ZADO: Counselor, I have one question about Lyke. The
19 portion of Lyke that describes an FPGA -- and I'll get you exactly to that
20 portion of Lyke.

21 MR. COCHRAN: I have it, Your Honor.

22 JUDGE ZADO: Bear with me for a moment. It's at column 8. I just
23 want to be clear on the record. It's at column 8. It begins at around line 48.
24 The matter set forth in the foregoing description and accompanying
25 drawings is offered by way of illustration only and not as a limitation.

26 It goes on to say, at line 55, a RAM-based field programmable gate
27 array, interfaced internally within the AIC and configured automatically

1 through a downloading mechanism involving AIC's internal CPU and access
2 of the non-volatile memory, may also be included.

3 I didn't see this particular description of a field programmable gate
4 array mentioned anywhere in the '177 patent; is that correct?

5 MR. COCHRAN: I do not think the '177 patent mentions this exact
6 passage in Lyke, no. So I think you are correct in that sense.

7 JUDGE ZADO: And can you point to anything in the prosecution
8 history showing that the examiner identified this passage of Lyke?

9 MR. COCHRAN: I can say that the examiner -- I cannot point to a
10 particular passage within the prosecution history where the examiner
11 identified this exact portion.

12 But the record, I think, is clear that the examiner was focusing in on
13 the FPGA aspect of the invention and did numerous searches looking for art
14 discussing the FPGA. So it's difficult to see how the examiner -- if he or she
15 did miss it, how it wouldn't have come up again when the examiner was
16 extensively searching it during his review.

17 I can also say that this passage in Lyke says nothing about
18 independence, separate, or in anyway configured to do anything other than
19 that it could just be added to the system.

20 And it's clear within the '177 patent, the background, and the
21 description of the invention, that this is a point of distinction and a point of
22 improvement of the '177 patent over the invention of Lyke.

23 I think that, ultimately, except for what Your Honor mentioned that
24 there's no statement or citation in the patent or the prosecution history to this
25 particular column 8, I don't think there's any evidence to the contrary either,
26 that the examiner didn't recognize this and decided not to use it.

1 In fact, I think the examiner studied Lyke quite a bit, used the Lyke
2 reference as its primary reference, and recognized that it did not in fact teach
3 what the Patent Owner was claiming at the time.

4 And this was said in the prosecution history as well. This is exhibit
5 1010, 1010. And the response to the examiner's rejection, which I may
6 actually take into -- so those -- on page 57 of Exhibit 1010 -- this is the
7 examiner's rejection -- it says explicitly, Lyke fails to disclose an embedded
8 memory for storing an initialization program and a field programmable gate
9 array coupled to the processor for parallel processing.

10 And in the response, describing the aspect of the invention -- or the
11 invented concept, says that the instrument controller of the present invention
12 offers enhanced power management and functional flexibility, separately
13 controllable FPGA.

14 And this -- I'm sorry -- is on page 43 of Exhibit 1010.

15 JUDGE ZADO: Counselor, my understanding -- I just want to make
16 sure that I have this right because the examiner -- well, first of all, the '177
17 patent and, frankly, the Patent Owner, in making these claims in the '177
18 patent that Lyke did not disclose an FPGA that can run independent parallel
19 processes, the Patent Owner neglected to even cite this passage.

20 But putting that aside for a moment, the examiner ultimately actually
21 found this claim limitation was obvious in view of Lyke. And so, even the
22 examiner found this to be obvious.

23 Now, the examiner -- we're not going to speculate as to whether the
24 examiner actually read the portion of Lyke that describes an FPGA or
25 whether the examiner ultimately felt that regardless of whether there was
26 expressed disclosure, this would have been obvious in view of Lyke. But

1 the examiner did find it would have been obvious in view of Lyke and
2 pointed to another reference, Cloutier, which is not at issue here.

3 And so, I just wanted to point that out for the record because I don't
4 seem to hear -- because my understanding is I don't believe Petitioner is
5 saying that Lyke expressly discloses that its FPGA is an independent --
6 discloses Limitation 1.5 but is rather arguing that what a skilled artisan
7 would have understood. So it seems to me that the argument really isn't
8 about whether Lyke actually expressly discloses this but whether a skilled
9 artisan reading Lyke would have found this obvious. And the examiner
10 actually found that this would have been obvious.

11 MR. COCHRAN: So I -- to answer that or to respond to that, the
12 examiner, to me, clearly does not find that Lyke -- to say that the FPGA
13 configured to run independent processes in parallel with the processor,
14 which was an element of the claims from the very, very beginning. It was in
15 the original application and the original claims. I don't see that the examiner
16 has found that obvious in view of Lyke.

17 I think the examiner has said that he didn't see that aspect in Lyke and
18 brought in Cloutier as a different reference to argue that it would've been
19 obvious over the combination of the two. And ultimately, he granted, or she
20 granted -- I forget if it was a he or she at this point -- allowed the application
21 after indicating that there was allowable subject matter.

22 JUDGE ZADO: So, Counselor, before we run out of time, I wanted
23 to briefly ask you a question that I also put to the Petitioner, and this is about
24 the level of ordinary skill in the art because Petitioner -- I think on the
25 education side, both parties were pretty much in the same place, but for the
26 experience, we have at least two -- Petitioner says it's at least two years of

1 experience related to the design and development of multichip modules
2 operating as instrument controllers.

3 And Patent Owner's position is it's at least four years of experience in
4 FPGA and processor systems design, including but not limited to system on
5 a chip or SOC and electronic vehicle sensor systems or related technologies.

6 And so, my question is, can you identify any argument in the record
7 made by Patent Owner because I did not see it, any argument in the record
8 by Patent Owner that either Petitioner or Dr. Shanfield's positions are
9 incorrect as a result of applying a different level of ordinary skill in the art?

10 MR. COCHRAN: Thank you, Your Honor. I think both definitions
11 of POSA are very similar, and the arguments would be the same under either
12 definition.

13 I do think that this is more than just a combination of off-the-shelf
14 products as Petitioner characterized it. I think that there is some specialty
15 here that would -- might require additional levels of experience. But
16 ultimately, I think both definitions provide -- I don't think it would make a
17 difference.

18 And if I may, if I'm running out of time, I'd like to address one quick
19 thing about Steele. So if I could take you, please, to --

20 JUDGE JURGOVAN: Counsel, before you go to Steele, can I ask
21 just a few questions? One is, the independent processes, I think that the
22 Petitioner says anyway, that the claim was allowed when the two last
23 wherein clauses were added to the claim.

24 And so, it says that the first portion of the gates does one signal
25 processing, and a second portion of the gates does distribution basically.
26 Are those connected to the independent processes? In other words, are you

1 saying those independent processes are programmed into the first and
2 second portions of gates referred to at the end of the claim?

3 MR. COCHRAN: I think they're certainly examples of what the
4 independent processes can be, and the portions of the gates -- you can go to
5 the claim language as a whole, which we need to look at in order to interpret
6 this particular piece.

7 JUDGE JURGOVAN: Okay. So if we're -- if that last distribution
8 matrix is rerouting signals for use within the instrument controller, do you
9 think that that excludes distributing those signals to the processor?

10 MR. COCHRAN: I think, maybe in this claim, possibly is yes.

11 JUDGE JURGOVAN: Same thing with the signal processing. Do
12 you think the FPGA is doing that on behalf of itself, or would it be doing
13 that on behalf of the processor?

14 MR. COCHRAN: I think, in this particular claim, that -- doing it on
15 behalf of itself.

16 JUDGE JURGOVAN: Thank you.

17 MR. COCHRAN: Sure. And just a few moments here with Steele, if
18 I may, if I'm running out of time. If I can take you to slide 39 of the
19 Petitioner's demonstratives, the --

20 JUDGE ZADO: And by the way, you still have about seven minutes.

21 MR. COCHRAN: I appreciate that. Thank you, Your Honor. So our
22 argument involving Steele is that Steele does not teach power conversion at
23 all.

24 And in the sur-reply, we added in the traditional equation for power,
25 and that is current multiplied by voltage. So the current and the voltage are
26 the variables, and the output is power. And if you change one variable, you
27 will be converting power.

1 And Steele, our argument is that Steele is not doing any sort of power
2 conversion at all. Whatever the -- it's not changing the variables, that is to
3 say. Whatever the output signal -- whatever the output voltage is supposed
4 to be, that's what the input voltage is.

5 And I think the passage in slide 39 of Petitioner's demonstratives, it's
6 the sentence that starts right above the highlighting, says -- and this is on the
7 right-hand side, at the bottom -- For example, a user could couple the VCCO
8 of CFB0 to a supply voltage of 5 volts while simultaneously coupling the
9 VCCO of CFB1 to a supply voltage of 3 volts.

10 Hence, output signals from block zero are at 5 volts, which could be
11 properly utilized. Meanwhile, output signals generated by block 1 are at 3
12 volts. These 3-volt output signals can then be used for those devices
13 operating at 3 volts.

14 It is taking an input of 3 volts and outputting 3 volts. And then it is
15 taking an input of 5 volts and is outputting 5 volts. It's not converting or
16 changing the voltage level at all, and therefore, not converting power in any
17 way. And there's no argument that current is changing here either, so the
18 other variable is not changing at all. And this is just simply not converting
19 power.

20 So, with that, I probably have a few minutes left. I'm happy to
21 address anything you have questions on, especially with the Dehkordi
22 references, but I'll reserve any time to respond to petition.

23 JUDGE ZADO: Okay. I don't have any questions right now. So it
24 looks like you have -- let me just calculate this -- 13 and a half minutes
25 remaining for rebuttal.

26 And so, we'll go now to Petitioner's rebuttal, and just as a reminder,
27 you have 7 minutes for rebuttal, and you may begin whenever ready.

REBUTTAL ARGUMENT

MR. SHNEIDMAN: Thank you, Your Honor. Just a couple points, and I won't take the full time here.

Earlier, you had asked about the POSITA, and I mentioned that Dr. Shanfield had provided his opinions under either construction, and I wanted to provide the cite to that, which is Exhibit 1050, paragraph 16, where he states that, my opinions do not change if Mr. Peck's definition were adopted, and he sort of explains his views there.

The second is the point that I think the Patent Owner concedes, which is we're fighting about a limitation that was already found obvious in prosecution.

And these two wherein clauses that were added were themselves not novel. They're also not limited, I'd say, which is I did hear that the Patent Owner concedes that these are examples of independent processes. I don't think that it is necessarily limited as to how those signal processing or routing -- the claim language doesn't specify a further limit, my reaction at listening there.

Oh, and then this last comment about Steele and the power, again, we're making a combination assertion. There's no question that Lyke discloses everything on the power conversion except for in an FPGA.

And I do think that Steele is read quite literally to suggest taking an object that the present invention has provided, output signal, voltage level which is derived from the input power supply. This is about doing power management and power conversion. I don't think there's a limit on what that means that the Petitioner -- excuse me, the Patent Owner is trying to build into this beyond what the claim simply says.

1 The claim describes what this is supposed to do. It's capable of
2 receiving an input voltage level and generating each operating and reference
3 voltage level within the instrument controller. And that's exactly what
4 Steele is describing, that output signals generated by this block are at a 3-
5 volt level, and they can be used as operating and reference signals.

6 But other than that, I don't think, unless the Board has other questions,
7 I'd heard anything that needs further response.

8 Oh, one other aspect. This whole software thing, we're not talking
9 about software. The claims and the definition of process that we gave is
10 from Patterson and Hennessy. It's a classic EE textbook.

11 On slide 14, right, the independent processes, the intrinsic record is
12 about processes or independent configurations of subsets of gates within the
13 FPGA.

14 We gave another example from Trimberger. It's an FPGA reference.
15 And that's all.

16 JUDGE ZADO: All right. Thank you. So, now, we'll turn to Patent
17 Owner's sur-rebuttal. Patent Owner has 13 and a half minutes.

18 And so, whenever you're ready, you may begin.

19 SURREBUTTAL ARGUMENT

20 MR. COCHRAN: Thank you, Your Honor. I also -- I quickly
21 mention first that their argument that there's a combination with the power
22 conversion, the portion of the gates configured for converting power was
23 that something the examiner identified as allowable subject matter and knew
24 that the examiner, of course, is saying that Lyke does not teach that. They
25 used Steele to teach the power conversion element, and as I just mentioned,
26 Steele does not.

1 So, with that, I'd like to mention a few things about Dehkordi 1 and
2 Dehkordi 2.

3 JUDGE ZADO: Before you do, is this in response to Petitioner's
4 rebuttal? Because sur-rebuttal is limited to responding to Petitioner's
5 rebuttal.

6 MR. COCHRAN: No. It would be something that I should have said
7 earlier, Your Honor. I thought I had half the time that I said I -- that I have
8 actually, so it would not be in response to his rebuttal.

9 JUDGE ZADO: So if you make this argument, I'm going to permit
10 Petitioner to respond. Petitioner still does have about four minutes of
11 argument time.

12 MR. COCHRAN: Fair enough, Your Honor. I think that it would just
13 be very briefly because it's all in our papers, I think, clearly.

14 The Petitioner uses what we call Dehkordi 1, the earlier Dehkordi
15 reference, as the basis for arguing that the field programmable gate array is
16 configured to run independent processes in parallel with the processor. And
17 I think at best -- and this was pointed out in your Institution Decision, but at
18 best, Dehkordi 1 is ambiguous unto exactly what is -- what it is doing and
19 what it is capable of doing. And the -- I think this will come down to the
20 claim construction ultimately, but Dehkordi does not discuss anything about
21 independent processes under Patent Owner's construction.

22 And I know that the Institution Decision points to Kostranov's data
23 path mode as a potential -- and there's two responses to that. One, I think
24 Kostranov itself is not in the grounds and is not established as just general
25 knowledge to a POSA, and it's a theoretical article about three different
26 types of modes that could potentially be there.

1 And second, Dehkordi 2, which is a follow-on paper to Dehkordi 1,
2 clearly states that the data path mode is not a mode of operation for
3 Dehkordi's system. In Dehkordi 2, either the processor is in control of
4 everything in the functional mode, or the FPGA is in control of everything in
5 the testing mode. It's not independent.

6 And then, finally, to allow the Petitioner to respond, I wanted to take a
7 quick look at slide 12 of our Patent Owner's presentation, which is how the
8 inventor, the applicant, described the invention and how it differentiated it
9 from Lyke, which says that the FPGA, again, freely reconfigurable and
10 separately programmable multipurpose digital system that can run
11 independent of the microprocessor. So it's that aspect of the system level
12 independence that I would argue with our claim construction. And with that,
13 I'll pass the mic.

14 PETITIONER RESPONSE

15 MR. SHNEIDMAN: Thank you, Your Honor. This is again Jeffery
16 Shneidman for Petitioner.

17 Just one thing I heard there which is a reference back to control, so to
18 the extent that that's relevant, I just point the Board to slide 22 of our
19 demonstratives. The '177 patent itself describes a CPU with a control line
20 because I heard this reference to this data path mode, et cetera. The '177
21 patent contemplates the processor has a control line to the FPGA. That's not
22 independence. That's pretty clear.

23 We asked the expert for the Patent Owner about this, Figure 1 being
24 an example of the multichip module that's claimed in the '177 patent. He
25 agreed that is the case. That says nothing about whether or not, again, going
26 to the claim language, the gate array is configured to run independent
27 processes. So we're looking at what's going on within the gate array.

1 JUDGE ZADO: All right, Counselors. Is that everything from
2 Petitioner?

3 MR. SHNEIDMAN: It is, Your Honor.

4 JUDGE ZADO: Okay. Well, I have no further questions, and I'm just
5 waiting to see if there are any further questions from the Panel.

6 (No response.)

7 JUDGE ZADO: All right. It appears we have no further questions.
8 And so, that is -- this concludes the hearing for IPR 2023-00195.

9 Once again, we ask that the counsel for each side remain on the line to
10 answer any questions that the court reporter may have, but this concludes the
11 hearing. Thank you, everyone.

12 MR. SHNEIDMAN: Thank you.

13 MR. COCHRAN: Thank you.

14 (Whereupon, the above-entitled matter went off the record at 2:24 p.m.)

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