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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/258,068	08/01/2017	9723662	SUP-104A	1056

74712 7590 07/12/2017
Muir Patent Law, PLLC
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Great Falls, VA 22066

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

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IDS Form PTO/SB/08: Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	15/258,068
				Filing Date	September 7, 2016
				First Named Inventor	Qifeng Ye
				Art Unit	2844
				Examiner Name	Vibol TAN
Sheet	2	of	3	Attorney Docket Number	SUP-104A (S16090US)

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

				LIGHTING ELECTRIC APPLIANCE CO.	
Change(s) applied to document, /J.E.B./ 6/21/2017		US20160102813	04-14-2016	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Ye, et al.
		US20160198535	07-07-2016	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Ye, et al.
		US20160212809	07-21-2016	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Xiong, et al.
		US20160219666	07-28-2016	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Xiong, et al.
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		US20160255694	09-01-2016	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Jiang, et al.
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		US20160381760	12-29-2016	~~JIAXING SUPER LIGHTING ELECTRIC~~	Xiong, et al.

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			Application Number	15/258,068	
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			Art Unit	2844	
Examiner Name	Vibol TAN				
Attorney Docket Number	SUP-104A (S16090US)				
Sheet	1	of	3		

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US20100102729	04-29-2010	Katzir	
		US20160081147	03-17-2016	Guang	
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		US20140265900	09-18-2014	Sadwick et al.	
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15/258,068	09/07/2016	Qifeng Ye	SUP-104A	1056
74712	7590	06/15/2017		
Muir Patent Law, PLLC P.O. Box 1213 9913 Georgetown Pike, Suite 200 Great Falls, VA 22066			EXAMINER TAN, VIBOL	
			ART UNIT	PAPER NUMBER
			2844	
			NOTIFICATION DATE	DELIVERY MODE
			06/15/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

cofficeaction@appcoll.com
pto@muirpatentlaw.com

Response to Rule 312 Communication	Application No. 15/258,068	Applicant(s) YE ET AL.
	Examiner Vibol Tan	Art Unit 2844

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ The amendment filed on 08 June 2017 under 37 CFR 1.312 has been considered, and has been:

- a) ☒ entered.
- b) ☐ entered as directed to matters of form not affecting the scope of the invention.
- c) ☐ disapproved because the amendment was filed after the payment of the issue fee.

Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

- d) ☐ disapproved. See explanation below.
- e) ☐ entered in part. See explanation below.

	/Vibol Tan/ Primary Examiner, Art Unit 2844
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Ye et al.	Attorney Docket:	SUP-104A
Serial Number:	15/258,068	Group Art Unit:	2844
Filed:	September 7, 2016	Examiner:	Vibol TAN
Confirmation Number:	1056		

Title: POWER SOURCE MODULE FOR LED TUBE LAMP

AMENDMENT UNDER 37 C.F.R. 1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

OK TO ENTER: /V.T/
06/12/2017

Dear Sir/Madam:

This amendment is filed in response to the Notice of Allowance of June 5, 2017.

Amendments to the claims begin on page 2 of this paper.

Remarks follow the amendment section of this paper.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Ye et al.	Attorney Docket:	SUP-104A
Serial Number:	15/258,068	Group Art Unit:	2844
Filed:	September 7, 2016	Examiner:	Vibol TAN
Confirmation Number:	1056		

Title: POWER SOURCE MODULE FOR LED TUBE LAMP

AMENDMENT UNDER 37 C.F.R. 1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir/Madam:

This amendment is filed in response to the Notice of Allowance of June 5, 2017.

Amendments to the claims begin on page 2 of this paper.

Remarks follow the amendment section of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims, in the application:

We Claim:

1. (Previously Presented) A power source module for an LED lamp, comprising:

a filament-simulating circuit electrically connected to a first bi-pin terminal and a second bi-pin terminal of the LED lamp, each of the first bi-pin terminal and the second bi-pin terminal configured to allow a current to flow from one pin to the other pin via the filament-simulating circuit during a pre-heat process executed by a ballast;

a current limiting circuit electrically connected to the filament-simulating circuit and configured to limit a current from the filament-simulating circuit;

a first rectifier electrically connected to the current limiting circuit and configured to rectify the current from the current limiting circuit; and

a filter electrically connected between the first rectifier and at least one LED of the LED lamp and configured to smooth the current from the first rectifier.

2. (Original) The power source module of claim 1, wherein the filament-simulating circuit comprises:

a first filament-simulating circuit comprising a first capacitor element electrically connected between two pins of the first bi-pin terminal; and

a second filament-simulating circuit comprising a second capacitor element electrically connected between two pins of the second bi-pin terminal.

3. (Original) The power source module of claim 2, wherein:

the first filament-simulating circuit further comprises a first pair of resistors electrically connected in series, the first capacitor element comprises a first pair of capacitors electrically connected in series, the first pair of resistors and the first pair of capacitors electrically connected in parallel between two pins of the first bi-pin terminal, and a connection point between the first pair of resistors being electrically connected to a connection point between the first pair of capacitors; and

the second filament-simulating circuit further comprises a second pair of resistors electrically connected in series, the second capacitor element comprises a second pair of

capacitors electrically connected in series, the second pair of resistors and the second pair of capacitors electrically connected in parallel between two pins of the second bi-pin terminal, and a connection point between the second pair of resistors being electrically connected to a connection point between the second pair of capacitors.

4. (Original) The power source module of claim 3, wherein an impedance of the first pair of resistors is ten times more than that of the first pair of capacitors, and an impedance of the second pair of resistors is ten times more than that of the second pair of capacitors.

5. (Previously Presented) The power source module of claim 2, wherein the first rectifier comprises two diodes electrically connected in series, and the first rectifier is electrically connected to the first filament-simulating circuit in series.

6. (Original) The power source module of claim 2, wherein the first rectifier comprises two diodes electrically connected in series and a connection node connecting the two diodes is coupled to the current limiting circuit, wherein a current flows from the at least one LED to one pin of the first bi-pin terminal through one of the two diodes and the current limiting

circuit, or from one pin of the first bi-pin terminal to the at least one LED through the other of the two diodes and the current limiting circuit.

7. (Original) The power source module of claim 6, wherein the current limiting circuit comprises at least a capacitor.

8. (Original) The power source module of claim 5, further comprising a second rectifier, wherein the second rectifier is a bridge rectifier electrically connected to the second filament-simulating circuit in parallel.

9. (Original) The power source module of claim 1, wherein the power source module is configured inside a casing of the LED lamp.

10. (Original) The power source module of claim 1, further comprising a discharging circuit electrically connected to the filter in parallel for discharging the filter.

11. (Previously Presented) The power source module of claim 1, wherein the current limiting circuit comprises:

a first capacitor, one end of the first capacitor being electrically connected to one pin of the first bi-pin terminal; and

a second capacitor, one end of the second capacitor being electrically connected to the other pin of the first bi-pin terminal, and the other end of the second capacitor being electrically connected to the other end of the first capacitor and the first rectifier.

12. (Original) The power source module of claim 11, wherein the current limiting circuit further comprises:

a third capacitor, one end of the third capacitor being electrically connected to the other ends of the first capacitor and the second capacitor, and the other end of the third capacitor being electrically connected to the first rectifier.

13. (Original) The power source module of claim 11, wherein the first rectifier comprises two diodes electrically connected in series and the connection node of the two diodes is electrically connected to the other ends of the first and second capacitor.

14. (Original) The power source module of claim 11, further comprising a discharging circuit electrically connected to the filter in parallel for discharging the filter.

15. (Original) The power source module of claim 1, wherein the filter comprises a filtering capacitor electrically connected to the at least one LED.

16. (Original) The power source module of claim 1, further comprising a discharging circuit electrically connected to the filter in parallel for discharging the filter.

17. (Previously Presented) A power source module for an LED lamp, comprising:

a rectifier electrically connected to terminals of the LED lamp and configured to receive a current;

a filter electrically connected between the rectifier and at least one LED of the LED lamp and configured to store energy from the rectifier and to smooth the current from the rectifier;

a discharging circuit electrically connected to the filter in parallel and configured to discharge the energy stored in the filter; and

a filament-simulating circuit electrically connected to a first bi-pin terminal and a second bi-pin terminal of the LED lamp, the filament-simulating circuit comprising at least one resistor connected in parallel to at least one capacitor and configured to simulate a filament of a fluorescent lamp during a pre-heat process executed by a ballast.

18. (Previously Presented) The power source module of claim 17, further comprising a current limiting circuit electrically connected to the first bi-pin terminal of the LED lamp, and configured to limit a current from the first bi-pin terminal.

19. (Original) The power source module of claim 18, wherein the current limiting circuit comprises:

a first capacitor, one end of the first capacitor being electrically connected to one pin of the first bi-pin terminal; and

a second capacitor, one end of the second capacitor being electrically connected to the other pin of the first bi-pin terminal, and the other end of the second capacitor being electrically connected to the other end of the first capacitor and the rectifier.

20. (Currently Amended) The power source module of claim ~~48~~19, wherein the current limiting circuit further comprises:

a third capacitor, one end of the third capacitor being electrically connected to the other ends of the first capacitor and the second capacitor, and the other end of the third capacitor being electrically connected to the rectifier.

21. (Previously Presented) A power source module for an LED lamp, comprising:

a first circuit comprising a first capacitor element electrically connected between two pins of a first bi-pin terminal of the LED lamp, and a second circuit comprising a second capacitor element electrically connected between two pins of a second bi-pin terminal, wherein the first and second circuits are configured to simulate a filament of a fluorescent lamp during a pre-heat process executed by a ballast;

a current limiting circuit electrically connected to the first bi-pin terminal and configured to limit a current from the first bi-pin terminal;

a rectifier electrically connected between the current limiting circuit and the second circuit and configured to rectify the current from the current limiting circuit and a current from the second bi-pin terminal; and

a filter electrically connected between the rectifier and at least one LED of the LED lamp to store energy from the rectifier and configured to smooth the current from the rectifier.

22. (Original) The power source module of claim 21, wherein:

the first circuit further comprises a first pair of resistors electrically connected in series, the first capacitor element comprises a first pair of capacitors electrically connected in series, the first pair of resistors and the first pair of capacitors electrically connected in parallel between two pins of the first bi-pin terminal, and a connection point between the first pair of resistors being electrically connected to a connection point between the first pair of capacitors; and

the second circuit further comprises a second pair of resistors electrically connected in series, the second capacitor element comprises a second pair of capacitors electrically connected in series, the second pair of resistors and the second pair of capacitors electrically connected in parallel between two pins of the second bi-pin terminal, and a connection point between the

second pair of resistors being electrically connected to a connection point between the second pair of capacitors.

23. (Previously Presented) An LED lamp, comprising:

a current limiting circuit electrically connected to a first terminal of the LED lamp for limiting a current from the first terminal;

a first rectifier electrically connected to the current limiting circuit for rectifying the current from the current limiting circuit;

a filter electrically connected between the first rectifier and at least one LED of the LED lamp for smoothing the current from the first rectifier; and

a filament-simulating circuit electrically connected to a first bi-pin terminal and a second bi-pin terminal of the LED lamp, each of the first and the second bi-pin terminals having a current flowing from one pin to the other pin of the respective bi-pin terminal via the filament-simulating circuit during a pre-heat process executed by a ballast.

24. (Original) The LED lamp of claim 23, wherein the filament-simulating circuit comprises:

a first filament-simulating circuit comprising a first capacitor element electrically connected between two pins of the first bi-pin terminal; and

a second filament-simulating circuit comprising a second capacitor element electrically connected between two pins of the second bi-pin terminal.

25. (Original) The LED lamp of claim 24, wherein:

the first filament-simulating circuit further comprises a first pair of resistors electrically connected in series, the first capacitor element comprises a first pair of capacitors electrically connected in series, the first pair of resistors and the first pair of capacitors electrically connected in parallel between two pins of the first bi-pin terminal, and a connection point between the first pair of resistors being electrically connected to a connection point between the first pair of capacitors; and

the second filament-simulating circuit further comprises a second pair of resistors electrically connected in series, the second capacitor element comprises a second pair of

capacitors electrically connected in series, the second pair of resistors and the second pair of capacitors electrically connected in parallel between two pins of the second bi-pin terminal, and a connection point between the second pair of resistors being electrically connected to a connection point between the second pair of capacitors.

26. (Original) The LED lamp of claim 23, wherein the current limiting circuit comprises:

a first capacitor, one end of the first capacitor being electrically connected to one pin of the first terminal; and

a second capacitor, one end of the second capacitor being electrically connected to the other pin of the first terminal, and the other end of the second capacitor being electrically connected to the other end of the first capacitor and the first rectifier.

27. (Original) The LED lamp of claim 26, wherein the current limiting circuit further comprises:

a third capacitor, one end of the third capacitor being electrically connected to the other ends of the first capacitor and the second capacitor, and the other end of the third capacitor being electrically connected to the first rectifier.

28. (Original) The LED lamp of claim 26, wherein the first rectifier comprises two diodes electrically connected in series and the connection node of the two diodes is electrically connected to the other ends of the first and second capacitor.

29. (Original) The LED lamp of claim 23, further comprising a discharging circuit electrically connected to the filter in parallel for discharging the filter.

30. (Original) The LED lamp of claim 24, wherein the first rectifier comprises two diodes electrically connected in series, and the first rectifier is electrically connected to the first filament-simulating circuit in parallel.

31. (Previously Presented) The power source module of claim 1, wherein the current limiting circuit comprises at least a capacitor.

32. (Previously Presented) The power source module of claim 1, wherein:

the filament-simulating circuit comprises a first filament-simulating circuit connected between two pins of the first bi-pin terminal, and a second filament-simulating circuit connected between two pins of the second bi-pin terminal; and

the current limiting circuit comprises at least a capacitor connected to the first filament-simulating circuit, and at least a capacitor connected to the second filament-simulating circuit.

33. (Previously Presented) The power source module of claim 1, wherein:

the LED lamp comprises an LED module comprising the at least one LED;

the filament-simulating circuit comprises a first filament-simulating circuit comprising an impedance element electrically connected between two pins of the first bi-pin terminal, and a second filament-simulating circuit comprising an impedance element electrically connected between two pins of the second bi-pin terminal; and

the power source module further comprises a second rectifier coupled between the second filament-simulating circuit and the LED module, wherein the second rectifier is electrically

connected to the second filament-simulating circuit in parallel and is electrically connected to the LED module in parallel.

34. (Previously Presented) The power source module of claim 17, further comprising a current limiting circuit electrically connected to the second bi-pin terminal of the LED lamp, and configured to limit a current from the second bi-pin terminal.

35. (Previously Presented) The power source module of claim 17, wherein the filament-simulating circuit comprises a first filament-simulating circuit connected between two pins of the first bi-pin terminal, and a second filament-simulating circuit connected between two pins of the second bi-pin terminal.

36. (Previously Presented) The power source module of claim 21, further comprising another current limiting circuit electrically connected to the second bi-pin terminal of the LED lamp, configured to limit a current from the second bi-pin terminal.

37. (Previously Presented) The LED lamp of claim 23, further comprising another current limiting circuit electrically connected to a second terminal of the LED lamp, configured to limit a current from the second terminal.

38. (Previously Presented) The LED lamp of claim 23, wherein the current limiting circuit comprises at least a capacitor.

39. (Previously Presented) The LED lamp of claim 23, wherein the filament-simulating circuit comprises a first filament-simulating circuit connected between a first pin and a second pin of the first bi-pin terminal, and a second filament-simulating circuit connected between a first pin and a second pin of the second bi-pin terminal.

40. (Previously Presented) The LED lamp of claim 23, further comprising:

an LED module comprising the at least one LED, wherein the filament-simulating circuit comprises a first filament-simulating circuit comprising an impedance element electrically connected between two pins of the first bi-pin terminal, and a second filament-simulating circuit

comprising an impedance element electrically connected between two pins of the second bi-pin terminal; and

a second rectifier coupled between the second filament-simulating circuit and the LED module, wherein the second rectifier is electrically connected to the second filament-simulating circuit in parallel and is electrically connected to the LED module in parallel.

41. (Previously Presented) An LED lamp, comprising:

a current limiting circuit electrically connected to a first terminal of the LED lamp for limiting a current from the first terminal;

a first rectifier electrically connected to the current limiting circuit for rectifying the current from the current limiting circuit;

a filter electrically connected between the first rectifier and at least one LED of the LED lamp for smoothing the current from the first rectifier; and

a first filament-simulating circuit electrically connected to a first bi-pin terminal of the LED lamp and a second filament-simulating circuit electrically connected to a second bi-pin terminal of the LED lamp, each of the first and the second bi-pin terminals arranged to have a

current flowing from one pin to the other pin of the respective bi-pin terminal via the respective first or second filament-simulating circuit during a pre-heat process executed by a ballast.

42. (Previously Presented) An LED lamp, comprising:

a current limiting circuit electrically connected to a first terminal of the LED lamp for limiting a current from the first terminal;

a first rectifier electrically connected to the current limiting circuit for rectifying the current from the current limiting circuit;

a filter electrically connected between the first rectifier and at least one LED of the LED lamp for smoothing the current from the first rectifier; and

a first filament-simulating circuit electrically connected to a first bi-pin terminal of the LED lamp, and a second filament-simulating circuit electrically connected to a second bi-pin terminal of the LED lamp, each of the first and the second bi-pin terminals arranged to have a current flowing from one pin to the other pin of the respective bi-pin terminal via the respective first or second filament-simulating circuit after the LED lamp is connected to a ballast and before a normal operation state of the LED lamp.

43. (Previously Presented) The LED lamp of claim 42, further comprising:

an LED module comprising the at least one LED, wherein the first filament-simulating circuit comprises an impedance element electrically connected between two pins of the first bi-pin terminal, and the second filament-simulating circuit comprises an impedance element electrically connected between two pins of the second bi-pin terminal; and

a second rectifier coupled between the second filament-simulating circuit and the LED module, wherein the second rectifier is electrically connected to the second filament-simulating circuit in parallel and is electrically connected to the LED module in parallel.

REMARKS

This amendment is being filed under 37 C.F.R. 1.312, to correct a claim dependency in order to provide sufficient antecedent basis for claim 20. Claim 20 has been amended to now depend from claim 19. No new matter has been added, and no further search or consideration is believed to be necessary. Therefore, Applicant requests that the Amendment be entered.

If the Examiner wishes to discuss any aspects of this response with Applicant, the Examiner is encouraged to contact Applicant's representative at the telephone number listed below.

In the event any fees are required in connection with this paper, please charge the Deposit Account No. 50-4574.

Respectfully submitted,

Date: June 8, 2017

/Bradley Edelman/

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NOTICE OF ALLOWANCE AND FEE(S) DUE

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EXAMINER

TAN, VIBOL

ART UNIT

PAPER NUMBER

2844

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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15/258,068

09/07/2016

Qifeng Ye

SUP-104A

1056

TITLE OF INVENTION: POWER SOURCE MODULE FOR LED LAMP

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	09/05/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

74712 7590 06/02/2017
Muir Patent Law, PLLC
P.O. Box 1213
9913 Georgetown Pike, Suite 200
Great Falls, VA 22066

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/258,068	09/07/2016	Qifeng Ye	SUP-104A	1056

TITLE OF INVENTION: POWER SOURCE MODULE FOR LED LAMP

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	09/05/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
TAN, VIBOL	2844	315-205000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.	2. For printing on the patent front page, list (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____ (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____ 3 _____
---	---

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.27
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____
Typed or printed name _____ Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/258,068	09/07/2016	Qifeng Ye	SUP-104A	1056
74712	7590	06/02/2017	EXAMINER	
Muir Patent Law, PLLC			TAN, VIBOL	
P.O. Box 1213			ART UNIT	PAPER NUMBER
9913 Georgetown Pike, Suite 200			2844	
Great Falls, VA 22066				

DATE MAILED: 06/02/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/258,068	Applicant(s) YE ET AL.	
	Examiner Vibol Tan	Art Unit 2844	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to td filed 4/24/17.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-43. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. ☒ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☒ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date <u>4/6/17</u> | 6. ☒ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other _____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

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1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Terminal Disclaimer

2. The terminal disclaimer filed on 4/24/17 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of 9,480,109 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Allowable Subject Matter

3. The following is an examiner's statement of reasons for allowance: in combination with other limitations of the claims, the cited prior arts fail to teach or suggest each of the first bi-pin terminal and the second bi-pin terminal configured to allow a current to flow from one pin to the other pin via the filament-simulating circuit during a pre-heat process executed by a ballast, as required by claim 1; the cited prior arts also fail to teach or suggest the filament-simulating circuit comprising at least one resistor connected in parallel to at least one capacitor and configured to simulate a filament of a fluorescent lamp during a pre-heat process executed by a ballast, as required by claim 17; the cited prior arts also fail to teach or suggest a first circuit comprising a first capacitor element electrically connected between two pins of a first bi-pin terminal of the LED lamp, and a second circuit comprising a second capacitor element electrically connected between two pins of a second bi-pin terminal, wherein the first and second circuits are configured to simulate a filament of a fluorescent lamp during a pre-heat process executed by a ballast, as required by claim 21; the cited prior

Art Unit: 2844

arts also fail to teach or suggest each of the first and the second bi-pin terminals having a current flowing from one pin to the other pin of the respective bi-pin terminal via the filament- simulating circuit during a pre-heat process executed by a ballast, as required by claim 23; the cited prior arts also fail to teach or suggest each of the first and the second bi-pin terminals arranged to have a current flowing from one pin to the other pin of the respective bi-pin terminal via the respective first or second filament-simulating circuit during a pre-heat process executed by a ballast, as required by claim 41; and the cited prior arts also fail to teach or suggest each of the first and the second bi-pin terminals arranged to have a current flowing from one pin to the other pin of the respective bi-pin terminal via the respective first or second filament-simulating circuit after the LED lamp is connected to a ballast and before a normal operation state of the LED lamp, as required by claim 42.

4. Claims 1-43 are in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571)272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an

Art Unit: 2844

interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alex Taningco can be reached on (571) 272-8048. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vibol Tan/
Primary Examiner, Art Unit 2844

Notice of References Cited	Application/Control No. 15/258,068		Applicant(s)/Patent Under Reexamination YE ET AL.	
	Examiner Vibol Tan		Art Unit 2844	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-9,629,216 B2	04-2017	Jiang; Tao	H05B33/0845	1/1
*	B	US-9,629,215 B2	04-2017	Xiong; Aiming	H05B33/0845	1/1
*	C	US-9,629,211 B2	04-2017	Xiong; Aiming	H05B33/0815	1/1
*	D	US-9,609,711 B2	03-2017	Jiang; Tao	H05B33/0845	1/1
*	E	US-8,870,415 B2	10-2014	Ivey; John	F21K9/17	362/221
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	191	(current adj limiting adj circuit) same rectifier same filter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/02/04 15:56
S2	34	(current adj limiting adj circuit) same rectifier same filter same lamp	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/02/04 15:56
S3	411	((("201416790") or ("204539571") or ("2009027847") or ("20080247207") or ("7696700") or ("203661367") or ("201995158") or ("204300731") or ("104948958") or ("102196614") or ("102427632") or ("204756542") or ("201416789") or ("1688186") or ("202425117") or ("103428959") or ("204929364") or ("203039947") or ("202857106") or ("202759649") or ("2015179652") or ("203801102") or ("201758472") or ("201414240") or ("202841636") or ("104812149") or ("102147053") or ("102147053") or ("102196627") or ("2884777") or ("2012221948") or ("102905429") or ("201339900") or ("102905429") or ("104968114") or ("203193958") or ("204498418") or ("202353882") or ("202190446") or ("103858521") or ("103858521") or ("20140306614") or ("201887988") or ("9155149") or ("201039522") or ("20110181190") or ("204761794") or ("202941026") or ("2819871") or ("2012129129") or ("201726573") or ("102438378") or ("102438378") or ("102984864") or ("101919315") or ("103179764") or ("102984864") or ("2355618A1") or ("202972697") or ("203023957") or ("202972696") or ("203225926") or ("202979368") or ("201718093") or ("202979420") or ("104968118") or ("204795685") or ("102905442") or ("20070096661") or ("204131808") or ("202634747") or ("2015513177") or ("102905442") or ("202406349") or ("103403439") or ("2010218811") or	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/02/04 16:15

		("7276858") or ("102635804") or ("104206021") or ("204836733U") or ("0822579") or ("2532763") or ("202941025") or ("102792778") or ("20140049171") or ("101437342") or ("102792778") or ("102635804") or ("20120161650") or ("103025014") or ("2014216310") or ("102186282") or ("202634835") or ("102480820") or ("203757484") or ("204408691") or ("202652610") or ("201657412") or ("102480820") or ("101626650") or ("103025014") or ("101437342") or ("9155136") or ("202972844") or ("201409247") or ("102186282") or ("8836229") or ("201585165") or ("201255369") or ("202019481") or ("202425143") or ("201003696") or ("204031554") or ("201590932") or ("201547539") or ("202841630") or ("105208750") or ("2015185378") or ("2432297") or ("203942688") or ("203968454") or ("104661392") or ("104968113") or ("203963646") or ("204145835") or ("102711339") or ("102984851") or ("201657413") or ("2011151010") or ("2842974") or ("104994638") or ("104125680") or ("203590562")).PN. or (("203289708") or ("104968112") or ("204291440") or ("102984851") or ("101626650") or ("101176129") or ("101655216") or ("101176129") or ("20120068606") or ("20100096999") or ("20140152185") or ("202535579") or ("100482015") or ("20130278152") or ("201479418U") or ("103269537") or ("20120074854") or ("20080116816") or ("101677482") or ("204836732") or ("103269537") or ("101711066") or ("101998726") or ("8884533") or ("201210760") or ("8072152") or ("7649322") or ("2013219963") or ("2011258589") or ("201199738")).PN. or (11/307815).APP.				
S5	4	((light adj emitting adj diode) or LED.u/c.) adj lamp) same terminal same (current adj limiting adj circuit) same rectifier same filter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/02/09 11:49
S6	13	((light adj emitting adj diode) or LED.u/c.) adj lamp) same terminal same dim\$4 same rectifier same filter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/02/09 11:53
S7	392	("201416790") or ("204539571") or ("2009027847") or ("20080247207") or ("7696700") or ("203661367") or ("201995158") or ("204300731") or ("104948958") or ("102196614") or	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2016/02/09 12:07

("102427632") or ("204756542") or ("201416789") or ("1688186") or ("202425117") or ("103428959") or ("204929364") or ("203039947") or ("202857106") or ("202759649") or ("2015179652") or ("203801102") or ("201758472") or ("202841636") or ("104812149") or ("102147053") or ("102147053") or ("102196627") or ("2884777Y") or ("2012221948") or ("201339900") or ("102905429") or ("102905429") or ("104968114") or ("203193958") or ("204498418") or ("202353882") or ("202190446") or ("103858521") or ("103858521") or ("201887988") or ("20140306614") or ("9155149") or ("201039522") or ("20110181190") or ("204761794") or ("202941026") or ("2819871") or ("201726573") or ("2012129129") or ("102438378") or ("102438378") or ("102984864") or ("101919315") or ("103179764") or ("102984864") or ("2355618A1") or ("202972697") or ("203023957") or ("202972696") or ("203225926") or ("202979368") or ("201718093") or ("104968118") or ("202979420") or ("204795685") or ("102905442") or ("20070096661") or ("204131808") or ("202634747") or ("2015513177") or ("102905442") or ("202406349") or ("103403439") or ("2010218811") or ("7276858") or ("104206021") or ("204836733") or ("102635804") or ("H822579") or ("202941025") or ("2532763") or ("102792778") or ("20140049171") or ("101437342") or ("102792778") or ("102635804") or ("103025014") or ("20120161650") or ("2014216310") or ("102186282") or ("102480820") or ("202634835") or ("204408691") or ("203757484") or ("202652610") or ("102480820") or ("201657412") or ("101626650") or ("103025014") or ("101437342") or ("9155136") or ("202972844") or ("201409247") or ("102186282") or ("8836229") or ("201585165") or ("201255369") or ("204993953") or ("202019481") or ("201003696") or ("202425143") or ("204031554") or ("201590932") or ("201547539") or ("202841630") or ("105208750") or ("2015185378") or ("203942688") or ("2432297") or ("203968454") or ("104661392") or ("203963646") or ("104968113") or ("204145835") or ("102711339") or ("102984851") or ("201657413") or ("2011151010") or ("2842974") or ("203590562") or ("104994638") or ("203289708")).PN. or ("204291440") or ("104968112") or ("102984851") or ("101176129") or ("101626650") or	DERWENT; IBM_TDB
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		("101655216") or ("101176129") or ("20120068606") or ("100482015") or ("20100096999") or ("20140152185") or ("202535579") or ("201479418") or ("20130278152") or ("103269537") or ("20120074854") or ("20080116816") or ("101677482") or ("204836732") or ("103269537") or ("101711066") or ("101998726") or ("2011258589") or ("8884533") or ("201210760") or ("8072152") or ("7649322")).PN. or ((20/141424) or (10/412568)).APP.				
S8	308	((("9241378") or ("202353882") or ("20150002039") or ("8648542") or ("103874267") or ("20120256551") or ("202353862") or ("2658347") or ("103139963") or ("20130278161") or ("102057751") or ("102057751") or ("204300731") or ("201844248") or ("103428959") or ("102032484") or ("103139963") or ("103052198") or ("203167342") or ("102907177") or ("202425143") or ("104019378") or ("2012221948") or ("20100079076") or ("102573181") or ("201983229") or ("2496056") or ("102523654") or ("2639987") or ("102523654") or ("102032484") or ("103857138") or ("20110025206") or ("201409247") or ("20140239834") or ("101655216") or ("2288235") or ("1249896") or ("8053995") or ("1171509") or ("8415889") or ("204598355") or ("104968114") or ("102376272") or ("20140117851") or ("2298030B1") or ("101655216") or ("103621179") or ("202005010") or ("204408691") or ("102011953") or ("203313480") or ("202143243") or ("203327323") or ("204761794") or ("103619093") or ("201547539") or ("102164440") or ("104582149") or ("201255369") or ("201898649") or ("204131813") or ("2013012488") or ("103460803") or ("103442502") or ("20150312989") or ("201830522") or ("102164440") or ("204305436") or ("204948416") or ("201242075") or ("102176797") or ("2009147563") or ("2009134946") or ("102176797") or ("201846506") or ("2298030") or ("2013066270") or ("201416790") or ("2014235778") or ("202005039") or ("2774457") or ("2015179652") or ("102635804") or ("102818141") or ("101977468") or ("103748961") or ("104378880") or ("2015525440") or ("203176981") or ("102635804") or ("102413599")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/02/09 12:58
S9	97	((("light adj emitting adj diode) or LED.u/c.) adj lamp) same bi-pin	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2016/02/09 13:22

			IBM_TDB			
S10	0	((light adj emitting adj diode) or LED.u/c.) adj lamp) same bi-pin same rectifier same filter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/02/09 13:23
S11	30	((light adj emitting adj diode) or LED.u/c.) adj lamp) and bi-pin and rectifier and filter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/02/09 13:24
S12	95	((light adj emitting adj diode) or LED.u/c.) adj lamp) same (terminal or pin) same ((limiting adj circuit) or capacitor) same rectifier same filter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/02/09 14:02
S13	37	(US-20110181190-\$ or US-20140049171-\$ or US-20130278152-\$ or US-20120161650-\$ or US-20120026761-\$ or US-20110291585-\$ or US-20080247207-\$ or US-20150312989-\$ or US-20140239834-\$ or US-20140117851-\$ or US-20130278161-\$ or US-20120256551-\$ or US-20110025206-\$ or US-20100079076-\$ or US-20150223303-\$ or US-20130221867-\$ or US-20080290814-\$ or US-20070228999-\$ or US-20150351171-\$).did. or (US-5777439-\$ or US-5606224-\$).did. or (WO-2010054523-\$ or EP-2432297-\$ or CA-2532763-\$).did. or (US-20120161650-\$ or CN-202190446-\$ or KR-1040833-\$ or CN-101998726-\$ or CN-201726573-\$ or CN-1688186-\$ or EP-2533607-\$ or US-20120286663-\$ or CN-102711329-\$ or CN-202425143-\$ or DE-102010029100-\$ or US-20110057572-\$).did.	US-PGPUB; USPAT; FPRS; DERWENT	OR	OFF	2016/02/09 16:17
S14	29	S13 AND ((H05B33/0809 OR H05B33/0815 OR H05B33/0803 OR H05B33/0812 OR H05B33/0806 OR H05B33/0884 OR H05B33/0887 OR H05B33/089 OR H05B37/02 OR Y02B20/386 OR Y02B20/40 OR Y02B20/186 OR Y02B20/342 OR Y02B20/346 OR F21K9/17).CPC.)	US-PGPUB; USPAT; FPRS; DERWENT	OR	OFF	2016/02/09 16:20
S15	45302	((H05B33/0809 H05B33/0815 H05B33/0803 H05B33/0812 H05B33/0806 H05B33/0884 H05B33/0887 H05B33/089 H05B37/02 Y02B20/386 Y02B20/40 Y02B20/186 Y02B20/342 Y02B20/346 F21K9/17).CPC.)	US-PGPUB; USPAT; FPRS; DERWENT	OR	OFF	2016/05/23 08:01
S16	45423	((H05B33/0809 H05B33/0815 H05B33/0803 H05B33/0812 H05B33/0806 H05B33/0884 H05B33/0887 H05B33/089 H05B37/02 Y02B20/386 Y02B20/40 Y02B20/186 Y02B20/342 Y02B20/346	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2016/05/23 08:01

		F21K9/17).CPC.)	DERWENT; IBM_TDB			
S17	2	S16 and (filament adj simulating adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:01
S18	3	rectifier and (filament adj simulating adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:05
S19	4	(filament adj simulating adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:06
S20	2	(filament-simulating adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:06
S21	4422	(filament near1 circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:06
S22	688	(filament near1 circuit) same rectifier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:07
S23	163	(filament near1 circuit) same rectifier same (capacitor or capacitance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:07
S24	0	(filament near1 circuit) same rectifier same (capacitor or capacitance) same bi-pin	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:12
S25	2	(filament near1 circuit) same rectifier same bi-pin	US-PGPUB; USPAT; USOCR;	OR	ON	2016/05/23 08:12

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S26	3	(filament near1 circuit) same bi-pin	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:14
S27	1	bi-pin and (filament adj simulating adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:14
S28	38	(US-20110181190-\$ or US-20140049171-\$ or US-20130278152-\$ or US-20120161650-\$ or US-20120026761-\$ or US-20110291585-\$ or US-20080247207-\$ or US-20150312989-\$ or US-20140239834-\$ or US-20140117851-\$ or US-20130278161-\$ or US-20120256551-\$ or US-20110025206-\$ or US-20100079076-\$ or US-20150223303-\$ or US-20130221867-\$ or US-20080290814-\$ or US-20070228999-\$ or US-20150351171-\$ or US-20160091147-\$).did. or (US-5777439-\$ or US-5606224-\$).did. or (WO-2010054523-\$ or EP-2432297-\$ or CA-2532763-\$).did. or (US-20120161650-\$ or CN-202190446-\$ or KR-1040833-\$ or CN-101998726-\$ or CN-201726573-\$ or CN-1688186-\$ or EP-2533607-\$ or US-20120286663-\$ or CN-102711329-\$ or CN-202425143-\$ or DE-102010029100-\$ or US-20110057572-\$).did.	US-PGPUB; USPAT; FPRS; DERWENT	OR	OFF	2016/05/23 10:08
S33	6	("20110057572" "20110121756" "20120299501" "20150173138" "20160081147" "9210744").PN.	US-PGPUB; USPAT	OR	OFF	2016/08/10 15:44
S34	6	("20110057572" "20110121756" "20120299501" "20150173138" "20160081147" "9210744").PN.	US-PGPUB; USPAT	OR	OFF	2016/08/10 15:45
S35	1	("9480109").PN.	USPAT; USOCR	OR	OFF	2017/03/13 12:50
S36	320	((("CHEN") near3 ("Zhong")).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/03/13 15:37
S37	6	((("ZHANG") near3 ("Yueqiang")).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/03/13 15:38
S38	307	((("JIANG") near3 ("Tao")).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/03/13 15:38
S39	13	((("YE") near3 ("Qifeng")).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/03/13 15:38

S40	634	S36 S37 S38 S39	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/03/13 15:39
S41	3	S40 and (bi-pin or bipin)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/13 15:39
S42	24	(filament adj simulating adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 09:15
S43	1090	((H05B33/0809 H05B33/0815 H05B33/0803 H05B33/0812 H05B33/0806 H05B33/0884 H05B33/0887 H05B33/089 H05B37/02 Y02B20/386 Y02B20/40 Y02B20/186 Y02B20/342 Y02B20/346 F21K9/17).CPC.) and (rectifier or rectification or rectifying) and filter\$3 and (current adj limit\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 09:49
S44	64	((H05B33/0809 H05B33/0815 H05B33/0803 H05B33/0812 H05B33/0806 H05B33/0884 H05B33/0887 H05B33/089 H05B37/02 Y02B20/386 Y02B20/40 Y02B20/186 Y02B20/342 Y02B20/346 F21K9/17).CPC.) and (rectifier or rectification or rectifying) and filter\$3 and (current adj limit\$3) and (bipin or bi-pin)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 09:50
S45	31	(filament adj simulating adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/27 09:01
S46	4	(filament adj simulating) and (bi adj pin)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/27 09:18
S47	0	(filament adj simulating) and (bipin)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/27 09:18
S48	4	(filament adj simulating) and (bi-pin)	US-PGPUB; USPAT; USOCR;	OR	ON	2017/04/27 09:18

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S49	28	((H05B33/0809 H05B33/0815 H05B33/0803 H05B33/0812 H05B33/0806 H05B33/0884 H05B33/0887 H05B33/089 H05B37/02 Y02B20/386 Y02B20/40 Y02B20/186 Y02B20/342 Y02B20/346 F21K9/17).CPC.) and (filament adj simulating adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/27 09:35
S50	45	("20100102729" "20160081147" "20150077001" "20140265900" "20120313540" "20120181952" "20150351171" "20110181190" "8648542" "8525427" "20110121756" "20110057572" "20150173138" "20120299501" "9210744" "20130320869" "20110176297" "20100220469" "20120300445" "20150176770" "7380961" "20100096976" "20140239827" "20100181925" "20140035463" "20110149563" "20070127242" "5936599" "8796943" "20160091147" "20160102813" "20160198535" "20160212809" "20160219666" "20160219658" "20160255694" "20160255699" "20160270184" "20160270165" "20160270164" "20160270166" "20160270173" "20160309550" "20160323948" "20160381760").PN.	US-PGPUB; USPAT	OR	OFF	2017/04/27 10:13
S51	6	(bi-pin or (bi adj pin)) same rectifier same filter same (LED.u/c. adj (lamp or module))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/27 10:30
S52	109	(bi-pin or (bi adj pin)) and rectifier and filter and (LED.u/c. adj (lamp or module))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/27 10:33
S53	0	(bi-pin or (bi adj pin)) near5 capacitors near5 resistors	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/27 12:22
S54	2	(bi-pin or (bi adj pin)) near10 capacitors near5 resistors	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/27 12:23
S55	2	(bi-pin or (bi adj pin)) near10 capacitors	US-PGPUB;	OR	ON	2017/04/27

		near10 resistors	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			12:23
S56	25	(bi-pin or (bi adj pin)) and rectifier and filter and (LED.u/c. adj (lamp or module)) and stimul\$5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/27 12:24
S57	3	((bi-pin or bipin) near5 current) same pre-heat	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/28 07:55
S58	15	(bi-pin or bipin) same pre-heat	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/04/28 07:55

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	11	(filament-simulating adj circuit).clm.	US-PGPUB; USPAT	OR	ON	2017/04/28 09:12
S29	1	(bi-pin and (filament adj simulating adj circuit)).clm.	US-PGPUB; USPAT	OR	ON	2016/05/23 10:04
S31	1	(bi-pin and (third adj capacitance)).clm.	US-PGPUB; USPAT	OR	ON	2016/05/23 10:05
S32	1	(bi-pin and (first adj capacitance)).clm.	US-PGPUB; USPAT	OR	ON	2016/05/23 10:05

4/ 28/ 2017 9:14:43 AM
C:\ Users\ vtan\ Documents\ EAST\ Workspaces\ 15258068.wsp

<i>Index of Claims</i> 	Application/Control No. 15258068	Applicant(s)/Patent Under Reexamination YE ET AL.
	Examiner VIBOL TAN	Art Unit 2844

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	04/28/2017								
	1	=								
	2	=								
	3	=								
	4	=								
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	6	=								
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<i>Index of Claims</i> 	Application/Control No. 15258068	Applicant(s)/Patent Under Reexamination YE ET AL.
	Examiner VIBOL TAN	Art Unit 2844

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	04/28/2017								
	37	=								
	38	=								
	39	=								
	40	=								
	41	=								
	42	=								
	43	=								

INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>			Complete if Known		
			<i>Application Number</i>	15/258,068	
			<i>Filing Date</i>	September 7, 2016	
			<i>First Named Inventor</i>	Qifeng Ye	
			<i>Art Unit</i>	2844	
			<i>Examiner Name</i>	Vibol TAN	
Sheet	1	of	3	<i>Attorney Docket Number</i>	SUP-104A (S16090US)

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials	Cite No. ¹	Document Number	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US20100102729	04-29-2010	Katzir	
		US20160081147	03-17-2016	Guang	
		US20150077001	03-19-2015	Takahashi	
		US20140265900	09-18-2014	Sadwick et al.	
		US20120313540	12-13-2012	Lin	
		US20120181952	07-19-2012	Rooer	
		US20150351171	12-03-2015	Tao et al.	
		US20110181190	07-28-2011	Lin et al.	
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		US8525427	12-29-2011	Samoilenko et al.	
		US20160081147	03-17-2016	Luo Hua GUANG	
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		US9210744	10-24-2013	Carmen et al.	
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		US20160081147	03-17-2016	Luo Hua GUANG	
		US20110176297	07-21-2011	Hsia et al.	
		US20100220469	09-02-2010	Ivey et al.	
		US20120300445	11-29-2012	Chu et al.	
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		US7380961	12-16-2004	Hideo Moriyama	
		US20100096976	04-22-2010	Myung Koo Park	
		US20140239827	08-28-2014	Myung Koo PARK	
		US20100181925	07-22-2010	Ivey et al.	
		US20140035463	02-06-2014	MIYAMICHI SABURO	
		US20110149563	06-23-2011	Hsia et al.	
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				<i>Application Number</i>	15/258,068
				<i>Filing Date</i>	September 7, 2016
				<i>First Named Inventor</i>	Qifeng Ye
				<i>Art Unit</i>	2844
				<i>Examiner Name</i>	Vibol TAN
Sheet	2	of	3	<i>Attorney Docket Number</i>	SUP-104A (S16090US)

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				Application Number	15/258,068
				Filing Date	September 7, 2016
				First Named Inventor	Qifeng Ye
				Art Unit	2844
				Examiner Name	Vibol TAN
Sheet	3	of	3	Attorney Docket Number	SUP-104A (S16090US)

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				APPLIANCE CO.	

Note: Submission of copies of U.S. Patents and published U.S. Patent Applications is not required.

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Examiner Signature	/VIBOL TAN/	Date Considered	04/27/2017
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /V.T/

Issue Classification 	Application/Control No. 15258068	Applicant(s)/Patent Under Reexamination YE ET AL.	
	Examiner VIBOL TAN	Art Unit 2844	

CPC						
Symbol					Type	Version
H05B		33	/	0812	F	2013-01-01
H05B		33	/	0809	I	2013-01-01
F21V		23	/	009	I	2013-01-01
F21V		23	/	023	I	2013-01-01
F21K		9	/	27	I	2016-08-01
Y02B		20	/	345	A	2013-01-01
F21K		9	/	278	I	2016-08-01
H05B		33	/	0845	I	2013-01-01
Y02B		20	/	343	A	2013-01-01
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CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 43	
/VIBOL TAN/ Primary Examiner.Art Unit 2844 (Primary Examiner) _____ (Date) _____		O.G. Print Claim(s) 1	O.G. Print Figure 1-2

Issue Classification 	Application/Control No. 15258068	Applicant(s)/Patent Under Reexamination YE ET AL.
	Examiner VIBOL TAN	Art Unit 2844

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17		33										
	2		18		34										
	3		19		35										
	4		20		36										
	5		21		37										
	6		22		38										
	7		23		39										
	8		24		40										
	9		25		41										
	10		26		42										
	11		27		43										
	12		28												
	13		29												
	14		30												
	15		31												
	16		32												

NONE	Total Claims Allowed: 43	
(Assistant Examiner)	(Date)	
/VIBOL TAN/ Primary Examiner.Art Unit 2844	04/28/2017	O.G. Print Claim(s) 1
(Primary Examiner)	(Date)	O.G. Print Figure 1-2

Search Notes 	Application/Control No. 15258068	Applicant(s)/Patent Under Reexamination YE ET AL.
	Examiner VIBOL TAN	Art Unit 2844

CPC- SEARCHED		
Symbol	Date	Examiner
H05B33/0809 H05B33/0815 H05B33/0803 H05B33/0812 H05B33/0806 H05B33/0884 H05B33/0887 H05B33/089 H05B37/02 Y02B20/386 Y02B20/40 Y02B20/186 Y02B20/342 Y02B20/346 F21K9/17 and text	3/14/2017	VTan

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor names search	3/14/2017	VTan
parent application 14/699,138 now US 9,480,109	3/14/2017	VTan
EAST text search	3/14/2017	VTan
EAST text update	4/27/2017	VTan

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
uspgpub & uspat	text	4/28/2017	VTan

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Doc Code: DIST.E.FILE Document Description: Electronic Terminal Disclaimer - Filed		PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce
Electronic Petition Request	TERMINAL DISCLAIMER TO OBIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	
Application Number	15258068	
Filing Date	07-Sep-2016	
First Named Inventor	Qifeng Ye	
Attorney Docket Number	SUP-104A	
Title of Invention	POWER SOURCE MODULE FOR LED LAMP	
☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action ☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.		
Owner	Percent Interest	
JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD.	100%	
The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s) 9480109 as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns. In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later: - expires for failure to pay a maintenance fee; - is held unenforceable; - is found invalid by a court of competent jurisdiction; - is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321; - has all claims canceled by a reexamination certificate; - is reissued; or - is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer. ☒ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.		

☐ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.	
Applicant claims the following fee status: ☐ Small Entity ☐ Micro Entity ☒ Regular Undiscounted	
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.	
THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES I certify, in accordance with 37 CFR 1.4(d)(4) that I am: ☒ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application Registration Number <u>57648</u> ☐ A sole inventor ☐ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application ☐ A joint inventor; all of whom are signing this request	
Signature	/Bradley Edelman/
Name	Bradley Edelman

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
 Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Doc Code: DISQ.E.FILE

Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 15258068

Filing Date: 07-Sep-2016

Applicant/Patent under Reexamination: Ye

Electronic Terminal Disclaimer filed on April 24, 2017

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Ye et al.	Attorney Docket:	SUP-104A
Serial Number:	15/258,068	Group Art Unit:	2844
Filed:	September 7, 2016	Examiner:	Vibol TAN
Confirmation Number:	1056		

Title: POWER SOURCE MODULE FOR LED TUBE LAMP

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir/Madam:

This amendment is filed in response to the Office Action of March 20, 2017.

Amendments to the claims begin on page 2 of this paper.

Remarks follow the amendment section of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims, in the application:

We Claim:

1. (Currently Amended) A power source module for an LED lamp, comprising:

a filament-simulating circuit electrically connected to a first bi-pin terminal and a second bi-pin terminal of the LED lamp, each of the first bi-pin terminal and the second bi-pin terminal configured to allow a current to flow from one pin to the other pin via the filament-simulating circuit during a pre-heat process executed by a ballast;

a current limiting circuit electrically connected to the filament-simulating circuit and configured to limit a current from the filament-simulating circuit;

a first rectifier electrically connected to the current limiting circuit and configured to rectify the current from the current limiting circuit; and

a filter electrically connected between the first rectifier and at least one LED of the LED lamp and configured to smooth the current from the first rectifier.

2. (Original) The power source module of claim 1, wherein the filament-simulating circuit comprises:

a first filament-simulating circuit comprising a first capacitor element electrically connected between two pins of the first bi-pin terminal; and

a second filament-simulating circuit comprising a second capacitor element electrically connected between two pins of the second bi-pin terminal.

3. (Original) The power source module of claim 2, wherein:

the first filament-simulating circuit further comprises a first pair of resistors electrically connected in series, the first capacitor element comprises a first pair of capacitors electrically connected in series, the first pair of resistors and the first pair of capacitors electrically connected in parallel between two pins of the first bi-pin terminal, and a connection point between the first pair of resistors being electrically connected to a connection point between the first pair of capacitors; and

the second filament-simulating circuit further comprises a second pair of resistors electrically connected in series, the second capacitor element comprises a second pair of

capacitors electrically connected in series, the second pair of resistors and the second pair of capacitors electrically connected in parallel between two pins of the second bi-pin terminal, and a connection point between the second pair of resistors being electrically connected to a connection point between the second pair of capacitors.

4. (Original) The power source module of claim 3, wherein an impedance of the first pair of resistors is ten times more than that of the first pair of capacitors, and an impedance of the second pair of resistors is ten times more than that of the second pair of capacitors.

5. (Currently Amended) The power source module of claim 2, wherein the first rectifier comprises two diodes electrically connected in series, and the first rectifier is electrically connected to the first filament-simulating circuit in ~~parallel~~series.

6. (Original) The power source module of claim 2, wherein the first rectifier comprises two diodes electrically connected in series and a connection node connecting the two diodes is coupled to the current limiting circuit, wherein a current flows from the at least one LED to one pin of the first bi-pin terminal through one of the two diodes and the current limiting

circuit, or from one pin of the first bi-pin terminal to the at least one LED through the other of the two diodes and the current limiting circuit.

7. (Original) The power source module of claim 6, wherein the current limiting circuit comprises at least a capacitor.

8. (Original) The power source module of claim 5, further comprising a second rectifier, wherein the second rectifier is a bridge rectifier electrically connected to the second filament-simulating circuit in parallel.

9. (Original) The power source module of claim 1, wherein the power source module is configured inside a casing of the LED lamp.

10. (Original) The power source module of claim 1, further comprising a discharging circuit electrically connected to the filter in parallel for discharging the filter.

11. (Currently Amended) The power source module of claim 1, wherein the current limiting circuit comprises:

a first capacitor, one end of the first capacitor being electrically connected to one pin of the first bi-pin terminal; and

a second capacitor, one end of the second capacitor being electrically connected to the other pin of the first bi-pin terminal, and the other end of the second capacitor being electrically connected to the other end of the first capacitor and the first rectifier.

12. (Original) The power source module of claim 11, wherein the current limiting circuit further comprises:

a third capacitor, one end of the third capacitor being electrically connected to the other ends of the first capacitor and the second capacitor, and the other end of the third capacitor being electrically connected to the first rectifier.

13. (Original) The power source module of claim 11, wherein the first rectifier comprises two diodes electrically connected in series and the connection node of the two diodes is electrically connected to the other ends of the first and second capacitor.

14. (Original) The power source module of claim 11, further comprising a discharging circuit electrically connected to the filter in parallel for discharging the filter.

15. (Original) The power source module of claim 1, wherein the filter comprises a filtering capacitor electrically connected to the at least one LED.

16. (Original) The power source module of claim 1, further comprising a discharging circuit electrically connected to the filter in parallel for discharging the filter.

17. (Currently Amended) A power source module for an LED lamp, comprising:

a rectifier electrically connected to terminals of the LED lamp and configured to receive a current;

a filter electrically connected between the rectifier and at least one LED of the LED lamp and configured to store energy from the rectifier and to smooth the current from the rectifier;

a discharging circuit electrically connected to the filter in parallel and configured to discharge the energy stored in the filter; and

a filament-simulating circuit electrically connected to a first bi-pin terminal and a second bi-pin terminal of the LED lamp, the filament-simulating circuit comprising at least one resistor connected in parallel to at least one capacitor and configured to simulate a filament of a fluorescent lamp during a pre-heat process executed by a ballast.

18. (Currently Amended) The power source module of claim 17, further comprising a current limiting circuit electrically connected to the first bi-pin terminal of the LED lamp, and configured to limit a current from the first bi-pin terminal.

19. (Original) The power source module of claim 18, wherein the current limiting circuit comprises:

a first capacitor, one end of the first capacitor being electrically connected to one pin of the first bi-pin terminal; and

a second capacitor, one end of the second capacitor being electrically connected to the other pin of the first bi-pin terminal, and the other end of the second capacitor being electrically connected to the other end of the first capacitor and the rectifier.

20. (Original) The power source module of claim 18, wherein the current limiting circuit further comprises:

a third capacitor, one end of the third capacitor being electrically connected to the other ends of the first capacitor and the second capacitor, and the other end of the third capacitor being electrically connected to the rectifier.

21. (Currently Amended) A power source module for an LED lamp, comprising:

a first circuit comprising a first capacitor element electrically connected between two pins of a first bi-pin terminal of the LED lamp, and a second circuit comprising a second capacitor element electrically connected between two pins of a second bi-pin terminal, wherein the first and second circuits are configured to simulate a filament of a fluorescent lamp during a pre-heat process executed by a ballast;

a current limiting circuit electrically connected to the first bi-pin terminal and configured to limit a current from the first bi-pin terminal;

a rectifier electrically connected between the current limiting circuit and the second circuit and configured to rectify the current from the current limiting circuit and a current from the second bi-pin terminal; and

a filter electrically connected between the rectifier and at least one LED of the LED lamp to store energy from the rectifier and configured to smooth the current from the rectifier.

22. (Original) The power source module of claim 21, wherein:

the first circuit further comprises a first pair of resistors electrically connected in series, the first capacitor element comprises a first pair of capacitors electrically connected in series, the first pair of resistors and the first pair of capacitors electrically connected in parallel between two pins of the first bi-pin terminal, and a connection point between the first pair of resistors being electrically connected to a connection point between the first pair of capacitors; and

the second circuit further comprises a second pair of resistors electrically connected in series, the second capacitor element comprises a second pair of capacitors electrically connected in series, the second pair of resistors and the second pair of capacitors electrically connected in parallel between two pins of the second bi-pin terminal, and a connection point between the

second pair of resistors being electrically connected to a connection point between the second pair of capacitors.

23. (Currently Amended) An LED lamp, comprising:

a current limiting circuit electrically connected to a first terminal of the LED lamp for limiting a current from the first terminal;

a first rectifier electrically connected to the current limiting circuit for rectifying the current from the current limiting circuit;

a filter electrically connected between the first rectifier and at least one LED of the LED lamp for smoothing the current from the first rectifier; and

a filament-simulating circuit electrically connected to a first bi-pin terminal and a second bi-pin terminal of the LED lamp, each of the first and the second bi-pin terminals having a current flowing from one pin to the other pin of the respective bi-pin terminal via the filament-simulating circuit during a pre-heat process executed by a ballast.

24. (Original) The LED lamp of claim 23, wherein the filament-simulating circuit comprises:

a first filament-simulating circuit comprising a first capacitor element electrically connected between two pins of the first bi-pin terminal; and

a second filament-simulating circuit comprising a second capacitor element electrically connected between two pins of the second bi-pin terminal.

25. (Original) The LED lamp of claim 24, wherein:

the first filament-simulating circuit further comprises a first pair of resistors electrically connected in series, the first capacitor element comprises a first pair of capacitors electrically connected in series, the first pair of resistors and the first pair of capacitors electrically connected in parallel between two pins of the first bi-pin terminal, and a connection point between the first pair of resistors being electrically connected to a connection point between the first pair of capacitors; and

the second filament-simulating circuit further comprises a second pair of resistors electrically connected in series, the second capacitor element comprises a second pair of

capacitors electrically connected in series, the second pair of resistors and the second pair of capacitors electrically connected in parallel between two pins of the second bi-pin terminal, and a connection point between the second pair of resistors being electrically connected to a connection point between the second pair of capacitors.

26. (Original) The LED lamp of claim 23, wherein the current limiting circuit comprises:

a first capacitor, one end of the first capacitor being electrically connected to one pin of the first terminal; and

a second capacitor, one end of the second capacitor being electrically connected to the other pin of the first terminal, and the other end of the second capacitor being electrically connected to the other end of the first capacitor and the first rectifier.

27. (Original) The LED lamp of claim 26, wherein the current limiting circuit further comprises:

a third capacitor, one end of the third capacitor being electrically connected to the other ends of the first capacitor and the second capacitor, and the other end of the third capacitor being electrically connected to the first rectifier.

28. (Original) The LED lamp of claim 26, wherein the first rectifier comprises two diodes electrically connected in series and the connection node of the two diodes is electrically connected to the other ends of the first and second capacitor.

29. (Original) The LED lamp of claim 23, further comprising a discharging circuit electrically connected to the filter in parallel for discharging the filter.

30. (Original) The LED lamp of claim 24, wherein the first rectifier comprises two diodes electrically connected in series, and the first rectifier is electrically connected to the first filament-simulating circuit in parallel.

31. (New) The power source module of claim 1, wherein the current limiting circuit comprises at least a capacitor.

32. (New) The power source module of claim 1, wherein:

the filament-simulating circuit comprises a first filament-simulating circuit connected between two pins of the first bi-pin terminal, and a second filament-simulating circuit connected between two pins of the second bi-pin terminal; and

the current limiting circuit comprises at least a capacitor connected to the first filament-simulating circuit, and at least a capacitor connected to the second filament-simulating circuit.

33. (New) The power source module of claim 1, wherein:

the LED lamp comprises an LED module comprising the at least one LED;

the filament-simulating circuit comprises a first filament-simulating circuit comprising an impedance element electrically connected between two pins of the first bi-pin terminal, and a second filament-simulating circuit comprising an impedance element electrically connected between two pins of the second bi-pin terminal; and

the power source module further comprises a second rectifier coupled between the second filament-simulating circuit and the LED module, wherein the second rectifier is electrically

connected to the second filament-simulating circuit in parallel and is electrically connected to the LED module in parallel.

34. (New) The power source module of claim 17, further comprising a current limiting circuit electrically connected to the second bi-pin terminal of the LED lamp, and configured to limit a current from the second bi-pin terminal.

35. (New) The power source module of claim 17, wherein the filament-simulating circuit comprises a first filament-simulating circuit connected between two pins of the first bi-pin terminal, and a second filament-simulating circuit connected between two pins of the second bi-pin terminal.

36. (New) The power source module of claim 21, further comprising another current limiting circuit electrically connected to the second bi-pin terminal of the LED lamp, configured to limit a current from the second bi-pin terminal.

37. (New) The LED lamp of claim 23, further comprising another current limiting circuit electrically connected to a second terminal of the LED lamp, configured to limit a current from the second terminal.

38. (New) The LED lamp of claim 23, wherein the current limiting circuit comprises at least a capacitor.

39. (New) The LED lamp of claim 23, wherein the filament-simulating circuit comprises a first filament-simulating circuit connected between a first pin and a second pin of the first bi-pin terminal, and a second filament-simulating circuit connected between a first pin and a second pin of the second bi-pin terminal.

40. (New) The LED lamp of claim 23, further comprising:

an LED module comprising the at least one LED, wherein the filament-simulating circuit comprises a first filament-simulating circuit comprising an impedance element electrically connected between two pins of the first bi-pin terminal, and a second filament-simulating circuit

comprising an impedance element electrically connected between two pins of the second bi-pin terminal; and

a second rectifier coupled between the second filament-simulating circuit and the LED module, wherein the second rectifier is electrically connected to the second filament-simulating circuit in parallel and is electrically connected to the LED module in parallel.

41. (New) An LED lamp, comprising:

a current limiting circuit electrically connected to a first terminal of the LED lamp for limiting a current from the first terminal;

a first rectifier electrically connected to the current limiting circuit for rectifying the current from the current limiting circuit;

a filter electrically connected between the first rectifier and at least one LED of the LED lamp for smoothing the current from the first rectifier; and

a first filament-simulating circuit electrically connected to a first bi-pin terminal of the LED lamp and a second filament-simulating circuit electrically connected to a second bi-pin terminal of the LED lamp, each of the first and the second bi-pin terminals arranged to have a

current flowing from one pin to the other pin of the respective bi-pin terminal via the respective first or second filament-simulating circuit during a pre-heat process executed by a ballast.

42. (New) An LED lamp, comprising:

a current limiting circuit electrically connected to a first terminal of the LED lamp for limiting a current from the first terminal;

a first rectifier electrically connected to the current limiting circuit for rectifying the current from the current limiting circuit;

a filter electrically connected between the first rectifier and at least one LED of the LED lamp for smoothing the current from the first rectifier; and

a first filament-simulating circuit electrically connected to a first bi-pin terminal of the LED lamp, and a second filament-simulating circuit electrically connected to a second bi-pin terminal of the LED lamp, each of the first and the second bi-pin terminals arranged to have a current flowing from one pin to the other pin of the respective bi-pin terminal via the respective first or second filament-simulating circuit after the LED lamp is connected to a ballast and before a normal operation state of the LED lamp.

43. (New) The LED lamp of claim 42, further comprising:

an LED module comprising the at least one LED, wherein the first filament-simulating circuit comprises an impedance element electrically connected between two pins of the first bi-pin terminal, and the second filament-simulating circuit comprises an impedance element electrically connected between two pins of the second bi-pin terminal; and

a second rectifier coupled between the second filament-simulating circuit and the LED module, wherein the second rectifier is electrically connected to the second filament-simulating circuit in parallel and is electrically connected to the LED module in parallel.

REMARKS

In the Non-Final Office Action of March 20, 2017, claims 1-10, 17-19, 21-25, and 29 were rejected under non-statutory type double patenting in view of U.S. 9,480,109 (the '109 patent), and claims 11-16, 20, 26-28, and 30 were objected to as depending from rejected claims.

Applicant agrees that at least claims 1-4 of the present application are properly rejected under the doctrine of obviousness-type double patenting as broader claims than the combined claims 4-7 of the '109 patent. The rejection of claims 6 and 7 in view of '109 claims 9 and 10 appear proper as well under this same doctrine. Similarly, the rejections of claims 9 and 10 appear proper in view of '109 claims 13 and 14, and the rejections of claims 23-25 and 29 appear proper in view of claims 4-6 and 14 of the '109 patent.

However, claim 5 has been amended and claim 8 depends from claim 5, and these claims are not believed to be subject to double patenting.

In addition, Applicant does not agree that claims 17-19 of this application are properly rejected in view of claim 14 of the '109 patent, as claim 14 does not include the same features as claims 17-19 of this application, contrary to the statements and explanation in the Office Action.

Furthermore, Applicant does not agree that claims 21 and 22 of this application are properly rejected in view of claims 4-6 of the '109 patent, as claim 6 (which depends from claims 5 and 4) does not include the same features as claims 21 (or claim 22) of this application, contrary to the statements and explanation in the Office Action.

To overcome the aspects of the double patenting rejection believed to be proper, Applicant hereby submits a terminal disclaimer. In addition, a few of the original claims have been slightly amended to address formality issues. Original claims 1-30 are believed to be in condition for allowance at this time.

In addition, Applicant has added new dependent claims 31-40, which are believed to be in condition for allowance as well.

Furthermore, Applicant has added new independent claims 41 and 42, and dependent claim 43, which are each believed to be allowable.

CONCLUSION

Applicant respectfully requests that claims 1-43 be allowed at this time.

If the Examiner wishes to discuss any aspects of this response with Applicant, the Examiner is encouraged to contact Applicant's representative at the telephone number listed below.

An extra claim fee for two (2) additional independent claims and thirteen (13) additional total claims is being submitted herewith. In the event any additional fees are required in connection with this paper, please charge the Deposit Account No. 50-4574.

Respectfully submitted,

Date: April 24, 2017

/Bradley Edelman/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/258,068	09/07/2016	Qifeng Ye	SUP-104A	1056
74712	7590	03/20/2017	EXAMINER	
Muir Patent Law, PLLC			TAN, VIBOL	
P.O. Box 1213			ART UNIT	PAPER NUMBER
9913 Georgetown Pike, Suite 200			2844	
Great Falls, VA 22066			NOTIFICATION DATE	DELIVERY MODE
			03/20/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

cofficeaction@appcoll.com
pto@muirpatentlaw.com

Office Action Summary	Application No. 15/258,068	Applicant(s) YE ET AL.	
	Examiner Vibol Tan	Art Unit 2844	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 9/7/16.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-30 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-10, 17-19, 21-25 and 29 is/are rejected.
- 8) ☒ Claim(s) 11-16, 20, 26-28 and 30 is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☒ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____. | 4) ☐ Other: ____. |

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file

provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

3. Claims 1-10, 17-19, 21-25 and 29 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 4-11, 13 and 14 of U.S. Patent No. 9,480,109. Although the claims at issue are not identical, they are not patentably distinct from each other because they essentially require the same claimed features.

Current Application	U. S. PAT. 9,480,109
Claims 1-10	Claims 4-11, 13 and 14
Claims 17-19	Claim 14
Claims 21 and 22	Claims 4 and 6
Claims 23-25 and 29	Claims 4-6 and 14

In claim 1 of current application, patented claim 4 teaches a power source module for an LED lamp (col. 6, line 60), comprising:

a filament-simulating circuit electrically connected to a first bi-pin terminal and a second bi-pin terminal of the LED lamp, each of the first bi-pin terminal and the second bi-pin terminal configured to allow a current to flow from one pin to the other pin via the filament-simulating circuit during a pre-heat process executed by a ballast (col. 7, lines 12-18);

a current limiting circuit electrically connected to the filament-simulating circuit configured to limit a current from the filament-simulating circuit (col. 6, lines 61-63);

a first rectifier electrically connected to the current limiting circuit configured to rectify the current from the current limiting circuit (col. 7, lines 6-8); and

a filter electrically connected between the first rectifier and at least one LED of the LED lamp configured to smooth the current from the first rectifier (col. 7; lines 9-11).

In claim 17 of current application, patented claim 14 which depends from claim 4 teaches a power source module for an LED lamp (col. 6, line 60), comprising:

a rectifier electrically connected to terminals of the LED lamp configured to receive a current (col. 7, lines 6-8);

a filter electrically connected between the rectifier and at least one LED of the LED lamp configured to store energy from the rectifier and to smooth the current from the rectifier (col. 7; lines 9-11);

a discharging circuit electrically connected to the filter in parallel configured to discharge the energy stored in the filter (col. 8, lines 14-15); and

a filament-simulating circuit electrically connected to a first bi-pin terminal and a second bi-pin terminal of the LED lamp, the filament-simulating circuit comprising at least one resistor connected in parallel to at least one capacitor and configured to simulate a filament of a fluorescent lamp during a pre-heat process executed by a ballast (col. 7, lines 12-18).

In claim 21 of current application, patented claim 4 teaches a power source module for an LED lamp (col. 6, line 60), comprising:

a first circuit comprising a first capacitor element electrically connected between two pins of a first bi-pin terminal of the LED lamp, and a second circuit comprising a second capacitor element electrically connected between two pins of a second bi-pin terminal, wherein the first and second circuits are configured to simulate a filament of a fluorescent lamp during a pre-heat process executed by a ballast (col. 7, lines 12-18);

a current limiting circuit electrically connected to the first bi-pin terminal configured to limit a current from the first bi-pin terminal (col. 6, lines 61-63);

a rectifier electrically connected between the current limiting circuit and the second circuit configured to rectify the current from the current limiting circuit and a current from the second bi-pin terminal (col. 7, lines 6-8); and

a filter electrically connected between the rectifier and at least one LED of the LED lamp to store energy from the rectifier configured to smooth the current from the rectifier (col. 7; lines 9-11).

In claim 23 of current application, patented claim 4 teaches an LED lamp (col. 6, line 60), comprising:

a current limiting circuit electrically connected to a first terminal of the LED lamp for limiting a current from the terminal (col. 6, lines 61-63);

a first rectifier electrically connected to the current limiting circuit for rectifying the current from the current limiting circuit (col. 7, lines 6-8);

a filter electrically connected between the first rectifier and at least one LED of the LED lamp for smoothing the current from the first rectifier (col. 7; lines 9-11); and

a filament-simulating circuit electrically connected to a first bi-pin terminal and a second bi-pin terminal of the LED lamp, each of the first and the second bi-pin terminals having a current flowing from one pin to the other pin of the respective bi-pin terminal via the filament-simulating circuit during a pre-heat process executed by a ballast (col. 7; lines 9-11).

Allowable Subject Matter

4. Claims 11-16, 20, 26-28 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Examiner's Remarks

Only the independent claims 1, 17, 21 and 23 have been mapped out to show the claimed features are the same as required in the patented claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571)272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alex Taningco can be reached on (571) 272-8048. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vibol Tan/
Primary Examiner, Art Unit 2844

Notice of References Cited	Application/Control No. 15/258,068		Applicant(s)/Patent Under Reexamination YE ET AL.	
	Examiner Vibol Tan		Art Unit 2844	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-9,445,463 B2	09-2016	Choi; Jaeyoung	H05B33/0815	1/1
*	B	US-9,526,133 B2	12-2016	Tao; Haimin	H05B37/02	1/1
*	C	US-8,896,207 B2	11-2014	Thomas; James	H05B33/0809	315/185R
*	D	US-8,729,809 B2	05-2014	Kit; John	H05B33/0809	315/185R
*	E	US-7,067,992 B2	06-2006	Leong; Susan J.	F21K9/00	315/291
*	F	US-6,853,151 B2	02-2005	Leong; Susan J.	H05B33/0803	315/185R
*	G	US-6,762,562 B2	07-2004	Leong; Susan J.	F21K9/00	315/51
*	H	US-2014/0239834 A1	08-2014	Choi; Jaeyoung	H05B33/0809	315/205
*	I	US-2016/0316533 A1	10-2016	Hsia; Chungho	F21V25/04	1/1
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	191	(current adj limiting adj circuit) same rectifier same filter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/02/04 15:56
S2	34	(current adj limiting adj circuit) same rectifier same filter same lamp	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/02/04 15:56
S3	411	((("201416790") or ("204539571") or ("2009027847") or ("20080247207") or ("7696700") or ("203661367") or ("201995158") or ("204300731") or ("104948958") or ("102196614") or ("102427632") or ("204756542") or ("201416789") or ("1688186") or ("202425117") or ("103428959") or ("204929364") or ("203039947") or ("202857106") or ("202759649") or ("2015179652") or ("203801102") or ("201758472") or ("201414240") or ("202841636") or ("104812149") or ("102147053") or ("102147053") or ("102196627") or ("2884777") or ("2012221948") or ("102905429") or ("201339900") or ("102905429") or ("104968114") or ("203193958") or ("204498418") or ("202353882") or ("202190446") or ("103858521") or ("103858521") or ("20140306614") or ("201887988") or ("9155149") or ("201039522") or ("20110181190") or ("204761794") or ("202941026") or ("2819871") or ("2012129129") or ("201726573") or ("102438378") or ("102438378") or ("102984864") or ("101919315") or ("103179764") or ("102984864") or ("2355618A1") or ("202972697") or ("203023957") or ("202972696") or ("203225926") or ("202979368") or ("201718093") or ("202979420") or ("104968118") or ("204795685") or ("102905442") or ("20070096661") or ("204131808") or ("202634747") or ("2015513177") or ("102905442") or ("202406349") or ("103403439") or ("2010218811") or	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/02/04 16:15

		("7276858") or ("102635804") or ("104206021") or ("204836733U") or ("0822579") or ("2532763") or ("202941025") or ("102792778") or ("20140049171") or ("101437342") or ("102792778") or ("102635804") or ("20120161650") or ("103025014") or ("2014216310") or ("102186282") or ("202634835") or ("102480820") or ("203757484") or ("204408691") or ("202652610") or ("201657412") or ("102480820") or ("101626650") or ("103025014") or ("101437342") or ("9155136") or ("202972844") or ("201409247") or ("102186282") or ("8836229") or ("201585165") or ("201255369") or ("202019481") or ("202425143") or ("201003696") or ("204031554") or ("201590932") or ("201547539") or ("202841630") or ("105208750") or ("2015185378") or ("2432297") or ("203942688") or ("203968454") or ("104661392") or ("104968113") or ("203963646") or ("204145835") or ("102711339") or ("102984851") or ("201657413") or ("2011151010") or ("2842974") or ("104994638") or ("104125680") or ("203590562")).PN. or (("203289708") or ("104968112") or ("204291440") or ("102984851") or ("101626650") or ("101176129") or ("101655216") or ("101176129") or ("20120068606") or ("20100096999") or ("20140152185") or ("202535579") or ("100482015") or ("20130278152") or ("201479418U") or ("103269537") or ("20120074854") or ("20080116816") or ("101677482") or ("204836732") or ("103269537") or ("101711066") or ("101998726") or ("8884533") or ("201210760") or ("8072152") or ("7649322") or ("2013219963") or ("2011258589") or ("201199738")).PN. or (11/307815).APP.				
S5	4	((light adj emitting adj diode) or LED.u/c.) adj lamp) same terminal same (current adj limiting adj circuit) same rectifier same filter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/02/09 11:49
S6	13	((light adj emitting adj diode) or LED.u/c.) adj lamp) same terminal same dim\$4 same rectifier same filter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/02/09 11:53
S7	392	("201416790") or ("204539571") or ("2009027847") or ("20080247207") or ("7696700") or ("203661367") or ("201995158") or ("204300731") or ("104948958") or ("102196614") or	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2016/02/09 12:07

("102427632") or ("204756542") or ("201416789") or ("1688186") or ("202425117") or ("103428959") or ("204929364") or ("203039947") or ("202857106") or ("202759649") or ("2015179652") or ("203801102") or ("201758472") or ("202841636") or ("104812149") or ("102147053") or ("102147053") or ("102196627") or ("2884777Y") or ("2012221948") or ("201339900") or ("102905429") or ("102905429") or ("104968114") or ("203193958") or ("204498418") or ("202353882") or ("202190446") or ("103858521") or ("103858521") or ("201887988") or ("20140306614") or ("9155149") or ("201039522") or ("20110181190") or ("204761794") or ("202941026") or ("2819871") or ("201726573") or ("2012129129") or ("102438378") or ("102438378") or ("102984864") or ("101919315") or ("103179764") or ("102984864") or ("2355618A1") or ("202972697") or ("203023957") or ("202972696") or ("203225926") or ("202979368") or ("201718093") or ("104968118") or ("202979420") or ("204795685") or ("102905442") or ("20070096661") or ("204131808") or ("202634747") or ("2015513177") or ("102905442") or ("202406349") or ("103403439") or ("2010218811") or ("7276858") or ("104206021") or ("204836733") or ("102635804") or ("H822579") or ("202941025") or ("2532763") or ("102792778") or ("20140049171") or ("101437342") or ("102792778") or ("102635804") or ("103025014") or ("20120161650") or ("2014216310") or ("102186282") or ("102480820") or ("202634835") or ("204408691") or ("203757484") or ("202652610") or ("102480820") or ("201657412") or ("101626650") or ("103025014") or ("101437342") or ("9155136") or ("202972844") or ("201409247") or ("102186282") or ("8836229") or ("201585165") or ("201255369") or ("204993953") or ("202019481") or ("201003696") or ("202425143") or ("204031554") or ("201590932") or ("201547539") or ("202841630") or ("105208750") or ("2015185378") or ("203942688") or ("2432297") or ("203968454") or ("104661392") or ("203963646") or ("104968113") or ("204145835") or ("102711339") or ("102984851") or ("201657413") or ("2011151010") or ("2842974") or ("203590562") or ("104994638") or ("203289708")).PN. or ("204291440") or ("104968112") or ("102984851") or ("101176129") or ("101626650") or	DERWENT; IBM_TDB
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		("101655216") or ("101176129") or ("20120068606") or ("100482015") or ("20100096999") or ("20140152185") or ("202535579") or ("201479418") or ("20130278152") or ("103269537") or ("20120074854") or ("20080116816") or ("101677482") or ("204836732") or ("103269537") or ("101711066") or ("101998726") or ("2011258589") or ("8884533") or ("201210760") or ("8072152") or ("7649322")).PN. or ((20/141424) or (10/412568)).APP.				
S8	308	((("9241378") or ("202353882") or ("20150002039") or ("8648542") or ("103874267") or ("20120256551") or ("202353862") or ("2658347") or ("103139963") or ("20130278161") or ("102057751") or ("102057751") or ("204300731") or ("201844248") or ("103428959") or ("102032484") or ("103139963") or ("103052198") or ("203167342") or ("102907177") or ("202425143") or ("104019378") or ("2012221948") or ("20100079076") or ("102573181") or ("201983229") or ("2496056") or ("102523654") or ("2639987") or ("102523654") or ("102032484") or ("103857138") or ("20110025206") or ("201409247") or ("20140239834") or ("101655216") or ("2288235") or ("1249896") or ("8053995") or ("1171509") or ("8415889") or ("204598355") or ("104968114") or ("102376272") or ("20140117851") or ("2298030B1") or ("101655216") or ("103621179") or ("202005010") or ("204408691") or ("102011953") or ("203313480") or ("202143243") or ("203327323") or ("204761794") or ("103619093") or ("201547539") or ("102164440") or ("104582149") or ("201255369") or ("201898649") or ("204131813") or ("2013012488") or ("103460803") or ("103442502") or ("20150312989") or ("201830522") or ("102164440") or ("204305436") or ("204948416") or ("201242075") or ("102176797") or ("2009147563") or ("2009134946") or ("102176797") or ("201846506") or ("2298030") or ("2013066270") or ("201416790") or ("2014235778") or ("202005039") or ("2774457") or ("2015179652") or ("102635804") or ("102818141") or ("101977468") or ("103748961") or ("104378880") or ("2015525440") or ("203176981") or ("102635804") or ("102413599")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/02/09 12:58
S9	97	((("light adj emitting adj diode) or LED.u/c.) adj lamp) same bi-pin	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2016/02/09 13:22

			IBM_TDB			
S10	0	((light adj emitting adj diode) or LED.u/c.) adj lamp) same bi-pin same rectifier same filter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/02/09 13:23
S11	30	((light adj emitting adj diode) or LED.u/c.) adj lamp) and bi-pin and rectifier and filter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/02/09 13:24
S12	95	((light adj emitting adj diode) or LED.u/c.) adj lamp) same (terminal or pin) same ((limiting adj circuit) or capacitor) same rectifier same filter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/02/09 14:02
S13	37	(US-20110181190-\$ or US-20140049171-\$ or US-20130278152-\$ or US-20120161650-\$ or US-20120026761-\$ or US-20110291585-\$ or US-20080247207-\$ or US-20150312989-\$ or US-20140239834-\$ or US-20140117851-\$ or US-20130278161-\$ or US-20120256551-\$ or US-20110025206-\$ or US-20100079076-\$ or US-20150223303-\$ or US-20130221867-\$ or US-20080290814-\$ or US-20070228999-\$ or US-20150351171-\$.did. or (US-5777439-\$ or US-5606224-\$.did. or (WO-2010054523-\$ or EP-2432297-\$ or CA-2532763-\$.did. or (US-20120161650-\$ or CN-202190446-\$ or KR-1040833-\$ or CN-101998726-\$ or CN-201726573-\$ or CN-1688186-\$ or EP-2533607-\$ or US-20120286663-\$ or CN-102711329-\$ or CN-202425143-\$ or DE-102010029100-\$ or US-20110057572-\$.did.	US-PGPUB; USPAT; FPRS; DERWENT	OR	OFF	2016/02/09 16:17
S14	29	S13 AND ((H05B33/0809 OR H05B33/0815 OR H05B33/0803 OR H05B33/0812 OR H05B33/0806 OR H05B33/0884 OR H05B33/0887 OR H05B33/089 OR H05B37/02 OR Y02B20/386 OR Y02B20/40 OR Y02B20/186 OR Y02B20/342 OR Y02B20/346 OR F21K9/17).CPC.)	US-PGPUB; USPAT; FPRS; DERWENT	OR	OFF	2016/02/09 16:20
S15	45302	((H05B33/0809 H05B33/0815 H05B33/0803 H05B33/0812 H05B33/0806 H05B33/0884 H05B33/0887 H05B33/089 H05B37/02 Y02B20/386 Y02B20/40 Y02B20/186 Y02B20/342 Y02B20/346 F21K9/17).CPC.)	US-PGPUB; USPAT; FPRS; DERWENT	OR	OFF	2016/05/23 08:01
S16	45423	((H05B33/0809 H05B33/0815 H05B33/0803 H05B33/0812 H05B33/0806 H05B33/0884 H05B33/0887 H05B33/089 H05B37/02 Y02B20/386 Y02B20/40 Y02B20/186 Y02B20/342 Y02B20/346	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2016/05/23 08:01

		F21K9/17).CPC.)	DERWENT; IBM_TDB			
S17	2	S16 and (filament adj simulating adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:01
S18	3	rectifier and (filament adj simulating adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:05
S19	4	(filament adj simulating adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:06
S20	2	(filament-simulating adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:06
S21	4422	(filament near1 circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:06
S22	688	(filament near1 circuit) same rectifier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:07
S23	163	(filament near1 circuit) same rectifier same (capacitor or capacitance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:07
S24	0	(filament near1 circuit) same rectifier same (capacitor or capacitance) same bi-pin	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:12
S25	2	(filament near1 circuit) same rectifier same bi-pin	US-PGPUB; USPAT; USOCR;	OR	ON	2016/05/23 08:12

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S26	3	(filament near1 circuit) same bi-pin	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:14
S27	1	bi-pin and (filament adj simulating adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 08:14
S28	38	(US-20110181190-\$ or US-20140049171-\$ or US-20130278152-\$ or US-20120161650-\$ or US-20120026761-\$ or US-20110291585-\$ or US-20080247207-\$ or US-20150312989-\$ or US-20140239834-\$ or US-20140117851-\$ or US-20130278161-\$ or US-20120256551-\$ or US-20110025206-\$ or US-20100079076-\$ or US-20150223303-\$ or US-20130221867-\$ or US-20080290814-\$ or US-20070228999-\$ or US-20150351171-\$ or US-20160091147-\$).did. or (US-5777439-\$ or US-5606224-\$).did. or (WO-2010054523-\$ or EP-2432297-\$ or CA-2532763-\$).did. or (US-20120161650-\$ or CN-202190446-\$ or KR-1040833-\$ or CN-101998726-\$ or CN-201726573-\$ or CN-1688186-\$ or EP-2533607-\$ or US-20120286663-\$ or CN-102711329-\$ or CN-202425143-\$ or DE-102010029100-\$ or US-20110057572-\$).did.	US-PGPUB; USPAT; FPRS; DERWENT	OR	OFF	2016/05/23 10:08
S33	6	("20110057572" "20110121756" "20120299501" "20150173138" "20160081147" "9210744").PN.	US-PGPUB; USPAT	OR	OFF	2016/08/10 15:44
S34	6	("20110057572" "20110121756" "20120299501" "20150173138" "20160081147" "9210744").PN.	US-PGPUB; USPAT	OR	OFF	2016/08/10 15:45
S35	1	("9480109").PN.	USPAT; USOCR	OR	OFF	2017/03/13 12:50
S36	320	((("CHEN") near3 ("Zhong")).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/03/13 15:37
S37	6	((("ZHANG") near3 ("Yueqiang")).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/03/13 15:38
S38	307	((("JIANG") near3 ("Tao")).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/03/13 15:38
S39	13	((("YE") near3 ("Qifeng")).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/03/13 15:38

S40	634	S36 S37 S38 S39	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/03/13 15:39
S41	3	S40 and (bi-pin or bipin)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/13 15:39
S42	24	(filament adj simulating adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 09:15
S43	1090	((H05B33/0809 H05B33/0815 H05B33/0803 H05B33/0812 H05B33/0806 H05B33/0884 H05B33/0887 H05B33/089 H05B37/02 Y02B20/386 Y02B20/40 Y02B20/186 Y02B20/342 Y02B20/346 F21K9/17).CPC.) and (rectifier or rectification or rectifying) and filter\$3 and (current adj limit\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 09:49
S44	64	((H05B33/0809 H05B33/0815 H05B33/0803 H05B33/0812 H05B33/0806 H05B33/0884 H05B33/0887 H05B33/089 H05B37/02 Y02B20/386 Y02B20/40 Y02B20/186 Y02B20/342 Y02B20/346 F21K9/17).CPC.) and (rectifier or rectification or rectifying) and filter\$3 and (current adj limit\$3) and (bipin or bi-pin)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 09:50

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S29	1	(bi-pin and (filament adj simulating adj circuit)).clm.	US-PGPUB; USPAT	OR	ON	2016/05/23 10:04
S31	1	(bi-pin and (third adj capacitance)).clm.	US-PGPUB; USPAT	OR	ON	2016/05/23 10:05
S32	1	(bi-pin and (first adj capacitance)).clm.	US-PGPUB; USPAT	OR	ON	2016/05/23 10:05

3/ 14/ 2017 12:12:56 PM
C:\ Users\ vtan\ Documents\ EAST\ Workspaces\ 15258068.wsp

Search Notes 	Application/Control No. 15258068	Applicant(s)/Patent Under Reexamination YE ET AL.
	Examiner VIBOL TAN	Art Unit 2844

CPC- SEARCHED		
Symbol	Date	Examiner
H05B33/0809 H05B33/0815 H05B33/0803 H05B33/0812 H05B33/0806 H05B33/0884 H05B33/0887 H05B33/089 H05B37/02 Y02B20/386 Y02B20/40 Y02B20/186 Y02B20/342 Y02B20/346 F21K9/17 and text	3/14/2017	VTan

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor names search	3/14/2017	VTan
parent application 14/699,138 now US 9,480,109	3/14/2017	VTan
EAST text search	3/14/2017	VTan

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/258,068	09/07/2016	Qifeng Ye	SUP-104A

CONFIRMATION NO. 1056

PUBLICATION NOTICE



OC000000088182531

74712
Muir Patent Law, PLLC
P.O. Box 1213
9913 Georgetown Pike, Suite 200
Great Falls, VA 22066

Title:POWER SOURCE MODULE FOR LED LAMP

Publication No.US-2016-0381746-A1

Publication Date:12/29/2016

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/258,068	09/07/2016	Qifeng Ye	SUP-104A

74712
Muir Patent Law, PLLC
P.O. Box 1213
9913 Georgetown Pike, Suite 200
Great Falls, VA 22066

CONFIRMATION NO. 1056
37 CFR 1.48 ACKNOWLEDGEMENT
LETTER



Date Mailed: 12/07/2016

NOTICE OF ACCEPTANCE OF REQUEST UNDER 37 CFR 1.48(a)

This is in response to the applicant's request under 37 CFR 1.48(a) submitted on 12/05/2016.

The request under 37 CFR 1.48(a) to correct the inventorship, to correct or update the name of an inventor, or to correct the order of names of joint inventors is accepted.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/ctuazon/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: Qifeng YE et al. Attorney Docket: SUP-104A
Serial Number: 15/258,068 Group Art Unit: 2844
Filed: September 7, 2016 Examiner: Not Yet Assigned
Confirmation Number: 1056
Title: POWER SOURCE MODULE FOR LED LAMP

REQUEST TO CHANGE INVENTORSHIP UNDER 37 C.F.R. 1.48(a)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir/Madam:

Applicant hereby requests change of the inventorship in the above identified non-provisional Application under 37 C.F.R. 1.48(a). Applicant submits with this filing (a) an executed inventor's oath/declaration; and (b) an electronic ADS revision.

A new inventor, Zhong Chen, is being added to this application.

A fee of \$140 is being paid with this submission. In the event any other fees are required in connection with this paper, please charge the Deposit Account No. 50-4574.

Respectfully submitted,

/Bradley Edelman/

MUIR PATENT LAW, PLLC.
9913 Georgetown Pike, Suite 200
Great Falls, VA 22066
Fax: (703) 757-7447

Bradley Edelman, Reg. No. 57,648
Tel: (703) 757-7449

CORRECTED ADS FORM

Application Number	15258068
Title of Invention	POWER SOURCE MODULE FOR LED LAMP

Inventor Information

****If no data is shown, no data has been corrected****

	Data of Record	Updated Data
Order Number	1	
Name	Qifeng Ye	

Residence Information

Residency	non-us-residency	
City	Jiaxing	
State		
Country of Residence	CN	

Mailing Address of Inventor

Address 1	No.1288 Jiachuang Rd. Xiuzhou Area,	
Address 2	Jiaxing City, Zhejiang, China	
City,State/Province, Postal Code	Jiaxing City	
Country	CN	

	Data of Record	Updated Data
Order Number	2	
Name	Tao Jiang	
Residence Information		
Residency	non-us-residency	
City	Jiaxing	
State		
Country of Residence	CN	
Mailing Address of Inventor		
Address 1	No.1288 Jiachuang Rd. Xiuzhou Area,	
Address 2	Jiaxing City, Zhejiang, China	
City,State/Province, Postal Code	Jiaxing City	
Country	CN	

	Data of Record	Updated Data
Order Number	3	
Name	Yueqiang Zhang	
Residence Information		
Residency	non-us-residency	
City	Jiaxing	
State		
Country of Residence	CN	
Mailing Address of Inventor		
Address 1	No.1288 Jiachuang Rd. Xiuzhou Area,	
Address 2	Jiaxing City, Zhejiang, China	
City,State/Province, Postal Code	Jiaxing City	
Country	CN	

	Data of Record	Updated Data
Order Number		<u>4</u>
Name		<u>Zhong Chen</u>

Residence Information

Residency		<u>non-us-residency</u>
City		<u>Jiaxing</u>
State		
Country of Residence		<u>CN</u>

Mailing Address of Inventor

Address 1		<u>No.1288 Jiachuang Rd. Xiuzhou Area,</u>
Address 2		<u>Jiaxing City, Zhejiang, China</u>
City,State/Province, Postal Code		<u>Jiaxing City OT</u>
Country		<u>CN</u>

Application Information

	Data of Record	Updated Data
Title of Invention	POWER SOURCE MODULE FOR LED LAMP	
Attorney Docket Number	SUP-104A	
Entity Type	Regular Undiscounted	

Domestic Benefit/National Stage Information

****If no data is shown, no data has been corrected****

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121,365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S. C. 119(e) or 120, and 37 CFR 1.78(a).

		Data of Record	Updated Data
	Prior Application Status		
	Application Number		
	Continuity Type		
	Prior Application Number		
	Filing Date (YYYY-MM-DD)		
	Patent Number		
	Issue Date (YYYY-MM-DD)		

Foreign Priority Information

****If no data is shown, no data has been corrected****

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

		Data of Record	Updated Data
	Application Number		
	Country		
	Filing Date		
	Access Code		

Applicant Information

****If no data is shown, no data has been corrected****

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

	Data of Record	Updated Data
Applicant Type		

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is		
Name of the Deceased or Legally Incapacitated Inventor		
Applicant is an Organization		
Name		
Organization Name		
Address 1		
Address 2		
City,State/Province,Postal Code		
Country		
Phone Number		
Fax Number		
Email Address		

Assignee Information including Non-Applicant Assignee Information

****If no data is shown, no data has been corrected****

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office

	Data of Record	Updated Data
Order		
Applicant is an Organization		
Name		

Organization Name		
-------------------	--	--

Mailing Address

Address 1		
Address 2		
City,State/Province,Postal Code		
Country		
Phone Number		
Fax Number		
Email Address		

Signature

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Bradley Edelman/	Registration Number	57648
First Name	Bradley	Last Name	Edelman

MUIR PATENT LAW, PLLC

ALI M. IMAM
703-757-7880
ali@muirpatentlaw.com

September 7, 2016

ATTORNEY DOCKET NO.: SUP-104A
CUSTOMER NO. 74,712

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

New U.S. Patent Application

Title: POWER SOURCE MODULE FOR LED LAMP

Inventor(s): Ye, Qifeng; Jiang, Tao; Zhang, Yueqiang.

Sir:

We enclose the following papers for filing in the United States Patent; and Trademark Office in connection with the above patent application.

1. Specification (22 pages);
2. Drawings (3 sheets);
3. Application Data Sheet (PTO/AIA/14);
4. Declaration (4 pages);
5. Power of Attorney (PTO/AIA/82B);
6. Power of Attorney Transmittal (PTO/AIA/82A);

This application is a continuation application of U.S. Application No. 14/699,138, filed April 29, 2015, the contents of which are incorporated herein by reference in their entirety. The U.S. Application No. 14/699,138 claims the benefit of the filing date of Chinese Patent Application No. 201420602526.2, filed Oct. 17, 2014, entitled "POWER SOURCE MODULE FOR LED LAMP," and the contents of which are hereby incorporated by reference in their entirety.

Please accord this application an application number and filing date.

This application is being filed electronically. The required fees are being paid via credit card. The Commissioner is hereby authorized to charge any additional filing fees due and any other fees due under 37 C.F.R. § 1.16, §1.17, §1.19, §1.20, or §1.21 during the pendency of this application, and to refund any overpayments, to our Deposit Account No. 50-4574.

Respectfully submitted,

MUIR PATENT LAW, PLLC

By: /Ali Imam/
Ali Imam
Reg. No. 58,755

POWER SOURCE MODULE FOR LED LAMP

PRIORITY CLAIM

[0001] This application is a continuation application of U.S. Application No. 14/699,138, filed April 29, 2015, the contents of which are incorporated herein by reference in their entirety. The U.S. Application No. 14/699,138 claims the benefit of the filing date of Chinese Patent Application No. 201420602526.2, filed Oct. 17, 2014, entitled "POWER SOURCE MODULE FOR LED LAMP," and the contents of which are hereby incorporated by reference in their entirety.

FIELD OF THE INVENTION

[0002] The present disclosure relates to a power source module for a light emitting diode (LED) lamp, and more particularly, the present disclosure relates to a power source module for enabling the LED lamp installed on the traditional fluorescent lamp base.

BACKGROUND

[0003] Fluorescent lamps have been used widely in the world for illumination. The traditional fluorescent lamp is detachably installed on a fluorescent lamp base to receive the power from the power source in the base to emit light. According to the principle of luminosity of the traditional fluorescent lamp, the fluorescent lamp base has to provide a starter and a ballast to drive the traditional fluorescent lamp. The starter is used for heating filaments in the fluorescent lamp and raising a voltage between the two terminals of the fluorescent lamp, so as to ignite the fluorescent lamp to light. The traditional fluorescent lamp has a negative incremental impedance

characteristic, so that it needs the ballast to limit the amount of the current for preventing the fluorescent lamp from damage.

[0004] The traditional fluorescent lamp is filled with Argon, Neon, Krypton at low atmospheric pressure, and a bit of mercury vapor which is harmful. The traditional fluorescent lamp also has the disadvantages of high power consumption and high heat generation. Compared to the traditional fluorescent lamp, the LED lamp has the advantages of absence of mercury pollution, more power saving, and longer life. Therefore, the LED lamps are adopted more widely in the world recently to replace the traditional fluorescent lamps.

[0005] To replace the traditional fluorescent lamp by the LED lamp, the original circuit included in the fluorescent lamp base might need to be modified to adapt the LED lamp. There are two types of fluorescent lamp bases: one adopts an independent starter and an inductance as the ballast; the other adopts an electrical ballast including the starter therein. The inductance opposes the change in current and so the inductance ballast would attempt to keep the current of the LED lamp in a substantially fixed current. The starter and the electrical ballast generate a gaseous electric discharge in the fluorescent lamp by raising the voltage, and so it would cause the LED lamp to burn away. For the first type of the fluorescent lamp base, the LED lamp can be installed on the base directly and operates normally by taking the starter away and retaining the inductance ballast, and the starter in this type of fluorescent lamp base can be easily taken away by the user. On the contrary, the electrical ballast needs to be removed away by the user, and further the circuit in the fluorescent lamp base must be modified correspondingly for the LED lamp.

[0006] The modification to the electric ballast type fluorescent lamp base is complicated to the user, even to the professional. Also, it needs manpower and material resources to make the

modification. The inconvenience of the modification to the electric ballast keeps the users from replacing the traditional fluorescent lamp with the LED lamp.

[0007] Accordingly, the present disclosure and its embodiments are herein provided to address the above issues.

SUMMARY OF THE INVENTION

[0008] One object of the present disclosure is to provide a power source module for an LED lamp for use in a fluorescent lamp base including a ballast.

[0009] According to an embodiment of the invention, the power source module includes a filament-simulating circuit, a first rectifier, and a filter. The filament-simulating circuit is electrically connected to a first and a second bi-pin terminals of the LED lamp. Each of the first and the second bi-pin terminals has a current flowing from one pin to the other pin via the filament-simulating circuit during a pre-heat process executed by the ballast of the fluorescent lamp base. The first rectifier is electrically connected to the first bi-pin terminal for rectifying the current from the first bi-pin terminal. The filter is electrically connected between the first rectifier and at least one LED of the LED lamp for smoothing the current from the first rectifier and then outputting the current to the LED.

[0010] The power source module prevents the LED lamp from burning away by a high voltage, so as to enable the LED lamp installed on the traditional fluorescent lamp base to operate normally without modifying the circuit in the base.

[0011] Another object of the present invention is to provide a power source module for an LED lamp having a current limiting circuit to protect the LED lamp.

[0012] According to another embodiment, the power source module includes a current limiting

circuit, a first rectifier, and a filter. The current limiting circuit is electrically connected to a first terminal of the LED lamp for limiting a current from the terminal. The first rectifier is electrically connected to the current limiting circuit, and the filter is electrically connected to the first rectifier, so as to rectify and smooth the current.

[0013] Another object of the present invention is to provide a power source module for an LED lamp having a discharge circuit to prevent the LED lamp from flicker when turning off the LED lamp.

[0014] According to another embodiment, the power source module includes a rectifier, a filter, and a discharge circuit. The rectifier is electrically connected to the terminals of the LED lamp for receiving a current, the filter is electrically connected between the rectifier and at least one LED of the LED lamp to store energy for smoothing the current, and the discharging circuit is electrically connected to the filter in parallel for discharging the energy in the filter.

[0015] On the advantages and the spirit of the invention, it can be understood further by the following invention descriptions and attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] FIG. 1 is a function block diagram illustrating a power source module for an LED lamp according to an embodiment of the invention.

[0017] FIG. 2 is a schematic diagram illustrating a power source module for an LED lamp according to another embodiment of the invention.

[0018] FIG. 3 is a schematic diagram illustrating a power source module for an LED lamp according to another embodiment of the invention.

DETAILED DESCRIPTION

[0019] Please refer to FIG. 1. FIG. 1 is a function block diagram illustrating a power source module 1 for an LED lamp according to an embodiment of the invention. The power source module 1 may be configured inside a casing of the LED lamp to connect an LED module 2 of the LED lamp to terminals of the LED lamp. The LED module includes at least one LED.

[0020] As shown in FIG. 1, the power source module 1 includes a filament-simulating unit 10, a current limiting circuit 12, a rectifier 14, and a filter 16. The filament-simulating unit 10 is electrically connected to the terminals of the LED lamp. The terminals of the LED lamp includes a first bi-pin terminal T1 and a second bi-pin terminal T2, and each of the first and the second bi-pin terminals T1, T2 further include two pins. These pins of the first and the second bi-pin terminals T1, T2 are configured to be detachably installed on the traditional fluorescent lamp base for receiving a current therefrom. The filament-simulating unit 10 also includes a first filament-simulating circuit 100 and a second filament-simulating circuit 102 connected to the pins of the first bi-pin terminal T1 and the second bi-pin terminal T2, and therefore, the filament-simulating unit 10 may also be referred to as a filament-simulating circuit 10. The power source module 1 may also be described as a power source circuit, or a power supply circuit.

[0021] The first filament-simulating circuit 100 and the second filament-simulating circuit 102 are able to receive current(s) via the bi-pin terminals T1, T2 and power source ends of the fluorescent lamp base from an external power source. During a pre-heat process executed by the ballast of the fluorescent lamp base, a current flows from one pin to the other pin of the first bi-pin terminal T1 via the first filament-simulating circuit 100, and similarly a current from one pin to the other pin of the second bi-pin terminal T2 via the second filament-simulating circuit 102 respectively. The current limiting circuit 12 is electrically connected to the first bi-pin terminals

T1, and used for limiting the current from the first bi-pin terminal T1 to be in a suitable range for driving the LED module 2. The rectifier 14 is electrically connected between the current limiting circuit 12 and the second filament-simulating circuit 102. The rectifier 14 is used for rectifying the current from the bi-pin terminals T1, T2. The current inputted from the external power source is an alternating current, and the rectifier 14 rectifies the alternating current to be a direct current. The filter 16 is electrically connected to the rectifier 14 for filtering the rectified current and outputting the filtered current to the LED module 2.

[0022] The ballast may execute a pre-heat process to the filaments of the traditional fluorescent lamp for pre-heating the filaments. The filament-simulating unit 10 can simulate a filament of the traditional fluorescent lamp, so as to prevent the ballast from erroneously judging that the filaments are open-circuited or short-circuited during the pre-heating process of the ballast.

[0023] Please refer to FIG. 2. FIG. 2 is a schematic diagram illustrating a power source module 3 for an LED lamp according to another embodiment of the invention.

[0024] As shown in FIG. 2, the power source module 3 includes a filament-simulating unit 30, a current limiting circuit 32, a rectifier 34, and a filter 36 electrically connected between the LED module 2 and two bi-pin terminals T1 and T2. It should be noted that although FIG. 2 only shows one LED of the LED module 2, the LED module 2 may include more than one LED connected in parallel and/or in series in another embodiment. The filament-simulating unit 30 includes a first filament-simulating circuit 300 connected to the first bi-pin terminal T1 and a second filament-simulating circuit 302 connected to the second bi-pin terminal T2.

[0025] The first filament-simulating circuit 300 includes a pair of resistors, e.g., resistances R1, R2 and a pair of capacitors, e.g., capacitances C1, C2. The term “capacitance(s)” described herein may also be referred to as “capacitor(s)” and the term “resistance(s)” described herein

may also be referred to as “resistor(s).” The resistances R1 and R2 are connected in series, and the capacitances C1 and C2 are connected in series. The pair of resistances and the pair of capacitances are connected in parallel between the pins of the first bi-pin terminal T_i. The connection point between resistances R1, R2 is electrically connected to the connection point between capacitances C1, C2. Thereby, when one of the resistances R1, R2 and the capacitances C1, C2 is open circuited, the first filament-simulating circuit 300 still works.

[0026] Similarly, the second filament-simulating circuit 302 includes a pair of resistors, e.g., resistances R3, R4 and a pair of capacitors, e.g., capacitances C3, C4. The connecting relations of R3, R4, T3, T4, and the pins of the second bi-pin terminal T2 are similar to those of the first filament-simulating circuit 300 and the first bi-pin terminal T1, as shown in FIG. 2.

[0027] The values of the resistances R1, R2, R3, R4 and the capacitances C1, C2, C3, C4 could be matched in a reasonable range, for example, when the ballast provides a high frequency signal into the power source module 3, the impedance of the first pair of resistances R1, R2 could be ten times more than that of the first pair of capacitances C1, C2, and an impedance of the second pair of resistances R3, R4 could be ten times more than that of the second pair of capacitances. In this embodiment, the value of the resistances could be 100 K Ω . and the value of the capacitances could be 220 nF. The resistances R1, R2, R3, R4 and the capacitances C1, C2, C3, C4 could be electrically connected to the ballast in the traditional fluorescent lamp base via the first bi-pin terminal T1 and the second bi-pin terminal T2, to simulate the filaments during the pre-heating process of the ballast. After the pre-heating process, the ballast enters a normal operation state, and outputs an alternating current with a high frequency, e.g., 45 KHz, to the current limiting circuit 32.

[0028] The current limiting circuit 32 includes at least one capacitor, and in this embodiment,

capacitances C5 and C6. The capacitances C5 and C6 may be film capacitances to increase the reliability of the power source module 3. One end of the capacitance C5 is connected to one of the pins of the first bi-pin terminal T1. One end of the capacitance C6 is connected to the other of the pins of the first bi-pin terminal T1. The other ends of the capacitance C5 and the capacitance C6 are connected together, and connected to the rectifier 34. The values of the capacitances C5 and C6 can be matched to limit the value the current in a reasonable range when the ballast provides a high voltage to the LED module 2. The reasonable range is defined to the current range which drives the LED module 2 to operate normally, so that the reasonable range would vary with different types of LED or LED array. In practice, the reasonable range could be under 217 mA. The capacitances C5 and C6 are connected to different pins of the first bi-pin terminal T1, so that the value of the current from any one of the pins is assured to be limited in the reasonable range.

[0029] Please refer to FIG. 3. FIG. 3 is a schematic diagram illustrating a power source module 3 for an LED lamp according to another embodiment of the invention. As shown in FIG. 3, the difference between this embodiment and the last embodiment is that the current limiting circuit 32 further includes the third capacitance C7 connected between the capacitances C5 and C6 and the rectifier 34, so as to ensure the value of the current in the reasonable range even if one of the capacitances C5 and C6 is damaged. In a preferred embodiment, the values of the capacitances C5, C6, C7 are in the range of 0.47 nF to 12 nF, and in this embodiment, the values of the capacitances C5, C6 are 3.3 nF, and the value of the capacitance C7 is 8.2 nF.

[0030] The rectifier 34 includes a first rectifier 340 and a second rectifier 342 electrically connected to the current limiting circuit 32 and the second filament-simulating circuit 302 respectively for receiving and rectifying the current from the current limiting circuit 32.

Furthermore, the rectifier 34 is connected to the LED module 2 for outputting the rectified current thereto. The rectifier 34 includes six diodes D1, D2, D3, D4, D5, and D6, wherein the first rectifier 340 includes diodes D1, D2 electrically connected in series and the second rectifier 342 includes diodes D3, D4, D5, and D6 electrically connected to each other to form a bridge rectifier. In the embodiment shown in FIG. 2, the first diode D1 has an anode connected to the junction point of the capacitances C5 and C6 and a cathode thereof connected to the anode of the LED module 2. In the embodiment shown in FIG. 3, the first diode D1 has an anode connected to the third capacitance C7 and a cathode thereof connected to the anode of the LED module 2. The second diode D2 has an anode connected to the cathode of the LED module 2 and a cathode thereof connected to the third capacitance C7. A current may flow from the LED module 2 to one pin of the first bi-pin terminal T1 through the diode D2 and the current limiting circuit 32, or from one pin of the first bi-pin terminal T1 to the LED module 2 through the diode D1 and the current limiting circuit 32. The third diode D3 has an anode connecting to one of the pins of the second bi-pin terminal T2 and a cathode connected to the anode of the LED module 2. The fourth diode D4 has an anode connected to the cathode of the LED module 2 and a cathode connected to the anode of the third diode D3. The fifth diode D5 has an anode connected to the other of the pins of the second bi-pin terminal T2 and a cathode connected to the anode of the LED module 2. The sixth diode D6 has an anode connected to the cathode of the LED module 2 and a cathode connected to the anode of the fifth diode D5 which is connected to the other of the pins of the second bi-pin terminal T2.

[0031] The diodes of the rectifier 34 make a full-wave rectification to the current limited by the current limiting circuit 32, to output a rectified, direct current with a double frequency. For example, the current from the current limiting circuit 32 was an alternating current with

frequency of 45 KHz, and the rectified current output by the rectifier 34 is a direct current with frequency of 90 KHz. The rating current/voltage values of the diodes of the rectifier 34 are 1A/1000V, in this embodiment.

[0032] The filter 36 includes a filtering capacitance C8 connected to the rectifier 34 and the LED module 2 in parallel, as shown in FIGS. 2 and 3. The filtering capacitance C8 is used for storing energy from the rectifier 34 to filter and smooth the rectified current from the rectifier 34, and then outputting the filtered current to drive the LED module 2. The value of the filtering capacitance C8 is 680 nF, in this embodiment.

[0033] In this embodiment, the power source module 3 further includes a pair of discharging resistances R5 and R6 connected in series. The discharging resistance pair is connected to the filter 36 and the LED module 2 in parallel. The discharging resistances R5 and R6 can discharge the energy stored in the filtering capacitance C8 rapidly to prevent the LED lamp from flicker when turning off the power inputted to the power source module.

[0034] As described above, the power source module for the LED lamp simulates the filaments to prevent the ballast from stopping supplying power due to the error judgement during the pre-heating process. The current provided by the external power source after the pre-heating process can be limited, rectified, and filtered by the power source module to a suitable direct current to drive the LED, and the energy can be discharge rapidly after turning power off. Therefore, the power source module enables the LED lamp installed on the traditional fluorescent lamp base to operate normally without modifying the circuit in the base.

[0035] Although the present invention has been illustrated and described with reference to the preferred embodiment thereof, it should be understood that it is in no way limited to the details

of such embodiment but is capable of numerous modifications within the scope of the appended claims.

CLAIMS

1. A power source module for an LED lamp, comprising:

a filament-simulating circuit electrically connected to a first bi-pin terminal and a second bi-pin terminal of the LED lamp, each of the first bi-pin terminal and the second bi-pin terminal configured to allow a current to flow from one pin to the other pin via the filament-simulating circuit during a pre-heat process executed by a ballast;

a current limiting circuit electrically connected to the filament-simulating circuit configured to limit a current from the filament-simulating circuit;

a first rectifier electrically connected to the current limiting circuit configured to rectify the current from the current limiting circuit; and

a filter electrically connected between the first rectifier and at least one LED of the LED lamp configured to smooth the current from the first rectifier.

2. The power source module of claim 1, wherein the filament-simulating circuit comprises:

a first filament-simulating circuit comprising a first capacitor element electrically connected between two pins of the first bi-pin terminal; and

a second filament-simulating circuit comprising a second capacitor element electrically connected between two pins of the second bi-pin terminal.

3. The power source module of claim 2, wherein:

the first filament-simulating circuit further comprises a first pair of resistors electrically connected in series, the first capacitor element comprises a first pair of capacitors electrically connected in series, the first pair of resistors and the first pair of capacitors electrically connected in parallel between two pins of the first bi-pin terminal, and a connection point between the first pair of resistors being electrically connected to a connection point between the first pair of capacitors; and

the second filament-simulating circuit further comprises a second pair of resistors electrically connected in series, the second capacitor element comprises a second pair of capacitors electrically connected in series, the second pair of resistors and the second pair of capacitors electrically connected in parallel between two pins of the second bi-pin terminal, and a connection point between the second pair of resistors being electrically connected to a connection point between the second pair of capacitors.

4. The power source module of claim 3, wherein an impedance of the first pair of resistors is ten times more than that of the first pair of capacitors, and an impedance of the second pair of resistors is ten times more than that of the second pair of capacitors.

5. The power source module of claim 2, wherein the first rectifier comprises two diodes electrically connected in series, and the first rectifier is electrically connected to the first filament-simulating circuit in parallel.

6. The power source module of claim 2, wherein the first rectifier comprises two diodes electrically connected in series and a connection node connecting the two diodes is coupled to

the current limiting circuit, wherein a current flows from the at least one LED to one pin of the first bi-pin terminal through one of the two diodes and the current limiting circuit, or from one pin of the first bi-pin terminal to the at least one LED through the other of the two diodes and the current limiting circuit.

7. The power source module of claim 6, wherein the current limiting circuit comprises at least a capacitor.

8. The power source module of claim 5, further comprising a second rectifier, wherein the second rectifier is a bridge rectifier electrically connected to the second filament-simulating circuit in parallel.

9. The power source module of claim 1, wherein the power source module is configured inside a casing of the LED lamp.

10. The power source module of claim 1, further comprising a discharging circuit electrically connected to the filter in parallel for discharging the filter.

11. The power source module of claim 1, wherein the current limiting circuit comprises:
a first capacitor, one end of the first capacitor being electrically connected to one pin of the first terminal; and

a second capacitor, one end of the second capacitor being electrically connected to the other pin of the first terminal, and the other end of the second capacitor being electrically connected to the other end of the first capacitor and the first rectifier.

12. The power source module of claim 11, wherein the current limiting circuit further comprises:

a third capacitor, one end of the third capacitor being electrically connected to the other ends of the first capacitor and the second capacitor, and the other end of the third capacitor being electrically connected to the first rectifier.

13. The power source module of claim 11, wherein the first rectifier comprises two diodes electrically connected in series and the connection node of the two diodes is electrically connected to the other ends of the first and second capacitor.

14. The power source module of claim 11, further comprising a discharging circuit electrically connected to the filter in parallel for discharging the filter.

15. The power source module of claim 1, wherein the filter comprises a filtering capacitor electrically connected to the at least one LED.

16. The power source module of claim 1, further comprising a discharging circuit electrically connected to the filter in parallel for discharging the filter.

17. A power source module for an LED lamp, comprising:

a rectifier electrically connected to terminals of the LED lamp configured to receive a current;

a filter electrically connected between the rectifier and at least one LED of the LED lamp configured to store energy from the rectifier and to smooth the current from the rectifier;

a discharging circuit electrically connected to the filter in parallel configured to discharge the energy stored in the filter; and

a filament-simulating circuit electrically connected to a first bi-pin terminal and a second bi-pin terminal of the LED lamp, the filament-simulating circuit comprising at least one resistor connected in parallel to at least one capacitor and configured to simulate a filament of a fluorescent lamp during a pre-heat process executed by a ballast.

18. The power source module of claim 17, further comprising a current limiting circuit electrically connected to the first bi-pin terminal of the LED lamp, configured to limit a current from the first bi-pin terminal.

19. The power source module of claim 18, wherein the current limiting circuit comprises:

a first capacitor, one end of the first capacitor being electrically connected to one pin of the first bi-pin terminal; and

a second capacitor, one end of the second capacitor being electrically connected to the other pin of the first bi-pin terminal, and the other end of the second capacitor being electrically connected to the other end of the first capacitor and the rectifier.

20. The power source module of claim 18, wherein the current limiting circuit further comprises:

a third capacitor, one end of the third capacitor being electrically connected to the other ends of the first capacitor and the second capacitor, and the other end of the third capacitor being electrically connected to the rectifier.

21. A power source module for an LED lamp, comprising:

a first circuit comprising a first capacitor element electrically connected between two pins of a first bi-pin terminal of the LED lamp, and a second circuit comprising a second capacitor element electrically connected between two pins of a second bi-pin terminal, wherein the first and second circuits are configured to simulate a filament of a fluorescent lamp during a pre-heat process executed by a ballast;

a current limiting circuit electrically connected to the first bi-pin terminal configured to limit a current from the first bi-pin terminal;

a rectifier electrically connected between the current limiting circuit and the second circuit configured to rectify the current from the current limiting circuit and a current from the second bi-pin terminal; and

a filter electrically connected between the rectifier and at least one LED of the LED lamp to store energy from the rectifier configured to smooth the current from the rectifier.

22. The power source module of claim 21, wherein:

the first circuit further comprises a first pair of resistors electrically connected in series, the first capacitor element comprises a first pair of capacitors electrically connected in series, the first pair of resistors and the first pair of capacitors electrically connected in parallel between two pins of the first bi-pin terminal, and a connection point between the first pair of resistors being electrically connected to a connection point between the first pair of capacitors; and

the second circuit further comprises a second pair of resistors electrically connected in series, the second capacitor element comprises a second pair of capacitors electrically connected in series, the second pair of resistors and the second pair of capacitors electrically connected in parallel between two pins of the second bi-pin terminal, and a connection point between the second pair of resistors being electrically connected to a connection point between the second pair of capacitors.

23. An LED lamp, comprising:

a current limiting circuit electrically connected to a first terminal of the LED lamp for limiting a current from the terminal;

a first rectifier electrically connected to the current limiting circuit for rectifying the current from the current limiting circuit;

a filter electrically connected between the first rectifier and at least one LED of the LED lamp for smoothing the current from the first rectifier; and

a filament-simulating circuit electrically connected to a first bi-pin terminal and a second bi-pin terminal of the LED lamp, each of the first and the second bi-pin terminals having a current flowing from one pin to the other pin of the respective bi-pin terminal via the filament-simulating circuit during a pre-heat process executed by a ballast.

24. The LED lamp of claim 23, wherein the filament-simulating circuit comprises:

a first filament-simulating circuit comprising a first capacitor element electrically connected between two pins of the first bi-pin terminal; and

a second filament-simulating circuit comprising a second capacitor element electrically connected between two pins of the second bi-pin terminal.

25. The LED lamp of claim 24, wherein:

the first filament-simulating circuit further comprises a first pair of resistors electrically connected in series, the first capacitor element comprises a first pair of capacitors electrically connected in series, the first pair of resistors and the first pair of capacitors electrically connected in parallel between two pins of the first bi-pin terminal, and a connection point between the first pair of resistors being electrically connected to a connection point between the first pair of capacitors; and

the second filament-simulating circuit further comprises a second pair of resistors electrically connected in series, the second capacitor element comprises a second pair of

capacitors electrically connected in series, the second pair of resistors and the second pair of capacitors electrically connected in parallel between two pins of the second bi-pin terminal, and a connection point between the second pair of resistors being electrically connected to a connection point between the second pair of capacitors.

26. The LED lamp of claim 23, wherein the current limiting circuit comprises:

a first capacitor, one end of the first capacitor being electrically connected to one pin of the first terminal; and

a second capacitor, one end of the second capacitor being electrically connected to the other pin of the first terminal, and the other end of the second capacitor being electrically connected to the other end of the first capacitor and the first rectifier.

27. The LED lamp of claim 26, wherein the current limiting circuit further comprises:

a third capacitor, one end of the third capacitor being electrically connected to the other ends of the first capacitor and the second capacitor, and the other end of the third capacitor being electrically connected to the first rectifier.

28. The LED lamp of claim 26, wherein the first rectifier comprises two diodes electrically connected in series and the connection node of the two diodes is electrically connected to the other ends of the first and second capacitor.

29. The LED lamp of claim 23, further comprising a discharging circuit electrically connected to the filter in parallel for discharging the filter.

30. The LED lamp of claim 24, wherein the first rectifier comprises two diodes electrically connected in series, and the first rectifier is electrically connected to the first filament-simulating circuit in parallel.

ABSTRACT

A power source module for an LED lamp includes a filament-simulating circuit electrically connected to a first bi-pin terminal and a second bi-pin terminal of the LED lamp, each of the first bi-pin terminal and the second bi-pin terminal configured to allow a current to flow from one pin to the other pin via the filament-simulating circuit during a pre-heat process executed by a ballast; a current limiting circuit electrically connected to the filament-simulating circuit configured to limit a current from the filament-simulating circuit; a first rectifier electrically connected to the current limiting circuit configured to rectify the current from the current limiting circuit; and a filter electrically connected between the first rectifier and at least one LED of the LED lamp configured to smooth the current from the first rectifier.

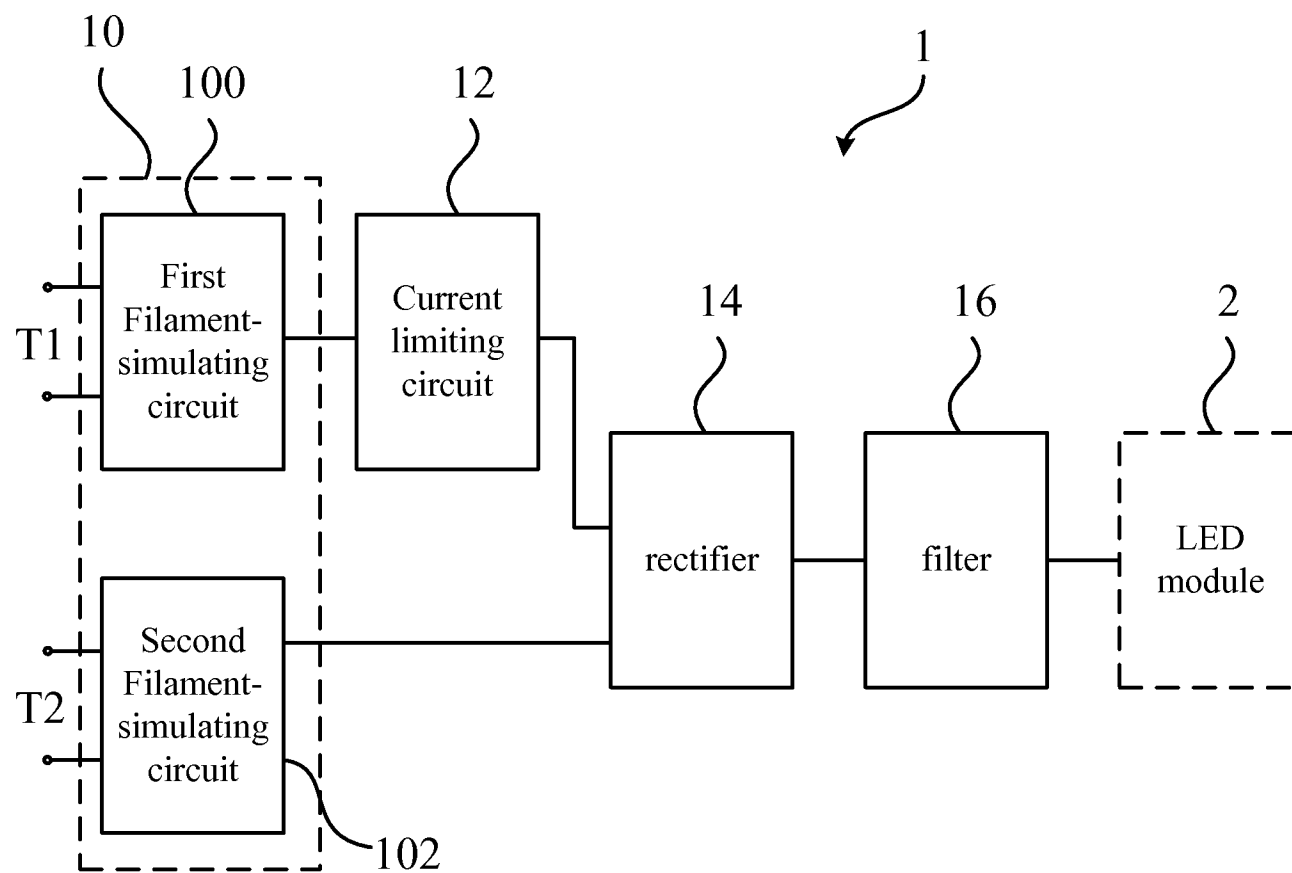


FIG. 1

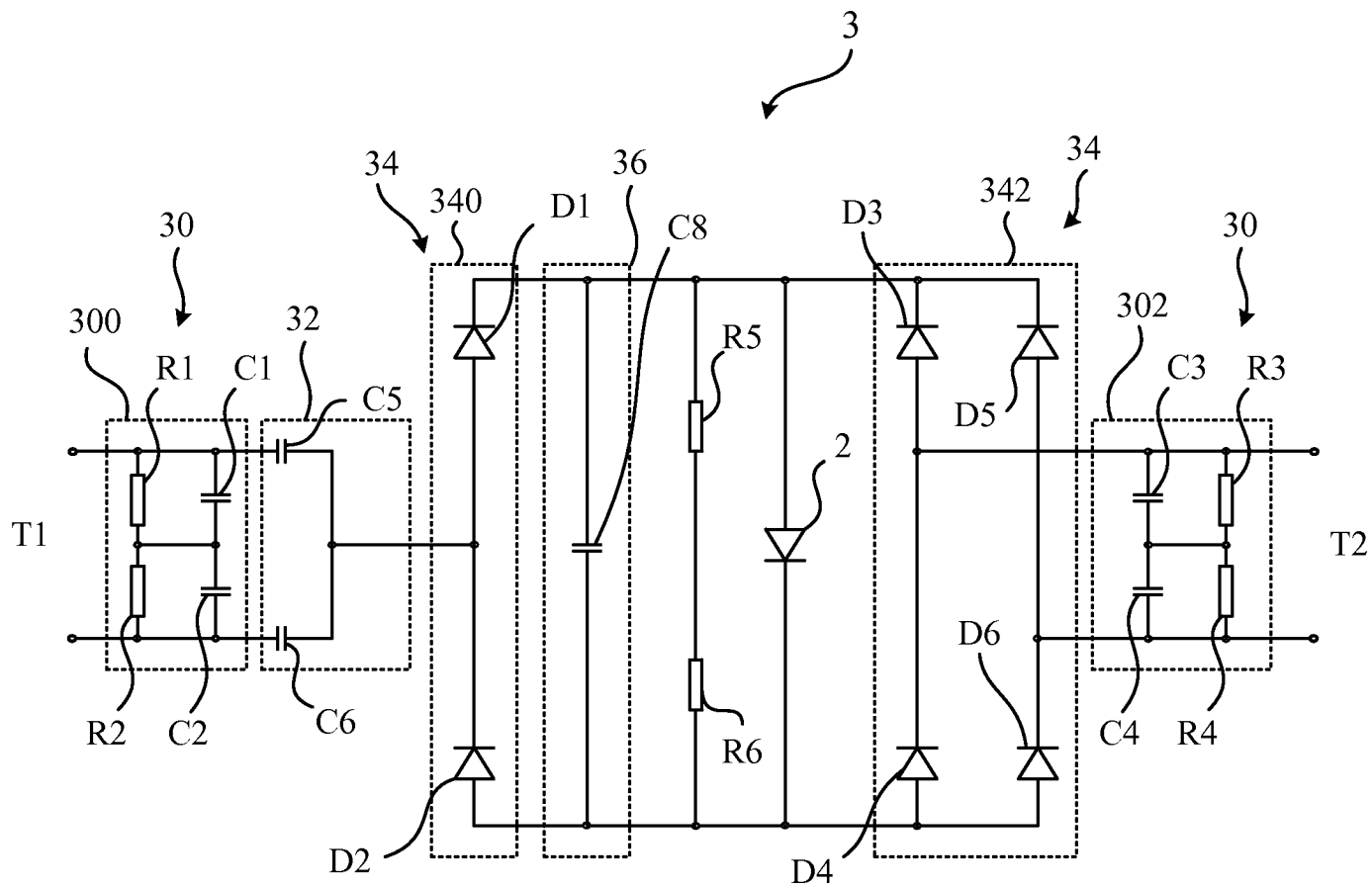


FIG. 2

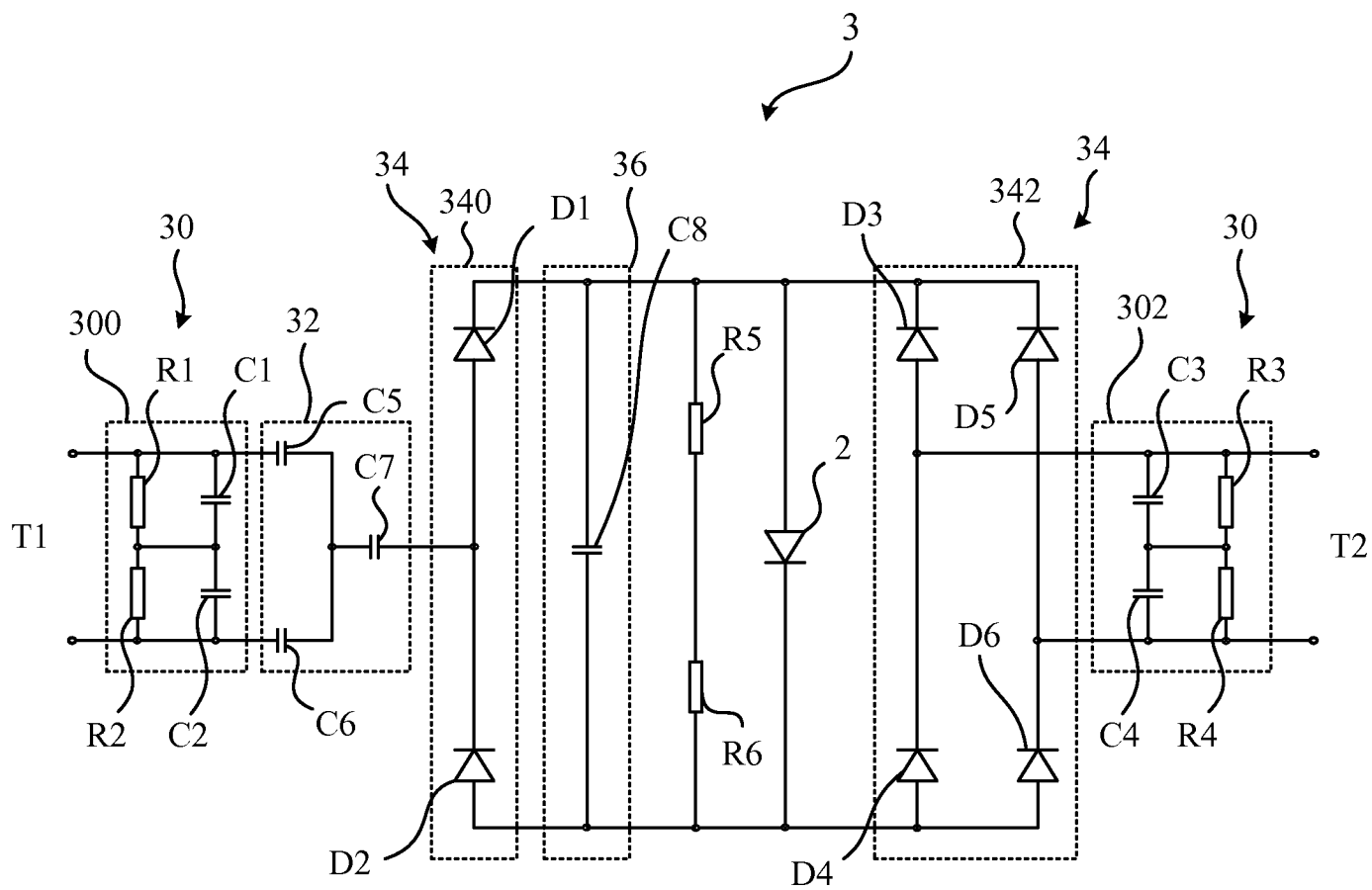


FIG. 3

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SUP-104A
		Application Number	
Title of Invention	POWER SOURCE MODULE FOR LED LAMP		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SUP-104A
		Application Number	
Title of Invention	POWER SOURCE MODULE FOR LED LAMP		

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Application Information:

Title of the Invention	POWER SOURCE MODULE FOR LED LAMP		
Attorney Docket Number	SUP-104A	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	3	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SUP-104A
		Application Number	
Title of Invention	POWER SOURCE MODULE FOR LED LAMP		

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	74712		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	14699138	2015-04-29
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ⁱ (if applicable)
201420602526.2	CN	2014-10-17	
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SUP-104A
		Application Number	
Title of Invention	POWER SOURCE MODULE FOR LED LAMP		

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

Authorization to Permit Access:

☒	Authorization to Permit Access to the Instant Application by the Participating Offices
If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application. In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application. In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.		
Applicant	1	Remove
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.		
Clear		
● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest

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		Application Number	
Title of Invention	POWER SOURCE MODULE FOR LED LAMP		

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

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Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name

Mailing Address Information For Applicant:

Address 1	No.1288 Jiachuang Rd. Xiuzhou Area		
Address 2	Jiaxing, Zhejiang, People's Republic of China.		
City	Jiaxing	State/Province	
Country	CN	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Add

Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee	1			
Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s).				
				Remove
If the Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SUP-104A
		Application Number	
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Mailing Address Information For Non-Applicant Assignee:			
Address 1			
Address 2			
City		State/Province	
Country ⁱ		Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Assignee Data may be generated within this form by selecting the Add button.			
			Add

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.					
Signature	/Ali Imam/			Date (YYYY-MM-DD)	2016-09-07
First Name	Ali	Last Name	Imam	Registration Number	58755
Additional Signature may be generated within this form by selecting the Add button.					Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.