

**Exhibit C**  
**Infringement Claim Chart for U.S. Patent No. 8,713,289 (“the ‘289 Patent”)**

As shown below, the Accused Products (*i.e.*, LzLabs Software Defined Mainframe (“SDM”)) infringe claims 1-3, 6, 10-12, 16, and 17 of U.S. Patent No. 8,713,289, entitled “Efficiently Emulating Computer Architecture Condition Code Settings Without Executing Branch Instructions.”

The evidence cited below is exemplary; plaintiff reserves the right to amend these preliminary infringement contentions as additional discovery is received and/or consistent with the local patent rules governing amendments to preliminary infringement contentions.

| <b>Claim 1</b>                                                                                                                                                                                  | <b>Exemplary Infringement Evidence</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
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| [1pre] A computer program product for emulating computer instructions from a source machine to produce sequences of instructions on a target machine, said computer program product comprising: | <p>To extent the preamble is limiting, Accused Products practice the limitation. For example, LzLabs SDM emulates computer instructions originating from a source machine to produce sequences of instructions on a target machine.</p> <p><i>See, e.g.,</i></p> <p>The LzLabs Software Defined Mainframe translates computer instructions from a source machine (object-level instructions in applications compiled to run on an IBM mainframe ISA computer) into sequences of instructions for a target machine (an x86 ISA computer). This is clear from various LzLabs announcements and other publications, <i>e.g.</i>:</p> <p>“LzLabs’ software solution allows the executable form of legacy customer mainframe programs to operate without changes and without compromise to performance in a contemporary and cost-effective computing environment, and enables mainframe data to be written and read in its native formats.” LzLabs Press Release, Zurich, 14 March 2016.</p> <p>“The LzLabs Software Defined Mainframe® design objective is to enable the applications to be rehosted on x86 without source-code changes or recompilation;</p> |

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|                                                                                                                                                                             | <p>yet with behavioural equivalence.” LzLabs White Paper: “The Software Defined Mainframe – Leveraging ‘the Power of Modern’,” September 2017, p. 2.</p> <p>“Next, as the object module is imported into the Software Defined Mainframe, LzLabs performs its patented Dynamic Instruction-Set Architecture Translation (DIT) process. This DIT step transforms the mainframe object module into an x86 object module. Such translation involves much more than simply converting one instruction set into another, memory management must be preserved plus a range of other considerations taken to ensure functional compatibility. But, the end result is a x86 program that behaves exactly like the original mainframe application program.” <i>Id.</i> at 3.</p> <p>“Three alternative solutions are possible for such a migration. These include:</p> <ul style="list-style-type: none"> <li>• Interpretive Execution</li> <li>• Incremental Just-in-Time Compiler</li> <li>• Load Module Decompiler/Compiler (LMD/LMC)</li> </ul> <p>The LzLabs Software Defined Mainframe® (SDM) Legacy Application Engine has three methods which it can use to execute customer programs in legacy load modules.” Jan Jaeger, Dale Vecchio, Roger Bowler, and Justin Bendich, <i>The Anatomy of Mainframe Workload Migration</i>, LzLabs White Paper, April, 2018 p. 2.</p> |
| [1a] a non-transitory computer readable storage medium read able by a processor and storing instructions for execution by the processor for performing a method comprising: | On information and belief, the Accused Products contain a non-transitory computer readable storage medium readable by a processor and storing instructions for execution by a processor. For example, LzLab SDM contains media, or is stored on and executed from media, storing computer instructions of the SDM.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| [1b] obtaining by the target machine a computer instruction from the source machine, said source machine having a different architecture from said target machine; and      | On information and belief, the Accused Products obtain, by the target machine, a computer instruction from the source machine, said source machine having a different architecture from said target machine. For example, SDM obtains computer instructions originating from a source machine having an architecture (z/Architecture or one of its predecessors) different from that (x86) of the target machine.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

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|  | <p><i>See, e.g.,</i></p> <p>“LzLabs’ software solution allows the executable form of legacy customer mainframe programs to operate without changes and without compromise to performance in a contemporary and cost-effective computing environment, and enables mainframe data to be written and read in its native formats.” LzLabs Press Release, Zurich, 14 March 2016.</p> <p>“The LzLabs Software Defined Mainframe® design objective is to enable the applications to be rehosted on x86 without source-code changes or recompilation; yet with behavioural equivalence.” LzLabs White Paper: “The Software Defined Mainframe – Leveraging ‘the Power of Modern’,” September 2017, at 2.</p> <p>“Next, as the object module is imported into the Software Defined Mainframe, LzLabs performs its patented Dynamic Instruction-Set Architecture Translation (DIT) process. This DIT step transforms the mainframe object module into an x86 object module. Such translation involves much more than simply converting one instruction set into another, memory management must be preserved plus a range of other considerations taken to ensure functional compatibility. But, the end result is a x86 program that behaves exactly like the original mainframe application program.” <i>Id.</i> at 3.</p> <p>“Three alternative solutions are possible for such a migration. These include:</p> <ul style="list-style-type: none"> <li>• Interpretive Execution</li> <li>• Incremental Just-in-Time Compiler</li> <li>• Load Module Decompiler/Compiler (LMD/LMC)</li> </ul> <p>The LzLabs Software Defined Mainframe® (SDM) Legacy Application Engine has three methods which it can use to execute customer programs in legacy load modules.” Jan Jaeger, Dale Vecchio, Roger Bowler, and Justin Bendich, <i>The Anatomy of Mainframe Workload Migration</i>, LzLabs White Paper, April, 2018, p. 2.</p> <p>The instructions in the mainframe application that LzLabs claims to be able to operate in its Software Defined Mainframe environment are instructions that</p> |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | <p>conform to IBM’s mainframe ISA, which is different from the x86 ISA of the instructions processed by the target machine on which the LzLabs Software Defined Mainframe runs. Such source machine instructions must be obtained by LzLabs DIT translation code on the target machine in order to translate them into x86 instructions.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <p>[1c] generating a sequence of target machine instructions which together operate to derive an encoding for a target machine condition code for the computer instruction, wherein the sequence of target machine instructions provides distinguishing information to distinguish between a plurality of possible outcomes for the target machine condition code, and directly calculates the target machine condition code without using branch instructions, the directly calculating comprising:</p> | <p>On information and belief, the Accused Products generate a sequence of target machine instructions which together operate to derive an encoding for a target machine condition code for the computer instruction, wherein the sequence of target machine instructions provides distinguishing information to distinguish between a plurality of possible outcomes for the target machine condition code, and directly calculates the target machine condition code without using branch instructions.</p> <p>For example, SDM generates sequence of target instructions which together operate to derive an IBM mainframe condition code (CC), the “target machine condition code,” for a particular IBM mainframe source instruction, as such a CC may be required to execute a subsequent IBM mainframe source instruction. Performance considerations for a processor such as an x86 using pipelining would dictate that this be done without using branch instructions. Target instructions would by necessity provide information distinguishing between different IBM mainframe CCs to ensure that the correct condition code is generated.</p> <p>The Intel x86 machines on which LzLabs claims to run its SDM employ pipelined processors, which means that the performance of such machines can be significantly affected by branches. Given its performance claims, it is not credible that LzLabs would not try to avoid the “branch penalty” by adopting an emulation technique that avoids the use of branch instructions to calculate the “target machine condition code” representation of the IBM mainframe condition code that must necessarily be maintained in the SDM while running translated versions of application programs composed of IBM mainframe ISA instructions.</p> <p>When emulating instructions from a source machine ISA on a target machine ISA system whose condition codes are different from those of the source machine ISA, it is necessary to have a target machine representation (encoding) of the source machine ISA condition code. This representation of the source machine ISA</p> |

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|                                                                                                                                                                                                                                                                          | <p>condition code is necessary to achieve accurate emulation on the target machine of source machine ISA instructions that depend on the specific settings and meanings of the source machine ISA condition code. It is this representation of the source machine ISA condition code that is referred to here as the “target machine condition code.”</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <p>[1d] determining an intermediate condition code value, the intermediate condition code value being a provisional value for the target machine condition code and subject to change based on the distinguishing information; and</p>                                   | <p>On information and belief, the Accused Products determine an intermediate condition code value, the intermediate condition code value being a provisional value for the target machine condition code and subject to change based on the distinguishing information.</p> <p>For example, in SDM, the procedure for generating a condition code involves successive updates to an IBM mainframe CC representation on the target machine based on other values.</p> <p>The sequence of non-branching target machine instructions that calculate the representation of the source ISA condition code does so in a step-by-step fashion, involving first calculating an intermediate value for the source ISA condition code representation, which may or may not be correct and thus may change in subsequent steps.</p>                                                                                                                       |
| <p>[1e] determining, based on the intermediate condition code value and based on the distinguishing information, the target machine condition code, wherein at least part of said distinguishing information is separate from the intermediate condition code value.</p> | <p>On information and belief, the Accused Products determine based on the intermediate condition code value and based on the distinguishing information, the target machine condition code, wherein at least part of said distinguishing information is separate from the intermediate condition code value.</p> <p>For example, the final IBM mainframe CC value would be determined based on the “intermediate” CC value referenced above and other distinguishing information used for final update.</p> <p>The step-by-step analysis is continued, using additional target machine instructions, the results of which provide additional distinguishing information that results in either retaining or modifying the intermediate condition code value until it is determined to be correct. The fact that the intermediate, or provisional, source ISA condition code representation may change means that some other distinguishing</p> |

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|  | information necessarily must be considered in order to determine if and how the intermediate condition code should be changed. |
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| <b>Claim 2</b>                                                                                                                                                                                 | <b>Exemplary Infringement Evidence</b>                                                                                                                                                                                                                                                  |
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| [2] The computer program product of claim 1, wherein said calculation of the target machine condition code comprises using at least one of carry, sign, and overflow codes in the calculation. | On information and belief, LzLabs SDM comprises the computer program product of claim 1, wherein said calculation of the target machine condition code comprises using at least one of carry, sign, and overflow codes in the calculation.<br><br>See citations for claim element [1c]. |

| <b>Claim 3</b>                                                                                                                      | <b>Exemplary Infringement Evidence</b>                                                                                                                                                                                       |
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| [3] The computer program product of claim 2, wherein said calculation employs temporary locations for storing intermediate results. | On information and belief, LzLabs SDM comprises the computer program product of claim 2, wherein said calculation employs temporary locations for storing intermediate results.<br><br>See citations for claim element [1c]. |

| <b>Claim 6</b>                                                                                                                                                                                                                             | <b>Exemplary Infringement Evidence</b>                                                                                                                                                                                                                                                                                              |
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| [6] The computer program product of claim 1, wherein the sequence of target machine instructions together operate to directly calculate the target machine condition code using at least one of addition, subtraction, and multiplication. | On information and belief, LzLabs SDM comprises the computer program product of claim 1, wherein the sequence of target machine instructions together operate to directly calculate the target machine condition code using at least one of addition, subtraction, and multiplication.<br><br>See citations for claim element [1c]. |

| <b>Claim 10</b>                                                                                                                                                                                                                                                                                   | <b>Exemplary Infringement Evidence</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
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| [10] The computer program product of claim 1, wherein determining the intermediate condition code value comprises storing the intermediate condition code value in a condition code storage location as the provisional target machine condition code, and wherein determining the target machine | On information and belief, LzLabs SDM comprises the computer program product of claim 1, wherein determining the intermediate condition code value comprises storing the intermediate condition code value in a condition code storage location as the provisional target machine condition code, and wherein determining the target machine condition code based on the distinguishing information and the intermediate condition code value comprises performing at least one operation on the intermediate condition code value stored in the condition code storage location to |

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| condition code based on the distinguishing information and the intermediate condition code value comprises performing at least one operation on the intermediate condition code value stored in the condition code storage location to obtain the target machine condition code and storing the target machine condition code in the condition code storage location. | <p>obtain the target machine condition code and storing the target machine condition code in the condition code storage location.</p> <p>See citations for claim element [1c].</p> |
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| Claim 11                                                                                                                                                                      | Exemplary Infringement Evidence                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
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| [11pre] A computer system for emulating computer instructions from a source machine to produce sequences of instructions on a target machine, the computer system comprising: | <p>To extent the preamble is limiting, Accused Products practice the limitation. For example, LzLabs SDM emulates computer instructions originating from a source machine to produce sequences of instructions on a target machine.</p> <p>See, e.g., citations for claim element [1pre].</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| [11a] a memory; and                                                                                                                                                           | <p>On information and belief, any computer system that implements LzLabs SDM contains memory. See generally, Jan Jaeger, Dale Vecchio, Roger Bowler, and Justin Bendich, <i>The Anatomy of Mainframe Workload Migration</i>, LzLabs White Paper, April, 2018 p. 1.</p> <p>“LzLabs’ software solution allows the executable form of legacy customer mainframe programs to operate without changes and without compromise to performance in a contemporary and cost-effective computing environment, and enables mainframe data to be written and read in its native formats.” LzLabs Press Release, Zurich, 14 March 2016.</p> <p>“The LzLabs Software Defined Mainframe® design objective is to enable the applications to be rehosted on x86 without source-code changes or recompilation;</p> |

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|                                                                                                                                                  | <p>yet with behavioural equivalence.” LzLabs White Paper: “The Software Defined Mainframe – Leveraging ‘the Power of Modern’,” September 2017, at 2.</p> <p>“Next, as the object module is imported into the Software Defined Mainframe, LzLabs performs its patented Dynamic Instruction-Set Architecture Translation (DIT) process. This DIT step transforms the mainframe object module into an x86 object module. Such translation involves much more than simply converting one instruction set into another, memory management must be preserved plus a range of other considerations taken to ensure functional compatibility. But, the end result is a x86 program that behaves exactly like the original mainframe application program.” <i>Id.</i> at 3.</p>                                                                                                                                                                                                                                                                                                                      |
| <p>[11b] a processor in communication with the memory, wherein the computer system is capable of performing a method, the method comprising:</p> | <p>On information and belief, the Accused Products obtain, by a processor, a machine instruction for execution, including by execution of instruction in an emulation environment such as that provided by the LzLabs SDM.</p> <p><i>See</i> Jan Jaeger, Dale Vecchio, Roger Bowler, and Justin Bendich, <i>The Anatomy of Mainframe Workload Migration</i>, LzLabs White Paper, April, 2018 p. f1–2 (SDM utilizes 3 different facilities to run, or “execute,” in its x86 Linux environment, applications compiled to run on the IBM mainframe, namely “Interpretive Execution,” “Incremental Just-in-Time Compiler,” and “Load Module Decompiler/Compiler (LMD/LMC).”)</p> <p><i>Id.</i> at 3 (“Currently LMD/LMC can be used with programs produced by the Enterprise COBOL compiler versions 3 and 4. Support for COBOL V5 and PL/I is under development.”)</p> <p>IBM’s COBOL V5 (the first release of the IBM COBOL V5 compiler) supports IBM’s z/Architecture through ARCH(11)<sup>1</sup>. In particular, COBOL V5 generates the Shift Significand z/Architecture instructions.</p> |

<sup>1</sup> ARCH option specifies the machine architecture for which the executable program instructions are to be generated. *See* <https://www.ibm.com/docs/en/cobol-zos/6.4?topic=options-arch>

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| [11c] obtaining by the target machine a computer instruction from the source machine, said source machine having a different architecture from said target machine; and                                                                                                                                                                                                                                                                                                                            | On information and belief, the Accused Products obtain, by the target machine a computer instruction from the source machine, said source machine having a different architecture from said target machine.<br><br><i>See, e.g.,</i> citations for claim element [1b].                                                                                                                                                                                                                                                                                           |
| [11d] generating a sequence of target machine instructions which together operate to derive an encoding for a target machine condition code for the computer instruction, wherein the sequence of target machine instructions provides distinguishing information to distinguish between a plurality of possible outcomes for the target machine condition code, and directly calculates the target machine condition code without using branch instructions, the directly calculating comprising: | On information and belief, the Accused Products generate a sequence of target machine instructions which together operate to derive an encoding for a target machine condition code for the computer instruction, wherein the sequence of target machine instructions provides distinguishing information to distinguish between a plurality of possible outcomes for the target machine condition code, and directly calculates the target machine condition code without using branch instructions.<br><br><i>See, e.g.,</i> citations for claim element [1c]. |
| [11e] determining an intermediate condition code value, the intermediate condition code value being a provisional value for the target machine condition code and subject to change based on the distinguishing information; and                                                                                                                                                                                                                                                                   | On information and belief, the Accused Products determine an intermediate condition code value, the intermediate condition code value being a provisional value for the target machine condition code and subject to change based on the distinguishing information.<br><br><i>See, e.g.,</i> citations for claim element [1d].                                                                                                                                                                                                                                  |
| [11f] determining, based on the intermediate condition code value and based on the distinguishing information, the target machine condition code, wherein at least part of said distinguishing information is separate from the intermediate condition code value.                                                                                                                                                                                                                                 | On information and belief, the Accused Products determine based on the intermediate condition code value and based on the distinguishing information, the target machine condition code, wherein at least part of said distinguishing information is separate from the intermediate condition code value.<br><br><i>See, e.g.,</i> citations for claim element [1e].                                                                                                                                                                                             |

| Claim 12 | Exemplary Infringement Evidence |
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| [12] The computer system of claim 11, wherein said calculation of the target machine condition code comprises using at least one of carry, sign, and overflow codes in the calculation. | On information and belief, LzLabs SDM comprises The computer system of claim 11, wherein said calculation of the target machine condition code comprises using at least one of carry, sign, and overflow codes in the calculation.<br><br><i>See citations for claim element [1c].</i> |
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| Claim 16                                                                                                                                                     | Exemplary Infringement Evidence                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
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| [16pre] A method for emulating computer instructions from a source machine to produce sequences of instructions on a target machine, said method comprising: | <p>To extent the preamble is limiting, Accused Products practice the limitation. For example, SDM emulates computer instructions originating from a source machine to produce sequences of instructions on a target machine.</p> <p><i>See, e.g.,</i></p> <p>The LzLabs Software Defined Mainframe solution meets the definition of emulation and does so in part by translating computer instructions from a source machine (object-level instructions in applications compiled to run on an IBM mainframe ISA computer) into sequences of instructions for a target machine (an x86 ISA computer). This is clear from various LzLabs announcements and other publications, e.g.:</p> <p>“LzLabs’ software solution allows the executable form of legacy customer mainframe programs to operate without changes and without compromise to performance in a contemporary and cost-effective computing environment, and enables mainframe data to be written and read in its native formats.” LzLabs Press Release, Zurich, 14 March 2016.</p> <p>“The LzLabs Software Defined Mainframe® design objective is to enable the applications to be rehosted on x86 without source-code changes or recompilation; yet with behavioural equivalence.” LzLabs White Paper: “The Software Defined Mainframe – Leveraging ‘the Power of Modern’,” September 2017, at 2.</p> <p>“Next, as the object module is imported into the Software Defined Mainframe, LzLabs performs its patented Dynamic Instruction-Set Architecture Translation</p> |

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|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | (DIT) process. This DIT step transforms the mainframe object module into an x86 object module. Such translation involves much more than simply converting one instruction set into another, memory management must be preserved plus a range of other considerations taken to ensure functional compatibility. But, the end result is a x86 program that behaves exactly like the original mainframe application program.” <i>Id.</i> at 3.                                                                                                                       |
| [16a] obtaining by the target machine a computer instruction from the source machine, said source machine having a different architecture from said target machine; and                                                                                                                                                                                                                                                                                                                            | On information and belief, the Accused Products obtain, by the target machine a computer instruction from the source machine, said source machine having a different architecture from said target machine.<br><br><i>See, e.g.</i> , citations for claim element [1b].                                                                                                                                                                                                                                                                                           |
| [16b] generating a sequence of target machine instructions which together operate to derive an encoding for a target machine condition code for the computer instruction, wherein the sequence of target machine instructions provides distinguishing information to distinguish between a plurality of possible outcomes for the target machine condition code, and directly calculates the target machine condition code without using branch instructions, the directly calculating comprising: | On information and belief, the Accused Products generate a sequence of target machine instructions which together operate to derive an encoding for a target machine condition code for the computer instruction, wherein the sequence of target machine instructions provides distinguishing information to distinguish between a plurality of possible outcomes for the target machine condition code, and directly calculates the target machine condition code without using branch instructions.<br><br><i>See, e.g.</i> , citations for claim element [1c]. |
| [16c] determining an intermediate condition code value, the intermediate condition code value being a provisional value for the target machine condition code and subject to change based on the distinguishing information; and                                                                                                                                                                                                                                                                   | On information and belief, the Accused Products determine an intermediate condition code value, the intermediate condition code value being a provisional value for the target machine condition code and subject to change based on the distinguishing information.<br><br><i>See, e.g.</i> , citations for claim element [1d].                                                                                                                                                                                                                                  |
| [16d] determining, based on the intermediate condition code value and based on the                                                                                                                                                                                                                                                                                                                                                                                                                 | On information and belief, the Accused Products determine based on the intermediate condition code value and based on the distinguishing information, the                                                                                                                                                                                                                                                                                                                                                                                                         |

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| distinguishing information, the target machine condition code, wherein at least part of said distinguishing information is separate from the intermediate condition code value. | target machine condition code, wherein at least part of said distinguishing information is separate from the intermediate condition code value.<br><br><i>See, e.g., citations for claim element [1e].</i> |
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| <b>Claim 17</b>                                                                                                                                                                | <b>Exemplary Infringement Evidence</b>                                                                                                                                                                                                                                        |
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| [17] The method of claim 16, wherein said calculation of the target machine condition code comprises using at least one of carry, sign, and overflow codes in the calculation. | On information and belief, LzLabs SDM practices the method of claim 16, wherein said calculation of the target machine condition code comprises using at least one of carry, sign, and overflow codes in the calculation.<br><br><i>See citations for claim element [1c].</i> |