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EXHIBIT A

Surface activated bonding for new flip chip and bumpless interconnect systems

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Abstract:

As microelectronic integration trends move toward ultrafine density flip chips and bumpless interconnect systems, it is necessary to develop a low cost, ultra-high density, low-damage and low-temperature interconnect technology. To satisfy this requirement, a new bonding method, the surface activated bonding (SAB), was introduced. In this process, the bonding pads on chips and bumps on substrates are first cleaned by Ar plasma or atom beam irradiation, precisely aligned with an accuracy of less than /spl plusmn/0.5 /spl mu/m. Then they are bonded directly to each other only by contact at room temperature or low temperature in a newly developed flip chip bonder. This procedure, which enables the bonding in an inert ambient atmosphere of N/sub 2,/ under atmospheric pressure, cuts down the bonding condition requirements and decreased the process cost. Some preliminary experiments have led to Au-Au

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Introduction

Recently, the authors have proposed a new concept of the bumpless interconnect for the next generation electronic packaging [1]. In high density integrated systems under the concept of bumpless interconnect, different types of device modules, which are fabricated in separate wafers by different processes, are bonded directly on to a global interconnect board composed of transmission line structure as another thin module. The "bumpless interconnect" means that two structures composed of interconnections and insulating layers are bonded directly to each other without bump-like electrode. The layer structures represent either combinations of chip on substrate, chip on chip, or wiring layer on active devices. In particular, separation of global interconnects from active device layer might improve the yield of multi-layer interconnection. Also an improvement in signal transmission rate can be expected by incorporating an adequate transmission line structure into the substrate and shortening interconnection between devices. Such ultra-fine pitch interconnect may allow two different devices, such as analog, RF, digital, or even MEMS devices to interconnect to each other in a vertical direction.

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Surface Activated Bonding for New Flip Chip and Bumpless Interconnect Systems

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Abstract

As the trend of microelectronic integration such as ultra-fine density flip chip or bumpless interconnect system, it is necessary to develop a low cost, ultra-high density, low-damage and low-temperature interconnect technology. To satisfy this requirement, a new bonding method, the Surface Activated Bonding (SAB), was introduced. In the process, the bonding pads on chip and bumps on substrate are cleaned at first by Ar plasma or atom beam irradiation, precisely aligned with accuracy of less than $\pm 0.5\mu\text{m}$. Then they are bonded directly to each other only by contact at the room temperature or low temperature in a newly developed flip chip bonder. The procedure that enables the bonding in inert ambient of N₂ under the atmospheric pressure cut down the bonding condition requirements and decreased the process cost. Some preliminary experiments led to Au-Au and Au-Cu direct bonding demonstrated a performance of the new bonding system.

Introduction

Recently, the authors have proposed a new concept of the bumpless interconnect for the next generation electronic packaging[1]. In high density integrated systems under the concept of bumpless interconnect, different types of device modules, which are fabricated in separate wafers by different processes, are bonded directly on to a global interconnect board composed of transmission line structure as another thin module. The "bumpless interconnect" means that two structures composed of interconnections and insulating layers are bonded directly to each other without bump-like electrode. The layer structures represent either combinations of chip on substrate, chip on chip, or wiring layer on active devices. In particular, separation of global interconnects from active device layer might improve the yield of multi-layer interconnection. Also an improvement in signal transmission rate can be expected by incorporating an adequate transmission line structure into the substrate and shortening interconnection between devices. Such ultra-fine pitch interconnect may allow two different devices, such as analog, RF, digital, or even MEMS devices to interconnect to each other in a vertical direction.

In order to realize the bumpless interconnect, a new bonding technique, which is referred as the surface activated bonding (SAB), has been introduced. SAB is a method which enables various types of materials bonded to each other at the room temperature or lower temperature than the conventional bonding techniques such as soldering and thermal compression bonding. The idea of SAB is based on the fact that two atomically clean solid surfaces under contact develop

an extremely strong adhesive force. The clean and activated surfaces can be obtained by Ar fast atom beam (FAB) bombardment in a certain clean atmosphere such as ultrahigh vacuum.

In the previous investigations[2]-[4], the SAB method has been proved as a potential tool for bonding of various combinations, such as metal to metal, metal to ceramic, and metal to semiconductor. Also hetero-junctions such as Si-GaAs, Si-InP, and GaAs-InP can be fabricated at the room temperature by using the method. Toyokohan Ltd. has adopted the SAB method on their cold rolling process for fabrication of metal laminates, and put it into mass-production of a part for the pressure-safety valve of Li-secondary battery composed of an Al-Al laminate.

In respect of the SAB applications for microbonding and bumpless bonding, some experiments have been carried out. Au electroplated bumps on Si substrate were bonded to Au, Al and Cu electrodes on Si chip, and it has been shown that the bonding is possible to happen even after exposure of surfaces to the atmosphere, depending on concentration of residual gases, the oxidation rate of metals, and material combinations. Bonding between Au and Au was successful without any difficulty under the atmospheric pressure of N₂. Other experiments have also shown that a bumpless direct bonding of Cu-Cu is feasible in model structures.

The purpose of the present study is to confirm the feasibility of the SAB method in more realistic circumstances and short range applications including conventional bump structure as well as bumpless structures. For this purpose, we have developed a new flip chip bonder combined by the SAB process. The bonder has a very high accuracy for alignment of chip and substrate better than 0.3 μm , and the room temperature or low temperature flip chip bonding is achieved for Au bump to Au or Cu electrode by means of the surface activation treatment using RF plasma irradiation.

New flip chip bonder

1. Configuration and operation of the bonder

1-1. Configuration

The bonder is divided into a pretreatment chamber for plasma cleaning and a bonding chamber as shown in Fig.1 and Fig.2. Between the chambers, there is a gate valve which allows the chambers to be separated so that they can be operated under the different gas pressures during the bonding operation. The pretreatment chamber is operated in a vacuum under the Ar background pressure, and the specimens on a tray are transferred into the bonding stage in the bonding chamber by a transfer mechanism. The bonding chamber is

filled with inert gas (N_2) up to atmospheric pressure. The bonding chamber consists of three sections as follows:

- The bonding head section (Z, X_0, Y_0) which holds a chip on the heat tool, adjusts the chip orientation to parallelize the chip and substrate, performs bonding, and applies a specific pressure.
- The bonding stage section (X, Y, θ) which holds a substrate on the heat stage and performs alignment.
- The camera table section (X, Y, Z) inserted between the chip and the substrate, which uses a 2-sight camera unit to identify reference marks on the chip and substrate, so that motions of the bonding head and the stage is calculated for the adjustment of alignment.

In addition, the camera table section transfers substrates from the tray to the heat stage, picks up individual chip from the tray, turns them over and delivers them to the heat tool.

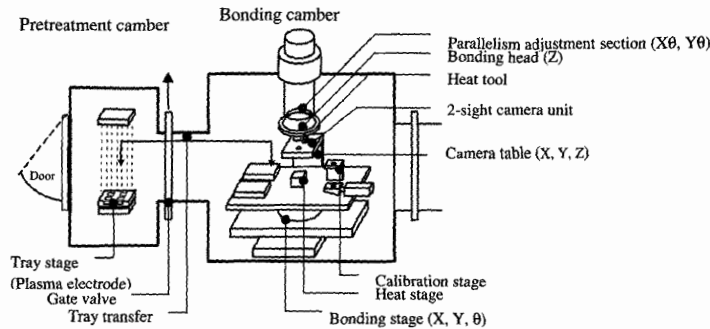


Fig. 1 Schematic drawing of the new flip chip bonding machine combined with SAB process.

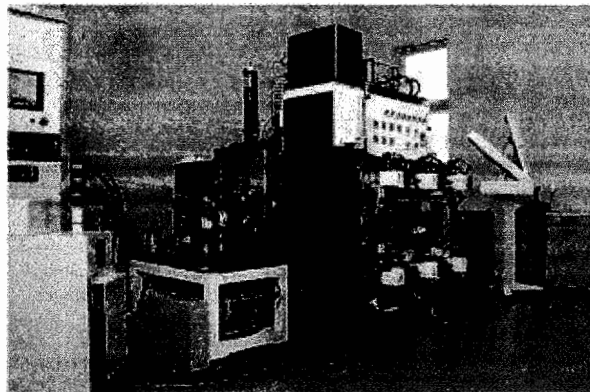


Fig. 2 A view of the SAB flip chip bonder.

1-2. Operation

1-2-1. Cleaning

Pairs of chip and substrate to be bonded can be held on a two-inch tray. First, the tray is set with the surface up for bonding. Then, the pretreatment chamber is evacuated, and the surfaces of chip and substrates are cleaned and activated by Ar RF plasma irradiation or Ar fast atom beam (FAB) irradiation for 10s to 60s. Etching speed for Au and Cu film is about 25nm/s. The time required for evacuation of the pretreatment chamber is about 1 minute and the purge time is about 20s, so that the whole pretreatment can be completed within 3 minutes.

1-2-2. Transfer

After the surface activation process is finished, the pretreatment chamber is filled with N_2 up to the atmospheric pressure. Then, the gate valve between the two chambers is opened, and the sample tray is transferred onto the bonding stage by the means of transfer mechanism. After transferring the tray, the next cleaning operation for another sample is performed in the pretreatment chamber while the bonding operation on the transferred chips and substrates starts in the bonding chamber. The time for transferring the sample into bonding chamber is about 2 minutes.

1-2-3. Bonding

A substrate on the sample tray is picked up and set by suction onto the heat stage. Then, a chip is picked up and flipped over so that the surface faces downwards for the heat tool to hold. The two-sight camera unit is inserted between the chip and the substrate. The reference marks on them are identified by image processing, and position alignment is performed by moving the stage. Then, the position error is evaluated again. Allignment time for this bonder is within 30s. After the alignment operation, the bonding head is lowered, and the bonding operation is performed under the specific contact pressure. Usually, bonding time is set within 1 minute. Both the tool and the stage have ceramic heaters, which provide a specific profile for heating. After bonding, the bonded sample is placed back on the sample tray.

1-2-4. Discharge

Although the sample tray is allowed to be discharged through the outlet on the opposite side to the pretreatment chamber, in the present experiments, it was returned to the pretreatment chamber.

2. Functions

The SAB flip chip bonder requires the following three attributes. Firstly, in respect of the bonding operation, a higher parallelism between the chip and the substrate is required than that for other conventional techniques, because the SAB is based on the solid state bonding between metals and therefore passive alignment is relatively effective. Secondly, the sub-micron bonding accuracy will be required for the future bumpless interconnect. Thirdly, a certain pressure is required to make the contact of a large number of bumps over a chip secure. At the same time, fine pressure control of a few grams is also required for weak devices such as GaAs chip.

2-1. Automatic parallelism adjustment

In this bonder, the distances between reference marks on chip and substrate are measured at three points. The parallelism is adjusted by the parallelism adjustment axes (X_θ , Y_θ) of the bonding head until the distances measured at the three points are within the specific value (i.e. parallel). In the case where a ten mm tool is used, the adjustment has allowed the parallelism with the accuracy of $\pm 0.3\mu\text{m}$, as seen in Fig.3.

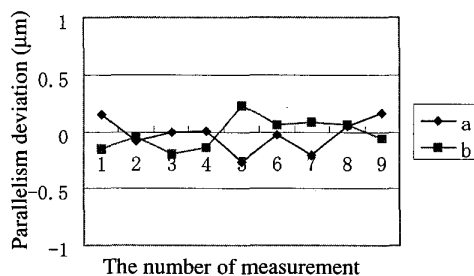


Fig. 3 Parallelism between chip and substrate.

2-2. Mounting accuracy

Mounting accuracy is measured by using a glass chip and a substrate which have reference marks on the adequate positions. Fig.4 shows the calibration stage on the bonding stage, the glass substrate being held by suction, and a camera positioned under the calibration stage to measure the position displacements between the chip and the substrate by recognizing the reference marks on them using image processing. Fig.5 shows the measurement results, which indicate a high mounting accuracy of sub-micron level: $\pm 0.2\mu\text{m}$ for 3σ .

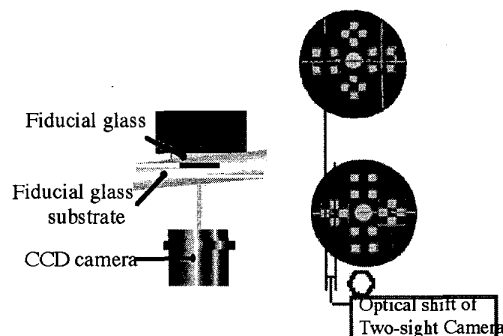


Fig. 4 Verification of the mounting accuracy.

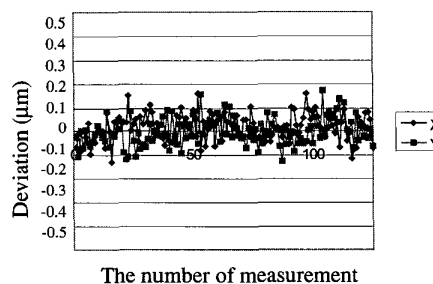


Fig. 5 Measurements of the mounting accuracy using a fiducial set of chip and substrate.

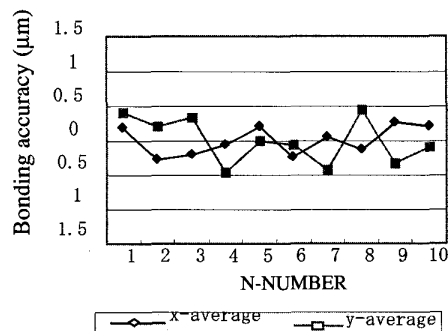


Fig. 6 Bonding accuracy in case of the conventional Au/Sn eutectic bonding.

The bonding accuracy of $\pm 0.5\sim 1\mu\text{m}$ was measured for the conventional Au/Sn eutectic bonding as shown in Fig. 6. The bonding accuracy is lower than the mounting accuracy, because the high bonding temperature of 623K creates a liquid phase of Au-Sn eutectic. Therefore the bonding at solid state

is expected to have almost the same accuracy as the mounting accuracy. The alignment operation is performed by using the 2-sight camera unit and the optical axis shifting has an influence upon the bonding position of the chip and the substrate. In order to achieve a bonding accuracy at sub-micron level under the influence, using the calibration stage and the glass substrate described above, the position displacement is offset automatically.

2-3. Fine pressure control

There are various size of chips to be bonded, therefore different pressures from a few grams to a few kilo grams are required. Bonding of optoelectronic devices requires fine pressure control of a few grams. As the pressure control for the head, an air cylinder is applied. The cylinder enables the sliding drag to be reduced to approximately zero by using air slide in the guide part. As a result, the pressure is controlled to be five grams at the minimum. Also, pressures of 5gf~500gf can be controlled by $\pm 1\text{gf}$ and pressures of 0.5kgf~50kgf can be controlled by $\pm 0.2\text{kgf}$. Table 1. summarizes the functions of the SAB flip chip bonder.

Table 1 Functions of the flip chip bonder.

Mounting accuracy	$\pm 0.2\mu\text{m}$
Parallelism adjustment function	$\pm 0.3\mu\text{m}/10\mu\text{m}$
Pressure $\left(\begin{array}{l} 5\text{gf}\sim 500\text{gf}\pm 1\text{gf} \\ 0.5\text{kgff}\sim 50\text{kgff}\pm 0.2\text{kgf} \end{array} \right)$	5gf~50kgff

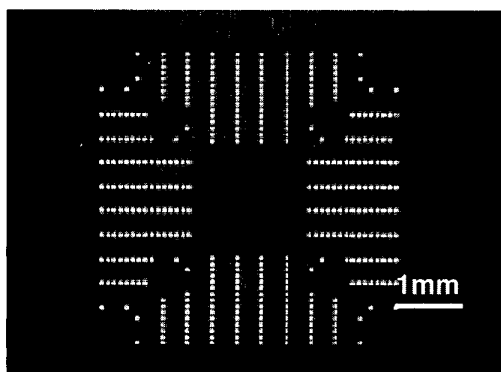


Fig. 7 Layout of Au bumps on Si substrate.

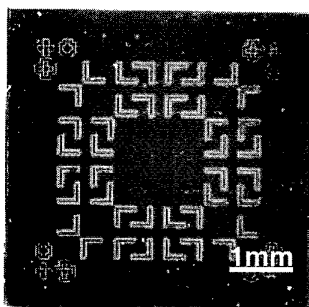


Fig. 8 Layout of Au pads on Si chip.

Bonding experiments

Si substrates with Au bump and Si chips with either Au or Cu pad were designed for surface activated flip chip bonding. The size of substrate and chip were $20\times 20\text{mm}^2$ and $6\times 6\text{mm}^2$ respectively. In the central area of the substrates, 400 bumps were fabricated by electroplating technique. The size of the bump is $40\mu\text{m}$ by $40\mu\text{m}$ with a height of $30\mu\text{m}$. In the peripheral area, 40 sets of probing pads are prepared. The thickness of the pad is about $0.3\mu\text{m}$. Fig.7 and Fig.8 illustrate the layouts of the bumps and the pads, respectively.

Surface activated bonding experiments for the flip chip configuration were carried out in the atmospheric pressure of N_2 . First, the substrate and the chip were subjected by Ar RF plasma in the pretreatment chamber connected directly to the bonding chamber, oxides and contamination on the surfaces of the bumps and the pads were removed, and the surfaces were activated. Then the substrate and the chip were transferred into the bonding chamber for alignment and bonding. The condition of the experiment was compiled in table 2. Ar was used as plasma irradiation ambience. The RF power output is 500W at the maximum. To prevent the temperature of the sample from being too high, and considering the thickness of the pad film, however, the power output of 100W is used in the present experiments. The plasma irradiation time was in the range of 10~60s at Ar flow rate of 30ccm and the plasma operation pressure of about 7.5 Pa.

Table 2. Experimental condition.

Ambience for bonding	N_2 , Air
Temperature of the bonding stage	298~523K
Contact load	5~46kgf
Plasma irradiation time	10~60s
Plasma power	100W

After the bonding experiment, electrical resistance of the bonded sample was measured by the four probe method. However the resistance values measured include the pad film resistance, the bump resistance, the barrier resistance, the electrode resistance and the contact resistance. The shear strength of the bonded samples is also measured.

Results & Discussion

In the surface activated flip chip bonding, the cleanliness and sufficient contact area of the surfaces to be bonded are the two important factors to ensure the success of the bonding and performance of the system. To fulfill this requirement, several factors should be considered carefully: the strength of the plasma and the irradiation time, the contact load and the temperature, the ambience gas and the oxygen concentration inside the bonding chamber, the exposure time before bonding. Among those, the effects of the plasma irradiation time, the contact load and the temperature would be the most crucial factors which will be discussed in the following sections.

1. Effect of the plasma irradiation time

The plasma irradiation contributes to remove the oxide and other contamination from the surface of the sample. As Cu is oxidized easily, the plasma irradiation time is more crucial for

to the Au-Cu system than for the Au-Au system. Fig.9 show the effect of the plasma irradiation time on the electrical resistance for the Au-Cu system bonded at 523K with the contact load of 46kgf. When the plasma irradiation time increased from 10s to 60s, the electrical resistance decreased from 4.3m Ω to 1.8m Ω , with the die shear strength of more than 9kgf. For further experiments, the plasma irradiation time of 30s was used.

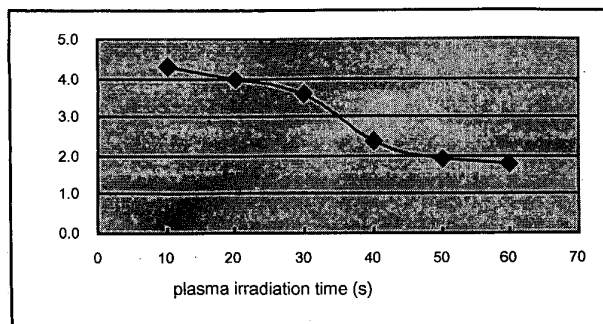


Fig. 9 Effect of the plasma irradiation time on the electrical resistance of the Au-Cu system bonded at 523K under 46kgf.

2. Effect of the bonding temperature

In the surface activated bonding, before the bonding process starts, the activated surface is kept in N₂ ambience for more than 3–4 minutes for sub-micron alignment. In general, oxygen concentration in the alignment chamber is about 0.03–0.08%, and therefore the surfaces of bumps and pads would be slightly oxidized and there would be layers of absorbed gases on the surface, thus direct bonding would be inhibited. The heating of the samples is expected then to enhance diffusion of such absorbed layers and plastic deformation of the metals in contact and to result in activating the surfaces for bonding. In case of the Au-Cu system, A strong bonding could be achieved at the bonding temperature of 523K with the contact load of 20kgf. The electrical resistance was about 6.2 m Ω and the bump shear strength was 30gf. Chip could not bond with substrate under the contact load of 20kgf if the bonding temperature was below 373K.

In case of the Au-Au system, as Au is not expected to be oxidized after the plasma irradiation process, a strong bonding could be achieved even in the air atmosphere. In case of N₂ ambience, the bonding was succeeded even in the room temperature. With increase of the bonding temperature from 298K to 373K, the electrical resistance was decreased from 5.2m Ω to 4.3 m Ω under the contact load of 46kgf.

3. Effect of the contact load

For the surface activated flip chip bonding, the surface roughness of the electroplated Au bump will determine the bonding pressure which is necessary for achieving the ultimate contact. If a too low contact load was set, the surfaces could not contact to each other. Fig. 10 shows that the surface roughness of Au bumps decreases in accordance with the increase in the contact load.

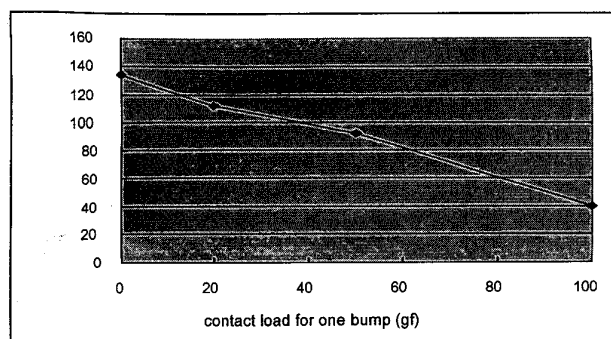


Fig. 10 Relationship between the surface roughness value, RMS, of Au bump and the contact load.

The decrease in the roughness leads to the increase in the bonding area. To evaluate the contact area, a simple two dimensional model was set up. The assumptions made for the model are as follows:

- 1) The surface profile of the bumps has a periodicity of a trapezoidal form and its volume will not change by deformation under the contact load.
- 2) The roughness RMS values is equal to those of the corresponding two-dimensional profile.
- 3) The original surface profile has a cone form, and the contact starts with the deformation of the top of the cones. However, considering the real profile observed by AFM images of the bump surface, the original shape is assumed as a truncated cone form having the same periodicity as the assumed cone form. Here, the volume ratio of the cone form and the truncated cone form is denoted by k ($1 \leq k < 3$), where $k=1$ corresponds to the cone and $k=3$ to the truncated cone consisting of completely flat area.

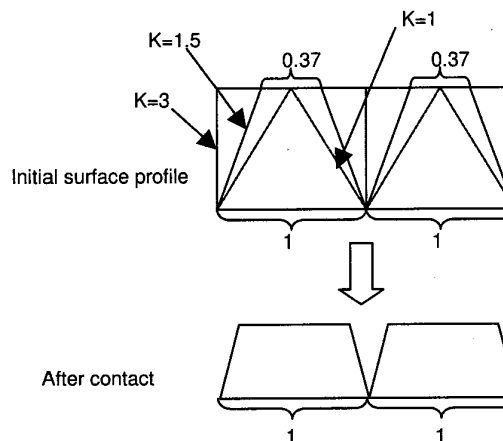


Fig. 11 Change of the surface profile under contact load.

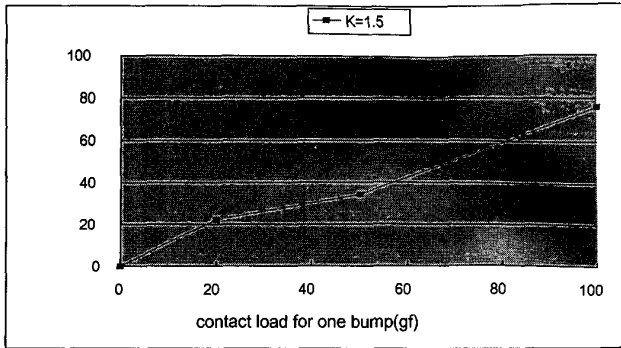


Fig. 12 Relationship between the bonded area and the contact load.

Based on the above assumptions, calculation was made and the relationship between the bonding area and the contact load for the case of $k=1.5$ was obtained as shown in Fig.12. Under the contact load of 20kgf, when $k=1$, the bonding area was about 5%, when $k=1.5$, about 22%, and when $k=2.5$, the bonding area increases to 80%. From the AFM observations of the surface profile of the Au bumps, it might reasonable to assume the k value was higher than 1.5, giving the contact area of more than 22%. At the same time, a too high contact load would result in serious damage of the chip or in even collapse.

For the Au-Cu system, when the contact load was below 10kgf, the bonding performance was not sufficient at the bonding temperature under 523K. When the contact load on 400 bumps was increased from 25kgf to 46kgf, the die shear strength increased from 8kgf to 9kgf above, even the silicon was broken, chip still bonded with substrate, and the electrical resistance was decreased from 5.6m Ω to 3.8m Ω .

For the Au-Au system, the effects of the contact load on the electrical resistance and the die shear strength in 373K are shown in Fig.13 and Fig.14, respectively. When the contact load increased from 5kgf to 30kgf, the electrical resistance decreased from 10m Ω to 4m Ω , and the die shear strength was increased from 2kgf to 6kgf. The bump was broken at the inside at the shear strength value of about 30kgf.

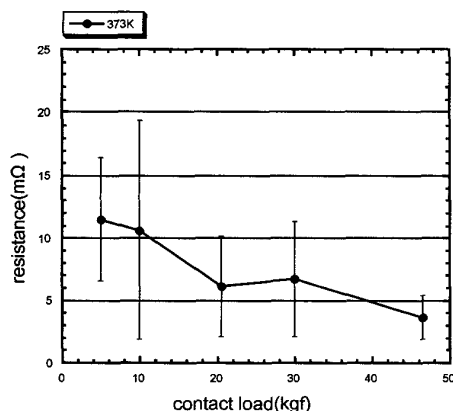


Fig. 13 Effect of the contact load on the electrical resistance of Au-Au bonded at 373K.

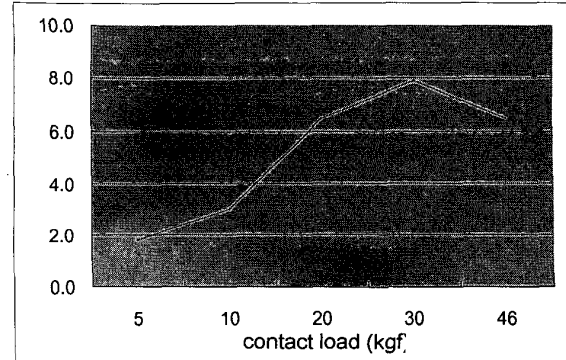


Fig. 14 Effect of the contact load on the die shear strength of Au-Au bonded at 373K.

As the contact load increased from 30kgf to 46kgf, the die shear strength decreased, and correspondingly, five to ten among 400 interconnections were found open in the region at the chip corner. When the contact load becomes too high, the elastic deformation may be also high in the contact area. After the contact load is removed, a strong backward force would occur at the bonded area. At the same time, as a result of the bump height deviation and the alignment error in the parallelism of the chip and substrate of about 0.3 μ m, some bump connections might be very weak. If the backward force is larger than the bonding force, the open of the connection will happen. Thus, the greater the contact force becomes, the more open connections happen. So it was found that the appropriate contact load was about 20~25kgf. It should be noticed, however, that the optimum contact load depends on the roughness of the bump surface and on the deviation in the bump height as well as on the flatness of the chip and the substrate.

Conclusions

1. A new flip chip bonding system was developed for combining the surface activated bonding process and a high accurate flip chip bonding system. The accuracy of the alignment of the chip and the substrate is as high as $\pm 0.2\mu$ m.
2. For model chips of Si with Au pads to Si substrates with electroplated Au bumps, the surface activated flip chip bonding was demonstrated successfully, even at the room temperature and in nitrogen ambience after 30s Ar plasma irradiation. Better bonding performance was obtained at the temperature of 373K with the contact load in the range of 20~25kgf.
3. In case of Si chips with Cu pads, the surface activated bonding was succeeded at the temperature in the range of 473~523K under the contact load of 20~25kgf in nitrogen with good bonding performance.
4. Under the above bonding conditions, for both Au-Au and Au-Cu systems, the electrical resistance was below 7m Ω , die shear strength was more than 5kgf and bump shear strength was about 30gf. These interconnect performances are expected to be improved by introducing a smoother surface of the bump.

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