

Exhibit A1

Claim Chart for U.S. Pat. No. 7,867,808

Sony Exmor RS CMOS Image Sensor

Part Number: Sony Sensor in Apple iPhone 13 Pro

Background

U.S. Patent No. 7,867,808 (“the ’808 Patent”)

Filing Date: December 28, 2008

Foreign Application Priority Date: December 28, 2007.

Sony Exmor RS CMOS Image Sensor

The Sony Exmor RS CMOS Image Sensor is a complementary metal oxide semiconductor (“CMOS”) stacked image sensor. The Sony Exmor RS is used, for example, in the wide-angle rear camera module of the Apple iPhone Pro 13.

The following chart maps a representative Sony Exmor RS CMOS Image Sensor from the wide-angle rear camera module of the Apple iPhone Pro 13 to the Asserted Claims of the ’808 Patent.

OVERVIEW: The Sony Exmor RS CMOS Image Sensor includes a CMOS image sensor (CIS) die stacked on an image signal processor (ISP) die. Each of the CIS and ISP dies includes a silicon (Si) substrate and interconnect metal levels. The figure below illustrates an exemplary cross-section of the stacked CIS and ISP dies.

Redefining the interchangeable-lens camera

Despite steady progress in digital imaging technology, mechanical limitations have restricted the benefits for digital-SLR users to relatively minor improvements in size and features.

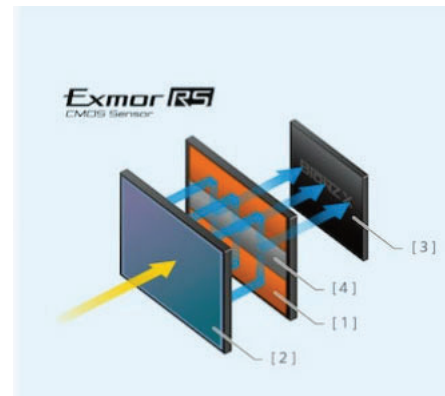
Now, with its ground-breaking innovation, Sony has transcended these limitations to redefine the future of interchangeable-lens cameras. The Exmor RS, the world's first ² 35mm full-frame stacked image sensor with integral memory, has achieved speed and performance well beyond the capabilities of other models, and while containing fewer resources.



Exmor RS. Evolution in action

The α9's sensor delivers great leaps in performance and image quality by providing rock-solid AF; silent, vibration-free continuous shooting up to 20fps ³ ; and a blackout-free ⁴ viewfinder.

<https://www.sony.com/za/electronics/eco-digital-imaging>



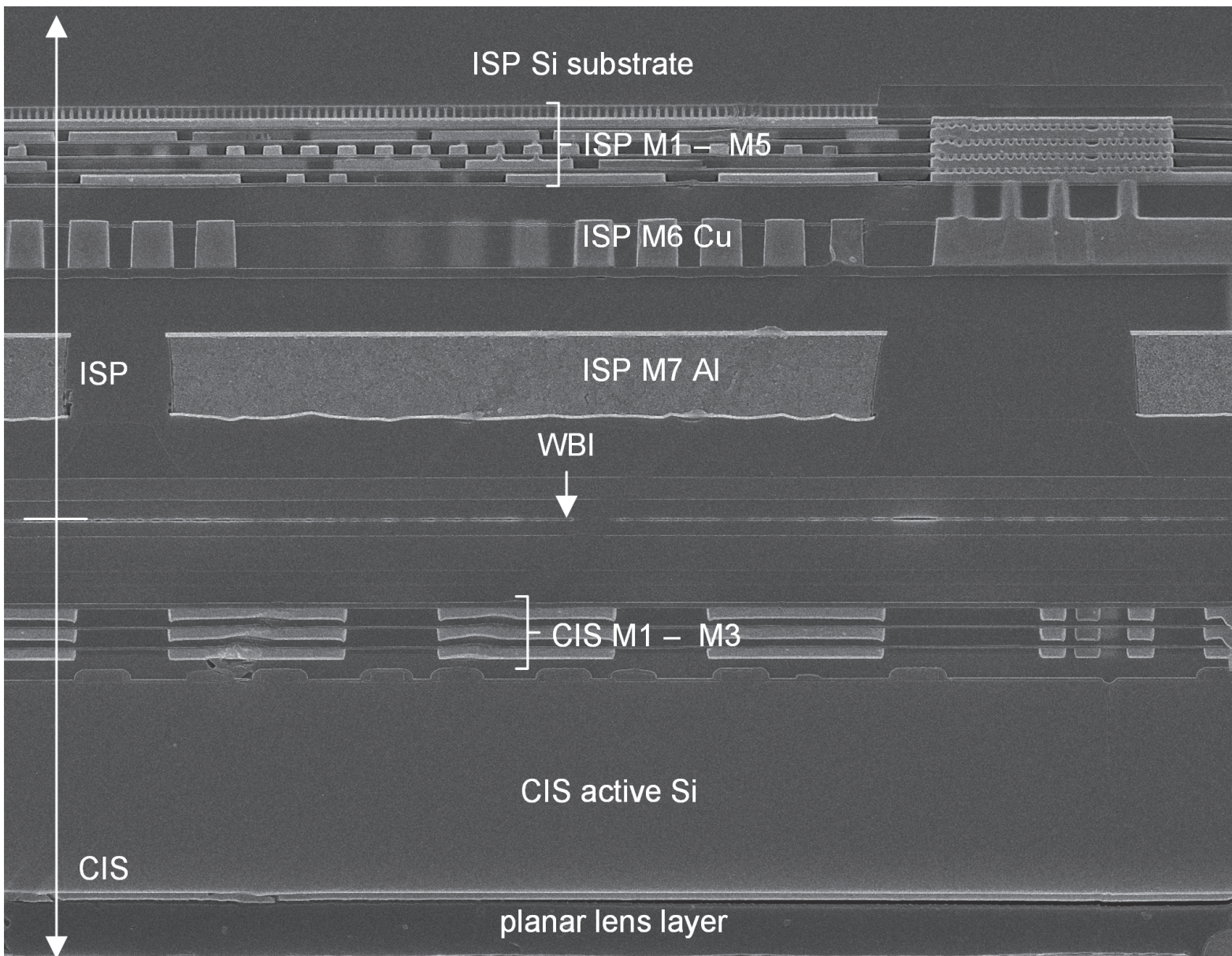
A sensor designed for performance

The new stacked CMOS sensor found in the α9 delivers professional performance, without the constraints of mechanical systems found in conventional digital-SLRs.

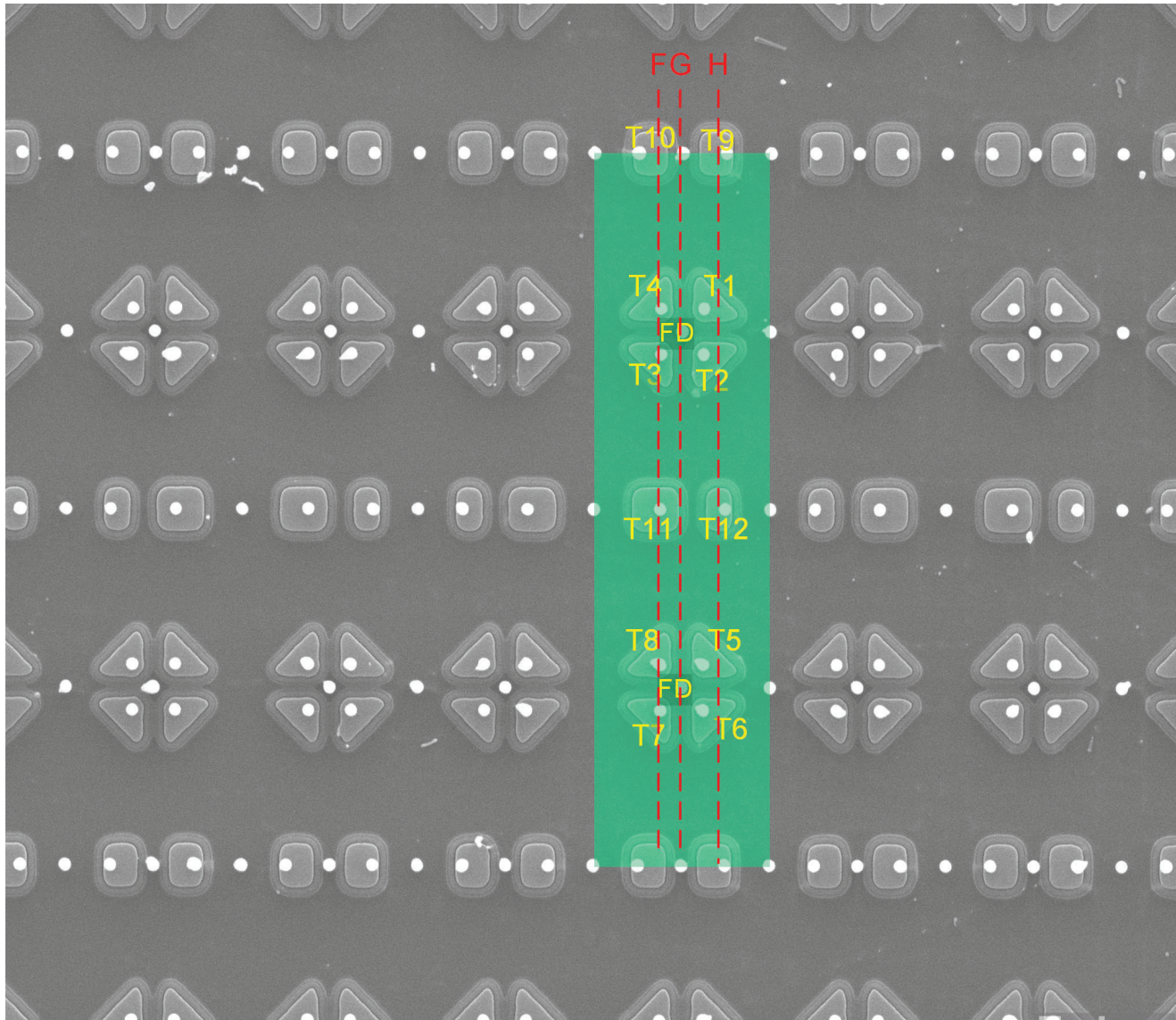
An industry-first ² , high-speed, stacked sensor produces approx. 24.2 effective megapixel full-frame images, with up to 20x ⁵ the readout speed thanks to integrated memory in the stack.

[1] Hi-speed signal processing circuit [2] Pixel area [3] Image processing engine [4] Integral memory

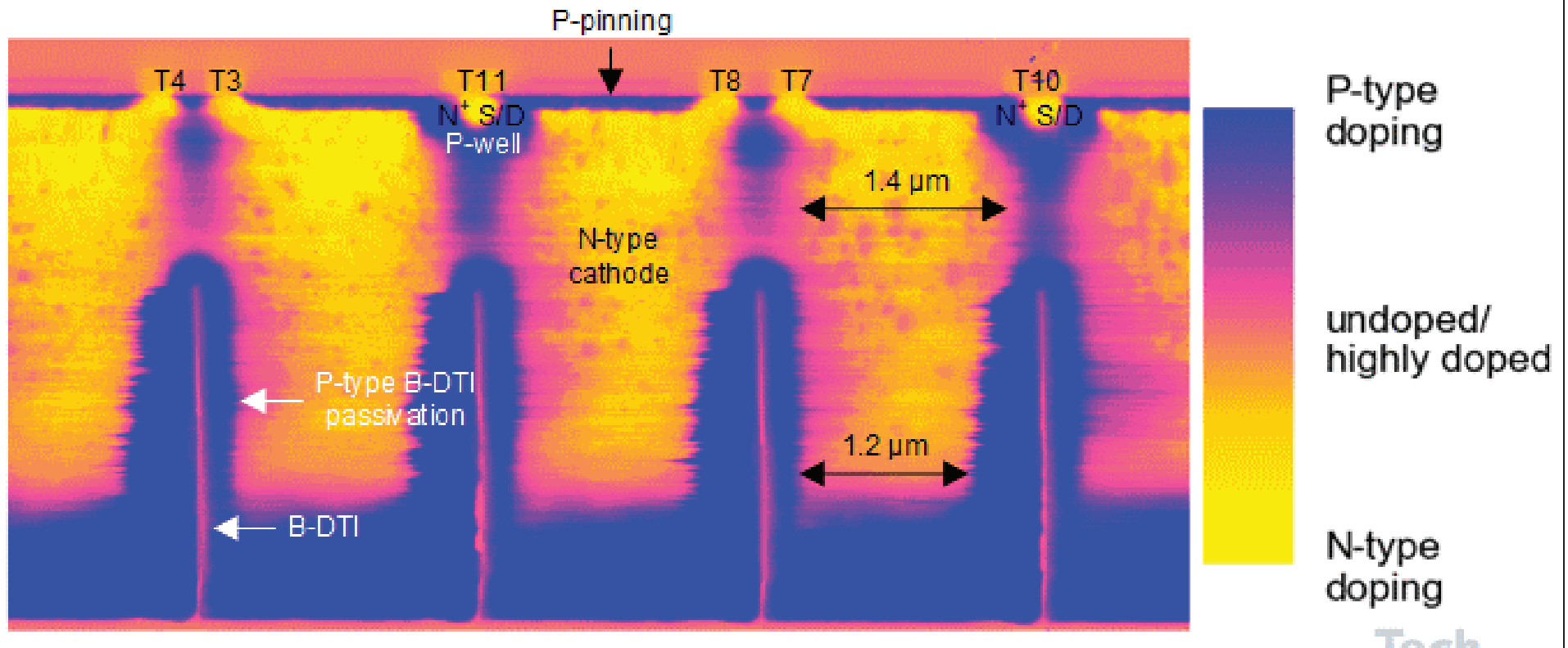
<https://www.sony.com/za/electronics/eco-digital-imaging>



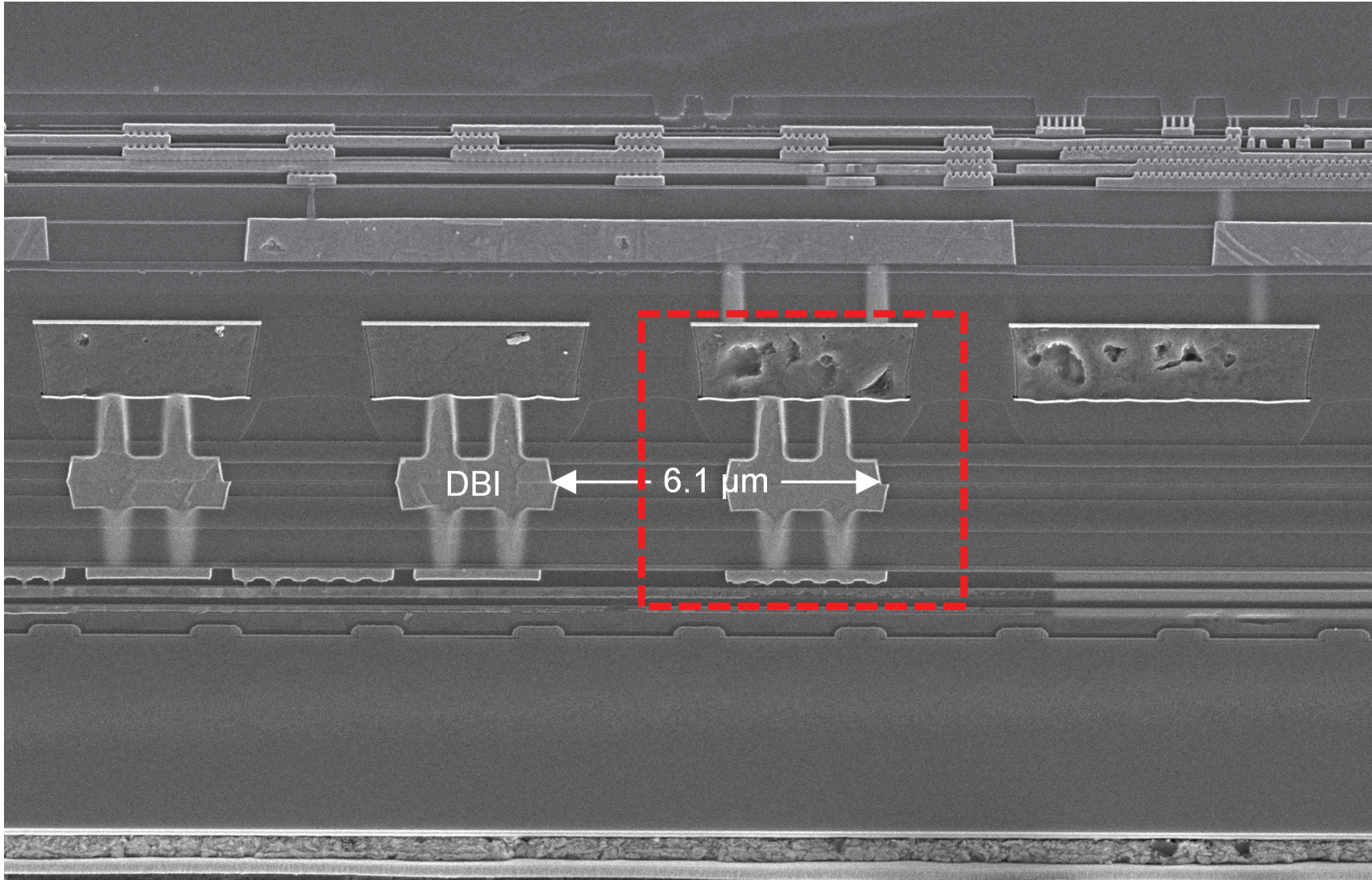
OVERVIEW (Cont'd): The CIS Si substrate includes an array of pixels. The figure below illustrates an exemplary SEM plan view of such pixels at a front surface of the CIS Si substrate. Pixel units are highlighted in green.



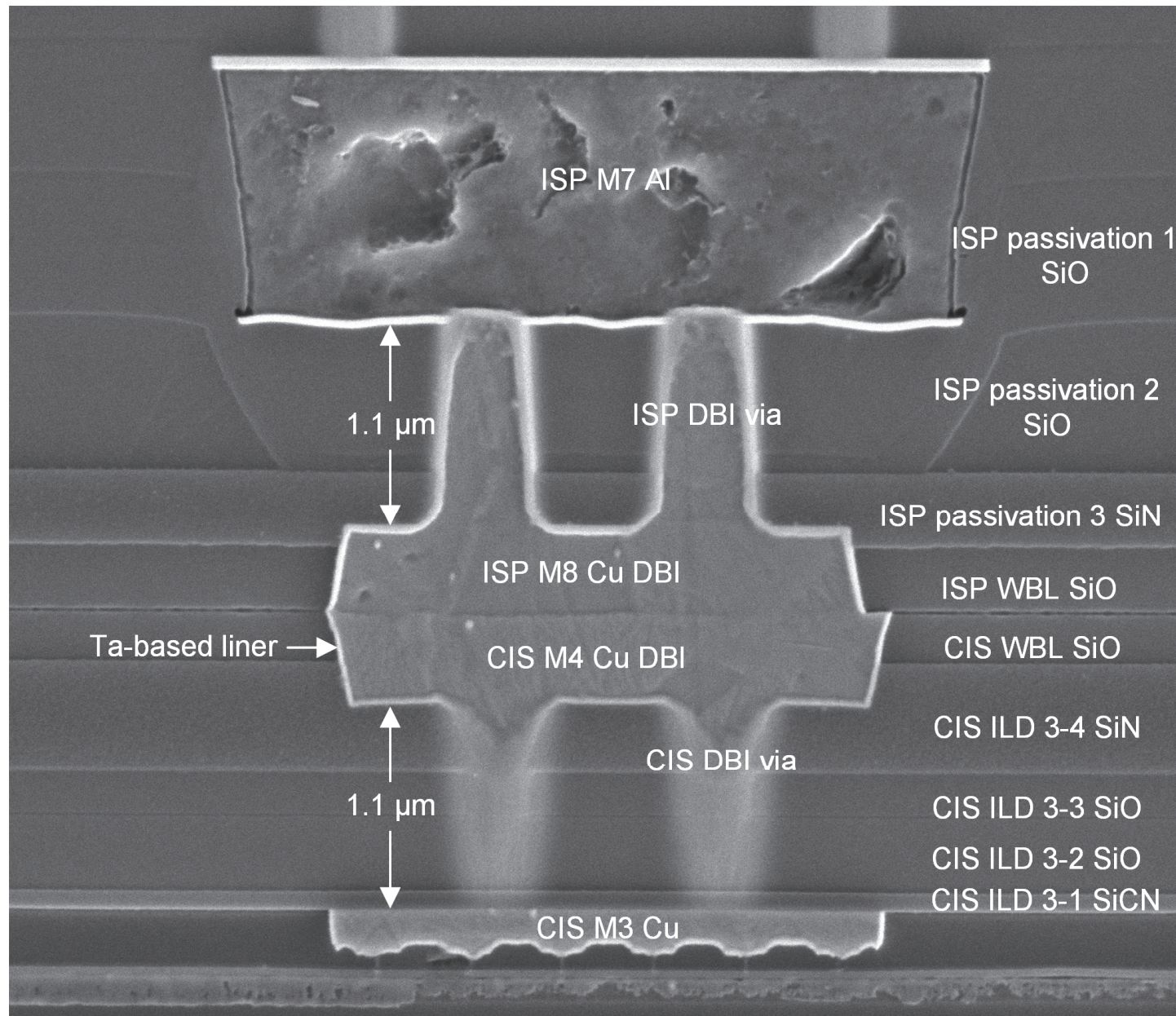
OVERVIEW (Cont'd): The figure below illustrates an exemplary scanning capacitance microscope (SCM) cross-section of such pixels in the CIS Si substrate, e.g., a cross-section along line F (in the above image). As shown below, a P-type pinning layer is formed over N-type cathodes of the photodiodes. Adjacent pixels are isolated from each other laterally by a combination of front P-type implant isolation layer and back deep trench isolation (B-DTI).



OVERVIEW (Cont'd): The CIS substrate and ISP substrate are electrically connected through direct bonding interconnects (DBIs). The figure below represents an exemplary scanning electron microscope (SEM) cross-section of such DBIs.



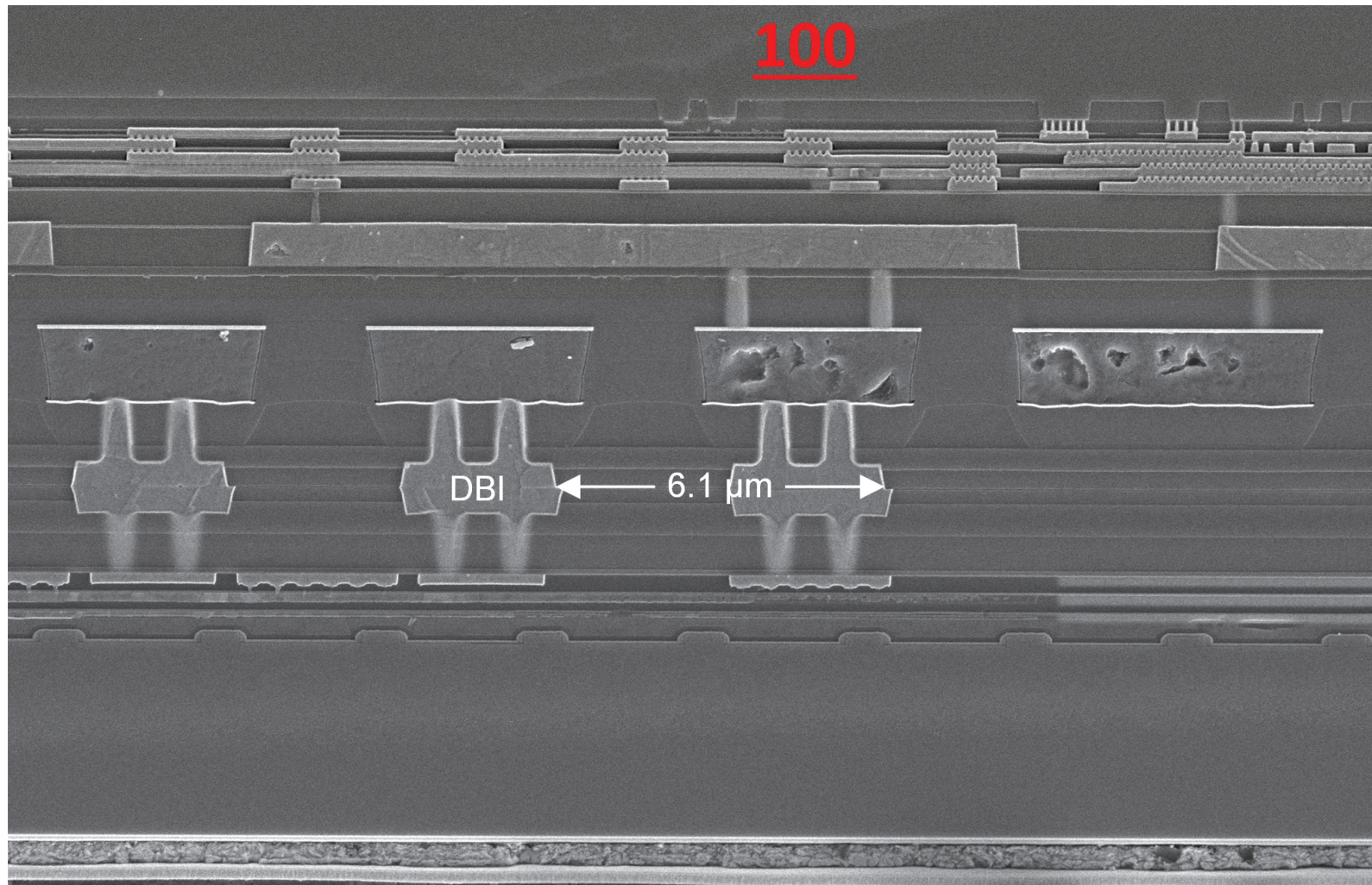
OVERVIEW (Cont'd): The figure below illustrates another exemplary SEM cross-section of such DBIs, e.g., a close-up of the region outlined by dashed red lines in the previous figure above.



Claim 1

A method, comprising: providing a first substrate; forming circuitry including a metal interconnection over the first substrate; forming a photodiode in a crystalline semiconductor layer of a second substrate; forming an ion implantation isolation layer in the photodiode; bonding the first substrate to the second substrate to connect the photodiode to the metal interconnection; and removing a lower portion of the second substrate to expose the photodiode, wherein forming the photodiode comprises: forming a second conduction type conduction layer in the crystalline semiconductor layer; and forming a first conduction type conduction layer over the second conduction type conduction layer, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer over the first conduction type conduction layer, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.

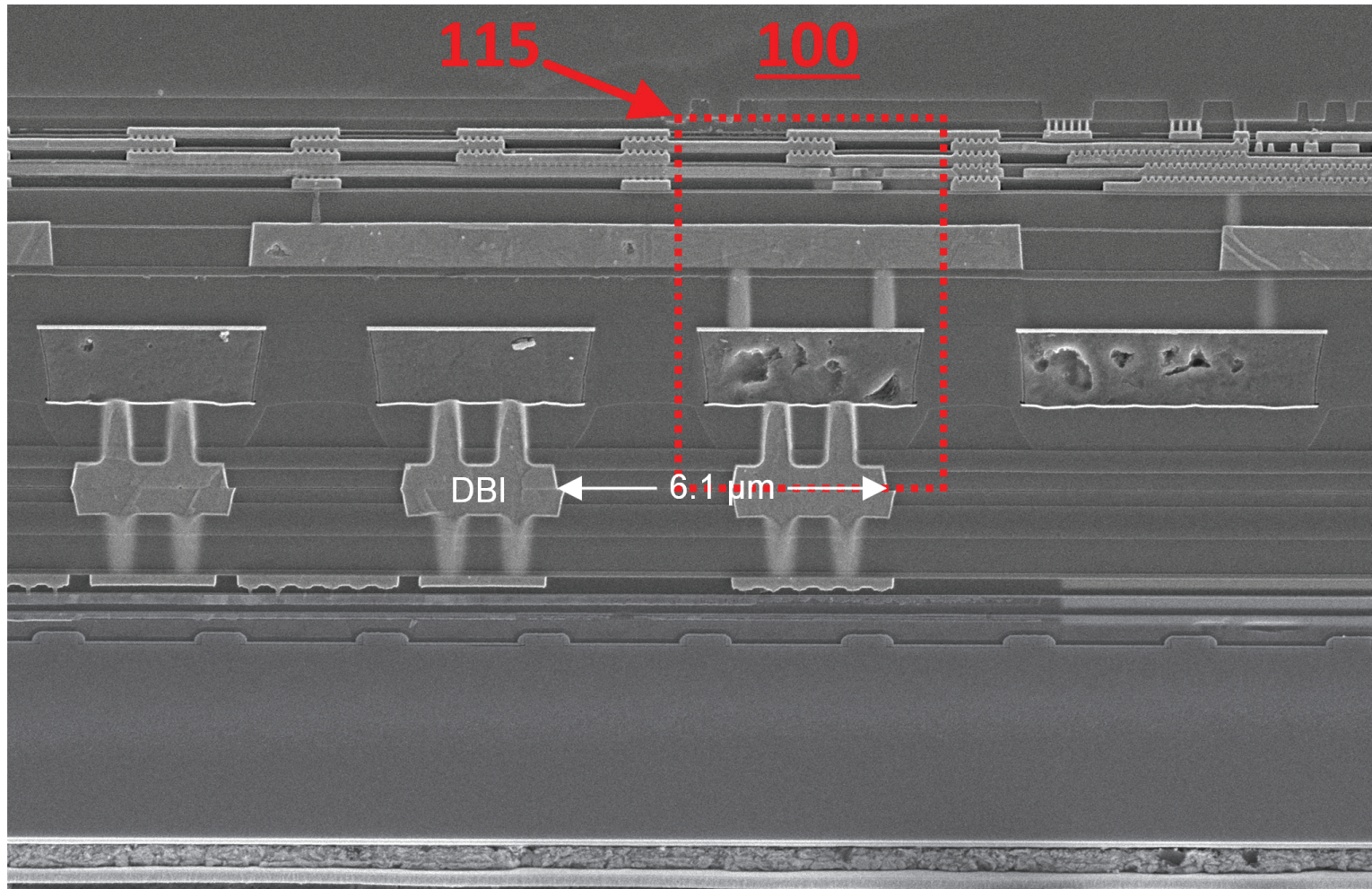
The ISP Si substrate (labeled 100) is provided.



Claim 1

A method, comprising: providing a first substrate; **forming circuitry including a metal interconnection over the first substrate;** forming a photodiode in a crystalline semiconductor layer of a second substrate; forming an ion implantation isolation layer in the photodiode; bonding the first substrate to the second substrate to connect the photodiode to the metal interconnection; and removing a lower portion of the second substrate to expose the photodiode, wherein forming the photodiode comprises: forming a second conduction type conduction layer in the crystalline semiconductor layer; and forming a first conduction type conduction layer over the second conduction type conduction layer, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer over the first conduction type conduction layer, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.

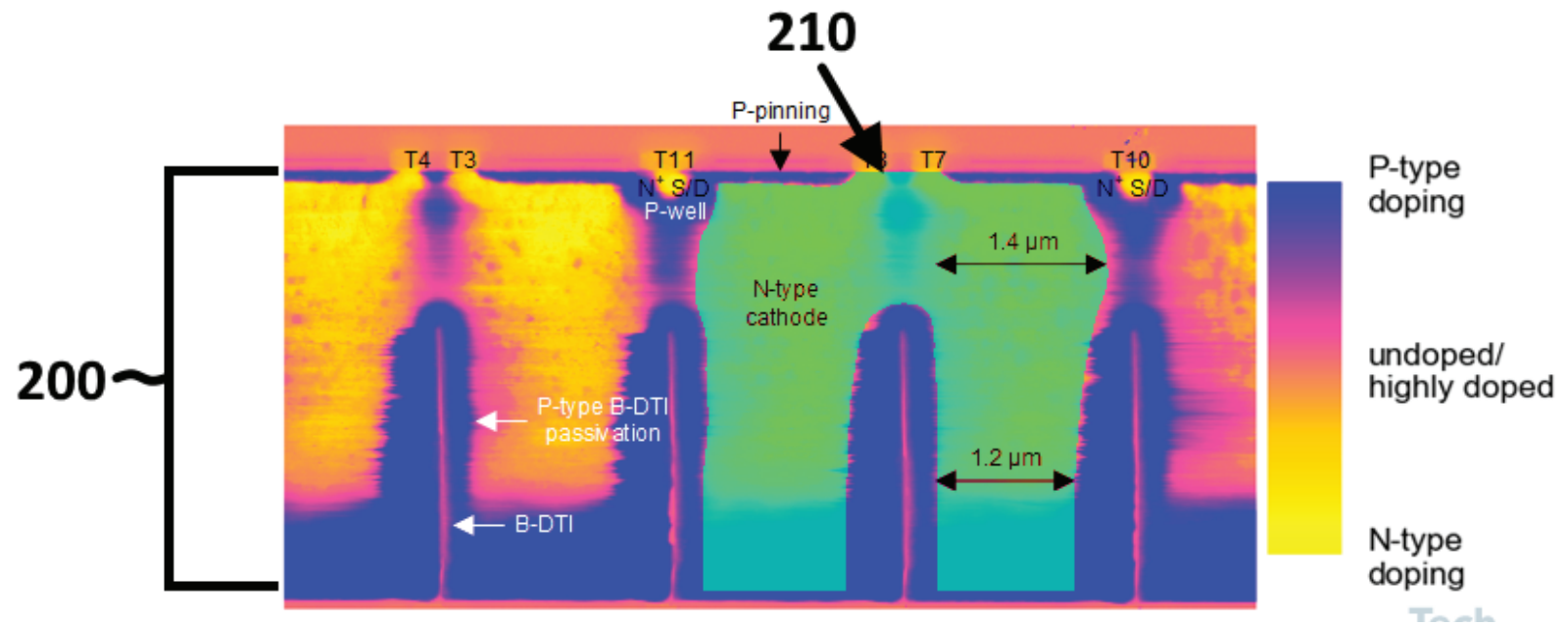
ISP metal interconnects (dotted red outline, labeled 115) are formed over ISP Si substrate 100. ISP metal interconnects 115 include metal pads and plugs. Note that the orientation of the figure is “upside down” relative to when ISP metal interconnect 115 is formed over the first substrate. The ISP DBI, and/or any and all of the ISP metal pads and plugs at metal levels 1 through 7 (ISP M1-M7) connected to the ISP DBI, may correspond to the claimed “metal interconnection,” since they are formed over ISP Si substrate 100.



Claim 1

A method, comprising: providing a first substrate; forming circuitry including a metal interconnection over the first substrate; **forming a photodiode in a crystalline semiconductor layer of a second substrate**; forming an ion implantation isolation layer in the photodiode; bonding the first substrate to the second substrate to connect the photodiode to the metal interconnection; and removing a lower portion of the second substrate to expose the photodiode, wherein forming the photodiode comprises: forming a second conduction type conduction layer in the crystalline semiconductor layer; and forming a first conduction type conduction layer over the second conduction type conduction layer, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer over the first conduction type conduction layer, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.

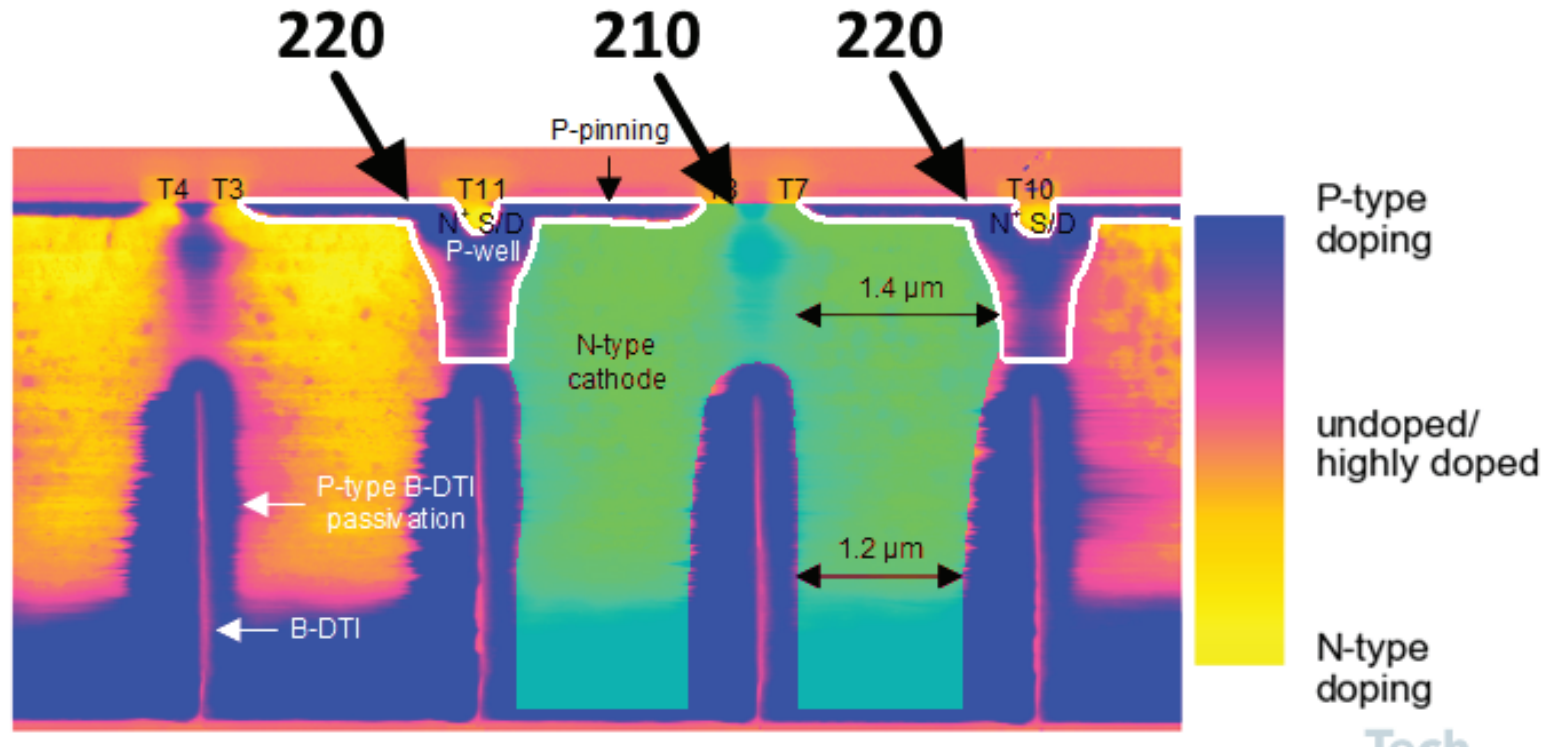
A photodiode (labeled 210) is formed in CIS Si substrate (labeled 200).



Claim 1

A method, comprising: providing a first substrate; forming circuitry including a metal interconnection over the first substrate; forming a photodiode in a crystalline semiconductor layer of a second substrate; **forming an ion implantation isolation layer in the photodiode**; bonding the first substrate to the second substrate to connect the photodiode to the metal interconnection; and removing a lower portion of the second substrate to expose the photodiode, wherein forming the photodiode comprises: forming a second conduction type conduction layer in the crystalline semiconductor layer; and forming a first conduction type conduction layer over the second conduction type conduction layer, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer over the first conduction type conduction layer, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.

An isolation layer (labeled 220) of P-type impurity ions is formed in photodiode 210. Two regions of P-type impurity ions collectively correspond to isolation layer 220: a P-type implant isolation layer, and a P-type pinning layer. Isolation layer 220 isolates pixels from each other.

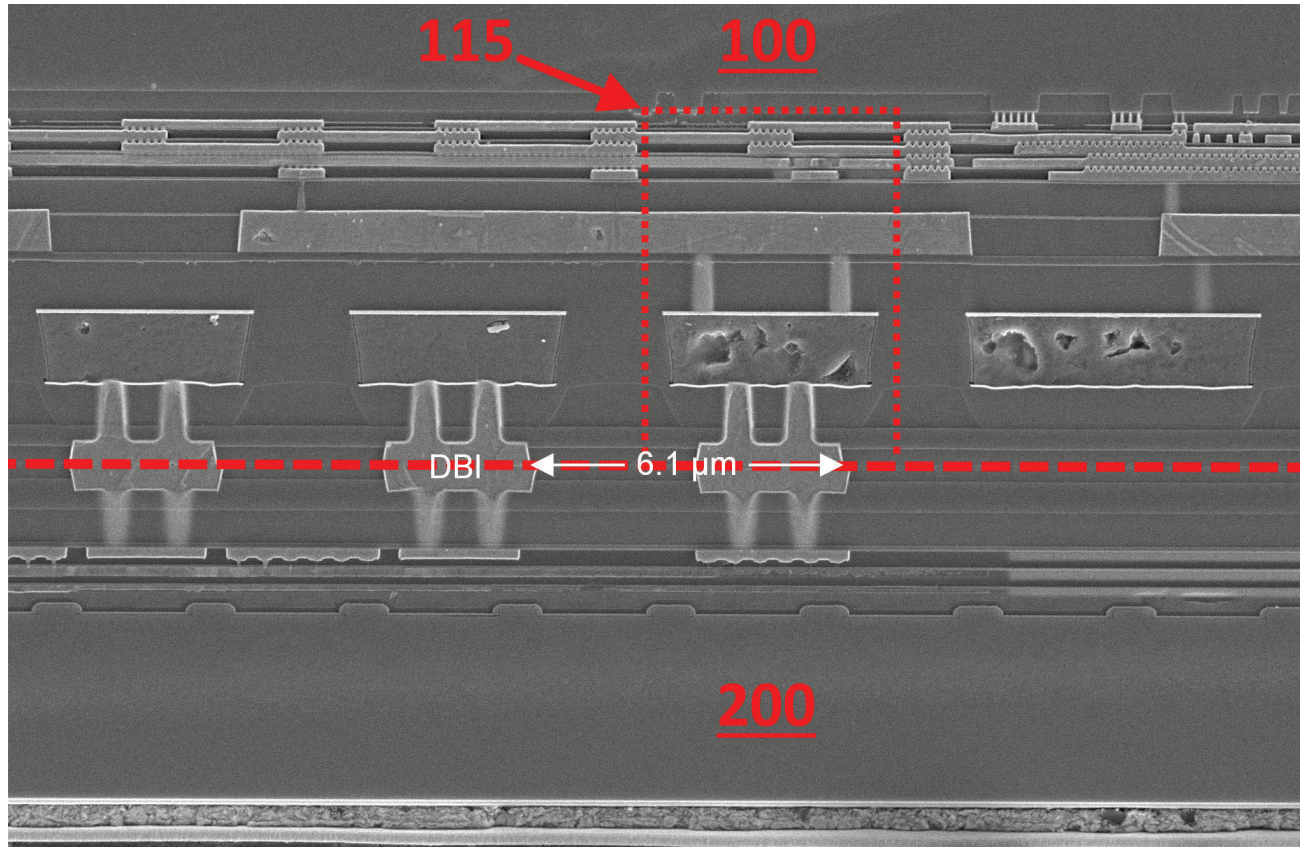


Claim 1

A method, comprising: providing a first substrate; forming circuitry including a metal interconnection over the first substrate; forming a photodiode in a crystalline semiconductor layer of a second substrate; forming an ion implantation isolation layer in the photodiode; **bonding the first substrate to the second substrate to connect the photodiode to the metal interconnection;** and removing a lower portion of the second substrate to expose the photodiode, wherein forming the photodiode comprises: forming a second conduction type conduction layer in the crystalline semiconductor layer; and forming a first conduction type conduction layer over the second conduction type conduction layer, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer over the first conduction type conduction layer, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.

The ISP and CIS dies are bonded together, and thus, corresponding ISP Si substrate 100 and CIS Si substrate 200 are bonded together. The bonding facilitates electrically connecting the photodiode and ISP metal interconnects 115. The figure depicts a column DBI which electrically connects a column out transistor of a pixel of the photodiode to ISP metal interconnects 115.

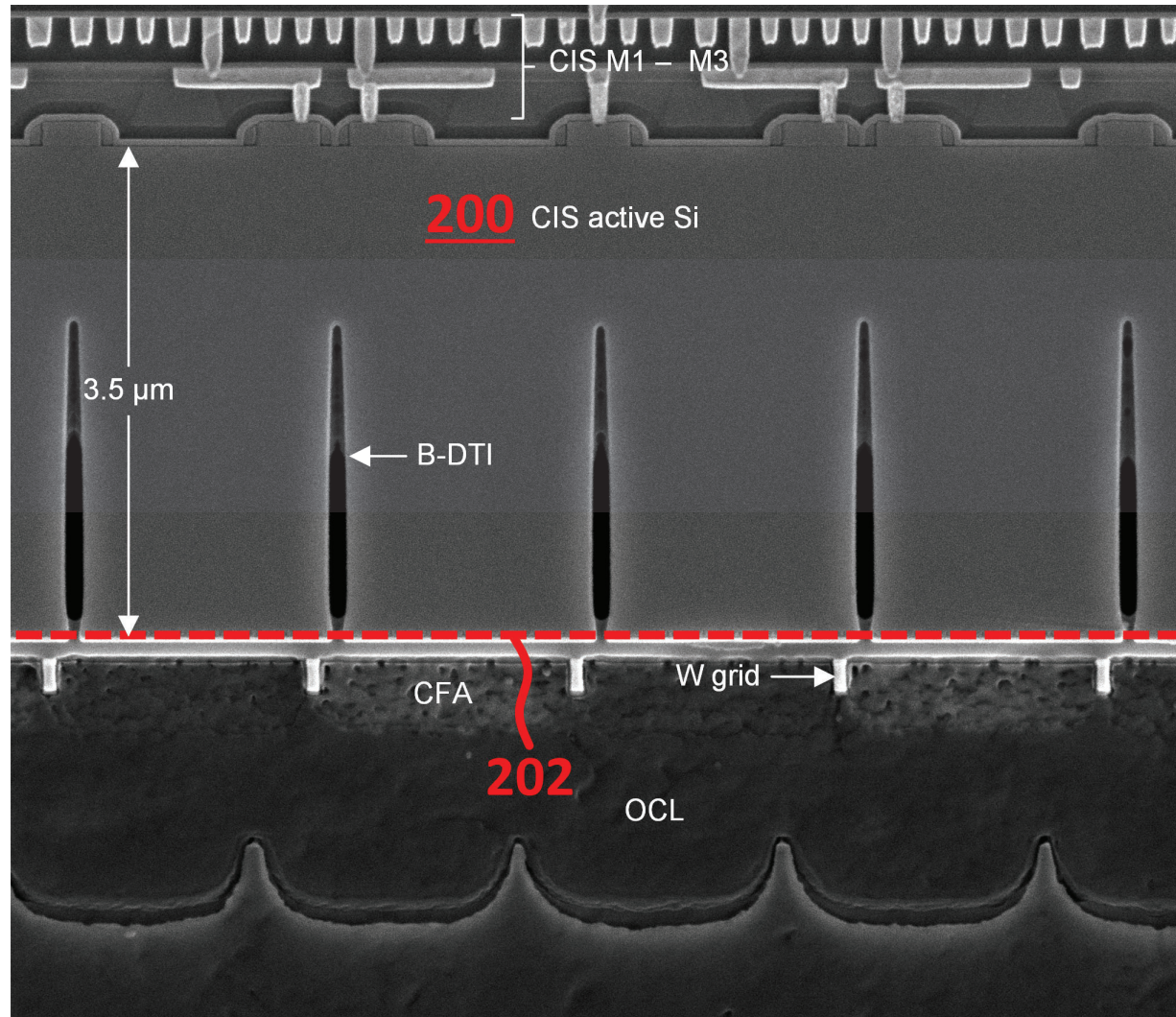
The photodiode and ISP metal interconnects 115 are electrically connected concurrently when ISP Si substrate 100 and CIS Si substrate 200 are bonded.



Claim 1

A method, comprising: providing a first substrate; forming circuitry including a metal interconnection over the first substrate; forming a photodiode in a crystalline semiconductor layer of a second substrate; forming an ion implantation isolation layer in the photodiode; bonding the first substrate to the second substrate to connect the photodiode to the metal interconnection; **and removing a lower portion of the second substrate to expose the photodiode**, wherein forming the photodiode comprises: forming a second conduction type conduction layer in the crystalline semiconductor layer; and forming a first conduction type conduction layer over the second conduction type conduction layer, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer over the first conduction type conduction layer, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.

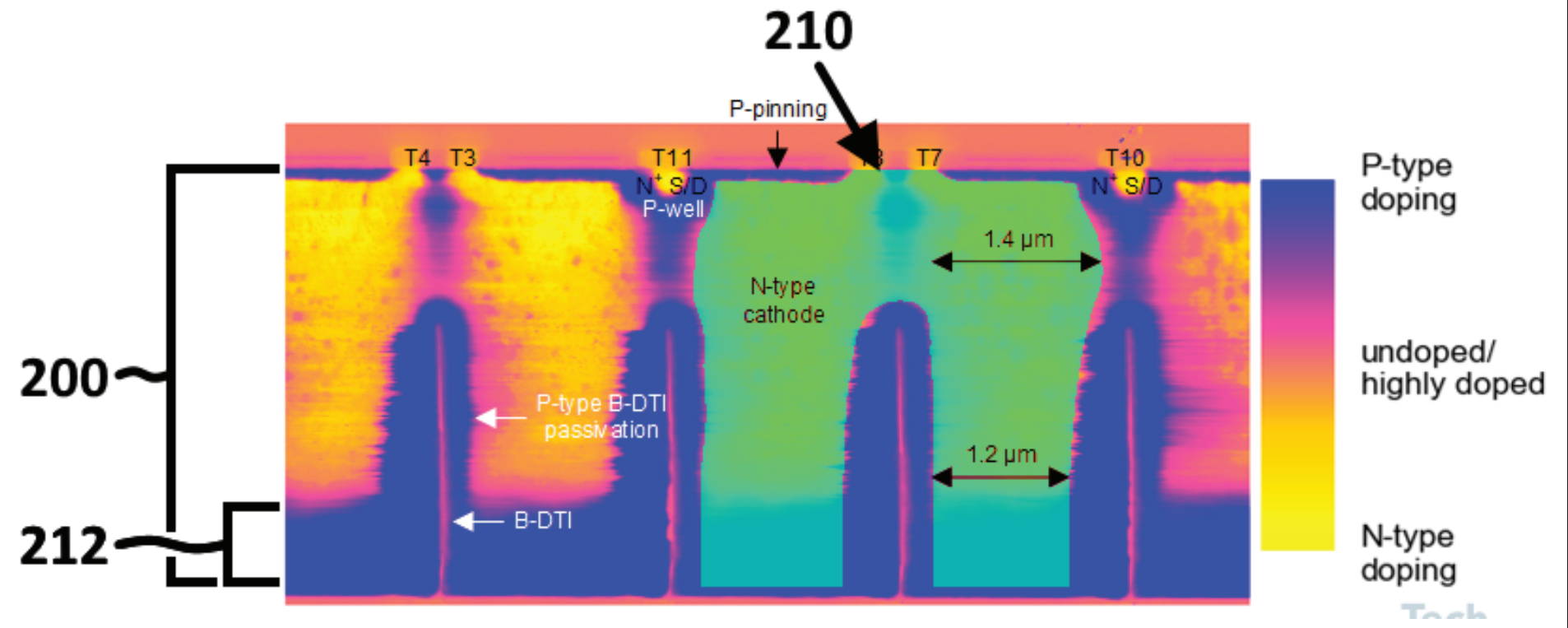
A lower portion of CIS Si substrate 200 is removed, thinning CIS Si substrate 200 down to back surface 202. The thinning exposes the photodiode to facilitate subsequent processing, including formation of B-DTIs, anti-reflective (AR) layers, a tungsten (W) grid, a color filter array (CFA), and on-chip lenses (OCLs).



Claim 1

A method, comprising: providing a first substrate; forming circuitry including a metal interconnection over the first substrate; forming a photodiode in a crystalline semiconductor layer of a second substrate; forming an ion implantation isolation layer in the photodiode; bonding the first substrate to the second substrate to connect the photodiode to the metal interconnection; and removing a lower portion of the second substrate to expose the photodiode, **wherein forming the photodiode comprises: forming a second conduction type conduction layer in the crystalline semiconductor layer;** and forming a first conduction type conduction layer over the second conduction type conduction layer, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer over the first conduction type conduction layer, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.

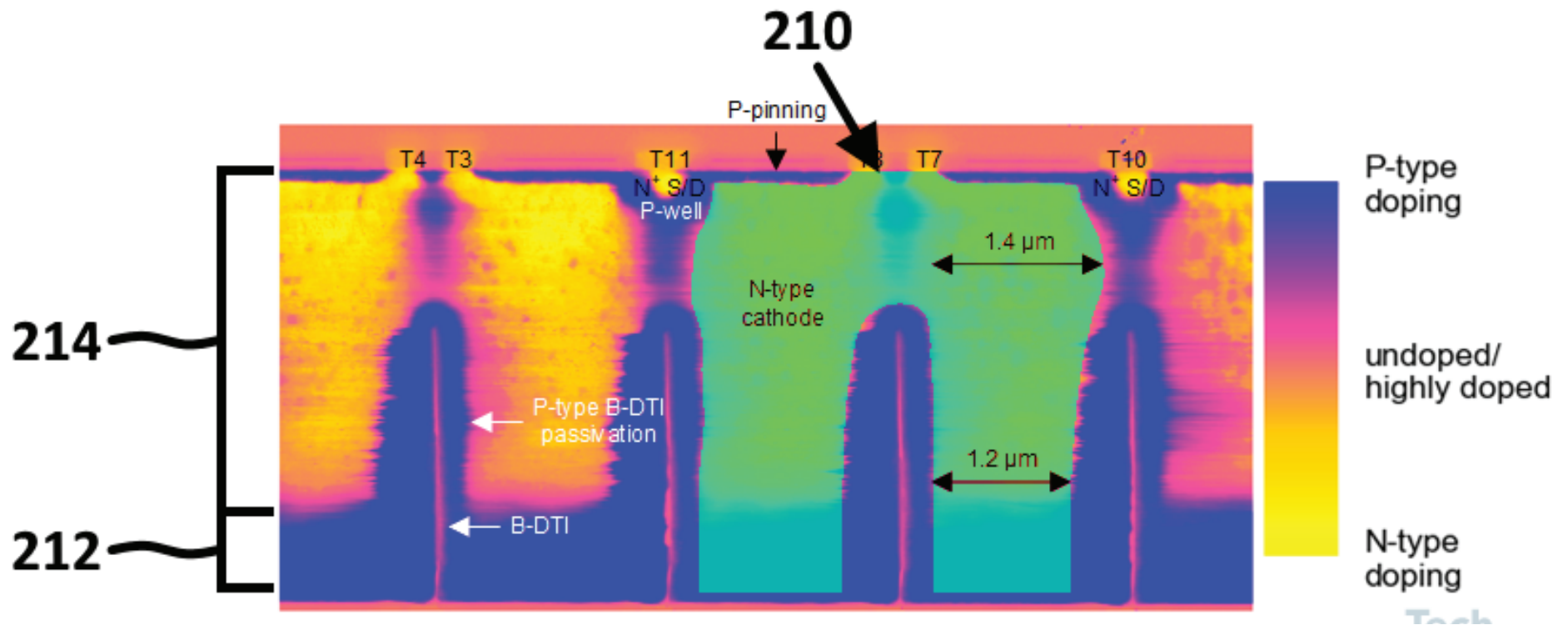
A layer (labeled 212) having P-type conduction is formed in CIS Si substrate 200. Layer 212 is utilized in forming photodiode 210.



Claim 1

A method, comprising: providing a first substrate; forming circuitry including a metal interconnection over the first substrate; forming a photodiode in a crystalline semiconductor layer of a second substrate; forming an ion implantation isolation layer in the photodiode; bonding the first substrate to the second substrate to connect the photodiode to the metal interconnection; and removing a lower portion of the second substrate to expose the photodiode, wherein forming the photodiode comprises: forming a second conduction type conduction layer in the crystalline semiconductor layer; **and forming a first conduction type conduction layer over the second conduction type conduction layer**, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer over the first conduction type conduction layer, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.

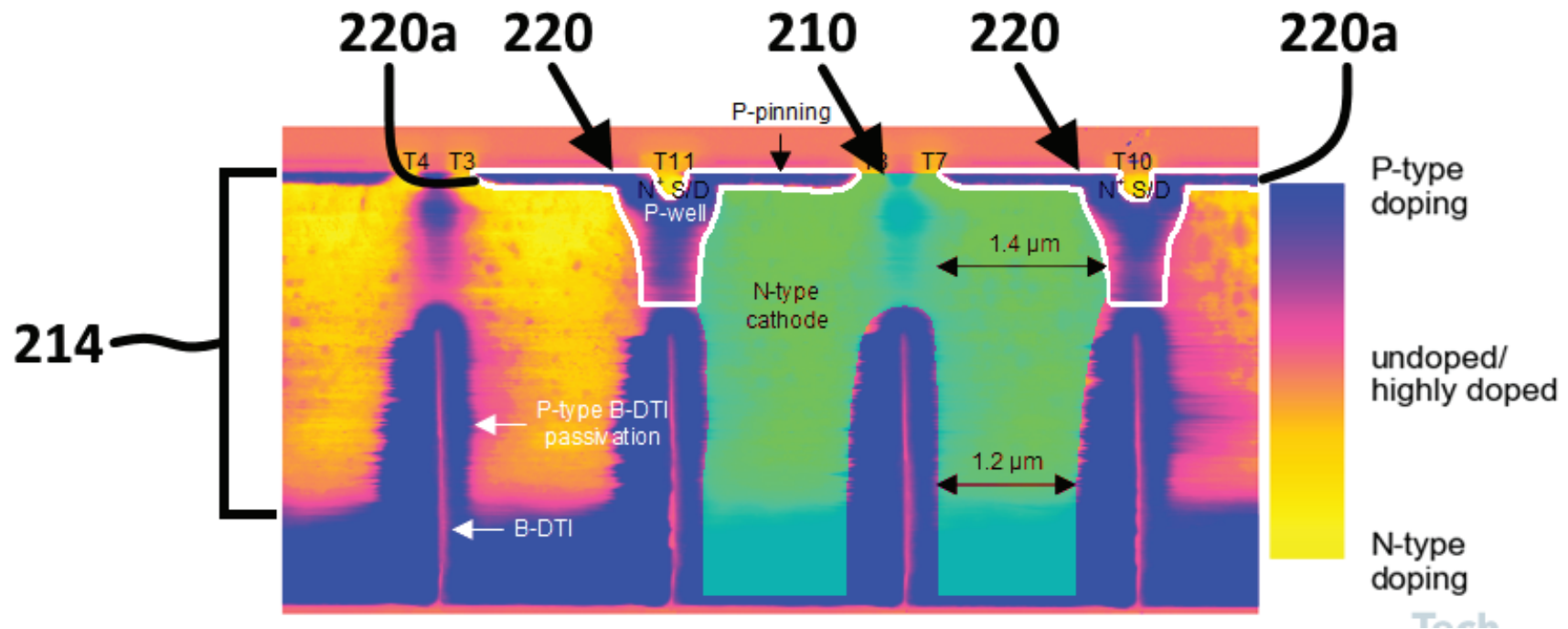
A layer (labeled 214) having N-type conduction is formed over second conduction type conduction layer 212. Layer 214 is utilized in forming photodiode 210.



Claim 1

A method, comprising: providing a first substrate; forming circuitry including a metal interconnection over the first substrate; forming a photodiode in a crystalline semiconductor layer of a second substrate; forming an ion implantation isolation layer in the photodiode; bonding the first substrate to the second substrate to connect the photodiode to the metal interconnection; and removing a lower portion of the second substrate to expose the photodiode, wherein forming the photodiode comprises: forming a second conduction type conduction layer in the crystalline semiconductor layer; and forming a first conduction type conduction layer over the second conduction type conduction layer, **wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer over the first conduction type conduction layer**, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.

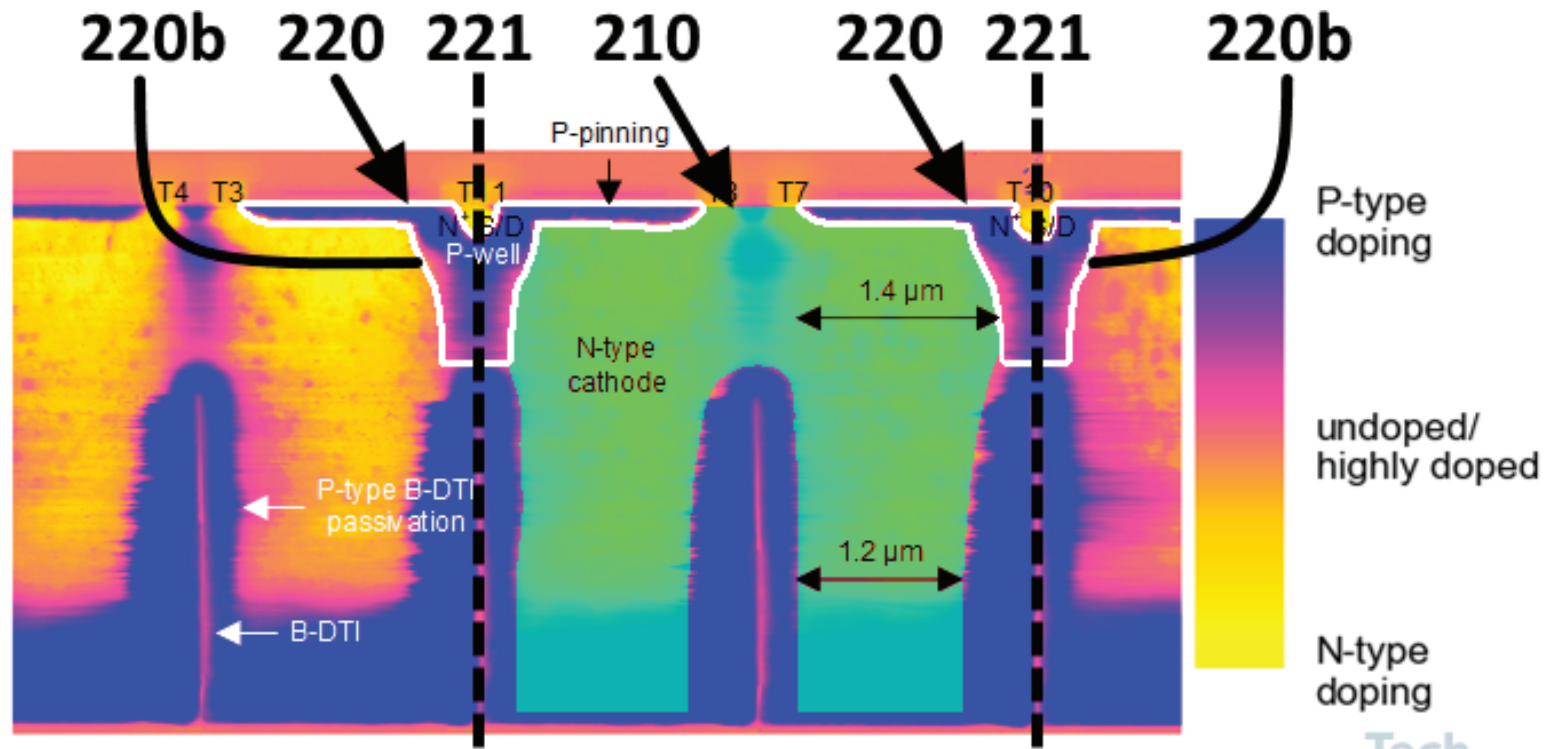
Forming ion implantation isolation layer 220 in photodiode 210 comprises forming a pinning layer (labeled 220a) of P-type impurity ions over first conduction type conduction layer 214.



Claim 1

A method, comprising: providing a first substrate; forming circuitry including a metal interconnection over the first substrate; forming a photodiode in a crystalline semiconductor layer of a second substrate; forming an ion implantation isolation layer in the photodiode; bonding the first substrate to the second substrate to connect the photodiode to the metal interconnection; and removing a lower portion of the second substrate to expose the photodiode, wherein forming the photodiode comprises: forming a second conduction type conduction layer in the crystalline semiconductor layer; and forming a first conduction type conduction layer over the second conduction type conduction layer, wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer over the first conduction type conduction layer, **wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.**

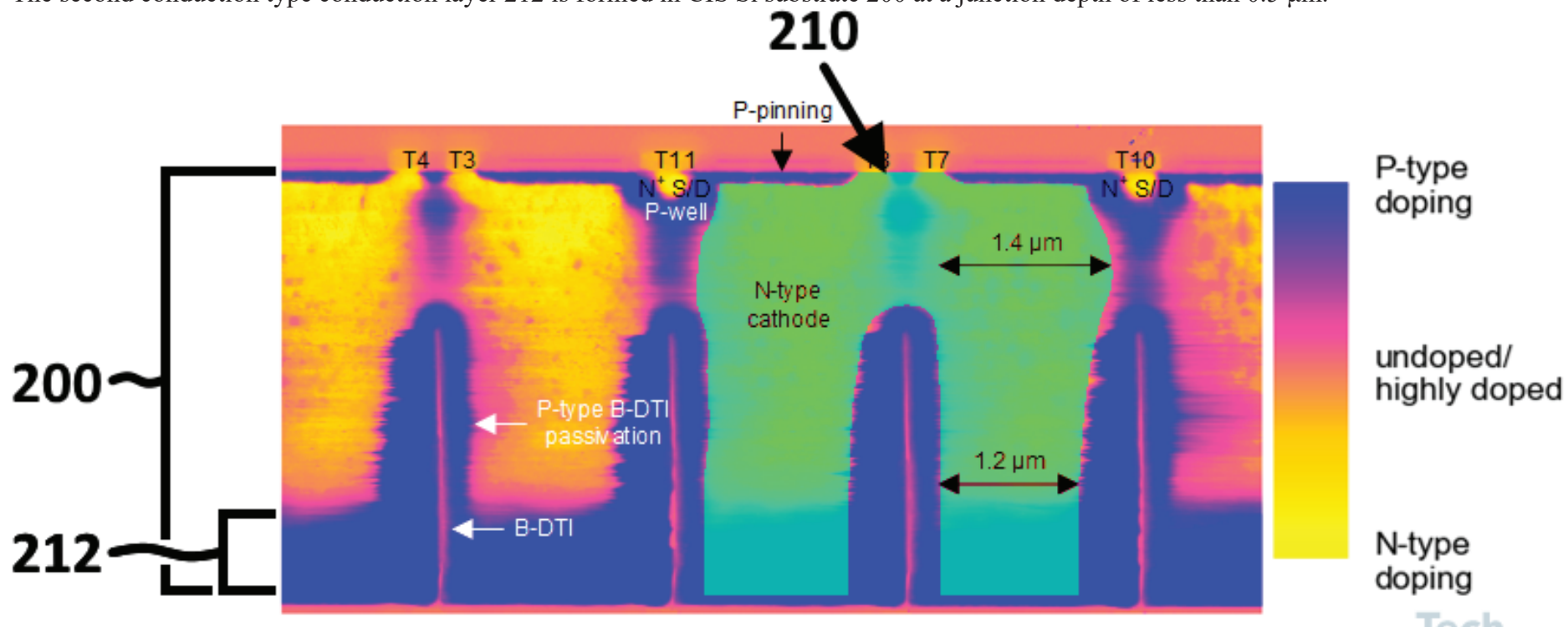
Forming ion implantation isolation layer 220 in photodiode 210 comprises forming an isolation layer (labeled 220b) of P-type impurity ions at pixel interfaces (labeled 221) of photodiode 210.



Claim 2

The method of claim 1, comprising forming the second conduction type conduction layer at a junction depth of less than approximately 0.5 μm.

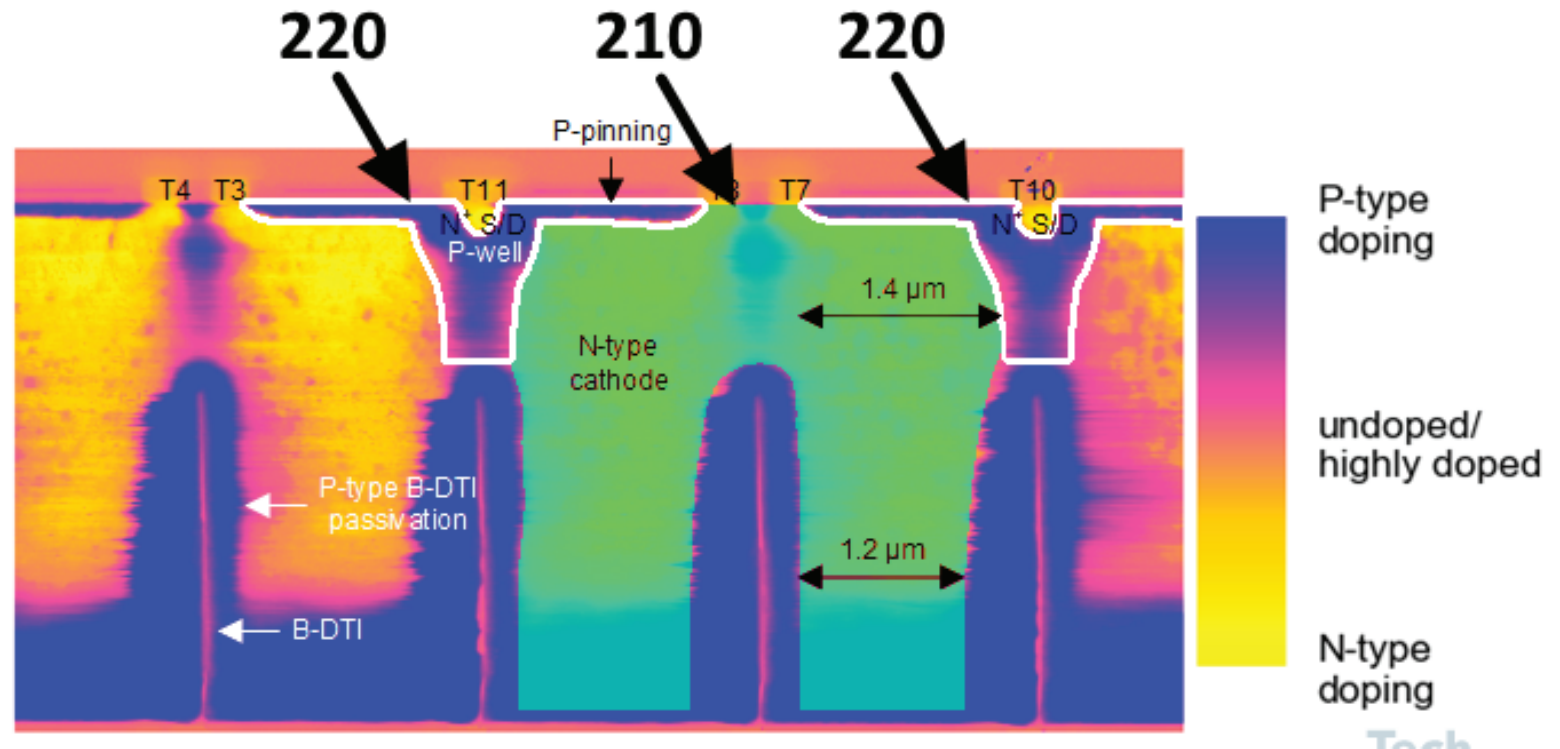
The second conduction type conduction layer 212 is formed in CIS Si substrate 200 at a junction depth of less than 0.5 μm .



Claim 4

The method of claim 1, comprising forming the ion implantation isolation layer over at least one of a side of the photodiode and a bottom of the photodiode.

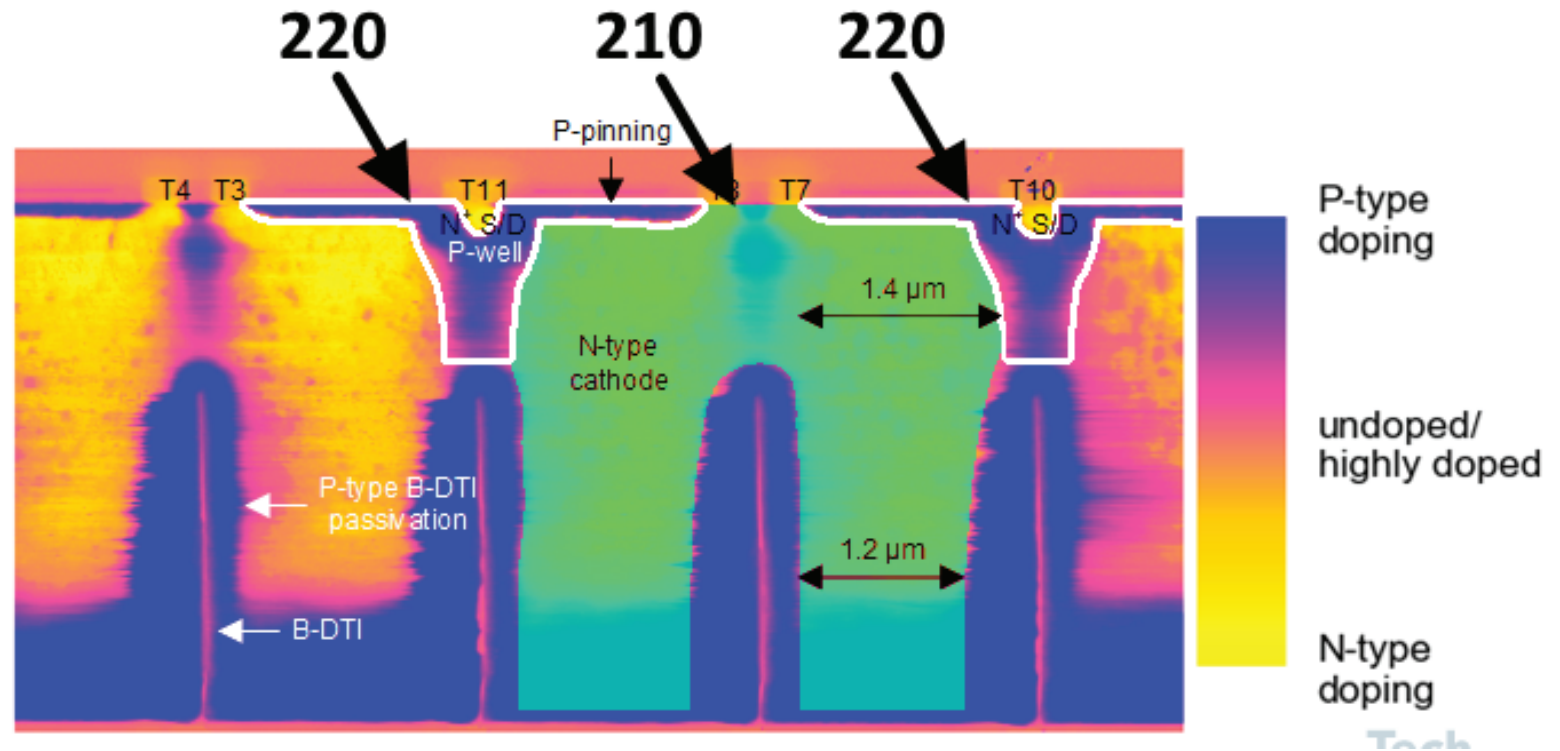
The ion implantation isolation layer 220 is formed over at least one of a side and a bottom of the photodiode 210.



Claim 5

The method of claim 1, wherein the ion implantation isolation layer comprises a P0 layer.

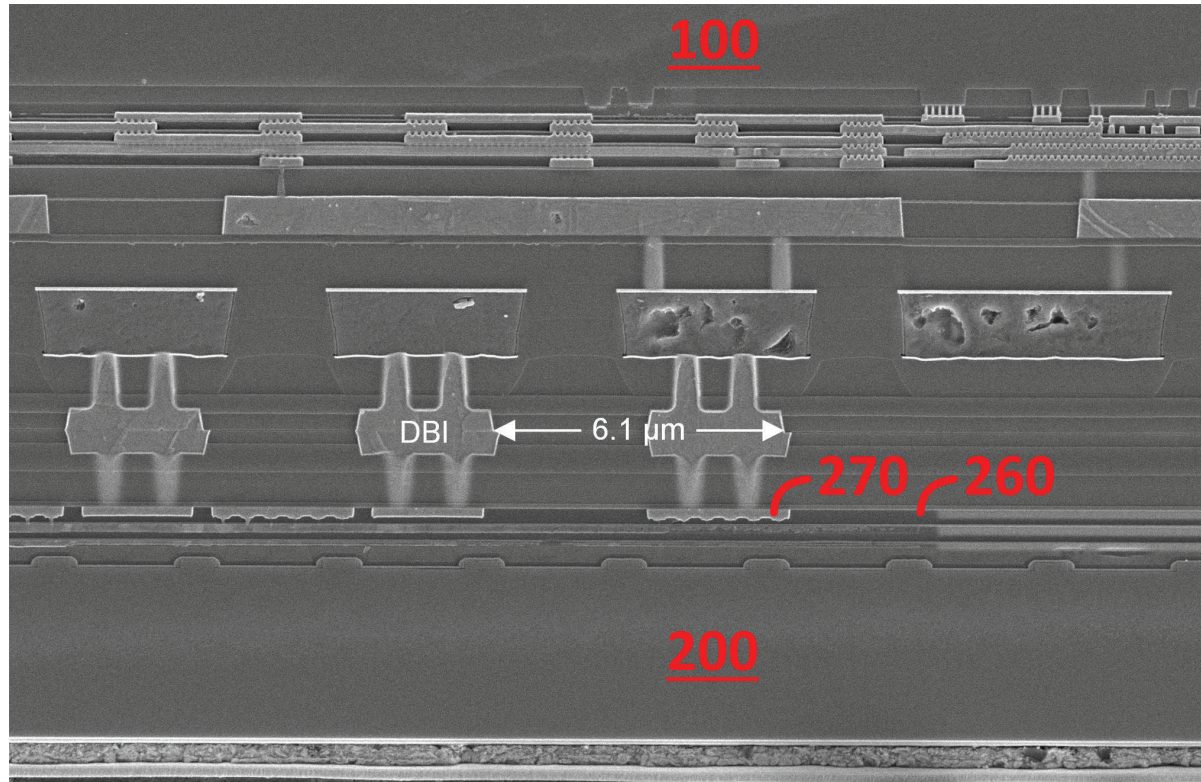
The ion implantation isolation layer 220 includes a P0 layer.

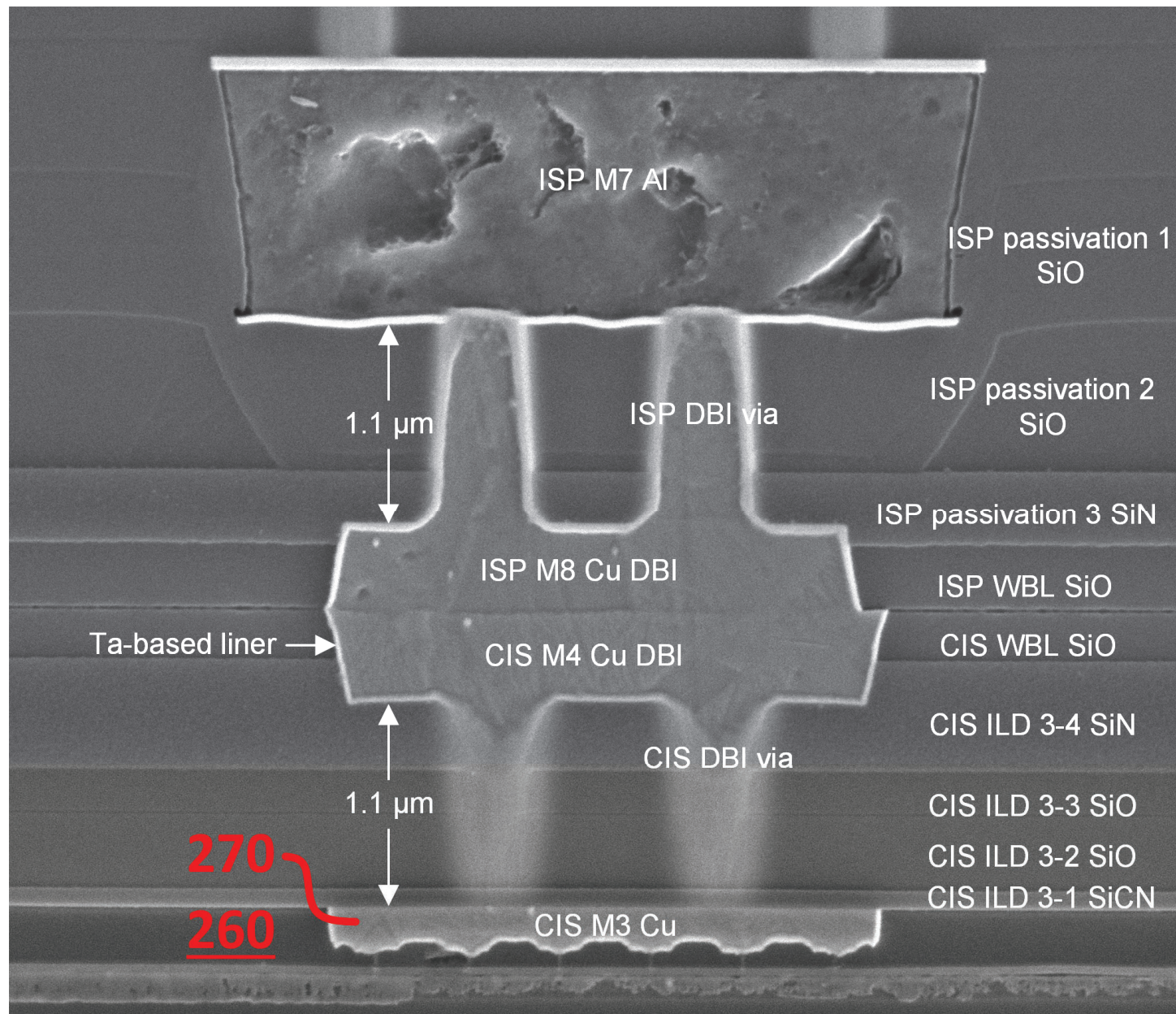


Claim 6

The method of claim 1, comprising: forming a dielectric over the photodiode of the second substrate before bonding the first and second substrates; and forming a metal pad in the dielectric.

An interlayer dielectric (CIS ILD, labeled 260) is formed over the photodiode of the CIS Si substrate 200 before bonding ISP Si substrate 100 and CIS Si substrate 200. A pad of CIS metal interconnect (labeled 270) at metal level 3 (CIS M3) is formed in CIS ILD 260.

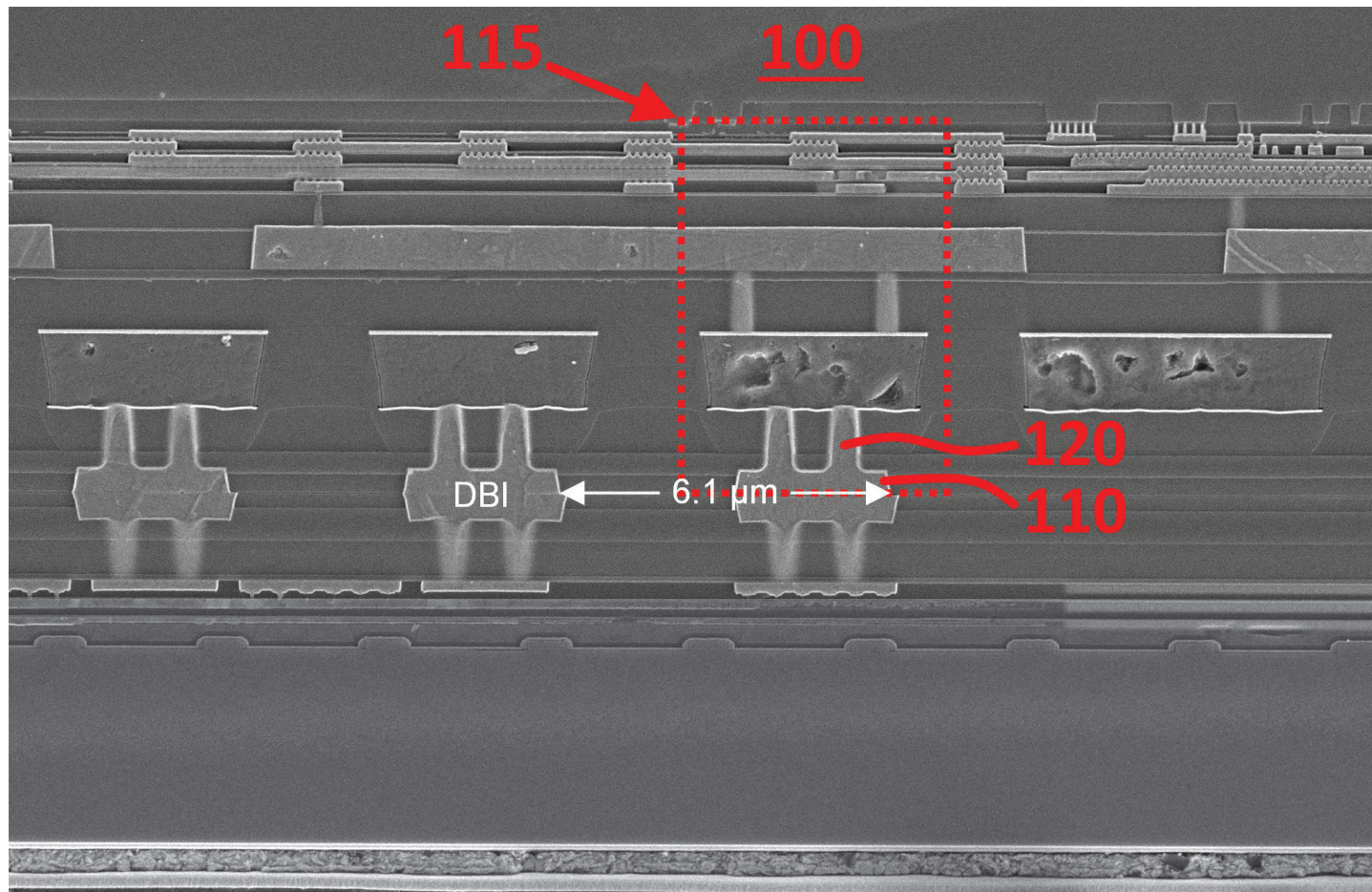


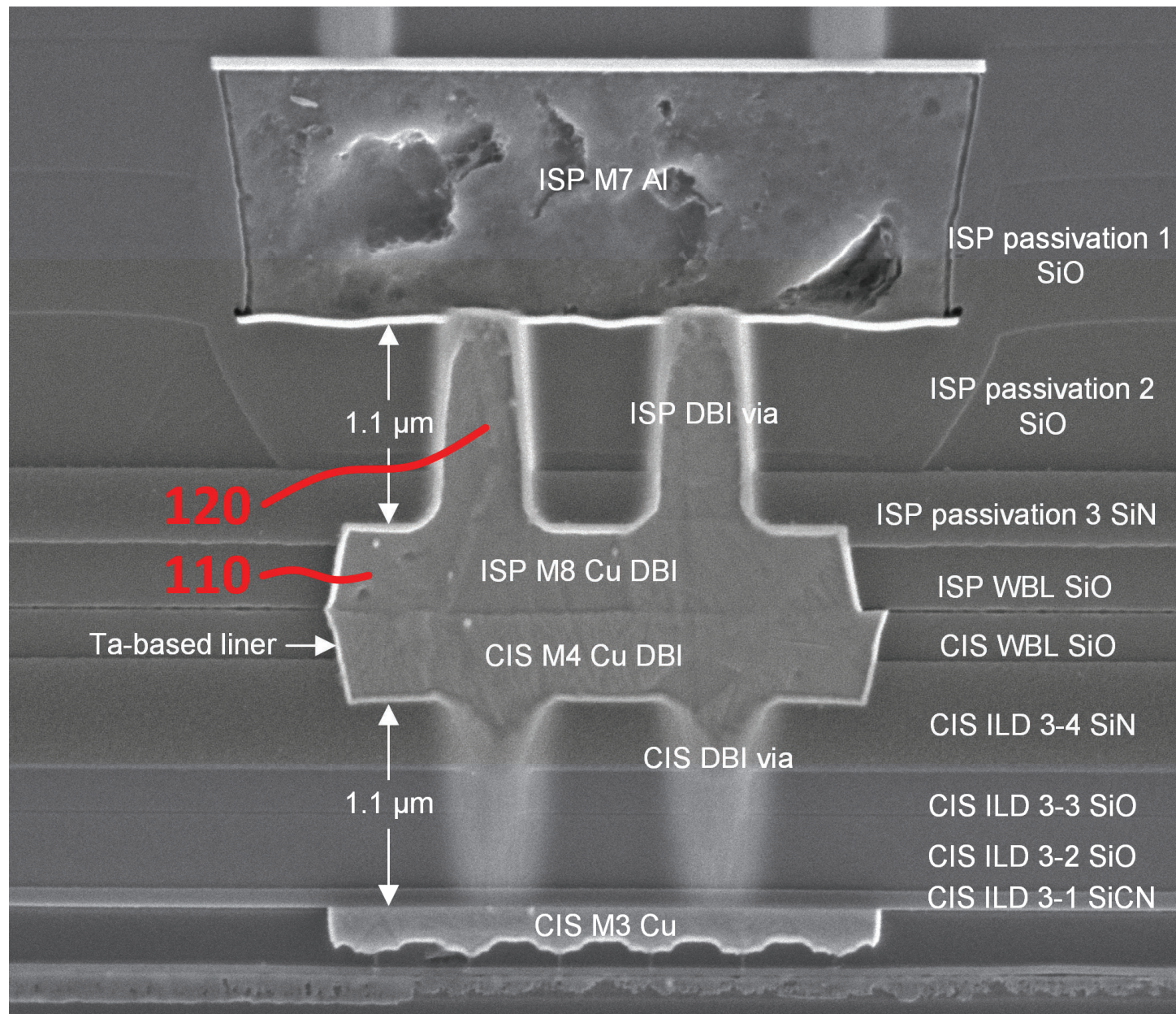


Claim 8

The method of claim 1, wherein forming the circuitry including the metal interconnection comprises forming a metal and a plug over the first substrate.

Forming ISP metal interconnects 115 comprises forming a metal (labeled 110) and a plug (labeled 120) over ISP Si substrate 100.





Claim 9

The method of claim 1, wherein the second conduction type second ion implantation isolation layer is disposed to directly contact on a top surface of the second conduction type first ion implantation isolation layer and a bottom surface of the second conduction type conduction layer.

The second conduction type isolation layer 220b is disposed to directly contact on a top surface of the second conduction type first ion implantation isolation layer 220a and the bottom surface of the second conduction type conduction layer 212.

