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Progress in the development of Vertically Integrated Sensor Arrays

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ABSTRACT

The demand continues to grow for small, compact imaging sensors, which include new capabilities, such as response in multiple spectral bands, increased sensitivity, wide high dynamic range, and operating at room temperature. These goals are dependant upon novel concepts in sensor technology, especially advanced electronic processing integrated with the sensor. On-focal plane processing is especially important to realize the full potential of the sensor. Since the area available for focal plane processing is extremely limited, a new paradigm in sensor electronic read-out technology is necessary to bridge the gap between multi-functional, high performance detector arrays and the off-focal plane processing. The Vertically Integrated Sensor Array (VISA) Program addresses this need through development of pixel-to-pixel interconnected silicon processors at the detector, thus expanding the area available for signal and image processing. The VISA Program addresses not only the array interconnection technology, but also investigates circuit development adapted to this new three-dimensional focal plane architecture. This paper reviews progress in the first phase of the program and outlines direction for demonstrations of vertically integrated sensor arrays.

1. INTRODUCTION

Sensor technology has advanced substantially in several areas, from applications for man-portable systems to high performance systems for vehicles and aircraft. Performance requirements continue to increase as the need expands for multiple sensor types; small, common aperture integrated sensors; on-focal plane functions for local area processing; and sensors that adapt to scene content. At the same time, users want sensor cost to decrease or remain constant, driving technology toward more integrated solutions. Read-out technology is becoming the major barrier to realization of these sophisticated imaging sensors with the performance and functions desired by the user.

The three-dimensional read-out integrated circuit (ROIC) addresses this barrier. This technology enables pixel to pixel interconnections at the detector and opens possibilities for increased functionality on the focal plane array. The VISA Program initiated by DARPA in 2001 addresses innovative approaches to realize these advanced read-out circuits.

The first phase of the program has demonstrated feasibility of the interconnection approaches, completed designs and test chip demonstrations for high dynamic range circuits, and investigated applications for maximum impact of VISA technology. Multiple contractors, each with a unique via and interconnection approach, are focused on the development of high aspect ratio vias at each pixel on the focal plane array, forming a three-dimensional read-out integrated circuit. The via and interconnection technology developed in the first phase of the VISA Program is compatible with high density imaging arrays, with 30 μm pixel-to-pixel spacing.

In parallel with via and interconnection development, large dynamic range analog-to-digital (A/D) converter circuits compatible with a 30 μm unit cell were demonstrated. These designs showed 16 – 18 bits at 1 KHz conversion rate with linearity better than 0.01 %.

The next phase of the program will integrate the via / interconnect technology with the circuits designed in Phase I, demonstrating the improved sensor performance with the VISA technology. Focal plane demonstrations are planned to show elevated operating temperature for three-to-five micrometer arrays; increased storage capacity for eight-to-ten micrometer arrays; and imaging in the presence of high intensity sources. In addition, plans include a ladar array with

less than one inch range resolution. These sensor demonstrations, planned for December 2005, will show the potential of the VISA approach to focal plane read-out circuits.

2. PROGRAM RATIONALE AND APPLICATIONS

The VISA technology provides a new tool to the system designer, opening options for improved performance and new capabilities in several areas, as shown in Table 1. The addition of processing layers at the detector can have an immediate impact on system performance, as well as providing technology for growth into more advanced imaging functions.

Increased Charge Storage	Higher operating temperature detectors
	Full utilization of available signal current
Local Processing at the Detector	On-focal plane windowing functions
	Decision making for large array read-out
Parallel Signal Manipulation	Frame-to-frame correlations
	Expanded multi-spectral FPAs with spatially registered bands

Table 1: The VISA technology provides an enabling technology for higher performance focal plane arrays, including advanced processing at the detector.

The additional charge storage at the detector offers an immediate impact on system performance. The need for a low noise amplifier and signal conditioning at the detector consumes area in the read-out unit cell, leaving reduced area for charge storage. The limited area available for charge storage area significantly limits detector sensitivity, especially for long wave length detectors with cut-off greater than ten micrometers. The VISA technology provides the opportunity to overcome this obstacle by adding read-out circuit area beneath the detector, which can be devoted to charge storage. For a twenty micron unit cell, the charge storage area increases from 10^8 to as large as 10^{10} carriers, allowing full utilization of the available signal from the detector, increasing sensitivity by nearly a factor of ten (X10) for long wave infrared imaging.

For 3-5 um detectors, the increased charge storage at the detector allows operation at higher temperature. The operating temperature of 3-5 um devices may be increased from approximately 100K to 200K, opening possibilities for battery operated coolers.

The VISA technology also offers the potential for longer term advances in innovative signal processing at the detector. The expanded processing area provides the opportunity to integrate windowing functions at the detector. The windowing technique can be implemented to detect changes from frame to frame, and only new information read-out from the focal plane. The smart windowing function provides elemental decision making at the focal plane, which is the enabling technology for efficient read-out of large arrays, while keeping power to a minimum.

Three-dimensional architecture at the detector also opens doors to higher performance detector arrays, especially the development of detector layers sensitive in multiple bands. Currently, dual band, pixel-to-pixel registered detectors have been demonstrated. The VISA technology offers the potential to expand the number of spectral bands to three or potentially a larger number of bands.

3. APPROACHES TO THREE-DIMENSIONAL INTEGRATION

There are several methods to implement the three-dimensional read-out circuit architecture, and realize the increased processing power at the detector. Generic approaches include stacking individual silicon die, a die-on-die approach; wafer-to-wafer bonding; and the integration of individual die-on-wafer. The ultimate goal of each of these approaches is that, to the user, the three-dimensional integrated circuit be indistinguishable from a conventional read-out, except for the increased processing power available.

The die-on-die approach provides the flexibility to experimentally validate new circuit designs on an individual die. The individual die can be tested and qualified before integration and only acceptable die used in the integration process. In the wafer-to-wafer approach, wafers are precision aligned and bonded, and the via formation process performed wafer scale. Although the wafers can be tested before wafer bonding, the designer must rely upon the statistics of wafer yield to achieve stacks of workable integrated circuits. With process controls in place for via formation and conformal deposition of the interconnection metalization, the yield of the three-dimensional wafer stack can be high. In each approach, circuit production must meet application needs for cost and volume.

4. VISA TECHNOLOGY

Figure 1 illustrates the VISA technology concept. A detector array is hybrid bump-bonded to a silicon layer that provides input circuits appropriate for the sensor. Monolithic implementations combining the input and the sensor – especially feasible with silicon sensors – are not precluded. The input circuit layer is thinned and vias are etched and metallized in order to make pixel level interconnects to the second layer of silicon circuits. Such a layer may provide, for example, analog non-uniformity correction, large capacitance for charge storage, or threshold timing and latching circuits that may be needed in a LADAR application. The second layer is thinned also and pixel-level interconnects are provided to the circuitry on a third level. The third level circuits may include color processing functions following non-uniformity correction in the second level. The final level (fourth level in figure 1) in most cases is anticipated to be used for converting the analog signals to digital format. This will allow for significant expansion of the dynamic range from approximately 14 bits to 20 bits or more.

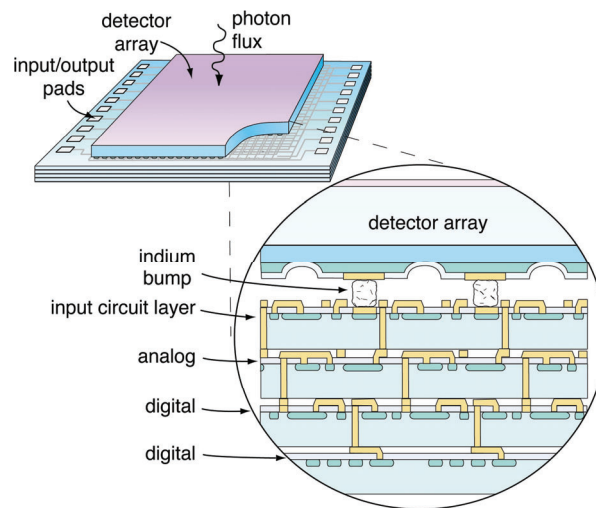


Figure 1 Multiple layers of readout circuits can be embedded underneath a detector array as shown in this diagram that illustrates four such layers. Each layer is fabricated in a silicon foundry, tested, and then thinned and glued over the layer below. Small vias are etched and metallized to interconnect the circuits at the pixel level.

Silicon integrated circuit technology had developed techniques for etching, insulating, and metalizing very small, deep trenches in order to make compact capacitors for solid-state memory chips. This was first accomplished in the mid-1980's with the introduction of some 1 MB DRAM designs. With the introduction of the 4 MB DRAM chip, all manufacturers used this approach. The key materials technology underlying trench formation is reactive ion etching. Gas plasma etching began in the early 1970's, initially for the removal of residual photo resist, and later for deposition and etching of insulators, metals, and silicon. Etching technology was directed at reducing the dimensions of integrated circuit features. This encouraged the development of chemically-reactive etching gas mixtures that provided selective etching of materials as well as anisotropic etching-where etching proceeds vertically into the surface at fast rates, but hardly at all in the lateral direction. Gas plasma chamber designs evolved to produce conditions that yielded maximum anisotropy-low gas pressures and directed beams of activated etching species. The VISA program utilizes reactive plasma etching to produce vias that connect circuitry on the surface of a thinned wafer to circuitry on another wafer below it. Shown in Figure 2 is an example of an etched via with conformal insulator produced by the DRS / MCNC team during the VISA Program.

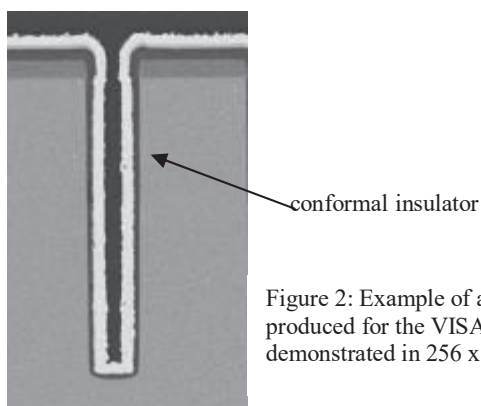


Figure 2: Example of an etched via with conformal insulation produced for the VISA Program. This via technology was demonstrated in 256 x 256 arrays.

Contractors under the VISA program have demonstrated 256 x 256 via arrays – 65,536 interconnections. An example of the via formation process sequence consists of the following steps:

- Thin wafer
- Via etch with reactive plasma
- Deposit insulator on via sidewalls
- Deposit metal on via sidewalls
- Electroplate to fill via
- Planarize surface

The materials and processes must be compatible with integrated circuit technology, since the via process will be done after circuit fabrication. Silicon integrated circuits can withstand temperatures in the range of 450C for brief times. Alignment of the layers must be relatively precise so that the etched via can be opened on the contact pad of the circuitry above, and properly terminates on the contact pad of the circuit below. Each contractor team will develop a unique process sequence for an integrated three-dimensional read-out circuit.

Wide dynamic range circuits are also being developed to increase the number of bits that could be handled by analog to digital converters. An Edan circuit, which is a variation of a sigma delta circuit uses both a coarse and fine A/D. The total number of bits for this circuit is $M = m + \log_2 N$, where N is the clock rate divided by the frame rate and m is the residue quantizer. For a ratio of clock rate to frame rate of 1024 and for a residue quantizer of 10 bits, the Edan circuit can produce 20-bit output resolution. Figure 3 shows this circuit in detail. Figure 4 shows a plot of dynamic range versus frame rate for three different clock rates. As can be seen, today's metric is about 12 bits at 300 Hertz. With the Edan circuit, it is possible to do 20 bits at a 1 kHz frame rate and 16 bits at 10 kHz using a 1 MHz clock rate.

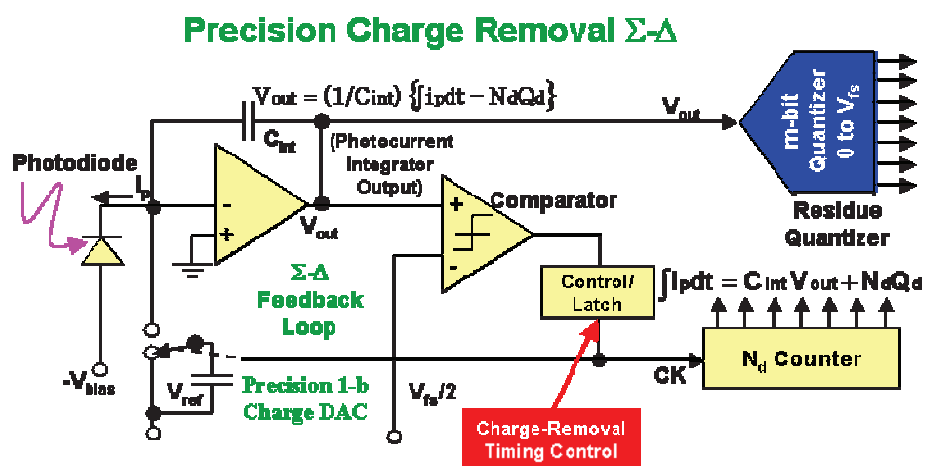


Figure 3: Schematic diagram of the Eden circuit, a variation of a sigma-delta quantizer that can output N+m bits

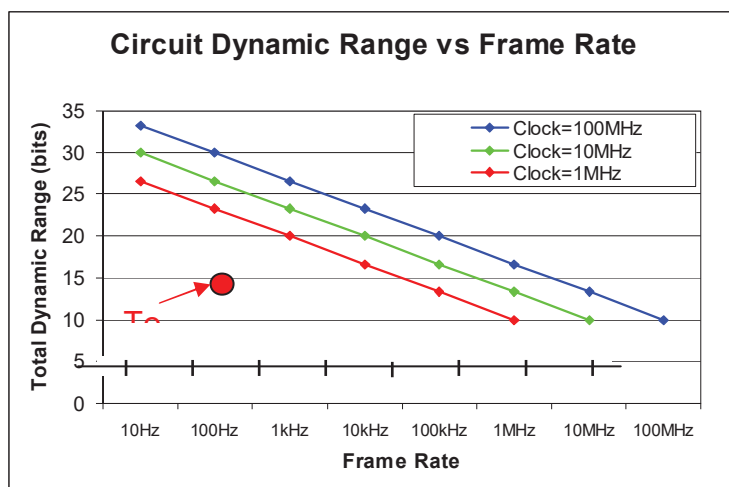


Figure 4: Bit dynamic range as a function of frame rate for three clock rates

5. VISA TECHNOLOGY STATUS

The contractors and their approaches to the three-dimensional read-out technology are outlined in Table 2. The contractors have demonstrated feasibility of the approaches, with measures of success including via and interconnection operability, circuit isolation, and thermal cycle reliability.

VISA Focal Plane Developers	VISA Technical Approach
DRS Infrared Technology /	Die-to-die
MCNC	Die-on-wafer;
Rockwell Scientific	Die-to-die;
	Thick (250um silicon)
Raytheon Vision Systems /	Wafer-to-wafer
University of NY at Albany	
Lincoln Laboratory	Wafer-to-wafer;
	Fully depleted SOI

Table 2: VISA focal plane array developers are each pursuing a unique approach to three-dimensional focal plane arrays.

In the approach at DRS / MCNC, the process is compatible with the DRS infrared detector fabrication process, which integrates individual detectors onto six inch silicon read-out wafer. In the VISA process, integrated circuit wafers are mounted to a carrier and thinned at DRS, and the via formation, isolation and metallization processes performed at MCNC. The vias are nominally four micron diameter and formed in silicon die thinned to approximately twenty to twenty-eight microns. Test arrays of 256x256 on thirty micron centers show a 99.92 % operability of the via formation and interconnection process. These test arrays consisted of a thin silicon layer bonded to a conventional read-out integrated circuit.

A major advance in the process was the development of techniques for formation of a uniform array of high aspect ratio (5-7) vias. The development included a conformal insulator deposition for the via sidewalls, and removal of the insulator from the bottom of the via to ensure contact to the read-out circuit metal pad. This process, demonstrated for individual die, will be extended to die mounted on silicon wafers, and processed with infrared material to show the feasibility of producing imaging arrays.

Rockwell Scientific is pursuing a process using thick (250 um) silicon wafers. The thicker wafers ease handling during the processing. The silicon wafers are etched from both sides of the wafer. Vias with a four micron diameter are etched through 100 um silicon on the front side of the wafer. These are aligned with eight micron vias, etched through the other side of the wafer. The wafers are interconnected using indium solder bumps, similar to the process used in producing focal plane arrays. Interconnect operability greater than 93% has been demonstrated on 64 x 64 areas of a 480 x 640 array.

The Lincoln Laboratory is developing a wafer-to-wafer interconnect process using fully depleted silicon on insulator (SOI) wafers. The SOI process provides the potential for focal plane arrays with improved performance, especially in speed / power product. The silicon on insulator process simplifies the through wafer via fabrication, since vias are etched directly through the insulator. The process has demonstrated high density vias with one micrometer diameter. Via interconnect operability of 100 % has been achieved with via chains of 10,000 vias.

A wafer to wafer approach is also being pursued by Raytheon and the State University of New York at Albany. The approach is unique in that a carrier wafer is used to facilitate handling, but a buried oxide layer provides an etch stop for removal of the carrier wafer. The vias are etched through the active layer. Vias with a four micrometer diameter are

etched though a wafer of thickness 10 - 20 um. An operability of greater than 98 % has been achieved on a 256 x 256 array with 30 um pixels.

These approaches to VISA process development fulfill a broad range of requirements for both rapid prototyping of unique focal plane arrays, and ultimately integrated circuit production for imaging arrays. The major consideration in this early phase of the development is high operability of the vias and interconnects. Consideration is also being given to the impact of VISA technology on FPA performance, compatibility with production processes, and further extensions and transition of the technology.

6. TECHNOLOGY DEMONSTRATIONS / APPLICATIONS

The demonstrations planned to show the benefits of the VISA technology in system applications are shown in Table 3. VISA benefits a wide range of sensor types, and the examples shown in Table 3 are only a small sample. But these demonstrations show the impact in several, diverse areas. The focal plane demonstrations are scheduled for completion by December 2005.

VISA Technology Demonstration	Characteristic
High Dynamic Range	18 – 20 bits at 1 Khz
Laser Jam and High Intensity Source	Imaging thru high intensity without saturation
Large Storage Capacity	Increase operating temp of 3-5um array by 100 C
High Resolution 3-D Ladar	1 inch range resolution 30 um pixels
Army Two-Color Mid LWIR FPAs	X5 – X10 LWIR sensitivity

Table 3: VISA technology demonstrations will show the advantages of the increased processing area at the detector. Further development of the VISA architecture will significantly extend the capability to more advanced focal plane processing functions.

A significant feature of the demonstrations will be the high dynamic range enabled by digitization at the pixel. The goal of an eighteen to twenty (18 – 20) bit dynamic range at a conversion rate of 1 KHz adds capability for target acquisition in high background. One of the VISA demonstrations will show that targets are visible in the presence of high intensity sources ten times (X10) the background level.

Other demonstrations will take advantage of the high storage capacity of the VISA technology, and show an increase in operating temperature for 3-5um detectors and the increased sensitivity possible with long wavelength detector utilizing full frame integration.

7. SUMMARY

The VISA technology addresses a major barrier in imaging sensor technology, the limited capability of the read-out circuit. Currently, the detector pitch defines the available signal processing area, and provides a physical limit to the design of the low noise amplifier and detector interface circuit. The VISA technology eliminates this barrier, extending the area under the detector into the third dimension.

Several approaches are being pursued, each with technology demonstration goals, and objectives for establishment of a new technology base with long term impact for sensor development. The initial demonstrations have established feasibility of the via / interconnect technology and the circuit designs for high dynamic range. The focal plane development in progress shows that three dimensional read-out circuits are practical additions to the current technology, and provide significant performance advantages.

These demonstrations are the beginning of the VISA technology. There are substantial gains to be realized in extension of the technology to a greater number of layers, higher density vias and larger arrays. The technology lends itself to focal plane designs for next generation image sensors, such as multi- and hyper-spectral imaging; room temperature infrared system-on-chip, and pixel-to-pixel registered multi-band imaging.

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