

ULSI Technology

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Mechanical control budget for processing and positioning large-diameter wafers
 Temperature uniformity and reproducibility budget within each wafer and from run to run
 Atmospheric budget for controlling gases used in the equipment
 Time control budget
 Absolute, repeatable temperature measurements on wafers

4.2.1 Thermal Budget

Dopants are introduced into Si by processes involving ion implantation, gaseous sources, solid sources, or crystal growth. Each method creates n- or p-type conductivity layers with a desired spatial distribution depending on the application. The desired time-at-temperature (thermal budget) to produce pn junctions at the desired depth from the Si surface for p-channel metal-oxide-silicon (MOS) transistor sources and drains is shown in Fig. 6. Assuming a gaseous dopant source is used that gives a boron (B) surface concentration of 1×10^{20} atoms/cm³, then the thermal budget as a function of temperature can be determined. In Fig. 6, the requirements for four MOS technologies specified by the minimum patterned feature sizes (2, 1, 0.5, and 0.25 μm) are plotted.¹⁵ Thus, for each generation of technology the time allowed at each temperature to form a junction at the necessary depth can be determined from the calculated lines. For example, for 0.25- μm devices, the time allowed to form the required 700 Å deep source-drain junction at 1000°C is only 24 seconds! This compares to junction-formation times of over 1000 sec at 1000°C for 2- μm technology.

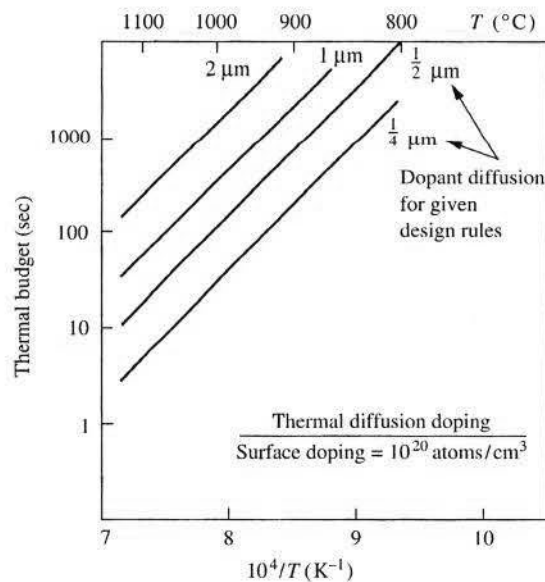


FIGURE 6

Available time-at-temperature (thermal budget) to produce scaled p⁺n junction depths for four MOS technologies. Thermal diffusion sources are assumed with a fixed surface concentration of 1×10^{20} atoms/cm³. (After Fair, Ref. 15. © 1990 IEEE)

This example shows us that the thermal budget requirements for MOS technology are driving a change in the type of furnaces needed to form pn junctions by diffusion. The natural question is, Why not keep the conventional batch furnaces and reduce the temperature to get more thermal budget time? If this were done for the last example, we could operate at 800°C and have 1000 seconds of processing time available. Although this certainly is feasible, gaseous source diffusion is generally not used, because it is difficult to get rid of the source after the junctions are formed. Traditional diffusion sources form doped glasses in the open windows that are defined in SiO₂. These glasses etch marginally faster than SiO₂, making them difficult to remove without losing the definition of the window itself. In addition, doping control is difficult with gaseous sources. The preferred process for introducing dopants into Si is ion implantation, since it is controllable and there is no residual source material to remove. However, implanting high-energy ions into a Si substrate produces extensive damage to the crystal through collisions between the incoming ions and the lattice atoms.¹⁶ Once the temperature of the implanted wafer is raised sufficiently, the implant damage begins to anneal or change form, producing large quantities of point defects, i.e., Si vacancies and Si self-interstitial atoms. If the implant dose exceeds approximately 2×10^{14} ions/cm², more stable, extended defects may form, such as dislocation lines and loops. As we will see, an 800°C anneal is not sufficient to remove these extended forms of damage, which may cause incomplete dopant activation or leaky junctions. Thus, the appropriate annealing temperatures for ion-implanted junctions are above 900°C, which constrains the thermal budgets for shallow junctions for ULSI devices to tens of seconds.

Perhaps the most significant factor associated with the use of ion implantation in junction formation for ULSI is the production of large quantities of point defects during the damage anneal. The basic process of thermal diffusion of dopants requires the presence of such point defects, usually found in the Si crystal at equilibrium concentrations. However, damage annealing can produce point defects in concentrations that may reach many orders of magnitude above equilibrium levels at the annealing temperature. As a result, dopant diffusion can be significantly enhanced during ion-implantation damage annealing when excess point defects are present.¹⁷

The time required to remove the simplest forms of damage produced by ion implantation (point defect clusters) is measured in seconds at temperatures above 1000°C. This time is considered insignificant for older MOS technologies with deep source/drain junctions that require considerable diffusion times. However, this is not the case for ULSI technologies, where junctions must be established in seconds. As a result, thermal budgets can be dominated by the effects of implantation damage annealing. The thermal budgets for ion-implanted p⁺ junctions for the same four generations of MOS technologies previously discussed in Fig. 6 are now shown in Fig. 7. Implants consisted of 6- to 10-keV BF₂ ions to form B-doped layers in Si with surface concentrations of 1×10^{20} atoms/cm³.⁵ The thermal-budget curves were calculated using the PREDICT simulator,¹⁸ which contains models for damage effects on diffusion. For 0.25-μm technology, only 2.5 seconds are available for a diffusion temperature of 1000°C, which is a factor of 10 less than the thermal budget for a comparable gaseous-source process in Fig. 6. And, as we have seen, reducing the diffusion temperature to buy more process time is a limited option. It is usually

CAPITLY

CHAPTER 8

Metallization

R. Liu

8.1 INTRODUCTION

Metallization is the process that connects individual devices together by means of microscopic wires to form circuits. These wires are necessary for a circuit to function, but they introduce parasitic resistance and capacitance, which degrade the performance of devices. Often these wires carry electrical currents in the milliamperere range, resulting in very high current density (10^5 A/cm^2) that threatens to break the submicron-size interconnects. Thus, as devices scale down with ever-improved output, the loss within the metal interconnects dissipates a greater portion of the improved performance. Therefore, the essence of metallization practice is to minimize the undesirable effects.

In this chapter metallization issues and techniques will be discussed. The introductory section discusses the major issues. Sections 8.2, 8.3, and 8.4 examine the key metallization processes. Section 8.5 concentrates on the two key techniques for multilevel metallization—interlayer dielectric and global planarization. Section 8.6 covers some aspects of metallization reliability not included in Chapter 12, and Section 8.7 presents a summary and discusses the future materials and processing needs.

8.1.1 Parasitics in Device Performance

The switching speed of a MOSFET is determined by how fast the gate capacitor, plus all the parasitic capacitors, can be charged. Since $Q = CV$ and $i = dQ/dt = C(dV/dt)$, the rate of charging is dominated by (1) the transconductance, which determines the current output of the MOSFET, and (2) the total capacitance. To improve switching speed one has to reduce the total capacitance and maximize the transconductance of the MOSFET.

10.6.3 α -Particle Protection

Soft errors in memory circuits caused by α -particles emanating from packaging materials were first reported⁵¹ in 1978; there have been many papers on the subject since then. The α -particles are emitted by the decay of uranium and thorium atoms contained as impurities in the packaging materials. Decreasing device design rules make circuits sensitive to this problem. Packaging materials, particularly molding compounds, have been pushed below the level of 0.001 to 0.01 α -particle/cm²-h. Because α -particles have low penetrating power in solids, low- α materials, typically polyimides, have been used as α -absorbing coatings on silicon chips.^{52, 53}

Although great progress has been made by reducing α -particle emission in current packaging materials, error correction is still required to control soft errors caused by α -particles.

10.7

OTHER ULSI PACKAGES

Sections 10.1 through 10.6 discuss standard assembly and package fabrication technologies, and they examine some design features that are mainly on standard single-chip packages. Other packages and their assembly techniques are described in this section.

10.7.1 Tape Carrier Package

Tape carrier package (TCP) is a generic term for packages in which a tape-automated bonding (TAB) technique is used for the pads-on-chip interconnects. The TAB technique, which started in gang-bonding, was originally used to improve the productivity of interconnects. TAB uses finely patterned thin metal, usually Cu foil plated with Au or Sn, in place of wires and connects the metal tips metallurgically to corresponding bumps (plated Au) formed on the Al pads on the chip. TAB has become a choice in finer-pitch interconnects for high-I/O ULSI devices because it enables finer pitch and longer span bondings than those achievable by wire bonding. TCPs are usually plastic-based.

Tape carrier

Figure 31⁵⁴ illustrates typical tape carriers used in TCP fabrication. The one-layer tape carrier is a thin Cu foil. It is cost effective but not preferred today; electrical testing of the packaged chip is difficult since all the Cu leads are mechanically connected as one body.

Two-layer tape that has a Cu layer, typically 25 μ m thick, on a polyimide base tape, typically 75 μ m thick, is manufactured in two ways—either Cu plating on the polyimide or polyimide casting on the Cu foil. A window in which to place the chip is formed, and along with other necessary holes, by etching away the polyimide tape, and the Cu layer is patterned into the designated shape by plating or etching

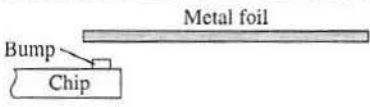
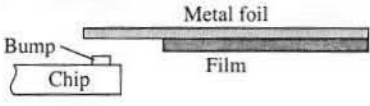
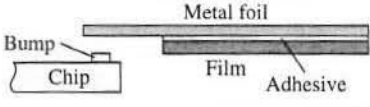
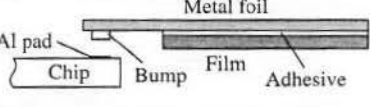
Type	Structure
One-layer	 Metal foil Bump Chip
Two-layer	 Metal foil Film Bump Chip
Three-layer	 Metal foil Film Adhesive Bump Chip
Bumped tape	 Metal foil Film Adhesive Bump Al pad Chip

FIGURE 31

Cross section of typical tape carriers used in TCP fabrication. (After Clain, Ref. 54.)

operations. Three-layer tape is similar to two-layer tape but has an additional adhesive layer between the Cu and the base plastic layers, enabling a choice of base plastics, such as glass-epoxy, BT resin, polyester, and the most prevailing polyimide resin.

Two-layer and three-layer tapes, particularly those with (0.5 μm -thick plating) Cu foils that are chemically Sn-plated are widely used in ULSI packaging. Bumped tape, which has Au bumps on the Cu foil innerlead tips, is also accepted to some extent, since it does not require wafer-bumping operations. Figure 32⁵⁵ illustrates the transfer-bumping operation used as a typical bumped-tape manufacturing method. Au bumps are formed by first performing plating operations on a substrate (typically glass-based). The bumps are then transferred to the aligned tips of the Cu foil (Sn-plated) through a bonding operation to formulate Au-Sn eutectic alloys. Bumped tape eliminates bumped chip availability problems.

Tape-automated bonding

Tape-automated bonding (also called innerlead bonding) is divided into two methods: bonding to the bumps-on-chip using one- to three-layer tapes, and bonding to Al pads-on-chip using a bumped tape. The former method is more popular in the industry today, therefore only this method is detailed here. In this method, bumps (25- μm -thick Au) are formed on the Al pads-on-chip and are attached to Sn-plated or Au-plated Cu foil tips.

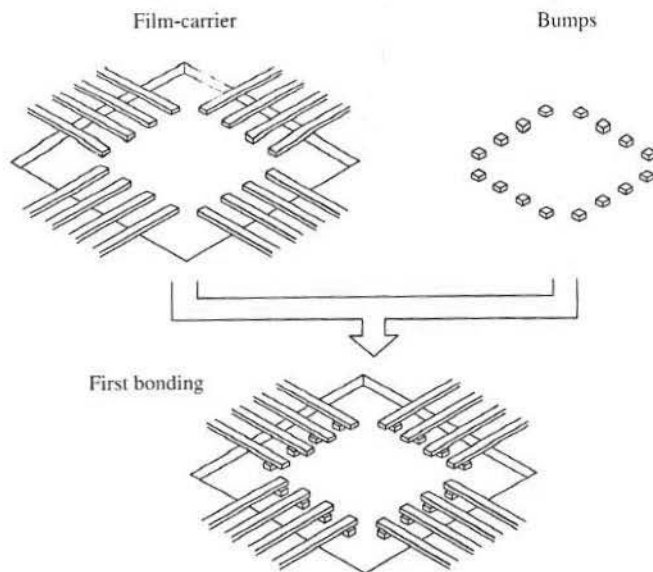


FIGURE 32
Illustration of the transfer-bumping operation. (After Hatada,
Ref. 55.)

Figure 33⁵⁶ illustrates an example of the Au-bump-formation process that is performed at the wafer stage. First, a wafer covered with passivation glass except for the bond-pad areas is full-face sputtered by a combination of barrier metals such as Cr/Cu/Au, Ti/Ni/Au, or TiW/Au. Next, photolithography, in which 25- to 30- μm -thick photoresist materials are used, forms open windows at the bond pads where 20- to 25- μm -thick Au electroplating is performed, forming the Au bumps. Photoresist removal operations, and the following barrier-metal-etching operations, in which the formed Au bumps serve as masks to protect the barrier metals beneath the bumps, complete the bump formation.

Tape-automated bonding is usually a gang operation that connects all the bumps and corresponding foil tips at one time. Typical process conditions are thermocompression using heated (approximately 500°C) flat tools made of diamond and applying loads (approximately 10 kg/mm²) for periods of time that range from 1 to 2 seconds. Figure 34 shows an example of a bonded chip at 110- μm pad spacing. Improved TAB techniques have been successful in reducing the spacing to less than 100 μm .

Tape-carrier package

Varieties of TCPs are used in industry today for ULSI devices. The package fabrication is usually done by plastic technologies—glob-top coating, or transfer molding that encapsulates the bonded chip with plastic resin materials. Figure 35 shows an example of a package in which the packaged chip can be electrically tested

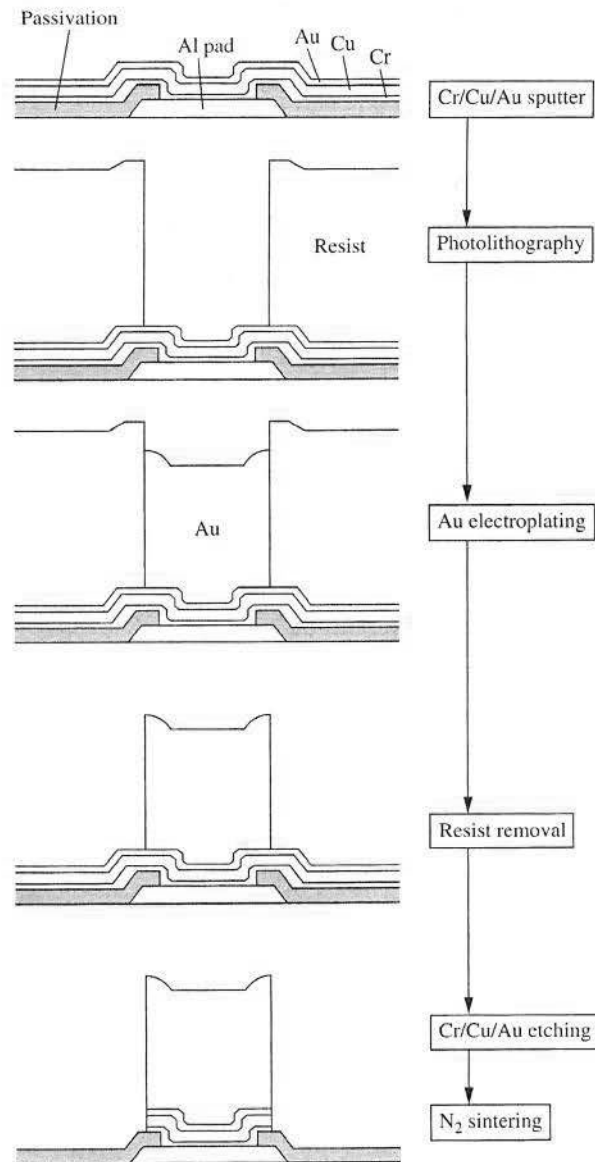


FIGURE 33
Example of the Au-bump-formation process that is done at the wafer stage. (After Kohara, Ref. 56.)

(including burn-in operations) using the larger test pads placed on the base polyimide tape that forms the opposite end of the bonded innerleads.⁵⁷ Posttesting and presoldering to the next-level packaging operation are the external lead-trim and form operations through which the package is formed into its final outer shape.

TCP has the potential to become a major choice in higher-I/O ULSI packaging since it enables one of the finest-pitch interconnects to be made. Obstacles to be

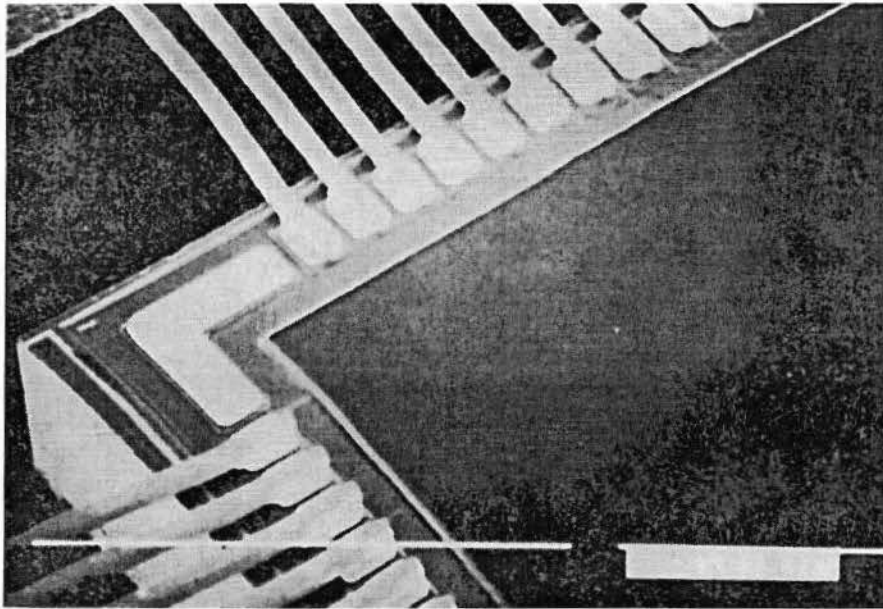
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10.7.2

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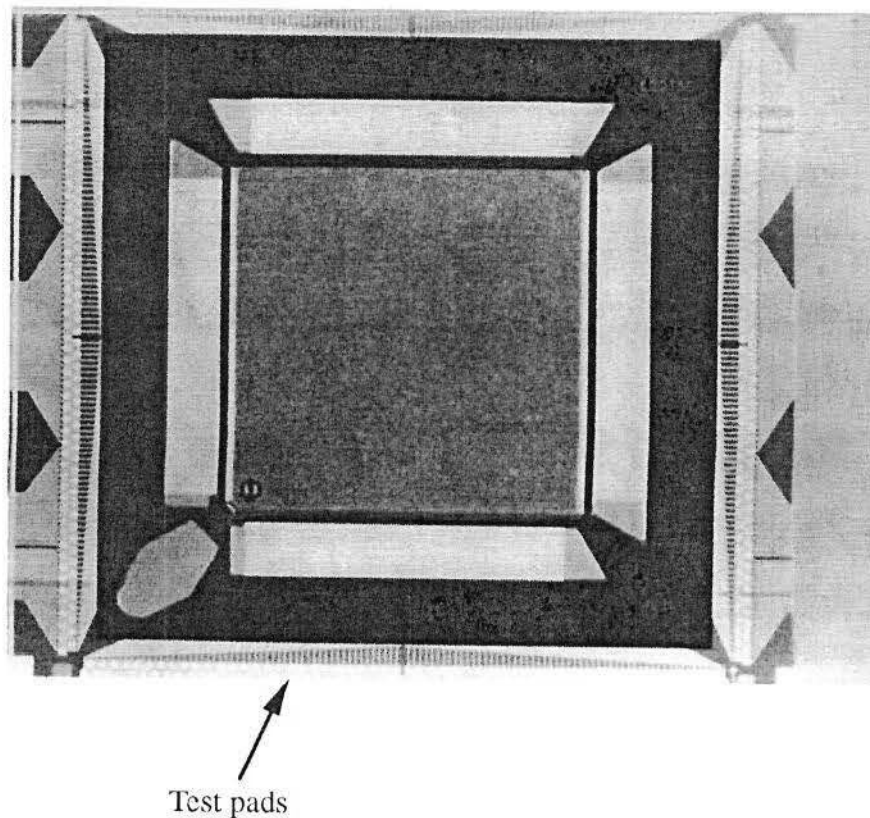
Scanning electron microscope photograph of an innerlead-bonded chip with 110- μm pad spacing. (Courtesy of Mitsubishi Electric Corp.)

surmounted are the relatively higher cost, the modest infrastructures involving test fixtures, and the next-level packaging technologies.

10.7.2 Flip-Chip Package

Flip-chip technologies fabricate bumps (typically Pb/Sn solders) on Al pads-on-chip and interconnect the bumps directly to the package media, which are usually ceramic- or plastic-based.

As Fig. 36⁵⁸ illustrates, in flip-chip technologies, the chip is face-down bonded to a package medium through the shortest path. These technologies can be applied not only to single-chip packaging, but also to higher or integrated levels of packaging in which the package media are larger and more sophisticated substrates that accommodate several chips to form larger functional units. Consequently, encapsulating flip-chip packages involves many variables, such as transfer molding, glob-top coating, and lid sealing, depending on the packaging level. Figure 36 shows a cross section in which the chip is attached to a ceramic substrate, yielding 528 pin interconnects. The flip-chip technique, using an area array, has the advantages of achieving the highest density of interconnection to the device and a very-low-inductance interconnection to the package. However, pretestability, postbonding visual inspection, and TCE matching to avoid solder bump fatigue are still challenges.

**FIGURE 35**

Example of a plastic TCP, in which the packaged chip can be electrically tested using the larger test pads placed on the base polyimide tape. (Courtesy of Mitsubishi Electric Corp.)

The solid, curved line in Fig. 37⁵⁹ shows that the original solder bump area is usually larger than that of barrier metals placed beneath. This area becomes closer in size to that of the barrier metals during the reflow-soldering operations. Thus, proper combinations of bump area, bump thickness, and barrier metal area must be selected to guarantee the interconnect integrities.

10.7.3 Ball-Grid Array Package

The recently developed ball-grid array (BGA) package is of interest in ULSI packaging. The BGA package is ceramic- or plastic-based and involves a variety of internal package structures. This package is now being assessed, standardized, and registered. This type of package features area-array external electrodes, usually Pb/Sn-

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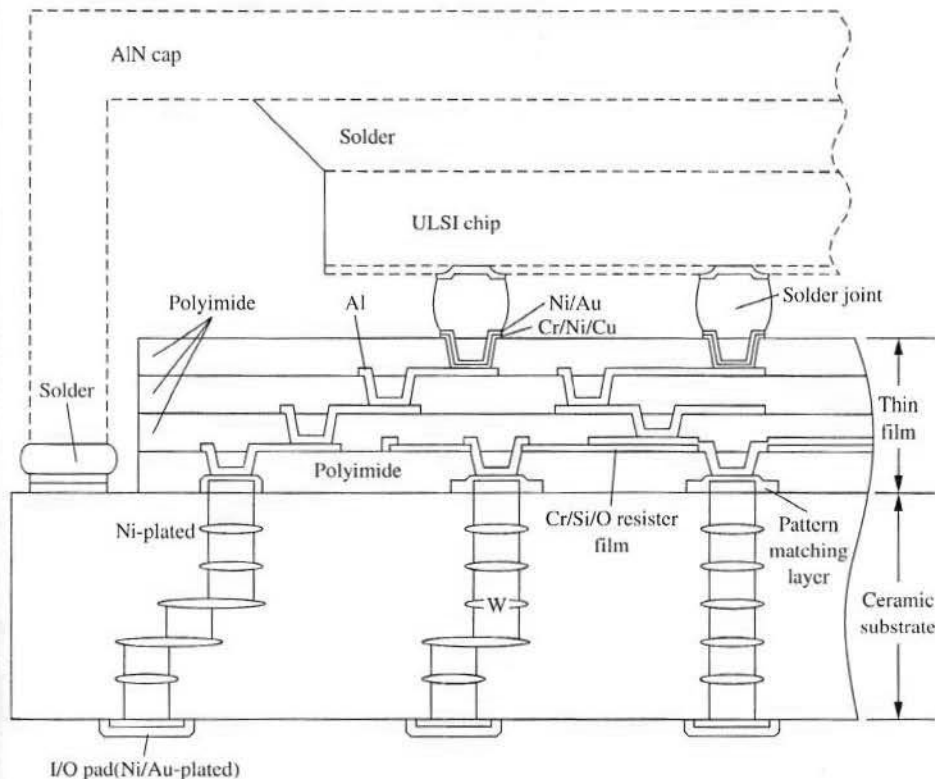
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FIGURE 36
Cross section of a solder bump

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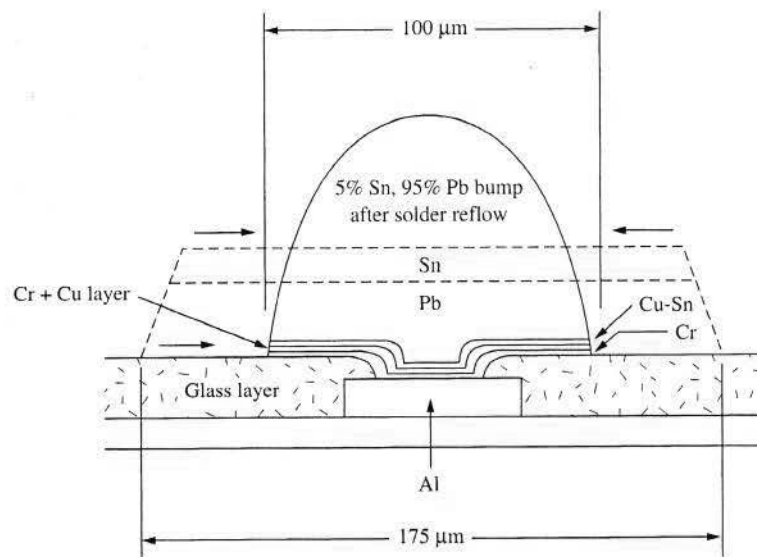
**FIGURE 36**

Cross section of a flip-chip package in which the chip is attached to a ceramic substrate and hermetically sealed. (After Inoue, Ref. 58.)

based bumps, placed on the package back surface at spaces ranging from 1 to 2 mm. The potential advantages are better external pin-count density, easier soldering to the PWB, lower inductance to the PWB, larger thermal paths to the package surroundings, and improved pretestability.

Figure 38⁶⁰ illustrates a simple BGA construction. An interconnected chip on a plastic resin substrate (typically BT resin) is transfer-molded, and solder balls are attached to the package back in post-molding operations. The figure shows thermal via holes placed in the substrate that provide shorter and significantly larger thermal paths from the chip to the mother PWB through the holes and the solder balls. More sophisticated BGA package structures have been proposed; these would contain multilayer substrates that have broader power planes, broader ground planes, or both for low-inductance and larger thermal-path connections.

Two popular choices for solder-bump formation are solder-ball attachment and solder-paste screen printing. Both methods would be followed by reflow operations to complete the metallurgical connections.

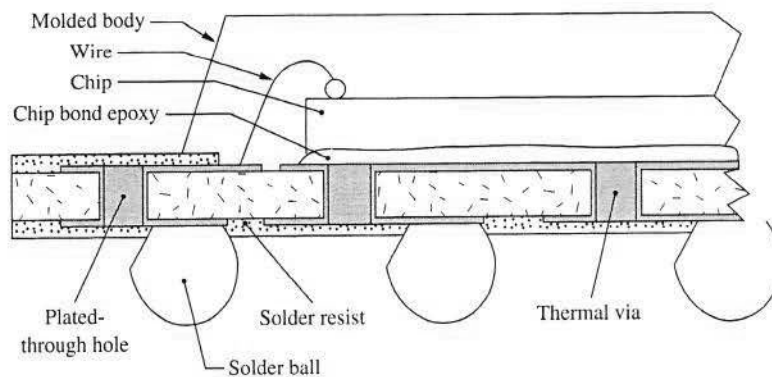
**FIGURE 37**

Cross section of a solder bump used in flip-chip technologies and the deformation caused by reflow-soldering operations. (After Totta and Sopher, Ref. 59.)

10.8

SUMMARY AND FUTURE TRENDS

Package pin count will undoubtedly continue to increase with increasing IC complexity. Alumina ceramic packages will continue to dominate a significant portion of the high-performance ULSI packaging technology until factors such as their high

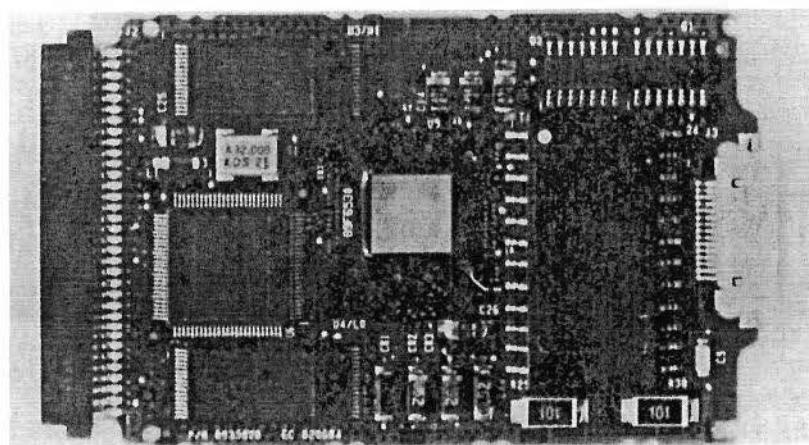
**FIGURE 38**

Cross section of a simple BGA package. The package is plastic-based and features area-array solder balls. (After Sloan, Ref. 60.)

dielectric constant, modest thermal conductivity, or cost force a change to other contending materials. Plastic packages, especially posttransfer-mold plastic packages, will dominate most of the ULSI packaging technology. Higher packaging density on the PWB level will continue to drive package design gradually but steadily toward smaller lead pitches, to approximately 0.3-mm spacings.

If chip integration keeps pace with decreasing feature size, today's interconnection technologies, especially wire bonding, will be challenged.^{61, 62} So far, wire bonding has successfully maintained the relative proportions of chip size and interconnection area generally up to an I/O of approximately 300 and often up to an I/O of approximately 500 interconnects on a chip with the penalties of cost, yield, or some chip design restrictions. TAB and flip-chip techniques will be the candidates to replace wire bonding. However, it probably will be some time before appropriate infrastructures are available to replace wire bonding technologies. Interconnections of high I/O (> 500 per chip) will have to be the choice among the three techniques.

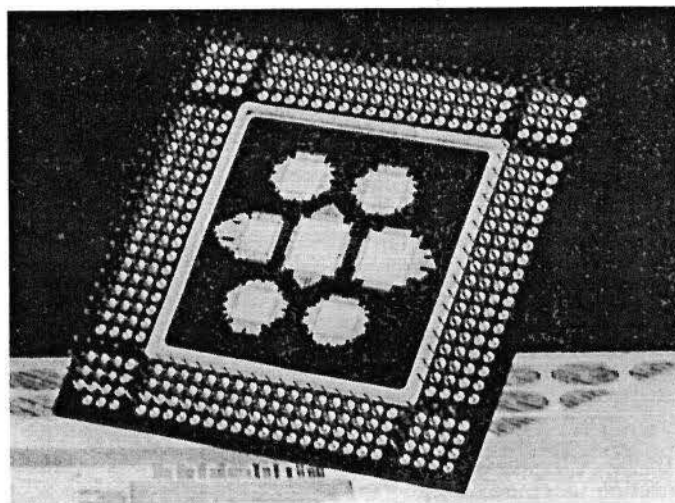
System design will increasingly depend on systematically optimizing the entire interconnection scheme to achieve the potential benefits of improved silicon capability. This optimization may lead to completely new requirements for assembly and packaging, but more than likely it will lead to sorting out the various existing assembly technologies and discovering the combinations that lend themselves to packaging-level integrations. The approach for various kinds of multichip modules (MCMs), shown in Fig. 39, verifies this trend.⁶³



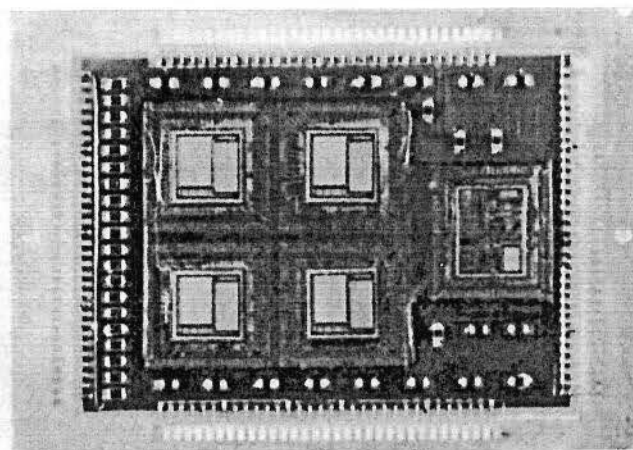
(a)

FIGURE 39

Three kinds of multichip modules. (a) MCM-Laminate (L) is PCB-based. Single-chip-packaged ULSI devices and other components, such as capacitors and resistors, are soldered onto the module. Sometimes bare chips can be used in lieu of packaged chips. Although the PWB is usually finely patterned, established surface-mount technology favors MCM-L growth. (Courtesy of IBM Japan, LTD.) (continued)



(b)



(c)

FIGURE 39 (continued)

(b) MCM-Ceramic (C) is co-fired ceramic-based. Although packaged devices can be placed on the substrate, MCM-C is more likely to have bare chips, since the ceramic provides excellent TCE matching and thermal conductivity. (Courtesy of Kyocera Corp.)

(c) MCM-Deposition (D) is usually ceramic- or silicon-based. Wiring patterns of the substrate are formed by deposition and achieve finer-features than MCM-L or MCM-C. Today, the use of this technology is limited, since the manufacturing cost is still high. (Courtesy of Mitsubishi Electric Corp.)

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