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1-Aug-1998	10 - 16 mu broad-band Quantum Well Infrared Photodetector	Bandara, S. V.; Gunapala, S. D.; Liu, J. K.; Luong, E. M.; Mumolo, J. M.; Hong, W.; Sengupta, D. K.; McKelvey, M. J.
13-Sep-1999	10 Gbps Shuttle-to-Ground Adjunct Communication Link Capability Experiment	Ceniceros, J.; Sandusky, J.; Hemmati, H.
18-Oct-1993	A ~10 km Resolution Image of Loki at 3.8 um	Goguen, J.; Veeder, G.; Matson, D.; Johnson, T.; Toomey, D.
Apr-2004	10 micron imaging of Seyfert galaxies from the 12 micron samples	Gorjian, V.; Werner, M. W.; Jarrett, T. H.; Cole, D. M.; Ressler, M. E.
Jun-1998	10 Micron Search for Cool Companions of Nearby Stars	Van Buren, D.; Brundage, M.; Ressler, M.; Terebey, S.
14-Jun-1993	10 <sub>mu</sub>m Spectra of Comets and the Composition of Silicate Grains	Hanner, M.; Lynch, D.; Russell, R.
1-Jul-1996	A 100 Hour Wear Test of the NASA NSTAR Ion Thruster	Polk, J. E.; Patterson, M. J.; Brown, J. R.; Rawlin, V. K.; Sovey, J. S.; Myers, R. M.; Blandino, J. J.; Goodfellow, K. D.; Garner, C. E.
30-May-2000	100 Months of Upper-Ocean Coastal Upwelling Computed from Alongshore Wind-Stress in the Southeast Pacific Ocean	Halpern, D.; Woiceshyn, P.
30-May-2000	100 Months of Upper-Ocean Coastal Upwelling Computed From Alongshore Wind-Stress in the Southeast Pacific Ocean	Halpern, D.; Woiceshyn, P.
19-Apr-2001	10-16 meu broadband 640X512 GaAs/AlGaAs quantum well infrared photodetector (QWIP) focal plane array	Gunapala, S. D.; Bandara, S. V.; Liu, J. K.; Rafol, S. B.; Mumolo, J. M.; Reininger, F. M.; Fastenau, J. M.; Liu, A. K.
26-Sep-2001	10-16 meu broadband 640X512 GaAs/AlGaAs quantum well infrared photodetector (QWIP) focal plane array	Gunapala, S. D.; Bandara, S. V.; Liu, J. K.; Rafol, S. B.; Mumolo, J. M.; Reininger, F. M.; Fastenau, J. M.; Liu, A. K.
May-2005	1024 x 1024 pixel mid-wavelength and long-wavelength infrared QWIP focal plane arrays for imaging applications	Gunapala, S. D.; Bandara, S. V.; Liu, J. K.; Hill, C. J.; Rafol, S. B.; Mumolo, J. M.; Trinh, J. T.; Tidrow, M. Z.; LeVan, P. D.
1995	10-30 micrometer Maps of the Central 5 parsecs of the Galaxy: Heating of the Cavity and Neutral-Gas Disk	Telesco, C.M.; Davidson, J.A.; Werner, M.W.
2001	10-ft. space simulator facility description	Brown, R.; Fisher, T. C.
5-Jun-2001	A 10GHz optoelectronic oscillator with continuous frequency tunability and low phase noise	Huang, S.; Maleki, L.; Le, T.
Aug-1995	The 10-Micron Silicate Feature in Short-Period Comets	Hanner, Martha S.
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7-Feb-2001	A 1.2 THz planar tripler using GaAs membrane based chips	Mehdi, I.
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5-Dec-2000	A 1.2 THz tripler using GaAs membranes	<i>Mehdi, I.</i>
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Jul-2000	Azimuth variation in microwave scatterometer and radiometer data over Antarctica	Long, D.; Drinkwater, M.
21-Mar-1994	Azimuthally-dependent Finite Element Solution to the Cylindrical Resonator	Osegueda, R.; Pierluissi, J.; Gil, L.; Revilla, A.; Villalva, G.; Dick, G.; Wang, D. SantiagoR.
Jan-2004	Bacillus odysseyi sp. nov., a round-spore-forming bacillus isolated from the Mars Odyssey spacecraft	Duc, M. T. La; Satomi, M.; Venkateswaran, K.
1996	Back to Mars	Frewing, Kent
6-Oct-1997	Back to Mars: The Mars Pathfinder Mission	Cook, R. A.; Spear, A. J.
17-Apr-2001	Background and architecture for an autonomous ground station controller	Paal, L.; Golshan, N.; Fisher, F.; James, M.
9-May-2000	Background and Introduction to Mission Data System and Other Software Architectures	Roquette, N.; Dvorak, D.; Rasmussen, B.; Sacks, A.
9-Jun-2005	A back-illuminated megapixel CMOS image sensor	Pain, Bedabrata; Cunningham, Thomas; Nikzad, Shouleh; Hoenk, Michael; Jones, Todd; Wrigley, Chris; Hancock, Bruce
22-Jan-2002	Backpropagation processing of GPS radio occultation data	Ao, C. O.; Hajj, G. A.; Leroy, S. S.; Meehan, T. K.; Juarez, M. de la Torre; Iijima, B. A.; Mannucci, A. J.
22-Jan-2002	Backpropagation processing of GPS radio occultation data	Ao, C.; Hajj, G. A.; Leroy, S.S.; Meehan, T. K.; Juarez, M. de la Torre; Iijima, B. A.; Mannucci, A. J.
1993	Backscatter Characteristics of the Winter Sea Ice Cover in the Beaufort	Kwok, R.; Cunningham, G. F.
1996	Backscatter for Ice Sheet 2 Growth Phase in the Winter 1994 Winter Sea Ice Experiment	Nghiem, S. V.
30-Oct-1996	Backscatter Identification of the Full Frost Flower Coverage Condition	Nghiem, S. V.; Martin, S.; Perovich, D. K.; Kwok, R.; Drucker, R.; Gow, A. J.
26-Sep-1994	Backscatter Model for the Unusual Radar Properties of the Greenland Ice Sheet	Rignot, E.
Jul-2005	Backscattering enhancement for Marshall-Palmer distributed rains for a W-band nadir-pointing radar with a finite beam width	Kobayashi, Satoru; Tanelli, Simone; Im, Eastwood; Oguchi, Tomohiro
8-Nov-2004	Backscattering enhancement with a finite beam width for millimeter - wavelength weather radars	Kobayashia, Satoru; Tanellia, Simone; Iguchib, Toshio; Im, Eastwood
25-Apr-2002	Backside device irradiation for single event upset tests of advanced devices	Swift, G. M.
30-May-1993	A Back-To-Back Barrier-N-N+ (bbBNN) Diode Tripler at 200 GHz	Choudhury, Debabani; Raisanen, Anti V.; Smith, R. Peter; Frerking, Margaret A.
30-Mar-1993	A Back-to-Back Barrier-N-N+(bbBNN) Diode Tripler at 200 GHz	Martin, D.; Choudhury, R. P.; Smith, A. V.; Raisanen, M. A.; Frerking, S.
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13-Jul-1993	A Review of Infrared Readout Electronics for Space Science Sensors	Pain, Bedabrata; Fossum, Eric R.
1996	On-Focal-Plane Successive Approximation A/D/Converters for Digital CMOS Image Sensors	Shou, Zhimin; Pain, Bedabrata; Fossum, Eric R.
1996	CMOS Active Pixel Sensor Star Tracker with Regional Electronic Shutter	Yadid-Pecht, Orly; Pain, Bedabrata; Staller, Craig; Clark, Christopher; Fossum, Eric
31-Jan-1996	Progress in Voltage and Current Mode On-Chip Analog-to-Digital converters for CMOS Image Sensors	Panicacci, Roger; Pain, Bedabrata; Zhou, Zhimin; Nakamura, Junichi; Fossum, Eric R.
31-Jan-1996	Programmable Multiresolution CMOS Active Pixel Sensor	Panicacci, Roger; Kemeny, Sabrina; Matthies, Larry; Pain, Bedabrata; Fossum, Eric R.
9-Apr-1996	Design and Operation of Self-Biased High-Gain Amplifier Arrays for Photon-Counting Sensors	Pain, Bedabrata; Fossum, Eric R.
9-Apr-1996	Recent Progress in On-Focal-Plane ADC	Zhou, Zhimin; Pain, Bedabrata; Panicacci, Roger; Nakamura, Junichi; Fossum, Eric R.
Sep-2003	New process and pixel structure of an SOI-CMOS imager	Zheng, Xinyu; Seshadri, Suresh; Wood, Michael; Wrigley, Chris; Pain, Bedabrata
9-Jun-2005	A back-illuminated megapixel CMOS image sensor	Pain, Bedabrata; Cunningham, Thomas; Nikzad, Shouleh; Hoenk, Michael; Jones, Todd; Wrigley, Chris; Hancock, Bruce

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Title: A back-illuminated megapixel CMOS image sensor

Authors: Pain, Bedabrata
Cunningham, Thomas
Nikzad, Shouleh
Hoenk, Michael
Jones, Todd
Wrigley, Chris
Hancock, Bruce

Keywords: Complementary Metal Oxide Semiconductor imager (CMOS)
back - illumination

Issue Date: 9-Jun-2005

Publisher: Pasadena, CA : Jet Propulsion Laboratory, National Aeronautics and Space Administration, 2005.

Citation: IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, Karuizawa, Japan, June 9-11, 2005.

Abstract: In this paper, we present the test and characterization results for a back-illuminated megapixel CMOS imager. The imager pixel consists of a standard junction photodiode coupled to a three transistor-per-pixel switched source-follower readout [1]. The imager also consists of integrated timing and control and bias generation circuits, and provides analog output. The analog column-scan circuits were implemented in such a way that the imager could be configured to run in off-chip correlated double-sampling (CDS) mode. The imager was originally designed for normal front-illuminated operation, and was fabricated in a commercially available 0.5 μ m triple-metal CMOS-imager compatible process. For backside illumination, the imager was thinned by etching away the substrate was etched away in a post-fabrication processing step.

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A BACK-ILLUMINATED MEGAPIXEL CMOS IMAGE SENSOR

Bedabrata Pain, Thomas Cunningham, Shouleh Nikzad,
Michael Hoenk, Todd Jones, Bruce Hancock, Chris Wrigley
Jet Propulsion Laboratory

California Institute of Technology

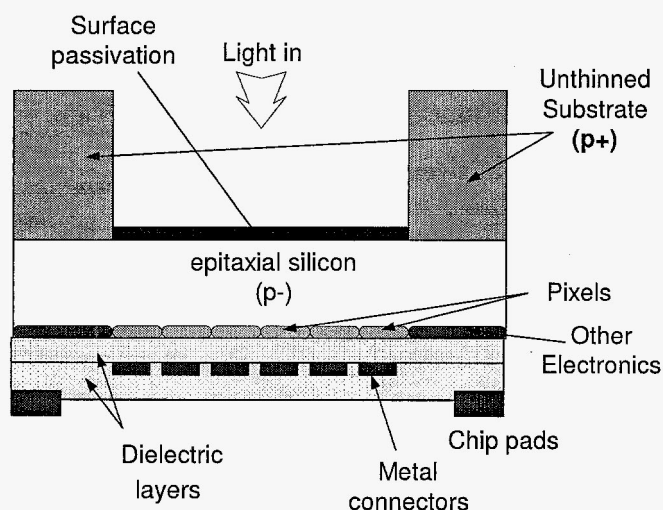
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Imaging with a back-illuminated CMOS imager provides a number of advantages, especially as the pixel size is reduced. These advantages include high (100%) fill-factor and increased quantum efficiency, efficient implementation of antireflection coatings, improved angular response, availability of the traditional "frontside" of the pixel to incorporate in-pixel processing circuits, and increased compatibility with the next generation metals (e.g Cu) and low-k dielectrics.

In this paper, we present the test and characterization results for a back-illuminated megapixel CMOS imager. The imager pixel consists of a standard junction photodiode coupled to a three transistor-per-pixel switched source-follower readout [1]. The imager also consists of integrated timing and control and bias generation circuits, and provides analog output. The analog column-scan circuits were implemented in such a way that the imager could be configured to run in off-chip correlated double-sampling (CDS) mode. The imager was originally designed for normal front-illuminated operation, and was fabricated in a commercially available 0.5 μm triple-metal CMOS-imager compatible process. For backside illumination, the imager was thinned by etching away the substrate was etched away in a post-fabrication processing step.

Figure 1 shows the schematic cross-section of the back-illuminated CMOS APS. The device structure consists of a low-doped ($\sim 3 \times 10^{14}/\text{cm}^3$) epitaxial p-type silicon, with the photo-detecting junction formed by a front-implanted n-well and the p-type epitaxial silicon. Photons enter the detector from the backside, and the resultant photo-electrons are collected in the front-side p-nwell junction.



The imager was thinned at an individual die level using a frame-thinning approach. Only the pixel area was thinned down to $\sim 7\text{-}10\ \mu\text{m}$ thickness (corresponding to epitaxial silicon thickness), leaving a thick peripheral region ($\sim 1\ \text{mm}$ wide). A surface passivation step was then applied to the thinned silicon layer.

The resultant structure provides increased mechanical stability, a significant ease of die handling, and protection against wrinkling of the thinned die. This approach is well-suited for a CMOS imager, since the imager consists not only of the pixels, but the support and signal chain electronics along the periphery of the pixel array.

Figure 1: Schematic cross-section of the back-illuminated imager

Backside thinning was carried out as follows. First, the front-side of the die is attached to a protective wax. Then a protective frame on the backside was created through deposition and patterning of a Si_3N_4 mask. The unmasked p^+ silicon substrate (with doping $\sim 1 \times 10^{19}/\text{cm}^3$) was then etched using hot KOH down to within $\sim 10\ \mu\text{m}$ of the final silicon thickness. The remainder of the etching was carried out in $\text{HF}:\text{HNO}_3:\text{CH}_3\text{COOH}$ solution (HNA etch) [2]. HNA etches silicon through a redox reaction where the silicon oxidation rate is dependent on the doping concentration. Due to its doping concentration dependence, the etch-rate significantly slows down when the silicon substrate is etched, leaving an optically flat thin ($\sim 10\ \mu\text{m}$ thick) epitaxial silicon layer. Following thinning, the front-side wax was removed, and the die was packaged in a standard pin-grid array (PGA) package (with its central portion removed to let light in) using a standard wire-bonding technique.

Passivation of the etched silicon presents a unique challenge. After thinning, the interface trap density at the unterminated silicon surface is unacceptably high, while a naturally formed native oxide (~20 Å thickness) causes the surface to become positively charged. Unwanted band-bending and the presence of dangling bonds result in a loss of QE and abnormally high dark currents, necessitating the use of post-metallization surface-passivation steps. Unfortunately, any post-metallization process step is challenging, since due to the presence of front-side metal with low melting point (~ 400°C), no high temperature step can be used. Thus, boron implantation and high-temperature furnace anneal is ruled out.

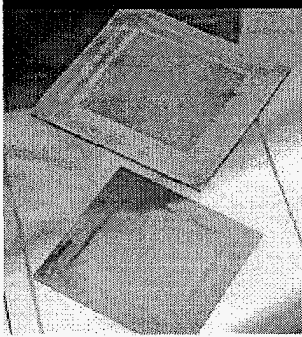


Figure 2: Photograph of the thinned megapixel imager

low-pressure oxide deposition [3,4,5,6].

Self-passivation can be achieved by controlling the HF concentration during the final stages of etching that leaves behind a 30-50 Å oxide. However, the lack of a well-defined end-point of the etching process makes it difficult to carry out reliable self-passivation of the etched silicon surface. To get around this problem, some CCDs have used alternate passivation techniques that include UV-flooding, flash gates (MBE deposited mono-layer of metal), boron-doping followed by high-energy pulsed-laser anneal, and

We have used a delta-doping technique for surface passivation [7]. The technique consists of a low-temperature molecular beam epitaxy (MBE) that places an extremely high density of dopant atoms ($> 10^{14}$ Boron/cm²) within a few atomic layers of the surface with no observable crystal defects and no requirement for post-growth annealing, making it compatible with post-metallization processing. Delta-doping is carried out under ultra-high vacuum conditions (10^{-10} torr) using electron-beam evaporation of elemental silicon and thermal evaporation of elemental boron. The process steps are as follows. A 1 nm-thick p+ silicon layer was grown first, followed by depositing ~30% of a monolayer of boron atoms. 1.5 nm-thick capping layer of epitaxial silicon was then grown. After removal from the MBE system, oxidation of the silicon capping layer protects the buried delta-doped layer. Finally, the resultant optically flat surface allows easy deposition of anti-reflection coating using deposited oxides and plasma-enhanced silicon nitrides.

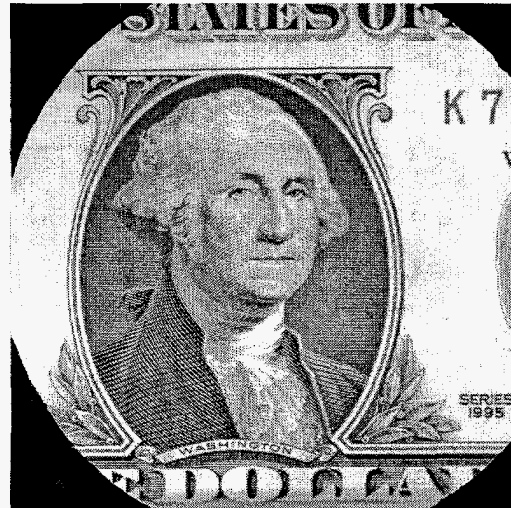


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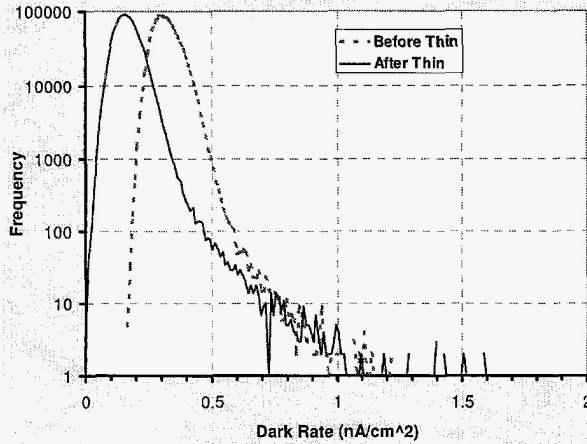


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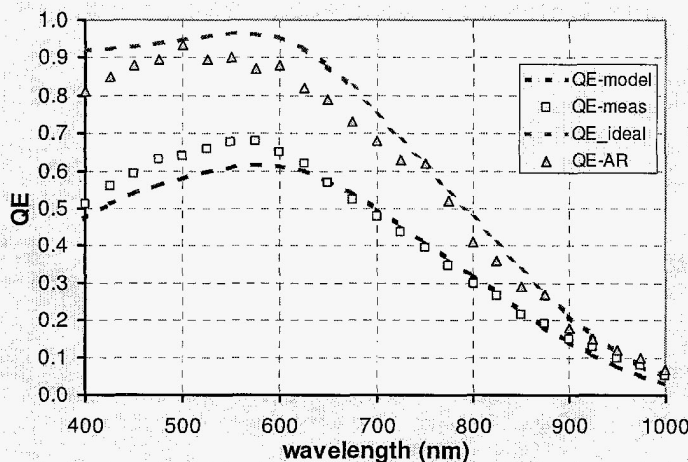


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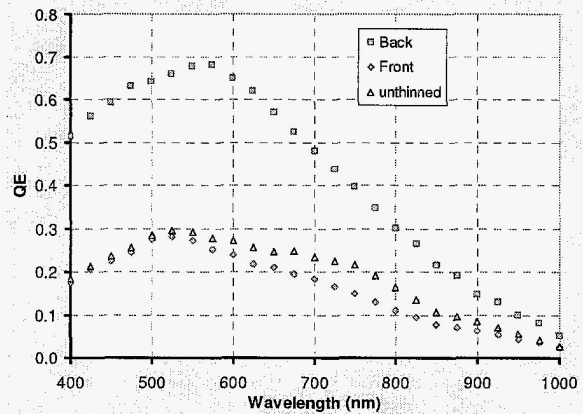


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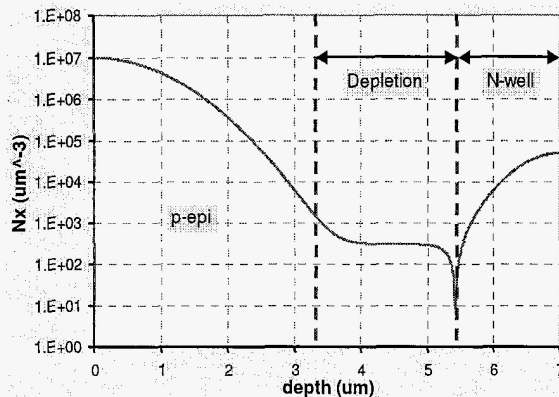


Figure 7: 1-D model of doping concentration variation from the backside surface to the front

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In conclusion, we have demonstrated a back-illuminated CMOS Imager with high QE by using a successful backside thinning and MBE-based surface passivation process. The main disadvantages of the thinning process are the absence of proper etch-stop required for accurate and reliable thinning, and the use of MBE for surface passivation, posing problems for wafer-level thinning and

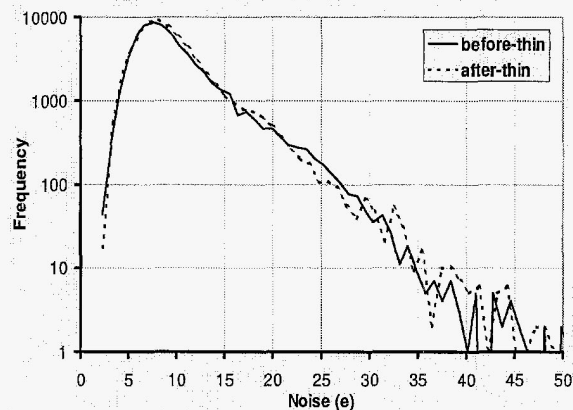


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Characteristics	Front-illum. (no thinning)	Back-illumination
Format	1024x1024	1024x1024
Pixel Pitch	8 μm	8 μm
QE @ 550 nm	25%	80%
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Modal read noise @ 2 MHz	7.6 e ⁻	8.2 e ⁻
PRNU @ 1/3 full-well	< 1%	< 1%
Signal handling capacity	200 ke ⁻	200 ke ⁻

Acknowledgments:

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A BACK-ILLUMINATED MEGAPIXEL CMOS IMAGE SENSOR

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Michael Hoenk, Todd Jones, Bruce Hancock, Chris Wrigley
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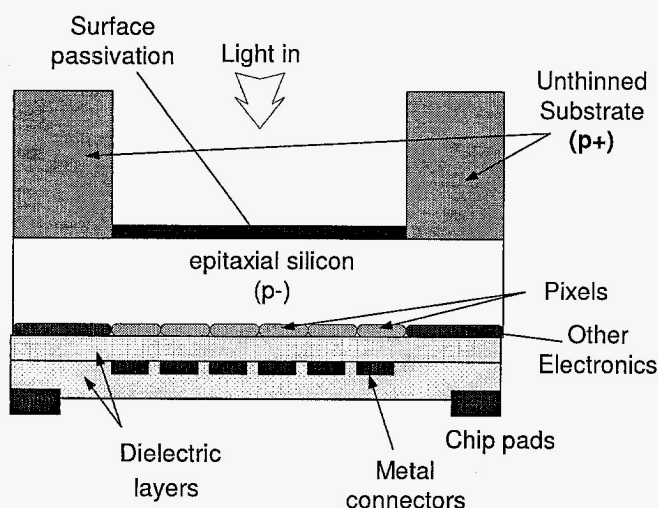
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Imaging with a back-illuminated CMOS imager provides a number of advantages, especially as the pixel size is reduced. These advantages include high (100%) fill-factor and increased quantum efficiency, efficient implementation of antireflection coatings, improved angular response, availability of the traditional "frontside" of the pixel to incorporate in-pixel processing circuits, and increased compatibility with the next generation metals (e.g. Cu) and low-k dielectrics.

In this paper, we present the test and characterization results for a back-illuminated megapixel CMOS imager. The imager pixel consists of a standard junction photodiode coupled to a three transistor-per-pixel switched source-follower readout [1]. The imager also consists of integrated timing and control and bias generation circuits, and provides analog output. The analog column-scan circuits were implemented in such a way that the imager could be configured to run in off-chip correlated double-sampling (CDS) mode. The imager was originally designed for normal front-illuminated operation, and was fabricated in a commercially available 0.5 μm triple-metal CMOS-imager compatible process. For backside illumination, the imager was thinned by etching away the substrate was etched away in a post-fabrication processing step.

Figure 1 shows the schematic cross-section of the back-illuminated CMOS APS. The device structure consists of a low-doped ($\sim 3 \times 10^{14}/\text{cm}^3$) epitaxial p-type silicon, with the photo-detecting junction formed by a front-implanted n-well and the p-type epitaxial silicon. Photons enter the detector from the backside, and the resultant photo-electrons are collected in the front-side p-nwell junction.



The imager was thinned at an individual die level using a frame-thinning approach. Only the pixel area was thinned down to $\sim 7\text{-}10\ \mu\text{m}$ thickness (corresponding to epitaxial silicon thickness), leaving a thick peripheral region ($\sim 1\ \text{mm}$ wide). A surface passivation step was then applied to the thinned silicon layer.

The resultant structure provides increased mechanical stability, a significant ease of die handling, and protection against wrinkling of the thinned die. This approach is well-suited for a CMOS imager, since the imager consists not only of the pixels, but the support and signal chain electronics along the periphery of the pixel array.

Figure 1: Schematic cross-section of the back-illuminated imager

Backside thinning was carried out as follows. First, the front-side of the die is attached to a protective wax. Then a protective frame on the backside was created through deposition and patterning of a Si_3N_4 mask. The unmasked p^+ silicon substrate (with doping $\sim 1 \times 10^{19}/\text{cm}^3$) was then etched using hot KOH down to within $\sim 10\ \mu\text{m}$ of the final silicon thickness. The remainder of the etching was carried out in $\text{HF}:\text{HNO}_3:\text{CH}_3\text{COOH}$ solution (HNA etch) [2]. HNA etches silicon through a redox reaction where the silicon oxidation rate is dependent on the doping concentration. Due to its doping concentration dependence, the etch-rate significantly slows down when the silicon substrate is etched, leaving an optically flat thin ($\sim 10\ \mu\text{m}$ thick) epitaxial silicon layer. Following thinning, the front-side wax was removed, and the die was packaged in a standard pin-grid array (PGA) package (with its central portion removed to let light in) using a standard wire-bonding technique.

Passivation of the etched silicon presents a unique challenge. After thinning, the interface trap density at the unterminated silicon surface is unacceptably high, while a naturally formed native oxide ($\sim 20 \text{ \AA}$ thickness) causes the surface to become positively charged. Unwanted band-bending and the presence of dangling bonds result in a loss of QE and abnormally high dark currents, necessitating the use of post-metallization surface-passivation steps. Unfortunately, any post-metallization process step is challenging, since due to the presence of front-side metal with low melting point ($\sim 400^\circ\text{C}$), no high temperature step can be used. Thus, boron implantation and high-temperature furnace anneal is ruled out.

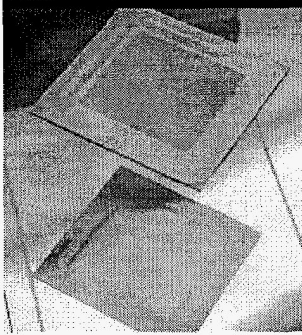


Figure 2: Photograph of the thinned megapixel imager

Self-passivation can be achieved by controlling the HF concentration during the final stages of etching that leaves behind a $30\text{-}50\text{ \AA}$ oxide. However, the lack of a well-defined end-point of the etching process makes it difficult to carry out reliable self-passivation of the etched silicon surface. To get around this problem, some CCDs have used alternate passivation techniques that include UV-flooding, flash gates (MBE deposited mono-layer of metal), boron-doping followed by high-energy pulsed-laser anneal, and low-pressure oxide deposition [3,4,5,6].

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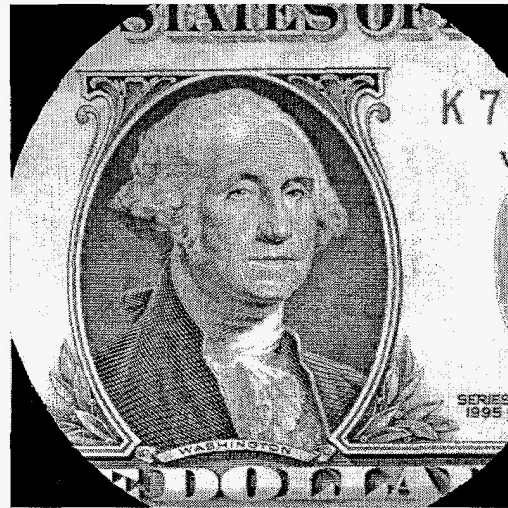


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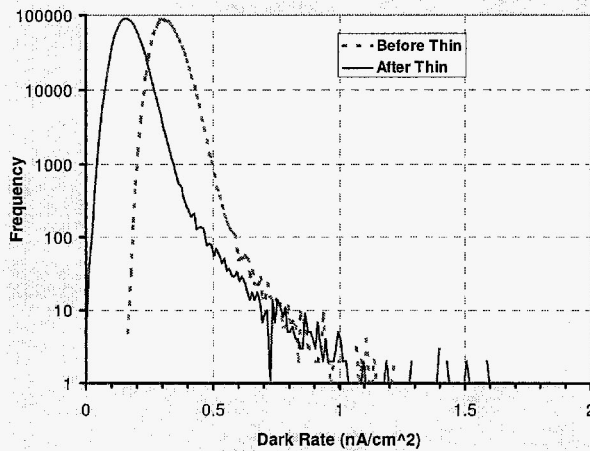


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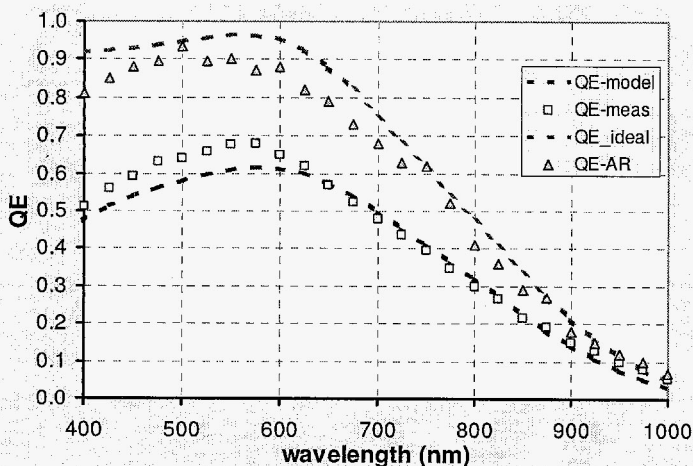


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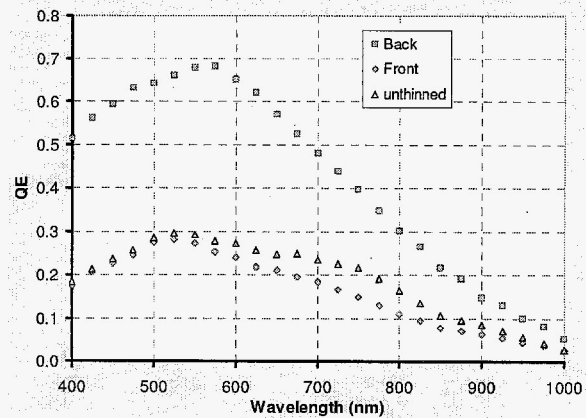


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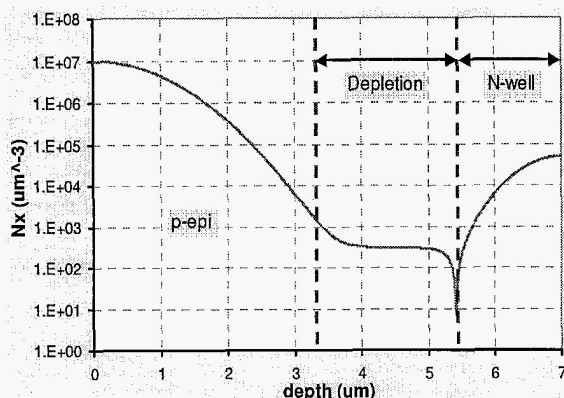


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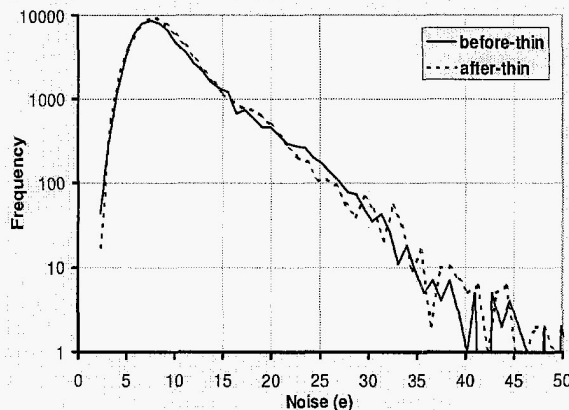


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