

Silicon Photonics

Mike Salib, Corporate Technology Group, Intel Corporation
Ling Liao, Corporate Technology Group, Intel Corporation
Richard Jones, Corporate Technology Group, Intel Corporation
Mike Morse, Corporate Technology Group, Intel Corporation
Ansheng Liu, Corporate Technology Group, Intel Corporation
Dean Samara-Rubio, Corporate Technology Group, Intel Corporation
Drew Alduino, Corporate Technology Group, Intel Corporation
Mario Paniccia, Corporate Technology Group, Intel Corporation

Index words: silicon, photonics, optics, modulator

ABSTRACT

We introduce our approach to opto-electronic integration, silicon photonics, and outline the key functions required for an opto-electronic integration platform: generation, control, and detection of light. Recent research results for silicon-based optical components are discussed including a tunable external cavity laser, a 2.5 GHz optical modulator and a silicon-germanium waveguide-based photodetector. Lastly, optical packaging challenges and potential next-generation designs are presented.

INTRODUCTION

Silicon photonics at Intel can be defined as the utilization of silicon-based materials for the generation (electrical-to-optical conversion), guidance, control, and detection (optical-to-electrical conversion) of light to communicate information over distance. The most advanced extension of this concept is to have a comprehensive set of optical and electronic functions available to the designer as monolithically integrated building blocks upon a single silicon substrate.

Silicon in the Optical Domain

Both the wavelength of light and the transport medium used vary with the application. Our current research is aimed at developing devices and proving functionality in the optical domain for infrared wavelengths common to silica fiber-optic telecommunications systems (1.3 μm to 1.6 μm). Within this range of wavelengths, silicon is nearly transparent and generally does not interact with the light, making it an exceptional medium for guiding optical data streams between active components. With appropriate design, the introduction of additional

materials such as silicon dioxide, standard electronic dopants, and SiGe alloys selectively enhances the electronic-to-optical interactions, allowing for the creation of active devices such as a light intensity modulator and a photodetector. Notwithstanding this flexibility, no practical modification to silicon has yet been conceived which gives efficient generation of light. Thus, the Intel Silicon Photonics platform requires the light source as an external component.

Silicon Electronics in Optical Communications

In the electrical domain, silicon integrated circuits have been widely adopted in all layers of the network, including physical media drivers, media access controls, and for complex network intelligence functions. In principal, monolithic integration of electronics and optics is possible, can reduce unwanted electrical parasitics, and can allow for a reduction in overall size. There are numerous theoretical and practical obstacles to achieving full monolithic opto-electronic integration. We are currently pursuing two parallel approaches to opto-electronic integration in silicon. The first is to achieve a high level of photonic integration with the goal of maximizing the level of optical functionality and optical performance. The second is to look for specific cases where close integration of an optical component and an electronic circuit can improve overall system performance. One such case would be to integrate a SiGe photodetector with a Complementary Metal-Oxide-Semiconductor (CMOS) transimpedance amplifier.

Integration: The Challenge and the Value

An optical transceiver module (sometimes called a transponder) is to be found at the terminations of virtually all optical communications links and the general functionality and architecture of the transceivers in service are similar regardless of performance requirements, communications protocols, and end-user applications. One vision of the future of optical communications links is one in which the drive for lower costs for higher performance (smaller size, lower power, higher data rate, greater transmit distance, expanded functionality, and expanded flexibility) will occur through an increased complexity in the optical domain. Some examples would be multiple wavelengths in one fiber from one ingress point, adaptive or reconfigurable optical components capable of recovering signal integrity under changing external conditions, all-optical packet switching, all-optical signal regeneration, and the use of shared optical media in so-called Passive Optical Networks (PONs) and optical Code Division Multiple Access networks (optical-CDMA). Such increased complexity in the optical domain will require increasingly sophisticated electronic control solutions, and at high data rates, there will be pressure to more closely integrate optical and electronic components. Monolithic integration of a suite of optical and electronic capabilities in one substrate is the natural progression of an integrated photonics vision.

However, in the foreseeable future, the vast majority of improvements at the cost-sensitive (high-volume) applications can be expected almost exclusively in the electronic domain (electronic dispersion compensation, electronic equalization, and electronic means of recovering signal integrity under changing external conditions). Furthermore, the past decade has shown that the simplicity of single-wavelength transceivers with serial On-Off-Key data encoding (OOK) have consistently been chosen over more complex optical solutions (e.g., parallel-optical and CWDM). This does not mean that there are not steady technical improvements in the optical domain, such as recent introductions of long-wavelength Vertical Cavity Surface Emitting Lasers (VCSELs), and deployments of InP Externally Modulated Lasers (EMLs) for mid-performance links. However, these improvements generally are not changing the external architecture of the link for cost-sensitive applications (still single-wavelength, one direction per fiber, etc.).

Thus, it is fair to say that a future with wide-scale deployment of highly integrated photonic and opto-electronic components will be one with a great many changes to the “where and how” light is used to transmit information. The most likely insertion points for integrated photonics will be in places where an extreme

amount of data (aggregate bandwidth) is required in a very small space. Two such applications would be microprocessor data busses (i.e., from microprocessor to memory or between multiple processors in a server) and in the backplane of server racks. Paradoxically, these applications violate a widely held axiom that says that optics is the best choice for long-distance transmission (hundreds of meters to hundreds of kilometers) whereas copper traces and copper cables own the application space for shorter distances. The key assumption that allows us to violate this axiom is that the aggregate bandwidth will be too large for a cost-effective copper-based solution. Present-day estimates indicate that a copper-based point-to-point serial link will become prohibitively expensive above 20 Gbps.

Identifying the potential insertion point for integrated photonics is one thing, but gaining insight into the details of the implementation is quite another matter. The architecture (point-to-point or shared media, encoding scheme, etc.), the transmission medium (polymer waveguide, silica fiber), the integration platform (silicon, GaAs, InP, polymer, silica), and finally the level of integration (monolithic opto-electronic, monolithic photonic integration with separate electronics, or optical platform with hybrid electronic and optical components) are all issues of active investigation in the research community.

Silicon Photonics at Intel

In the first section of this paper we explore Intel’s ongoing research to define one particular technology platform for integrated photonics, namely Silicon Photonics. We introduce the building blocks of the technology and explore the technical advancements and critical challenges to making high-performance components for the integrated platform. The cornerstone technologies being developed at Intel are the tunable External Cavity Laser (ECL), the Silicon Modulator, Silicon-Germanium (SiGe) photodetector, and low-cost interconnection techniques.

A single mode, tunable ECL has been demonstrated by coupling an AR coated III-V semiconductor laser diode to a silicon-based waveguide Bragg grating. The lasing wavelength is selected by the grating and can be tuned by using the thermo-optic effect and simply heating the grating, producing a tuning rate of 12.5 nm/100° C.

Until recently, waveguide-based silicon optical modulators have been limited to relatively moderate speeds, the fastest reported being around 20 MHz. We have made a breakthrough by moving away from the conventional current injection-based devices to a novel MOS capacitor-based architecture. This has allowed us to achieve a 2.5 GHz phase modulation with modeling

predicting bandwidth scaling to beyond 10 GHz. This means that silicon could quickly become a viable alternative to the more conventional III-V or LiNbO_3 modulators currently used for optical communications.

Detection of light for wavelengths typically used for optical communications (1.310-1.550 μm) is not possible in silicon, which is naturally transparent in this region. We are therefore developing photodetectors based on SiGe alloys in order to push the responsivity out to longer wavelengths to achieve efficient operation.

Interconnecting the Silicon Photonic platform, such as to the transmission medium (e.g., silica fiber), is not trivial. To address high-volume applications it is imperative to have simple and low-cost coupling and packaging procedures.

In this next section we highlight waveguide tapering, passive fiber alignment, and passive hybrid alignment techniques.

SILICON LIGHT SOURCE

In this section the use of silicon photonics applied to the light source is discussed. While a silicon laser is still out of reach, work is being done worldwide on silicon light emitters that emit both visible and infrared radiation. A silicon emitter is the missing piece for monolithic integration as it would enable all optical elements and drive electronics to be fabricated on a common substrate. Because we are using silicon waveguides to guide light, the emitter must be in the infrared region of the wavelength spectrum ($> 1.1 \mu\text{m}$) where optical absorption loss is low.

We first summarize the different paths researchers are investigating to achieve electrically pumped light emission, known as Electro Luminescence (EL), from silicon. Until a reliable and efficient silicon emitter can be produced, hybrid integration must be considered (i.e., using a non-silicon-based light source coupled to silicon waveguides). In such a hybrid integrated approach, we show how a simple gain element (III-V gain chip) coupled to a silicon-based Bragg filter can be used to form an ECL. Proof of principal of this tunable, single-mode laser is discussed.

The difficulty in making a silicon light emitter arises from silicon's indirect band-gap. This indirect bandgap results in radiative (light emitting) decay being less likely compared to other non-radiative (e.g., Auger recombination) routes, and thus in a less-efficient corresponding light emission. Forming a laser or even a light emitter from silicon is therefore difficult, although not impossible, and research worldwide has shown light emission from silicon and silicon-based materials by a wide variety of different methods; see, for example, the

summary in [i]. These range from photo-luminescence in textured bulk silicon [ii], to fabrication of nano-scale [iii] or porous silicon [iv] to doping with exotic ions [vii], to Raman emission [v].

To achieve infrared light emission from silicon, the silicon must be doped with a suitable material, such as $\beta\text{-FeSi}_2$ [vi], or Erbium [vii]. Erbium-doped silicon waveguides have shown infrared light emission when the silicon is co-doped with oxygen to produce optically active ions in the lattice [vii]. A PN junction can be formed and the erbium ions pumped electrically to form EL. These kind of doped bulk silicon devices suffer from a major problem: although emission can be relatively strong below 100 K, the emission intensity falls rapidly when the device is heated to room temperature [viii]. This greatly limits the application of these devices.

A different approach to enhance the efficiency of light emission in silicon is to reduce the other non-radiative mechanisms for electron hole recombination. This can be done by restricting carrier diffusion to the non-radiative recombination centers in the lattice. This increases the probability for radiative transitions and hence increases light emission efficiency. A Very Large Scale Integration (VLSI) compatible means to achieve this carrier confinement is to use nano-crystals. Silicon nano-crystals suspended in silicon-rich oxide restrict carrier movement while still allowing electrical pumping [ix]. Pavesi has shown optical gain in these structures [iii] and Franzo et al. have doped silicon nano-crystals with erbium to achieve EL in the infrared region of the spectrum [x]. Other means to obtain carrier confinement and efficient emission of infrared wavelengths include using Ge/Si quantum dots [xi] or crystalline defects [xii].

In all these approaches the use of erbium as the dopant can be changed to allow emission at other wavelengths; e.g., ytterbium or terbium allows emission at 0.980 and 0.540 μm in resonant cavity silicon LEDs [xiii]. For these devices to be used in practical applications, however, their lifetimes and reliability still need to be optimized.

Another limitation for all forward-biased silicon light emitters is their low direct modulation speeds ($\sim 1 \text{ MHz}$) [xiv]. This means that realistically this kind of silicon emitter will require an external modulator for high-speed communication links. Reverse biasing has the potential for achieving higher direct modulation speeds ($\sim 200 \text{ MHz}$), but at the moment this comes at the expense of light emission efficiency [xv].

Device Architecture

The work towards a silicon-based emitter is ongoing but still far from mature. Until an efficient, reliable silicon-based light source is available, a photonic integrated system will need to use a conventional III-V material light

emitter. This section describes how a silicon waveguide-based Bragg grating [xvi] can be used in an external cavity to alter the lasing properties of a III-V gain chip to produce a useful source for optical communications. The strong thermo-optic effect in silicon [xvii] can be used to tune the lasing wavelength by heating the silicon grating. The driving force behind this is to produce an inexpensive narrow line-width source suitable for optical communications.

The Bragg grating is fabricated by etching a set of $1.2 \times 2.3 \mu\text{m}$, $3.4 \mu\text{m}$ deep, trenches into a $4 \mu\text{m}$ thick Silicon-on-Insulator (SOI) wafer. One thousand of these trenches are laid out in a line along the waveguide with a range of periods around $2.445 \mu\text{m}$ (although these were laid out as rectangular trenches, due to litho resolution, they were rounded after processing). These trenches are then filled with poly-silicon and annealed to reduce the loss due to the poly-silicon [xviii]. The poly-silicon is then chemically/mechanically polished to obtain a planar surface and the $3.5 \mu\text{m}$ wide, $0.9 \mu\text{m}$ deep rib is patterned using standard lithography and etching. The last step in the fabrication is to deposit a final, $0.5 \mu\text{m}$ thick, low-temperature layer of oxide to provide the necessary upper cladding for the rib waveguides [xvi]. A schematic of the Bragg grating is shown in Figure 1.

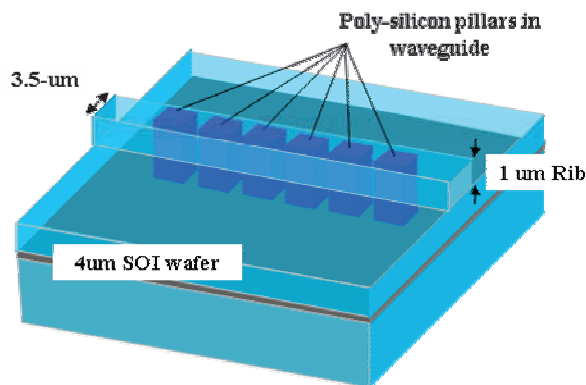


Figure 1: Schematic of polycrystalline-silicon grating in SOI

The novel property of this Bragg grating is that it only reflects a narrow, 0.5 nm wide range of wavelengths back through the waveguide with a reflectivity of 70% [see xvi]. An example of a reflection spectrum from a 1500-trench grating filter is shown in Figure 2. As a separate component these Bragg filters can be used in optical communication networks as channel filters for wavelength division multiplexed systems.

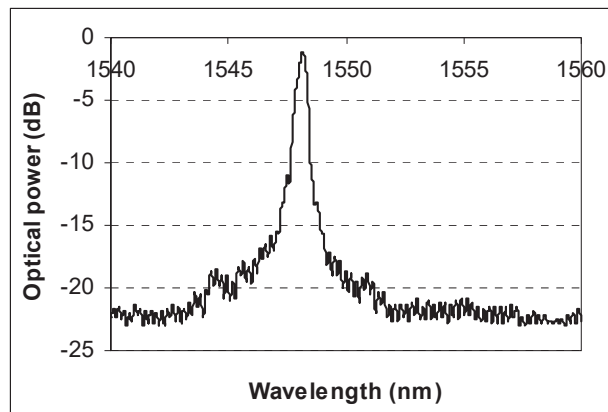


Figure 2: Reflection spectrum of grating filter with 1500 periods at a pitch of $2.455 \mu\text{m}$

The ECL is formed by butt coupling a Single Angled Facet (SAF) gain chip to a waveguide containing the polycrystalline/crystalline silicon Bragg grating. The laser cavity is formed between the Bragg grating as one end mirror, and a 90% high-reflection coating of the gain chip as the other mirror. The 8° angled facet between the two chips decreased the effective reflectivity of that facet to $\sim 10^{-3}$. Combining an angled facet with a 1% anti-reflection coating resulted in an effective facet reflectivity of $\sim 10^{-5}$ [xix]. The output of the laser was taken from the 90% high-reflectivity coated side of the laser diode with a conical polished (140°) lensed single-mode fiber [Figure 3]. The purpose of this lensed optical fiber was to increase the coupling between the laser and the optical fiber.

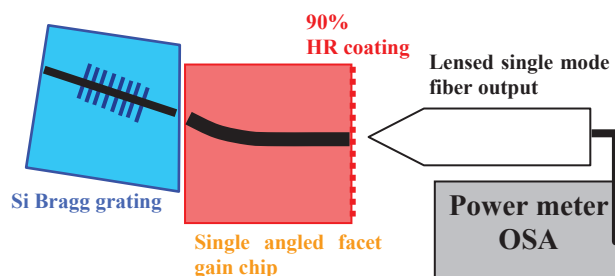


Figure 3: Schematic of the external cavity laser

Technical Results

With the SAF gain chip butt coupled to the Bragg grating, the ECL runs single mode with a line width of 118 MHz , as shown in Figure 4. The optimized output power of the ECL, when the gain chip was driven at 250 mA , as measured out of the single-mode fiber was $450 \mu\text{W}$. The output power is limited by a number of factors: the coupling of the gain chip to the waveguide, the 90% HR coating, and the coupling of the gain chip to the fiber. The 90% output coating can be optimized for increased output

power at the expense of the laser threshold, while the coupling can be enhanced by tapering the silicon waveguide so that its optical mode better matches the mode of the gain chip.

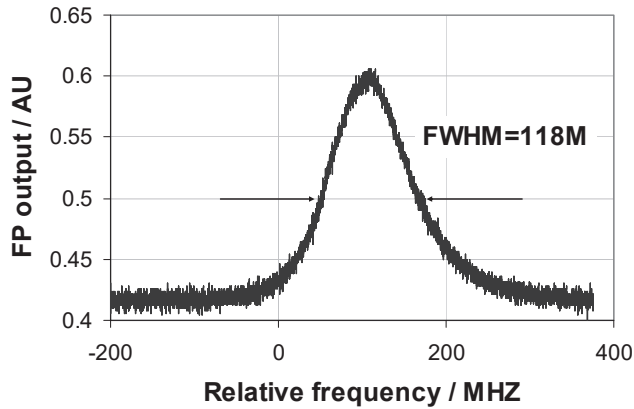


Figure 4: The line-width of the ECL is 118 MHz at 1.539 μm

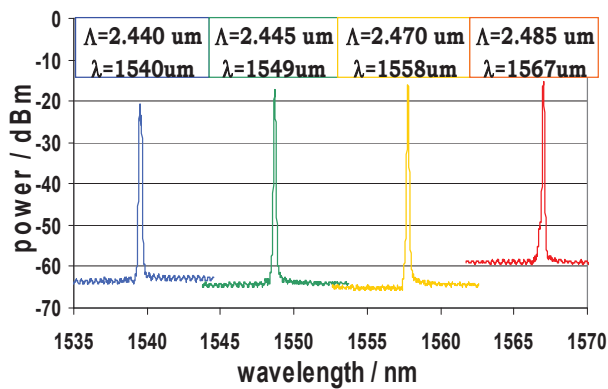


Figure 5: The lasing wavelength (λ) for different periods (Λ) of poly grating

By altering the period of the grating, different wavelengths can be fed back into the gain chip. This allows the lasing wavelength of the ECL to be changed. Figure 5 shows the spectra of the ECL for four different grating pitches. The wavelength range here is limited by the selection of gratings fabricated rather than the gain spectra of the SAF gain chip. The side-mode suppression ratio (ratio of peak emission to background) of the ECL can be seen to be over 40 dB.

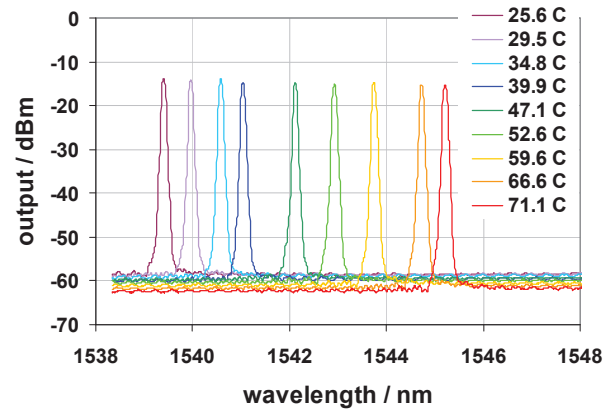


Figure 6: The variation of the output spectra of the ECL with temperature (2.440 μm period Bragg chip)

The refractive index of silicon can be altered by using the thermo-optic effect [xvii]. This means that the Bragg wavelength of the polycrystalline/crystalline silicon grating can be tuned by heating the silicon substrate. This was done by placing the silicon die on a thermo-electric cooler and monitoring its temperature with a thermocouple. As can be seen in Figure 6, heating the 2.440 μm Bragg chip from 27° C to 71° C resulted in a tuning of the ECL from 1.5395 μm to 1.5455 μm . A plot of lasing wavelength vs. die temperature is shown in Figure 7 for three different period gratings. The tuning is linear with die temperature with a rate of 12.6 nm/100° C.

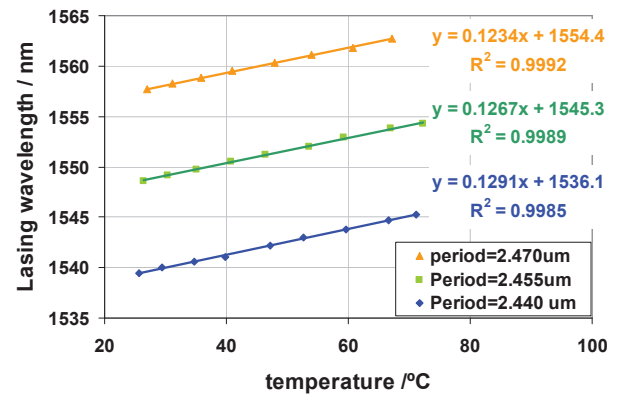


Figure 7: The variation of lasing wavelength with temperature for three different period Bragg gratings

Challenges/Technical Hurdles

In this section the various means of obtaining EL from silicon are discussed. Given the current limited lifetime and efficiency of silicon light emitters, a hybrid integration approach has been taken of coupling a III-V gain chip to an SOI waveguide. The proof of concept of an external cavity, single-mode laser that can be tuned

using the thermo-optic effect at the rate of 12.6 nm/100° C has been demonstrated.

Of course there is still some device optimization that needs to take place to make this ECL a useful building block for silicon photonics. Future work will focus on optimizing the coupling between the silicon waveguide and both the InP gain chip and the output fiber to achieve the 5 mW output power needed for a viable communications system. One approach to achieving this would be to taper the silicon waveguide, which is discussed more in the optical coupling and packaging section.

Tuning speed is another issue. While the thermo-optic effect is relatively large in silicon, it is also rather slow providing tuning speeds between 1 ms and 1 s [xx]. By using other device architectures, e.g., ring resonator structures [xxi], tuning can be achieved by using faster effects, e.g., the plasma dispersion effect. This could provide much faster tuning and potentially allow for more intelligent communication systems.

For photonic integrated circuit applications, the ECL architecture described here, where the tuning is done on one side of the ECL and the output taken from the other side, involves coupling to both sides of the gain medium. This is complicated from a device assembly point-of-view, and different laser geometries are being investigated where both tuning and the laser output can be done by coupling to just one side of the ECL without degrading its output performance.

SI MODULATOR

Background

In the previous section we discussed our approach of coupling a silicon-based Bragg grating filter to an III-V compound semiconductor laser diode to build a narrow line-width, tunable laser. The laser output is a continuous wave, meaning it carries no data or information. To encode data onto this continuous wave of light, for use in an optical communications link, we need an optical modulator. Optical modulator devices with speeds greater than 1 GHz are typically fabricated from either the electro-optic crystal LiNbO₃ [xxii, xxiii] or III-V semiconductor compounds and multiple quantum wells such as GaAs/AlGaAs and InGaAsP-InP, which utilize the quantum confined Stark effect [xxiv, xxv, xxvi] or the electro-absorption effect [xxvii]. These devices have shown modulation frequencies in excess of 40 GHz [xxiii, xxvii].

The demand for low-cost solutions has prompted studies of silicon-based modulators. These are attractive from a cost standpoint because mature silicon processing technology and manufacturing infrastructure already exist

and can be used to build cost-effective devices in volume. In addition, silicon photonics technology provides the possibility of monolithically integrating optical elements and advanced electronics on silicon using bipolar or CMOS technology [xxviii].

Numerous silicon waveguide-based optical modulators have been proposed and demonstrated [xxix, xxx]. The majority of research has focused on using the free carrier plasma dispersion effect in a forward-biased pin diode geometry. This is because unstrained pure crystalline silicon exhibits no linear electro-optic effect, and the refractive index changes due to the Franz-Keldysh and Kerr effects are also small [xxxi]. Since the modulation speed due to the free carrier plasma dispersion effect is determined by the rate at which carriers can be injected and removed, the long recombination carrier lifetime in the intrinsic silicon region generally limits the modulation frequency of these silicon-based devices. Although there is literature showing theoretically that ~1 GHz modulation frequency might be achievable by reducing the waveguide dimensions to sub-micrometer range [xxxii], the previous fastest demonstrated speed of an optical modulator based on current injection in SOI is approximately 20 MHz [xxix, xxx]. These devices are of little practical interest because today's communication networks are demanding GHz performance.

Architecture

Here we present an experimental demonstration of a silicon optical intensity modulator with a modulation bandwidth of 2.5 GHz at optical wavelengths of around 1.55 μm [xxxiii]. This modulation frequency is two orders of magnitude higher than has been demonstrated by any silicon waveguide modulator to date. The high-speed modulation is achieved by using a novel phase shifter design based on a metal-oxide-semiconductor (MOS) capacitor embedded in a passive silicon waveguide Mach-Zehnder Interferometer (MZI). **Figure 8** is a schematic representation of one MZI modulator discussed in this paper. Light wave coupled into the MZI is split equally into the two arms, each of which may contain an active section which converts an applied voltage into a small modification in the propagation velocity of light in the waveguide. Over the length of the active section(s), the velocity differences result in a phase difference in the two waves. Depending on the relative phase of the two waves after passing through the arms, the recombined wave will experience an intensity modulation.

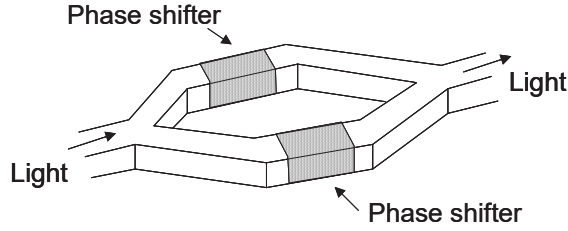


Figure 8: Schematic of a Mach-Zehnder interferometer modulator with two phase shifter sections

The novel component, as well as the essence, of our silicon MZI modulator is the MOS capacitor phase shifter. Figure 9 is a schematic of its cross-sectional view. It comprises a $\sim 1.4 \mu\text{m}$ n-type doped crystalline silicon slab (the silicon layer of the SOI wafer) and a p-type doped poly-silicon rib with a $120 \text{ \AA}$ gate oxide sandwiched between them. The poly-silicon rib and the gate oxide widths are both $\sim 2.5 \mu\text{m}$, and the total poly-silicon thickness at the centre of the waveguide is $\sim 0.9 \mu\text{m}$. In order to minimize the metal contact loss, we designed a wide ($\sim 10.5 \mu\text{m}$) top poly-silicon layer on top of the oxide layers on both sides of the poly-silicon rib. Aluminum contacts are deposited on top of this poly-silicon layer as shown in Figure 9. The oxide regions on either side of the rib maintain horizontal optical confinement and prevent the optical field from penetrating into the metal contact areas. Vertical optical confinement is provided by the $\sim 0.375 \mu\text{m}$ buried oxide and an oxide cover (not shown in Figure 9). Modeling and testing confirm that the waveguide phase shifter is a single-mode device at wavelengths around $1.55 \mu\text{m}$.

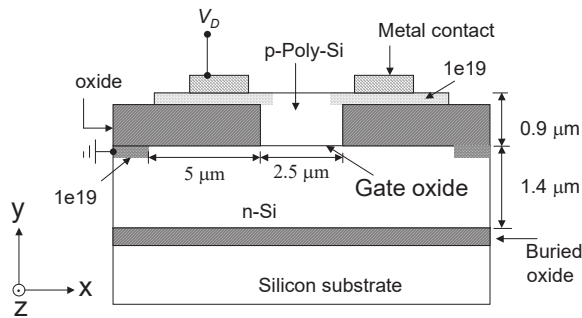


Figure 9: Schematic diagram showing the cross-sectional view of a MOS capacitor waveguide phase shifter in SOI. Optical mode propagates along the z direction.

In accumulation, the n-type silicon in the MOS capacitor phase shifter is grounded and a positive drive voltage, V_D , is applied to the p-type poly-silicon causing a thin charge layer to accumulate on both sides of the gate oxide. The voltage-induced charge density change ΔN_e (for electrons)

and ΔN_h (for holes) is related to the drive voltage by [xxxiv]

$$\Delta N_e = \Delta N_h = \frac{\epsilon_0 \epsilon_r}{et_{ox}t} [V_D - V_{FB}] \quad (1)$$

where ϵ_0 and ϵ_r are the vacuum permittivity and low-frequency relative permittivity of the oxide, e is the electron charge, t_{ox} is the gate oxide thickness, t is the effective charge layer thickness, and V_{FB} is the flat band voltage of the MOS capacitor. Due to the free carrier plasma dispersion effect, the accumulated charges induce a refractive index change in the silicon. At a wavelength of $1.55 \mu\text{m}$, the index changes caused by electrons and holes, which were obtained from experimental absorption spectra through Kramers-Kronig analysis [xxxv], are given by

$$\Delta n_e = -8.8 \times 10^{-22} \Delta N_e \quad (2)$$

$$\Delta n_h = -8.5 \times 10^{-18} (\Delta N_h)^{0.8} \quad (3)$$

where electron and hole density changes are in units of cm^{-3} . The change in refractive index results in a phase shift $\Delta\phi$ in the optical mode given by

$$\Delta\phi = \frac{2\pi}{\lambda} \Delta n_{eff} L \quad (4)$$

where L is the length of the phase shifter, λ is the wavelength of light in free space, and Δn_{eff} is the effective index change in the waveguide, which is the difference between the effective indices of the waveguide phase shifter before and after charge accumulation. Because charge transport in the MOS capacitor is governed by majority carriers, device bandwidth is not limited by the relatively slow carrier recombination processes of pin diode devices. As a result, this capacitor-based design has allowed us to demonstrate bandwidth that is unprecedented in a silicon-based modulator.

Technical Results

Phase shifter performance was evaluated in detail. Figure 10 shows the measured and modeled phase shift as a function of the drive voltage for different phase shifter lengths, $L=1, 2.5, 5$, and 8 mm . The phase measurement was performed in a free space interferometer. The data show good agreement between simulation and measurement for all phase shifter lengths. The measured phase shift is almost linearly dependent on the drive voltage. The data also confirm the linear dependence of the phase shift on the phase shifter length for a given drive voltage, as expected from equation (4). As a figure of merit, the product $V_\pi L$ can be determined from the measured phase shift, where V_π is the drive voltage swing (or $V_D - V_{FB}$) required for π phase shift and L is the device length. Using data in Figure 10, and taking into account the flat band voltage of $V_{FB}=1.25 \text{ V}$, we obtain a $V_\pi L$

product for our current device of 8 V cm. The accumulation capacitance of the MOS structure was measured to be 7pF/mm using an RF impedance analyzer.

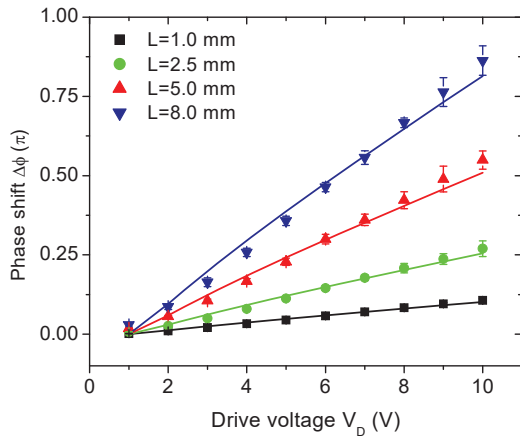


Figure 10: Phase shift $\Delta\phi$ versus drive voltage V_D of the MOS capacitor phase shifter in Figure 9 at a wavelength of $\lambda = 1.55 \mu\text{m}$ for different phase shifter lengths. The symbols represent the measured phase shifters, and the solid lines are the simulated phase shifts.

To facilitate laboratory testing, the arm lengths of the MZI of Figure 8 have been mismatched by $\sim 16.7 \mu\text{m}$ allowing for tuning of the interferometer bias point via small adjustments to the input laser wavelength. For these asymmetric devices, wavelength adjustments of 20 nm or less are sufficient to tune the MZI bias but do not significantly affect other properties of the devices. Y junctions are used to split and combine the optical wave in the MZI, which has an overall length of 1.5 cm. To characterize the performance of our silicon MZI modulator, we measured the optical output intensity as a function of drive voltage for an MZI having a 10 mm phase shifter, in each arm. A slow voltage ramp was applied to one of the two phase shifters. The modulator showed an extinction ratio of more than 16 dB with an applied peak-to-trough voltage of $\sim 7.7 \text{ V}$ which is close to the value of 8 V.cm predicted by the $V_\pi L$ measurements. This device has an on-chip loss of $\sim 6.7 \text{ dB}$, which is mainly attributed to the doped polysilicon phase shifter and undoped polysilicon waveguide. The waveguide loss was measured using the cutback method [xxxvi].

To determine the intrinsic bandwidth of the modulator, we performed a small-signal measurement using an MZI with a single 2.5 mm phase shifter. To ensure the MZI operates in a high-sensitivity region, an input wavelength of $1.558 \mu\text{m}$ was chosen and the MOS capacitor was

biased into accumulation with $3V_{\text{DC}}$. A constant amplitude AC source was delivered to the 17pF MOS capacitor through 50-ohm coax cable, a short section of 50-ohm PCB trace, and a simple network of resistors near the phase-shifter to form an approximate broadband 50-ohm termination. Because of the non-ideal source termination, the voltage arriving at the phase shifter bond pad was monitored with a 6 GHz high-impedance oscilloscope probe. The output light was collected into a 15 GHz high-frequency photo-receiver and measured on an electrical spectrum analyzer. Figure 11(a) shows these measured values. The normalized response of the device (photo-receiver output/on-chip voltage) is presented in Figure 11(b) and shows that the phase shifter has an intrinsic bandwidth of approximately 2.5 GHz (as determined from the -3dB point).

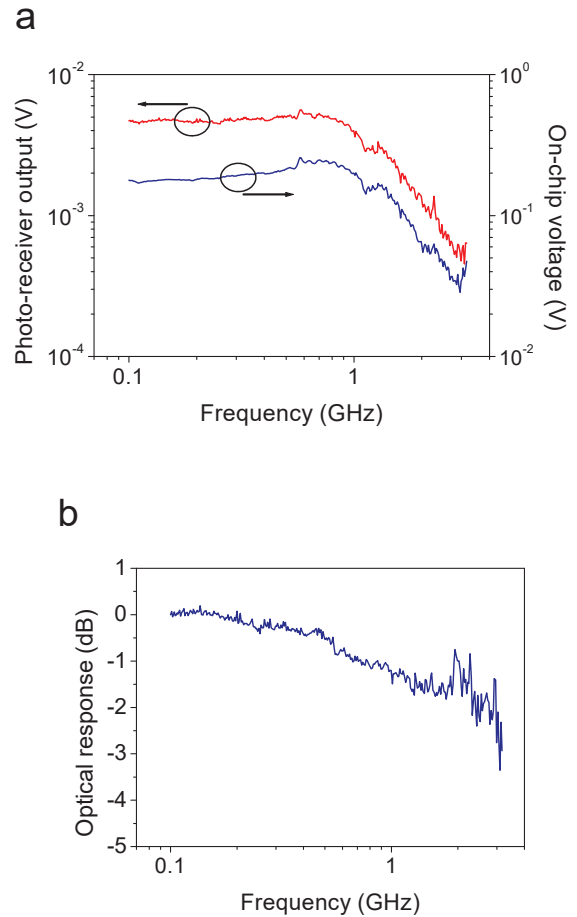


Figure 11 (a): On-chip modulation voltage (V_{RMS}) and photo-receiver output of an MZI containing a single 2.5 mm phase shifter (b): Phase shifter normalized response (photo-receiver output/on-chip voltage) showing an intrinsic bandwidth of approximately 2.5 GHz. The device was biased into accumulation with a 3V DC bias.

To create a large-signal modulation, we used the MZI that has two 10 mm phase shifters. The MOS capacitor is again biased into accumulation with $3V_{DC}$. With an applied single-ended voltage swing of 1.6 V (3.2 V differential swing), the phase shifters should provide sufficient phase shift for the modulator to exhibit an extinction ratio of 5.8 dB when it is biased at quadrature. Figure 12 shows the optical response of the modulator driven with a $2^{32}-1$ pseudorandom bit sequence at 1 Gbps. The data show that the optical signal faithfully reproduces the electrical data stream. Furthermore, the measured high-frequency extinction ratio is 5 dB, which is close to the expected value.

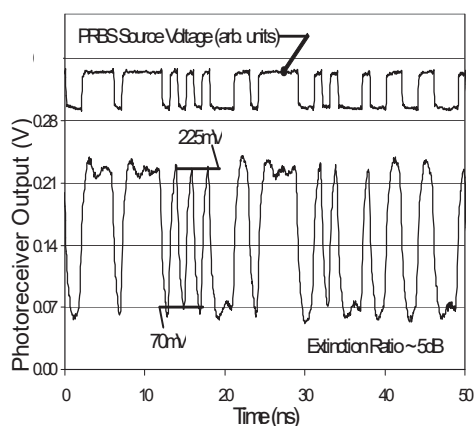


Figure 12: Output signal of a MZI driven with a $2^{32}-1$ pseudorandom bit sequence (PRBS) at 1 Gbps. The MZI has two 1 cm phase shifters and is driven differentially with a total amplitude of 3.2 V (1.6 V single-ended). The RF extinction ratio is 5 dB. The input wavelength was chosen to bias the MZI at quadrature.

Challenges/Technical Hurdles

Our modulator with MOS capacitor phase shifters has demonstrated bandwidth performance previously unseen in silicon modulators, and modeling suggests that high-speed modulation at 10 GHz is achievable with design optimization. To realize such performance improvement, we need to overcome a number of technical challenges, two of which are discussed below.

As mentioned above, our current MZI modulator has an on-chip loss of ~ 6.7 dB, which is primarily due to the doped and undoped polysilicon regions in the waveguide. Because the polysilicon has a much larger optical loss than single-crystal silicon [xxxv], we can significantly reduce the present modulator loss by replacing the polysilicon region with single-crystal silicon. Modeling suggests that we can reduce the on-chip loss to ~ 2 dB by this method. Another approach to lowering on-chip loss is

to create a graded doping profile in the y direction (Figure 9) in the waveguide phase shifter, while still maintaining the device speed. For example, we can design a phase shifter with higher doping densities in the areas close to the gate oxide and metal contacts, but with lower doping concentrations in the rest of the waveguide. Yet another approach is to reduce the active waveguide length required for π phase shift; in other words, increase the phase modulation efficiency. This can be done by reducing the waveguide dimensions, which will increase the interaction between the optical mode and the accumulated charges.

To improve bandwidth performance, the obvious thing to do is to lower device RC. This can be done by increasing the doping levels in the MOS capacitor and reducing the device size. For the moment, however, frequency response of our modulator is limited by other factors, which can be identified by taking another look at the data in Figure 11. The on-chip drive voltage drops to $<50\%$ of its low-frequency value at 1.5 GHz, despite the fact that the intrinsic bandwidth of the optical device is 2.5 GHz. Besides phase shifter capacitance, other contributors to this effect are the output impedance of the drive circuit used and interconnect parasitics. We have been actively engaged with circuit designers to tackle these driver issues. Furthermore, we are reducing the gate oxide thickness of our MOS capacitor to reduce the drive voltage requirements and high-frequency power dissipation.

SI-BASED PHOTODETECTORS

The final active optical component that would need to be integrated onto an all-silicon optical platform is the photodetector. Silicon photodetectors have already found wide acceptance for visible light (0.400-0.700 μm) applications because of their near perfect efficiency at those wavelengths. However, most communication-grade semiconductor lasers are operating in the near infrared wavelength (usually 0.850, 1.310, and 1.550 μm), a region where silicon is a poor detector. In order to improve the performance of silicon-based detectors, the most common approach is to introduce germanium to reduce the bandgap and extend the maximum detectable wavelength. The effect on the absorption coefficient and penetration depth, defined as distance that light travels before the intensity falls to 36% ($1/e$), is clearly shown in Figure 13. The InGaAs material is typical of that used for commercial detectors at 1.310 and 1.550 μm . Note that the data in Figure 13 represent unstrained bulk material with no voltage applied. By introducing strain or electrical bias, it is possible to shift the curves slightly to a higher wavelength due to a reduction in the effective bandgap. This could be critical for detection at 1.550 μm , where a pure Ge film with the appropriate strain or bias

could potentially be shifted to reduce the penetration depth to acceptable values.

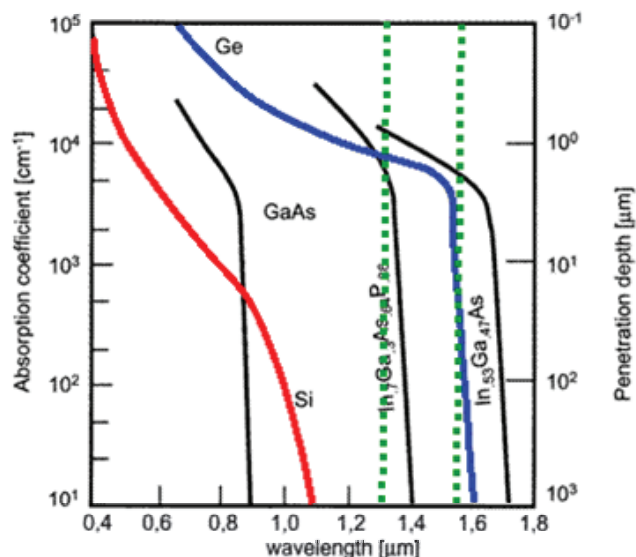


Figure 13: Absorption coefficient and penetration depth of various bulk materials as a function of wavelength. The green lines mark the important wavelengths for telecommunications of 1.310 and 1.550 μm .

Two critical benchmarks for a photodetector are directly related to the absorption coefficient or penetration depth of the light; responsivity, and bandwidth. The responsivity is the ratio of collected photocurrent to the optical power incident on the detector. Responsivities for commercial III-V photodetectors are typically close to 0.8 A/W. Unless the detector is poorly designed, the responsivity should clearly increase as the absorption coefficient increases. The bandwidth of a photodetector can be limited by the transit time required for the photocarriers to travel to the contacts or the RC time constant. If the light penetrates 10 μm into the material, for example, some photocarriers might have to travel 10 μm back to the surface to be collected by a top contact. Typical photodetectors do not have an electric field extending that deep, so the carriers will slowly diffuse up, causing a significant low frequency component to the response. Good detector design eliminates the lethargic diffusion current by using very thin films that can be fully depleted to prevent the generation of diffusion current or effectively reducing the diffusion length of minority carriers. This has been done by using a second (and deeper) p-n junction to siphon off the slow carriers before they can reach the “real” collection junction or by introducing recombination sites near the depletion region to eliminate the carriers. The collection of the much faster drift current is then optimized by keeping the depletion

width as thin as possible as determined by the penetration depth. If the penetration depth can be kept to below 2 μm , the transit time alone could support a bandwidth of 10 Gb/s.

The inherent tradeoff that is made in these devices when the light is incident from above them is that the electrical and optical distances are coupled. Maximizing the light absorption by making the layers thicker results in a reduction of bandwidth due to transit time issues. The way around this problem is to illuminate the device from the side. By doing this, the transit time can be kept low while the effective length of the detector is increased from a few micrometers to as long as a few millimeters. This is the approach used for waveguide-based photodetectors. Another advantage of the waveguide detector is its planar nature, which lends itself to integration with other optical devices.

We are using the same SOI platform as the modulator work to make SiGe waveguide-based photodetectors. A cross-section of this structure is shown in Figure 14 where the SiGe layer is directly on top of a silicon rib waveguide. Our initial detectors used 18 $\text{Si}_{0.5}\text{Ge}_{0.5}$ multiple quantum wells as the absorbing material, with a well thickness of 4 nm separated by 25 nm of silicon Figure 15. They were made on 2.5 and 4 μm thick SOI wafers with waveguide widths varying between 2.5 and 15 μm , and silicon rib etch depths sufficient to achieve multimode operation. The responsivity was as high as approximately 0.1 A/W at 1.319 μm for some devices. We believe that this can be increased to 0.5 A/W through a combination of increasing the number of quantum wells, and changing the placement of the SiGe in the waveguide, among others. Further improvements to responsivity would entail increasing the germanium concentration in the quantum wells, forcing them to even thinner structures to prevent relaxation. This reduced area counters the higher absorption coefficient, pushing any performance gain into the region of diminishing returns. The bandwidth of the devices was limited to below 500 MHz due to a large offset in the valence band that hindered the transport of holes. This can be fixed by altering the film composition, and modeling predicts that data rates approaching 10 Gb/s could be possible. The advantage of this device structure is that it is fully strained, meaning that few, if any, defects are formed in the active SiGe material. These defects are known to increase the dark current of the device that reduce the Signal to Noise Ratio (SNR). Higher optical power would then be needed to compensate and achieve acceptable Bit Error Rates (BER). Our best devices had a dark current of less than 1 μA ($<1 \text{ nA}/\mu\text{m}^2$) at 3 V, which is acceptable for most applications. For comparison, InGaAs pin photodetectors typically have dark currents close to 1 nA.

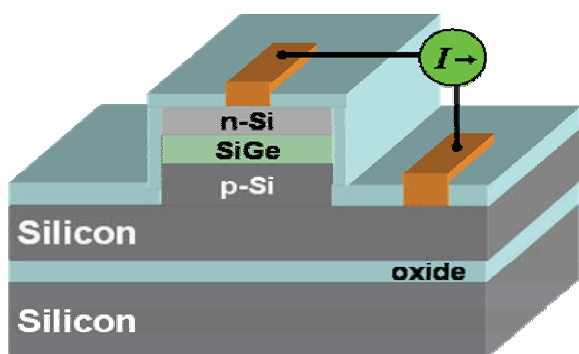


Figure 14: $\text{Si}_{1-x}\text{Ge}_x$ waveguide-based photodetector on a SOI wafer. The waveguide is formed by the ridge of p-Si material and is running perpendicular to the cross-section. The SiGe MQW are inside the region labeled SiGe in the picture.

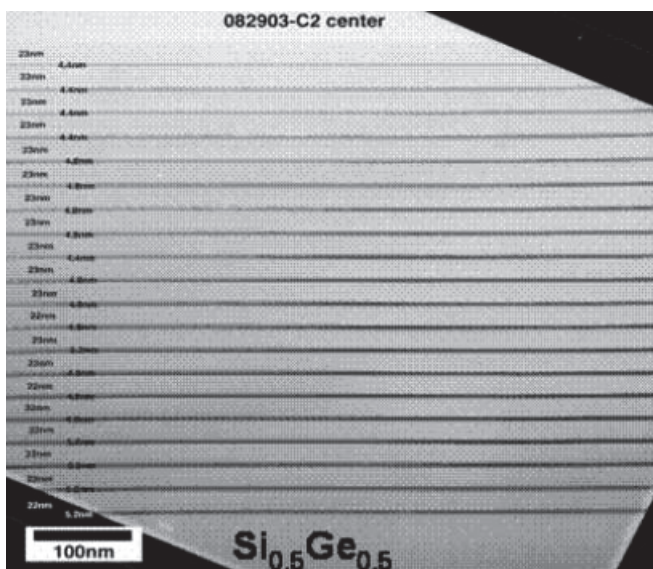


Figure 15: TEM cross-section of a $\text{Si}_{1-x}\text{Ge}_x$ MQW film. The dark regions are the SiGe multiple quantum wells.

Integration Issues with Germanium

The amount of germanium required for efficient photodetection is dependent on the wavelength. If detection at 1.310 or 1.550 μm is desired, then very high (>40%) germanium concentrations are needed. This is much higher than that found in SiGe Heterojunction Bipolar Transistors (HBTs) or strained silicon, and as a result new integration issues have to be dealt with in the fab, including strain and stability.

Since most useful strained $\text{Si}_{1-x}\text{Ge}_x$ films are metastable with respect to defect formation, exposing the wafer to high temperatures after growth can be problematic. Certainly, long times at temperatures above the growth

temperature (550-650° C) should be avoided. Higher temperatures might be possible for short times, such as in rapid thermal annealing, but this is conditional on the film quality. Amorphous, poly-crystalline, or relaxed single crystal films will not have this temperature limitation.

Chemical stability is also an issue for films with high germanium concentration. Since germanium does not form a stable oxide like silicon does when exposed to oxidizing chemicals, the SiGe films tend to be susceptible to corrosion during wet cleans or Chemo-Mechanical Polishing (CMP). We have developed alternate processing modules to accommodate for the difference and maintain the integrity of the SiGe films.

OPTICAL COUPLING AND PACKAGING

One of the most difficult challenges facing high-index contrast optical systems is efficiently coupling light into and out of the chip. Particularly difficult is the coupling of light from a standard optical fiber or external light source to a silicon waveguide. Overcoming these challenges requires the development of processes and structures in addition to the core device.

Tapers

A single-mode fiber core ($n = 1.5$) usually has a diameter of 8 μm with a symmetric mode while a silicon waveguide ($n = 3.45$) is typically only a few micrometers in width with an asymmetric mode. To overcome these large differences in effective index, core size, and symmetry, one frequently used method is to employ a waveguide taper. Tapers allow for a reduction in coupling loss through an adiabatic modal transformation and can also be used to increase the alignment tolerance of other optical devices, such as III-V lasers. Several taper methods have been proposed and have demonstrated efficient coupling from a relatively large silicon waveguide into an optical fiber. Two of these methods are (1) pseudo-vertical tapering and (2) gradual horizontal and vertical modal tapering using gray-scale lithography. Figure 16 is a schematic depiction of these two mode transform designs. Pseudo-vertical tapering from a 12 μm by 12 μm input to 4-5 μm waveguides has demonstrated losses as low as 0.5 dB/facet [xxxvii].

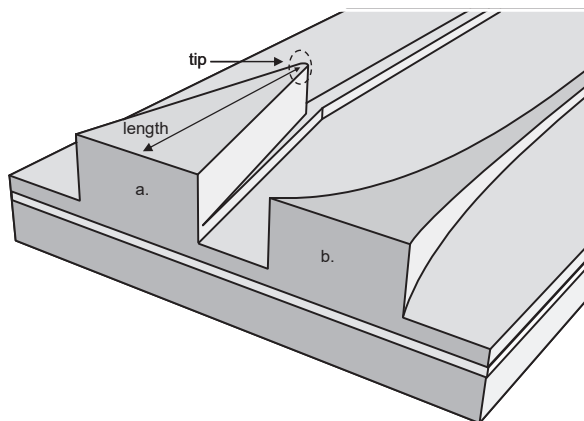


Figure 16: Schematic of (a) pseudo-vertical tapering and (b) 3D gray-scale taper into an SOI-based waveguide

The key processing parameters essential to the success of either mode-transfer device are the lithography and etching processes. For pseudo-vertical tapering, a horizontally tapered waveguide is patterned on top of another waveguide and the optical mode is gradually squeezed from the top taper to the smaller, lower waveguide. The most important parameters for this transition are the length of the taper (the longer the length the more slowly one can transform the mode resulting in lower loss) and the taper tip width (see Figure 16a). In order to reduce optical losses associated with the finite size of the tip width, the tip should be designed such that the minimum width is substantially smaller than the wavelength of light transmitted in the waveguide. Figure 17 shows a Scanning Electron Micrograph (SEM) image of a pseudo-vertical taper patterned onto a Si waveguide at Intel Corporation.

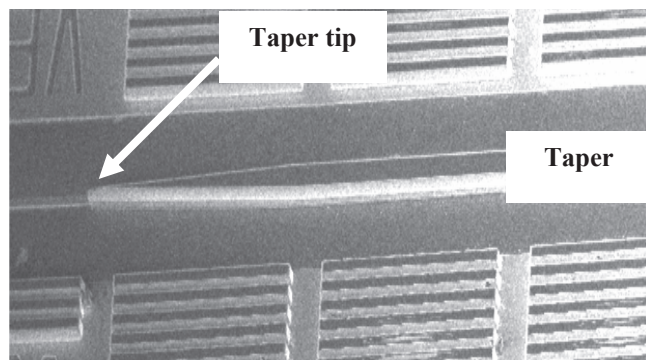


Figure 17: Scanning Electron Micrograph of a pseudo-vertical taper patterned on top of a silicon waveguide

Optimally, the tip width should be small enough to not support an optical mode in the tip region. For

wavelengths of interest around $\lambda_0 \approx 1.550 \mu\text{m}$, this corresponds to a wavelength in silicon of about $\lambda \approx 0.450 \mu\text{m}$. This final tip dependency is very critical, and the effect of tip width variation on taper loss is shown in Figure 18.

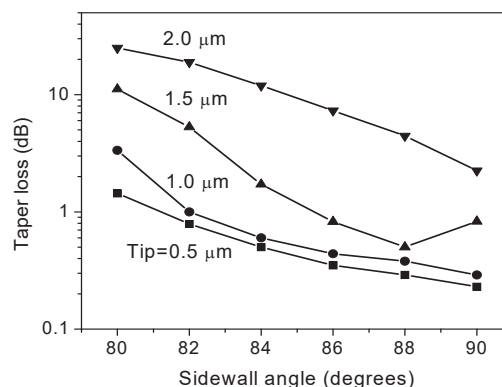


Figure 18: Plot of pseudo-vertical taper loss as a function of sidewall angle for several tip widths

The plot shows results of simulation of a pseudo-vertical taper design starting from $10 \mu\text{m}$ by $10 \mu\text{m}$ and tapering down to $2.5 \mu\text{m}$ by $2.3 \mu\text{m}$, performed by using a commercial software package called BeamPROP [xxxviii], which incorporates finite-difference beam propagation techniques. For this simulation, the loss due to sidewall roughness was assumed to be zero, the taper length was set equal to 1 mm , and a free space wavelength of $1.550 \mu\text{m}$ was used. One can see from Figure 18 that for a fixed side wall angle of 80° , a change in tip width from $2 \mu\text{m}$ to $0.5 \mu\text{m}$ improves the total taper loss by more than 20 dB . Unfortunately, to fabricate such a taper, lithographic patterning and photo resist capabilities are not enough. In order to complete the process, etching these taper devices invariably leads to some rounding of all sharp edges, which inhibits processing the designed sharp point.

In the case of gray-scale techniques, appropriate resists and etch recipes must be created and controlled to provide smooth surfaces and a slow variation of the height of the taper from the input down to the final waveguide dimension. The technique of gray-scale lithography has been known for several years and is widely used in optical Micro Electrical Mechanical Systems (MEMS) to create lenses, prisms, and various other structures [xxxix]. However, gray-scale-based lithography adds additional complexity and cost. A gray-scale reticle is several times more expensive than a standard lithography reticle, and process tweaking to develop and pattern the resist is more complicated than standard processing. Although,

fundamentally, tapers based on gray-scale should result in much lower loss, these types of tapers have not been as prominent as top (pseudo-vertical) tapers.

Another key parameter for processing tapers is that of sidewall roughness and sidewall angle as a result of the silicon etch. Creating taper devices usually relies on significant etching away of silicon material in order to produce the final taper design. Although one can use wet-chemistry for etching, it is often difficult to control and not practical, especially if one would like to obtain vertical sidewalls or more exotic profiles, such as a parabolic design. Thus the most common approach is Reactive Ion Etching (RIE). RIE also has its drawbacks, however, as it produces surface roughness on the exposed sidewall. Since the optical loss due to surface roughness is strongly dependent on waveguide size, the loss due to roughness should be minimal at the beginning of the taper since the taper dimension is large. At the taper end, however, the waveguide becomes smaller and the loss contribution from the roughness becomes larger. Therefore, it is critical to control the surface roughness at the smaller end of the taper. Techniques to reduce loss have been proposed and demonstrated, which involve smoothing waveguides by use of repeated oxidation and stripping steps [xl,xli]. However, oxide smoothing also results in rounding of sharp points which could add additional loss due to tip width rounding.

Another approach to reduce the effect due to surface roughness would be to pattern the taper into a thick Low Temperature Oxide (LTO) layer and then grow the taper using an epitaxial growth step. This may result in lower loss due to the reduction of the silicon etch step but adds complexity into the process which may jeopardize the entire process flow, as discussed previously.

In addition to surface roughness one must monitor the resulting sidewall angle of the pseudo-vertical taper after silicon etching is complete. Figure 19 shows the effect of the sidewall angle on the taper loss. It can be seen that a sidewall angle variation from 90° to 80° can increase the loss by up to 20 dB for a given tip width.

Top tapers have been successful for coupling to waveguides with cross-sectional dimensions of 4-5 μm , but modeling suggests that these designs may not work well when the waveguides are smaller than 2 μm . This is true even with a tip width as small as 0.05 μm and a tapering length of 5.2 mm. Thus a different approach must be used for coupling to very small waveguides (on the order of 1 μm or less) to standard optical fibers. Alternative approaches have recently been proposed for coupling to sub-micron waveguides, including the use of grating assisted couplers [xlii] and inverted tapers [xliii].

Fiber Attach

In order to integrate the optical devices, discussed in this paper, into optical networks, they must be integrated with fibers. As discussed in the previous section, the small waveguide dimensions and high index contrast of the silicon system lead to a fundamental difference in the optical mode profile between the waveguide and fiber. The integration of waveguide tapers at the waveguide/fiber interface can solve this problem.

Current fiber attach techniques are “active,” relying upon the closed loop optimization of fiber position in order to ensure low loss coupling. This technique is time consuming however and hence costly. Passive alignment techniques for fiber attachment remove the need for closed-loop optimization by creating highly precise lithographically defined structures on the silicon surface in order to align the fiber to the waveguide aperture. A photograph of passively aligned fibers using an etched U-shaped groove processed by Intel is shown below in Figure 19.

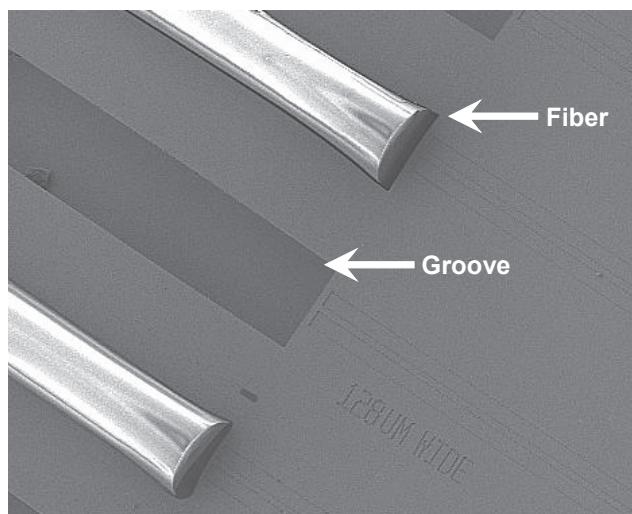


Figure 19: Scanning Electron Micrograph of several U-grooves, two of which are populated with optical fibers and aligned to silicon waveguides

Active alignment techniques are typically capable of placement tolerances better than 1 μm . The accuracy required of a passive alignment technique will depend upon the mode field overlap of the fiber and waveguide modes, which can be controlled by the waveguide tapers, discussed in the earlier section. As an example, the lateral alignment tolerance of an 8 μm single-mode fiber core to a 13 μm x 13 μm square waveguide input facet was modeled using FIMMPROP [xliv]. The modeled results, based on film mode matching and local mode expansion methods, indicate that the lateral alignment tolerance is ~ 1.7 μm for 1 dB excess loss. By increasing the input taper to 15 μm by 15 μm , the alignment tolerance is

increased by over 50% to $\sim 2.6 \mu\text{m}$. The achievable accuracy of the passive alignment technique will depend upon both the processing tolerance of the etched U-groove and also upon the manufacturing tolerance of the fiber. Widely accepted fiber specifications define the fiber diameter to $\pm 1 \mu\text{m}$ of accuracy; newer fibers are specified to $\sim \pm 0.3 \mu\text{m}$ of accuracy. The combination of the waveguide tapers and tightly specified fiber will require that the trench dimensions be defined to $\sim 1\text{-}2 \mu\text{m}$ of accuracy, a challenging although not unrealizable goal. Additionally the large index contrast of the silicon waveguide will result in a reflection of $\sim 30\%$ at each silicon/air interface unless an anti-reflection (AR) coating is used. The etched facets created in the passive alignment process for fiber attachment are readily amenable to wafer scale AR coating using standard dielectric films available in a CMOS fab.

FUTURE POSSIBILITIES

We now look ahead at two next-generation optical devices in silicon, examining opportunities for additional miniaturization and functionality of optical components.

Unlike the case for silicon electronics, significant changes to silicon photonics cannot be brought about through direct scaling and reduction of Critical Dimensions (CDs). Rather, changes to the underlying physics of operation will be needed to radically change optical device designs. Some of the more recent developments in materials processing have helped develop an area of research focused on devices using critical dimensions on the order of nanometers. In the current landscape of silicon photonics, two “nano-photonics” technologies are of particular interest: Photonic Crystals (PCs) and Ring Resonators (RRs).

Photonic Crystals

Photonic crystals are the optical analog to electronic semiconductor crystals. Through the periodic arrangement of two materials with dissimilar dielectric constants, a PC will exhibit a band of forbidden frequencies of propagation (Photonic Band Gap (PBG)). This PBG is analogous to the forbidden energy gap of semiconductors; just as forbidden electronic states are due to the periodic arrangement of atoms in a crystalline lattice, the periodic arrangement of dielectrics on the order of the wavelength of light creates an optical gap (see Figure 20). The most common example of a PC is a 1-dimensional Bragg grating for which a forbidden optical gap or “stop-band” is achieved. For most 2-dimensional planar SOI-based PBG waveguides, a triangular lattice of holes in silicon is used (see Figure 21).

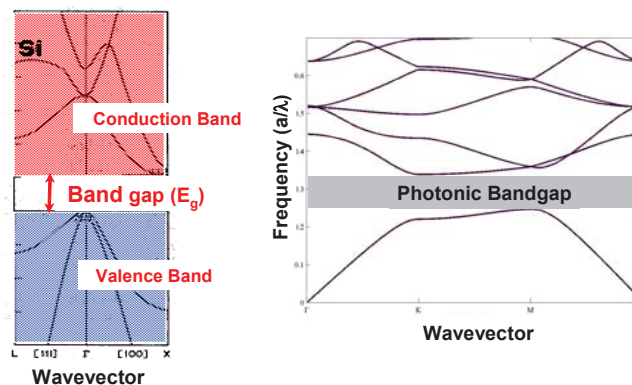


Figure 20: Examples of (a) electrical energy band gap for a semiconductor (silicon), and (b) a photonic band gap for a photonic crystal, where a is the pitch of the lattice

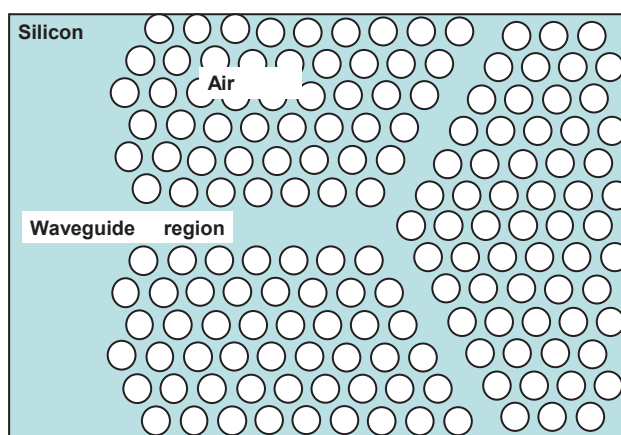


Figure 21: Schematic (plan view) of a Photonic crystal comprised of holes arranged in a triangular lattice in silicon

Photonic crystals have been gaining considerable research attention since reports by researchers working in silicon were brought to mainstream attention. Their dispersive properties and nonlinear optical effects, combined with the promise to drastically reduce the dimensions of common optical designs are fueling many of the PC research efforts found in literature today, such as super prisms [xlv,xlvi,xlvii] and ultra-low threshold lasers [xlviii,xlix]. Almost all research conducted in 2-dimensional planar PCs designed for $1.55 \mu\text{m}$ and $1.31 \mu\text{m}$ light are processed using e-beam lithography. Several advantages of research e-beam lithography systems (e.g., Raith 150) are their relatively low cost, ability to pattern $< 20 \text{ nm}$ features, and their ease of use for processing pieces of wafers. The same e-beam system can have patterning times of 30 minutes or more for a $10 \mu\text{m}^2$ field with a 50% pattern density of 100 nm minimum feature sizes. Most PC structures (holes) designed for 1.55 and $1.31 \mu\text{m}$

light are of similar dimensions/design rules as those for 0.130 μm and 0.090 μm CMOS transistor designs. One group at the Interuniversity Micro-Electronics Center (IMEC) in Belgium has fabricated PCs with conventional Deep-UV Lithography and Reactive Ion Etch techniques [1]. Their successes with 0.18 μm technology node tools have demonstrated a compatibility with PC designs. This in turn has brought increased attention to the possibility of pursuing PC research in a modern high-volume fab. The only additional complexity to optical lithography-based patterning of PCs vs. e-beam patterning is that for 1.55 and 1.31 μm PC designs, CD control requires Optical Proximity Correction (OPC) to design layouts. Overall, standard optical lithography can deliver equal or better results than most research e-beam systems for today's planar optical designs. In addition, by using standard fab equipment, PC designs-of-experiments can be dramatically expanded by skewing lithography and etch parameters across one experimental run. The most challenging processing problems that face PCs, whether fabricated using e-beam or DUV lithography, are coupling losses and optical loss through the waveguides. Several groups have managed to demonstrate relatively low-loss couplers to these small waveguide designs [li, lii]. Recently, researchers at IBM managed to create PC waveguides in SOI with transmission losses as low as 20 dB/cm [liii].

Ring Resonators

Optical Ring Resonators (RRs) are useful components for wavelength filtering, multiplexing, switching, and modulation. The key performance characteristics of the RR includes the Free-Spectral Range (FSR), the finesse (or Q factor), the resonance transmission, and the extinction ratio. These quantities depend not only on the device design but also on the fabrication tolerance. Although state-of-the-art lithography may not be required for most conventional waveguide designs, RR and PC designs require CD values at or below 100 nm.

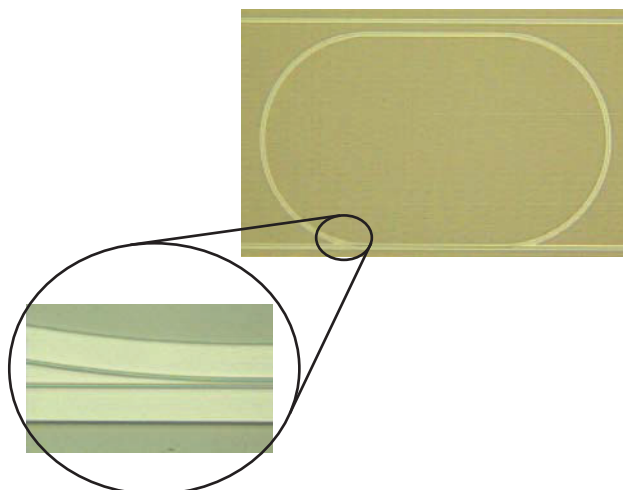


Figure 22: Example of a Ring Resonator device fabricated in silicon. The expanded region in the inset shows the separation between the straight “bus” and the resonator “ring.”

For such designs, resolution and CD control are both important to the success of the devices. In the case of Si-based ring resonators, one of the critical parameters to control is the coupling efficiency between the RR and the input/output waveguide. As a compact waveguide (for example, 220 nm x 500 nm strip waveguide) is usually used in the RR to obtain a large FSR, the gap between the ring and bus waveguide is 100-200 nm (inset of Figure 22). Since the device operates through evanescent coupling, the coupling is exponentially dependent on the size of the separating gap. Thus, in order to reliably process high-Q RR devices, control of a few nm demands CD control readily achieved by modern 0.18 μm or 0.13 μm lithography.

CONCLUSION

Although research in the area of planar optics in silicon has been underway for several decades, recent efforts at Intel Corporation have provided better understanding of the capabilities of such devices as silicon modulators, ECLs, and SiGe detectors. Incorporating silicon in an ECL opens a path towards hybrid silicon photonic integration, or even a Silicon Optical Bench (SiOB) platform for silicon photonics. Silicon modulators operating at 2.5 GHz have demonstrated two orders of magnitude improvement over other known si-based modulators, with theoretical modeling indicating performance capabilities beyond 10 GHz. And initial results from SiGe photodetectors have shown the feasibility of monolithically integrated waveguide detectors. Through further research and demonstration of novel silicon photonics devices, we hope to continue bringing the vision of integrated silicon photonics into focus as a viable future for commercial opto-electronics.

Mexico. His e-mail address is andrew.c.alduino at intel.com.

Richard Jones is a senior researcher in the Photonics Technology Lab of Intel's Corporate Technology Group. His research interests include integrated optical components and bio-photonics. He received his Ph.D. degree in Biomedical application of ultra-fast lasers from Imperial College, University of London in 1997. His e-mail is richard.jones at intel.com.

Ling Liao is a senior researcher in the Photonics Technology Lab of Intel's Corporate Technology Group. Her recent work has focused on developing high-speed optical phase shifters and modulators. She holds both B.S. and M.S. degrees in Materials Science and Engineering from the Massachusetts Institute of Technology. Her e-mail is ling.liao at intel.com.

Ansheng Liu is a senior researcher developing silicon photonic devices in the Corporate Technology Group. Before joining Intel in 2000, he worked at NASA Ames Research Center, the National Institute of Standards and Technology, and at the University of Aalborg as an assistant professor. His interests include nonlinear optics of nanostructures, near-field optics, opto-electronics, and photonics. Ansheng received his Ph.D. degree from the University of Aalborg in 1992. His e-mail is ansheng.liu at intel.com.

Mike Morse is a senior researcher in the Photonics Technology Lab of Intel's Corporate Technology Group. He is currently working on SiGe photodetectors and epitaxial processes for the modulator. Mike received a Ph.D. in Materials Science and Engineering from MIT in 1997, and a B.S. in Ceramic Engineering from Ohio State University in 1991. His e-mail is mike.morse at intel.com.

Mario Paniccia is director of the Photonics Technology Lab where he leads a research team focused on developing silicon-based photonic building blocks using standard CMOS processing for future use in enterprise and data center communications. Mario earned a B.S. degree in Physics in 1988 from the State University of New York at Binghamton and a Ph.D. degree in Solid State Physics from Purdue University in 1994. Mario has been working at Intel since 1995. His e-mail is mario.paniccia at intel.com.

Mike Salib is a senior researcher in the Photonics Technology Lab of Intel's Corporate Technology Group. His technical interests include photonic crystals and tapers. Mike earned B.S. and Ph.D. degrees in Physics from the State University of New York at Buffalo in 1993 and 1998, respectively. He has been working for Intel since 1998. His e-mail is michael.s.salib at intel.com.

Dean Samara-Rubio is a senior researcher in the Photonics Technology Lab of Intel's Corporate Technology Group. Dean's contributions include design of integrated circuits and optical components, optoelectronic characterization, and silicon modulator project management. Dean received a Ph.D. in Electrical Engineering from the University of Texas at Austin in 1997, and a B.S. degree in Electrical Engineering from the University of Illinois at Urbana-Champaign in 1991. His e-mail is dean.samararubio at intel.com.

Copyright © Intel Corporation 2004. This publication was downloaded from <http://developer.intel.com/>.

Legal notices at
<http://www.intel.com/sites/corporate/tradmarx.htm>.

REFERENCES

- i G T Reed and A P Knights: *Silicon Photonics: An Introduction*, John Wiley and Sons, ISBN: 0-470-87034-6.
- ii MA Green, J Zhao, A Wang, PJ Reece, and M GAL, "Efficient silicon light-emitting diodes" *Nature* 412 page 805 (2001).
- iii L Pavesi, L Dal Negro, G Mazzoleni, G Franzo and F Priola, "Optical gain in silicon nano-crystals," *Nature* 408, 440-444 (2000).
- iv AG Cullis, LT Canham, and PDJ Calcott, "The structural and luminescence properties of porous silicon," *Applied Physics Reviews* 82 no 3, 909-965 (1997).
- v R Claps, D Dimitropoulos, and B Jalali, "Stimulated Raman scattering in silicon waveguides," *Electronic letters* 381352-1354 (2002).
- vi L Martinelli, E Grilli, M Guzzi, MG Grimaldi, "Room temperature electro-luminescence of ion-beam synthesized b-FeSi₂ precipitates in Si," *Applied Physics Letters* 83 no 4 794-796 (2003).
- vii G Franzo, S Coffa, F Priola, and C spinella, "Mechanism and performance of forward and reverse bias electroluminescence at 1.54 μ m from Er-doped Si diodes," *Journal of Applied Physics* 81, 2784-2793 (1997).
- viii S Coffa, G Franzo, F Priola, A Polman, and R Serna, "Temperature dependence and quenching processes of the intra-4f luminescence of Er in crystalline Si," *Physics Review B* 49 16313-16320 (1994).
- ix A Irrera, D Pacifici, M Miritello, "Electro-luminescence properties of light emitting devices based on silicon nanocrystals," *Physica E* 16, 395-399 (2003).
- x G Franzo, D Pacifica, V Vinciguerra, F Priola, and F Iacona, "Er³⁺ ions-si nanocrystals interactions and their effects on

- the luminescence properties," *Applied Physics Letters* 76, 2167-2169 (2000).
- xi WH Chang, AT Chou, WY Chen, HS Chang, TM Hsu, Z Pei, PS Chen, SW Lee, LS Lai, SC Lu and M-J Tsai, "Room temperature electroluminescence at 1.3 and 1.5 μm from Ge/Si self assembled quantum dots," *Applied Physics Letters* 83 No 14 pp 2958-2960 (2003).
- xii WL Ng, MA Loenco, RM Gwilliam, G Shao, and KP Hoemwood, "An efficient room-temperature silicon based light emitting diode," *Nature* 410, 192-194 (2001).
- xiii S Coffa, ME Castagna, M Monaco, A Muscara, and S Loretti, "High efficient light emission devices in silicon," *Photonics West*, Proc SPIE 2004.
- xiv TI Cox, AJ Simons, A Loni, PDJ Calcott, LT Canham, MJ Uren, and KJ Nash, "Modulation speed of an efficient porous silicon light emitting device," *Journal of Applied Physics* 86 no 5, 2764-2773 (1999).
- xv LW Snyman, M du Plessis, E Seevinck, and H Aharoni, "An efficient low voltage, high frequency silicon CMOS light emitting device and electro-optical interface," *IEEE Electron Device Letters* 20 no. 12 614-616 (1999).
- xvi L Liao, A Liu and M J Paniccia, "Tunable bragg grating filters in SOI waveguides," Submitted for publishing IPR 2004.
- xvii R A Soref and B R Bennett, "Electrooptical effects in Silicon," *IEEE J Quant Elec* 23 123-129 (1987).
- xviii A M. Agarwal, L Liao, J S Foresi, M R. Black, X Duan, and L C Kimerling, "Low-loss polycrystalline silicon waveguides for silicon photonics," *Journal Applied Physics*, 80 6120-6123 (1996).
- xix P J S Heim, Z F Fan, S H Cho, K Nam, M Dagenais, F G Johnson and R Leavitt, "Single-angled-facet for widely tunable external cavity semiconductor lasers with high spectral purity," *Elect Lett* 33 1387-1389 (1997).
- xx I. Abe, O. Frazão, P. S. André, J. C. Cardozo da Silva, H. J. Kalinowski, J. L. Pinto, F. M. Araújo, "The use of Fibre Bragg Gratings Filters in Optical Communications," *3rd Conference on Telecommunications - Conftele* 2001, pp. 276-278, Figueira da Foz, Portugal, Abril 2001.
- xxi B Liu, A Shakouri and J E Bowers, "Wide Tunable Double Ring Resonator Coupled Lasers," *IEEE Phot. Tech. Lett.* 14 600-602 (2002).
- xxii E. L. Wooten et al. "A review of lithium niobate modulators for fiber-optic communications systems," *IEEE J. Selected Topics in Quantum Electron* 6, 69-82 (2000).
- xxiii M. M. Howerton, R. P. Moeller, A. S. Greenblatt, and R. Krahenbuhl, "Fully packaged, broad-band LiNbO₃ modulator with low drive voltage," *IEEE Photon. Technol. Lett.* 12, 792-794 (2000).
- xxiv J. E. Zucker, K. L. Jones, B. I. Miller, and U. Koren, "Miniature Mach-Zehnder InGaAsP quantum well waveguide interferometers for 1.3 μm ," *IEEE Photon. Technol. Lett.* 2, 32-34 (1990).
- xxv J. S. Cites and P. R. Ashley, "High-performance Mach-Zehnder modulators in multiple quantum well GaAs/AlGaAs," *J. Lightwave Technol.* 12, 1167-1173 (1992).
- xxvi M. Fetterman, C.-P. Chao, and S. R. Forrest, "Fabrication and analysis of high-contrast InGaAsP-InP Mach-Zehnder modulators for use at 1.55 μm wavelength," *IEEE Photon. Technol. Lett.* 8, 69-71 (1996).
- xxvii T. Ido et al., "Ultra-high-speed multiple-quantum-well electro-absorption optical modulators with integrated waveguides," *J. Lightwave Technol.* 14, 2026-2034 (1996).
- xxviii R. A. Soref, "Silicon-based optoelectronics," *Proc. IEEE* 81, 1687-1706 (1993).
- xxix C. K. Tang and G. T. Reed, "Highly efficient optical phase modulator in SOI waveguides," *Electron. Lett.* 31, 451-452 (1995).
- xxx P. Dainesi et al. "CMOS compatible fully integrated Mach-Zehnder interferometer in SOI technology," *IEEE Photon. Technol. Lett.*, 12, 660-662 (2000).
- xxxi R. A. Soref and B. R. Bennett, "Electro optical effects in silicon," *IEEE J. Quantum Electron*, QE-23, 123-129 (1987).
- xxxii A. Irace, G. Breglio, and A. Cutolo, "All-silicon optoelectronic modulator with 1 GHz switching capability," *Electron. Lett.* 39, 232-233 (2003).
- xxxiii A. Liu, R. Jones, L. Liao, D. Samara-Rubio, D. Rubin, O. Cohen, R. Nicolaescu, and M. Paniccia, "A high-speed silicon optical modulator based on a metal-oxide-semiconductor capacitor," *Nature* 427, 615-618 (2004).
- xxxiv Sze, S. M., *Physics of Semiconductor Devices* 2nd ed. (Wiley, New York, 1981).

- xxxv Soref, R. A. and Bennett, B. R., "Kramers-Kronig analysis of electro-optical switching in silicon," *Proc. SPIE* 704, 32-37 (1986).
- xxxvi Liao, L. et al., "Optical transmission losses in polycrystalline silicon strip waveguides: effects of waveguide dimensions, thermal treatment, hydrogen passivation, and wavelength," *J. Electron. Mater.* 29, 1380-1386 (2000).
- xxxvii I. Day et al., "Tapered silicon waveguides for low insertion loss highly efficient high speed electronic variable attenuators," *IEEE OFC*, March 24-27, 2003.
- xxxviii www.rsoftdesign.com*
- xxxix M.B. Frish, et al., 2002 IEEE International SOI Conference. Proceedings: *IEEE*, 2002. pp. 165-166.
- xl K. Lee, et al., *Optics Letters* 26, 1888-1890 (2001).
- xli L. Lai, E.A. Irene, "Limiting Si/SiO₂ interface roughness resulting from thermal oxidation," *Journal Applied. Physics*, 86, 1729-1735 (1999).
- xlvi G. T. Reed, C. E. Png, G. Masanovic, S. T. Lim, S. P. Chan, W. Headley, T. W. Ang, A. Liu, and M. Paniccia, "Silicon nanophotonic circuits," Invited Paper, *XLVII ETRAN Conf.*, 813 June 2003, Herceg Novi, Serbia and Montenegro.
- xlvi V. R. Almeida et al., "Nanotaper for compact mode conversion," *Optics Letters* Vol. 28, No. 15, August 2003, p. 1302-1304.
- xliv www.photond.com*
- xlv L. Wu et. al, "Superprism Phenomena in Planar Photonic Crystals," *Journal of Quantum Electronics*, vol. 38, No. 7 July 2002, pp. 915-918.
- xlvi H. Kosaka et. al, "Superprism Phenomena in Photonic Crystals: Toward Microscale Lightwave Circuits," *Journal of Lightwave Technology*, vol. 17, No. 11 November 1999, pp. 2032-2038.
- xlvii Toshihiko Baba and Masanori Nakamura, "Photonic Crystal Light Deflection Devices using the Superprism Effect," *Journal of Quantum Electronics*, vol. 38, No. 7 July 2002, pp. 909-914.
- xlviii A. Scherer, et al., "Photonic Crystals for Confining, Guiding, and Emitting Light, IEEE Transactions on Nanotechnology," Vol. 1, No 1, March 2002, pp. 4-11.
- xlix M. Loncar, et al., "Low-threshold photonic crystal laser," *Applied Physics Letters*, Vol. 81, No 15, October 2002, pp. 2680-2682.
- I W. Bogaerts et al., "Fabrication of Photonic Crystals in Silicon-on-Insulator Using 248-nm Deep UV Lithography," *Journal of Selected Topics in Quantum Electronics*, Vol. 8, No. 4 July/August 2002, pp. 928-934.
- li V. R. Almeida, et al., "Nanotaper for compact mode conversion," *Optics Letters*, Vol. 23, No 15, August 1, 2003 pp. 1302-1304.
- lii H. Yokoi, et al., "Nonreciprocal TE-TM mode converter with semiconductor guiding layer," *Electronic Letters*, Vol. 38, No 25, December 2002, pp. 1670-1671.
- liii S.J. McNab and Yu. A. Vlasov, "SOI 2D Photonic Crystals For Microphotonic Integrated Circuits," *Digest of the IEEE-LEOS Summer Topical Meetings*, 2003, p. 79, IEEE Catalog Number 03TH8701, ISBN 0-7803-7982-9.

Copyright of Intel Technology Journal is the property of Intel Corporation and its content may not be copied or emailed to multiple sites or posted to a listserv without the copyright holder's express written permission. However, users may print, download, or email articles for individual use.