

3D Interconnect through Aligned Wafer Level Bonding

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Abstract

Wafer Level Packaging and 3-D Interconnect Technologies are driven by the increasing device density, functionality as well as the reduction of total packaging costs. Many devices such as PDAs, memory cards, smart cards and cellular phones utilize the resulting chip scale packages. Key enabling technologies for 3D Interconnect are high precision alignment and bonding systems and thick resist processing. Unique processing equipment has been developed to meet requirements of high volume production. This paper will review advances in equipment processing capabilities and provide a guideline for new processing techniques available.

Wafer to wafer alignment can be carried out in various different ways. Traditionally aligned wafer bonding is a well-established technology in the MEMS (Micro Electro Mechanical Systems) industry. Special requirements for 3D Interconnects are highest accuracy, the use of single side processed wafers and 8 inch capability. A comparison of wafer alignment technologies will be presented. Additionally a novel face-to-face alignment method will be described and analyzed regarding accuracy of alignment before and after bonding.

Wafer bonding is carried out subsequently to the alignment step in a separated process module. A summary of different bonding methods will be given. Intermediate layers that act as bonding agent can be spun on to the wafer. Such coating processes for wafer level packaging applications vary greatly from the requirements for VLSI (Very Large Scale Integration) processing. VLSI photoresist processes use thin layers to transfer small features with sub-micron tolerances. Wafer level bumping typically is performed with 5 – 150 micron films, to transfer large (20 – 250 micron) features, with tolerances approaching micron scale. High Density Interconnect (HDI) applications require thicker adhesive layers. The paper concludes with application examples with different intermediate layers such as BCB.

1. Introduction

Wafer level packaging (WLP) and 3D interconnection technologies (advanced packaging) are most promising solutions to achieve more than one layer of active devices. Device stacking is justified by the potential benefits attainable: size reduction, increase in "silicon efficiency", reduction of signal time delay, reduced parasitic, decrease in power consumption, increase in speed, increase in number of neighboring devices and extension of bandwidth. Any issues with thermal management and increased design complexities will not prevent stacking technology from eventually being accepted. Wafer-to-wafer alignment and subsequent bonding are key enabling process steps for 3D interconnection of

wafers through stacking. Application examples for increased functionality through stacked wafers include Memory Devices, Logic & Memory wafer, Advanced MEMS, Optical & Electrical wafer, Analog/Digital wafer (mixed signals).

3-D interconnect bonding is the process of bonding two (or more) device wafers together with the intention of creating a three dimensional network of circuitry. The process steps involved in the aligned bonding procedure are the application of an intermediate layer, wafer alignment, and bonding. Because of the high density of interconnects required between the substrates, a large degree of alignment is necessary between the substrates to ensure proper assembly. An additional constraint is placed on the process by the fact that the IC industry almost exclusively uses single side processing. Therefore, process equipment has been developed that allows the high precision, face to face alignment of wafers. Figure 1 shows two wafers, which are aligned and bonded together using an adhesive layer. Copper vias connect the conventional interconnects on both wafers, with high aspect ratio backside contacts.

2. Intermediate Layers for Wafer Bonding

Present advanced packaging applications require a bonding platform that can accommodate wafer-to-wafer bonding in various sizes and configurations. In addition, it is important to have the ability to perform the process repeatedly without compromising in precision¹.

For R&D applications, the scale must apply to substrates ranging in size from pieces smaller than 10 mm square, through 200 mm wafers. Manually loaded single chamber bonding systems are ideally suited for this purpose. For high volume production (Figure 1) fully automated systems are

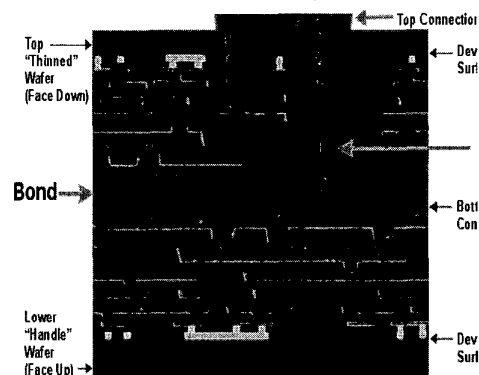


Figure 1. Schematic view of 3-D chip stacking.

Courtesy of Focus Center – New York, Rensselaer: interconnections for Gigascale Integration.

required with face-to-face alignment capability combined with an automated 200 mm bonding system with multiple bond chambers. Bonding Systems for both R&D applications and fully automated integrated systems feature bond forces of up to 40 kN, class 1 clean room compatible stainless steel base designs, and temperatures up to 550°C with excellent uniformity, stability and reproducibility. A clear roadmap for availability of 300 mm systems in 2002 can be provided.

These major technical features are necessary in order to be suited for the large variety of intermediate layers for advanced 3D Interconnects and packaging applications such as:

- Solder alloys, requiring low temperature and low force.
- Gold to gold wafer bonding, requiring high temperature and high force.
- Copper to copper wafer bonding, requiring high temperature and high force.
- Aluminum to Aluminum wafer bonding, requiring reducing atmosphere (forming gas), high temperature and high force.
- Anodic bonding, requiring high temperature, high vacuum and high voltage.
- Silicon Direct Bonding (SDB), requiring ultra-clean bond environment
- Polymer bonding, requiring low temperature, low force and high vacuum.

The use of low temperature or low contact force is imposed by the different materials present onto the wafer surface (e.g. metal layers, semiconductor epi-layers, low-k dielectrics) or by the mechanical properties of the bonding partners (fragility, thermal mismatch).

During the bonding process the intermediate layer gets compressed. A flow of viscous materials must be minimized in order to maintain alignment accuracy. Post bond alignment accuracy identical to pre bond accuracy has been observed at certain conditions. Typical post bonding results are within +/- 1 micron from pre bonding across 200 mm wafer diameter. Integrated production systems achieve post bond alignment accuracy better than 1µm (3 sigma).

3. Application of Low-k Dielectrics

One of the main benefits of using polymers as intermediate layers is the lower processing temperature requirement (in the order of 150 – 300°C) compared to most metal to metal bonds. Among the possible materials are low-k dielectrics such as BCB (Cyclotene™) and spin on dielectrics (SOG). A variety of other polymers are currently under investigation². The application of the intermediate layer prior to aligned bonding is a key step for successful bonding.

Thick resist coatings are a requirement for many MEMS and IC process steps. Highly uniform coats at low material usage have been achieved. Two approaches to apply BCB have been investigated in the EV Group application lab: spin coating and spray coating.

The most commonly used approach is spin coating of such materials. Thick film thickness is largely dependent on the rotational speed used in the coating process in relation to the

viscosity of the resist. A major difference exists between spin coating of thick and standard resists. The first is the low solvent to resist ratio for most of the thick photoresists and polymers. The result of this is the second major difference, a much higher viscosity than is found in standard resists.

The use of an integrated cover prevents solvent evaporation within the coating chamber, creating a solvent rich atmosphere. This reduces the loss of solvent within the resist, allowing the resist to spread evenly to the thickness that is determined by the rotational speed. This effect can be further optimized by the addition of an exhaust/purge system that can be used to precisely control the level of solvent within the spinning chamber. The use of this integrated cover with the coating system (Figure 2) improves the repeatability and coating uniformity. Required thickness or polymers for subsequent bonding processes ranges from 3 micron to 20 micron with uniformity approaching 1%.

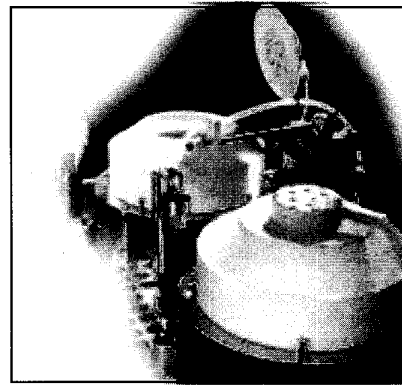


Figure 2: Coating system with integrated bowl cover

Spray coating is an alternative to spin coating and can be especially useful for higher topography wafers, rectangular substrates or substrates with etched trough via holes. The achieved resist thickness in the spray coating process is dependent on the amount of dispensed material as well and the programmed motion of dispense arm and spinner chuck.

While the wafer rotates slowly with 30-100 rpm, the atomizing nozzle starts spraying right outside the wafer area and moves over the wafer center to the other side (Figure 3). To get uniform layer thickness over the whole wafer, the speed of the nozzle increases towards the wafer center and decreases from there on outwards according to a recipe controlled speed profile.

Tests were made using blank 200 mm Si wafers. The average uniformity achieved through spray coating over one wafer batch (25 coats) is 7.5%. For flat wafers this is about 4 times higher than in a spin coat process. Using high topography or non-round substrates the uniformity of spray coating can be superior to spin coating. A significant reduction in material usage to about 30% was observed using the spray coating process. Figure 4 summarizes the results.

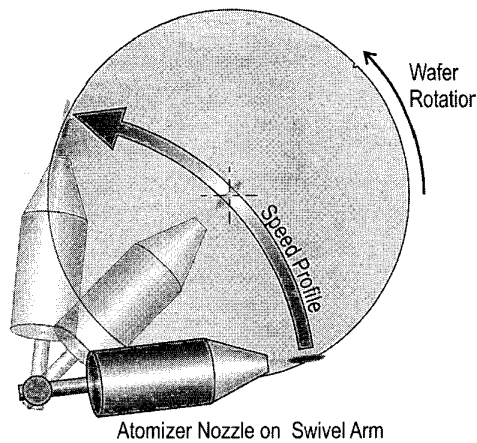


Figure 3: Schematic sketch of the dynamics in the spray-coating process. The wafer is slowly rotated while the polymer spray is dispensed across the wafer diameter.

BCB 4024-40 Application 5 μ m on 200mm Wafers

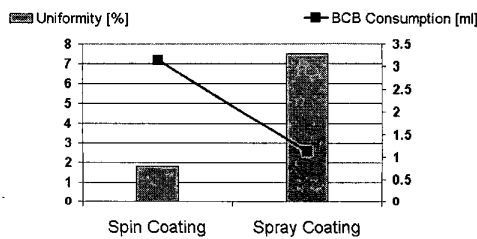


Figure 4: Uniformity and Consumption for a 5 μ m thick BCB coat on 200 mm Wafer achieved through spin and spray coating.

4. Wafer Alignment

Interconnects can be formed using deep etched cavities (vias) in one wafer³. This would require the assembly to be thinned subsequent to stacked wafer bonding. Usual procedures for the thinning process⁴ are: mechanical grinding, lapping, reactive ion etching (RIE), wet etching, and ADP-DCE (Atmospheric Downstream Plasma – Dry Chemical Etching). After thinning, the vias become accessible from the topside allowing the process to be repeated, so that a stack of multiple wafers can be achieved (Figure 5). A final thinning step can then be performed on the backside of the resulting wafer stack. In order to produce a flip chip or chip scale package, bumps can be created at wafer level using thick resist lithography. Unlike MEMS wafers that frequently involve double sided processing, IC and CMOS wafers are always processed on a single side. Therefore wafer to wafer alignment must use alignment targets situated in the bond interface. The following paragraphs will present the methods and the respective equipment that is utilized to perform alignment and bonding processes.

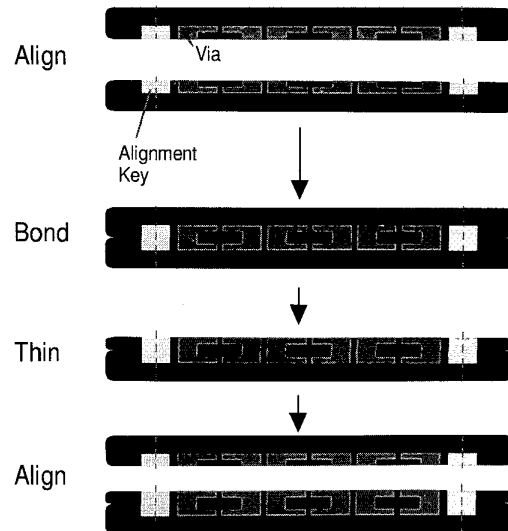


Figure 5: 3D Interconnects through aligned wafer bonding

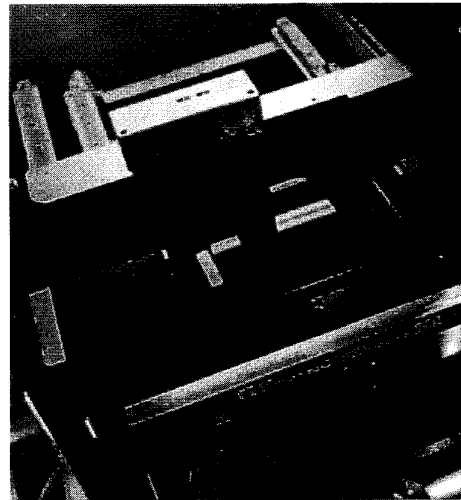


Figure 6: Photograph of a close-up view of the SmartView™ aligner optics

To realize high levels of device integration, alignment must be precisely performed. Many different alignment methods are available, however, most suffer from one or more issues that prevent them from being utilized as a generic solution⁵. A new alignment approach is required. The SmartView™ alignment system (shown in Figure 6) is able to achieve micron alignment tolerances using a face-to-face alignment method, thus potentially eliminating extra processing steps, such as back side alignment key definition.

A schematic of the SmartView™ working principle is shown in Figure 7. Instead of using a single microscope in between the wafers, as is used in other substrate alignment platforms, the SmartView™ system employs two microscopes for alignment. One microscope is placed above and the other below the wafer stack. The dual microscopes focus on a common optical axis calibrated for each alignment. Each

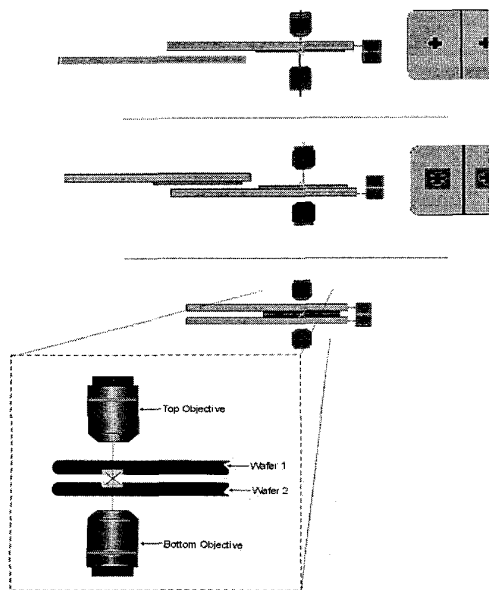


Figure 7: Process overview of precision aligned wafer to wafer bonding using the SmartView™ face-to-face alignment

microscope objective observes one alignment key on the surface of the wafer.

The detailed process flow of SmartView™ alignment is presented below:

Step 1: The top wafer is loaded face up and is then rotated face down and loaded into the alignment position. Next it is observed by the bottom optics. The optics are adjusted to bring the alignment keys into view, and then the image is digitized and stored electronically.

Step 2: The top wafer is retracted, the bottom wafer is loaded and brought into position beneath the top optics and then aligned to the existing digitized image of the top wafer. Once complete the two wafers are automatically moved into alignment by calculating the relative X and Y locations of the alignment keys on each wafer and moving the wafers into the final alignment position.

Step 3: When alignment is completed the wafers are brought into contact and secured for bonding.

Wafer alignment is accomplished using encoded stage motors allowing X and Y movements in increments of 0.1 μm steps and minimized Z-axis travel controlled by three software controlled spindle motors to preserve planarization between the top and bottom wafers. The repeatability of the measurement system is $<0.35 \mu\text{m}$.

Figure 8 shows typical alignment results between pairs of 200 mm wafers by using the SmartView™ wafer-to-wafer bond alignment system. All pairs of wafers are within 1.5 micron alignment accuracy in X and Y. The standard deviation in this graph is between 0.3 and 0.4 microns.

5. Integrated Systems for Alignment and Bonding

All of the above mentioned processes require equipment today for R&D mode and future high volume production of 3D integrated devices. Availability of fully automated

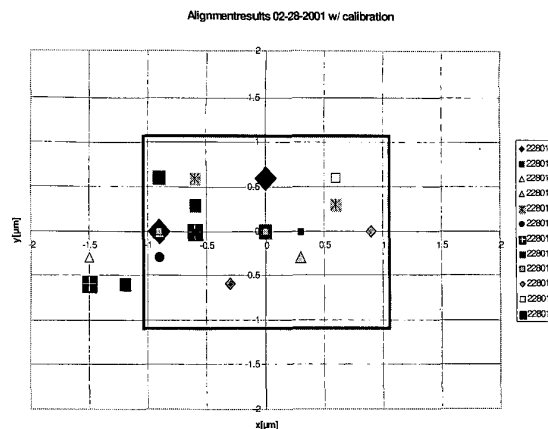


Figure 8: SmartView™ Alignment Results

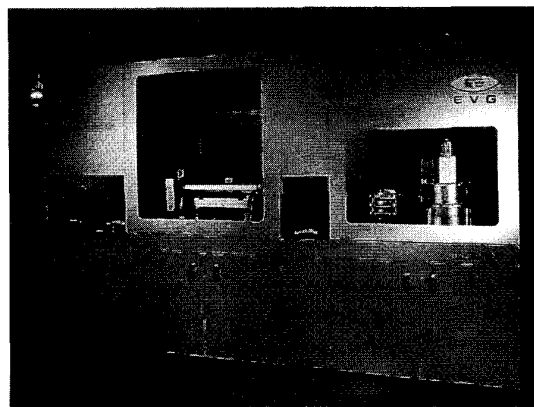


Figure 9: GEMINI™ fully automated production bond system with SmartView™ alignment and multiple bond chambers

production equipment such as EV Groups GEMINI™ (Figure 9) an automated wafer bonding system with integrated SmartView™ alignment will be key to fast volume ramp up. Further a clear roadmap showing 300mm systems in 2002 is provided.

6. Conclusions

3D Interconnect offers a promising approach to increase device density and functionality. Required process steps and equipment features for wafer level aligned bonding were reviewed. Several different intermediate layers are currently being investigated for bonding. Low temperature dielectrics are one candidate with the benefit to keep the bonding temperature low.

Application of BCB (Cyclotene™) was performed using spin and spray coating with good uniformity and optimized material usage. Today's bonding systems for future high volume production of 3D interconnected wafers are fully integrated and support 200 mm with a clear roadmap to migrate to 300 mm within 2002.

SmartView™ alignment is a new alignment technology developed for wafer stacking providing submicron accurate face-to-face alignment.

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