

Compliant Bumps for Adhesive Flip-Chip Assembly

Kathryn Keswick, Randy L. German, Mark Breen, and Rick Nolan

Abstract—Flip-chip-on-glass (FCOG) is susceptible to electrical opens for a variety of reasons including, but not limited to, movement in the Z -axis caused by flip-chip adhesive CTE and water absorption of the adhesive. Flip-chip assembly to co-fired ceramic and laminate substrates suffers from these problems as well as others, such as bow or twist in the substrate and bond pad height irregularities. Success with adhesive flip-chip connections to these substrates has, to date, been limited. Commercially available adhesives have either failed to produce reliable bonds, or have suffered from long cure time or a lack of reworkability.

A solution to these problems has been demonstrated by forming compliant bumps on the chip or substrate bond pads using a photo-imagible polymer coated with a thin layer of gold. Bumps $17\text{ }\mu\text{m}$ tall with diameters between $17\text{ }\mu\text{m}$ and $95\text{ }\mu\text{m}$ have been fabricated and bonded. The resulting compliant bump structure provides 30% of the bump height ($5\text{ }\mu\text{m}$) within the elastic compression range. This compliance eliminates many of the demands placed on the assembly adhesives by other electrical contacting methods (such as solid metal bumps or particles). Compliant bumps allow the use of commercially available, fast curing, easily reworkable adhesives for reliable flip-chip assembly.

MCC's compliant bumps have been mechanically cycled from minimum compression (needed for electrical contact) to maximum compression (based on diminishing compression distance versus applied force) 1000 times, with minimal degradation of the polymer core or metal overcoat. Assemblies have been subjected to temperature cycling and steam pot aging with substantial improvement in reliability when compared to assemblies using solid metal bumps. Using compliant bump technology, low temperature rework has been demonstrated with compliant bumped chips on glass, laminate and MCM-C substrates. Chips or substrates with compliant bumps are re-usable, a significant advantage over conventional gold bump processes where the bump structure is permanently deformed by the bonding process.

I. PROBLEM SOLVED

FOR THE past three years, MCC and its member companies have led several efforts to commercialize adhesive flip-chip technology. As part of these efforts, we have identified several reliability and manufacturability barriers to widespread use of adhesive flip chip.

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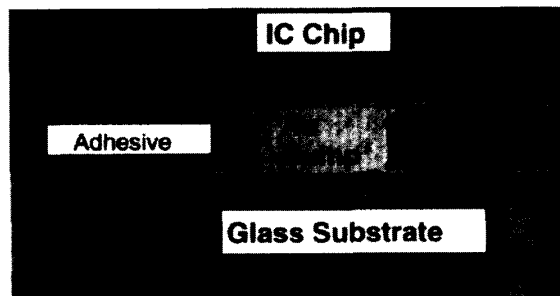


Fig. 1. "Microbump" adhesive flip-chip technology is fine-pitch capable, but the gold bumps' lack of compliance limits reliability.

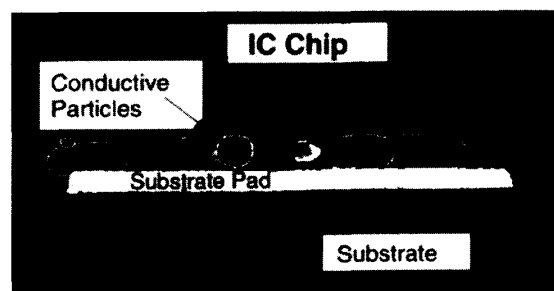


Fig. 2. " Z -axis" adhesive flip chip is limited to relatively large I/O pitch, and the small particle size produces a thin adhesive bond line that produces excessive stress in the bonded assembly.

Failures occur in adhesive flip-chip assemblies on glass or ceramic for a variety of reasons. Electrical connections in most adhesive flip-chip technologies are achieved through pressure contact between chip and substrate pads. This contact pressure is maintained throughout the product's life by tensile stress in the adhesive. Loss of electrical contact can occur when the adhesive expands or swells in the Z -axis direction, due to thermal expansion or moisture absorption. Gross delamination and tensile stress cracking can occur in the adhesive when the bond stresses are excessive [1].

Adhesive flip-chip systems commonly use solid metal bumps (Fig. 1), or solid metal or metal-coated polymer particles (anisotropically conducting adhesives, or ACA, see Fig. 2) to achieve electrical connections from the chip to the substrate [2]. This is because the chip pad is typically recessed $1\text{ }\mu\text{m}$ or more in the chip passivation coating. Other chip or substrate topography may also preclude electrical contact without some sort of bump or particle between the chip and substrate.

In the case of ACA flip-chip technology, the particles are relatively small (less than $10\text{ }\mu\text{m}$ diameter) [3]. This is so that

3D Model Results



Fig. 3. 3-D finite element modeling predicts excessive stresses at the corners of this "Z-axis" adhesive flip-chip assembly.

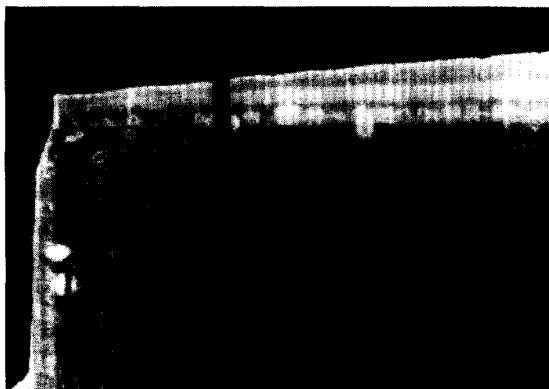


Fig. 4. Test vehicle results confirm modeling predictions. This sample exhibits delamination and tensile stress cracking in the corners and around the bondpads after exposure to MIL-STD 883 Schedule B conditions.

they can be spaced as closely as possible without touching to insure reliable "Z-axis" conductivity without lateral conductivity. The resulting bond line thickness is also less than $10\text{ }\mu\text{m}$, resulting in high tensile stresses—particularly at the corners of the chip (see Figs. 3–5). Technologies using solid metal bumps have an advantage in that they can optimize bond line thickness for optimum stress levels by adjusting bump height. Unfortunately, taller bumps and thicker bond lines aggravate another problem. The CTE of the metal bump is typically much lower than that of the adhesive. As the assembly increases in temperature, the adhesive expands faster than the bump, resulting in an open circuit.

Because of these issues, adhesive flip-chip technology requires an adhesive with extraordinary mechanical properties. CTE and moisture absorption must be very low, while glass transition temperature, storage modulus, and tensile and adhesion strengths must be high. Few adhesives have been found to meet these requirements. When one is found, it typically has manufacturability problems such as a short pot life, lack of reworkability, residual ionics, or a long cure time. To date, successful adhesive flip-chip bonding has been achieved mainly with heat-curing epoxies which are far from ideal. When bonding on opaque ceramic or laminate substrates, heat curing adhesives are required. For display driver applications,



Fig. 5. "Z-axis" adhesive flip chip on glass assembly. The arrow points to a crack in the silicon chip that propagates along an "iso-stress" plane predicted by the finite element models.

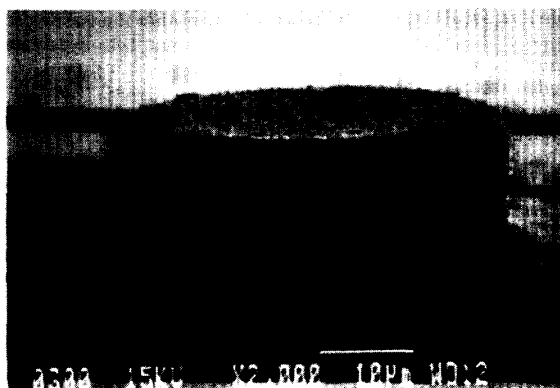


Fig. 6. Oblique view of an MCC compliant bump. The concave top surface is due to polymer shrinkage during cure.

UV curing adhesives are more desirable because they can be cured at low temperatures [4]. UV curing also eliminates the bonder "dwell" time needed to raise the bonder thermode to curing temperature and then cool it down again.

II. METHOD OF SOLUTION

A solution to these problems has been demonstrated by forming compliant bumps on the chip or substrate bond pads (see Figs. 6 and 7). Standard tape automated bumping (TAB) processes and equipment are used to form polymer bumps on IC wire bond pads. The pad and bump are then overcoated with gold metallization. The bumps are elastically compressible up to 30% of the total bump height, which dramatically alters the mechanics of adhesive flip-chip bondings (see Figs. 8 and 9). The result is reliable, cost-effective flip-chip assembly and rework using commercially available adhesives.

The compliant bump process can be used for bumping either substrates or die. Chip wafer bumping is generally the most cost-effective, since many chips are prepared for each piece processed. Substrate bumping results in fewer chip sites

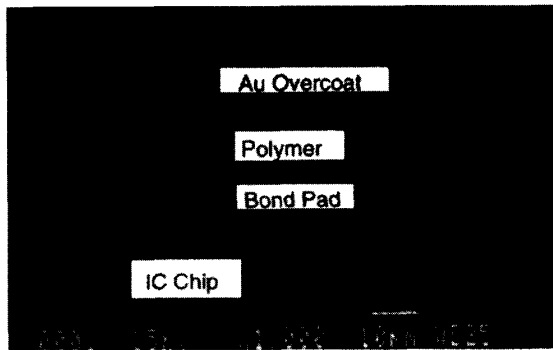


Fig. 7. Cross-sectional view of a compliant bump.

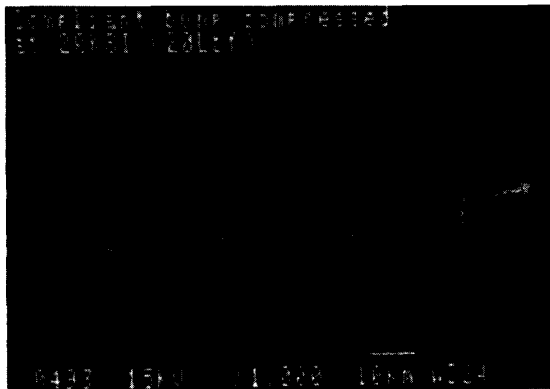


Fig. 8. Compliant bump assembled to borosilicate glass, using an assembly force of 20 lb. The bump is compressed to about 85% of its original height.

bumped per piece processed, but is attractive if the assembly uses chips from many different suppliers (or chips not available in wafer form). Demonstrations thus far have been on silicon wafers with aluminum pads and silicon nitride passivation (see Fig. 10). Finished bump height is currently $17\text{ }\mu\text{m}$ for an assembled height of around $14\text{ }\mu\text{m}$ (determined to be optimum through finite element analysis and test vehicle results). Bump diameters range from 18 to $93\text{ }\mu\text{m}$.

The compliancy of the polymer provides a mechanism by which the bumps can adjust for warp or bow or pad height nonuniformities in the substrate. Better bump height uniformity can be achieved with polymer bump processing compared to conventional electroplating. Polymer bump uniformity was measured at 3% whereas gold bump uniformities average 10%. Polymers respond elastically over a larger range of strain loads than metals. These factors allow bonding forces to be lower than with solid metal bumps, because there is no need to plastically deform metal bumps to correct for bump nonuniformity. Therefore, a wider range of bonding parameters can be used, while ensuring electrical continuity.

Process parameters can also be optimized to reduce as-bonded stress. In conventional adhesive flip-chip systems, as-bonded stress is maximized to provide insurance against loss of electrical contact due to moisture-induced swelling, creep-relaxation, and thermal expansion. With compliant bumps, the

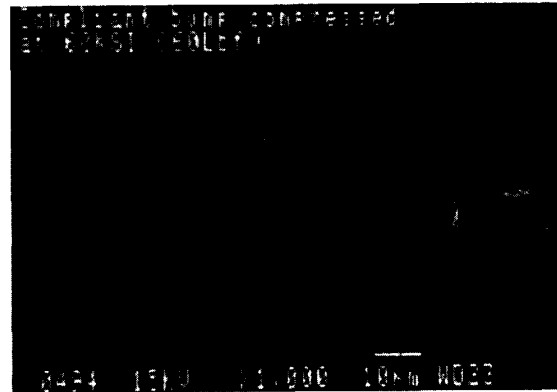


Fig. 9. Another compliant bump flip-chip assembly. Assembly force was 60 lb, resulting in an approximately 30% compression of the bump.

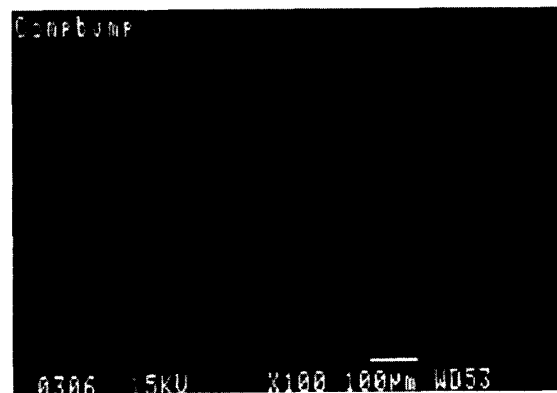


Fig. 10. MCC compliant bumps fabricated on a wafer of 216I/O, 150- μm pitch silicon test chips.

bump tends to spring back to its original height. Even if the bump's composite CTE is lower than the bonding adhesive, or if the adhesive absorbs moisture and swells, the bump will maintain a contact force commensurate with its effective compression modulus until it has returned to its original height. The effective compression modulus of the bump can be tailored by adjusting the polymer composition and/or the metal plating thickness.

Desired polymer properties are: high glass transition temperature (T_g), high yield stress, linear elastic response over a large stress-strain region, and a high compressive strength. Many polymers available today satisfy these requirements. A high T_g is optimum for assemblies that operate at elevated temperatures because material creep occurs at temperatures near the T_g . If the T_g is too near the high end of the temperature operating region then material creep could cause an electrical open circuit. Young's or elastic modulus varies slightly with temperature, but it is not markedly temperature dependent—therefore a high modulus is desirable, although not required. However, too high of a modulus could result in a very brittle material that would fracture under large bonding forces. Compliant bump technology provides for a wide range of bump sizes and shapes.

III. PROCESS DESCRIPTION: POLYMER BUMP FORMATION

Three approaches to bump formation are proposed: dry etch, wet etch, and photoimaging processes. Each process uses a polymer material as the core of the bump but the bumps are formed by different processing sequences. First, the polymer material is applied to the wafer/substrate, then the material is imaged or masked and removed from the field areas so that a polymer bump is formed on top of the bond pads. Alternative proposed process sequences for metallization will be described later.

A. Dry Etch Process

The dry etch approach to compliant bump formation uses plasma etch processing. The polymer material is coated onto the substrate and then cured. An etch mask is used for pattern definition—the mask material can be an erodable mask made of resist or a metal hard mask. The mask is patterned either by photolithography or wet etching. After the mask is imaged, the polymer material is etched to form the bumps.

There are advantages and disadvantages to the dry etch process approach. One advantage is that the side wall profile can be modified by adjusting the etch process parameters. One problem is that very large aspect ratios are difficult to achieve. This is because the undercut is large with hard masked, dry etch processes when etching very thick films. Etch rates for polymer dry etch processes are 0.5 to 2.0 $\mu\text{m}/\text{min}$. Subsequently, for very thick films the etch process is lengthy and throughput is low.

B. Wet Etch Process

Wet etch processing of the polymer is similar to the dry etch approach, but pattern definition is achieved by wet chemical etch instead of plasma. The polymer material is coated onto the substrate and partially cured. Photoresist is then coated over the polymer, and the photoresist is exposed and developed to form the etch mask. Lastly, the polymer is etched to form the bumps. The advantages to this approach over dry etch are that no costly dry etching equipment is necessary and there are fewer steps. This approach may be limited by geometry, and very large aspect ratios are difficult to fabricate. Additionally, sidewall profiles are not easily modified when using wet etch materials. Bump height uniformity is very good when using the wet etch approach.

C. Photoimaging Process

Bumps are formed using a photoimaging polymer, resulting in significant process simplification. As with the other two approaches, the substrate is coated with the polymer material, but no etch mask is required. The bumps are formed by directly exposing and developing the polymer material. The advantages to this approach are that bump size and shape can be modified by varying the exposure parameters, large aspect ratios are obtainable, and processing is quick and simple and can be performed using conventional photolithography equipment. Bump height uniformities are very good with this approach. For these reasons, MCC's development work has focused on

photoimaging polymers. Most photoimaging materials shrink up to 50% during cure, resulting in a slight dish-shaped bump after cure. During the bonding process, the bump's top surface conforms to the mating pad's topography.

IV. PROCESS DESCRIPTION: METALLIZATION

Several processing options are available for coating metal onto compliant polymer bumps, including direct wet metallization processing using conventional PCB techniques, subtractive metallization using sputter or evaporation deposition, or additive processing using a sputtered or evaporated plating buss with a plating mask. There are advantages and disadvantages with each process.

A. Direct Metallization

The wet metallization process makes use of standard techniques used in the PCB industry. The process consists of applying a plating catalyst to the polymer bump and electrolessly plating a ductile metal, such as gold, onto the bump and surrounding bond pad. Wet metallization processes permit high throughput of parts and do not require a vacuum metallization step. However, care must be taken to insure that the aluminum electrodes of the IC device are not damaged by the wet metallization process. A barrier metal may be needed to protect the aluminum from the wet metallization process. In addition, a resist mask may be needed to prevent plating on the IC passivation.

B. Pattern Etching

A subtractive approach can be used to apply metal to the polymer bumps. This process consists of depositing the metal over the entire surface of the substrate in the desired thickness, by evaporation or sputtering, and applying an etch mask to the bumps, then etching the field metal away. The subtractive technique described has few steps and can be done with equipment available in a typical integrated circuit (IC) manufacturing facility. However, this is a costly method, because the metal thicknesses required can result in lengthy evaporator cycles, and most of the metal deposited in the vacuum deposition process is etched away.

C. Pattern Plating

An electroplating process can also be used to metallize the polymer bumps. An electrolytic plating approach requires that a thin plating buss be deposited, typically by sputtering, and then a plating mask must be applied to define the desired areas to be plated. After electroplating in the desired areas, the plating mask and the plating buss are removed. An additive process using electroplating could be performed using equipment that is commonly used in the printed circuit board (PCB) industry. This method is more cost-effective than pattern etching because the evaporator/sputter cycle times are short, and very little material is lost in the final etching process. This metallization approach was used to demonstrate the feasibility of the compliant bump process approach.

V. FABRICATION COST ANALYSIS

Conventional solid metal bumping techniques usually include sputtering a thin metal interconnect layer onto a passivated substrate. The substrate/wafer is masked using photoresist and metal is electroplated into the resist openings. Finally, the resist and metal interconnect are removed. This method is simple, well established, and has high yield. A typical price for gold bumps on a 4 in wafer is \$150/wafer. If compliant bumps solve the problems noted in the introduction at a competitive cost, this technology is suitable for a wide range of applications. The analysis that follows looks at the cost of producing compliant bumps using a polymer/metal composite structure.

Two different processing sequences are analyzed. The first is called the "dry etch process," the second sequence is called the "photoimageable polymer process." The main difference between the two approaches is the method of polymer formation. The standard process uses a metal mask for dry etching of the polymer. The reduced steps process uses a photoimageable polymer to form the bumps.

Our analysis shows that compliant bumps can be fabricated at a cost that is competitive with conventional gold bumps, and that capital equipment cost is dominant at volumes below 10 k wafers/yr. For the analysis that follows, certain definitions are useful:

- **Dedicated equipment:** Equipment purchased for the production of a certain product. All capital depreciation cost for this equipment must be absorbed by that product, even if it uses the equipment for only a small fraction of the available line time. For example, suppose that a facility needs to do polymer coating on 4000 wafers/yr and that one coater can do all 4000 coatings. If production time for those 4000 wafers is 2 min/wafer, the coater will be used for only 2% of the working hours during the year. No other process will be run on the machine to pay for the cost of the coater. Manufacturing cost with dedicated equipment is highly dependent on manufacturing volume.
- **Non-dedicated equipment:** Equipment that is shared between product lines. Each product covers capital depreciation cost only for the portion of available line time that it uses the equipment. Using the example cited above, suppose that a machine is used for 2% of the working hours in a given year to produce polymer coatings for compliant bumps. Then only 2% of the cost of ownership for the equipment is charged to compliant bump formation. Manufacturing cost on nondedicated equipment is independent of manufacturing volume, as long as the equipment is fully used by a mix of product lines.
- **Labor:** Labor includes only direct labor (with benefits) used to run equipment. Labor rates were assumed to be \$30/h, representative of technician wages and benefits. These rates do not include maintenance, administration, or other overhead, which may account for as much as 60% of total production cost.
- **Materials:** Materials that are used to form the compliant bump, the ancillary materials used during production, and

TABLE I
COST BREAKDOWN FOR DEDICATED AND NONDEDICATED EQUIPMENT AT VARIOUS YIELDS AND PRODUCTION VOLUMES USING STANDARD PLASMA ETCH PROCESSING. COSTS ARE LISTED BY COST CENTER

Cost center	Dry Etch Process (\$/wafer)			
	Non-dedicated Equipment		Dedicated Equipment	
	100% yield	80% yield	100% yield	80% yield
3.5k wfr/yr				
Labor	\$30.03	\$37.54	\$30.03	\$37.54
Material	\$8.28	\$10.35	\$8.28	\$10.35
Equipmt.	\$23.49	\$29.37	\$208.00	\$208.00
Total	\$61.80	\$77.26	\$246.31	\$255.89
35k wfr/yr				
Labor	\$30.03	\$37.54	\$30.03	\$37.54
Material	\$8.28	\$10.35	\$8.28	\$10.35
Equipmt.	\$23.49	\$29.37	\$35.00	\$35.00
Total	\$61.80	\$77.26	\$73.00	\$83.00
100k wfr/yr				
Labor	\$30.03	\$37.54	\$30.03	\$37.54
Material	\$8.28	\$10.35	\$8.28	\$10.35
Equipmt.	\$23.49	\$29.37	\$27.32	\$31.43
Total	\$61.80	\$77.26	\$65.63	\$79.32

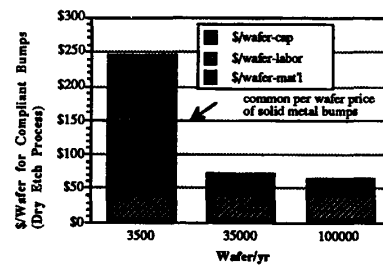


Fig. 11. The effect of volume on fabrication cost of compliant bumps when using plasma etch to form the polymer. Labor and material costs are not affected by volume, but capital is directly affected. This figure assumes dedicated equipment.

a waste disposal multiplier.

A. Cost for the "Dry Etch Process"

The most important cost factor in the dry etch process is throughput at the dry etch step. Etch rates of polymers are usually 1 $\mu\text{m}/\text{min}$. At that rate, wafer throughput is less than 10 wafers/h. Low throughput leads to high capital and labor cost at the etch step.

For the dry etch process, dedicated capital equipment costs are dominant at production volumes below 10 000 wafers/yr (see Fig. 11 and Table I). At production volumes of 100 000 wafers/yr, capital equipment and labor charges are roughly even at 40% to 45% of the total cost per wafer. Material cost is just over 10% of the total cost.

B. Cost for the "Photoimageable Polymer Process"

The process flow used for the analysis of the photoimageable polymer method allows for a more balanced production line. The lowest wafer throughput at any step is 15 wafers/h.

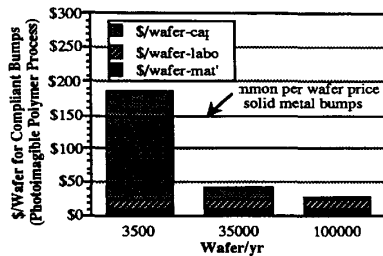


Fig. 12. The effect of volume on fabrication cost of compliant bumps when using photoimaging to form polymer bumps. Labor and material are not affected by volume, but capital is directly affected. This figure assumes dedicated equipment.

TABLE II
COST BREAKDOWN FOR DEDICATED AND NONDEDICATED EQUIPMENT
AT VARIOUS YIELDS AND PRODUCTION VOLUMES USING
PHOTOPOLYMER PROCESSING. COSTS ARE LISTED BY COST CENTER

Photo Polymer Process (\$/wafer)				
Cost center	Non-dedicated Equipment		Dedicated Equipment	
	100 % yield	80 % yield	100 % yield	80 % yield
3.5k wfr/yr				
Labor	\$10.95	\$13.69	\$10.95	\$13.69
Material	\$9.35	\$11.69	\$9.35	\$11.69
Equipmt.	\$3.88	\$4.85	\$160.20	\$160.20
Total	\$24.18	\$30.23	\$181.00	\$186.00
35k wfr/yr				
Labor	\$10.95	\$13.69	\$10.95	\$13.69
Material	\$9.35	\$11.69	\$9.35	\$11.69
Equipmt.	\$3.88	\$4.85	\$16.02	\$16.02
Total	\$24.18	\$30.23	\$36.32	\$41.40
100k wfr/yr				
Labor	\$10.95	\$13.69	\$10.95	\$13.69
Material	\$9.35	\$11.69	\$9.35	\$11.69
Equipmt.	\$3.88	\$4.85	\$5.01	\$5.50
Total	\$24.18	\$30.23	\$25.31	\$30.88

Production volumes can exceed 50 000 wafers/yr before any duplicate equipment needs to be purchased. The total number of process steps and associated capital equipment spending is much smaller than that used for the dry etch process. As a result, production cost for the photoimaging polymer method is approximately 50% less expensive than the dry etch process (see Fig. 12 and Table II).

VI. RELIABILITY

For reliability assessment, the MCC "FC216" test vehicle was used. This test vehicle "kit" includes the chip, substrate, and TAB tape designs. The chip measures 8.9 mm $\times$ 8.9 mm and has 216 I/O on 150- μ m pitch. 210 I/O are connected in a dual "nested" daisy chain pattern. This allows continuity checking of these connections with two resistance measurements, each reading through 105 connections. Adjacent bump electrical isolation is determined by measuring the resistance between the two daisy chains.

Six of the chip pads are used to connect a "triple-track" feature that can be used for surface insulation resistance

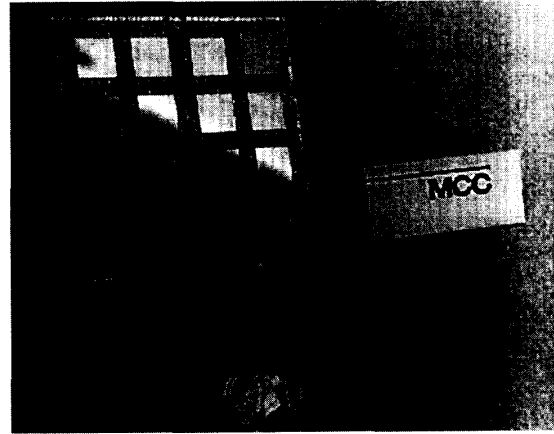


Fig. 13. The 16-chip test vehicle is the MCC "FC216". The test vehicle in the lower right is for true 4-wire contact resistance measurements of flip-chip connections.

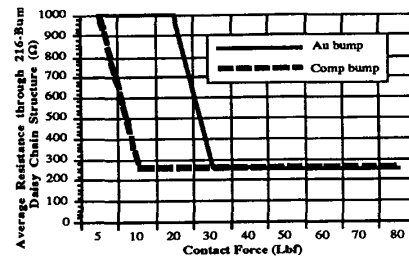


Fig. 14. Daisy chain resistance, measured as contact force, is increased for both solid gold-bumped chips and compliant bumped chips. The substrate in this test was borosilicate glass with very thin, sputtered chrome/gold metallization. Thus, about 250 Ω in each reading is due to bulk resistance of the substrate and chip metallization.

and electromigration tests. Triple tracks can also be used for thermal testing by biasing two of the tracks as heating elements (for a total of 25 W/chip) and using the center track for a thermistor. The substrate used for this project was display quality borosilicate glass, sputtered with chrome/gold, and patterned with the "FC216" substrate design, which complements the chip features.

True 4-wire contact resistance measurements are not possible with the "FC216" test vehicle. An approximation of compliant bump contact resistance is determined by comparing total daisy chain resistance for compliant bump assemblies to that of other "FC216" adhesive flip-chip technologies that have also been characterized in a separate, 4-wire-capable test vehicle (see Fig. 13).

Chips were first aligned and pressed to substrate sites without the introduction of adhesive in order to determine the minimum force application needed to establish contact at all pads. Force was increased until there was no further reduction in daisy chain resistance. The results are summarized in Fig. 14.

Mechanical cycling of the bumps was performed on the flip-chip bonder, using compression ranges from 20 to 70 lbf (equal to approximately 20 to 70 kpsi over the total bump area) for



Fig. 15. Compliant bump after 3000 mechanical cycles from 20 to 70 ksi loading. Significant elasticity range is lost, but the bump remains conductive and somewhat compliant.

1000 cycles. After this test, the elastic range of compression was reduced by 50% because of plastic deformation in the gold overcoat. There were no cracks observed in either the metallization or the polymer core. Bumps cycled 3000 times showed significant degradation of the metal overcoat (see Fig. 15). This mechanical cycling, however, was performed without adhesive. In a real assembly, adhesive would fully surround the bump, supporting the metal and reducing metal extrusion radially outward as was seen in our mechanical cycling tests.

Based on this data, a range of initial bonding force parameters was chosen, and chips assembled to glass using a commercially available UV-curing adhesive. Typical UV exposure times were 15–30 s. For the lower exposure times, a UV “post-bake” was performed to ensure total cure. As a control, assemblies were made with solid gold-bumped chips to identical substrate sites.

Compliant bump and gold bump FCOG assemblies were subjected to a high temperature operating test. Resistance through the daisy chains was monitored while assemblies were heated slowly to 140°C. All solid gold-bump assemblies failed between 65°C and 80°C. Compliant bump assemblies failed between 120°C and 135°C (well above the glass-transition temperature of the adhesive). All assemblies that lasted to 135°C were assembled using identical force parameters. All compliant bump assemblies returned to nominal resistance when cooled to room temperature. Open circuits in the solid gold bump assemblies remained when returned to room temperature.

Gold and compliant bump FCOG assemblies were subjected to 121°C, 100% relative humidity for 2 h. At the conclusion of this test, 50% of the gold-bump samples had failed and 12.5% of the compliant-bump samples had failed. Subsequently, compliant-bump assemblies were coated with a commercially available silicone encapsulant. These assemblies have survived 8 h of 121°C at 100% RH with no failures.

Rework was performed on several assemblies through the course of this testing. A simple fixture was made to immerse the chip to be removed in a solvent while protecting the adjacent chips from solvent exposure. Solvent soak was successful at room temperature, and can be accelerated by raising

the solvent temperature to 80°C. Both the substrate and chip emerge from this process intact and re-usable. Some of the chips and substrate sites included in the tests described above had been reworked twice.

Compliant bumped chips have also been assembled to FR4 and MCM-D substrates, using heat curing adhesives. Two adhesives have been used to-date. One provides commercial reliability levels and is easily reworkable. The other provides full MIL-STD-883 schedule D reliability, but is only reworkable in partially cured form. Flip-chip assemblies with this second adhesive can be subjected to solder assembly temperature profiles with no degradation of the adhesive flip-chip connections. This is important for applications where the flip-chip assembly must subsequently be solder-assembled to a motherboard. For example, a low profile Ball-Grid-Array package can be built using existing chip designs (compared to C4 or DCA technology, where the chip I/O pads must be no less than 250- μ m pitch, which usually dictates an array format).

VII. CONCLUSION

Compliant bump technology has been demonstrated using a polymer core bump with a thin metal overcoat. The compliant-bump process approach solves many of the problems associated with adhesive flip-chip assemblies made with solid metal bumps or small conductive particles. Polymer bump formation and metallization can be done in several different ways. All approaches use equipment that is commonly purchased for TAB bumping.

Compliant bumps solve the problem of Z-axis movement that is associated with UV or heat curing adhesives (due to mismatched CTE and moisture absorption) by elastically rebounding to maintain electrical contact. The compliant bumps also promise to reduce the detrimental effects of bowed and twisted substrates and irregular pad heights. The bumps can be manufactured with standard TAB bumping processes and equipment at a cost comparable to that of solid metal bumps.

Preliminary reliability testing has shown compliant-bump flip-chip assemblies to be more reliable than identical assemblies using solid-gold bumped chips. Further reliability testing is underway. Additionally, compliant bumps can be reworked either at room temperature or at slightly elevated temperature.

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