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Paper No. ____

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY GROUP CORPORATION
Petitioner,

v.

VISIONX TECHNOLOGIES, LLC,
Patent Owner.

Case No. IPR2023-00296
Patent No. 7,867,808

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1 *et seq.***

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REGULATIONS

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37 C.F.R. § 42.100(b)	8
37 C.F.R. § 42.104(a)	1
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EXHIBIT LIST

Exhibit	Description
1001	U.S. Patent No. 7,867,808
1002	Prosecution History of U.S. Patent No. 7,867,808
1003	Declaration of Dr. L. Richard Carley
1004	Curriculum Vitae of Dr. L. Richard Carley
1005	U.S. Patent Application Pub. No. US 2006/0197007 A1 (“Iwabuchi”)
1006	Japanese Patent Application Pub. No. JP 2006-93587 A (“Maruyama”)
1007	Exhibit A to Declaration of Gordon Macpherson, T. Suga et al., “Surface activated bonding for new flip-chip and bumpless interconnect systems.” <i>52nd Electronic Components and Technology Conference</i> 2002, pp. 105-111, 2002 (“Suga”)
1008	PCT Application Pub. No. WO 2006/109937 A1 (“Lee”)
1009	Japanese Patent Application Publication No. JP 2006-303385 A (“Masagaki”)
1010	Japanese Patent Application Publication No. JP 2005-353996 (“Shiraiwa”)
1011	G. C. Bethea et al., “Long wavelength infrared 128×128 Al _x Ga _{1-x} As/GaAs quantum well infrared camera and imaging system,” <i>IEEE Transactions on Electron Devices</i> , vol. 40, no. 11, pp. 1957-1963, Nov. 1993 (“Bethea”)
1012	V. Dragoi and P. Lindner, “Plasma Activated Wafer Bonding of Silicon: In Situ and Ex Situ Processes.” <i>ECS Transactions</i> , vol. 3, no. 6, pp. 147-154, 2006 (“Dragoi”)
1013	Pages from S.M. Sze and Kwok K. Ng, <i>Physics of Semiconductor Devices</i> , John Wiley & Sons (3d ed. 2007) (“Sze”)
1014	A. Rogalski, “Infrared Detectors: Status and Trends.” <i>Progress in Quantum Electronics</i> , vol. 27, pp. 59-210, 2003 (“Rogalski”)
1015	U.S. Patent Application Pub. No. 2006/0043519 A1 (“Ezaki”)
1016	U.S. Patent Application Pub. No. 2003/0025160 A1 (“Suzuki”)

Exhibit	Description
1017	Exhibit A1 to VisionX Infringement Contentions in <i>VisionX Technologies, LLC v. Sony Group Corp. et al.</i> , No. 2:22-cv-00178 (E.D. Tex.), served September 8, 2022 (“IC-A1”)
1018	U.S. Patent No. 6,074,895 (“Dery”)
1019	K. W. Oh and C. H. Ahn, “Flip-chip packaging with micromachined conductive polymer bumps.” <i>Proceedings of 3rd International Conference on Adhesive Joining and Coating Technology in Electronics Manufacturing</i> 1998 (Cat. No.98EX180), pp. 224-228, 1998 (“Oh”)
1020	R. Balcerak and S. Horn, “Progress in the development of vertically integrated sensor arrays,” <i>Proc. SPIE</i> 5783, Infrared Technology and Applications XXXI, pp. 384-390, 2005 (“Balcerak”)
1021	B. Pain et al., “A Back-Illuminated Megapixel CMOS Image Sensor,” in <i>Proceedings IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors</i> , pp. 35-38, 2005 (“Pain2005”)
1022	U.S. Patent No. 6,762,473 B1 (“Gouscha”)
1023	Pages from <i>The Penguin Complete English Dictionary</i> (2006)
1024	U.S. District Court – Judicial Caseload Profile for the Eastern District of Texas, <i>available at</i> https://www.uscourts.gov/sites/default/files/fcms_na_distprofile0630.2022_0.pdf , p.35 (last visited September 30, 2022).
1025	U.S. Patent No. 5,903,021 (“Guidash”)
1026	Pages from <i>Wiley Electrical and Electronics Engineering Dictionary</i> , John Wiley & Sons, Inc. (2004)
1027	R.S. Patti, “Three-Dimensional Integrated Circuits and the Future of the System-on-Chip Designs.” <i>Proceedings of the IEEE</i> , vol. 94, no. 6, pp. 1214-1224, 2006 (“Patti”)
1028	U.S. Patent Pub. 2003/0038336 (“Mann”)
1029	U.S. Patent Application Publication No. US 2005/0161795 A1 (“Tong”)
1030	U.S. Patent No. 7,750,488 (“Patti488”)
1031	U.S. Patent Application Publication No. US 2006/0043438 A1 (“Holm”)
1032	PCT Application Pub. No. WO 2006/129762 A1 (“Iwabuchi-762”)

Exhibit	Description
1033	Pages from C.Y. Chang and S.M. Sze, <i>ULSI Technology</i> . The McGraw-Hill Companies, Inc., 1996. (“ULSI”)
1034	Pages from <i>The American Heritage Dictionary of the English Language</i> , Houghton Mifflin Company (4th ed. 2000).
1035	IPC-7351: Generic Requirements for Surface Mount Design and Land Pattern Standard (2005)
1036	INTERPOSER-TECH07: Lead-free to Tin/Lead BGA Interposer (Advanced Interconnections 2007)
1037	Pages from S.M. Sze, <i>Physics of Semiconductor Devices</i> (2d ed. 1981) (“Sze-1981”)
1038	Affidavit of Nathaniel E. Frank-White (“Frank-White Affidavit”)
1039	RESERVED
1040	A. El Gamal and H. Eltoukhy, H., “CMOS image sensors,” <i>IEEE Circuits and Devices Magazine</i> , 21(3), pp.6-20 (2005) (“Gamal”).
1041	Declaration of Gordon Macpherson with Exhibit A, R.S. Patti, “Three-Dimensional Integrated Circuits and the Future of the System-on-Chip Designs.” <i>Proceedings of the IEEE</i> , vol. 94, no. 6, pp. 1214-1224, 2006
1042	S. Tiwari et al., “Lateral p-i-n photodetectors with 18 GHz bandwidth at 1.3 μm wavelength and small bias voltages,” <i>International Electron Devices Meeting 1991</i> [Technical Digest], 1991, pp. 421-424 (“Tiwari”)
1043	U.S. Patent No. 6,984,816 B2 (“Holm-816”)
1044	Pages from S.M. Sze, <i>Semiconductor Devices: Physics and Technology</i> , John M. Wiley & Sons (2d ed. 2002) (“Sze-2002”).
1045	Mike Salib et. al, “Silicon Photonics,” <i>Intel Technology Journal</i> , volume 8, no. 2, pp. 143-160, 2004 (“Salib”)
1046	P. Lindner et al., “3D Interconnect Through Aligned Wafer Level Bonding,” in <i>52nd Electronic Components and Technology Conference 2002</i> (Cat. No. 02CH37345), pp. 1439-1443 (May 28, 2002) (“Lindner”)
1047	K. Keswick, R. L. German, M. Breen and R. Nolan, “Compliant bumps for adhesive flip-chip assembly,” <i>IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B</i> , vol. 18, no. 3, pp. 503-510, Aug. 1995 (“Keswick”)

Exhibit	Description
1048	J. H. Wu et al., “A high aspect-ratio silicon substrate-via technology and applications: through-wafer interconnects for power and ground and Faraday cages for SOC isolation,” <i>International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138)</i> , 2000, pp. 477-480 (“Wu”)

MANDATORY NOTICES

A. Real Party-In-Interest – § 42.8(b)(1)

Petitioner Sony Group Corporation (“Sony”) is a real-party-in-interest. In an abundance of caution, Petitioner states that other Sony affiliates could be real parties-in-interest. In particular, Petitioner identifies Sony Corporation, Sony Semiconductor Manufacturing Corporation, Sony Semiconductor Solutions Corporation, Sony Corporation of America, and Sony Electronics Inc. as additional real parties-in-interest.

B. Related Matters – § 42.8(b)(2)

A decision in this proceeding could affect, or be affected by, *VisionX Technologies, LLC v. Sony Group Corporation et al.*, 2:22-cv-00178 (E.D. Tex.) (“the Litigation”), in which VisionX asserts U.S. Patent No. 7,867,808.

C. Counsel and Service Information – § 42.8(b)(3) and (b)(4)

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A power of attorney is submitted with the Petition. Counsel for Petitioner consents to service of all documents via electronic mail.

Sony requests *inter partes* review (“IPR”) of claims 1-2 & 4-9 (the “challenged claims”) of U.S. Patent No. 7,867,808 (“the ’808 patent”) (Ex. 1001).

I. INTRODUCTION

The ’808 patent concerns manufacturing a “vertical type photodiode” for a semiconductor image sensor. The method forms a photodiode in one substrate and metal interconnections over another, and bonds the substrates together. The photodiode includes ion-implanted “isolation layers” providing “pixel-to-pixel isolation” in the sensor.

Every aspect of the ’808 patent—including the ion-implanted isolation layers—was known long before its 2007 priority date. Sony itself filed patent applications on CMOS imagers using these ideas—*e.g.*, separating imager fabrication from processing circuit fabrication, forming ion-implanted pixel isolation layers, and substrate bonding—before 2007. One such application, Iwabuchi, underlies Grounds 1A-1C. Another prior art reference, Lee, also describes separately forming sensors and support circuitry in different substrates and bonding them together. Lee underlies Grounds 2A-2C.

II. STANDING CERTIFICATION

The ’808 patent is available for IPR. Petitioner is neither barred nor estopped from requesting IPR of its claims. 37 C.F.R. § 42.104(a).

III. UNPATENTABILITY GROUNDS

Petitioner requests cancellation of claims 1-2 and 4-9. Pre-AIA law applies because the '808 patent was filed before March 16, 2013.

Ground	Reference	Claim(s)	Basis
1A	Iwabuchi	1, 4-6, 8-9	§ 103
1B	Iwabuchi+Maruyama	2	
1C	Iwabuchi+Suga	7	
2A	Lee+Masagaki+Shiraiwa	1, 4-6, 8-9	
2B	Lee+Masagaki+Shiraiwa+Maruyama	2	
2C	Lee+Masagaki+Shiraiwa+Tong	7	

IV. '808 PATENT

The '808 patent was filed December 28, 2008, claiming priority to a Korean application filed December 28, 2007. 1:4-6.¹ There are nine method claims. Claim 1 is independent. A claim list is appended.

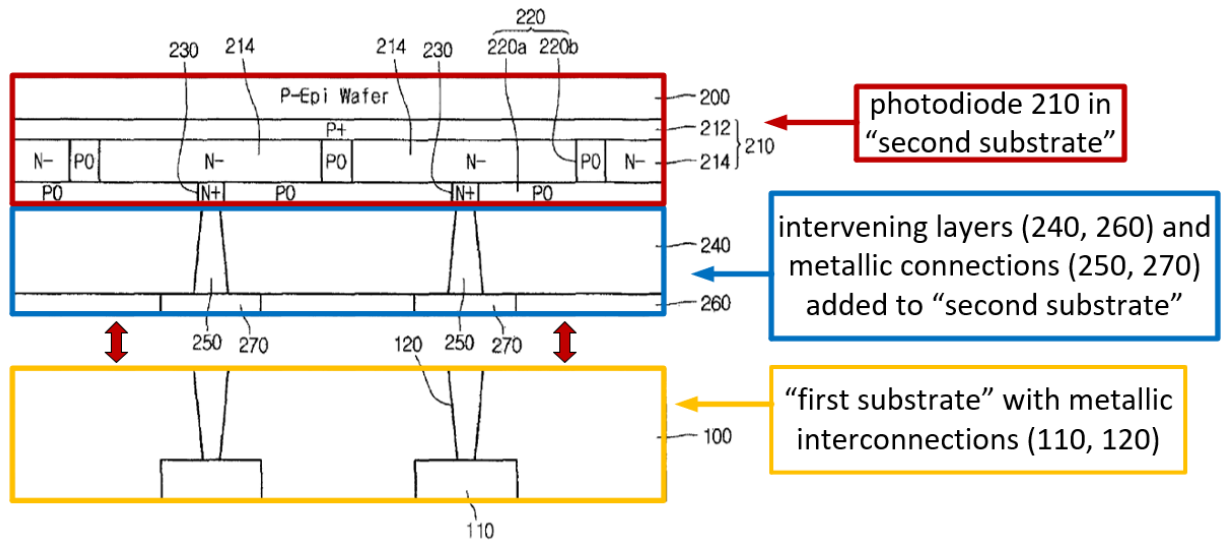
A. Embodiments

The '808 patent describes manufacturing an image sensor by forming a semiconductor photodiode in *a “second” substrate* and electrically connecting the photodiode to metallic interconnections formed on a *different “first” substrate*. 1:47-49, 2:25-33, 3:3-10, Figs. 7, 8.

¹ Unless otherwise noted, Section IV citations refer to Ex. 1001.

After bonding the “first” and “second” substrates (red arrows below), the “vertical” integration provides a continuous conductive path from photodiode 210 to metallic interconnections 110, 120 on the “first” substrate.

FIG. 7



This approach responded to purported problems in prior art CMOS image sensors having photodiodes and transistors “horizontally arranged,” with transistors consuming area that could otherwise be devoted to light detection, fabricated using processes optimized for forming CMOS transistors but not photodiodes. 1:16-43. The ’808 patent allegedly solved these problems by forming a photodiode in a substrate without transistors. 2:38-41, Figs. 2-8; Ex. 1003 (“Carley”), ¶¶56-57.

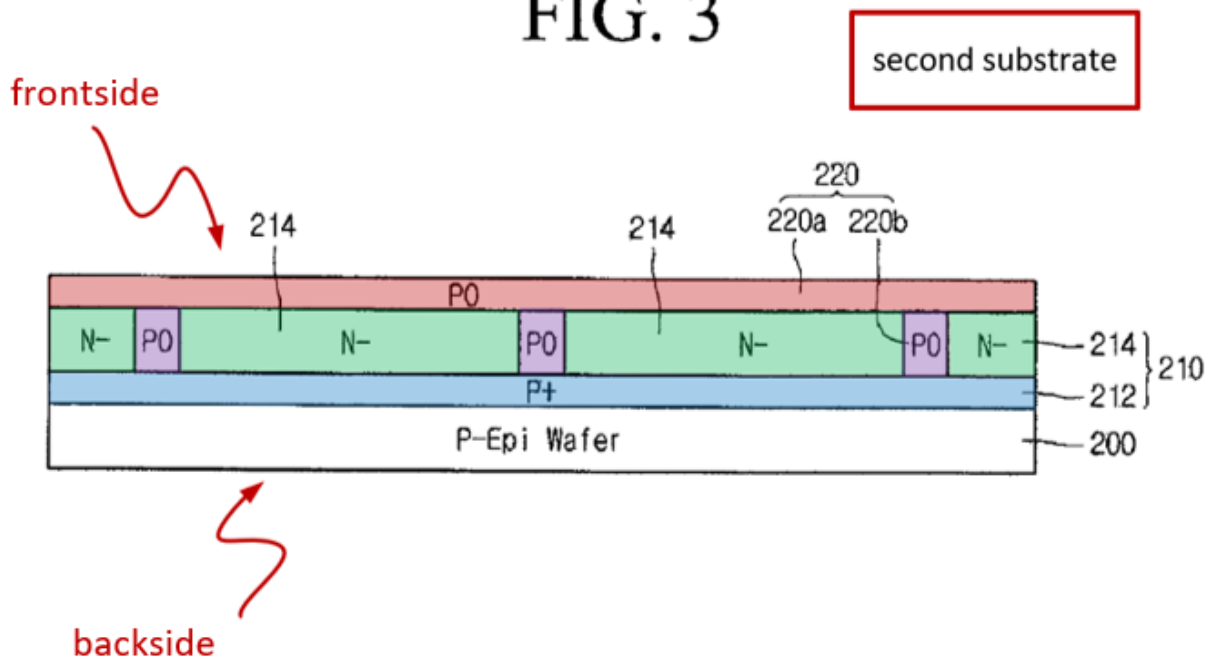
Separating photodiode fabrication from integrated electronics fabrication by putting a photodiode in its own substrate (1:66-2:2, Fig. 2) provided the full light-incident surface for photodetection, and processes forming the sensor layer could be optimized for photodiode fabrication. Carley, ¶58. These advantages were well-known in the art. Carley, ¶¶59-65.

Bonding the substrates connected a metal interconnection on the first substrate (metal 110 and plug 120) to a photodiode (at N- conduction layer 214) with a conductive path through “metal pad” 270, tungsten plug 250, and N+ conductive layer 230. 2:25-32, 4:1-35, Figs. 7, 8. The patent’s “vertical type photodiode” has no transistors in the sensor substrate. *Id.*; Carley, ¶66.

B. Challenged Claims

Claim 1 recites forming metal interconnections on a first substrate, forming a photodiode in a second substrate, and bonding the two together. Removing material from the second substrate’s backside exposes the photodiode. This provides a backside-illuminated (“BSI”) photodiode—meaning that when used light strikes the substrate’s “backside” including the photodiode (*e.g.*, Fig. 3 (bottom) or Fig. 8 (top)—with second substrate flipped relative to the Fig. 3 orientation). Carley, ¶¶67-68.

FIG. 3



The patent identifies the surface defined by “removing the lower portion of the second substrate” as the “backside.” 4:47-50 (“P-Epitaxial layer...may be removed by performing a cleaving or backside thinning process[.]”); Carley, ¶69. **Before** thinning, the second substrate “backside”—depicted above—is the lower surface of the “P-Epi Wafer” 200 in Fig. 3, while **after** thinning, the “backside” is the remaining second substrate surface opposite layer 220a. Carley, ¶70. The “frontside” opposes the “backside” (see annotated Fig. 3). Carley, ¶71. The frontside conventionally meant the surface where masks were placed to define features for fabrication process steps or—as the patent describes for layer 212—through which maskless “blanket” ion implantation was done. 3:19-30; *Id.* For example, ’808 patent Figures 2-6 depict the second substrate “frontside” on top because the patent describes working on that surface and adding layers. *Id.* A

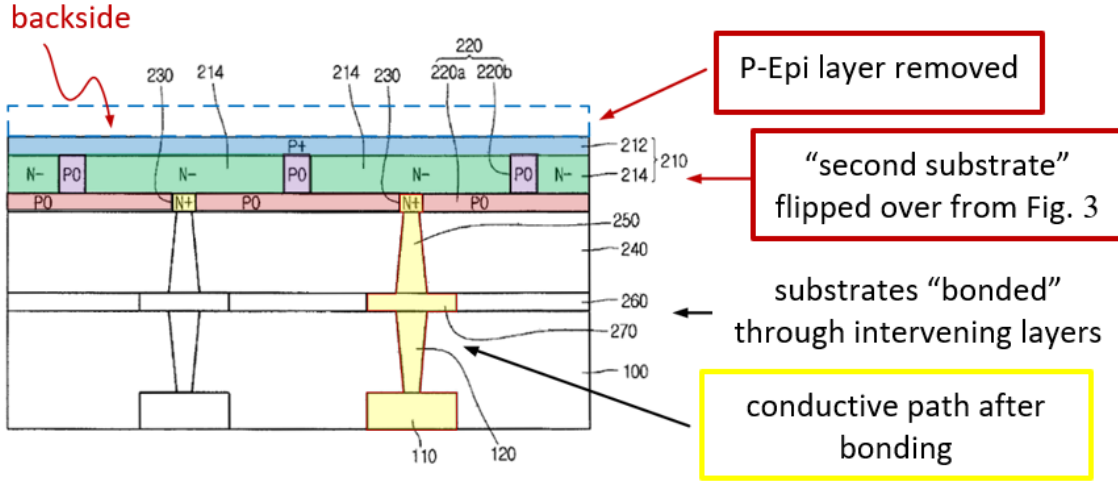
backside layer (*e.g.*, '808 patent, Fig. 3 “P-Epi” layer 200) was conventionally a thick layer for mounting or handling the substrate while working on the frontside. Carley, ¶72.

Claim 1 requires forming a photodiode comprising four layers in the “second substrate.” The photodiode is formed in a crystalline semiconductor layer (step [1.c]) with two conduction layers having opposing n and p doping types. Steps [1.g], [1.g.1], [1.g.2], 3:19-61, Figs. 2-3; Carley, ¶73. The “first” type conduction layer (step [1.g.2], **green N- layer 214**) must be formed “over” the “second” type conduction layer (step [1.g.1], **blue P+ layer 212**), so that step [1.g.1] must be performed before step [1.g.2]. Carley, ¶74.

Claim 1 also requires forming two “isolation layers”—steps [1.h.1] (**red layer 220a**) and [1.h.2] (**purple regions 220b**)—by ion implantation. Steps [1.d], [1.h.1], [1.h.2], 3:44-4:4, Figs. 2-4. The “second” “isolation layer” (step [1.h.2], **220b**) is “at an interface between pixels” and defines the lateral boundaries of each pixel (*e.g.*, each light-collecting region). 2:44-47, 4:2-4; Carley, ¶¶75-76.

Figures 7-8 flip the second substrate (with photodiode), from the “backside-down” orientation in Figures 2-6, to a “backside-up” orientation that illustrates bonding the two substrates (step [1.e]) and thinning the second substrate (step [1.f]).

FIG. 8



Dependent claims add minor variations concerning junction depth, doping levels, isolation layer placement, bonding, and interconnects.

C. Prosecution History

A single action rejected all claims as obvious. Ex. 1002, 137-139. The applicant amended the independent claim (application-claim 10, which issued as challenged claim 1) to incorporate application-claims 11 (steps [1.g.1], [1.g.2]), 14 (step [1.h.1]), and 15 (step [1.h.2]), and distinguished prior art based on the “isolation layer” ([1.h.1] and [1.h.2]). *Id.*, 147-148, 150-152. The Examiner allowed the claims without explanation. *Id.*, 157.

D. Level of Ordinary Skill in the Art

A person of ordinary skill in the art (“POSA”) would have had a Bachelor’s degree in electrical engineering, physics, or materials science and at least 4 years of industry or research experience in solid-state imager design and fabrication.

Carley, ¶48. To design an image sensor, a POSA would have had to understand the imager device structure, how that structure could be fabricated, design limitations imposed by fabrication techniques, circuit design supporting pixel operation, and the overall readout control architecture that forms an image. *Id.* Alternatively, a POSA would have had a Master’s degree in one of the foregoing fields and at least 2 years of experience as described. *Id.*

V. CLAIM INTERPRETATION

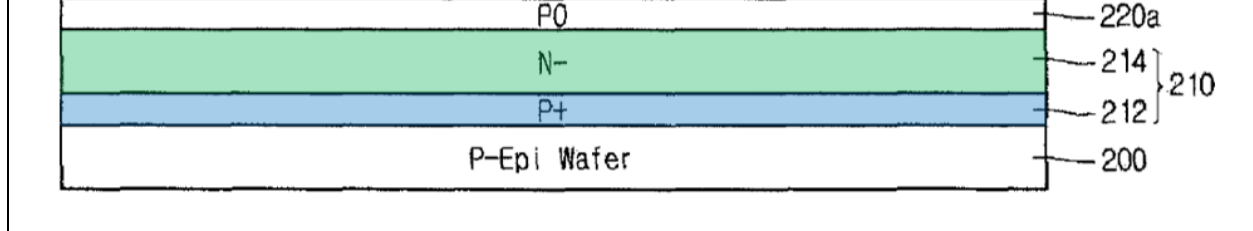
Claim construction follows the civil standard under 35 U.S.C. § 282(b), using “the ordinary and customary meaning” understood by POSAs with context from the intrinsic record. 37 C.F.R. § 42.100(b). The Board need only interpret terms to resolve disputes between the parties. *Nidec v. Zhongshan*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); 83 Fed. Reg. 51,340, 51,353.

Claim 1’s plain language requires performing step [1.g.1] before [1.g.2].²

1.g.1	forming a second conduction type conduction layer in the crystalline semiconductor layer; and
1.g.2	forming a first conduction type conduction layer over the second conduction type conduction layer ,

² Unless otherwise noted, emphasis is added throughout the petition.

FIG. 2



A claim's logic or grammar can require performing steps in the order written. *Loral Fairchild v. Sony*, 181 F.3d 1313, 1321 (Fed. Cir. 1999); *Medtronic v. Teleflex Innovations*, IPR2020-01341, Paper 93, 20-21 (Feb. 7, 2022).

By logic and grammar the second conduction layer formed in step [1.g.1] ***must already be in place*** in order to form the first conduction layer “***over***” it in step [1.g.2]. *Loral*, 181 F.3d at 1321 (“By the literal [claim] language...the implantation barrier regions [edges] are aligned with...the insulation layer [edges]; hence, the insulation layer ***must already be in place*** in order to align the barrier regions with it during ion implantation.”).

In *TALtech v. Esquel Apparel*, the Federal Circuit required “placing a bonding element” ***before*** “folding a portion...such that a lower surface...***abuts*** the...bonding element” because “the bonding element ***must already be in place***” before a portion could be folded to “abut” it. 279 F. App’x. 974, 978 (Fed. Cir. 2008). Here the [1.g.1] “second” conduction layer likewise “***must already be in place***” ***before*** the [1.g.2] “first” conduction layer can be formed ***over*** it.

The lone embodiment confirms this sequence, forming the [1.g.1] conduction layer **before** forming the [1.g.2] conduction layer. Ex. 1001, 3:21-43 (describing forming “second conduction type conduction layer 212” [1.g.1] **before** “first conduction type conduction layer 214” [1.g.2], asserting layer 214 “may be formed **on and/or over**” layer 212); *Loral*, 181 F.3d at 1321; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005) (en banc) (specification is “single best guide to the meaning of a disputed term”).

All other terms should be given their ordinary meaning or (where indicated) the construction Patent Owner (“PO”) advocates through infringement contentions. *10X Genomics v. Bio-Rad Labs.*, IPR2020-00086, Paper 8, 17-19 (April 27, 2020) (claim constructions based on patent owner’s infringement contentions comply with 37 C.F.R. § 42.104(b)(3)).

VI. GROUND 1A: IWABUCHI RENDERS OBVIOUS CLAIMS 1, 4-6, 8-9

A. Iwabuchi

U.S. Patent Publication 2006/0197007 (Ex. 1005, “Iwabuchi”), published September 7, 2006, is pre-AIA § 102(b) prior art. Iwabuchi describes manufacturing a CMOS image sensor with backside-illuminated photodetectors. Iwabuchi separates the image sensor and signal processing circuitry into different chips. Iwabuchi, [0003], [0017], [0124]-[0125]. Iwabuchi replicates a unit cell photodetector, or pixel, in a planar array on the sensor chip. *Id.*, [0094]. A

“peripheral circuit unit” including a “signal processing circuit” on the signal processing (“DSP”) chip processes the image. *Id.*, [0020], [0023], [0117].

Iwabuchi describes integrating sensor and signal processing chips through an interposer or by direct bonding. *Id.*, [0124]-[0125], [0140], [0153]. One embodiment provides each pixel its own interconnection for signal output. *Id.*, [0192]. Iwabuchi allows “the pixel size [to] become very small in accordance with increase of integration degree of pixel without lowering a saturation electric charge amount and sensitivity.” *Id.*, [0194].

B. Claim analysis

1. Claim 1

a. Preamble

Iwabuchi describes methods for manufacturing an imager. Iwabuchi, [0021], claims 5-20. Carley, ¶84.

b. Step 1.a

1.a	providing a first substrate;
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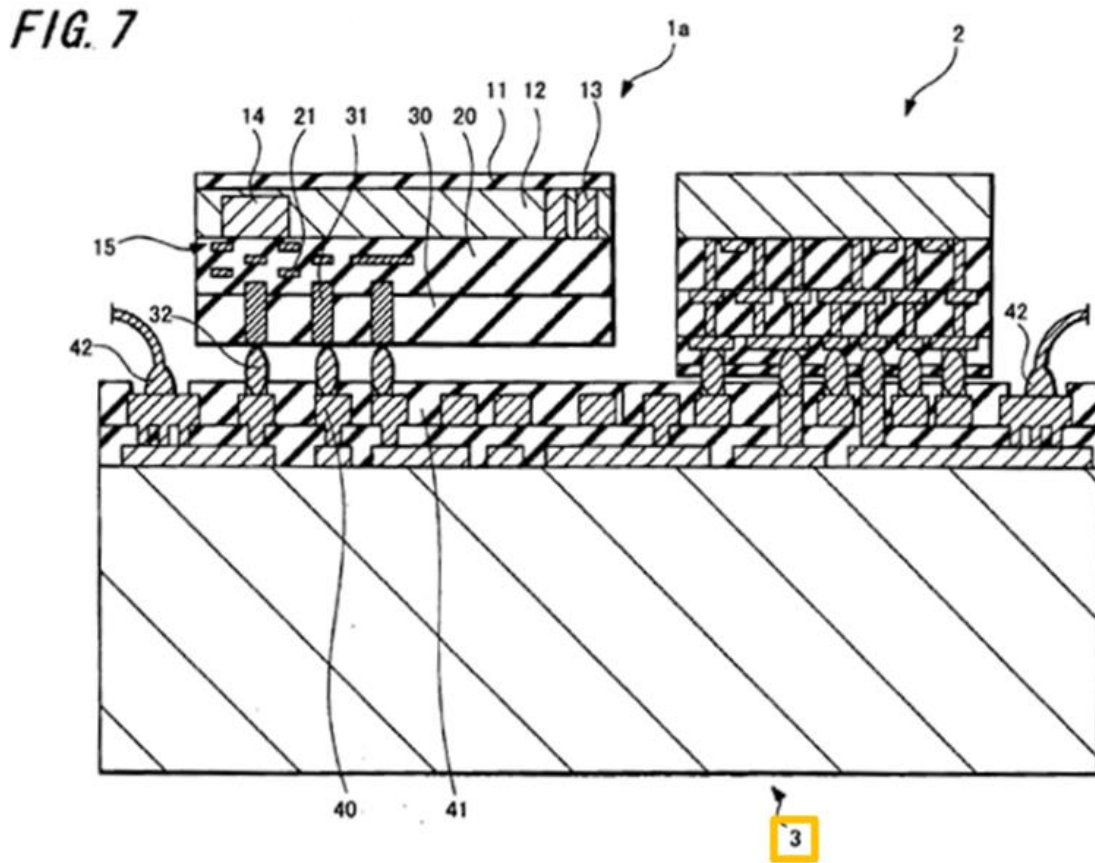
Iwabuchi meets [1.a] at least three ways.

i. interposer

Iwabuchi describes providing an “interposer (intermediate substrate) 3.” Iwabuchi, [0117]. Iwabuchi describes mounting sensor chip 1a and DSP chip 2 on

it. Iwabuchi, [0020]-[0021], [0117], [0124]-[0125], [0162], Fig. 7; Carley, ¶¶90.

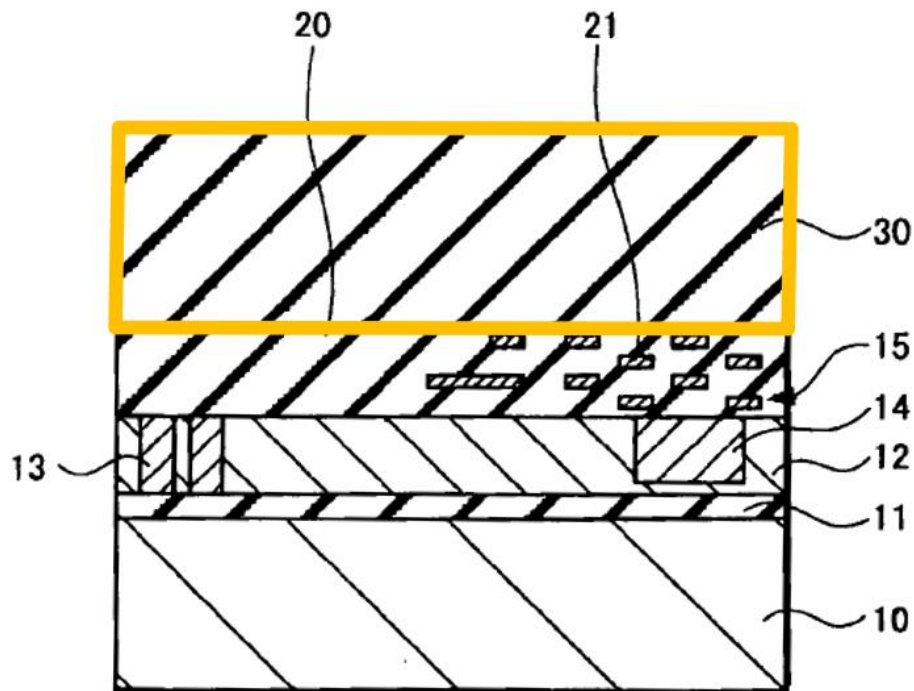
The interposer is a “first substrate.” Carley, ¶¶86-90.



ii. supporting substrate

Iwabuchi describes providing “supporting substrate 30 in order to stabilize the shape” of semiconductor layer 12. Iwabuchi, [0122]; *id.*, [0079], [0118], [0121], [0146], Fig. 10C; Carley, ¶¶91-94. The “supporting substrate 30” is a “first substrate.” Carley, ¶¶95.

FIG. 10C



iii. DSP substrate

“[T]he sensor chip can be directly mounted on the signal processing chip as a module.” Iwabuchi, [0153]. The DSP chip has “a peripheral circuit unit such as a signal processing circuit provided thereon[.]” *Id.*, [0117]; *see also id.*, [0130], [0020]. POSAs would have understood that “chip” referred to a substrate on which the “peripheral circuit unit” was formed. Carley, ¶¶96-97. The DSP chip would conventionally have been implemented as solid-state circuits formed on a substrate. Carley, ¶98. The DSP chip substrate is a “first substrate.” Carley, ¶99.

c. Step 1.b

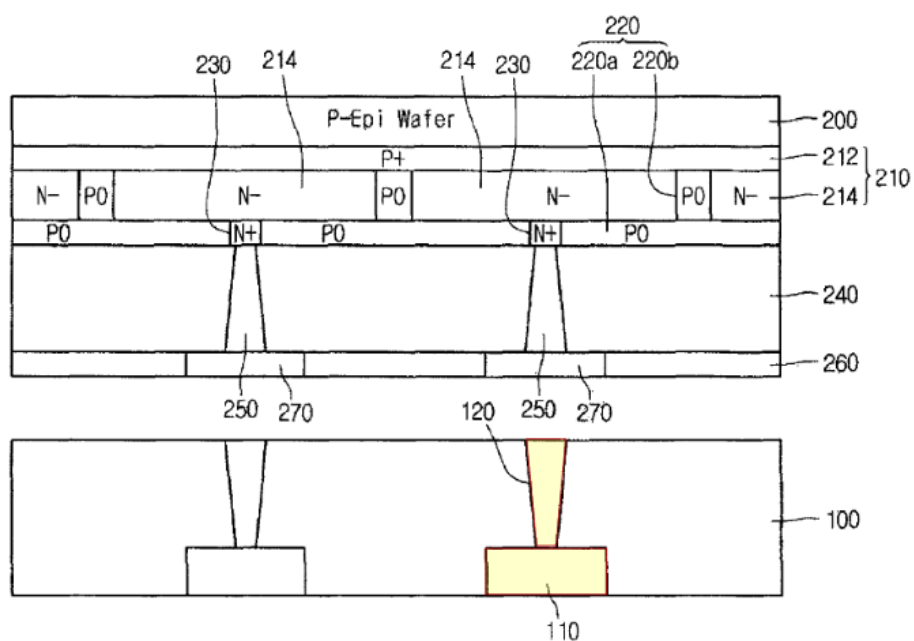
1.b	forming circuitry including a metal interconnection over the first substrate;
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Claim 8, depending from claim 1, recites “The method of claim 1, wherein forming the circuitry including the metal interconnection comprises forming a metal and a plug over the first substrate.” Subject matter that satisfies claim 8 necessarily meets step [1.b]. *Alcon Research v. Apotex*, 687 F.3d 1362, 1367 (Fed. Cir. 2012). Thus, a metal and a plug meet [1.b]’s “circuitry including a metal interconnection.” Indeed, the specification never identifies circuit components beyond conductive elements such as metal 110 and plug 120 with first substrate 100. Ex. 1001, 4:25-30, Fig. 7; Carley, ¶100. PO’s contentions likewise map [1.b]’s “circuitry” to “metal pads and plugs.” IC-A1³, 12; Carley, ¶101.

The specification does not define “plug.” It states, “[a] metal interconnection of first substrate 100 may include metal 110 and plug 120.” Ex. 1001, 4:29-30, Fig. 7.

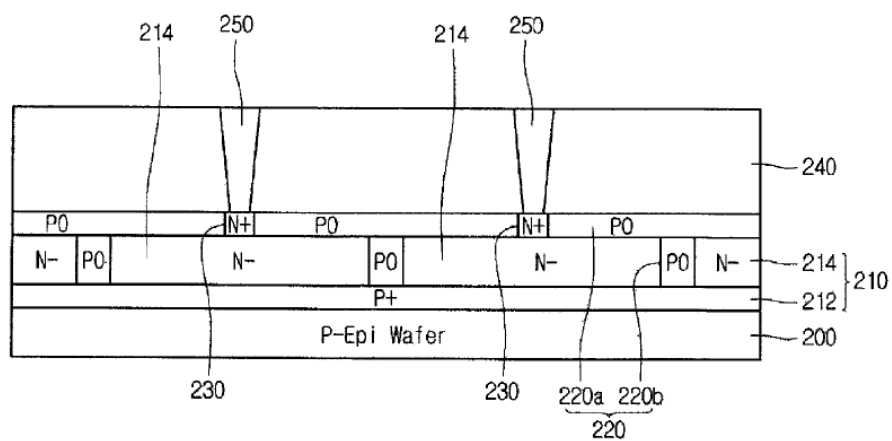
³ For exhibit short cites, see Exhibit List, pp. v-vii.

FIG. 7



The specification refers to “metal plug 250” formed from tungsten in a “first dielectric 240.” *Id.*, 4:8-14, Fig. 5.

FIG. 5

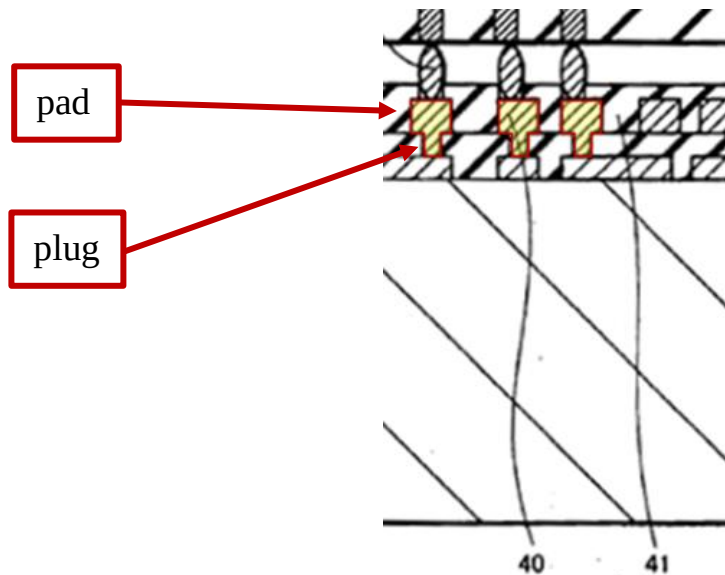


The '808 patent's "plug 250" and "plug 120" correspond to vias, which connect **through** a material. *Id.*, Figs. 5, 7; Carley, ¶101. PO's contentions likewise map "plug" to a feature labelled "ISP DBI via." IC-A1, 34-35.

Iwabuchi meets step [1.b] in at least three ways, corresponding to the three "first substrates" identified below. Carley, ¶102. The "metal and a plug" in each instance comprises an "interconnection" because each provides a signal path between a photodiode and signal processing circuits. Each alternative meets the "metal and plug" of claim 8, which in turn necessarily also meets [1.b]. Iwabuchi, [0140], [0154], [0189], [0192]; Carley, ¶102.

i. interposer

Iwabuchi describes forming wirings 40 over interposer 3. Iwabuchi, [0124], Fig. 7. Wiring 40 forms a pad. *Id.* The stem below the pad is a plug. *Id.*, Fig. 7; Carley, ¶103.

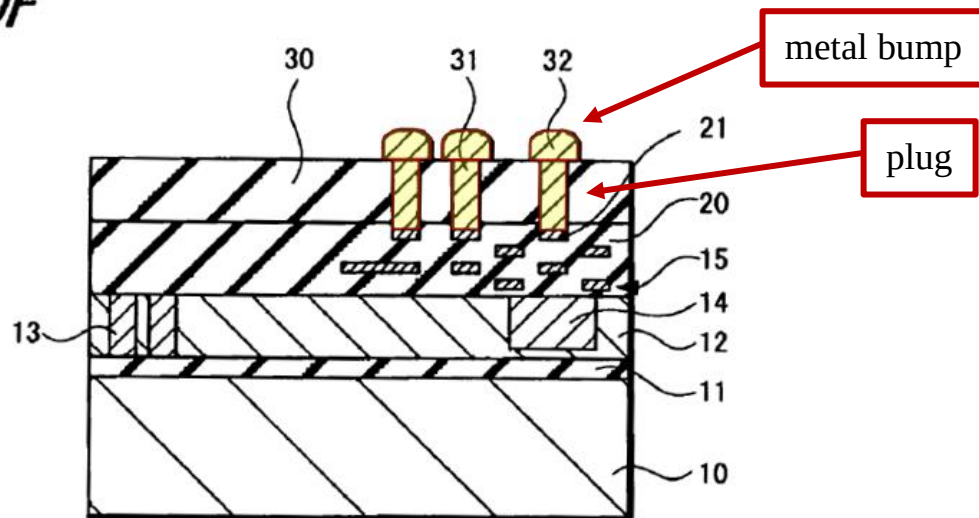


The pad compression-bonds with bump 32. *Id.*, [0153], Fig. 7. Bump 32 comprises metal. *Id.*, [0120], [0149]. Figure 7 shows forming wiring 40, the plug, and bump 32 from the same material class because they have the same cross-hatching. *Id.*, Fig. 7; 37 C.F.R. § 1.84(ii)(3) (“The various parts of a cross section of the same item should be hatched in the same manner and should accurately and graphically indicate the nature of the material(s)....Different types of hatching should have different conventional meanings as regards the nature of a material seen in cross section.”); Carley, ¶104. POSAs would also have formed wiring 40 from metal because flip-chip compression bonding conventionally used metal plating to receive bumps. *Id.*, ¶105; Tong, [0050] (“metal bonding pads”); Dery, 4:16-24 (“solder plating” on “contacts 126”), Figs. 1D-1E; *cf.* Ex. 1001, 4:29-30, Fig. 7. It was also conventional to form vias from metal. Carley, ¶¶105-107.

ii. supporting substrate

Iwabuchi describes forming “protrusion-like **metal** electrode” bumps 32 (Iwabuchi, [0120]), on copper substrate penetrating wires 31 (*id.*, [0148]-[0149]), over supporting substrate 30 (*id.*, Fig. 10F). Carley, ¶108. Iwabuchi describes forming “substrate penetrating wiring 31” by dry-etching substrate 30 and filling the opening with “low-resistance metal such as copper.” Iwabuchi, [0148]; Carley, ¶109. Wiring 31 is a “plug” like “plug 250” in the ’808 patent and the “ISP DBI via” in the contentions. Carley, ¶110; Ex. 1001, 4:8-14, Figs. 5, 7; IC-A1, 34-35.

FIG. 10F



iii. DSP substrate

Iwabuchi's "sensor chip can be directly mounted on the signal processing chip" with the same flip-chip bonding described for mounting the sensor on the interposer. Iwabuchi, [0153]. It was well-known to flip-chip bond die together with metal lands on one die receiving bumps on another die. Rogalski, 82-83, Fig. 14 (below); Balcerak, Fig. 1; Iwabuchi-762, Figs. 1, 26B, 31A (below); Carley, ¶111.

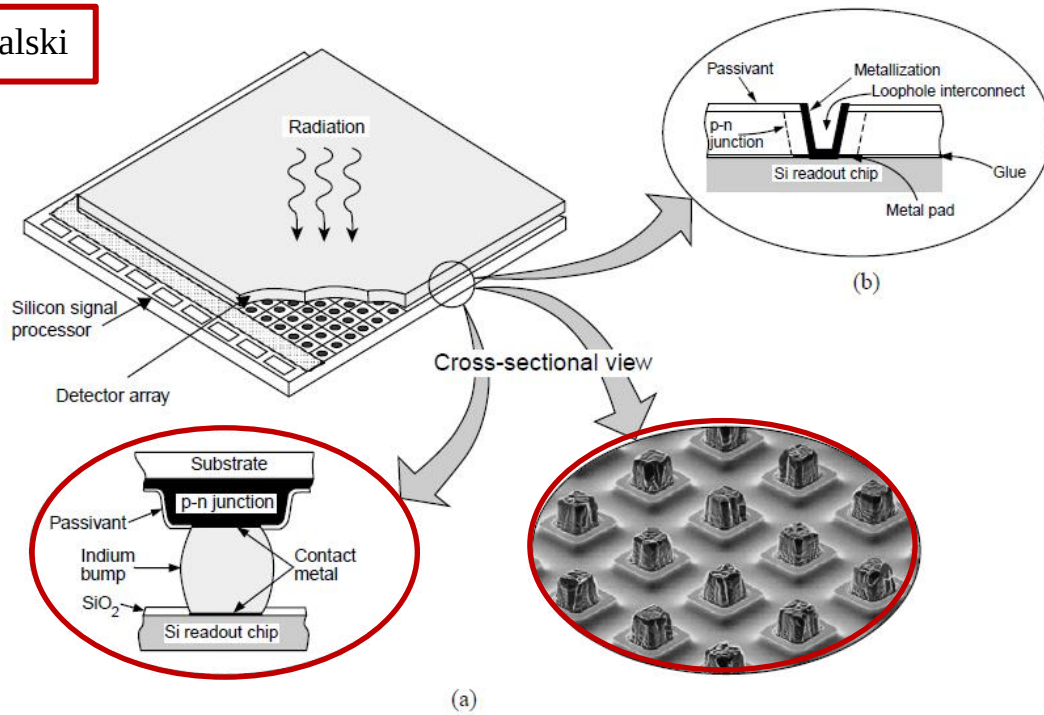


Fig. 14. Hybrid IR FPA with independently optimised signal detection and readout: (a) indium bump technique, (b) loophole technique.

FIG. 1

51

Iwabuchi-762

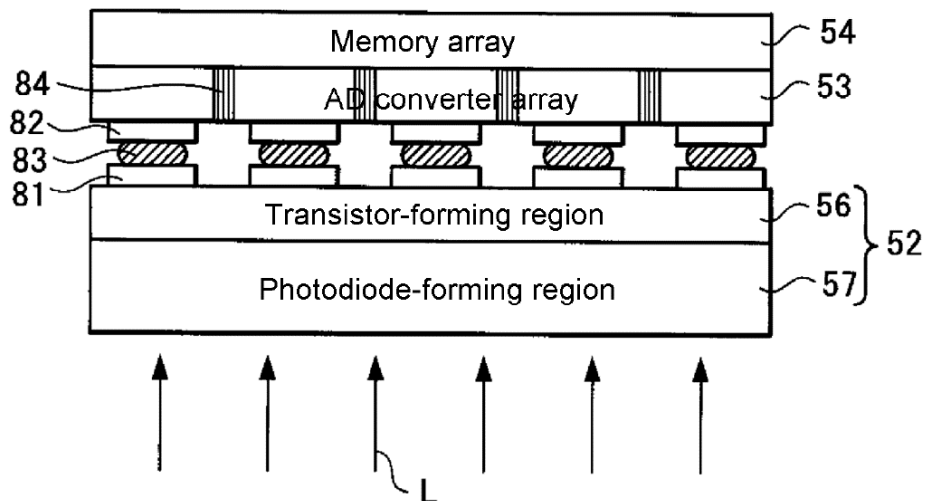


FIG. 26B

Iwabuchi-762

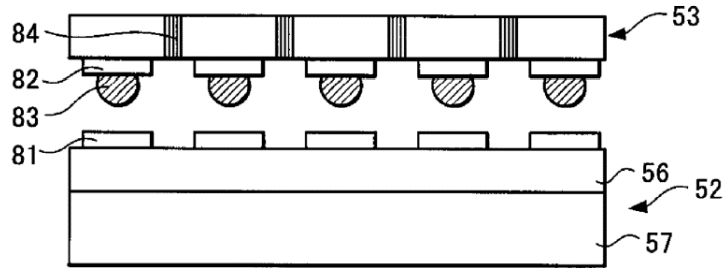
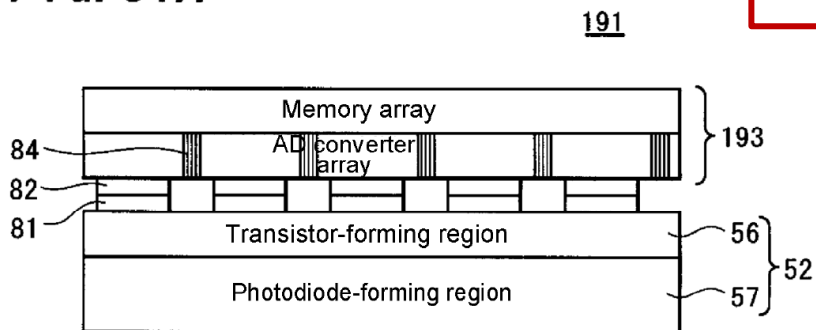


FIG. 31A

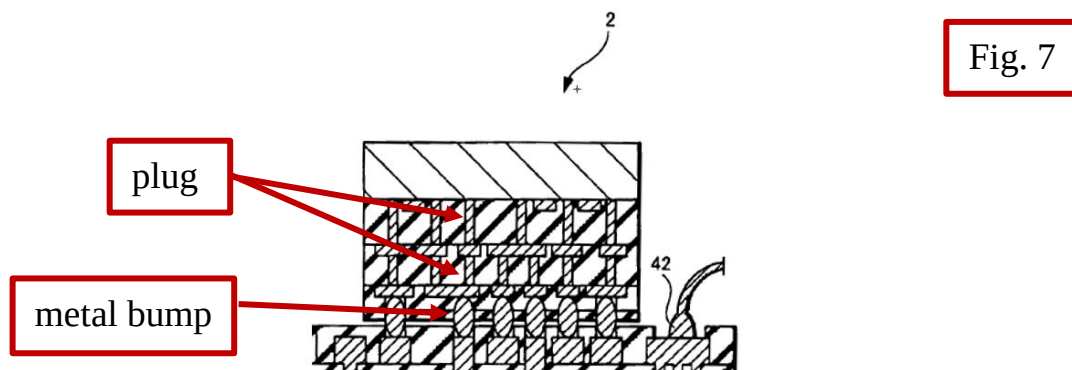
Iwabuchi-762



The DSP chip has a “peripheral circuit unit such as a signal processing circuit provided thereon,” (Iwabuchi, [0117], [0020]), meaning the peripheral circuit unit is formed over the DSP chip substrate as claimed. Carley, ¶112.

Iwabuchi describes flip-chip bonding the sensor and DSP chips to the interposer using metal bumps 32. Iwabuchi, [0125], [0154], Fig. 7. POSAs would have understood that the sensor chip could conventionally bump bond the DSP chip, per Iwabuchi [0153], by replacing bumps 32—on either the sensor chip or the DSP chip—with metal lands. Iwabuchi-762, Figs. 26B, 31A; Tong, [0050] (“metal bonding pads”); Carley, ¶¶113-114. Flip-chip compression bonding conventionally used metal plating to receive bumps. *Id.*, ¶113.

Figure 7 shows the DSP chip includes vias comprising plugs, which as explained above would conventionally have been formed from metal. *Id.*



d. Conduction layers

i. Step [1.c]

1.c	forming a photodiode in a crystalline semiconductor layer of a second substrate;
-----	--

“A photodiode has a depleted semiconductor region with a high electric field that serves to separate photogenerated electron-hole pairs.” Sze, 671. The ’808 patent involves a p-n photodiode having a p-n junction formed by semiconductor layers with opposing types. Carley, ¶¶115, 124-125. The specification identifies “photodiode 210” (Ex. 1001, 3:20-21), comprising a p-n junction formed by “first” n-type layer 214 and “second” p-type layer 212. *Id.*, Figs. 2, 3; Carley, ¶125.

Iwabuchi meets [1.c] for the reasons explained below for [1.g.1] and [1.g.2], and because Iwabuchi describes forming photodiodes 14 in semiconductor layer 12. Iwabuchi, [0121], [0144]; Carley, ¶¶122, 125-126. Semiconductor layer 12 (**red** below) is “formed of a suitable material such as silicon” that is “deposited on the upper layer of insulating layer 11...and it is used as an SOI (silicon on insulator) **substrate**.” Iwabuchi, [0143]; *see also id.*, [0089], Figs. 10A-10B; Carley, ¶¶115-121. The “second substrate” is Iwabuchi’s SOI wafer including semiconductor layer 12. Carley, ¶¶121-123.

It was well-known that “the top silicon layer of an SOI (silicon-on-insulator) wafer is high-quality single-crystalline material that is suitable for high-performance and high-density integrated circuits.” Sze, 343-344; Carley, ¶121. Layer 12 is therefore a “crystalline semiconductor layer” as claimed. Carley, ¶121.

FIG. 10A

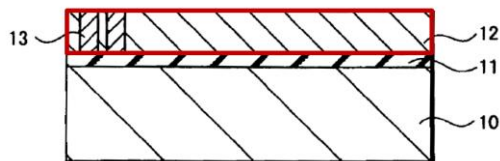
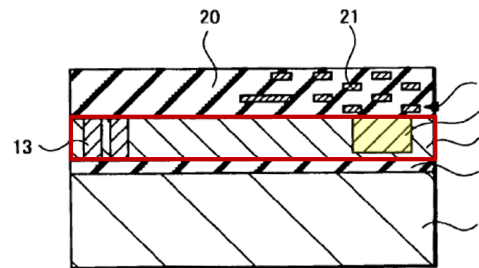


FIG. 10B



ii. Steps [1.g], [1.g.1]

1.g	wherein forming the photodiode comprises:
1.g.1	forming a second conduction type conduction layer in the crystalline semiconductor layer; and

“Conduction type” refers to the method by which electric current is carried in a conductor. Sze, 16-17; Carley, ¶124. The difference between the number of n-type and p-type dopants incorporated into the semiconductor crystal determines the semiconductor type. Carley, ¶124; *accord* Ex. 1001, 3:19-23 (“impurity ions may be implanted into a crystalline semiconductor layer” to form conduction layers). Relative to undoped material, an “n-type conduction layer” has substantially more n-type dopants than p-type dopants, and vice-versa for p-type. Carley, ¶124.

In the '808 patent, the “second conduction type” is p while the “first conduction type” is n. Ex. 1001, 3:23-25, 3:38-40. Iwabuchi uses the same convention.

Iwabuchi describes forming a backside-illuminated “photodiode” comprising n-type semiconductor region 1052, p⁺ accumulation layer 1053, p-type well 1046, and p⁺ accumulation layer 1054, around n-type substrate 1042. *Id.*, [0094], [0096], Fig. 5; Carley, ¶¶125-129. The p⁺ accumulation layer 1054 is the “second conduction type conduction layer.” Carley, ¶130. Layer 1054 is formed in the crystalline semiconductor layer 12 (*supra* § VI.B.1.d.i). Carley, ¶130.

[illegible]

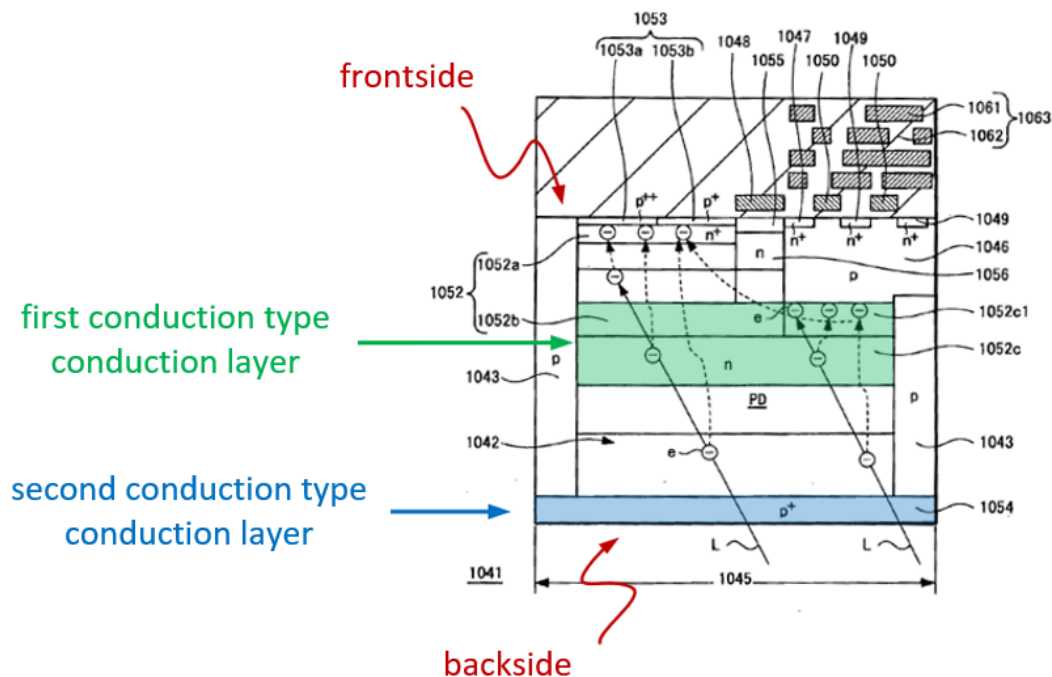
1.g.2	forming a first conduction type conduction layer over the second conduction type conduction layer ,
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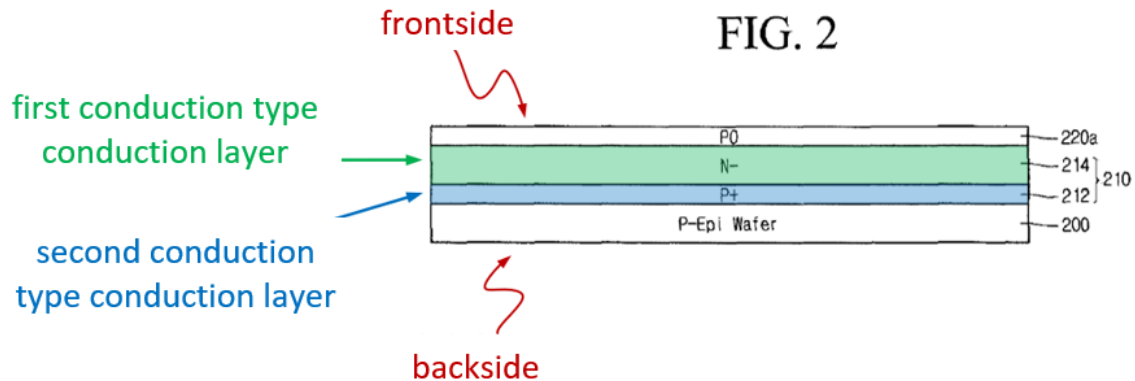
Forming a “first... layer **over**” a “second...layer” does not require direct contact between layers. Ex. 1023, 993 (“over” means “higher than”); *Innova/Pure Water v. Safari Water Filtration Sys.*, 381 F.3d 1111, 1118 (Fed. Cir. 2004) (“In the absence of modifiers, general descriptive terms are typically construed as having their full meaning.”); Carley, ¶133.

Dependent claim 9 confirms this usage by reciting “disposed to directly contact on,” distinguishing “directly contact on” from “over.” *Innova/Pure Water*, 381 F.3d at 1120 (“[W]hen an applicant uses different terms in a claim it is permissible to infer that he intended his choice of different terms to reflect a differentiation in the meaning of those terms.”). The specification distinguishes “on” from “over” when explaining that first conduction layer (214) may be formed “on and/or over” second conduction layer (212). Ex. 1001, 3:34-38; Carley, ¶133.

Relative to the backside surface, n-type layers 1052 (meeting [1.g.2]) are “over” p-type layer 1054 (meeting [1.g.1]), just as n-type layer 214 is “over” p-type layer 212 in the ’808 patent’s Figure 2. Carley, ¶134.

FIG. 5





e. Conduction layer fabrication sequence

POSAs would have understood that Iwabuchi provided reasons to form p⁺ layer 1054 **before** n⁺ layers 1052. Carley, ¶¶135-141; *supra* § V (claim 1 requires forming [1.g.1] layer **before** [1.g.2] layer).

Iwabuchi describes forming p⁺ layer 1054 through ion implantation: (1) it is part of the photodiode (Iwabuchi, [0096]; Carley, ¶¶136-137), which is formed by ion implantation (Iwabuchi, [0176]; Carley, ¶137); (2) it forms a p-n junction with n-type region 1042 (Iwabuchi, Fig. 5; Carley, ¶¶126, 138); and (3) p-n junctions are formed by ion implantation. Iwabuchi, [0144] (“[A] pn junction is formed **by implanting ions of p type conductive impurities** on the n type semiconductor layer 12 and **thereby the photodiode 14...is formed.**”); Carley, ¶139.

Ion implantation was conventionally done through the frontside. *Supra* § IV.B; Iwabuchi, [0006]-[0007]; Carley, ¶140. POSAs would have formed layer 1054 by ion implantation through the frontside of crystalline layer 12 because ion implantation through Iwabuchi's thick backside substrate 10 would not have been conventional, and Iwabuchi describes the sensor chip being "formed" (*i.e.*, complete) **after** thinning substrate 10 **without** describing any further ion implantation or other doping. Iwabuchi, [0150]-[0151]; Carley, ¶¶141-143. This mirrors the '808 patent's description of forming layer 212 by ion implantation through the substrate 200's frontside before removing bottom layer 200. Ex. 1001, 3:19-33, 4:47-53, Fig. 8; Carley, ¶144.

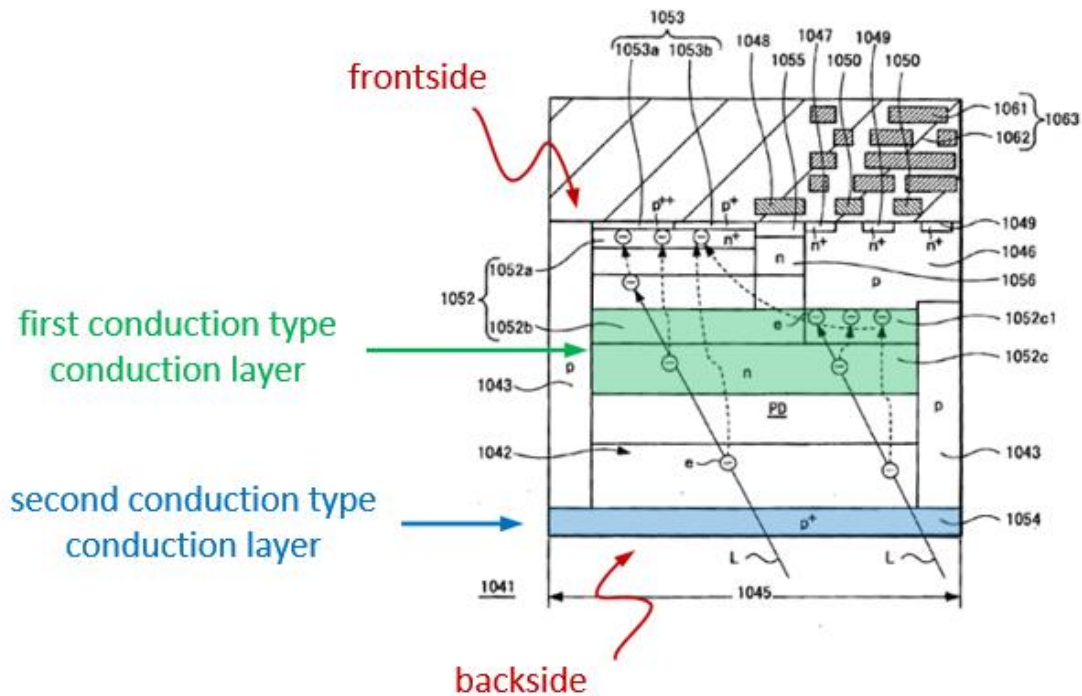
With Iwabuchi's SOI substrate 10 in place, POSAs would have found it conventional to implant p-type layer 1054 **before** forming graded n-type layers 1052 because p⁺ layer 1054 is a blanket layer across the crystalline layer 12 backside. Iwabuchi, Fig. 5; Carley, ¶¶145-146. POSAs would conventionally form a deep blanket implant **first**, then pattern new, shallower features over it, because implanting through other patterned features would interfere with forming a flat and uniform layer 1054 as shown. Carley, ¶147. The '808 patent describes the same approach for layer 212. Ex. 1001, 3:19-33; Carley, ¶146.

Moreover, ion implantation requires subsequent thermal annealing to repair lattice damage from the implantation. Carley, ¶148. POSAs would have

understood that layer 1054 would have required a relatively high-energy implantation because it is heavily doped and furthest from the front surface. *Id.*, ¶149. POSAs would have understood that the crystal lattice damage from such a high-energy implant would have required a relatively long, high-temperature anneal. *Id.*, ¶¶149-150. If layers 1052 were already formed, then the high temperature anneal for the layer 1054 implantation would significantly alter the layers 1052 doping concentrations and placement by causing dopants to diffuse within the crystal lattice. *Id.*, ¶150.

Forming layers 1052 after layer 1054 does not have this problem with sequential annealing steps. Carley, ¶151. *I.e.*, POSAs would implant layer 1054, then do a high-temperature anneal. *Id.* Then POSAs would implant layers 1052 and anneal at a much lower temperature and/or duration to cure the lattice damage by that later implant. *Id.* Therefore, POSAs would have preferred implanting the p⁺ layer 1054 first. *Id.*, ¶¶151-152.

FIG. 5



Iwabuchi also describes forming a potential distribution in n-type conduction layers 1052 “by controlling the impurity concentration” in the vertical direction through “stepwise increasing the n-type impurity concentration...from the back surface side of the substrate to the substrate surface side,” and from layer 1052c1 to layer 1052a. *Id.*, [0100]-[0101]; Carley, ¶153. POSAs would have conventionally accomplished this through serial ion implantation at different depths. *E.g.*, Masagaki, [0030] (describing ion implantation “being divided into several implantations in the depth direction”); Carley, ¶154.

It would have been conventional to form the stepwise doping grading by ion implantation from the backside to the frontside in Figure 5, *e.g.*, from the layers

furthest from the frontside surface, entailing the deepest (and highest energy) implantation, to the layers that are shallowest relative to the frontside surface. Carley, ¶155. POSAs would therefore have found it conventional to form the graded n-type layers 1052 *after* forming layer 1054 because, relative to the frontside surface, layer 1054 is “deepest” and would be implanted first, whereas by comparison layers 1052 are “shallower” and would be implanted later. *Id.*; Iwabuchi, Fig. 5.

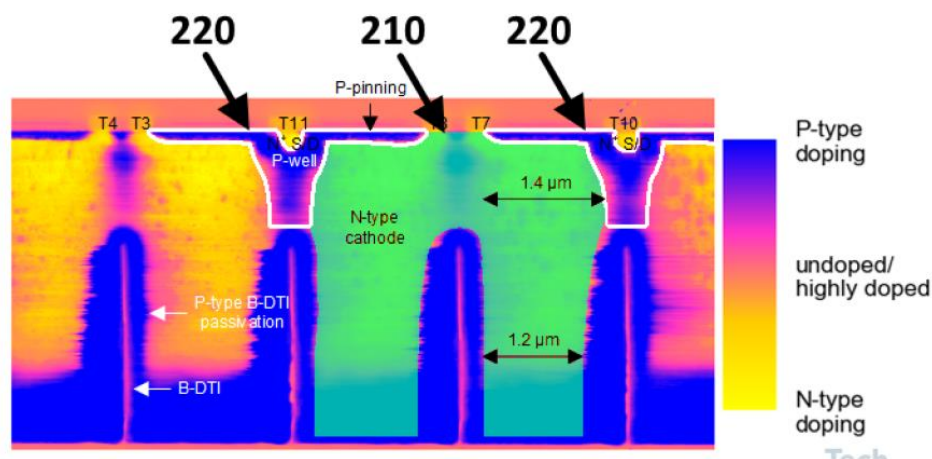
f. Isolation layers

i. Step [1.d]

1.d	forming an ion implantation isolation layer in the photodiode;
-----	--

The specification describes isolation layers providing “pixel-to-pixel isolation” by “insulating” adjacent “pixels” from each other. Ex. 1001, 3:44-61, 4:2-4, 4:56-60; Carley, ¶156. POSAs would have understood that the isolation layer prevents carriers generated outside a pixel from crossing into the pixel and being collected with photogenerated carriers. Carley, ¶157.

PO's contentions assert that ion implantation isolation layer "220" is formed "in the photodiode" identified as "210," using labels corresponding to reference numerals 220 and 210 in '808 patent Figure 3. IC-A1, 16 ("An isolation layer (labeled 220) of P-type impurity ions is formed *in photodiode 210*. Two regions of P-type impurity ions collectively correspond to isolation layer 220: a P-type implant isolation layer, and a P-type pinning layer."); Ex. 1001, Fig. 3; Carley, ¶¶158-161. As explained for steps [1h.1] and [1.h.2], Iwabuchi discloses the same two p-type isolation layers as PO's contentions. Carley, ¶162.



Based on VisionX's contentions, and for the reasons explained below for steps [1.h.1] and [1.h.2], Iwabuchi meets step [1.d]. Carley, ¶163.

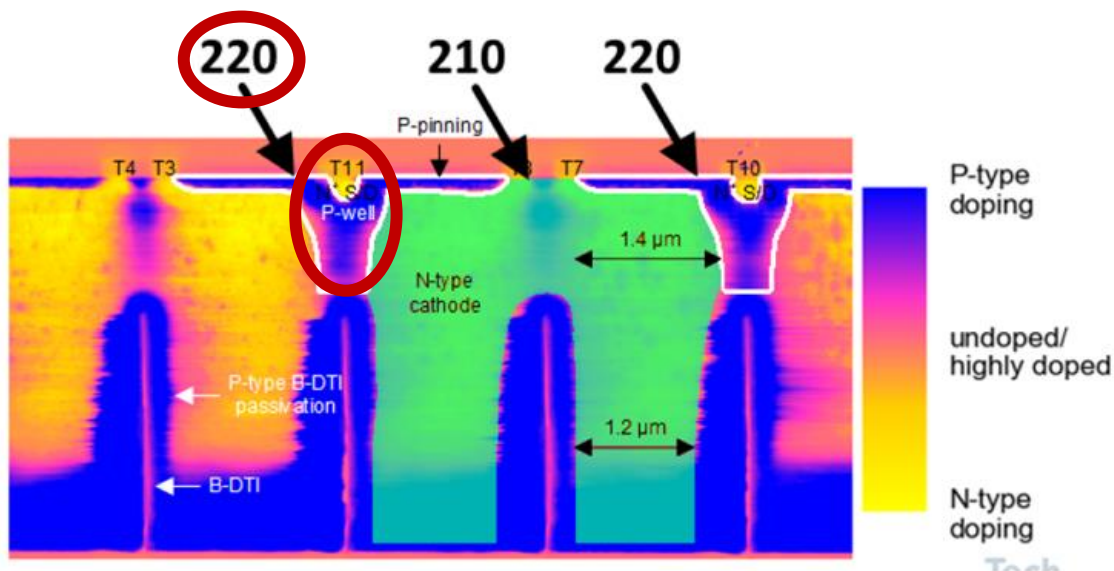
ii. Step [1.h.1]

1.h.1	wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer over the first conduction type conduction layer ,
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Iwabuchi meets [1.h.1] in at least two ways.

(1) p-region 1046

Iwabuchi's "p type semiconductor well region 1046" provides a "second conduction type isolation layer" "over" the "first conduction type" conduction layer because region 1046 is "higher than" layers 1052c and 1052c1. Iwabuchi, [0096], Fig. 5; *supra* § VI.B.1.d.iii (discussing "over"); Carley, ¶165. This matches PO's contentions, IC-A1, 16, 25, 27 (red circles added), treating a p-well as an isolation layer 220. Carley, ¶166.

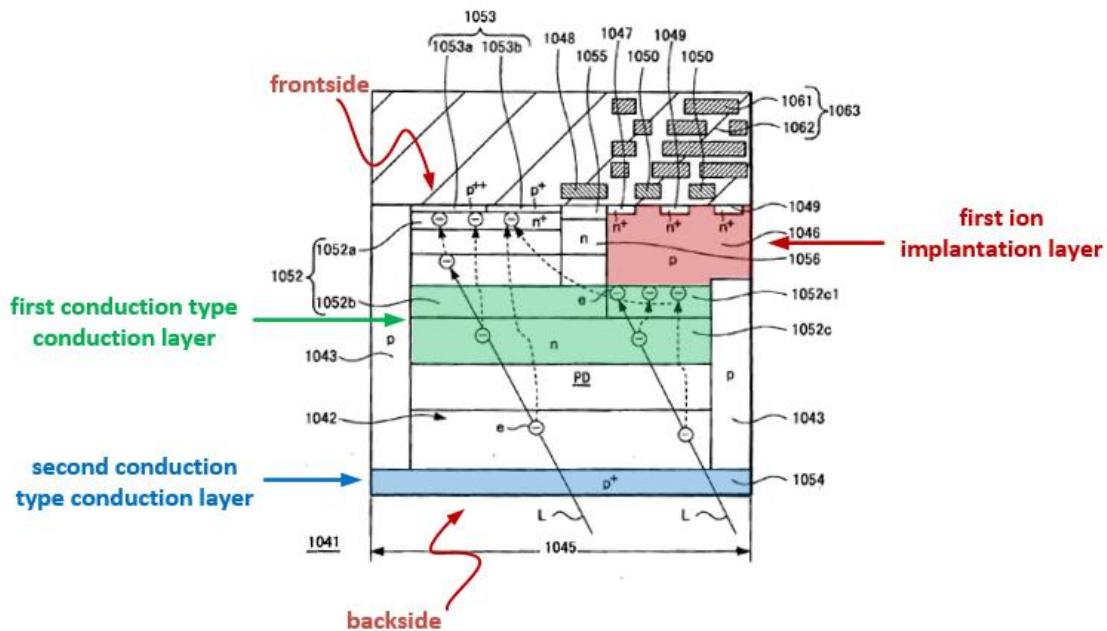


IC-A1, 16.

Iwabuchi's region 1046 is "in the photodiode" just like the "P-well" in PO's contentions. Carley, ¶¶166-167. Region 1046 is also "in the photodiode" because it defines a p-n junction with layer 1052, and Iwabuchi expressly describes that p-n junction as providing an electric field directing photogenerated electrons toward

accumulation region 1052a. Iwabuchi, [0096]-[0103], Fig. 5 (dashed line indicating photogenerated electron drift from 1052c1, adjacent region 1046, to region 1052a); Carley, ¶¶167-170. Region 1046 provides carrier isolation between adjacent pixels in the volume including region 1046. Carley, ¶167. Iwabuchi describes forming p-region 1046 by ion implantation because p-n junctions are formed by p-type ion implantation. Iwabuchi, [0144]; Carley, ¶¶171-172.

FIG. 5



Iwabuchi further describes an embodiment with lateral grading of the p-type doping in region 1046. Iwabuchi, [0102] (“[T]he above-described potential distribution of substantially the lateral direction can be formed by progressively or stepwise decreasing the p type impurity concentration of the portion adjoining the n type semiconductor region 1052c1 of the p type semiconductor well region 1046

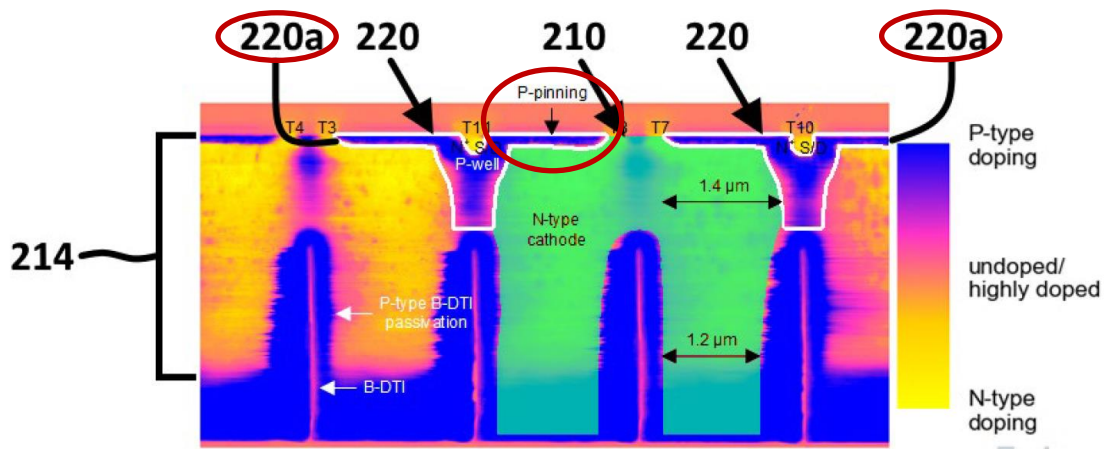
toward the n type electric charge accumulation region 1052a[.]”). POSAs would have understood that forming this progressive doping distribution in p-region 1046 would conventionally have been done by multiple masks and ion implantation. Carley, ¶174.

In any event, POSAs would have known that forming p-type region 1046 by ion implantation was conventional. *E.g.*, Suzuki, [0057], Fig. 4 (“deep P well 43” formed by ion implantation); Carley, ¶173. POSAs would have been motivated to form p-well 1046 by ion implantation because this provided better control than basic diffusion over dopant placement and concentration, flexibility in forming dopant profiles, and reduced the time at high temperatures required for diffusion, all making it possible to form devices with sub-micron features. Sze-2002, 453, 469; Carley, ¶¶175-176. Indeed, by December 2007, excepting regions formed by doped epitaxial growth, virtually all semiconductor device structures—including a p-well like 1046—were formed by ion implantation. Carley, ¶176.

POSAs would also have understood that forming p-region 1046 by ion implantation would have meant forming it **after** forming n-type conduction layers 1052c1 and 1052c, which are deeper than region 1046, for the same reasons a POSA would form layer 1052 after layer 1054, and that this sequence would have been conventional. *Supra* § VI.B.1.e (layer fabrication sequence); Carley, ¶177.

(2) p-layer 1053

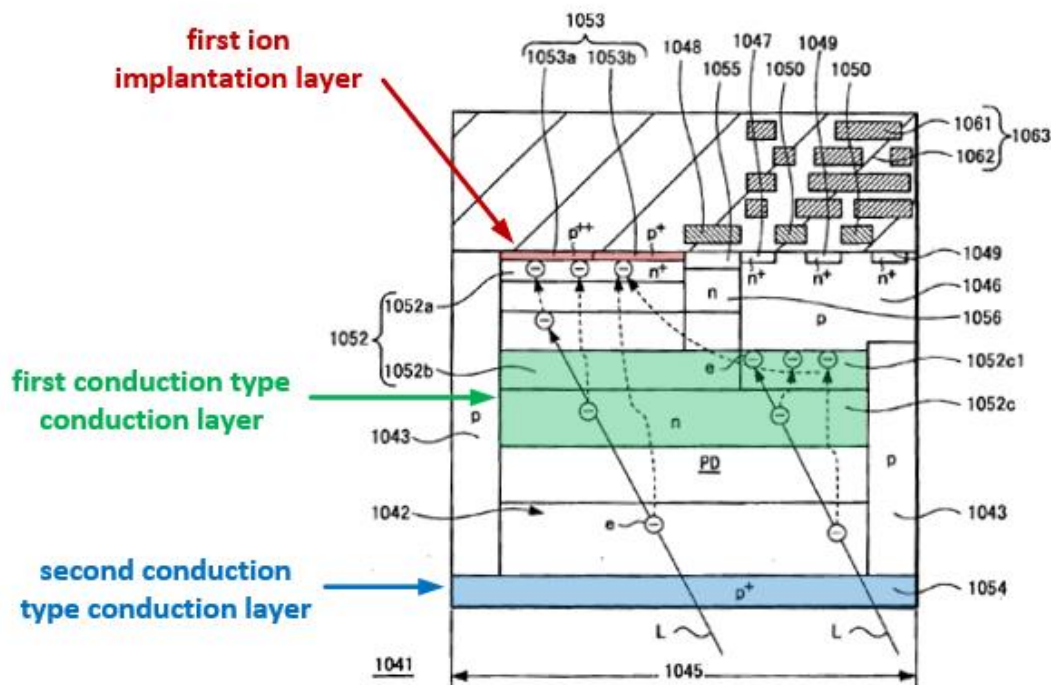
PO's contentions assert a highly-doped p-type shallow planar layer that it labels "P-pinning" meets the [1.h.1] isolation layer (corresponding to '808 patent layer 220a). IC-A1, 25 (red circles added); Carley, ¶178.



IC-A1, 25.

Based on those contentions, Iwabuchi's p^{++}/p^{+} layer 1053 is a "second conduction type" isolation layer meeting [1.h.1]. Carley, ¶179; *10X Genomics*, Paper 8, 19; *supra* § VI.B.1.d.ii. POSAs would have understood that layer 1053 is a pinning layer exactly like the layer PO's contentions map to [1.h.1]. IC-A1, 25; Guidash, Abstract, 4:43-45 & Fig. 4 (pinning layer 34); Carley, ¶179. Layer 1053 is "over" the "first conduction type conduction layer" 1052 from step [1.g.2]. Iwabuchi, Fig. 5; Carley, ¶180.

FIG. 5



Layer 1053 is “in the photodiode.” Iwabuchi, [0096]; Carley, ¶181.

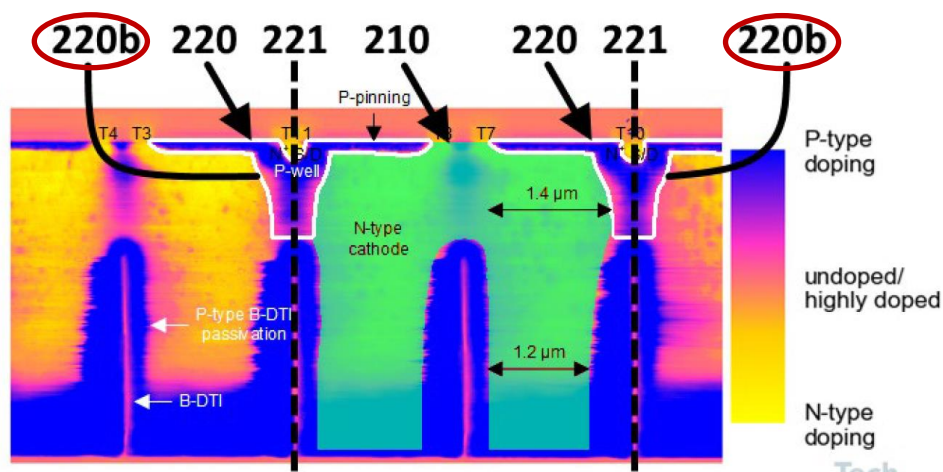
Iwabuchi describes forming layer 1053 by ion implantation, for the same reasons discussed for layer 1054. Iwabuchi, [0144]; Carley, ¶182; *supra* § VI.B.1.e. It was conventional to form a pinning layer like 1053 by ion implantation. *E.g.*, Guidash, 8:16-19; Maruyama, [0023] (accumulation layer 12); Carley, ¶183. Moreover, Iwabuchi describes laterally grading the p^+ impurity concentration in layer 1053. Iwabuchi, [0104]. POSAs would have known that ion implantation was a conventional way to form a lateral doping gradient. Carley, ¶¶174, 184.

POSAs would have formed layer 1053 by implantation *after* forming n-type conduction layers 1052 in step [1.g.2] because layer 1053 is the shallowest layer, and would be formed last when implanting from deepest to shallowest. Carley, ¶185. This sequence would have been conventional for the reasons discussed above. *Supra* § VI.B.1.e; Carley, ¶186.

iii. Step [1.h.2]

1.h.2	wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.
-------	--

Based on PO’s contentions, isolation layer “220b” at an interface “221” between pixels of *adjacent photodiodes*⁴ is “*in the photodiode*...at an interface between pixels of *the photodiode*” so that Iwabuchi’s p-well 1046 *and* separation regions 1043 each alternatively (or together) meet [1.h.2]. IC-A1, 27 (below, red circles added); *10X Genomics*, Paper 8, 19; Carley, ¶¶187-191.



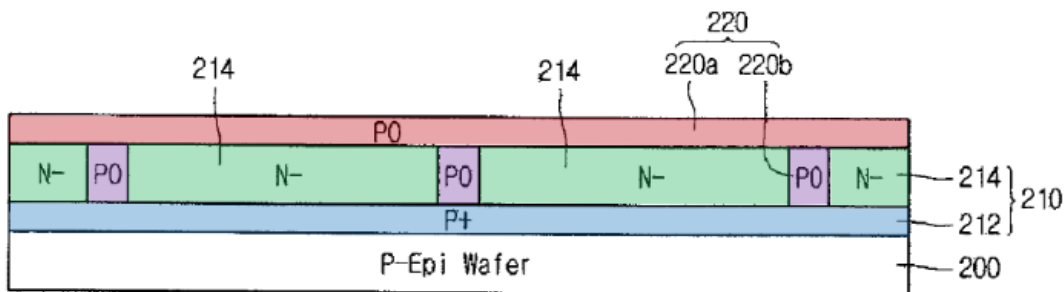
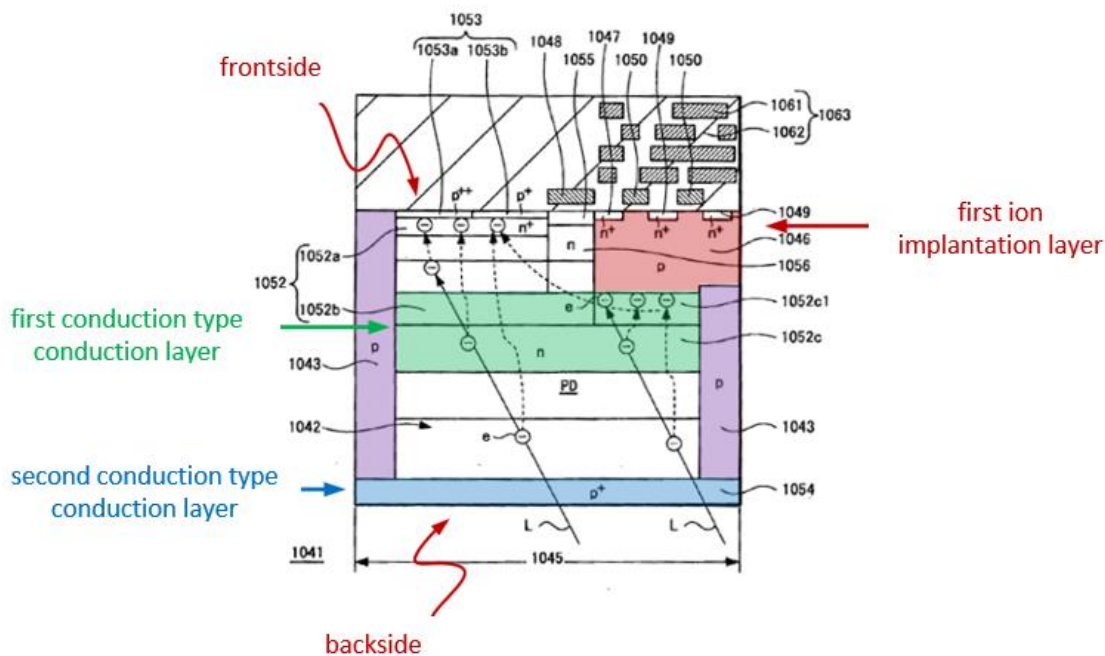
⁴ PO argues that Sony’s sensors comprise “photodiodes” (plural). IC-A1, 6.

Based on PO's contentions, Iwabuchi's ion-implanted p-well 1046 is "at an interface between pixels of the photodiode" and meets [1.h.2], just like "P-well" "220b" labeled in the contentions. IC-A1, 27; Carley, ¶¶192-193. Iwabuchi's Figure 5 defines a "unit pixel 1045." Iwabuchi, [0094], Fig. 5. "A large number of unit pixels 1045 are arranged in an XY matrix fashion," *id.*, [0094], and POSAs would have understood that this forms p-well 1046 at an interface with an adjacent pixel. Carley, ¶193.

Iwabuchi's p-type separation region 1043 also meets [1.h.2]. Carley, ¶195. Pixel separation region 1043 "divide[s] respective pixels[.]" Iwabuchi, [0094]. Region 1043 meets [1.h.2] because it defines the pixel boundaries in the same manner as region 220b in the '808 patent and in PO's contentions. Iwabuchi, [0094]-[0095], Fig. 5; Ex. 1001, Fig. 3; IC-A1, 27; Carley, ¶195.

If p-region 1046 provides step [1.h.1]'s "first ion implantation layer," then region 1043 provides step [1.h.2]'s "second ion implantation layer." If p⁺⁺ layer 1053 provides step [1.h.1]'s "first ion implantation layer," then step [1.h.2]'s "second ion implantation layer" can be either region 1043 or region 1046. Carley, ¶194.

FIG. 5



Separation region 1043 is “in the photodiode” because it forms a p-n junction at each interface with adjacent n-type regions 1052. Iwabuchi, Fig. 5; Carley, ¶196. The “separation” region 1043 provides isolation because it prevents lateral carrier movement to adjacent photodiodes/pixels. Iwabuchi, Fig. 5; Carley, ¶197.

Pixel separation region 1043 is formed by ion implantation because it forms a p-n junction with n-type layer 1052 (Iwabuchi, [0102], Fig. 5; Carley, ¶198), and p-n junctions are formed by p-type ion implantation. Iwabuchi, [0144]; Carley, ¶198; *supra* § VI.B.1.e. Moreover, it would have been conventional to form region 1043 by ion implantation. Iwabuchi describes one embodiment forming separation region 1043 by stepwise decreasing the p-type doping level along the vertical axis in Fig. 5. Iwabuchi, [0058], [0102]; Carley, ¶199. It was well-known to form a vertical doping gradient through a series of ion implants. *E.g.*, Masagaki, [0030]; Carley, ¶200. Even without a stepwise gradient, it was conventional to form pixel separation regions by ion implantation, and POSAs would have had a reasonable expectation of success in doing so. *E.g.*, Maruyama, [0023]; Suzuki, [0057], Fig. 4 (“deep P well 43” formed by ion implantation); Gouscha, 3:24-30, Fig. 2 (implanting diffusion 8); Carley, ¶¶200-201.

g. Step [1.e]

1.e	bonding the first substrate to the second substrate to connect the photodiode to the metal interconnection; and
-----	---

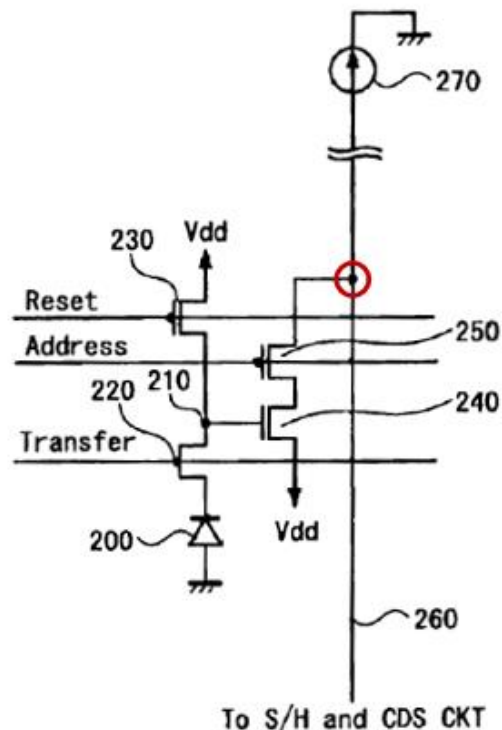
i. “bonding...to connect the photodiode to the metal interconnection”

PO’s contentions allege that electrical connection between a metal interconnection and “a column out transistor of a pixel of the photodiode” meets

“connect.” IC-A1, 17. This “facilitates electrically connecting the photodiode and ISP metal interconnects.” *Id.*

Iwabuchi shows the same structure, *e.g.*, a pixel readout, from the photodiode (labeled 200 in Fig. 9), through a column out transistor 250 output to line 260. Iwabuchi, [0133] (“[S]ignals of respective pixels are read out...at every pixel column through the vertical signal line 260.”), [0088], Fig. 9; Carley, ¶¶202-204. Vertical signal line 260 connects to the DSP chip, which includes the CDS (correlation double sampling) circuit identified in Figure 9. Iwabuchi, [0020], [0130]; Carley, ¶205.

FIG. 9

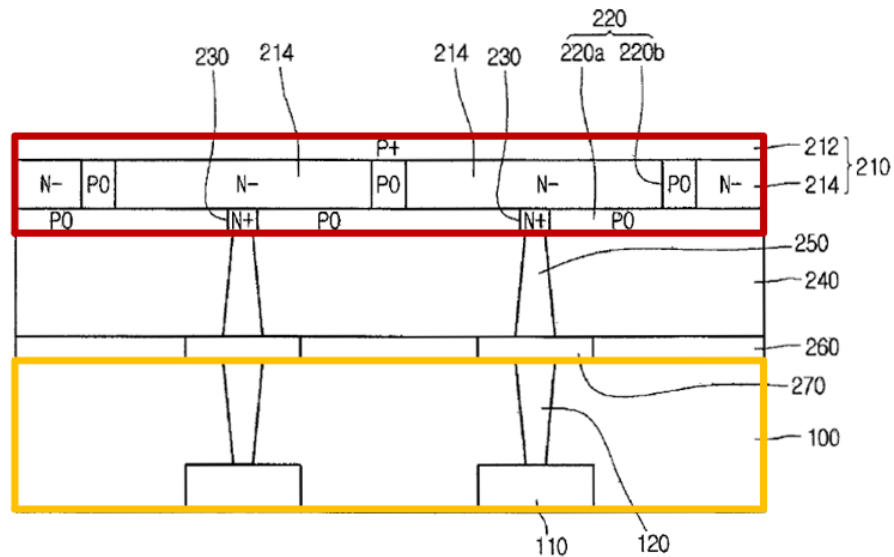


Under PO's contentions (*10X Genomics*, Paper 8, 19), Iwabuchi meets [1.e] for the interconnection on each first substrate described *supra* § VI.B.1.c (step [1.b]), because when bonding the first and second substrates, line 260 is “electrically connected” (IC-A1, 17) to the CDS circuit on the DSP chip through metal interconnections on the supporting substrate 30, metal interconnections on the DSP chip, and—when used—metal interconnections on the interposer. Carley, ¶¶206-208.

ii. “bonding the first substrate to the second substrate”

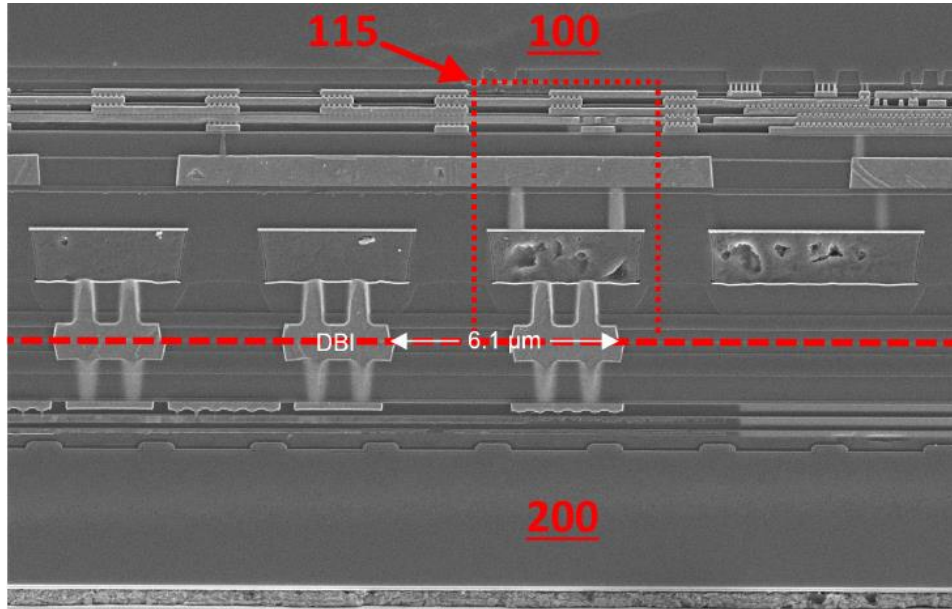
No '808 patent embodiment bonds a first and second substrate with ***direct contact*** between the substrates. Carley, ¶¶209-210. The lone embodiment interposes dielectric layers 240 & 260, plug 250, and contact 270 between the “second substrate 200” and the “first substrate 100.” Ex. 1001, Fig. 8; 4:8-21; Carley, ¶211.

FIG. 8



A claim construction that excludes a preferred embodiment “is rarely, if ever correct[.]” *Vitronics v. Conceptronic*, 90 F.3d 1576, 1583 (Fed. Cir. 1996). The principle applies even more strongly to excluding a sole embodiment. *Kaufman v. Microsoft*, 34 F.4th 1360, 1372 (Fed. Cir. 2022). Thus, step [1.e], “bonding the first substrate to the second substrate,” requires either that (a) “substrate” means an originally-identified substrate as modified by subsequent process steps, or (b) “bonding” includes joining substrates through intervening layers (like dielectrics 240 or 260) without requiring direct contact. Carley, ¶212.

PO's contentions likewise equate bonding **dies** (chips) to bonding **substrates** in a die, by asserting that step [1.e]'s "bonding" is met when "[t]he ISP and CIS **dies** are bonded together, and thus, **corresponding ISP Si substrate 100 and CIS Si substrate 200** are bonded together." IC-A1, 17.



IC-A1, 17.

In PO's contentions, the ISP and CIS **dies** include metal and dielectric layers formed on silicon (Si) substrates. Carley, ¶¶213-214. This bonding makes physical contact between layers added to substrates "100" and "200." Carley, ¶214.

Each "first substrate" identified *supra* § VI.B.1.b (step [1.a]) bonds to the second substrate (with semiconductor layer 12), like the PO's contentions and the '808 patent specification. Carley, ¶215. *10X Genomics*, Paper 8, 19.

(1) interposer

The sensor chip “is mounted on the interposer through the bump 32 by flip-chip bonding” using compression bonding. Iwabuchi, [0153], Fig. 7; Carley, ¶216. This bonds the second substrate to the interposer through intervening layers, just like the ’808 patent describes bonding second substrate 200 (red) to first substrate 100 (orange), and just like PO maps step [1.e] in its contentions. Ex. 1001, 4:25-31 & Fig. 8; IC-A1, 17; Carley, ¶¶217-218.

FIG. 8

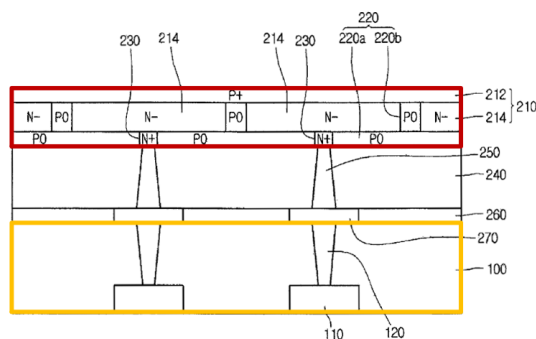
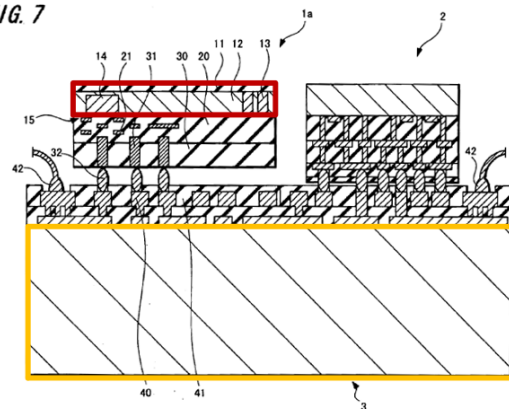


FIG. 7



(2) supporting substrate

Supporting substrate 30 is “bonded to the upper layer of the interlayer insulator 20 by a suitable method such as thermo compression bonding using a thermosetting resin as an adhesive.” Iwabuchi, [0146], Fig. 10C. The insulator layer 20 is formed on semiconductor layer 12 (*id.*, [0145]) the same way that the ’808 patent describes forming “first dielectric 240” (which can be “an oxide layer”) “over second substrate 200.” Ex. 1001, 4:8-12, Figs. 5, 8; Carley, ¶219.

FIG. 8

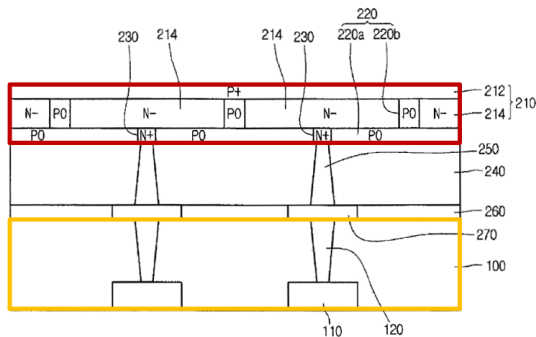
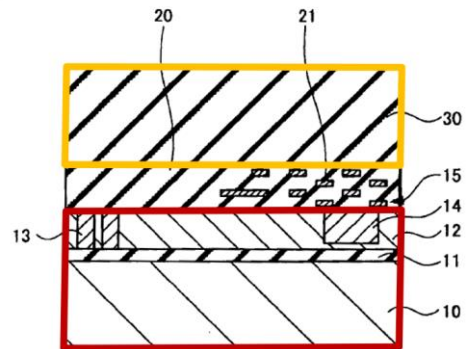


FIG. 10C



Iwabuchi thus describes bonding substrate 30 to the “second substrate” with intervening layer 20 just like the ’808 patent describes bonding the first and second substrates with intervening layers 240 and 260. Carley, ¶220.

(3) DSP substrate

Iwabuchi’s sensor and DSP chips are flip-chip bump bonded in the same manner that Iwabuchi describes flip-chip bonding the sensor chip to the interposer. Iwabuchi, [0153] (“sensor chip can be directly mounted on the signal processing chip as a module”); Carley, ¶221. It was well-known to flip-chip bond dies together. *E.g.*, Iwabuchi-762, [0047], Figs. 1, 26B, 31A (below); Rogalski, 82-83 (flip-chip bonding using indium bump), Fig. 14 (below); Balcerak, 386, Fig. 1 (same); Carley, ¶¶222-230.

FIG. 1

51

Iwabuchi '762

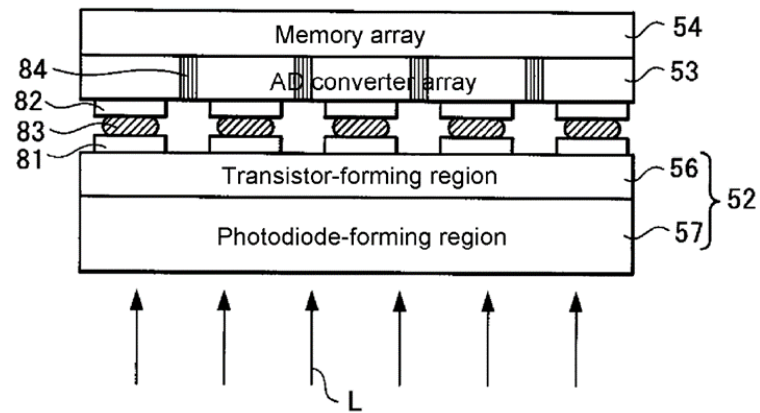


FIG. 26B

Iwabuchi '762

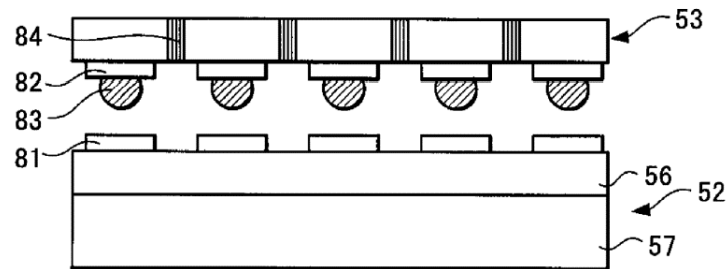
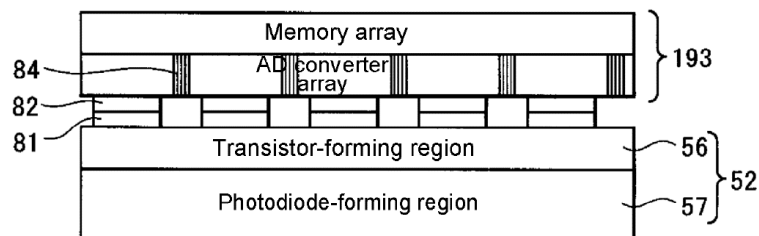


FIG. 31A

191

Iwabuchi '762



Rogalski

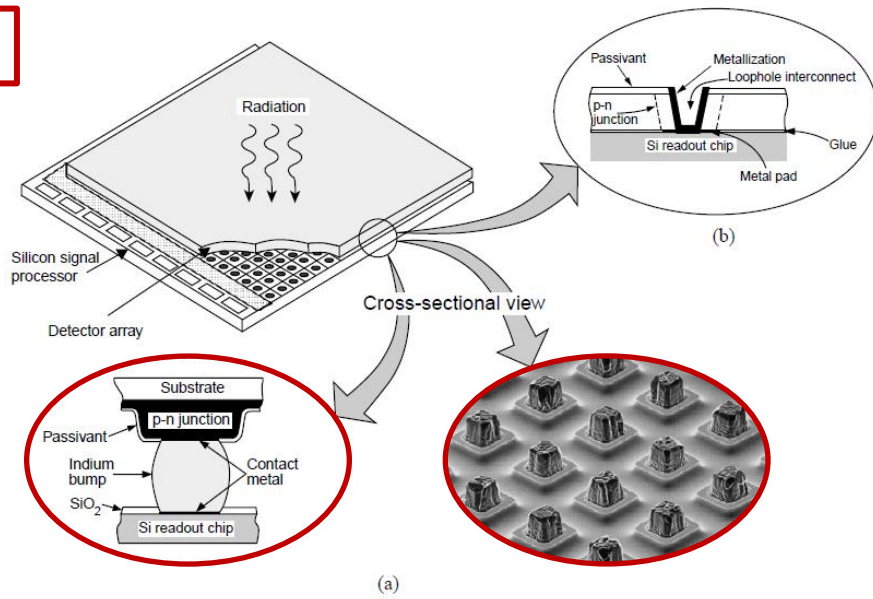
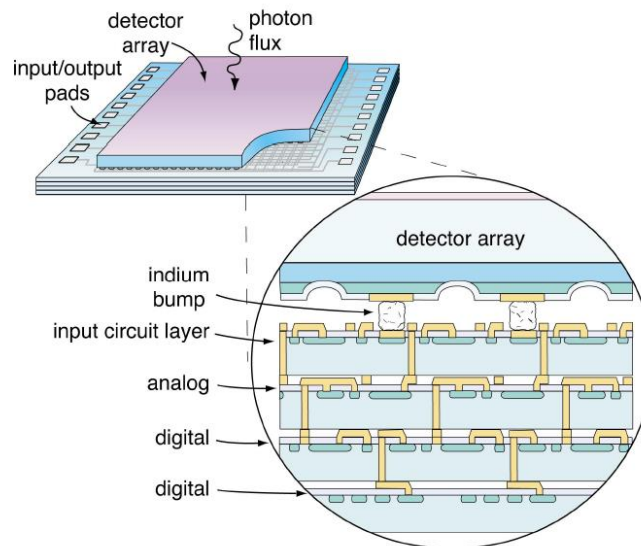


Fig. 14. Hybrid IR FPA with independently optimised signal detection and readout: (a) indium bump technique, (b) loophole technique.

Balcerak



As explained *supra* § VI.B.1.c.iii (step [1.b]), it was known to form planar metal landing pads on the sensor (or DSP) chip, in place of bumps 32 used to bond the sensor chip to the interposer, (Iwabuchi, [0125], [0154], Fig. 7), for bonding DSP (or sensor) chip metal bumps 32. Iwabuchi, [0153], Fig. 7; Carley, ¶228; *cf.* Iwabuchi-762, Figs. 26B; Rogalski, Fig. 14; Balcerak, Fig. 1. POSAs would also have found it conventional to compression bond Iwabuchi’s sensor chip 1a to the DSP chip using metal contact pads. Iwabuchi-762, Fig. 31A; Carley, ¶¶229-230.

h. Step [1.f]

1.f	removing a lower portion of the second substrate to expose the photodiode,
-----	--

Substrate 10 is a lower portion of the second substrate just like the “P-Epi Wafer” in the ’808 patent. Iwabuchi, [0142], Fig. 10A; Carley, ¶¶231-234. This comports with defining material layers as “over” by reference to the backside light-incident surface in step [1.g.2]. *Supra* § VI.B.1.d.iii; Ex. 1001, Fig. 2; Carley, ¶231.

FIG. 2

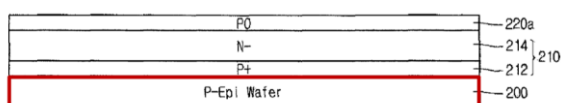
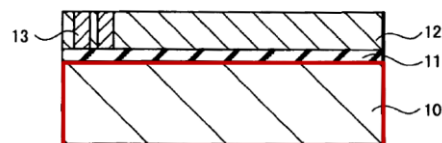
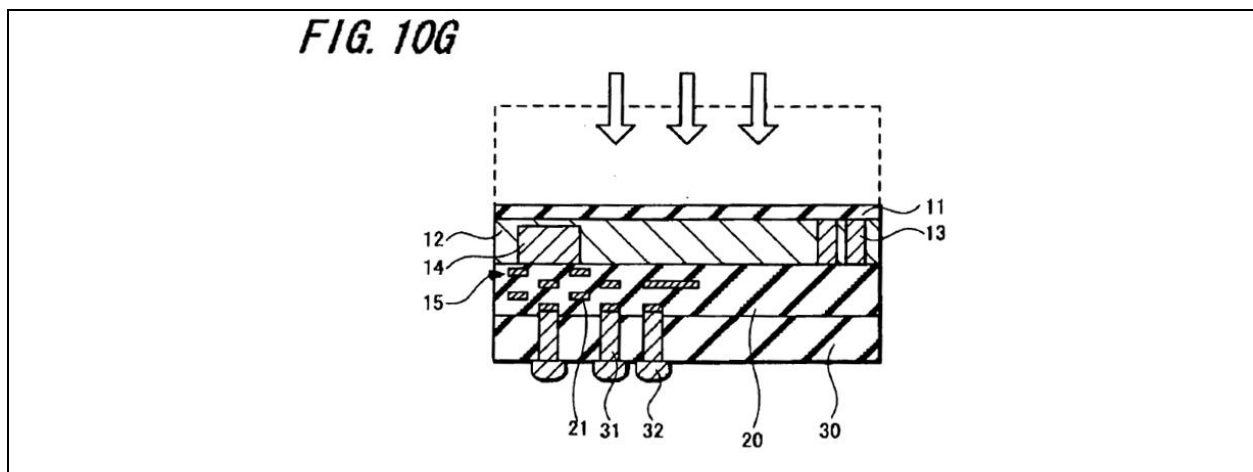


FIG. 10A



The term “to expose” means to “allow to be subjected to an action, influence, or condition” or “to subject...to the action of light.” Ex. 1034, 626; Carley, ¶¶232-233. Iwabuchi describes removing substrate 10 to expose the photodiode. “[S]emiconductor substrate 10 is decreased in thickness until the photodiode 14 becomes able to receive light from the side of the semiconductor substrate 10 of the SOI substrate,” (Iwabuchi, [0150]; *accord id.*, [0065], Fig. 10G), just like the ’808 patent describes removing the “P-Epitaxial layer” (Ex. 1001, 4:36-53, Fig. 8). Carley, ¶234. This meets [1.f].



Furthermore, although Figure 10G depicts backside-illuminated photodiode 14 as not completely extending to the backside surface of substrate 12, POSAs would have known that extending the photodiode so that the backside of layer 1054 in Fig. 5 coincided with the interface of substrate 12 and oxide 11 was conventional. Maruyama, [0032], Fig. 5B; Ezaki, Figs. 1-3, 6; Lee, Fig. 10; Suzuki, Fig. 8; Carley, ¶235. Further, removing oxide layer 11 was also conventional. Shiraiwa, [0010], Fig. 9E; *accord id.*, [0037], Fig. 5E; Carley,

¶¶235-236. Thus, even if “to expose the photodiode” was interpreted to require an absence of material over the photodiode, meeting that step would have been obvious. Carley, ¶236.

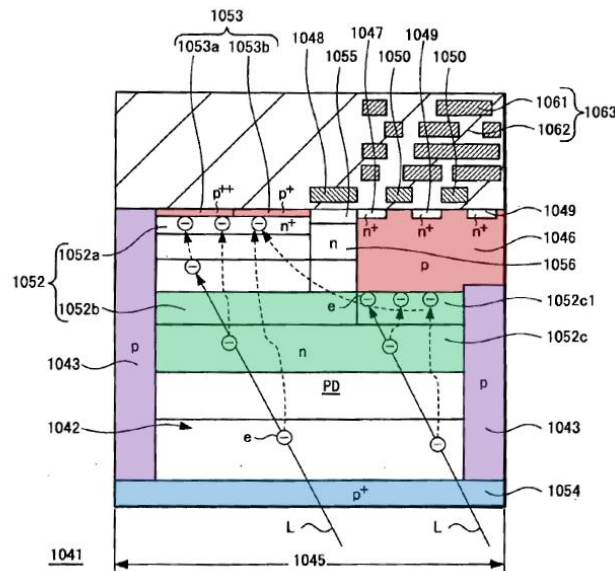
Claim 1 as a whole would have been obvious over Iwabuchi. Carley, ¶237.

2. Claim 4

The method of claim 1, comprising forming the ion implantation isolation layer over at least one of a side of the photodiode and a bottom of the photodiode.

Iwabuchi’s separation region 1043, layer 1053, and region 1046 each comprise ion implantation isolation layers formed “over” layer 1054. *Supra* §§ *Supra* § VI.B.1.d.iii (discussing “over”), VI.B.1.f.ii ([1.h.1]), VI.B.1.f.iii ([1.h.2]); Iwabuchi, Fig. 5; Carley ¶¶238-239. Relative to the ion implantation layers, layer 1054 is closest to “a bottom of the photodiode.” Iwabuchi, Fig. 5; Carley, ¶238.

FIG. 5



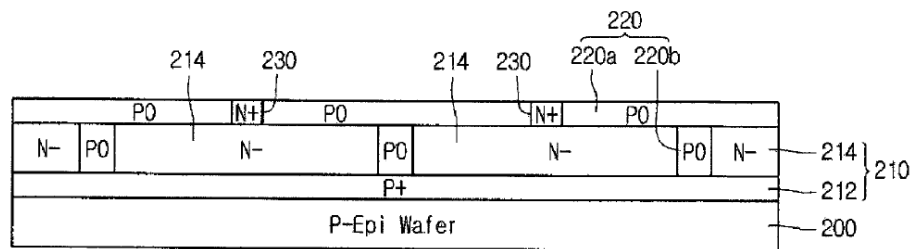
Iwabuchi therefore meets claim 4, rendering it obvious. Carley, ¶240.

3. Claim 5

The method of claim 1, wherein the ion implantation isolation layer comprises a P0 layer.

The '808 patent does not define “P0 layer.” The term “P0” has no known meaning in the art. Carley, ¶242.

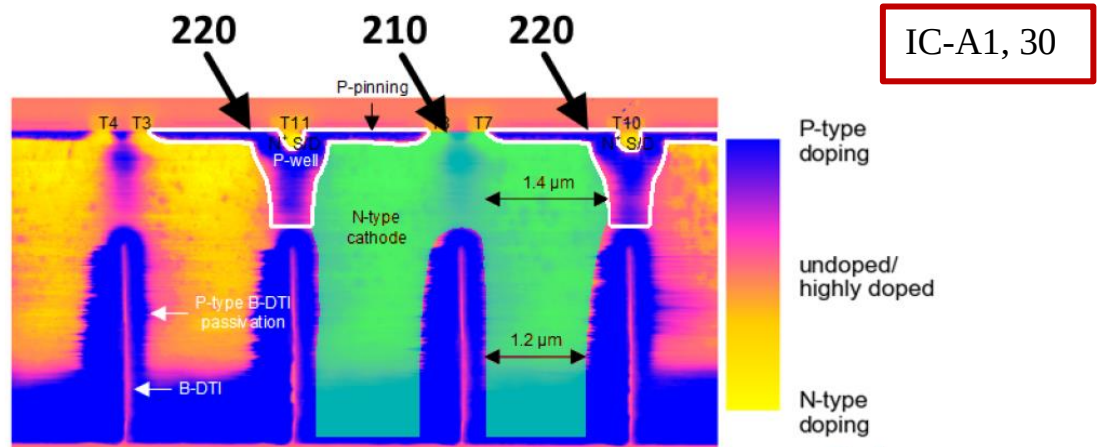
FIG. 4



The specification describes forming “P0” layers 220a and 220b by ion implantation. *Id.*, 3:44-61. Lacking any definition, POSAs would have surmised that P0 could mean either (a) **any** p-type doping level, or (b) p-type doping **less than** p⁺.⁵ Carley, ¶¶242-247. PO’s contentions allege “ion implantation layer 220 includes a P0 layer,” citing an image with blue coloration, and legend, suggesting heavily p-doped (*e.g.*, p⁺) “P-pinning” and “P-well” regions 220. IC-A1, 30; Carley, ¶246. The arbitrary white outline defining layer “220” in PO’s contentions

⁵ Petitioner reserves the litigation argument that “P0” is indefinite.

includes a pink/purple-colored metallurgical transition from p^+ to n^+ doping in adjacent conduction layers. Carley, ¶247.



Based on the contentions, Iwabuchi meets claim 5 because p layer 1043, p region 1046, and p^+ layer 1053, are each isolation layers and the moderate “p” doping in 1043 and 1046 is less than the p^+ concentration. *Supra* §§ VI.B.1.f.ii(1) (region 1046), VI.B.1.f.ii(2) (layer 1053), VI.B.1.f.iii (layer 1043); Carley, ¶248; *10X Genomics*, Paper 8, 19. Real devices would include a non-abrupt transition between these p-type isolation layers and neighboring n-type regions, and thus meet claim 5 just like PO’s contentions. Carley, ¶248.

4. Claim 6

Iwabuchi meets claim 6 at least two ways.

a. Step [6.a]

6.a	The method of claim 1, comprising: forming a dielectric over the photodiode of the second substrate before bonding the first and second substrates; and
-----	---

“Dielectric” means “a material which is an electric insulator.” Ex. 1026, 184; Carley, ¶250.

i. insulator layer 20

With the interposer, supporting substrate, or DSP chip substrate as “first substrate,” Iwabuchi meets [6.a] because it describes forming insulator layer 20 over layer 12 (second substrate) and photodiode 14. Iwabuchi, [0144]-[0145], Fig. 10B; Carley, ¶251 ; *supra* § VI.B.1.d.i. Insulator layer 20 is a dielectric. Carley, ¶251.

Layer 20 is formed over the photodiode in layer 12 before bonding any “first substrate” (support substrate 30, interposer 3, or DSP chip, *supra* § VI.B.1.b (step [1.a])) to the second substrate (*supra* § VI.B.1.d.i (step [1.c])). Iwabuchi, [0146]; *supra* § VI.B.1.g.ii (step [1.e]); Carley, ¶252.

ii. supporting substrate 30

With the interposer or DSP chip substrate as “first substrate,” Iwabuchi meets [6.a] with supporting substrate 30 as the “dielectric.” Substrate 30 can be formed from “an insulating resin substrate.” Iwabuchi, [0146]. The insulating resin is a dielectric. Carley, ¶253. In this example substrate 30 is “formed” on the first substrate by bonding it to insulator layer 20 (Iwabuchi, [0146]) before bonding to the interposer or DSP chip. *Id.*

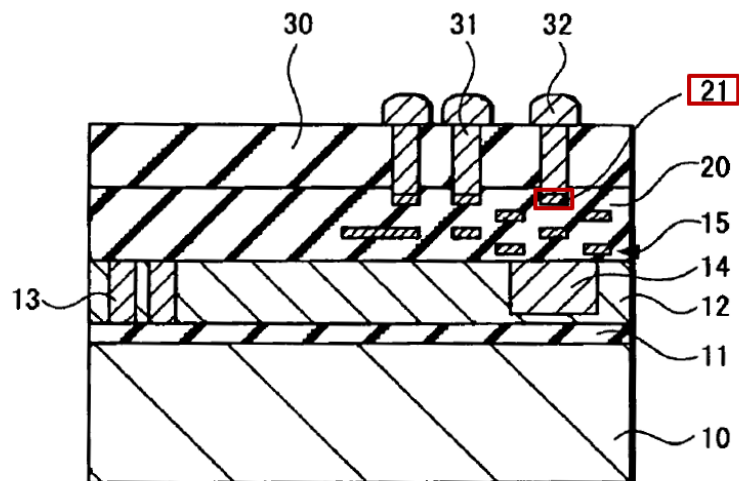
b. Step [6.b]

6.b	forming a metal pad in the dielectric.
-----	--

i. insulator layer 20

Iwabuchi describes forming “buried wiring layer 21” in “interlayer insulator 20.” Iwabuchi, [0145]. Wiring layer 21 connects to “substrate penetrating wiring 31” formed in substrate 30. *Id.*, [0148], Fig. 10F; Carley, ¶254.

FIG. 10F



POSAs would have understood that a conventional way to join wiring 21 to wiring 31 would have been to form wiring 21 into a metal pad in layer 20, for receiving metal plating forming wiring 31 (a via). Iwabuchi, [0148]-[0149]; Carley, ¶255.

ii. supporting substrate 30

Iwabuchi explains that “bump (micro-bump) 32 is a protrusion-like metal electrode **formed on a pad**...by a suitable method such as electrolytic plating.”

Iwabuchi, [0120]. POSAs would have understood this describes “forming a metal pad” in substrate 30 for receiving micro-bump 32, and that in any event forming a metal pad would have been obvious. Carley, ¶256.

5. Claim 8

The method of claim 1, wherein forming the circuitry including the metal interconnection comprises forming a metal and a plug over the first substrate.

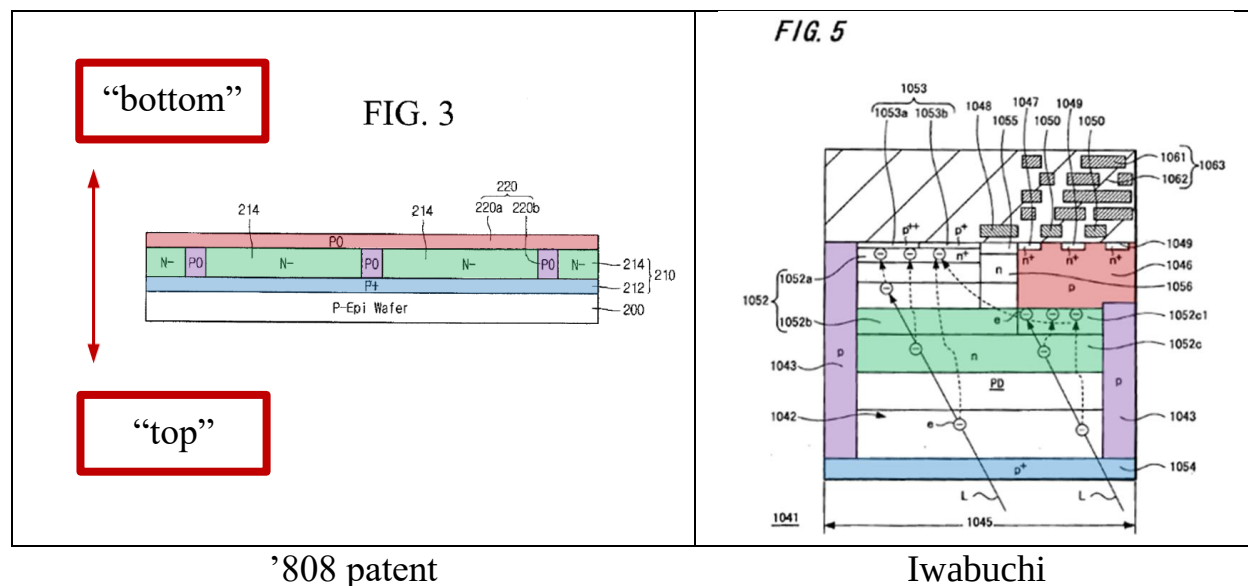
Iwabuchi meets claim 8 as explained *supra* § VI.B.1.c (step [1.b]). Carley, ¶257.

6. Claim 9

The method of claim 1, wherein the **second conduction type second ion implantation isolation layer** is disposed to directly contact on a top surface of the **second conduction type first ion implantation isolation layer** and a bottom surface of the **second conduction type conduction layer**.

Separation region 1043 is the “**second conduction type second ion implantation isolation layer**” (*supra* § VI.B.1.f.iii ([1.h.2])), and p region 1046 is the “**second conduction type first ion implantation isolation layer**” (*supra* § VI.B.1.f.ii(1) ([1.h.1])). Layer 1054 is the “**second conduction type conduction layer**” (*supra* § VI.B.1.d.ii ([1.g.1])). Region 1043 “is disposed to directly contact

on a bottom surface” of layer 1054 and a “top surface” of region 1046. Iwabuchi, Fig. 5; Carley, ¶¶258-261.



This spatial relation between separation region 1043, p^+ layer 1054, and p region 1046, follows the '808 patent treating the second substrate's front surface (e.g., the top of Iwabuchi Fig. 5 or '808 patent Fig. 3) as “down” when depicting 212, 220a, and 220b in Fig. 3. Carley, ¶262.

VII. GROUND 1B: IWABUCHI+MARUYAMA RENDERS OBVIOUS CLAIM 2

A. Maruyama

JP 2006-93587A (Ex. 1006, “Maruyama”), published April 6, 2006, is pre-AIA § 102(b) prior art. Maruyama describes a back-illuminated solid-state imager, Maruyama, [0001], with a unit pixel similar to the one described in Iwabuchi, including a backside p^+ layer 15 analogous to Iwabuchi p^+ layer 1054. *Id.*, [0010]-[0012], [0017], Fig. 2; Carley, ¶¶263-264.

Iwabuchi does not provide doping concentration or junction depth details. Carley, ¶270. POSAs building Iwabuchi’s design would have consulted Maruyama because Maruyama describes manufacturing a backside-illuminated photodetector similar to Iwabuchi’s. Carley, ¶271. Iwabuchi+Maruyama uses Maruyama’s junction depth to ensure blue-light sensitivity in Iwabuchi. *KSR v. Teleflex*, 550 U.S. 398, 417 (2007) (“[W]hen a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious.”); Carley, ¶272. This applies Maruyama’s known technique to Iwabuchi’s known device to yield predictable results. *KSR*, 550 U.S. at 416; Carley, ¶¶272-273. POSAs would have reasonably expected Iwabuchi+Maruyama to work as intended for the same reasons that Maruyama’s detector worked. Carley, ¶¶272-273.

C. Claim 2

The method of claim 1, comprising forming the **second conduction type conduction layer** at a junction depth of less than approximately 0.5 µm.

The ’808 patent does not explain “junction depth.” POSAs would have understood “junction depth” refers to the distance from a light incident surface to the furthest metallurgical junction between p and n type materials for a particular layer. *E.g.*, Ezaki, [0011], Figs. 2-3 (depth “h2b”); Carley, ¶274.

Iwabuchi+Maruyama renders claim 1 obvious for the same reasons as Iwabuchi alone. *Supra* § VI.B.1. In Iwabuchi+Maruyama, layer 1054 is the

“**second conduction type conduction layer**” (*supra* § VI.B.1.d.ii (step [1.g.1])

and has a junction depth less than 0.5 μm , *supra* § VII.B, rendering claim 2

obvious. Carley, ¶275.

VIII. GROUND 1C: IWABUCHI+SUGA RENDERS OBVIOUS CLAIM 7

A. Suga

Suga (Ex. 1007), published in 2002, is pre-AIA § 102(b) prior art. Suga describes “a low cost, ultra-high density, low-damage and low-temperature” process for “ultra-fine density flip chip” bonding. Suga, 105. “[T]he bonding pads on chip and bumps on substrate” are “bonded directly to each other only by contact at the room temperature” without solder. *Id.* “[T]he room temperature or low temperature flip chip bonding is achieved for Au [gold] bump to Au or Cu [copper] electrode by means of the surface activation treatment using RF plasma irradiation.” *Id.* Suga’s surface activation “cut down the bonding condition requirements and decreased the process cost.” *Id.*

B. Iwabuchi+Suga

Manufacturing Iwabuchi’s imager with gold bumps 32 on the sensor chip and copper landing pads on the interposer or DSP chip, using Suga’s surface activated bonding, is Iwabuchi+Suga.

1. Reasons to combine

Iwabuchi describes flip-chip bonding the sensor chip to the interposer or DSP chip. Iwabuchi, [0153]; Carley, ¶279. Iwabuchi provides a “micro-bump” for each pixel. Iwabuchi, [0140], [0192]; Carley ¶280. Iwabuchi “intends to provide a solid-state image pickup device in which the pixel size can be made very small[.]” Iwabuchi, [0048]; *id.*, [0046]-[0047]. POSAs would have understood that reducing pixel dimensions would **increase** the flip-chip bump density because smaller pixel dimensions would move bumps closer together. Carley, ¶¶280-281. The higher density bumps have smaller contact area for bonding. Carley, ¶282. Smaller contact area reduces the surface available for adhesion, which was known to decrease the bond reliability. Carley, ¶282. POSAs would have known that Suga’s plasma activation process would increase adhesion at the bump surface in Iwabuchi’s flip-chip bonding, which would increase bump-bond reliability. Suga, 105; Carley, ¶283. To use Suga’s methods, POSAs would have formed gold bumps 32 on the sensor chip, and copper metal lands on the interposer or DSP chip. Suga, 105; Carley, ¶284.

POSAs would have known that “conventional solder bump technology” had “several drawbacks due to high soldering temperature and multiple depositions of metal layers, thereby [providing] a high-cost technology[.]” Oh, 224; Carley, ¶285. Higher temperature can damage metallization. Dragoi, 147; Kim, 449; Carley, ¶285.

For these reasons, POSAs would have recognized Suga’s “low cost, ultra-high density, low-damage and low-temperature” process for “ultra-fine density flip chip” bonding would avoid stated drawbacks and lower process costs as reported in Suga. Carley, ¶286. This applies Suga’s known techniques to Iwabuchi’s manufacturing process yielding predictable results. KSR, 550 U.S. at 417; Carley, ¶287.

2. Reasonable expectation of success

POSAs would have expected Suga to reduce flip-chip bonding costs and increase bump adhesion and reliability, providing high-density flip-chip bonding at lower temperatures, for the same reasons that Suga achieved these outcomes. Carley, ¶288. Thus, POSAs would have expected Suga’s methods to improve the bump bonding in Iwabuchi in a similar way. *Id.*

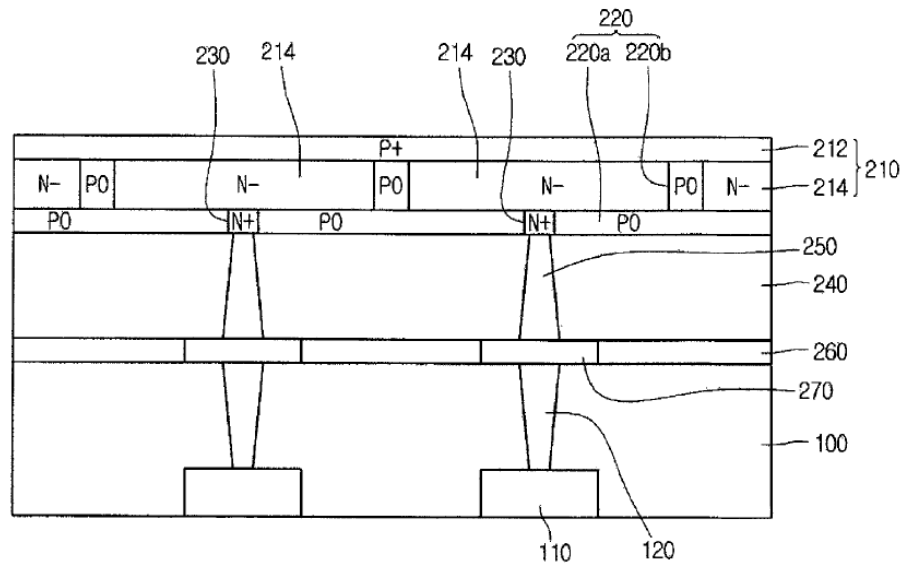
C. Claim 7

The method of claim 1, wherein bonding the first substrate to the second substrate comprises contacting the first substrate and the second substrate with each other and performing activation by plasma.

1. “contacting substrate[s]”

The '808 patent shows contacting a “first substrate 100” with metal and dielectric layers formed over “second substrate 200.” Ex. 1001, 4:25-35, Figs. 7-8; Carley, ¶289. The specification describes the same intervening layers between substrates as discussed with “bonding.” Ex. 1001, 4:8-35, Figs. 5-8; *Supra* § VI.B.1.g.ii (step [1.e]); Carley, ¶290. It discloses “contacting first substrate 100 and second substrate 200 with each other” by contacting dielectric 260 and metal 270—formed on dielectric 240 and metal 250—to a surface of substrate 100. Ex. 1001, 4:31-35, Fig. 8. Carley, ¶291.

FIG. 8

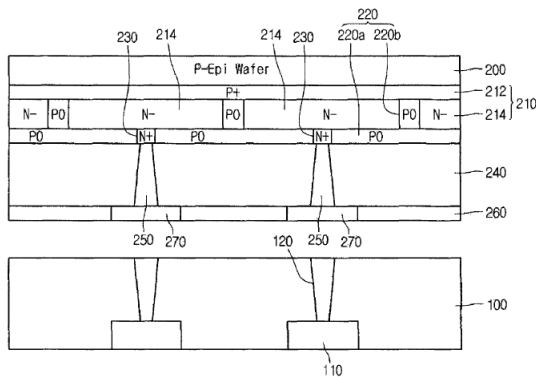


To cover the patent’s sole “contacting” embodiment, either (1) “contacting substrates” must encompass electrically contacting substrates or (2) “substrate” must encompass layers and metal formed on, or over, an initial substrate (or both). *Vitronics*, 90 F.3d at 1583; *Kaufman*, 34 F.4th at 1372.

2. Analysis

Iwabuchi+Suga meets claim 1 for the same reasons that Iwabuchi alone meets claim 1. *Supra*, § VI.B.1; Carley, ¶293. The sensor chip includes the “second substrate.” *Supra*, § VI.B.1.b.iii. Iwabuchi describes bump-bonding the sensor chip to the interposer (*supra* § VI.B.1.g.ii(1)), or the DSP chip (*supra* § VI.B.1.g.ii(3)). POSAs would have implemented Iwabuchi’s flip-chip bonding with Suga’s bumpless bonding. Carley, ¶294.

FIG. 7

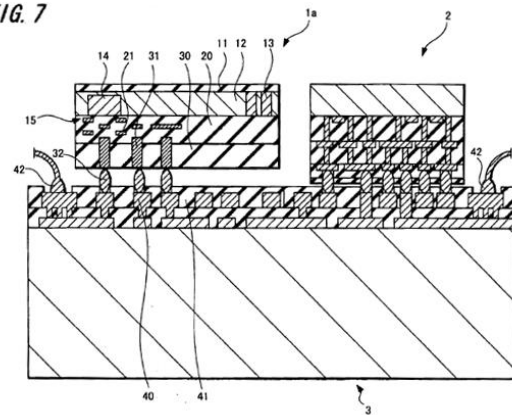


a. contacting

Flip-chip bonding the sensor chip to the interposer, or DSP chip, is “contacting the first substrate and second substrate with each other.” Carley, ¶295. Flip-chip bonding was understood as physically and electrically joining substrates. *E.g.*, Dery, 2:8-11 (“The IC chip is joined to a chip carrier via a plurality of solder bumps electrically connecting a plurality of contact pads on the IC chip to corresponding contacts on the chip carrier.”); Carley, ¶296. Suga’s method gives the same result. Carley, ¶296.

Flip-chip bonding electrically contacts the photodiodes in layer 12 (second substrate) with wiring 40 on the interposer (Iwabuchi, Fig. 7; Carley, ¶297) and with the metal landings replacing the bumps on the DSP chip. *Supra* §§ VI.B.1.c (step [1.b]); VI.B.1.g.ii(3) (step [1.e]). Carley, ¶297. Flip-chip bonding the sensor chip to the interposer, or the DSP chip, physically “contacts” the “first” and “second” substrates “with each other.” Carley, ¶298.

FIG. 7



In each case “substrate” encompasses gold micro-bumps 32 formed over layer 12 (“second substrate”); copper wiring 40 formed on the interposer (*supra* § VI.B.1.c.i (step [1.b])) and copper landings formed over the DSP chip. *Supra* §§ VI.B.1.c.ii (sensor chip), VI.B.1.c.iii (DSP chip); Iwabuchi Fig. 7; Carley, ¶299.

b. activation

Suga discloses bumpless flip-chip bonding with a “Surface Activation Bonding” process in which the “flip chip bonding is achieved for Au bump to Au or Au to Cu electrode by means of the surface activation treatment using RF plasma irradiation.” Suga, 105. Carley, ¶300. This is “performing activation by plasma.” Carley, ¶300. Iwabuchi+Suga renders obvious claim 7. Carley, ¶301.

IX. GROUND 2A: LEE+MASAGAKI+SHIRAIWA RENDERS OBVIOUS CLAIMS 1, 4-6, AND 8-9

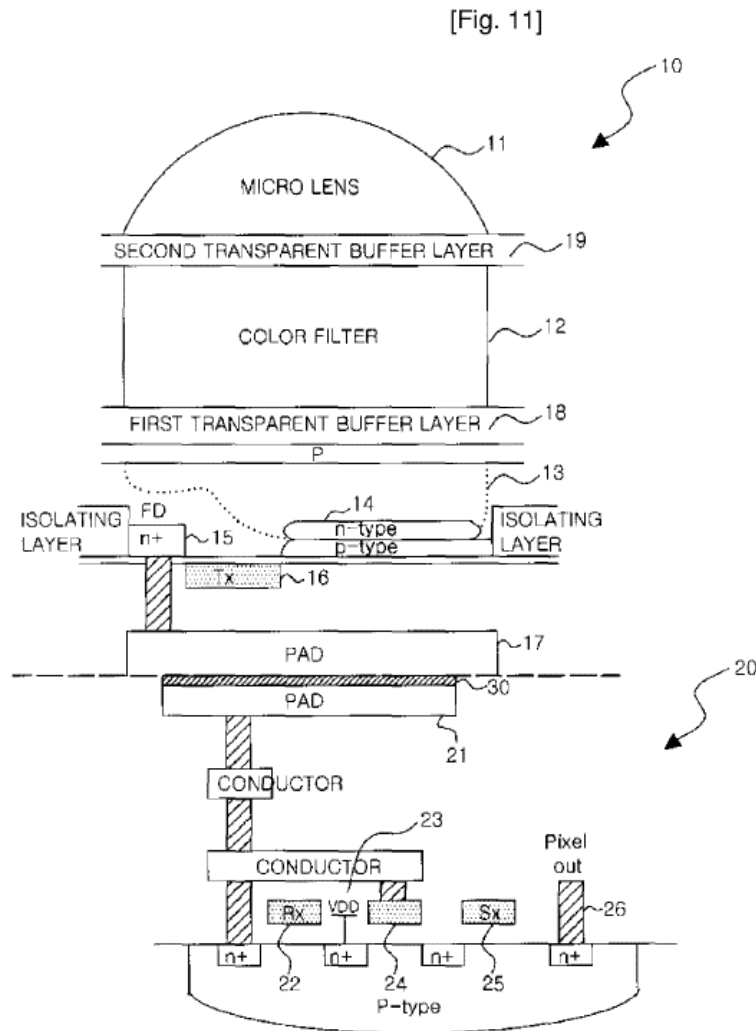
A. References

Lee, Masagaki, and Shiraiwa each published more than a year before December 28, 2008 and are pre-AIA § 102(b) prior art.

1. Lee

PCT Publication WO 2006/109937 (Ex. 1008, “Lee”) published October 19, 2006. Lee describes manufacturing a solid-state imager with a “3D structure” by bonding a sensor wafer to a circuit wafer. *Id.*, [14]-[15]. The sensor wafer provides a unit pixel array. *Id.*, [10]; Carley, ¶303. Each backside-illuminated pixel has a photodiode and a transfer transistor. Lee, [1], [13]-[14], [29], [38], Fig.

10; Carley, ¶304. Lee calls this a “separation type unit pixel.” Lee, [13]. Lee locates remaining readout transistors, and additional circuitry, on a second wafer. *Id.*, [14], [35]; Carley, ¶305. Interconnections including vias and conduction pads take the image signal to the second wafer from a floating diffusion. Lee, Abstract, Figs. 10-11, claim 2; Carley, ¶306.



2. Masagaki

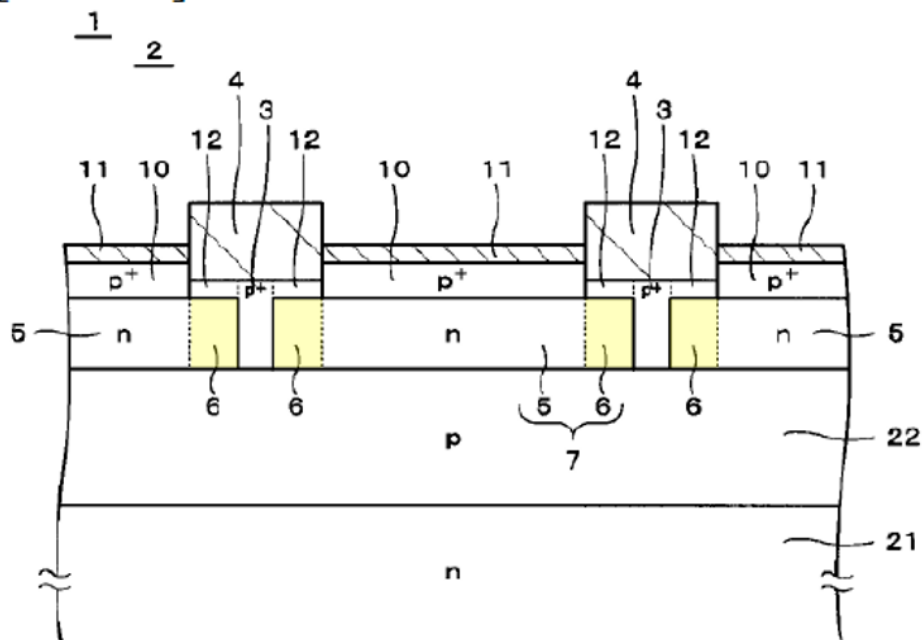
Japanese Patent Publication JP 2006-303385 (Ex. 1009, “Masagaki”)

published November 2, 2006. Masagaki’s Figure 11 discloses a prior art unit pixel

almost identical to that in Lee (shown side-by-side *infra* § IX.B). Masagaki describes improving the prior art unit pixel with a photodiode, formed in a “silicon semiconductor substrate,” having a charge storage region extended laterally below a pinning or planar isolation layer, bounded by a “device separation region.”

Masagaki, [0009], [0018], [0020], Fig. 10, claim 1; Carley, ¶308. Masagaki Figure 10 provides a cross-section perpendicular to the cross-section shown in its Figure 11, and shows region 6 extending charge storage region 5 below isolation layer 12 to adjacent pixel separation region 3. Carley, ¶309.

[FIG. 10]

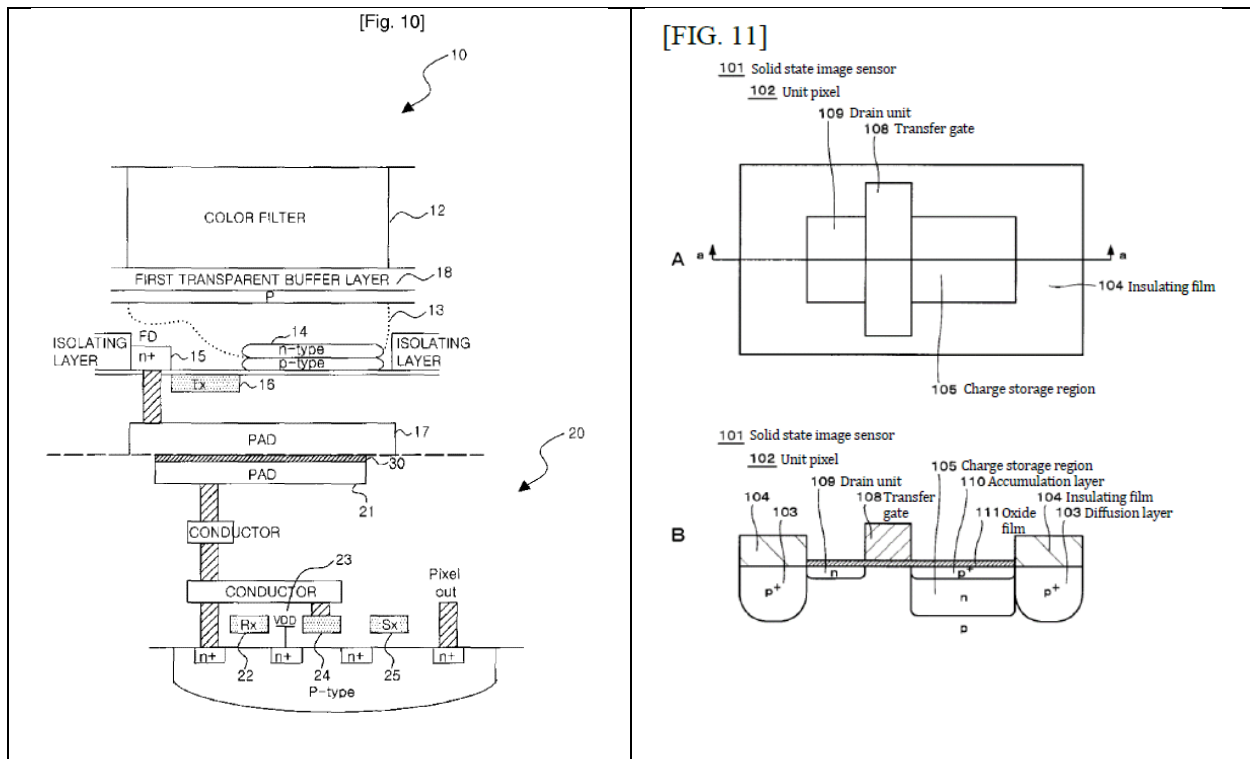


Like the '808 patent, Masagaki describes forming layers 12 and 3 by ion implantation, replacing prior art STI with “an inter-device separation structure made up of a diffusion layer” to avoid dark-current-generating crystal defects.

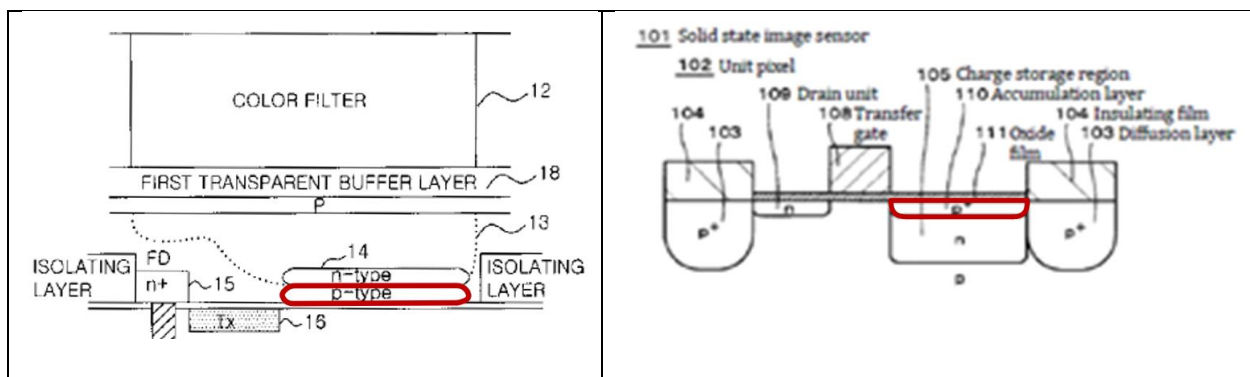
Masagaki, [0003] (“an inter-device separation region structure...replaces STI”); *id.* [0002], [0037], [0040]; Ex. 1001, 2:57-62; Carley, ¶¶310, 312-314. *See also* Masagaki, [0029]. Extending the charge storage region 5 with region 6 mitigates reduced charge storage associated with reducing pixel dimensions, leading to “a worsened S/N ratio” and “decreased dynamic range.” Masagaki, [0007]-[0008]; Carley, ¶310. Forming the device separation region by ion implantation facilitates extending the charge storage region in Masagaki. Carley, ¶311.

3. Shiraiwa

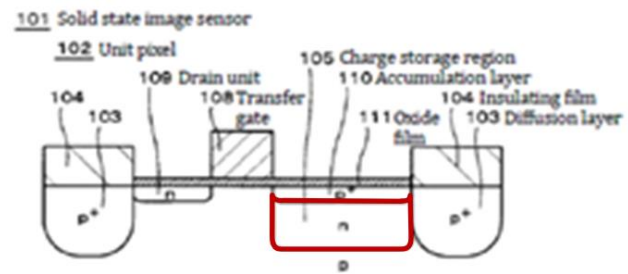
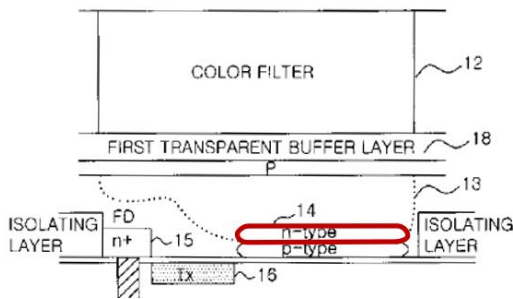
Japanese Patent Publication No. JP 2005-353996 (Ex. 1010, “Shiraiwa”) published December 22, 2005. Shiraiwa describes thinning the semiconductor substrate’s backside without using an SOI wafer’s oxide layer as an etch stop. Shiraiwa, [0014]-[0024]. Figure 5E shows thinning silicon substrate 22 by setting end point detection portion 42 that defines the thinning stopping point at the same thickness as the photodiode. *Id.*, [0037], Fig. 5E.



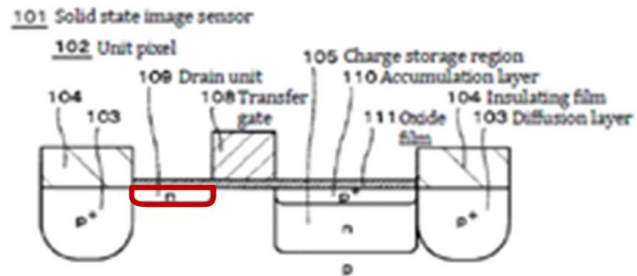
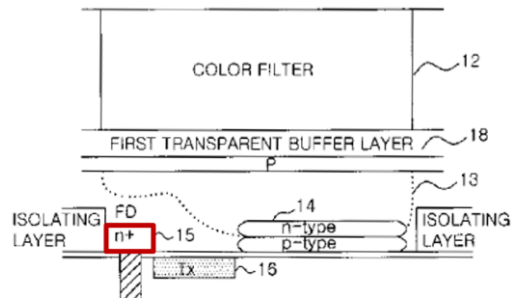
Both Lee and Masagaki disclose a p-type pinning layer (not numbered in Lee, 110 in Masagaki) (Carley, ¶318),



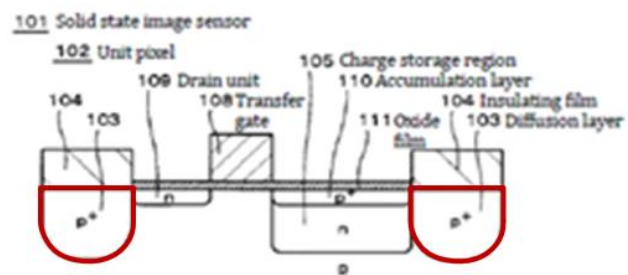
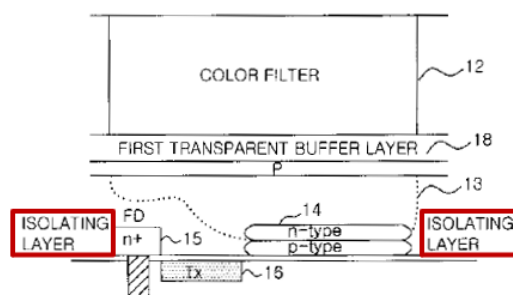
n-type conduction layer 14 (Lee) and 105 (Masagaki) (Carley, ¶319),



transfer transistor with gate (16 (Lee), 108 (Masagaki)) and n-type floating diffusion (15 (Lee), 109 (Masagaki)) (Carley, ¶320),



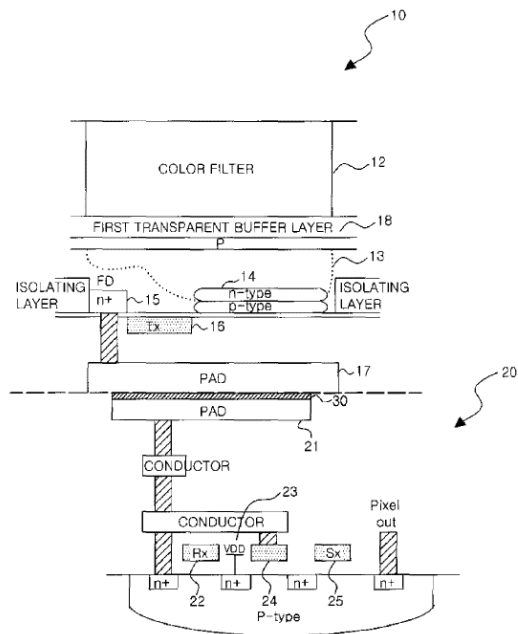
and lateral isolation layer (“isolating layer” (Lee), 103 (Masagaki)) (Carley, ¶321).



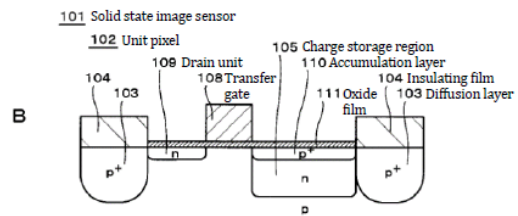
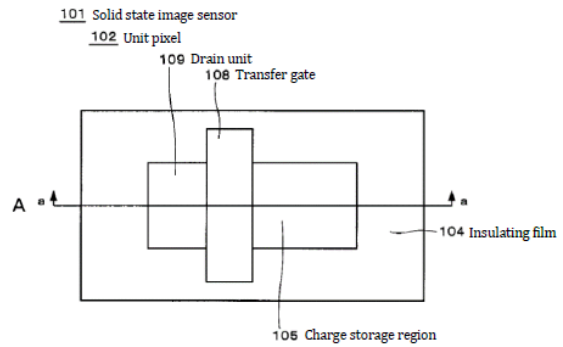
E.g., along the cross-sectional views in Lee Fig. 10 and Masagaki Fig. 11, Lee’s backside-illuminated detector provides the same photodetector features as the prior art frontside-illuminated detector in Masagaki Fig. 11. Carley, ¶322. Below shows the correspondence between Lee’s separation unit pixel and the

Masagaki unit cell, which is inverted to correspond to the backside-illuminated implantation.

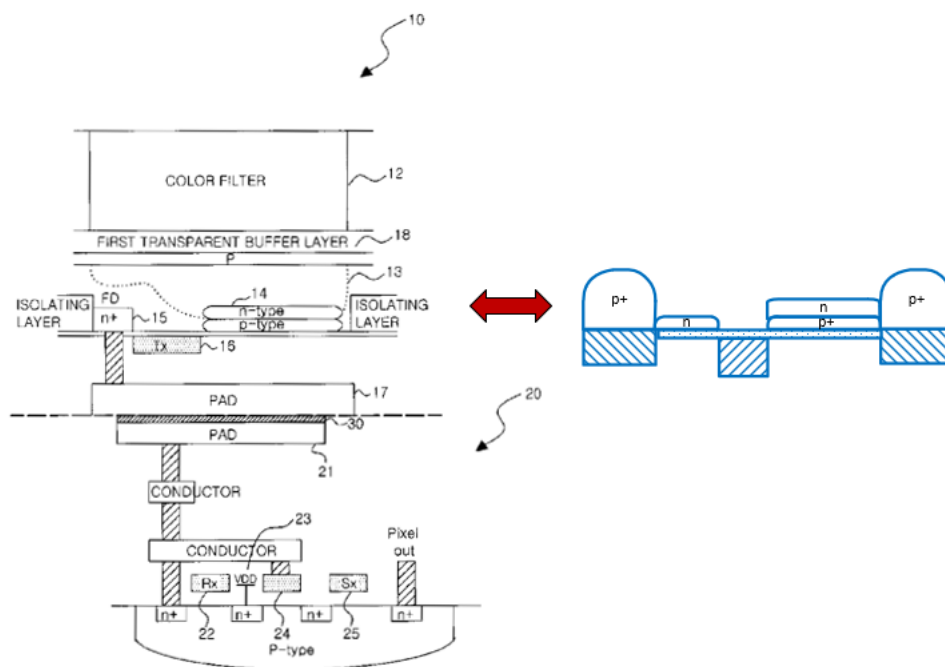
[Fig. 10]



[FIG. 11]

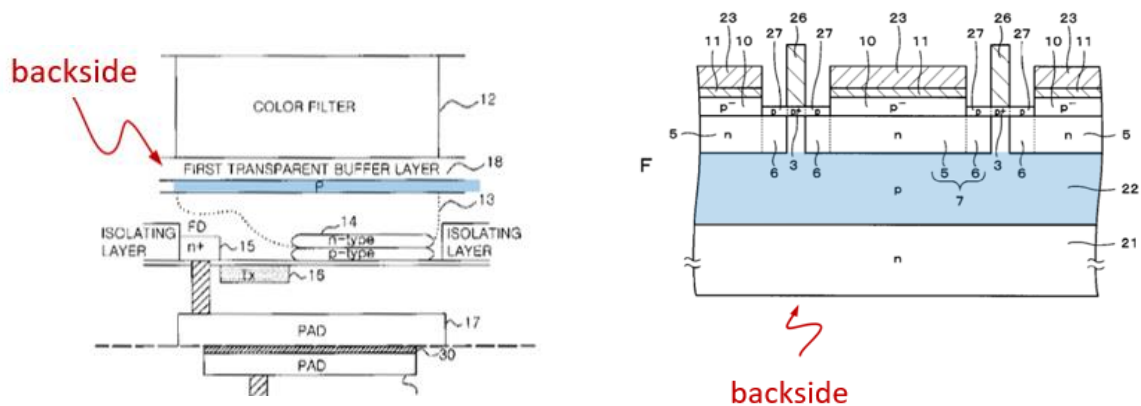


[Fig. 10]



Lee+Masagaki+Shiraiwa is Lee's 3D imager. It replaces Lee's separation-type unit pixel conduction and isolation layers, which correspond to the photodetector structure in Masagaki's prior art Figure 11, with Masagaki's improved device and its extended charge storage region extension. It forms the photodetector, using Masagaki's processes, as described for "the unit pixels [that] are adjacent to each other via the device separation region." Masagaki, [0034]; Carley, ¶325. The combination does not use Masagaki's insulating film 4, or etching to place it, because the frontside surface abuts the insulator layer providing the gate dielectric for transfer transistor 15, between the p-type pinning layer and the dielectric that contains pad 17 in Lee's 3D imager. Carley, ¶326.

In Lee+Masagaki+Shiraiwa's unit pixel, backside p-layer (Lee, Fig. 10) corresponds to Masagaki p-type layer 22 (Masagaki Figure 10) after thinning using Shiraiwa's methods to remove the lower portion of the sensor wafer substrate 21. Shiraiwa, [0037]; *accord* Lee, [52], Fig. 12 (step S540); Shiraiwa, [0030], Fig. 2 (describing corresponding p⁺ accumulation layer 54); Carley, ¶327.



The unit pixel in Lee+Masagaki+Shiraiwa is made using Masagaki's methods to form the photodiode and isolation layers. Carley, ¶328. "[N]ormal processes are used to form the drain region 9 of the [transfer] transistor [*e.g.*, the floating diffusion] and the accumulation layer 10[.]" Masagaki, [0040]; Carley, ¶328. Lee+Masagaki+Shiraiwa uses the floating diffusion and transfer transistor in both Lee and Masagaki, and the floating diffusion connects to Lee's second wafer through a via to pad 17 as in Lee Figure 10. Carley, ¶328.

1. Reasons to combine

POSAs would have had several reasons to combine Lee, Masagaki, and Shiraiwa. Carley, ¶329. As discussed above, Lee and Masagaki disclose almost identical structures, excepting the novel charge storage region extension in Masagaki that would improve Lee for the same reasons it improves Masagaki's near-identical structure. Carley, ¶330. Both Lee and Masagaki are concerned with mitigating the loss in photodiode sensitivity when reducing pixel dimensions. Carley, ¶331. Both recognized that "the amount of available electric charge

decreases when the size of the photodiode decreases,” and this adversely affected imaging. Lee, [8] (“The amount of available electric charge of the photodiode is a basic feature of determining a dynamic range of the image sensor, and the decrease of the amount of available electric charge directly affects the image quality...”); Masagaki, [0007] (“[A]rea reduction of a photodiode leads to a decreased charge storage amount and a worsened S/N ratio and causes a problem of worsened imaging characteristics of the image sensor such as a decreased dynamic range.”); Carley, ¶332.

Lee addresses this issue with a “separation type unit pixel” in which “sensitivity drops far less...than a conventional case in the manufacturing of a miniature pixel.” Lee, [12]. Masagaki’s objective was “to provide a solid state image sensor wherein a unit pixel can be miniaturized without sacrificing an effective area of a charge storage region[.]” Masagaki, [0008]. POSAs would have understood that Masagaki’s solution—extending the charge storage region—would improve the sensitivity of Lee’s similar photodiode structure, and further mitigate the loss of sensitivity associated with reducing pixel dimensions. Carley, ¶¶333-334.

Both Lee and Shiraiwa describe wafer-scale backside-thinned device fabrication. While Lee describes reducing wafer thinning by backside etching or grinding, Fig. 12 (S540), Shiraiwa provides precise substrate thickness at lower

cost and with less planar variation than obtained when using the oxide layer in SOI wafers as an etch stop. Shiraiwa, [0021]-[0022]. POSAs would have used Shiraiwa because it gives more detailed process information on backside thinning than Lee. Carley, ¶335.

In short, POSAs would have recognized that Masagaki's manufacturing techniques and pixel including an extended charge storage region below and adjacent ion-implanted diffusions could be used to improve the charge storage in Lee's separation unit pixel in the same way that it improved charge storage in Masagaki's unit pixel, further mitigating adverse effects of pixel miniaturization on signal to noise ratio, dynamic range, and image quality. *KSR*, 550 U.S. at 417; Carley, ¶336. Using Shiraiwa's backside thinning would have applied known backside-thinning methods to improve the device. Carley, ¶337.

2. Reasonable expectation of success

Several factors would have given POSAs a reasonable expectation of success in combining Lee, Masagaki and Shiraiwa. Carley, ¶338. Lee demonstrates that Masagaki's architecture was compatible with Lee's unit pixel because, other than the illumination surface, Lee uses the same prior art pixel features that Masagaki modified to improve charge storage with shrinking pixel dimensions. *Id.* Both Lee and Shiraiwa describe process steps, like backside thinning, associated with making backside-illuminated detectors. Lee, [52]-[55], Figs. 8, 11; Shiraiwa, [0027]-[0028], Figs. 1-2; Carley, ¶339. As Lee demonstrates, it was well-known that photodetector structures for a frontside detector like Masagaki could be implemented in a backside-illuminated architecture like Lee's unit pixel. *E.g.*, Pain2005, 35; Ex. 1038; Lee, Fig. 12 (step S530); Carley, ¶340.

Because Lee describes separately fabricating the first and second wafers before bonding them, POSAs would have reasonably expected that forming pixel structures using Masagaki’s known methods, and thinning the substrate using Shiraiwa’s more detailed process steps with Lee, would succeed because this would use known and predictable fabrication methods in known and conventional ways. Carley, ¶341. Moreover, since Lee+Masagaki+Shiraiwa has the same transfer transistor, floating diffusion, and vias that worked in Lee, POSAs would have expected the resulting 3D architecture would work just like Lee. Carley, ¶342.

C. Claim analysis

1. Claim 1

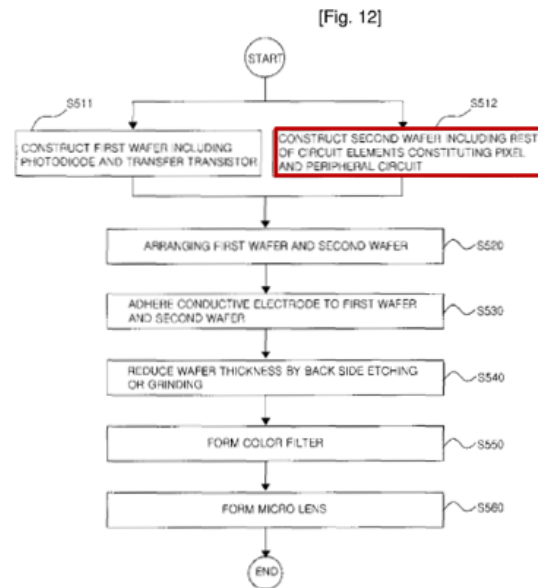
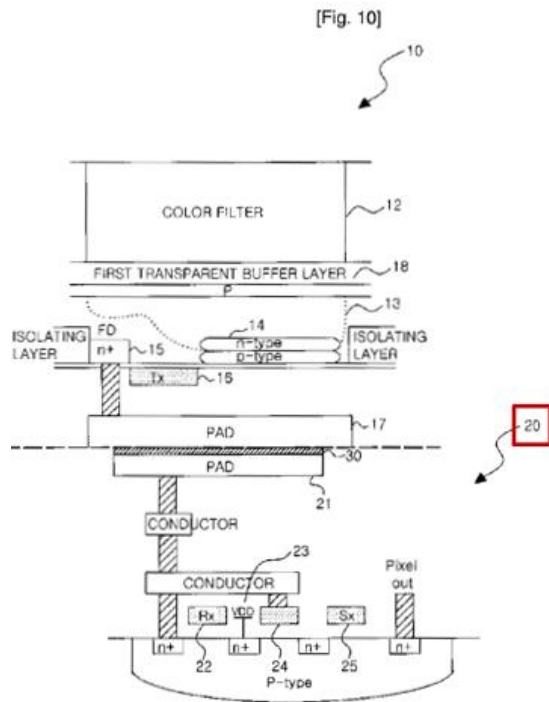
a. Preamble

Lee+Masagaki+Shiraiwa meets the preamble because Lee describes methods for manufacturing a three-dimensional (3D) imager. Lee, [21], claim 7; Carley, ¶343.

b. Step 1.a

1.a	providing a first substrate;
-----	------------------------------

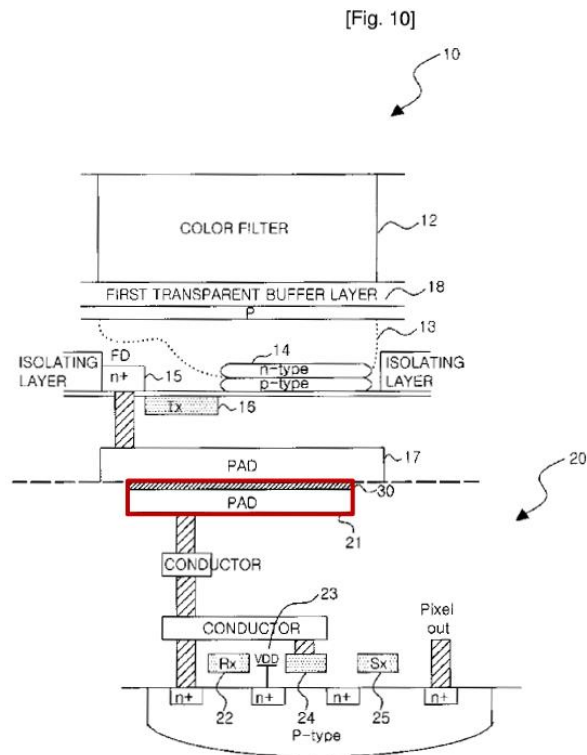
Lee+Masagaki+Shiraiwa meets [1.a] because Lee describes providing a “second wafer” with circuit elements. Lee, [14], [33], [35], Figs. 10 (wafer 20), 12 (step S512). Lee’s “second wafer” is the “first substrate.” Carley, ¶344.



c. Step 1.b

1.b	forming circuitry including a metal interconnection over the first substrate;
-----	---

Lee+Masagaki+Shiraiwa meets [1.b] because Lee describes forming “conductive pad 21” and other circuitry over “second wafer 20.” Lee, [15], [41]-[42], [47], Figs. 10, 12 (S512); Carley, ¶345. The conductive pads 17 (on “first wafer 10”) and 21 (on “second wafer 20”) are “for external connection,” *e.g.*, interconnection. Lee, [36]; Carley, ¶346. POSAs would have understood that “conductive pads” 17 and 21 conventionally comprised a metal like copper or gold because this was a standard way to provide surface contacts for solid-state devices and interconnection in wafer-to-wafer bonding. Carley, ¶347. POSAs would have found it conventional to form conductive pad 21 from metal. *Id.*



d. Conduction layers

i. Step [1.c]

1.c	forming a photodiode in a crystalline semiconductor layer of a second substrate;
-----	--

Lee+Masagaki+Shiraiwa meets [1.c]. Lee discloses forming a photodiode in a semiconductor substrate comprising the first sensor wafer. Lee, [1], [13]-[14], Fig. 10; Carley, ¶348. Masagaki describes forming a photodiode in a “silicon semiconductor substrate” with a charge storage region extended laterally below a pinning or planar isolation layer and bounded by a “device separation region.” Masagaki, [0009], [0018], [0020], Fig. 10, claim 1; Carley, ¶349.

While neither Lee, Masagaki, nor Shiraiwa describe their substrate as “crystalline,” POSAs would have understood that their discussion of SOI wafers, CMOS imagers, and forming transistors in the photodetector meant Lee, Masagaki, and Shiraiwa each formed photodiodes in a crystalline semiconductor layer such as layer 12 in Iwabuchi. *Supra*, § VI.B.1.d.i (step [1.c]); Carley, ¶350.

Shiraiwa describes forming photodiodes in silicon substrates for CMOS solid-state imagers with readout transistors similar to Iwabuchi’s detector. Shiraiwa, [0001], [0027], [0030], [0037], Fig. 2. Shiraiwa’s silicon substrate replaces the top layer of prior art SOI wafers, which were known to be “high-quality single-crystalline material that is suitable for high-performance and high-density integrated circuits.” Sze, 343-344; Shiraiwa, [0014], [0022]; Carley, ¶351.

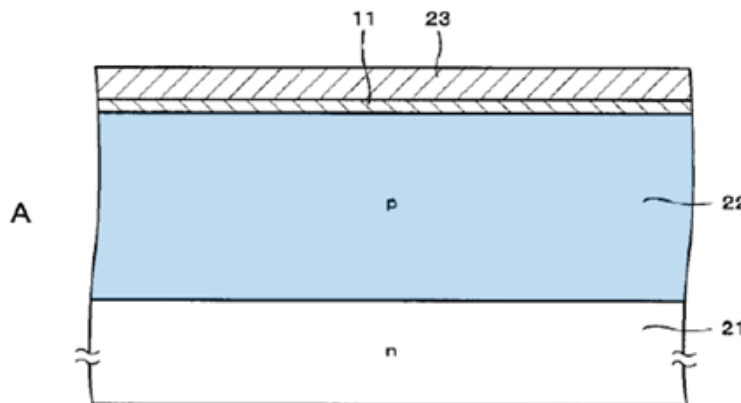
Masagaki describes a CMOS solid-state image sensor with conduction layers “formed on a silicon semiconductor substrate.” Masagaki, [0018]-[0019]; Carley, ¶352. Lee describes forming a transfer transistor in the unit pixel containing a photodiode. Lee, [46], Fig. 10; Carley, ¶353. It was well-known and conventional to form CMOS imagers and CMOS transistors in crystalline semiconductor substrates and this would have been obvious given the disclosures in Lee, Masagaki, and Shiraiwa. Carley, ¶354.

ii. Steps [1.g], [1.g.1]

1.g	wherein forming the photodiode comprises:
1.g.1	forming a second conduction type conduction layer in the crystalline semiconductor layer; and

Lee+Masagaki+Shiraiwa meets [1.g] and [1.g.1]. Masagaki describes forming a photodiode comprising p-type layer 22 on silicon substrate 21 as the first step in making the unit pixel. Masagaki, [0035], Fig. 7; Carley, ¶355. The p-type layer 22 is the [1.g.1] second conduction type conduction layer. *Id.*

[FIG. 7]



iii. Step [1.g.2]

1.g.2	forming a first conduction type conduction layer over the second conduction type conduction layer ,
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Lee+Masagaki+Shiraiwa meets [1.g.2]. After forming p-layer 22, Masagaki describes forming “charge storage region” n-type layer 7. Masagaki, [0038]-[0039], Fig. 9F; Carley, ¶356. This comprises “main portion 5” and “extended portion 6.” Masagaki, [0031], Fig. 9F; Carley, ¶357. The n-type charge storage

region 7, including extended region 6, is the [1.g.2] “first conduction type conduction layer.” Relative to the backside surface, layer 7 is “over” layer 22 just like the '808 patent describes layer 214 is over layer 212. *Compare* Masagaki, Fig. 9F, *with* Ex. 1001, Fig. 2; Carley, ¶357.

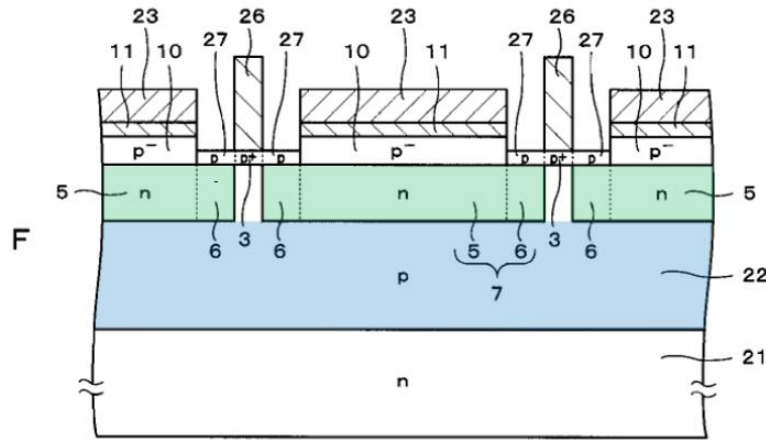
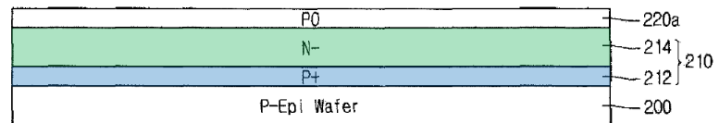


FIG. 2



e. Conduction layer fabrication sequence

As just explained, Masagaki describes forming layer 22 (step [1.g.1]) before forming layer 7 (step [1.g.2]). Carley, ¶358.

f. Isolation layers

i. Step [1.d]

1.d	forming an ion implantation isolation layer in the photodiode;
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Lee+Masagaki+Shiraiwa meets [1.d] as explained for steps [1.h.1] and [1.h.2]. Carley, ¶359.

ii. Step [1.h.1]

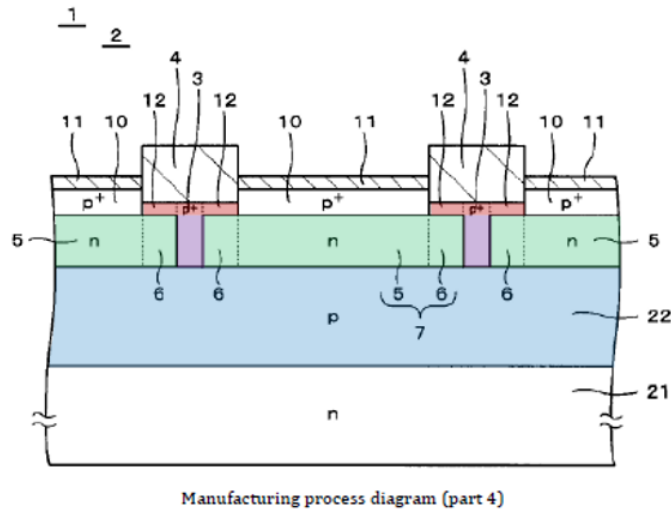
1.h.1	wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer over the first conduction type conduction layer ,
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Lee+Masagaki+Shiraiwa meets [1.h.1]. Carley, ¶360. Masagaki describes forming “extending diffusion layer 12” by p-type (“second conduction type”) ion implantation after having formed the [1.g.2] conduction layer. Masagaki, [0040] (describing “implantation of a p-type impurity” to form “extended diffusion layer 12 having approximately the same p-type impurity concentration as the diffusion layer 3[.]”); Carley, ¶360.

Moreover, “accumulation layer 10 suppresses dark current due to an interface state” and also meets [1.h.1]. Masagaki, [0020]; Carley, ¶361. POSAs would have formed layer 10 by ion implantation after forming n-layer 5.

Masagaki, [0033]; Mann, [0024]; Carley, ¶361.

[FIG. 10]



Masagaki requires the layer 12 implant **after** forming n-type region 6 because the n-type implant to form region 6 for step [1.g.2] “decreased” the p-type impurity concentration in the region of layer 12. Masagaki, [0040]; Carley, ¶362. Layers 10 and 12 comprise an isolation layer because they isolate the n-type charge storage region 6 from the frontside interface (with gate dielectric in Lee Fig. 10), which contains interface states that cause white spots in imaging. Masagaki, [0018]-[0020], Fig. 10; Carley, ¶363. Masagaki forms layers 10 and 12 “over” layer 7, *e.g.*, the first conduction type conduction layer, *supra* § IX.C.1.d.iii (step [1.g.2]), and in particular forms layer 12 “over” extended portion 6. Masagaki, Fig. 10; Carley, ¶364. Layer 12 has the same conductivity as layer 3. Masagaki, [0040]; Carley, ¶364. For step [1.h.1], the “second conduction type first isolation layer” is *the planar top of the “T” provided by layers 12 and the top of layer 3* as

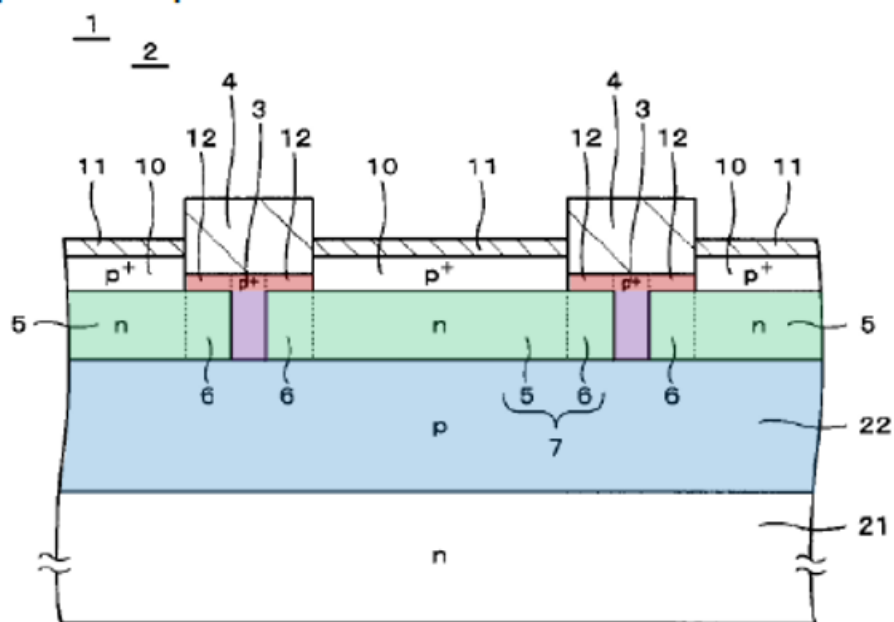
shaded red in annotated Fig. 10. Carley, ¶365. In the alternative, the “second conduction type first isolation layer” also includes layer 10. Carley, ¶366.

iii. Step [1.h.2]

1.h.2	wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.
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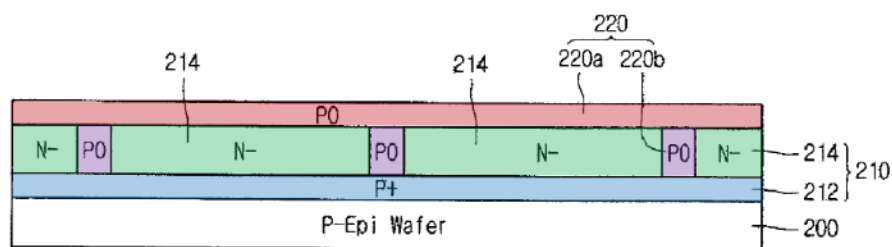
Lee+Masagaki+Shiraiwa meets [1.h.2]. Masagaki describes forming “the diffusion layer 3 that ultimately constitutes the device separation region” by p-type ion implantation. Masagaki, [0037]; Carley, ¶367. POSAs would have understood that Masagaki’s description of forming separation region 3 by “ion implantation that increases the depth of the diffusion layer 3” or “several implantations in the depth direction” in a first embodiment of Fig. 4 (Masagaki, [0030]) also applied to the embodiment shown in Figures 9 and 10, because the two embodiments have the same pixel separation region 3, formed in the substrate, and extending to the depth of the charge storage layer 7. Masagaki, Figs. 4, 6, 9, 10; Carley, ¶368.

[FIG. 10]



Manufacturing process diagram (part 4)

FIG. 3



Masagaki forms diffusion layer 3 “at an interface between pixels of the photodiode” because it separates adjacent pixels exactly like 220b in the ’808 patent, and like the “P-well” labeled “220b” in PO’s contentions. Masagaki, [0034] (“This embodiment describes a manufacturing method in a situation wherein only the unit pixels are adjacent to each other via the device separation

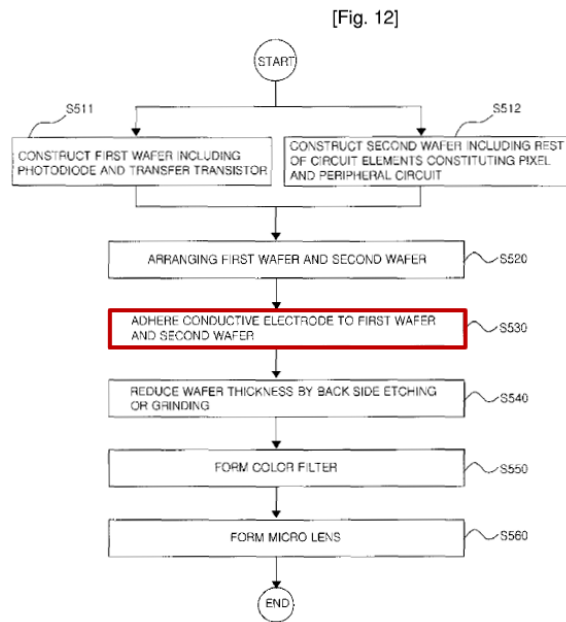
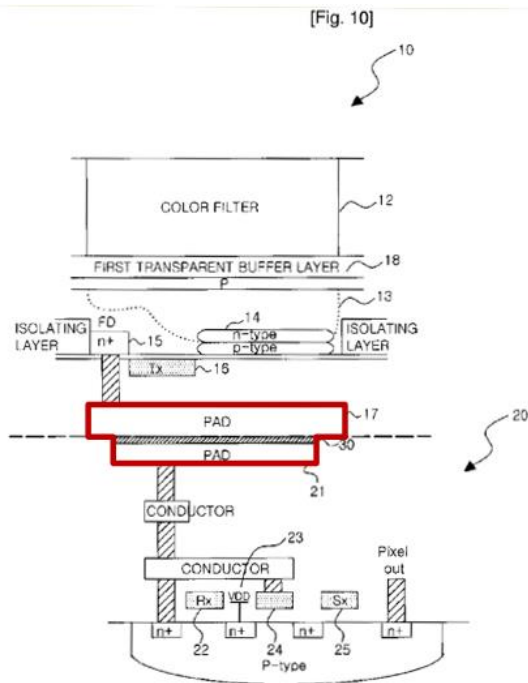
region.”); Ex. 1001, Fig. 3; IC-A1, 27; *supra* § VI.B.1.f.iii (discussing IC-A1, 27); Carley, ¶369. Thus, forming layer 3 meets [1.h.2]. Carley, ¶369.

g. Step 1.e

1.e	bonding the first substrate to the second substrate to connect the photodiode to the metal interconnection; and
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i. “bonding”

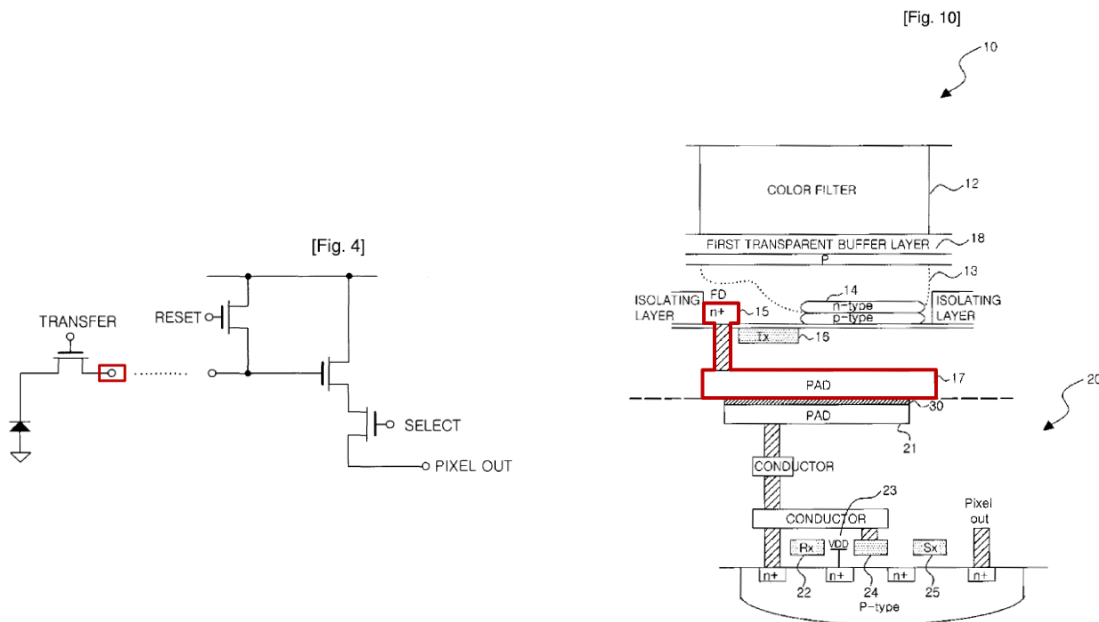
Lee+Masagaki+Shiraiwa meets [1.e] because Lee describes bonding the first wafer to the second wafer. Carley, ¶370. “[T]here is provided a manufacturing method...comprising...(d) adhering a pad of a unit pixel on the first and second wafers arranged up and down[.]” Lee, [15]; *id.*, [51], [53] (describing thinning step “[a]fter the first wafer is adhered to the second wafer[.]”), Figs. 10 & 12 (step S530); Carley, ¶370. Moreover, it was well-known and conventional to bond wafers by adhering opposing metal contacts. Exs. 1027, 1030; Carley, ¶371.



ii. “bonding... to connect”

Based on the PO’s contentions, *supra* § VI.B.1.g.i (step [1.e]), Lee+Masagaki+Shiraiwa further meets [1.e] because Lee describes conductive pad 21 and the second wafer pixel readout circuitry electrically connecting to the floating diffusion (“FD”) 15 in each pixel. Lee, [39] (“[T]he floating diffusion area 15 connected to the external circuit is connected to the conductive pad 17”), Abstract (“a first wafer...includes a photodiode, a transfer transistor, a node of a floating diffusion area...and a pad connecting the floating diffusion area and the transfer transistor to an external circuit”), Figs. 4, 10, claim 1; Carley, ¶372. The FD “transfers optical electric charge included in the photodiode[.]” Lee, [13]; *id.*,

[29] (“A transfer transistor 6 connects and separates the floating diffusion area 5 and photodiode 4.”), Fig. 8; Carley, ¶¶373-375.



h. Step 1.f

1.f	removing a lower portion of the second substrate to expose the photodiode,
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Lee+Masagaki+Shiraiwa meets [1.f] because Lee describes thinning and Shiraiwa describes removing the silicon substrate’s lower portion to expose the photodiode. Shiraiwa, [0037], Fig. 5E, *supra* § IX.A.3; Lee, [52]-[53], [60]-[61], Figs. 12 (step S540), 14, claim 7 (step (e)) (describing thinning “the back side of the first wafer...to reduce the wafer thickness”); Carley, ¶376. This was conventional. Gouscha, 4:33-63; Iwabuchi, [0065], [0150], Fig. 10G; Carley, ¶376.

* * *

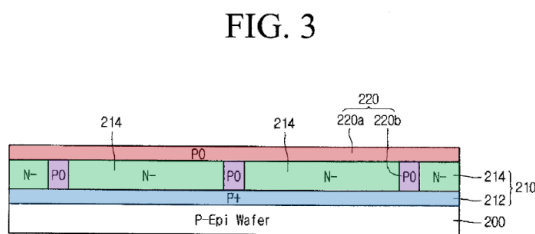
Taken as a whole, claim 1 would have been obvious over

Lee+Masagaki+Shiraiwa. Carley, ¶377.

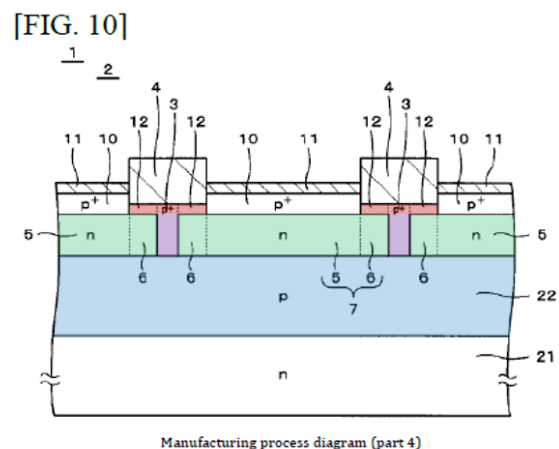
2. Claim 4

The method of claim 1, comprising forming the ion implantation isolation layer over at least one of a side of the photodiode and a bottom of the photodiode.

Lee+Masagaki+Shiraiwa renders claim 4 obvious because Masagaki forms diffusion 3—the [1.h.2] ion implantation layer—“over a side of the photodiode” in exactly the same way as layer 220b in the '808 patent. Masagaki, Fig. 10; Ex. 1001, Fig. 3; Carley, ¶378.



'808 patent



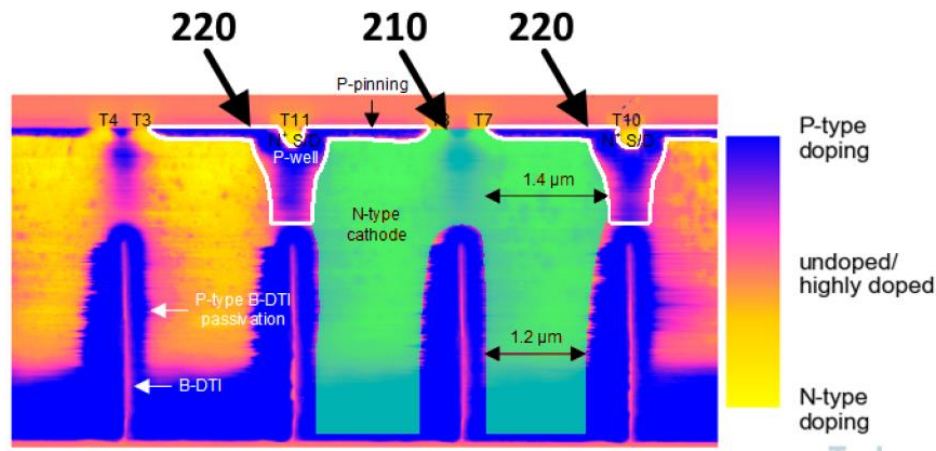
Masagaki

3. Claim 5

The method of claim 1, wherein the ion implantation isolation layer comprises a P0 layer.

Under PO's contentions, *supra* § VI.B.3, Lee+Masagaki+Shiraiwa meets claim 5 because Masagaki's p-type ion implantations in layers 10, 12 and 3 (a) are

p-type, and/or (b) necessarily have a real-world transition in doping concentration at the junction with the abutting n-type doping layer 7. *10X Genomics*, Paper 8, 19; Carley, ¶¶379-380.



PO contentions (claim 5). IC-A1, 30.

Masagaki describes a second p-type implant to form layer 12 because the n-type implant through diffusion 3 to form layer 6 would have reduced p-type dopant concentration. Masagaki, [0040]; Carley, ¶381. POSAs would have understood that annealing to cure crystal damage from ion implantation would have caused p and n dopants to diffuse, which would contribute to a non-abrupt transition from p^+ to n^+ concentrations near a metallurgical junction. Carley, ¶381.

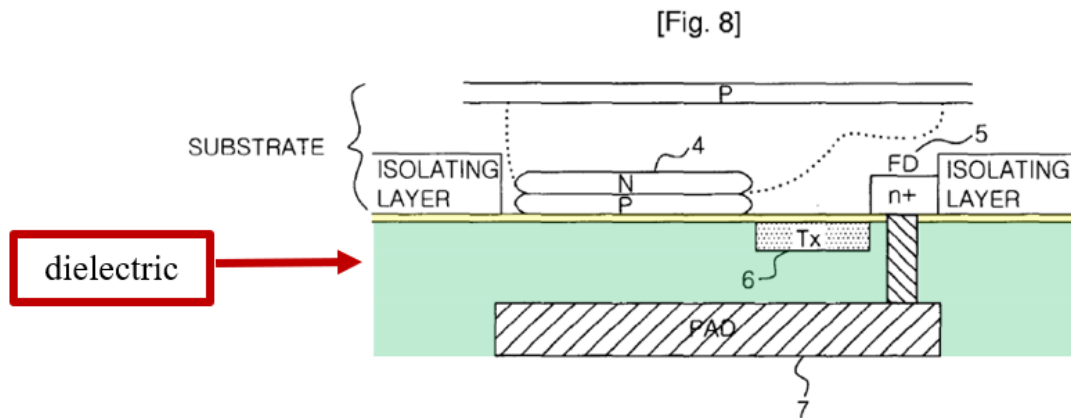
4. Claim 6

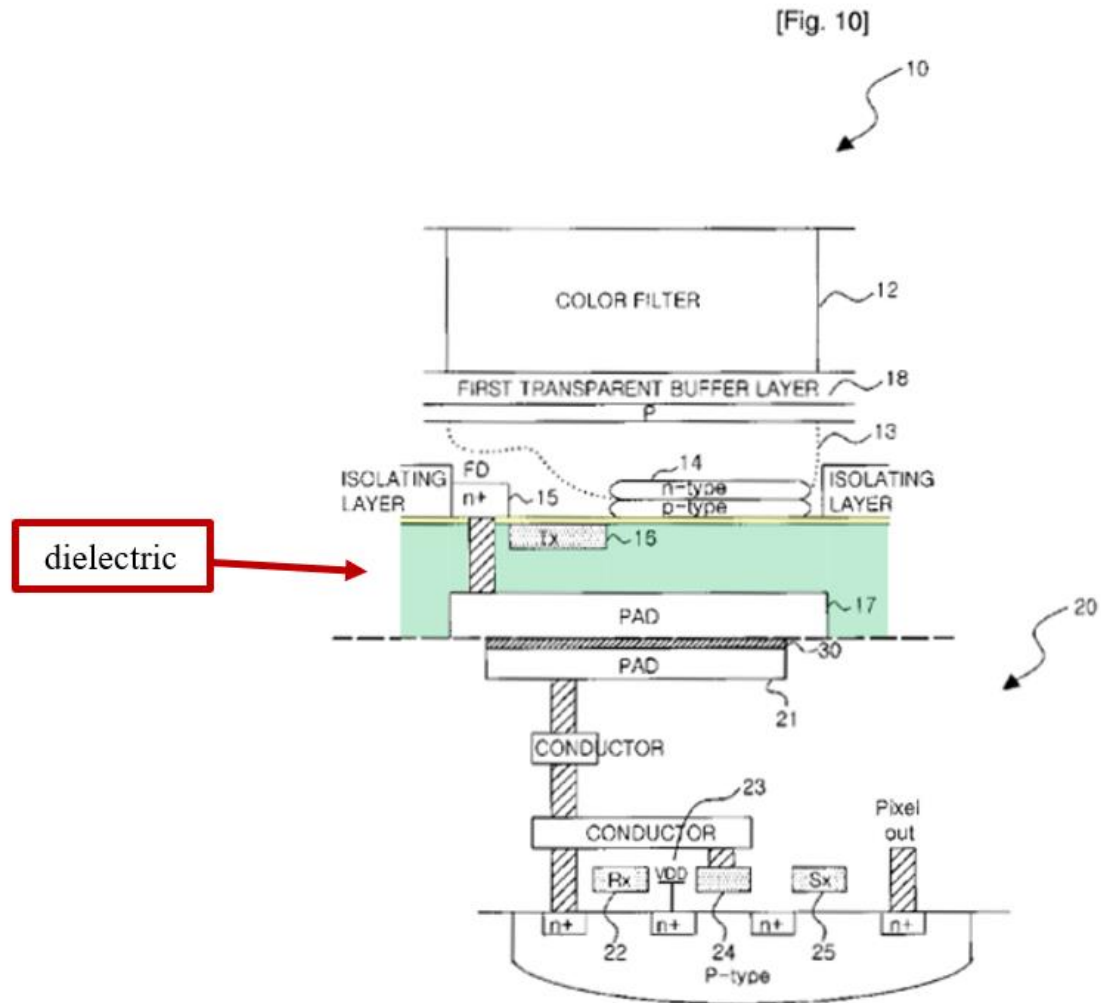
Lee+Masagaki+Shiraiwa meets claim 6 as follows.

a. Step 6.a

6.a	The method of claim 1, comprising: forming a dielectric over the photodiode of the second substrate before bonding the first and second substrates; and
-----	---

Lee shows the separation unit pixel on the first wafer (“second substrate”) with a dielectric formed “over” the photodiode in the unit pixel. *E.g.*, Lee, Figs. 8 & 10; Carley, ¶383.





Lee describes placing conductive pad 17 on the first wafer (Lee [37]-[39]) but does not describe forming the layer that receives pad 17. Carley, ¶384. Nonetheless, Figs. 8 and 10 clearly show a material layer holding pad 17 and, in Fig. 10, forming a physical connection to the second wafer (first substrate) after a bonding step. Lee, Figs. 8, 10; Carley, ¶384. Forming transistor gates, metal layers like pad 17, and the via connecting pad 16 to FD 17, in a dielectric, was well-known. *E.g.*, Iwabuchi, [0145] (forming interlayer insulator 20 with transistor

15), Figs. 10B, 10C, & 11; Keswick; Carley, ¶385. POSAs would have formed a dielectric over the photodiode in the Lee+Masagaki+Shiraiwa unit pixel because this was conventional, thus meeting [6.a]. Carley, ¶386.

b. Step 6.b

6.b	forming a metal pad in the dielectric.
-----	--

Lee shows conductive pad 17 formed in the region marked “dielectric” above. Lee, Figs. 8, 10; Carley, ¶387. While Lee does not describe pad 17 as “metal,” POSAs would have found it conventional to form pad 17 from metal for the same reason it would have been conventional to form conductive pad 21 from metal. *Id.*; *supra* § IX.C.1.c (step [1.b]).

Thus, Lee+Masagaki+Shiraiwa renders obvious claim 6. Carley, ¶388.

5. Claim 8

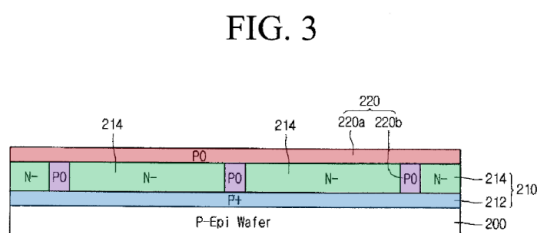
The method of claim 1, wherein forming the circuitry including the metal interconnection comprises forming a metal and a plug over the first substrate.

Under PO’s contentions, *supra* § VI.B.5, Lee+Masagaki+Shiraiwa renders obvious claim 8 because Lee describes conductive pad 21 and multiple vertical conductors in the second wafer 20 (“first substrate”). Lee, [41]-[42], Fig. 10; Carley, ¶390.

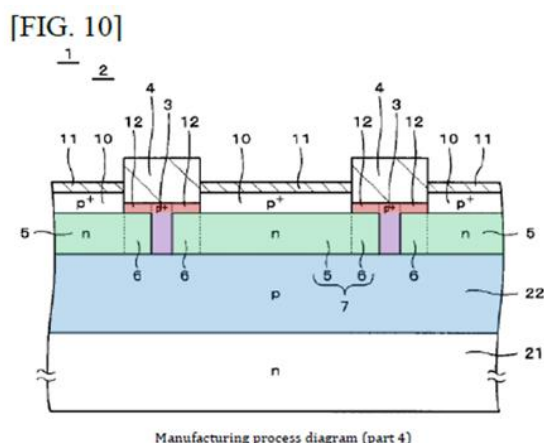
6. Claim 9

The method of claim 1, wherein the **second conduction type second ion implantation isolation layer** is disposed to directly contact on a top surface of the **second conduction type first ion implantation isolation layer** and a bottom surface of the **second conduction type conduction layer**.

Masagaki layer 3 is the “**second conduction type second ion implantation isolation layer**” in [1.h.2] (*supra* § IX.C.1.f.iii), and that top of the “T” comprising layer 12 and the top of layer 3 shaded red in annotated Fig. 10 is the “**second conduction type first ion implantation isolation layer**” in [1.h.1] (*supra* § IX.C.1.f.ii). Carley, ¶396. Layer 22 is the “**second conduction type conduction layer**” in [1.g.1] (*supra* § IX.C.1.d.ii). Carley, ¶396.



'808 patent



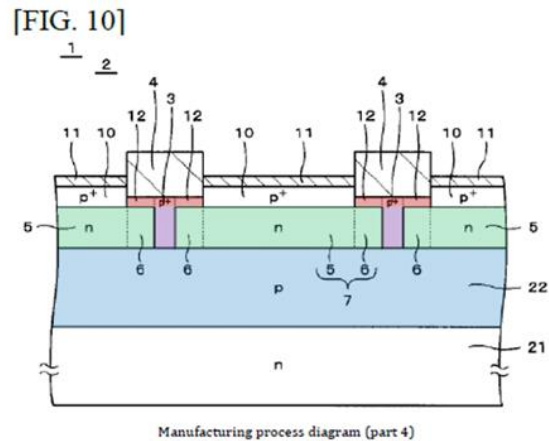
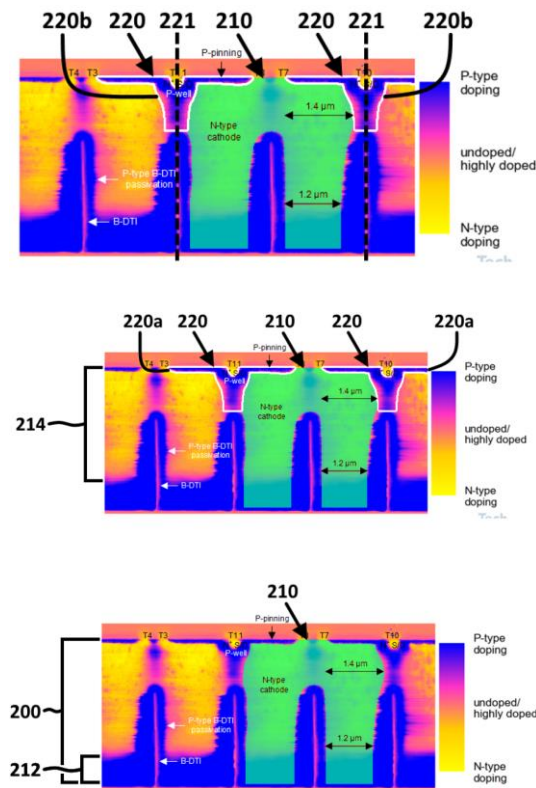
Masagaki

Layer 3 “is disposed to directly contact on a bottom surface” of layer 22 and a “top surface” of layer 12 in the same manner that '808 patent layer 220b contacts the “bottom” of layer 212 and “top” of layer 220a, with “bottom” and “top”

referenced to a topside surface (top of '808 patent Fig. 3 or Masagaki Fig. 10).

Masagaki, Fig. 10; Ex. 1001, Fig. 3; Carley, ¶397.

Lee+Masagaki+Shiraiwa meets claim because Masagaki shows layer 3 contacting layer 12 and layer 22 in the same way that PO's contentions map claim 9 to regions marked 220b, 212, and 220a. IC-A1, 36-38; Carley, ¶398.



PO contentions. IC-A1, 36-38.

Masagaki

Thus, Lee+Masagaki+Shiraiwa renders claim 9 obvious. Carley, ¶399.

X. GROUND 2B: LEE+MASAGAKI+SHIRAIWA+MARUYAMA RENDERS OBVIOUS CLAIM 2

Neither Lee, Masagaki, nor Shiraiwa provide junction depth details. POSAs would have used Maruyama's known methods of setting the p-layer 22 junction

depth for the same reasons, and with the same expectations of success, explained with Iwabuchi *supra* § VII.B. Carley, ¶400.

Lee+Masagaki+Shiraiwa+Maruyama meets claim 1 for the same reasons that Lee+Masagaki+Shiraiwa alone meets claim 1. *Supra* § IX.C.1; Carley, ¶401.

In Lee+Masagaki+Shiraiwa+Maruyama backside p-layer in Lee (Fig. 10), which corresponds to Masagaki p-layer 22 in a backside format, has a junction depth under 0.5 μm as described in Maruyama. This meets claim 2. Carley, ¶402.

XI. GROUND 2C: LEE+MASAGAKI+SHIRAIWA+TONG RENDERS OBVIOUS CLAIM 7

A. Tong

U.S. Patent Application Publication No. US 2005/0161795 A1 (Ex. 1029, “Tong”) published July 28, 2005 and is pre-AIA § 102(b) prior art to all challenged claims. Tong describes low-temperature wafer direct bonding using plasma treatment to “enhance the bonding energy at room temperature for both metal/metal and oxide/oxide bonds.” Tong, [0080].

B. Lee+Masagaki+Shiraiwa+Tong

Lee describes adhering wafers at conductive pads without describing the bonding process. Lee, [51]. Tong’s methods improved existing techniques by bonding at room temperature, providing hermetic bonds without the stress and inhomogeneity of adhesive bonding. Tong, [0009]. Tong also benefited three-dimensional systems-on-chip (“SoC”) like Lee because it allowed “direct wafer

bonding of non-metal between wafers” allowing “[v]ery small bonding metal pads” resulting in low parasitics, reduced power, and increasing bandwidth capacity. Tong, [0010], [0012].

As explained *supra* § IX.C.4.a, Lee discloses bonding hybrid wafer surfaces with conductive pads formed in a dielectric. Tong describes bonding “opposing wafers with reciprocal metal bonding pads” just like Lee. Tong, [0082]; *supra* § IX.C.1.g.i (step [1.e]); Lee, [51] (bonding wafers by adhering opposing conductive pads). On each wafer, insulator surrounds Lee’s conductive pads. Lee, Fig. 10; *supra* § IX.C.4. In Tong, “the bonding of the non-metal regions generates the requisite forces to form the metal-to-metal interconnections across the dies.” Tong, [0083].

POSAs would have understood that Tong’s plasma activation would have improved the adhesion between metal pads in Lee and improved bonding between the opposing dielectrics surrounding Lee’s conductive pads, in the same way that it enhanced low temperature bonding energy in Tong. Carley, ¶407. POSAs would have reasonably expected Tong’s methods to improve yield and allow smaller bonding pads with electrical performance improvements for the reasons explained in Tong and because Lee+Masagaki+Shiraiwa+Tong uses Tong’s known fabrication methods in predictable semiconductor device manufacturing in Tong’s known ways. Tong, [0008]; Carley, ¶408.

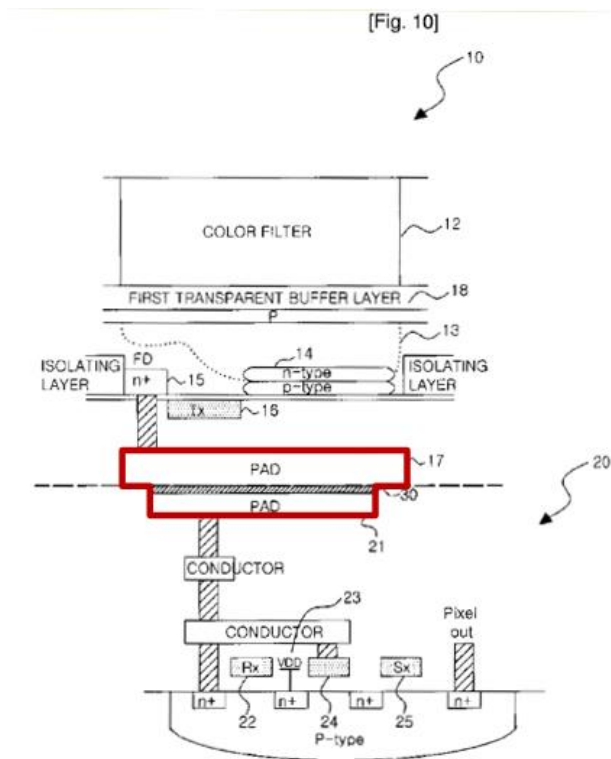
Manufacturing Lee+Masagaki+Shiraiwa's imager with Tong's bonding methods is Lee+Masagaki+Shiraiwa+Tong.

C. Claim 7

The method of claim 1, wherein bonding the first substrate to the second substrate comprises contacting the first substrate and the second substrate with each other and performing activation by plasma.

Lee+Masagaki+Shiraiwa+Tong meets claim 1 for the same reasons that Lee+Masagaki+Shiraiwa alone meets claim 1. *Supra*, § IX.C.1. As explained *supra* § IX.C.1.c (step [1.b]), POSAs would have found it obvious to form Lee's conductive pads 17 and 21 in Lee's first and second wafers using gold or copper. Carley, ¶411. To the extent Lee+Masagaki+Shiraiwa's conductive pads comprised copper, following Tong a POSA would have coated the copper bonding pad with oxidation-resistant gold. Tong, [0075], [0080]; Carley, ¶412. Then Tong describes plasma treatment to "enhance the bonding energy at room temperature for both metal/metal and oxide/oxide bonds." Tong, [0080]. This is plasma activation. Carley, ¶412.

Lee+Masagaki+Shiraiwa+Tong renders obvious claim 7. Carley, ¶413.



XII. DISCRETIONARY DENIAL IS UNWARRANTED

A. Not Warranted Under *Fintiv*

The Petition provides compelling evidence of unpatentability. Under the Director’s Interim Procedure for Discretionary Denials (June 21, 2022) (“IP”), “the PTAB will not deny institution based on *Fintiv*.” IP, 5.

Fintiv also favors institution based on efficiency, fairness, and patent quality. *Apple v. Fintiv*, IPR2020-00019, Paper 11 at 5 (Mar. 20, 2020) (“*Fintiv*”) (precedential).

1. Factor 1: Litigation stay.

Factor 1 is neutral because no party has requested a stay and the district court has not addressed one. *Fintiv*, Paper 15, 12 (May 13, 2020) (informative)

(“*Fintiv* DI”); *Sand Revolution II v. Continental Intermodal*, IPR2019-01393, Paper 24, 7 (June 16, 2020) (informative); *Peloton Interactive v. iFit*, IPR2022-00030, Paper 12, 39 (April 22, 2022), (citing *Fintiv* DI, 12).

2. Factor 2: Median-time-to-trial relative FWD.

The Eastern District of Texas median-time-to-trial is 24.5 months (Ex. 1024; IP, 9 n.12), which would result in a June 2024 trial. Institution six months from Petition filing would result in FWD in June 2024. This favors institution. IP, 8-9.

3. Factor 3: Investment in litigation.

Factor 3 favors institution. Petitioner filed this petition early in litigation: Petitioner has not answered, discovery is just starting, no expert reports have been filed, no trial date or Markman hearing has been set, and no substantive orders have issued. This “weigh[s] against exercising the authority to deny institution[.]” *Apple v. Seven*, IPR2020-00156, Paper 10, 11-12 (June 15, 2020) (“*Seven*”) (quoting *Fintiv*, 11); see also *Amperex. v. Maxell*, IPR2021-01442, Paper 16, 10-11 (April 12, 2022) (Factor 3 weighs against discretionary denial on similar facts).

4. Factor 4: Overlapping issues.

The “issue overlap” factor favors institution because Petitioner stipulates that, should the Board institute review, Petitioner will not rely in litigation on any invalidity grounds based on *Iwabuchi* and/or *Lee* (i.e., the primary references). *Sand Revolution II*, 11–12.

5. Factor 5: Parties.

Factor 5 is neutral. Petitioner is a party to the Litigation, and it is speculative which tribunal will decide invalidity first. *Google v. Parus*, IPR2020-00846, Paper 9, 20-21 (Oct. 21, 2020).

6. Factor 6: Other considerations.

The Petition's "strong showing on the merits" weighs against denial. *Seven*, 20-22.

B. Not Warranted Under Section 325(d)

The Petition asserts substantial new, noncumulative prior art and arguments. The Office never considered this art. Discretionary denial under Section 325(d) is not warranted.

XIII. CONCLUSION

The Board should institute review and cancel claims 1-2 and 4-9.

Dated: 12/9/2022

Respectfully submitted,

/Michael N. Rader/

Michael N. Rader, Reg. No. 52,146
WOLF, GREENFIELD & SACKS, P.C.

CERTIFICATE OF SERVICE UNDER 37 C.F.R. § 42.6 (E)(4)

I certify that on December 9, 2022, I will cause a copy of the foregoing document, including any exhibits or appendices filed therewith, to be served via Overnight FedEx at the following correspondence address of record for the patent:

Farjami & Farjami LLP
26522 La Alameda Avenue, Suite 360
Mission Viejo, CA

Date: December 9, 2022

/MacAulay Rush/
MacAulay Rush
Paralegal
WOLF, GREENFIELD & SACKS, P.C.

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24, the undersigned certifies that the foregoing Petition for *Inter Partes* Review contains 13,999 words excluding a table of contents, a table of authorities, Mandatory Notices under § 42.8, a certificate of service or word count, or appendix of exhibits or claim listing, but including annotations added to figures. Petitioner has relied on the word count feature of the word processing system used to create this paper in making this certification, manually adding to that the number of words present in annotations to figures.

Date: December 9, 2022

/MacAulay Rush/
MacAulay Rush
Paralegal
WOLF, GREENFIELD & SACKS, P.C.

U.S. PATENT NO. 7,867,808 CLAIM LIST

Ref Claim

1.p	A method, comprising:
1.a	providing a first substrate;
1.b	forming circuitry including a metal interconnection over the first substrate;
1.c	forming a photodiode in a crystalline semiconductor layer of a second substrate;
1.d	forming an ion implantation isolation layer in the photodiode;
1.e	bonding the first substrate to the second substrate to connect the photodiode to the metal interconnection; and
1.f	removing a lower portion of the second substrate to expose the photodiode,
1.g	wherein forming the photodiode comprises:
1.g.1	forming a second conduction type conduction layer in the crystalline semiconductor layer; and
1.g.2	forming a first conduction type conduction layer over the second conduction type conduction layer,
1.h.1	wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer over the first conduction type conduction layer,
1.h.2	wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.
2	The method of claim 1, comprising forming the second conduction type conduction layer at a junction depth of less than approximately 0.5 μm .
3	The method of claim 1, comprising forming the first conduction type conduction layer at a junction depth ranging from approximately 1.0 μm to 2.0 μm .
4	The method of claim 1, comprising forming the ion implantation isolation layer over at least one of a side of the photodiode and a bottom of the photodiode.
5	The method of claim 1, wherein the ion implantation isolation layer comprises a P0 layer.
6.a	The method of claim 1, comprising: forming a dielectric over the photodiode of the second substrate before bonding the first and second substrates; and
6.b	forming a metal pad in the dielectric.

Ref Claim

7	The method of claim 1, wherein bonding the first substrate to the second substrate comprises contacting the first substrate and the second substrate with each other and performing activation by plasma.
8	The method of claim 1, wherein forming the circuitry including the metal interconnection comprises forming a metal and a plug over the first substrate.
9	The method of claim 1, wherein the second conduction type second ion implantation isolation layer is disposed to directly contact on a top surface of the second conduction type first ion implantation isolation layer and a bottom surface of the second conduction type conduction layer.