

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY GROUP CORPORATION
Petitioner,

v.

VISIONX TECHNOLOGIES, LLC,
Patent Owner.

Case No. IPR2023-00296
Patent No. 7,867,808

**DECLARATION OF L. RICHARD CARLEY, Ph.D.
IN SUPPORT OF PETITION FOR
INTER PARTES REVIEW OF U.S. PATENT NO. 7,867,808**

TABLE OF CONTENTS

I.	INTRODUCTION	1
A.	Engagement	1
B.	Background and Qualifications	2
C.	Bases of My Opinions and Materials Considered	5
D.	My Understanding of Patent Law	6
1.	Anticipation	7
2.	Obviousness.....	8
3.	Claim Interpretation	14
II.	DESCRIPTION OF THE RELEVANT FIELD AND THE RELEVANT TIME FRAME.....	16
III.	PERSON HAVING ORDINARY SKILL IN THE ART	17
IV.	THE '808 PATENT.....	20
A.	Embodiments	20
B.	Challenged Claims.....	26
C.	Prosecution History	30
V.	GROUND 1A: IWABUCHI RENDERS OBVIOUS CLAIMS 1, 4-6, AND 8-9	30
A.	Iwabuchi	30
B.	Claim analysis.....	31
1.	Claim 1	31
2.	Claim 4	100
3.	Claim 5	101
4.	Claim 6	105
5.	Claim 8	108
6.	Claim 9	108
VI.	GROUND 1B: IWABUCHI+MARUYAMA RENDERS OBVIOUS CLAIM 2.....	110

A. Maruyama	110
B. Iwabuchi+Maruyama.....	113
C. Claim 2	115
VII. GROUND 1C: IWABUCHI+SUGA RENDERS OBVIOUS CLAIM 7....	115
A. Suga	115
B. Iwabuchi+Suga	116
1. Reasons to combine.....	116
2. Reasonable expectation of success.....	118
C. Claim 7	119
1. “contacting substrate[s]”	119
2. Analysis	120
VIII. GROUND 2A: LEE+MASAGAKI+SHIRAIWA RENDERS OBVIOUS CLAIMS 1, 4-6, AND 8-9.....	122
A. References	122
1. Lee	123
2. Masagaki	124
3. Shiraiwa.....	127
B. Lee+Masagaki+Shiraiwa.....	128
1. Reasons to combine.....	135
2. Reasonable expectation of success.....	137
C. Claim analysis.....	138
1. Claim 1	138
2. Claim 4	153
3. Claim 5	154
4. Claim 6	155
5. Claim 8	158
6. Claim 9	160
IX. GROUND 2B: LEE+MASAGAKI+SHIRAIWA+MARUYAMA RENDERS OBVIOUS CLAIM 2	162

X.	GROUND 2C: LEE+MASAGAKI+SHIRAIWA+TONG RENDERS OBVIOUS CLAIM 7.....	163
A.	Tong.....	163
B.	Lee+Masagaki+Shiraiwa+Tong.....	163
C.	Claim 7	165
XI.	CONCLUSION.....	166
	APPENDIX A: MATERIALS CONSIDERED	168
	APPENDIX B: U.S. PATENT NO. 7,867,808 CLAIM LIST	171

I, L. Richard Carley, declare:

I. INTRODUCTION

A. Engagement

1. I have been retained on behalf of Sony Group Corporation (“Sony” or “Petitioner”) as an independent technical expert in the above-captioned IPR proceeding (“the IPR”). This document provides certain of my opinions concerning the patentability of claims in U.S. Patent No. 7,867,808 (Ex. 1001, “the ’808 patent”), specifically claims 1-2 and 4-9 (the “Challenged Claims”). I make this Declaration in support of Sony’s petition in the IPR.

2. For my work as an expert in this matter, I am being compensated for my services at my standard rate, plus actual expenses. My hourly compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other personal or financial stake or interest in the outcome of the present proceeding. I do not have any expectation or promise of additional business with the Petitioner in exchange for the positions explained herein.

3. I make this Declaration based on my personal knowledge, including my education, training, research, and professional experience.

B. Background and Qualifications

4. My curriculum vitae (“CV”) detailing my educational background, professional experience, and list of publications is provided as Exhibit 1004. Some of my background and experience that qualifies me to offer the opinions in this Declaration as an expert in the technical issues in this case are as follows.

5. I am Full Professor of Electrical and Computer Engineering at Carnegie Mellon University (“CMU”). I have taught in the Department of Electrical and Computer Engineering at CMU since 1984 except for a brief leave of absence from 2001-2003.

6. I was the ST Microelectronics Professor of Engineering at Carnegie Mellon University from 2001 to 2020. This Chaired professorship was established by ST Microelectronics, S.A., at Carnegie Mellon University in 2001 and I was its first recipient.

7. I hold the degrees of S.B. in Electrical Engineering and Computer Science, S.M. in Electrical Engineering and Computer Science, and Ph.D. in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology in 1976, 1978 and 1984, respectively.

8. Since 1984, in addition to carrying out teaching and research at Carnegie Mellon, I have also consulted for over 25 companies.

9. From 1997 to 2002 I served as the chief circuit designer and co-founded Neolinear, where I helped to develop integrated circuit (IC) computer-aided design tools for analog and mixed analog/digital circuits. My efforts at Neolinear included user interface design, automated analog circuit sizing and biasing tools and automated place-and-route tools for analog circuits. Neolinear was acquired by Cadence Design Systems, the leader in the integrated circuit computer-aided design market in 2004. It is now the analog/mixed signal division of Cadence Design Systems.

10. From 2001 to 2003 I served as the Chief Executive Officer (CEO) and Chief Technology Officer (CTO) of IC Mechanics, Inc. IC Mechanics focused on developing novel low-cost very large-scale integration (“VLSI”) manufacturing technologies for Micro-Electro-Mechanical Systems (“MEMS”) inertial sensing integrated circuits (“ICs”). Among my responsibilities at IC Mechanics, I designed and developed both IC sensors and manufacturing processes for building those IC sensors.

11. In 2008, I served as the part-time acting CEO of Resonance Semiconductor. At Resonance Semiconductor I worked on projects involving radio frequency (“RF”) integrated circuit design using MEMS resonators.

12. I am the author or co-author of over 250 technical publications dealing with the design of integrated circuits and other topics in Electrical and Computer Engineering.

13. I am a Fellow of the Institute of Electrical and Electronics Engineers. I am a named inventor on 28 patents related to circuit design and signal processing. I have also been awarded various honors, including the Semiconductor Research Corporation Technical Excellence Award, many best-paper awards at conferences including two at the Design Automation Conference (DAC), a best-panel session award at the International Solid-State Circuits Conference (ISSCC) and the Eta Kappa Nu Excellence in Teaching Award at Carnegie Mellon University.

14. I have carried out extensive research and development in the area of complementary metal-oxide-semiconductor (“CMOS”) image sensors. From 1989 through 1992, I led a National Science Foundation funded research grant that developed active CMOS image sensors that measured range to the reflecting surface along every line of sight. During this project, we developed, taped out, fabricated through a CMOS foundry, and tested, three generations of CMOS image sensors for range finding. Our work resulted in U.S. Patent No. 5,107,103, “Integrated Circuit Having At Least A Sensor And A Processor Thereon,” which issued April 12, 1993. The work was also published in the premier journal for integrated circuits, the IEEE Journal of Solid State Circuits in March of 1991.

15. A more detailed description of my qualifications, experience, publications, awards, and patents is included in my Curriculum Vitae, provided as Ex. 1004.

C. Bases of My Opinions and Materials Considered

16. I have reviewed the '808 patent, its prosecution history, and the prior art and other documents and materials cited herein. For ease of reference, the full list of documents that I have considered is included in Appendix A. I have also considered the documents cited and referenced herein, even if not included in Appendix A. Each of these materials is a type of document that experts in my field would have reasonably relied upon when forming their opinions and would have had access to either through the applicable patent office and/or well-known libraries, conferences, publications, organizations, and websites in the field as further discussed herein.

17. My opinions in this Declaration are based on my review of these documents, as well as upon my education, training, research, knowledge, and experience. When developing the opinions set forth in this declaration, I assumed the perspective of a person having ordinary skill in the art, as set forth in Section III below.

18. The opinions and comments formulated during this assessment are based on observations and information available at the time of this investigation.

D. My Understanding of Patent Law

19. In developing my opinions, I discussed various relevant legal principles with Petitioner's attorneys. I have relied upon such legal principles, as explained to me, while forming the opinions set forth in this declaration. My understanding in this respect is as follows:

20. I understand that *inter partes* review ("IPR") is a proceeding before the United States Patent & Trademark Office ("USPTO") for evaluating the patentability of an issued patent's claims based on prior-art patents and printed publications.

21. I understand that, in this proceeding, Sony has the burden of proving that the challenged claims of the '808 patent are unpatentable by a preponderance of the evidence. I understand that a "preponderance of the evidence" means that the evidence establishes that a fact or conclusion is more likely true than not true.

22. I understand that patent claims can be independent or dependent. I understand that a dependent claim must reference a claim previously set forth, and then must specify a further limitation of the claimed subject matter. I also understand that a dependent claim is treated as incorporating by reference all limitations of the previously recited claim that it references. I understand that an independent claim does not reference or incorporate limitations from a previously disclosed claim.

23. I understand that, in IPR proceedings, claim terms in a patent are given their ordinary and customary meaning as understood by a person of ordinary skill in the art (“POSA”) in the context of the entire patent and the prosecution history pertaining to the patent. I discuss the qualifications of the POSA relevant to the ’808 patent below, *infra* § III. If the specification provides a special definition for a claim term that differs from the meaning the term would otherwise possess, the specification’s special definition takes precedence. I have applied these standards in preparing the opinions in this declaration.

24. I understand that for an invention claimed in a patent to be patentable, it must be, among other things, new (and consequently not anticipated) and not obvious from the prior art. My understanding of these two legal standards is set forth below.

1. Anticipation

25. I understand that, for a patent claim to be “anticipated” by the prior art (and therefore not novel), each and every claim limitation must be disclosed, expressly or inherently, in the subject matter provided by a single prior-art reference. I understand that anticipation requires that all of the elements of a claim have to be arranged in the same manner as in the claims or can be immediately envisaged. I understand that a claim limitation is disclosed for the purpose of anticipation if a POSA would have understood the reference to disclose the

limitation based on inferences that a POSA would reasonably be expected to draw from the explicit teachings in the reference when read in the context provided by the POSA's knowledge and experience.

26. I understand that a claim limitation is inherent in a prior art reference if that limitation is necessarily present when practicing the teachings of the reference, regardless of whether a POSA recognized the presence of that limitation in the prior art.

2. Obviousness

27. I understand that a patent claim may be unpatentable if it would have been obvious to a POSA in view of a single prior-art reference or a combination of prior-art references. I have been informed that obviousness is determined from the perspective of a hypothetical person of ordinary skill in the art and that the asserted claims of the patent should be read from the point of view of such a person at the time the alleged invention was made. I have been informed that a hypothetical person of ordinary skill in the art is assumed to know and to have all relevant prior art in the field of endeavor covered by the '808 patent and would thus have been familiar with each of the references cited herein, as well as the background knowledge in the art discussed and the full range of teachings they contain.

28. I have been informed that there are two criteria for determining whether prior art is analogous and thus can be considered prior art: (1) whether the

art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the patentee's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the patentee is involved. I have also been informed that the field of endeavor of a patent is not limited to the specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field. I have also been informed that a reference is reasonably pertinent if, even though it may be in a different field from that of the patentee's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to a patentee's attention in considering his problem.

29. I understand that a patent claim is obvious if the differences between the subject matter of the claim and the prior art are such that the claimed subject matter, as a whole, would have been obvious to a POSA at the time the invention was made. I have been informed as well that a prior art reference should be viewed as a whole. Specifically, I understand that the obviousness question involves a consideration of: the scope and content of the prior art; the differences between the prior art and the claims at issue; the knowledge of a POSA; and any "secondary considerations" of non-obviousness

30. I have been informed that certain factors called "secondary considerations" can include (1) the invention's commercial success, (2) long felt

but unresolved needs, (3) the failure of others, (4) skepticism by experts, (5) praise by others, (6) teaching away by others, (7) recognition of a problem, (8) copying of the invention by competitors, and (9) other relevant factors. I have been informed, however, that for such objective evidence to be relevant to the obviousness of a claim, there must be a causal relationship (called a “nexus”) between the claim and the evidence and that this nexus must be based on what is claimed and novel in the claim rather than something in the prior art. I also have been informed that even when they are present, secondary considerations may be unable to overcome primary evidence of obviousness (*e.g.*, motivation to combine with predictable results) that is sufficiently strong.

31. I am not aware of any such “secondary considerations” applicable to the Challenged Claims. To my knowledge, the Patent Owner (“PO”) has not asserted any such secondary considerations with respect to the ’808 patent. However, should any be presented, I reserve the right to address those unknown factors if asked by the Petitioner to do so.

32. I understand that for a claimed invention to be considered obvious, a POSA must have had a reason for combining teachings from multiple prior-art references (or for altering a single prior-art reference, in the case of obviousness in view of a single reference) in the fashion proposed.

33. I have also been informed that in considering whether an invention for a claimed combination would have been obvious, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the marketplace, and/or the background knowledge possessed by a person having ordinary skill in the art. I have been informed that other principles may be relied on in evaluating whether an alleged invention would have been obvious, and that these principles include the following:

- A combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results;
- When a device or technology is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or in a different one, so that if a person of ordinary skill in the art can implement a predictable variation, the variation is likely obvious;
- If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar

devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill;

- An explicit or implicit teaching, suggestion, or motivation to combine two prior art references to form the claimed combination may demonstrate obviousness, but proof of obviousness does not depend on, or require, showing a teaching, suggestion, or motivation to combine;
- Market demand, rather than scientific literature, can drive design trends and may show obviousness;
- In determining whether the subject matter of a patent claim would have been obvious, neither the particular motivation nor the avowed purpose of the named inventor controls;
- One of the ways in which a patent's subject can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims;
- Any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed;

- “Common sense” teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle;
- A person of ordinary skill in the art is also a person of ordinary creativity, and is not an automaton;
- A patent claim can be proved obvious by showing that the claimed combination of elements was “obvious to try,” particularly when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions such that a person of ordinary skill in the art would have had good reason to pursue the known options within his or her technical grasp; and
- One should be cautious of using hindsight in evaluating whether an alleged invention would have been obvious.

34. I understand that a POSA must have a reasonable expectation of success in combining the references. I understand that a reasonable expectation of success refers to the likelihood of success in combining references to meet the limitations of the claimed invention. I understand that in evaluating a combination, a predictable result means not only that the prior art elements are capable of being

physically combined, but also that the combination would have worked for its intended purpose.

35. I have been asked to consider the patentability of the Challenged Claims. I have been informed that for *inter partes* reviews (“IPR”), unpatentability must be shown under a preponderance of the evidence standard. I have been informed that to establish something by a preponderance of the evidence one needs to prove it is more likely true than not true. I have concluded that the Challenged Claims are unpatentable at least as obvious based on the references described below and as explained herein.

3. Claim Interpretation

36. I understand that determining whether a claimed invention is novel and non-obvious requires comparing the prior art to the challenged claim. In this Section, I discuss the interpretations that I applied to certain claim terms in my analysis.

37. I have been informed that patent claims are construed from the viewpoint of a person of ordinary skill in the art at the time of the alleged invention. I have been informed that patent claims generally should be interpreted consistent with their plain and ordinary meaning as understood by a person of ordinary skill in the art in the relevant time period (i.e., at the time of the purported invention, or the so called “effective filing date” of the patent application), after

reviewing the patent claim language, the specification and the prosecution history (i.e., the intrinsic record).

38. I have further been informed that a person of ordinary skill in the art must read the claim terms in the context of the claim itself, as well as in the context of the entire patent specification. I understand that in the specification and prosecution history, the patentee may specifically define a claim term in a way that differs from the plain and ordinary meaning. I understand that the prosecution history of the patent is a record of the proceedings before the U.S. Patent and Trademark Office, and may contain explicit representations or definitions made during prosecution that affect the scope of the patent claims. I understand that an applicant may, during the course of prosecuting the patent application, limit the scope of the claims to overcome prior art or to overcome an examiner's rejection, by clearly and unambiguously arguing to overcome or distinguish a prior art reference, or to clearly and unambiguously disavow claim coverage.

39. In interpreting the meaning of the claim language, I understand that a person of ordinary skill in the art may also consider "extrinsic" evidence, including expert testimony, inventor testimony, dictionaries, technical treatises, other patents, and scholarly publications. I understand this evidence is considered to ensure that a claim is construed in a way that is consistent with the understanding of those of skill in the art at the time of the alleged invention. This can be useful for technical

terms whose meaning may differ from its ordinary English meaning. I understand that extrinsic evidence may not be relied on if it contradicts or varies the meaning of claim language provided by the intrinsic evidence, particularly if the applicant has explicitly defined a term in the intrinsic record.

40. I understand that determining whether a claimed invention is novel and non-obvious requires comparing the prior art to the challenged claim. In this Declaration, I apply the above standards to the terms in the challenged claims. The meanings of specific terms are discussed below in connection with evaluating the disclosure in the priority documents.

II. DESCRIPTION OF THE RELEVANT FIELD AND THE RELEVANT TIME FRAME

41. I have reviewed the '808 patent (Ex. 1001) and its prosecution history (Ex. 1002).

42. I understand that the '808 patent issued from U.S. Patent Application Ser. No. 12/344,538 ("the '538 application"), filed on December 28, 2008. Ex. 1001 (Fields 21 & 22).

43. I understand that the '538 application relates to a Korean Patent Application No. 10-2007-0139749, which was filed on December 28, 2007. Ex. 1001 (Field 30).

44. I have been instructed by counsel to assume the relevant timeframe for my analysis of the prior art in this Declaration is on or before December 28, 2007.

45. Based on my review of this material, I believe that the relevant general fields for the purposes of the '808 patent are solid-state imager design and fabrication techniques for integrated circuit systems such as solid-state image sensors.

III. PERSON HAVING ORDINARY SKILL IN THE ART

46. My opinions are based on what a person of ordinary skill in the art ("POSA") in the technical field of the alleged invention would have understood at the time of the alleged invention of the Challenged Claims. As I explained above, the relevant timeframe in the analysis in this Declaration is on or before December 28, 2007. I have been informed and understand that the content of a patent and prior art should be interpreted the way a person of ordinary skill in the art would have interpreted those references at the time of the alleged invention of the patent using the ordinary and customary meanings of the claim terms. I understand that a person of ordinary skill in the art is a hypothetical concept referring to one who thinks along the lines of conventional wisdom at the time. I have applied this standard throughout my declaration.

47. I was asked to provide an opinion as to the level of skill for a person of ordinary skill in the art pertinent to the subject matter set forth in the Challenged Claims of the '808 patent on December 28, 2007.

48. In the context of the '808 patent and the prior art, it is my opinion that the POSA to whom the patent is addressed, on December 28, 2007, would have had a Bachelor's degree in electrical engineering, physics, or material science and at least 4 years of industrial or research experience in solid-state imager design and fabrication. In order to design an image sensor a POSA would have had to understand the imager device structure, how that structure could be fabricated and the design limitations imposed by fabrication techniques, circuit design supporting pixel operation, and the overall readout control architecture that forms an image. Alternatively, a POSA would have had a Master's degree in one of the same fields and at least 2 years of experience as described.

49. The basis for my familiarity with the level of ordinary skill is my own technical experience and my interaction with students and professionals in the field of Electrical and Computer Engineering who were at this level of skill as of December 28, 2007. I am well aware of the knowledge that a person of ordinary skill in the art would have had at the time this patent was written as I have been actively teaching and carrying out research with such students all through that period.

50. In reaching this opinion as to the hypothetical person of ordinary skill in the art, I have considered the types of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level and professional capabilities of workers in the field.

51. As summarized above with regards to my qualifications and experience, I possessed at least the level of skill of a person of ordinary skill in the art at the time of the alleged invention of the '808 patent.

52. I have worked with many people who fit the characteristics of the POSA, and I am familiar with their level of skill in and around December 2007. When developing the opinions set forth in this declaration, I assumed the perspective of a POSA as set forth above.

53. Except as noted below whenever I offer an opinion in this declaration about the knowledge of a POSA, the manner in which a POSA would have understood the claims of the '808 patent or its description, the manner in which a POSA would have understood the prior art, or what a POSA would have been led to do based on the prior art, I am referencing the December 2007 timeframe, even if I do not say so specifically in each case.

IV. THE '808 PATENT

54. The '808 patent describes a method for manufacturing a solid-state image sensor. It was filed December 28, 2008, claiming priority to a Korean application filed December 28, 2007. 1:4-6.¹ There are nine method claims. Claim 1 is independent. Throughout this declaration when I refer to a claim element, I mean claim language associated with a particular claim element reference as provided in the claim list at Appendix B.

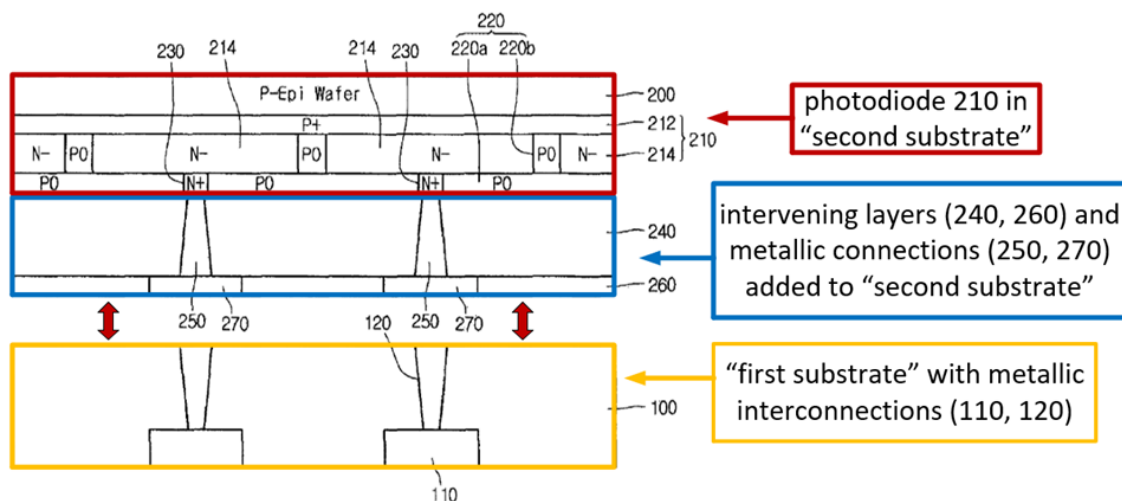
A. Embodiments

55. The '808 patent describes methods for manufacturing an image sensor with a “vertical type photodiode” by forming a semiconductor photodiode in ***one substrate*** and electrically connecting the photodiode to metallic interconnections formed on a ***different substrate***. 1:47-49, 2:25-33, Figs. 7, 8. When the “first” and “second” substrates are “bonded” (**red** arrows below), the “vertical” result provides a continuous conductive path from a photodiode 210 to the metallic interconnections on the “first” substrate. The “N+ layer 230 may serve as an electron movement path of electrons generated from pixels, and may contribute to

¹ Unless otherwise indicated all citations in this section refer to Exhibit 1001, the '808 patent. Additionally, throughout this declaration, unless otherwise indicated, emphasis is added to quoted content.

ohmic contact.” 4:5-7. That means “N+ layer 230” provides electrical connection to the N- region and after substrates are bonded together connects the N- region to the metal interconnections on the “first substrate.” P0 layers 220a and 220b “may serve as... a ground line.” 4:3-4.

FIG. 7



56. The '808 patent purports to respond to problems with prior art CMOS image sensors that had photodiode and transistors “horizontally arranged” adjacent to each other, with transistors consuming area that could otherwise be devoted to light detection, fabricated using processes optimized for forming CMOS transistors but not optimized for forming photodiodes. 1:16-43.

57. The '808 patent “solved” these problems with a “vertical type photodiode in which a photodiode may be positioned over circuitry” with a photodiode formed in a substrate without transistors. 2:38-41, Figs. 2-8;

58. Separating the photodiode fabrication from CMOS device fabrication by putting the photodiode in its own substrate or layer (1:66-2:2, Fig. 2) removed these drawbacks so that the full light-incident surface could be used for photodetection and processes used in the sensor layer could be optimized for photodiode fabrication.

59. The advantages from forming imagers with a photodetector on one layer or wafer and electronics on another were well-known in the art by December 2007. Back in the 1980's and 1990's, it was well known to create photodiodes on one wafer that was bonded by metals to the electronics and control wafer. I worked on a project in the late 1980's with Hughes Aircraft Corporation in which we designed, fabricated, and tested an infra-red photodiode array on one substrate and control electronics on another substrate, and then bonded them together using fine pitch indium bumps. In this case, the advantage was that completely different semiconductor materials could be used in the photodiode array, ones optimized for sensitivity at the desired infra-red wavelength, while the readout electronics were fabricated in a standard electronics fabrication technology. A similar approach was described in the IEEE Transactions on Electron Devices in Nov. 1993 by authors from AT&T and Amber Engineering. They bonded GaAs multi-quantum well photodiodes to CMOS readout electronics. Ex. 1011, G. C. Bethea et al., "Long wavelength infrared 128×128 $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ quantum well infrared camera and

imaging system,” *IEEE Transactions on Electron Devices*, vol. 40, no. 11, pp. 1957-1963, Nov. 1993. Even for visible wavelength image sensors, it was well-known prior to the ’808 patent that backside illumination and bonding of at least an image sensor substrate and a CMOS electronics substrate offered significant improvements in the size and sensitivity of CMOS imagers. For example, Holm provides a long list of advantages accruing to fabricating the photodiodes on a separate substrate from the CMOS control electronics. Ex. 1031 (“Holm”), [0002]-[0008], [0050]-[0055].

60. It was well-known in the art at the time of invention to make solid-state imagers in a three-dimensional stack that vertically integrated electronics on one or more wafers or substrates with a focal plane array or sensor on another wafer or substrate. POSAs had several reasons to pursue this approach.

61. First, by making the photodetector and electronics on different wafers or substrates, the fabrication techniques—and materials—could be optimized for each particular application. This was important because semiconductor fabrication processes optimized for forming CMOS devices in silicon were often not optimized to form photodetectors in silicon, or other material systems with different bandgaps and optoelectronic properties that might be preferred as a substrate for a sensor layer. *E.g.*, Holm, [0003]. For example, “thick absorbing layers and deep junctions may be needed to achieve high efficiency; these same

design criteria generally being in conflict with those for high performance electronic applications.” *Id.*

62. Second, the electronics and photodetectors are also subject to different scaling trends, so that while reducing the electronics dimensions in advanced process nodes provided benefits for advanced electronics, reducing the pixel area and volume for photodetectors is associated with increased dark current and, consequently, photodetectors with reduced signal to noise ratios. *E.g., id., [0004]* . Additionally, “reduced lateral dimensions” in the pixel “are generally attended by reduced vertical dimensions leading to thinner layers and shallower junctions as well as higher doping levels and reduced carrier diffusion lengths. Reduced supply voltages also may negatively impact charge collection and storage capability of the PD [photodiode]. Moreover, an ever-increasing number of interconnect levels and corresponding isolating dielectric layers generally decreases the optical throughput and coupling efficiency to the photodetector and introduces additional sources of reflection and scattering that can lead to elevated levels of optical crosstalk.” *Id., [0006]*. It is thus desirable to scale the pixels and readout and other electronics differently, using different processes for their fabrication. Forming the sensor layer and the supporting electronics layers in different substrates, then bonding the wafers or die together, makes it possible to optimize the fabrication techniques separately for each layer.

63. Third, it was known in the art to increase the transistor count associated with each pixel to provide “digital pixel sensors” with enhanced functionality compared to 3 or 4 transistors in a typical readout circuit for an “active pixel sensor.” *E.g., id.*, [0005]. “This desire for increased signal processing functionality within the pixel escalates competition for ‘real estate’ within the pixel area creating additional problems generally associated with shrinking the PD [photodiode] active area, reducing the fill factor within the pixel, and applying advanced process technologies.” *Id.*

64. Fourth, “[e]fforts to improve the level of PD [photodiode] performance can limit flexibility and performance in the CMOS electronics as well. Minimizing the number of interconnect levels to improve the optical coupling to the PD, for example, may make interconnect routing more difficult and less area-efficient.” *Id.*, [0007].

65. In short, “[t]he co-integration of the photosensor with the CMOS electronics (i.e., within the same material layer, using the same processes, etc.) within the pixel of CMOS imagers may severely limit both the performance of the photosensor and the flexibility of the system architectural design. This problem may be further complicated by progression to more advanced CMOS technology generations which generally utilize... non-transparent [silicide], and increasing numbers of interconnect levels. The... trend toward increase functionality within

the pixel (as with digital pixel sensors—DPS) adds more electronic circuitry within the pixel creating competition for pixel area, decreasing fill factor and further compromising of performance.” *Id.*, [0008]. POSAs knew that vertical integration provides improved performance, lower system cost, increased functionality, lower power consumption, and smaller form factors.

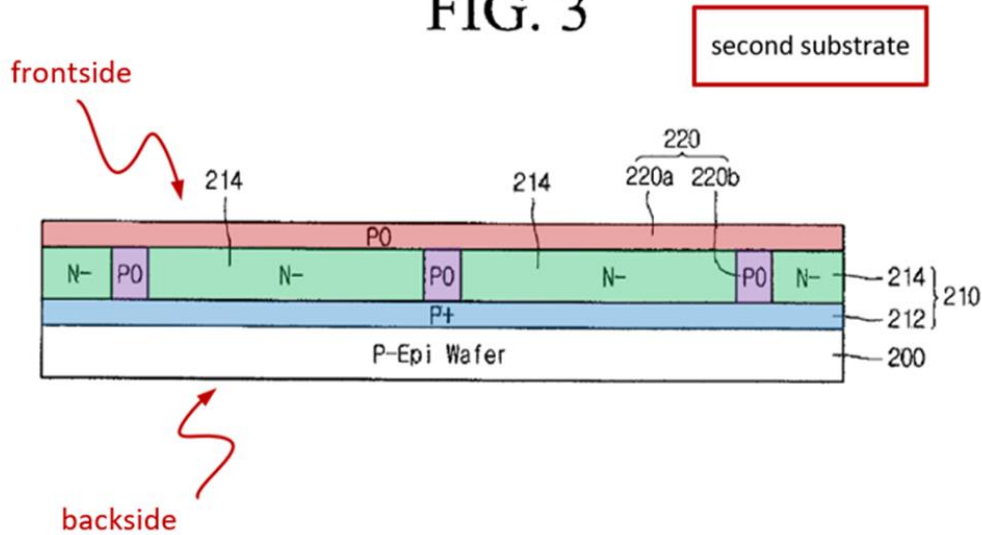
66. Bonding the substrates in the “vertical type photodiode” connected a metal interconnection on the first substrate (metal 110 and plug 120) to a photodiode (at N- conduction layer 214) with a conductive path through “metal pad” 270, tungsten plug 250, and N+ conductive layer 230. 2:25-32, 4:4-18, Figs. 7 & 8. The patent’s “vertical type photodiode” has no transistor in the sensor substrate. *Id.*

B. Challenged Claims

67. Claim 1 recites forming metal interconnections on a first substrate, a photodiode in a second substrate, and bonding them together. Removing material from the backside of the second substrate exposes the photodiode. This provides backside-illuminated (“BSI”) photodiode, meaning light is incident on the “backside” of the substrate in which the photodiode (*e.g.*, bottom of Fig. 3 or top of Fig. 8).

68. The backside surface varies with processing steps but always refers to the backside of the layer or substrate.

FIG. 3



69. The patent identifies the surface defined by “removing the lower portion of the second substrate” as the “backside.” 4:47-50 (“P-Epitaxial layer...may be removed by performing a cleaving or backside thinning process[.]”).

70. Before thinning, the second substrate “backside”—depicted above—is the lower surface of the “P-Epi Wafer” 200 in Fig. 3, while after thinning, the “backside” is the remaining second substrate surface opposite layer 220a.

71. The “frontside” surface opposes the “backside,” as in annotated Fig. 3 above. The frontside conventionally meant the surface on which photolithographic or other masks were placed to define features for fabrication process steps including ion implantation or—as the patent describes for layer 212—through which maskless “blanket” ion implantation was done. 3:19-30. POSAs would

have understood that the top surface in Fig. 3 is the “frontside” because during fabrication that is the surface through which dopants are typically implanted.

72. A backside layer such as “P-Epi” layer 200 in Figure 3 of the ’808 patent was conventionally a thick layer used to mount or handle the substrate while working on the frontside, or to add rigidity to a thin epitaxial film so that features could be formed in it through the frontside.

73. The claims require forming a photodiode with four layers in the “second substrate.” The photodiode is formed in a crystalline semiconductor layer (step [1.c]) with two conduction layers having opposing n (donor) or p (acceptor) doping types. Steps [1.g], [1.g.1], [1.g.2], 3:19-61 & Figs. 2-3.

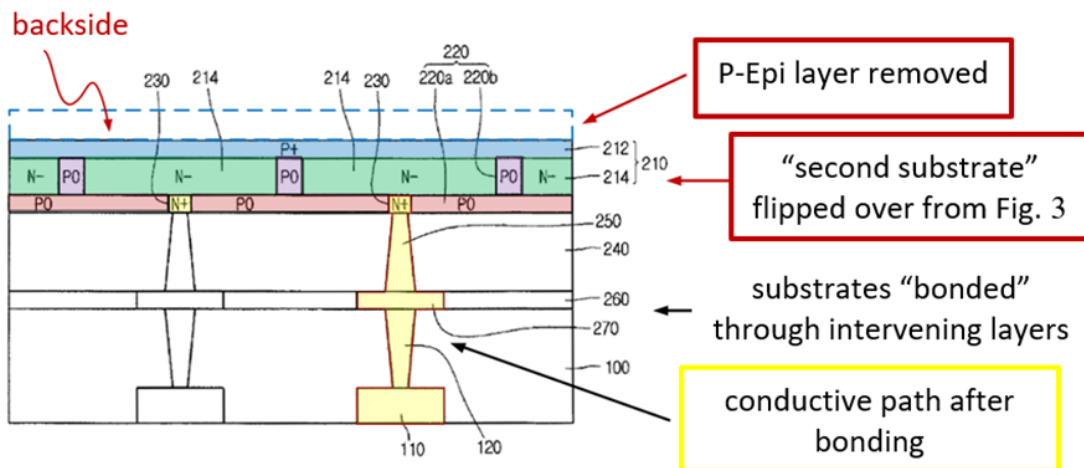
74. POSAs reading claim 1 would have understood that the “first” type conduction layer (step [1.g.2], **green N- 214**) must be formed “over” the “second” type conduction layer (step [1.g.1], **blue P+ 212**), imposing a sequence with step [1.g.1] performed before step [1.g.2], because the step [1.g.2] refers to placing the first conduction type conduction layer in relation to a second conduction type conduction layer that has already been formed. I apply this understanding in my analysis below.

75. The claims also require forming two “isolation layers” (steps [1.h.1] (**red 220a**) and [1.h.2] (**purple 200b**)) by ion implantation. Steps [1.d], [1.h.1], [1.h.2], 3:44-4:4, Figs. 2-4. The “second” “isolation layer” (step [1.h.2], 220b) is

“at an interface between pixels” and defines the lateral boundaries of each pixel (e.g., an individual light-collecting region). 2:44-47.

76. The isolation layers (from steps [1.h.1] and [1.h.2]) “may serve as a pixel-to-pixel isolator.” 4:2-4.

FIG. 8



77. Before bonding the second substrate (with the photodiode) is flipped from the “backside-down” orientation in Figures 2 to 6 to the “backside-up” orientation in Figures 7 and 8, which illustrate bonding the two substrates (step [1.e]) and thinning the second substrate by removing material to expose the photodiode (step [1.f]).

78. Dependent claims add minor variations to claim 1 concerning junction depth, doping levels, isolation layer placement, bonding, and metal interconnects.

C. Prosecution History

79. Prosecution involved a single action rejecting all method claims as obvious. Ex. 1002, 137-139. The applicant amended the independent claim (application-claim 10, which issued as challenged claim 1) to incorporate application-claims 11 (steps [1.g.1], [1.g.2]), 14 (step [1.h.1]), and 15 (step [1.h.2]), Ex. 1002, 147-148, 150-152, then distinguished prior art based on “isolation layer” limitations ([1.h.1] and [1.h.2]). Ex. 1002, 150-152. The examiner thereafter allowed all claims without explanation. Ex. 1002, 157.

V. GROUND 1A: IWABUCHI RENDERS OBVIOUS CLAIMS 1, 4-6, AND 8-9

A. Iwabuchi

80. U.S. Patent Application Publication No. US 2006/0197007 A1 (Ex. 1005, “Iwabuchi”), published September 7, 2006.

81. Iwabuchi describes methods for manufacturing a CMOS image sensor with backside-illuminated photodetectors that separate the image sensor and associated signal processing circuitry into different chips. Iwabuchi, [0003], [0017], [0124]-[0125]. A unit cell for the photodetection, or pixel, is replicated and formed into a planar array on the sensor chip. *Id.*, [0094]. Peripheral circuitry on the signal processing (“DSP”) chip process the image. *Id.*, [0140].

82. Iwabuchi describes multiple ways to integrate the sensor and signal processing chips, including through an interposer or by direct bonding.

The CMOS image sensor having the above-described arrangement becomes able to directly input the signal outputted from the pixel of the CMOS image sensor to the signal processing device through the micro-bump at the pixel unit...[providing] a high performance and highly-capable device in which signal processing speed among devices is high and in which the image sensor and the signal processing device are integrated as one chip.

Id.

83. The image signal is routed to the signal processing circuit through the back of the pixel, opposite the light-incident backside surface (or back surface).

Id., [0129]-[0130], Figs. 5, 7. The frontside surface (or front surface), at the back of the pixel, is where patterning is carried out to form features like the transfer transistor 1048 in the unit pixel. *Id.*, Fig. 5. In one embodiment each pixel has its own interconnection for signal output. *Id.*, [0192]. Iwabuchi's design makes it "possible to make the pixel size become very small in accordance with increase of integration degree of pixel without lowering a saturation electric charge amount and sensitivity." *Id.*, [0194].

B. Claim analysis

1. Claim 1

a. Preamble

84. Iwabuchi describes methods for manufacturing an imager. *E.g.*, Iwabuchi, [0021], claims 5-20.

b. Step 1.a

1.a	providing a first substrate;
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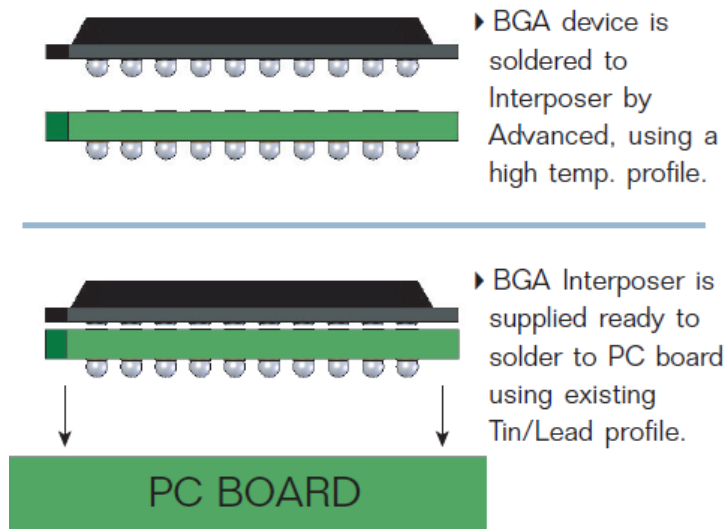
85. Iwabuchi meets [1.a] at least three ways.

i. interposer

86. Iwabuchi describes an “intermediate substrate” called interposer 3.

Iwabuchi, [0117]. An interposer is commonly used to connect two or more silicon integrated circuits together within a single package. Typically such interposers are silicon chips themselves that only have metal layers such as copper and gold patterned on them to connect the silicon integrated circuits together and to connect them to a printed circuit board. Ex. 1035, 60 (describing copper defined land pattern), Ex. 1033, 576 (describing formation of gold pillars).

87. For example, Ex. 1036 describes a ball grid array (“BGA”) interposer using FR-4, a dielectric with a specific permittivity commonly used as the substrate for circuit boards, instead of silicon. In one figure, Ex. 1036 shows a BGA device with bumps on one surface bonded to flat metal lands on one side of the interposer, which is shaded green.



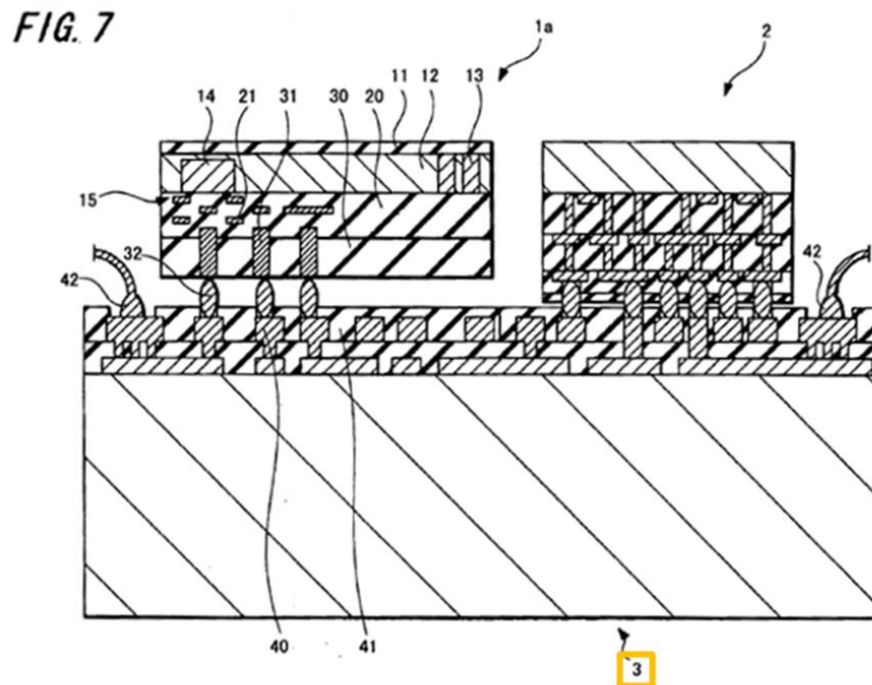
88. In this example the interposer itself has tin/lead solder balls on its opposing surface, to mount to a PC Board or other substrate.



89. Choosing an interposer substrate material that matches the material used in the active chips offers the advantage of reducing stress fatigue due to

thermal cycling. Multiple silicon chips can be bonded to such an interposer allowing them to be electrically interconnected.

90. The interposer is “provided” because Iwabuchi describes mounting a sensor chip 1a and DSP chip 2 on it in the embodiment shown in Fig. 7. Iwabuchi, [0020]-[0021], [0117], [0124], [0162], Fig. 7. The interposer is the “first substrate.”



ii. supporting substrate

91. Iwabuchi describes providing a “supporting substrate 30 in order to stabilize the shape” of semiconductor layer 12. Iwabuchi, [0122]; *id.*, [0079], [0118], [0121], [0146], Figs. 10A, 10C.

92. In [0117], Iwabuchi explains that it is discussing the back-illuminated type of CMOS solid-state image pickup device and sensor chip 1a in Figure 7. In the section discussing the embodiment shown in Figure 7, at [0121] Iwabuchi discusses forming photodiode 14 in semiconductor layer 12, while in [0122] Iwabuchi explains “[i]n the above-described arrangement, the semiconductor layer is obtained by decreasing the thickness of the back surface of the semiconductor substrate and it has the structure in which it is bonded to the supporting substrate 30 in order to stabilize the shape of the substrate.”

93. There are, in short, two “substrates” mentioned in [0122]. POSAs would understand that the thinned “substrate”—e.g., the “semiconductor substrate” whose back surface is defined by decreasing the thickness of the substrate from the backside—means semiconductor layer 12 and, in the Figure 7 embodiment, insulator 11, which Iwabuchi later explains (Figure 10G) is the result of removing the handle wafer or lower portion 10 of the semiconductor-on-insulator (“SOI”) wafer shown in Figure 10A.

94. The “supporting substrate 30” is self-explanatory and is the substrate that is bonded to interlayer dielectric 15 as shown in Figures 7 and 10C. POSAs would understand that the support substrate would add rigidity to the thinned semiconductor substrate (layers 12 and 11) so that they could be manipulated and subject to further fabrication steps like bonding the die to interposer 3 as shown in

95. The “supporting substrate 30” is the “first substrate.”

96. “[T]he sensor chip can be directly mounted on the signal processing chip as a module.” Iwabuchi, [0153]. The DSP chip is “provided” because Iwabuchi describes manipulating it. *E.g.*, Iwabuchi, [0117], [0125], [0153].

- 36 -

have understood “chip” referred to a substrate on which the “peripheral circuit unit” was formed.

98. The DSP chip would conventionally have been implemented as solid-state circuits formed on a substrate. DSP chips were generally fabricated in standard digital CMOS process technologies; *i.e.*, a silicon substrate upon which CMOS transistors and metal interconnects are patterned on the front side. All integrated circuits are fabricated upon some kind of substrate, typically a silicon wafer. They are then diced into many chips after the fabrication is complete. The bottom of the chip is still referred to as the substrate even after dicing.

99. The DSP chip substrate is the “first substrate.”

c. Step 1.b

1.b	forming circuitry including a metal interconnection over the first substrate;
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100. Claim 8 states “forming the circuitry including the metal interconnection ***comprises forming a metal and a plug*** over the first substrate.” The specification never identifies circuit components beyond conductive elements. The figures at most show metal 110 and plug 120 with first substrate 100. *E.g.*, Ex. 1001, 4:25-30 & Fig. 7. These sources demonstrate that a metal and a plug meet [1.b] “circuitry including a metal interconnection.” I understand that the Patent Owner’s (“PO”) infringement contentions in a parallel litigation apply this

usage by mapping [1.b] to “metal pads and plugs.” IC-A1², 12. Consequently, for this analysis, I treat the term “forming circuitry including a metal interconnection over the first substrate” as met by metallic traces and plugs formed over a first substrate consistent with how the PO mapped this step to accused products in its infringement contentions.

101. The ’808 patent does not define “plug.” The specification states “[a] metal interconnection of first substrate 100 may include metal 110 and plug 120.” Ex. 1001, 4:29-30, Fig. 7. The specification also refers to “metal plug 250” formed from tungsten in a “first dielectric 240.” *Id.*, 4:8-14, Fig. 5. The ’808 patent’s “plug 250” and “plug 120” correspond to vias, which connect through a material. *Id.*, Figs. 5, 7. PO’s infringement contentions map “plug” to a feature labelled “ISP DBI via.” IC-A1, 34-35.

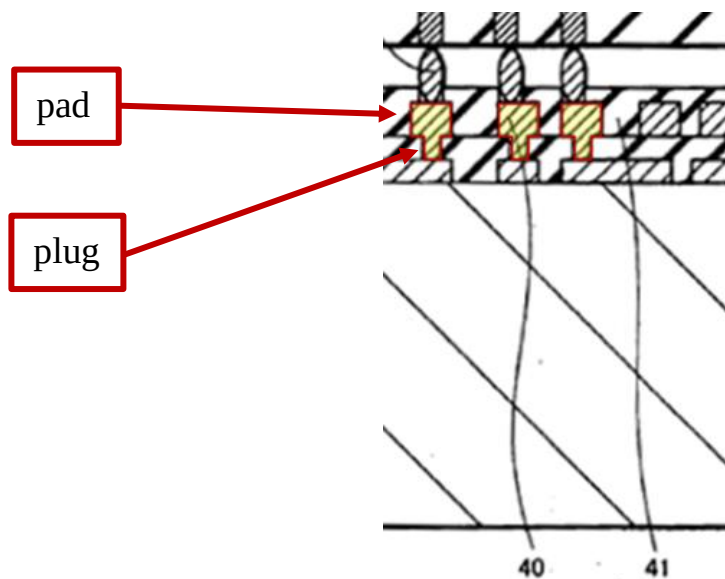
102. Iwabuchi meets [1.b] for each “first substrate” identified *supra* § V.B.1.b ([1.a]). The “metal and a plug over the first substrate” in each instance comprises an “interconnection” because each provides a signal path between a photodiode and signal processing circuits: metal wiring 40 and stem (interposer), bump 32 and wiring 31 (supporting substrate), and land / bump 32 with vias on DSP chip are each an “interconnection” because each provides part of a signal path

² For exhibit short cites, see the Materials Considered at Appendix A.

between a photodiode and signal processing circuits. E.g., Iwabuchi, [0140], [0154], [0189], [0192].

i. interposer

103. Iwabuchi describes forming wirings 40 over interposer 3. Iwabuchi, [0124], Fig. 7. Wiring 40 forms a pad. *Id.* The stem below the pad is a plug. *Id.*, Fig. 7.

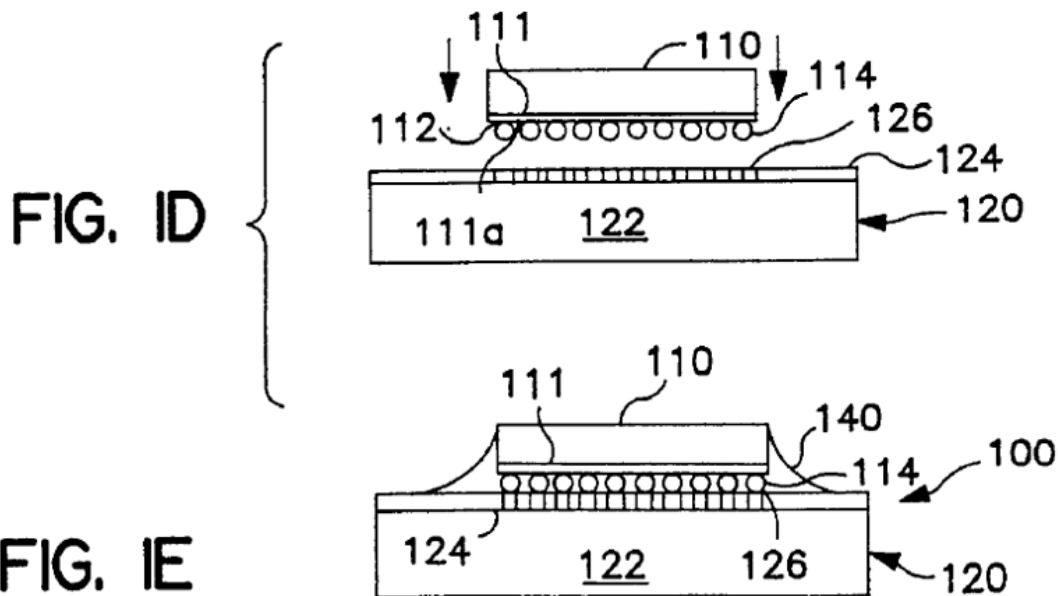


104. The pad compression-bonds with bump 32. *Id.*, [0153], Fig. 7. Bump 32 comprises metal. *Id.*, [0120], [0149]. A POSA would have assumed that wiring 40, the plug, and bump 32 are formed from the same class of material—conductors—because Figure 7 shows them with the same cross-hatching, *id.*, Fig. 7 and because the description of Fig. 7 identifies them all as wiring, which in general would be metal or heavily doped semiconductor.

105. POSAs would also have formed wiring 40 from metal because flip-chip compression bonding conventionally used metal plating to receive bumps. It was conventional to provide metal contacts for receiving bumps in flip-chip bonding. *E.g.*, Tong, [0050] (referring to “**metal** bonding pads”), [0066]-[0067]. For example, Dery, 4:16-24 discusses “solder plating” on “contacts 126” as shown in Figs. 1D, 1E (below). Solder is a conventionally an alloy of tin and other metals. As a result, POSAs would have known that wiring 40 comprising the pad is metal because Iwabuchi [0153] describes compression bonding interposer 3 with sensor chip 1a using wiring 40 as pads on the interposer and microbumps 32 as contact points on the sensor chip 1a. POSAs would have known that the plug or via below the pad in Iwabuchi Fig. 7 would also have conventionally been formed from metal like the pad. *E.g.*, Ex. 1027, 1218, Fig. 8 (describing tungsten vias to copper pads); *cf.* Ex. 1001, 4:8-14 (describing forming metal plug 250 from tungsten).

106. A POSA would understand from Fig. 7 that the photodiodes are connected to metal interconnects, which are then passed through the metal vias in substrate 30, and connected by bump 32 to metal pad 40. From there those lines are connected through the interposer through bumps to the DSP chip.

- 41 -



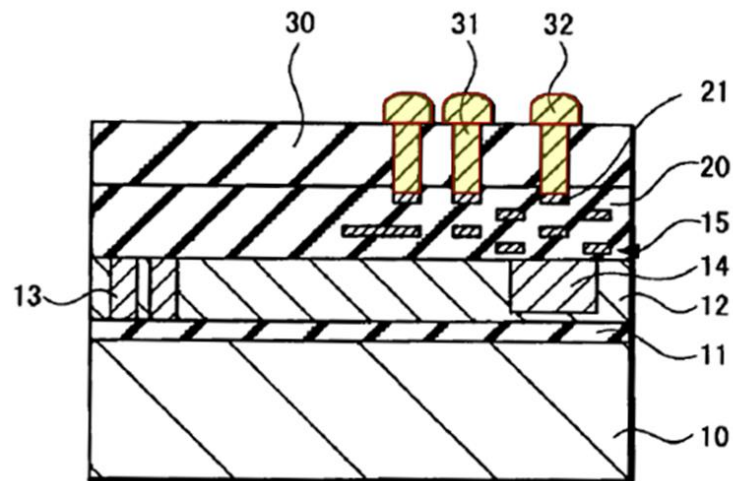
ii. supporting substrate

108. Iwabuchi describes forming “protrusion-like *metal* electrode” bumps 32 (Iwabuchi, [0120]), on copper substrate penetrating wires 31 (*id.*, [0148]-[0149]), over supporting substrate 30 (*id.*, Fig. 10F).

109. Iwabuchi describes forming “substrate penetrating wiring 31” by dry-etching substrate 30 and filling the opening with “low-resistance metal such as copper.” Iwabuchi, [0148].

110. Wiring 31 is a “plug” like “plug 250” in the ’808 patent and the “ISP DBI via” in the contentions. Ex. 1001, 4:8-14, Figs. 5, 7; IC-A1, 34-35. Metal bump 32 is “a metal.”

FIG. 10F



iii. DSP substrate

111. Iwabuchi's "sensor chip can be directly mounted on the signal processing chip" with the same flip-chip bonding described for mounting the sensor on the interposer. Iwabuchi, [0153]. It was well-known to flip-chip bond die and whole wafers together with metal lands on one die (or wafer) receiving bumps on another die (or wafer). *E.g.*, Rogalski, 82-83 & Fig. 14 (below); Balcerak, Fig. 1; Iwabuchi-762, Fig. 1, 26B, 31A (below).

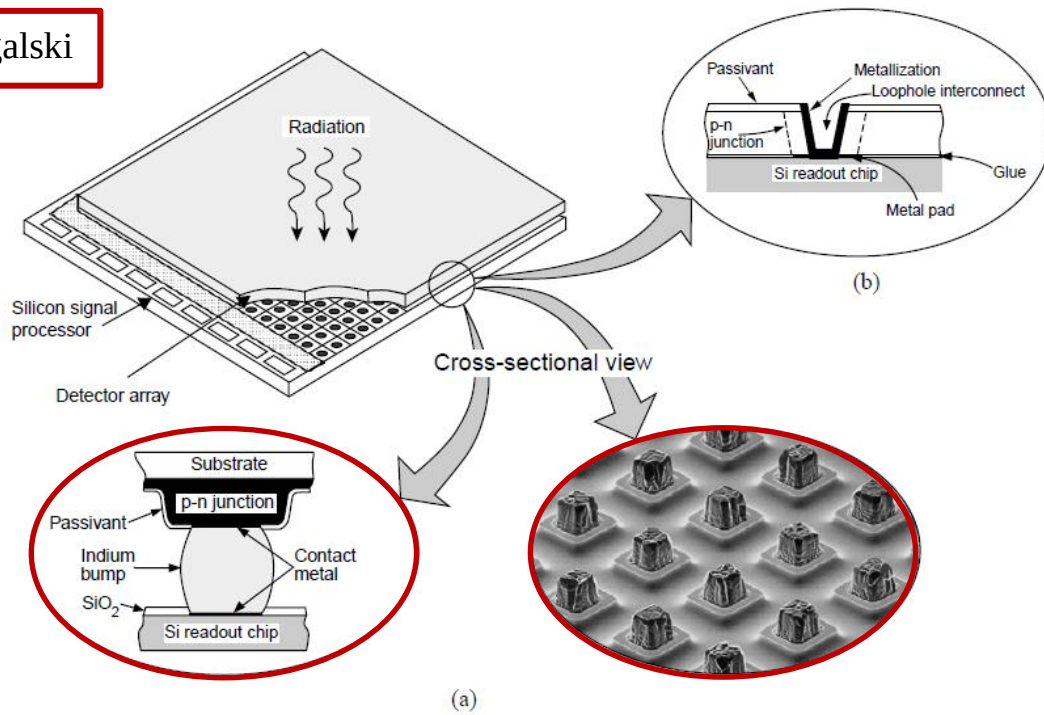
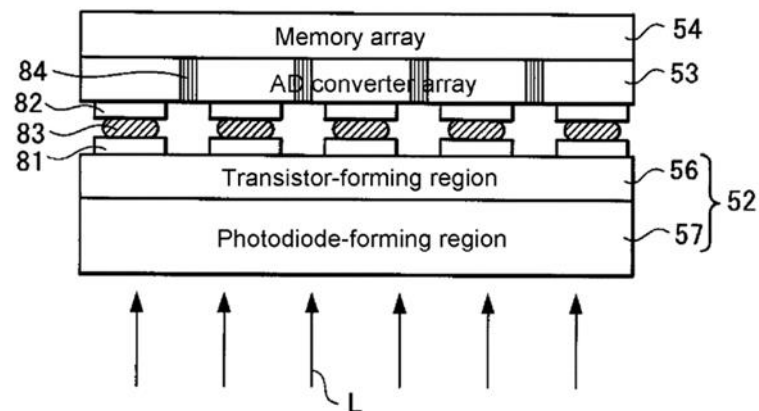


Fig. 14. Hybrid IR FPA with independently optimised signal detection and readout: (a) indium bump technique, (b) loophole technique.

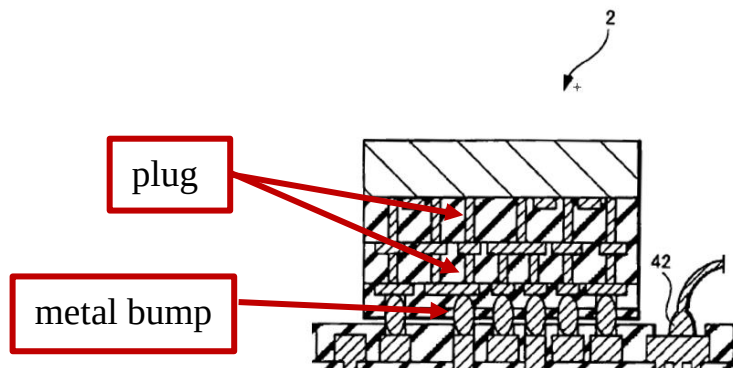
FIG. 1

51

Iwabuchi-762



metal interconnections, and the vias shown in Fig. 7 would conventionally have been metal.



114. Directly bonding a photodiode die or wafer onto a supporting electronics wafer was well-known in the art long before 2007. In fact, I was involved in designing an infrared image sensor that used wafer-to-wafer bonding with indium bumps between photodiodes and the supporting electronics wafer back as far back as the mid-1980's, similar to the bonding described in Rogalski and Balcerak.

d. Conduction layers

i. Step [1.c]

1.c	forming a photodiode in a crystalline semiconductor layer of a second substrate;
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115. POSAs would have understood that “[a] photodiode has a depleted semiconductor region with a high electric field that serves to separate photogenerated electron-hole pairs.” Sze, 671. Sze is a leading textbook on the physics of semiconductor devices that is regularly used and consulted by

practitioners. POSAs would have been familiar with and used Sze. The '808 patent specifically concerns p-n photodiodes. I explain the meaning of “photodiode” in the context of the '808 patent below with steps [1.g] and [1.g.1] because the definition involves the meaning of p and n conduction types. Nonetheless, for step [1.d], Iwabuchi describes forming photodiodes 14 in semiconductor layer 12. Iwabuchi, [0121], [0144]. Semiconductor layer 12 (**red** below) is “formed of a suitable material such as silicon” that is “deposited on the upper layer of the insulating layer 11...by a suitable method such as...bonding...and it is used as an SOI (semiconductor on insulator) substrate.” Iwabuchi, [0143]; *see also id.*, [0089], Figs. 10A-10B. The “second substrate” is Iwabuchi’s SOI wafer including semiconductor layer 12.

116. POSAs would have understood that Iwabuchi Figures 10A to 10G illustrate manufacturing processes for making the photodetector embodiments shown in Figures 5 and 7.

117. First, after describing the “first embodiment” illustrated in Figure 5, Iwabuchi, [0092]-[0113], Iwabuchi explains that “[a] method of manufacturing a CMOS solid-state image pickup device according to the embodiment of the present invention will be described below with reference to the drawings.” Iwabuchi, [0114].

118. Second, Iwabuchi's "second embodiment of the present invention" shown in Figure 7 incorporates the first embodiment shown in Figure 5. Iwabuchi, [0115]-[0116].

119. Then, after describing this second embodiment, Iwabuchi, [0115]-[0140], Iwabuchi explains that Figures 10A-10G describe a "method of manufacturing a back-illuminated type CMOS solid-state image pickup device according to" the second embodiment. Iwabuchi, [0141].

120. The upshot of this series of disclosures is that Figures 10A-10G provide process steps for making Iwabuchi's second embodiment, which incorporates the first embodiment shown in Figure 5. So, among other things, Figures 10A-10G show process steps to manufacture the photodetector in Figure 5.

121. Iwabuchi describes forming its sensor on a SOI wafer. Iwabuchi, [0143]. The semiconductor portion of the SOI wafer can be any crystalline material. When the semiconductor is silicon, the same wafer is also called a **silicon**-on-insulator wafer, while continuing to refer to it as "SOI," since silicon is a common crystalline semiconductor substrate for forming solid-state devices. It was well-known that "the top silicon layer of an SOI (silicon-on-insulator) wafer is high-quality single-crystalline material that is suitable for high-performance and high-density integrated circuits." Sze, 343-344. Layer 12 is a "crystalline semiconductor layer."

122. Photodiode 14 is formed in layer 12. Iwabuchi, [0144] & Fig. 10B.

FIG. 10A

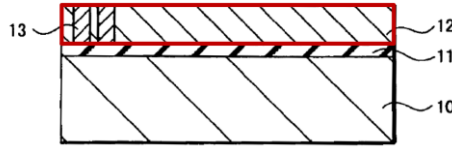
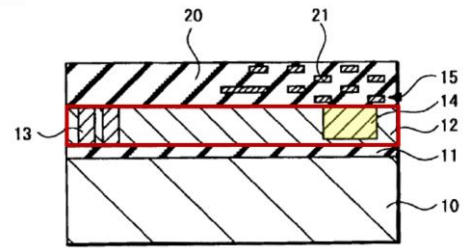


FIG. 10B



123. Iwabuchi's SOI wafer comprising substrate 10, insulator layer 11, and crystalline layer 12 are "provided" and comprise the "second substrate" in [1.c]. Iwabuchi, Fig. 10A.

ii. Steps [1.g], [1.g.1]

1.g	wherein forming the photodiode comprises:
1.g.1	forming a second conduction type conduction layer in the crystalline semiconductor layer; and

124. The term "conduction type" refers to the method by which electric current is carried in a conductor. In these patents, there are elements composed of three conduction type – metals, n-type semiconductors and p-type semiconductors. Whether a semiconductor is n-type or p-type is determined by the difference between the number of n-type dopants and p-type dopants incorporated into the semiconductor crystal. N-type semiconductors have substantially more n-type dopants than p-type dopants and vice versa. Sze, 16-17. Doped layers are formed by adding dopants to a crystal lattice. Sze, 16-22. The n-type dopants contribute mobile electrons, while p-type dopants contribute mobile holes. Sze, 16-17.

The '808 patent follows this usage of conduction type. Ex. 1001, 3:19-21 (“impurity ions may be implanted into a crystalline semiconductor layer”), 3:23-25 (treating “second conduction type” as p), 3:38-40 (treating “first conduction type” as n). Relative to undoped material an “n-type” layer has net excess mobile electrons, while a “p-type” layer has net excess mobile holes.

125. The claims concern a semiconductor photodiode in a “crystalline semiconductor layer” (step [1.b]) having two conduction type layers that POSAs would understand are p and n type. Ex. 1001, 3:23-25, 38-40, Fig. 3. The semiconductor absorbs photons, providing photogenerated mobile electron-hole pairs. In the context of the '808 patent claims, which require forming a photodiode with conduction layers in a crystalline semiconductor substrate, the photodiode has a junction between p type and n type material (a p-n junction). Between the n-type and p-type regions is a transition region that is called a “depletion layer” in which there is a very strong electric field. The electric field in the depletion layer separates photogenerated holes and electrons which then flow into the p region and the n region respectively. Sze, 671, 674-676, 679, Figs. 6, 9(b); Rogalski, 68-69. The charge separation prevents photogenerated carriers from recombining, so that image signal can be extracted. Sze, 675, Fig. 6. The specification uses this ordinary meaning by identifying “photodiode 210,” Ex. 1001, 3:20-21, comprising

a p-n junction formed by “first” n-type layer 214 and “second” p-type layer 212. *E.g.*, Ex. 1001, Figs. 2, 3.

126. Lateral structures in a photodiode have also been used to form p-n junctions having depletion layers that contribute to charge collection. For example, Ex. 1042, S. Tiwari et al., “Lateral p-i-n photodetectors with 18 GHz bandwidth at 1.3 μm wavelength and small bias voltages,” *International Electron Devices Meeting* 1991 [Technical Digest], 1991, pp. 421-424, describes lateral structures forming p-n junctions that contribute to charge collection. Holm-816 also describes lateral structures forming p-n junctions that contribute to charge collection. *E.g.*, Holm-816, 6:47-7:8, Fig. 7.

127. Iwabuchi uses the same mapping for conduction types as the '808 patent so that the “first conduction type” is n and the “second conduction type” is p.

128. Iwabuchi describes forming a backside-illuminated “image pickup device” including a “photodiode” (Iwabuchi, [0094], [0106], Fig. 5) comprising n-type semiconductor region 1052, p+ accumulation layer 1053, p-type well 1046, and p+ accumulation layer 1054, around n-type substrate 1042 (Iwabuchi, [0094], [0096]).

129. As I explained with step [1.c], Figure 10B photodiode 14 represents the photodiode unit cell shown in Iwabuchi Figure 5, and an array (“a plurality of

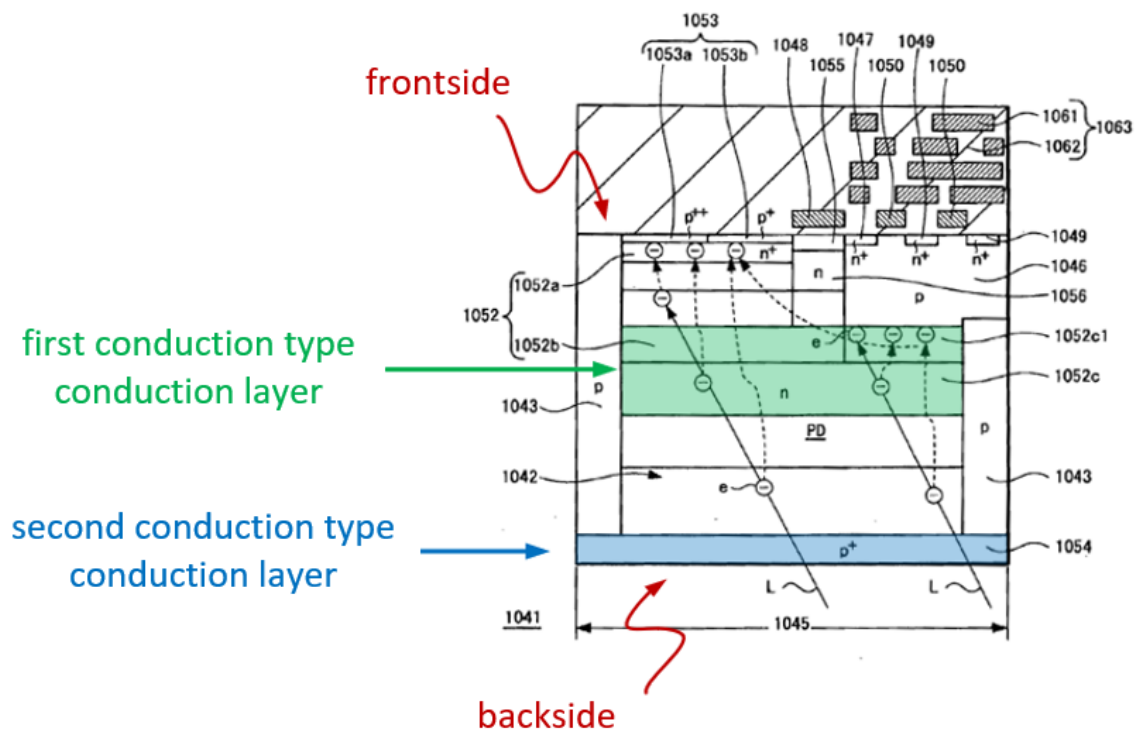
132. Iwabuchi describes forming n type semiconductor region 1052 in terms of several discrete layers illustrate in Figure 5, namely, “a heavily-doped n type electric charge accumulation region 1052a formed on the substrate surface side, an n type region 1052b having an impurity concentration higher than that of this electric charge accumulation region 1052a and which is extended from the electric charge accumulation region 1052a to the back surface side of the substrate and an [n] type semiconductor region 1052c extended to the underside of the p type semiconductor well region 1046.” Iwabuchi, [0096]. Each of these layers forms part of the photodiode and with the p-n junctions provided by the contact faces between the p-type regions and the n-type regions contributes to the depletion region that separates the photogenerated electrons in the unit pixel in Figure 5 and sends the photogenerated electrons to the accumulation region 1052a, where they can be read as signal.

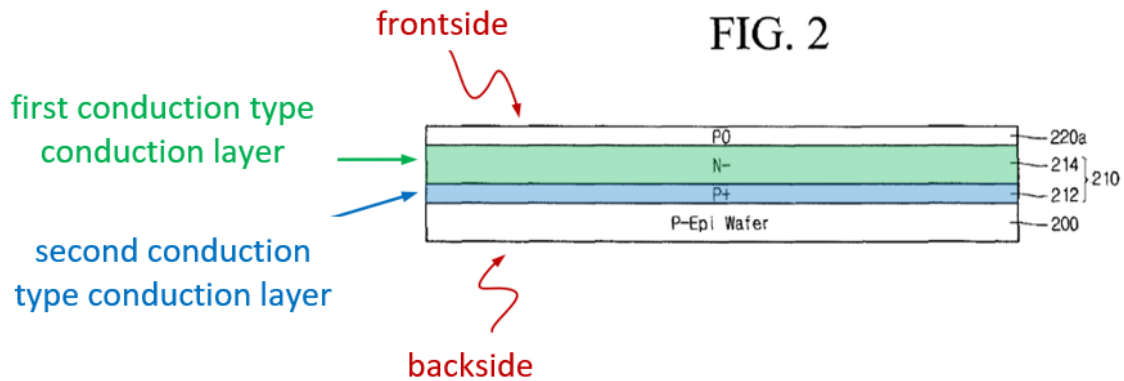
133. In this analysis of step [1.g.2] “forming a first... layer **over**” a “second” layer, “over” does not require direct contact between layers. Claim 9 confirms this usage by reciting “disposed to directly contact on,” demonstrating the applicant knew how to claim a relationship of “direct contact” when intended but selected the broader relational term “over” in claim 1. The specification confirms this distinction between “on” and “over” when describing the first (layer 214) and second (layer 212) conduction layers. Ex. 1001, 3:34-38 (“layer 214 may be

formed **on and/or over**” layer 212). Thus, for this analysis I am asked to assume that “over” as used in the claims does not require direct contact between layers, and this is consistent with how a POSA would have understood “over” in the claims. Ex. 1023, 993 (“over” is a preposition that means “higher than”).

134. Relative to the backside surface, n-type layers 1052 meeting [1.g.2] are “over” p-type layer 1054 meeting [1.g.1], just as n-type layer 214 is “over” p-type layer 212 in the ’808 patent, Fig. 2.

FIG. 5





e. Conduction layer fabrication sequence

135. As noted above POSAs would have understood that claim 1 requires forming the [1.g.1] conduction layer **before** forming the [1.g.2] conduction layer. Iwabuchi meets this.

136. Iwabuchi describes forming p^+ layer 1054 meeting [1.g.1] through ion implantation.

137. First, p^+ layer 1054 is part of the photodiode (Iwabuchi, [0096]); and the photodiode is formed by ion implantation (Iwabuchi, [0176]). “The photodiode PD is composed of...a heavily-doped p type semiconductor region formed on the interface of the back surface side of the n type semiconductor region, that is, so-called p^+ accumulation layer 1054.” Iwabuchi, [0096].

138. Second, layer 1054 forms a p-n junction with n-type region 1042 (*id.*, Fig. 5). Layer 1054 is doped p^+ , while region 1042 is doped n. This forms a p-n junction where the two layers meet.

139. Third, Iwabuchi makes clear that p-n junctions are formed by ion implantation. *Id.*, [0144] (“[A] pn junction is formed by implanting ions of p type conductive impurities on the n type semiconductor layer 12 and thereby the photodiode 14...is formed in the semiconductor layer 12.”).

140. Ion implantation was conventionally done through the frontside (front surface) of a substrate like Iwabuchi’s SOI wafer (the “second substrate” in the claim), particularly where the backside was covered by a thick layer such as Iwabuchi’s substrate layer 10.

141. POSAs would have understood Iwabuchi as providing reasons to form p+ layer 1054 **before** n-type layers 1052. This follows from the fact that, for several reasons, Iwabuchi describes forming p+ layer 1054 through ion implantation. In other words, while the claims do not require forming conduction layers by ion implantation, the fact that Iwabuchi would form those conduction layers by ion implantation leads to the sequence in which p+ layer 1054 would be formed before n+ layers 1052.

142. POSAs would have understood that layer 1054 is formed by ion implantation directed through the frontside of crystalline layer 12 because ion implantation through thick backside substrate 10 would not have been conventional, and Iwabuchi describes the sensor chip being “formed” (i.e.,

complete) after thinning backside substrate 10 without describing any further ion implantation or other doping. Iwabuchi, [0150]-[0151].

143. Although it was known to form layers like 1054 by implantation from the backside, this would not have been done while the lower substrate 10 of an SOI wafer remained in place. Iwabuchi describes forming layer 1054 while the SOI substrate 10 is in place. As a result, POSAs would have known that the ion implantation forming layer 1054 would have been done through the frontside of Iwabuchi's SOI wafer, and through crystalline layer 12 in particular.

144. This methodology mirrors the '808 patent's description of forming layer 212 by ion implantation through the frontside of substrate 200 before removing the bottom epitaxial layer. Ex. 1001, 3:19-33, 4:47-53, Fig. 8.

145. POSAs would have found it conventional to implant p-type layer 1054 *before* forming graded n-type layers 1052 for several reasons.

146. Iwabuchi's p⁺ layer 1054 is a blanket implant layer just like the '808 patent layer 212. This is a heavily doped and deep layer relative to the frontside surface that would require high energy ion implantation for an extended period of time. Forming layer 1054 by blanket ion implantation in fact mirrors the '808 patent description of forming layer 212 by blanket implant. Ex. 1001, 3:19-33. The blanket implant can be formed without a mask. *Id.* The blanket implant

would cover the entire region used for a focal plane array in the crystalline layer, e.g., where pixels are formed, if not the entire wafer.

147. A POSA would conventionally form this layer 1054 first, then form additional layers or features patterned into shapes over this blanket implant because it was intended that the p+ layer 1054 would be flat and uniform. The POSA would realize that subsequent layers implanted onto the photodiode substrate would be patterned to form the pixel. Therefore, implanting the p+ dopants after patterned layers had been formed would create variability in the p+ implant dose and in the resulting p+ doping with position on the wafer. In order to avoid this complication, POSAs would normally carry out this deep uniform deposition first, and then carry out the patterned depositions; *i.e.*, POSAs would normally think about forming devices from the bottom up. For that reason alone, a POSA would form layer 1054 before forming the n type conduction layer 1052.

148. Moreover, a POSA would have understood that any processing of the crystalline wafer using high-energy ion beams will result in some amount of crystal lattice damage that is normally repaired by heating the entire wafer up to an elevated temperature for a period of time in order to allow the crystalline bonds to be repaired. Sze-2002, 477-480. Further, a POSA would also have known that a high-temperature anneal such as that required to heal high-energy ion implant

crystal damage would also potentially alter the lateral doping concentration and placement of other layers that were already implanted. Sze-2002, 477-480.

149. The POSA would be aware that the higher the energy of the implant ion beam and the higher the dose, the more lattice damage will be done. And, that more lattice damage will require an annealing step that is higher in temperature and/or longer in duration. Ex. 1044 (“Sze-2002”), a standard textbook on semiconductor device physics and technology that would have been familiar to POSAs, discusses this issue at length in Chapter 13 on impurity doping, and in particular at Section 13.5 on implant damage and annealing. Sze-2002, 477-480. In fact, the annealing temperature needed after the heavy p-type doping, for Iwabuchi layer 1054, could be significantly higher than the annealing temperature needed after the much lower dose n-type implant, for Iwabuchi layer 1052, as the POSA would have known from Sze-2002, Figure 22 at 479.

150. Therefore, it would have been clear to a POSA that creating the described structure would best be done by first implanting the p⁺ layer, followed by the necessary annealing, and then the n layer would be diffused or sequentially implanted into the substrate. Layer 1054 would have required a relatively high-energy implantation because it is heavily doped and furthest from the front surface. Sze-2002, 477-480. POSAs would have understood that remediating the crystal lattice damage from such a high-energy implant would have required a relatively

long, high-temperature anneal. *Id.* If layers 1052 were already formed, then the high temperature anneal for the layer 1054 implantation would significantly alter those layer 1052 doping concentrations and placement by causing layers 1052 to diffuse outward and laterally. *Id.*

151. Because the n-type layer is shallower than the p+-type layer, a lower temperature and/or shorter duration annealing would be needed after the n type implants compared to the annealing for layer 1054. Sze-2002, 477-480. The POSA would understand that while the p+ implant could be added after the graded n region was created, the required higher-temperature annealing step would disturb the grading and patterning of the n-type region because the higher thermal energy would enable the n-type dopants to diffuse within the crystalline lattice. POSAs would have known that this problem could be avoided by implanting layer 1054 before layers 1052.

FIG. 5



152. Thus, POSAs would have understood that Iwabuchi described and gave reasons to implement step [1.g.1] **before** step [1.g.2], and that in any event this sequence would have been conventional process flow.

FIG. 5

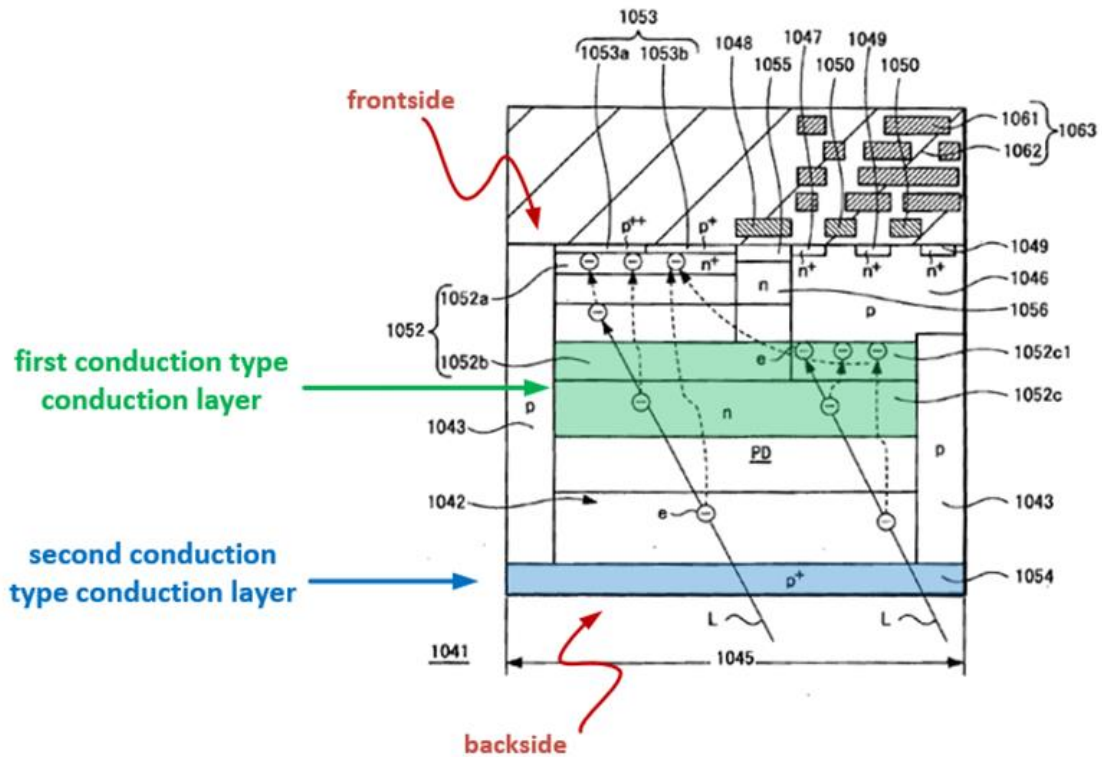
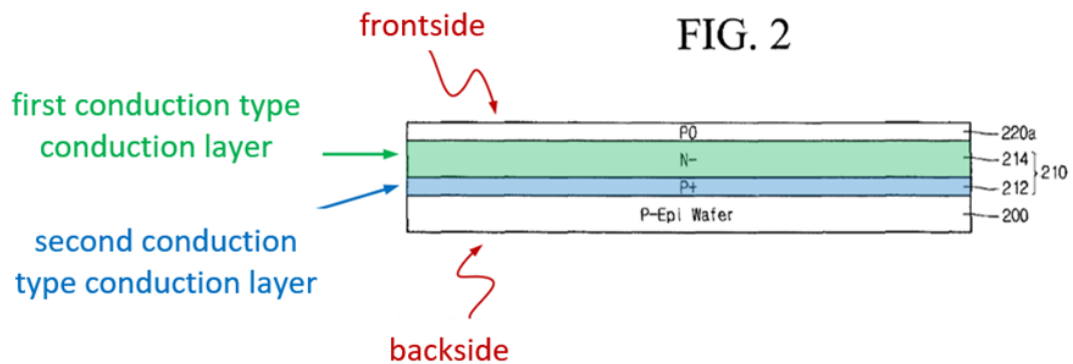


FIG. 2



153. Moreover, Iwabuchi describes forming a potential distribution in n-type conduction layers 1052 in layer 12 “by controlling the impurity concentration” in the vertical direction by “stepwise increasing the n type impurity

concentration” in layer 1052 both “from the back surface side of the substrate to the substrate surface side,” and from layer 1052c1 to layer 1052a. *Id.*, [0100], [0101].

154. POSAs would have understood that a conventional way to stepwise increase the n-type impurity concentration in layers 1052 would have been through either serial ion implantation at different depths in the substrate (*e.g.*, Masagaki, [0030], describing ion implantation “being divided into several implantations in the depth direction”) or through diffusion of n-type dopants from the surface of the substrate. Sze-2002, 477-480. POSAs would have understood that this conventional approach was applicable because—as explained for step [1.c] (*supra* § V.B.1.d.i)—Iwabuchi describes forming the photodiode in the crystalline layer rather than forming these graded conduction layers by other methods, such as growing epitaxial layers with different doping concentrations.

155. As discussed above with layer 1054, it would have been conventional to form the stepwise doping grading in layers 1052 by ion implantation from the backside to the topside in Figure 5. Thus, Iwabuchi describes forming n-type conduction layers 1052 *after* p+ layer 1054, and POSAs would have understood that this sequence would have been conventional.

f. Isolation layers

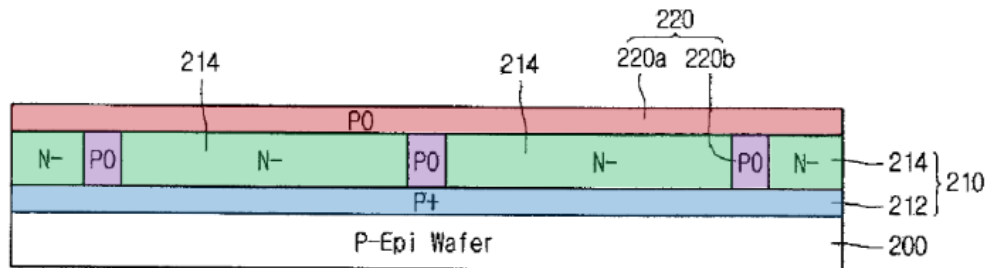
i. Step [1.d]

1.d	forming an ion implantation isolation layer in the photodiode;
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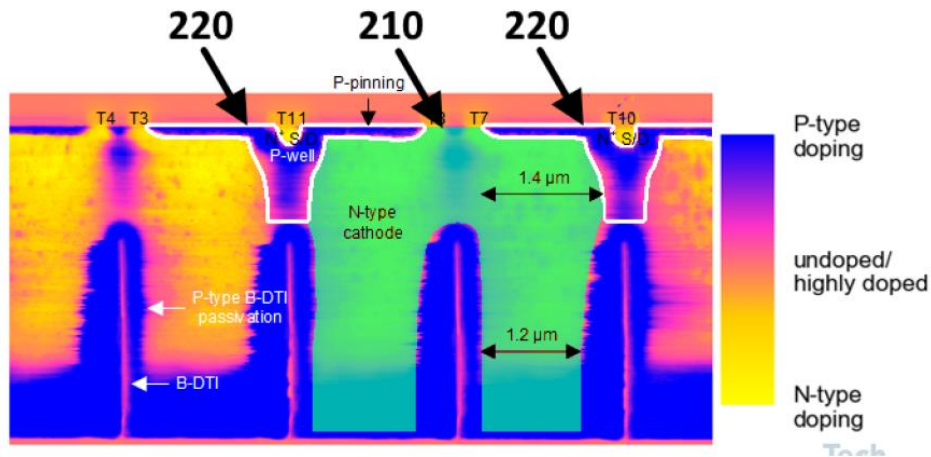
156. The '808 patent specification describes isolation layers as providing “pixel-to-pixel isolation” by “insulating” adjacent “pixels” from each other, comparing the functionality to the prior art shallow trench isolation (STI). Ex. 1001, 3:44-61, 4:2-4, 4:56-60. At the same time, the '808 patent describes the isolation layer as a ground line (not an insulator). Ex. 1001, 4:2-4. From these two facts, a POSA would conclude that the isolation layers must be oppositely doped to the collection region itself. For the case of a pixel that has an n-type core this would be a p-type isolation region. Iwabuchi’s p type implants provide isolation just like the p-type implants that PO identifies as “isolation layers” in its infringement contentions. IC-A1, 16 (“Isolation layer 220 isolates pixels from each other.”) The p-type regions PO’s contentions identify as “[a]n isolation layer (labeled 220)” border n-type regions and form p-n junctions exactly like the Iwabuchi isolation layers described for [1.h.1] and [1.h.2]. *Id.*

157. POSAs would have understood that the isolation layer prevents carriers generated outside a pixel from crossing into a pixel and being collected with photogenerated carriers. The reverse is also true because the designer does not want photogenerated carriers to escape the photodetector, which would reduce sensitivity.

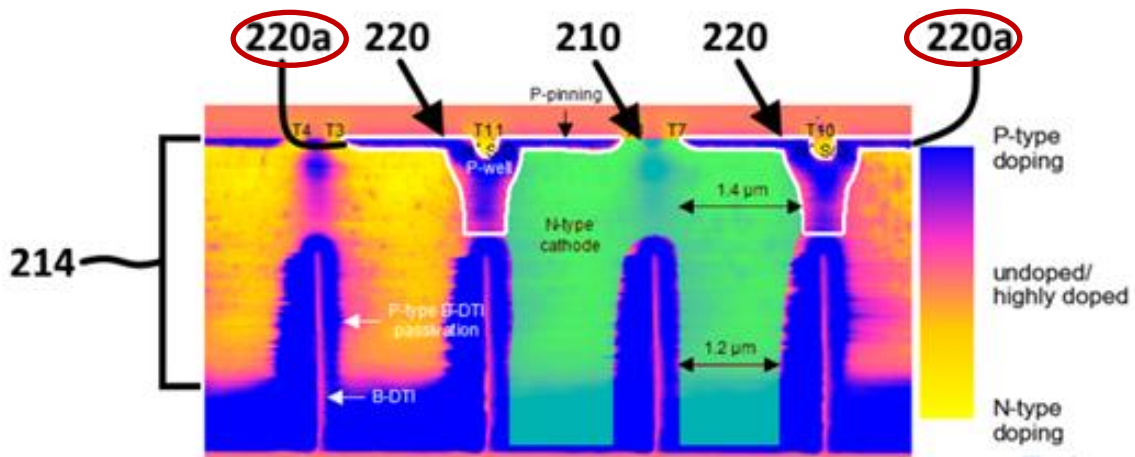
158. When alleging infringement PO mapped the [1.h.1] isolation layer to a p+ pinning layer between photodiode and the frontside surface of the second substrate, and the [1.h.2] isolation layer to a “P-well” structure between n-type regions of adjacent “pixels,” adding labels corresponding to reference numerals 220a and 220b in ’808 patent Figure 3. *E.g.*, IC-A1, 16, 25, 27.



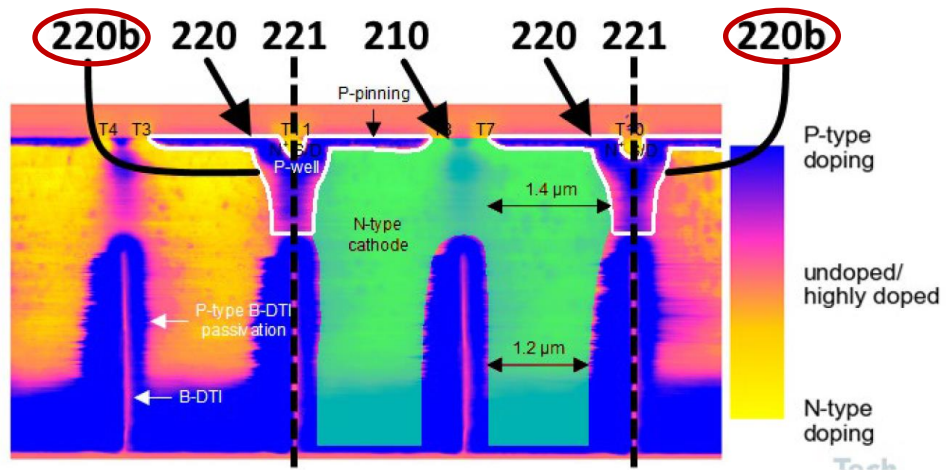
159. Without explanation, PO’s infringement contentions assert that ion implantation isolation layer “220” is formed “*in the photodiode*” identified as “210,” adding labels corresponding to reference numerals 220 and 210 in ’808 patent Figure 3. IC-A1, 16 (“An isolation layer (labeled 220) of P-type impurity ions is formed *in photodiode 210*. Two regions of P-type impurity ions collectively correspond to isolation layer 220: a P-type implant isolation layer, and a P-type pinning layer.”); Ex. 1001, Fig. 3.



160. PO's infringement contentions on step [1.h.1] at IC-A1, 25 provide:



161. PO's infringement contentions on step [1.h.2] at IC-A1, 27 provide:



162. As explained for steps [1h.1] and [1.h.2], Iwabuchi discloses the same two isolation layers that PO labels 220 in its contentions.

163. Iwabuchi meets step [1.d] for the reasons explained for steps [1.h.1] and [1.h.2].

ii. Step [1.h.1]

1.h.1	wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer over the first conduction type conduction layer ,
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164. Iwabuchi meets [1.h.1] in at least two ways.

(1) p-region 1046

165. First, “p type semiconductor well region 1046” provides a “second conduction type isolation layer” “over” the “first conduction type” conduction layers 1052c1 and 1052c because region 1046 is “higher than” (e.g., above) layers 1052c and 1052c1. Iwabuchi, [0096], Fig. 5; *supra* § V.B.1.d.ii (discussing “over”).

166. This is consistent with PO’s infringement contentions, IC-A1, 16, 25, 27, treating a p-well as an isolation layer. Like Iwabuchi’s p-well region 1046, the “P-well” in PO’s infringement contentions contains a CMOS transistor source or drain, marked “N⁺ S/D”. *E.g.*, IC-A1, 16; *accord id.*, 25, 27. In other words, the p-well in the infringement contentions, and the p well region 1046 in Iwabuchi, serve multiple functions that include providing a p type material in which to form

n-type CMOS transistor source or drain, and—for purposes of claim 1—providing an isolation layer.

167. Region 1046 is “in the photodiode” because Iwabuchi expressly describes the p-n junction between p-region 1046 and n-type conduction layers as directing photogenerated electrons towards accumulation region 1052a. Iwabuchi, [0096]-[0097], [0102]-[0103], Fig. 5 (dashed line indicating photogenerated electron drift from 1052c1 to 1052a). That means p well region 1046 provides an electric field and a p-n junction that is part of the photodiode. Directing photogenerated electrons to the accumulation layer also provides carrier isolation between adjacent pixels in the volume including region 1046, and between the pixel and the materials at the frontside surface interface for the pixel. n type semiconductor region 1052c under the p type semiconductor well region 1046.” *Id.*, [0098].

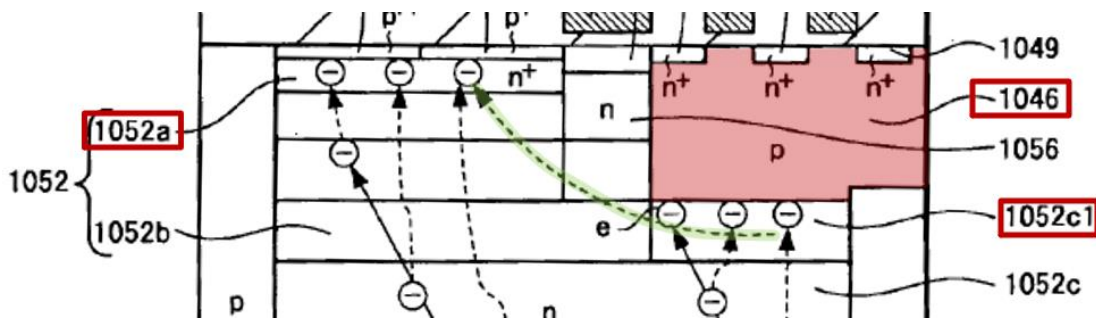
168. The electric field that separates photogenerated electrons by lateral motion under p-well region 1046 is established by forming a lateral doping gradient in p-well 1046. “As another example of methods of forming the above-described potential distributions...the above-described potential distribution of substantially the lateral direction can be formed by progressively or stepwise decreasing the p type impurity concentration of the portion adjoining the n type semiconductor region 1052c1 of the p type semiconductor well region 1046 toward

the n type electric charge accumulation region 1052a under the condition in which the n type impurity concentrations of the n type semiconductor regions 1052b and 1052c are made constant similarly.” *Id.*, [0102]. This means that p-well 1046 is in the photodiode because it provides a high electric field (the lateral potential distribution) that serves to separate photogenerated electron-hole pairs and direct the electrons to the accumulation layer 1052a.

169. Figure 5 shows this relationship. The solid-line rays marked “L” show light incident on the backside surface and passing through p+ layer 1054. The light comprises photons. The encircled “-” icons represent electrons that are photogenerated, with holes, when incident photons are absorbed, generating an electron-hole pair. These are shown at different points along the same rays marked “L” to indicate that a single incident ray has many photons and their absorption—and accompanying carrier generation—occurs at many points in the substrate. The photogenerated holes are not shown. In other words, in the process of photogeneration a photon is absorbed by an electron bound to a crystal atom. The photon’s energy promotes the electron to a conduction band, and leaves behind a “hole” in the valence band. This is what is meant by a photogenerated “electron-hole pair.”

170. Both electrons and holes have mobility in a crystal lattice, so the photogenerated electron is a mobile negative charge and the hole is a mobile

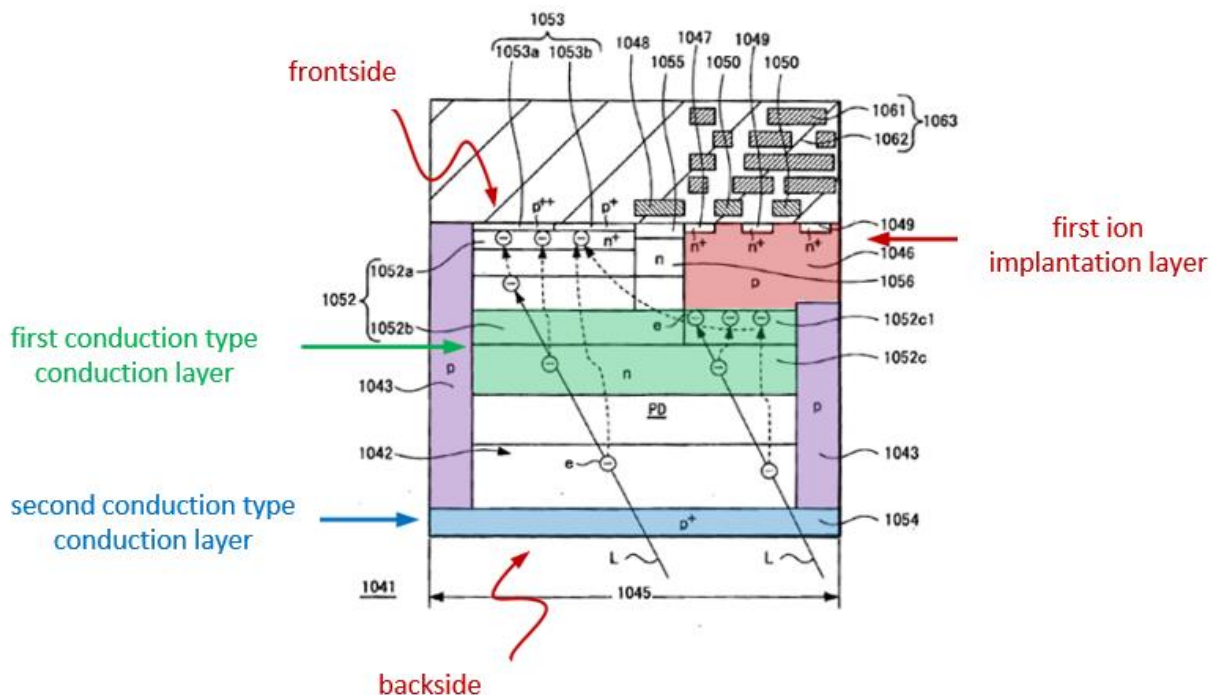
positive charge. The dashed lines in Figure 5 represent the direction of motion that photogenerated electrons follow along electric field lines from low to high potentials. The electrons flow towards positive or higher potentials while the holes flow towards negative or lower potentials. This is why the electric field in the depletion region separate photogenerated charges. The arrow curving from the electrons shown at the interface of 1052c1 and 1046, to 1052a, shows the photogenerated electron flow along the electric field established in part by the lateral doping in p-well 1046 as explained above and in part by the vertical electric field in 1052 as explained above.



171. Iwabuchi describes forming p-region 1046 by ion implantation because as I just explained p-type well 1046 forms a p-n junction with n-type layer 1052, defining part of the photodiode in the unit pixel. Iwabuchi, [0096].

172. As I noted above, Iwabuchi explains that p-n junctions are formed by p-type ion implantation. Iwabuchi, [0144]. A POSA would have known that a p-n junction is the result of a p-type region being adjacent to an n-type region. Sze-2002, 85-127.

FIG. 5



173. In any event, POSAs would have known that it would have been conventional to form p-type region 1046 by ion implantation. *E.g.*, Suzuki, [0057], Fig. 4 (“deep P well 43” formed by ion implantation).

174. POSAs would also have understood that creating a progressive doping distribution in p-region 1046 to provide the lateral “progressive[] or stepwise” doping distribution described in Iwabuchi, [0102], would conventionally have been done by multiple masks and multiple ion implantations.

175. POSAs would have been motivated to form p-well 1046 by ion implantation because this would have provided better control over the doping profile and shape of the implant than basic diffusion. *E.g.*, Sze-2002, 453, 469

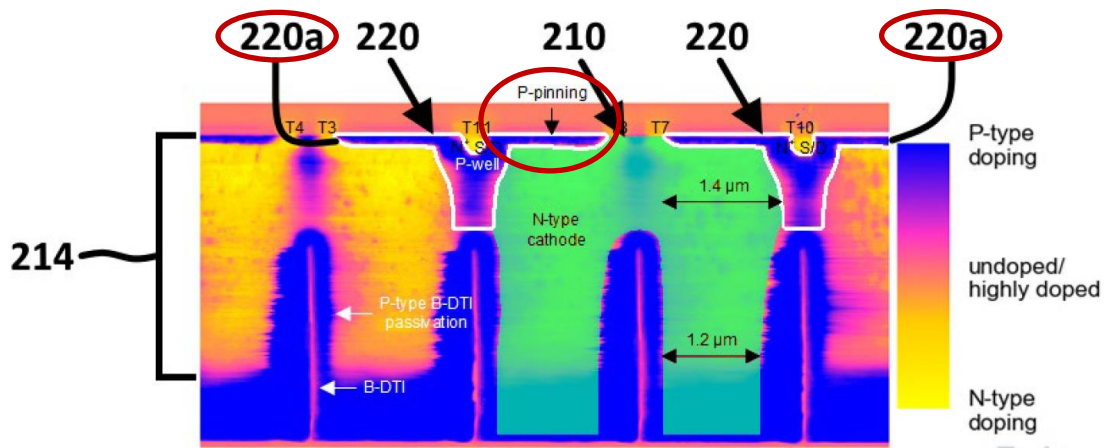
(“The main advantages of ion implantation are its more precise control and reproducibility of impurity dopings and its lower processing temperature compared with those of the diffusion process.”); Sze-1981, 70 (“The main advantages of ion implantation include (1) precise control over total dose, depth profile, and area uniformity; (2) low-temperature processing; and (3) implanted junctions that can be self-aligned to the edge of the mask.”).

176. By December 2007, excepting regions formed by doped epitaxial growth, virtually all semiconductor device structures—including p-wells like 1046—were formed by ion implantation. ULSI, 153 (“The preferred process for introducing dopants in Si is ion implantation since it is controllable and there is no residual source material to remove.”). This provided more precise control of dopants, flexibility in forming desired dopant profiles, and reducing the time at high temperatures required for diffusion. *E.g.*, Sze-2002, 469-476; ULSI, 153; Sze-1981, 70.

177. POSAs would also have understood that forming p-region 1046 by ion implantation would have meant forming it **after** forming n-type conduction layers 1052c1 and 1052c, for the reasons discussed with step [1.g.1], and that this sequence would have been conventional. *Supra* § V.B.1.e.

(2) p-layer 1053

178. In its infringement contentions PO asserts that the [1.h.1] isolation layer (corresponding to '808 patent layer 220a) is met by a highly-doped p-type shallow planar layer that it labels “P-pinning.” IC-A1, 25. Based on the contentions “isolation layer” includes a pinning layer between the n-type conduction layer and the “frontside” surface of the “second” substrate, as well as between the n-type conduction layer and the “first” substrate.

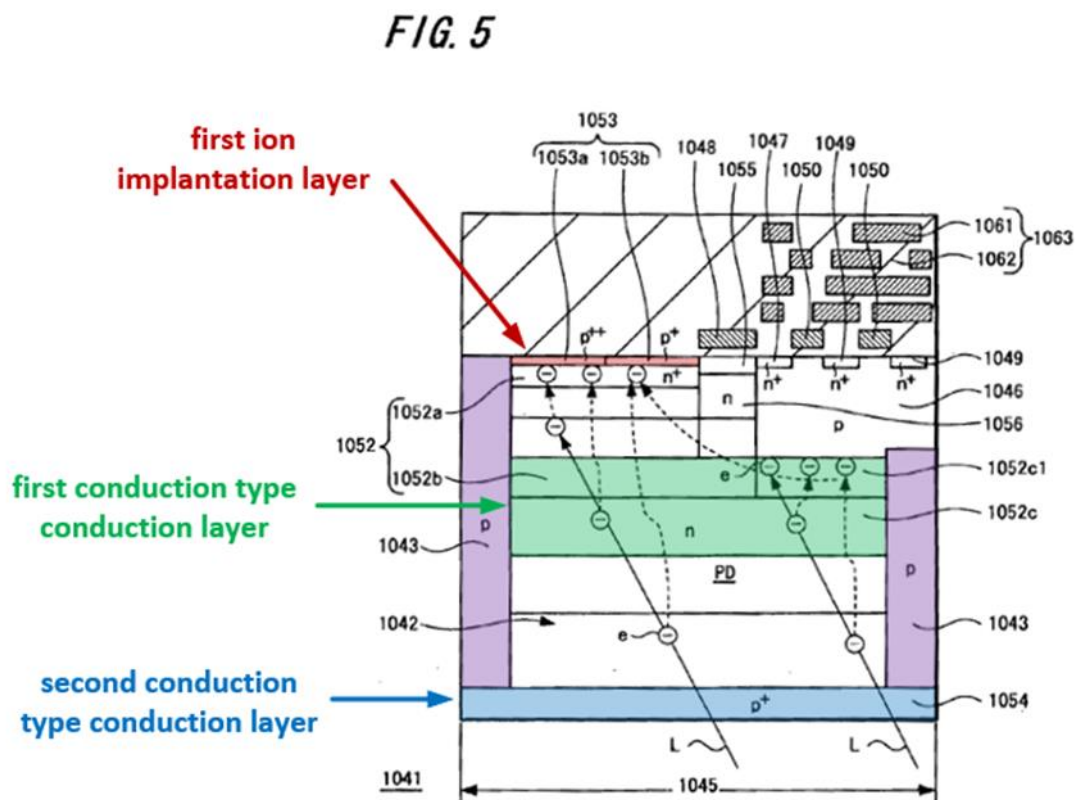


PO infringement contention (IC-A1 at 25).

179. Based on PO’s infringement contentions, Iwabuchi p++/p+ layer 1053 is a “second conduction type” isolation layer meeting [1.h.1]. POSAs would have understood that layer 1053 is a pinning layer, exactly like the pinning layer PO’s contentions map to [1.h.1]. IC-A1, 25 (“Forming ion implantation isolation layer 220 in photodiode 210 comprises *forming a pinning layer (labeled 220a)* of P-type impurity ions over first conduction type conduction layer 214.”); Guidash, Abstract, 4:43-45 & Fig. 4 (pinning layer 34). A pinning layer creates a p-n

depletion region that forces mobile photocharges away from the surface which typically has higher defects. While PO only labels one structure a “pinning layer” in its contentions, that same structure provides a pinning layer at each point where it is replicated across the image in PO’s contentions.

180. As shown in Figure 5, layer 1053 is “over” the “first conduction type conduction layer” 1052 from step [1.g.2] because layer 1053 is “higher than” (e.g., above) layers 1052c and 1052c1. Iwabuchi, Fig. 5; *supra* § V.B.1.d.ii (discussing “over”).



181. Layer 1053 is “in the photodiode.” Iwabuchi, [0096] (“The photodiode PD is composed of... a heavily-doped p type semiconductor region

formed on the interface of the surface side of the n type semiconductor region 1052, that is, so-called p⁺ accumulation layer 1053.”). It also defines a p-n junction with the n⁺-type accumulation layer 1052a.

182. Iwabuchi describes forming layer 1053 by ion implantation, for the same reasons discussed for layer 1054. Iwabuchi, [0144]; *supra* § V.B.1.d.ii (step [1.g.1]).

183. It was conventional to form a pinning layer like 1053 by ion implantation. *E.g.*, Guidash, 8:16-19; Maruyama, [0023] (accumulation layer 12). Maruyama’s accumulation layer 12 is conventionally described as a pinning layer and in any event serves the same function in the same location as Iwabuchi layer 1053.

184. Moreover, Iwabuchi describes laterally grading the p⁺ impurity concentration in layer 1053. Iwabuchi, [0104]. POSAs would have understood that ion implantation was a conventional way to achieve a lateral doping gradient.

185. POSAs would have formed layer 1053 by implantation ***after*** forming n-type conduction layers 1052 in step [1.g.2] because layer 1053 was the shallowest layer and would be formed last when implanting from deepest to shallowest.

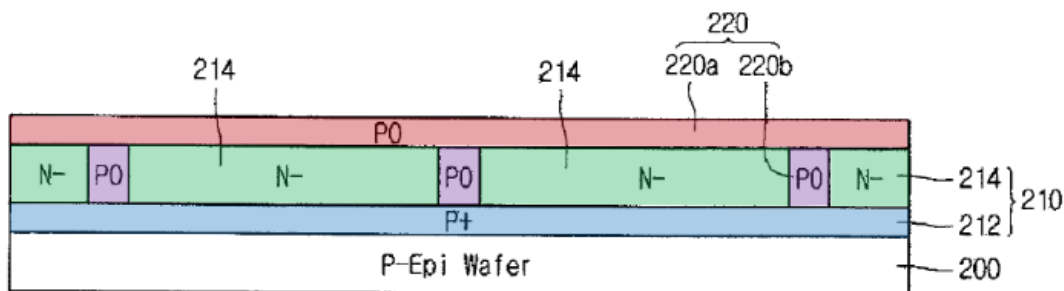
186. This process sequence would have been conventional for the reasons discussed in step [1.g.1]. *Supra* § V.B.1.d.ii (step [1.g.1]).

iii. Step [1.h.2]

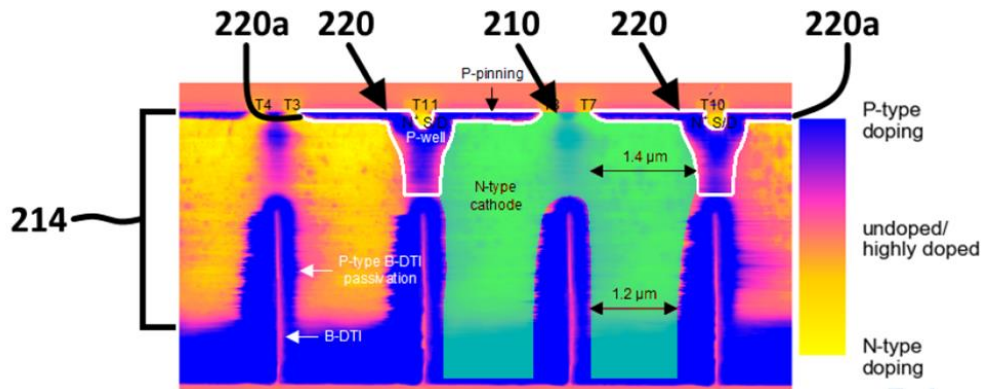
1.h.2	wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.
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187. The PO's infringement contentions show a colorized result of a cross sectional depiction of an accused product. In these contentions the PO appended labels that appear to correspond to isolation layers 220a and 220b of "isolation layer 220" in the '808 patent.

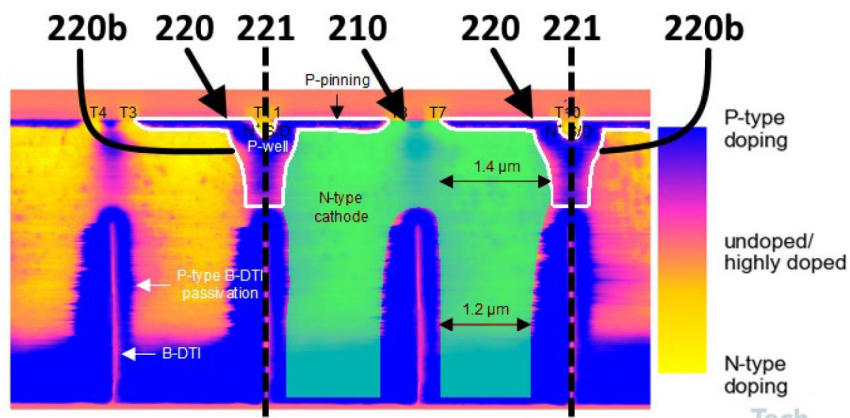
FIG. 3



188. For step [1.h.1], PO's infringement contentions show this cross section (IC-A1, 25):



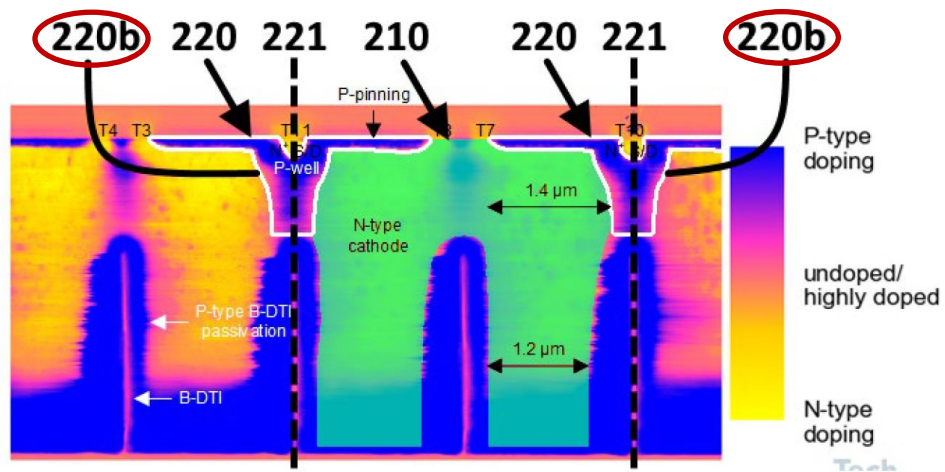
189. For step [1.h.2], PO's infringement contentions show this cross section (IC-A1, 27):



190. While the color bar reference to “undoped/highly doped” cannot simultaneously be true for any region, the contentions suggest that dark blue corresponds to regions with high p type doping concentrations, while yellow corresponds to regions with high n type doping concentrations, and magenta / orange seems to denote a region that transitions from p to n type doping (or the reverse).

191. Based on PO's contentions isolation layer "220b" at an interface "221" between pixels of *adjacent photodiodes* is "*in the photodiode...*at an interface between pixels of *the photodiode*" so that both Iwabuchi region 1046, and Iwabuchi separation region 1043, each in the alternative (or together) meet [1.h.2]. IC-A1, 27 (below). PO argues that the accused sensors as shown in the infringement contentions comprise "photodiodes" (plural). IC-A1, 6.

192. The orange and green colorations in the infringement contentions correspond to adjacent photodiodes in an accused product. IC-A1, 27 (red circles added):



193. Based on PO's contentions Iwabuchi p-well 1046 meets [1.h.2] just like "P-well" "200b". IC-A1, 27. As noted above with step [1.h.1], Iwabuchi p-well 1046 is formed by ion implantation. *Supra* § V.B.1.f.ii(1). Iwabuchi p-well 1046 is p-type, it provides isolation, and based on the PO contentions it is "at an interface between pixels of the photodiode" just like the region that PO labels "P-

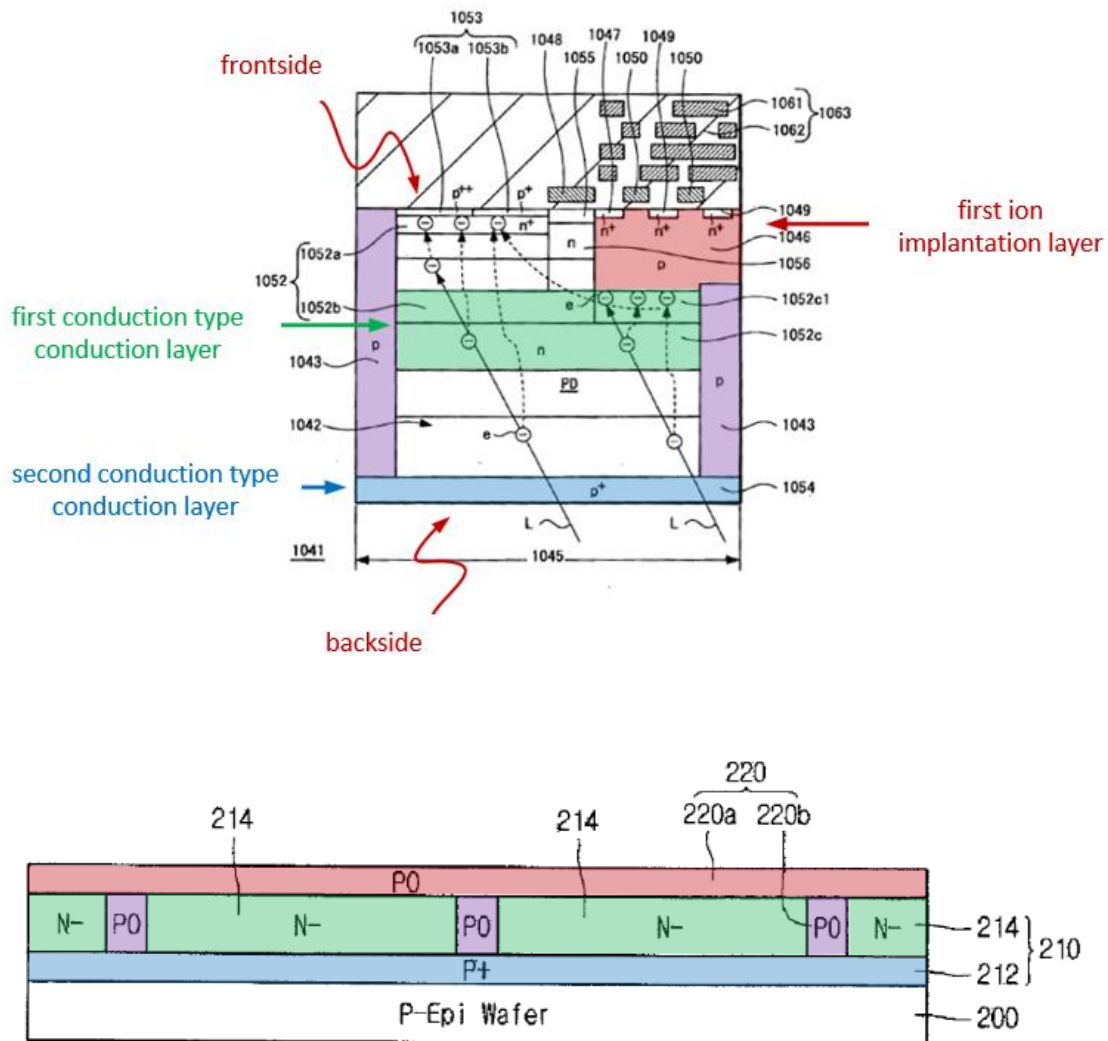
well” and “200b” in the contentions. Figure 5 defines a “unit pixel 1045.”

Iwabuchi, [0094] & Fig. 5. “A large number of unit pixels 1045 are arranged in an XY matrix fashion[.]” *Id.*, [0094]. POSAs would have understood that in this pixel array another pixel would be located adjacent to unit pixel 1045 in Fig. 5, so that p-well region 1046 is “at an interface between pixels of the photodiode” exactly like PO shows for “P-well” marked “200b” in the infringement contentions. IC-A1, 27.

194. If p-region 1046 is identified as step [1.h.1]’s “first ion implantation layer,” then region 1043 is step [1.h.2]’s “second ion implantation layer.” If p^{++/+} layer 1053 is step [1.h.1]’s “first ion implantation layer,” then step [1.h.2]’s “second ion implantation layer” can be either region 1043 or region 1046.

195. Separation region 1043 also meets [1.h.2]. It is also p-type (“second conduction type”). *Supra* § V.B.1.d.ii. Forming pixel separation region 1043 “divides respective pixels[.]” *Id.*, [0094]. Region 1043 is “at an interface between pixels of the photodiode” because it defines the pixel boundaries in the same manner as 220b in the ’808 patent, Iwabuchi, [0094], [0095], Fig. 5; Ex. 1001, Fig. 3, and just like the region labelled “P-well” and “220b” in PO’s contentions. IC-A1, 27.

FIG. 5



196. Separation region 1043 is also “in the photodiode” because it forms a p-n junction at each interface with adjacent n-type regions 1052. Iwabuchi, Fig. 5.

197. The “separation” region 1043 provides isolation because the p-n junction repels photogenerated electrons and directs them back into the n-type layers, preventing their lateral movement to adjacent photodiodes (and pixels). Iwabuchi, Fig. 5. These p-n junctions create an electric field going from the n type

region to the p type region over a space called the depletion region. This electric field drives mobile electrons back into the n-type region.

198. Pixel separation region 1043 is formed by ion implantation because it forms a p-n junction with n-type layer 1052, defining part of the photodiode in the unit pixel. Iwabuchi, [0102], Fig. 5. As noted above, Iwabuchi explains that p-n junctions are formed by p-type ion implantation. Iwabuchi, [0144].

199. Moreover, it would have been conventional to form separation region 1043 by ion implantation. In one embodiment Iwabuchi describes forming separation region 1043 by stepwise decreasing the p-type doping level along the vertical axis in Fig. 5. Iwabuchi, [0058], [0102].

200. POSAs would have understood that it was well-known and conventional to form a vertical stepwise doping gradient through a series of ion implants. *E.g.*, Masagaki, [0030] (describing ion implantation “being divided into several implantations in the depth direction”). POSAs would also have known that even without a stepwise gradient it was conventional to form pixel separation regions by ion implantation. *E.g.*, Maruyama, [0023]; Suzuki, [0057] & Fig. 4 (“deep P well 43” formed by ion implantation); Gouscha, 3:24-30 & Fig. 2 (implanting diffusion 8). Suzuki deep P well 43 is a combination of p layers 1043 and 1046 in Iwabuchi.

of a pixel of the photodiode.” IC-A1, 17. This “facilitates electrically connecting the photodiode and ISP metal interconnects.” *Id.*

The ***ISP and CIS dies are bonded together***, and ***thus, corresponding ISP Si substrate 100 and CIS Si substrate 200 are bonded together***.

The bonding facilitates electrically connecting the photodiode and ISP metal interconnects 115. The figure depicts a column DBI which electrically connects a column out transistor of a pixel of the photodiode to ISP metal interconnects 115.

The photodiode and ISP metal interconnects 115 ***are electrically connected*** concurrently ***when ISP Si substrate 100 and CIS Si substrate 200 are bonded***.

IC-A1, 17.

203. Iwabuchi shows the same structure that PO contends meets step [1.e], *e.g.*, a pixel readout, from photodiode 200, through a column out transistor 250 output to line 260. Iwabuchi, [0133] (“[S]ignals of respective pixels are read out... at every pixel column through the vertical signal line 260.”); *id.*, [0088] & Fig. 9.

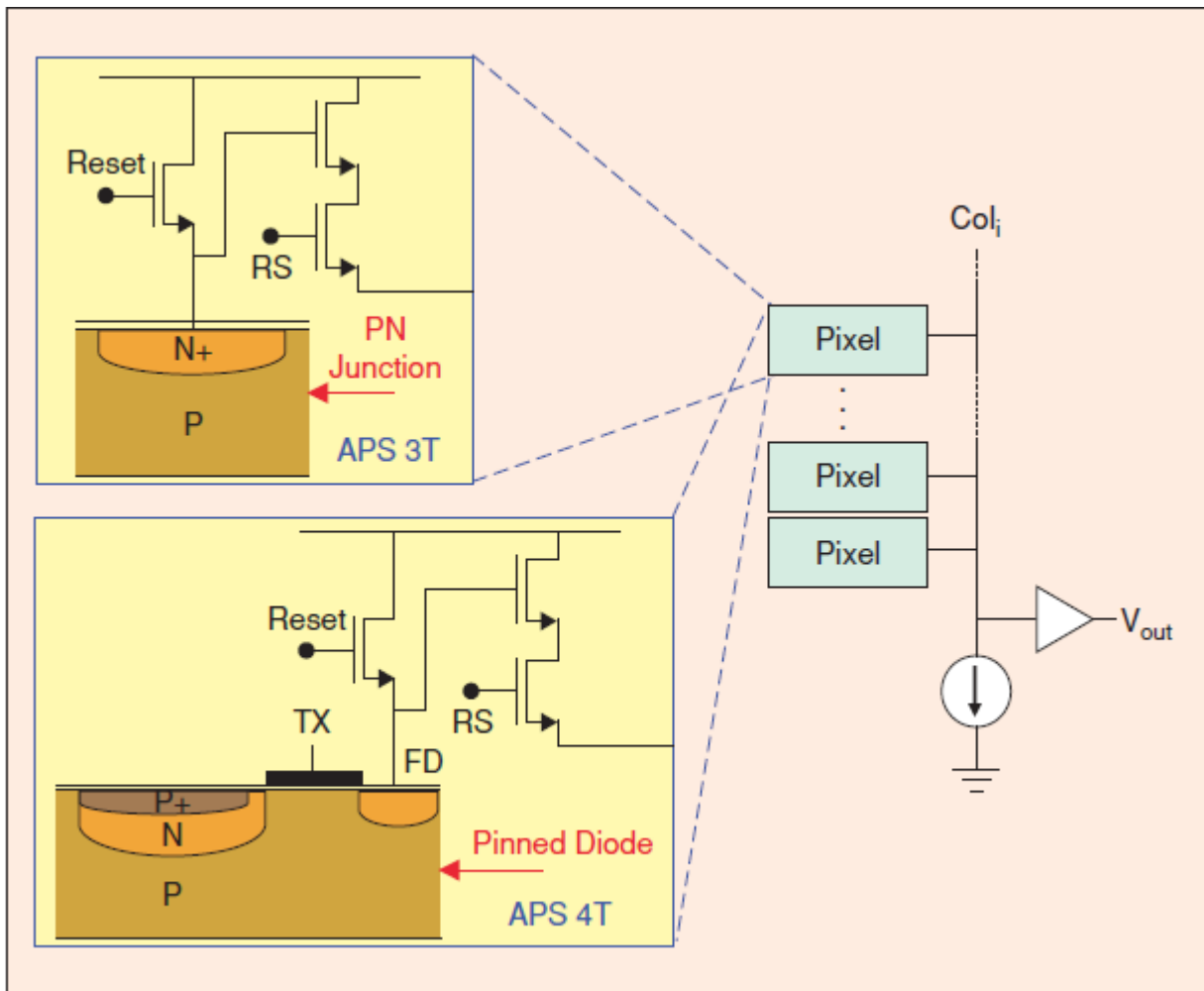
204. As I explained above, *supra* § V.B.1.d.i (step [1.c]), Iwabuchi’s Figures 10A to 10G provide process steps for making the photodetector, and photodiode, in Iwabuchi Fig. 5. Figure 5 provides detail about the specific features making the unit pixel, photodiode, and various readout transistors. Figures 10B to 10G label the photodiode as 14 as formed in crystalline layer 12 on the SOI wafer comprising layers 10, 11, and 12. *Supra* § V.B.1.d.i (step [1.c]). These process

step figures do not address the photodiode internal structure like Figure 5.

Iwabuchi's Figure 9 provides a readout circuit diagram that labels the same photodiode with 200 as a circuit element. Despite the different numbers associated with the photodiode in the different figures, POSAs would understand that each of these figures refers to the same photodiode shown in Iwabuchi Figure 5.

205. Vertical signal line 260 connects to the DSP chip, which includes the CDS (correlation double sampling) circuit identified in Figure 9. Iwabuchi, [0020], [0130].

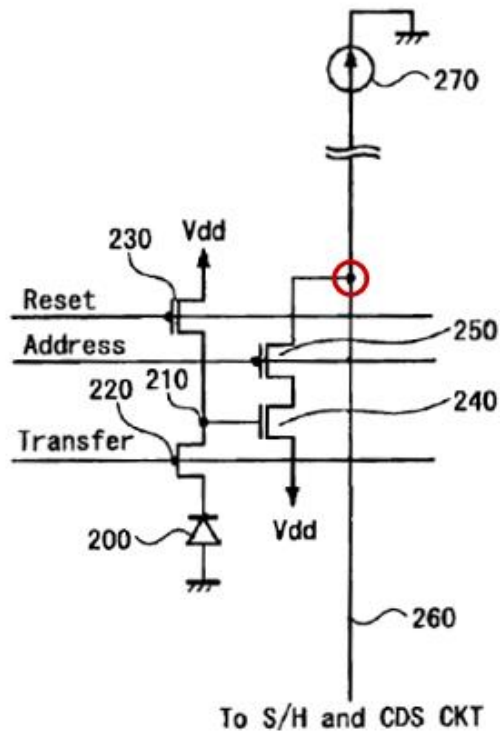
206. Iwabuchi describes a more sophisticated approach than the one described in the '808 patent because Iwabuchi incorporates transistors into the photodiode array, whereas the '808 patent specification describes only the case where all of the transistors are placed on the DSP substrate. There are many different kinds of photodiode substrates: (1) photodiodes only, (2) a single select transistor for each pixel, (3) a three transistor (3T) cell that includes a charge transfer transistor, a source follower transistor and a select transistor, (4) a four transistor (4T) cell that includes a charge transfer transistor, a reset transistor, a source follower transistor and a select transistor (shown in Fig 9 below). *See, e.g.,* Gamal, 8-12. Gamal Fig. 5 illustrates the difference between 3T and 4T circuits as follows:



5. A schematic of a 3- and 4-T active pixel sensor (APS).

207. In all of these cases, there is a conduction path from the photodiode through to the metal output pads at some point during each image readout process.

FIG. 9



208. Based on PO's infringement contentions, Iwabuchi meets [1.e] for the interconnection on each alternative first substrate described *supra* § V.B.1.c (step [1.b]), because in each case when the first and second substrates are "bonded" line 260 connects to the CDS circuit on the DSP chip through metal interconnections on the supporting substrate 30, and through metal interconnections on the DSP chip, as well as through metal interconnections on the interposer when it is used as the first substrate.

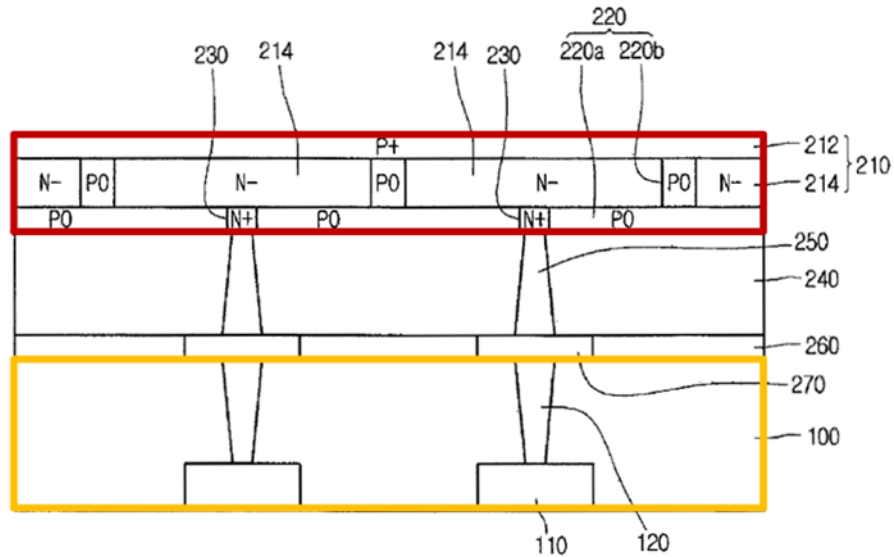
ii. “bonding the first substrate to the second substrate”

209. Based on the '808 patent specification either “bonding” does not require direct contact, or “substrate” includes layers formed in process steps after the substrate is “provided” in steps [1.b] or [1.c].

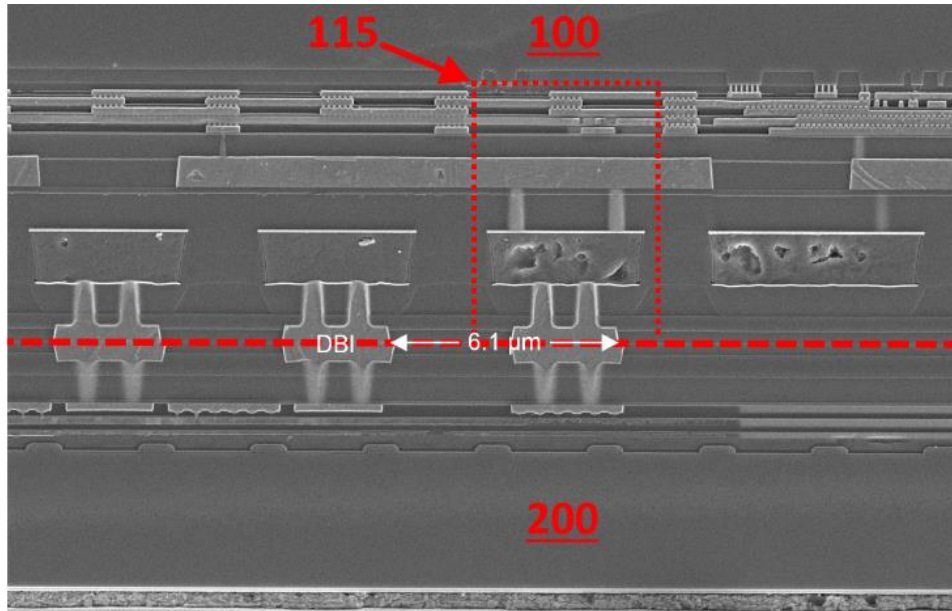
210. The '808 patent specification does not provide a single embodiment in which a first and second substrate are bonded with ***direct contact*** between the substrates.

211. The only bonding embodiment interposes dielectric layers 240 & 260, plug 250, and contact 270 between the “second substrate 200” and the “first substrate 100” when bonded. Ex. 1001, Fig. 8; *id.*, 4:8-10 (“[F]irst dielectric 240 may be formed on and/or over second substrate 200.... [M]etal plug 250 may then be formed.”), 4:15-16(“[S]econd dielectric 260 may be formed on and/or over photodiode 210 of second substrate 200.”), 4:20-21 (“[S]ubstrates may be bonded after forming dielectric 260 and a metal pad 270.”).

FIG. 8



212. In order to cover the embodiments disclosed in the '808 patent specification, step [1.e] “bonding the first substrate to the second substrate” requires either that (a) “substrate” means an originally-identified substrate as modified by subsequent process steps, or (b) “bonding” substrates includes joining substrates through intervening layers (like dielectrics 240 or 260) without requiring direct contact between originally-defined substrates.



PO infringement contention mapping step [1.e] “bonding” (IC-A1, 17).

213. PO’s infringement contentions equate bonding **dies** (chips) to bonding **substrates** contained in a die, by asserting that step [1.e] “bonding” is met when “[t]he ISP and CIS **dies** are bonded together, and thus, corresponding ISP Si substrate 100 and CIS Si substrate 200 are bonded together,” relying on a micrograph that purports to show bonding between metal contacts and dielectric surfaces disposed between “substrates” “100” and “200.” IC-A1, 17.

214. In PO’s contentions, the ISP and CIS **dies** include metal and dielectric layers formed on silicon (Si) substrates. PO’s contentions encompass physical contact between layers added to substrates “100” or “200,” and thus adopts the above usage from the ’808 patent specification.

215. Based on PO’s infringement contentions, each “first substrate” identified *supra* § V.B.1.b (step [1.a]) is bonded to the second substrate (with

semiconductor layer 12), under either meaning of “bonding...substrate[s]” in the ’808 specification.

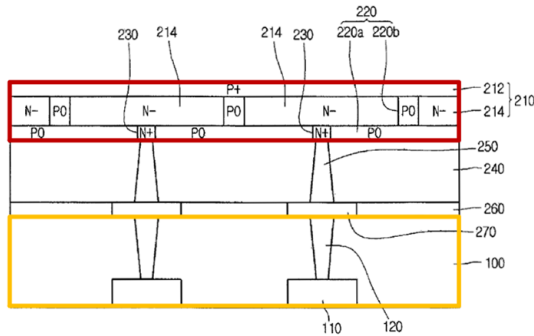
(1) interposer

216. The sensor chip “is mounted on the interposer through bump 32 by flip-chip bonding” using compression bonding. Iwabuchi, [0153] (“[L]ands and bumps on the wirings of the interposer and bumps on the supporting substrate of the sensor chip may be compression-bonded together at a temperature lower than a melting point of wirings used within the sensor chip and the signal processing chip and also at a temperature in which bumps can be electrically connected together with high stability.”).

217. This bonds the second substrate to the interposer through intervening layers, in the same way the ’808 patent describes bonding substrate 200 to substrate 100, and just as PO maps step [1.e] in its infringement contentions. Ex. 1001, 4:25-31 & Fig. 7; IC-A1, 17.

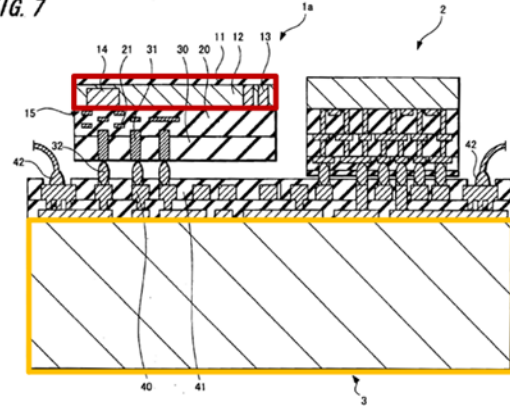
218. The annotated figures show the second substrate 200 (red) and first substrate 100 (orange) in the ’808 patent and Iwabuchi.

FIG. 8



'808 patent

FIG. 7



Iwabuchi

(2) supporting substrate

219. The supporting substrate is “bonded to the upper layer of the interlayer insulator 20 by a suitable method such as thermo compression bonding using a thermosetting resin as an adhesive.” Iwabuchi, [0146], Fig. 10C. The insulator layer 20 is formed on semiconductor layer 12, *id.*, [0145], the same way that the '808 patent describes forming “first dielectric 240” (which can be “an oxide layer”) “over second substrate 200.” Ex. 1001, 4:8-12, Figs. 5, 8.

(3) DSP substrate

- 92 -

compression bonding the sensor chip 1a to the interposer 3. Compression bonding is a form of clip chip bonding that avoids using solder.

222. It was well-known to flip-chip bond die together with metal lands on one die receiving bumps on another die. *E.g.*, Iwabuchi-762, [0047] & Fig. 1; Rogalski, 82-83 (flip-chip bonding using indium bump) & Fig. 14 (below); Balcerak, 386 & Fig. 1 (same).

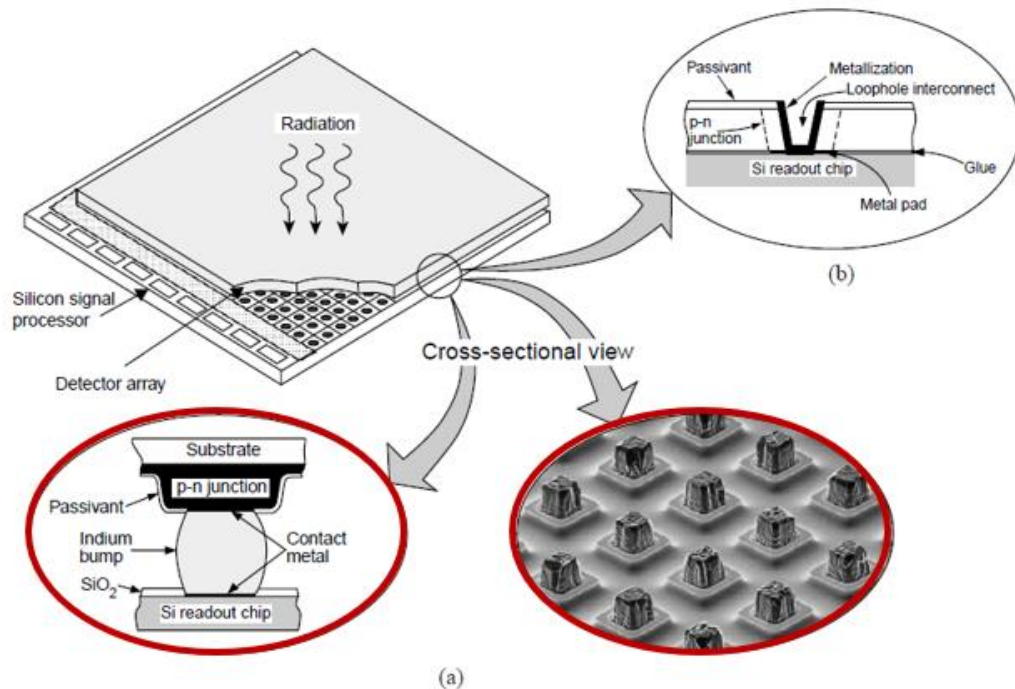
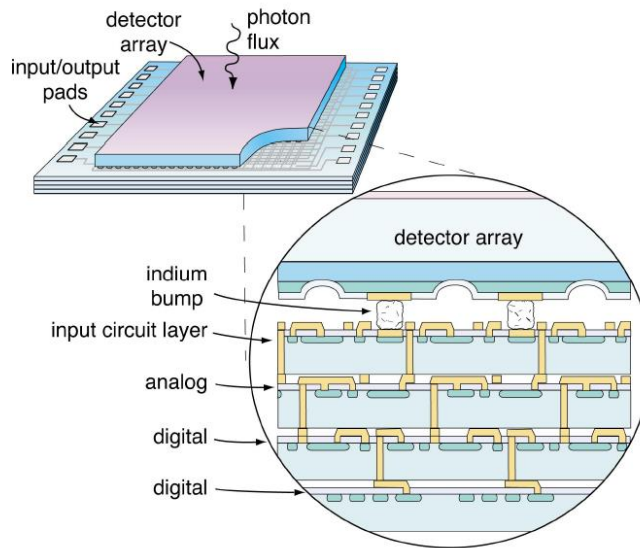


Fig. 14. Hybrid IR FPA with independently optimised signal detection and readout: (a) indium bump technique, (b) loophole technique.

Rogalski, Fig. 14

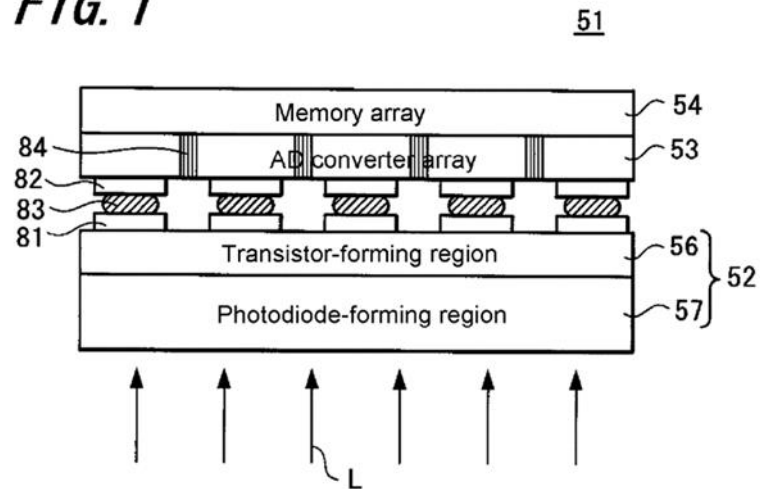


Balcerak, Fig. 1

223. Iwabuchi-762, a published international patent application also naming Shin Iwabuchi an inventor like the Iwabuchi reference used here, illustrates the suggestion, Iwabuchi, [0153], that the sensor die be flip-chip bonded directly to the DSP chip.

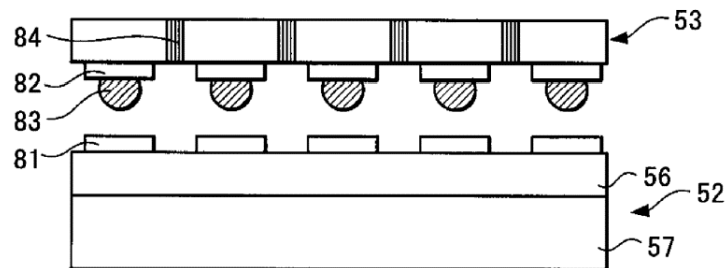
224. Iwabuchi-762 shows at least two ways to flip-chip bond sensor and electronics chips. First, Fig. 1 shows conventional flip-chip bonding. “First semiconductor chip 52” comprises a photodiode-forming region and transistor forming region and corresponds to the “second substrate.” Iwabuchi-762, [0029]. “[S]emiconductor chip 53” comprises an analog/digital (“AD”) converter array, and “semiconductor chip 54” comprises a memory array. *Id.* Chip 53 corresponds to the “first substrate.” “[C]onnection pads 81, 82 thereof are electrically connected by way of conductive connectors, e.g. bumps 83.” *Id.*, [0036].

FIG. 1



225. In another embodiment shown in Fig. 26B, Iwabuchi-762 explains that “[c]onductive microbumps 83 are provided on the pads 82 of the second semiconductor chip 53, and the pads 82 of the second semiconductor chip 53 and the pads 81 on the front surface side of the first semiconductor chip 52 are electrically connected by way of the microbumps 83 with the second semiconductor chip 53 facing downward.” *Id.*, [0067], Fig. 26B.

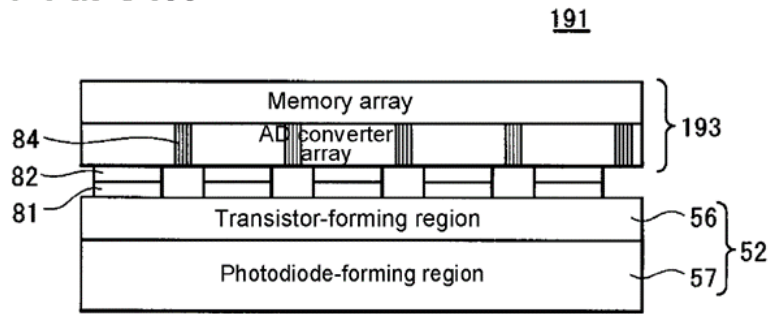
FIG. 26B



226. In this example, the sensor chip 52 has pads 81 while conductive microbumps 83 are associated with the circuit chip (semiconductor chip 53) that corresponds to Iwabuchi's DSP chip. POSAs would have found it trivial to associate microbumps 83 with sensor chip 52 (Iwabuchi sensor chip 1a) rather than semiconductor chip 53 (Iwabuchi DSP chip). Either way, this example illustrates Iwabuchi's suggestion at [0153] to flip-chip bond sensor chip 1a (second substrate) to the DSP chip (first substrate).

227. In another embodiment Iwabuchi-762 describes thermocompression bonding sensor chip 52 to semiconductor chip 193 using conductive pads 81 and 82 without microbumps. Iwabuchi-762, [0089] ("The semiconductor image sensor module 191 in fig. 31A is configured by forming the pads 82 on the lower surface of the second semiconductor chip 193, forming the pads 81 on the upper surface of the first semiconductor chip 52, and thermocompression bonding the first semiconductor chip 52 and the second semiconductor chip 193 so that both pads 82 and 81 are connected."), Fig. 31A. Furthermore, Iwabuchi-762 explains that "[t]he bonding strength between the first and second semiconductor chips 52 and 193 may be further increased by using an adhesive material to bond regions outside the pads 81, 82." *Id.*, [0089].

FIG. 31A



228. As explained *supra* § V.B.1.c.iii (step [1.b]), planar metal landing pads are formed on Iwabuchi's sensor chip 1a or the DSP chip, in place of bumps 32 used to bond either to the interposer, (Iwabuchi, [0125], [0154], Fig. 7), for receiving the conductive metal bumps 32 on the opposing chip. Iwabuchi, [0153]; Iwabuchi-762, Fig. 26B.

229. POSAs would also have found it conventional to compression bond Iwabuchi's sensor chip 1a to its DSP chip using compression bonding with conductive pads on each chip but without using conductive microbumps 32, as shown in Iwabuchi-762 Fig. 31B.

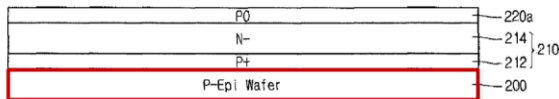
230. Flip-chip bonding for die to die bonding was well-known in the art. *E.g.*, Iwabuchi-762, Figs. 1, 26B, 31A; Rogalski, Fig. 14; Balcerak, Fig. 1. Then the sensor and DSP chips could be flip-chip bump bonded in the same manner that Iwabuchi describes flip-chip bonding the sensor chip to the interposer. Iwabuchi, [0153].

h. Step [1.f]

1.f	removing a lower portion of the second substrate to expose the photodiode,
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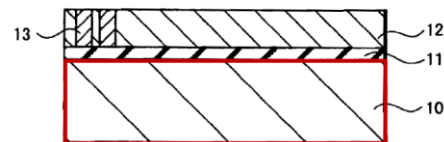
231. Substrate 10 is a lower portion of the second substrate. Iwabuchi, [0142] & Fig. 10A. This comports with defining material layers as “over” by reference to the backside light-incident surface in step [1.g.2]. *Supra* § V.B.1.d.iii; Ex. 1001, Fig. 2.

FIG. 2



'808 patent

FIG. 10A



Iwabuchi

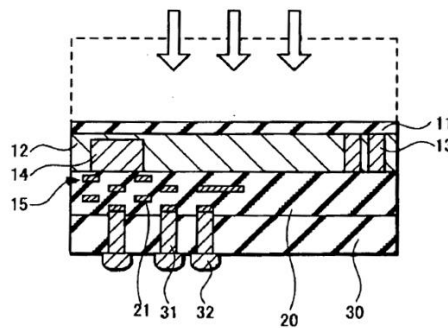
232. The ordinary meaning of “to expose” is “to allow to be subjected to an action, influence, or condition” or “to subject to the action of light.” Ex. 1034, 626.

233. POSAs would have understood in the context of backside thinning a photodetector that “removing [substrate] to expose the photodiode” meant removing enough of the base or handle substrate that the photodiode could receive (“be subjected to”) incident light through the backside surface. This is exactly what Iwabuchi discloses.

234. Iwabuchi describes removing substrate 10 to expose the photodiode. “[S]emiconductor substrate 10 is decreased in thickness until the photodiode 14 becomes able to receive light from the side of the semiconductor substrate 10 of

the SOI substrate,” (Iwabuchi, [0150]; *accord id.*, [0065] & Fig. 10G), just like the ’808 patent describes removing the “P-Epitaxial layer” (Ex. 1001, 4:36-53 & Fig. 8). This meets [1.f].

FIG. 10G



235. Furthermore, although Figure 10G depicts backside-illuminated photodiode 14 as not completely extending to the backside surface of substrate 12, POSAs would have known that extending the photodiode so that the backside of Iwabuchi layer 1054 in Fig. 5 coincided with the interface of substrate 12 and oxide 11 would have been conventional. *E.g.*, Maruyama, [0032], Fig. 5B; Ezaki, Figs. 1-3 & 6; Lee, Fig. 10; Suzuki, Fig. 8.

236. POSAs would also have found it obvious to further remove oxide layer 11 to expose photodiode 14 to air or vacuum, because this was a known and conventional process step. *E.g.*, Shiraiwa, [0010], Fig. 9E; *accord id.*, [0037] & Fig. 5E.

* * *

237. Taken as a whole claim 1 would have been obvious over Iwabuchi.

2. Claim 4

The method of claim 1, comprising forming the ion implantation isolation layer over at least one of a side of the photodiode and a bottom of the photodiode.

238. Iwabuchi renders claim 1 obvious. *Supra* § V.B.1. Iwabuchi separation region 1043 is an ion implantation layer. *Supra* § V.B.1.f.iii ([1.h.2]). Region 1043 is formed over layer 1054. Relative to the ion implantation layers, layer 1054 is closest to “a bottom of the photodiode.” *Supra* § V.B.1.d.iii (step [1.g.2], discussing “over”); Ex. 1023, 993; Iwabuchi, Fig. 5. Therefore, region 1043 (and as I explain further below, layer 1053 and region 1046) are “over... a bottom of the photodiode” because they are “over” layer 1054. POSAs would have understood layer 1054 to be the “bottom of the photodiode” because this is consistent with the frame of reference for ascertaining “over” in claim 1, which evaluated a layer’s relative position by reference to the photodiode’s backside light incident surface, and is consistent with the sole embodiment shown in the ’808 patent figures.

[illegible]

240. Iwabuchi meets claim 4, rendering it obvious.

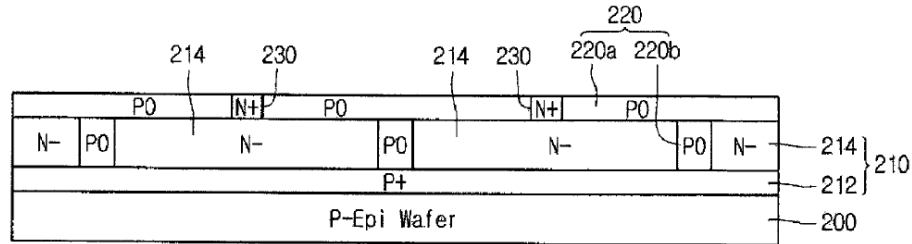
The method of claim 1, wherein the ion implantation isolation layer comprises a P0 layer.

- 101 -

242. The '808 patent does not explain the meaning of "P0 layer." The term "P0" has no known meaning in the art. Generally, one refers to very heavily doped p-type layers as p++, heavily doped p-type layers as p+, moderately doped p-type layers as p, and lightly doped p-type layers as p-. P0 does not have any specific common usage. The only clear meaning in the context of claim 1 is that it refers to P type doped region. But if the term only meant that a region should be doped p-type, then POSAs would denote the doping of a p-type region as "P-type" (using the '808 patent terminology) or "p-type" (conventional usage). The use of the numeric "0" takes the place of a degree of doping, which I just explained is conventionally denoted with "+" or "-". The '808 patent gives no guidance what degree of doping, e.g., doping concentration, P0 requires.

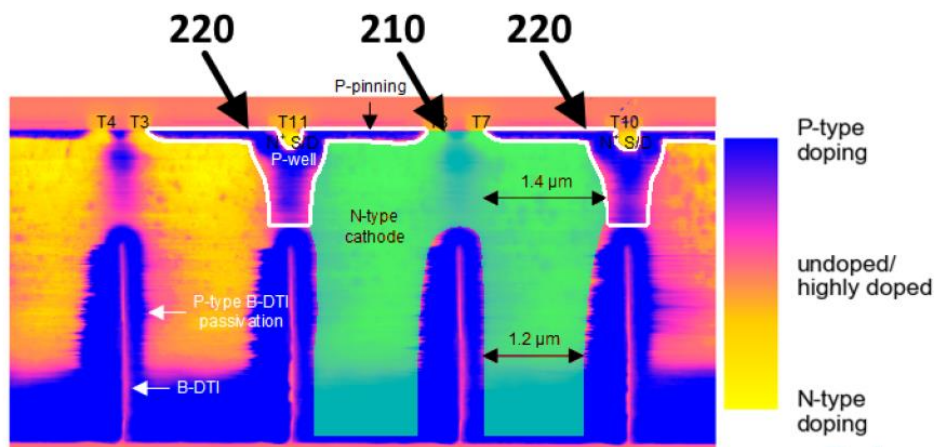
243. While the specification does not explain the meaning of "P0," it also refers to P+, N+, and N- layers. Ex. 1001, Fig. 4. "P+" layer 212 refers to "a high concentration P-type conduction layer," (Ex. 1001, 3:23-25), while "N-" layer 214 refers to "a low concentration N-type conduction layer" (*id.*, 3:38-40) and "N+" layer 230 refers to a "high concentration [n type] ion implantation region" (*id.*, 3:62-64). Iwabuchi follows the same convention using lower case p or n. *E.g.*, Iwabuchi, [0096] (referring to "p+ accumulation layer 1053" as a "heavily-doped p type semiconductor region," meaning it has a high dopant concentration).

FIG. 4



244. The specification describes forming “P0” layers 220a and 220b by ion implantation. *Id.*, 3:44-61. Given the lack of any definition, POSAs would have surmised that P0 could mean either (a) **any** p-type doping level, or (b) p-type doping less than p+.

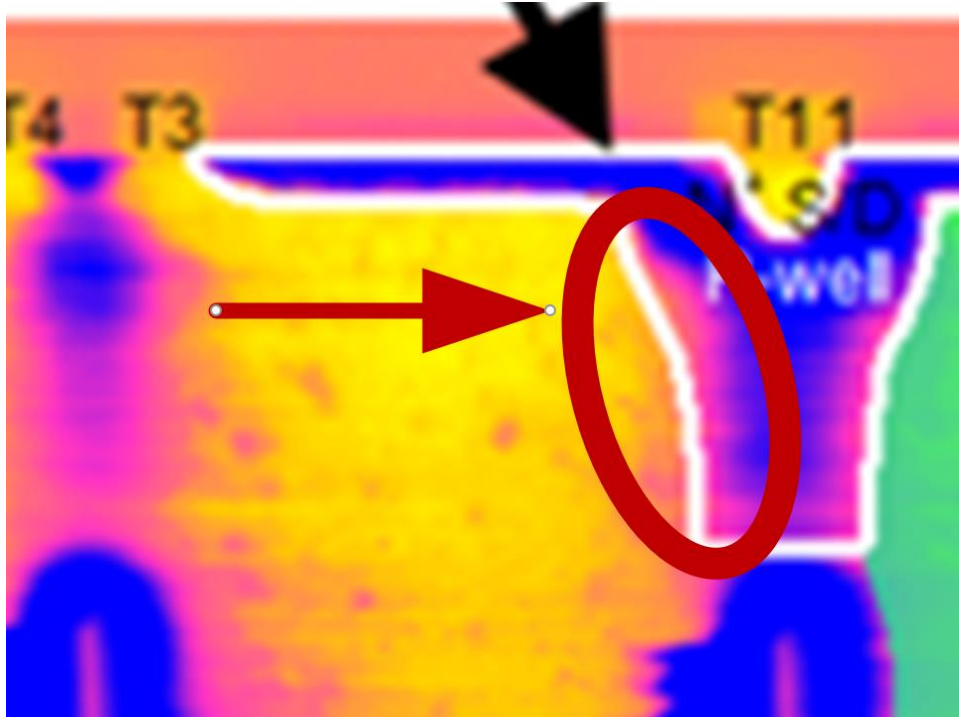
245. The infringement contentions allege that “ion implantation layer 220 includes a P0 layer” without explaining what a P0 layer is. IC-A1, 30.



PO infringement contentions (claim 5) (IC-A1, 30).

246. The legend and blue coloration in the cross-section makes clear that the “P-pinning” and “P-well” regions 220 are heavily doped p+.

247. As shown below the white layer “220” outline in the contentions includes a pink/purple-colored metallurgical transition from p+ to n+ doping in adjacent conduction layers. This suggests that PO treats “P0” as meaning either (a) any P-type doping, or (b) a moderate p-type doping as net doping transitions from p to n. The PO’s choice of where to draw this white outline, of course, is completely arbitrary, since the PO could just as easily have placed the white outline at the edge of the area shown in blue. There is



248. Based on the usage in the contentions Iwabuchi meets claim 5 because p layer 1043, p region 1046, and p+ layer 1053, are each p-type isolation layers and the moderate “p” doping in 1043 and 1046 is less than the p+ concentration.

Supra §§ V.B.1.f.ii(1) (region 1046), V.B.1.f.ii(2) (layer 1053), V.B.1.f.iii (layer 1043). POSAs would also have understood that annealing to cure crystal damage from ion implantation would have caused p and n dopants in Iwabuchi’s layers to diffuse in a real device, which would contribute to a non-abrupt transition from p+ to n concentrations in the region of a metallurgical junction. *E.g.*, Sze-2002, 466-480.

4. Claim 6

249. Iwabuchi renders claim 1 obvious. *Supra* § V.B.1. Iwabuchi meets claim 6 at least two ways.

a. Step [6.a]

6.a	The method of claim 1, comprising: forming a dielectric over the photodiode of the second substrate before bonding the first and second substrates; and
-----	---

250. The ordinary meaning of “dielectric” is “a material which is an electric insulator.” Ex. 1026.

i. “dielectric” is insulator layer 20

251. With either the interposer, supporting substrate, or DSP chip substrate as “first substrate,” Iwabuchi meets [6.a] because it describes forming insulator layer 20 over layer 12 and photodiode 14. Iwabuchi, [0144]-[0145], Fig. 10B. Insulator layer 20 is a dielectric. A POSA would have known that in general a dielectric refers to an insulator with a particular dielectric constant.

252. Layer 20 is formed over the photodiode in layer 12 before any “first substrate” (support substrate 30, interposer 3, or DSP chip, *supra* § V.B.1.b (step [1.a])) is bonded to the second substrate (*supra* § V.B.1.d.i (step [1.c])). Iwabuchi, [0146]; *supra* § V.B.1.g.ii (step [1.e]).

ii. “dielectric” is supporting substrate 30

253. With the interposer or DSP chip substrate as “first substrate,” Iwabuchi meets [6.a] with supporting substrate 30 as the “dielectric.” Substrate 30 can be formed from “an insulating resin substrate.” *Id.*, [0146]. The insulating resin is a dielectric. In this example substrate 30 is “formed” on the first substrate by bonding it to insulator layer 20. Iwabuchi, [0146]. As with layer 20, this is done before bonding to the interposer or DSP chip.

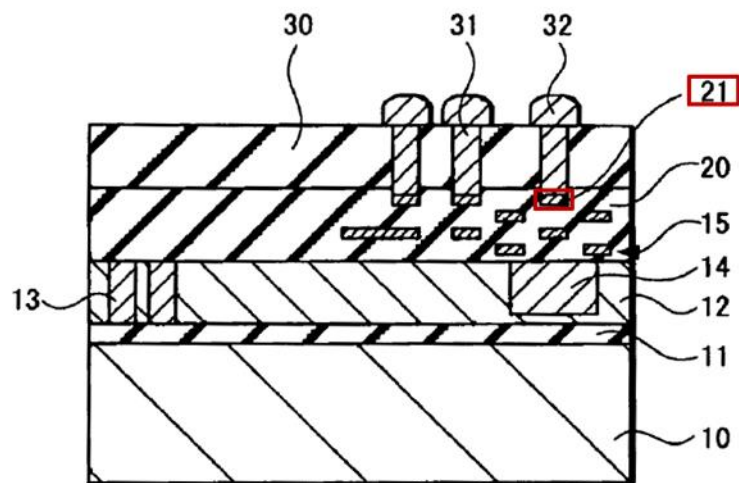
b. Step [6.b]

6.b	forming a metal pad in the dielectric.
-----	--

i. “dielectric” is insulator layer 20

254. Iwabuchi describes forming “buried wiring layer 21” in “interlayer insulator 20.” Iwabuchi, [0145]. Wiring layer 21 connects to “substrate penetrating wiring 31” formed in supporting substrate 30. *Id.*, [0148] & Fig. 10F.

FIG. 10F



255. POSAs would have understood that a conventional way to join wiring 21 to substrate penetrating wiring 31 would have been to form wiring 21 into a metal pad in layer 20 defining the location for dry etching through layer 30, for receiving metal plating to form wiring 31 contacting wiring layer 21. Iwabuchi, [0148]-[0149]. Sze-2002, 432-442, Fig. 33.

ii. “dielectric” is supporting substrate 30

256. Iwabuchi explains that “bump (micro-bump) 32 is a protrusion-like metal electrode **formed on a pad** smaller than an ordinary pad electrode...by a suitable method such as electrolytic plating.” Iwabuchi, [0120]. POSAs would have understood this describes “forming a metal pad” in substrate 30 for receiving micro-bump 32, and that in any event forming a metal pad would have been obvious.

5. Claim 8

The method of claim 1, wherein forming the circuitry including the metal interconnection comprises forming a metal and a plug over the first substrate.

257. Iwabuchi renders claim 8 obvious for the same reason that Iwabuchi meets step [1.b]. *Supra* § V.B.1.c

6. Claim 9

The method of claim 1, wherein the second conduction type second ion implantation isolation layer is disposed to directly contact on a top surface of the second conduction type first ion implantation isolation layer and a bottom surface of the second conduction type conduction layer .
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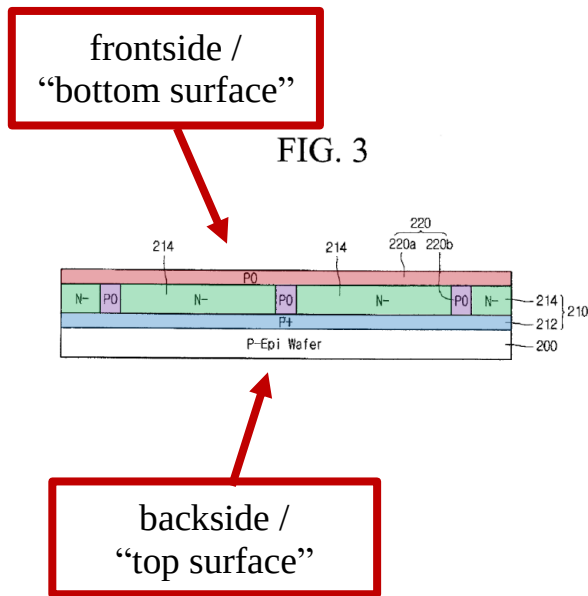
258. Claim 9 refers to “top surface” and bottom surface” in a way that reverses the frame of reference that was used in claim 1. In claim 9, the “top surface” of the various layers takes the backside of the second substrate as the “top,” whereas in claim 1 the usage of “over” took the frontside of the second substrate as above other layers by reference to the backside or back surface. In other words, the “top surface of the second conduction type first ion implantation

isolation layer” 1046 in Iwabuchi is furthest from the frontside of the crystalline layer 12 where the transistor source/drains are formed.

259. POSAs would have known this because the only disclosed embodiment in the '808 patent that can meet claim 9 is shown in the figures, such as Figure 3 below, and it meets this understanding of taking the frontside as the frame of reference setting the “bottom” by which to ascertain the top or bottom of the various layers: the “top” of each layer is furthest from the frontside. Moreover, as noted above, Iwabuchi explains that its unit pixel is arrayed in an XY fashion, Iwabuchi, [0094], so that POSAs would have known that the right-side of Iwabuchi Figure 5, with its isolation layer 1043 disposed between isolation layer 1046 and conduction layer 1054, would be contiguous with a neighboring pixel isolation layer 1043 shown on the left side of Iwabuchi Figure 5.

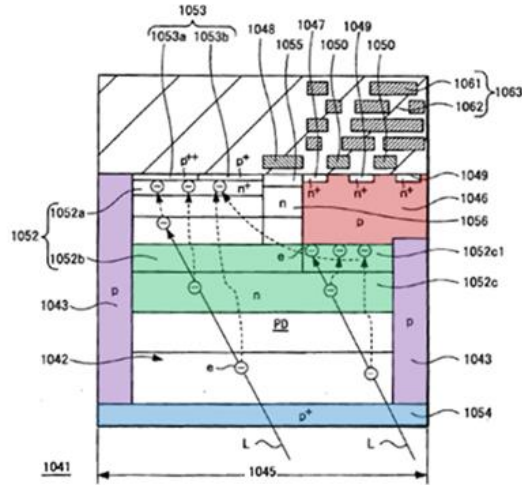
260. Iwabuchi renders claim 1 obvious. *Supra* § V.B.1. Separation region 1043 is the “**second conduction type second ion implantation isolation layer**” in [1.h.2] (*supra* § V.B.1.f.iii), and p region 1046 is the “**second conduction type first ion implantation isolation layer**” in [1.h.1] (*supra* § V.B.1.f.ii(1)). Layer 1054 is the “**second conduction type conduction layer**” in [1.g.1] (*supra* § V.B.1.d.iiV.B.1.f.ii(1)).

261. Region 1043 “is disposed to directly contact on a bottom surface” of layer 1054 and a “top surface” of region 1046. Iwabuchi, Fig. 5.



'808 patent

FIG. 5



Iwabuchi

262. This spatial relation of separation region 1043, to p+ layer 1054 and p region 1046, is consistent with the '808 patent depiction of 212, 220a, and 220b in Fig. 3. In this orientation, “bottom” and “top” are used taking the front surface of the second substrate (e.g., the top of Iwabuchi Fig. 5 or '808 patent Fig. 3) as “down” in relation to a material layer.

VI. GROUND 1B: IWABUCHI+MARUYAMA RENDERS OBVIOUS CLAIM 2

A. Maruyama

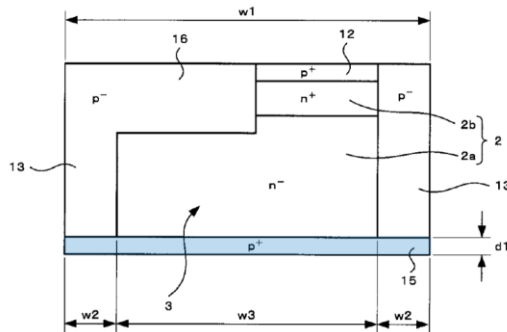
263. JP 2006-93587 A (Ex. 1006, “Maruyama”) published April 6, 2006. The inventor, Yasushi Maruyama, is also a named inventor in Iwabuchi.

264. Maruyama describes a back-illuminated solid-state imager. Maruyama, [0001]. It describes a photodiode unit cell or unit pixel similar to the

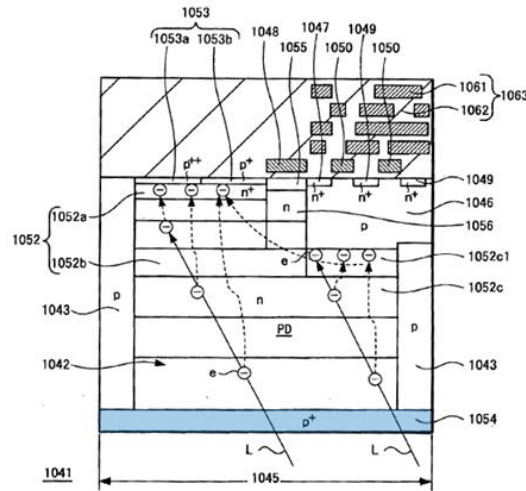
one described in Iwabuchi, including a backside p+ layer 15 analogous to Iwabuchi p+ layer 1054. Maruyama, [0010]-[0012], [0017] & Fig. 2.

FIG. 5

【 図 2 】



Maruyama Fig. 2.



Iwabuchi Fig. 5.

265. Maruyama's p+ layer 15 "has a junction depth from the back face of the semiconductor substrate of not greater than 0.4 μm ." *Id.*, [0011].

266. POSAs would have understood that " μm " was a standard abbreviation for micrometer or a distance of 10^{-6} meters.

267. Limiting the junction depth to under 0.4 μm ensures "blue-light sensitivity, and a color image of favorable image quality can be obtained." Maruyama, [0014].

268. The light-absorbing properties of silicon are well-known. For example, Ex. 1045, Mike Salib et. al, "Silicon Photonics," *Intel Technology Journal*, volume 8, no. 2, pp. 143-160, 2004, Fig. 13 at 152, shows the penetration

depth of light in μm (e.g., units of 10^{-6} meters) for different materials as a function of wavelength. In the annotated figure below a blue shaded region denotes the range of free-space wavelengths typically regarded as providing blue visible light (approximately 400 to 500 nm, or 0.4 μm to 0.5 μm). The wavelength range is, quite literally, a spectrum. Wavelengths closer to 0.4 μm are blue-violet, while wavelengths closer to 0.5 μm are blue-turquoise. The penetration depth of light in silicon is shown by the red line labeled “Si”. The logarithmic scale on the right side, labeled “penetration depth,” proceeds in factors of 10 from the shortest distance, 10^{-1} or 1/10 of a μm at top, to the longest distance, 1000 μm (e.g., a millimeter), at the bottom. The shorter wavelengths are to the left of the x axis. The red line in the plot therefore shows that shorter wavelengths are expected to penetrate in bulk silicon only a very short distance before being absorbed. The dashed blue line annotation approximates a penetration depth of 0.5 μm , which for silicon occurs within the range of wavelengths identified as blue light. As Murayama explains, POSAs would know that setting a junction depth more than 0.4 μm would exclude much of this range of blue light because that light would be absorbed before photogenerated electrons could be separated by the photodiode depletion layer.

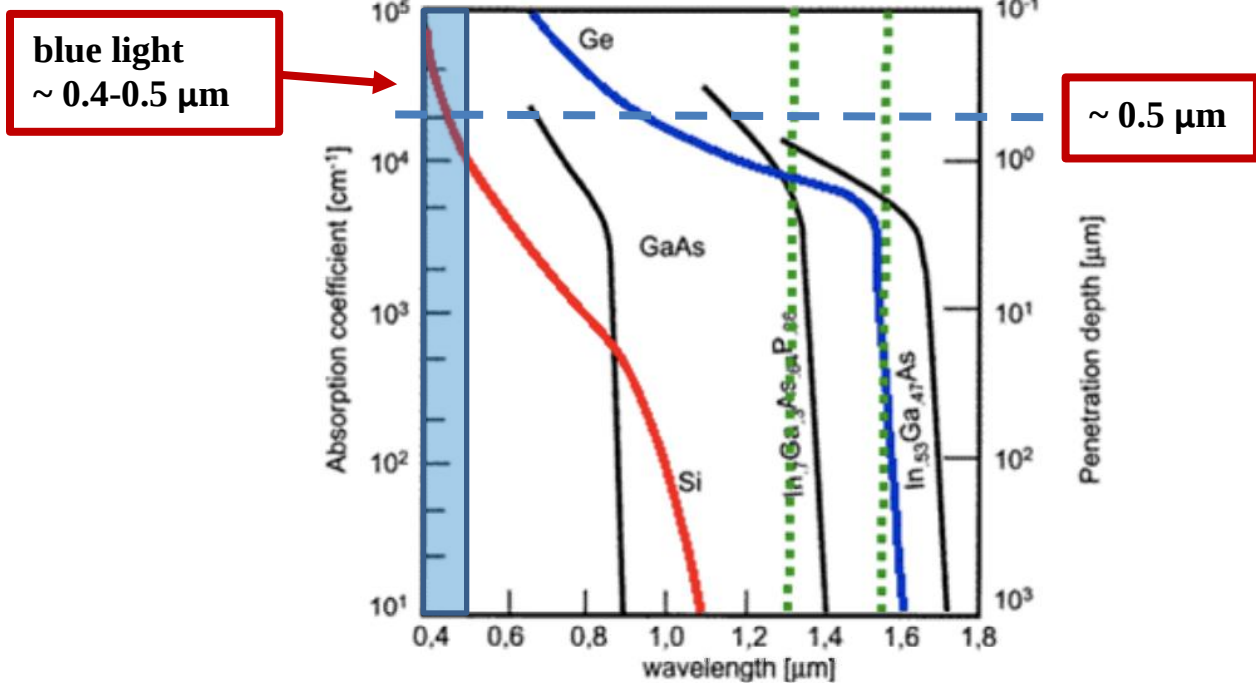


Figure 13: Absorption coefficient and penetration depth of various bulk materials as a function of wavelength. The green lines mark the important wavelengths for telecommunications of 1.310 and 1.550 μm .

B. Iwabuchi+Maruyama

269. Iwabuchi+Maruyama comprises the detector in Iwabuchi limiting the p+ layer 1054 junction depth to under 0.4 μm as described in Maruyama.

270. While Iwabuchi provides some manufacturing details for the described photodetector, it does not provide details of doping concentrations or junction depths.

271. POSAs implementing Iwabuchi's design would turn to Maruyama for additional manufacturing detail because Maruyama describes manufacturing a backside illuminated photodetector design similar to that in Iwabuchi.

272. Iwabuchi+Maruyama would use Maruyama's junction depth to ensure blue-light sensitivity in Iwabuchi. This would simply arrange old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement. This would also apply Maruyama's known technique to Iwabuchi's known device to yield predictable results.

273. POSAs would have reasonably expected Iwabuchi+Maruyama to work as intended for the same reasons that Maruyama's detector worked. Furthermore, although Maruyama describes forming its p-layer 15 with ion implantation from the backside, Maruyama, [0013], POSAs would have known that forming Iwabuchi's layer 1054 by ion implantation through the frontside would reliably form a layer that creates a p-n junction with a junction depth less than 0.5 μm as recited in claim 2 because as I explained above the depth and thickness of a blanket implant like layer 1054 could be tightly controlled. *E.g.*, Sze-2002, 469 ("The main advantages of ion implantation are its more precise control and reproducibility of impurity dopings and its lower processing temperature compared with those of the diffusion process."), 470 ("The average depth can be controlled by adjusting the acceleration energy."), Fig. 14(b) (showing two-dimensional distribution of implanted ions); Sze-1981, 70 ("The main advantages of ion implantation include (1) precise control over total dose,

depth profile, and area uniformity; (2) low-temperature processing; and (3) implanted junctions that can be self-aligned to the edge of the mask.”).

C. Claim 2

The method of claim 1, comprising forming the **second conduction type conduction layer** at a junction depth of less than approximately 0.5 μm .

274. While the '808 patent does not explain the meaning of “junction depth,” POSAs would have understood that “junction depth” refers to the distance from a light incident surface to the furthest metallurgical junction between a p and n type material for a particular layer. *E.g.*, Ezaki, [0011] & Figs. 2 & 3 (depth “h2b”).

275. Iwabuchi+Maruyama renders claim 1 obvious for the same reasons as Iwabuchi alone. *Supra* § V.B.1. In Iwabuchi+Maruyama, layer 1054 is the “**second conduction type conduction layer**” (*supra* § V.B.1.d.ii (step [1.g.1]) and has a junction depth less than 0.5 μm . *Supra* § VI.B.

VII. GROUND 1C: IWABUCHI+SUGA RENDERS OBVIOUS CLAIM 7

A. Suga

276. T. Suga et al., “Surface Activated Bonding for New Flip Chip and Bumpless Interconnect Systems,” *52nd Electronic Components and Technology Conference* 2002, pp. 105-111, (Ex. 1007, “Suga”), published in 2002.

277. Suga describes “a low cost, ultra-high density, low-damage and low-temperature” process for “ultra-fine density flip chip” bonding. Suga, 105. “[T]he

room temperature or low temperature flip chip bonding is achieved for Au [gold] bump to Au or Cu [copper] electrode by means of the surface activation treatment using RF [radio frequency] plasma irradiation.” *Id.* Suga’s surface activation “cut down the bonding condition requirements and decreased the process cost.” *Id.*

B. Iwabuchi+Suga

278. Manufacturing Iwabuchi’s imager with gold bumps 32 on the sensor chip and copper landing pads on the interposer or DSP chip, using Suga’s surface activated bonding, is Iwabuchi+Suga.

1. Reasons to combine

279. Iwabuchi describes flip-chip bump-bonding the sensor chip to the interposer or DSP chip. Iwabuchi, [0153].

280. Iwabuchi provides a “micro-bump” for each pixel. Iwabuchi, [0140], [0192]. “Further, the bump, which protrudes from the surface of the supporting substrate, can be formed on the whole of the chip area. For example, ***independent bumps can be formed at every pixel of the CMOS image sensor*** and connected to a suitable element on the DSP chip whereby signal electric charges can be read out at every pixel.” Iwabuchi, [0192]. Iwabuchi “intends to provide a solid-state image pickup device in which the pixel size can be made very small[.]” Iwabuchi, [0048]; *id.*, [0046]-[0047]. Where a contact is provided for each pixel, POSAs would have understood that reducing pixel dimensions would ***increase*** the flip-

chip bump density because smaller pixel dimensions would move flip-chip bumps closer together.

281. Even where a contact is provided for row and column addressing but not necessarily for each pixel, using higher density array formats allowed by smaller pixel dimensions would also increase the contact density for the flip-chip bonding.

282. The higher density bumps have smaller contact area for bonding. The smaller contact area reduced the surface available for adhesion, which was known to decrease the bond reliability.

283. POSAs would have known that Suga's plasma activation process would increase the adhesion at the bump surface in Iwabuchi's flip-chip bonding, which would increase the bump-bond reliability. *E.g.*, Suga, 105.

284. In order to use Suga's methods POSA would have formed gold bumps 32 on the sensor chip, and copper metal lands on the interposer or DSP chip. Gold was commonly used to form integrated circuit contacts because it is soft and malleable, has good conductivity, and does not form a native oxide. Gold, including gold plating on other metals like copper, was commonly to provide contacts in flip-chip bonding. This is described, for example, in Keswick and Ex 1035, 576 .

285. POSAs also would have known that “conventional solder bump technology [had] several drawbacks due to high soldering temperature and multiple depositions of metal layers, thereby [providing] a high-cost technology[.]” Oh, 224. Higher temperature can damage metallization. For example, aluminum metallization on a die cannot be exposed to a bonding process with temperature above 450 degrees Celsius. Dragoi, 147.

286. For these reasons, POSAs would have recognized using Suga’s “low cost, ultra-high density, low-damage and low-temperature” process for “ultra-fine density flip chip” bonding would avoid the drawbacks of high temperature conventional flip-chip bonding and would lower process costs as reported in Suga.

287. This would apply Suga’s known techniques to Iwabuchi’s manufacturing process yielding predictable results.

2. Reasonable expectation of success

288. POSAs would have expected Suga to reduce flip-chip bonding costs and increase bump adhesion and reliability, providing high-density flip-chip bonding at lower temperatures, for the same reasons that Suga achieved these outcomes. Thus, POSAs would expect Suga’s methods to improve the bump bonding in Iwabuchi in a similar way.

C. Claim 7

The method of claim 1, wherein bonding the first substrate to the second substrate comprises contacting the first substrate and the second substrate with each other and performing activation by plasma.

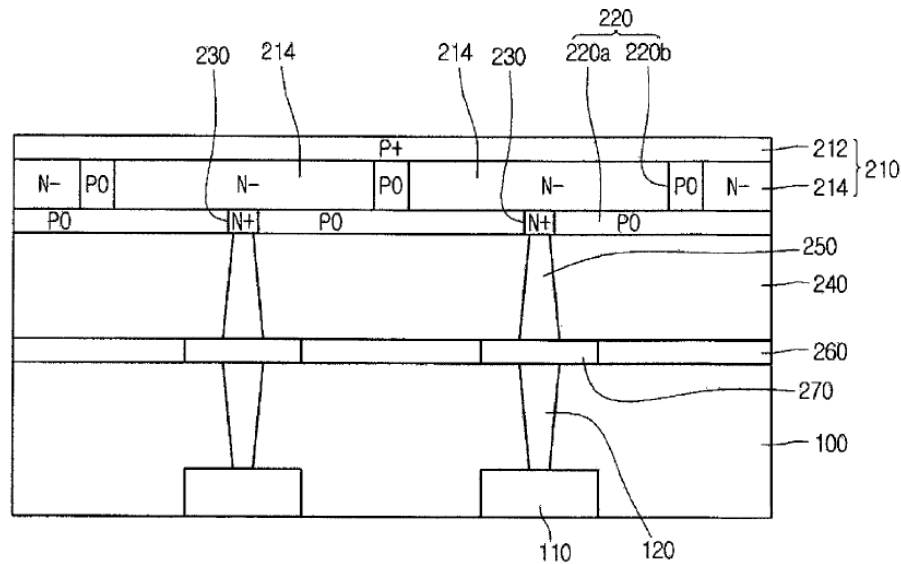
1. “contacting substrate[s]”

289. The ’808 patent provides an expansive usage of “bonding substrates.” *Supra* § V.B.1.g.ii (step [1.e]). It takes a similarly broad view of “contacting substrates.” The ’808 patent provides one example of “contacting” substrates that shows contacting a “first substrate 100” with metal and dielectric layers that are formed over “second substrate 200.” Ex. 1001, 4:25-35, Figs. 7 & 8.

290. The specification’s “contacting” discussion describes the same intervening layers (dielectrics 240 & 260, metal plug 250, metal pad 270) between substrates as discussed with “bonding.” Ex. 1001, 4:8-35 & Figs. 5-8; *Supra* § V.B.1.g.ii (step [1.e]).

291. The specification describes “contacting first substrate 100 and second substrate 200 with each other” by contacting dielectric 260 and metal 270—which are formed on dielectric 240 and metal 250—to a surface of substrate 100. *Id.* 4:31-35 & Fig. 8.

FIG. 8



292. For claim 7 to cover the sole “contacting” embodiment in the ’808 patent specification, either (1) “contacting substrates” must encompass electrically contacting substrates or (2) “substrate” must encompass layers and metal formed on, or over, an initial substrate (or both).

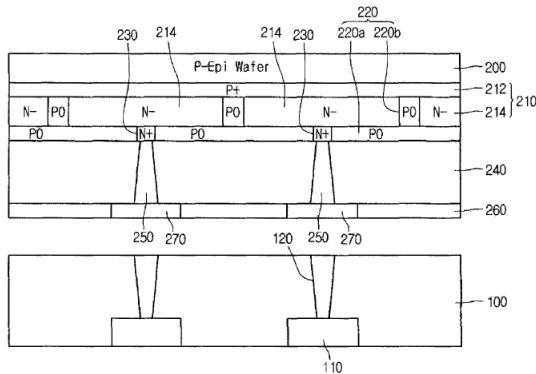
2. Analysis

293. Iwabuchi+Suga meets claim 1 for the same reasons that Iwabuchi alone meets claim 1. *Supra*, § V.B.1.

294. The sensor chip includes the “second substrate.” *Supra*, § V.B.1.d.i. Iwabuchi describes bump-bonding the sensor chip to the interposer (*supra* § V.B.1.g.ii(1) (step [1.b])), or the DSP chip (*supra* § V.B.1.g.ii(3) (step [1.b])).

POSAs would have implemented Iwabuchi's flip-chip bonding with Suga's bumpless bonding.

FIG. 7



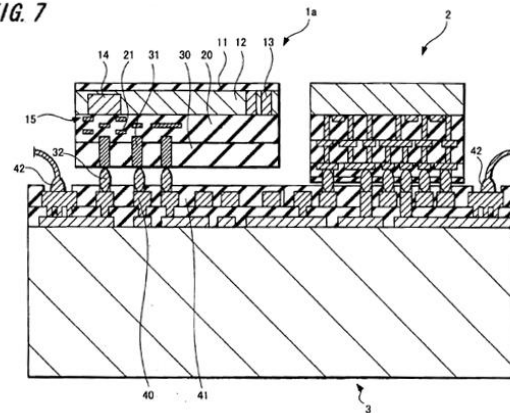
a. contacting

295. Flip-chip bonding the sensor chip to either the interposer or DSP chip, is “contacting the first substrate and second substrate with each other.”

296. Flip-chip bonding was understood in the art as physically and electrically joining substrates. *E.g.*, Dery, 2:8-11 (“The IC chip is joined to a chip carrier via a plurality of solder bumps electrically connecting a plurality of contact pads on the IC chip to corresponding contacts on the chip carrier.”); Tong, [0014] (“An object of the present invention is thus to obtain mechanical and electrical contact between wafers and die with a single bonding step[.]”). Suga’s method provides the same result.

297. Bump bonding electrically contacts the photodiodes in layer 12 (second substrate) with wiring 40 on the interposer, Iwabuchi, Fig. 7, and with the

FIG. 7



metal landings replacing the bumps on the DSP chip. *Supra* § V.B.1.c (step [1.b]); V.B.1.g.ii(3) (step [1.e]).

298. Flip-chip bonding the sensor chip to the interposer, or the DSP chip, physically “contacts” the “first” and “second” substrates “with each other.”

299. In each case “substrate” encompasses gold micro-bumps 32 formed over layer 12 (“second substrate”); copper wiring 40 formed on the interposer (*supra* § V.B.1.c.i (step [1.b])) and copper landings formed over the DSP chip. *Supra* §§ V.B.1.c.ii (sensor chip), V.B.1.c.iii (DSP chip); Iwabuchi Fig. 7.

b. activation

300. Suga combines flip-chip bonding with a “Surface Activation Bonding process” in which the “flip chip bonding is achieved for Au or Au to Cu electrode by means of the surface activation treatment using RF plasma irradiation.” Suga, 105. This is “performing activation by plasma.”

301. Iwabuchi+Suga renders obvious claim 7.

VIII. GROUND 2A: LEE+MASAGAKI+SHIRAIWA RENDERS OBVIOUS CLAIMS 1, 4-6, AND 8-9

A. References

302. Lee, Masagaki, and Shiraiwa each published more than a year before December 28, 2008.

1. Lee

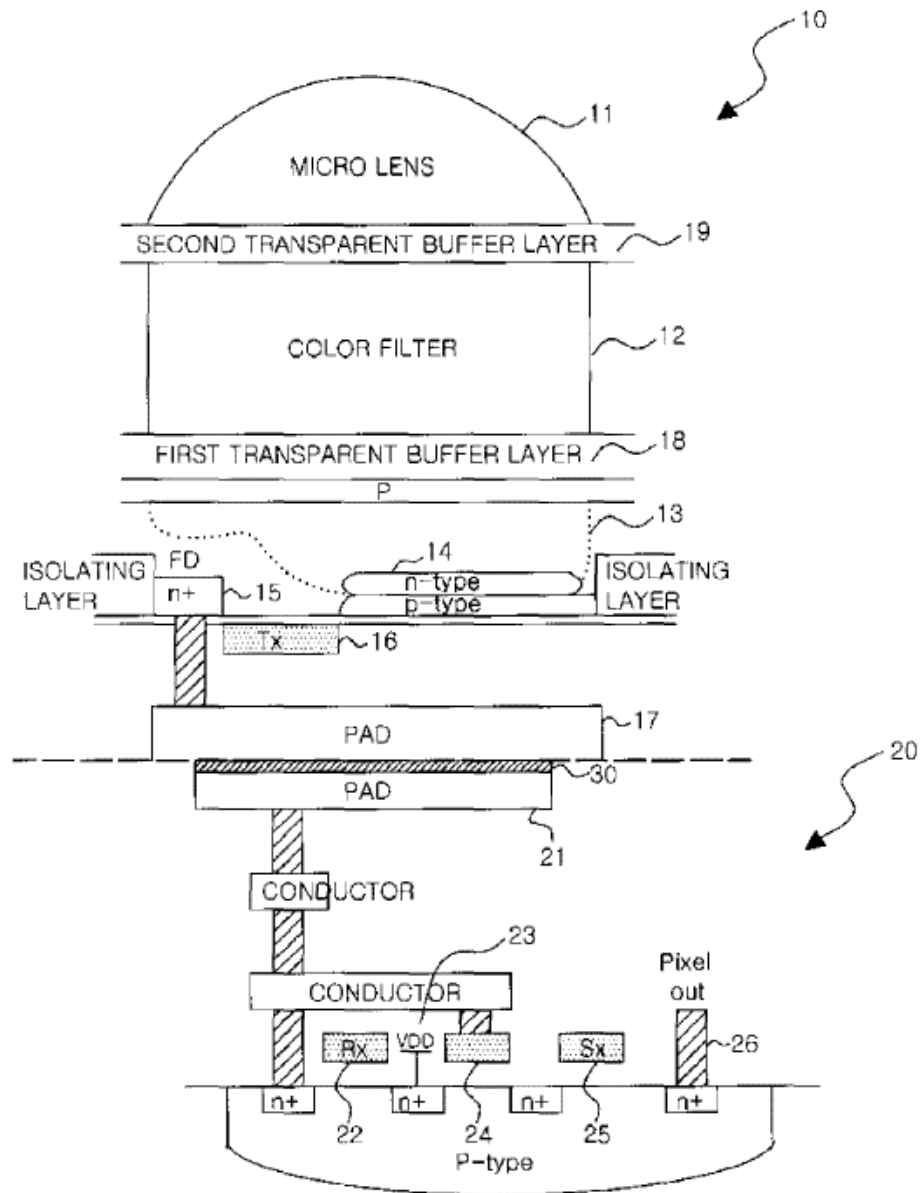
303. PCT Publication No. WO 2006/109937 (Ex. 1008, “Lee”) published October 19, 2006. Lee describes methods of manufacturing a solid-state imager with a “3D structure” by bonding a sensor wafer to a circuit wafer. *E.g.*, Lee, [14]-[15]. The sensor wafer provides an array of unit pixels. *Id.*, [10]. Each unit pixel has a photodiode, a transfer transistor, and is backside-illuminated. Lee, [1], [13]-[14], Fig. 10.

304. The backside illumination moves the transfer transistor and interconnects to the “rear” of the unit pixel (sensor wafer frontside), so that the entire light-incident backside surface can receive light. Lee, Fig. 10. The transfer transistor has a source provided by a photodiode charge accumulation layer and a drain provided by a floating diffusion. Lee, [29], [38], Fig. 10.

305. Lee calls this a “separation type unit pixel.” Lee, [13]. The remaining readout transistors, and additional circuitry, are moved to a second wafer. Lee, [14], [35].

306. The image signal is taken to the readout and other circuits on the second wafer from the floating diffusion in the unit pixel through interconnections including vias and conduction pads connecting each pixel. Lee, Abstract, Figs. 10 & 11, claim 2.

[Fig. 11]



2. Masagaki

307. JP 2006-303385 (Ex. 1009, “Masagaki”) published November 2, 2006.

308. Masagaki describes a hole accumulation photodiode (“HAD”) formed in a “silicon semiconductor substrate” with a charge storage region extended

laterally below a pinning or planar isolation layer and bounded by a “device separation region.” Masagaki, [0009], [0018], [0020], Fig. 10, claim 1.

[FIG. 10]

310. Masagaki describes forming both layers 12 and 3 by ion implantation, replacing prior art STI with “an inter-device separation structure made up of a diffusion layer” to avoid dark-current generating crystal defects just like the ’808 patent. Masagaki, [0003] (“an inter-device separation region structure...replaces STI”); id. [0002], [0037], [0040]; Ex. 1001, 2:57-62. *See also* Masagaki, [0029]. Extending the charge storage region mitigates reduced charge storage, associated

with reducing pixel dimensions, leading to “a worsened S/N ratio” and “decreased dynamic range.” Masagaki, [0007], [0008].

311. Forming the device separation region by ion implantation facilitated extending the charge storage region as taught by Masagaki because it allowed precise control over the features, layers 12 and 3, bounding the extended charge region 6. Sze-1981, 70 (“The main advantages of ion implantation include (1) precise control over total dose, depth profile, and area uniformity; (2) low-temperature processing; and (3) implanted junctions that can be self-aligned to the edge of the mask.”). In addition, in order to maximize the pixel density, a POSA would want to minimize the width of the PO region between pixels. The POSA would have realized that ion implantation provides deeper, narrower doped regions when compared with the common alternative, diffusion of dopants.

312. Masagaki demonstrates that the only allegedly novel aspects of the challenged claims, two isolation layers formed by ion implantation, were known in the art. *Supra*, § IV.C.

313. Like the '808 patent, Masagaki explains that it was known to replace a shallow trench isolation (“STI”) with “a diffusion layer” because STI was likely to introduce crystal defects that adversely affected device operation. Masagaki, [0002]-[0003]. Trench isolation generally refers to etching out silicon in a trench and refilling the trench with silicon dioxide. Between adjacent photodiodes such a

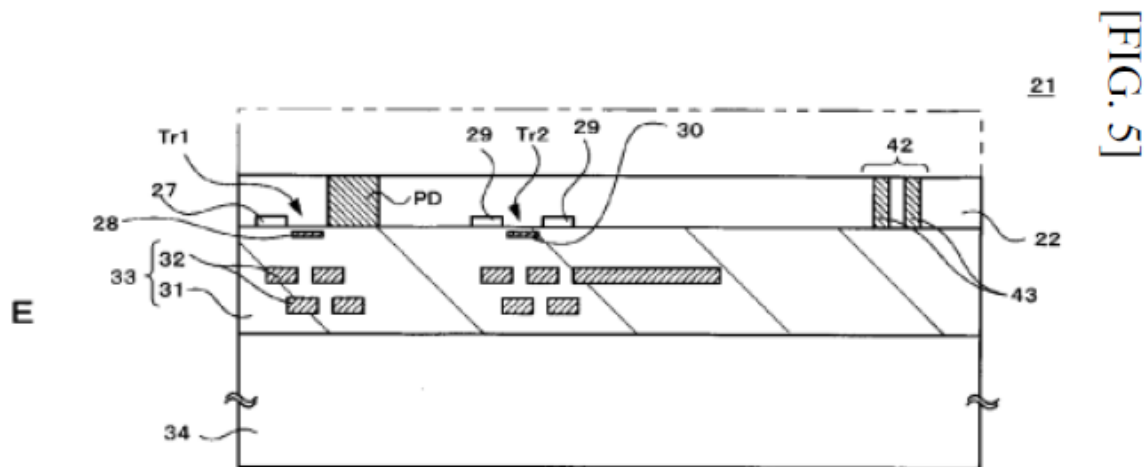
trench can prevent any carriers from flowing between pixels. Therefore, this technique was used for lateral isolation of photodiodes but, as just noted, had the drawback of introducing dark current. The '808 patent also recognizes this known issue. Ex. 1001, 4:54-62. Thus, it was well-known that replacing STI features with ion implanted isolation layers would provide the benefits of an isolation layer but avoid the drawback of the STI's additional dark current generation.

314. Masagaki also explains that it was known that this “diffusion layer” 3 comprised a device separation region, and that it was known to form this region by ion implantation (Masagaki, [0005], [0018]) “between the unit pixel and an adjacent pixel” in a sensor array (*id.*, [0004]).

3. Shiraiwa

315. Japanese Patent Application Publication No. JP 2005-353996 (Ex. 1010, “Shiraiwa”), published December 22, 2005.

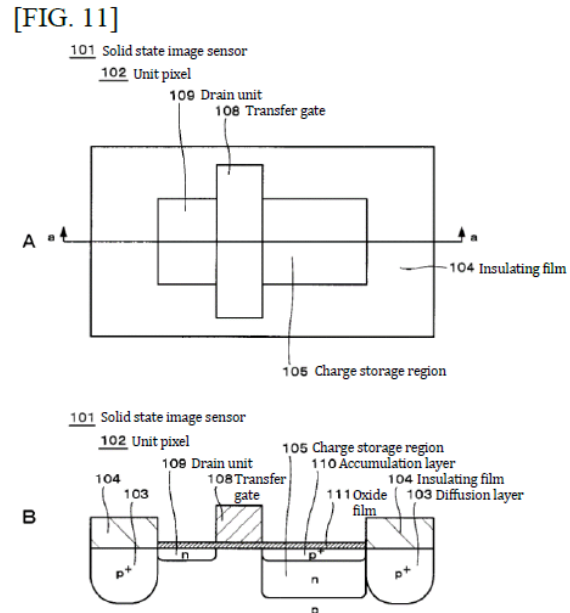
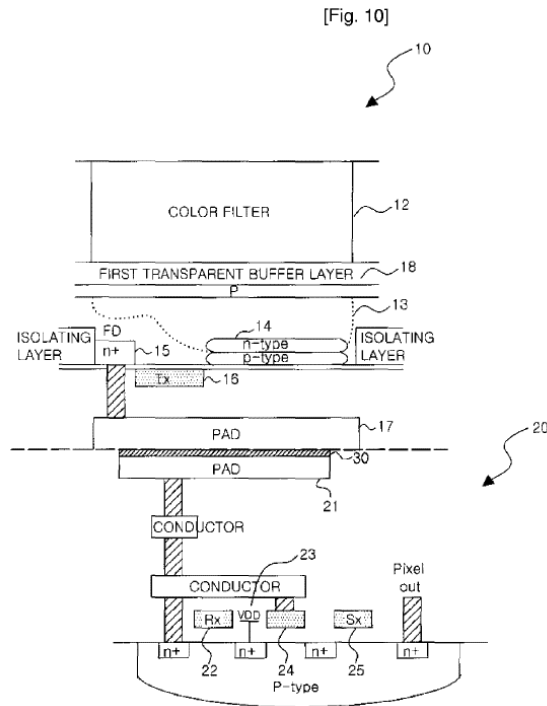
316. Shiraiwa describes a method for thinning the backside of a semiconductor substrate without using the oxide layer in an SOI wafer as an etch stop. Shiraiwa, [0014]-[0024]. Figure 5E shows thinning silicon substrate 22 to expose the photodiode (“PD”) by setting end point detection portion 42 that defines the stopping point for the backside thinning at the same thickness as the photodiode. *Id.*, [0037], Fig. 5E.



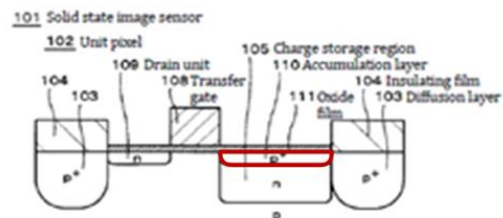
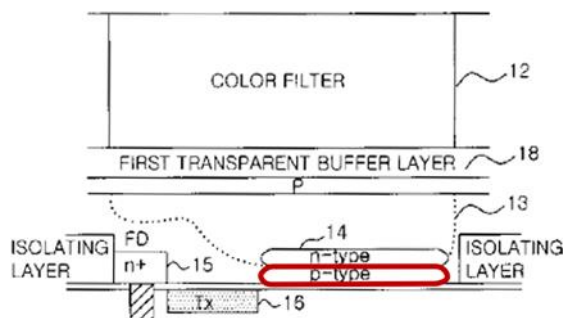
B. Lee+Masagaki+Shiraiwa

317. Lee's separation unit pixel architecture corresponds to a backside-illuminated implementation of Masagaki's prior art unit pixel, shown in cross section on a plane denoted by **a-a** (Masagaki, Fig. 11A) extending vertically through the unit pixel. In other words, Masagaki Figure 11A provides a planar view looking down on the frontside of the unit photodiode. The cross-sectional view marked by the line "**a-a**" is a vertical cut into the device, and out of the page. The arrows on "**a-a**" point in the direction for viewing the cross-sectional view in Figure 11B. This view in Figure 11B is analogous to the cross-sectional view presented by Lee Figure 10. The unit pixels in Lee and Masagaki have the same features, meaning conduction layers, isolation layers, and transfer transistor, with the difference being that Lee shows a unit pixel for a backside-illuminated format, while Masagaki shows the same features arranged for a frontside-illuminated

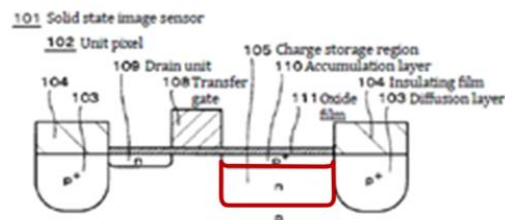
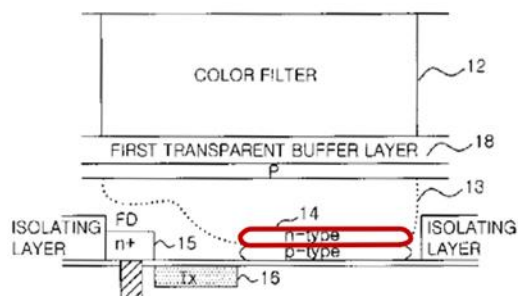
format. Compare Lee, Fig. 10 with Masagaki Fig. 11A & B. In the annotated figures below, Lee is left and Masagaki is right.



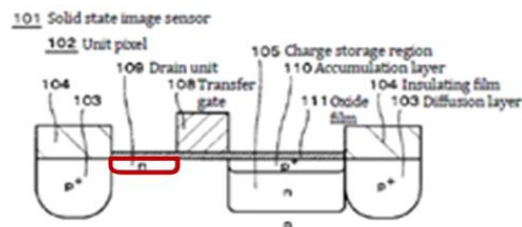
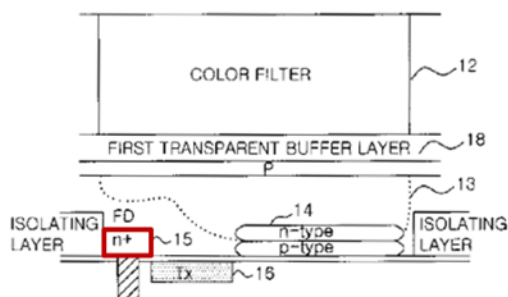
318. Both Lee and Masagaki disclose a photodetector with a p-type pinning layer (unlabeled in Lee, 110 in Masagaki). Masagaki's "accumulation layer 110" is a pinning layer just like Iwabuchi layer 1053, as I explained above for step [1.h.1] with Iwabuchi. *Supra* § V.B.1.f.ii(2).



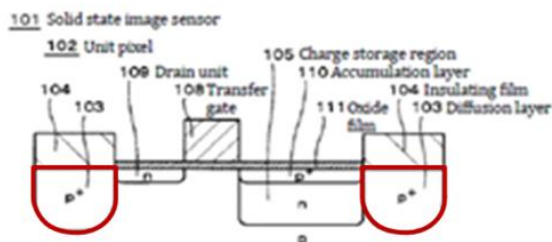
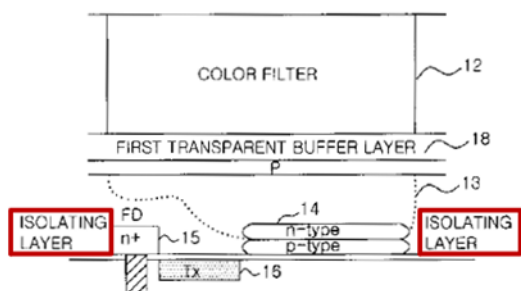
319. Both Lee and Masagaki disclose n-type conduction layer 14 (Lee) and 105 (Masagaki).



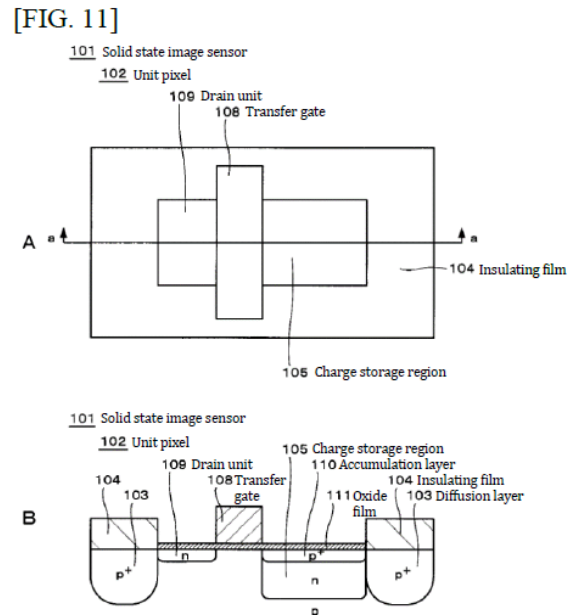
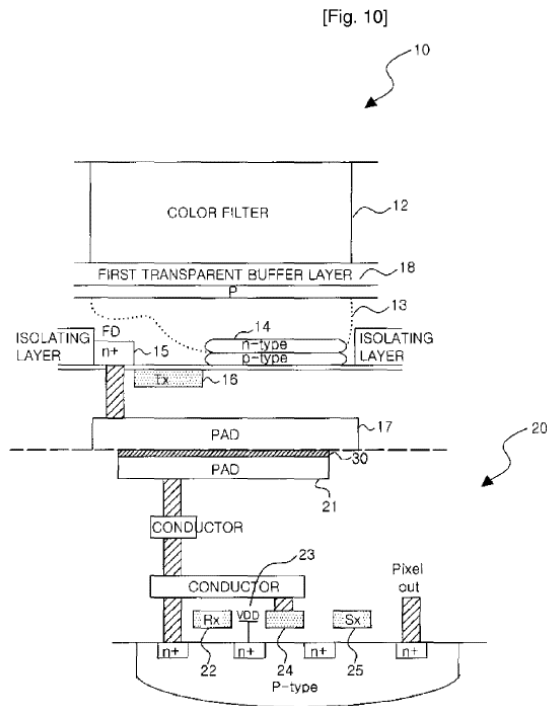
320. Both Lee and Masagaki disclose a transfer transistor with gate 16 (Lee) and 108 (Masagaki) and n-type floating diffusion 15 (Lee) and 109 (Masagaki).

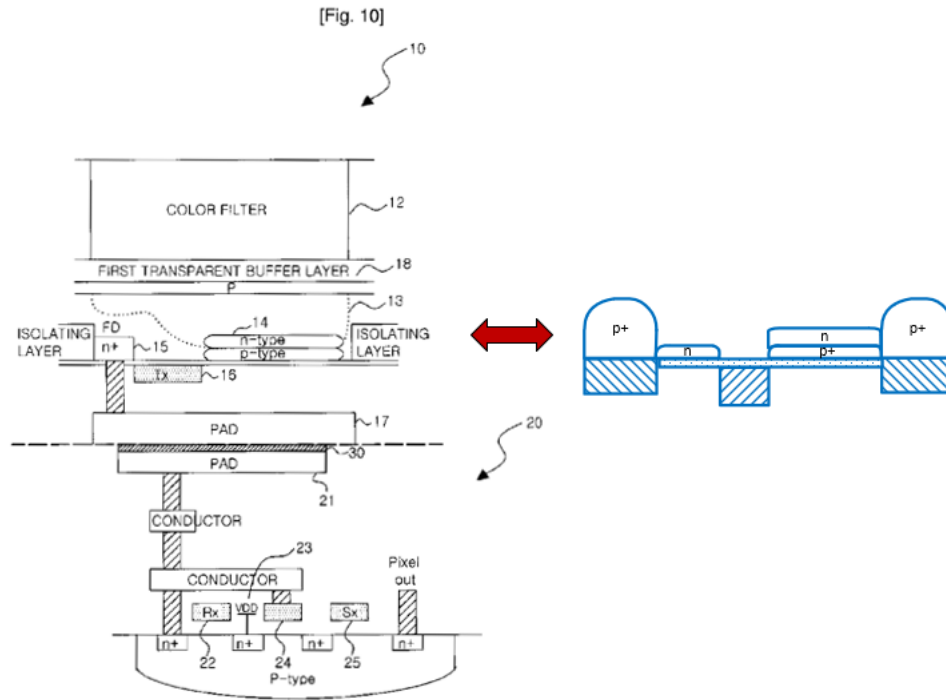


321. Both Lee and Masagaki disclose lateral isolation layers (“isolating layer” in Lee, 103 in Masagaki).



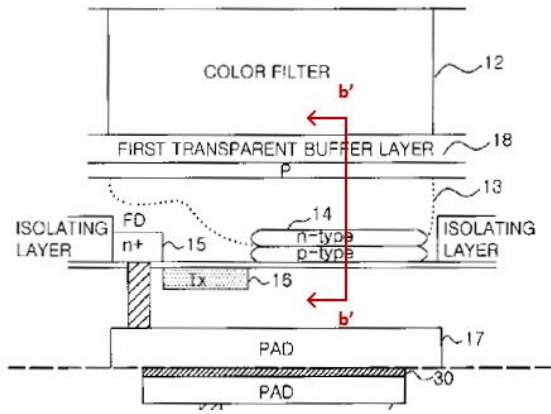
322. In other words, along the cross-sectional views in Lee Fig. 10 and Masagaki Fig. 11, Lee's backside-illuminated detector implements the same photodetector features as the prior art frontside-illuminated detector in Masagaki Fig. 11.



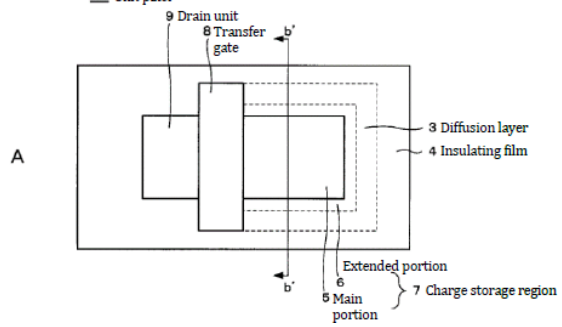


323. Masagaki's novel charge storage region extension involves features in a cross-sectional view on a plane denoted by **b'-b'** as shown in Masagaki Figures 1A, 10.

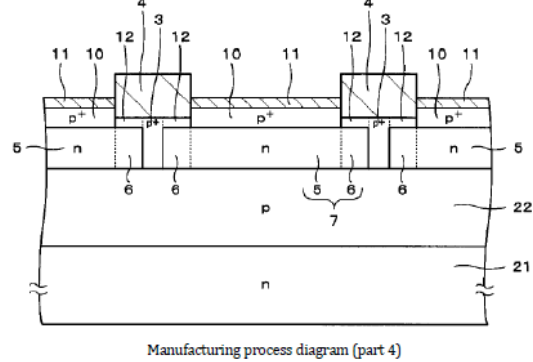
324. Lee's figures do not provide a comparable perspective. Rather, Masagaki's Figure 10 corresponds to a cross-sectional view of the improvement over the prior art structure in Lee, and Figure 11, on a plane **b'-b'** that extends into the page and vertically bisects layer 14 in Lee Fig. 10. Lee, [38], Fig. 10. If Lee had presented this cross-section, it would look similar to that shown in Masagaki Figure 10, without the charge storage region extension 6 in Masagaki Figure 10.



1 Solid state image sensor
2 Unit pixel



1



Masagaki, [0034].

in Lee, Fig. 10 and the floating diffusion connects to Lee's second wafer through a via to pad 17 as shown in Lee Fig. 10.

1. Reasons to combine

329. POSAs would have had several reasons to combine Lee, Masagaki, and Shiraiwa.

330. As discussed above, Lee and Masagaki disclose almost identical structures, with the exception of the novel charge storage region extension in Masagaki, which would improve Lee for the same reason it improves Masagaki's near-identical structure.

331. Both Lee and Masagaki are concerned with mitigating the loss in photodiode sensitivity when reducing pixel dimensions.

332. Both Lee and Masagaki recognized that "the amount of available electric charge decreases when the size of the photodiode decreases," and this adversely affected imaging. Lee, [8] ("The amount of available electric charge of the photodiode is a basic feature of determining a dynamic range of the image sensor, and the decrease of the amount of available electric charge directly affects the image quality of the sensor."); *accord* Masagaki, [0007] ("area reduction of a photodiode leads to a decreased charge storage amount and a worsened S/N ratio and causes a problem of worsened imaging characteristics of the image sensor such as a decreased dynamic range").

333. Lee addresses this problem with a “separation unit pixel” in which “sensitivity drops far [less] than a conventional case in the manufacturing of a miniature pixel.” Lee, [12]. Masagaki’s objective was “to provide a solid state image sensor wherein a unit pixel can be miniaturized without sacrificing an effective area of a charge storage region[.]” Masagaki, [0008].

334. POSAs would have understood that Masagaki’s solution of extending the charge storage region would further improve the sensitivity of the largely similar photodiode structure in Lee’s separation unit pixel, and thus further mitigate the loss of sensitivity associated with reducing pixel dimensions.

335. Both Lee and Shiraiwa describe wafer scale backside-thinned device fabrication. While Lee describes reducing wafer thinning by back side etching or grinding, Fig. 12 (S540), Shiraiwa explains how to do the thinning to provide a precise substrate thickness at lower cost and with less planar variation than obtained when using the oxide layer in SOI wafers as an etch stop. Shiraiwa, [0021]-[0022]. POSAs would have used Shiraiwa because it gives more detailed process information on backside thinning than Lee.

336. In short, POSAs would have recognized that Masagaki’s techniques of manufacturing a unit pixel with an extended charge storage region below and adjacent ion-implanted diffusions could be used to improve the amount of charge storage in Lee’s separation unit pixel in the same way that it improved charge

storage in Masagaki's unit pixel, thereby further mitigating adverse effects of pixel miniaturization on signal to noise ratio, dynamic range, and image quality.

337. Using Shiraiwa's backside thinning methods would have applied known backside-thinning process methods to improve the device

2. Reasonable expectation of success

338. Several factors would have given POSAs a reasonable expectation of success in combining Lee with Masagaki and Shiraiwa. Lee demonstrates that Masagaki's architecture was compatible with Lee's unit pixel because other than the illumination surface Lee uses essentially the same prior art pixel structure that Masagaki modified to improve charge storage as pixel dimensions are reduced.

339. Both Lee and Shiraiwa describe process steps, like backside thinning, and adding a color filter and micro lens, associated with making backside-illuminated detectors. Lee, [52]-[55], Figs. 8 & 11; Shiraiwa, [0027]-[0028], Figs. 1 & 2.

340. Moreover, as Lee demonstrates, it was well-known that photodetector structures for a frontside detector like Masagaki could be implemented in a backside-illuminated architecture like Lee's unit pixel. *E.g.*, Pain2005, 35; Ex. 1038; Lee, Fig. 12 (step S530).

341. Because Lee already describes separately fabricating the first and second wafers before bonding them, POSAs would reasonably expect that using

Masagaki’s known methods to form sensor pixel structures and incorporating Shiraiwa’s more detailed process steps with Lee to form the backside sensor would succeed because it would use known and predictable fabrication methods in known and conventional ways.

342. Because the unit pixel in Lee+Masagaki+Shiraiwa has the same transfer transistor and floating diffusion as Lee, POSAs would have reasonably expected the 3D architecture to continue to work in the same manner as in Lee alone.

C. Claim analysis

1. Claim 1

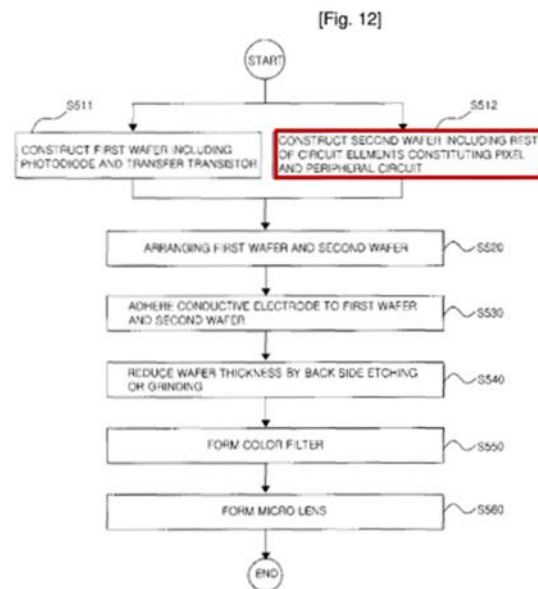
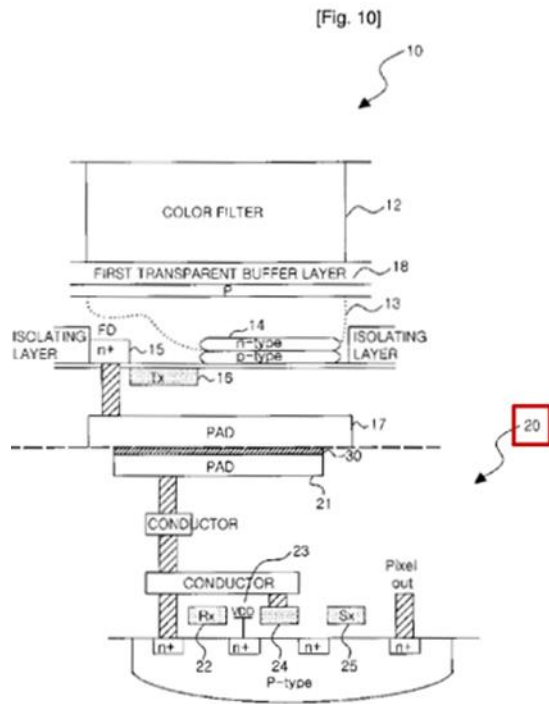
a. Preamble

343. Lee+Masagaki+Shiraiwa meets the preamble because Lee describes methods for manufacturing a three-dimensional (3D) imager. *E.g.*, Lee, [21], claim 7.

b. Step 1.a

1.a	providing a first substrate;
-----	------------------------------

344. Lee+Masagaki+Shiraiwa meets [1.a] because Lee describes providing a “second wafer” with circuit elements. Lee, [14], [33], [35], Figs. 10 (wafer 20) & 12 (step S512). The “second wafer” is the “first substrate.”



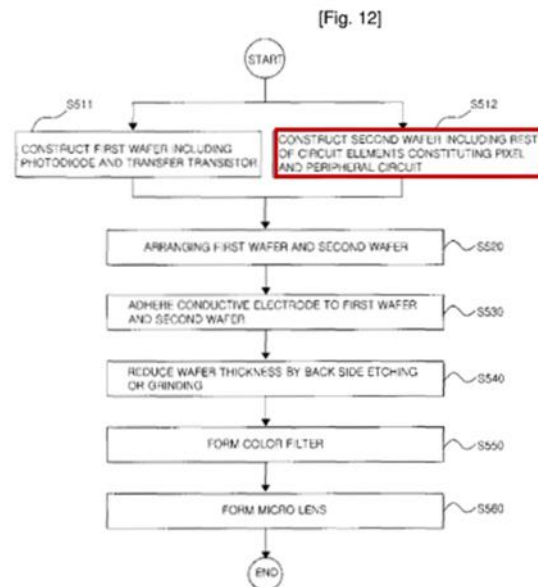
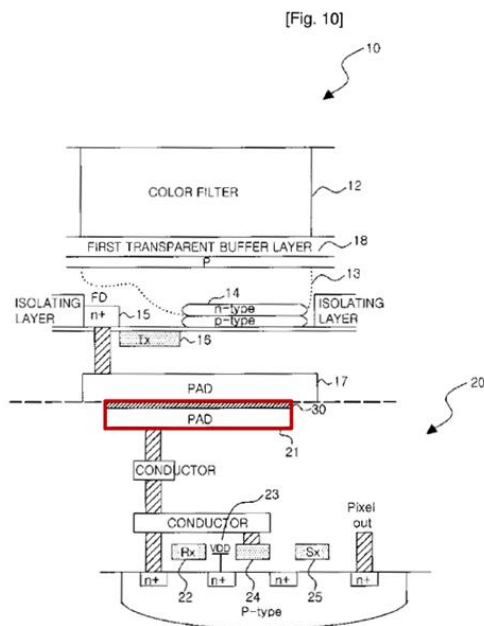
c. Step 1.b

1.b	forming circuitry including a metal interconnection over the first substrate;
-----	---

345. Lee+Masagaki+Shiraiwa meets [1.b] because Lee describes forming “conductive pad 21” and various circuitry over “second wafer 20.” Lee, [15] (“constructing a second wafer”), [41]-[42], [47], Figs. 10 & 12 (S512). For example, each box labeled “n+” in Lee Figure 10 represents a source or drain for “reset transistor 22,” “source-follower transistor 24,” and “select transistor 25.” Lee, [42]. These are formed in Lee’s “second wafer 20,” which is the “first substrate” in steps [1.a] and [1.b].

346. The conductive pads 17 (on the “first wafer 10” / second substrate) and 21 (on the “second wafer 20” / first substrate) are “for external connection,” *e.g.*, interconnection. Lee, [36].

347. POSAs would have understood that “conductive pads” 17 and 21 conventionally comprised a metal such as copper or gold because this was a standard way to provide surface contacts for solid-state devices and a known method to provide interconnection in wafer-to-wafer bonding. This process is termed metallization. ULSI, 371. The term metallization also applies to interconnection between stacked die or wafers. *E.g.*, Balcerak, 386, 389. For example, Patti’s “metal-to-metal” bonding uses metal conductive pads as contacts for vertical interconnection. Patti, 1217; *generally id.*, 1217-1220. POSAs would have found it conventional to form conductive pad 21 over the second wafer from metal.



d. Conduction layers

i. Step [1.c]

1.c	forming a photodiode in a crystalline semiconductor layer of a second substrate;
-----	--

348. Lee+Masagaki+Shiraiwa meets [1.c]. Lee discloses forming a photodiode in a semiconductor substrate comprising the first sensor wafer. Lee, [1], [13]-[14], Fig. 10.

349. Masagaki describes forming a photodiode in a “silicon semiconductor substrate” with a charge storage region extended laterally below a pinning or planar isolation layer and bounded by a “device separation region.” Masagaki, [0009], [0018], [0020], Fig. 10, claim 1.

350. While neither Lee, Masagaki, nor Shiraiwa describe their substrate as “crystalline,” POSAs would have understood that their discussion of SOI wafers, CMOS imagers, and forming transistors in the photodetector meant Lee, Masagaki, and Shiraiwa each involve forming photodiodes in a crystalline semiconductor layer such as layer 12 in Iwabuchi. *Supra*, § V.B.1.d.i (step [1.c]).

351. Shiraiwa describes forming photodiodes in silicon substrate for CMOS solid-state imagers with readout transistors similar to Iwabuchi’s detector. Shiraiwa, [0001], [0027], [0030], [0037], Fig. 2. Shiraiwa’s silicon substrate replaces the top layer of prior art SOI wafers, which were known to be “high-

quality single-crystalline material that is suitable for high-performance and high-density integrated circuits.” Sze, 343-344; Shiraiwa, [0014], [0022].

352. Masagaki describes a CMOS solid-state image sensor with conduction layers “formed on a silicon semiconductor substrate.” Masagaki, [0018] (“In this p-type semiconductor well region, a plurality of unit pixels 2 is made by being formed in a partitioned manner, the unit pixels 2 being insulated from each other by a device separation region[.]”), [0019] (“Each unit pixel 2 has, at the least, a charge storage region 7 constituting a photoelectric conversion unit—that is, a photodiode; a transfer gate 8 and a drain unit 9 constituting a floating diffusion[.]”).

353. Lee describes forming a transfer transistor in the unit pixel containing a photodiode. Lee, [46], Fig. 10.

354. It was well-known and conventional to form CMOS imagers and CMOS transistors in crystalline semiconductor substrates and this would have been obvious given these disclosures in Lee, Masagaki, and Shiraiwa.

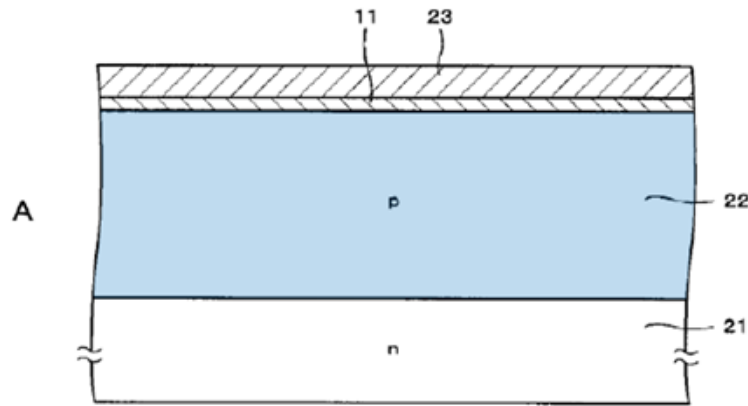
ii. Steps [1.g], [1.g.1]

1.g	wherein forming the photodiode comprises:
1.g.1	forming a second conduction type conduction layer in the crystalline semiconductor layer; and

355. Lee+Masagaki+Shiraiwa meets [1.g] and [1.g.1]. Masagaki describes forming a photodiode comprising p-type layer 22 on silicon substrate 21 as the first

step in making the unit pixel. Masagaki, [0035] & Fig. 7. The p-type layer 22 is the [1.g.1] second conduction type conduction layer.

[FIG. 7]



iii. Step [1.g.2]

1.g.2	forming a first conduction type conduction layer over the second conduction type conduction layer ,
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356. Lee+Masagaki+Shiraiwa meets [1.g.2]. After forming p-layer 22, Masagaki describes forming n-type layer 7, which it calls a charge storage region. Masagaki, [0038]-[0039] & Fig. 9F.

357. This comprises “main portion 5” and “extended portion 6.” Masagaki, [0031], Fig. 9F. The n-type charge storage region 7, including extended region 6, is the [1.g.2] “first conduction type conduction layer.” Relative to the backside surface, layer 7 is “over” layer 22 just like the ’808 patent describes layer 214 is over layer 212. *Compare* Masagaki, Fig. 9F, *with* Ex. 1001, Fig. 2.

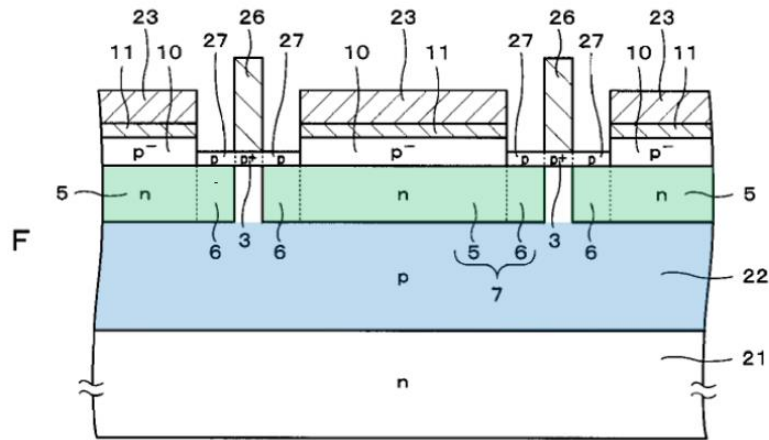
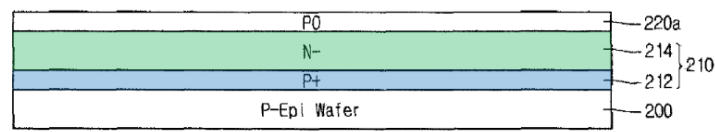


FIG. 2



iv. Conduction layer fabrication sequence

358. As just explained, Masagaki describes forming layer 22 (step [1.g.1]) before forming layer 7 (step [1.g.2]).

e. Isolation layers

i. Steps [1.d]

1.d	forming an ion implantation isolation layer in the photodiode;
-----	--

359. Lee+Masagaki+Shiraiwa meets [1.d] as explained for steps [1.h.1] and [1.h.2].

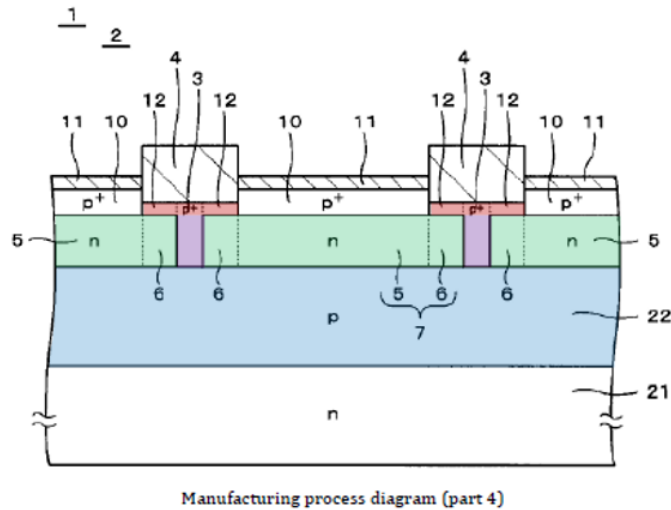
ii. Step [1.h.1]

1.h.1	wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer over the first conduction type conduction layer ,
-------	--

360. Lee+Masagaki+Shiraiwa meets [1.h.1]. Masagaki describes forming “extending diffusion layer 12” by p-type (“second conduction type”) ion implantation after having formed the [1.g.2] conduction layer. Masagaki, [0040] (describing “implantation of a p-type impurity” to form “extended diffusion layer 12 having approximately the same p-type impurity concentration as the diffusion layer 3[.]”).

361. Moreover, “accumulation layer 10 suppresses dark current due to an interface state[.]” Masagaki, [0020]. Masagaki layer 10 is also an ion implantation isolation layer meeting step [1.h.1]. POSAs would have formed layer 10 by ion implantation after forming n layer 5. Masagaki, [0033] (“normal processes are used to form...layer 10”); Mann, [0024] (“The isolation surface implant 410 is used to provide electrical isolation to the photodiode 105 to prevent the depletion region of the photodiode 105 from contacting the silicon surface.”).

[FIG. 10]



362. POSAs would have formed layer 10 by ion implantation after forming n layer 5. Masagaki requires this implant after forming n-type region 6 because the n-type implant to form region 6 for step [1.g.2] “decreased” the p-type impurity concentration in the region of layer 12. Masagaki, [0040].

363. Layers 10 and 12 are an isolation layer because they are a diffusion that isolates the n-type charge storage region 6 from the frontside surface interface, which contains interface states that cause white spots in imaging. Masagaki, [0018]-[0020], Fig. 10. In the combination Lee+Masagaki+Shiraiwa, the frontside surface interface is at the junction between pixel features and the gate dielectric shown in Lee Figs 8 and 10 extending across the frontside surface of the pixel.

364. Layers 10 and 12 are formed “over” layer 7 meeting [1.g.2], *supra* § VIII.C.1.d.iii, and in particular it is formed “over” extended portion 6. Masagaki,

Fig. 10. Layer 12 is formed to have the same conductivity as layer 3. Masagaki, [0040].

365. For purposes of step [1.h.1], the “second conduction type first isolation layer” is *the planar top of the “T” provided by layers 12 and the top of layer 3* as shaded red in annotated Fig. 10.

366. In the alternative, the “second conduction type first isolation layer” further includes layer 10.

iii. Step [1.h.2]

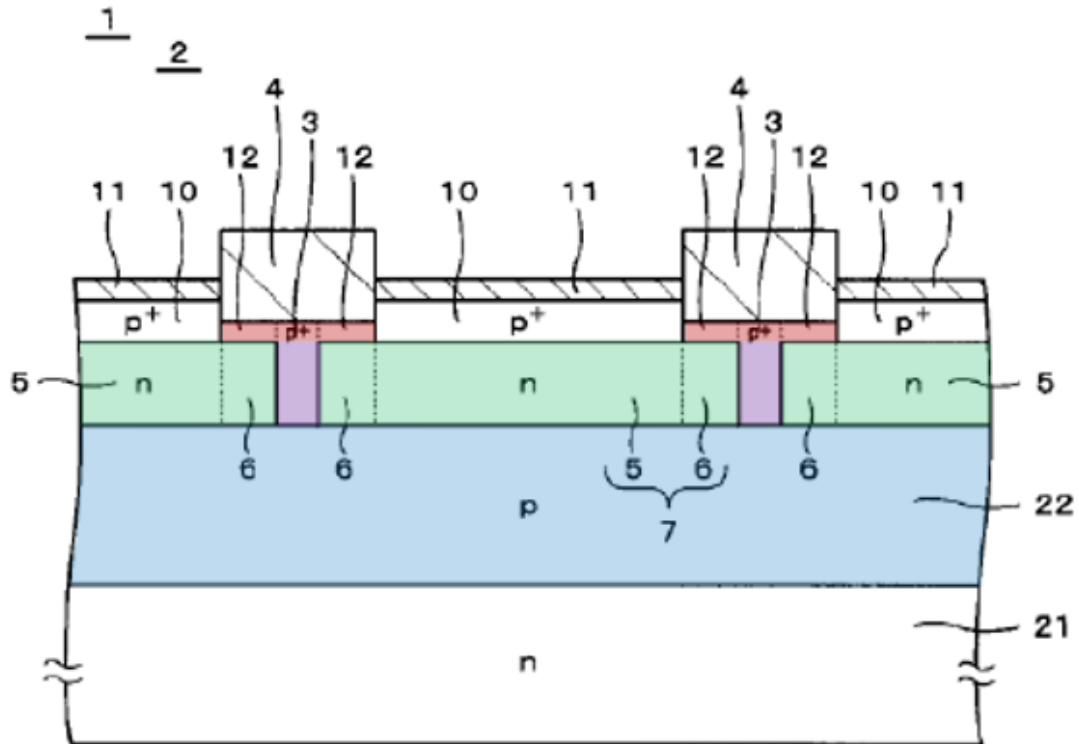
1.h.2	wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.
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367. Lee+Masagaki+Shiraiwa meets [1.h.2]. Masagaki describes forming “the diffusion layer 3 that ultimately constitutes the device separation region” by p-type ion implantation. Masagaki, [0037].

368. POSAs would have understood that Masagaki’s description of forming separation region 3 by “ion implantation that increases the depth of the diffusion layer 3” or “several implantations in the depth direction” in a first embodiment of Fig. 4, Masagaki, [0030], was also applicable to the embodiment shown in Figures 9 and 10, even if not specifically described for this second embodiment, because the two embodiments are shown with the same pixel

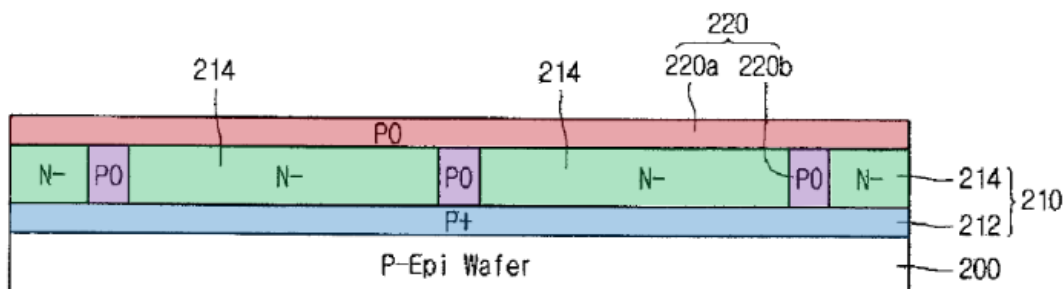
separation region 3, formed in the substrate, and both extending to the depth of the charge storage layer 7. Masagaki, Figs. 4, 6, 9, 10.

[FIG. 10]



Manufacturing process diagram (part 4)

FIG. 3



369. Masagaki forms diffusion layer 3 “at an interface between pixels of the photodiode” because it separates adjacent pixels exactly like 220b in the ’808 patent, and like the “P-well” labeled “220b” in PO’s infringement contentions. Masagaki, [0034] (“This embodiment describes a manufacturing method in a situation wherein only the unit pixels are adjacent to each other via the device separation region.”); Ex. 1001, Fig. 3; IC-A1, 27; *supra* § V.B.1.f.iii (discussing IC-A1, 27). Thus, forming layer 3 meets [1.h.2].

f. Step 1.e

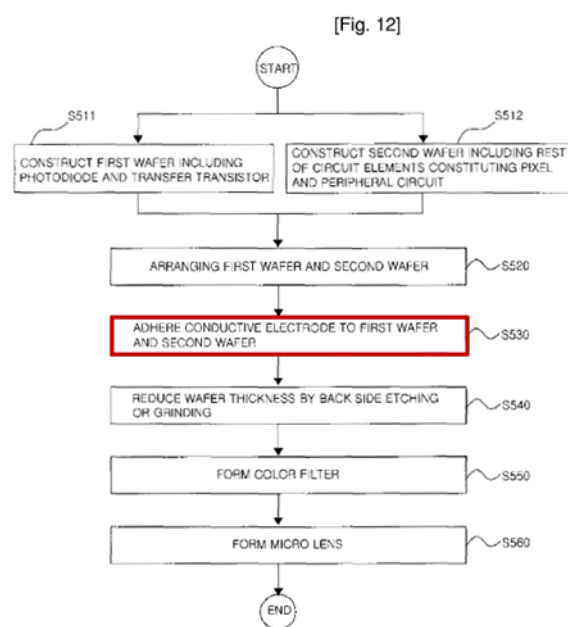
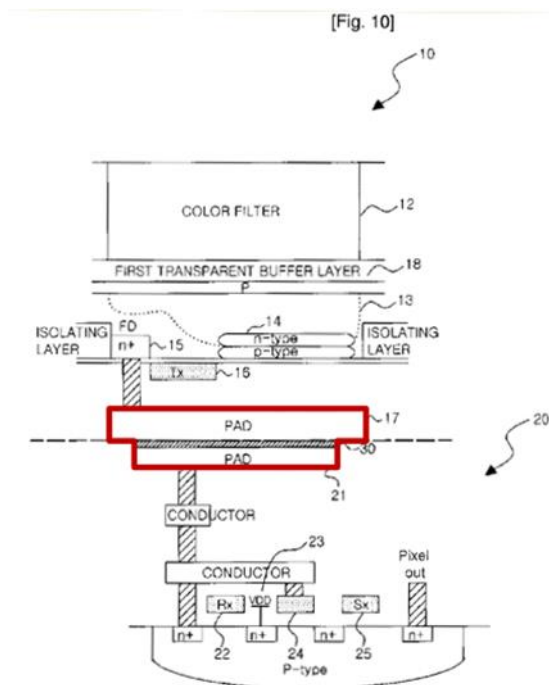
1.e	bonding the first substrate to the second substrate to connect the photodiode to the metal interconnection; and
-----	---

i. “bonding”

370. Lee+Masagaki+Shiraiwa meets [1.e] “bonding the first substrate to the second substrate” because Lee describes bonding the first wafer to the second wafer. “[T]here is provided a manufacturing method” “comprising” “(d) adhering a pad of a unit pixel on the first and second wafers arranged up and down[.]” Lee,

[15]; *id.*, [51], [53] (describing thinning step “[a]fter the first wafer is adhered to the second wafer[.]”), Figs. 10 & 12 (step S530).

371. Moreover, it was known to bond wafers by adhering opposing metal contacts. Exs. 1027, 1030. The most common method was flip-chip bonding invented by IBM in the 1970’s for packaging bipolar arrays, and adapted for wafer-to-wafer bonding in the 1980’s. *E.g.*, Lindner. As the desired interconnect density increased, this moved to copper pillar bonding and microbump bonding at the wafer-to-wafer level. The same assembly can be carried out at the chip level or the wafer level, but wafer level bonding offers the lowest cost per interconnection because of the improved stiffness and planarity of the wafers. *E.g.*, Patti, 1216.



ii. “bonding... to connect”

372. Lee+Masagaki+Shiraiwa further meets [1.e] “bonding... to connect the photodiode to the metal interconnection” based on the PO’s construction of “to connect” in its infringement contentions, *supra* § V.B.1.g.i (step [1.e]), because Lee describes conductive pad 21 and the second wafer pixel readout circuitry electrically connecting to a floating diffusion (“FD”) 15 in each pixel. Lee, [39] (“In the present invention, the floating diffusion area 15 connected to the external circuit is connected to the conductive pad 17.”), Abstract (“a first wafer [] includes a photodiode, a transfer transistor, a node of a floating diffusion area...and a pad connecting the floating diffusion area and the transfer transistor to an external circuit”), Figs. 4 & 10, claim 1.

373. The FD “transfers optical electric charge included in the photodiode[.]” Lee, [13]; *id.*, [29] (“A transfer transistor 6 connects and separates the floating diffusion area 5 and photodiode 4.”), Fig. 8.

[60]-[61], Figs. 12 (step S540) & 14, claim 7 (step (e)) (describing thinning “the back side of the first wafer” “to reduce the wafer thickness”). This was conventional. Gouscha, 4:33-63; Iwabuchi, [0065], [0150] & Fig. 10G.

* * *

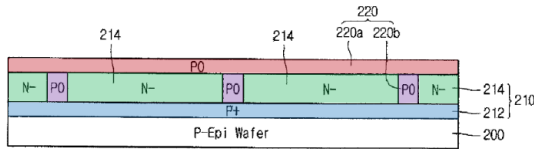
377. Taken as a whole claim 1 would have been obvious over Lee+Masagaki+Shiraiwa.

2. Claim 4

The method of claim 1, comprising forming the ion implantation isolation layer over at least one of a side of the photodiode and a bottom of the photodiode.

378. Lee+Masagaki+Shiraiwa renders claim 1 obvious. *Supra* § VIII.C.1. Lee+Masagaki+Shiraiwa also renders claim 4 obvious because Masagaki describes diffusion 3, which is the [1.h.2] ion implantation layer, formed “over a side of the photodiode” in exactly the same way as layer 220b in the ’808 patent. Masagaki, Fig. 10; Ex. 1001, Fig. 3.

FIG. 3



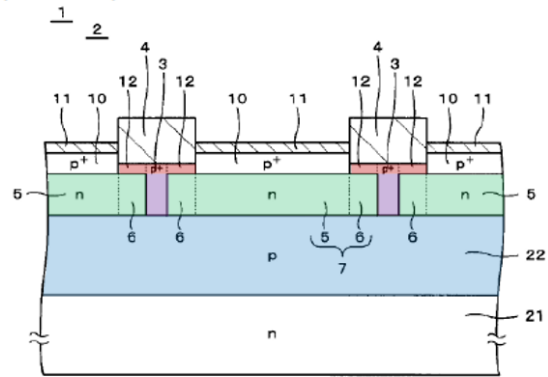
'808 patent

3. Claim 5

The method of claim 1, wherein the ion implantation isolation layer comprises a P0 layer.

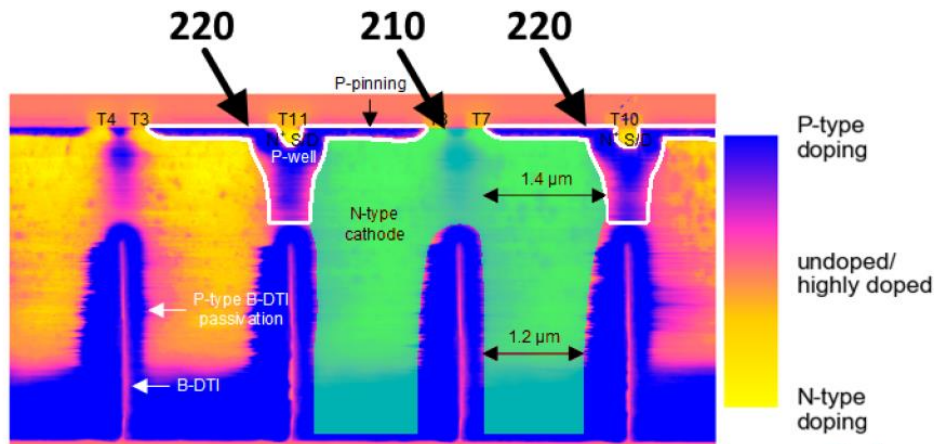
379. As explained *supra* § V.B.3, PO's infringement contentions contend that a doping concentration transition from p^+ to n^+ between a p^+ well and n^+ conduction layer meets claim 5 because this "includes" a "P0 layer." IC-A1, 30 (in region marked 220 doping concentration transition colored pink/purple between blue p well and orange n conduction layer).

[FIG. 10]



Manufacturing process diagram (part 4)

Masagaki



PO infringement contentions (claim 5). IC-A1, 30.

380. Based on PO's infringement contentions, as discussed *supra* § V.B.3, Lee+Masagaki+Shiraiwa meets claim 5 because Masagaki's p-type ion implantations in layers 10, 12 and 3 (a) are p-type. and/or (b) will necessarily have a real-world transition in doping concentration at the junction with the abutting n-type doping layer 7.

381. Masagaki describes a second p-type implant to form layer 12 because the n-type implant through diffusion 3 to form layer 6 would have reduced p-type dopant concentration. Masagaki, [0040]. POSAs would have understood that annealing to cure crystal damage from ion implantation would have caused p and n dopants to diffuse, which would contribute to a non-abrupt transition from p⁺ to n⁺ concentrations in the region of a metallurgical junction. *E.g.*, Sze-2002, 466-480.

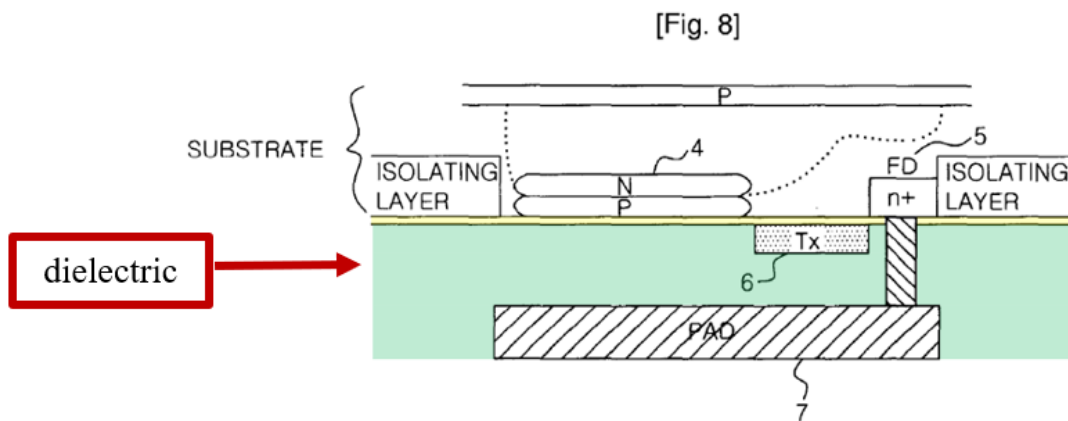
4. Claim 6

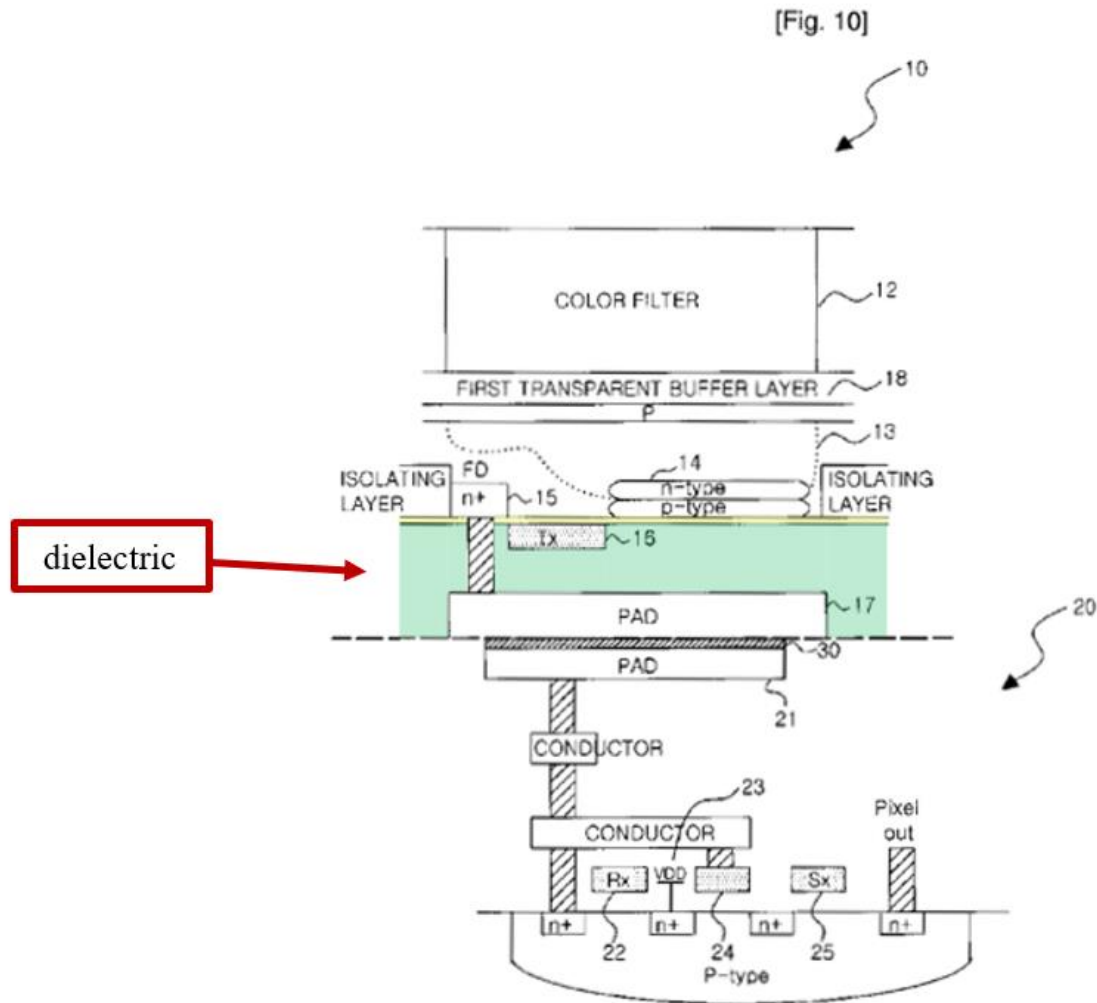
382. Lee+Masagaki+Shiraiwa meets claim 6 as follows.

a. Step 6.a

6.a	The method of claim 1, comprising: forming a dielectric over the photodiode of the second substrate before bonding the first and second substrates; and
-----	---

383. Lee+Masagaki+Shiraiwa meets claim 1. *Supra* § VIII.C.1. Lee further meets step [6.a]. Lee shows the separation unit pixel on the first wafer (“second substrate”) with a dielectric formed “over” the photodiode in the unit pixel. *E.g.*, Lee, Figs. 8 & 10.





384. Lee describes placing conductive pad 17 on the first wafer, Lee [37]-[39], but does not describe forming the layer that receives pad 17. Nonetheless, Figs. 8 and 10 clearly show a material layer holding pad 17 and, in Fig. 10, forming part of a physical connection to the second wafer (first substrate) after a bonding step. Lee, Figs. 8, 10.

385. It was well-known to form transistor gates, metal layers like pad 17, and the via connecting pad 16 to FD 17, in a dielectric. *E.g.*, Iwabuchi, [0145] (forming interlayer insulator 20 with transistor 15), Figs. 10B, 10C, & 11. These would be formed in standard CMOS VLSI style deposition and etching steps. Sze-2002, 396, 400. In addition, direct gold bump connections and compliant bump technologies were known at the time. *E.g.*, Keswick.

386. Thus a POSA would have understood that it was conventional to form a dielectric over the photodiode in the Lee+Masagaki+Shiraiwa unit pixel, meeting [6.a].

b. Step 6.b

6.b	forming a metal pad in the dielectric.
-----	--

387. Lee shows conductive pad 17 formed in the region marked dielectric layer B. Lee, Figs. 8, 10. While Lee does not describe pad 17 as “metal,” POSAs would have found it conventional to form pad 17 from metal for the same reason it would have been conventional to form conductive pad 21 from metal. *Supra* § VIII.C.1.c (step [1.b]).

388. Thus, Lee+Masagaki+Shiraiwa renders obvious claim 6.

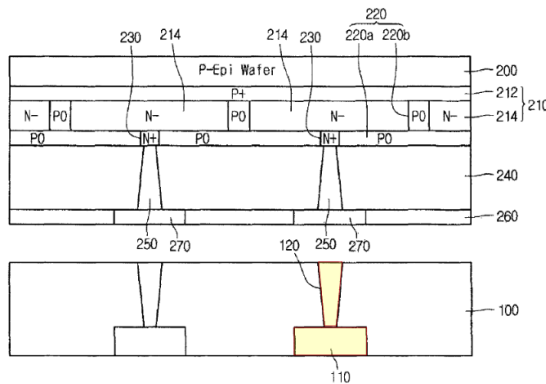
5. Claim 8

The method of claim 1, wherein forming the circuitry including the metal interconnection comprises forming a metal and a plug over the first substrate.

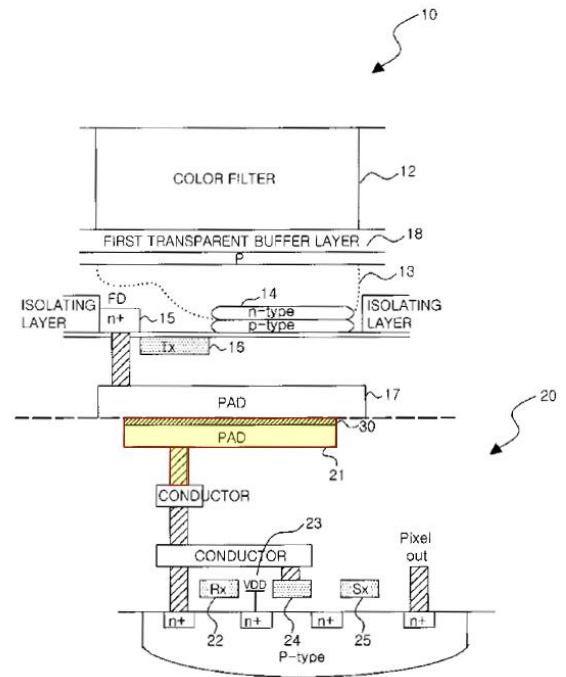
389. Lee+Masagaki+Shiraiwa meets claim 1. *Supra* § VIII.C.1.

390. Based on PO's infringement contentions as discussed *supra* § V.B.5, Lee+Masagaki+Shiraiwa renders obvious claim 8 because Lee describes conductive pad 21 and multiple vertical conductors in the second wafer ("first substrate). Lee, [41]-[42], Fig. 10.

FIG. 7



[Fig. 10]



391. POSAs would have understood that conventionally conductive pad 21 would be formed as a metal pad. *Supra* § VIII.C.4.b (step [6.b]). While Lee does not describe the vertical interconnects formed in the second wafer, it was well-known and conventional to provide conductive vertical interconnects as metal-filled vias. *E.g.*, Iwabuchi, [0148]. J.H. Wu demonstrated through wafer vias in 2000. Wu, 20.1.1 ("To provide a low-inductance interconnect, we have developed

a through-wafer via technology in silicon that incorporates a silicon nitride barrier liner and is filled with electroplated Cu.”).

392. POSAs would therefore have found it conventional to form the vertical connections in the second wafer in Lee’s Fig. 10 as metal-filled vias.

393. Based on PO’s infringement contentions, *supra* § V.B.5, conductive pad 21 provides a “metal” and a metal-filled via provides a “plug,” meeting claim 8.

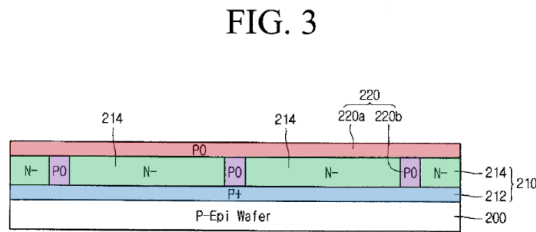
6. Claim 9

The method of claim 1, wherein the **second conduction type second ion implantation isolation layer** is disposed to directly contact on a top surface of the **second conduction type first ion implantation isolation layer** and a bottom surface of the **second conduction type conduction layer**.

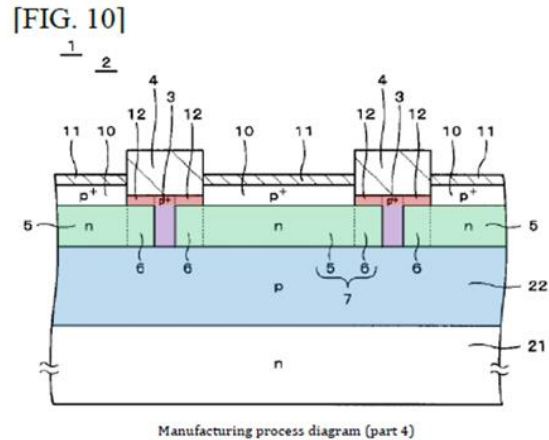
394. Lee+Masagaki+Shiraiwa meets claim 9.

395. First, Lee+Masagaki+Shiraiwa meets claim 1. *Supra* § VIII.C.1.

396. Second, Masagaki layer 3 is the “**second conduction type second ion implantation isolation layer**” in [1.h.2] (*supra* § VIII.C.1.e.iii), and that top of the “T” comprising layer 12 and the top of layer 3 shaded red in annotated Fig. 10 is the “**second conduction type first ion implantation isolation layer**” in [1.h.1] (*supra* § VIII.C.1.e.ii). Layer 22 is the “**second conduction type conduction layer**” in [1.g.1] (*supra* § VIII.C.1.d.ii).



'808 patent

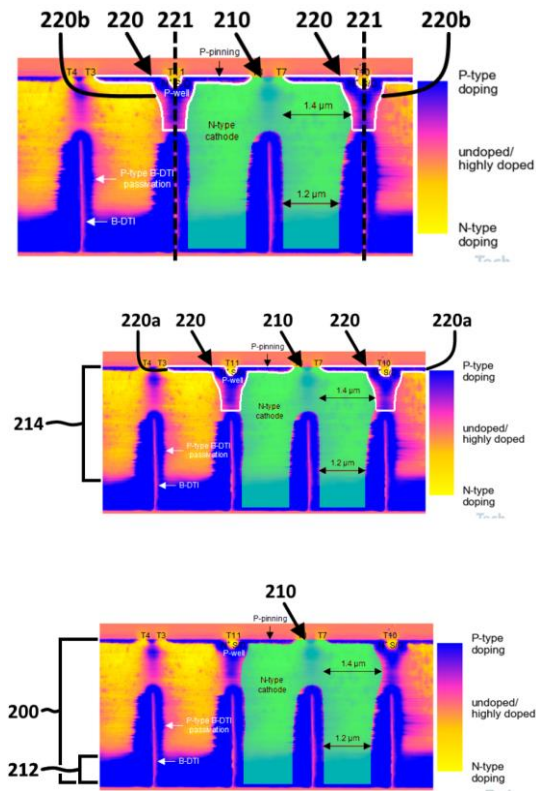


Masagaki

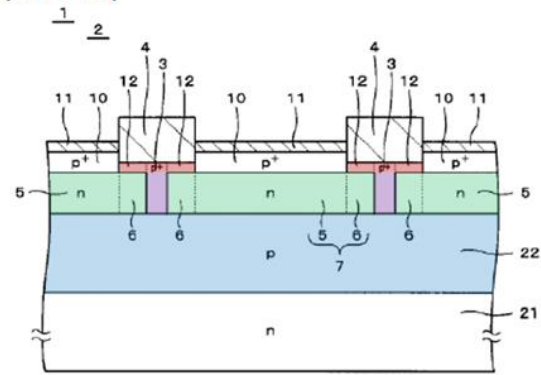
397. Layer 3 “is disposed to directly contact on a bottom surface” of layer 22 and a “top surface” of layer 12 in the same manner that '808 patent layer 220b contact the “bottom” of layer 212 and “top” of layer 220a, with “bottom” and “top” referenced to a topside surface (top of '808 patent Fig. 3 or Masagaki Fig. 10).

Masagaki, Fig. 10; Ex. 1001, Fig. 3.

398. In its infringement contentions, PO contends that claim 9 is met by layer 220b as shown below. IC-A1, 36-38. Lee+Masagaki+Shiraiwa meets claim because Masagaki shows layer 3 contacting layer 12 and layer 22 in the same way that PO maps claim 9 to regions labelled 220b, 212, and 220a in its infringement contentions.



[FIG. 10]



PO contentions. IC-A1, 36-38.

Masagaki

399. Thus, Lee+Masagaki+Shiraiwa renders claim 9 obvious.

IX. GROUND 2B: LEE+MASAGAKI+SHIRAIWA+MARUYAMA RENDERS OBVIOUS CLAIM 2

400. Neither Lee, Masagaki, nor Shiraiwa provide junction depth details.

POSAs would have used Maruyama's known methods of setting the p layer 22 junction depth for the same reasons, and with the same expectations of success, explained with Iwabuchi *supra* § VI.B.

401. Lee+Masagaki+Shiraiwa+Maruyama meets claim 1 for the same reasons that Lee+Masagaki+Shiraiwa alone meets claim 1. *Supra* § VIII.C.1.

402. In Lee+Masagaki+Shiraiwa+Maruyama backside p-layer in Lee (Fig. 10), which corresponds to Masagaki p-layer 22 in a backside format, has a junction depth under 0.5 μm as described in Maruyama. This meets claim 2.

X. GROUND 2C: LEE+MASAGAKI+SHIRAIWA+TONG RENDERS OBVIOUS CLAIM 7

A. Tong

403. U.S. Patent Application Publication No. US 2005/0161795 A1 (Ex. 1029, “Tong”) published July 28, 2005.

404. Tong describes low-temperature wafer direct bonding using plasma treatment with inert gases to “enhance the bonding energy at room temperature for both metal/metal and oxide/oxide bonds.” Tong, [0080].

B. Lee+Masagaki+Shiraiwa+Tong

405. Lee describes adhering wafers at conductive pads without describing the bonding process. Lee, [51]. Tong’s wafer direct bonding improved on existing techniques by bonding at room temperature, providing hermetic bonds without the stress and inhomogeneity of adhesive bonding. Tong, [0009]. Tong also benefited three-dimensional systems-on-chip (“SoC”) like Lee because it allowed “direct wafer bonding of non-metal between wafers” allowing “[v]ery small bonding metal pads” resulting in low parasitics, reduced power, and increasing bandwidth capacity. Tong, [0010], [0012].

406. As explained *supra* § VIII.C.4.a, Lee discloses bonding hybrid wafer surfaces with conductive pads formed in a dielectric. Tong describes bonding “opposing wafers with reciprocal metal bonding pads” just like Lee. Tong, [0082]; *supra* § VIII.C.1.f.i (step [1.e]); Lee, [51] (bonding wafers by “adhering” opposing conductive pads). On each wafer Lee’s conductive pads are surrounding by insulator. Lee, Fig. 10; *supra* § VIII.C.4. In Tong, “the bonding of the non-metal regions generates the requisite bonding force to form the metal-to-metal interconnections across the dies.” Tong, [0083].

407. POSAs would have understood that Tong’s plasma activation would have improved the adhesion between metal pads in Lee and improved bonding between the opposing dielectrics surrounding Lee’s conductive pads, in the same way that it enhanced low temperature bonding energy in Tong.

408. POSAs would have reasonably expected Tong’s methods to improve yield and allow smaller bonding pads with electrical performance improvements for the reasons explained in Tong and because Lee+Masagaki+Shiraiwa+Tong uses Tong’s known fabrication methods in predictable semiconductor device manufacturing in Tong’s known ways. Tong, [0008].

409. Manufacturing Lee+Masagaki+Shiraiwa’s imager with Tong’s bonding methods is Lee+Masagaki+Shiraiwa+Tong.

C. Claim 7

The method of claim 1, wherein bonding the first substrate to the second substrate comprises contacting the first substrate and the second substrate with each other and performing activation by plasma.

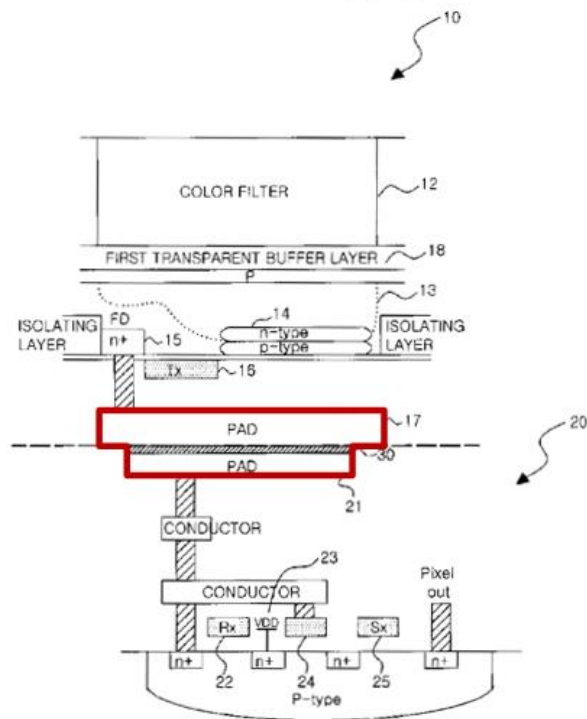
410. Lee+Masagaki+Shiraiwa+Tong meets claim 1 for the same reasons that Lee+Masagaki+Shiraiwa alone meets claim 1. *Supra*, § VIII.C.1.

411. As explained *supra* § VIII.C.1.c (step [1.b]), POSAs would have found it obvious to form Lee’s conductive pads 17 and 21 in Lee’s first and second wafers, respectively, using gold or copper.

412. To the extent the Lee+Masagaki+Shiraiwa conductive pads comprised copper, following Tong a POSA would have coated the copper bonding pad with oxidation-resistant gold. Tong, [0075], [0080]. Then Tong describes plasma treatment to “enhance the bonding energy at room temperature for both metal/metal and oxide/oxide bonds.” Tong, [0080]. This is plasma activation.

413. Lee+Masagaki+Shiraiwa+Tong renders obvious claim 7.

[Fig. 10]



XI. CONCLUSION

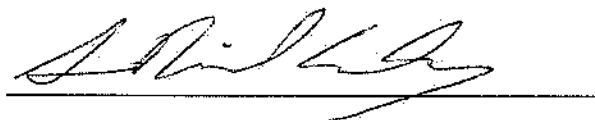
414. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner or its expert(s) may raise and to account for new information as it becomes available to me.

* * *

I declare that all statements made herein of my own knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

I declare under penalty of perjury that the foregoing is true and correct.

Dated: 12/9/2022

A handwritten signature in dark ink, appearing to read "L. Richard Carley", written over a horizontal line.

L. Richard Carley, Ph.D.

APPENDIX A: MATERIALS CONSIDERED

Exhibit	Description
1001	U.S. Patent No. 7,867,808
1002	Prosecution History of U.S. Patent No. 7,867,808
1003	RESERVED
1004	Curriculum Vitae of Dr. L. Richard Carley
1005	U.S. Patent Application Pub. No. US 2006/0197007 A1 (“Iwabuchi”)
1006	Japanese Patent Application Pub. No. JP 2006-93587 A (“Maruyama”)
1007	T. Suga et al., “Surface activated bonding for new flip chip and bumpless interconnect systems.” <i>52nd Electronic Components and Technology Conference</i> 2002, pp. 105-111, 2002 (“Suga”)
1008	PCT Application Pub. No. WO 2006/109937 A1 (“Lee”)
1009	Japanese Patent Application Publication No. JP 2006-303385 A (“Masagaki”)
1010	Japanese Patent Application Publication No. JP 2005-353996 (“Shiraiwa”)
1011	G. C. Bethea et al., “Long wavelength infrared 128×128 Al _x Ga _{1-x} As/GaAs quantum well infrared camera and imaging system,” <i>IEEE Transactions on Electron Devices</i> , vol. 40, no. 11, pp. 1957-1963, Nov. 1993 (“Bethea”)
1012	V. Dragoi and P. Lindner, “Plasma Activated Wafer Bonding of Silicon: In Situ and Ex Situ Processes.” <i>ECS Transactions</i> , vol. 3, no. 6, pp. 147-154, 2006 (“Dragoi”)
1013	Pages from S.M. Sze and Kwok K. Ng, <i>Physics of Semiconductor Devices</i> , John Wiley & Sons (3d ed. 2007) (“Sze”)
1014	A. Rogalski, “Infrared Detectors: Status and Trends.” <i>Progress in Quantum Electronics</i> , vol. 27, pp. 59-210, 2003 (“Rogalski”)
1015	U.S. Patent Application Pub. No. 2006/0043519 A1 (“Ezaki”)
1016	U.S. Patent Application Pub. No. 2003/0025160 A1 (“Suzuki”)
1017	Exhibit A1 to VisionX Infringement Contentions in <i>VisionX Technologies, LLC v. Sony Group Corp. et al.</i> , No. 2:22-cv-00178 (E.D. Tex.), served September 8, 2022 (“IC-A1”)
1018	U.S. Patent No. 6,074,895 (“Dery”)
1019	K. W. Oh and C. H. Ahn, “Flip-chip packaging with micromachined conductive polymer bumps.” <i>Proceedings of 3rd International Conference on Adhesive Joining and Coating Technology in Electronics Manufacturing</i> 1998 (Cat. No.98EX180), pp. 224-228, 1998 (“Oh”)

Exhibit	Description
1020	R. Balcerak and S. Horn, "Progress in the development of vertically integrated sensor arrays," <i>Proc. SPIE</i> 5783, Infrared Technology and Applications XXXI, pp. 384-390, 2005 ("Balcerak")
1021	B. Pain et al., "A Back-Illuminated Megapixel CMOS Image Sensor," in <i>Proceedings IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors</i> , pp. 35-38, 2005 ("Pain2005")
1022	U.S. Patent No. 6,762,473 B1 ("Gouscha")
1023	Pages from The Penguin Complete English Dictionary (2006)
1024	RESERVED
1025	U.S. Patent No. 5,903,021 ("Guidash")
1026	Pages from <i>Wiley Electrical and Electronics Engineering Dictionary</i> , John Wiley & Sons, Inc. (2004)
1027	R.S. Patti, "Three-Dimensional Integrated Circuits and the Future of the System-on-Chip Designs." <i>Proceedings of the IEEE</i> , vol. 94, no. 6, pp. 1214-1224, 2006 ("Patti")
1028	U.S. Patent Pub. 2003/0038336 ("Mann")
1029	U.S. Patent Application Publication No. US 2005/0161795 A1 ("Tong")
1030	U.S. Patent No. 7,750,488 ("Patti488")
1031	U.S. Patent Application Publication No. US 2006/0043438 A1 ("Holm")
1032	PCT Application Pub. No. WO 2006/129762 A1 ("Iwabuchi-762")
1033	Pages from C.Y. Chang and S.M. Sze, <i>ULSI Technology</i> . The McGraw-Hill Companies, Inc., 1996. ("ULSI")
1034	Pages from The American Heritage Dictionary of the English Language, Houghton Mifflin Company (4th ed. 2000).
1035	IPC-7351: Generic Requirements for Surface Mount Design and Land Pattern Standard (2005)
1036	INTERPOSER-TECH07: Lead-free to Tin/Lead BGA Interposer (Advanced Interconnections 2007)
1037	Pages from S.M. Sze, <i>Physics of Semiconductor Devices</i> (2d ed. 1981) ("Sze-1981")
1038	Affidavit of Nathaniel E. Frank-White ("Frank-White Affidavit")
1039	RESERVED
1040	A. El Gamal and H. Eltoukhy, H., "CMOS image sensors," <i>IEEE Circuits and Devices Magazine</i> , 21(3), pp.6-20 (2005) ("Gamal").
1041	Declaration of Gordon Macpherson with Exhibit A, R.S. Patti, "Three-Dimensional Integrated Circuits and the Future of the System-on-Chip

Exhibit	Description
	Designs.” Proceedings of the IEEE, vol. 94, no. 6, pp. 1214-1224, 2006
1042	S. Tiwari et al., “Lateral p-i-n photodetectors with 18 GHz bandwidth at 1.3 μm wavelength and small bias voltages,” <i>International Electron Devices Meeting 1991</i> [Technical Digest], 1991, pp. 421-424 (“Tiwari”)
1043	U.S. Patent No. 6,984,816 B2 (“Holm-816”)
1044	Pages from S.M. Sze, <i>Semiconductor Devices: Physics and Technology</i> , John M. Wiley & Sons (2d ed. 2002) (“Sze-2002”).
1045	Mike Salib et. al, “Silicon Photonics,” <i>Intel Technology Journal</i> , volume 8, no. 2, pp. 143-160, 2004
1046	P. Lindner et al., “3D Interconnect through Aligned Wafer Level Bonding,” in <i>52nd Electronic Components and Technology Conference 2002</i> (Cat. No. 02CH37345), pp. 1439-1443 (May 28, 2002) (“Lindner”)
1047	K. Keswick, R. L. German, M. Breen and R. Nolan, “Compliant bumps for adhesive flip-chip assembly,” <i>IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B</i> , vol. 18, no. 3, pp. 503-510, Aug. 1995 (“Keswick”)
1048	J. H. Wu et al., “A high aspect-ratio silicon substrate-via technology and applications: through-wafer interconnects for power and ground and Faraday cages for SOC isolation,” <i>International Electron Devices Meeting 2000. Technical Digest. IEDM</i> (Cat. No.00CH37138), 2000, pp. 477-480 (“Wu”)

APPENDIX B: U.S. PATENT NO. 7,867,808 CLAIM LIST

Ref Claim

1.p	A method, comprising:
1.a	providing a first substrate;
1.b	forming circuitry including a metal interconnection over the first substrate;
1.c	forming a photodiode in a crystalline semiconductor layer of a second substrate;
1.d	forming an ion implantation isolation layer in the photodiode;
1.e	bonding the first substrate to the second substrate to connect the photodiode to the metal interconnection; and
1.f	removing a lower portion of the second substrate to expose the photodiode,
1.g	wherein forming the photodiode comprises:
1.g.1	forming a second conduction type conduction layer in the crystalline semiconductor layer; and
1.g.2	forming a first conduction type conduction layer over the second conduction type conduction layer,
1.h.1	wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer over the first conduction type conduction layer,
1.h.2	wherein forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.
2	The method of claim 1, comprising forming the second conduction type conduction layer at a junction depth of less than approximately 0.5 μm .
3	The method of claim 1, comprising forming the first conduction type conduction layer at a junction depth ranging from approximately 1.0 μm to 2.0 μm .
4	The method of claim 1, comprising forming the ion implantation isolation layer over at least one of a side of the photodiode and a bottom of the photodiode.
5	The method of claim 1, wherein the ion implantation isolation layer comprises a P0 layer.
6.a	The method of claim 1, comprising: forming a dielectric over the photodiode of the second substrate before bonding the first and second substrates; and
6.b	forming a metal pad in the dielectric.

Ref Claim

7	The method of claim 1, wherein bonding the first substrate to the second substrate comprises contacting the first substrate and the second substrate with each other and performing activation by plasma.
8	The method of claim 1, wherein forming the circuitry including the metal interconnection comprises forming a metal and a plug over the first substrate.
9	The method of claim 1, wherein the second conduction type second ion implantation isolation layer is disposed to directly contact on a top surface of the second conduction type first ion implantation isolation layer and a bottom surface of the second conduction type conduction layer.