

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY GROUP CORPORATION,
Petitioner

v.

VISIONX TECHNOLOGIES, LLC,
Patent Owner

IPR2023-00296
U.S. Patent No. 7,867,808

**PATENT OWNER'S PRELIMINARY RESPONSE
TO PETITION FOR *INTER PARTES* REVIEW
*37 C.F.R. §42.107***

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PATENT OWNER'S CURRENT EXHIBIT LIST¹

Exhibit	Brief Description
2001	Consent to Proceed Before Magistrate Judge Payne
2002	Amended Docket Control Order
2003	VisionX Notice of Compliance re Infringement Contentions
2004	Sony's Notice of Compliance re Invalidity Contentions
2005	Sony's Invalidity Contentions and ID of Doc Production
2006	U.S. Dist. Courts—National Judicial Caseload Profile

¹ Relevant portions of exhibits may be highlighted to help the Board locate cited sections.

I. INTRODUCTION

A. THE '808 PATENT

The '808 patent (Ex. 1001, U.S. Patent No. 7,867,808) is directed to a method for manufacturing an image sensor. '808 patent, Abstract, 2:22-24. The method comprises providing a first substrate (100) and forming circuitry including a metal interconnection, which may include a metal (110) and/or a plug (120), over the first substrate. *Id.*, Figs. 7-8, 2:26-29, 4:25-27, 4:29-30. The method also comprises forming a photodiode (210) in a crystalline semiconductor layer of a second substrate (200). *Id.*, Fig. 2, 2:29-30, 3:5-7, 3:19-21. Forming the photodiode comprises forming a first conduction type conduction layer (214) and a second conduction type conduction layer (212) in the crystalline semiconductor layer. *Id.*, Fig. 2, 2:34-38, 3:21-43. An ion implantation isolation layer (220) is formed in the photodiode. *Id.*, Fig. 3, 2:32-33, 2:55-59. Forming the ion implantation isolation layer in the photodiode comprises forming a second conduction type first ion implantation isolation layer (220a) over the first conduction type conduction layer, and forming a second conduction type second ion implantation isolation layer (220b) at an interface between pixels of the photodiode. *Id.*, Fig. 3, 2:52-55, 3:44-61. The first substrate is bonded to the

second substrate to connect the photodiode to the metal interconnection. *Id.*, Fig. 7, 2:29-32, 4:27-29, 4:31-35. Thereafter, a lower portion of the second substrate is removed to expose the photodiode. *Id.*, Fig. 8, 4:41-50.

B. CLAIM INTERPRETATION

1. STEPS [1.g.1] AND [1.g.2]

Petitioner has proposed an interpretation of claim steps² [1.g.1] and [1.g.2] to mean that “the second conduction layer ... ***must already be in place*** in order to form the first conduction layer ‘***over***’ it” Pet. 9 (emphasis in original). The claim language that Petitioner wants interpreted is not at issue in the present proceeding. Petitioner has not stated, in any of its arguments related to art references relied upon, how or why its proposed interpretation would affect the outcome of the present proceeding. The Board “need only construe terms ‘that are in controversy ...’.” *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Therefore, Patent Owner takes no position

² For ease of reference, Patent Owner refers to claim clauses and the acts recited therein in the same style as the Petition. That is, “step [1.a]” through “step [1.h.2]” refer to the corresponding claim clauses recited in the Petition.

on this particular claim interpretation requested in the Petition, and merely notes that claim interpretation of steps [1.g.1] and [1.g.2] is unnecessary at this juncture.³

2. STEPS [1.e] AND [1.f]

“[A] claim ‘requires an ordering of steps when *the claim language*, as a matter of logic or grammar, requires that the steps be performed in the order written, *or the specification directly or implicitly requires’ an order of steps.*” *Mformation Techs., Inc. v. Research in Motion Ltd.*, 764 F.3d 1392, 1398 (Fed. Cir. 2014) (citations omitted).⁴

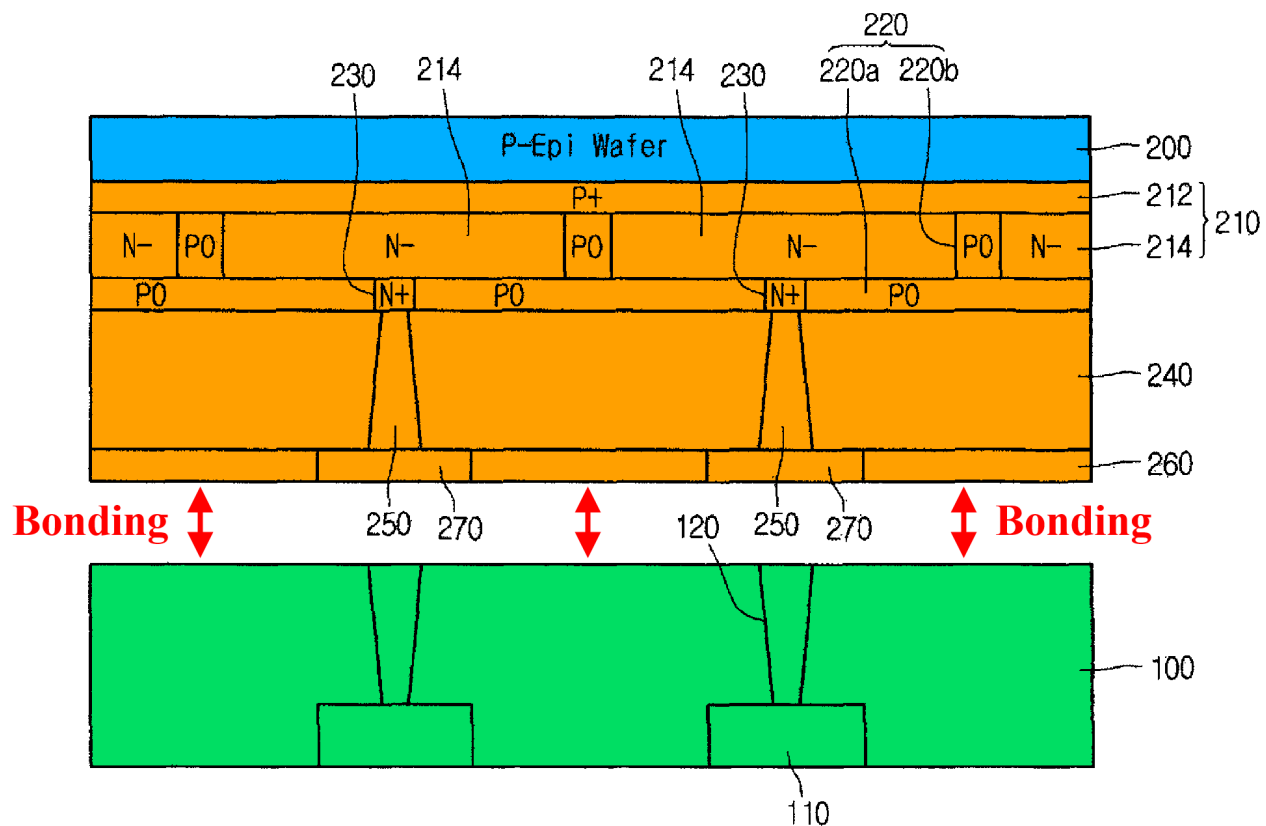
In the lone embodiment of the ‘808 patent, the detailed description, drawings, and claim 1 of the ‘808 patent make it amply clear that step [1.f] (that is “*removing* a lower portion of the second substrate to expose the photodiode”) must occur after step [1.e] (that is “*bonding the first substrate to the second substrate to connect* the photodiode to the metal interconnection”).

³ Patent Owner does not waive any arguments necessary for interpretation of claims, including claim steps [1.g.1] and [1.g.2], in any proceeding.

⁴ Emphasis is added throughout unless otherwise noted.

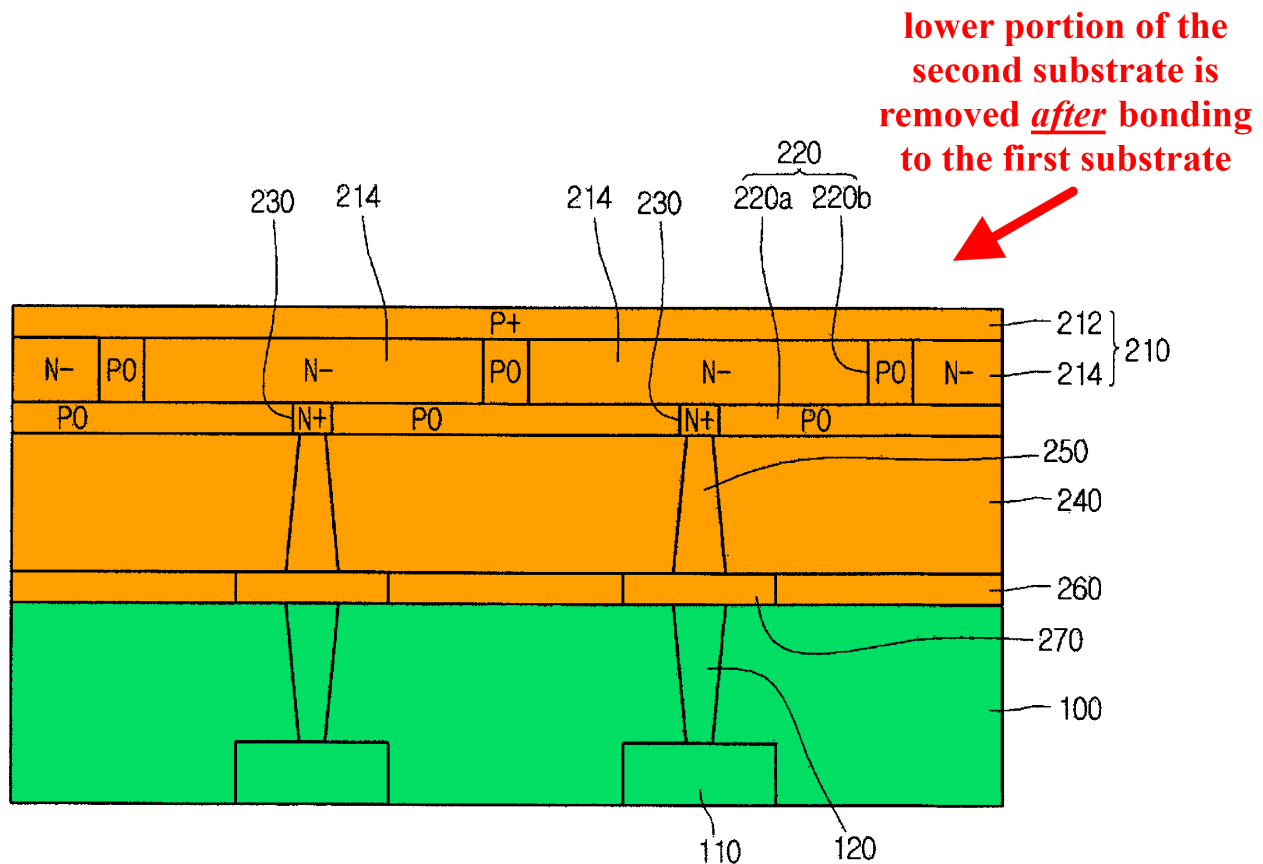
Claim 1 recites step [1.f] after step [1.e]. The claim language and logic indicates that for the portion of the second substrate to be removed in step [1.f], the second substrate would first need to be bonded to the first substrate in step [1.e] otherwise it would not be present for removal in step [1.f]. That is, if hypothetically, the order of steps [1.e] and [1.f] were reversed, the bonding action would be between the first substrate and a *remaining portion* of the second substrate. However, step [1.e] recites “the second substrate” and not a “remaining portion of the second substrate.”

Moreover, Figures 7 and 8 and the corresponding detailed description clearly require that step [1.f] must occur after step [1.e]. The annotated Figure 7 below illustrates that, according to step [1.e], first substrate 100 is bonded to second substrate 200. The bonding action is described in relation to Figure 7. *See, e.g.*, ‘808 patent, 4:25-31.



'808 Patent Fig. 7

The '808 patent then transitions to a description of Figure 8 which illustrates removal of the "lower portion of the second substrate" as claimed in step [1.f]. *Id.*, 4:36-50. It is clear from the annotated Figure 8 below that the "P-Epi Wafer" in substrate 200 (blue in Figure 7 above) *is removed after the bonding action* in Figure 7.



‘808 Patent Fig. 8

Moreover, referring to Figure 8 that shows the bonded structure after Figure 7, the ‘808 patent specifies that “*a portion of second substrate 200 may then be removed*” (*id.*, 4:41-42), that is after completing the bonding action in Figure 7. The ‘808 patent further specifies that “P-Epitaxial layer, which may be at *an upper portion of second substrate 200, may be removed ... after bonding the first and second substrates.*” *Id.*, 4:47-50.

Petitioner has also understood claim 1 to require step [1.f] to occur after step [1.e]. *See, e.g.* Pet. 4 (“Claim 1 recites forming metal interconnections on a first substrate, forming a photodiode in a second substrate, and ***bonding the two together. Removing material from the second substrate’s backside*** exposes the photodiode ...”). Petitioner has not contended (as it cannot) that step [1.f] occurs prior to step [1.e]. Thus, it is not disputed (and it cannot be disputed) that step [1.f] occurs after step [1.e].

II. GROUNDS 1A, 1B, AND 1C FAIL TO DISCLOSE OR MAKE OBVIOUS ALL STEPS OF CLAIM 1

Under Grounds 1A, 1B, and 1C, Iwabuchi (Ex. 1005) is the only art reference relied upon as rendering claim 1 obvious. As discussed below, Iwabuchi fails to disclose or make obvious at least claim step [1.e].⁵

A. IWABUCHI DOES NOT RENDER CLAIM 1 OBVIOUS

With respect to Iwabuchi, the Petition is utterly confusing and misleadingly flip-flops between three different interpretations of what constitutes a “first

⁵ The fact that a claim clause, or “step,” or element is not discussed in this Preliminary Response does not indicate that Patent Owner agrees that the claim clause, step, or element is disclosed or made obvious as argued in the Petition.

substrate.” The first interpretation is “interposer 3” (Pet. 11), the second is “supporting substrate 30” (Pet. 12), and the third is “the DSP chip” (i.e. signal processing chip 2) (Pet. 13). These three different “first substrates” are shown together in Figure 7 of Iwabuchi. Supporting substrate 30 (second interpretation for the “first substrate”) is shown as part of sensor chip 1a, which is mounted on interposer 3 (first interpretation for the “first substrate”). Iwabuchi, Fig. 7. Signal processing chip 2 (third interpretation for the “first substrate”) is also mounted on interposer 3 next to sensor chip 1a. *Id.*

As discussed below, one or more steps in method claim 1 are not met using any one of the three interpretations of the “first substrate.”

1. STEPS [1.e] AND [1.f] ARE NOT DISCLOSED OR MADE OBVIOUS BY IWABUCHI SINCE NEITHER “INTERPOSER 3” NOR “SIGNAL PROCESSING CHIP 2” CAN BE THE PURPORTED “FIRST SUBSTRATE”

The Petition must establish that, according to Iwabuchi’s disclosure, step [1.f] occurs *after* step [1.e]. As noted above, the Petition has stated that either interposer 3 or signal processing chip 2 can be the “first substrate.” Pet. 11-13. According to the Petition, the “second substrate” is “Iwabuchi’s SOI wafer including semiconductor layer 12” (Pet. 23), and resides in sensor chip 1a (Iwabuchi, Fig. 7).

Therefore, the removing of a lower portion of “Iwabuchi’s SOI wafer” must occur after it is “bonded” to the first substrate, i.e. after sensor chip 1a (which houses “Iwabuchi’s SOI wafer”) is “bonded” to the “first substrate” (interposer 3 or signal processing chip 2). However, in discussing step [1.f] on pages 50-52 of the Petition, Petitioner has in effect acknowledged that neither interposer 3 nor signal processing chip 2 can be considered the “first substrate.”

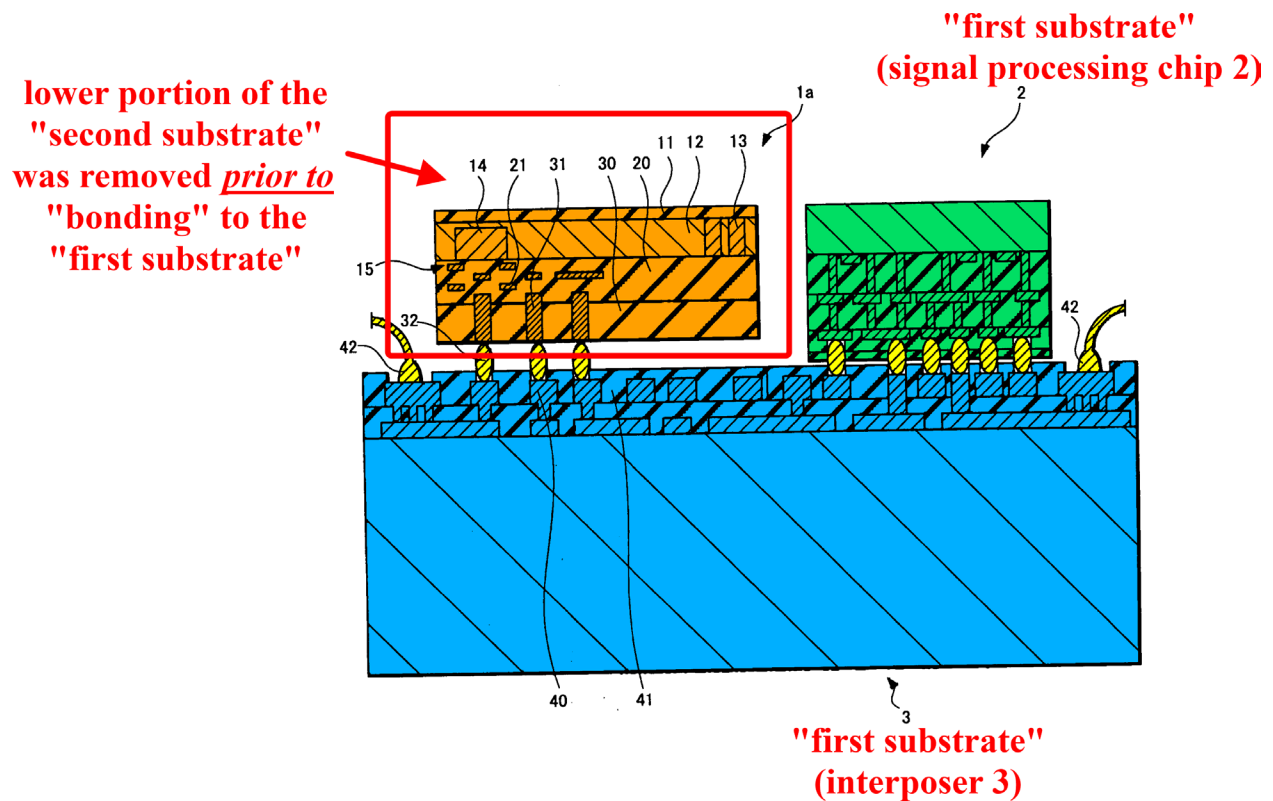
In discussing step [1.f], *the only alternative “first substrate” that is shown to accompany the second substrate is supporting substrate 30 in Figure 10G.* Pet. 50-52. By *using supporting substrate 30 as the only alternative “first substrate”* to meet step [1.f], Petitioner has been compelled to make the assumption (without explicitly disclosing the assumption) that the previous action, i.e. step [1.e] (that is “*bonding the first substrate* to the second substrate ...”) was also required to use *only supporting substrate 30* as the “first substrate” and could not have used either interposer 3 or signal processing chip 2 as the “first substrate.”

The reason Petitioner does not argue that either interposer 3 or signal processing chip 2 is an alternative “first substrate” to meet step [1.f] is clear. No argument can be made that a portion of the “second substrate,” that is a portion of “Iwabuchi’s SOI wafer” residing in sensor chip 1a, is removed *after* “bonding” the

“second substrate” to interposer 3 or to signal processing chip 2. Although this argument is necessary to make in order to meet steps [1.e] and [1.f], Petitioner has not made such an argument anywhere in the Petition, as it cannot.

The Petition has stated that “[s]*ubstrate 10* is a lower portion of the second substrate” that is removed to meet step [1.f] (that is “*removing* a lower portion of the second substrate to expose the photodiode”). Pet. 50-51. It is clear that substrate 10 is removed *before* sensor chip 1a is completed, *and before* sensor chip 1a is mounted (“bonded”) on interposer 3 in Figure 7. *See, e.g.,* Iwabuchi [0150]-[0151], [0153]. Iwabuchi clearly explains that sensor chip 1a is completed, and specifically the removing of substrate 10 shown in Figure 10G of Iwabuchi is completed, *prior to* mounting (“bonding”) of sensor chip 1a on interposer 3 and *prior to* any connection to interposer 3 or to signal processing chip 2. *See, e.g.,* Iwabuchi [0150]-[0151], [0153]-[0154].

Annotated Figure 7 of Iwabuchi (below) illustrates that *the “lower portion of the second substrate” (substrate 10 in Iwabuchi) has been removed prior to* “bonding” sensor chip 1a to “first substrate” interposer 3 or “first substrate” signal processing chip 2. No second substrate removal operation occurs after “bonding” sensor chip 1a to interposer 3 or signal processing chip 2.



Iwabuchi Fig. 7

According to the Petition, Iwabuchi's process to decrease the thickness of semiconductor substrate 10 is "*just like the '808 patent,*" and "[t]his meets [1.f]."

Pet. 51. However, as discussed above, the thickness reduction process in Iwabuchi that purportedly "meets [1.f]" is performed *before "bonding"* sensor chip 1a to either interposer 3 or signal processing chip 2. In stark contrast, step [1.f] in the '808 patent is clearly disclosed and claimed to occur *after the bonding* process, i.e. after step [1.e].

Thus, Petitioner could not (and did not) present interposer 3 or signal processing chip 2 in its discussion of step [1.f]. It follows that even in the prior step, i.e. in step [1.e], interposer 3 or signal processing chip 2 could not have been the “first substrate.” Relying on interposer 3 or signal processing chip 2 as the “first substrate” would require a reversal of the temporal order of steps [1.e] and [1.f], which would be quite contrary to the method disclosed and claimed in the ‘808 patent.

Therefore, the only alternative that could possibly be a plausible candidate for the “first substrate” would be “supporting substrate 30.” As such, *the only alternative for the “first substrate” that should have been proposed in the Petition from the beginning is supporting substrate 30.* However, in a vexing attempt to overcome the shortcomings of using only supporting substrate 30 as “the first substrate,” Petitioner has contrived the other two alternatives for the first substrate (i.e. interposer 3 and signal processing chip 2). These other two alternatives for the “first substrate” have been in effect abandoned by Petitioner in its analysis of step [1.f]. In any event, Petitioner’s reliance on these two alternatives as the “first substrate,” clearly results in failure of Iwabuchi to disclose or suggest steps [1.e] and [1.f].

**2. STEP [1.e] IS NOT DISCLOSED OR MADE OBVIOUS
BY IWABUCHI WHEN USING SUPPORTING
SUBSTRATE 30 AS THE “FIRST SUBSTRATE”**

In relation to step [1.e] (that is “***bonding*** the first substrate to the second substrate ***to connect the photodiode to the metal interconnection***”), Petitioner has made several vague and contradictory statements as to what constitutes the “second substrate” in Iwabuchi. Initially, the Petition states: “***Semiconductor layer 12 ... is used as an SOI (silicon on insulator) substrate.***” Pet. 23 (referring to Figs. 10A-10B of Iwabuchi) (underlined emphasis in original). Then the Petition defines the “second substrate” to be “Iwabuchi’s ***SOI wafer including semiconductor layer 12.***” *Id.* When substituting “semiconductor layer 12” with “SOI substrate,” the result is the perplexing statement that the “second substrate” is ***Iwabuchi’s SOI wafer including SOI substrate.*** The Petition has never defined what it deems to be “Iwabuchi’s SOI wafer,” and the term “SOI wafer” is never used in Iwabuchi. The Petition has never defined the distinction or similarity between Iwabuchi’s SOI wafer and Iwabuchi’s SOI substrate.

Petitioner has introduced an additional layer of confusion. On page 23 of the Petition, Figure 10A illustrates three layers (semiconductor substrate 10, insulating film 11, and semiconductor layer 12), while Figure 10B illustrates four

layers (semiconductor substrate 10, insulating film 11, semiconductor layer 12, and interlayer insulator 20).⁶ Although the Petition has referred to and shown both Figures 10A and 10B of Iwabuchi in relation to its definition of the “second substrate,” it has not stated whether it considers the “second substrate” to include three layers (Figure 10A) or four layers (Figure 10B).

The Petition has introduced more bewilderment by later referring to “Iwabuchi’s *SOI substrate 10* ...” (Pet. 28), which runs counter to Petition’s earlier definition, that is: “*Semiconductor layer 12 ... is used as an SOI (silicon on insulator) substrate.*” Pet. 23. The confusion is again exacerbated by the statement that “the photodiode 14 becomes able to receive light from the side of the *semiconductor substrate 10 of the SOI substrate*” Pet. 51. While the Petition had earlier referred to “SOI substrate 10,” it is later indicating that the SOI substrate includes more than substrate 10 (“semiconductor substrate 10 *of the SOI substrate*” Pet. 51).

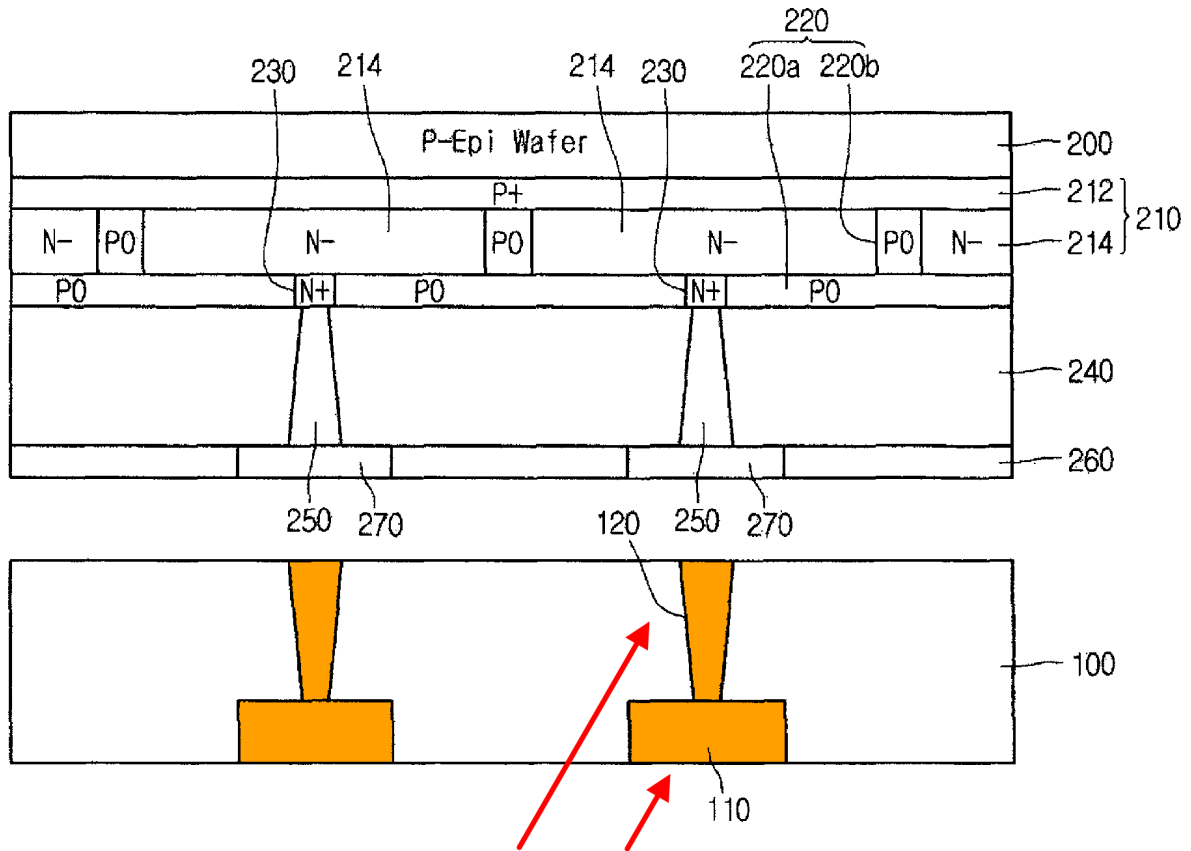
⁶ Numerals 10, 11, and 12 are missing from the Petition’s reproduction of Figure 10B, but they appear in Iwabuchi.

Regardless of Petitioner's conflicting definitions of what constitutes the "second substrate," using supporting substrate 30 as the "first substrate" results in Iwabuchi's failure to meet [1.e]. Step [1.e] requires "***bonding*** the first substrate to the second substrate ***to connect the photodiode to the metal interconnection.***"

The '808 patent states that "[a] ***metal interconnection*** of first substrate 100 may include metal 110 and plug 120." '808 patent, 4:29-30. Figure 7 of the '808 patent shows substrate 100 with its metal interconnection (e.g., metal 110 and plug 120). Iwabuchi does not disclose connecting its photodiode 14 to a metal interconnection of supporting substrate 30 ("the first substrate") when supporting substrate 30 is bonded to Iwabuchi's "second substrate."

The ordinary and customary meaning of "bonding ... to connect" is that when bonding is performed a connection is made. Further, the specification of the '808 patent is consistent with and expressly supports this ordinary and customary meaning. Annotated Figure 7 (below) of the '808 patent illustrates that when first substrate 100 is bonded to second substrate 200, metal 110 and plug 120 are already present in substrate 100. As such, photodiode 210 is connected to the metal interconnection (e.g., metal 110 and/or plug 120) of substrate 100 at the time of bonding the first and second substrates.

‘808 Patent Fig. 7



Metal 110 and Plug 120 Are Present When Bonding the First and Second Substrates

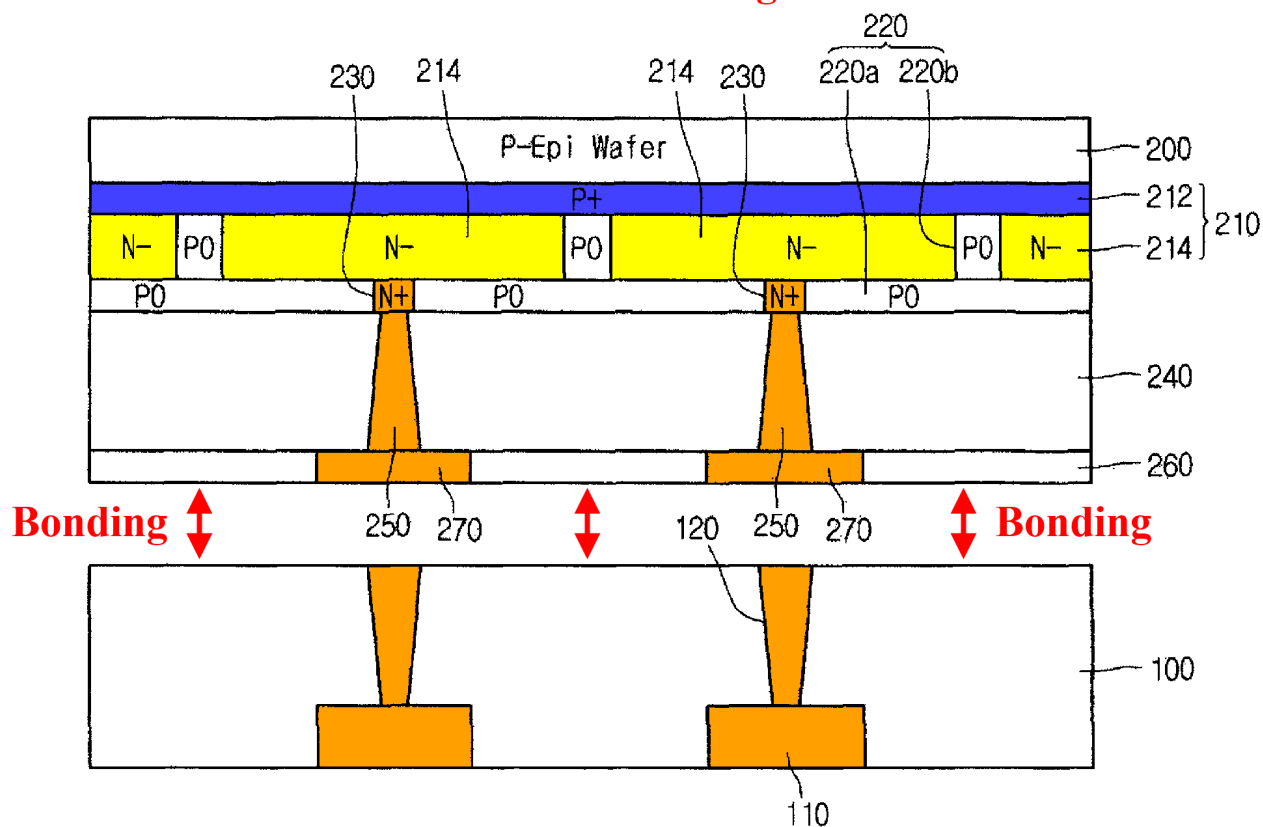
There is no additional or different process or step disclosed in the ‘808 patent for connecting photodiode 210 to the metal interconnection (e.g., metal 110 and/or plug 120) of substrate 100. Prior to discussing Figure 7, the ‘808 patent states that the disclosed image sensor includes: “A first substrate on and/or over which circuitry including a metal interconnection may be formed. A photodiode in a crystalline semiconductor layer *bonded to the first substrate*, where the

photodiode may be electrically *connected to the metal interconnection.*” ‘808 patent, 1:64 to 2:1. The ‘808 patent further discloses: “**Bonding** the first and second substrates to each other, which may *connect the photodiode* to the metal interconnection.” *Id.*, 2:8-10.

Thereafter, when discussing Figure 7, the ‘808 patent states: “[F]irst substrate 100 may be *bonded to second substrate 200* through a wafer-level bonding. A *metal interconnection of first substrate 100* may include metal 110 and plug 120 ... *bonding may be performed by contacting first substrate 100 and second substrate 200* with each other” *Id.*, 4:27-33, Fig. 7.

Therefore, as shown in Figure 7 and described in the detailed description of the ‘808 patent, *photodiode 210 of second substrate 200 connects with the metal interconnection (e.g., metal 110 and/or plug 120) of first substrate 100 when bonding first substrate 100 to second substrate 200.* Figure 7 of the ‘808 patent annotated below shows photodiode 210 being connected to metal interconnection (e.g., metal 110 and/or plug 120) of first substrate 100 through metal pad 270, metal plug 250, and N+ layer 230.

Bonding to Connect Photodiode 210 to Metal 110 and/or Plug 120



‘808 Patent Fig. 7

In plain contrast, photodiode 14 of Iwabuchi’s “second substrate” *does not connect* with any metal interconnection of supporting substrate 30 (the “first substrate”) when bonding supporting substrate 30 to Iwabuchi’s “second substrate.” As such, Iwabuchi does not disclose or suggest “*bonding* the first substrate to the second substrate *to connect the photodiode to the metal interconnection*” when the “first substrate” is Iwabuchi’s supporting substrate 30.

The Petition has skipped directly addressing how step [1.e] is met when the “first substrate” is supporting substrate 30. Pet. 41-43. Instead of referring to a structure drawing in Iwabuchi to discuss “bonding the first substrate to the second substrate,” Petitioner has referred to a largely irrelevant circuit diagram, that is Figure 9 of Iwabuchi, and has provided the following cryptic and incorrect statement as to how step [1.e] is met when supporting substrate 30 is the “first substrate”: “[W]hen **bonding the first and second substrates**, line 260 is ‘electrically connected’ (IC-A1, 17) to the CDS circuit on the DSP chip through metal interconnections on the supporting substrate 30, metal interconnections on the DSP chip, and - when used - metal interconnections on the interposer.” Pet. 43.

To the extent that the above explanation can be understood, it is incorrect. It is also the only explanation in the Petition as to how bonding supporting substrate 30 with the “second substrate” **connects** photodiode 14 with a metal interconnection of supporting substrate 30. As understood by Petitioner, “**bonding the first substrate to the second substrate to connect the photodiode to the metal interconnection**” refers to connecting the photodiode to the metal interconnection **when the bonding action takes place**. Petitioner has itself acknowledged this fact by stating: “[W]hen **bonding the first and second substrates**, line 260 is

‘electrically connected’ ... to the CDS circuit” *Id.* In other words, Petitioner has not argued, as it cannot, that a connection of the photodiode with the metal interconnection of the first substrate that occurs not at the time of bonding, but in a later step *after* the bonding step, meets step [1.e]. The Petition has acknowledged that to meet step [1.e], the connection needs to occur “*when bonding* the first and second substrates.” Pet. 43.

However, in meeting the requirement for the connection to occur “*when bonding* the first and second substrates” (*id.*), the Petition has misleadingly directed attention to the “bonding” of sensor chip 1a (which houses the purported “second substrate”) with interposer 3 and signal processing chip 2, that is the other two alternatives of the “first substrate,” *instead of supporting substrate 30*. The Petition has omitted to state that supporting substrate 30 had been already bonded to the “second substrate” *several process steps before* mounting (“bonding”) sensor chip 1a on interposer 3.

In Iwabuchi, sensor chip 1a is completed after conclusion of all process steps in Figure 10G (Iwabuchi, [0150]-[0151]), and thereafter sensor chip 1a is mounted on interposer 3 (Iwabuchi, [0153]). Both the completion of sensor chip 1a and its

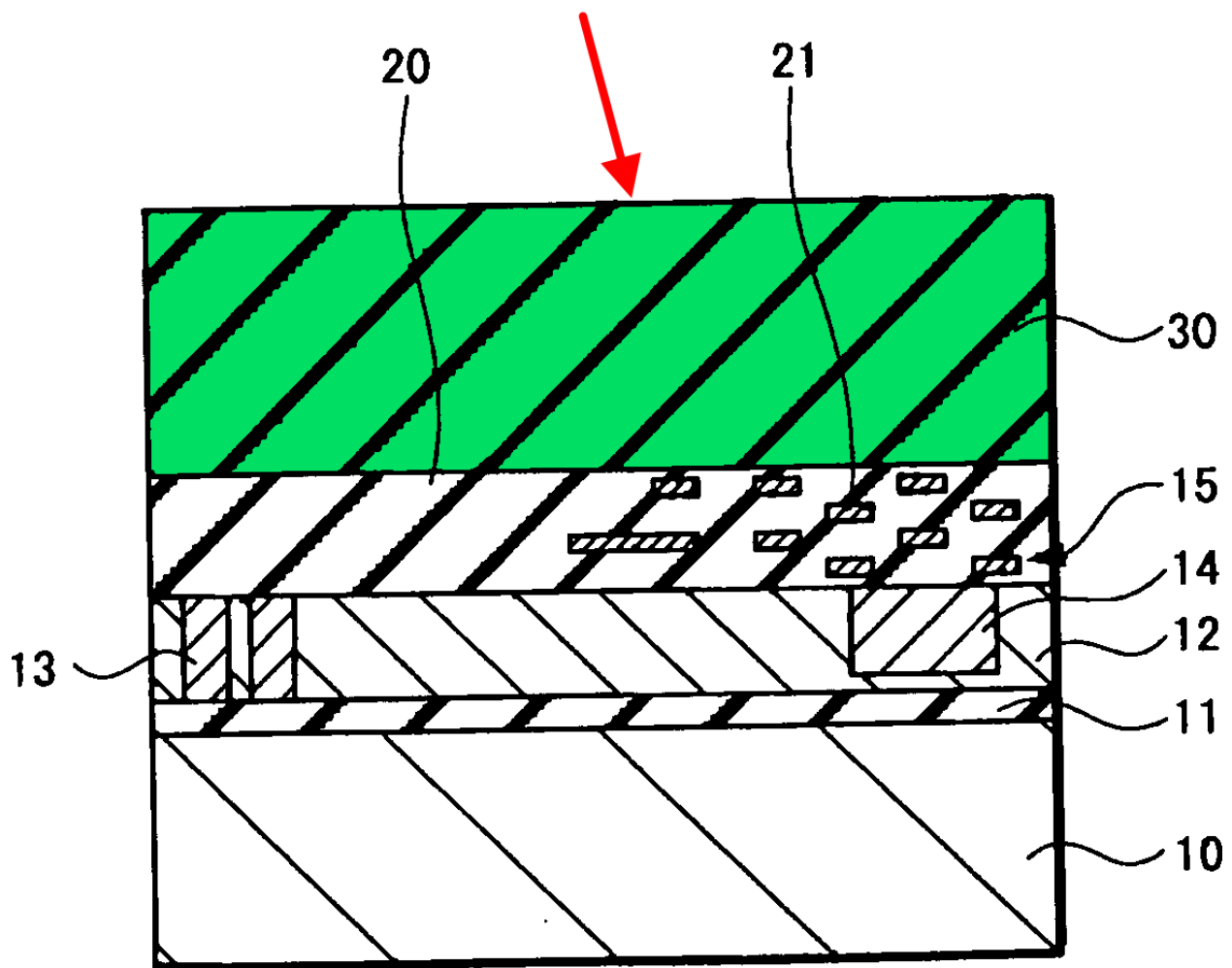
mounting on interposer 3 are *several process steps after* bonding Iwabuchi's "second substrate" with supporting substrate 30 in Figure 10C (Iwabuchi, [0146]).

Petitioner's statement that "when bonding the first and second substrates, line 260 is 'electrically connected' (IC-A1, 17) to the CDS circuit on the DSP chip through metal interconnections on the supporting substrate 30, metal interconnections on the DSP chip, and - when used - metal interconnections on the interposer" (Pet. 43), is apparently intended to convey that "metal interconnections on the supporting substrate 30" are somehow used to make a connection to the photodiode in the second substrate at the time of bonding, and somehow line 260 is involved in such a connection. However, supporting substrate 30 *has no metal interconnections* at the time of bonding with the second substrate and, further, line 260 is not part of supporting substrate 30.⁷ Petitioner's statement above is quite vague, confusing and misleading – and it is the sole statement in the Petition as to how Iwabuchi meets step [1.e] when the first substrate is supporting substrate 30.

⁷ Iwabuchi states that "vertical signal line 260" is a part of "image pickup pixel unit 112." Iwabuchi, [0130]-[0131]. Iwabuchi never mentions or suggests that "image pickup pixel unit 112" is in supporting substrate 30.

Annotated Figure 10C of Iwabuchi below illustrates that when bonding with the “second substrate,” supporting substrate 30 (“the first substrate”) (green) is a bare “silicon substrate or an insulating resin substrate” (Iwabuchi, [0146]) and does not include any wirings or “metal interconnection,” and it certainly does not include “line 260.”

Bare Silicon Substrate with No Wirings or Metal Interconnection



Iwabuchi Fig. 10C

Penetrating wirings 31 in supporting substrate 30 are not fabricated until the process step in Figure 10E (Iwabuchi, [0148]), *that is two process steps after supporting substrate 30 is bonded* to the “second substrate.” When supporting substrate 30 is bonded to the “second substrate” of Iwabuchi (Iwabuchi, Fig. 10C),

there are no penetrating wirings 31 to connect to, and certainly there is no line 260 in supporting substrate 30 to connect to. It is plain that photodiode 14 of Iwabuchi does not get connected to any metal interconnection of supporting substrate 30 when bonding supporting substrate 30 (the “first substrate”) to the “second substrate.” Thus, the Petition clearly fails to show that Iwabuchi discloses or suggests step [1.e], that is “***bonding*** the first substrate to the second substrate ***to connect the photodiode to the metal interconnection***” when supporting substrate 30 is the “first substrate.”

III. GROUNDS 2A, 2B, AND 2C FAIL TO DISCLOSE OR MAKE OBVIOUS ALL STEPS OF CLAIM 1

Under Grounds 2A, 2B, and 2C, Lee+Masagaki+Shiraiwa is relied upon as rendering claim 1 obvious. As discussed below, Lee+Masagaki+Shiraiwa fails to disclose or make obvious at least claim steps [1.h.2] and [1.f].

A. LEE DOES NOT DISCLOSE OR MAKE OBVIOUS VARIOUS STEPS, SUCH AS STEPS [1.d], [1.h.1], [1.h.2], AND [1.f]

As essentially acknowledged by Petitioner, Lee (Ex. 1008) does not provide a disclosure applicable to steps [1.d], [1.h.1], and [1.h.2]. Pet. 88-92. Petitioner relies on Masagaki (Ex.1009) for disclosing steps [1.d], [1.h.1], and [1.h.2]. *Id.*

Lee is essentially silent on formation of an “isolating layer” in a photodiode. The phrase “isolating layer” does not appear anywhere in Lee. Even similar phrases such as “insulating layer” or terms such as “isolation” or “insulation” or “insulator” do not appear anywhere in Lee. The label “isolating layer” appears only as an incomplete box in Figures 8, 10, and 11 of Lee and, as noted above, there is no discussion about the “isolating layer” at all. Therefore, as essentially acknowledged by the Petition, Lee does not provide a disclosure applicable to steps [1.d], [1.h.1], [1.h.2] in claim 1.

Moreover, with respect to step [1.f], Lee does not provide a disclosure regarding exposing a photodiode by removing a portion of a substrate. Therefore, Petitioner relies on Shiraiwa (Ex. 1010) as disclosing step [1.f]. Pet. 94.

B. MASAGAKI DOES NOT DISCLOSE OR MAKE OBVIOUS VARIOUS STEPS, SUCH AS STEPS [1.h.2] AND [1.f]

Petitioner has essentially acknowledged that Masagaki does not provide a disclosure applicable to steps [1.a], [1.b], [1.e], and [1.f]. Pet. 82-83, 92, 94. Petitioner relies on Lee for disclosing steps [1.a], [1.b], [1.e] (*id.*, 82-83, 92), and on Shiraiwa for disclosing step [1.f] (*id.*, 94).

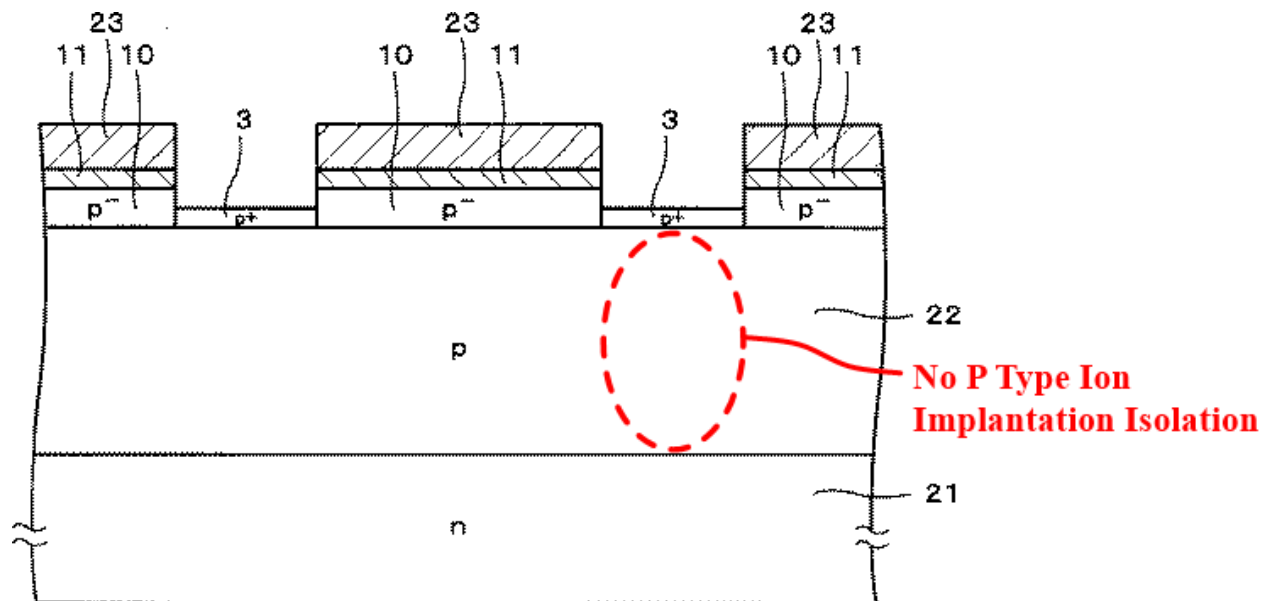
Contrary to the Petition’s arguments (*id.*, 90-92), Masagaki does not disclose or make obvious various claim 1 steps, such as step [1.h.2], that is

“wherein forming the ion implantation isolation layer in the photodiode comprises *forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.*”

In its discussion of Masagaki, the Petition has relied almost exclusively on the second embodiment of Masagaki (i.e. the second method in relation to Figures 7 through 10 (Masagaki, [0034]-[0040])). With one exception that will be addressed below, the Petition has not referred to the first embodiment of Masagaki (i.e. the first method in relation to Figures 3 through 6 (Masagaki, [0025]-[0033])). Similarly, the Petition has not proposed that Masagaki’s first embodiment can be combined with Lee and Shiraiwa. Accordingly, this Preliminary Response addresses Petition’s specific contentions with respect to the second embodiment of Masagaki, and does not address Masagaki’s first embodiment other than to respond to the only instance that Masagaki’s first embodiment has been referred to in the Petition.

Masagaki’s second embodiment begins by depositing a blanket layer of silicon nitride hard mask 23 on the underlying layers of silicon oxide film 11, P type semiconductor well region 22, and N type silicon substrate 21. Masagaki, [0035], Fig. 7A. Next, openings are created by etching to remove portions of hard

mask 23 and the underlying silicon oxide film 11. *Id.*, [0036], Fig. 7B. Then, shallow grooves are formed by etching into semiconductor well region 22 in the openings previously created, and then P type impurity is ion implanted in the shallow grooves to form high doped P⁺ type diffusion layer 3. *Id.*, [0037], Fig. 8C. ***Importantly, diffusion layer 3 is a surface diffusion layer*** that is confined to the shallow grooves on the surface of semiconductor well region 22. Regions below the high doped P⁺ type diffusion layer 3 (i.e. areas below the shallow grooves) do not undergo the P type ion implantation isolation and, unlike surface diffusion layer 3, are not designated as P⁺ regions in Masagaki. Annotated Figure 8C below illustrates the regions that do not undergo P type ion implantation isolation.

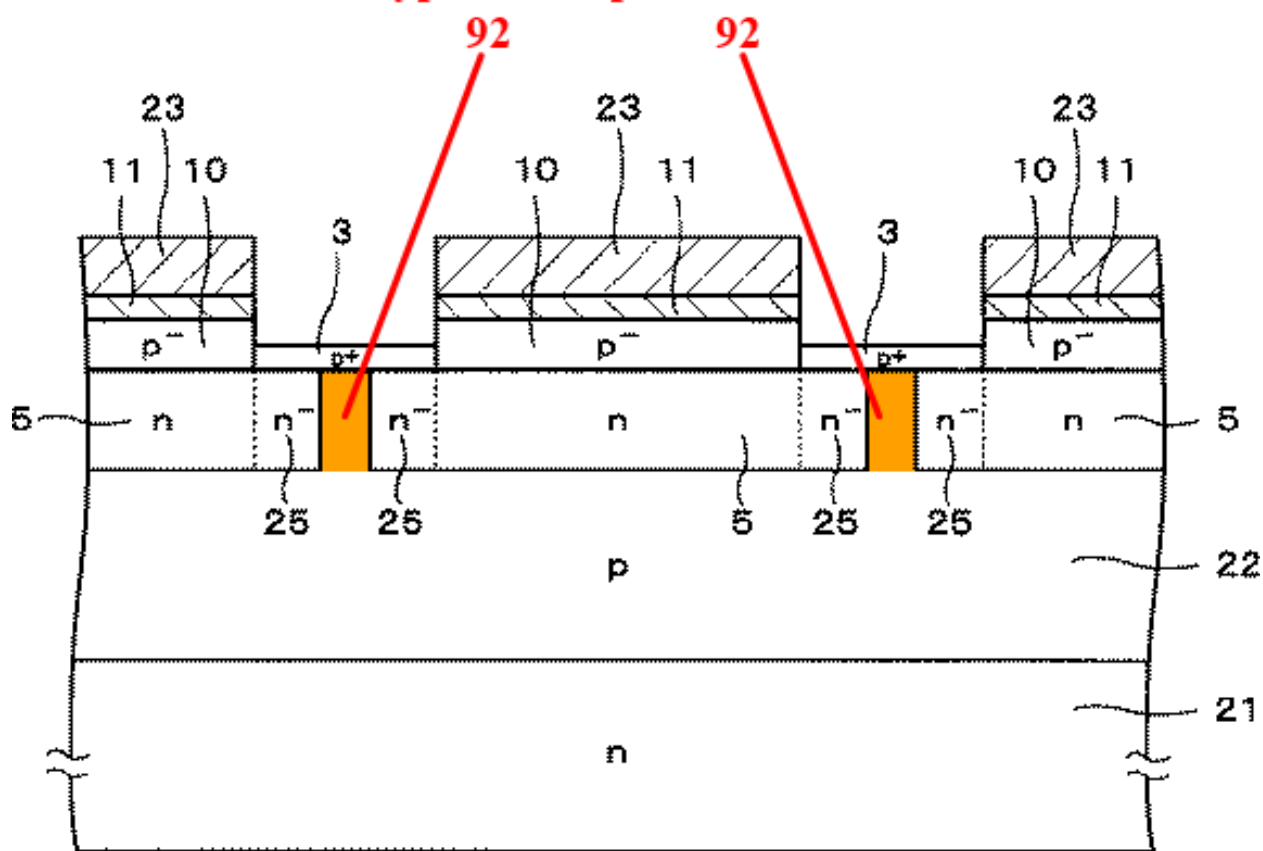


Masagaki Fig. 8C

Next, hard mask 23 is removed from everywhere and resist 24 is deposited over diffusion layer 3. *Id.*, [0038], Fig. 8D. Thereafter, N type ion implantation in areas that are not protected by resist 24 is performed to produce N type “main portions 5” in P type semiconductor well region 22. *Id.*, [0038], Fig. 9E. Some of the N type implanted ions from main portions 5 diffuse into areas that are protected by resist 24 and form low doped N⁻ type regions 25 abutting N type main portions 5. *Id.*, [0038]-[0039], Fig. 9E.

Significantly, the portions of P type semiconductor well region 22 between low doped N⁻ type regions 25 have still not received any P type ion implantation isolation, and are not designated as high doped P⁺ type, unlike the high doped P⁺ type diffusion layer 3 on the surface of semiconductor well region 22. The un-implanted portions in P type semiconductor well region 22 between low doped N⁻ type regions 25 are shaded orange in the illustration below and identified by reference numeral 92. As discussed below, portions 92 ***will never receive P type ion implantation isolation***, and the second embodiment of Masagaki is completed without ever ion implanting portions 92 with P type impurities.

No P Type Ion Implantation Isolation



Masagaki Fig. 9E

In order to complete charge storage region 7, extended portions 6 are formed by increasing the doping level of low doped N⁻ type regions 25 to be approximately the same as that of main portion 5. This is accomplished by forming resist 26 and ion implanting N type impurities into low doped N⁻ type regions 25. *Id.*, [0039], Fig. 9F.

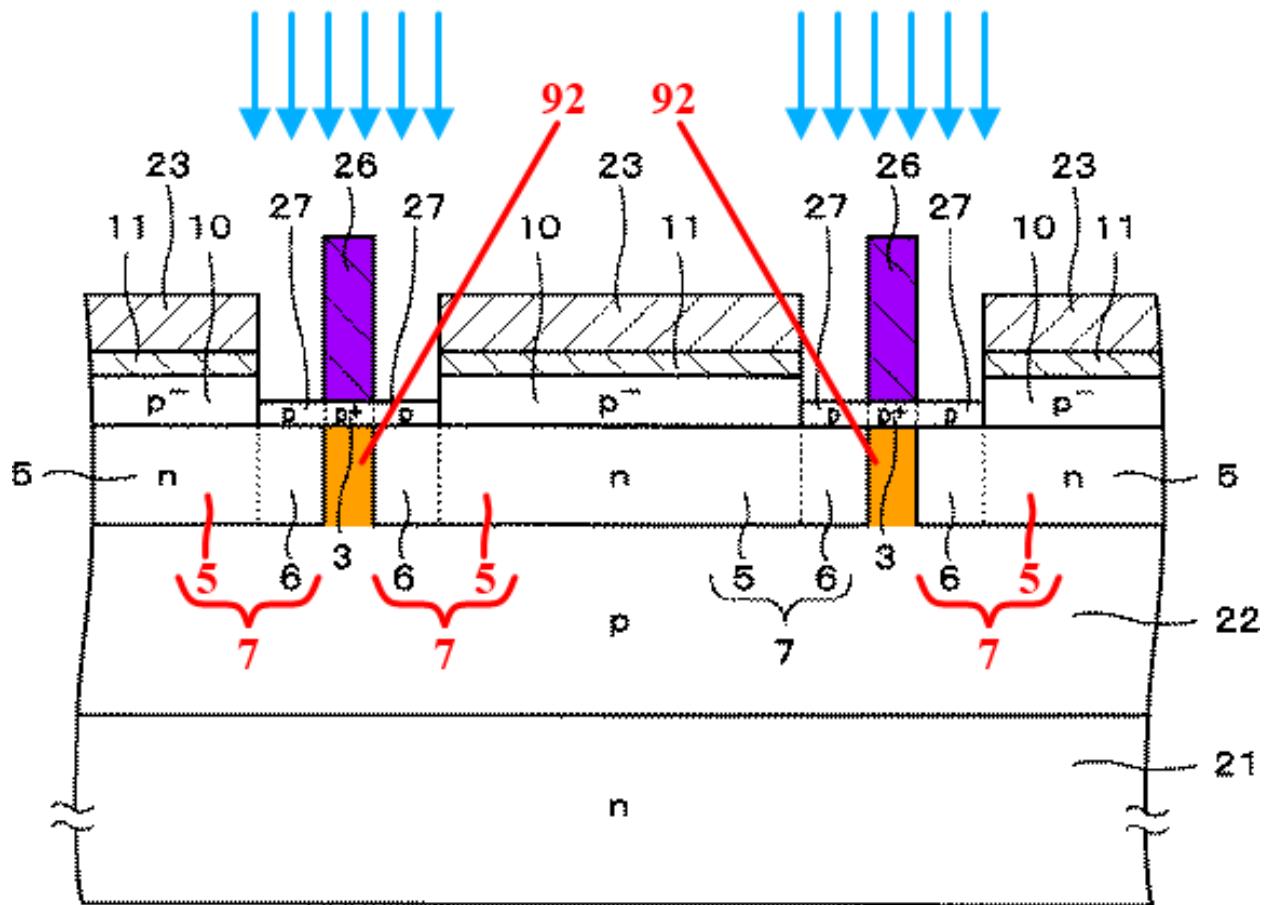
Next, resist 26 remains in place while P type impurity ions are implanted on surface portion 27 of surface diffusion layer 3 where P type doping concentration was decreased due to the N type ion implantation in the previous step. *Id.*, [0040], Fig. 9F. The result is turning surface portion 27 to extended surface diffusion layer 12 with approximately the same P type impurity concentration as surface diffusion layer 3. *Id.*, [0040], Fig. 10. Extended diffusion layer 12 is contiguous with and on both sides of surface diffusion layer 3. *Id.*, Fig. 10.

Due to the use of resist 26, semiconductor regions between extended portions 6 (that are below surface diffusion layer 3) are blocked from receiving any P type ion implantation isolation. *Id.*, Figs. 9F, 10. Moreover, extended diffusion layer 12, like diffusion layer 3, is a surface diffusion layer and does not penetrate N type extended portion 6. *Id.*, Fig. 10. As such, the contiguous diffusion layer that includes surface diffusion layer 3 and extended diffusion layer 12 is a surface diffusion layer. Therefore, due to use of resist 26, the portions of semiconductor well region 22 between N type extended portions 6 (i.e. the orange-shaded portions 92 pointed out above), ***do not receive any P type ion implantation isolation at any time.***

In other words, the portions of semiconductor region 22 between charge storage regions 7 (i.e. between photodiodes of Masagaki)⁸ ***do not receive any P type ion implantation isolation at any time.*** Moreover, any attempted P type ion implantation isolation into the portions of semiconductor region 22 between charge storage regions 7 would have worked against proper formation of the adjoining N type extended portions 6. Therefore, Masagaki’s second embodiment does not disclose or suggest P type ion implantation isolation under resist 26. Indeed, as shown in annotated Figure 9F below, ***the purpose of resist 26 (purple) is to block any P type ion implantation between charge storage regions 7 (id., Fig. 9F).***

⁸ In Masagaki, the charge storage region is frequently referred to as a “photodiode.” *See, e.g.,* Masagaki, [0004] (“a charge storage region 105 constituting a photoelectric conversion unit—that is, a photodiode”); and *id.*, [0007] (similar); and *id.*, [0019] (similar); and *id.*, [0038] (similar).

**Resist 26 Blocks Implantation into Portions 92 at the Interface
Between Adjacent Charge Storage Regions 7**



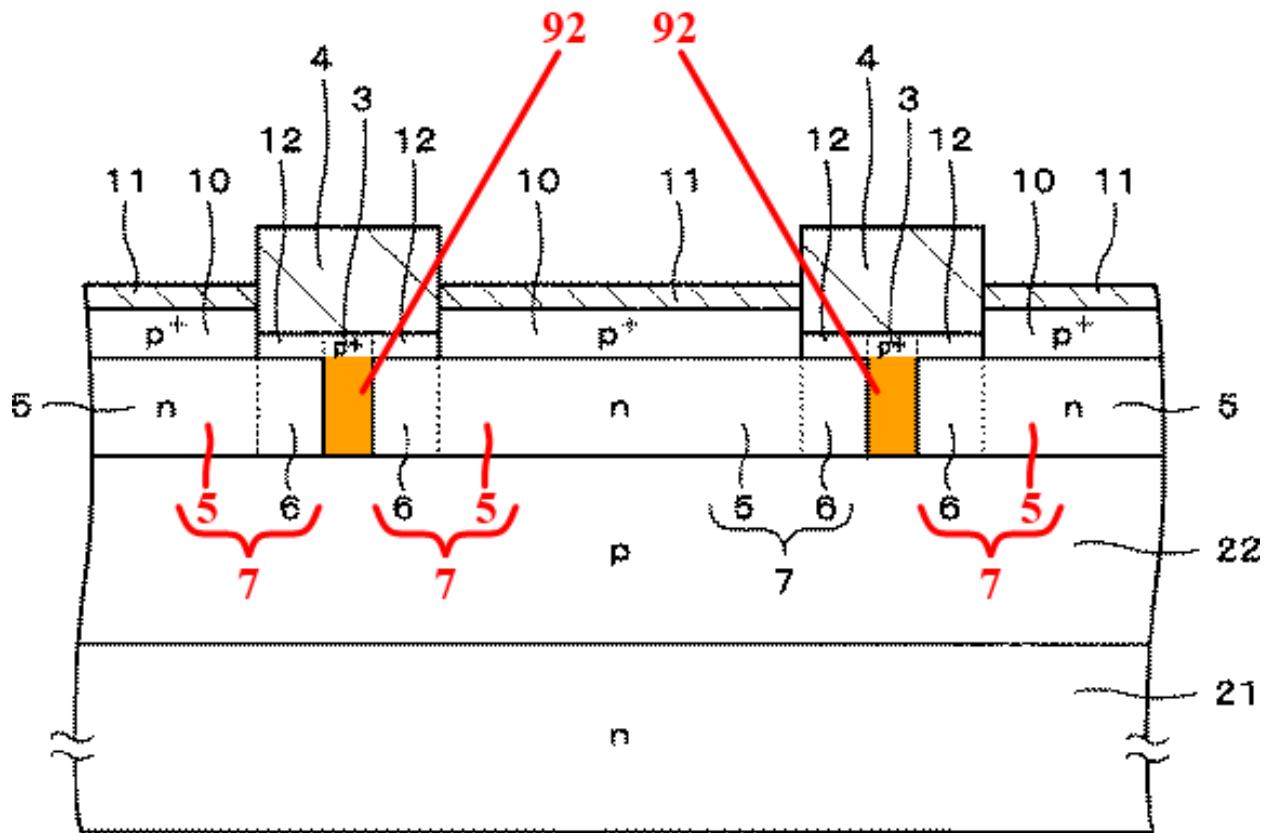
Masagaki Fig. 9F

Masagaki therefore teaches away from P type ion implantation isolation in portions 92 (shaded orange above) situated between adjacent extended portions 6, i.e. at the interface between adjacent charge storage regions 7.

The final step is to remove resist 26 and deposit insulting layer 4 over surface diffusion layer 3 and extended surface diffusion layer 12. *Id.*, [0040], Fig. 10. Insulating layer 4 is deposited in the openings of silicon nitride film 23 to have a top surface flush with the top surface of silicon nitride film 23, and thereafter silicon nitride film 23 is removed. *Id.*, Fig. 10. Thus, insulating layer 4 remains as a protruding insulating layer over surface diffusion layer 3 and extended surface diffusion layer 12, which, together with insulating layer 4, constitute the “device separation region” as taught by Masagaki. *Id.*, [0009], [0018], Fig. 10, claim 1.

As noted above, the portions of semiconductor well region 22 between charge storage regions 7 (i.e. between photodiodes of Masagaki) ***do not receive any P type ion implantation isolation at any time.*** In the annotated Masagaki Figure 10 below, these portions of semiconductor well region 22 are shaded orange and designated by reference numeral 92.

**No P Type Ion Implantation Isolation at the Interface
between Adjacent Charge Storage Regions 7**



Masagaki Fig. 10

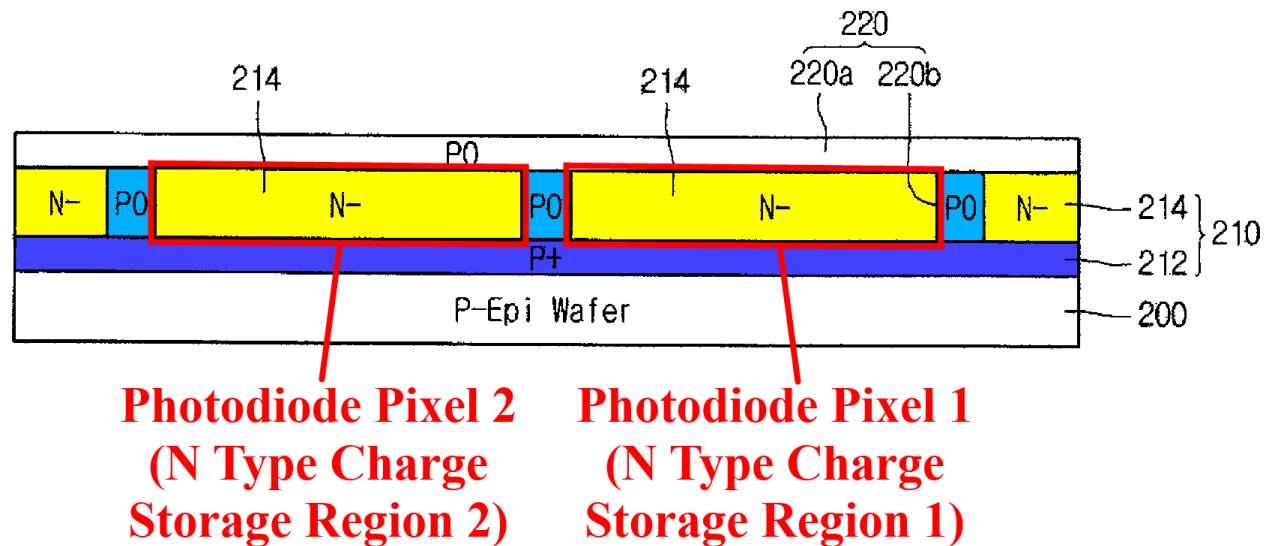
The above-discussed second embodiment of Masagaki clearly fails to disclose or make obvious, and in fact teaches away from step [1.h.2], that is *“forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.”*

As described and shown in the ‘808 patent, “second conduction type conduction layer” (for example, P type layer 212) of photodiode 210 is formed by

a “blanket-ion implantation.” ‘808 patent, 3:19-30, Fig. 2. Also, “first conduction type conduction layer” (for example, N type layer 214) of photodiode 210 is formed by another “blanket-ion implantation” layer. *Id.*, 3:34-40, Fig. 2. P type layer 212 and N type layer 214 together form a contiguous photodiode 210. *Id.*, 3:19-30, 3:34-40, Fig. 2. P type layer 212 and N type layer 214 are blanket photodiode layers that are generally formed without a mask. *Id.*, 3:28-30, 3:34-38.

According to the ‘808 patent, each individual photodiode belonging to an individual pixel is defined and formed due to second conduction type second ion implantation isolation layer 220b that is formed at an interface between pixels, thereby defining the boundaries of each photodiode in adjacent pixels based on such ion implantation. As stated in the ‘808 patent: “[S]econd conduction type second *ion implantation isolation layer 220b may be formed at an interface between pixels of photodiode 210 [L]ayer 220b may be formed at an interface between pixels* using a photolithographic process and *an ion implantation process [L]ayer 220b may be used for pixel-to-pixel isolation of N– layer 214 ... used as the photodiode*” *Id.*, 3:52-60, Fig. 3. The annotated Figure 3 below shows how formation of P type ion implantation isolation layer 220b within N type layer 214 defines “pixels of the photodiode.”

Two adjacent pixels of the photodiode in N type layer 214 are identified below as “photodiode pixel 1” (corresponding to “N type charge storage region 1”) and “photodiode pixel 2” (corresponding to “N type charge storage region 2”).



‘808 Patent Fig. 3

Thus, in each pixel of photodiode 210, an isolated N type charge storage region in layer 214 is defined and formed upon ion implantation of P type isolation layer 220b at the interface between pixels of the photodiode. In contrast, in the second embodiment of Masagaki, portions 92 (shaded orange in Figure 10 above) situated between adjacent extended portions 6, i.e. at the interface between charge storage regions 7, ***do not receive any P type ion implantation isolation at all at any time***. No depthwise ion implantation isolation layer equivalent to the ‘808

patent's ion implantation isolation layer 220b is formed. Therefore, ***“forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode”*** is not disclosed or made obvious by the second embodiment of Masagaki.

Masagaki explains that ***“resist 26*** used to form the extended portion 6 ***continues to be used as a mask***, and a second implantation of a p-type impurity is performed ***on a surface portion 27*** of the diffusion layer 3” Masagaki, [0040], Figs. 9F, 10. Thus, ***the purpose of resist 26 of Masagaki is to block any P type ion implantation between N type extended portions 6*** below diffusion layer 3, which is a surface diffusion layer. Masagaki therefore teaches away from P type ion implantation isolation between charge storage regions 7 since these regions are situated below surface diffusion layer 3, and are blocked by resist 26. *Id.*

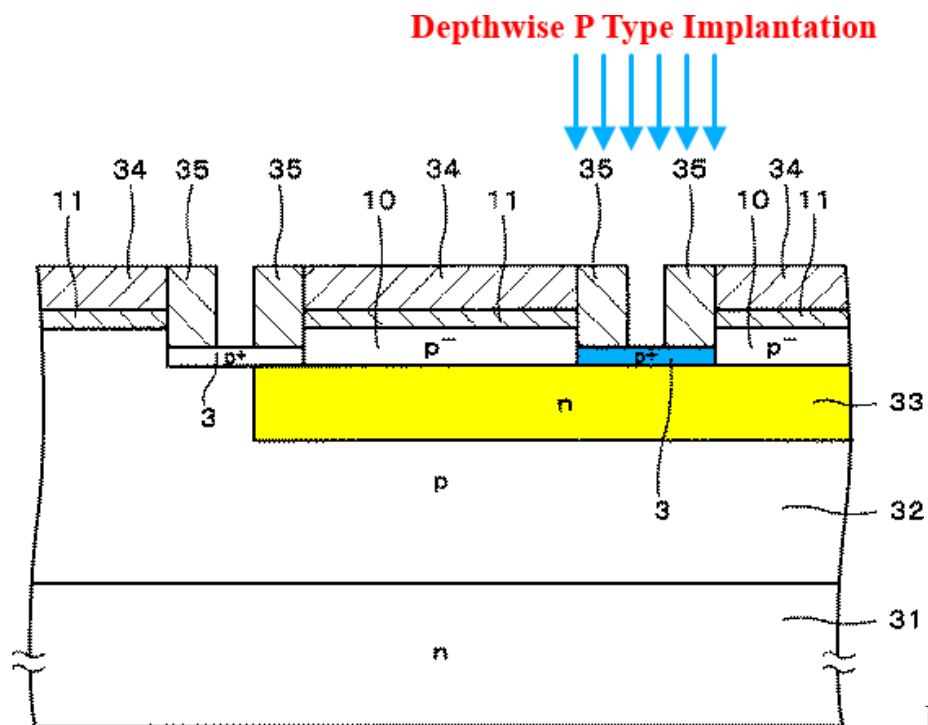
In discussing step [1.h.2], ***the Petition has acknowledged that the second embodiment of Masagaki does not disclose “implantations in the depth direction”*** (Pet. 90) ***between charge storage regions 7, i.e. for “extending to the depth of the charge storage layer 7.”*** *Id.* In light of this admitted lack of a key disclosure in the second embodiment of Masagaki for “implantations in the depth

direction” and extending the implantations “to the depth of the charge storage layer 7,” the Petition has switched to Figure 4 of the first embodiment.

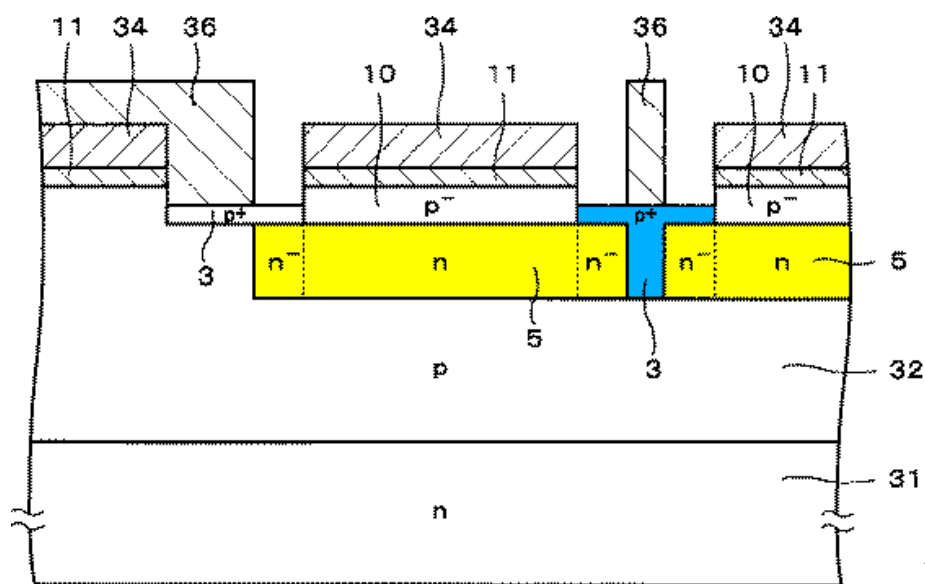
The following paragraph is the Petition’s entire discussion in relation to Figure 4 of the first embodiment that purportedly provides the essential disclosure that is missing from the second embodiment of Masagaki: “POSAs would have understood that Masagaki’s description of forming separation region 3 by *‘ion implantation that increases the depth of the diffusion layer 3’* or *‘several implantations in the depth direction’* in a first embodiment of Fig. 4 (Masagaki, [0030]) also applied to the embodiment shown in Figures 9 and 10, because the two embodiments have the same pixel separation region 3, formed in the substrate, and extending to the depth of the charge storage layer 7.” Pet. 90.

However, Masagaki’s two embodiments are fundamentally different when addressing “*forming a second conduction type second ion implantation isolation layer at an interface between pixels of the photodiode.*” In the first embodiment, the fabrication process *begins with forming an N type region 33*. Masagaki, [0026], Fig. 3A. Then, resist 35 is formed to leave narrow openings over diffusion layer 3. *Id.*, [0029], Fig. 4C. Thereafter, a depthwise P type ion implantation is performed in the narrow openings to create a deep diffusion layer 3 inside N type

region 33 in the depth direction, i.e. between main portions 5. *Id.*, [0030], Fig. 4D. The reason for the depthwise P type ion implantation in the first embodiment is that the *starting point in Figure 3A is an N type region* that is contiguous and that must be separated by depthwise P type ion implantation isolation to form individual N type charge storage regions. The annotated drawings below illustrate that N type layer 33 is contiguous in Figure 4C, and then broken up by the depthwise ion implantation of P type diffusion layer 3 between main portions 5 as shown in Figure 4D. *This process is performed in the first embodiment to separate and isolate adjacent N type charge storage regions that are otherwise contiguous.*



Masagaki Fig. 4C

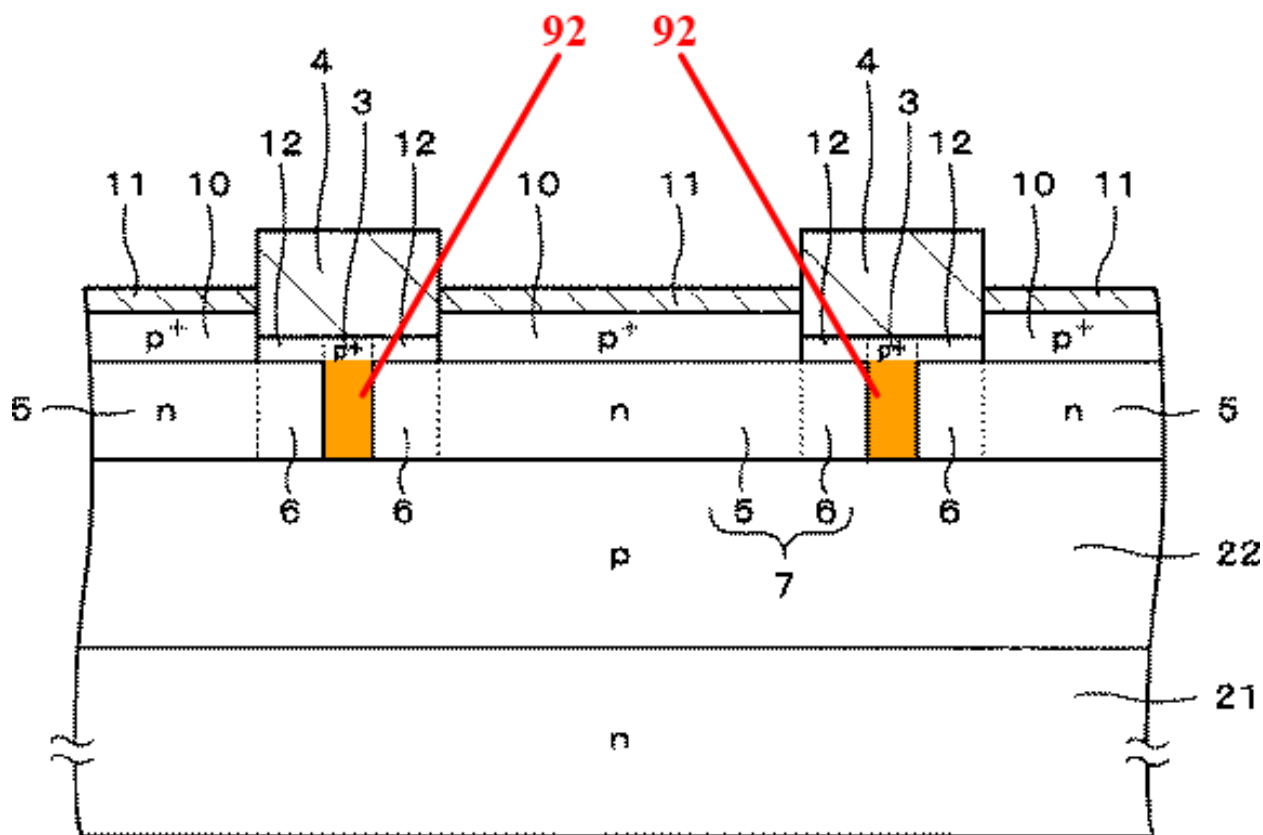


Masagaki Fig. 4D

In stark contrast, the starting point of the second embodiment (a P type region) is opposite the starting point of the first embodiment (an N type region).

In the second embodiment, N type ion implantation is performed in a pre-existing P type region 22 to create the charge storage regions 7 shown in Figures 9E, 9F, and 10. ***Thus, the N type ion implanted regions are already separated*** by P type region 22 pre-existing between storage regions 7 (i.e. portions 92 shaded orange in Figure 10 below). Therefore, ***the second embodiment purposefully avoids an extra step of P type ion implantation isolation since P type isolation already exists between adjacent N type charge storage regions.***

**Already Isolated - Without Any
P Type Ion Implantation Isolation**



Masagaki Fig. 10

As such, the second embodiment of Masagaki *teaches away* from performing a depthwise P type ion implantation isolation that is meant for the first embodiment, but purposely blocked by resist 26 in the second embodiment, since *the starting point of the second embodiment (a P type region) is opposite the starting point of the first embodiment (an N type region).*

Quite the opposite to what the Petition proposes, the second embodiment of Masagaki cannot and would not apply the depthwise ion implantation step of the first embodiment — which the second embodiment purposely blocks — for “implantations in the depth direction” for “extending to the depth of the charge storage layer 7.” (Pet. 90).

C. A POSA WOULD NOT HAVE HAD REASON OR MOTIVATION TO COMBINE LEE AND MASAGAKI, AND ANY SUCH COMBINATION WOULD BE MISSING VARIOUS STEPS, SUCH AS STEPS [1.h.2] AND [1.f]

Petitioner essentially acknowledges that Lee and Masagaki do not provide a disclosure regarding exposing a photodiode by removing a portion of a substrate. Petitioner relies on Shiraiwa as disclosing step [1.f]. Pet. 94.

With respect to step [1.h.2], Petitioner relies only on Masagaki. *Id.*, 90-92. As discussed above, Masagaki does not disclose or render obvious step [1.h.2].

Therefore, even if a POSA had reason or motivation to combine Lee and Masagaki and even if such combination was workable, a combination of Lee with Masagaki would, at the very least, be missing steps [1.h.2] and [1.f].

Nevertheless, the Petition has failed to show that a POSA would have had reason or motivation to combine Lee and Masagaki. The Petition states that “*Masagaki’s Figure 11 discloses a prior art unit pixel almost identical* to that in

Lee” Pet. 69-70. And that: “Lee’s separation unit pixel architecture *corresponds to Masagaki’s prior art unit pixel ...* .” *Id.*, 72. Thereafter, three pages of the Petition are dedicated to annotated drawings purportedly illustrating similarities between “prior art unit pixel” in Masagaki’s Figure 11 and the “separation unit pixel architecture” in Lee’s Figure 10. *Id.*, 73-75. Petitioner then asserts that “Lee’s backside-illuminated detector provides the *same photodetector features* as *the prior art* frontside-illuminated detector in *Masagaki Fig. 11* [i.e. Masagaki’s ‘prior art unit pixel’].” *Id.*, 74.

However, the arguments advanced by Petitioner as “reasons to combine” Masagaki with Lee are not for achieving the structure that is “almost identical to that in Lee” (i.e. Masagaki’s “prior art unit pixel” in Figure 11), but for achieving a different structure, that is Masagaki’s second embodiment in Figures 7 through 10. Therefore, the objective of the combination is not the structure that a POSA is purportedly motivated to achieve — that is the “prior art unit pixel” in Figure 11 of Masagaki — but it is a different structure, which is Masagaki’s solution in its Figures 7 through 10. Thus, as an initial matter, Petitioner’s argument for the combination is logically flawed.

Petitioner's argument before it addresses "reasons to combine" Lee and Masagaki can be summarized as follows:

"Lee's separation unit pixel architecture corresponds to Masagaki's prior art unit pixel" Pet. 72. And that "Masagaki's novel charge storage region extension involves features in a cross-sectional view on a plane denoted by b'-b' in Masagaki Figures 1A, 10. Carley, ¶323. Lee's figures have no comparable perspective. Carley, ¶324. Rather, Masagaki's Figure 10 corresponds to a cross-sectional view of the improvement over the prior art structure in Lee, and Figure 11, on a plane b'-b' that vertically bisects layer 14 in Lee Fig. 10."⁹ *Id.*, 76.

The Petition then asserts that: "The combination [of Lee and Masagaki] does not use Masagaki's insulating film 4, or etching to place it, because the frontside surface abuts the insulator layer providing the gate dielectric for transfer transistor

⁹ Petitioner has not provided any clarification as to the meaning of this difficult to understand paragraph. This paragraph is quoted herein since it appears to include key contentions relevant to a *prima facie* case of obviousness that Petitioner wants to advance. However, the paragraph is ambiguous and perplexing to a degree that Patent Owner is unable to make a direct response to it.

15 [*sic*], between the p-type pinning layer and the dielectric that contains pad 17 in Lee’s 3D imager.”¹⁰ *Id.*, 77.

The Petition then sets forth its “reasons to combine” by stating that: “Both Lee and Masagaki are concerned with mitigating the loss in photodiode sensitivity when reducing pixel dimensions.” *Id.*, 78. And that “Lee addresses this issue [i.e. loss of sensitivity] with a ‘separation type unit pixel’ in which ‘sensitivity drops far less ... than a conventional case in the manufacturing of a miniature pixel.’ Masagaki’s objective was ‘to provide a solid state image sensor wherein a unit pixel can be miniaturized without sacrificing an effective area of a charge storage region[.]’ ... POSAs would have understood that Masagaki’s solution—extending the charge storage region—would improve the sensitivity of Lee’s similar photodiode structure, and further mitigate the loss of sensitivity associated with reducing pixel dimensions.” *Id.*, 79.

¹⁰ No clarification is provided by Petitioner, and Patent Owner is unable to adequately understand this paragraph. The paragraph is quoted since it appears to include key contentions relevant to a *prima facie* case of obviousness that Petitioner is attempting to set forth.

Petitioner’s “reasons to combine” Lee with Masagaki fail at several levels and for many reasons. To state that “[b]oth Lee and Masagaki are concerned with mitigating the loss in photodiode sensitivity when reducing pixel dimensions,” even if true, is to recite a very general goal that involves practically any image sensor design effort. In other words, a primary goal of an image sensor is to have higher quality images due to more sensitive photodiodes and greater number of pixels (which has a direct relation with reducing pixel dimensions). Therefore, the statement that both Lee and Masagaki are concerned with mitigating the loss in photodiode sensitivity when reducing pixel dimensions, even if true, is no more than stating that both Lee and Masagaki are relevant to the same field of endeavor of achieving a high quality image sensor.

The Board has held such broad recitations as insufficient reason or motivation to combine: “Demonstrating that a reference is ... relevant to the field of endeavor of the challenged patent is not sufficient to establish ... [a] reason to combine its teachings with other prior art in the manner set forth in the claim.” *Johns Manville Corp. v. Knauf Insulation, Inc.*, IPR2018-00827, Paper 9, at 10 (Oct. 16, 2018). *See also Securus Techs., Inc. v. Global Tel*Link Corp.*, 701 F. App’x 971, 977 (Fed. Cir. 2017) (non-precedential) (“***a broad***

characterization of [prior art references] as both falling within the same alleged field ... without more, is not enough for [Petitioner] to meet its burden of presenting a sufficient rationale to support an obviousness conclusion”).

The Board followed the same line of reasoning in *William Wesley Carnes, Sr., Inc. v. Seaboard Int’l Inc.*, IPR2019-00133, Paper 10, at 18 (May 8, 2019):

“[The] statement of similarity, however, does not constitute an articulated reasoning with rational underpinning as to why a POSITA would combine elements of one reference with another, and why a POSITA would modify the teachings of the references to arrive at the claimed invention.”

Petitioner’s statements that Masagaki’s techniques “could be used” in Lee, also do not provide sufficient reason for a combination. Petitioner states that: “Masagaki’s manufacturing techniques and pixel including an extended charge storage region below and adjacent ion-implanted diffusions *could be used* to improve the charge storage in Lee’s separation unit pixel” Pet. 80. The Petition similarly states that “photodetector structures for a frontside detector like Masagaki *could be implemented* in a backside-illuminated architecture like Lee’s unit pixel.” *Id.*, 81.

The Board has maintained that statements that a combination “could be” made do not provide sufficient reason to make the combination obvious: “Furthermore, to the extent that Petitioner is asserting that a POSITA ‘*could*’ *have combined*’ the references to reach the claimed invention, this is also insufficient for obviousness. *See Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017) (saying that references *could be combined* ‘does not imply a motivation to pick [the references] and combine them to arrive at the claimed invention.’); *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1074 (Fed. Cir. 2015) (‘obviousness concerns whether a skilled artisan *not only could have made but would have been motivated to make the combinations* or modifications of prior art to arrive at the claimed inventions.’).” *William Wesley Carnes, Sr., Inc., supra*, at 18-19.

Vast quantity of academic literature and patents and other art references are directed to the common goal of increasing photodiode sensitivity and reducing pixel dimensions, employing numerous different designs and methods. If the goal of increasing photodiode sensitivity and reducing pixel dimensions was sufficient reason or motivation to pick and combine any two art references within the entire universe of the relevant art references, there would be reason and motivation to

combine a countless number of image sensor art references, and the requirement for articulating sufficient reason to combine would be rendered meaningless.

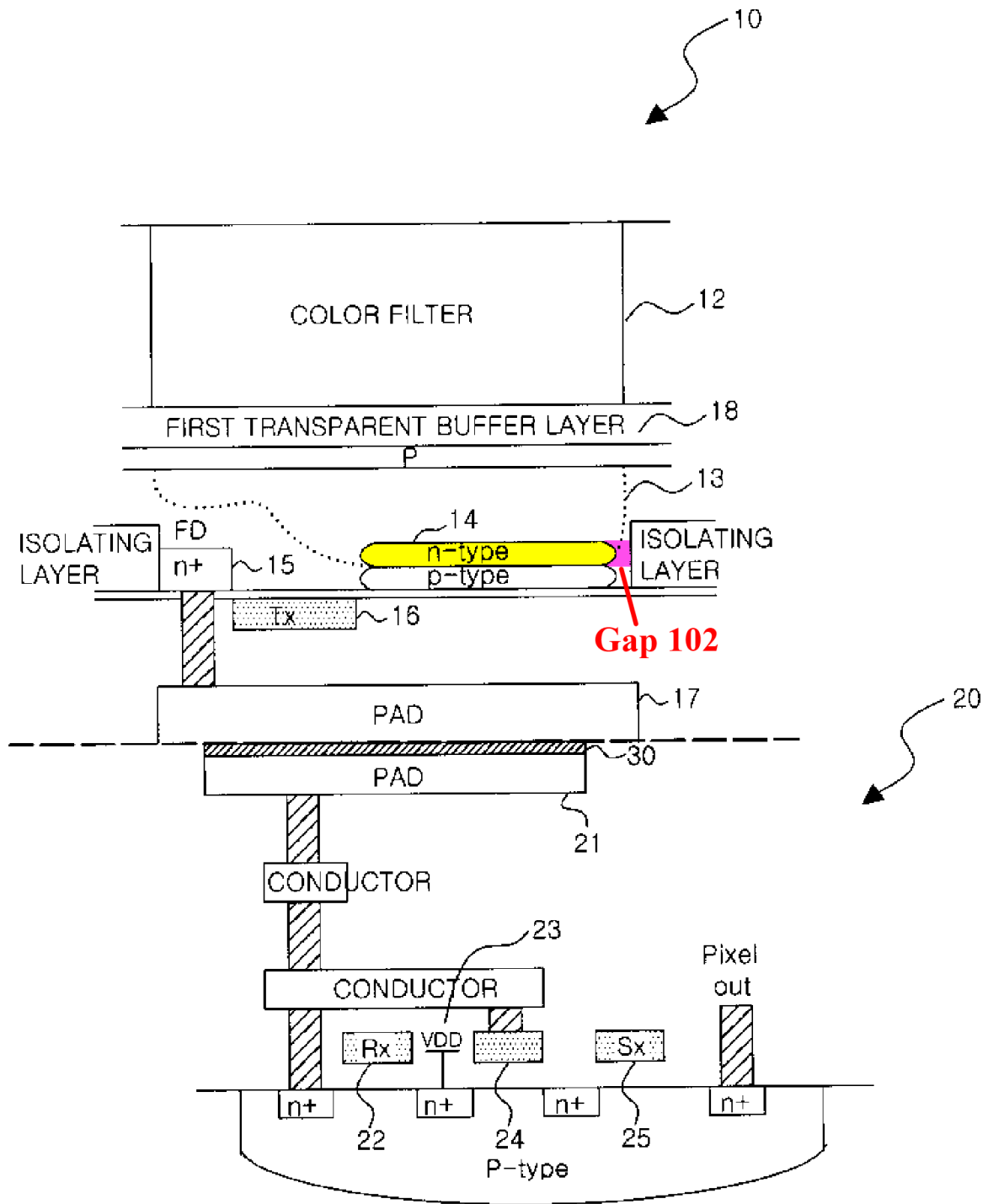
Any analysis beyond the general recitation of a broad goal of increasing photodiode sensitivity and reducing pixel size would reveal the clearly divergent approaches adopted by Lee and Masagaki, and the fact that there would not be sufficient reason or motivation for a POSA to apply the unique processes of Masagaki to Lee's image sensor.

Lee provides no reason or motivation for "extending [its] charge storage region ['photodiode 14' or 'n-type 14' in Lee's Figure 10)]" (Pet. 79) underneath an ion implanted isolation region (in the manner taught by Masagaki) to "improve the sensitivity of Lee's similar photodiode structure." Pet. 79.

First, as discussed below, Lee does not disclose or suggest a *semiconductor* isolating layer and, therefore, does not disclose or suggest an ion implanted isolation layer. Second, in Lee's Figures 8, 10, and 11, charge storage region 14 is shown as not reaching or touching the box labeled "isolating layer." If Lee was concerned with the idea of extending the charge storage region in any manner, at a minimum Lee would have extended charge storage region 14 to reach Lee's isolating layer. According to Masagaki's technique for improving photodiode



All of Lee's drawings depict charge storage region 14 as not reaching the edge of the "isolating layer," and certainly not extending underneath the "isolating layer." The gap colored pink and pointed to by numeral 102 shows that Lee's charge storage region 14 does not reach the "isolating layer."



Lee Fig. 10

In fact, a POSA would be deterred from combining Lee and Masagaki since Lee utilizes fundamentally different process steps, architecture, and physical structure for increasing photodiode sensitivity and reducing pixel dimensions than Masagaki.

Petitioner has repeatedly referred to the phrase “***separation*** type unit pixel” used in Lee and has also introduced Petitioner’s own modified phrase “Lee’s ***separation*** unit pixel” for the purpose of implying an equivalence or a relation with the phrase “device ***separation*** region” in Masagaki. Pet. 69, 72, 74, 77, 79, 80, 97. However, the phrase “separation type unit pixel” in Lee has a completely different meaning than “device separation region” in Masagaki. It is clear throughout Lee that the phrase “separation type unit pixel” refers to the ***two separate wafers*** by means of which various components of the “unit pixel” have been separated.

There is ample reason to know that Lee’s “separation type unit pixel” has nothing to do with the “isolating layer” in Lee. For example, Lee states that “there is provided a ***manufacturing method of a separation type unit pixel*** ... comprising: ***(a) constructing a first wafer which includes a photodiode***, a transfer transistor, and a floating diffusion area ... ; ***(b) constructing a second wafer which includes the rest of the circuit elements constituting a pixel*** (i.e., a reset transistor,

a source-follower transistor, and a blocking switch transistor)" Lee [15].

Also: "*The separation type unit pixel includes a first wafer 10 and a second wafer 20.*" *Id.*, [33].

Lee's drawings also make clear what "separation type unit pixel" refers to. Figures 1 through 3 of Lee "show circuit diagrams of a *conventional pixel structure* of an image sensor." *Id.*, [16]. In contrast, Figures 4 through 7 show "circuit diagrams of a *separation type unit pixel* of an image sensor according to an embodiment *of the present invention.*" *Id.*, [17]. Figures 1 through 3 use all solid lines, indicating a complete circuit connection within the same wafer. In contrast, Figures 4 through 7 show that the "transfer" transistor is connected by a dotted line to the remaining transistors, indicating circuit connection between two separate wafers.

Lee further states: "FIG. 12 is a flowchart of a manufacturing method of a *separation type unit pixel having a 3D structure*" *Id.*, [45]. In the flowchart of Figure 12, and wherever Lee refers to a "3D structure," it is clear that a "3D structure" refers to the three-dimensional stacking of the "first wafer" on the "second wafer." Lee, Fig. 12 (S511, S512, S520). It is thus plain that Lee is not referring to

any isolation structure when using the phrase “separation type unit pixel.” No isolation structure is discussed anywhere in Lee.

In Lee “the separation unit pixel” refers to a *two-wafer architecture*. Petitioner incorrectly asserts that “*Lee’s separation unit pixel architecture corresponds to Masagaki’s prior art unit pixel ...*” Pet. 72. And that “*Lee’s separation type unit pixel* conduction and isolation layers ... *correspond to the photodetector structure in Masagaki’s prior art Figure 11 ...*” *Id.*, 77.

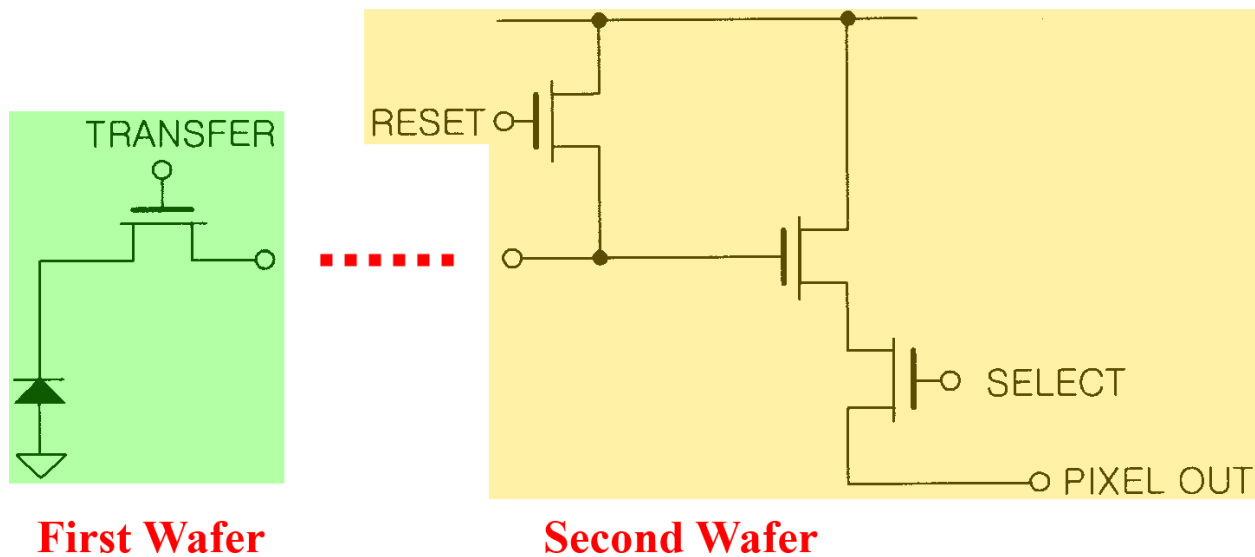
Moreover, as discussed in detail below, Lee’s “isolating layer” is very likely a dielectric layer and not a semiconductor layer (and Petitioner has not argued that Lee’s “isolating layer” is a semiconductor layer). Given the vastly different architectures and physical structures of Lee and Masagaki, the fact that Lee is completely silent on its “isolating layer,” and that it is very likely a dielectric layer and not a semiconductor layer, it is not clear how and what in Lee’s unit pixel and isolating layer “corresponds to” the unit pixel and semiconductor isolation in Masagaki.

Masagaki discloses a frontside-illuminated photodiode (*see, e.g.*, Pet. 74) using a single wafer (*see, e.g.*, Masagaki, Figs. 10-12). Lee discloses a backside-illuminated photodiode (*see, e.g.*, Pet. 68, 79) using two wafers (*see, e.g.*, Lee,

Figs. 10-12). That is one of the reasons that Lee's approach for increasing photodiode sensitivity and reducing pixel dimensions is fundamentally different than Masagaki.

Lee comments on a conventional design prior to Lee's "separation type unit pixel," where the reset, source-follower, and blocking switch [i.e. the select] transistors are not separated from the pixel's photodiode as follows: "***Due to the existence of transistors in a pixel circuit, as shown in FIG. 1 to 3, a fill factor of a photodiode, that is an area for the photodiode with respect to a pixel size, is naturally reduced.*** ... Light that is incident onto the rest area of 55 - 80 % of the pixel is therefore lost." Lee, [5].

In contrast, Figures 4 through 7 of Lee show Lee's "separation type unit pixel" in circuit schematic form, wherein the reset, source-follower, and blocking switch [i.e. the select] transistors are separated from the transfer transistor and photodiode as indicated by a dotted line that indicates the separation. This is illustrated below in the annotated Figure 4 of Lee.



Lee Fig. 4

The separated transistors are fabricated in a different wafer than the wafer in which the photodiode resides. A direct result of this separation is to create additional area for a larger photodiode with a concomitant greater charge storage capacity and improved sensitivity while reducing pixel dimensions due to moving most of the transistors to the second wafer. Lee states that the area of the pixel is made to be almost the same as the area of the photodiode (since most of the associated transistors have been removed). According to Lee, the pixel area is almost entirely occupied by the (larger) photodiode (instead of being shared with several transistors). The larger photodiode has greater charge storage capacity and sensitivity: “Accordingly, the present invention has advantages in that, by *forming*

an area for a photodiode and an area for a pixel almost the same, an image sensor can be manufactured to *have a good sensitivity* in a subminiature pixel” Lee [64].

Further, Lee’s backside illumination results in greater photodiode sensitivity, compared with frontside illumination disclosed in Masagaki. For example, Iwabuchi compares frontside illumination with backside illumination as follows: “[I]n the above-mentioned *back-illuminated type* CMOS solid-state image pickup device 1021, since the light L is introduced from the back surface side of the substrate into this CMOS solid-state image pickup device 1021, it is possible to *increase the light-receiving area as compared with the surface-illuminated type* CMOS solid-state image pickup device *and hence sensitivity can be increased.*” Iwabuchi, [0047].

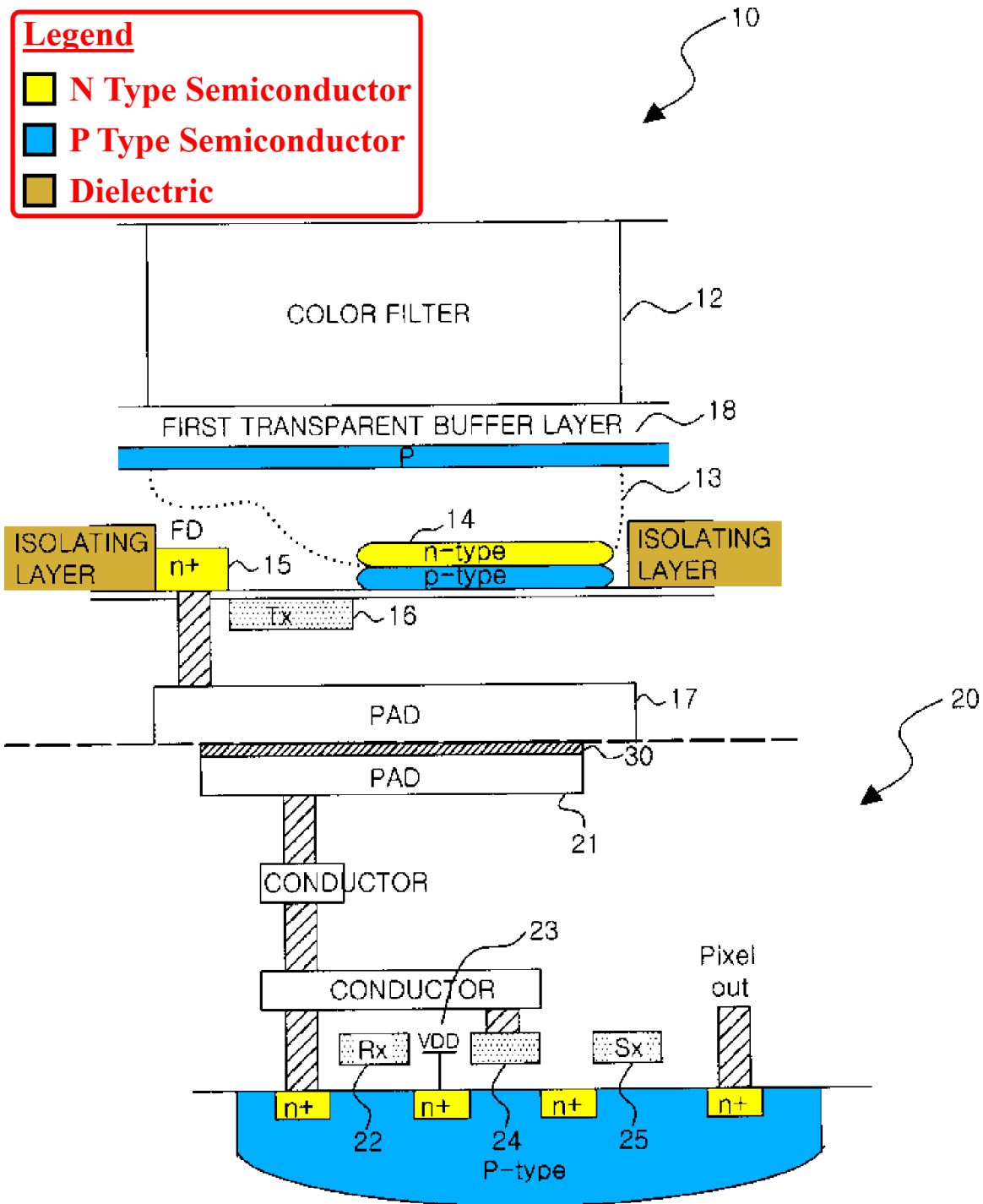
As another example, Pain (Ex. 1021) explains that: “*Imaging with a back-illuminated CMOS imager provides a number of advantages, especially as the pixel size is reduced. These advantages include high (100%) fill-factor*” Pain, 35.

Therefore, Lee’s approach to “mitigating the loss in photodiode sensitivity when reducing pixel dimensions” (Pet. 78) is drastically different from Masagaki’s

approach. Neither Lee nor Masagaki provides a reason or motivation to apply Masagaki's single-wafer, frontside-illuminated technique for extending the charge storage region by unique processes to Lee's two-wafer, backside-illuminated technique that focuses on creating space for a larger photodiode by removing most of the transistors from the pixel where the photodiode resides.

To support its arguments for a combination with Masagaki, Petitioner has made much of Lee's "isolating layer," while Lee itself is silent on the "isolating layer" and is not concerned with the fabrication, function, or constituent material of the "isolating layer." Based on the only information available in Lee, it is quite unlikely that Lee's "isolating layer" includes an "N type" or a "P type" semiconductor. Lee has identified and labeled its semiconductor layers and semiconductor features, **but not** its "isolating layer," as "n-type" or "p-type" or "n+" or "N" or "P" in Figures 8, 10, and 11. It can thus be logically and strongly inferred that Lee's "isolating layer" shown in Figures 8, 10, and 11 is very likely a dielectric layer, and not a semiconductor layer, and specifically not an N type or a P type semiconductor layer. Moreover, Petitioner has not contended that Lee's "isolating layer" is a semiconductor layer, or an N type or a P type semiconductor layer. In Lee's Figure 10 below, various layers have been shaded yellow

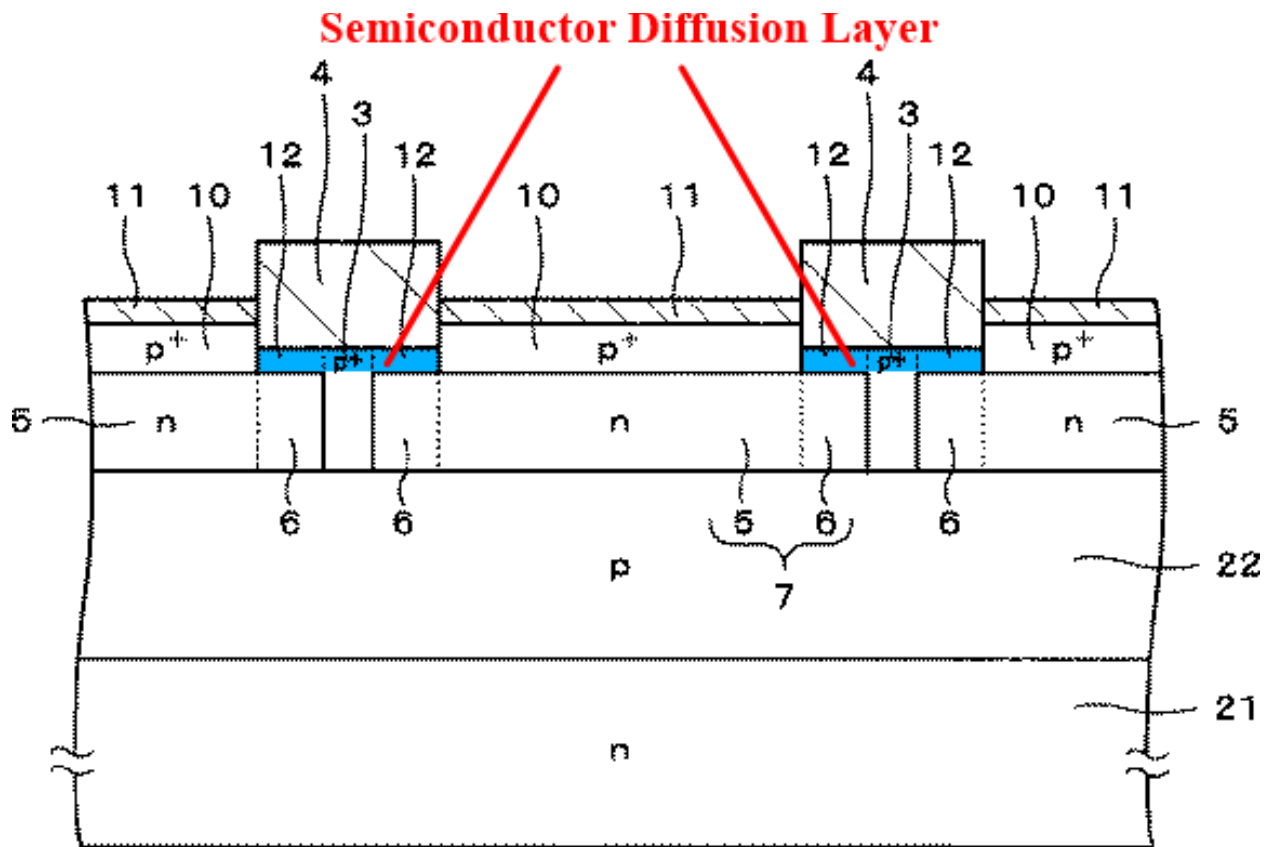
corresponding to “N Type Semiconductor” and blue corresponding to “P Type Semiconductor.” The “isolating layer” has been shaded gold corresponding to “Dielectric.”



Lee Fig. 10

Therefore, Petitioner has made an unsupportable and unexplained assumption that Lee’s “isolating layer” is akin to semiconductor “ion-implanted diffusions” (Pet. 80) of Masagaki. The implicit assumption is apparent in the Petition’s following coded comment and its related annotated drawing: “lateral isolation layer (‘isolating layer’ (Lee), 103 (Masagaki))” Pet. 74.

Unlike Lee’s “isolating layer” (whose material is not described in Lee, but is very likely a dielectric), Masagaki’s “device separation region” relies on a ***semiconductor*** diffusion layer for isolation between photodiodes. *See, e.g.*, Masagaki, [0034], Fig. 10 (surface diffusion layers 3 and 12), and [0037], Fig. 8C (surface diffusion layer 3). The annotated Figure 10 of Masagaki below illustrates semiconductor surface diffusion layers 3 and 12 shaded blue in Masagaki’s “device separation region.”



Masagaki Fig. 10

Lee provides no reason or motivation for a POSA to modify its isolating layer. Nevertheless, even if a POSA had reason to or was motivated to modify Lee's isolating layer, there is no reason to adopt the unique processes of Masagaki.

As discussed above, the ion implantation structures in Masagaki are not at all similar to the "isolating layer" in Lee. As another example, there is the existence of the protruding insulating layer (or insulating film) 4 in Figure 10 of Masagaki. The protruding insulating layer 4 is included in every "device

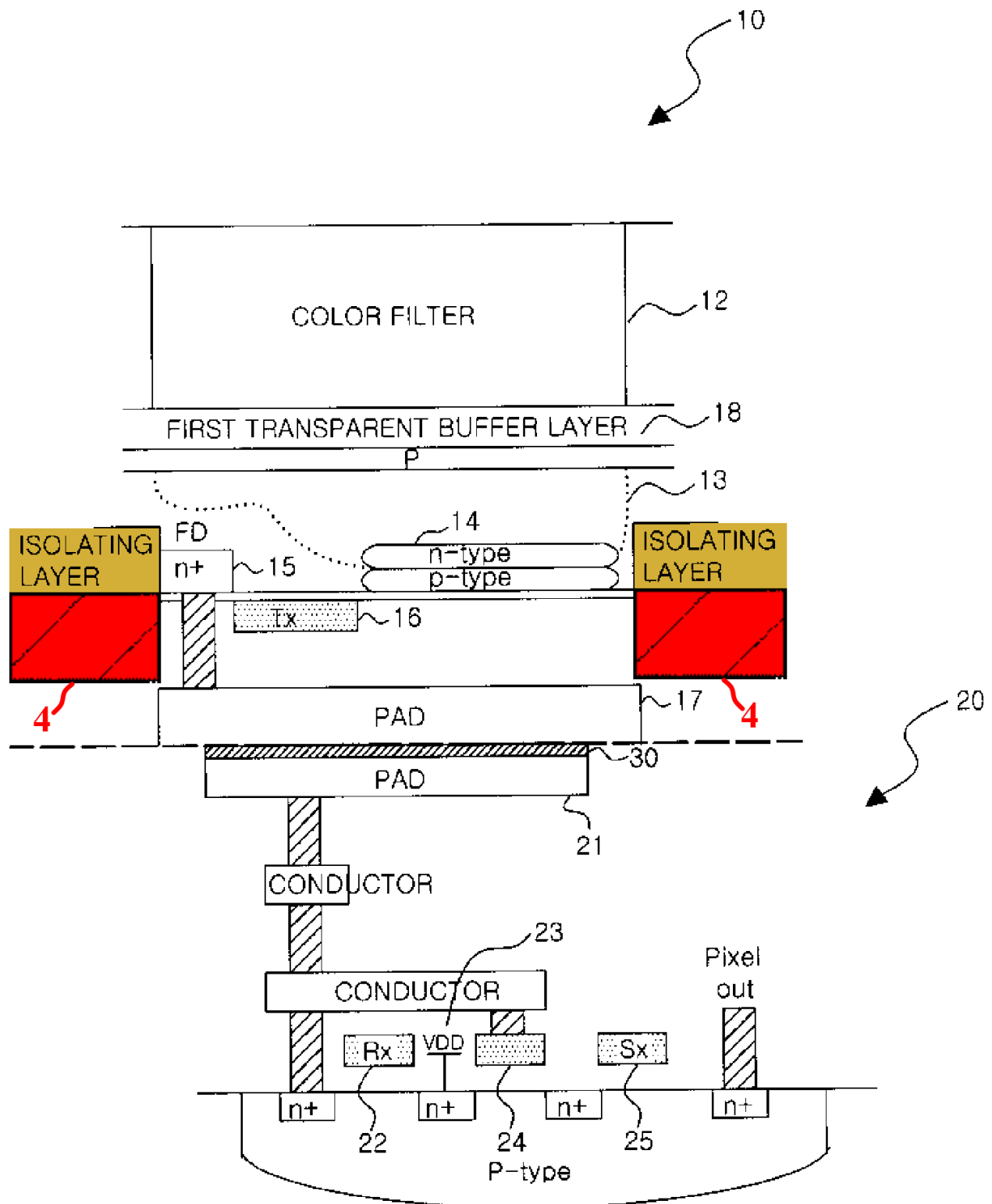
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Masagaki's disclosed method, and is used as an insulating filler between etched out portions of the hard mask. *See, e.g., id.*, [0035], [0040], Figs. 9F, 10. Insulating layer 4 is not an optional insulating layer that can be avoided or optionally added; it is always situated over surface diffusion layers 3 and 12.

There is no reason or motivation to incorporate the protruding insulating layer 4 into Lee's image sensor. Petitioner has acknowledged this problem, and has provided only the following purported resolution:

"The combination does not use Masagaki's insulating film 4, or etching to place it, *because* the frontside surface abuts the insulator layer providing the gate dielectric for transfer transistor 15 [*sic*], between the p-type pinning layer and the dielectric that contains pad 17 in Lee's 3D imager." Pet. 77. There is no reasoning or clarification from Petitioner as to how what follows "because" supports the conclusion that "the combination does not use Masagaki's insulating film 4."

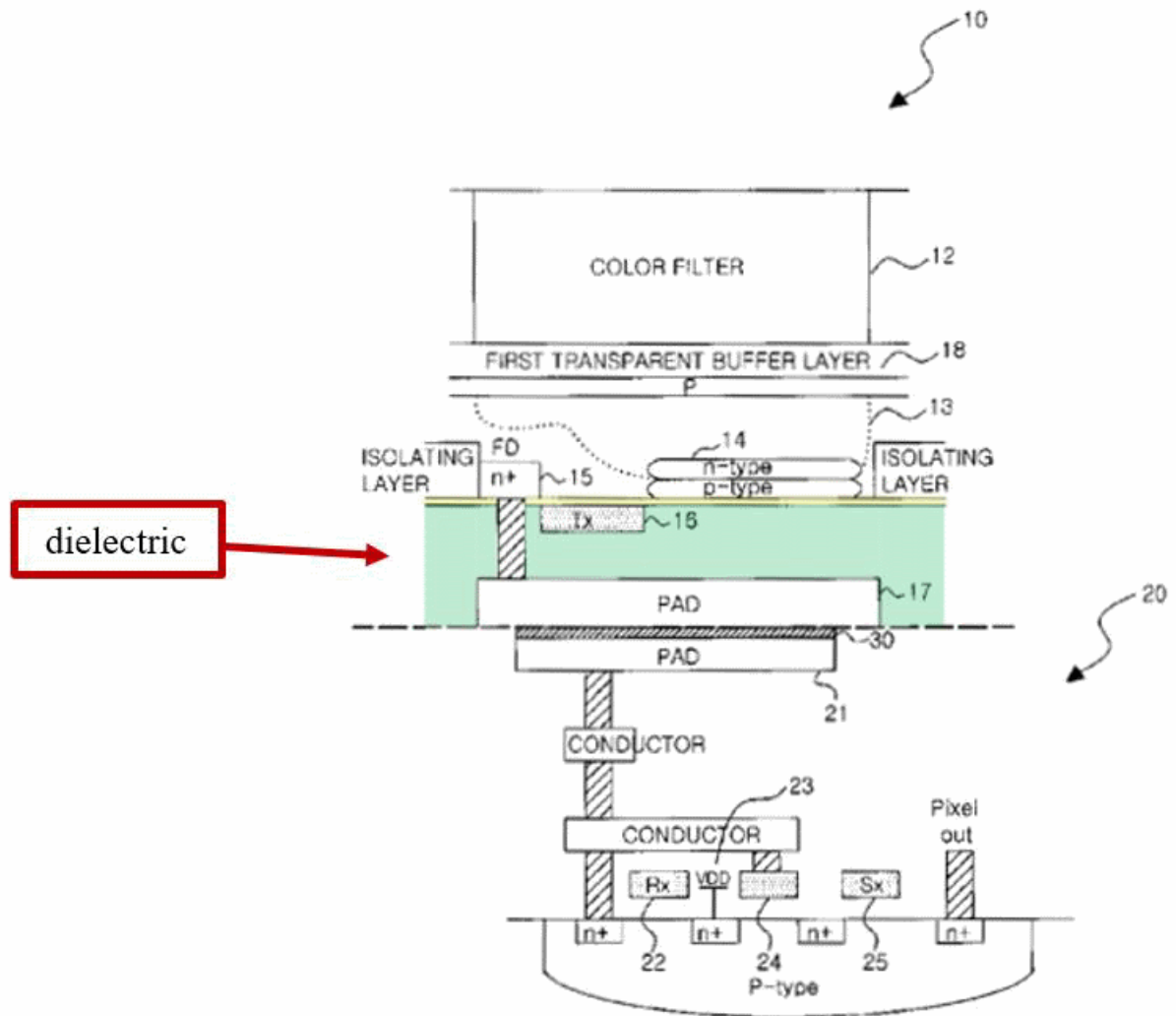
The following drawings show how the protruding insulating layer 4 would appear on the opposite side of Lee's isolating layer in a hypothetical combination of Lee and Masagaki.



Masagaki's "insulating layer 4," shaded red, would awkwardly protrude from the opposite side of Lee's "isolating layer."

In the drawing on page 98 of the Petition, reproduced below, Petitioner itself has designated the entire expanse between the top surface of wafer 20 and Lee's "isolating layer" as "dielectric" (appearing in a red box). The Petition simply does not address how insulating layer 4 of Masagaki would be reconciled with this pre-existing blanket "dielectric" layer in Lee. It is not at all discussed as to how or why a POSA would do away with insulating layer 4 in Masagaki and replace it with the blanket dielectric layer in Lee. A POSA would be deterred to combine Masagaki's insulating layer 4 into Lee's image sensor without any reason to do so, especially when the protruding insulating layer 4 is incompatible with the blanket dielectric layer that, according to Petitioner, already exists in Lee's image sensor.

[Fig. 10]



D. SHIRAIWA DOES NOT DISCLOSE OR MAKE OBVIOUS VARIOUS STEPS, SUCH AS STEPS [1.d], [1.h.1], [1.h.2], AND [1.f]

As essentially acknowledged by Petitioner, Shiraiwa does not disclose steps [1.d], [1.h.1], and [1.h.2]. Pet. 88-92. Petitioner relies on Masagaki for disclosing steps [1.d], [1.h.1], and [1.h.2]. *Id.* Petitioner relies on Shiraiwa as disclosing step [1.f]. *Id.*, 94.

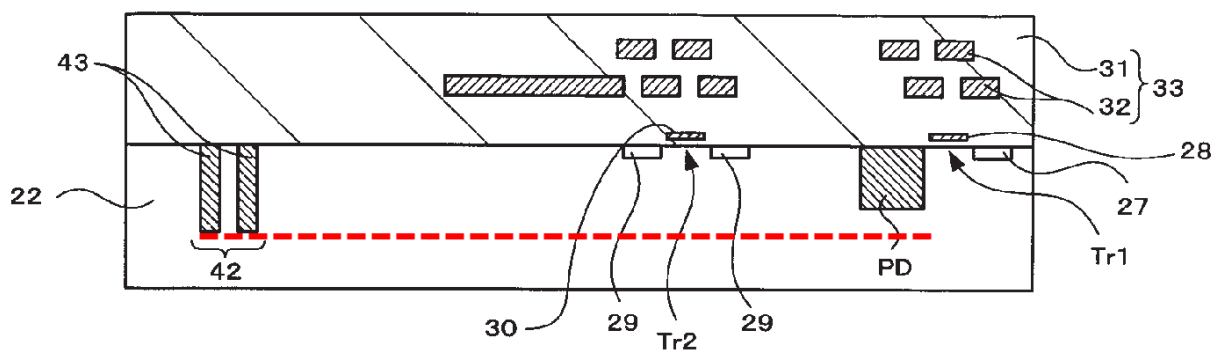
Contrary to the Petition’s arguments (*id.*, 94), Shiraiwa does not disclose or make obvious various claim 1 steps, such as step [1.f], that is “removing a lower portion of the second substrate to expose the photodiode.”

Although Figure 5E of Shiraiwa depicts photodiode PD without overlying layers, Petitioner’s assertion that “Shiraiwa *describes* removing the silicon substrate’s lower portion *to expose the photodiode*” (Pet. 94, citing Shiraiwa, [0037]) is incorrect. Nowhere does Shiraiwa provide such a description. Rather, in the cited paragraph [0037], Shiraiwa describes *exposing end point detection portion 42* as one metric for when to end the thinning action: “Next, as illustrated in FIG. 5E, ... by using, for example, an end point detector (EPD), *the end point of thinning is* detected by the emission intensity change *when* the embedded silicon

oxide film 43 of the *end point detection portion 42* formed in FIG. 3B *is exposed.*” Shiraiwa, [0037].

In fact, Shiraiwa never mentions *exposing* the photodiode, or the desirability of doing so. At best, the exposing of photodiode PD in Figure 5E is a mere coincidence with the exposure of end point detection portion 42. Such coincidence, without any mention of a desired goal or benefit of exposing the photodiode, would not provide a POSA the necessary reason or motivation for “*removing ... to expose the photodiode.*”

The exposure of photodiode PD in Figure 5E is also inconsistent with Figures 4C and 4D of Shiraiwa. For example, Figure 4D (below, annotated) shows that end point detection portion 42 is *deeper* than photodiode PD immediately prior to the backside thinning of semiconductor substrate 22.



Shiraiwa, Fig. 4D

Thus, if, as described in Shiraiwa, the backside thinning action ends when end point detection portion 42 is exposed, then the backside thinning action *would not* expose photodiode PD. Indeed, Shiraiwa describes that the depth of end point detection portion 42 from the front surface of semiconductor substrate 22 is equivalent to the thickness of semiconductor substrate 22 after it is thinned: “***The end point detection portion 42 is formed*** from an embedded layer 43 of a material different from that of the semiconductor substrate 22 ***at a depth equivalent to the thinned thickness*** from the front surface of the semiconductor substrate 22.” Shiraiwa, [0028].

End point detection portion 42 would need to be shallower than, or at the same depth as, photodiode PD if the backside thinning action were to expose photodiode PD. Shiraiwa does not describe making end point detection portion 42 shallower than, or at the same depth as, photodiode PD. Thus, Shiraiwa does not describe “***removing ... to expose the photodiode,***” and does not provide a POSA the necessary reason or motivation for doing so.

Moreover, in the ‘808 patent, “to expose the photodiode” uses the ordinary meaning, and refers to exposing the photodiode such that no material is covering it. For example, as shown in Figures 7 and 8 of the ‘808 patent, a portion of second

substrate 200 is removed to expose photodiode 210 such that no material is covering it. ‘808 patent, Figs. 7-8, 4:40-43. Shiraiwa uses the term “expose” three times: Twice with respect to end point detection portion 42 in Figure 5E (Shiraiwa, [0037]), and once with respect to silicon layer 3 in Figure 9E (*id.*, [0010]). Each time, the term is used consistently with its usage in the ‘808 patent. Shiraiwa clearly understands how to describe an element being exposed. Yet — despite Shiraiwa’s statement that “. . . the silicon substrate 22 may be thinned to a required thickness by controlling the timing of subsequent dry etching after detecting the emission intensity change and detecting that the . . . end point detection portion 42 is exposed” (*id.*, [0037]), and illustrations in Figures 1 and 5E that appear to show photodiode PD and end point detection portion 42 at close to the same level — Shiraiwa never uses the term “expose,” or any variant or synonym thereof, with respect to photodiode PD. Shiraiwa’s failure to describe exposing photodiode PD is not inadvertent.

Rather, in light of Shiraiwa’s express descriptions that “[t]he end point detection portion 42 is formed . . . at a depth equivalent to the thinned thickness from the front surface of the semiconductor substrate 22” (*id.* [0028]), as well as the inconsistent depiction of the depth of end point detection portion 42 from

Figures 4C, and 4D to Figure 5E, it is apparent that Shiraiwa is unconcerned with exposing photodiode PD.

With respect to the final structure shown in its Figure 1, Shiraiwa describes: “The photodiode PD is formed so as to extend from the front surface side to the back surface side of the semiconductor substrate 22 ...” and “light is radiated on the photodiode PD from the substrate back surface side through the on-chip lens 40.” *Id.*, [0027]. However, this description does not mean that the thinning action reaches photodiode PD and exposes the photodiode, just that photodiode PD extends towards the back side and light can reach it from the back side.

E. A POSA WOULD NOT HAVE HAD REASON OR MOTIVATION TO COMBINE LEE AND MASAGAKI AND SHIRAIWA, AND ANY SUCH COMBINATION WOULD BE MISSING VARIOUS STEPS, SUCH AS STEPS [1.h.2] AND [1.f]

As discussed above, any combination of Lee and Masagaki does not disclose or make obvious various claim 1 steps, such as steps [1.h.2] and [1.f]. *Supra* §III.C.

Moreover, as essentially acknowledged by Petitioner, Shiraiwa does not disclose step [1.h.2]. Pet. 90-92. As also discussed above, Shiraiwa does not disclose or make obvious various claim 1 steps, such as step [1.f]. *Supra* §III.D.

Therefore, even if a POSA had reason or motivation to combine Lee and Masagaki and Shiraiwa, and even if such combination was workable, a purported combination of Lee and Masagaki and Shiraiwa would, at the very least, be missing steps [1.h.2] and [1.f].

The Petition has introduced Shiraiwa in the combination only in relation to step [1.f], that is “removing a lower portion of the second substrate to expose the photodiode.” Pet. 79-80, 94. In discussing a combination of Lee and Masagaki and Shiraiwa, the Petition has argued only for a combination of Lee with Shiraiwa (*id.*) and has not included Masagaki in those arguments since, unlike Lee and Shiraiwa, Masagaki discloses a frontside-illuminated, single-wafer image sensor and is not relevant to step [1.f].

However, the Petition has failed to show that a POSA would have had reason or motivation to combine Lee and Shiraiwa. For “reasons to combine” Lee and Shiraiwa, the Petition states that: “Both Lee and Shiraiwa describe wafer-scale backside-thinned device fabrication. While Lee describes reducing wafer thinning by backside etching or grinding, ... Shiraiwa provides precise substrate thickness at lower cost and with less planar variation than obtained when using the oxide layer in *SOI wafers* as an etch stop. Shiraiwa, [0021]-[0022]. POSAs would have

used Shiraiwa because it gives more detailed process information on backside thinning than Lee.” Pet. 79-80.

Petitioner misleadingly refers to Shiraiwa as providing “precise substrate thickness at lower cost and with less planar variation.” The cited paragraphs [0021]-[0022] in Shiraiwa refer to the high cost of **SOI wafers**. Further, according to Shiraiwa, the SOI wafer’s oxide layer (“oxide film 2”) is used as a stopper to control the thinning process of the SOI wafer. *See, e.g.*, Shiraiwa, [0008], [0010] (“silicon oxide film 2 as a stopper film”), Fig. 7A. Oxide film 2 is an integral and necessary part of the SOI wafer (i.e., the “Insulator” in the “Silicon-On-Insulator” wafer). *See, e.g.*, Shiraiwa [0008], Fig. 7A (showing silicon layer 3 on oxide film 2, that is “Silicon-On-Insulator”). In the SOI wafer, photodiode PD is situated in silicon layer 3 which is atop oxide film 2. *Id.*, [0008], Fig. 7B.

Shiraiwa states that “there is a problem in that manufacturing costs increase because ***the SOI substrate is ten times as expensive as a normal silicon substrate.***” *Id.*, [0012]. When using the much less expensive “normal silicon substrate,” a stopper other than oxide film 2 must be used since oxide film 2 (an integral part of the SOI wafer) is not a part of a “normal silicon substrate.” In the non-SOI wafer, photodiode PD is situated in silicon substrate 22 and, unlike the

SOI wafer, silicon substrate 22 is **not** atop an oxide film. *See, e.g., id.*, [0035], Fig. 4C.

Shiraiwa discloses using much less costly non-SOI wafers instead of using expensive SOI wafers. *See, e.g., Shiraiwa*, [0021-0024], [0034], Fig. 3B. The non-SOI wafer must rely on a stopper other than oxide film 2, which does not exist in the non-SOI wafer. Shiraiwa states: “According to the semiconductor device of the present invention, ... a semiconductor substrate [is] ***thinned by an end point detection portion provided on the semiconductor substrate, without using an SOI substrate. Therefore, a low-cost ... device can be provided.***” *Id.*, [0023].

Thus, Shiraiwa’s point is a comparison between using expensive SOI wafers as opposed to much less costly non-SOI wafers. Shiraiwa does not compare the precision, cost, and variation of its non-SOI process (that use end point detection portion 42) with a competing non-SOI process. Lee is a non-SOI process since Lee makes no use or mention of using SOI wafers (and Petitioner has not argued that Lee uses SOI wafers). Therefore, Shiraiwa’s comparison of precision, cost, and variation is not applicable to Lee.

Petitioner’s other “reasons to combine” are also unavailing. The proposition that “both Lee and Shiraiwa describe wafer-scale backside-thinned device

fabrication” (Pet. 79) is not a reason to combine references. “[A] broad characterization of [prior art references] as both falling within the same alleged field ... without more, is not enough for [Petitioner] to meet its burden of presenting a sufficient rationale to support an obviousness conclusion.” *Securus Techs., Inc. supra.*

Further, the proposition that “POSAs would have used Shiraiwa because it gives more detailed process information on backside thinning than Lee” (Pet. 80) does not provide a reason to modify Lee’s backside thinning process. Lee discloses using “a grinding process, a chemical mechanical polishing (CMP) process, or an etching process” (Lee, [53]), none of which suggests or relies on using an end point detection portion. The “more detailed process information” provided in Shiraiwa is about using an end point detection portion, but such information would not be useful to Lee unless there was first a reason to replace or modify Lee’s process of grinding, or CMP, or etching with the end point detection process of Shiraiwa.

In fact, Shiraiwa’s use of end point detection portion 42 as a stopper adds much complexity in that a POSA would need equipment that “detects a change in the emission intensity of a specific wavelength of the plasma emission due to a

difference in material when the semiconductor substrate 22 is polished”

Shiraiwa, [0028]. The added complexity would deter a POSA from combining Shiraiwa with Lee, especially because Lee does not provide any reason or motivation for a POSA to modify its back side thinning process.

Lee describes: “After the first wafer is adhered to the second wafer, the back side of the first wafer is thinned to reduce the wafer thickness. In order to reduce the thickness of the back side of the first wafer, the back side of the wafer is processed by a grinding process, a chemical mechanical polishing (CMP) process, or an etching process performed on the back side surface of the wafer.” Lee, [53].

Lee does not attribute any special importance to the thinning action and does not indicate any particular goal the thinning action must achieve other than “to reduce the wafer thickness.” Lee especially does not disclose or suggest that exposing the photodiode from the back side is desirable or critical. Accordingly, Lee’s comment “to reduce the wafer thickness” would not have driven a POSA to seek out Shiraiwa’s fundamentally different process to fabricate and use end point detection portions for performing the thinning action, especially since Lee treats conventional processes such as grinding, or etching, or CMP as suitable.

Since it would not have been obvious to combine Lee and Shiraiwa, a combination of Lee and Masagaki and Shiraiwa would have also not been obvious for the reasons discussed above. Moreover, any purported combination of Lee and Masagaki and Shiraiwa would, at the very least, be missing steps [1.h.2] and [1.f].

IV. DEPENDENT CLAIMS 2 AND 4-9

Claims 2 and 4-9 depend from independent claim 1 and have added limitations that render them nonobvious for additional reasons not presented in this Preliminary Response.

V. THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION UNDER 35 U.S.C. §314(a)

As detailed below, the factors listed in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15, at 7-8 (May 13, 2020) (informative) favor discretionary denial under §314(a).

Factor 1: The “EDTX Proceeding” (*VisionX Tech., LLC. v. Sony et al.*, Case No. 2:22-cv-00178, filed May 26, 2022 (E.D. Tex.)) is ongoing before Magistrate

Judge Payne in the Eastern District of Texas.¹¹ Sony has not moved to stay the case pending the resolution of this IPR, nor is there evidence that such a stay would be granted. For example, in a recent denial issued by Judge Payne, the Court noted that the Supreme Court’s decision in *SAS Inst., Inc. v. Iancu*, 138 S.Ct. 1348 (2018), “precluded the PTAB from instituting only a portion of the patent claims, so any institution decision occurring after *SAS* provides a weaker inference that the PTAB will determine that all challenged claims are unpatentable.” *Peloton Interactive, Inc. v. Flywheel Sports, Inc.*, Case No. 2:18-cv-390, 2019 WL 3826051, at *5 (E.D. Tex. Aug. 14, 2019) (Payne, J.) (holding that “*SAS* alters the Motion to Stay analysis and makes institution decisions less indicative that all claims will be found unpatentable”); *see also Arbor Global Strategies LLC v. Samsung Elec. Co., Ltd.*, Case No. 2:19-cv-333, 2020 WL 6305883, at *3 (E.D. Tex. Aug. 10, 2020) (Payne, J.) (holding that a movant “may need to show that the

¹¹ During the parties’ scheduling conference on September 26, 2022, the Sony Defendants and Patent Owner consented to trial before the Magistrate Judge, further increasing the likelihood that the EDTX Proceeding will reach trial before the Board issues any final written decision. Ex. 2001 at 3.

Board is likely to invalidate every asserted claim—a showing that may require more than just pointing to a successful petition”).

Similarly, in evaluating motions to stay pending an IPR proceeding, Judge Payne also considers whether the Board has granted institution with respect to all asserted patents. *See Peloton Interactive, supra*, at *4 (noting that “the simplification factor weighed against a stay where the PTAB had not instituted IPR proceedings for all asserted patents”). In the EDTX Proceedings, Patent Owner has asserted three patents against Sony, each targeting different features of Sony’s CMOS image sensors. Each of the asserted patents are subject to a Petition for IPR filed by Sony: IPR2023-00296 (Patent 7,867,808); IPR2023-00298 (Patent 7,868,366); and IPR2023-00389 (Patent 8,035,143).

As a result, in order to prevail on a motion to stay, Sony would have to show not only that the Board is likely to invalidate every asserted claim, but that the Board is likely to invalidate every asserted claim from every asserted patent.

Accordingly, this factor favors denial of institution because Petitioner has not sought a stay pending outcome of any of the three IPRs, and evidence exists that the EDTX Proceeding Judge would not grant a stay even if institution were to occur, especially if institution does not occur for all three IPRs.

Factor 2: If the Board reaches its institution decision within three months of receiving the preliminary response, 35 U.S.C. §314(b), and issues a final written decision within 1 year of institution, 35 U.S.C. §316(a)(11), a final written decision would likely not issue until around late July 2024 - 4 months after the scheduled trial date of March 18, 2024 (Ex. 2002 at 1) and 2 months after the median statistics for the Eastern District of Texas suggest the trial would occur (Ex. 2006 at 35). As a result, a final written decision here is highly unlikely to issue early enough to avoid duplication or simplify any issues for trial. Thus, this factor favors denial.

Factor 3: The investment in the parallel proceedings is significant. In the EDTX Proceeding, the parties have exchanged discovery, including technical, marketing, and sales materials relating to Sony's CMOS image sensor products. Similarly, both infringement and invalidity contentions have already been served. Ex. 2003; Ex. 2004. The parties are also on the eve of the claim construction process, with deadlines for exchanging terms and proposed constructions coming up next month in May and claim construction briefing starting in July of 2023. Ex. 2002 at 4-5.

Factor 4: All of Sony’s asserted grounds in this proceeding are also part of its preliminary invalidity contentions in the EDTX Proceeding. *See* Ex. 2005 at 73 (Ground 1A: Iwabuchi), 73-74 (Ground 1B: Iwabuchi + Maruyama), 74 (Ground 1C: Iwabuchi + Suga¹²), 76 (Ground 2A: Lee + Masagaki + Shiraiwa¹³), 76 (Ground 2B: Lee + Masagaki + Shiraiwa + Maruyama), and 76 (Ground 2C: Lee + Masagaki + Shiraiwa + Tong¹⁴). Thus, instituting this proceeding would lead to entirely duplicative efforts here and in the EDTX Proceeding.

Petitioner Sony argues that this factor weighs against denial because it “stipulate[s] that, should the Board institute review, Petitioner will not rely in litigation on any invalidity grounds based on Iwabuchi and/or Lee (i.e. the primary references.) Pet. 107. However, such a narrow stipulation still favors exercising discretionary denial. As the Board noted in its precedential opinion in *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (Dec. 1, 2020), what is

¹² Sony lists Suga as a “Plasma Activation Reference.” *See* Ex. 2005 at 46-47.

¹³ Sony lists Shiraiwa as an “End Point Reference.” *See* Ex. 2005 at 45.

¹⁴ Sony lists the Tong as a “Plasma Activation Reference.” *See* Ex. 2005 at 46-47.

important is whether the “Petitioner broadly stipulates to not pursue ‘any ground raised *or that could have been reasonably raised.*’” *Id.* at 19.

Petitioner’s offer to conditionally litigate one set of invalidity theories in the PTAB and a separate set of invalidity theories in the EDTX Proceeding does little to provide an “inexpensive resolution of every proceeding.” *See* 37 C.F.R. §42.1(b). In fact, Petitioner’s approach simply increases the costs for all parties, creating a duplication of litigation rather than the desired “cost-effective alternative to litigation.” *See* 77 Fed. Reg. 48680-01 (Aug. 14, 2012).

Even worse, Sony’s narrow stipulation would not even cover another Iwabuchi reference that shares priority with Sony’s primary Iwabuchi reference. For example, Sony’s narrow stipulation applies only to the Iwabuchi reference in Ex. 1005 (the ‘007 Publication) and ignores the fact that Sony has also relied on Iwabuchi-‘762 (Ex. 1032). Both Iwabuchi references are related and claim priority to at least Japanese Patent Application No. 2005-163267. *See* Ex. 1005 at 1, and Ex. 1032 at 118. As a result, Sony’s stipulation, on its face, does nothing to avoid the duplication of issues in this IPR and the EDTX Proceeding.

Factor 5: As Sony concedes in the Petition, “Petitioner is a party to the Litigation.” Pet. 108. Under the Board’s precedential *Sotera* opinion, when the parties are the same, this factor supports denying institution. *Sotera, supra*, at 19.

Factor 6: As discussed above, the merits of this Petition are particularly weak. Iwabuchi (Grounds 1A, 1B, and 1C) clearly fails to disclose or make obvious at least step [1.e]. Lee+Msagaki+Shiraiwa (Grounds 2A, 2B, and 2C) clearly fails to disclose or make obvious at least steps [1.h.2] and [1.f]. Therefore, it is unlikely that Petitioner would prevail in its challenges to the claims.

Additionally, as mentioned above, Petitioner is pursuing two additional IPR petitions against the other asserted patents from the underlying litigation. As with the instant Petition, those Petitions are also particularly weak. For example, in IPR2023-00298, Patent Owner’s Preliminary Response illustrates how various claim elements are missing in each asserted ground. Similarly, in IPR2023-00389, Patent Owner’s Preliminary Response illustrates how various claim elements are missing in each asserted ground and, moreover, in contravention of 37 C.F.R. §42.104(b)(4), the Petition in IPR2023-00389 has not specified where each element of the challenged independent claim is found in the prior art relied upon.

On balance, the *Fintiv* factors favor discretionary denial.

VI. CONCLUSION

For at least the foregoing reasons, Patent Owner respectfully requests that the Board deny institution of *inter partes* review.

Respectfully submitted,

Date: April 25, 2023

/michael farjami/

Michael Farjami

Reg. No. 38,135

Lead Counsel for Patent Owner VisionX

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24, the undersigned certifies that the paper, Patent Owner's Preliminary Response, contains 13,887 words excluding a table of contents, a table of authorities, a certificate of service, a certificate of word count, or exhibit list, but including annotations added to figures. In making this certification, Patent Owner has relied on the word count feature of the word processing system used to prepare the paper, and manually adding the number of words present in annotations to figures.

Date: April 25, 2023

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CERTIFICATE OF SERVICE

I hereby certify that on April 25, 2023, copies of the foregoing PATENT OWNER'S PRELIMINARY RESPONSE and all documents filed with it were served via electronic mail, as agreed to by counsel, upon the following counsel for the Petitioner:

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