

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY GROUP CORPORATION,
Petitioner,

v.

VISIONX TECHNOLOGIES, LLC,
Patent Owner.

Case No. IPR20XX-00000
Patent No. 7,868,366

DECLARATION OF R. MICHAEL GUIDASH

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I. INTRODUCTION

1. I, R. Michael Guidash, have been retained by counsel to render certain opinions as an expert witness, for the above-referenced *inter partes* review (“IPR”) proceeding regarding U.S. Patent No. 7,868,366 (“’366 patent”). In connection with my analysis, I have reviewed the ’366 patent, the respective file history, and the documents listed in Section IV (which starts on page 7). I have been asked to provide a declaration regarding my opinions on the validity of claims 1-8 (the “challenged claims”) of the ’366 patent.

2. This declaration sets forth the opinions I have formed in this IPR and provides the bases and reasons for those opinions. I have summarized my educational background, professional experience, and publications herein and have attached my complete curriculum vitae, labeled as Exhibit 1004.

3. This report is based on information currently available to me. I declare that I have personal knowledge of the facts set forth in this declaration and, if called to testify as a witness, could and would do so competently.

4. I am being compensated at my usual consulting rate of \$600.00 per hour, plus actual expenses, for my work on this matter. My compensation is in no way dependent upon my opinions or testimony or the outcome of this proceeding.

II. SUMMARY OF OPINIONS

5. For reasons that I will address in more detail below, it is my firm belief and opinion that, at the time of the purported invention claimed by the '366 patent, the challenged claims would have been anticipated or obvious to a person having ordinary skill in the art ("POSA").

6. **Petition Ground 1:** Claims 1, 2, and 4-8 would have been obvious over Pyo in view of Choi because Pyo discloses the stacked design of those claims except that Pyo's metal lines (104) lack a conductive barrier layer. But Pyo discloses that its metal interconnections can be copper as an alternative to aluminum and the advantages of using copper interconnections in a CMOS sensor were well-known, Choi being one of many references disclosing such advantages. Choi also discloses how to implement copper interconnections in a CMOS sensor, including having metal interconnections on an interlayer dielectric and using a conductive barrier layer on the metal interconnections.

7. **Petition Ground 2:** Claim 3 would have been obvious over Pyo in view of Choi and Dublin because Dublin discloses that a cobalt tungsten phosphide ("CoWP") alloy as a barrier material that was preferred for copper interconnections.

8. **Petition Ground 3:** I understand that in *VisionX Technologies, LLC v. Sony Group Corporation et al.*, Case No. 2:22-cv-00178 (E.D. Tex.) (the "Texas

Litigation”), Patent Owner VisionX Technologies, LLC (“VisionX” or “Patent Owner”) alleges that a claim element may be “on” a corresponding claim element if the element is either above, adjacent to, or below the corresponding element. Under this claim interpretation, Imaoka’s sensor meets every element of claims 1-2 and 4-8, anticipating those claims.

9. **Petition Ground 4:** Under the claim interpretation noted in the preceding paragraph concerning Ground 3, claim 3 would likewise have been obvious over Imaoka in view of Dublin because Dublin discloses a CoWP alloy that was a preferred barrier material for copper interconnections.

10. **Petition Ground 5:** Even under a narrower interpretation of the term “on” than the one advanced by VisionX in the Texas Litigation, claims 1, 2, and 4-8 would have been obvious over Imaoka in view of Choi because Imaoka discloses that its via is formed from copper and also acknowledges copper as an alternative to aluminum for the remaining interconnections. Copper interconnections were long known to have performance advantages over aluminum. The dual-damascene process disclosed in Choi was a well-known method for incorporating copper interconnections and yielded a conductive barrier layer on copper interconnections on an interlayer dielectric.

11. **Petition Ground 6:** Claim 3 would have been obvious over Imaoka in view of Choi and Dublin because Dublin discloses a CoWP alloy that was a preferred barrier material for copper interconnections.

III. PROFESSIONAL BACKGROUND AND QUALIFICATIONS

12. A description of my professional background and qualifications is provided below. An additional account of my work experience and qualifications is included in my curriculum vitae, which is labeled as Exhibit 1004.

13. I started my career with Eastman Kodak as a product engineer for Photometer ASICs for Kodak film cameras after graduating with a Bachelor of Science in Electrical Engineering from the University of Delaware in 1981. In 1986, I transferred to the Kodak Research Laboratories and CCD wafer fabrication facility. During my time with the Kodak Research Laboratories and CCD wafer fabrication facility, I developed 2 micrometer (μm) and 1 μm CMOS processes, and a 30V 4 μm BiCMOS process. These processes were used for gate arrays for many Kodak products and output driver ASICs for all of Kodak's copiers. During this time, I was also awarded entrance into the Special Opportunity Graduate Program allowing me to obtain a Master's of Science in Electrical Engineering from the Rochester Institute of Technology.

14. In 1989, I transferred to the Smart Sensor Group, which developed BiCMOS-CCD processes to provide fully integrated CCD systems on a chip. I also

served as a product engineer and yield-enhancement engineer for Kodak's CCDs. During this time, I led product delivery and technology development of all ASIC and smart-sensor products. I developed a number of products during this time to include (1) an interline CCD integrated with 2 μ m CMOS on the same chip, (2) the world's first pinned-photodiode Active Pixel CMOS Sensor product, and (3) linear CCD image sensors with on-chip timing and control. I also led and directed the CCD dark current and point-defect reduction team.

15. In 1996, I formally started the CMOS Image Sensor group at Kodak. From 1996 to 2009, I managed the research and development and product development of CMOS Image Sensor (CIS) programs. As further shown in my curriculum vitae, I was the inventor or co-inventor of many key patents in the field of CMOS image sensors. The inventions of these patents include Pinned Photodiode Pixels, Camera-on-a-Chip architecture, and shared amplifier pixel architectures. During this time, I also led development of the world's first pinned-photodiode CIS product, a Megapixel CIS device, and a shared amplifier CIS pixel product. Further, I led development of the world's first half-inch optical format 1.3 megapixel CMOS image sensor for mass production, which was successfully implemented into several compact digital camera products. I also led the development of an early 3D hybrid stacked BSI CIS architecture. This led to

demonstration of very high performance, low-dark current BSI prototype sensors with pixel sizes ranging from 0.9 μm to 5.0 μm .

16. Much of my experience in CIS development was directed to working with various wafer foundry partners to modify their baseline CMOS process flows for use in manufacturing high quality CIS devices for Kodak. Wafer foundry partners included Motorola, Intel, Tower Semiconductor, IBM and TSMC. The process modifications included incorporation of additional process steps for formation of the photodetector structure, as well as modification of the metal interconnect processes to optimize optical performance.

17. One such project related to optical performance done with IBM from 2003-2005, was implementation of a thin copper (Cu) metallization. This project was directed to reducing the optical stack height of the CIS device so that the microlens in each pixel could be more effective at focusing light from a wide set of incident angles on the photodetector in the pixel. This was a key performance metric required for low-cost CIS devices used in cell phone cameras. The replacement of the standard aluminum-based metallization with Cu metallization enabled making the optical stack shorter without affecting the electrical and clock skew performance of the pixel array readout, due to the low resistivity of Cu. This project also included modification of the Cu barrier layer (from silicon nitride to a CoWP alloy), to reduce reflections in the dielectric stack above the photodiode in

order to increase the amount of light transmitted to the photodiode. A paper on this work was presented at the 2005 Advanced Metallization Conference, a copy of which is included as Exhibit 1023 (“Gambino”).

18. In late 2009, when Eastman Kodak closed its CMOS Image Sensor Business, I transitioned into a role as an intellectual-property technologist and coordinator. This role included managing the remaining image sensor patent applications and respective office actions, managing broad electronic components patent applications and respective office actions, and providing technical support for intellectual property sales and licensing teams.

19. In early 2012, I left Eastman Kodak and transitioned into a role of providing technical consulting services relating to CMOS image sensors. In this role I provide consulting services for process, pixels, circuits, sensor architectures, systems, and intellectual property to companies and clients.

IV. MATERIALS REVIEWED AND CONSIDERED

20. My findings, as explained below, are based on my years of education, research, experience, and background in the field of CMOS image sensors, as well as my investigation and study of relevant materials for this declaration. When developing the opinions set forth in this declaration, I assumed the perspective of a POSA, as set forth in Section VII (which starts on page 31).

21. In forming my opinions, I have studied and considered the materials identified in the list below and any other materials mentioned in this declaration.

Exhibit	Description
1001	U.S. Patent No. 7,868,366 (“ 366 patent ”)
1002	Prosecution history of the ’366 patent
1005	Certified English Translation of Korean Unexamined Patent Application Publication No. 10-2006-0077132 (“ Pyo ”)
1006	Certified English Translation of Japanese Patent No. 3800335 (“ Imaoka ”)
1007	U.S. Patent Publication No. 2005/0012166 A1 (“ Choi ”)
1008	U.S. Patent No. 5,695,810 (“ Dublin ”)
1009	U.S. Patent No. 6,576,550 (“ Brase ”)
1010	Reid, Jonathan, Chapter 16, Handbook of Semiconductor Manufacturing Technology, 2nd Ed., Doering, Robert et al. eds., (2008) (“ Doering ”)
1011	Declaration of Rachel J. Watters authenticating: Edelstein, D., et al., Full Copper Wiring in a Sub-0.25 μ m CMOS ULSI Technology, 1997 International Electron Devices Meeting Technical Digest, 773-776 (1997) (“ Edelstein ”)
1012	U.S. Patent No. 6,429,120 (the “’120 patent”)
1013	Declaration of Nathaniel E. Frank-White authenticating: Pratt, Annabelle, Overview of the Use of Copper Interconnects in the Semiconductor Industry (2004) (“ Pratt ”)
1014	Quirk, Michael and Julian Serda, Semiconductor Manufacturing Technology, 257-333 (2001) (“ Quirk ”)
1015	Certified English Translation of Japanese Unexamined Patent Application 2004-206377 (“ Yanagida ”)

Exhibit	Description
1016	Japanese Unexamined Patent Application 2004-206377 (original Japanese language version) ¹
1017	Certified English Translation of Korean Registered Patent 10-0664864 (“ Yun ”)
1018	Certified English Translation of Undated Response to a February 21, 2008, Office Action from the Korea Intellectual Property Office regarding Korean Patent Application No. 10-2007-0024914
1019	Certified English Translation of February 21, 2008, Office Action from the Korea Intellectual Property Office regarding Korean Patent Application No. 10-2007-0024914
1020	U.S. Patent No. 7.651,941 (the “’941 patent”)
1021	Complaint, <i>VisionX Technologies LLC v. Sony Group Corporation, et al.</i> , No. 2-22-cv-00178, Dkt. No. 1 (E.D. Tex. May 26, 2022)
1022	U.S. Patent Publication No. 2004/0245649 A1 (the “’649 Pub.”)
1023	Declaration of Seema Rampersad authenticating: Gambino, J., et al., Optimization of Cu Interconnect Layers for CMOS Image Sensor Technology, Conference Proceedings AMC XXI, 151-157 (2006) (“ Gambino ”)
1024	Yadid-Pecht, Orly and Ralph Etienne-Cummings (Eds.), CMOS Imagers: From Phototransduction to Image Processing, 75-139 (2004) (“ Yadid-Pecht ”)
1025	International Publication No. WO 2006/008637 A1
1026	Springer History, https://www.springer.com/us/about-springer/history (accessed October 12, 2022)
1027	Plaintiff’s Infringement Contentions, <i>VisionX Technologies LLC v. Sony Group Corporation, et al.</i> , No. 2-22-cv-00178 (E.D. Tex. Sept. 8, 2022)
1028	Certified English Translation of International Publication No. WO 2006/129762 A1 (“ Iwabuchi ”).

¹ While I relied on the certified English translation of Yanagida, not its original Japanese language version, I include the original in this list as a matter of completeness.

22. In this declaration, citations to issued patents are made by column and line number. Citations to patent application publications are made by paragraph number. Citations to all other exhibits are to the page number added by the exhibit label.

V. UNDERSTANDING OF APPLICABLE LEGAL STANDARDS

23. Although I am not an attorney, I have a general understanding of the applicable legal standards pertaining to the patentability issues presented in this proceeding based on my work experience both at Kodak and in my time as a consultant.

A. Burden of Proof

24. I understand that, in this IPR, Petitioner has the burden of proving that each challenged claim is unpatentable by a preponderance of the evidence. I understand that “preponderance of the evidence” means that a fact or conclusion is more likely true than not true.

B. Anticipation

25. I understand that one way a patent claim may be invalid is if it is “anticipated” by the prior art. I understand that, for a patent claim to be “anticipated” by the prior art, each and every limitation of the claim must be found, expressly, implicitly or inherently, in a single embodiment found in a prior art reference.

26. I understand that a claim limitation is implicit in a prior art reference if POSA understood the reference to disclose the limitation based on inferences that a POSA would reasonably be expected to draw from the express teachings in the reference when read in light of the POSA's knowledge and experience.

27. I understand that a claim limitation is inherent in a prior art reference if that limitation is necessarily present when practicing the teachings of the reference, regardless of whether a POSA recognized the presence of that limitation in the prior art.

C. Obviousness

28. I understand that a patent claim is unpatentable if, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of the prior art to yield the patent claim. I also understand that it is not required (although it is acceptable) that each element of a patent claim be found in a single reference in order to find a patent claim obvious. For a patent claim to be found obvious, all the elements of the patent claim may be found in a combination of references at which a POSA would have been reasonably expected to arrive. I understand that a proper analysis of whether an invention is unpatentable for obviousness includes a review of the scope and content of the prior art, the differences between the patent claims at issue and the prior art, the

level of ordinary skill in the field of the invention at the time of the invention, and other objective considerations identified below.

29. I understand that a showing of obviousness requires some articulated reasoning with a rational underpinning to support the combination of the references. I understand that in consideration of the issue of obviousness it is important to identify whether a reason existed at the time of the invention that would have led a POSA to combine elements of the references in a way that yields the claimed invention.

30. I understand that a claim may be considered unpatentable for obviousness for various reasons. I have been informed that the following exemplary rationales may support a finding of obviousness:

- A. combining prior art elements according to known methods to yield predictable results;
- B. simply substituting one known element for another to obtain predictable results;
- C. use of a known technique to improve similar devices in the same way;
- D. applying a known technique to a known device ready for improvement to yield predictable results;
- E. choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;

F. known work in a field that prompts variations in the work in the same or a different field that leads to predictable results; and

G. some teaching, suggestion, or motivation in the prior art that would have led a POSA to modify a prior art reference or combine multiple prior art references or teachings to arrive at the claimed invention.

31. I understand that various objective or “real world” factors may be indicative of non-obviousness. I understand that such factors include:

A. the commercial success of the claimed invention;

B. the existence of a long-felt, unresolved need for a solution to the problem solved by the claimed invention;

C. failed attempts to solve the problem solved by the claimed invention;

D. copying of the claimed invention;

E. unexpected results of the claimed invention;

F. praise for the claimed invention by others in the relevant field; and

G. willingness of others to accept a license under the patent because of the merits of the claimed invention.

D. Person of Ordinary Skill in the Art (“POSA”)

32. I understand that obviousness is determined from the vantage point of a POSA at the time of the alleged invention. I understand that a POSA is a

hypothetical person who is presumed to be aware of all pertinent prior art and the conventional wisdom in the art and is a person of ordinary creativity.

33. I understand that factors that may be considered in determining the level of ordinary skill in the art may include: (A) type of problems encountered in the art; (B) prior art solutions to those problems; (C) rapidity with which innovations are made; (D) sophistication of the technology; and (E) educational level of active workers in the field. In a given case, every factor may not be present, and one or more factors may predominate.

E. Claim Construction

34. I understand that, in IPR proceedings, claim terms in a patent are given their ordinary and customary meaning as understood by a POSA in the context of the entire patent and the prosecution history pertaining to the patent. I understand that when construing claim terms that are terms of art, that the claim term should be construed in a manner consistent with the scientific and technical context in which it is used in the patent. But, if the specification provides a special definition for a claim term that differs from the meaning the term would otherwise possess, the specification's special definition controls.

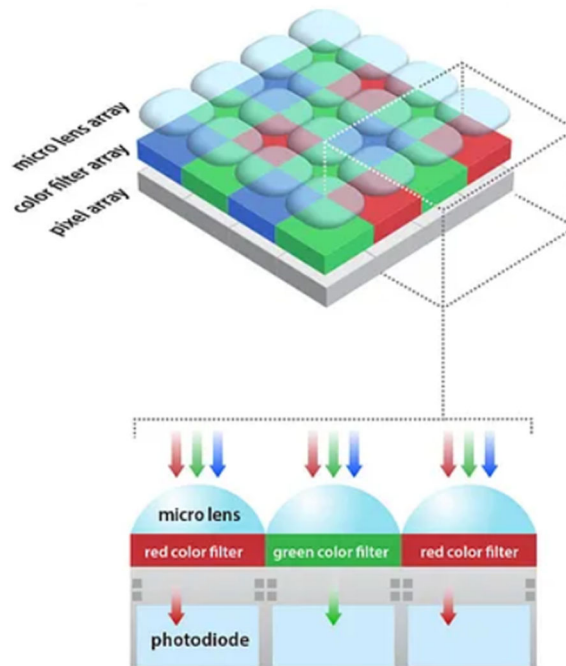
35. I have applied these standards in preparing the opinions in this declaration.

VI. TECHNOLOGY BACKGROUND

A. CMOS Image Sensors

36. The '366 patent relates to a CMOS image sensor. '366 patent, 1:14-28. CMOS stands for “Complementary Metal Oxide Semiconductor.” CMOS sensors are semiconductor image sensors that convert light into electrical signals.

37. In a CMOS sensor, light² enters the sensor – often through a microlens and a color filter – and is directed to a photodiode, illustrated below.



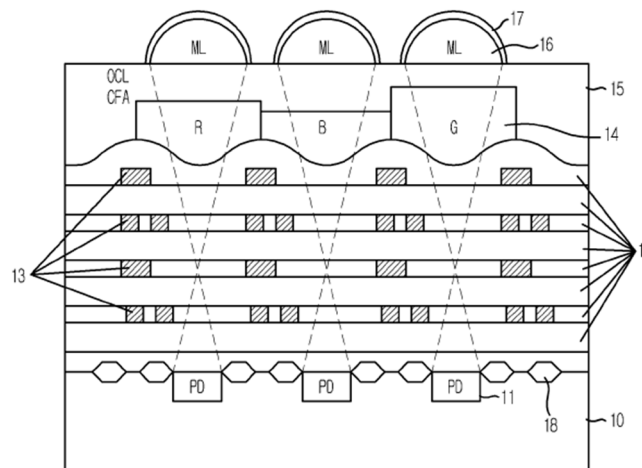
38. Each pixel site has a photodiode and when light is incident on it, it generates an electron-hole pair due to the photoelectric effect. Circuitry associated with each pixel site converts the charge to a voltage, which is amplified, and then

² Light is a type of electromagnetic radiation. In particular, “light” often refers to radiation that has a wavelength within the visible spectrum of about 380 nm to about 750 nm.

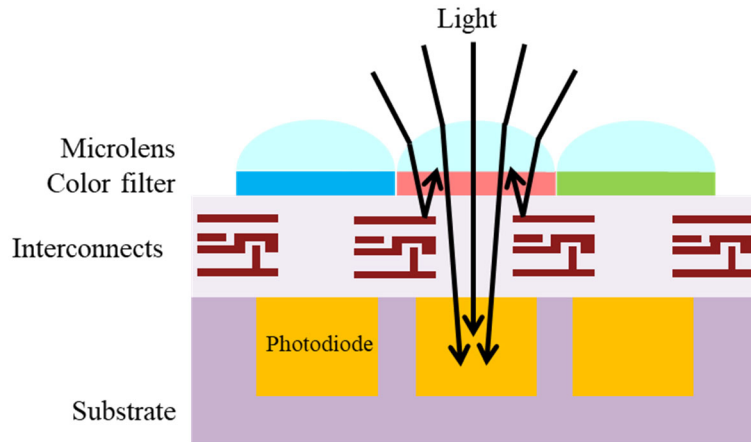
transmitted out of each pixel through a conductor to an output line by MOS transistor switches associated with each pixel. *See e.g.* Pyo (Ex. 1005), 4 (The “transistor comprises a reset transistor, a drive transistor, a select transistor, and the like; in the case of a structure comprising four transistors, a transfer transistor may be further comprised.”).

39. Metal interconnections conduct the voltage signal from the pixels to logic circuitry and/or to the sensor’s output interface. In one common type of front-side-illuminated sensor, the interconnections are located in between the photodiode and the color filter and microlens. Yun (Ex. 1017), Fig. 1 (original, below).

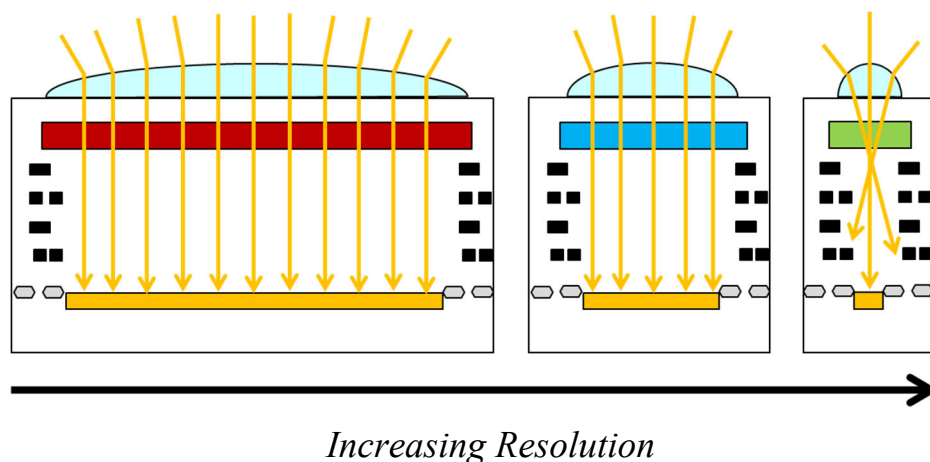
Yun, Fig. 1



40. The location of the interconnections in this location, however, can reflect or absorb some of the incident photons, reducing the number of photons that reach the photodiode as shown below.

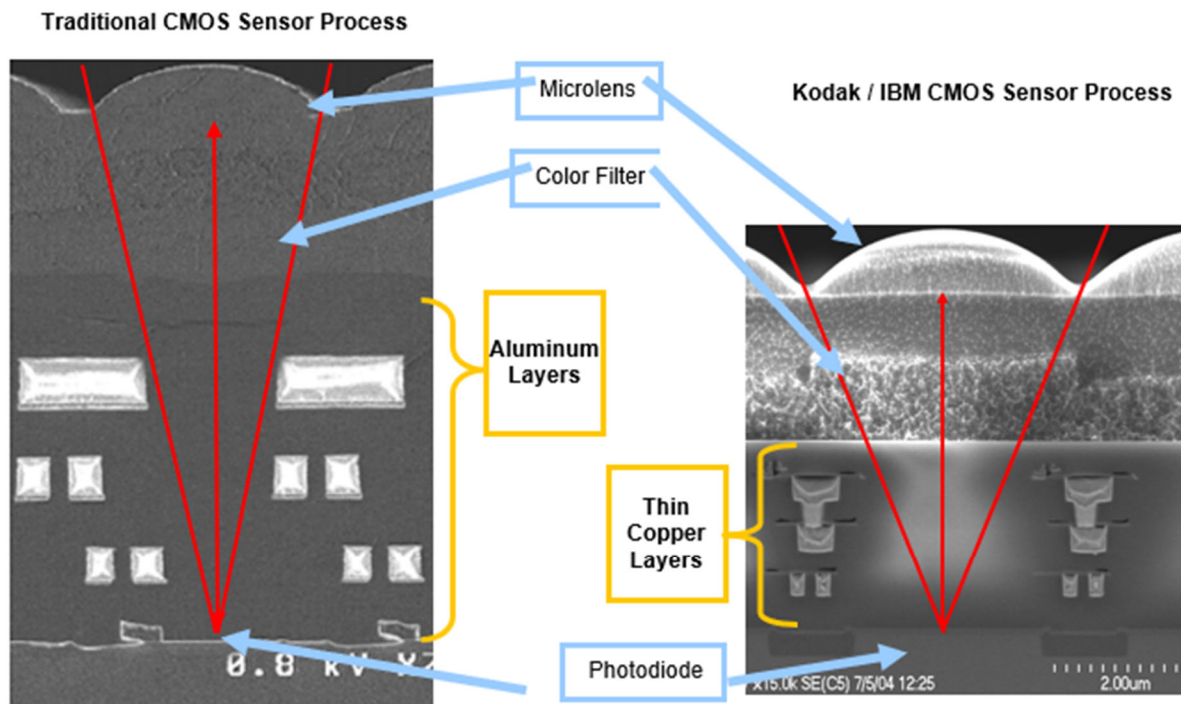


41. This was a known problem in the mid-2000s. For example, Yun disclosed this type of sensor design, stating that while “it is most ideal that the first incident light reaches 100% of the photodiode 11,” as “the size of the unit pixel is gradually reduced,” “the area ratio of the photodiode 11 per unit pixel is reduced to 30% or less.” Yun (Ex. 1017), 8. This phenomenon is illustrated in the figure below.



42. The presence of a microlens array helped focus more photons to the photodiode than a comparable sensor without a microlens array, but microlens arrays have limitations. Yun explains that “as the distance from the microlens 16 to

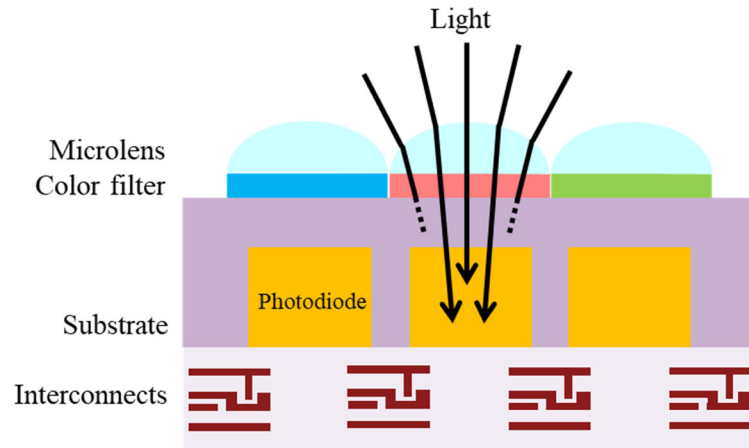
which the light is incident to the photodiode 11 increases, the focus is disturbed ... resulting in loss of light.” Yun (Ex. 1017), 8, Fig. 1. Pyo similarly discloses that “an increase in the distance from the photodiode to the color filter” “causes a decrease in light sensitivity.” Pyo (Ex. 1005), 2, Fig. 1. This phenomenon is illustrated in the figure below.



© Eastman Kodak Company, 2006

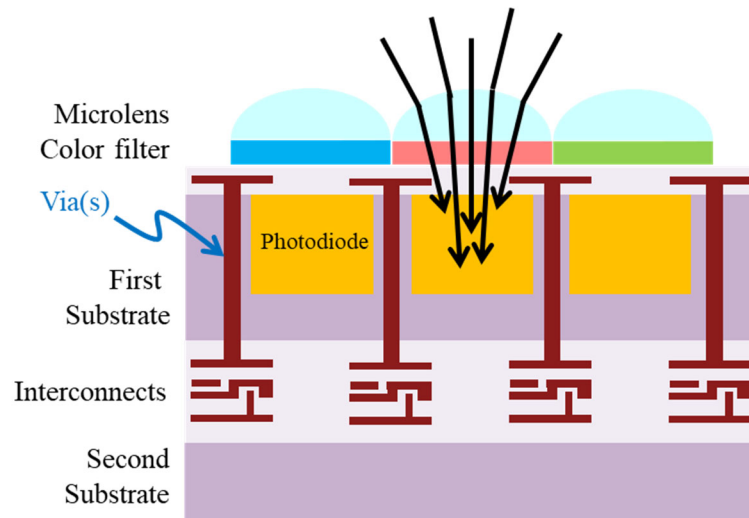
RM Guidash

43. One known solution to increase the CMOS sensor efficiency was to flip the CMOS sensor upside-down such that incident light entered from the back side of the silicon, relocating microlens array and color filters to the back side of the silicon substrate, as shown below.



In this sensor design, the incident light's optical path is shorter, and there are no metal interconnections in between the microlens and the photodiode, which allows a microlens array to better focus light on individual photodiodes. Yanagida discloses such an arrangement. Yanagida (Ex. 1015), Fig. 2.

44. A different known solution to increase the CMOS sensor light focusing efficiency was to relocate the metal interconnects required to form peripheral circuits to a separate substrate stacked underneath the first containing the photodiodes, shown below. In this configuration, the number of metal layers used in the pixel array substrate can be reduced by connecting electrical signals from the photodiode array to the interconnects on the second substrate through one or more conductive vias which are connected to column output lines and/or the peripheral circuits. This configuration combines an advantageously short optical path as illustrated in the figure below.



Pyo and a Japanese patent to Imaoka both disclose this stacked type of sensor. Pyo (Ex. 1005), Fig. 3; Imaoka (Ex. 1006), Fig. 3. As will be explained further below, the challenged claims also cover this stacked type of sensor, having a logic chip bonded to an imaging chip. '366 patent, Fig. 8.

B. Copper Interconnections

45. CMOS image sensors have much the same structure as other types of CMOS chips used in computers, such as memory chips. Yadid-Pecht (Ex. 1024), 30-31. Where memory chips employ multiple rows and columns of transistors to record and readout electrical data, CMOS image sensors contain rows and columns of photodiodes coupled with transistors to control the collection and readout of the electric signal in the photodiodes. Similar to the aforementioned standard CMOS devices, CMOS image sensors also have peripheral analog and digital circuits outside of the pixel array to perform timing and control, analog to digital conversion and other image processing functions. This means that CMOS image

sensors can be manufactured by modifying the same processes used to produce memories, microprocessors and other chips. *Id.*,³ 30 (“active pixel sensors (APS) are fabricated in a commonly used CMOS process”).

46. Aluminum, or aluminum-copper alloys, had historically been the dominant interconnect material in semiconductor manufacturing. Pratt (Ex. 1013), 5. Copper began to be used instead, due to a number of advantages over aluminum and aluminum-copper alloys as described further below.

47. **Lower resistivity.** A 2001 textbook by Quirk disclosed that “interconnect wiring resistivity reduces from 2.65 $\mu\Omega$ -cm for aluminum to 1.678 $\mu\Omega$ -cm at 20°C for copper, reducing RC signal delay.” Quirk (Ex. 1014), 59. A 1997 paper by Edelstein disclosed that “Cu wiring has advantages of significantly lower resistance.” Edelstein (Ex. 1011), 9. And a U.S. patent publication to Choi disclosed “copper having a low resistance, thereby minimizing problems.” Choi (Ex. 1007), [0139]. Other references similarly disclose copper’s low resistivity over aluminum. Pratt (Ex. 1013), 5-7; Doering (Ex. 1010), 4; Brase (Ex. 1009), 1:15-22.

48. **Reduction in power consumption.** Lower resistivity results in narrower lines, which have lower capacitance and can be driven by lower current

³ I understand that the abbreviation “*Id.*” is short for the Latin word “idem,” which means “the same” and is conventionally used to refer to the last citation to the record. I have adopted this convention in this declaration.

drivers, which “consume less power.” Quirk (Ex. 1014), 59. The Doering textbook disclosed that “the resistivity advantage of copper over aluminum ... allowed for smaller line dimensions.” Doering (Ex. 1010), 4-5. And Pratt discloses “copper results in a power consumption reduction of 30%.” Pratt (Ex. 1013), 8.

49. **Resistance to electromigration.** “Electromigration causes transport of the conductor material as a result of high current densities, which can ultimately lead to a void in the conductor.” *Id.* “[C]opper has ten to 100 times more resistance to electromigration failures than aluminum.” *Id.*; *see also* Quirk (Ex. 1014), 60; Doering (Ex. 1010), 5; Brase (Ex. 1009), 1:22-24.

50. **Fewer processing steps resulting in higher yields.** Narrower lines mean “interconnect routing can be simplified, reducing the number of interconnect levels and resulting in fewer process steps.” Pratt (Ex. 1013), 8; Doering (Ex. 1010), 5 (“the advantages of copper interconnects result in ... fewer interconnect metal levels”); Quirk (Ex. 1014), 82 (“Reducing process steps in wafer fabrication is important for improving the yield of the process, since fewer process steps translate to fewer sources of error that reduce assembly yield.”).

51. **Tighter packing density.** “Narrower lines permit tighter circuitry packing.” Quirk (Ex. 1014), 60. “As wafer fabrication design rules reduce to 0.15- μ m linewidths and below, the increased packing density ... leads to improved chip performance.” *Id.* One of the reasons tighter packing density leads to improved

CMOS image sensor performance is by reducing the dimensions of the circuitry, that increases the aperture to allow light to reach the photodiodes as shown in the figure following paragraph 42 (*see* page 18). Tighter circuitry packing is particularly important due to the industry's constant push to miniaturization, as shown in Table 1 of Pratt (Ex. 1013), reproduced below.

Table 1 Attributes of microprocessor chips at different technology nodes [3]

Year	2001	2003	2005	2007
Technology node	130 nm	100 nm	80 nm	65 nm
Transistors/chip	276 M	439 M	697 M	1106 M
Transistors/cm ² (including on-chip SRAM)	38.6 M	61.2 M	97.2 M	154.3 M
Chip size	3.1 cm ²	3.1 cm ²	3.1 cm ²	3.1 cm ²
Local wiring pitch	350 nm	245 nm	185 nm	150 nm
Number of metal layers	8	8	10	10
Total interconnect length (excluding global wiring)	7.8 mi	11.1 mi	17.5 mi	21.5 mi
Interconnect RC delay 1 mm line	86 psec	176 psec	256 psec	342 psec

52. These benefits of using copper interconnects were long recognized, but replacement of aluminum by copper in the early 1990s was an obstacle for semiconductor process engineers, since aluminum is deposited over the entire wafer surface and then patterned by reactive ion etching (RIE), and efforts to apply RIE to copper failed. Pratt (Ex. 1013), 8.

C. The Dual-Damascene Process

53. The breakthrough came in the later 1990s when the damascene and dual-damascene processes were invented and developed. The damascene processes started with a planar dielectric layer. The dielectric layer was first patterned and etched to form trenches and vias where the interconnects would be placed and

connected to an underlying layer respectively. Next, copper was used to fill in the trenches and vias in the dielectric. The first working microprocessor using copper was made by IBM in 1997 and by 1998 the process was used in high-volume manufacturing in IBM's Burlington, Vermont, facility. *Id.*

54. The invention and development of the damascene and dual-damascene processes was of great value because it was easier to manufacture copper lines and vias below about 0.13 to 0.10 μm than fabricating aluminum interconnects at that same narrow width. Choi discloses, for example, that “[w]hen manufacturing semiconductor devices having a pattern size less than about 0.13 μm , aluminum is no longer satisfactory as an electrical interconnection material.” Choi (Ex. 1007), [0007]. The Doering textbook disclosed “aluminum etch to circuit dimensions below 0.10 μm has been difficult.” Doering (Ex. 1010), 5.

55. Copper did not have this minimum width limitation. Choi discloses “multi-layered interconnections [using] copper having a low resistance, thereby minimizing problems, ... under a process condition having a design rule of about 0.13 micrometer.” Choi (Ex. 1007), [0139]. As early as 2004, semiconductor fabrication machinery manufacturers were offering tools for copper interconnect fabrication “extendable beyond the 65 nm node” and “[s]everal advanced chipmakers have announced breakthrough technologies down to 45 nm.” Pratt (Ex. 1013), 10.

56. The combination of the ease of fabricating narrow copper interconnects and the difficulty of fabricating aluminum interconnects of the same dimensions meant that “nearly all high performance logic devices have made the transition to copper, as of 2004.” Doering (Ex. 1010), 5. While that statement is directed primarily to CMOS chips used in computers, because CMOS image sensors were commonly made using similar fabrication machinery, using copper interconnections was the natural choice for CMOS image sensors as well in the same time period. Yadid-Pecht (Ex. 1024), 30-31 (noting image sensors “are fabricated in a commonly used CMOS process” and that the “continuous advances in CMOS technology for processors and DRAMs have made CMOS sensor arrays a viable alternative to the popular charge-coupled devices (CCD) sensor technology”); *see also id.*, 19 (“CMOS process development is funded by high-volume sales of standard CMOS logic and memory chips,” hence, “CMOS imaging technology does not have to bear the process development costs and consequently has cheaper process costs than CCD imagers.”).

57. For example, as explained in Section III (which starts on page 4, I was personally involved in work while at the Eastman Kodak Company to fabricate a 0.18 μm CMOS imager sensor that used three levels of copper interconnections. Gambino (Ex. 1023), 21. The CMOS imager sensor was fabricated using a 0.18 μm foundry process disclosed in 1999 with changes made only “to (1) optimize the

photodiode, (2) optimize the optical path through the dielectric stack, and (3) to add color filters and microlenses.” *Id.*

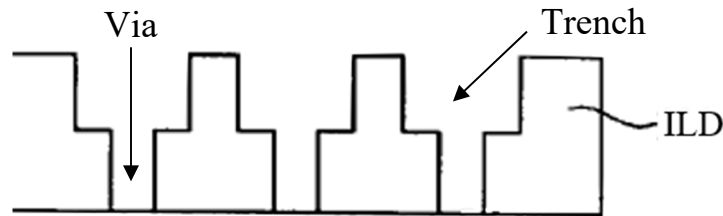
58. By at least 2001, the “dual-damascene process became the consensus process for copper metallurgy.” Quirk (Ex. 1014), 80; *see also* Pratt (Ex. 1013), 8-10 (“The damascene process has emerged as the industry standard.”); Doering (Ex. 1010), 4 (“A variation of the damascene process, known as the dual damascene process, has been widely implemented as the most cost-effective means of producing copper interconnect circuitry.”).

59. The dual-damascene process generally involves the following steps. *See* Quirk (Ex. 1014), 80-82 (describing the dual damascene process); Choi (Ex. 1007), Figs. 5A-5I, [0113]-[0134] (same).

1. Patterning Trenches and Vias in an Interlayer Dielectric (“ILD”)

60. The dual-damascene process begins with creating a pattern of trenches and vias in an inter-layer dielectric (ILD) layer, shown below. While there is some variation in how trenches and holes were formed (trenches then vias, vias first, or both simultaneously – *see* Quirk (Ex. 1014), 80-82; Brase (Ex. 1009), 1:47-2:10), regardless of that variation, the end result was the same.

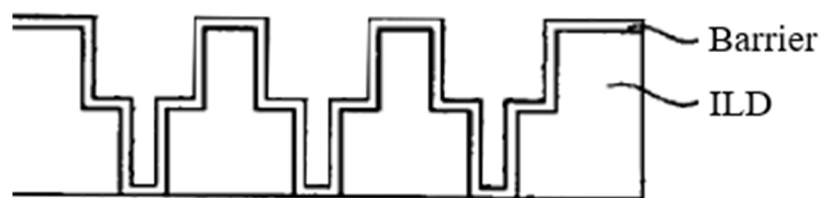
Formation of Trenches and Vias



2. First Metal Barrier Layer

61. The next step in the dual-damascene process is forming a metal barrier layer in the trenches prior to depositing copper. Such a “diffusion barrier layer . . . prevent[s] diffusion of the copper into surrounding materials.” Choi (Ex. 1007), [0008]; *see also id.*, [0126] (A “barrier *metal* layer 203 is formed along a profile of the first trench and the first via to cover the second insulating interlayer 190.”),⁴ Fig. 5E. The figure below illustrates such a barrier layer, which is made of metal to minimize resistivity Quirk (Ex. 1014), 62, *see also id.* 81 (“7. Deposit barrier *metal*”).

Deposition of Barrier Layer



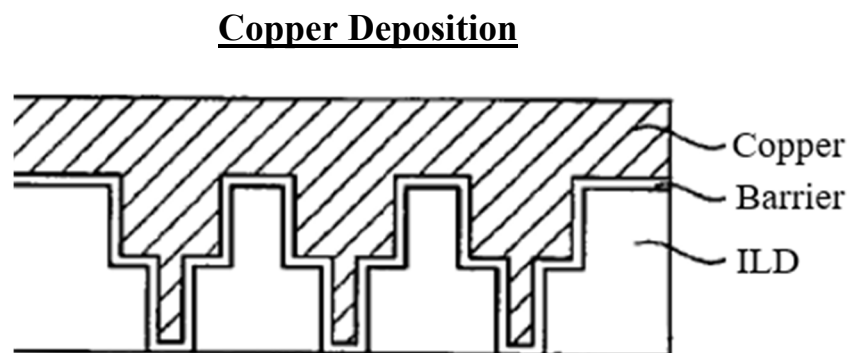
62. As early as 1997, a “variety of materials [were] known for forming diffusion barriers on copper.” Dublin (Ex. 1008), 2:25-28. Such materials included

⁴ Emphasis added unless otherwise noted.

tungsten (W) and tungsten nitride (WN) (Choi (Ex. 1007), [0071]), tantalum (Ta) and tantalum nitride (TaN) (*id.*, [0066]), and others such as titanium tungsten alloy (TiW) (Dublin, 2:25-28). *See also* Quirk (Ex. 1014), 62-63 (listing copper barrier metals). Of the known barrier materials, cobalt tungsten phosphide alloy (CoWP) was known to “significantly enhance[] the barrier properties” and was “preferred since copper can be electrolessly deposited on CoWP without the need for activation of the CoWP material surface for fabricating subsequent layers of lines and vias. Dublin, 3:1-7. Such CoWP barrier materials were used for copper interconnections in CMOS image sensors as well. Gambino (Ex. 1023), 25.

3. Copper Deposition

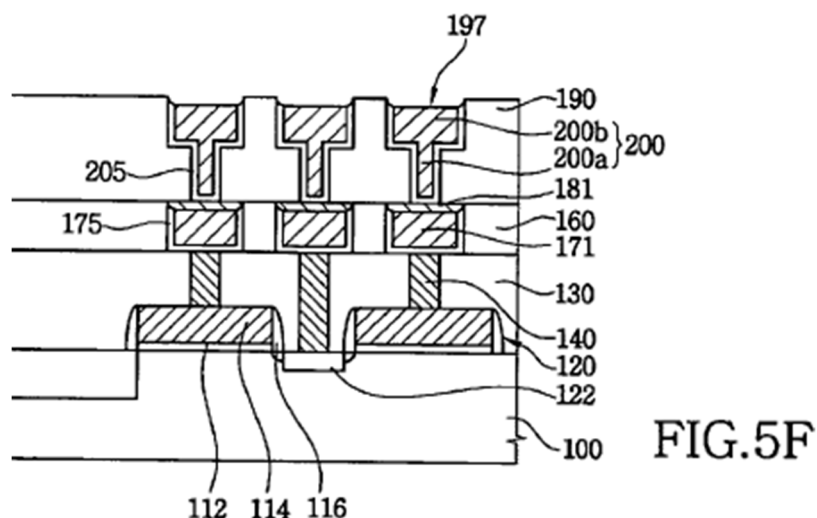
63. Next, copper is formed on the barrier metal layer to fill the trench and the via, as shown below. Choi (Ex. 1007), [0126], Fig. 5E; Quirk (Ex. 1014), 80-82; Pratt (Ex. 1013), 10.



4. Chemical Mechanical Planarization (“CMP”)

64. Next, a portion of the copper is removed using a method such as CMP to create space for an additional metal barrier layer to prevent the copper from

diffusing. For example, Choi discloses using CMP to create a recess (197) for a second barrier layer, as shown in Figure 5F of Choi (excerpt reproduced below). Choi (Ex. 1007), [0128], Fig. 5F; *see also* Yun (Ex. 1017), 13 (“excessive polishing is performed so that the copper layer 313 and the third barrier layer 312 filled in the upper trench are recessed”), Fig. 3i.

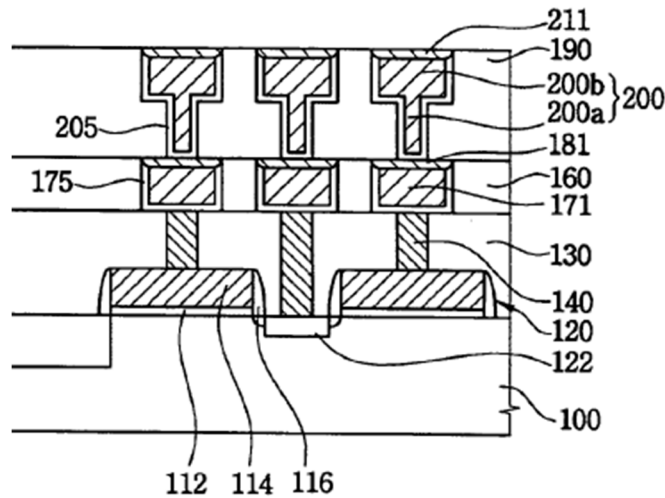


5. Second Metal Barrier Layer

65. The above-noted CMP creates space for another barrier (i.e., “encapsulation”) layer using a high corrosion resistance material, which is necessary to prevent the copper interconnect from oxidizing and thereby degrading performance. Dublin (Ex. 1008), 2:16-24 (“The oxidized copper degrade[s] the electrical and mechanical properties of the copper interconnect” and, accordingly, “a protection (or encapsulation) layer of high corrosion resistance material is necessary on the copper surface.”). The top surface of the copper is thus covered with a barrier layer that sits flush with the top surface of the dielectric. *Id.*, Fig. 10;

Choi (Ex. 1007), [0129], Fig. 5G (excerpt below). The top barrier layer made is preferentially of a metal such that it need not be subsequently removed in subsequent processing. Choi (Ex. 1007), [0082] (when the top barrier layer “includes a conductive metal,” it “will not interfere with the electrical connection” and need not be removed), [0125] (but when the top barrier layer is an insulator, it would need to be removed to make an electrical connection).

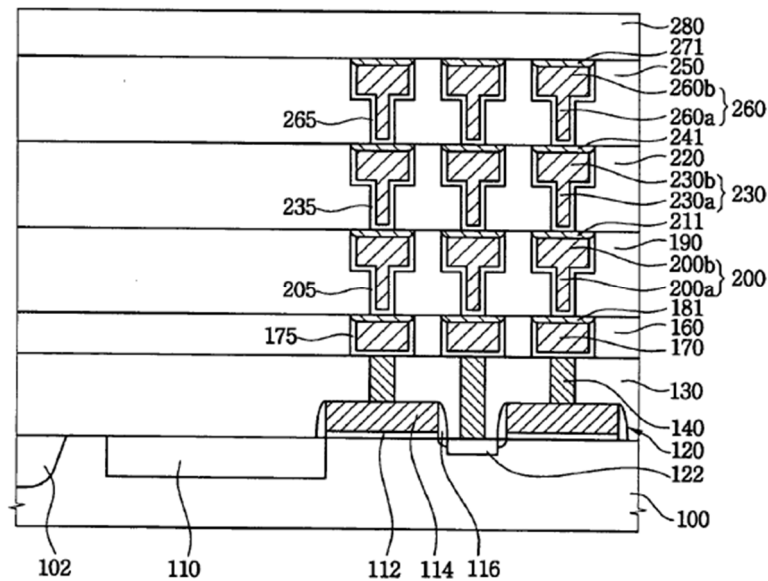
FIG.5G



6. Repeat (Optional)

66. If desired, the above-described process can be repeated for subsequent and additional layers of lines and vias. Choi (Ex. 1007), [0130], Fig. 5H (below).

FIG.5H



VII. PERSON OF ORDINARY SKILL IN THE ART (“POSA”)

67. For the purposes of my declaration, I have assumed that the relevant priority date of the '366 patent is March 14, 2007, the date of the earliest filed application to which the '366 patent claims priority. However, my views expressed herein would not change even under an alleged invention date of up to a year earlier.

68. I worked in the relevant field as described above with such persons of ordinary skill in the art at, and leading up to, the time of the alleged invention of the '366 patent and I am thus familiar with the knowledge and skills that a POSA had at the time.

69. Based on my knowledge, training, skill, academic and commercial experience, and my review of the '366 patent, a POSA as of the claimed priority date would have had at least a Bachelor's degree in electrical engineering, physics, microelectronics, or material science and approximately 3-5 years of industrial experience or equivalent research or teaching experience, or a Master's degree in the same fields and 1-3 years of industrial experience or equivalent research or teaching experience in the field of semiconductor image sensor design and fabrication. The levels of education, experience and knowledge can trade off against one another.

70. By 2007, I had over twenty years of experience with CMOS sensor design and fabrication. Therefore, I was a person of more than ordinary skill in the art during the relevant timeframe. However, I worked with many people who fit the characteristics of the POSA, and I am familiar with their level of skill. When developing the opinions set forth in this declaration, I assumed the perspective of a person having ordinary skill in the art, as set forth above.

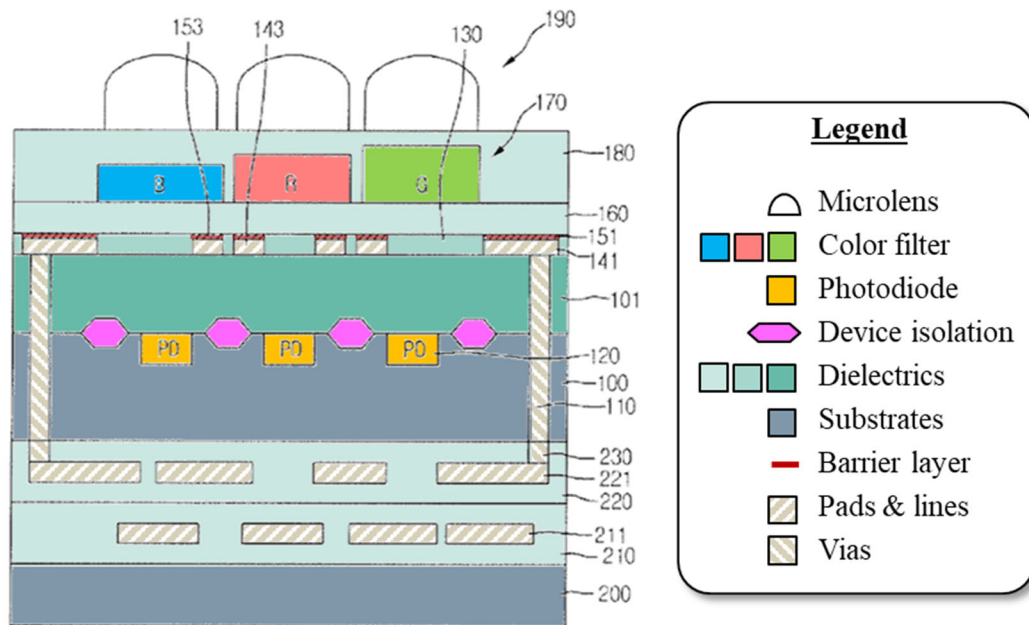
VIII. THE '366 PATENT

71. The '366 patent was filed on March 14, 2008, and claims the benefit of Korean application filed on March 14, 2007 (KR 10-2007-0024914) ("KR '914"). I have been asked to assume, for purposes of this declaration, that the '366 patent is entitled to a priority date of March 14, 2007.

A. Described Embodiments

72. The '366 patent discloses a CMOS image sensor, a cross-sectional view of which is shown in Figure 8, to which I have annotated below.

'366 patent, Fig. 8 (Annotated)



73. The '366 patent discloses that the photodiodes in the pixel region of the disclosed embodiment are connected to the interconnections on the first substrate by “a contact (not shown).” '366 patent, 2:43-44. The interconnections are in turn connected to the first via, which penetrates down though both the pre-metal dielectric and the first substrate to be exposed at the bottom surface of the first substrate. *Id.*, 2:35-43. The interconnects on the second substrate are also electrically connected using a via. *Id.*, 3:26-31. The second substrate is then bonded to the underside of the first, allowing the signal to pass through the

exposed first via down into the interconnects of the second substrate through the second via. *Id.*, 2:63-67, 3:1-4.

B. Prosecution of the Korean Priority Application

74. The '366 patent's Korean priority application, KR '914, was filed with 15 claims. Ex. 1018, 4-8. Claims 1-6 were directed to an image sensor and claims 7-15 were directed to a method of manufacturing an image sensor. *Id.*

75. On February 21, 2008, the Korean examiner rejected claim 1 because it was "similar to the configuration in [Pyo]." Ex. 1019, 2-3. The Korean examiner identified only one difference, "the conductive barrier film on the metal wiring," but noted that "this is commonly used in this field," citing a Japanese application "in which a barrier metal is formed on the wiring layer." *Id.*, 3. The Korean examiner similarly rejected dependent claims 2-6 because "these limitations limit simple materials or are merely structural changes, and it is not technically difficult to apply these limitations." *Id.* The Korean examiner thus rejected the sensor claims over Pyo in view of commonly used barrier layers.

76. Claims 1-5 rejected by the Korean examiner (as translated into English in a certified English translation) were substantially the same as claims 1 and 3-5 of the '366 patent as shown in the below comparisons. *Comparing* Ex. 1018, 4-5 *with* Ex. 1001 ('366 patent).

KR '914 Claim 1	'366 patent Claim 1 ⁵
An image sensor, comprising the following:	[1.pre] An image sensor, comprising:
a first semiconductor substrate on which a pixel and a first via are formed;	[1.3] a first semiconductor substrate on the second interlayer dielectric, the first semiconductor substrate having a unit pixel; [1.5] a first via penetrating the pre-metal dielectric and the first semiconductor substrate, the first via being connected to the second via;
an interlayer insulating film comprising a metal wiring and a conductive barrier film formed on the first semiconductor substrate;	[1.4] a pre-metal dielectric on the first semiconductor substrate; [1.6] a first interlayer dielectric on the pre-metal dielectric including the first via; [1.8] a conductive barrier layer on the first metal interconnection;
metal wiring, comprising a color filter array and a microlens formed on the interlayer insulating film so as to be connected to the first via exposed through the rear surface of the first semiconductor substrate; and	[1.7] a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel; [1.9] a color filter and a microlens on the first interlayer dielectric on the unit pixel.

⁵ I have applied the same labels to the elements of claim 1 of the '366 patent as I have in the claim listing in Appendix A.

KR '914 Claim 1	'366 patent Claim 1⁵
a second semiconductor substrate on which an interlayer insulating film comprising a second via is formed.	[1.1] a second semiconductor substrate including a second metal interconnection and a second interlayer dielectric; [1.2] a second via penetrating the second interlayer dielectric so that the second via is connected to the second metal interconnection;

KR '914 Claim 2	'366 patent Claim 1
The image sensor according to Claim 1, wherein the conductive barrier film of the first semiconductor substrate is formed only on the metal wiring.	[1.8] a conductive barrier layer on the first metal interconnection;

KR '914 Claim 3	'366 patent Claim 3
The image sensor according to Claim 1, wherein the metal wiring of the first semiconductor substrate is formed of copper, and the conductive barrier layer is formed of a cobalt (Co) or nickel (Ni) alloy.	The image sensor according to claim 1, wherein the conductive barrier layer comprises cobalt (Co) or nickel (Ni) alloy.

KR '914 Claim 4	'366 patent Claim 4
The image sensor according to Claim 1, wherein the metal wiring of the first semiconductor substrate is formed lower than the interlayer insulating layer to have a step difference with the interlayer insulating layer.	The image sensor according to claim 1, wherein the first metal interconnection has a top surface lower than that of the first interlayer dielectric, such that the first metal interconnection and the first interlayer dielectric have a height difference.

KR '914 Claim 5	'366 patent Claim 5
The image sensor according to Claim 1, wherein the metal wiring of the second semiconductor substrate is formed of copper (Cu) or aluminum (Al).	The image sensor according to claim 1, wherein the second metal interconnection comprises copper (Cu) or aluminum (Al).

77. While the Applicant amended the method of manufacturing claims 7-15 to overcome the rejection, the Applicant canceled (“deleted”) the sensor claims 1-6 without responding to the Korean examiner’s arguments rejecting them. Ex. 1018, 4-8.

C. Prosecution of the '366 Patent

78. The application that led to the '366 patent was filed on March 14, 2008 – three weeks after the Korean examiner had rejected substantially similar claims in the Korean prosecution on February 21, 2008. The Applicant filed an Information Disclosure Statement (“IDS”) listing Pyo and provided an English-language translation of the Pyo abstract, but submitted the entire Pyo reference

only in the original Korean. Ex. 1002, 29-39, 53-54. The Applicant did not submit a copy of the Korean examiner's rejection or the Applicant's cancelation of the sensor claims.

79. The English translation of the Pyo Abstract attached to the IDS fails to expressly disclose several elements the are disclosed by Pyo, including at least, (1) a first and a second interlayer dielectric (limitations [1.1] and [1.6]), (2) a pre-metal dielectric (limitation [1.5]), (3) a first metal interconnection (the abstract only discloses metal lines on the second substrate) (limitation [1.7]), and (4) a color filter (limitation [1.9]). *Id.*, 30.

80. Apparently unaware of the significance of Pyo and without the Korean examiner's rejection as a guide, the U.S. Examiner allowed the challenged claims without rejection over any prior art. *Id.*, 97-104.

D. The Challenged Claims

81. I provide in Appendix A, attached hereto, a listing of claims 1-8 of the '366 patent. I will refer throughout this declaration to the elements of the claims with reference to the number and letter designations that have been added in the left column (e.g., "[1.pre]," "[1.1]," "[1.2]," etc.).

IX. ORDINARY AND CUSTOMARY MEANING OF CERTAIN TERMS

82. I have been asked to consider the terms found in the challenged claims of the '366 patent based on how those terms would have been understood by a

POSA at the time of the alleged claimed invention in March 2007, consistent with my understanding of the legal framework explained in Section V.E (*see* page 14). I have applied the constructions provided below in my analysis and in forming my opinions.

A. “On” – Claim 1

83. Claim 1 requires that various elements of the image sensor be “on” other elements. The ’366 patent states: “When the terms “on” or “over” are used herein, when referring to layers, regions, patterns, or structures, it is understood that the layer, region, pattern or structure can be directly on another layer or structure, or intervening layers, regions, patterns, or structures may also be present.” ’366 patent, 2:17-22.

84. The elements of the image sensor disclosed by the ’366 patent plainly conform to the positional relationship claimed by claim 1 except the “first metal interconnection” (limitation [1.7]), which claim 1 requires to be “on” the first interlayer dielectric, and which appears to be more nuanced, as explained below.

85. In describing the embodiment shown in Figure 8, the ’366 patent states that the “[f]irst and second metal interconnections 141 and 143 can be disposed on the first interlayer dielectric 130.” *Id.*, 2:40-44. But Figure 8 does not depict any portion of the first and second metal interconnections 141 and 143 being above the first interlayer dielectric 130.

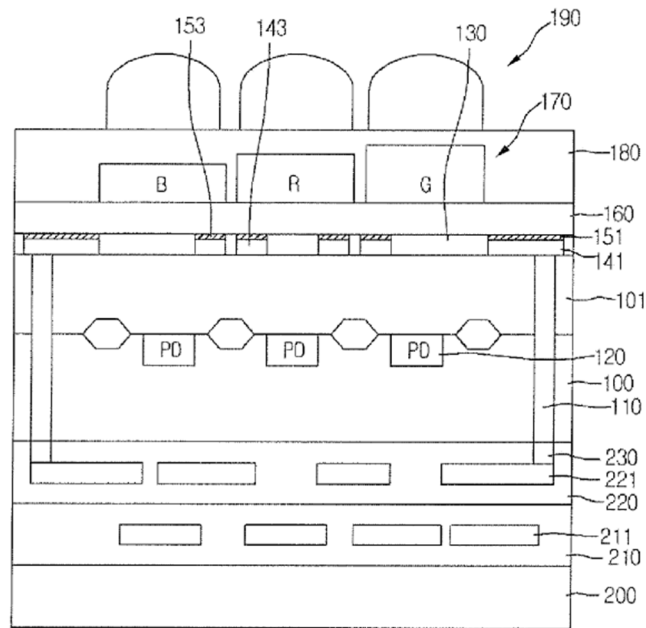


FIG. 8

86. This is in contrast to Figure 5 (reproduced below), which shows a portion of the interconnection 143 that is above a portion of the interlayer dielectric 130, making the interconnection 143 undisputedly “on” the interlayer dielectric 130. But the ’366 patent states: “FIG. 5 is illustrated for explaining the *method* for forming the metal interconnection and *should not be construed as limiting*” and that the “trench may be formed in various shapes through a single or dual Damascene process.” *Id.*, 4:52-55.

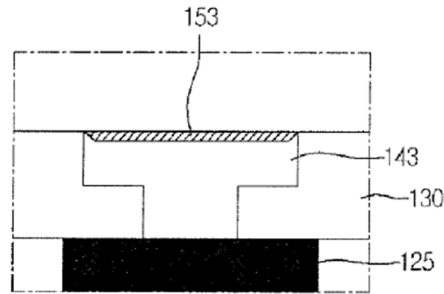
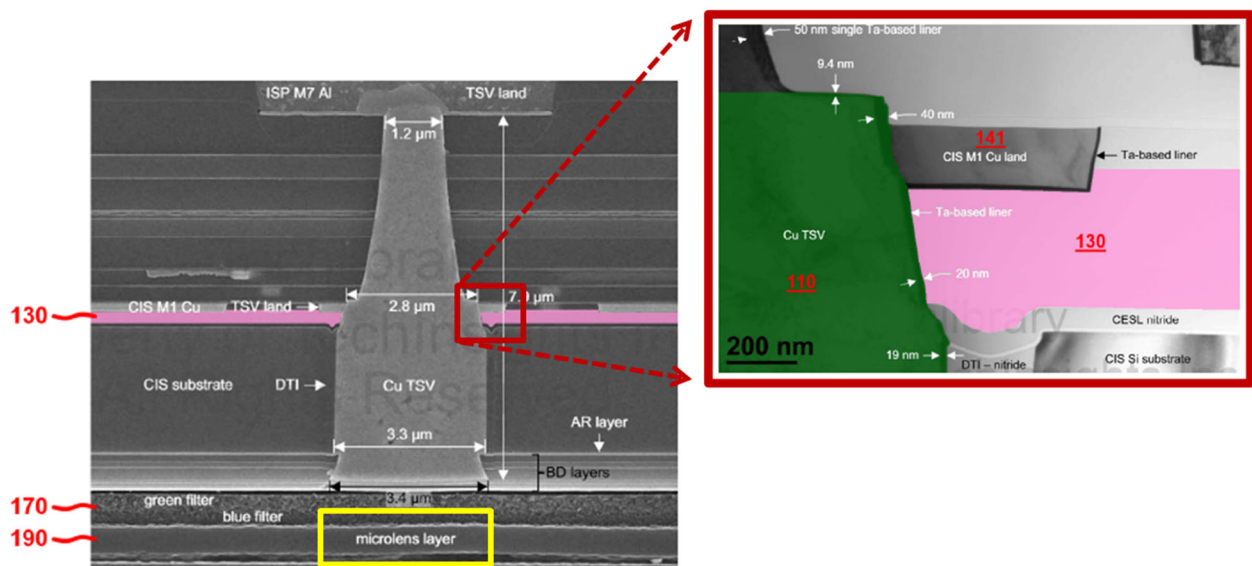


FIG. 5

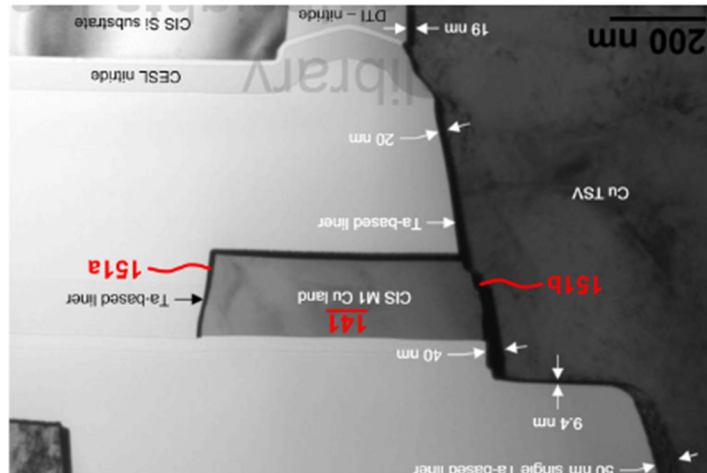
87. I understand that the Patent Owner, VisionX, has interpreted the term “on” broadly in the co-pending Texas Litigation. To show this, I first note that VisionX's complaint from the Texas Litigation depicts an accused product with the microlens layer at the bottom of the image (see yellow annotation, below). Ex. 1021, 35-36. This represents a 180-degree different orientation than the orientation of Figure 8 of the '366 patent, which has the microlens facing up.



88. Viewing the images from the VisionX complaint in the same orientation as Figure 8 of the '366 patent, it is apparent that VisionX alleges that interconnection 141 is “on” alleged interlayer dielectric 130 even though interconnection 141 is partly adjacent to and partly below the first interlayer dielectric, with no part of the interconnection 141 above the dielectric 130. *Id.*, 35 (below, re-orientated to match that of Figure 8 of the '366 patent).



89. Patent Owner alleges barrier layer (151a and 151b) is above, and thus “on” the alleged interconnection (141) as claimed by limitation [1.8]. *Id.*, 36 (below, re-orientated to match that of Figure 8 of the '366 patent).



90. I have thus assumed for the purposes of my opinions in this declaration that VisionX’s interpretation of “on” is correct and that an element is “on” a corresponding element when the element is above, adjacent to, or underneath the corresponding element. But, as I explain in further detail below, the challenged claims are invalid over the prior art even under a narrower interpretation of the term “on” requiring an element to be at least in part above a corresponding element (in reference to the orientation shown in Figure 8 of the ’366 patent).

B. “Interconnection” – Claim 1

91. Claim 1 requires both a first and second metal “interconnection.” The ’366 patent does not define this term, but it is a term of art that “describes the conductor materials, ... that create the metal wiring that carries electrical signals to different parts of the chip.” Quirk (Ex. 1014), 54. Such conductor materials broadly includes: (i) “lines” that extend parallel to the top surface of the silicon

chip; (ii) “vias” that are holes filled with a metal plug that “form an electrical pathway” from one metal layer to another; and (iii) contacts (a.k.a. pads) formed at the surface of the semiconductor structure. *Id.*; *see also* Brase (Ex. 1009), 1:40-45.

92. The ’366 patent uses the term “interconnection” consistently with its meaning in the art because, for example, in claim 1, (i) the first metal interconnection is connected to the unit pixel and the first via to carry a signal from the unit pixel to the first via and (ii) the second metal interconnection is connected to the second via to carry a signal to or from the second via to different parts of the chip.

C. “Interlayer Dielectric” – Claim 1

93. Claim 1 requires both a first and second “interlayer dielectric.” The ’366 patent does not define this term, but it is a term of art that means “an insulating film between two conducting metals or adjacent metal lines.” Quirk (Ex. 1014), 14.

94. The ’366 patent uses the term “interlayer dielectric” consistently with its meaning in the art because, for example, as seen in Figure 8 of the ’366 patent, (i) the first interlayer dielectric 130 electrically insulates the space between the first and second metal interconnections 141 and 143, which are adjacent metal lines, and (ii) the second interlayer dielectric 210 electrically insulates the space between

the plurality of metal interconnections 211, both between layers and between adjacent metal lines. '366 patent, 2:32-44, 3:10-14, Fig. 8.

D. “Via” – Claim 1

95. Claim 1 requires both a first and second “via.” The '366 patent does not define this term, but it is a term of art that means a specific type of interconnect defined by a hole that is filled with a metal plug to “form an electrical pathway” from one metal layer to another. Quirk (Ex. 1014), 54; *see also* Brase (Ex. 1009), 1:40-45.

96. The '366 patent uses the term “via” consistently with its use in the field as referring to an interconnection that forms an electrical pathway from one metal layer to another. For example, claim 7 requires “the first via and the second via comprise *the same material*.” Of course, a hole would not comprise any material, and so claim 7 must be referring to the conductive material of the via.

97. The specification of the '366 patent uses the term “via hole” when referring to the hole and “via” when referring to the conductor. '366 patent, 3:65-4:6 (“in order to form the first via 110, ... a *via hole* is formed by etching the PMD 101 and the first semiconductor substrate 100 using the photoresist pattern as an etch mask” and a “metal layer can be deposited on the PMD 101 to gap-fill the via hole, and then *the metal layer can be planarized to form the first via 110*.”). The specification of the '366 patent also describes the vias as providing electrical

connections, which require a conductor. *Id.*, Abstract (“the first via being *electrically* connected to the second via”), 1:42-44 (“first via penetrating the pre-metal dielectric and the first semiconductor substrate to *electrically* connect with the second via”), 2:65-3:4 (“The second via 230 is disposed under the first via 110 and can be *electrically* connected to the first via 110. That is, the first semiconductor substrate 100 and the second semiconductor substrate 200 can be *electrically* connected together through the first via 110 and the second via 230”).

98. I understand that VisionX has taken the position in the co-pending Texas Litigation that Petitioner’s accused product meets the claimed first and second vias with a single thru-silicon via (“TSV”). Ex. 1021, ¶¶ 64-66, Fig. 6 (reproduced below, annotated).

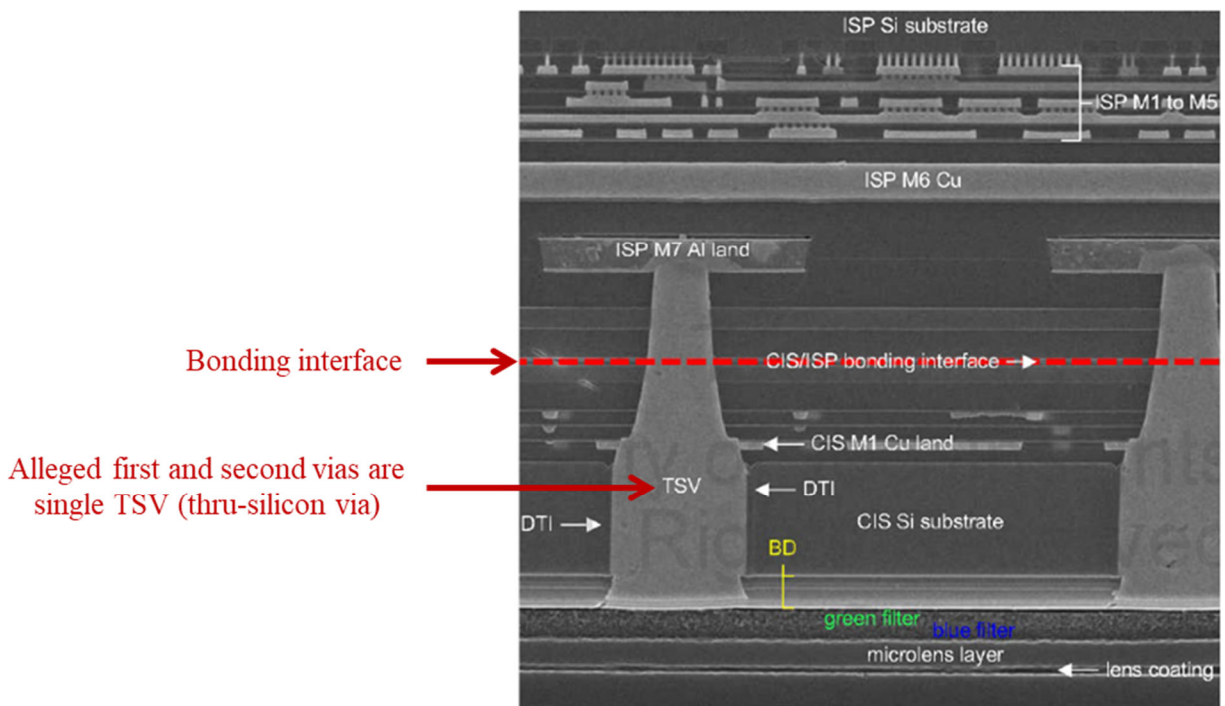


Figure 6

99. Indeed, Patent Owner asserts that claims 1, 2 and 4-8 of the '366 patent are infringed by “any back-illuminated and stacked CMOS image sensors utilizing TSVs.” Ex. 1027, 3.

100. I have assumed for the purposes of my opinions in this declaration that the Patent Owner is correct that a single via may meet the requirements of both the first and second vias if the single structure otherwise meets the claimed requirements of each. But, as I explain in further detail below, the challenged claims are invalid over the prior art even if two vias are required to meet the first and second vias as claimed.

E. “Pre-Metal Dielectric” – Claim 1

101. Claim 1 requires a “pre-metal dielectric.” The '366 patent does not define this term, but it is a term of art. “The dielectric layer between the active devices in silicon and the first metal layer ... is also called the *premetal dielectric (PMD)*.” Quirk (Ex. 1014), 13 (italics in original).

102. The '366 patent uses the term “pre-metal dielectric” consistently with its meaning in the art because, for example, claim 1 requires the first semiconductor substrate have a unit pixel (which is where the active devices are located), the pre-metal dielectric is located on the first semiconductor substrate, and the first metal interconnection is located on the pre-metal dielectric. Thus,

claim 1 requires the pre-metal dielectric to be located in between the active devices in the first semiconductor substrate and the first metal interconnection.

X. PRIOR-ART REFERENCES

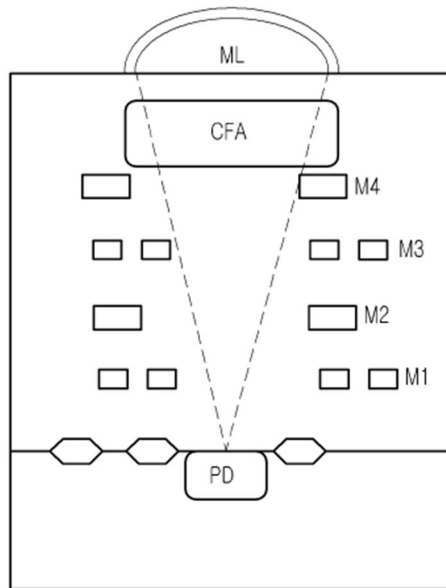
103. In this Section below, I briefly introduce various prior-art references discussed in this declaration.

A. Pyo (Ex. 1005, 2-10)

104. Pyo published as a Korean Unexamined Patent Application Publication No. 10-2006-0077132 on July 05, 2006. Pyo, 2. Pyo was published in Korean. *Id.*, 11-19. A certified English translation is also provided. *Id.*, 2-10. I understand and was informed that Pyo qualifies as prior art to the '366 patent. I reviewed the prosecution history of the '366 patent, and Pyo was cited in an IDS but was not cited in any rejection made or relied upon in any other way by the Examiner during prosecution of the '366 patent.

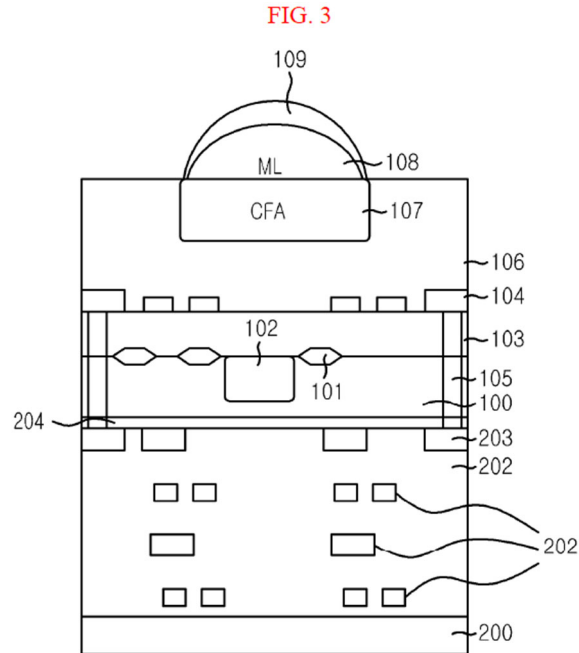
105. Pyo discloses that “conventional CMOS image sensor[s]” have multiple layers “comprising a plurality of metal lines and an insulating film” on top of the photodiodes that “causes a decrease in light sensitivity due to an increase in the distance from the photodiode to the color filter,” among other problems. *Id.*, 2. Figure 1 of Pyo shows “a conventional CMOS image sensor.” *Id.*, 3, Fig. 1 (reproduced below).

FIG. 1



106. Pyo discloses that it solved the problem of conventional CMOS sensors by separating the conventional CMOS image sensor into “an image chip” and “a logic chip” bonded to the back side of the image chip. *Id.*, 2. Pyo discloses that “since a plurality of metal lines on the top of the photodiode are omitted, the distance between the photodiode and the microlens is reduced to dramatically reduce the optical path, thereby improving the photosensitivity.” *Id.* Pyo discloses that “the present invention can solve the problems caused by the conventional stacked structure of the metal line and the insulating film.” *Id.*, 4.

107. Pyo discloses that “FIG. 3 is a cross-sectional view showing a CMOS image sensor according to one embodiment of the present invention.” *Id.*, 3, Fig. 3 (reproduced below).



I note that Figure 3 contains an error because it has mis-labeled the metal lines as 202, when the metal lines are designated with the reference number 201 as shown in the “Explanation of Symbols for Main Parts of the Drawings.” *Id.*, 3.

108. Pyo discloses that on the logic chip, “a plurality of metal lines 201 each surrounded by an insulating film 202 are formed on the second substrate 200.” *Id.*, 4. Pyo discloses that “[t]he metal line 201 is formed of aluminum or copper.” *Id.*, 6. Pyo discloses that “the pad 203 [is] connected to the metal line 201.” *Id.* A POSA would have understood that this connection would have been made by a via (not shown in Pyo’s figures) because vias are the interconnects that “form an electrical pathway from one metal layer to the adjacent metal layer.” Quirk (Ex. 1014), 54. Indeed, Pyo discloses “it is possible to form a logic element with 6-layer wiring or more without any major problems” further indicating the

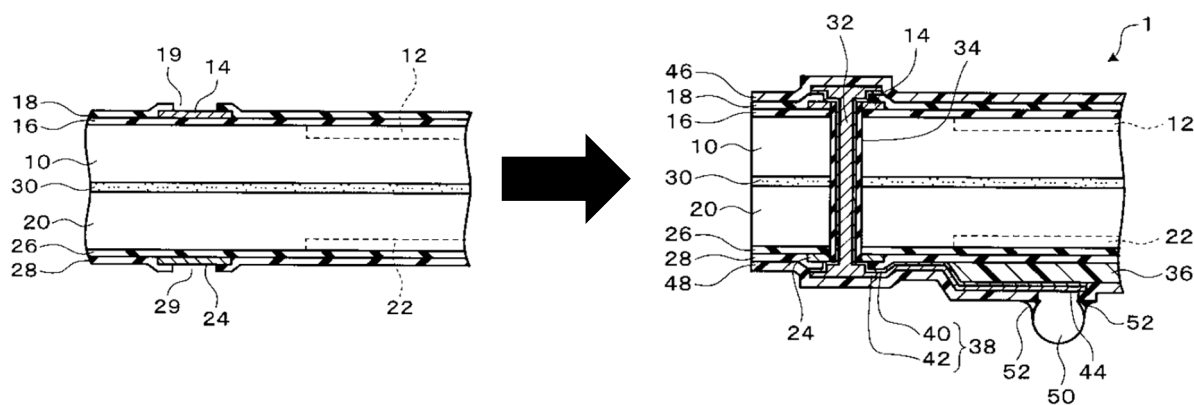
lines on the second substrate are interconnected using vias. Pyo, 5. While Pyo identifies its other via as a “connecting portion 105” (*id.*), Pyo also discloses it is formed using a “super *via* process” (*id.*, 6), which is an additional reason why a POSA would identify the connections between different levels of the pad 203 and metal lines 201 as vias.

109. “A plurality of transistors (not shown) are disposed on the first substrate 100 spaced apart from the photodiode 102.” *Id.*, 5. Pyo discloses that the “transistor comprises a reset transistor, a drive transistor, a select transistor, and the like.” *Id.* Pyo discloses that “the plurality of transistors are connected to the pads 203 of the second substrate 200 through the connecting portion 105 penetrating the first substrate 100” and that the “pads 203 are connected to the plurality of metal lines 201.” *Id.* Pyo discloses that the “connecting portion 105 comprises a metal such as tungsten, aluminum, or copper.” *Id.* The “connecting portion 105” is what is commonly known as a via (Quirk (Ex. 1014), 54), which Pyo discloses is formed using a “super via process.” Pyo, 6.

110. Below is Pyo’s fabrication process of bonding the image chip (Fig. 2a) to the logic chip (Fig. 2b). *Id.*, 5-6, Figs. 2a, 2b, 3.

that “the first and second semiconductor substrates are electrically connected through a conductive part ... thus enabling miniaturization to be attained.” *Id.*

113. The illustration below shows how “the first and second semiconductor substrates 10 and 20 are mutually stacked.” *Id.*, [0014], Fig. 5A. The first semiconductor substrate 10 has a “first integrated circuit 12,” an “optical part 13” (shown in Fig. 1), and a “first pad 14” while the second semiconductor substrate 20 has a “second pad 24.” *Id.*, [0009], [0011], [0036]. The two substrates are then electrically connected by a conductive part 38 as shown in Figure 3, reproduced below. *Id.*, [0009], [0024].



Id., Figs. 5(A) (left), and 3 (right).

C. Choi (Ex. 1007)

114. Choi published as U.S. Publication No. 2005/0012166A1 on January 20, 2005, from an application filed on June 16, 2004. Choi, face. I understand and was informed that Choi qualifies as prior art to the '366 patent.

115. Choi discloses that “multi-layered interconnections electrically connected to the transistors [that] include copper hav[e] a low resistance, thereby minimizing problems, such as a low speed and a high resistance, under a process condition having a design rule of about 0.13 micrometer.” *Id.*, [0139]. Choi cautions, however, that “copper atoms tend to diffuse into surrounding materials, such as into an interlayer dielectric layer, and can negatively impact the electrical characteristics of underlying transistors or other elements.” *Id.*, [0007]. Choi discloses “[t]herefore, in order to use copper as an interconnection material in an integrated circuit device, a diffusion barrier layer is necessary to prevent diffusion of the copper into surrounding materials.” *Id.*, [0008].

116. Choi discloses using tantalum (Ta) and tantalum nitride (Ta_N) for a barrier layer under the copper interconnection (*id.*, [0066]) and tungsten (W) and tungsten nitride (W_N) for a barrier layer capping the copper interconnection (*id.*, [0071]) in a multi-layer dual-damascene structure shown below. *Id.*, Fig. 4 (reproduced and annotated below).

The diagram is a cross-sectional view of a semiconductor device. It shows a substrate 100 with a series of layers and structures. At the bottom, there are regions 102, 110, 112, 114, and 116. Above these, there are layers 120, 122, 130, 140, 150, 160, 170, 175, 181, 190, 200, 200a, 200b, 211, 220, 230, 230a, 230b, 241, 250, 260, 260a, 260b, 271, 280, 290, and 300. A curved line 310 is shown at the top. Various materials are indicated by different hatching patterns: diagonal lines for Ta, TaN barrier layers (205, 235, 265); cross-hatching for W, WN barrier layers (181, 211); and a grid pattern for Cu interconnections (200, 230, 260). Arrows point from the text labels to the corresponding layers in the diagram.

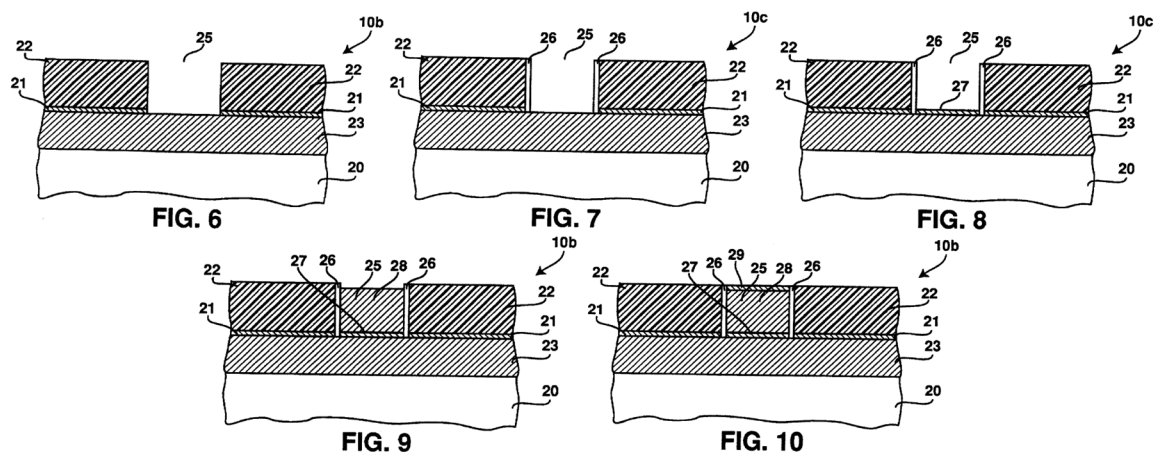
D. Dublin (Ex. 1008)

117. Dublin issued as U.S. Patent No. 5,695,810 on December 9, 1997, from an application filed on November 20, 1996. Dublin, face. I understand and was informed that Dublin qualifies as prior art to the '366 patent.

118. Dublin discloses that “[a] variety of materials are known for forming diffusion barriers on copper” including “Ta, W, Mo, TiW, TiN, TaN, WN, TiSiN and TaSiN.” *Id.*, 2:25-27. Dublin discloses “[f]urthermore, Ni, Co and Ni-Co alloys can be electrochemically deposited to serve as a diffusion barrier for Cu metallization.” *Id.*, 2:44-48. Dublin discloses “electrolessly depositing CoWP as a barrier material in order to protect or encapsulate a conductive material,” in particular, copper “which is utilized for forming interconnect structures on a semiconductor wafer.” *Id.*, 2:63-3:1. Dublin discloses that the “CoWP material is

preferred since copper can be electrolessly deposited on CoWP without the need for activation of the CoWP material surface,” “CoWP can be electrolessly deposited on copper without the need for activating the copper surface for CoWP deposition,” and “the presence of W in CoWP significantly enhances the barrier properties.” *Id.*, 3:1-7.

119. Dublin discloses a damascene process and structure for depositing the copper (28) and CoWP barrier layers (27, 29) as shown below. *Id.*, Figs. 6-10 (reproduced below).



E. Brase (Ex. 1009)

120. Brase issued as U.S. Patent No. 6,576,550 on June 10, 2003, from an application filed on June 30, 2000. Brase, face. I understand and was informed that Brase qualifies as prior art to the '366 patent.

121. Brase discloses that “the interconnect metallurgy is shifting from aluminum-based metals to copper, which has a lower resistivity.” *Id.*, 1:18-20. Brase discloses that “[t]he higher conductivity and lower cost of copper makes it

very desirable for interconnecting the circuit components” and that “copper has a better resistance to electromigration failures than Al or Al-Cu and therefore, better reliability.” *Id.*, 1:20-24.

F. Doering (Ex. 1010)

122. Doering is an excerpt of a textbook entitled “Handbook of Semiconductor Manufacturing Technology,” published by “CRC Press,” and bears a 2008 copyright date and the ISBN number “978-1-57444-675-3.” Doering, 1-2. I understand and was informed that Doering does not qualify as prior art to the ’366 patent but that it can be used as evidence of the state of the art.

123. Doering discloses that “aluminum etch to circuit dimensions below 0.10 μm has been difficult,” and due to the push for miniaturization, “nearly all high performance logic devices have made the transition to copper, as of 2004.” *Id.*, 5.

G. Edelstein (Ex. 1011, 9-12)

124. Edelstein is a paper entitled “Full Copper Wiring in a Sub-0.25 μm CMOS ULSI Technology,” published by the Institute of Electrical and Electronics Engineers (IEEE) at its 1997 International Electron Devices Meeting (IEDM) Technical Digest. Edelstein, 7-8.

125. Edelstein is cited by U.S. Patent No. 6,429,120, which issued on August 6, 2002. Ex. 1012, 1:40-46. Rachel J. Watters, librarian and Director of

Wisconsin TechSearch (“WTS”) at the University of Wisconsin-Madison, stated in a sworn declaration that the Kurt F. Wendt Library of the University of Wisconsin-Madison received a copy of the Technical Digest containing Edelstein on March 4, 1998 (Edelstein, 1-2, 6), which was then “catalogued and available to library patrons within a few days or at most 2 to 3 weeks after March 4, 1998.” *Id.*, 2. I understand and was informed that Edelstein qualifies as prior art to the ’366 patent.

126. Edelstein states:

We present the first fully integrated ULSI CMOS/copper interconnect technology. Up to 6 Cu wiring levels are built at minimum metal-contacted pitch of 0.63 μm , with W local-interconnect and contact levels and a poly contacted pitch of 0.81 μm , on a fully-scaled sub 0.25 μm , 1.8V CMOS technology. The Cu wiring has advantages of significantly lower resistance, higher allowed current density, and increased scalability, relative to comparable Ti/Al(Cu) wiring. These benefits in turn have enabled the scaling of pitch and thickness, from reduced-capacitance, high-density lower levels to low-RC global wiring levels, consistent with high-performance and high-density needs. The integrated Cu hardware was evaluated according to a comprehensive set of yield, reliability, and stress tests. This included fully functional, high-density 288K SRAM chips which were packaged into product modules and successfully tested for reliability. Overall, we find the results for full Cu wiring meet or exceed the standards set by our Al(Cu)/W-stud technology.

Id., 9.

H. Pratt (Ex. 1013, 4-23)

127. Pratt is a white paper bearing a 2004 copyright of Advanced Energy Industries, Inc. and states “Printed in U.S.A.” Pratt, 23. Nathaniel Frank-White,

Records Request Processor at the Internet Archive, stated in a sworn declaration that Pratt was archived by the Wayback Machine as early as June 21, 2006 (*id.*, 1-2) and attached a copy of that archived copy to his declaration (*id.*, 4-23). I understand and was informed that Pratt qualifies as prior art to the '366 patent.

128. Pratt explains several benefits of copper interconnections including low resistance, “power consumption reduction of 30%,” “ten to 100 times more resistance to electromigration failures than aluminum,” and a reduced “the number of interconnect levels and resulting in fewer process steps,” among others. *Id.*, 5-8. Pratt discloses that as of 2004 semiconductor fabrication machinery manufacturers were offering tools for copper interconnect fabrication “extendable beyond the 65 nm node” and “[s]everal advanced chipmakers have announced breakthrough technologies down to 45 nm.” *Id.*, 10.

I. Quirk (Ex. 1014)

129. Quirk is an excerpt of a textbook entitled “Semiconductor Manufacturing Technology,” published by “Prentice-Hall,” and bears a 2001 copyright date and the ISBN number “0-13-081520-9.” Quirk, 1-2. I understand and was informed that Quirk qualifies as prior art to the '366 patent.

130. Quirk discloses that as of at least its publication date in 2001, the “dual-damascene process became the consensus process for copper metallurgy.” *Id.*, 80. Quirk discloses the steps in the dual-damascene process at pages 80-82.

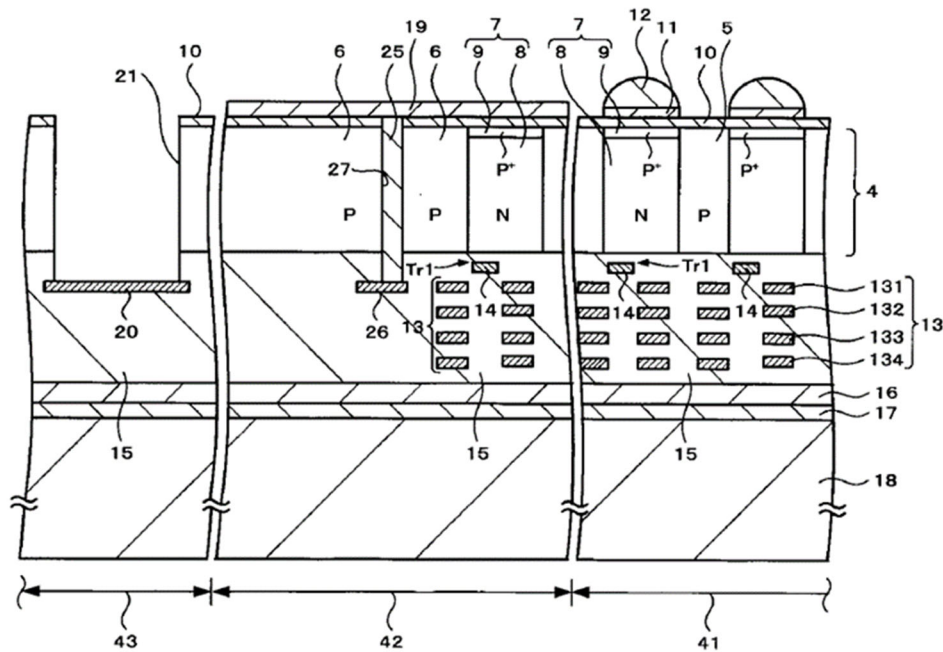
J. Yanagida (Ex. 1015)

131. Yanagida published as a Japanese Unexamined Patent Application No. 2006-32497 on February 2, 2006. Yanagida was published in Japanese (Ex. 1016) but reference in this declaration will be made to the certified English translation (Ex. 1015). I understand and was informed that Yanagida qualifies as prior art to the '366 patent.

132. Yanagida discloses that in conventional front-side irradiated image sensors, “the incident light is absorbed or reflected by the electrode layer or the like disposed on the front face side, giving rise to problems, such as reduced photoelectric conversion efficiency and reduced sensitivity with respect to incident light.” *Id.*, [0004]. Yanagida discloses that “[a]ccordingly, in recent years, as a construction to solve these problems, a so-called backside irradiation type solid-state image sensor has been introduced to increase the aperture ratio for photoreception and suppress absorption or reflection of incident light.” *Id.*, [0005].

133. Yanagida states “a first embodiment of the invention” is shown in Figure 2 (reproduced below). *Id.*, [0022]-[0023].

Yanagida, Fig. 2

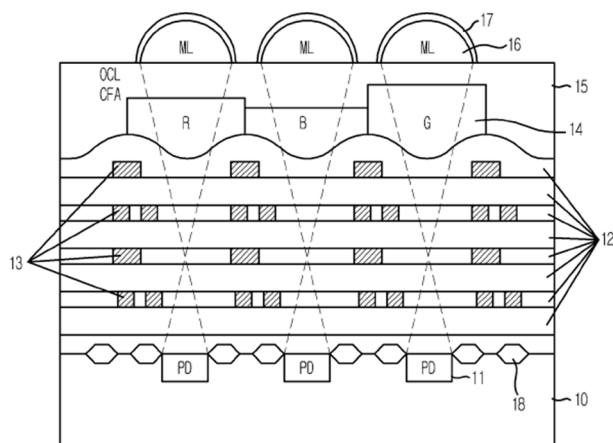


K. Yun (Ex. 1017, 2-17)

134. Yun published as a Korean Registered Patent 10-0664864 on January 3, 2007. Yun, 2. Yun was published in Korean (*id.*, 19-34) and a certified English translation is also provided (*id.*, 2-17). I understand and was informed that Yun qualifies as prior art to the '366 patent.

135. Yun disclosed a CMOS image sensors having a single substrate with interconnects above the photodiode array as shown in Figure 1 (reproduced below).

Yun, Fig. 1



136. Yun disclosed that “it is most ideal that the first incident light reaches 100% of the photodiode 11.” *Id.*, 8. Yun explains that “as the distance from the microlens 16 to which the light is incident to the photodiode 11 increases, the focus is disturbed ... resulting in loss of light.” *Id.* Yun disclosed that as demands for image resolution increased, “the size of the unit pixel is gradually reduced, so that the area ratio of the photodiode 11 per unit pixel is reduced to 30% or less.” *Id.*, 8.

L. Gambino (Ex. 1023, 21-27)

137. Gambino is a paper entitled “Optimization of Cu Interconnect Layers for CMOS Image Sensor Technology” (Gambino, 21), first presented at the Advanced Metallization Conference 2005 held on September 27- 29, 2005, in Colorado Springs, Colorado (*id.*, 5), and subsequently published by the Materials Research Society in 2006 (*id.*, 6).

138. Seema Rampersad, representative of the British Library, stated in a statutory declaration that the British Library received a copy of the conference proceedings containing Gambino on December 14, 2006 (*id.*, 1, 3), which was then catalogued and shelved on December 22, 2006, where it would have “been available for public use” from that date forward. *Id.*, 1. I understand and was informed that Gambino qualifies as prior art to the ’366 patent.

139. I was also personally involved in the research published in Gambino while working for the Eastman Kodak Company as I described in Section III, and I have personal knowledge that Gambino was made publicly available at the 2005 Advanced Metallization Conference. Since the work presented was a joint project between Kodak and IBM, the content of the paper was reviewed and approved by me and by Kodak corporate for presentation and publication at the aforementioned conference.

140. Gambino discloses a “0.18 μm CMOS imager sensor ... that uses Cu interconnects.” Gambino (Ex. 1023), 21. Gambino discloses that “[c]opper wiring results in a thinner dielectric stack compared to Al wiring, which provides an improved angular response of the photodiode.” *Id.* Gambino also discloses “a self-aligned CoWP passivation layer” to eliminate “the SiN capping layers on top of the Cu wires.” *Id.*

141. Figure 7 of Gambino (reproduced below) illustrates the advantages of using copper interconnects to make the dielectric stack, (often referred to as the optical stack height), between the microlens and the photodiode surface thinner.

Gambino, Fig. 7

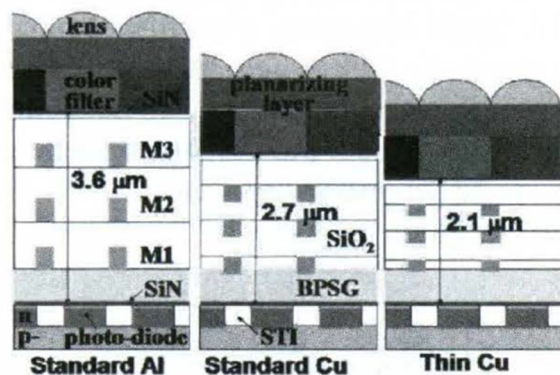


Fig. 7. Schematic comparing thicknesses of optical path with either standard 0.18 μm Al, standard 0.18 μm, Cu, or thin Cu metallization.

M. Yadid-Pecht (Ex. 1024)

142. Yadid-Pecht is an excerpt of a textbook entitled “CMOS Imagers: From Phototransduction to Image Processing,” published by “Kluwer Academic Publishers,” and bears a 2004 copyright date and the ISBN number “1-4020-7961-3.” Yadid-Pecht, 1-3. International Publication No. WO 2006/008637 A1, which published on January 26, 2006, cites Yadid-Pecht, listing the publisher as “Springer.” Ex. 1025, 5-6. Springer’s website states that it was formed after a merger between BertelsmannSpringer and Kluwer Academic Publishers in 2003, “producing the world’s second-largest academic publishing house,” and adopting

the new “Springer” name and logo “in 2004” (Ex. 1026, 2), which explains why Ex. 1025 lists the publisher of Yadid-Pecht as “Springer,” but Yadid-Pecht itself lists the publisher as Kluwer Academic Publishers. I understand and was informed that Yadid-Pecht qualifies as prior art to the ’366 patent.

143. Yadid-Pecht discloses that “CMOS process development is funded by high-volume sales of standard CMOS logic and memory chips,” hence, “CMOS imaging technology does not have to bear the process development costs and consequently has cheaper process costs than CCD imagers.” Yadid-Pecht, 19. Yadid-Pecht also discloses that “active pixel sensors (APS) are fabricated in a commonly used CMOS process,” and that the “continuous advances in CMOS technology for processors and DRAMs have made CMOS sensor arrays a viable alternative to the popular charge-coupled devices (CCD) sensor technology.” *Id.*, 30-31.

N. Iwabuchi (Ex. 1028, 118-260)

144. Iwabuchi published as International Publication No. WO 2006/129762 A1 on December 7, 2006, from an application filed on June 1, 2006. Iwabuchi, 118. Iwabuchi was published in Japanese. *Id.*, 2-117. A certified English translation is also provided. *Id.*, 118-260. I understand and was informed that Iwabuchi qualifies as prior art to the ’366 patent.

145. Iwabuchi teaches bonding a sensor chip (52) to a circuit chip (193) by bonding a first via 84" in the sensor chip to a second via 84 of the circuit chip. *Id.*, [0095]-[0096], Figs. 34A-34B. Iwabuchi states:

The first semiconductor chip 52 and the second semiconductor chip 193 are formed first of all, as shown in fig. 34A. The first semiconductor chip 52 has a configuration comprising ... contact portions 84" being formed in the transistor-forming region 56. ... In the second semiconductor chip 193, the via-contact portions 84 are formed on the lower portion side ..., the via-contact portions 84 penetrating this lower portion side. The first and second semiconductor chips 52, 193 are formed without pads.

Next, as shown in fig. 34B, the first semiconductor chip 52 and the second semiconductor chip 193 are joined by thermocompression bonding so that the contact portions 84" and the via-contact portions 84 thereof are connected face-to-face. *Id.*, [0095]-[0096].

146. Figures 34A and 34B of Iwabuchi are reproduced below.

FIG. 34A

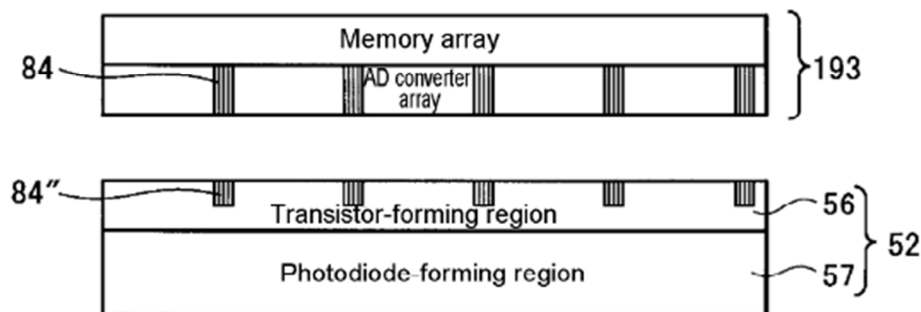
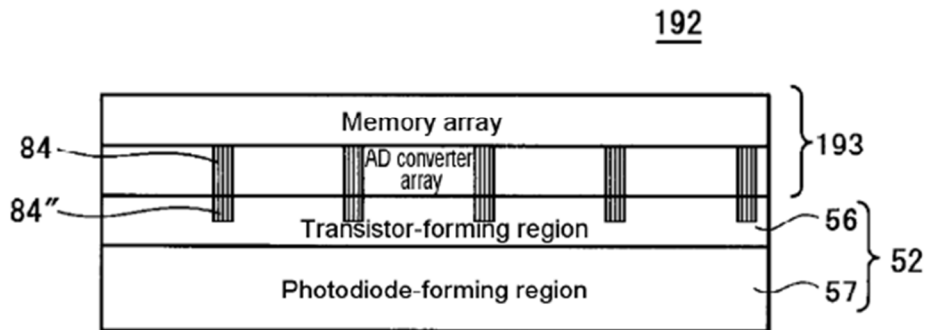


FIG. 34B

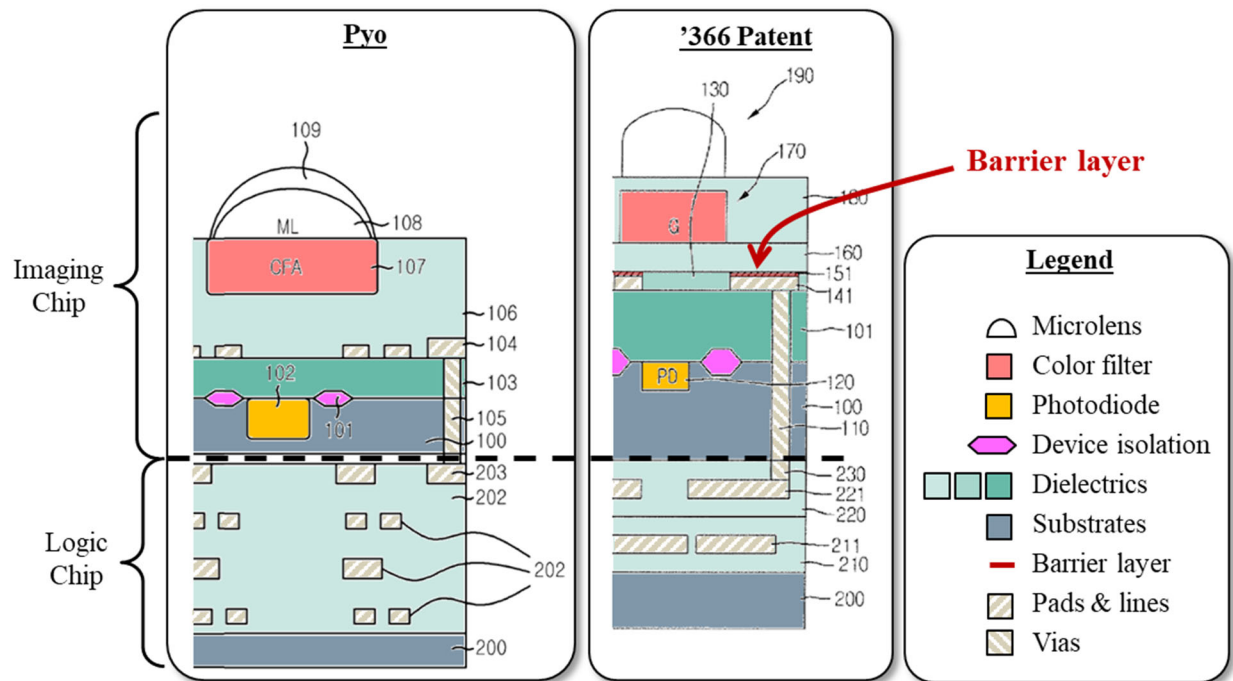


XI. FACTS AND OPINIONS RELEVANT TO THE UNPATENTABILITY GROUNDS ASSERTED IN THE PETITION

147. I have been asked to provide my opinion concerning whether claims 1-8 of the '366 patent (the “challenged claims”) would have been anticipated or obvious to a POSA in light of the prior-art references identified in the Petition. For the reasons explained below, it is my opinion that each of the challenged claims would have been anticipated under Patent Owner’s claim interpretations and obvious to a POSA even under narrower claim interpretations.

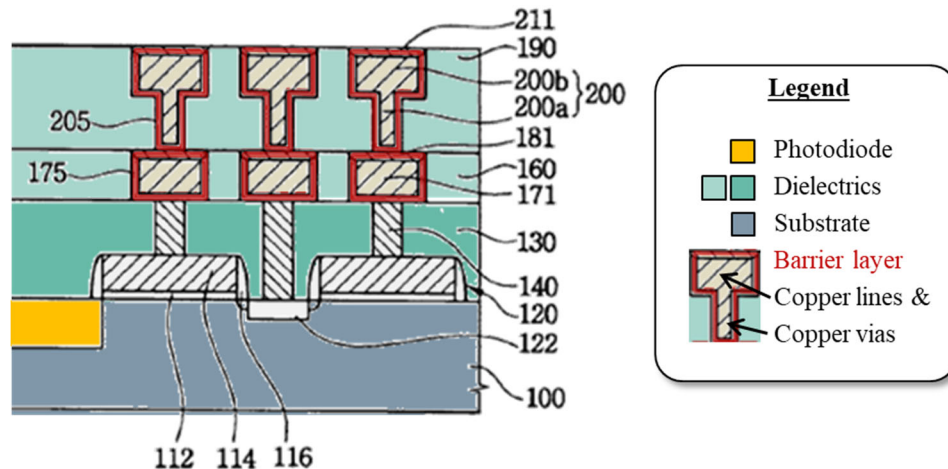
A. Ground 1: Pyo in view of Choi Renders Claims 1, 2, and 4-8 Obvious

148. Claims 1, 2, and 4-8 cover image sensors having a logic chip bonded to an imaging chip, below right. '366 patent, Fig. 8. Pyo disclosed a similar sensor, below left. Pyo (Ex. 1005), Fig. 3. The difference between them is Pyo’s sensor does not have a conductive barrier layer on its metal lines (104).

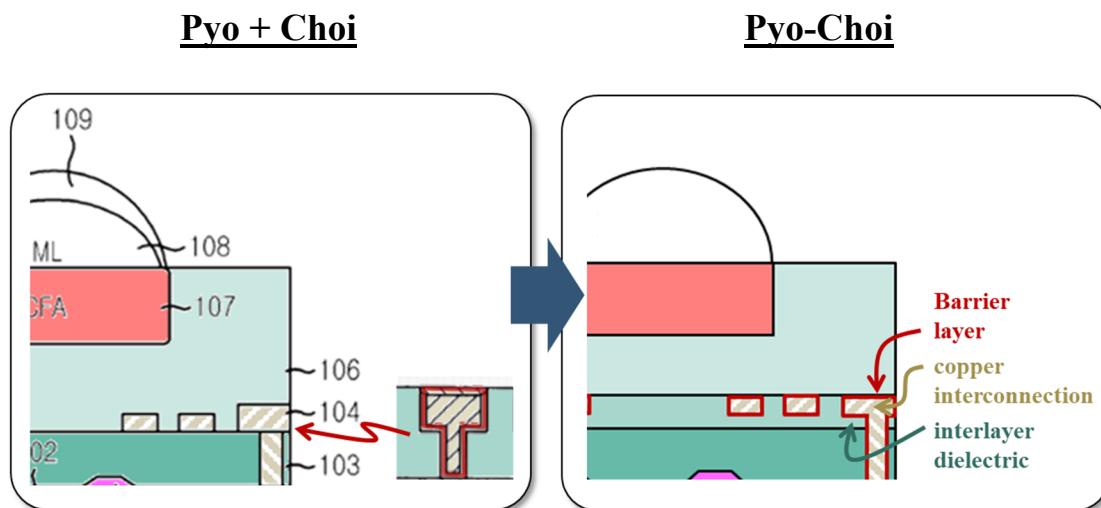


149. Pyo does not identify the metal used to fabricate lines (104) but discloses other metal lines (201)—mislabeled as “202” in Figure 3—can be copper.

150. Choi disclosed copper interconnections had advantages over aluminum interconnections when fabricating CMOS image sensors, but copper required barrier layers. Choi is one of many references disclosing such advantages of copper interconnections. Choi also discloses how to implement copper interconnections in a CMOS sensor by using a dual-damascene process which results in metal interconnections on an interlayer dielectric and using a conductive barrier layer on the metal interconnections, rendering claims 1, 2, and 4-8 obvious. Choi (Ex. 1007), Fig. 5G (excerpted and annotated below).



151. Copper's advantages over aluminum (the only other natural choice for interconnections) would have made it a natural choice for Pyo's metal lines (104) when implementing Pyo's design in 2007.



Doing so using Choi's well-known methods would have resulted in conductive metal barrier layers, on copper interconnections, on an interlayer dielectric, as required by the challenged claims, as shown above.

1. Reasons to Use Copper Throughout Pyo's Sensor

152. Pyo does not disclose the material for the metal lines on the image chip. But Pyo states that the metal lines on its second substrate are “formed using copper or aluminum” and that the via connecting the metal lines on the first substrate to the second “comprises a metal such as tungsten, aluminum, or copper.” Pyo (Ex. 1005), 5. Pyo discloses its metal lines (104) also serve a “light-shielding function.” *Id.* Light shielding requires only an opaque material to block the incident light. Aluminum and copper were each well-known options for interconnections in CMOS manufacturing, and each would achieve light-shielding and interconnection functions of Pyo's metal lines (104) because each is opaque and conductive. POSAs would have had several reasons to modify Pyo's sensor design to use copper in all of Pyo's interconnects, including the metal lines on the first substrate as well.

153. **Higher Performance:** Copper has several performance advantages over aluminum and aluminum-copper alloys including: (1) lower resistivity resulting in thinner and narrower lines, and providing further improvement in the optical efficiency of the pixel, (reduced optical stack height, a wider aperture around the photodiode), and smaller pixels for increased sensor resolution, (2) reduced power consumption, which was a critical need for image sensors used in mobile phones, and (3) resistance to electromigration, resulting in higher reliability

(fewer product failures and reduced packaging complexity and cost. *See* Section VI.B (which starts on page 20); *see also* Quirk (Ex. 1014), 59-60; Edelstein (Ex. 1011), 9; Choi (Ex. 1007), [0139]; Pratt (Ex. 1013), 5-8; Doering (Ex. 1010), 4-5; Brase (Ex. 1009), 1:15-25; Dublin (Ex. 1008), 1:35-38; Gambino (Ex. 1023), 21. The advantages of copper over prior metals meant that “nearly all high Performance logic devices have made the transition to copper, as of 2004.” Doering (Ex. 1010), 5. And Gambino discloses a 0.18 μm CMOS imager sensor that used three levels of copper interconnections in 2005. Gambino (Ex. 1023), 21. In 2006, a POSA would have thus had reason to modify Pyo’s design to use copper interconnects throughout to take advantage of any one of these performance advantages alone or in combination.

154. **Compatibility with Production Equipment:** An independent reason to modify Pyo’s design was to utilize then-current CMOS fabrication equipment (“fabs”) for manufacturing. Pyo (Ex. 1005), 3 (disclosing the desirability of using “the CMOS technology that has previously been set-up ... interchangeably” “to lower the manufacturing cost”). By 2007, that meant using copper interconnections. Doering (Ex. 1010), 5 (“nearly all high performance logic devices have made the transition to copper, as of 2004”); Yadid-Pecht, 19 (“CMOS process development is funded by high-volume sales of standard CMOS logic and memory chips,” hence, “CMOS imaging technology does not have to bear the

process development costs and consequently has cheaper process costs than CCD imagers.”), 30-31 (noting that sensors “are fabricated in a commonly used CMOS process,” and that the “continuous advances in CMOS technology for processors and DRAMs have made CMOS sensor arrays a viable alternative to the popular charge-coupled devices (CCD) sensor technology”).

155. Pratt discloses that as of 2004, manufacturers of semiconductor fabrication machinery were offering tools “extendable beyond the 65 nm node” and “[s]everal advanced chipmakers have announced breakthrough technologies down to 45 nm.” Pratt (Ex. 1013), 10. Pratt predicted that semiconductor manufacturers would achieve an 80 nm design rule by 2005 and a 65 nm design rule by 2007. *Id.*, 5 (Table 1). But “[w]hen manufacturing semiconductor devices having a pattern size less than about 0.13 μm , aluminum is no longer satisfactory as an electrical interconnection material.” Choi (Ex. 1007), [0007]; *see also* Doering (Ex. 1010), 5 (“aluminum etch to circuit dimensions below 0.10 μm has been difficult”). In contrast, “multi-layered interconnections [using] copper having a low resistance, thereby minimizing problems, ... under a process condition having a design rule of about 0.13 micrometer.” Choi (Ex. 1007), [0139]. Thus, by 2004, “nearly all high performance logic devices [had] made the transition to copper.” Doering (Ex. 1010), 5.

156. CMOS image sensors were commonly made using similar fabrication machinery as other CMOS chips. Yadid-Pecht (Ex. 1024), 30-31 (noting image sensors “are fabricated in a commonly used CMOS process” and that the “continuous advances in CMOS technology for processors and DRAMs have made CMOS sensor arrays a viable alternative to the popular charge-coupled devices (CCD) sensor technology”); *see also id.*, 19 (“CMOS process development is funded by high-volume sales of standard CMOS logic and memory chips,” hence, “CMOS imaging technology does not have to bear the process development costs and consequently has cheaper process costs than CCD imagers.”). Using the then existing processes which commonly employed copper interconnections was the natural choice for CMOS image sensors by 2007.

157. Given that Pyo states “[t]he metal line 201 is formed of aluminum or copper” and that “it can be loaded with core logic technology of 130 nm and 90 nm or less as it is” (Pyo (Ex. 1005), 5), a POSA would have understood that Pyo’s sensor was compatible with 130 nm or 90 nm design rules and could be implemented using then-existing 130 nm or 90 nm CMOS fabs, which in many instances used copper for interconnections. This would have been a strong reason to modify the Pyo design to use copper interconnects.

158. **Fewer Processing Steps and Higher Yields:** A POSA would have been independently motivated to modify Pyo’s design to use copper

interconnections because a copper dual-damascene process results in fewer processing steps. Pratt disclosed that “interconnect routing can be simplified, reducing the number of interconnect levels and resulting in fewer process steps.” Pratt (Ex. 1013), 8; *see also* Quirk (Ex. 1014), 60 (“Narrower lines permit tighter circuitry packing, which means that fewer levels of metal are needed.”); Doering (Ex. 1010), 5 (“the advantages of copper interconnects result in ... fewer interconnect metal levels”).

159. Fewer processing steps also “translates to cost savings and higher device yield.” Pratt (Ex. 1013), 8; *see also* Quirk (Ex. 1014), 82 (“fewer process steps translate to fewer sources of error that reduce assembly yield.”); Dublin (Ex. 1008), 1:39-47 (Use of copper results in “low processing cost,” including equipment that is “relatively less expensive, as compared to other semiconductor equipment for depositing metals,” thus “overall costs can be reduced.”); Brase (Ex. 1009), 1:18-25 (The “lower cost of copper makes it very desirable for interconnecting the circuit components.”). A POSA would thus be motivated to implement copper interconnects to reduce the number of process steps, increase yields, and decrease costs.

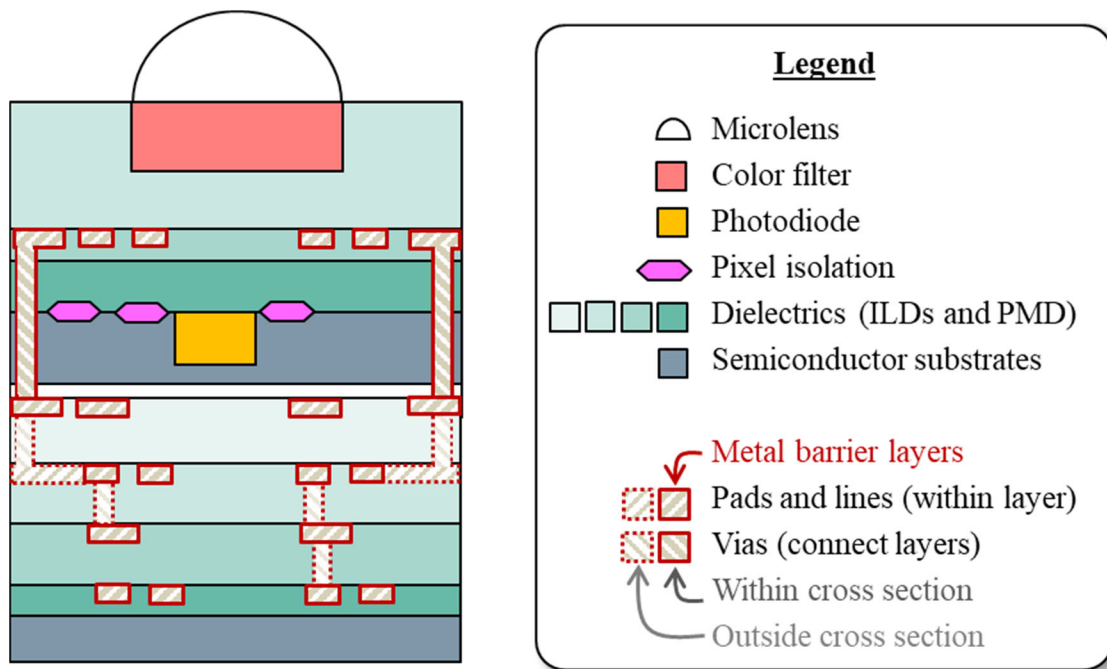
160. **Pyo Only Discloses Two Possible Metals for Lines:** While Pyo is technically silent as to the composition of lines 104, Pyo states that the “metal line 201 is formed using copper or aluminum.” Pyo (Ex. 1005), 5. POSAs would have

understood that the disclosure elsewhere about copper or aluminum was applicable to lines 104 as well, especially given what was already known in the art about interconnections. It would have been obvious to try copper as one out of the two possibilities disclosed.

2. Resulting Pyo-Choi Sensor

161. The sensor resulting from modifying Pyo’s design to use copper interconnections throughout (“Pyo-Choi Sensor”) is shown below.

Pyo-Choi Sensor

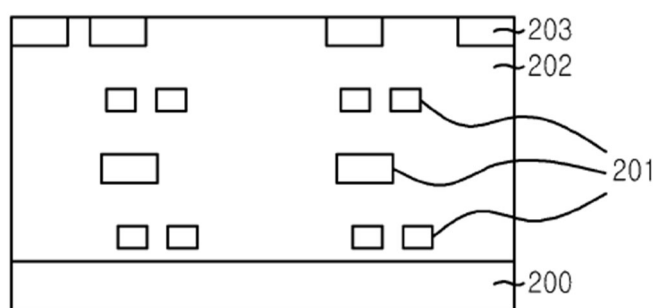


162. Pyo separately fabricates logic and image chips before bonding them together. Pyo (Ex. 1005), 5-6, Figs. 2a, 2b, 3. POSAs would do the same to fabricate the Pyo-Choi sensor.

a. Fabricating the Logic Chip

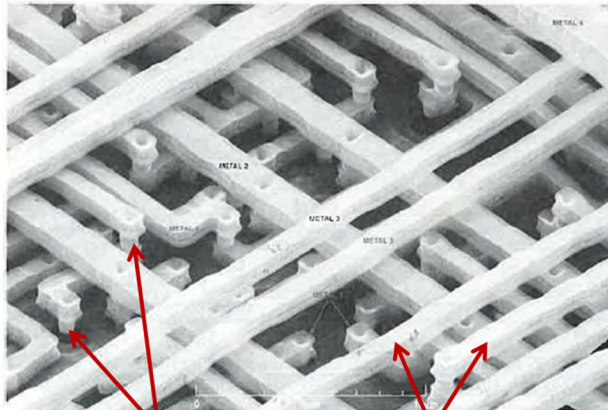
163. Pyo discloses its logic chip has a “a plurality of metal lines 201”; the figures show four levels of wiring, and Pyo also discloses “it is possible to form a logic element with 6-layer wiring or more.” *Id.*, 5, Figs. 2b (below, original) and 3. Pyo also describes “pads 203” as “connected to the plurality of metal lines 201.” *Id.*, 5. POSAs would therefore recognize the existence of a connection from pad 203 to metal lines 201 even though not expressly reflected in Pyo’s figures.

FIG. 2b



164. POSAs would similarly recognize Pyo’s logic chip had connections between layers of wiring (201) even though not expressly reflected in Pyo’s figures. Such simplifications were commonplace in such figures; for example, a two-dimensional cross-section (Quirk (Ex. 1014), 55 (annotated, below right)) does not illustrate all the vias and lines in the network shown in a three-dimensional micrograph (*id.*, 55 (annotated, below left)).

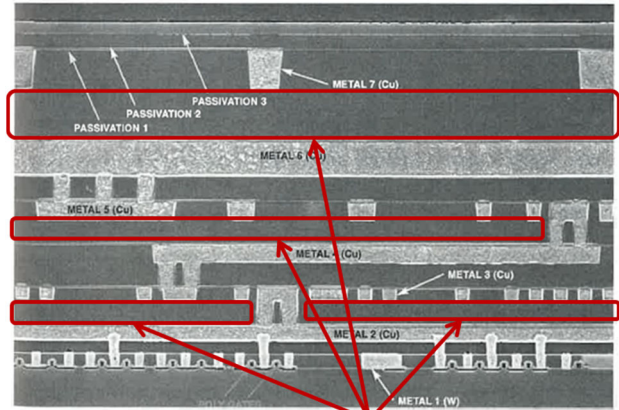
Three-Dimensional View



Vias

Lines / wires

Cross-Section



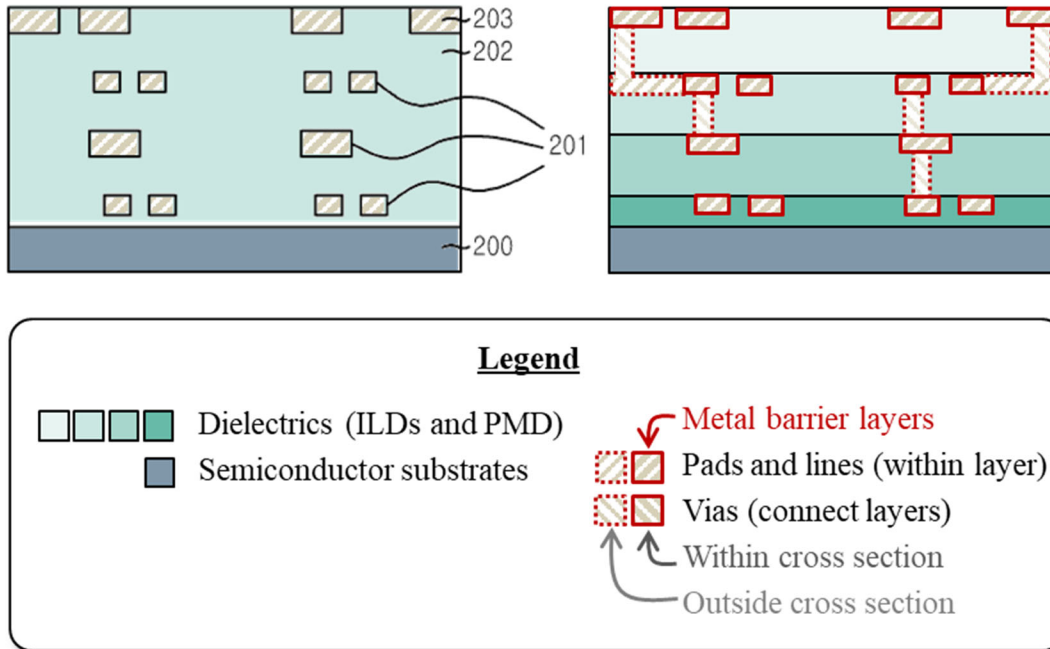
Vias Connecting Wires Not Shown

165. POSAs would understand Pyo's design had interconnections between levels of metal lines (201) even though Pyo's figures do not illustrate such details. Such interconnections are required for Pyo's sensor to function. Exemplary lines and vias outside the cross section are thus illustrated below, right, to better depict Pyo's sensor's "three-dimensional structure." Pyo (Ex. 1005), 4, Fig. 2b (annotated, below left).

Pyo

Pyo-Choi

FIG. 2b



i. Choi's Fabrication Method

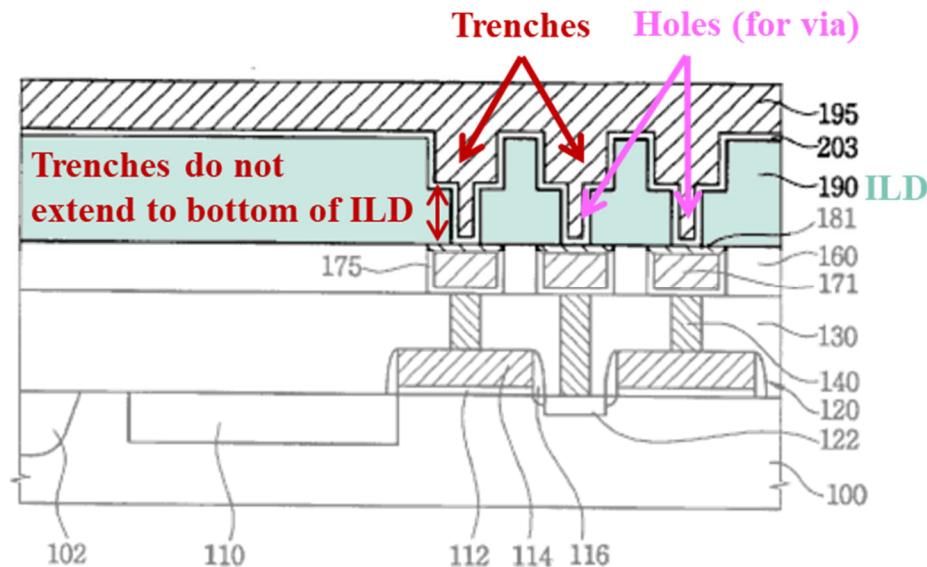
166. Choi discloses image sensors in which copper-based lines and vias are fabricated together—a technique commonly known as the dual-damascene process. Choi (Ex. 1007), [0124]-[0132], Figs. 5E – 5G.

(1) ILD and Patterning

167. First, an “insulating interlayer 190” is formed and then “partially removed, e.g., etched using photolithography.” *Id.*, [0124]-[0125], Fig. 5E. While Choi patterns trenches and holes in one etching step, POSAs would have known multiple etches could be used in various orders interchangeably (*see, e.g.*, Quirk (Ex. 1014), 80-82, Brase (Ex. 1009), 1:47-2:10)—yielding the same results. Choi

teaches trenches for lines would not extend to the bottom of the ILD layer. Choi (Ex. 1007), Fig. 5E (below, annotated).

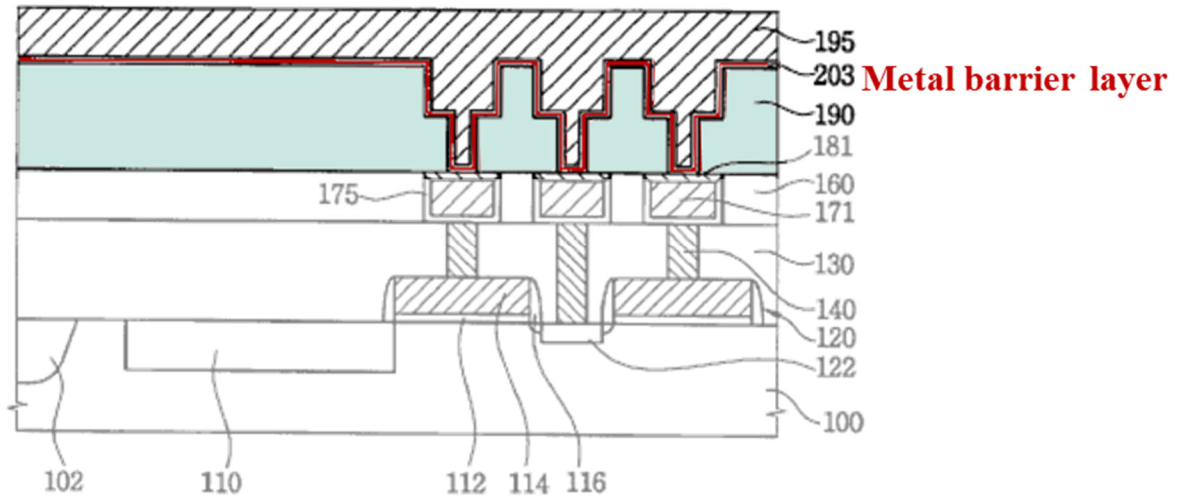
Choi Fig. 5E (Annotated)



(2) Bottom Metal Barrier Layer

168. Choi deposits a metal barrier layer over the patterned ILD. *Id.*, [0126], Fig. 5E (below, annotated). Such barrier “prevent[s] diffusion of the copper into surrounding materials.” *Id.*, [0008]. Choi discloses tantalum (Ta) and tantalum nitride (Ta₂N₅) as suitable. *Id.*, [0066]. Each is a conductive metal. Quirk (Ex. 1014), 62-63 (listing Ta, TaN, and WN as meeting the criteria of copper barrier metals as having for low resistivity).

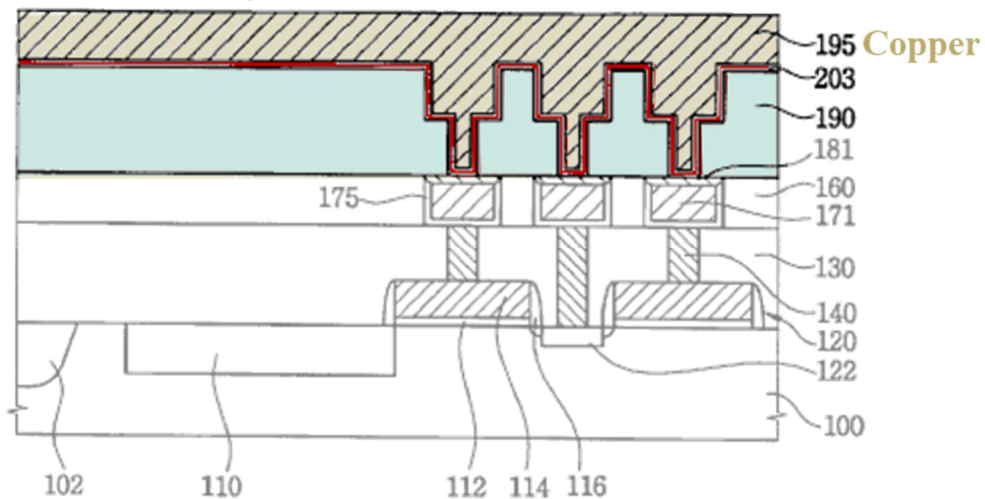
Choi Fig. 5E (Annotated)



(3) Copper Deposition

169. Next, trenches and holes (“vias”) are filled with copper. Choi (Ex. 1007), [0126], Fig. 5E (below, annotated).

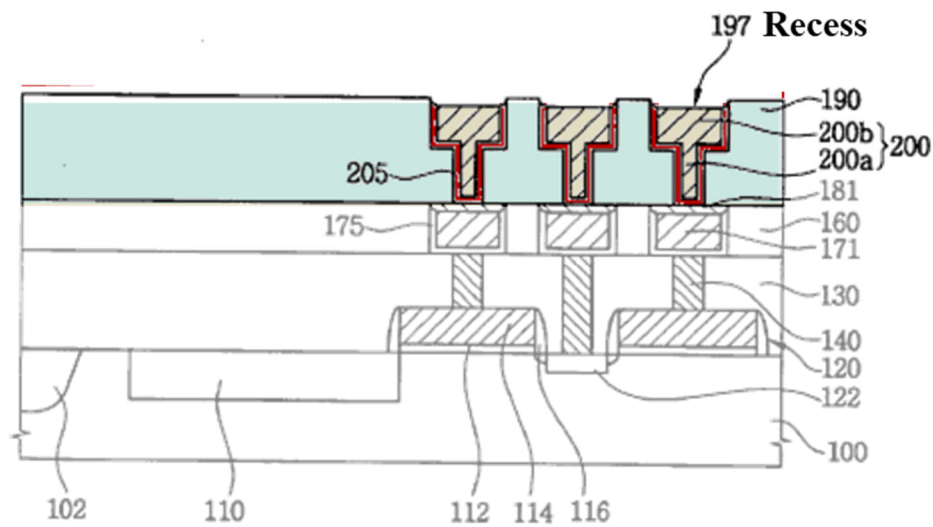
Choi Fig. 5E (Annotated)



(4) Chemical Mechanical Polishing (“CMP”)

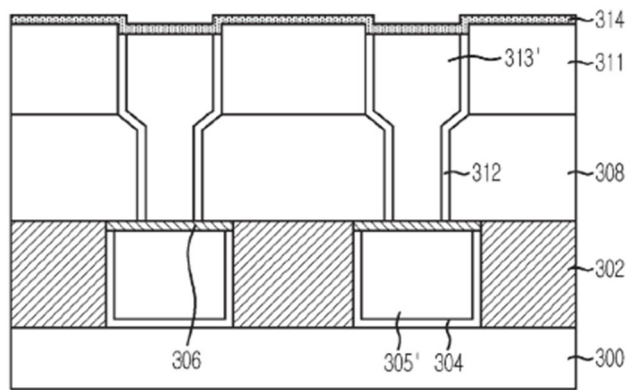
170. “[C]opper layer 195 is removed, e.g., using CMP, so that the first copper interconnection 200 ... is formed” with “upper surface of the first copper interconnection 200 ... positioned ... lower than the upper surface of the second insulating interlayer 190, so a second recess 197 ... is formed.” *Id.*, [0128], Fig. 5F (below, annotated).

Choi Fig. 5F (Annotated)



171. Creating a recess as Choi does was common in CMOS manufacturing. Yun (Ex. 1017), 13 (“excessive polishing is performed so that the copper layer 313 and the third barrier layer 312 filled in the upper trench are recessed”), Fig. 3i (below).

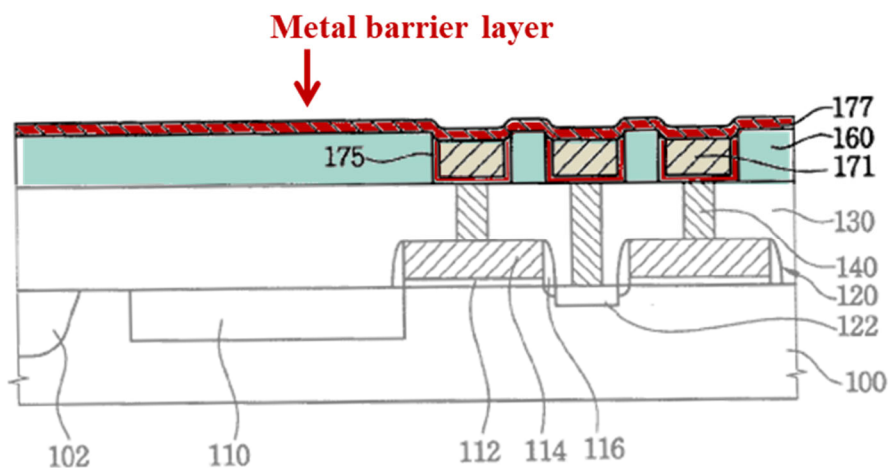
FIG. 3i



(5) Top Metal Barrier Layer

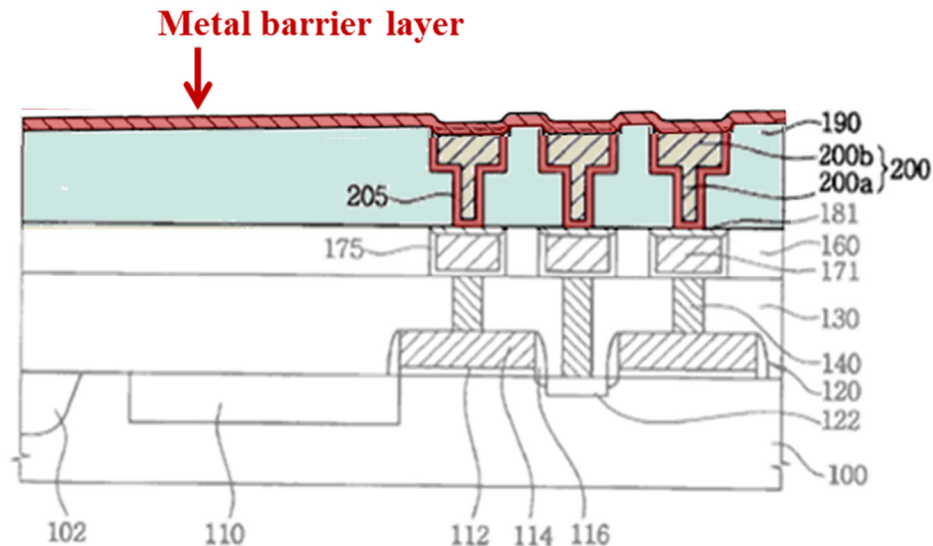
172. A metal barrier layer is next deposited across the surface. Choi (Ex. 1007), [0129]. Figure 5C (part of Choi's related single-damascene process) shows such a barrier layer. *Id.*, [0121]-[0122] (describing a “diffusion preventing pattern”).

Choi Fig. 5C (Annotated)



173. The metal barrier layer applied to Choi's Figure 5F would appear as shown below.

Choi Fig. 5F (Modified)



174. POSAs would understand Choi’s “diffusion preventing pattern” prevents copper from diffusing into surrounding materials (*id.*, [0007]) and subsequent layers from oxidizing the copper (Dublin (Ex. 1008), 2:16-24), making it a barrier layer. Choi discloses tungsten and tungsten nitride are suitable. Choi (Ex. 1007), [0122]. Each are conductive metals. Quirk (Ex. 1014), 62-63 (listing Ta and WN as meeting the criteria of copper barrier metals as having for low resistivity), 56 (Tungsten (W) has an even lower resistivity ($8\ \mu\Omega\text{-cm}$) than tantalum (Ta) (“13 to 16” $\mu\Omega\text{-cm}$)).

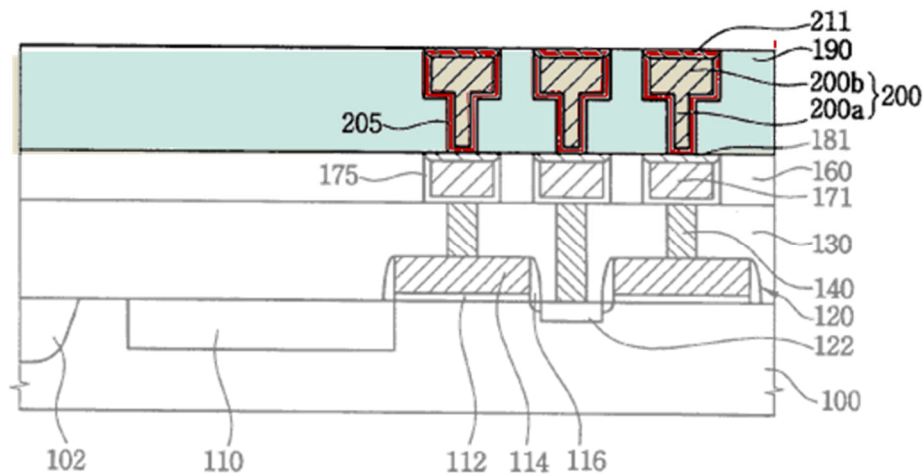
175. While Choi also discloses insulators silicon nitride (“SiN”) and silicon carbide (“SiC”) as alternative barrier materials, Choi discloses they “may negatively impact the performance of image devices” (Choi (Ex. 1007), [0008]) and discloses that insulators such as silicon nitride need to “be removed during the

etching” in order to make electrical connection with other layers of the wiring (*id.*, [0125]). Indeed, this was the same issue my team at Kodak encountered in making a CMOS sensor with copper interconnects and chose to omit the top silicon nitride barrier layer in favor of a CoWP conductive metal barrier layer. Gambino (Ex. 1023), 21. POSAs would have thus preferentially used conductive metals, not insulators. Quirk (Ex. 1014), 62-63; Gambino (Ex. 1023), 21.

(6) Planarization

176. Choi then planarizes the barrier layer “by CMP, such that [it] remains only in the second recess 197.” Choi (Ex. 1007), [0129], Fig. 5G (below, annotated).

Choi Fig. 5G (Annotated)

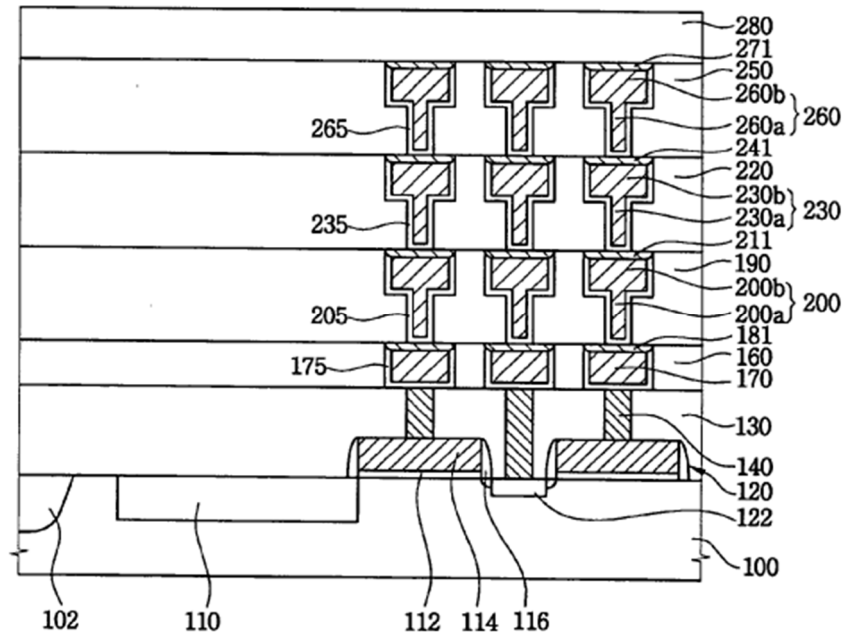


(7) Subsequent Levels

177. Choi repeats steps (1) through (6) to form subsequent metal layers. *Id.*, [0130]-[0132] (“a multi-layered structure” may be formed “by repeatedly

performing the processes described”), Fig. 5H (below). Notably, when using metal barrier layers as discussed above, they need not be etched away for subsequent levels. *Id.*, [0125].

Choi, Fig. 5H



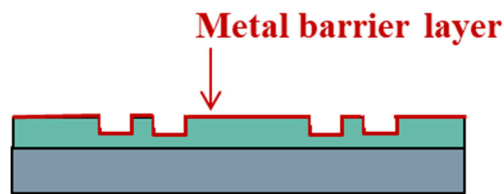
ii. Applying Choi’s Process to Fabricate the Pyo-Choi Logic Chip

178. As of at least 2001, “*the dual-damascene process became the consensus process for copper metallurgy*” and thus a routine means for incorporating copper interconnections. Quirk (Ex. 1014), 80. It would thus have been an obvious choice when implementing Pyo’s sensor with copper interconnections. Starting with second substrate 200, POSAs would have applied Choi’s process as follows to create the first layer of metallization.

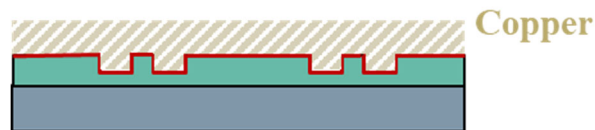
179. **Deposit ILD and pattern trenches for lines (201) and holes for vias** (not shown). Choi (Ex. 1007), [0124]-[0125], Fig. 5E; Quirk (Ex. 1014), 80-82; Brase (Ex. 1009), 1:47-2:10.



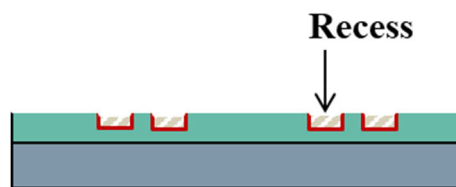
180. **Deposit bottom metal barrier layer.** Choi (Ex. 1007), [008], [0066], [0126], Fig. 5E; Quirk (Ex. 1014), 56, 62-63.



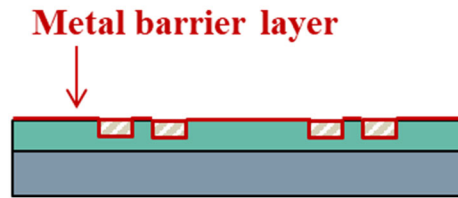
181. **Deposit copper.** Choi (Ex. 1007), [0126], Fig. 5E.



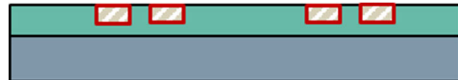
182. **Polish to create recess.** *Id.*, [0128], Fig. 5F; Yun, (Ex. 1017), 13, Fig. 3i.



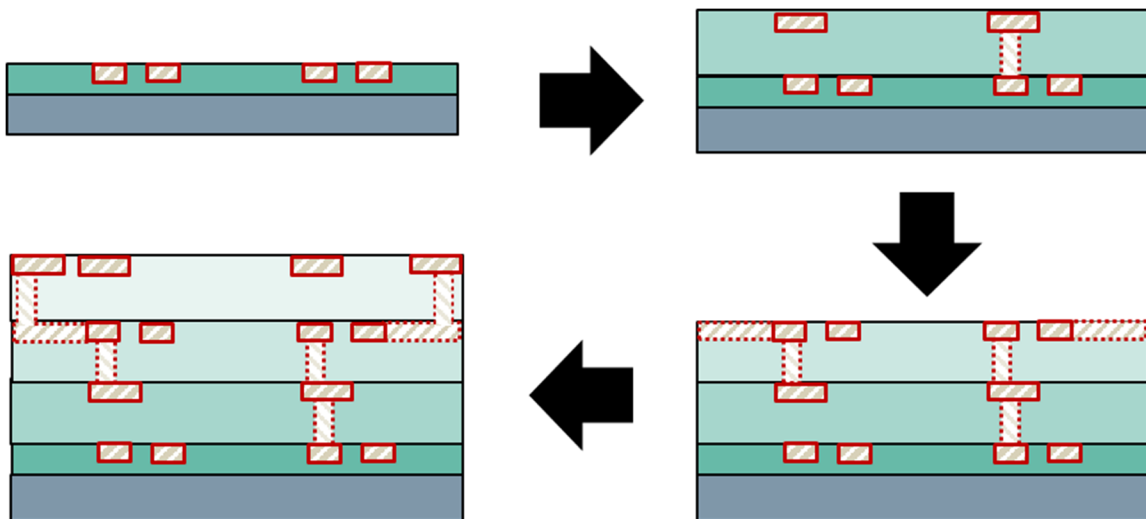
183. **Deposit top metal barrier layer.** Choi (Ex. 1007), [0121]-[0122], [0129], Fig. 5C.



184. **Planarize.** *Id.*, [0129], Fig. 5G.



185. POSAs would have repeated these steps to fabricate each subsequent metal layer. *Id.*, [0125], [0130]-[0132], Fig. 5H.

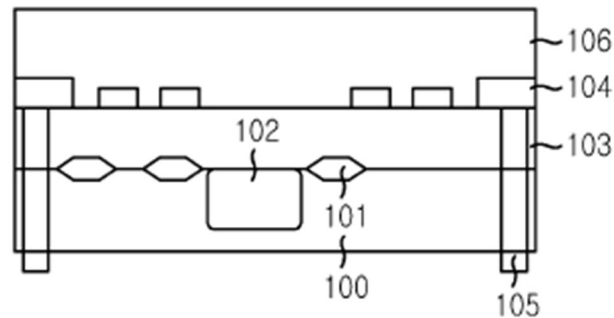


b. Fabricating the Image Chip

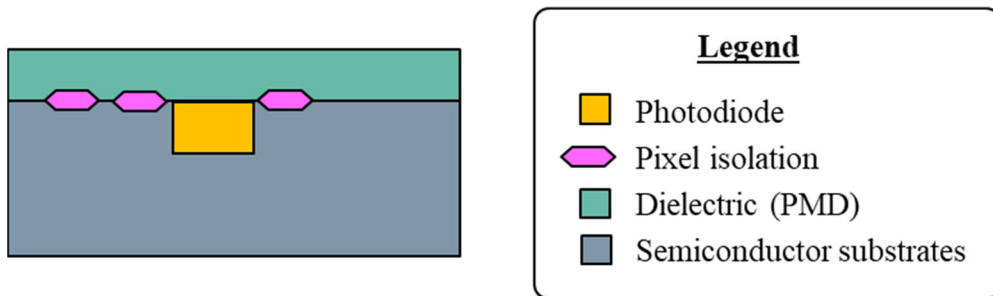
186. Pyo's image chip included "a field oxide layer 101" "on the first substrate 100," a "photodiode 102," "a plurality of transistors constituting a unit pixel," "an insulating film 103," and a "metal line 104" "connected to the gate electrode or source/drain of the transistor through a contact," where "a connecting

portion 105 [is] connected to the metal line 104” using a “super via process.” Pyo (Ex. 1005), 5-6, Fig. 2a (below).

FIG. 2a



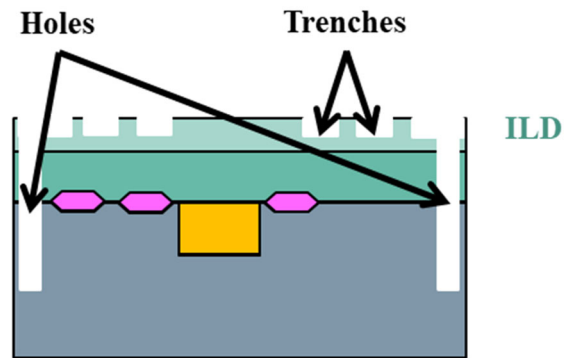
187. POSAs would understand applying the same dual-damascene process as described for the logic chip would have been an obvious way to implement copper interconnections for Pyo’s image chip.



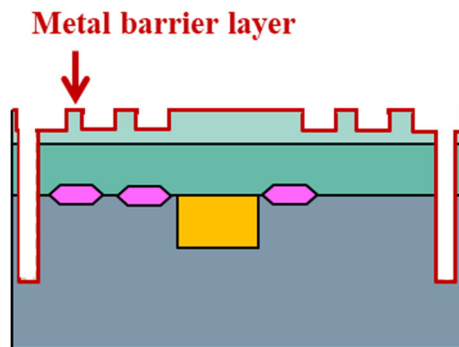
188. Starting with Pyo’s image chip after insulating film 103 is deposited (shown above), POSAs would have applied the following steps to create lines (104) and vias (105) in the image chip.

189. **Deposit ILD and pattern** trenches for lines (104) and holes for vias (105). Choi (Ex. 1007), [0124]-[0125], Fig 5E. While there is some variation in how trenches and holes were formed (trenches first then vias, vias first then

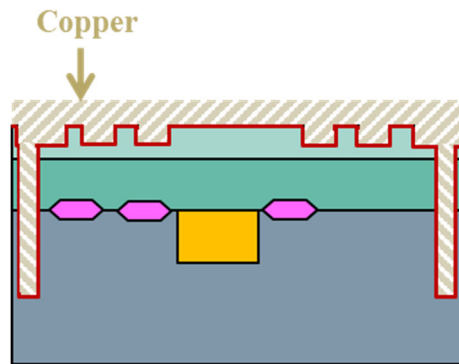
trenches, or both simultaneously – *see* Quirk (Ex. 1014), 80-82, Brase (Ex. 1009), 1:47-2:10), regardless of that variation, the end result was the same. Using Choi's method, trenches would not extend to the bottom of the interlayer dielectric layer, below. Choi (Ex. 1007), Fig. 5E.



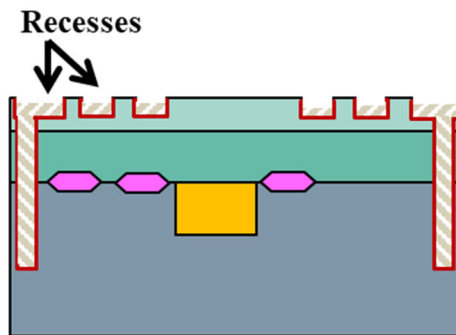
190. **Deposit bottom metal barrier layer.** Choi (Ex. 1007), [008], [0066], [0126], Fig. 5E; Quirk (Ex. 1014), 56, 62-63.



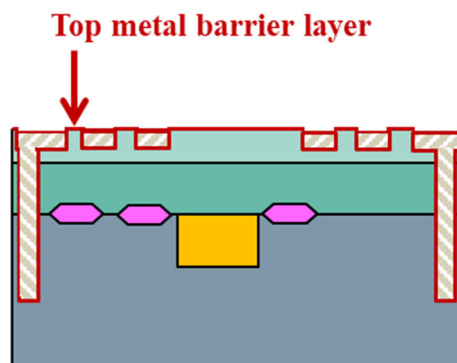
191. **Deposit copper.** Choi (Ex. 1007), [0126], Fig. 5E.



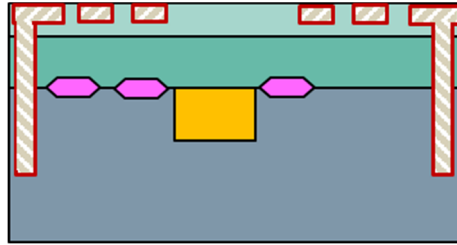
192. **Polish to create recess.** *Id.*, [0128], Fig. 5F; Yun, 13, Fig. 3i.



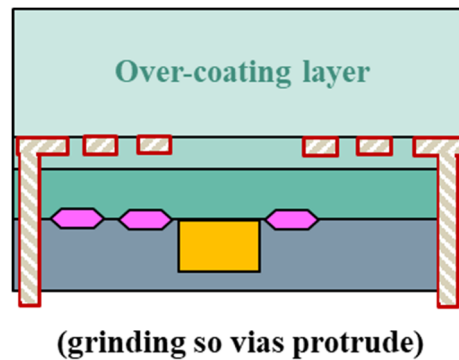
193. **Deposit top metal barrier layer.** Choi (Ex. 1007), [0121]-[0122], [0129], Fig. 5C.



194. **Planarize.** *Id.*, [0129], Fig. 5G.

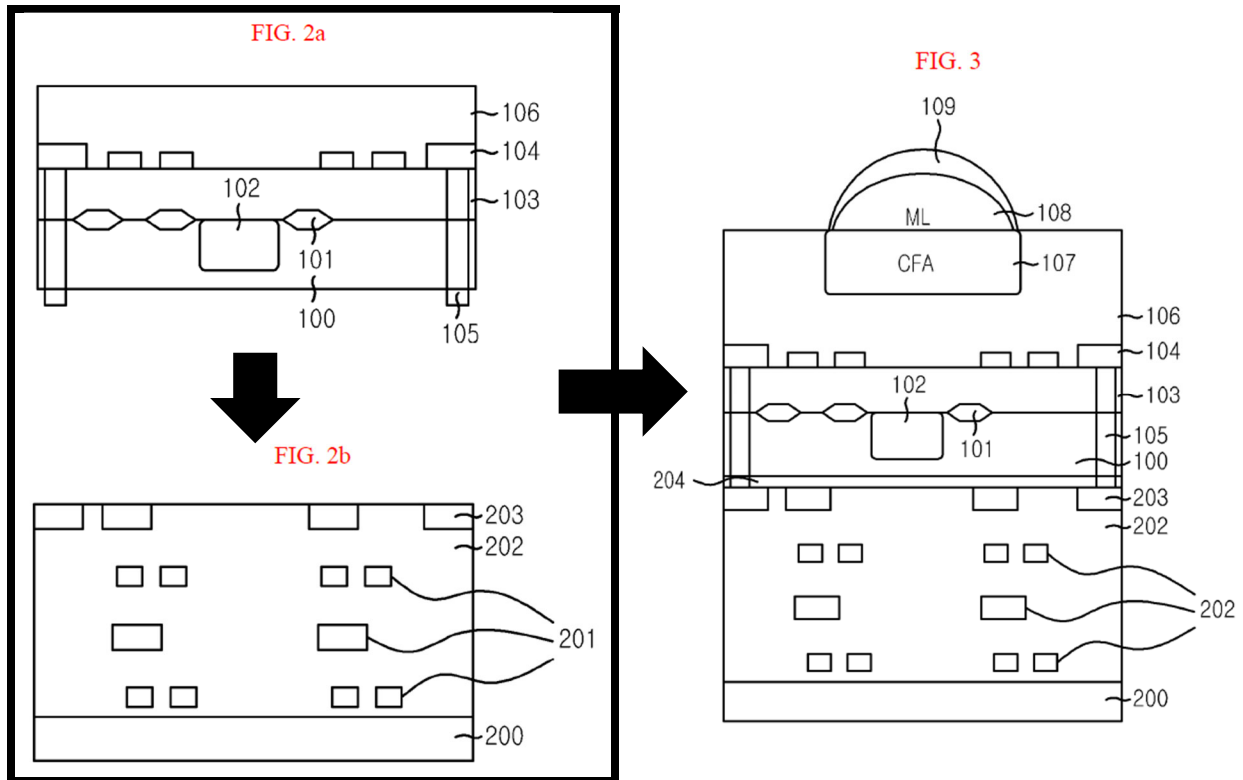


195. Pyo completes the image chip by depositing “an over-coating layer 106” (Pyo (Ex. 1005), 5, Fig. 2a) and “grinding the rear surface of the first substrate 100 so that the connecting portion 105 protrudes” (*id.*, 6, Fig. 2a). POSAs would perform these same steps to finish the Pyo-Choi image chip too, below.

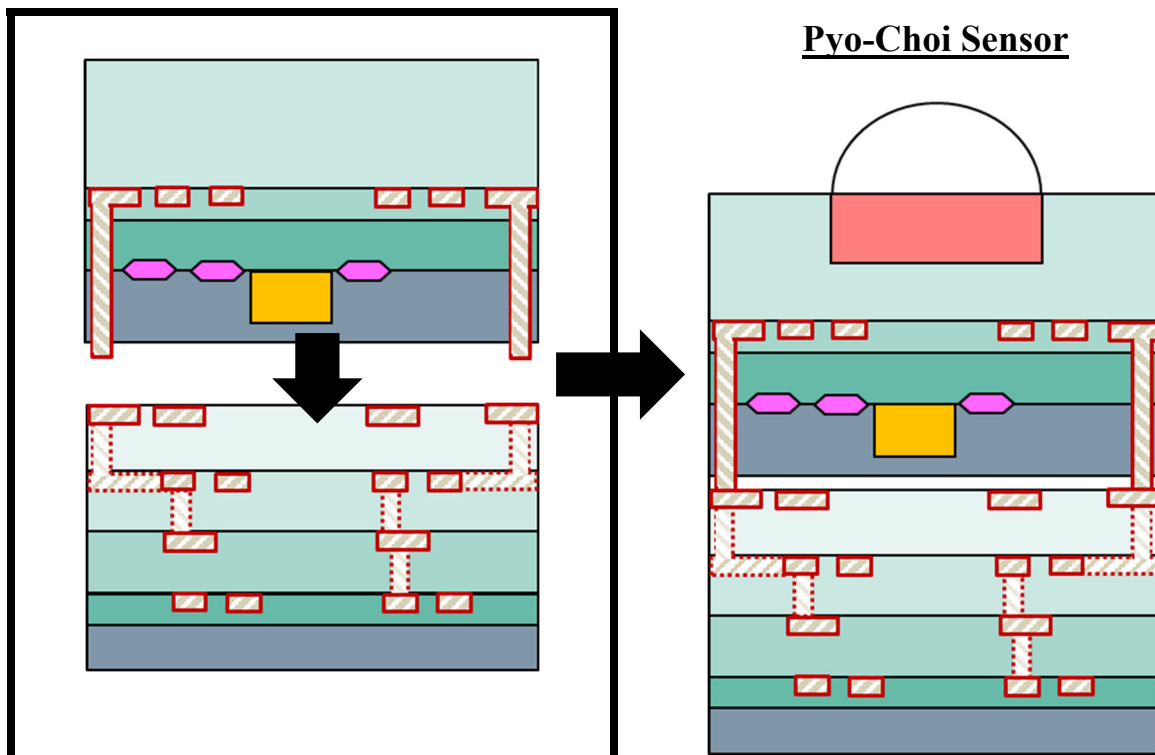


c. Bonding

196. Pyo discloses bonding the logic chip to the image chip and thereafter forming the “color filter array 107, the microlens 108, and the protective film 109.” *Id.*, 5-6, Figs. 2a, 2b, 3.



197. POSAs would have done the same for the Pyo-Choi Sensor, below.



3. Reasonable Expectation of Success

198. A POSA would have had a reasonable expectation success in modifying the Pyo sensor to use copper interconnections throughout.

199. **First**, Pyo itself discloses copper as a suitable material for its metal lines and vias. Pyo (Ex. 1005), 5 (“The connecting portion 105 comprises a metal such as tungsten, aluminum, or copper” and the “metal line 201 is formed using copper or aluminum.”). While Pyo does not specifically disclose the material used for the metal lines (104), Pyo’s silence on the material used for the metal lines (104) would tend to indicate they were made out of a common material and Pyo discloses common materials for the other interconnections. A POSA would have expected that if the metal lines (104) were made out of an unusual material, then Pyo would have disclosed what the material was—Pyo did not. A POSA would thus have had a reasonable expectation of successfully using the very same materials that Pyo discloses are suitable for other interconnections for all of the interconnections, including the metal lines (104) as well.

200. **Second**, a POSA would have known that the dual-damascene process used for copper interconnect fabrication was well-known by at least 2004. Doering (Ex. 1010), 4-5; Choi (Ex. 1007), [0139]; Quirk (Ex. 1014), 80. And this included for CMOS image sensors specifically. Gambino (Ex. 1023), 21. A POSA would

thus have had a reasonable expectation of implementing copper interconnections using such a well-known process.

4. Claim-by-Claim Analysis

201. The analysis below demonstrates that the Pyo-Choi Sensor meets each and every element of claims 1, 2, and 4-8 of the '366 patent.

a. Claim 1

202. The Pyo-Choi Sensor satisfies each and every limitation of claim 1 as explained below, rendering it obvious given the above-discussed reasons for the modification.

i. [1.pre]

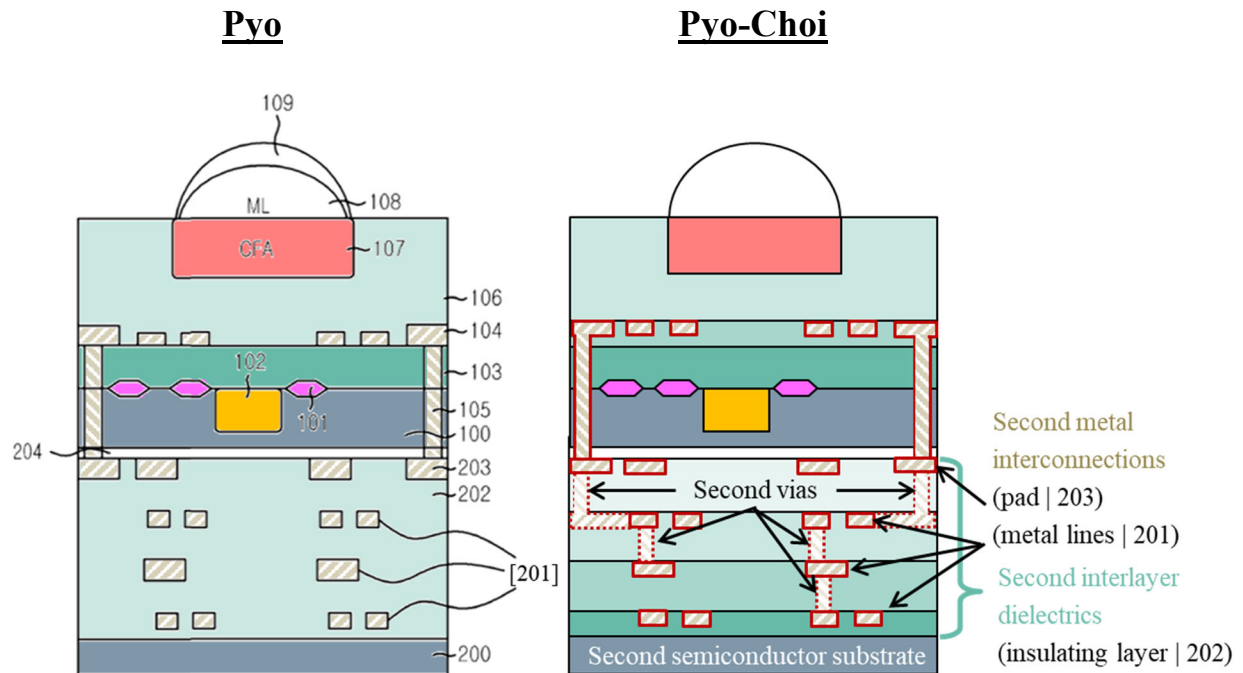
[1.pre] An image sensor, comprising:

203. To the extent the preamble is limiting, the Pyo-Choi Sensor satisfies the preamble because Pyo's device is an image sensor and that would remain unchanged after modification. Pyo (Ex. 1005), 2 ("The present invention is a ... solution to the *next-generation CMOS image sensor.*"), 3 ("The present invention relates to *an image sensor....*").

ii. [1.1]

[1.1] a second semiconductor substrate including a second metal interconnection and a second interlayer dielectric;

204. The Pyo-Choi Sensor satisfies limitation [1.1] because Pyo’s sensor has a second semiconductor substrate 200 including a pad 203, metal lines 201, each insulated by insulating layer 202, and these aspects would remain unchanged after modification while incorporating metal barrier layers, not relevant to limitation [1.1].



205. **Second semiconductor substrate:** Pyo discloses that its “logic chip [is] disposed on a *second substrate*,” which a POSA would understand is a *semiconductor* substrate because Pyo’s CMOS image sensor is a “*semiconductor* device.” *Id.*, 4. The same is true of the Pyo-Choi Sensor; Choi itself describes a CMOS-based image sensor incorporating a semiconductor substrate. Choi (Ex. 1007), [0040]-[0041], [0058]-0060], [0099]-[0100], [0114]-[0115], [0136], [0138].

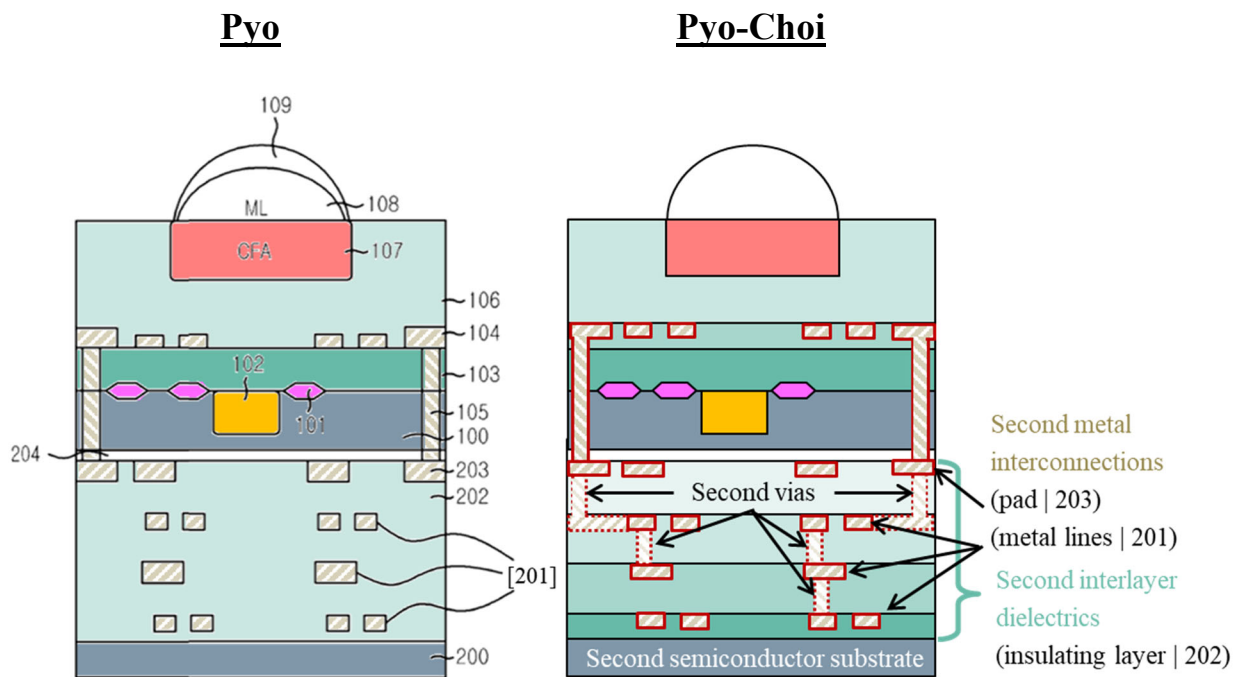
206. **Second metal interconnection:** Pyo discloses that “[a] plurality of metal lines 201 each surrounded by an insulating film 202 are formed on the second substrate 200” and “a pad 203” is formed “on the upper portion of [a] metal line,” as shown above. Pyo (Ex. 1005), 4, Fig. 3. A POSA would understand that “metal lines 201” and “pad 203” are interconnections because they are conductive metals forming “a logic element with 6-layer wiring” to carry the electrical signals to different parts of the chip. *Id.*, 5; *see also* Section IX.B (which starts on page 43, explaining the meaning of an “interconnection”). Any of the metal lines 201 and pads 203 thus satisfies the required “second metal interconnection” of limitation [1.1].

207. **Second interlayer dielectric:** Pyo further discloses that the metal lines and pads are formed in an “insulating layer 202” on the second substrate as shown above. Pyo (Ex. 1005), 5, Fig. 3A POSA would understand that the “insulating layer 202” is the claimed second interlayer dielectric because it is an insulating film between two conducting metals or adjacent metal lines. *See* Section IX.C (explaining the meaning of an “interlayer dielectric”). The “insulating layer 202” thus meets the requirement of the second interlayer dielectric of limitation [1.1].

iii. [1.2]

[1.2] a second via penetrating the second interlayer dielectric so that the second via is connected to the second metal interconnection;

208. The Pyo-Choi Sensor satisfies limitation [1.2], because Pyo's sensor has second vias, each penetrating the insulating layer 202 so that the second vias are each connected to the pad 203 and/or the metal lines 201 and these aspects would remain unchanged after modification.



209. Pyo discloses that the “pads 203 are **connected** to the plurality of metal lines 201” and the second substrate has a “a logic element with 6-layer wiring or more.” Pyo (Ex. 1005), 4-5, Fig. 3. A POSA would have understood that the pads 203 and the plurality of metal lines 201 are connected by one or more

vias. These vias each meet the claimed requirement of a second via because they penetrate the insulating layer 202 (second interlayer dielectric) to connect the pads 203 to the first level of metal lines 201 or to provide additional connections between the layers of metal lines 201, forming a logic element with 6-layer wiring or more.

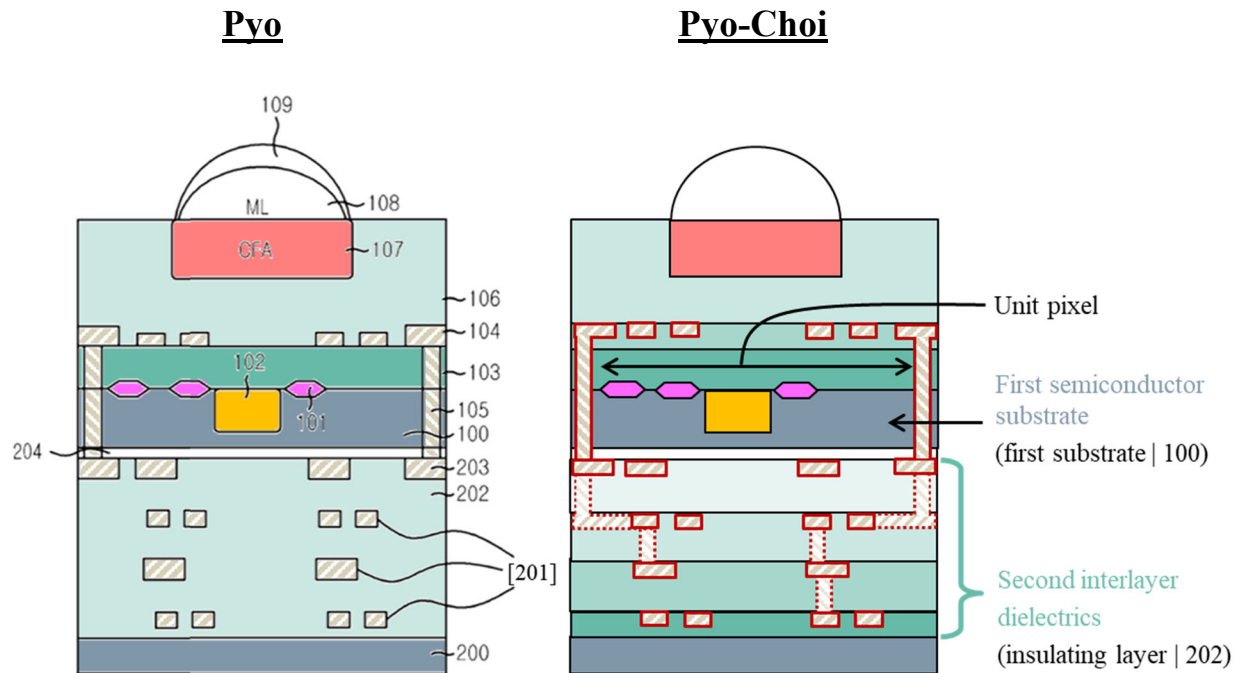
210. In any event, incorporating a via would also have been obvious because a via is defined as an interconnection that electrically connects two metal layers. *See* Section IX.D (which starts on page 45, explaining the meaning of a “via”); *see also* Quirk (Ex. 1014), 12 (“The *metal layers are connected by* openings in the dielectric film referred to as *vias.*”), 54; Brase (Ex. 1009), 1:40-45. Thus, by disclosing the pads 203 are connected to the metal lines 201 which form a logic element with 6-layer wiring or more, Pyo also renders obvious the claimed second via.

211. Any one of the vias shown above penetrate the “insulating layer 202” (second interlayer dielectric) to make the connection and thus meets the claimed second via of limitation [1.2].

iv. [1.3]

[1.3] a first semiconductor substrate on the second interlayer dielectric, the first semiconductor substrate having a unit pixel;

212. The Pyo-Choi Sensor satisfies limitation [1.3] because Pyo’s sensor has a first semiconductor substrate 100 having a unit pixel on the insulating layer 202 and these aspects would remain unchanged after modification.



213. **First semiconductor substrate:** Pyo discloses that its “image chip [is] disposed on a *first substrate*,” which a POSA would understand is a *semiconductor* substrate because Pyo’s CMOS image sensor is a “*semiconductor* device.” Pyo (Ex. 1005), 4. It would also have been obvious to include a semiconductor substrate because Choi discloses using a semiconductor substrate for its CMOS image sensor. Choi (Ex. 1007), [0040]-[0041], [0058]-0060], [0099]-[0100], [0114]-[0115], [0136], [0138].

214. **On the second interlayer dielectric:** The first semiconductor substrate is located “on” the second interlayer dielectric as shown above. Per the

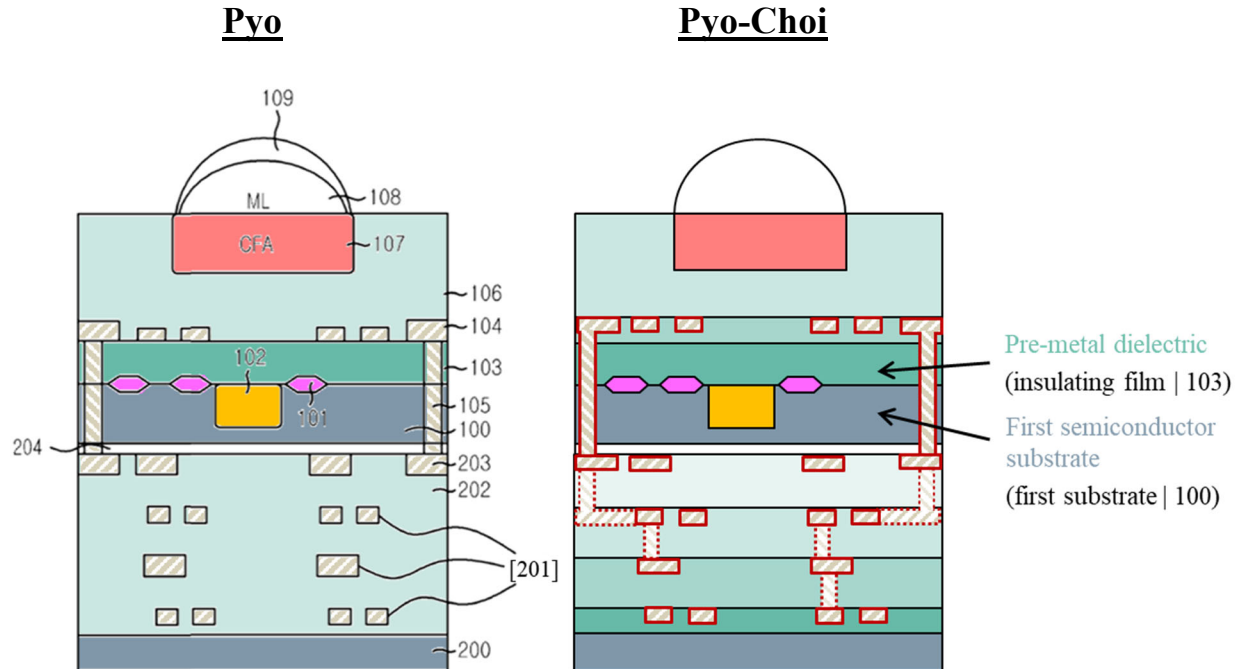
'366 patent's definition of "on," the first semiconductor substrate need not be directly in contact with the second interlayer dielectric because "intervening layers, regions, patterns, or structures may also be present." '366 patent, 2:17-22. Thus, the intervening bonding layer 204 (*see* Pyo (Ex. 1005), Fig. 3), for example, does not change that the first semiconductor substrate is located "on" the insulating film 202 (second interlayer dielectric).

215. **Having a unit pixel:** The Pyo-Choi Sensor meets the unit pixel requirement because Pyo discloses that its first semiconductor substrate has a unit pixel, which would not be impacted by the modification to incorporate copper interconnects throughout. *Id.*, 5 (After "the photodiode 102 is formed on the first substrate 100," a "plurality of transistors *constituting a unit pixel*, such as a transfer transistor, are formed" and the "metal line[s] for interconnecting the transistor[s] *constitute[e] the unit pixel.*").

v. [1.4]

[1.4] a pre-metal dielectric on the first semiconductor substrate;

216. The Pyo-Choi Sensor satisfies limitation [1.4] because Pyo's sensor has an insulating film 103 on the first semiconductor substrate 100 and these aspects would remain unchanged after modification.



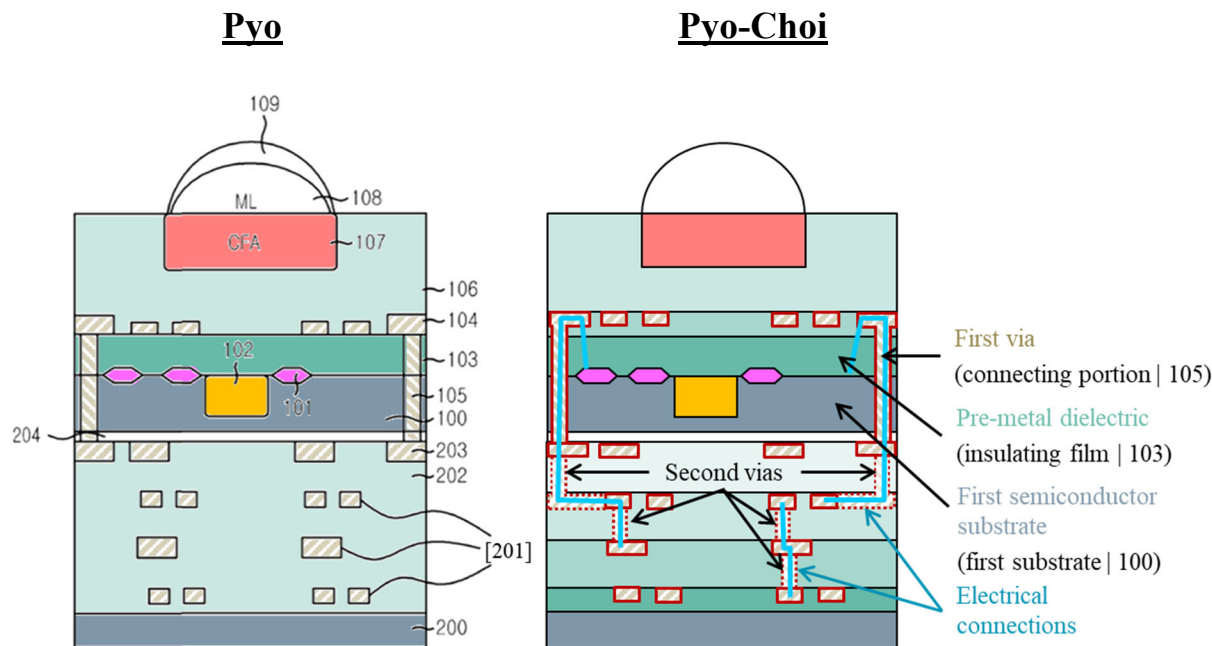
217. Pyo discloses “an insulating film 103” above the first substrate 100 and below the metal line 104. Pyo (Ex. 1005), 6, Fig. 3. A POSA would understand this insulating film 103 to be a “pre-metal dielectric” because it is in between the active devices (i.e., the photodiode and unit pixel transistors) and the metal lines 104. *See* Section IX.E (which starts on page 47, explaining the meaning of “pre-metal dielectric”).

vi. [1.5]

[1.5] a first via penetrating the pre-metal dielectric and the first semiconductor substrate, the first via being connected to the second via;

218. The Pyo-Choi Sensor satisfies limitation [1.5] because Pyo’s sensor has a connecting portion 105 that penetrates the insulating film 103 and first

substrate 100, which is connected to the second vias that are part of the second substrate and these aspects would remain unchanged after modification.



219. First via penetrating the pre-metal dielectric and the first semiconductor substrate: Pyo discloses “a connecting portion 105 connected to the metal line 104 through the rear surface of the first substrate 100,” penetrating the insulating film 103 (pre-metal dielectric) and the first semiconductor substrate. Pyo (Ex. 1005), 6, Fig. 3. A POSA would recognize that the connecting portion 105 as a via because it electrically connects different metal interconnection layers. *See* Section IX.D (which starts on page 45, explaining the meaning of a “via”).

220. Being connected to the second via: As illustrated above, Pyo discloses that the connecting portion 105 (first via) is electrically connected to the pad 203 and metal lines 201 (second metal interconnects) of the logic chip on the

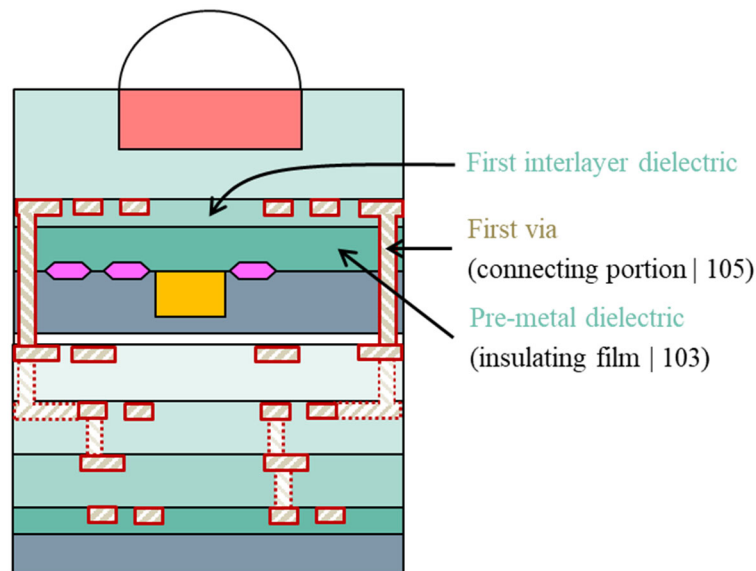
second substrate. Pyo (Ex. 1005), 6 (“[T]he connecting portion 105 needs to be **connected** to the logic chip.” “[T]he pad 203 must be **connected** to the connecting portion 105.” “[T]he pad 203 [is] connected to the metal line[s] 201.”), 5 (“[T]he plurality of transistors are **connected** to the pads 203 of the second substrate 200 through the connecting portion 105 penetrating the first substrate 100, and the pads 203 are **connected** to the plurality of metal lines 201.” “The metal line 104 is **connected** to the pad 203 through the connecting portion 105.”).

221. A POSA would understand that “connected” encompasses electrical connections because the ’366 patent discloses that the connections in the disclosed embodiment include electrical connections. *See* ’366 patent, Abstract (“the first via being **electrically connected** to the second via”), 1:42-44 (“first via penetrating the pre-metal dielectric and the first semiconductor substrate to **electrically connect** with the second via”), 2:65-3:4 (“The second via 230 is disposed under the first via 110 and can be **electrically connected** to the first via 110. That is, the first semiconductor substrate 100 and the second semiconductor substrate 200 can be **electrically connected** together through the first via 110 and the second via 230.”). Moreover, at least one embodiment connects the two vias “using polymer,” such that the two vias would not even be physically touching—permitting only an electrical connection. *Id.*, 7:5-8.

vii. [1.6]

[1.6] a first interlayer dielectric on the pre-metal dielectric including the first via;

222. The Pyo-Choi Sensor satisfies limitation [1.6] because, as explained in Section XI.A.2 (*see* page 75), and as shown in the figure below, the Pyo-Choi Sensor would have a first interlayer dielectric on the pre-metal dielectric including the first via.



223. Pyo discloses that the standard way to form metal lines is using “an inter-metal dielectric (IMD)” layer. Pyo (Ex. 1005), 6; *see also id.*, 4 (“the metal line process, is similar to the manufacturing process of the semiconductor device” and “different insulating materials must be used to form PMD (Pre-Metal Dielectric), IMD (Inter-Metal Dielectric)...”). A POSA would understand that Pyo’s inter-metal dielectric constitutes a first interlayer dielectric because it is an

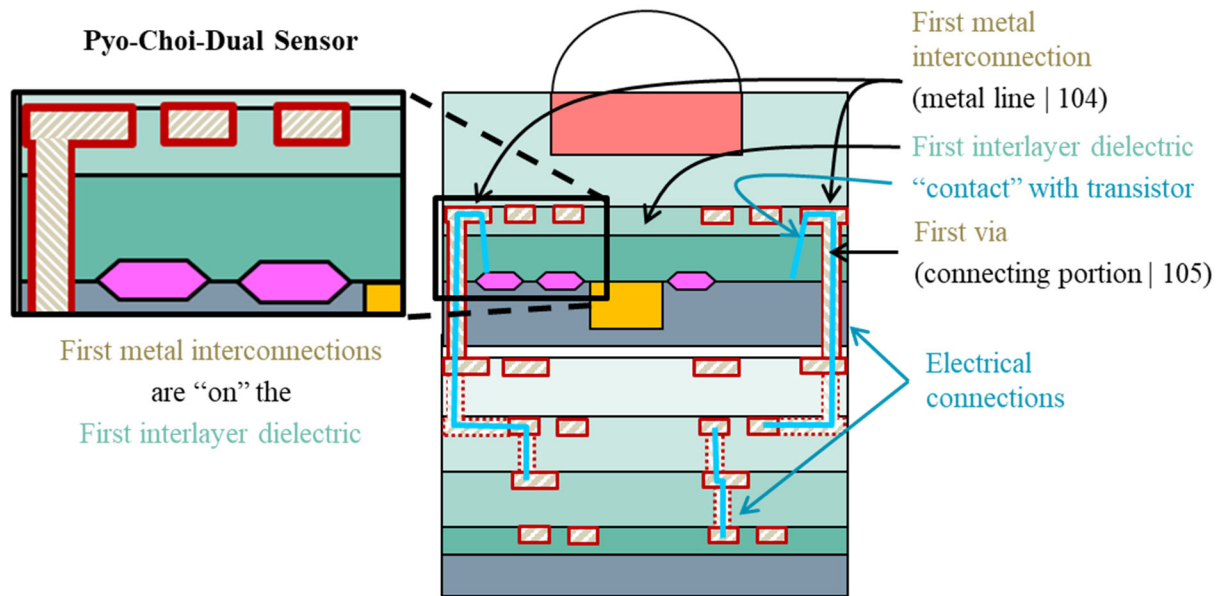
insulating film between two adjacent metal lines. *See* Section IX.C (which starts on page 44, explaining the meaning of “interlayer dielectric”).

224. The Pyo-Choi Sensor has an interlayer dielectric as shown above resulting from a damascene process. *See* Sections XI.A.2.b (which starts on page 87). The ILD would be located on the pre-metal dielectric because that is where Pyo discloses the metal lines 104 are located. Pyo (Ex. 1005), 6 (“an insulating film 103 is deposited and [then] a metal line 104”), Fig. 3. In the Pyo-Choi Sensor, metal lines 104 would be copper and fabricated using the dual-damascene process, including placement of an ILD.

viii. [1.7]

[1.7] a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel;

225. The Pyo-Choi Sensor satisfies limitation [1.7] because, as explained in Section XI.A.2.b (*see* page 87), and as shown in figure below, the Pyo-Choi Sensor would have a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel.



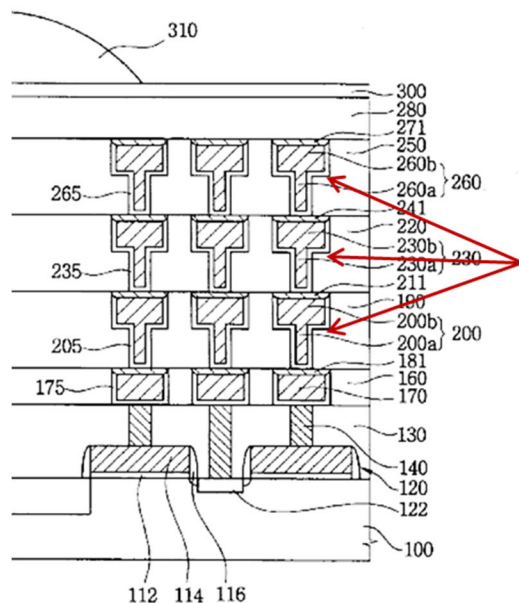
226. **First metal interconnection connected to the first via and the unit pixel:** Pyo describes "[r]eference number '104'" as "a metal line." Pyo (Ex. 1005), 5. A POSA would understand the "metal line 104" is a metal interconnection because Pyo discloses it is "for *interconnecting* the transistor constituting the unit pixel and the lower portion metal line 201," that the "metal line 104 is *connected* to the pad 203 through the connecting portion 105," and that the "metal line 104 [is] *connected* to the gate electrode or source/drain of the transistor through a contact." *Id.*, 5-6.

227. The metal line 104 thus carries the electrical signal from the unit pixel to the logic chip, meeting the definition of an interconnection. *See* Section IX.B (which starts on page 43, explaining the meaning of an "interconnection"). The electrical connection from the unit pixel through the metal line 104 and down to the logic chip includes the metal line 104 being connected to the connecting

portion 105 (first via) as shown in blue above. Pyo (Ex. 1005), Fig. 3. The metal line 104 thus meets the requirements of the first metal interconnect in limitation [1.7].

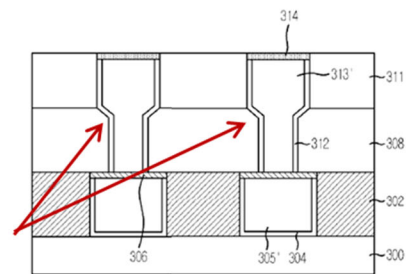
228. **“On” the first interlayer dielectric:** The Pyo-Choi Sensor would locate the metal line 104 (first metal interconnection) “on the first interlayer dielectric” because that is how the well-known dual-damascene process for implementing copper-based lines would dictate placement of the line as shown below.

Dual-Damascene Interconnections

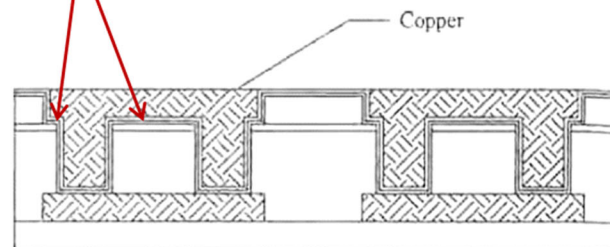


Choi Fig. 4 (excerpt)

Dual-damascene metal lines are “on” the interlayer dielectric



Yun Fig. 3j



Quirk, 82

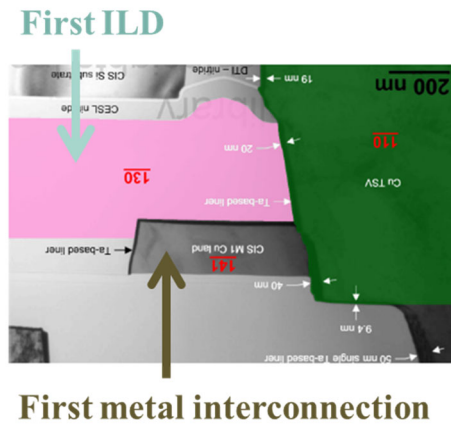
229. For example, Choi discloses that its metal interconnections (reference numbers 200b, 230b, and 260b) are all on the interlayer dielectric (reference numbers 190, 220, and 250). Choi (Ex. 1007), [0106], [0108], [0110], Fig. 4. Yun

and Quirk disclose similar structures where the metal lines are on the first interlayer dielectric. Yun (Ex. 1017), 12-13, Fig. 3j (the “metal line and the via contact 313” is on the “dielectric layer 308”); Quirk (Ex. 1014), 80-82 (showing the copper is on the “ILD oxide”).

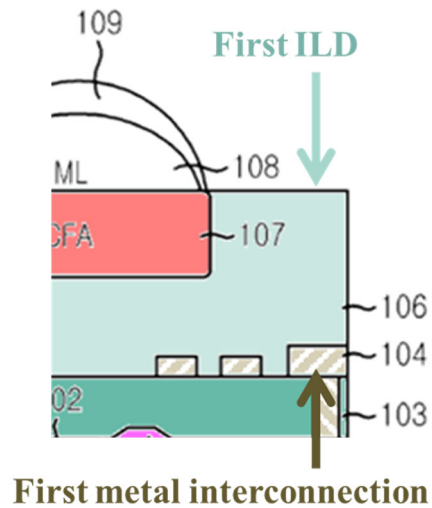
230. It would have been obvious to locate the metal line 104 (first metal interconnection) on the first interlayer dielectric as claimed in limitation [1.7] in the process of incorporating copper interconnects as previously discussed and in particular using the dual-damascene process given the “dual-damascene process became the consensus process for copper metallurgy” by at least 2001 (Quirk (Ex. 1014), 80; *see also* Pratt (Ex. 1013), 8-10; Doering (Ex. 1010), 4). The Pyo-Choi Sensor therefore would include “a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel” as claimed in limitation [1.7].

231. But even if the metal line 104 was located as shown in Figure 3, a POSA would still understand that to be within the scope of limitation [1.7] under VisionX’s interpretation as explained in Section IX.A, which begins on page 39, because the metal lines (104) in Figure 3 are at least adjacent to the first interlayer dielectric, and would remain so when using an interlayer dielectric in a damascene process, and thus fall within the scope of limitation [1.7] under VisionX’s interpretation.

Accused Product



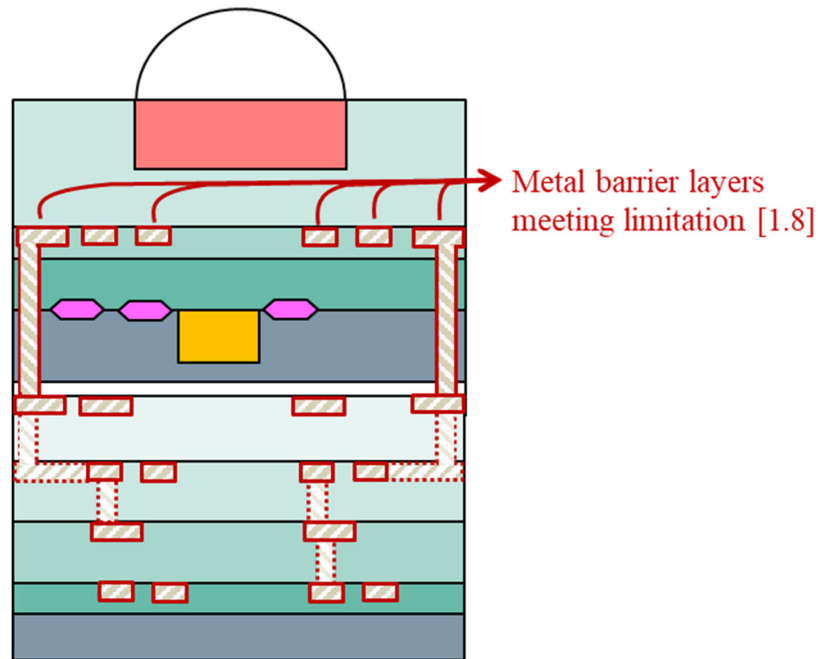
Pyo, Fig. 3 (excerpt, annotated)



ix. [1.8]

[1.8] a conductive barrier layer on the first metal interconnection; and;

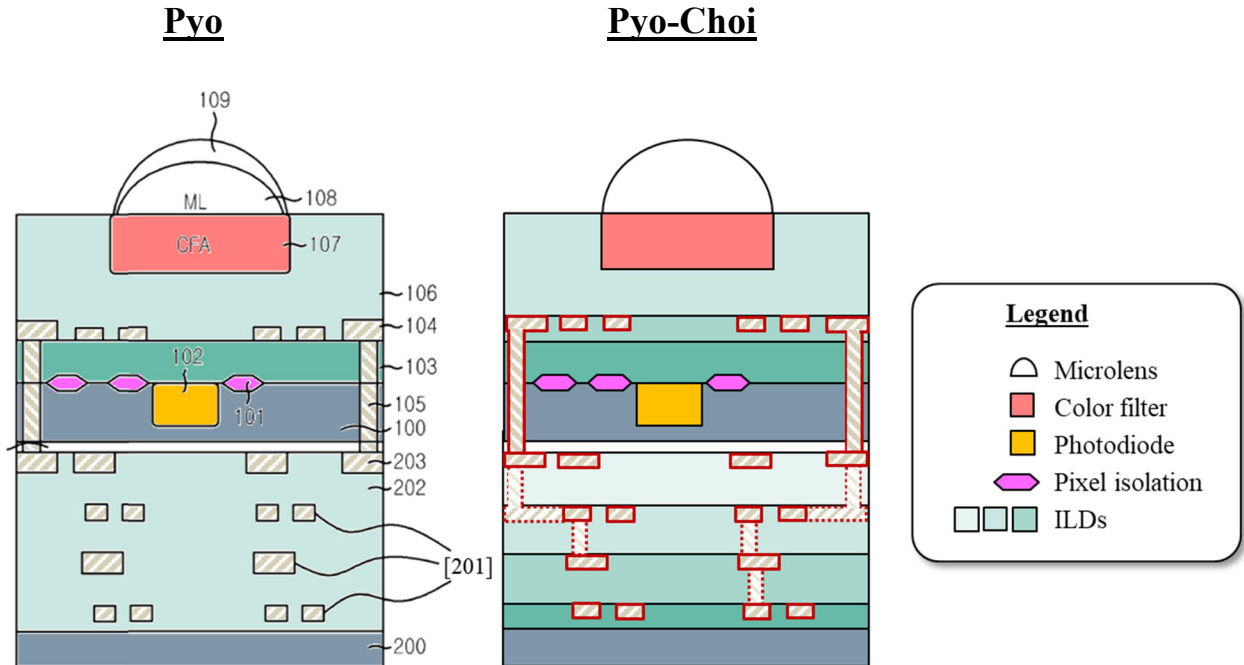
232. The Pyo-Choi Sensor satisfies limitation [1.8] because, as explained further in Section XI.A.2.b (*see* page 87), and as shown in the figure below, in modifying Pyo to use copper lines and vias, a POSA would have used a conductive metal barrier layer on the copper interconnections to prevent the copper from diffusing into the dielectric and prevent the dielectric from oxidizing the copper.



x. [1.9]

[1.9] a color filter and a microlens on the first interlayer dielectric on the unit pixel.

233. The Pyo-Choi Sensor satisfies limitation [1.9] because Pyo's sensor has a color filter 107 and a microlens 108 and these aspects would remain unchanged after modification.



234. Pyo discloses its “image chip” has “a color filter array and a microlens.” Pyo (Ex. 1005), 4; *see also id.*, 5 (pointing out “a color filter array 107” and a “microlens 108” as shown in Figure 3), Fig. 3. Per the ’366 patent’s definition of “on,” the color filter and microlens need not be directly in contact with the first interlayer dielectric or unit pixel; instead, “intervening layers, regions, patterns, or structures may also be present.” ’366 patent, 2:17-22. The color filter array 107 and the microlens 108 are thus on the first interlayer dielectric and unit pixel as shown above, meeting limitation [1.9]. These features would not be impacted by the above-noted modifications and use of the dual-damascene process as disclosed in Choi; even Choi’s image sensor included a “microlens formed on the color filter,” which is “formed on the upper insulation layer.” Choi (Ex. 1007), [0024].

b. Claim 2

2. The image sensor according to claim 1, wherein the first metal interconnection comprises copper (Cu).

235. As explained further above in Section XI.A.2 (which starts on page 75), a POSA would have modified the Pyo sensor to use copper lines and vias throughout, including for the first metal interconnection. The Pyo-Choi Sensor thus satisfies the additional limitation of claim 2, rendering it obvious given the above-discussed reasons for the modification.

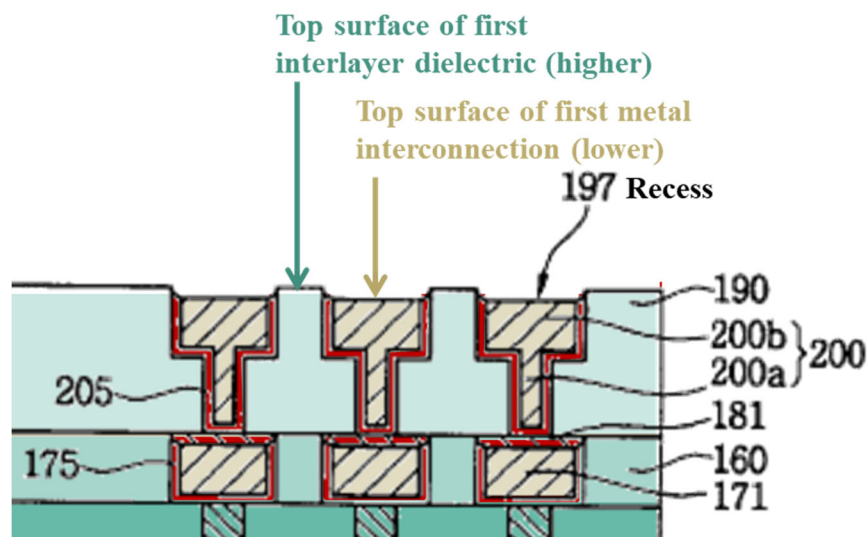
c. Claim 4

4. The image sensor according to claim 1, wherein the first metal interconnection has a top surface lower than that of the first interlayer dielectric, such that the first metal interconnection and the first interlayer dielectric have a height difference.

236. As explained further above in Section XI.A.2.b (which starts on page 87), polishing of the copper in the dual-damascene process to create a recess for the top barrier layer was common and would have been an obvious step when implementing the dual-damascene process for the Pyo-Choi Sensor. Choi specifically discloses polishing the copper to create a “recess 197,” or a height difference, such that the first metal interconnection has a top surface lower than

that of the first interlayer dielectric. Choi (Ex. 1007), [0128]-[0129], Figs. 5E, 5F (excerpted and annotated below), and 5G.

Choi Fig. 5F (Excerpted & Annotated)



237. In implementing the dual-damascene process for the Pyo-Choi Sensor, a POSA would have likewise polished the copper such that its top surface was lower than that of the first interlayer dielectric as disclosed by Choi. The Pyo-Choi Sensor thus satisfies the additional limitation of claim 4, rendering it obvious given the above-discussed reasons for the modification.

d. Claim 5

5. The image sensor according to claim 1, wherein the second metal interconnection comprises copper (Cu) or aluminum (Al).

238. Pyo discloses the “metal line 201 [(the second metal interconnection)] is formed using copper or aluminum.” Pyo (Ex. 1005), 5. A POSA would have

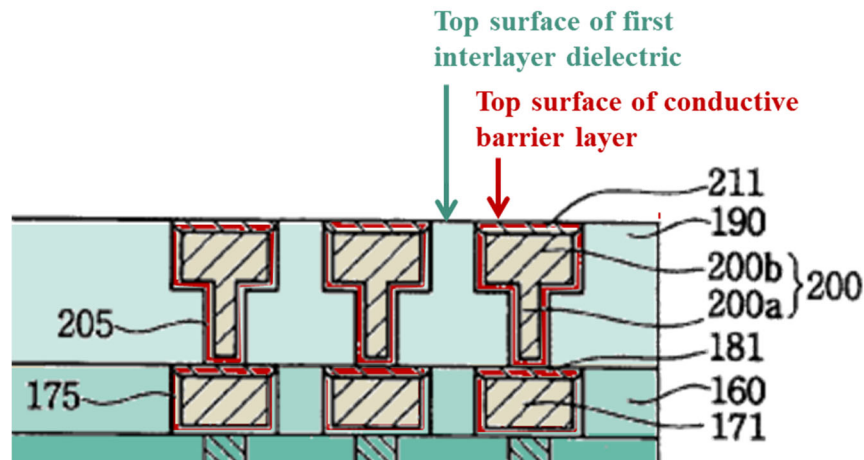
used copper lines and vias throughout, including for the second metal interconnection as explained in Section XI.A.2 (which starts on page 75). The Pyo-Choi Sensor thus satisfies the additional limitation of claim 5, rendering it obvious given the above-discussed reasons for the modification.

e. Claim 6

6. The image sensor according to claim 1, wherein the conductive barrier layer has at top surface substantially even with the top surface of the first interlayer dielectric.

239. As explained for claim 4, Choi discloses creating a recess 197 in the polishing step of the dual-damascene process. Choi also discloses depositing a barrier layer and then planarizing using CMP such that the top surface of the barrier layer is even with the top surface of the first interlayer dielectric. Choi (Ex. 1007), [0129] (referencing back to [0122]-[0123]), Fig. 5G (excerpted and annotated in red below).

Choi Fig. 5G (Excerpted & Annotated)



240. In implementing the dual-damascene process for the Pyo-Choi Sensor, a POSA would have likewise fabricated a conductive metal barrier layer in the recess above the copper lines and then polished the structure so that the top surface of the barrier layer was substantially even with the top surface of the first interlayer dielectric. The Pyo-Choi Sensor thus satisfies the additional limitation of claim 6, rendering it obvious given the above-discussed reasons for the modification.

f. Claim 7

7. The image sensor according to claim 1, wherein the first via and the second via comprise the same material.

241. As explained in Section XI.A.2 (which starts on page 75), a POSA would have modified the Pyo sensor to use copper lines and vias throughout, including for the first and second vias. The Pyo-Choi Sensor thus satisfies the

additional limitation of claim 7, rendering it obvious given the above-discussed reasons for the modification.

g. Claim 8

8. The image sensor according to claim 1, wherein the second semiconductor substrate provides metal interconnections for connection to a power line and an external signal line.

242. Metal interconnections for power and signal lines were standard and universal for semiconductor devices and would have been a standard way to implement a CMOS image sensor. POSAs would have recognized the desirability to make the Pyo-Choi Sensor operational by connecting the metal interconnections to a power line and an external signal line—thereby sending the electrical signals required to operate the sensor and the electrical signals the sensor generates from optical images. Edelstein (Ex. 1011), 10 (requiring “DC power distribution, [and] off-chip I/O”); Imaoka (Ex. 1006), [0049] (requiring a “power supply terminal” and an “input/output terminal”); Choi (Ex. 1007), [0005] (“A complementary MOS image sensor (CIS) converts an optical image into an electrical signal.”).

243. POSAs would have understood where Pyo placed such interconnections for the power line and external signal line and therefore the place to locate such interconnections in the Pyo-Choi Sensor would be on the second

substrate. Pyo discloses it was desirable to remove such interconnections from the image chip to the logic chip in order to improve the performance of the sensor. Pyo (Ex. 1005), 5 (“by removing the multi-layer consisting of a plurality of metal lines 201 and an insulating film 202 [from the image chip], it is possible to maximize photosensitivity”). Pyo further discloses that the metal interconnections for the first substrate are used for connecting unit pixel transistors and providing a light shield for the transistors. *Id.*

244. A POSA would thus have included the metal interconnections for connection to a power line and an external signal line to make the sensor operational on the second semiconductor substrate, rendering claim 8 obvious.

B. Ground 2: Pyo in view of Choi and Dublin Renders Claim 3 Obvious

245. Claim 3 depends from claim 1 and further requires cobalt (Co) or nickel (Ni) alloy for the conductive barrier layer. But as of 2007, Dublin disclosed a cobalt tungsten phosphide (CoWP) alloy as a preferred option for a for a conductive barrier layer in copper interconnections. Claim 3 would therefore have been obvious over Pyo in view of Choi (as previously discussed concerning claim 1) and further in view of Dublin.

1. Reasons to Use a CoWP Barrier Layer

246. For all the reasons set forth in Section XI.A.1, a POSA would have been motivated to combine Pyo and Choi and obtain the Pyo-Choi Sensor as described in Section XI.A.2 (which starts on page 75).

247. A POSA would have been further motivated to use Dublin's CoWP as the conductive metal barrier layer instead of those disclosed by Choi.

248. **Enhanced barrier properties:** Dublin acknowledges the materials used by Choi as barrier layers were known. *Compare* Dublin (Ex. 1008), 2:25-57 (disclosing Ta, W, TaN, and WN as copper barrier materials) *with* Choi (Ex. 1007), [0066] and [0071] (same). Dublin discloses, however, that CoWP “significantly enhances the barrier properties,” making it “preferred.” Dublin (Ex. 1008), 3:1-7. CoWP alloy allows for “increased thermal stability, improved corrosion resistance and mechanical properties (such as wear resistance).” *Id.*, 5:17-23. A POSA would thus have been motivated to use this preferred material for its enhanced properties.

249. **Eliminates polishing step:** In addition, Dublin discloses that CoWP can be selectively deposited on copper, eliminating the need for Choi's final polishing step. *Id.*, 8:66-9:3; Choi (Ex. 1007), [0122]-[0123], [0129]. Using the CoWP would thus simplify the manufacturing process. Quirk (Ex. 1014), 82 (“Reducing process steps in wafer fabrication is important for improving the yield

of the process, since fewer process steps translate to fewer sources of error that reduce assembly yield.”). A POSA would thus have been motivated to use CoWP for its selective deposition properties.

250. **Simple substitution:** Finally, using Dublin’s CoWP barrier material would have been nothing more than simple substitution. Dublin discloses that its CoWP barrier layer used the damascene process as a copper barrier layer. *Id.*, 8:1-65. Thus, Dublin’s CoWP alloy could readily replace Ta, W, TaN, and WN materials. Indeed, this was the very thing my team at Kodak did in 2005 when we substituted a CoWP barrier layer for a SiN barrier layer disclosed by the basic process disclosed in 1999. Gambino (Ex. 1023), 25. Using Dublin’s CoWP alloy instead of those disclosed by Choi would thus have been nothing more than simple substitution.

2. Resulting Sensor and Reasonable Expectation of Success

251. The sensor resulting from using Dublin’s CoWP alloy would have an identical structure to the Pyo-Choi Sensor as described in Ground 1 except the conductive metal barrier layer would be made from CoWP.

252. A POSA would have had a reasonable expectation of successfully using the CoWP alloy because Dublin discloses that its CoWP barrier layer is fabricated using a damascene process like the one used to fabricate the Pyo-Choi Sensor. *Compare* Section XI.A.2.b *with* Dublin, 8:1-65. And again, this was the

very thing my team at Kodak did in 2005 when we substituted a CoWP barrier layer for a SiN barrier layer disclosed by the basic process disclosed in 1999. Gambino (Ex. 1023), 25. A POSA would thus have reasonably expected a similar substitution to work for the Pyo-Choi Sensor as well.

3. Claim 3 Analysis

3. The image sensor according to claim 1, wherein the conductive barrier layer comprises cobalt (Co) or nickel (Ni) alloy.

253. The resulting sensor includes a conductive metal barrier layer that comprises cobalt (Co) alloy (i.e., CoWP), thereby fulfilling the additional element of claim 3 and rendering the claim obvious. Dublin discloses a “technique of electrolessly depositing CoWP as a barrier material in order to protect or encapsulate a conductive material” such as “copper.” Dublin (Ex. 1008), 2:63-66. Figure 10 of Dublin “is a cross-sectional view showing a selective formation of another CoWP barrier layer of the present invention above the copper.” *Id.*, 3:53-55. CoWP is conductive. Ex. 1020, 1:22-23 (“a conductive barrier film such as cobalt tungsten phosphorous (CoWP) is formed on a Cu wiring”).

C. Ground 3: Imaoka Anticipates Claims 1, 2, and 4-8

254. Imaoka’s sensor meets every element of claims 1-2 and 4-8 under Patent Owner’s claim interpretations in the Texas Litigation, anticipating those claims.

1. Claim 1

a. [1.pre]

[1.pre] An image sensor, comprising:

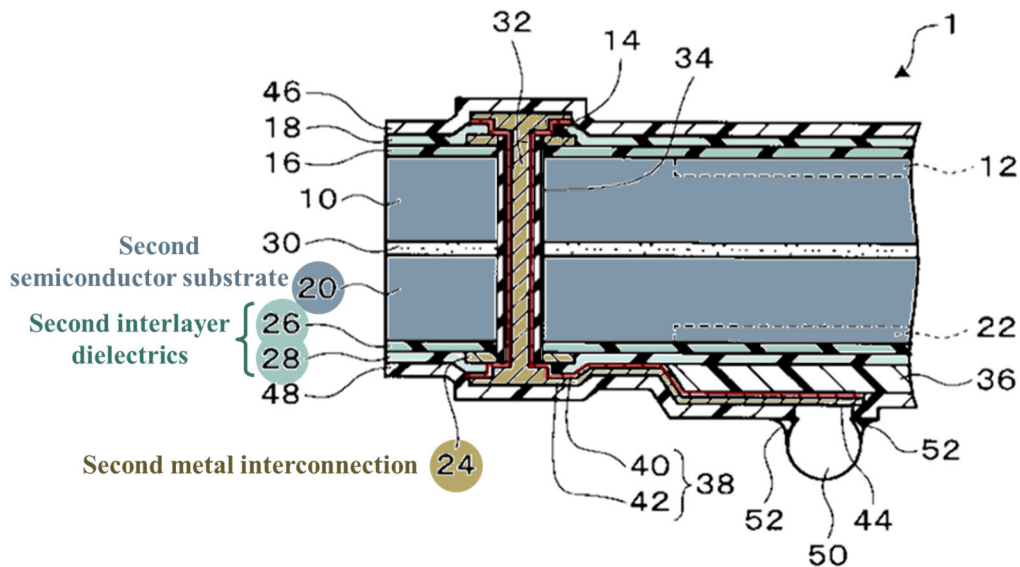
255. To the extent the preamble is limiting, Imaoka's device is an image sensor. Imaoka (Ex. 1006), [0006] ("In this optical device, ... [the] light-receiving elements may be arrayed for *image sensing*."), [0011] ("the optical device may be an *image sensor* (for example, ... a CMOS *image sensor*)").

b. [1.1]

[1.1] a second semiconductor substrate including a second metal interconnection and a second interlayer dielectric;

256. **Second semiconductor substrate:** Imaoka includes "second semiconductor substrate 20" with "pad 24" and "passivation films 26 and 28." *Id.*, [0010], Fig. 3 (below, annotated).

Imaoka, Fig. 3 (Annotated)



257. **Second metal interconnection:** A POSA would understand that the pad 24 is a second metal interconnection because Imaoka discloses it “may be formed of an aluminum type or a copper type of metal” (*id.*, [0009], [0010] (noting “contents of the second semiconductor substrate 20 may be the same as the above-mentioned first semiconductor substrate 10”)) and it connects the signal from the via to the integrated circuit 22 on the second semiconductor. *Id.*, [0018] (“The conductive part 38 is electrically connected to at least one (both in Fig. 3) of the first and the second pad 14 and 24.”). Imaoka also discloses that the pad 24 is connected to an electrical connection 44. *Id.*, [0019] (“electrical connection part 44 may ... overlap the second pad 24”). A POSA would have thus understood that the pad 24 is an interconnection. *See* Section IX.B (which starts on page 43, explaining the meaning of “interconnection”).

258. **Second interlayer dielectric:** A POSA would understand that passivation films 26 and 28 are insulators because the pads 24 are in direct contact with each film and if both films were not insulators, it would cause a short circuit between the various pads 24. Imaoka (Ex. 1006), Figs. 2, 3. In addition, Imaoka also discloses that passivation films 16 and 18 could be made from “SiO₂, SiN, [and] a polyimide resin” (*id.*, [0009]), each of which are insulators. Imaoka discloses “[o]ther contents of the second semiconductor substrate 20,” such as passivation films 26 and 28 “may be the same as the above-mentioned first semiconductor substrate 10,” making passivation films 26 and 28 insulators as well. *Id.*, [0010]. A POSA would understand that films 26 and 28, are an interlayer dielectric because the films are insulating between two conducting metals such as the plurality of pads 24. *See* Section IX.C (which starts on page 44, explaining the meaning of “interlayer dielectric”).

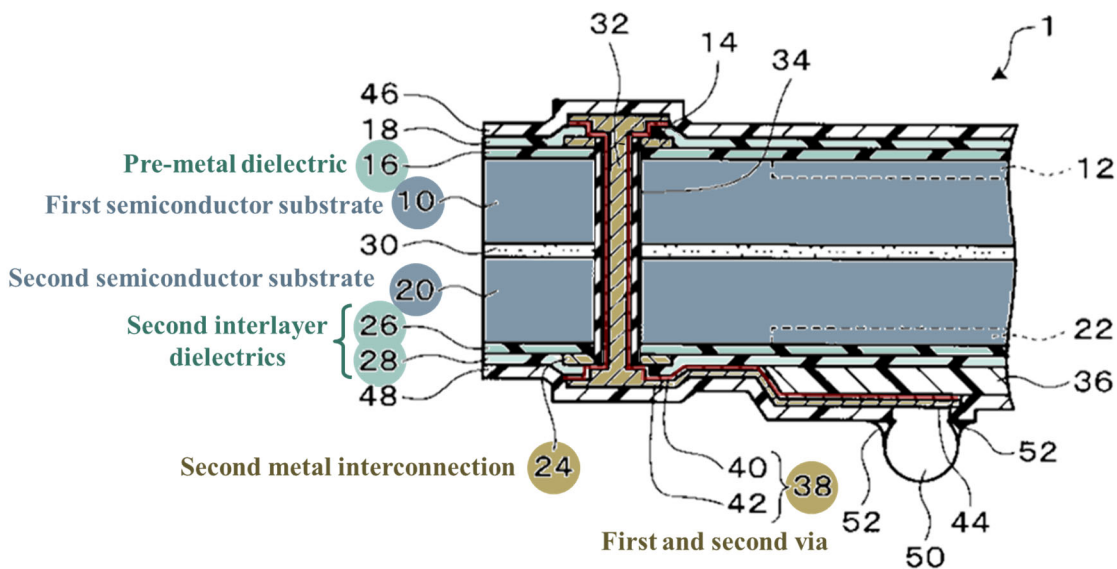
c. [1.2]

[1.2] a second via penetrating the second interlayer dielectric so that the second via is connected to the second metal interconnection;

259. Imaoka discloses a “conductive part 38” that electrically connects the first and second substrates. Imaoka (Ex. 1006), [0018]-[0020]; Fig. 3. A POSA would understand the conductive part 38 is a via because it forms an electrical

pathway from one metal layer to another. *See* Section IX.D (which starts on page 45, explaining the meaning of “via”). As seen in Figure 3, the conductive part 38 penetrates the passivation films 26 and 28 (second interlayer dielectrics). Imaoka also discloses that “[t]he conductive part 38 is electrically connected to at least one (both in Fig. 3) of the first and the second pad 14 and 24.” Imaoka (Ex. 1006), [0018].

Imaoka, Fig. 3 (Annotated)



260. A POSA would understand that the term “connected” in limitation [1.2] includes electrical connections because the ’366 patent discloses that the connections in the disclosed embodiment include electrical connections. *See* ’366 patent, Abstract (“the first via being *electrically connected* to the second via”), 1:42-44 (“first via penetrating the pre-metal dielectric and the first semiconductor substrate to *electrically connect* with the second via”), 2:65-3:4

(“The second via 230 is disposed under the first via 110 and can be *electrically connected* to the first via 110. That is, the first semiconductor substrate 100 and the second semiconductor substrate 200 can be *electrically connected* together through the first via 110 and the second via 230.”). Imaoka thus discloses that the conductive part 38 is connected to pad 24 (the second metal interconnection).

261. While Imaoka discloses only a single “conductive part 38 [that] is formed inside the through-hole 32,” under VisionX’s construction (*see* Section IX.D, which starts on page 45), Imaoka’s conductive part 38 satisfies every requirement of both the first and second via. Specifically, the conductive part 38: (i) penetrates the passivation films 26 and 28 (second interlayer dielectrics) (*see* Imaoka (Ex. 1006), Fig. 3), (ii) is connected to the pad 24 (second metal interconnection) (*see id.*, [0018], Fig. 3), (iii) penetrates the pre-metal dielectric and first semiconductor substrates and is a single via and thus the first and second vias are “connected” as required by limitation [1.5] (*see* annotated Fig. 3, above), and (iv) the first metal interconnection is connected to it (*see* annotated Fig. 3, above). Imaoka (Ex. 1006), [0018]-[0020]; Fig. 3. The single conductive part 38 also performs the same functions of the first and second vias because it forms an electrical pathway from the first metal interconnection past the bond between the first and second semiconductor substrates through to the second metal interconnection. *Id.*, [0018]-[0020]; Fig. 3.

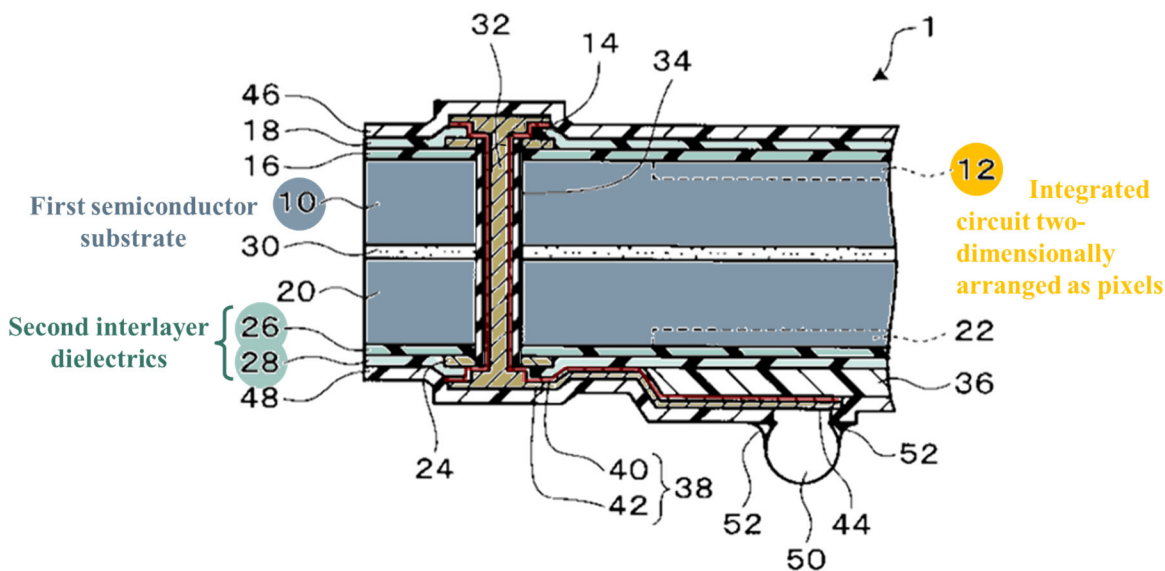
d. [1.3]

[1.3] a first semiconductor substrate on the second interlayer dielectric, the first semiconductor substrate having a unit pixel;

262. **First semiconductor substrate on the second interlayer dielectric:**

Imaoka discloses that “the first and the second semiconductor substrates 10 and 20 may be bonded to each other.” *Id.*, [0015]. As seen in the annotated Figure 3, below, the first semiconductor substrate is located above the passivation films 26 and 28 (second interlayer dielectrics), thus meets the requirement of being “on” it notwithstanding other intervening layers. ’366 patent, 2:17-22.

Imaoka, Fig. 3 (Annotated)



263. **Having a unit pixel:** A POSA would understand the first semiconductor substrate has a unit pixel because Imaoka discloses that “[a]

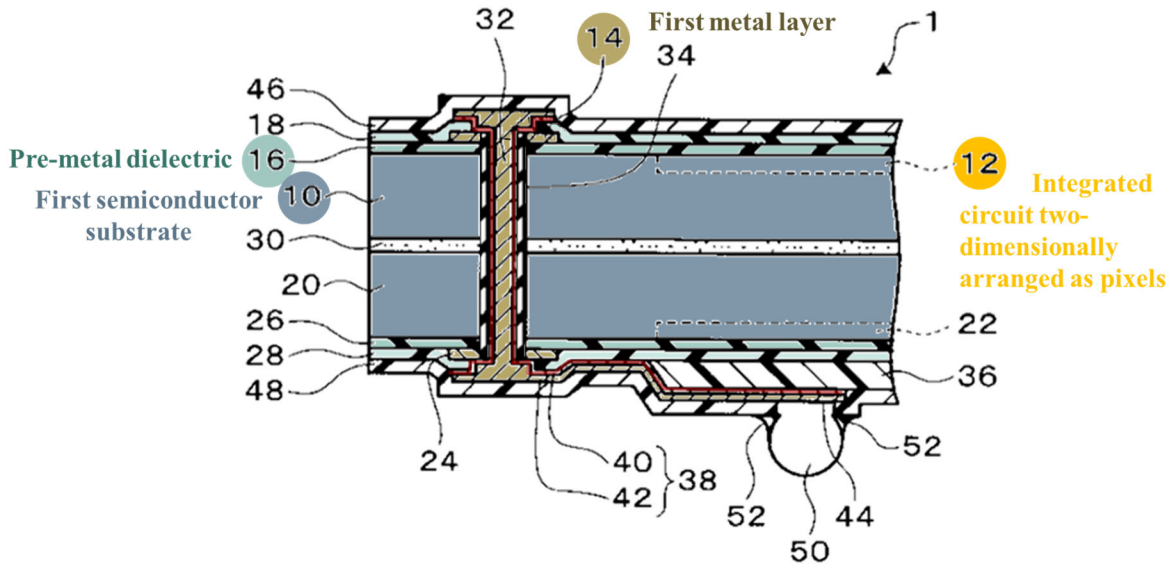
plurality of light receiving elements may be so disposed [on the first semiconductor substrate 10] as to enable image sensing by corresponding to each of a plurality of pixels two-dimensionally arrayed.” Imaoka (Ex. 1006), [0011].

e. [1.4]

[1.4] a pre-metal dielectric on the first semiconductor substrate;

264. **Pre-metal dielectric:** Imaoka discloses that “[a]s Fig. 3 shows, passivation films 16 and 18 are formed in one or a plurality of layers on the first semiconductor substrate 10.” *Id.*, [0009]. POSAs would understand film 16 is a pre-metal dielectric because it insulates adjacent pads to prevent electrical shorts (*id.*, Figs. 2 and 3), is made from insulators (*id.*, [0009] (“SiO₂, SiN, [and] a polyimide resin”)), and is located between active devices in substrate 12 and first metal layer 14. *See* Section IX.E (which starts on page 47, explaining the meaning of “pre-metal dielectric”).

Imaoka, Fig. 3 (Annotated)



f. [1.5]

[1.5] a first via penetrating the pre-metal dielectric and the first semiconductor substrate, the first via being connected to the second via;

265. Imaoka’s “part 38” meets the requirements of both first and second
vias. *See* Section on limitation [1.2] (the second via) (which starts on page 123).

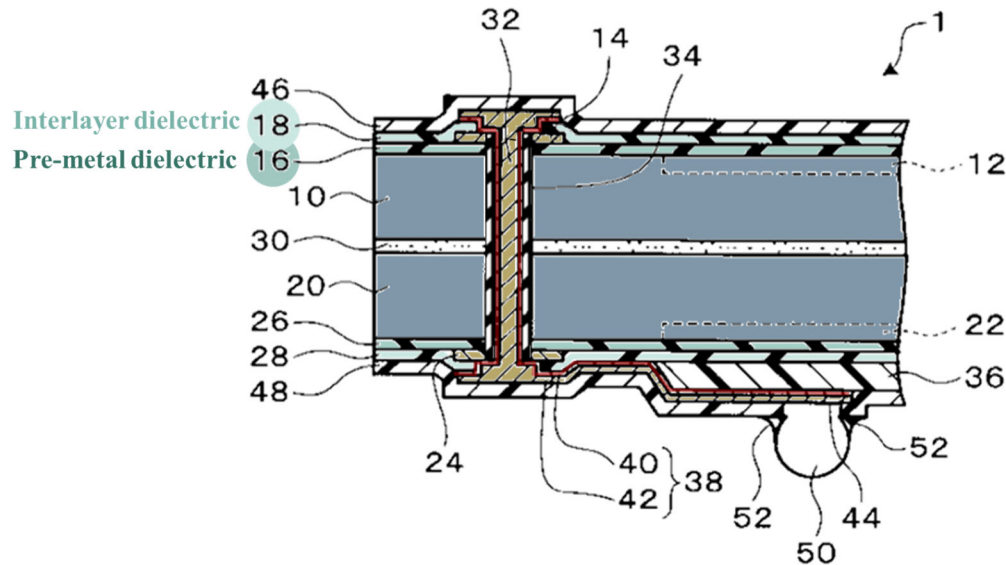
g. [1.6]

[1.6] a first interlayer dielectric on the pre-metal dielectric including the first via;

266. Imaoka has “passivation films 16 and **18** ... ***on*** the first semiconductor substrate 10.” Imaoka (Ex. 1006), [0009], Fig. 3 (below, annotated). POSAs would understand film 18 is an ILD because it insulates adjacent pads (14)

to prevent electrical shorts (*id.*, Figs. 2-3) and is made from insulators (*id.*, [0009] (“SiO₂, SiN, [and] a polyimide resin”)). See Section IX.C (which starts on page 44, explaining the meaning of “interlayer dielectric”).

Imaoka, Fig. 3 (Annotated)



h. [1.7]

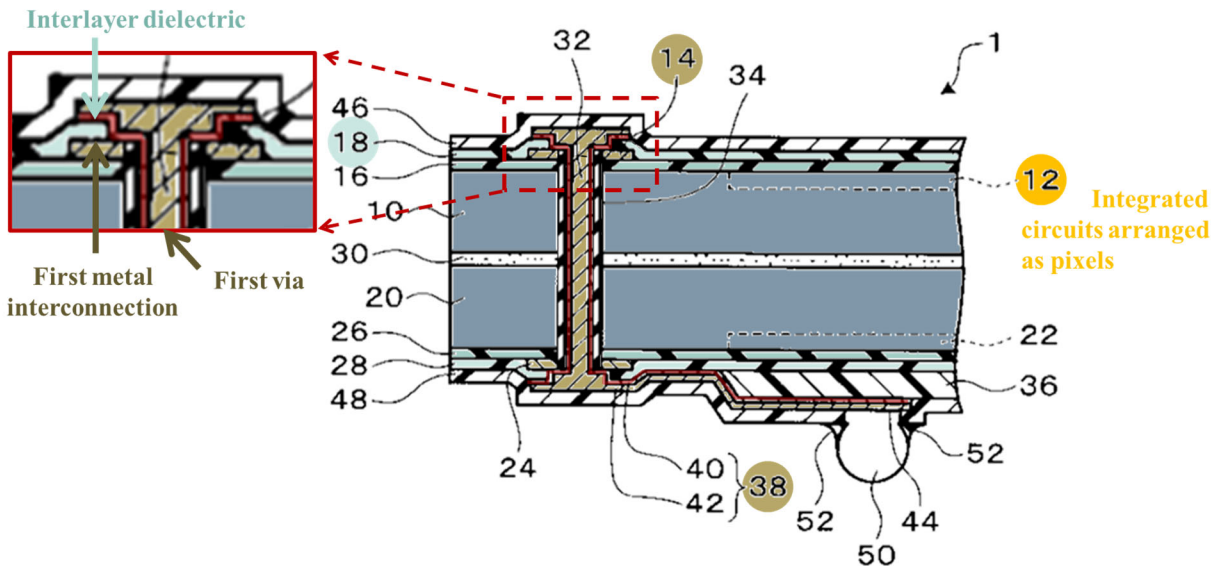
[1.7] a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel;

267. **First metal interconnection:** POSAs would understand Imaoka’s pads (14) are metal interconnections because they are “aluminum” or “a copper type of metal” that are electrically connected to first and second vias (part 38) (Imaoka (Ex. 1006), [0018]) and “to the first semiconductor circuit” (12) (*id.*,

[0009]), which contains the unit pixel (*id.*, [0011]) See Section IX.B (which starts on page 43, explaining the meaning of an “interconnection”).

268. **Connected to the first via and the unit pixel:** A POSA would understand that the pad 14 is “connected to the unit pixel” because Imaoka discloses that the pad 14 is “electrically connected to the first semiconductor circuit” (Imaoka (Ex. 1006), [0009]), the “first integrated circuit 12” has a “energy converter” which has “light receiving elements” “(for example a photodiode)” “corresponding to each of a plurality of pixels two-dimensionally arrayed” (*id.*, [0011]).

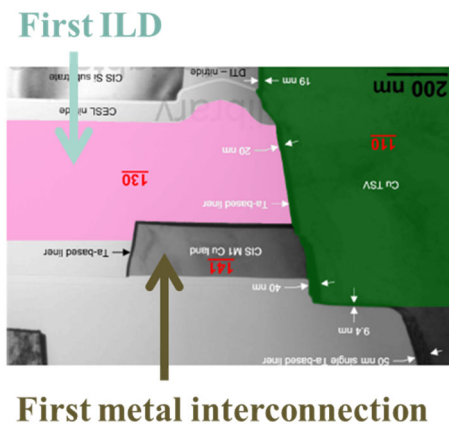
Imaoka, Fig. 3 (Annotated)



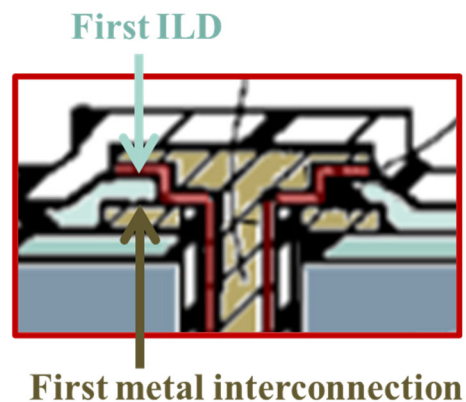
269. **On the first interlayer dielectric:** As shown in the figures above and below, Imaoka’s pads 14 are “on” ILD 18 because they are below and adjacent to

dielectric 18 pursuant to VisionX's claim construction as explained in Section IX.A (see page 39).

Accused Product



Imaoka

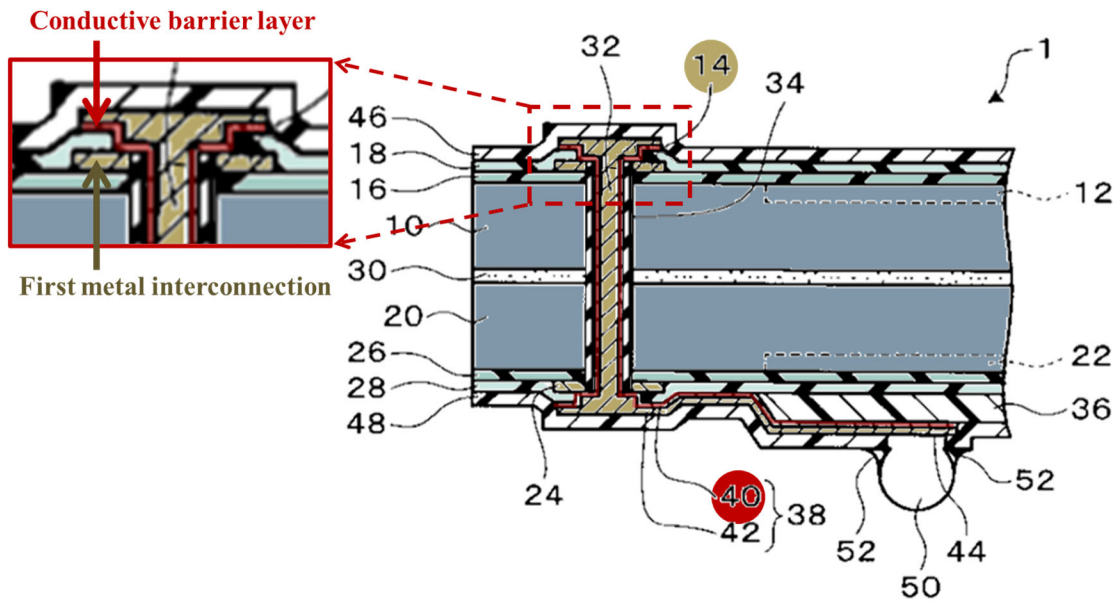


i. [1.8]

[1.8] a conductive barrier layer on the first metal interconnection; and;

270. Imaoka discloses that the “first conductive layer 40 may at least include a barrier layer” (Imaoka (Ex. 1006), [0041]), which according to Figure 3 is disposed above (i.e. “on”) the pad 14 (i.e. the “first metal interconnection”) as shown below.

Imaoka, Fig. 3 (Annotated)



j. [1.9]

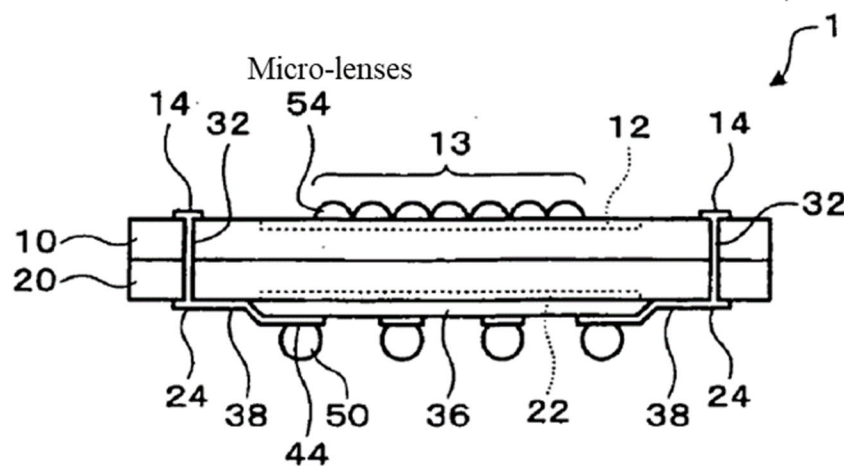
[1.9] a color filter and a microlens on the first interlayer dielectric on the unit pixel.

271. **Color filter:** Imaoka discloses “[t]he optical part 13 may have a color filter (not illustrated)” that the “color filter is provided corresponding to each of the plurality of the light-receiving elements” and that the “color filter may be formed between the micro-lenses 54 and the light-receiving elements.” *Id.*, [0013]. Imaoka thus discloses a color filter on the first interlayer dielectric on the unit pixel.

272. **Microlens:** Imaoka also discloses that the “optical part 13 may be equipped with a plurality of micro-lenses 54” that the “micro-lenses 54 are provided corresponding to each of the plurality of the light-receiving elements” as

shown in Figure 1, and that the “micro-lenses 54 are placed on the side of the surface on which the first integrated circuit 12 on the first semiconductor substrate 10 is formed.” *Id.*, [0012]. As the first interlayer dielectric is on the first semiconductor substrate, Imaoka discloses the microlens is “on” the first interlayer dielectric and the unit pixel corresponding to each of the plurality of the light-receiving elements.

Imaoka, Fig. 1 (Annotated)



2. Claim 2

2. The image sensor according to claim 1, wherein the first metal interconnection comprises copper (Cu).

273. Imaoka discloses its pads 14 and 24 “may be formed of an aluminum type or *a copper type of metal.*” *Id.*, [0009]. I note that U.S. Patent Publication No. 2004/0245649 (“’649 Pub.”) claims Imaoka as its foreign priority application. Ex.

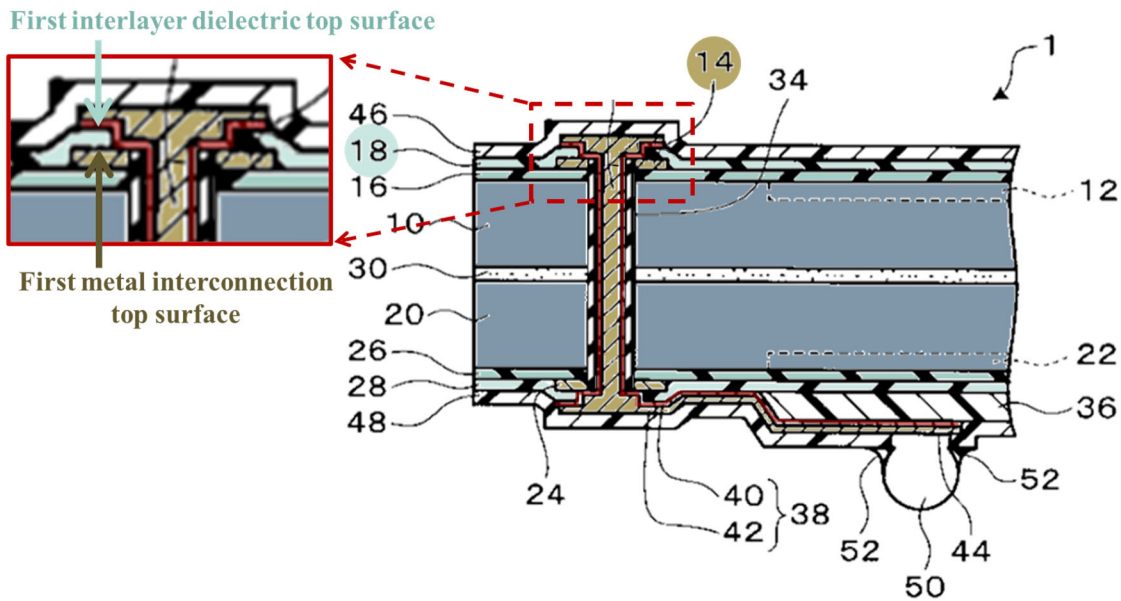
1022, face. While the '649 Pub. discloses the pad 14 may be “steel type of metal” (*id.*, [0050]), a POSA would understand that as an error because steel is not used for interconnections in semiconductors. A POSA would have thus understood Imaoka as disclosing at least one example as having copper pads.

3. Claim 4

4. The image sensor according to claim 1, wherein the first metal interconnection has a top surface lower than that of the first interlayer dielectric, such that the first metal interconnection and the first interlayer dielectric have a height difference.

274. Imaoka satisfies claim 4’s additional limitation that the first metal interconnection has a top surface lower than that of the first ILD, such that there is a “height difference” between the two because Figure 3 shows the claimed height difference. Imaoka (Ex. 1006), Fig. 3.

Imaoka, Fig. 3 (Annotated)



4. Claim 5

5. The image sensor according to claim 1, wherein the second metal interconnection comprises copper (Cu) or aluminum (Al).

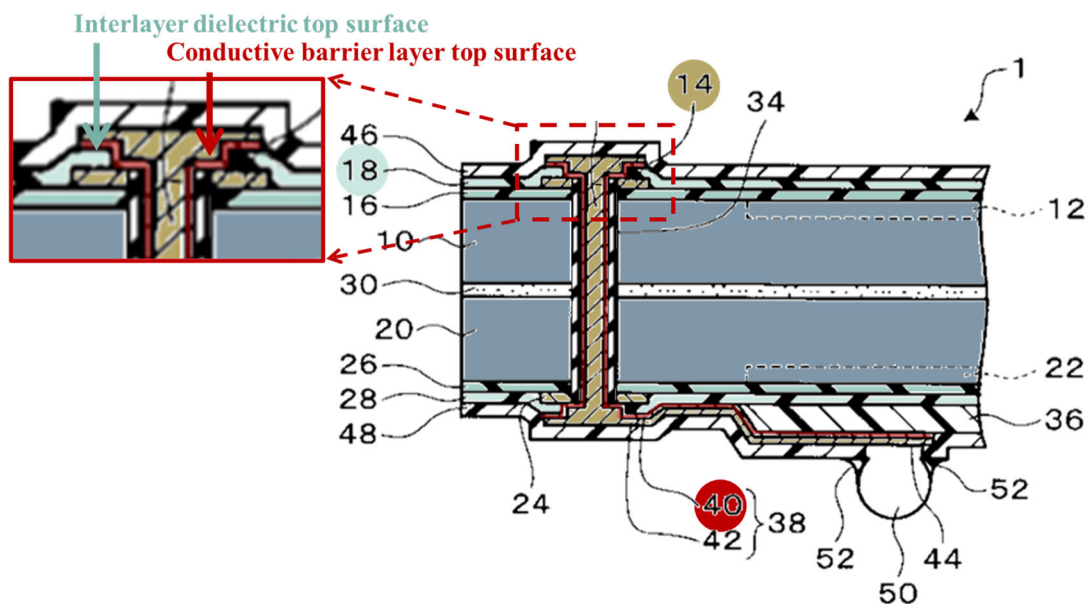
275. Imaoka discloses its pads 14 and 24 “may be formed of an aluminum type or a copper type of metal.” *Id.*, [0009], [0010] (noting “contents of the second semiconductor substrate 20 may be the same as the above-mentioned first semiconductor substrate 10”).

5. Claim 6

6. The image sensor according to claim 1, wherein the conductive barrier layer has at top surface substantially even with the top surface of the first interlayer dielectric.

276. Imaoka satisfies claim 6's additional limitation that the conductive barrier layer has at top surface "substantially even" with the top surface of the first ILD because Figure 3 shows the barrier layer (40) having top surface "substantially even" with the top surface of the first ILD (18).

Imaoka, Fig. 3 (Annotated)



6. Claim 7

7. The image sensor according to claim 1, wherein the first via and the second via comprise the same material.

277. Imaoka discloses its via is formed from copper, which would include both the first and second vias as described above for limitation [1.2] (*see* page 123). Imaoka (Ex. 1006), [0041] (stating the “seed layer” for the plug in the via “may be formed of the same material as the material set up thereon (for example, Cu)”).

7. Claim 8

8. The image sensor according to claim 1, wherein the second semiconductor substrate provides metal interconnections for connection to a power line and an external signal line.

278. Imaoka discloses its sensor has a “power supply terminal” and an “input/output terminal.” *Id.*, [0049]. Imaoka further discloses that its sensor has an “external terminal 50” as part of the “second semiconductor substrate 20.” *Id.*, [0017]. This external terminal provides the external connections for the circuit’s power and external signal line. POSAs would thus understand from Imaoka’s disclosure that the “external terminal 50” are metal interconnections for connection to a power line and an external signal line that is part of the second substrate.

D. Ground 4: Imaoka in view of Dublin Renders Claim 3 Obvious

279. Claim 3 depends from claim 1 and further requires cobalt (Co) or nickel (Ni) alloy for the conductive barrier layer. Imaoka does not disclose the material for its barrier layer, but as of 2007, Dublin disclosed a cobalt tungsten phosphide (CoWP) alloy as a preferred option for a conductive barrier layer in copper interconnections. Claim 3 would therefore have been obvious over Imaoka in view of Dublin under Patent Owner's claim interpretations in the Texas Litigation.

1. Reasons to Use a CoWP Barrier Layer

280. POSAs would have used CoWP (an alloy having cobalt) as Imaoka's conductive barrier layer because Imaoka does not disclose the material for its barrier layer and CoWP had better performance than other known materials.

281. **Enhanced barrier properties:** Dublin discloses that CoWP “significantly enhances the barrier properties,” making it “preferred” over other known barrier materials. Dublin (Ex. 1008), 3:1-7. CoWP alloy allows for “increased thermal stability, improved corrosion resistance and mechanical properties (such as wear resistance).” *Id.*, 5:17-23. A POSA would thus have been motivated to use this preferred material for its enhanced properties.

282. **Does not require a polishing step:** Imaoka does not disclose the use of a polishing step between deposition of the barrier layer and deposition of the

copper. Imaoka (Ex. 1006), [0041]. Dublin discloses that CoWP can be selectively deposited without requiring any polishing. *Id.*, 8:66-9:3; Choi (Ex. 1007), [0122]-[0123], [0129]. Using the CoWP would thus be compatible with Imaoka's process.

2. Resulting Sensor and Reasonable Expectation of Success

283. The sensor resulting from using Dublin's CoWP alloy would have an identical structure to Imaoka's except using CoWP as the conductive barrier material.

284. POSAs would have had a reasonable expectation of successfully using CoWP as a barrier material because Imaoka discloses its part 38 is made of copper (Imaoka (Ex. 1006), [0041] (stating the "seed layer" for the plug in the via "may be formed of the same material as the material set up thereon (for example, Cu)")) and Dublin discloses CoWP is for copper interconnections in semiconductor devices. Dublin, 2:63-3:7. This was the very thing my team at Kodak did in 2005 when we substituted a CoWP barrier layer for a SiN barrier layer disclosed by the basic process disclosed in 1999. Gambino (Ex. 1023), 25.

3. Claim 3 Analysis

3. The image sensor according to claim 1, wherein the conductive barrier layer comprises cobalt (Co) or nickel (Ni) alloy.

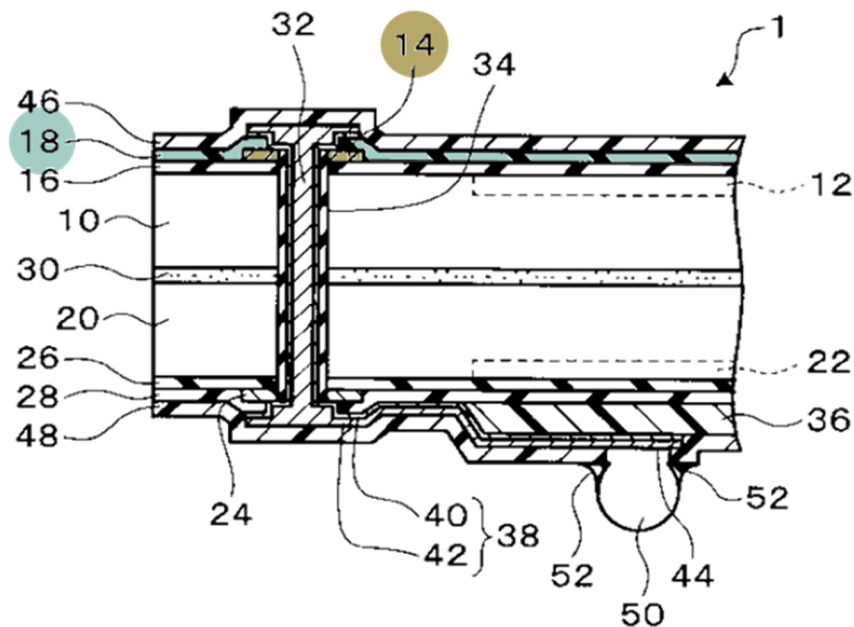
285. The resulting sensor would include a conductive metal barrier layer that comprises cobalt (Co), thereby rendering claim 3 obvious. Dublin discloses a

“technique of electrolessly depositing CoWP as a barrier material in order to protect or encapsulate a conductive material” such as “copper.” Dublin (Ex. 1008), 2:63-66. Figure 10 of Dublin “is a cross-sectional view showing a selective formation of another CoWP barrier layer of the present invention above the copper.” *Id.*, 3:53-55. CoWP is conductive. Ex. 1020, 1:22-23 (“a conductive barrier film such as cobalt tungsten phosphorous (CoWP) is formed on a Cu wiring”). Dublin’s conductive CoWP barrier layer as used in Imaoka’s sensor thus satisfies and renders obvious claim 3.

E. Ground 5: Imaoka in view of Choi Renders Claims 1, 2, and 4-8 Obvious

286. Imaoka’s pads 14 are formed from “an aluminum type or a copper type of metal.” Imaoka (Ex. 1006), [0009]. Nevertheless, POSAs would infer the sensor in Imaoka’s Figures 1-4 uses aluminum rather than copper for pad 14 because film 18 overcoats pad 14; a copper structure would instead normally be disposed within film 18. *Id.*, Fig. 3.

Imaoka, Fig. 3 (Annotated)



287. However, POSAs would have had reason to fabricate Imaoka’s sensor using copper rather than aluminum, and in particular would have had reason to use Choi’s damascene process for such fabrication. The resultant sensor would satisfy all elements of claims 1-2 and 4-8 even if interpreting “on” more narrowly than Patent Owner’s suggestion in the Texas Litigation.

1. Reasons to Pick Copper for Pad 14

288. POSAs would have had reason to pick copper instead of aluminum for pad 14 given its lower resistivity, reduced power consumption, resistance to electromigration, and tighter packing density as discussed in Section VI.B that begins on page 20. In addition, Imaoka states that its “seed layer” that will form the interconnect between the first and second substrates “may be formed of the same

material as the material set up thereon (for example, Cu).” Imaoka (Ex. 1006), [0041]. A POSA would understand this as disclosing the use of copper for the via connecting the first and second substrates as Imaoka discloses no other material for a seed layer and a copper seed layer would be used with a copper plug. Imaoka also states that its pads are formed from “an aluminum type or *a copper type of metal.*” *Id.*, [0009]. POSAs implementing Imaoka’s Figures 1-4 would naturally also select copper for pad 14 to fill both the vias and the interconnections in a single step—reducing the number of processing steps. *See* Section VI.B beginning on page 20.

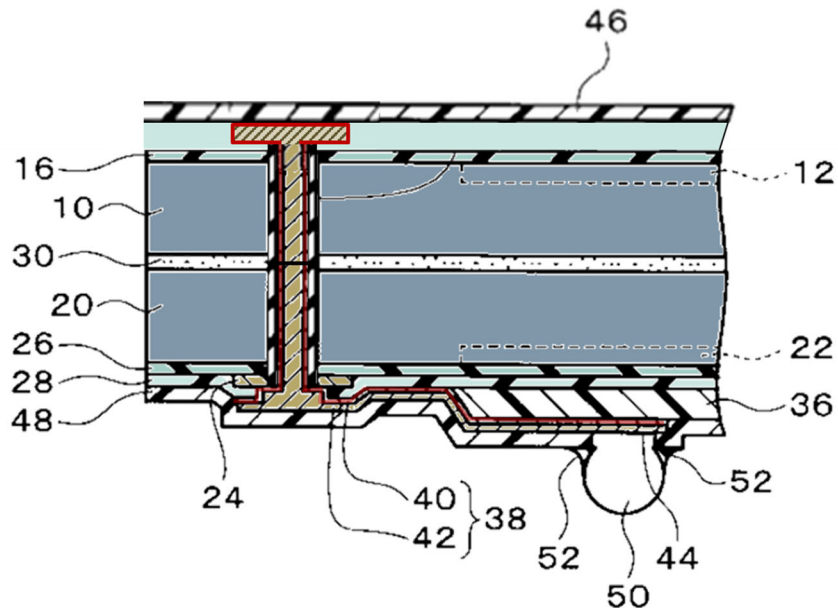
289. As Imaoka does not disclose a structure specific to copper pads, POSAs would have consulted references such as Choi. The dual-damascene process disclosed by Choi would be used because it was so common and well-known by at least 2001. Quirk (Ex. 1014), 80; Pratt (Ex. 1013), 8-10; Doering (Ex. 1010), 4.

290. POSAs would have also had reason to make pad 24 and electrical connection part 44 out of copper for the same reasons as for pad 14. However, for purposes of the analysis herein, it is immaterial whether POSAs would have taken that additional step, which would have required removing or modifying Imaoka’s resin layer (36) to apply Choi’s copper interconnection process and in particular Choi’s planarization step.

2. Resulting Imaoka-Choi Sensor

291. The sensor resulting from modifying Imaoka's design for use of copper in pads 14 ("Imaoka-Choi Sensor") is shown below.

Imaoka-Choi Sensor



292. Imaoka discloses stacking the semiconductor substrates (Imaoka (Ex. 1006), [0034]-[0035]) prior to fabricating the interconnections (*id.*, [0036]-[0044]). But using Choi's process to fabricate pads 14 after the first and second semiconductors had already been bonded together would have required applying Choi's process to fabricate the interconnections on the second substrate as well as the first. That would have in turn required removing or modifying Imaoka's resin layer (36) as that resin layer creates topography incompatible with Choi's planarization process.

293. But POSAs would have known a straightforward way of fabricating pads 14 from copper without altering the structure of the second substrate by (1) fabricating the interconnections on the top substrate according to Choi and Imaoka (as described further below), (2) fabricating the interconnections on the bottom substrate as described by Imaoka (*id.*, [0036]-[0044]), and then (3) bonding the two substrates thereafter. This approach would have been straightforward because POSAs would have been well aware of the processes needed to separately fabricate an image chip and a logic chip, bonding them together afterwards.

294. For example, Pyo discloses this approach of fabricating an image chip and a logic chip on two different substrates and then bonding the two together. Pyo, 4 (“[T]he first substrate and the second substrate are bonded through a connecting portion protruding from the rear surface of the first substrate and a pad on the upper portion of the second substrate.”). Iwabuchi also discloses bonding an image chip and a logic chip, connecting vias (84”) in the image chip (52) directly to vias (84) in the logic chip (193), without any intervening pads. Iwabuchi, [0095]-[0096], Figs. 34A-34B (excerpts, below). POSAs would have thus been familiar with this approach of separately fabricating an image chip and logic chip and then bonding them together using vias to connect the two chips.

FIG. 34A

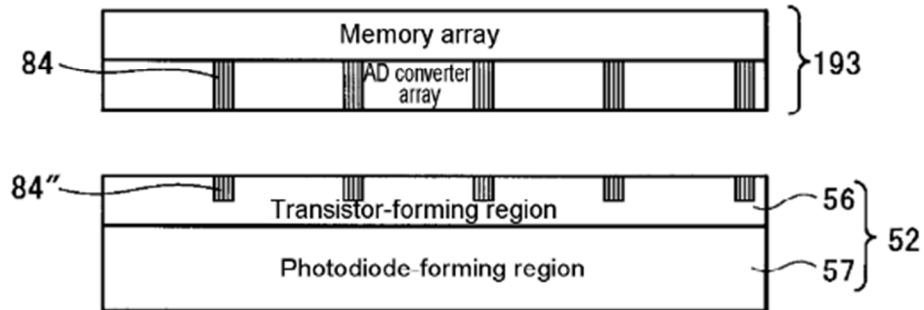
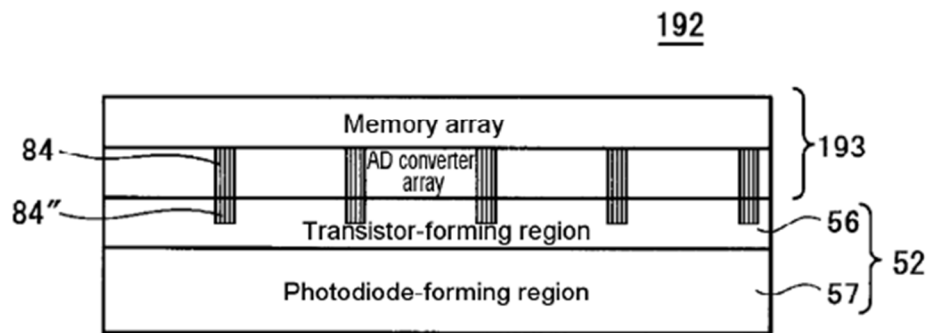


FIG. 34B



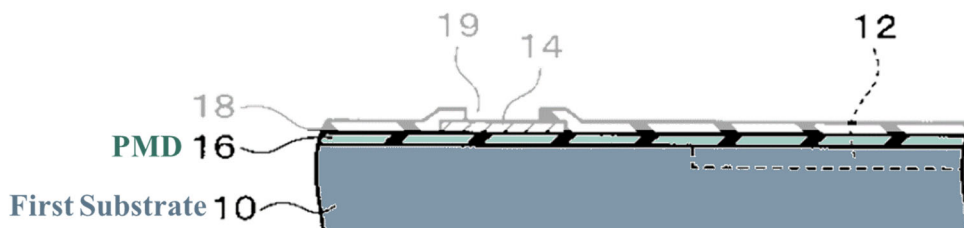
295. Using this approach, POSAs would have fabricated the pads 14 and part 38 in the first substrate and then bonded the first and second substrates as follows.

a. Deposit PMD

296. POSAs would have first deposited a PMD layer as disclosed by Imaoka. Imaoka, [0036], Fig. 5(A) (below, modified). Passivation film 16 is a PMD because it insulates the active devices (12) from the first metal layer. *See*

Section IX.E (which starts on page 47, explaining the meaning of “pre-metal dielectric”).

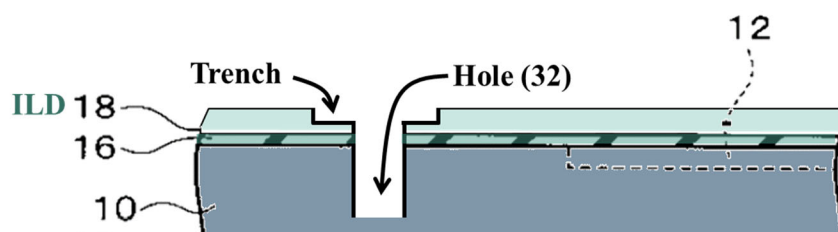
Imaoka, Fig. 5(A) (Modified)



b. Deposit ILD and Pattern

297. POSAs would have then deposited an ILD layer and etched it to form trenches for pad 14 and a hole (32) for part 38. *See* Section XI.A.2.a.i(1) (starting on page 78); Imaoka (Ex. 1006), [0036]-[0037], Fig. 5B (below, modified); Choi, [0124]-[0125], Fig. 5E.

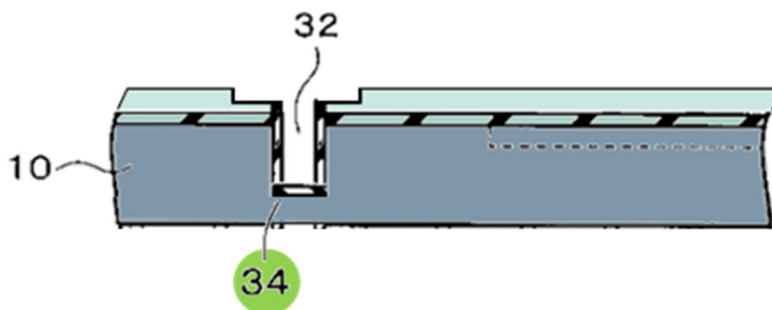
Imaoka, Fig. 5(B) (Modified)



c. Insulating Layer

298. POSAs would have next fabricated an “insulating layer 34” inside the hole as directed by Imaoka. Imaoka (Ex. 1006), [0038], Fig. 5C (below, modified).

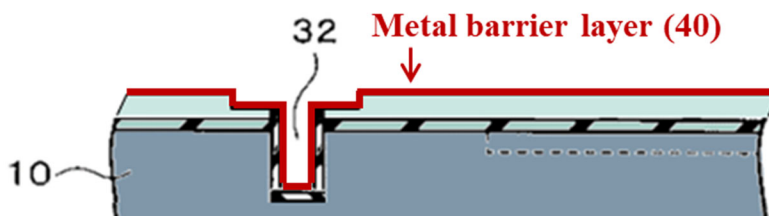
Imaoka, Fig. 5(C) (Modified)



d. Metal Barrier Layer

299. POSAs would have next deposited a metal barrier layer. *See* Section XI.A.2.a.i(2) (starting on page 79); Imaoka (Ex. 1006), [0041] (a “barrier layer may be formed ... (for example, TiW or TiN)”), Fig. 6(B) (below, modified).

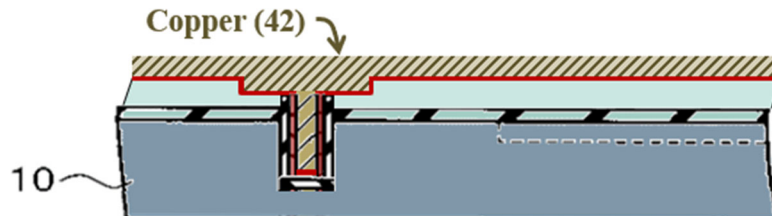
Imaoka, Fig. 6(B) (Modified)



e. Copper Deposition

300. POSAs would have deposited a “seed layer” (Imaoka (Ex. 1006), [0041]), a “photoresist layer 92” to the bottom (*id.*, [0042]), which is not required on the top due to subsequent CMP, and deposited copper. *See* Section XI.A.2.a.i(3) (starting on page 80); Imaoka (Ex. 1006), [0041]-[0042], Fig. 6(C) (below, modified)).

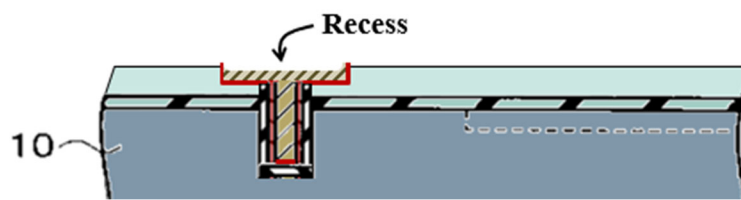
Imaoka, Fig. 6(C) (Modified)



f. CMP

301. POSAs would next perform CMP to create a recess above the interconnection, below. *See* Section XI.A.2.a.i(4) (starting on page 81).

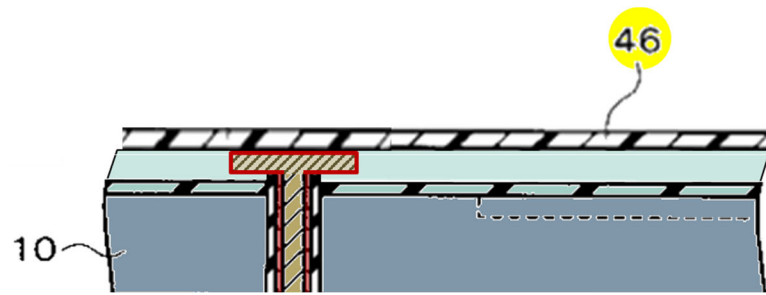
Imaoka, Fig. 7(A) (Modified)



g. Top Metal Barrier Layer; Planarization

302. POSAs would next deposit a top metal barrier layer (*see* Section XI.A.2.a.i(5), starting on page 82) and planarize (*see* Section XI.A.2.a.i(6), starting on page 84). POSAs would deposit insulating layer 46, below. Imaoka (Ex. 1006), [0044], Fig. 7(B) (below, modified). POSAs would thin the back side of the substrate to expose the via for connection to the via in the second substrate. Pyo, 6 (“grinding the rear surface of the first substrate 100 so that the connecting portion 105 protrudes”).

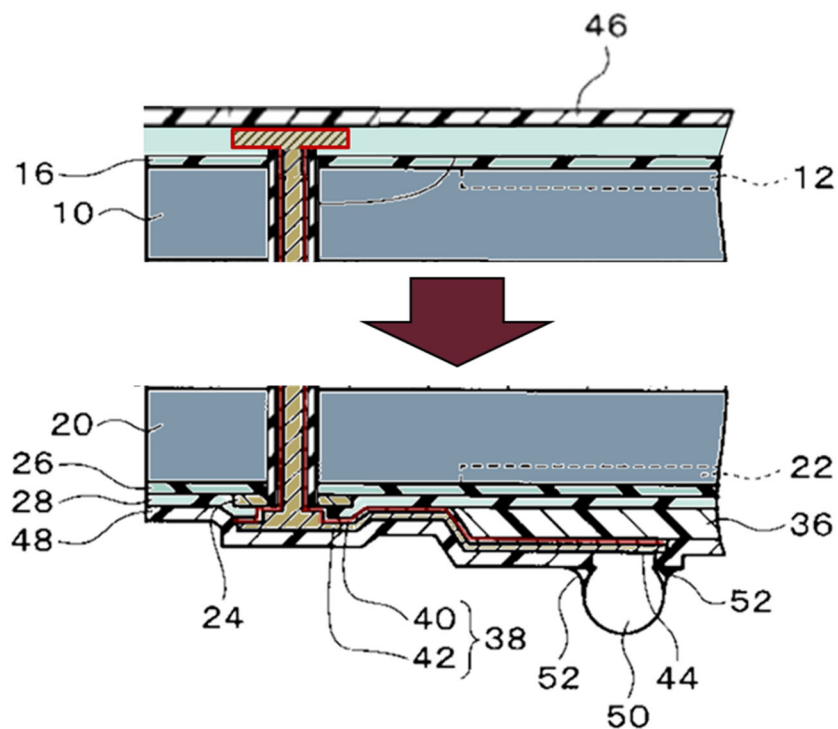
Imaoka, Fig. 7(B) (Modified)



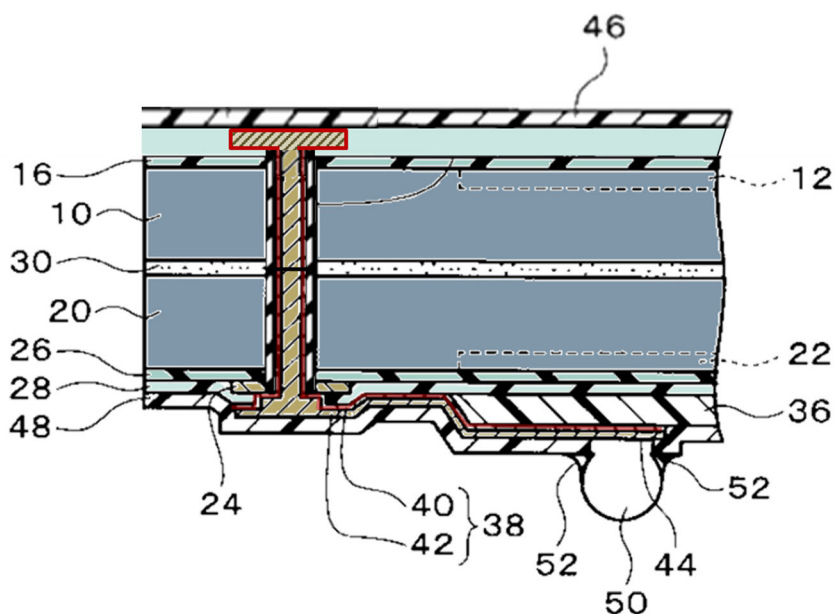
h. Bonding

303. POSAs would next bond the first substrate (as described above) to the second substrate (described by Imaoka, [0036]-[0044]). *E.g.*, Pyo 4; Iwabuchi, [0095]-[0096], Figs. 34A-34B.

Bonding



Imaoka-Choi Sensor



3. Reasonable Expectation of Success

304. A POSA would have had a reasonable expectation of success in modifying the Imaoka sensor as described above because as it would have been a straight-forward application of Choi's well-known dual-damascene process, which Choi itself and Gambino had already applied to image sensors. And bonding an image chip to a logic chip, with connections between the two, was also a known process. Pyo, 4; Iwabuchi, [0095]-[0096], Figs. 34A-34B.

4. Claim-by-Claim Analysis

305. The analysis below demonstrates that the Imaoka-Choi Sensor meets each and every element of claims 1, 2, and 4-8 of the '366 patent as explained below, rendering it obvious given the above-discussed reasons for the modification.

a. Claim 1

i. [1.pre]

[1.pre] An image sensor, comprising:

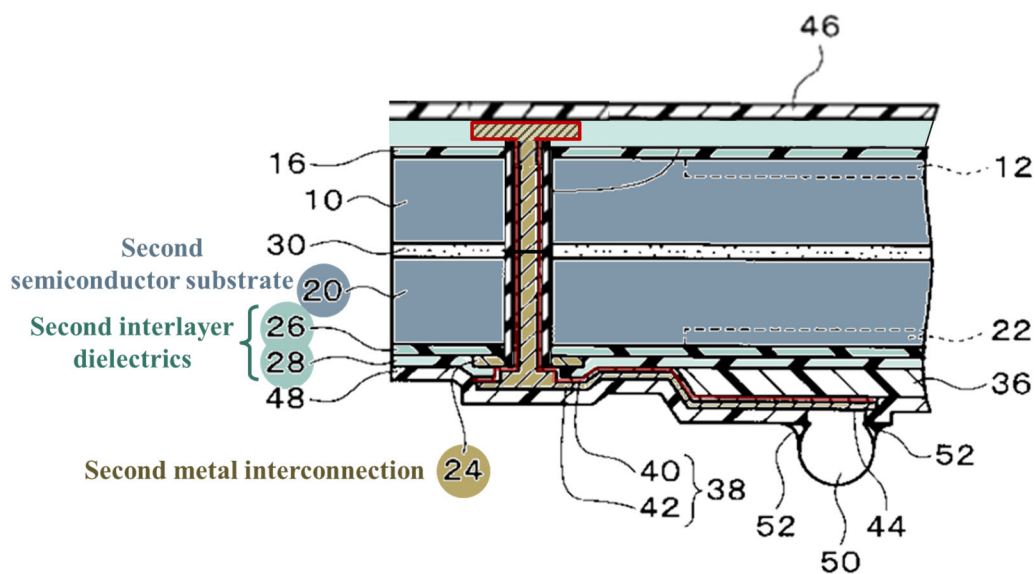
306. To the extent the preamble is limiting, the Imaoka-Choi Sensor satisfies the preamble because Imaoka's device is an image sensor (*see* Section XI.C.1.a starting on page 121) and that would remain unchanged after modification.

ii. [1.1]

[1.1] a second semiconductor substrate including a second metal interconnection and a second interlayer dielectric;

307. The Imaoka-Choi Sensor satisfies limitation [1.1] because Imaoka discloses its sensor has a second semiconductor substrate including a pad 24 (second metal interconnection) and passivation films 26 and 28 (second interlayer dielectrics) (*see* Section XI.C.1.b, starting on page 121) and these aspects of Imaoka would remain unchanged after modification.

Imaoka-Choi Sensor

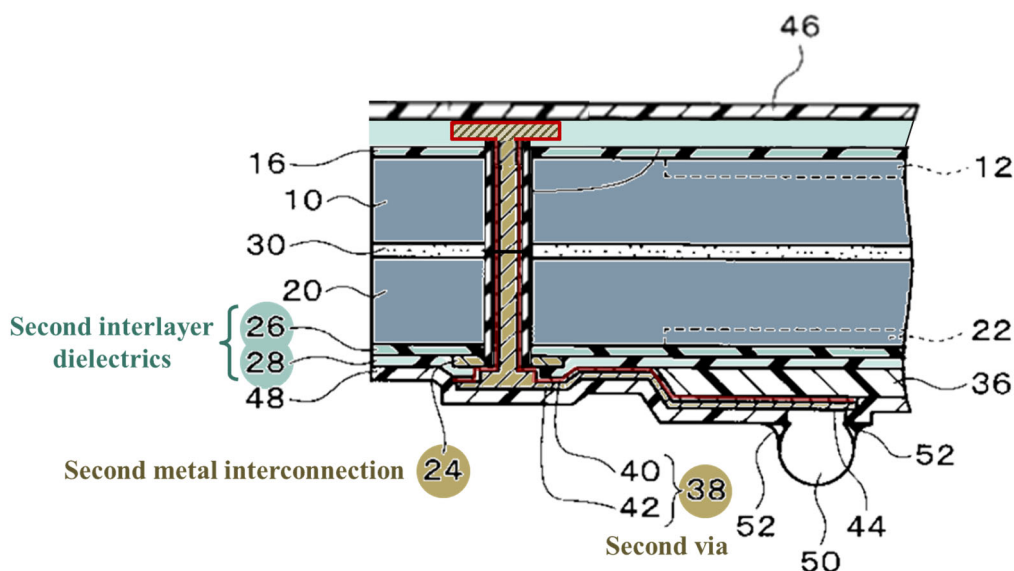


iii. [1.2]

[1.2] a second via penetrating the second interlayer dielectric so that the second via is connected to the second metal interconnection;

308. The Imaoka-Choi Sensor satisfies limitation [1.2] because Imaoka's sensor does (*see* Section XI.C.1.c, starting on page 123) and these aspects would remain unchanged after modification.

Imaoka-Choi Sensor

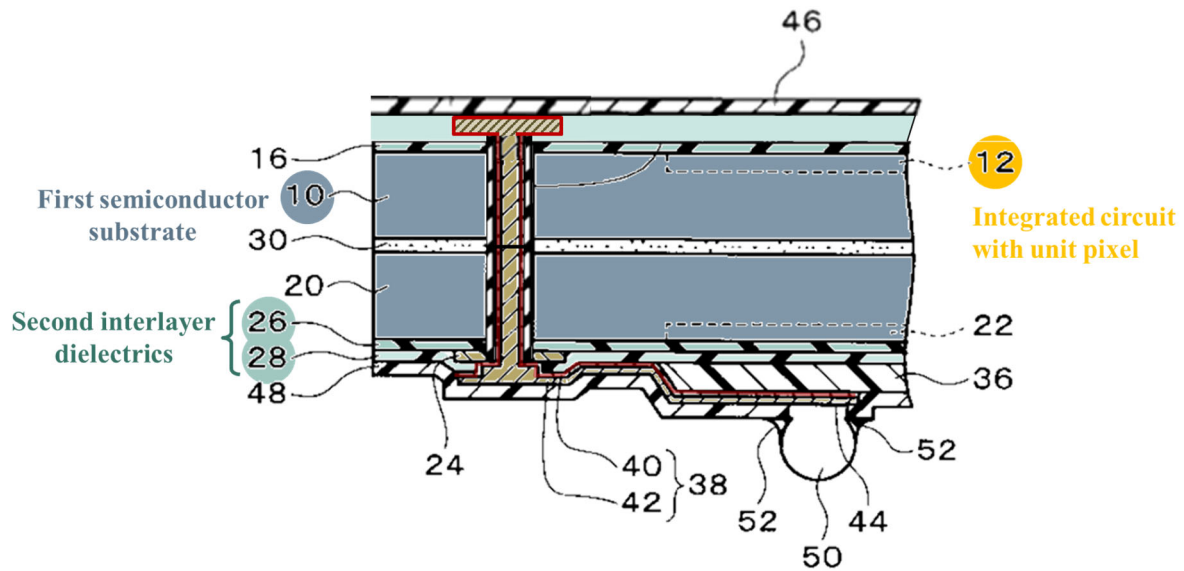


iv. [1.3]

[1.3] a first semiconductor substrate on the second interlayer dielectric, the first semiconductor substrate having a unit pixel;

309. The Imaoka-Choi Sensor satisfies limitation [1.3] because Imaoka's sensor does (*see* Section XI.C.1.d, starting on page 126) and these aspects would remain unchanged after modification.

Imaoka-Choi Sensor

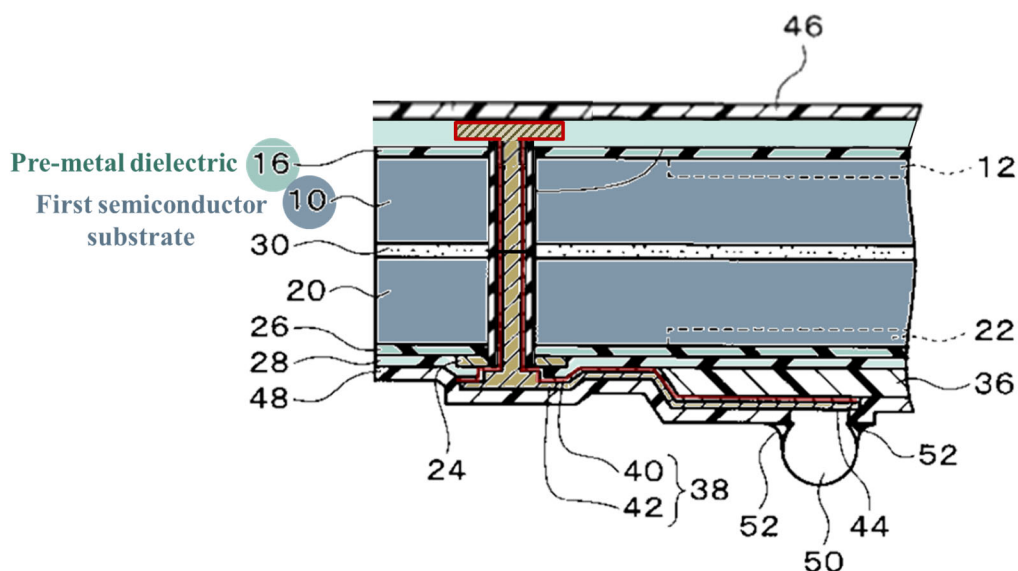


v. [1.4]

[1.4] a pre-metal dielectric on the first semiconductor substrate;

310. The Imaoka-Choi Sensor satisfies limitation [1.4] because Imaoka's sensor does (*see* Section XI.C.1.e, starting on page 127) and these aspects would remain unchanged after modification.

Imaoka-Choi Sensor

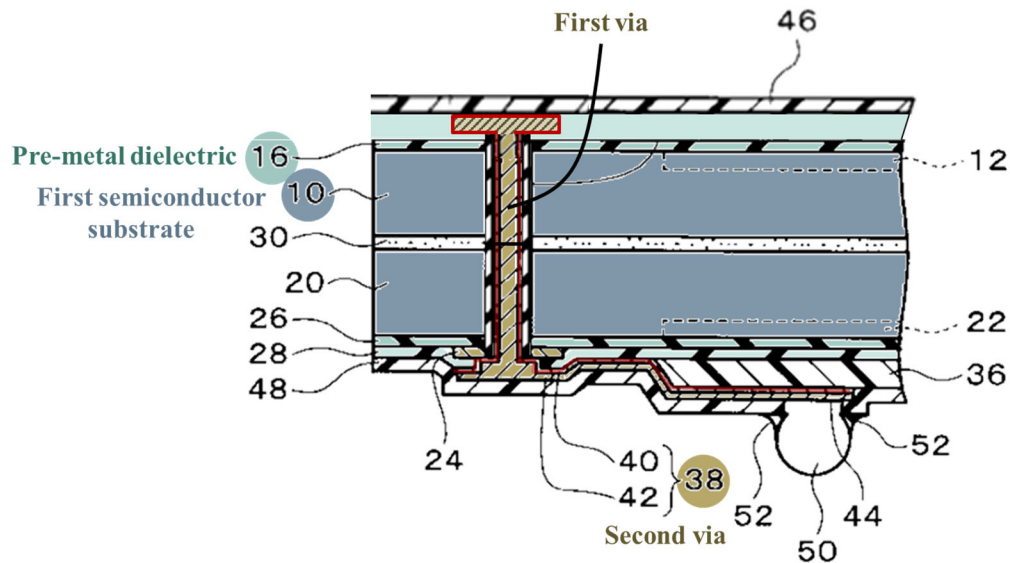


vi. [1.5]

[1.5] a first via penetrating the pre-metal dielectric and the first semiconductor substrate, the first via being connected to the second via;

311. The Imaoka-Choi Sensor satisfies limitation [1.5] under even a narrower interpretation than Patent Owner’s interpretation in the Texas Litigation because the “conductive part 38” would be fabricated in the first substrate separately from the second substrate before both substrates are bonded together, thus connecting the first and second substrates. *See* Section XI.E.2 (starting on page 143).

Imaoka-Choi Sensor



vii. [1.6]

[1.6] a first interlayer dielectric on the pre-metal dielectric including the first via;

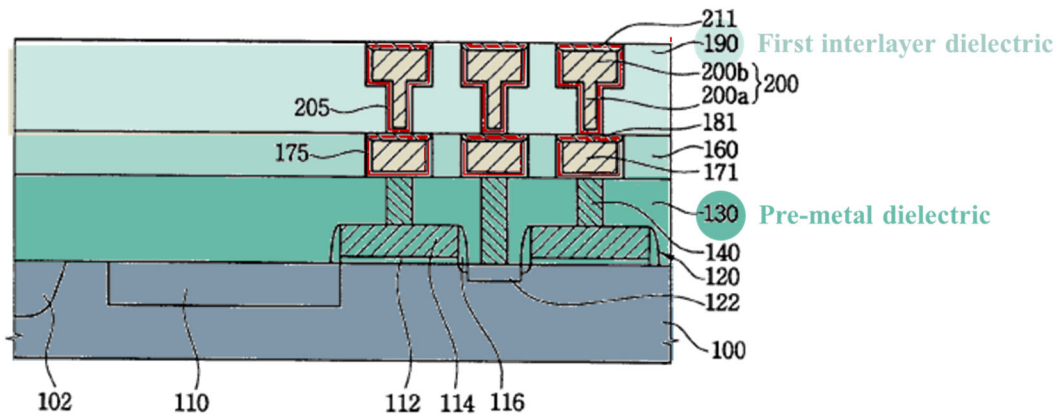
312. The Imaoka-Choi Sensor satisfies limitation [1.6] because, when implementing pads 14 in copper using Choi's process, the resulting sensor has a first interlayer dielectric on the pre-metal dielectric (that includes the first via), below. *See* Section XI.E.2 (starting on page 143).

Imaoka-Choi Sensor



313. Specifically, Choi requires an interlayer dielectric (“interlayer 190”) on a pre-metal dielectric (“lower insulation layer 130”). Choi (Ex. 1007), [0115], [0124], Fig. 5E (below, annotated).

Choi, Fig. 5E (Annotated)

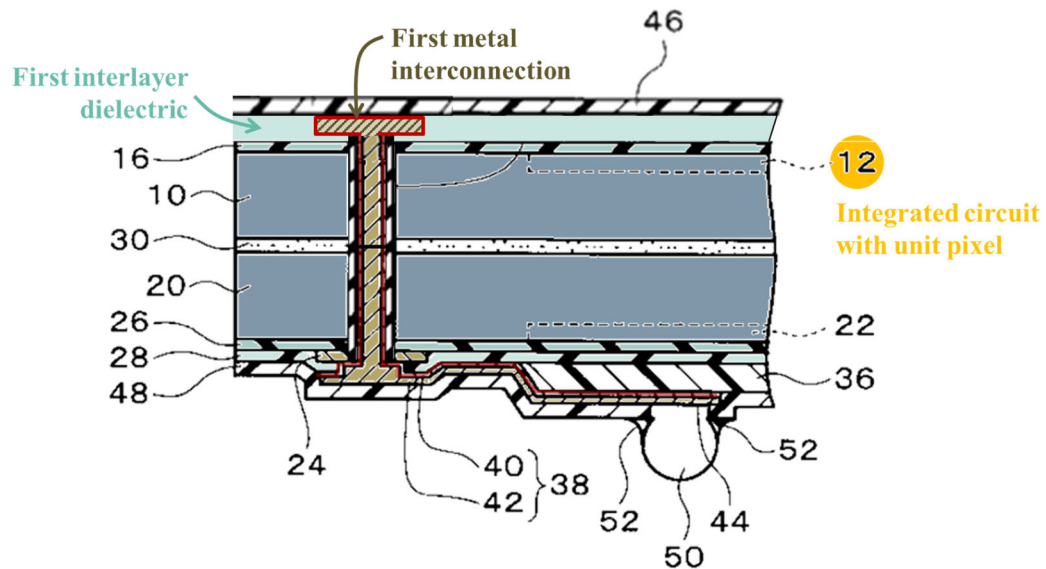


viii. [1.7]

[1.7] a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel;

314. The Imaoka-Choi Sensor satisfies limitation [1.7] because when implementing pads 14 in copper using Choi’s processes, the pad would be located “on” a first interlayer dielectric, below. *See* Section XI.E.2 (starting on page 143).

Imaoka-Choi Sensor



ix. [1.8]

[1.8] a conductive barrier layer on the first metal interconnection; and;

315. The Imaoka-Choi Sensor satisfies limitation [1.8] because when implementing pads 14 in copper using Choi's processes, POSAs would have encapsulated the copper pads with a conductive barrier layer, including "on" the pads, shown below. *See* Section XI.E.2 (starting on page 143).

Imaoka-Choi Sensor



Legend

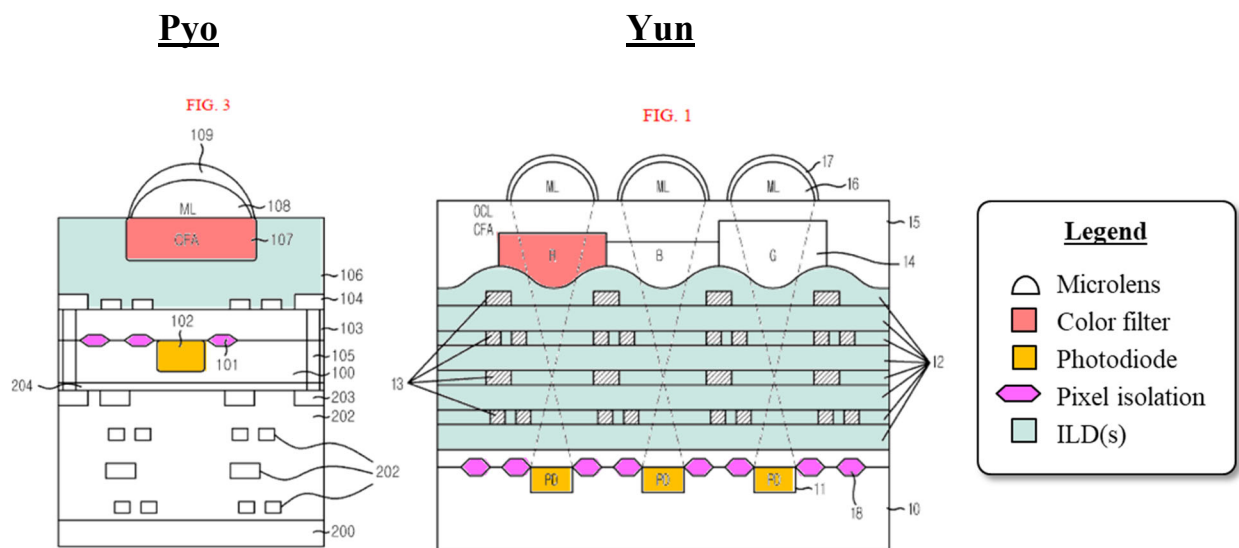
- Dielectrics (ILD and PMD)
- Semiconductor substrate
- Metal barrier layers
- Copper interconnections

x. [1.9]

[1.9] a color filter and a microlens on the first interlayer dielectric on the unit pixel.

316. The Imaoka-Choi Sensor satisfies limitation [1.9] because Imaoka's sensor does (*see* Section XI.C.1.j, starting on page 132) and these aspects would remain unchanged after modification.

317. Moreover, an obvious place to locate a color filter and microlens for the Imaoka-Choi Sensor would have been “on” the first ILD on the unit pixel because each would naturally have been fabricated on the first substrate *after* the unit pixel and ILD layer had already been formed, a common location to put the microlens and color filter. *E.g.* Pyo (Ex. 1005), Fig. 3 (below left); Yun (Ex. 1017), Fig. 1 (below right).



318. The color filter and microlens would be “on” the first ILD and the unit pixel in the Imaoka-Choi Sensor notwithstanding any intervening layers. ’366 patent, 2:17-22 (allowing for “intervening layers”).

b. Claim 2

2. The image sensor according to claim 1, wherein the first metal interconnection comprises copper (Cu).

319. The Imaoka-Choi Sensor satisfies claim 2’s additional limitation of the first metal interconnection being copper. *See* Section XI.C.2 (starting on page 133). POSAs would have selected copper for pad 14. *See* Section XI.E.1 (starting on page 141). Claim 2 is thus unpatentable as obvious.

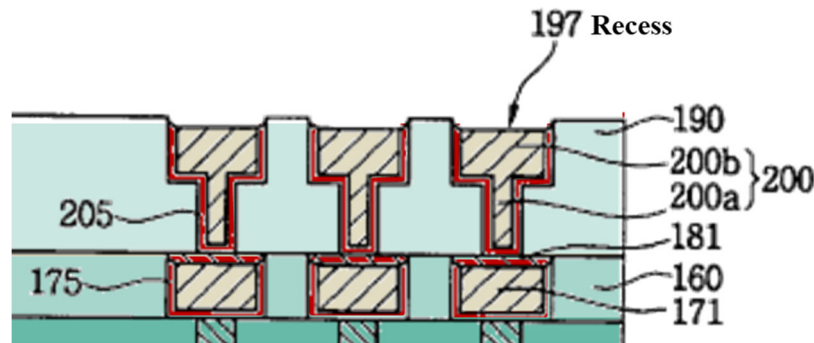
c. Claim 4

4. The image sensor according to claim 1, wherein the first metal interconnection has a top surface lower than that of the first interlayer dielectric, such that the first metal interconnection and the first interlayer dielectric have a height difference.

320. The Imaoka-Choi Sensor satisfies claim 4’s additional limitation that the first metal interconnection has a top surface lower than that of the first ILD, such that there is a “height difference” between the two, because Choi discloses creating a recess for a top barrier layer, a common practice and would have been an

obvious when implementing copper interconnections in Imaoka's sensor with Choi's processes. *See* Section XI.E.2.f (starting on page 148); Choi (Ex. 1007), [0128]-[0129], Figs. 5E, 5F (excerpted and annotated, below), and 5G. Claim 4 is thus unpatentable as obvious.

Choi, Fig. 5F (Excerpted, Annotated)



d. Claim 5

5. The image sensor according to claim 1, wherein the second metal interconnection comprises copper (Cu) or aluminum (Al).

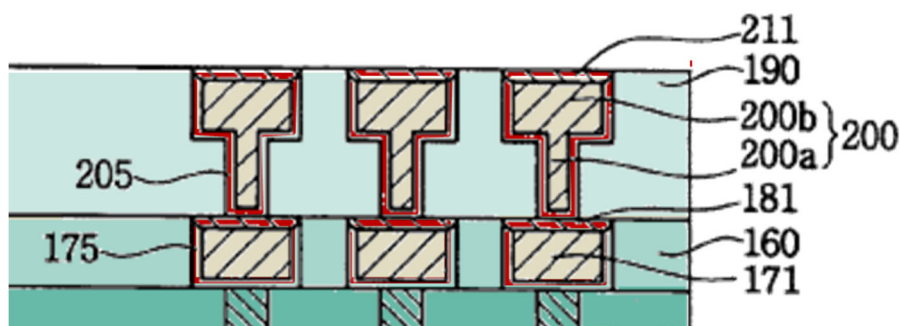
321. The Imaoka-Choi Sensor satisfies claim 5's additional limitation that the second metal interconnection comprises copper or aluminum (*see* Section XI.C.4, starting on page 135) and this aspect would remain unchanged after modification. Claim 5 is thus unpatentable as obvious.

e. Claim 6

6. The image sensor according to claim 1, wherein the conductive barrier layer has at top surface substantially even with the top surface of the first interlayer dielectric.

322. The Imaoka-Choi Sensor satisfies claim 6's additional limitation that the conductive barrier layer has at top surface substantially even with the top surface of the first ILD because Choi discloses depositing a barrier layer in a recess above the copper interconnections and planarizing so the top surface of the barrier layer is even with the top surface of the first ILD, a common practice, and would have been obvious when implementing copper interconnections in Imaoka's sensor with Choi's processes. *See* Sections XI.E.2.f (starting on page 148); Choi (Ex. 1007), [0129] (referencing back to [0122]-[0123]), Fig. 5G (excerpted and annotated, below). Claim 6 is thus unpatentable as obvious.

Choi, Fig. 5G (Excerpted, Annotated)



f. Claim 7

7. The image sensor according to claim 1, wherein the first via and the second via comprise the same material.

323. The Imaoka-Choi Sensor satisfies claim 7's additional limitation that the first via and the second via comprise the same material (*see* Section XI.C.6, starting on page 137) and this aspect would remain unchanged after modification. Claim 7 is thus unpatentable as obvious.

g. Claim 8

8. The image sensor according to claim 1, wherein the second semiconductor substrate provides metal interconnections for connection to a power line and an external signal line.

324. The Imaoka-Choi Sensor satisfies claim 8's additional limitation that the second semiconductor substrate provides metal interconnections for connection to a power line and an external signal line (*see* Section XI.C.7, starting on page 137) and this aspect would remain unchanged after modification. Claim 8 is thus unpatentable as obvious.

**F. Ground 6: Imaoka in view of Choi and Dublin Renders
 Claim 3 Obvious**

325. When implementing the Imaoka-Choi Sensor discussed in Ground 5, it would have been obvious to use a CoWP alloy for the conductive barrier layer as disclosed in Dublin—thereby also rendering obvious claim 3, which depends from claim 1 and further requires cobalt or nickel alloy for the conductive barrier layer.

1. Reasons to Use a CoWP Barrier Layer

326. POSAs would have used CoWP as the conductive barrier layer for the same reasons discussed in Sections XI.B.1 (starting on page 118) and XI.D.1 (starting on page 138).

2. Resulting Sensor and Reasonable Expectation of Success

327. The resulting sensor would be identical to the Imaoka-Choi Sensor described in Ground 5 except using CoWP as the conductive barrier material. POSAs would have had a reasonable expectation of successfully using CoWP as a barrier material because it is fabricated using the industry-standard dual-damascene process. *Compare* Section XI.E.2 (starting on page 143) *with* Dublin, 8:1-65. And this was the very thing my team at Kodak did in 2005 when we substituted a CoWP barrier layer for a SiN barrier layer disclosed by the basic process disclosed in 1999. Gambino (Ex. 1023), 25.

3. Claim 3 Analysis

3. The image sensor according to claim 1, wherein the conductive barrier layer comprises cobalt (Co) or nickel (Ni) alloy.

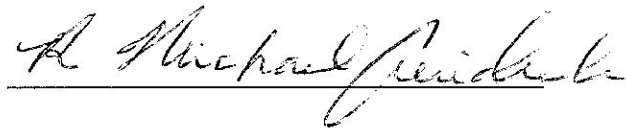
328. The resulting sensor would include a conductive metal barrier layer that comprises cobalt (Co), thereby rendering claim 3 obvious. Dublin discloses a “technique of electrolessly depositing CoWP as a barrier material in order to protect or encapsulate a conductive material” such as “copper.” Dublin (Ex. 1008), 2:63-66. Figure 10 of Dublin “is a cross-sectional view showing a selective formation of another CoWP barrier layer of the present invention above the copper.” *Id.*, 3:53-55. CoWP is conductive. Ex. 1020, 1:22-23 (“a conductive barrier film such as cobalt tungsten phosphorous (CoWP) is formed on a Cu wiring”). Dublin’s conductive CoWP barrier layer as used in the Imaoka-Choi Sensor thus satisfies and renders obvious claim 3.

* * *

I declare that all statements made herein of my own knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

I declare under penalty of perjury that the foregoing is true and correct.

Dated: 12/1/2022

A handwritten signature in cursive script, reading "R. Michael Guidash", written over a horizontal line.

R. Michael Guidash

APPENDIX A TO THE DECLARATION OF R. MICHAEL GUIDASH

CLAIM LISTING

Ref	Claim
[1.pre]	An image sensor, comprising:
[1.1]	a second semiconductor substrate including a second metal interconnection and a second interlayer dielectric;
[1.2]	a second via penetrating the second interlayer dielectric so that the second via is connected to the second metal interconnection;
[1.3]	a first semiconductor substrate on the second interlayer dielectric, the first semiconductor substrate having a unit pixel;
[1.4]	a pre-metal dielectric on the first semiconductor substrate;
[1.5]	a first via penetrating the pre-metal dielectric and the first semiconductor substrate, the first via being connected to the second via;
[1.6]	a first interlayer dielectric on the pre-metal dielectric including the first via;
[1.7]	a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel;
[1.8]	a conductive barrier layer on the first metal interconnection; and
[1.9]	a color filter and a microlens on the first interlayer dielectric on the unit pixel.
2	The image sensor according to claim 1, wherein the first metal interconnection comprises copper (Cu).
3	The image sensor according to claim 1, wherein the conductive barrier layer comprises cobalt (Co) or nickel (Ni) alloy.
4	The image sensor according to claim 1, wherein the first metal interconnection has a top surface lower than that of the first interlayer dielectric, such that the first metal interconnection and the first interlayer dielectric have a height difference.
5	The image sensor according to claim 1, wherein the second metal interconnection comprises copper (Cu) or aluminum (Al).
6	The image sensor according to claim 1, wherein the conductive barrier layer has at top surface substantially even with the top surface of the first interlayer dielectric.
7	The image sensor according to claim 1, wherein the first via and the second via comprise the same material.
8	The image sensor according to claim 1, wherein the second semiconductor substrate provides metal interconnections for connection to a power line and an external signal line.