

Handbook of **Semiconductor Manufacturing Technology**

Second Edition

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16.1 Introduction

16.1.1 Damascene Process

Formation of interconnect circuitry for integrated circuits (IC) or other electronic components is normally accomplished through either subtractive or additive processing. In subtractive processing, a continuous layer of metal is deposited on a dielectric substrate. The interconnect circuit pattern is then generated by etching away undesired metal, usually as defined by a photoimaged resist pattern. Interconnects for IC's have traditionally been formed by subtractive dry etching of blanket aluminum alloy films to produce the desired circuit lines as defined by a photoresist pattern. In a standard additive process, a circuit pattern is generated in photoresist laminated onto a thin metal seed covering a dielectric

surface. Metal is next deposited, usually by electroplating, on the seed surface which is defined by the resist pattern to form full-thickness metal lines. Finally, the resist and seed layer are removed leaving only the metal circuit pattern. Additive processes have traditionally been used in high-end printed circuit board and flexible circuitry applications.

A unique variety of additive processing, known commonly as the damascene process, was introduced by IBM [1–3] in the 1990s as a means for the formation of copper IC interconnects. Using this process, a line or via pattern is defined by photo-processing and this pattern is etched into a dielectric layer. Following etching of the dielectric, the photoresist is removed and a copper diffusion barrier, such as tantalum, and a copper seed layer are sequentially deposited on all surfaces of the dielectric. The seed layer provides the conductivity across the wafer necessary for the electroplating process, as well as a surface upon which nucleation of the electroplated film can begin. Copper is then electroplated to form the desired circuitry by filling the seeded recesses in the dielectric [4]. Using this process, however, copper is also electroplated on the entire surface of the wafer as a continuous film. This excess copper is removed in a subsequent chemical mechanical polishing (CMP) step to define the circuit pattern. A variation of the damascene process, known as the dual damascene process, has been widely implemented as the most cost-effective means of producing copper interconnect circuitry. Using dual damascene processing, a via layer and an interconnect line layer are sequentially photoimaged and etched prior to seeding and plating. This eliminates several process steps compared to either two single damascene process steps or traditional subtractive aluminum processing with tungsten vias. The dual damascene plating sequence is illustrated in Figure 16.1.

16.1.2 The Need for Copper

The cost savings associated with the copper dual damascene process sequence may be significant in some applications, however, the transition from aluminum to copper interconnects has been driven primarily by three technical reasons [1–3]. First, the resistivity advantage of copper over aluminum has significantly reduced RC delay times in advanced logic devices, as well as allowed for smaller line dimensions

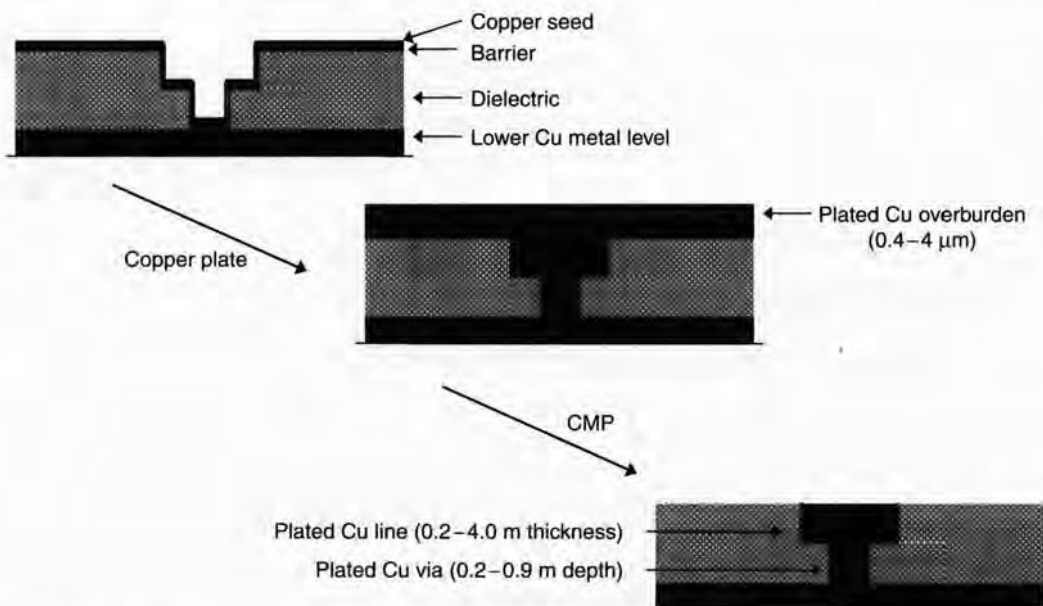


FIGURE 16.1 Damascene line formation sequence.

without increased heat generation. Second, as circuit dimensions decrease and line current densities increase the Electromigration (EM) life advantage of copper relative to aluminum becomes critical in ensuring device life. Finally, the extendibility of aluminum etch to circuit dimensions below $0.10\text{ }\mu\text{m}$ has been difficult, while damascene processing of copper is easily extendable below these dimension. Taken together, the advantages of copper interconnects result in interconnect solutions with flexibility to achieve improved EM life, higher device speed, less heat generation, and fewer interconnect metal levels depending on specific requirements. As a result of these advantages, nearly all high performance logic devices have made the transition to copper, as of 2004 [5].

16.1.3 Alternatives to Electrodeposition for Damascene Applications

Electrodeposition on a physical vapor deposition (PVD) seed layer to form dual damascene circuits was not initially recognized as a preferred means of copper interconnect formation. Early development of copper interconnect formation concentrated on chemical vapor deposition (CVD) [6,7], electroless copper deposition [8,9], and PVD [10] methods. In some cases, these methods were combined with each other or with copper reflow processes [11] as a means for deposition of seed layers or bulk copper films. Nearly all studies concluded that optimum adhesion of copper to barrier films was obtained using PVD copper deposition, thus necessitating the use of PVD copper as an initial seed layer. For bulk copper deposition, electroless, and CVD processes available resulted in a conformal film of copper within features and on the wafer surface. As shown in Figure 16.2, this can lead to a seam or void in the center of copper lines if the dielectric etch profile is re-entrant or near vertical. Such seams present reliability concerns in a metal such as copper, which can undergo EM. As also shown in Figure 16.2, PVD processes result in large voids within features when used for bulk copper deposition owing to the geometric limitation of metal flux into the feature relative to the flux on the field. While very high pressure and temperature have been shown to reflow copper into features, this approach has not been put into practice.

By providing a continuous film across the wafer surface and within features, PVD copper seed meets the basic requirement of electrical continuity needed for subsequent copper electrodeposition. Subsequent electrodeposition processes would be expected to yield conformal film deposition and seam voids as observed for CVD or electroless copper plating, however, it was recognized that copper electrodeposition using certain organic additives could result in accelerated copper growth from the base of high aspect ratio (AR) features resulting in void-free filling as shown in Figure 16.2. This capability of void-free filling, along with the near bulk resistivity value of the plated Cu and the relatively low cost of electrodeposition, led to its selection for interconnect formation.

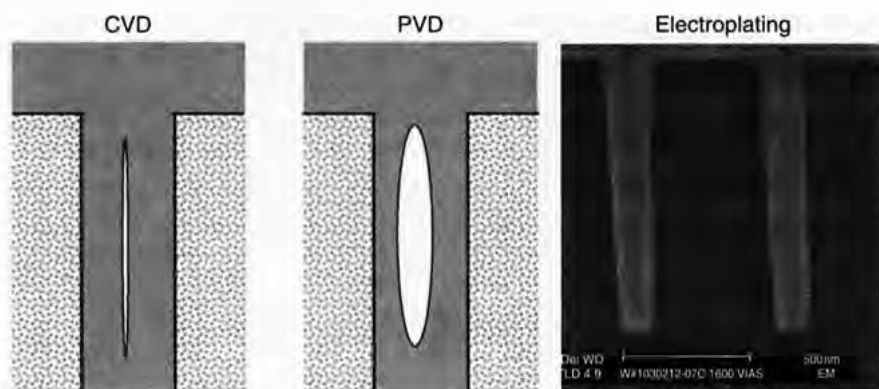


FIGURE 16.2 Profiles of copper deposits in high aspect ratio features formed using CVD, PVD, and electroplating processes.

16.1.4 Cu Electroplating Evolution and Applications

Electrodeposition of metal is performed by immersing a conductive surface in a solution containing ions of the metal to be deposited. The surface is electrically connected to an external power supply and current is passed across and through the surface to be plated causing reaction of the metal ions (M^{z+}) of charge (z) with electrons (e^-) to form metal (M):



Copper electrodeposition from sulfate solutions was first investigated in the early 1800s [12]. Important industrial applications since that time have included flatware plating, wire, and foil formation, and printed circuit and connector formation. Concurrently, the relatively simple reaction kinetics of cupric ion reduction in sulfate solutions resulted in its use as the standard chemistry for most early fundamental electrochemical studies. Recently, interest in copper plating as a method of forming IC interconnects has increased. The evolution of activities related to copper electrodeposition is summarized in Figure 16.3.

16.1.5 Cu Deposition for Damascene Applications

In the case of electrodeposition of copper onto a silicon wafer, the wafer is typically coated with a 50–300 Å thick Tantalum based diffusion barrier and a 300–2000 Å thick copper seed layer prior to plating. The seed layer should have acceptable adhesion to the barrier layer, provide adequate conductivity across the surface of the wafer, and be continuous with full coverage in high aspect ratio features to be filled during the plating process. As illustrated in Figure 16.4, the seeded wafer is immersed in a solution containing cupric ions, sulfuric acid, chloride ion and proprietary additives. Electrical contact is made to the seed layer and current is passed such that the reaction $Cu^{2+} + 2e^- \rightarrow Cu(O)$ occurs at the wafer surface. The wafer is referred to as the cathode. Another electrically active surface, known as the anode, is present in the conductive solution to complete the electrical circuit. At the anode, an oxidation reaction occurs which balances the current flow at the cathode, thus maintaining electrical neutrality in the solution. When a copper anode is used during copper plating, all cupric ions removed from solution by deposition onto the wafer are replaced by dissolution of the anode.

In the absence of any secondary reaction, the current delivered to a conductive surface during electroplating is directly proportional to the quantity of metal deposited (Faraday's law of electrolysis).

$$W = ItA_w/nF \quad (16.2)$$

where W , weight of deposit in grams; t , time in seconds; I , current in Amperes; F , Faraday constant (96,500 C/eq); n , number of electrons transferred per atom deposited; A_w , atomic weight.

Using this relationship, the mass of Cu deposited can be readily controlled through variations of plating current and time.

With no applied potential and no imposed current flow across the interface between a metal and a solution, an equilibrium potential exists between the two. This potential is often known as the rest potential. Once potential is shifted from the equilibrium potential by an external power source, a current will be driven across the interface. Under conditions typical of most plating processes, this current density (I) is approximated by an exponential relationship known as the Tafel equation.

$$I = i_0[e^{-\alpha n F \eta / RT}] \quad (16.3)$$

where i_0 , exchange current density; α , charge transfer coefficient; η , applied potential (V); T , absolute temperature; R , gas constant.

Figure 16.5 shows a current–potential curve typical of a copper deposition process. As potential applied to the wafer is scanned from the equilibrium potential to more negative values, the current

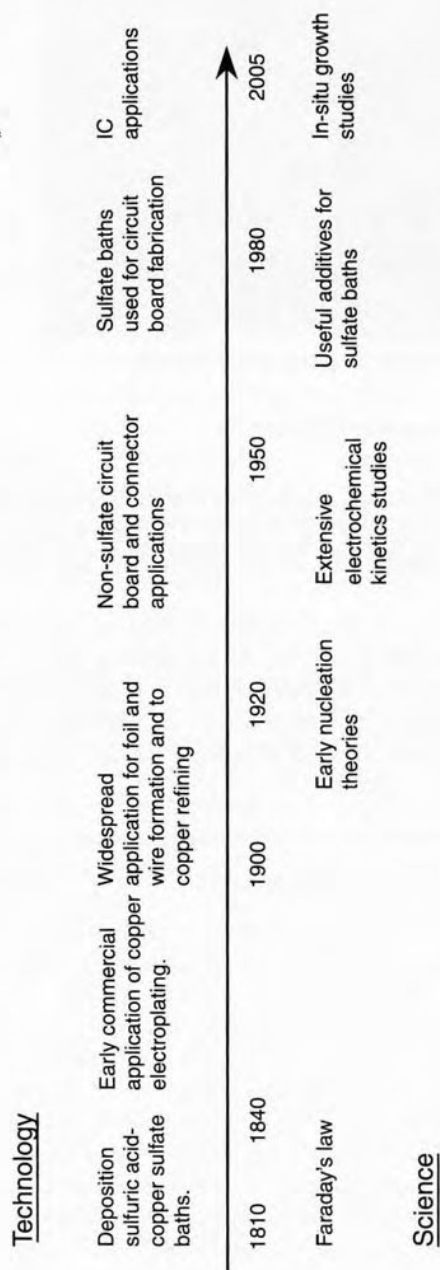


FIGURE 16.3 Evolution of copper electroplating.

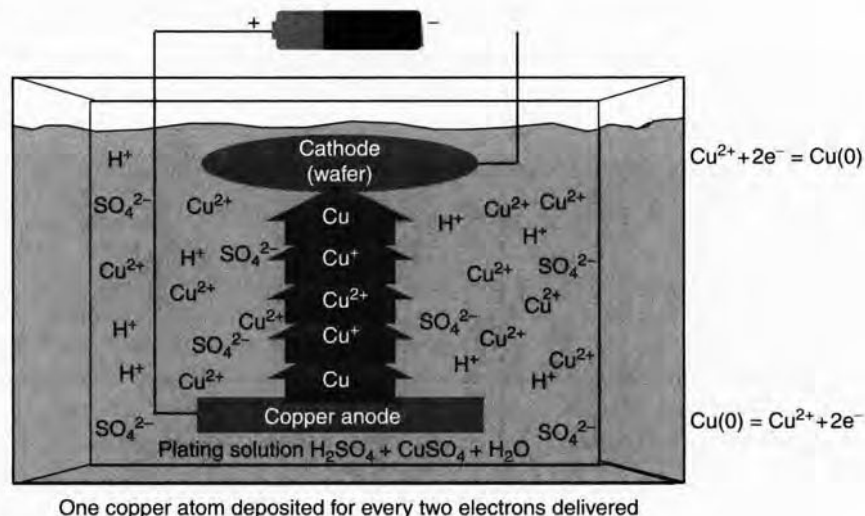


FIGURE 16.4 Schematic diagram of copper electroplating cell.

increases in an exponential manner (Tafel region) where the overall deposition rate is determined largely by charge transfer or reaction rate kinetics at the cathode. This strong dependence of current upon potential results in the need for plating cell designs which yield uniform potentials across the wafer surface.

As the potential continues to increase, mass transfer limitation on current gradually becomes dominant and a limiting current plateau is reached. At the limiting current species reacting at the cathode (Cu^{2+}) no longer reach the interface at a rate sufficient to sustain the rate of reaction possible at a high applied potential. As a general rule, plating processes are operated at currents no greater than 30%–50% of the limiting current in order to avoid undesirable deposit characteristics.

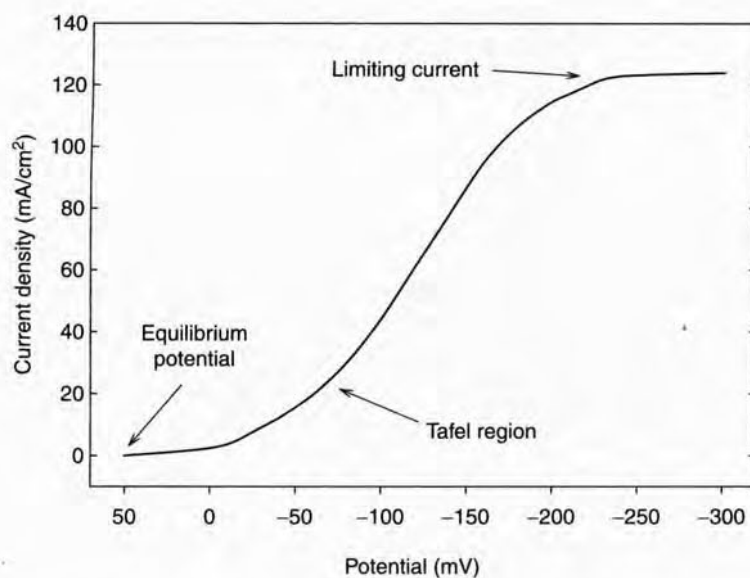


FIGURE 16.5 Current–potential relation for Cu electroplating.

To ensure that the rate of mass transfer of electro-active species to the interface is large compared to the reaction rate, and uniform across the wafer surface, the rates of cupric ion migration, diffusion, and convection must be understood and controlled. During wafer electroplating, convection must be accurately controlled while diffusion and migration are characteristic of a process but not normally controlled. Mass transfer due to convection can vary from stagnant to laminar or turbulent flow depending on hardware configuration. Convection includes impinging flow caused by solution pumping, flows due to substrate movement, ultrasonics, and flows resulting from density variations.

Electroplating can be carried out using a constant current, a constant voltage, or waveforms involving variable current or voltage. Using a constant current, accurate control of the mass of deposited metal is most easily obtained based on Faraday's law. Plating at a constant voltage and using variable waveforms requires more complex equipment and control, but can be useful in tailoring specific thickness distributions and film properties. A constant voltage also allows deposition at a uniform current density while plated surface area changes.

Copper plating bath components include sulfuric acid, copper sulfate, chloride ion, and trace organic additives [12,13]. Copper sulfate is added to baths to maintain the concentration of cupric ions in the range of 10–70 g/L. Low concentrations of cupric ion are utilized to obtain optimum thickness distribution control [14]. High cupric ion concentrations allow generally higher plating currents (deposition rate) and thus can allow increased throughput. Sulfuric acid concentrations up to 300 g/L can be utilized. High acid concentrations are often chosen to provide high solution conductivity and thus reduce electric field variability in the bath. A uniform electric field is essential to obtain a uniform current density and deposition rate [15]. Low acid concentrations uniformly increase bath resistance between the wafer and the anode and thus reduce the relative impact of seed resistance on current flow across the wafer. This reduces center-to-edge deposition rate variability on thin seeds which otherwise tend to plate more rapidly near the wafer edge where electrical contact is made [16,17]. Chloride ions are present in the bath at concentrations in the range of 30–100 mg/L.

Complex mixtures of organic chemicals are added to copper plating baths to influence deposit metallurgy and deposit thickness distribution. A typical additive mixture contains one or more chemicals which act to increase the current at a given voltage (accelerators), and at least one other class of molecules that act to reduce current at a given voltage (suppressers). Together, and at proper concentrations, these additives largely determine the desired filling behavior, grain structure, and purity of the deposited copper and as a result control ductility, hardness, surface roughness, stress, and tensile strength.

Primary responses to be considered during process optimization for copper electroplating of IC interconnects include filling performance, within die uniformity, within wafer uniformity, grain size, copper electromigration behavior, defects in the deposited film, and defects in the circuitry following CMP. Variables that will impact these responses include concentrations and types of accelerators, suppressors, and leveler, concentrations of chloride ion, copper, and acid, and other parameters such as flow, temperature, current density, and current waveform [18,19]. Achievement of robust filling performance required for a given product usually determines the general parameter space over which all responses must be investigated by process window experiments.

In order to fully fill high aspect ratio features with copper during electroplating, it is essential that the plating process proceed at an accelerated rate within the features compared to the rate on the surface of the wafer. This super-filling behavior is achieved by selection of organic additives which suppress the plating rate on the surface of the wafer relative to the rate within the feature. Differences in plating rate between the surface and feature base have been attributed to the slower mass transfer rate of current suppressing additive species into the features compared to the mass transfer rate to the surface. More recent filling models are based on the gradual accumulation of current accelerating species within high aspect ratio features as their internal surface area decreases during initial plating [18–21].

Figure 16.6 shows a typical sequence in which a high aspect ratio via with a thin copper seed layer is filled with electroplated copper. Initially the seed layer coverage within the via is only a few hundred angstroms thick, while the thickness on the wafer surface is over 1000 Å. Following electrodeposition for 10 s, the copper growth rate on via sidewalls is approximately equal to the growth rate on the wafer

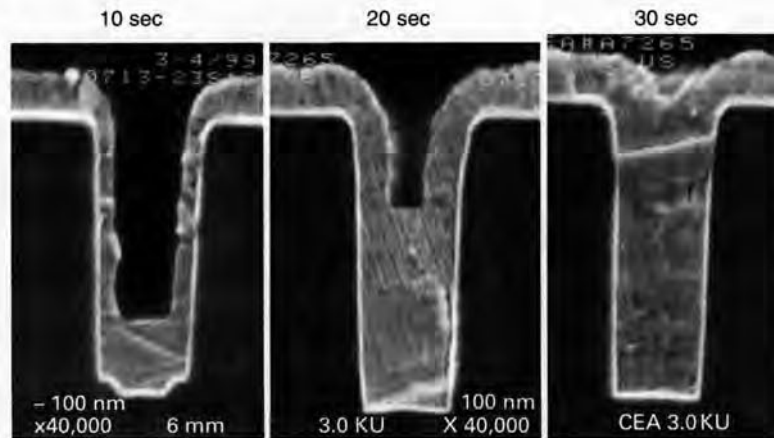


FIGURE 16.6 Deposition of copper in 0.3 μm vias as a function of plating time at a current density of 10 mA/cm^2 .

surface and the growth rate at the base of the via has accelerated. Both of these aspects of initial growth behavior are required for successful filling of damascene features by electrodeposition. Initial nucleation and growth on all surfaces is necessary to prevent sidewall void formation, and accelerated growth at the feature base is required to achieve complete fill prior to pinch-off of the feature due to conformal growth at the feature neck. Fill continues from the bottom up, until it is complete after about 30 s. Depending on the organic additives and the current waveform, accelerated growth may continue after filling is complete. This leads to an excessive deposit thickness over superfilled features and increases the difficulty of the subsequent CMP process.

Copper can also be deposited from solutions using electroless and immersion deposition [8,9]. Electroless deposition is analogous to electroplating in many respects, however, the electrons required for cupric ion reduction are supplied by chemical reactions involving a reducing agent such as formaldehyde, thus eliminating the need for power supplies and electrical connection to plated surfaces. Immersion plating takes place when metal ions in solution are reduced to form metal atoms on a surface which itself is oxidized to supply the required electrons, thus limiting this method to very thin film depositions on readily oxidized surfaces. These processes have not been implemented in damascene applications.

16.2 Fundamentals of Electroplating

16.2.1 Kinetics

The relationship equating electromotive force (EMF) or voltage to free energy of an electrochemical charge transfer reaction in solution is given by Equation 16.4:

$$E_0 = -\Delta G/nF \quad (16.4)$$

where E_0 , standard EMF of cell reaction ($\text{Cu}^{2+} + 2e^- = \text{Cu}$) (V); n , number of electrons per atom reacted; F , charge on a mole of electrons (Faraday constant, C/mol); ΔG , free energy of reaction (J/mol).

The units of the terms in this equation are seen to be equivalent since

$$V = J/C = (J/\text{Mol})/\{(\text{electrons/atom})(C/\text{Mol})\}.$$

The standard EMF for an electrochemical reaction such as $\text{Cu}^{2+} + 2e^- = \text{Cu}$ must be expressed as a voltage relative to some other reaction as explained in detail in electrochemistry textbooks [22]. It has been found that a convenient and reproducible reference voltage (NHE) is created by the reaction of

Reaction	Reduction potential vs NHE
$\text{Au}^+ + \text{e}^- = \text{Au}$	1.68
$\text{O}_2 + 4\text{H}^+ + 4\text{e}^- = 2\text{H}_2\text{O}$	1.229
$\text{Pt}^{2+} + 2\text{e}^- = \text{Pt}$	1.2
$\text{Ag}^+ + \text{e}^- = \text{Ag}$	0.799
$\text{Cu}^{2+} + 2\text{e}^- = \text{Cu}$	0.345
$2\text{H}^+ + 2\text{e}^- = \text{H}_2$	0
$\text{Pb}^{2+} + 2\text{e}^- = \text{Pb}$	-0.126
$\text{Sn}^{2+} + 2\text{e}^- = \text{Sn}$	-0.134
$\text{Ni}^{2+} + 2\text{e}^- = \text{Ni}$	-0.23
$\text{Co}^{2+} + 2\text{e}^- = \text{Co}$	-0.28
$\text{Cd}^{2+} + 2\text{e}^- = \text{Cd}$	-0.403
$\text{Fe}^{2+} + 2\text{e}^- = \text{Fe}$	-0.409
$2\text{H}_2\text{O} + 2\text{e}^- = \text{H}_2 + 2\text{OH}^-$	-0.827
$\text{Ti}^{2+} + 2\text{e}^- = \text{Ti}$	-1.63
$\text{Al}^{3+} + 3\text{e}^- = \text{Al}$	-1.76
$\text{Na}^+ + \text{e}^- = \text{Na}$	-2.71

FIGURE 16.7 Electrochemical series of standard E_0 values for reduction of metal ions.

hydrogen gas to form hydrogen ions and electrons on a platinum electrode surface. Based on the definition of the EMF for the hydrogen oxidation reaction as 0.00 V, the standard reduction potentials (E_0) of several metals at 1.0 M solution concentration are given in Figure 16.7. Equilibrium reduction potentials (E) for divalent metal ions shift by about 29 mV per decade of metal ions activity [O] change from the 1.0 M reference point according to the Nernst equation:

$$E = E_0 + (RT/nF)\ln[\text{O}] \quad (16.5)$$

where [O], molar concentration of oxidized species.

Metals that are thermodynamically unstable, such as sodium, exhibit negative potentials for reduction of the ion to the metal. The negative potentials correspond to a relatively non-spontaneous positive free energy of reaction. Noble metals, such as gold, which are thermodynamically stable, exhibit positive potentials for reduction of the ion to the metal. The positive potentials correspond to a negative free energy of reaction. As illustrated in Figure 16.8, when a potential more negative than the E_0 value of a metal/ion couple is applied at a surface immersed in a solution containing ions of the metal, reduction of the metal ion to the metal takes place. This is an electroplating process. In the convention normally used for electroplating, the electrons supplied for the metal ion reduction constitute a positive current flow. If the potential is held at the E_0 value no current will flow, while if the potential is held at a value more positive than E_0 the metal will thermodynamically favor dissolution to metal ions resulting in a negative current flow. Numerous factors can influence the rates of reduction and oxidation reactions as the potential of an interface is moved away from E_0 . Kinetically fast reactions can allow current to increase sharply with applied voltage changes of less than 50 mV, while slow reactions require larger applied voltages to drive substantial current. Typical electroplating reactions take place at applied interfacial potentials of several tenths of a volt relative to their E_0 value.

Using standard electrochemical conventions, the applied voltages which result in a substantial current flow corresponding to metal ion reduction becomes increasingly negative as the metal ion to be reduced

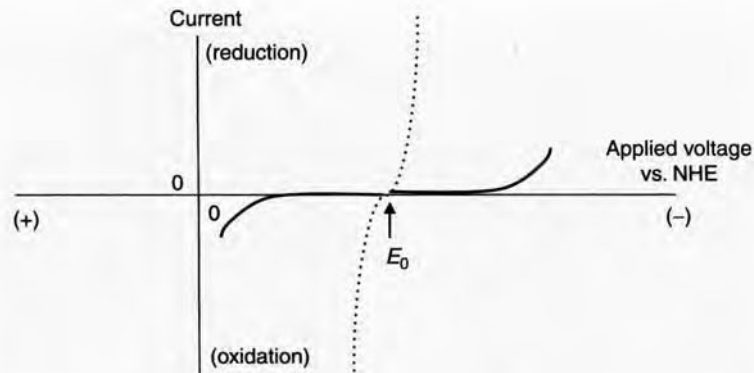


FIGURE 16.8 Current as a function of applied potential for metal ion reduction and oxidation at metal surface with high and low degrees of charge transfer resistance.

becomes less noble (see Figure 16.9). When an electrolyte contains several metal cations which can be electroplated onto a cathode, the voltage which is applied will determine which reactions proceed. As shown in Figure 16.9, a voltage of about -0.3 V relative to Normal hydrogen electrode (NHE) will cause cupric ion reduction. At this applied voltage, free metal ions such as Pt and Ag will also undergo reduction. Ions in solutions such as Ti will not be reduced, and water itself is stable. As a result of this behavior, copper deposition can be carried out in practical systems containing significant levels of metals such as Na, K, Ti, Ca, Fe, and Mg, which are difficult to reduce without resulting in significant deposit contamination. Electrolyte contamination with Ag, Au, or other noble metals will result in their co-deposition when copper plating is carried out.

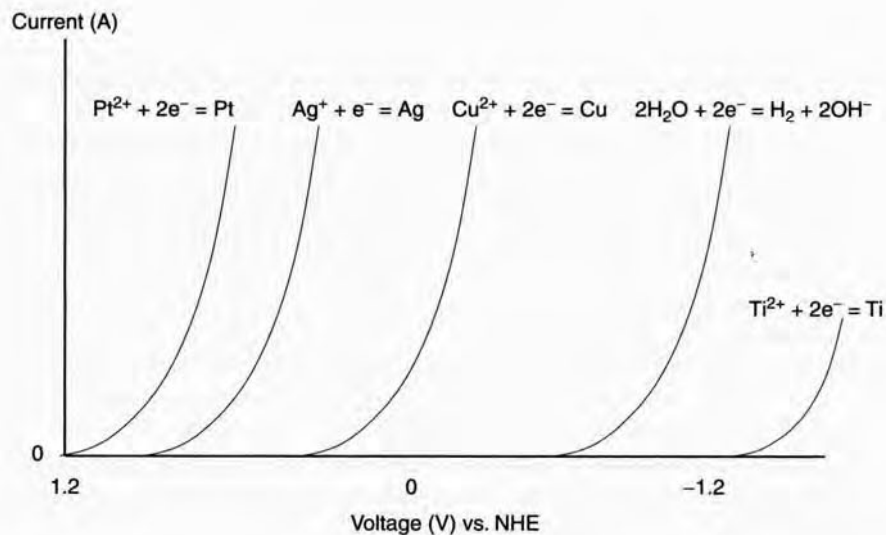


FIGURE 16.9 Current-potential characteristics for reduction of several metal ions and water.

Although plating is normally performed at controlled currents, it is convenient to express current flow at a given point on the cathode surface as a function of applied voltage, interfacial kinetics, and mass transfer using the relationship:

$$I = i_0[O_{(0,t)}]e^{-\alpha nF(E_a - E)/RT} \quad (16.6)$$

where $E_a = \eta + E$, applied potential at metal/solution interface; $O_{(0,t)}$, oxidized species concentration at the interface at a given time and other terms are as defined previously. While this equation is generally difficult to solve, it accurately reflects the effects of applied interfacial potential, concentration of the ion at the interface, and inherent interfacial kinetics on the reduction current at a given point on a surface.

Increases in applied potential result in exponential increases in the deposition current at a given interfacial ion concentration and exchange current. In this respect, the current dependence on potential can be considered analogous to a reaction rate dependence on temperature in an Arrhenius equation. Alternatively, the interface can be considered as a resistance element in an equivalent circuit, which decreases in value as the applied voltage increases.

The exchange current determines deposition current sensitivity to applied voltage and interfacial concentration changes. Large exchange currents, which correspond to very rapid and usually reversible metal reduction charge transfer kinetics, result in strong dependence of the deposition current on mass transfer and applied potential. A comparison of exchange current impact on deposition current sensitivity to applied potential is illustrated in Figure 16.8. In copper plating systems, the exchange current can be reduced by deposition at lower temperatures and use of organic additives, which slow kinetics.

The current flow at a given point on the surface is proportional to the concentration of metal ions at the interface regardless of other factors. The interfacial concentration is typically increased by faster mass transfer and higher bulk concentrations of metal ion in solution. Figure 16.10 illustrates metal ion concentration profiles as a function of distance from the cathode at different mass transfer rates assuming a fixed current density. Faster mass transfer corresponds to a higher interfacial ion concentration and a shorter distance from the interface at which the bulk ion concentration is reached. Plots of the cupric ion deposition current density as a function of applied potential are shown in Figure 16.11 for several rotating disk electrode rotation rates. The range of rotation rates includes the range of mass transfer conditions normally employed during wafer processing. At low applied potentials or current, a relatively

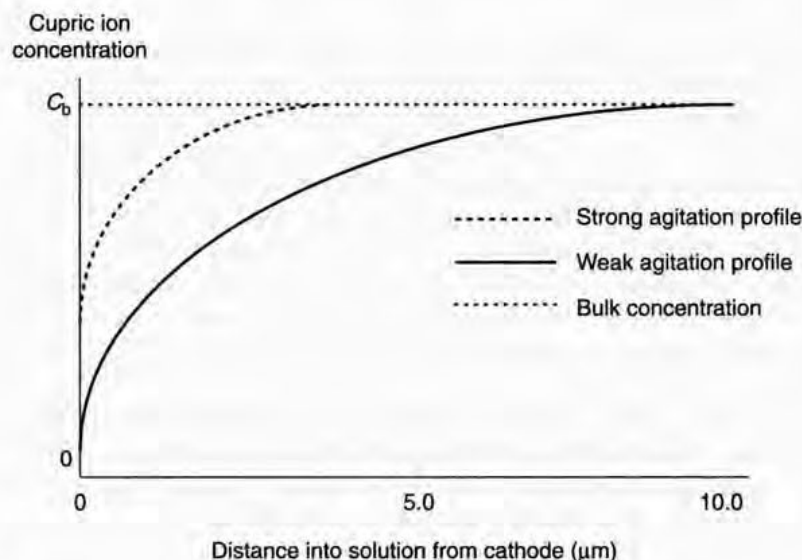


FIGURE 16.10 Cupric concentration profiles in solution at fixed current.

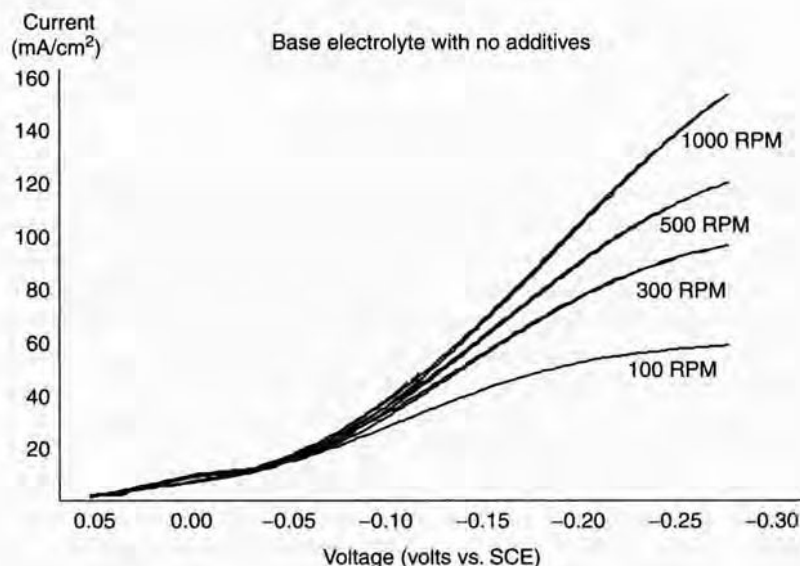


FIGURE 16.11 Effect of mass transfer on I-E relationship.

small dependence of the current density on the mass transfer rate is seen. Gradually, as applied potential or current is increased and larger concentration gradients develop between the interface and the bulk solution, the dependence of the current density on the mass transfer rate increases.

Thus, based on Equation 16.6, uniform deposition rates across large surfaces such as wafers can best be generated using uniform mass transfer and applied potential conditions across the wafer surface. Selection of process conditions with a relatively low exchange current will also enhance thickness uniformity.

16.2.2 Mass Transfer

Mass transfer of metal ions in electroplating solutions takes place as a result of convection, diffusion, and migration mechanisms. Convection includes ion movement as a result of pumping of plating solution to achieve directed flow, mechanical agitation or rotation, ultrasonics, and as a result of thermal gradients. In electroplating systems, convection due to pumping and mechanical agitation is usually primarily responsible for maintaining equilibrium concentrations of species across distances much greater than a distance of about 1 mm. Both laminar or turbulent flow are common, with laminar flow generally desired except when very high rates of mass transfer are required to achieve a high current density and rate of deposition. Increasing convection decreases the thickness of the stagnant diffusion layer at the cathode interface. Typical diffusion layers, across which diffusion and migration of the cupric ions are the primary means of mass transfer, range from a few microns to about 100 μm in thickness.

Migration is the movement of ions which takes place as a result of the potential gradient applied across a solution between the anode and the cathode during plating [22]. As a result of migration, cations will move toward the negatively charged cathode and anions will move toward the positively charged anode. In the bulk of the plating solution, the amount of mass transfer due to migration is negligible. However, near the interface where convection is small, migration of a metal ion can become significant when the charge carrying capacity of the metal ion in solution becomes significant compared to the charge carrying capacity of other ions in solution. This condition takes place when the transport number for the metal

ion, T_i , as given in Equation 16.7, becomes a significant fraction of 1.0.

$$T_i = \frac{C_i Z_i D_i}{\sum C_x Z_x D_x} \quad (16.7)$$

C_i, C_x , concentrations of metal ion and other ionic species respectively; Z_i, Z_x , charge of metal ion and other ionic species respectively, D_i, D_x , diffusion coefficient of metal ion and other ionic species respectively.

In typical copper plating applications, the high concentration and diffusion coefficient of hydrogen ions result in its domination of charge migration behavior. This results in relatively small amounts of migration of cupric ion toward the interface compared to the rate of diffusion. In plating solutions with very low amounts of hydrogen ions, however, mass transfer of cupric ion toward the interface can be increased due to migration.

Diffusion, the movement of ions in solution across a concentration gradient, is relatively fast across distance scales such as the dimension of IC features or the stagnant interfacial diffusion layer. For cupric ion, a diffusion coefficient of $5 \times 10^{-6} \text{ cm}^2 \text{ s}^{-1}$ [23] results in a 0.1 ms time for diffusion across a 0.1 μm distance, and a 1.0 ms time for diffusion across a 10 μm distance. The short times for diffusion across these distances result in ample replenishment of cupric ion within high aspect ratio features during a typical 5–20 s filling process even though the volume of solution containing sufficient cupric ion to form the copper metal deposit in a feature is 200–400 times the feature volume.

16.2.3 Geometry Effects on Local Kinetics

So far, the deposition process has been considered as if it were taking place at a single point or assuming that all points on a surface are equivalent. Although the basic kinetic and mass transfer behavior can be consistent across a surface, the actual interfacial voltage, which drives the deposition reaction usually varies with position on the surface [24–26]. For example, the interfacial voltage may be different at the center and the edge of a wafer for several reasons. The variation of the interfacial voltage across a plated surface can be broken in to four classes of behavior. First, if part of a plated surface is closer to the anode than another part of the plated surface, then the voltage drop through the solution from the anode to the closer cathode surface is smaller and more voltage is available to drive the deposition reaction at the closer surface. A higher current on the surface closer to the anode results. This behavior is utilized in Hull cell testing to conveniently observe plated deposit appearance across a wide range of current densities, but is not usually a factor in well designed plating cells which maintain a constant anode to cathode distance. Second, the edge of a plated surface will normally plate at a higher rate than an adjacent continuous surface. This behavior is often characterized as a field or antenna effect, however, it is more accurate to consider that the ohmic voltage drop from an anode through solution to an edge will be less than the corresponding voltage drop from the anode to a non-edge surface. Edge effects can be prevented by using a plating cell with internal wall dimensions defined by an insulating cylinder of internal dimension equal to the wafer diameter. Third, when plating only part of a surface to form a defined pattern, there are often variations in the density of plated surface area relative to dielectric covered or non-plated area. In this case, the areas of lower plated density will plate more quickly than dense areas. This effect is similar to edge (antenna) behavior and result as a higher available interfacial voltage is possible due to a reduced voltage drop through the bulk of the solution in the less dense pattern area. Normal pattern density effects are not observed in damascene plating since all surfaces are plated, however, an inverse effect due to the high plated surface area within features is possible in high circuit density areas of the wafer before feature fill is complete. Pattern density and edge effects on thickness distribution can be reduced by using highly conducting electrolytes and low plating currents, both of which reduce voltage drop variability in solution. Fourth, a resistive voltage drop across the anode or the cathode itself can result in higher interfacial voltages and plating rates at surfaces nearest an electrical connection to the power supply. In damascene electroplating this is known as the terminal effect and will be described in greater detail in the section covering damascene plating thickness distribution control.

16.3 Damascene Cu Electroplating Chemistry

16.3.1 Electrolytes

Considerations for choosing an electrolyte include solution conductivity, wetting and oxide dissolution ability, rate of dissolution of the copper seed layer in the solution, adequate cupric ion concentration to support high current density, diffusion and migration behavior of the solution, solubility and activity of additives, cost, and waste treatment capability. To date, electrolytes commonly used for damascene copper applications contain sulfuric acid as a supporting electrolyte, copper sulfate pentahydrate as a source of cupric ions, and chloride ion to modulate cupric ion oxidation and reduction reactions. Among the numerous electrolytes used for non-damascene Cu plating applications [12], damascene related evaluations of as methane or propane sulfonic acid/copper sulfonate, and copper pyrophosphate electrolytes have been reported [18].

The sulfate based electrolytes for damascene applications can be divided into three categories based on their composition and performance as summarized in Table 16.1. High acid electrolytes (175 g/L acid, 17.5 g/L Cu) were initially introduced for all damascene applications based on their high solution conductivity and resulting ability to reduce field or edge effects on thickness distribution in various plating cell geometries. The demonstrated manufacturability of the high acid baths for high-end printed circuit board applications was also considered. High acid solutions were also well suited for use with existing additives and were especially effective in rapidly dissolving copper oxide present on the seed layer prior to plating.

As damascene plating evolved, requirements for higher throughput, reduced seed dissolution, and deposition of uniform films on thinner and more resistive seed layers gradually increased. Low acid and intermediate acid or highly saturated electrolytes were introduced to address these issues. In low acid electrolytes, the concentration of sulfuric acid is reduced to about 10 g/L, resulting in a sharp solution resistance increase. While this is detrimental to antenna or edge effects on thickness distribution, the increase in solution resistance reduces the importance of seed layer resistance and improve can the thickness distribution across the wafer. In addition, when the sulfuric acid concentration is reduced, more cupric ion can be added to the electrolyte without exceeding the solubility product of cupric sulfate. Concentrations of cupric ion in low acid electrolytes that are usually 40 g/L or higher allow deposition at relatively high current density without depletion of cupric ion at the interface. Finally, the low concentration of hydrogen ion in these baths begins to result in migration of cupric ion toward the cathode interface (see Equation 16.7). This helps to maintain a high interfacial cupric ion concentration, although the effect still tends to be small compared to the rate of cupric ion diffusion. Potential concerns with low acid electrolytes include the performance of additives and the rate of copper oxide dissolution upon wafer immersion in the bath. The capability of additives to generate bottom-up fill becomes poor as the acid concentration is decreased below about 5 g/L, probably due to increased ionization and solubility and decreased adsorption of the disulfonic acid accelerator molecule.

A compromise between the low and high acid electrolytes, which has been investigated and occasionally used for damascene plating is often called intermediate acid. Typical compositions contain from 20 to 60 g/L of acid and 28 to 70 g/L of copper. The more saturated solutions approach the solubility of copper sulfate in water. This reduces the dissolution of copper seed compared to high

TABLE 16.1 Electrolytes for Damascene Electroplating

Bath Type	Cupric Ion (g/L)	Sulfuric Acid (g/L)	Chloride (mg/L)	Bath Temperature
High acid	15–20	150–200	25–75	20–30
Low acid	35–70	5–20	25–75	20–30
Intermediate acid	30–70	20–60	25–75	20–30

and low acid electrolytes, and can result in improved nucleation and bottom-void performance on thin copper seeds. Except for the loss of thickness distribution control across highly resistive seeds achieved using lower acid concentration, these electrolytes generally result in good on-wafer performance. Drawbacks of concentrated electrolytes include the formation of excessive amounts of copper sulfate crystals on tool surfaces due to evaporation, and a tendency for anode passivation since the copper sulfate solubility product can be exceeded near the anode surface as cupric ion dissolves and results in a locally high concentration.

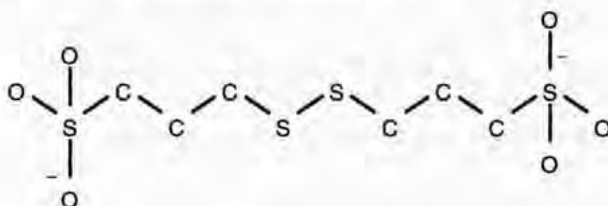
Chloride ions, added as HCl, are present at concentration of 20–100 ppm in all sulfate baths used in damascene applications. Nominal concentrations are usually close to 50 ppm. Although chloride ions are considered to be part of the electrolyte, the primary requirement for their addition to solution is based on interactions with the organic additives required to achieve desired metallurgy and fill performance. By itself, chloride ion adsorbs strongly on the plated Cu surface and provides a charge transfer site which are slightly catalytic or depolarizing in sulfate electrolytes [27]. With the organic polymer suppressor additive present, however, interaction between the adsorbed chloride ion and the suppressor results in formation of a well-adsorbed polymer film which blocks interfacial charge transfer and is therefore highly polarizing [28–31]. Current suppression on the wafer field by this mechanism is essential to achieve bottom-up fill. In addition to the interaction with the suppressor, more recent work [32] has shown that the chloride ion interacts with the accelerator additives in charge transfer reactions during cupric ion reduction. Finally, a uniformly defect-free and smooth plated surface and desired metallurgy are achieved only using chloride ions along with organic additives.

Chloride ions have been reported to serve other functions such as anode depolarization, or to enhance formation of anode films [12], but the importance of these effects is not clear in damascene applications. Bromide ions are known to have effects similar to those of chloride ions in sulfate baths, however, bromide ions are not used with any commercially available additive systems. Iodide ions are insoluble in copper sulfate baths and therefore have little effect.

16.3.2 Organic Additives

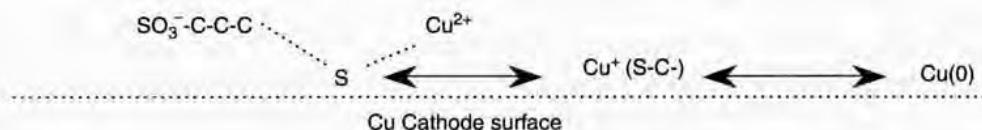
Organic additives are added to copper sulfate plating solutions to achieve the desired metallurgy, defect, thickness distribution, reliability, and fill performance. The terminology used to describe these additives has varied among chemical suppliers and has sometimes been confusing and not related to the specific function or structure of an additive. Here, the additives are referred to as accelerator, suppressor, and leveler species based on the primary function of each of the three additive types.

Accelerators are defined as species which increase the current at a given applied voltage when they are added to a plating bath containing other additives. Accelerators are commonly added to the electrolyte as the sodium or potassium salt of dimercaptopropane sulfonic acid (SPS) at concentrations in the range of 2–20 ppm. The structure of the accelerator molecule, as shown below, results in unique adsorption properties and interactions with the cupric ion reduction process.



In general, sulfide, and thiol like functional groups result in very strong adsorption on copper, gold, and similar metal surfaces [33]. In the case of SPS, the (–C–S–S–C–) portion of the molecule is believed to interact with the copper surface and result in strong adsorption. Normally, strongly adsorbed thiols or sulfides are rapidly incorporated in a plated film, resulting in a short lifetime on the copper surface and high levels of sulfur and carbon in the plated films. With SPS, however, the disulfonic acid functional

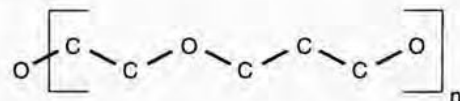
group of the molecule is highly soluble in the plating solution. This characteristic may inhibit incorporation in the plated film, and almost indefinitely extend its lifetime on the plated copper surface. While on the copper surface, SPS and its related monomer, mercaptopropone sulfonic and (MPS), are believed to act as charge transfer sites with a lower energy for the rate limiting step of Cu^{2+} to Cu^+ reduction [34–38].



Based on the adsorption and charge transfer properties, and the observation that catalytic properties can be imparted by pre-dipping in SPS and MPS containing solutions, these molecules are believed to behave as catalysts participating repeatedly in cupric ion reduction reactions [38]. At the low solution concentrations normally used during plating, the catalytic activity of the molecule can increase with time as accumulation on the plated surface continues [39]. The accumulation of this molecule is also the basis for rapid bottom-up filling and the subsequent overplating as will be discussed in the feature fill section.

The accelerator molecules are subject to a variety of oxidation and reduction reactions at the cathode and the anode [40,41] and can form several by-products and complexes with cupric or cuprous ions. Most of these species are unstable and eventually decompose to form propane sulfonic acid or insoluble molecules.

Suppressors are defined as species which adsorb to reduce the current density at a given applied voltage as they are added to a plating bath containing accelerator additives. Suppressors are normally polyethylene glycol (PEG) or polypropylene glycol (PPG) type polymers or co-polymers with the characteristic structure as shown below.



Molecular weights of suppressors generally range from about 1000 up to 10,000 and solution concentrations generally range from 100 to 1000 ppm, much higher than typical accelerator or leveler concentrations. Because of the relatively high suppressor concentration in solution, suppressor adsorption rapidly results in monolayer-like film formation on the copper surface [31,42,43]. Microbalance [44] and current response studies suggest that film formation is complete in about 0.2 s under typical conditions. The film acts to inhibit deposition current at a given applied potential. Several models for current inhibition by the adsorbed film have been suggested including blocking of growth sites, restriction of cupric ion diffusion to the surface, complexation of reacting ions, and formation of a polymer electrolyte films in which ions are solvated [45]. Figure 16.12 shows current as a function of voltage as potential is cycled from the rest potential to -360 mV vs. saturated calomel electrode (SCE) reference electrode and back. As the suppressor concentration is increased from 100 to 1600 ppm, in an electrolyte containing approximately 2 ppm SPS, the current suppression behavior increases, especially at higher currents and during the scan from -360 mV back to the rest potential. This hysteresis between anodic and cathodic potential scans is characteristic of systems containing accelerator and suppressor additives, which are capable of bottom-up filling.

The degree of suppression achieved depends on the molecular weight of the polymer, its structure, and its relative PEG/PPG content. The strongest current suppression is achieved for polymers with higher molecular weights up to about 10,000 [41], and greater PPG content. Interaction with adsorbed chloride ion greatly increases suppressor adsorption strength. Various Raman and FTIR spectroscopy studies have suggested specific chemical interactions between the C–O bonds in the glycol molecules and the adsorbed chloride [46].

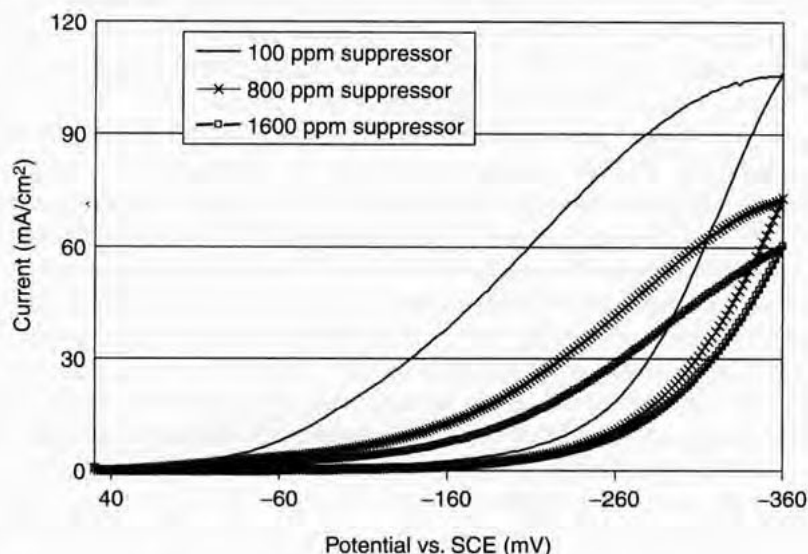


FIGURE 16.12 Polarization curves showing increasing current suppression as polymer suppressor concentration is increases in an electrolyte containing 2 ppm SPS accelerator.

Suppressors also function to reduce the surface tension of the plating solution and improve its ability to wet the copper surface. The surface tension of plating solutions is reduced from about 70 dynes/cm without suppressors added, to 40–60 dynes/cm as suppressor concentration increases. This results in improved wetting behavior as measured by a decrease in the contact angle of the plating solution on the copper seed as shown in Figure 16.13. Low contact angles ensure complete rapid wetting of small features. Assuming reasonably low contact angles, hydrostatic pressure of up to several atmospheres is generated in sub-micron features by capillary action. This results in rapid air dissolution or removal. Suppressor selection for uniform wetting of the copper seed surface is key to avoiding pit defects which can result when air is not fully displaced during initial wafer entry into the plating bath.

Suppressors are reasonably stable in plating solutions in the absence of current flow, but cleave into lower molecular weight fragments as a result of anodic oxidation and other mechanisms during plating.

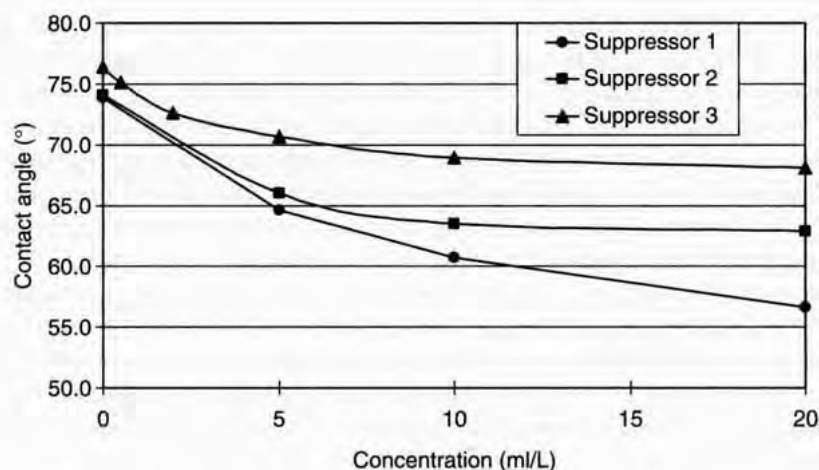


FIGURE 16.13 Contact angle as a function of suppressor concentration for three suppressor molecules.

Usually, the lower molecular weight fragments are less current suppressing than initial suppressor species and become virtually inert at a molecular weight below about 300 [31,41]. Since polypropylene glycol above a molecular weight of about 1200 is not highly soluble in plating baths, it is essential to avoid suppressor structures which can cleave to form this type of fragments.

Levelers are normally known in plating applications as molecules, which adsorb to suppress the rapid plating which may otherwise take place at corners, edges, or other geometric irregularities on a plated surface as a result of field and mass transfer effects [47–49]. Levelers are usually strongly current suppressing nitrogen containing polymers with molecular weights in the range of 1000–15,000. In the acidic plating baths, the nitrogen functional groups may be protonated, leading to a net cationic charge on the molecule. Since the function of levelers is intended to be localized to the rapidly growing surfaces, the concentrations of levelers in solution is kept low, often near or under 1 ppm, and leveler lifetime on the plated surface is ideally low due to either incorporation in the film or decomposition. Under these conditions, leveler surface coverage is diffusion limited, and generally higher at corners, edges, or surface irregularities resulting in slower growth on these surfaces. If the leveler is cationic, migration to highly cathodic edge or corner surfaces may be enhanced, leading to more coverage at sites, which would have a higher current density for normal field effect reasons.

In damascene applications, levelers are added to the plating bath primarily to reduce the rapid copper growth over features which have undergone bottom-up fill, and thus improve the planarity of the film for subsequent CMP processing. In this application, specific chemical interactions in which the leveler neutralizes adsorbed accelerator species present at a high surface concentration over filled features is useful to achieve good deposit planarity. Levelers can also impact fill behavior by either reducing the growth rate of copper at the upper sidewall of a feature to allow better filling, or by adsorbing at the feature's base and slowing otherwise rapid bottom-up filling. Because levelers are often incorporated in the plated film, proper selection is important for film purity, resistivity, and reliability behavior.

16.3.3 Anodes and Anode Films

As was shown in Figure 16.4, a copper metal anode is normally immersed in the plating solution and undergoes oxidation based on the equation $\text{Cu(O)} \rightarrow \text{Cu}^{2+} + 2\text{e}^-$. This maintains both chemical and electrical equilibrium in the plating bath. In some copper plating baths, high purity or “oxygen free” copper anodes are used [50–53]. In acidic sulfate baths, however, use of these anodes was found to result in rapid decomposition of organic additives, as well as formation of fine copper particles which contaminated the plating solution and resulted in defect formation in plated films. Use of anodes containing 400–600 ppm of phosphorous was found to solve these problems, and these “phosphorized copper” anodes are most commonly used for damascene applications [53–56]. Except for phosphorus, anode purity is usually 99.99% or higher. The most common impurities are silver, iron, nickel, arsenic, zinc, and tin each of which is typically present at about one ppm or less. Most anode impurities are not readily deposited on the wafer because their reduction potentials are considerably more cathodic than that of cupric ion (see Figure 16.7), although Ag is readily co-deposited with copper.

The reduction in additive consumption and fine copper particulates seen using phosphorized copper anodes is largely achieved by formation of an adherent low density black film which forms on the anodes during plating. The film is believed to restrict additive mass transfer to the anode interface, and inhibit the loss of partially dissolved grains before they are fully oxidized. Black films generally increase in thickness up to several mm as an anode is initially used. In some applications this change can result in variable additive use during tool start-up, and has been addressed by anode conditioning to prepare a black film before tool use. In addition to the phosphorous content of the anodes, suppressor, and possibly other additive components are required for this film formation. Molecular composition of anode films is not well understood, but analysis shows P, C, Cu, S, O, Cl, and sometimes silver as typical constituents of an amorphous structure.

Anode grain structure and the distribution of phosphorus in the anodes can vary among manufacturers using proprietary fabrication methods. Usually, grain sizes are on the order of 25–

100 μm and phosphorous is present at the grain boundaries. This P distribution may also inhibit fine copper grain loss by reducing electrolytic dissolution along the grain boundaries. Phosphorous has also been associated with inhibition of the undesired anodic reaction $\text{Cu}(\text{O}) \rightarrow \text{Cu}^+ + \text{e}^-$, although this effect is not well documented.

Damascene plating hardware has been designed to reduce the possibility of fine copper or anode film particles from reaching the wafer [57], however, complete anode particle elimination can be achieved by using inert anodes such as platinum coated titanium. When platinized titanium or similar anodes are substituted for copper in a standard bath, the anode reaction becomes $2\text{H}_2\text{O} \rightarrow \text{O}_2 + 4\text{H}^+ + 4\text{e}^-$. Difficulties with this approach include the generation of large volumes of oxygen which can form undesired bubbles, rapid oxidation of additives on the platinum anodes, and a decrease of copper concentration in the plating bath during plating. Copper concentration in this type of plating system can be maintained by cupric oxide addition [58,59]. An alternative inert anode approach in which ferric and ferrous iron salts are added to the copper plating bath has also been proposed [60]. In this system, the reaction $\text{Fe}^{2+} \rightarrow \text{Fe}^{3+}$ takes place at the inert anode to eliminate oxygen evolution, while cupric ion is replenished and Fe^{2+} is replaced in a separated reaction of Fe^{3+} with copper metal. Iron is not co-deposited with copper as a result of its more negative reduction potential [60].

16.4 Damascene Film Deposition

16.4.1 Feature Fill and Leveling Capability and Mechanism

16.4.1.1 Fill Mechanism

Void-free filling is the most basic requirement of copper electroplating for damascene applications. The ability to fill high aspect ratio features using copper electroplating is based on achieving significantly more rapid deposition kinetics near the base of a deep feature compared to the kinetics on the field of the wafer. This allows filling from the base of the feature before conformal plating on the top corners of the features joins together to leave a void. Such capability is usually called bottom-up fill or superfill in the literature, and is achieved by non-equilibrium distribution of current accelerating and suppressing additives between the feature base and the field [13,20,61].

It is useful to consider the current–potential behavior of several plating solutions to understand the capability for bottom-up fill in electroplating. Figure 16.14a shows polarization behavior at a rotating disk electrode of electrolyte containing cupric ions, sulfuric acid, and chloride. Current is measured as potential is first swept negatively from the equilibrium value of +50 mV vs. SCE to –280 mV vs. SCE, and then cycled back to the equilibrium potential. Results are shown for three electrode rotation rates corresponding to different rates of mass transfer. In this simple system, the current increases in an approximately exponential manner until mass transfer begins to limit overall current flow. At 50 rpm limitation of cupric ion mass transfer reduces the overall current magnitude over much of the practical current density range (10–50 mA/cm^2), while at 1000 rpm mass transfer effects on current flow are minimal until current densities above 100 mA/cm^2 are reached. It should be noted that the current at any given potential during the cathodic potential sweep is nearly equal to the current at the same potential during the subsequent sweep toward anodic potentials. This lack of hysteresis between the potential cycles implies that a single current corresponds to each applied voltage regardless of the potential sweep history, and suggests rapidly equilibrating surface morphology and growth characteristics when no organic additives are present. Inability of a plated surface in a given bath to exhibit more than one current at a given applied voltage makes bottom-up filling based on surface kinetic differences impossible in that bath since applied voltages will never be higher near a feature base than on adjacent field surfaces.

Polarization curves using the same electrolyte along with an early generation organic additive formulation, containing accelerator, leveler, and suppressor species are shown in Figure 16.14b. Two major differences are noted in the polarization behavior following additive addition. First, currents are reduced at a given voltage. This behavior reflects changes at the interface caused by the additives including blockage of growth sites, formation of interfacial complexes, topography changes, and film

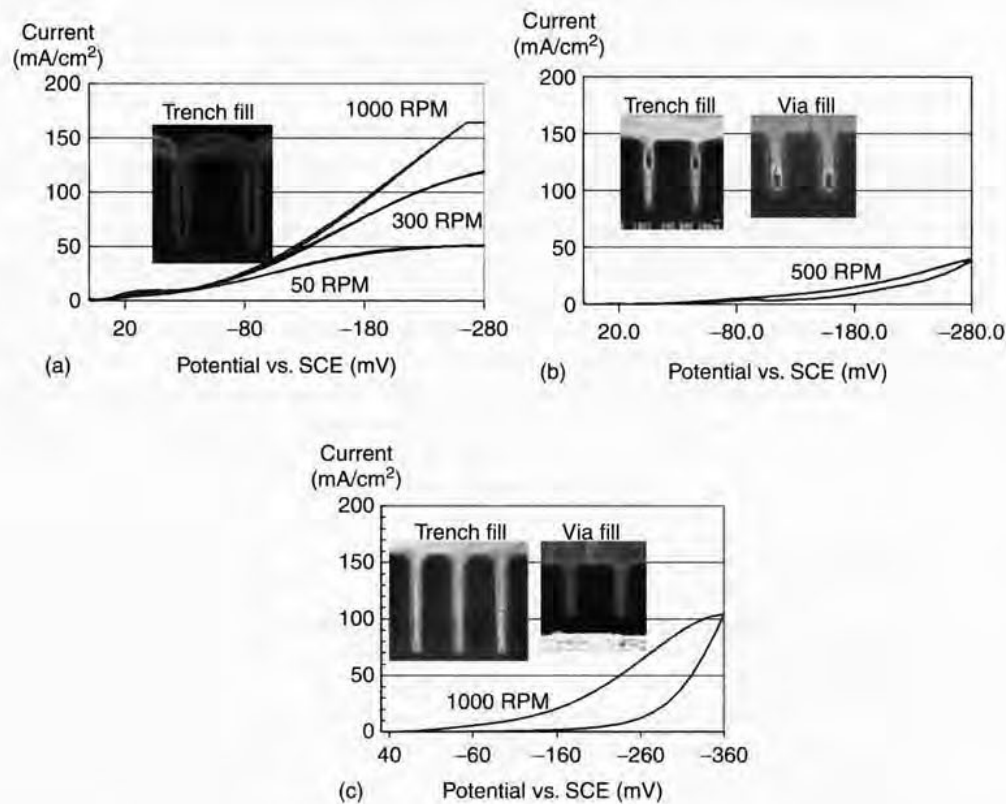


FIGURE 16.14 Polarization and fill results with and without additives. (a) Electrolyte with no additives present. (b) Electrolyte with early damascene additive package. (c) Electrolyte with suppressor and accelerator additives selected for filling performance.

formation, which reduces metal ion mass transfer to the interface. Second, there is a hysteresis behavior in the current flow between the cathodic and anodic potential sweeps such that currents at a given voltage during the initial cathodic sweep are lower than those observed during the subsequent anodic sweep.

In Figure 16.14c, polarization curves measured for a two component (accelerator—suppressor) additive containing bath formulated to achieve very rapid bottom-up fill are shown. This bath exhibits stronger current suppression and more hysteresis between current flows during the cathodic and anodic sweeps. The degree of hysteresis reflects the ability of a plating bath to support both high and low currents at a given applied voltage, and thus can suggest capability of a bath to provide bottom-up fill [19,61–65]. During the initial cathodic potential sweep, the currents measured using this chemistry are also significantly lower than those shown in Figure 16.14a and b. This polarization behavior difference results in higher voltages being applied in order to achieve a given initial current flow. Higher applied voltages are well known to be more effective in achieving uniform nucleation on variable surfaces and to prevent corrosion of metal. As a result, these more polarizing electrolytes are considered useful in achieving growth on discontinuous seed layers. Highly suppressed currents on the wafer field can allow increased growth rate differentiation between the field and the feature base as long as the feature base is not also strongly polarized.

Trench fill and via fill results obtained by plating in the additive free, early generation, and bottom-up fill baths are also shown in Figure 16.14a–c. The trench fill results provide a good means to evaluate the bottom-up fill acceleration capability of a plating chemistry on a well seeded surface. Without additives present, the copper deposition rate on all surfaces within the feature is approximately equal. This leads to

conformal growth and a large center void extending much of the length of the 5:1 aspect ratio trench. This result is observed over a current density range of approximately 5–50 mA/cm². At current densities above approximately 50 mA/cm², depletion of cupric ion within the feature further limits growth within the feature and the void volume increases further. Fill performance in vias with discontinuous or very thin and oxidized PVD copper seed provides a good means to evaluate the nucleation capability of a plating bath. In the relatively non-polarized bath with no additives, a large void at the base of a via (bottom void) as shown in Figure 16.14a is observed. This reflects an initial dissolution rate or Ostwald ripening of the thinner seed, which exceeded the initial plating rate.

When early generation additives are added to the electrolyte, complete filling of 5:1 AR trenches is achieved, thus demonstrating the existence of bottom-up fill. A center void is, however, observed following plating of 6:1 or higher aspect ratio, 0.17 μm trenches as shown in Figure 16.14b. The bottom void performance is improved somewhat on a discontinuous seed as compared to results for the bath with no additives, but a void is still observed if the seed coverage is poor.

Using strongly current suppressing additives, which result in increased current–voltage hysteresis, full fill of 9:1 AR trenches is achieved, as shown in Figure 16.14c. This rapid bottom-up fill capability has been incorporated in all commercially available additive systems now in use for IC copper circuitization. Via fill is also complete, indicating the additional applied voltages required to drive a given current early in the process which were sufficient to improve nucleation and growth on the thinner areas of the seed to a rate which exceeded seed dissolution. While plating in highly suppressed plating baths is useful to add margin to the filling processes, it is generally necessary to optimize seed processes to yield continuous films to guarantee consistent void free filling and optimum reliability.

Based on the hysteresis behavior in mixed additive systems, and the current accelerating and suppressing characteristics of the additives alone, it is possible to generate bottom-up fill based on two mechanisms. According to the first mechanism, which can be descriptively named “field suppression”, the additives quickly adsorb on the field of the wafer to form a current suppressing film. Within the features, however, current suppressing molecules fail to form a suppressing film due to diffusion limitations or steric hindrance based on similarity of the suppressor and feature sizes [4,66–69]. Current–potential characteristics leading to fill based on this mechanism are illustrated in Figure 16.15. Fill performance based on this mechanism can be estimated based on electrochemical studies comparing I–E behavior on an electrode using a complete additive system to simulate deposition on the field, with I–E behavior without additives present to simulate deposition at the feature base. A fill acceleration ratio

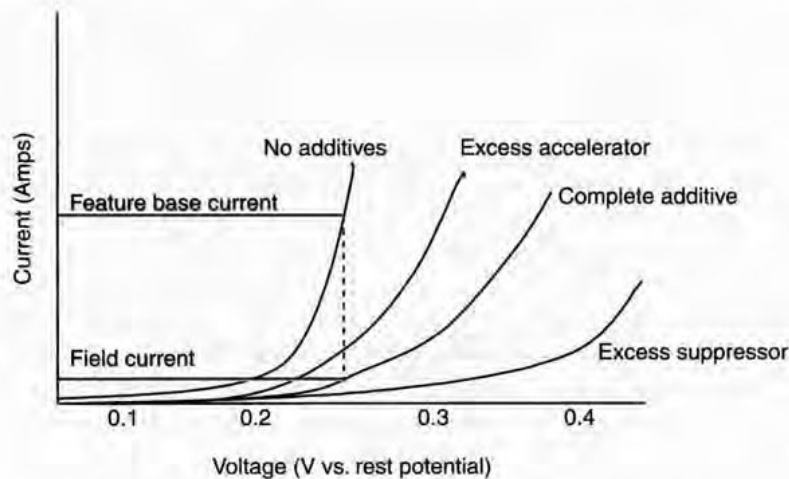


FIGURE 16.15 Polarization characteristics of wafer field and feature base which lead to bottom-up fill based on lack of suppressor diffusion into feature.

TABLE 16.2 Polymer Size and Diffusion Coefficient vs Molecular Weight

Polymer MW	Spherical Conformation Diameter (nm)	Diffusion Coefficient (cm ² /s)
100	0.62	0.7×10^{-5}
1,000	1.32	0.25×10^{-5}
10,000	2.85	0.11×10^{-5}
1,00,000	6.2	0.05×10^{-5}
10,00,000	13.2	0.025×10^{-5}

at a given applied voltage can be calculated by comparing the current for the no additive case to the current for the case with all additives present. Ratios as high as 30:1 are often calculated based on comparing rotating disk electrode data for complete additive systems with the data without additives present. In a practical case, it is unlikely that suppression by additives at the feature base will be zero since diffusion distances and times are on the micron per millisecond scale and polymer additives, normally of molecular weight under 10,000, are smaller than typical feature sizes as shown in Table 16.2. A variation of this mechanism involves limitation of chloride, rather than polymer, mass transfer into small features. Since adsorbed Cl is required for strong polymer based current suppression using typical PEG suppressors, high currents within features could result from lack of adsorbed chloride [70].

According to the second mechanism, which can be descriptively named “accelerator accumulation”, additives initially adsorb with reasonable uniformity on the copper seed surfaces both on the field and within the features on the wafer [19,20]. Deposition begins conformally on all surfaces according to this mechanism. As conformal growth continues and features are partially filled, the surface area within small features decreases, especially at the feature base corners. This decrease in surface area is believed to concentrate the strongly adsorbed accelerator additives, leading to displacement of the polymer suppressor and increased current within the features. Current-potential behavior leading to this fill mechanism is illustrated in Figure 16.16. Like Figure 16.15, the field I-E behavior can be approximated by measuring the full additive system using a rotating disk electrode. In this case, however, the current near the feature base is estimated by measuring current-potential behavior at an electrode immersed in an electrolyte containing accelerator only. Current acceleration ratios of about 10:1 are typically obtained

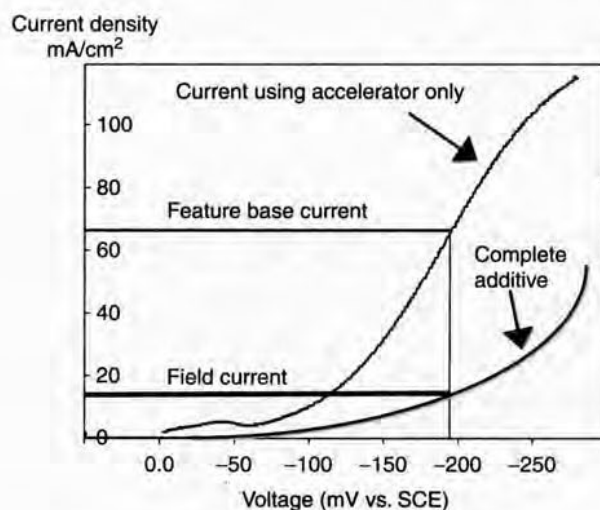


FIGURE 16.16 Polarization characteristics of wafer field and feature base which lead to bottom-up fill based on a depolarization of suppression within features due to accelerator accumulation.

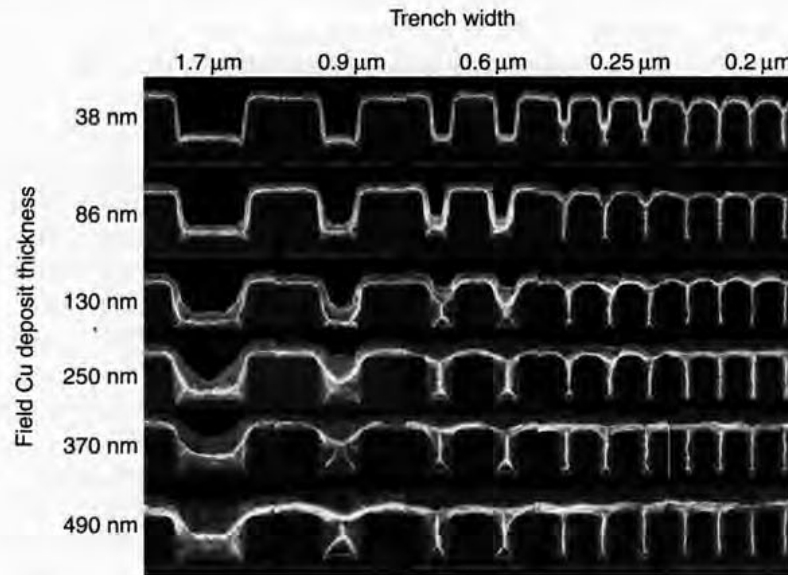


FIGURE 16.17 Fill evolution in trenches as a function of trench width and copper thickness deposited on the wafer field.

over a range of applied voltages comparing the simulated field current to the simulated feature base current. This is in good agreement with measured fill acceleration rates obtained by comparing growth rate within a feature adjacent field growth rates. Measurement of hysteresis during potential cycling at electrodes can also be used to approximate current density or applied voltage ranges over which optimum bottom up fill can be generated [64].

16.4.2 Fill Evolution Behavior

Figure 16.17 shows fill evolution in 1.2 μm deep trenches of 0.2, 0.25, 0.6, 0.9, and 1.7 μm widths following electrodeposition of 38, 86, 130, 250, 370, and 490 nm of copper on the wafer field at a nominal current density of approximately 10 mA/cm^2 .

After electrodeposition of 38 nm of Cu, the total Cu thickness on the field is approximately 188 nm when the thickness of the 150 nm seed layer is considered. At this point in the filling sequence, the largest features (0.6–1.7 μm) show conformal growth with a 80 nm layer of copper on all surfaces within the trenches. In the 0.25 μm trenches, the sidewalls in the upper portion of the trench show conformal growth, however, a distinct surface of copper growing parallel to the base of the trench has formed about 0.6 μm above the base of the trench. This surface is characteristic of accelerated bottom-up growth. Once formed, this surface moves rapidly up the feature, ultimately yielding complete fill. This filling process has nearly been completed in the 0.2 μm trenches.

After electrodeposition of 86 nm, fill acceleration in the corners of 0.9 and 1.7 μm trenches has become evident. The 0.6 μm trenches now show a flat growth surface which has progressed to about 0.5 μm from the trench base. Approximately 600 nm of vertical fill has been achieved in the 0.25 μm trenches during the 48 nm of deposition which takes place between the 38 and 86 nm nominal field deposition. This is a $12.5\times$ acceleration relative to the field thickness increase of 48 nm, and suggests a current density of approximately 125 mA/cm^2 on the localized bottom-up growth surface. The 0.20 μm trench size shows growth which has proceeded above the field by approximately 100 nm, forming the characteristic overplating bump which can follow bottom-up filling.

Between 86 and 130 nm nominal deposition, the vertical growth in the 0.6 μm trench is approximately 600 nm. This is a $13\times$ acceleration relative to the nominal growth rate, similar to that achieved in the 0.25 μm features. After 130 nm deposition, more pronounced corner growth is also noted in the 0.9 and 1.7 μm trenches, and fill of the 0.6 μm trench is complete.

After 250 nm deposition, further corner growth is noted in the 1.7 μm trenches, and the 0.9 μm trenches have undergone the transition from accelerated corner growth to rapid bottom-up fill to form the characteristic flat growth surface. Longer deposition times result in similar transitions to rapid bottom-up growth fronts in features as large as approximately 3.0 μm in a 1 μm deep dielectric. The exact delay time, or nominal deposit thickness, required for the transition to accelerated bottom-up fill varies with nominal current density for all feature sizes. Very low current densities never result in transition to bottom-up fill, and currents above an optimum value generally increase the nominal thickness required for the transition.

The feature size dependence of initiation of bottom-up fill acceleration and the observation of initially accelerated corner growth are consistent with the requirement of a threshold surface area change within the feature prior to fill acceleration. During the initial conformal deposition, localized concentration of the strongly adsorbing accelerating species takes place. Accumulation of accelerator is initially most pronounced in the corners at the base of trenches where surface area change is also initially significant. In features between 0.3 and 0.9 μm in width, the total surface area within the trenches has decreased by 40%–50% at the point when rapid growth acceleration begins. The feature size dependence of the timing of bottom-up filling is difficult to explain solely in terms of a filling mechanism based on diffusion limited suppression.

16.4.3 Fill Response to Plating Chemistry

Although the electrolyte and additive formulations used for IC filling applications vary, several trends in the response of fill to additive chemistry have been commonly observed [19]. In general, all filling baths contain cupric ion, sulfuric acid, chloride ion, accelerator, and suppressor. Leveler is not required for fill, but may be present.

Strongly accelerated fill has not been achieved in electrolytes containing suppressing polymers alone or with chloride ion when no accelerator is present in solution. Growth in these baths appears to be largely conformal except at very low Cl ion concentrations where some evidence of filling has been reported [70]. On the other hand, bottom-up fill is most pronounced for systems, which typically contain 50–200 ppm suppressor concentrations along with suitable accelerator additives and chloride ion concentrations. It is clear that suppressors are required to reduce the current on the field of the wafer in order to achieve bottom-up fill. Optimum filling is observed when the concentration, diffusion behavior, and adsorption strength of the suppressor are selected so that suppression on the field is maximized, while suppressor adsorption within features is not strong enough to prevent localized accelerated growth. Very strong suppressors and high concentrations of most suppressors will prevent bottom-up filling by uniformly suppressing growth both within the features and on the field, however, certain suppressors can yield good fill performance at concentrations as high as 2000 ppm.

As the chloride ion concentration is increased from zero, fill acceleration increases from near zero to a maximum value and then decreases as the chloride concentration is further increased. Typically, optimum fill is observed when Cl concentrations are in the range of 30–50 ppm and fill becomes more conformal as Cl concentrations approach 100 ppm. Chloride concentrations sufficient to enhance polymer suppressor adsorption on the field are required for fill. Excessive Cl can diminish fill, possibly by resulting in excessive suppression within features. The maximum fill rate is usually achieved when the Cl concentration is reduced to a point where polymer suppression remains adequate on the field, but becomes limited at the feature base due to a Cl concentration gradient within the feature.

As the accelerator concentration is increased from zero to the 5–25 ppm range, bottom-up fill increases from near zero to a maximum rate at typical suppressor concentrations. Fill becomes conformal as accelerator concentration is further increased. No fill is observed using an accelerator if a suppressor is not present. An accelerator additive is required to achieve the rapid growth within features which takes place while the field remains suppressed. Too much accelerator, however, results in a loss of growth rate difference between the field and the feature due to a lack of field suppression. The recognition that accelerator additives which preferentially adsorb (relative to suppressors) on copper surfaces could be concentrated within small growing features yielding faster local deposition kinetics was key in explaining the ability to achieve very rapid bottom-up filling.

For a given additive system, too low a copper concentration diminishes the bottom-up fill capability in high aspect ratio features simply due to depletion of cupric ion within the features. Successful filling applications have used as little as 17.5 g/L cupric ion. More commonly, concentrations in the range of 40–50 g/L are employed for optimal fill performance.

Sulfuric acid is not known to participate in filling, however, fill performance does vary with acid concentration. At low sulfuric acid concentrations, the mercaptosulfonic acid accelerator molecule becomes ionized in solution and fails to adsorb strongly on the copper surface. As a result, higher accelerator concentrations are required for bottom-up fill when the acid concentration is decreased to the 5–30 g/L range and little filling can be achieved above a pH of about 2.0. The acid concentration may also result in changes in fill capability due to changes in the suppressor adsorption behavior, however, no general trend has been reported.

16.4.4 Leveling after Fill

Accelerated growth in electrolytes containing a two component (accelerator/suppressor) additive system continues over a damascene feature following bottom-up fill. This growth can result in over a micron of excess copper thickness above features which underwent bottom-up fill, compared to the adjacent field copper thickness. This growth is most pronounced over large arrays of closely spaced lines, which act to cumulatively concentrate accelerator species on the wafer surface following fill. Figure 16.18 illustrates the growth behavior of copper during and after bottom-up fill with and without leveler added to the plating bath. Ideally, the addition of a leveler component serves to suppress current on the rapidly growing fill surface once it protrudes above the field, without impacting the growth rate of the copper

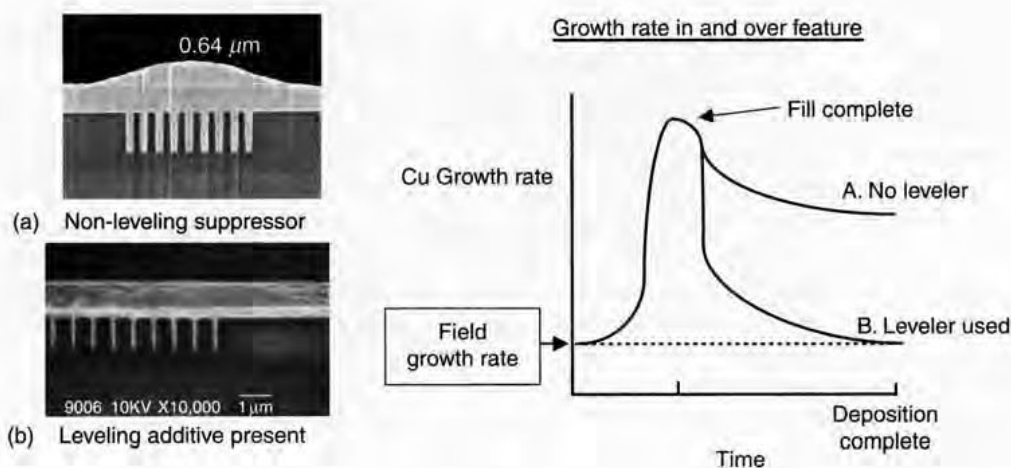


FIGURE 16.18 Copper growth rate in and above a feature during bottom-up fill with and without a leveler added to the plating solution.

within the feature. In practice, the addition of excessive leveler often results in a loss of bottom-up fill, probably due to diffusion of leveler into the filling feature. Development of levelers with diffusion and adsorption characteristics which reduce impact to growth within features remains an area of strong interest. Using modern levelers in the 2–20 ppm concentration range, the copper thickness over dense features following fill is typically less than 1000 Å thicker than the thickness of the adjacent field. The mechanism of overplating reduction by a leveler has not been well studied. However, a specific interaction of the leveler to neutralize adsorbed accelerating species is suggested by its activity at very low solution concentrations and by the relatively small impact of same levelers on the polarization behavior of additive containing solutions.

16.4.5 Fill Behavior in Alternate Electrolytes

Fill performance has been evaluated in non-sulfate based electrolytes including propanesulfonic acid–copper propanesulfonate [18] using additives which yield bottom-up fill in sulfate electrolytes. Little change from the behavior in sulfate electrolytes was noted either in the optimized bottom-up fill rate or the ability to deposit on thin or discontinuous seed. The similarity in via bottom void formation observed using organic and inorganic anion based electrolytes, despite the expected wetting differences, suggests that the wetting limitations of the electrolyte do not contribute strongly to poor electrodeposition behavior on a discontinuous seed.

Rapid bottom-up fill has not been reported using alkaline electrolytes such as pyrophosphate or cyanide in which the cupric ion must be strongly complexed. In these electrolytes the deposition kinetics are limited by complex dissociation, which makes differences in kinetics due to additive adsorption less significant.

16.4.6 Current Waveform and Mass Transfer Impact on Filling

Damascene features are usually filled using direct current (DC) controlled processes in which the field current density is in the range of 3–15 mA/cm² (0.07–0.36 μm/min). Lower currents have been observed to result in both bottom voids due to seed dissolution and poor bottom-up acceleration, possibly because the times for filling are so long that additive adsorption on the field and within the feature equilibrates to the same levels. A higher field current density than 15 mA/cm² during filling necessitates an extremely high current density within the features in order to maintain a high fill efficiency. This results in copper depletion in the feature, and can cause fill to take place over a time scale shorter than required for desired additive adsorption.

At the beginning of the process, current or voltage can be applied to the wafer immediately as it enters the plating solution, or after several seconds of immersion in the plating solution. To prevent dissolution of the seed, in production processes wafers usually enter the plating bath with a current or voltage applied. However, bottom-up fill rate on sufficiently thick seeds is usually not strongly effected by long immersion times before plating begins.

Pulse reverse plating has been applied successfully to improve fill performance of certain additive systems [69,71]. Such plating methods are believed to accelerate dissolution of copper at the opening of high aspect ratio features or to cause the adsorption behavior of the additives to vary in a way that enhances filling. Fill performance using pulse plating has been found to respond in generally the same way as DC plating to process variables and additive concentration changes, suggesting that the basic fill mechanisms remain the same.

The rate of mass transfer of electrolyte to the wafer surface can influence the rate at which additives adsorb. Fill performance has generally been found to vary only slightly within the flow and wafer rotation conditions used for damascene applications. This suggests that the surface behavior of the accelerator and suppressor additives is generally more important than their rate of mass transfer to the surface. Mass transfer rates can be modulated to control leveler adsorption during plating, and higher mass transfer in leveler containing baths usually reduces the amount of overplating.

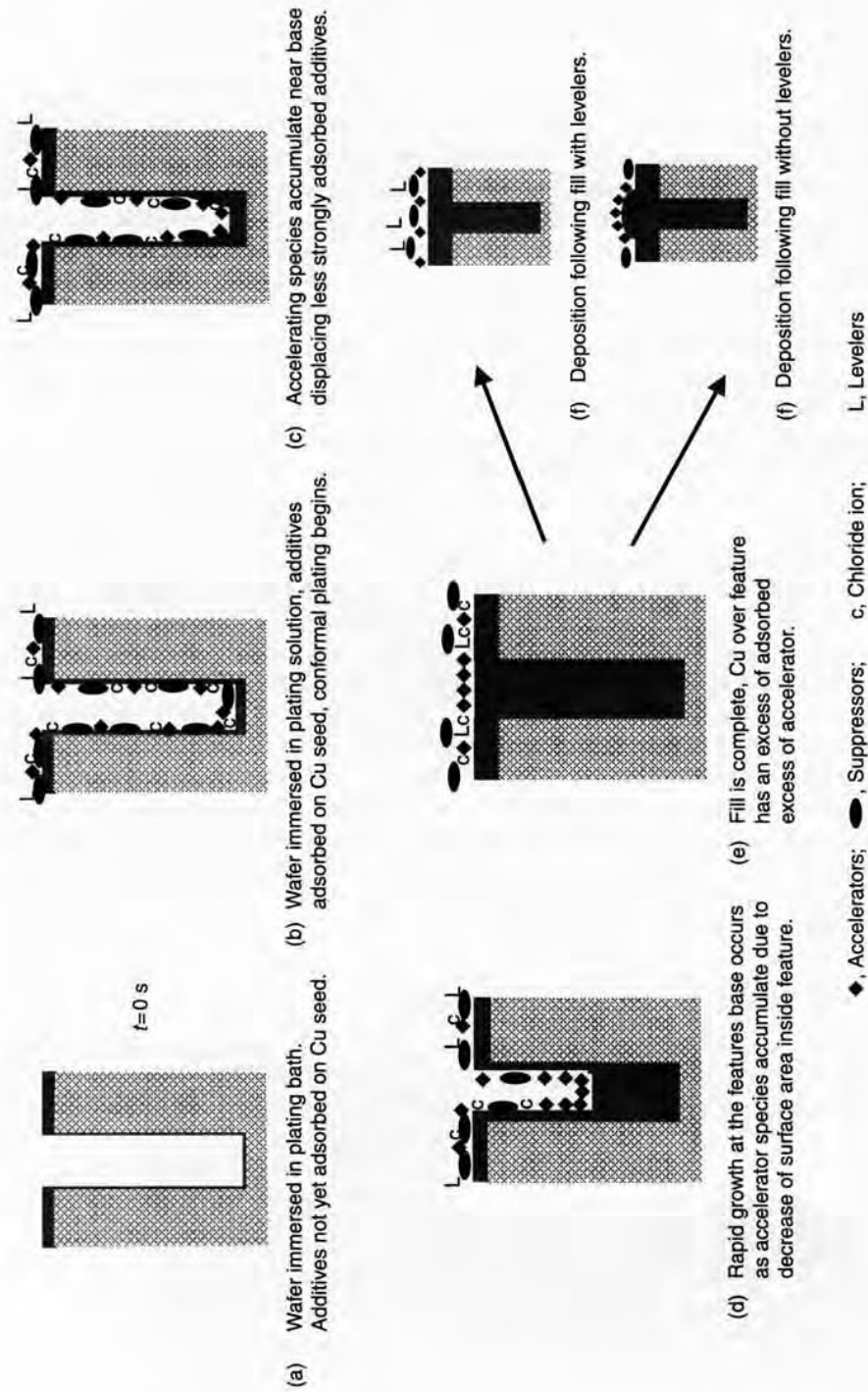


FIGURE 16.19 Fill evolution during bottom-up fill based on accelerator accumulation at the feature base. ♦, Accelerators; ●, Suppressors; c, Chloride ion; L, Levelers.

16.4.7 Summary of Additive Behavior during Filling

Additive adsorption behavior during bottom-up filling can be described based on the dependence of fill evolution on feature size, fill rate and electrochemical suppression behavior as a function of additive concentrations, and current and mass transfer effects on filling. This additive adsorption behavior during filling is illustrated in Figure 16.19a–f.

When a wafer is first immersed in the plating solution, a concentration gradient of suppressing or accelerating species may exist between a feature base and the field. This can happen when the quantity of additive species required to form an adsorbed layer on the surface within the feature, exceeds the amount of additive contained in the solution volume within the feature, or when the suppressing species are large compared to the feature width. This effect could account for less suppression at the via base by slowly diffusing polymer species when relatively low suppressing polymer concentrations (< 100 mg/L) are present in solution. Although diffusion limitations at the feature base effect may enhance fill in some cases, the lack of a strong fill rate dependence on wafer immersion time prior to application of current, as well as the relatively long times of plating required for bottom-up fill to begin in large features suggest that this is not critical. Assuming this, by the time significant current flow begins, the adsorption of chloride ion, suppressor, and accelerator species will take place across all field and within-feature surfaces as shown in Figure 16.19b. This should result in similar currents on all surfaces.

After a period of time which depends on current density, feature size, and chemical concentrations, the initial conformal growth leads to a decrease in surface area within features, especially at the bottom corners. This phenomena causes accumulation of the accelerator additives or their accelerating by-products and displacement of suppressor, and results in the initially fast growth observed in corners at the start of the filling process as shown in Figure 16.19c. At this corner surface, the local current density is believed to undergo transition from the lower current to the higher current observed during a cyclic potential scan exhibiting strong hysteresis. Excessively strongly adsorbing suppressor molecules, which prevent bottom-up fill, apparently cannot be displaced by accumulating accelerator and can inhibit this transition.

Once bottom-up fill begins, a growth front moves rapidly upward within features and continues to accumulate accelerating additives as shown in Figure 16.19d. The growth rate within the feature during this stage of filling reaches a maximum and continues until the feature is filled as shown in Figure 16.19e. In the absence of levelers, accelerators remain concentrated over features even after filling and rapid growth diminishes slowly so that overplating above features becomes significant as shown in Figure 16.19f. Addition of levelers at proper concentrations neutralizes the effect of the accelerator as fill within the feature approaches planarity with the field so that overplating is largely eliminated.

16.4.8 Deposit Planarity and Surface Roughness

While overplating above dense features can increase topography variation across a die, the overall planarity after copper plating is also strongly influenced by dielectric etch depth as illustrated in Figure 16.20. Although the copper electroplating process is effective in filling features with aspect ratio's

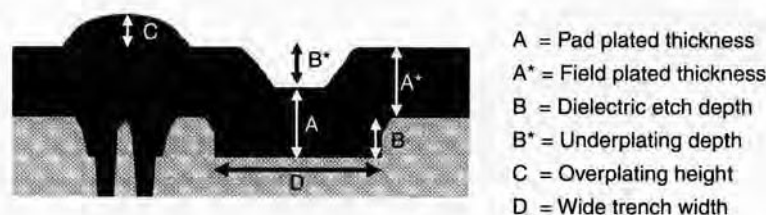


FIGURE 16.20 Overall topography after copper plating of damascene circuitry patterns with super-filled small features as well as large conformally plated pads.

as low as about 1:5 at an accelerated rate, large pads plate at a deposition rate nearly equal to the field deposition rate. As a result, the amount of copper deposited for a given metal layer must at least equal the dielectric etch depth, and the Z position of the copper over large pads after plating is below that of the field by approximately the dielectric etch depth. As a result of this behavior, and the need for a planar copper topography after CMP, plating thickness in the range of 1.3–2.0 times the dielectric etch depth of a given metal level is typical in production.

Plating processes, which deposit little copper on the field while fully filling large pads have been described [72], and continue to be of interest as a result of the associated reduction in CMP cost. These processes involve a combination of electrodeposition and mechanical contact with the wafer surface during electrodeposition rather than simple process or plating chemistry changes. To date, such processes have not been widely implemented.

Plated copper used for IC application usually has a bright reflective appearance with a reflectivity of at least 130% that of bare Si using 460 nm light. The surface roughness of the copper, as measured by Atomic force microscopy (AFM) is usually in the range of 4–8 nm root mean square (RMS). Roughness variability has not been associated with yield or electrical properties of the copper, but is often controlled in order to maintain a reproducible ability to monitor defects using visible light based tools. As feature dimensions decrease into the 45 nm range it becomes increasingly important that roughness evolution remains small compared to the internal dimensions of lines in order to avoid intermittent voids corresponding to rough deposition protruding from the upper sidewall of features during bottom-up filling.

16.4.9 Thickness Distribution

The goal for most damascene copper deposition processes is to form a film of uniform thickness across the wafer. Specifications in the range of 1.5%–2% one sigma thickness distribution, determined from at least 49 point resistivity or laser-acoustic measurements on blanket wafers, are usually met or exceeded in production. Thickness measurement on damascene pattern wafers is complicated by the varying contribution of copper within features to the overall thickness measured using typical methods. In some applications, plated copper is specified to be edge thick or edge thin to match a specific CMP capability. In order to control the thickness distribution, damascene plating equipment has been optimized to control the terminal effect, field, and flow influences on deposition kinetics at a given location on the wafer.

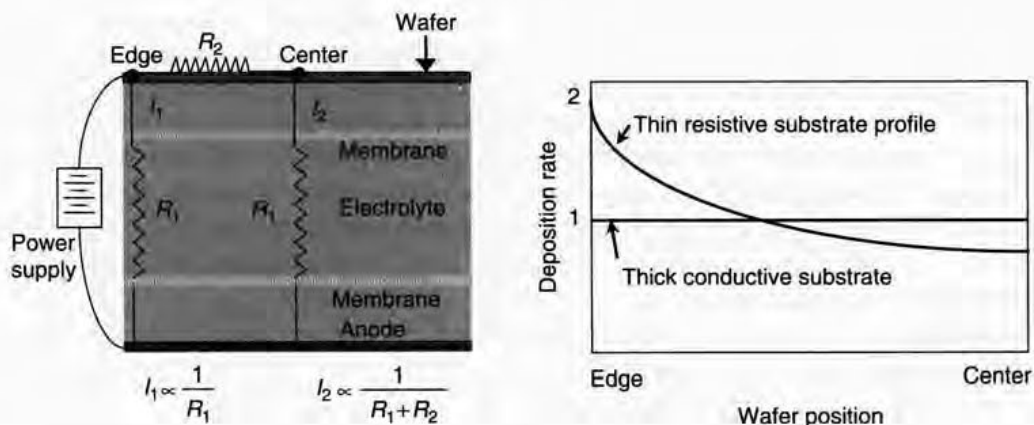


FIGURE 16.21 Circuit diagram of plating cell illustrating terminal effect impact on current density between wafer center and edge.

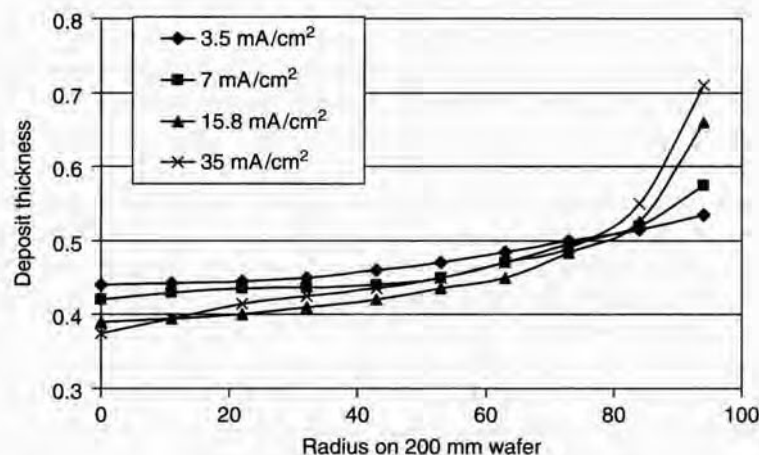


FIGURE 16.22 Plated thickness as a function of radial position for deposition on 100 Å thick ($4 \Omega/\text{sq}$) copper seed as a function of plating current density.

16.4.10 Terminal Effect

When copper deposition was introduced in the mid-1990s seed layer thicknesses were generally in the range of 1500–2000 Å, the wafer size was 200 mm, and plating was not usually carried out at high current densities. Under these conditions, resistive voltage drops across the seed layer were too small to influence plating rates. As illustrated in Figure 16.21, when seed layers become thin, the resistive voltage drop through the seed layer from contact points at the edge of the wafer to the wafer center can become significant. This results in a higher interfacial potential at the wafer edge. From polarization curve data (see Figure 16.11), it is seen that interfacial potential differences between the wafer center and edge as small as 10–20 mV begin to impact local current density and deposits will become center thin. Thickness distributions showing the impact of the resistance drop across the wafer while plating on 100 Å thick seed at several current densities are shown in Figure 16.22. A somewhat lower impact of this terminal effect is observed at lower currents since the voltage drops across the seed layers are less under these conditions.

In a plating system, the overall resistance between all points on the wafer and the anode surface should be uniform in order to achieve uniform current densities. Based on this, a number of hardware and process approaches have been used to diminish the terminal effect in semiconductor processing equipment.

First, increasing the resistivity of the plating solution by lowering the acid content has a pronounced impact on the thickness distribution on resistive seeds [17] as discussed earlier. Typical high acid bath conductivity of $0.5 (\Omega\text{-cm})^{-1}$ results in a cell impedance of about 0.1Ω and overall cell voltages on the order of 1–4 V using standard plating cell geometries. When bath conductivity is decreased to the range of $0.05 (\Omega\text{-cm})^{-1}$ by lowering the acid concentration, the relative change in potential between the wafer center and wafer edge compared to the overall potential drop through the plating cell becomes small and the thickness distribution is improved. The plating bath can be considered to behave like a large swamping resistor in an electrical circuit.

A second method, relying on the principle of increased cell resistance involves placing continuous highly resistive membranes or insulating surfaces in the plating solution adjacent to the wafer. Often, an effective resistivity of $100\times$ the bath resistance can be achieved by using suitable materials. This highly resistive layer dominates overall plating cell impedance behavior and effectively forces an equal current density through all portions of the layer. If the layer is sufficiently close to the wafer there is little possibility for current to redistribute between the wafer center and edge and the thickness distribution

across the wafer is improved. The drawback of this method is the 30–60 V which may be required to drive current through a resistive layer, several times higher than the voltages normally used during plating.

A third method of modification of thickness distribution is the use segmented or multiple anodes [73]. Using this method, one anode is normally positioned below the center portion of the wafer and one or more additional electrically isolated anodes are positioned concentrically around the central anode. Current applied to the anodes is then controlled individually. To create a uniform current density on a thin seed, a higher voltage is applied to the anode nearer the wafer center compared to other anodes. Because there is a lower resistance through solution between the center anode and the wafer center compared to the wafer edge, current will flow preferentially to the wafer center. The drawback of this method is the complexity of power supply and anode cell design and maintenance.

A fourth method of across wafer thickness distribution control is the placement of insulating shielding in the plating bath near the wafer edge to restrict current flow to this portion of the wafer. This method can be highly effective in generating uniform films when seed thickness and plating thickness are constant. However, a shield configuration, which yields uniform current density across the wafer on thin seed, will result in too much deposition near the wafer center on partially plated films or thicker seed. As a solution to this problem, the use of dynamic and asymmetric shields has been suggested [74]. Such methods have the drawback of additional moving parts near the wafer and increased mechanical complexity.

A fifth method involves additional cathodes or “thieves”, which are placed near the wafer edge. These surfaces, which can be controlled either by the same power supply as the wafer or with an additional power supply, help divert current from the wafer edge. Generally, this method is effective over short distances compared to the wafer diameter and is more effective in controlling distribution near the wafer edge than across the full wafer.

Finally, it was noted earlier [14] that plating bath compositions with very slow deposition kinetics effectively introduce a large and uniform electrical resistance at the wafer interface. This resistance acts to redistribute current as described for resistive membranes placed near the wafer. To achieve interfacial resistance increases, sufficient to counter the terminal effect, the copper concentration in sulfate baths must be sharply lowered or electrolyte compositions, in which the cupric ions are complexed, must be used. To date, these bath compositions have not been shown to have sufficient superfill performance for use early in the plating process.

16.4.11 Field Effects

An ideal plating cell configuration, which avoids field effects during copper deposition on wafers, is a cylinder, which tightly surrounds an anode and a wafer of equal size which are placed at opposite ends of the cylinder. In this configuration, all field lines will be parallel and of equal density across the plating solution and uniform deposition will result in the absence of terminal effects or flow differences. In actual semiconductor equipment it is necessary to have some open space in a plating cell beyond that enclosed by a wafer diameter cylinder. This results in additional field lines or current pathways through the solution and a tendency for a higher current density near the wafer edge. Plating equipment is generally kept as close to an ideal cylinder design as possible. Insulating surfaces (shields) are often placed in the solution around the wafer perimeter to correct for edge effects resulting from non-ideal cell design by redistributing current toward the wafer center.

16.4.12 Mass Transfer

Most wafer plating systems achieve relatively uniform solution flow across the wafer surface using a combination of wafer rotation and pumped electrolyte flow directed toward the wafer at a uniform rate through a manifold or membrane. To the degree to which uniform flow cannot be achieved, mass transfer rates of cupric ion and additive species to the wafer surface vary with wafer position, and plating rates can exhibit corresponding variability (see Equation 16.6). The direction and degree of rate variation,

TABLE 16.3 Properties of Electroplated Copper

Property	Typical Value
Elongation to failure	10–25%
Stress	± 50 MPa
Hardness	110–130 Knoop at 1 g load; 1.5–2.8 GPa
Tensile strength	50 KPSI
Modules of Elasticity	100–150 GPa
Reflectivity (vs. Si)	130% @ 460 nm
Roughness	4–11 nm RMS
Grain Size	~ 1 μ m for 1 micron film
Resistivity	1.75–1.8 μ m- Ω -cm
Purity	99.98–99.998
Texture	20–70% <111>

however, depends on the plating chemistry and the nominal current density. In the simplest case, too little mass transfer to an area of the wafer results in depletion of cupric ions, and a reduction of the plating rate. This effect becomes more pronounced at higher nominal current densities, in baths with lower cupric ion concentration, and when using lower nominal flow rates. In some cases, depletion of cupric ion near the wafer edge can be used to balance field effects, which tend to produce thicker films at the edge of the wafer [75]. Differences in the mass transfer rate of additives to different location on the wafer surface can impact the thickness distribution independent of cupric ion depletion. Baths with high concentrations of leveling additives can exhibit a reduced current density in areas of high mass transfer. In leveler-free baths the degree of accelerator adsorption on the wafer surface can impact plating rate; in this case an increased current density in areas of higher mass transfer is observed. Like the terminal effect, the impact of mass transfer differences on the thickness distribution is always proportional to the overall impedance differences between each point on the wafer and the anode. As a result, resistive electrolytes and resistive elements placed near the wafer will generally reduce the impact of mass transfer differences on thickness.

16.4.13 Metallurgy and Reliability

For optimum reliability and electrical performance copper films with large grains, high density, and low or controlled levels of impurities are preferred. Electroplated copper meets these requirements, however, the desired metallurgy is a complex result of deposition current, additive selection, and film annealing conditions. Properties of plated copper are summarized in Table 16.3 and Table 16.4 for films annealed at room temperature.

Ductility, hardness, and tensile strength are rarely monitored in copper deposited for IC applications. Stress in electroplated Cu films can vary from slightly compressive to slightly tensile, and normally approaches zero during room temperature anneal. Relatively high stresses of 200–300 MPa can be generated in plated Cu by annealing the copper above the plastic deformation temperature of about 230°C. Purity of plated copper varies depending on plating chemistry, mass transfer, and current conditions. In baths without a leveler, or in baths containing a leveler which is not incorporated in the

TABLE 16.4 Electroplated Copper Impurity Levels

Additive Type	Approximate Copper Impurity Concentrations (rpm)					
	C	S	Cl	O	N	All Metals
Standard 3 component additive	15–50	5–20	30–100	1–10	1–10	<1.0
Additive system in which no leveler is co-deposited during plating	1–5	1–5	1–5	<2	<2	<1.0

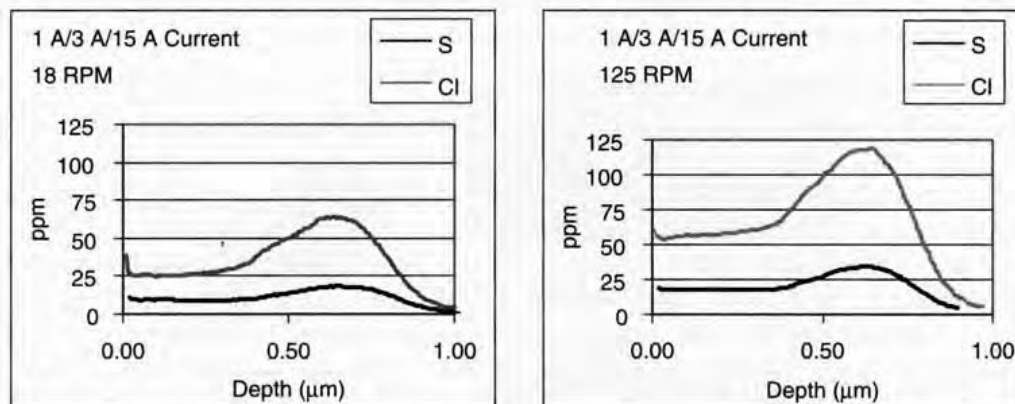


FIGURE 16.23 Copper film purity as a function of depth for films plated at an initial current of 1 A for 11 s followed by a current of 3 A for 30 s and a current of 15 A for 38 s. Films plated using 18 and 125 rpm wafer rotation rates are shown.

plated film, very high Cu purities are achieved. Most levelers used in damascene applications co-deposit during plating to yield significant levels of Cl, S, and C in the copper films. The degree of incorporation always increases with higher mass transfer rates and usually increases at lower plating current densities, both conditions which allow more leveler to diffuse to the wafer surface per unit of copper deposited. This behavior often results in purity variations as a function of depth in the plated films as shown in Figure 16.23. In this example, the upper portion of the film is plated at a higher current density, and exhibits much lower impurity levels than the lower portion of the film plated at a low current density. Higher impurity levels are also observed in the film plated using the higher wafer rotation rate of 125 rpm compared to 18 rpm as the result of greater mass transfer of leveler to the wafer surface. Purity measurement of copper within small features, which undergo bottom-up filling has been difficult to perform accurately because the analysis spot size exceeds the feature dimension for high accuracy measurement methods. The high localized currents during filling and somewhat more limited mass transfer of leveler into small features is expected to lead to an in-feature purity similar to that of copper plated at high currents. Texture of plated copper is more complex than that of Al since $\langle 111 \rangle$

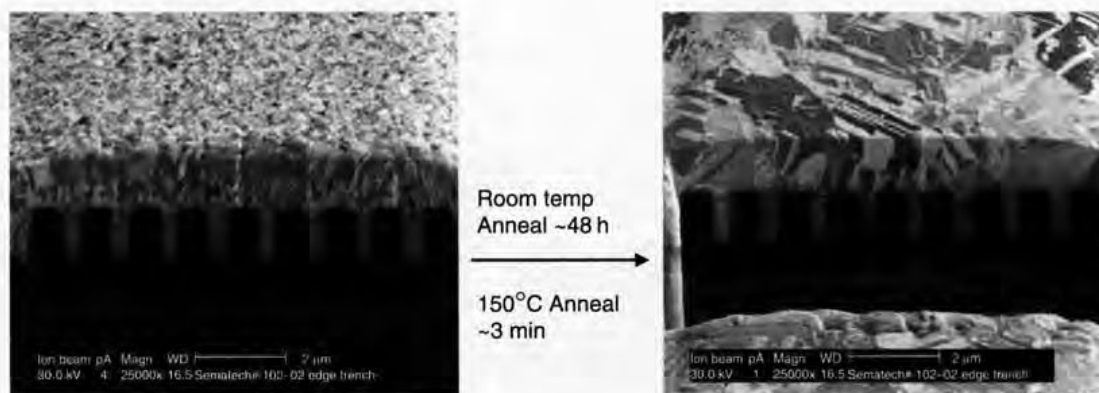


FIGURE 16.24 Focused ion beam (FIB) images of grain structure of plated copper films immediately after deposition and following anneal at room temperature.

orientation can be with respect to the field or the feature sidewall [76]. For copper, development of a large grain size, rather than a specific orientation, may be more relevant to reliability.

16.4.13.1 Grain Size and Anneal Behavior

Without additives present, or with a suppressor additive alone, copper generally grows to form columnar grains which follow the seed grain structure. With accelerator and suppressor additives present, the nucleation characteristics during copper growth are changed dramatically such that grains are continually formed during deposition. This results in a very small nominal grain size. The actual grain size after plating has been difficult to verify because of the unstable nature of the grains. Results such as those shown in Figure 16.24a for an ion beam cut of a plated film obtained within 15 min of deposition suggest as plated grains have dimensions of approximately 0.05–0.10 μm . Following deposition, electroplated copper films undergo grain growth even at room temperature to form grains which have dimensions as large or larger than the thickness of the plated film [77,78]. Figure 16.24b shows grains after room temperature anneal for the film shown in Figure 16.24a. In this example grains have grown to approximately 1.0 μm dimensions indicating about 99.9% of the initially plated grains have been consumed by other grains. Films as thick as 80 μm have been shown to undergo analogous growth behavior. This behavior is noted with films over a very wide range of impurity contents [79]. The stress, ductility [77], hardness [80], and resistivity [78] properties of the plated copper shift along with the grain growth, with fully annealed films being more ductile, softer, and about 20% more conductive.

Generally, the grain growth rate increases sharply as temperature of annealing is increased 1 μm thick films achieve nearly complete grain growth after as little as 60 s at 250°C. An activation energy of 19 Kcal/mol for grain growth of copper has been calculated based on stress, ductility, and resistivity change [77]. Anneal rates have been found to depend strongly on plated film thickness, with thinner films requiring a much longer time to undergo complete anneal, and films under 0.3 μm in thickness sometimes failing to undergo anneal at room temperature almost indefinitely. The time to anneal plated copper films has also been found to decrease as copper seed thickness decreases for a fixed plated thickness. In most cases films of higher purity undergo more rapid anneal at room temperature than lower purity films, possibly as the result of less grain boundary pinning by the impurities [79]. Plots of resistivity change as a function of time during grain growth at room temperature are shown for one micron films with high medium and low purity levels in Figure 16.25. After sufficient anneal, the resistivity difference between high and low purity films is generally found to be less than 2% and is

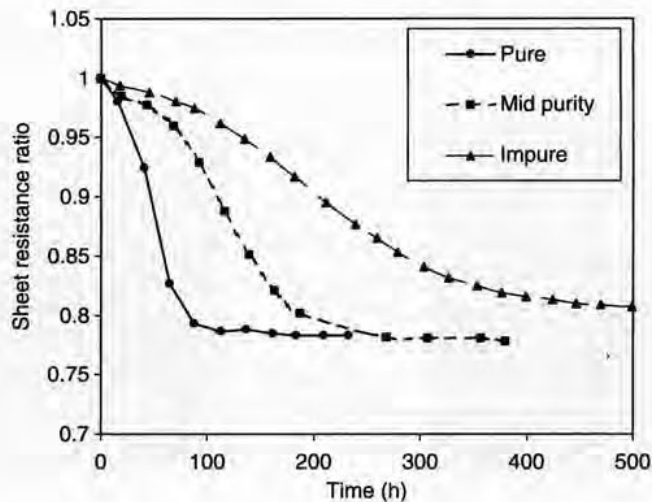


FIGURE 16.25 Resistivity changes during room temperature anneal of plated copper of several purity levels.

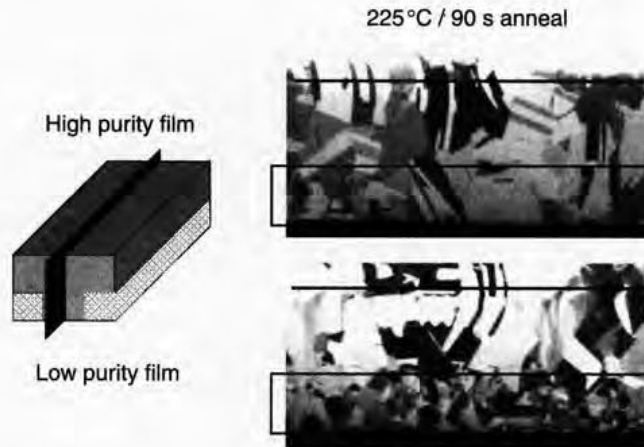


FIGURE 16.26 Cross section along length of 0.2 μm wide, 1.0 μm deep line showing growth of large grains in fine lines for higher purity films, but small grains remaining in lines for lower purity films.

difficult to measure. Anneal rates have also been found to increase for copper films plated at higher current density, independent of their purity [78]. In these cases, the as deposited films have also been noted to show higher initial resistivity possibly suggesting smaller as deposited grains with lower thermodynamic stability.

The grain growth, which electroplated copper on the wafer field undergoes, has been found to drive grain growth within adjacent small features as shown in Figure 16.26, potentially providing improved resistivity and reliability performance. As a result of this behavior, it is usually advantageous to anneal plated copper films prior to CMP of copper to obtain optimum EM and resistivity performance. Nearly all manufacturing process flows follow this anneal sequence and an anneal capability is frequently included in copper electroplating tools. Low purity films may require a higher temperature and a longer anneal time to achieve grain growth within features.

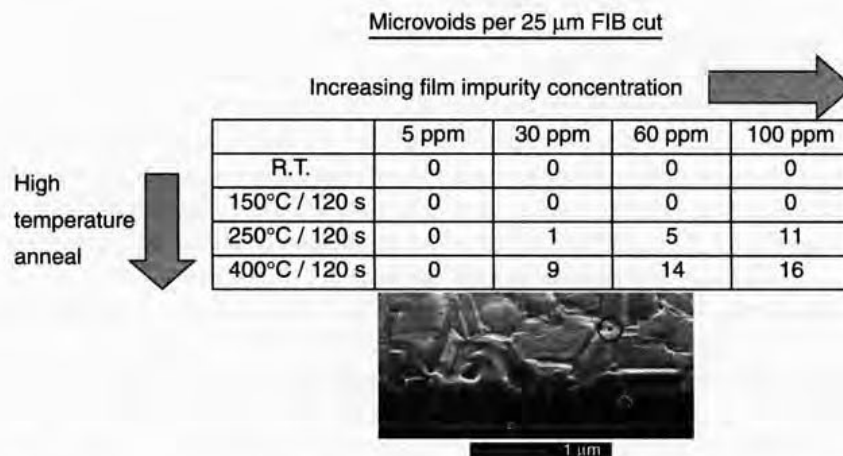


FIGURE 16.27 Microvoid formation following anneal of copper films of high and low purity.

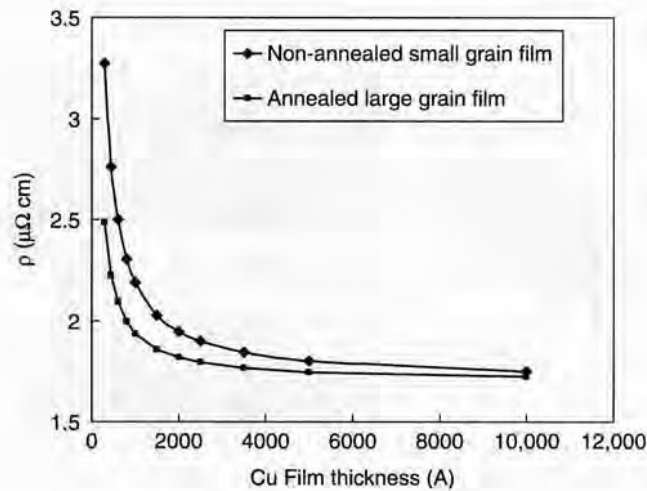


FIGURE 16.28 Copper resistivity as a function of film thickness for highly annealed large grained and small grained films.

During anneal and grain growth it has been found that small voids, frequently called “microvoids”, begin to appear in electroplated copper films [81]. Microvoids are usually in the range of 0.02–0.05 μm in diameter and appear at grain boundaries or triple points. Examples of microvoids in a continuous copper films are shown in Figure 16.27 as a function of the anneal temperature and film purity. Microvoid density and size is directly related to the plated copper film purity. High purity films develop only occasional microvoids following 400°C anneal while low purity films develop microvoids with increasing size and frequency as the anneal temperature is increased above 200°C. Chloride impurity levels have been suggested as being most strongly correlated with the tendency to form microvoids, however, the nature of the relationship between impurities and microvoids is not clearly understood. Microvoids can appear within features, however, their formation appears to require consolidation of numerous grain boundaries making formation in large continuous copper volumes more likely.

16.4.13.2 Resistivity

The transition from aluminum to copper interconnects was driven in part by the relatively low copper resistivity of 1.8–2.0 $\mu\text{m-}\Omega\text{-cm}$ which could be achieved in 90–130 nm generation features. As features become smaller and exhibit physical or grain dimensions similar to the 35 nm electron mean free path in copper, resistivity begins to increase. Figure 16.28 shows copper resistivity as a function of the planar film thickness for films with grains of dimension similar to the film thickness, and for films with uniformly large micron-size grains. The thin large grained films were specially prepared by CMP of fully annealed 1.0 μm thick films. The resistivity of the copper increases sharply as film thickness decreases, for both the very large and small grained films at film thickness below about 30 nm. This behavior, primarily due to electron surface scattering, suggests similar behavior will be seen for Cu resistivity in sub 30 nm features regardless of grain size. In the film thickness range between 50 and 100 nm the large grained films show a considerably reduced resistivity, suggesting grain boundary scattering can be important in features of similar dimension. Similar behavior has been reported and modeled as a function of line dimension [82,83]. The overall importance of fine line resistivity remains unresolved since fine lines may tend to be of relatively short length making their impedance dominated by capacitive, rather than resistive, effects. From a plating process perspective, annealing condition, field thickness, and purity of the plated copper will be important in extending the low resistivity nature of copper to smaller feature

dimensions, although the physical limit imposed by surface scattering is already beginning to impact 45–65 nm generation resistivity characteristics.

16.4.13.3 Stress Migration and Electromigration

Electromigration behavior in copper interconnects depends strongly on the barrier/seed and dielectric cap properties [82], however, the purity of electroplated copper and the grain size within features can also influence EM life. Electromigration life for high purity films is usually about three times longer than that of low purity films [84] for the ranges of impurity shown in Table 16.4 above. Work has suggested that the microvoids present in low purity films migrate to, and move along interfaces, during EM testing eventually accumulating and leading to earlier failure of the lower purity films [84]. Anneal conditions sufficient to grow large copper grains, but at a low enough a temperature so as not to induce significant microvoid formation, have also been found to improve electromigration life [85].

Efforts to improve EM of copper by alloying it with metals have been reported [86,87], however, the degree of improvements have been similar to the impact of the normal film impurities. Most alloying elements cannot be added to copper at concentrations over about 1% without impacting line resistance. This limits somewhat the use of bulk film alloys as a means to improve EM.

Like EM, stress migration life of interconnects depends most strongly on barrier/seed adhesion to dielectric and overall integration schemes. A failure during stress migration testing is usually an open due to missing copper near the base of a via located on a relatively large pad. Stress migration test failures are thought to be the result of stress induced vacancy movement toward or atomic migration away from the high stress location near the via base [88,89], often combined with interface failure between the barrier/seed or dielectric and the copper line or pad. Higher copper purity [90,91] has been found to be associated with earlier stress migration failures. Stress measurements of copper during thermal cycling has shown that high purity films have somewhat greater strength or lower ductility and accumulate more stress than the low purity films [90], probably explaining the relationship of stress migration life to film purity. It has also been suggested that impurities in the plated film act to reduce the diffusion of vacancies under stress, thus reducing the void formation and failure [91]. Based on the high microvoid content of low purity films which show generally improved stress migration behavior, it is unlikely that microvoids migrating from the bulk film are the primary cause for the stress migration failures.

When performing stress migration tests on high aspect ratio features, voids related to incomplete filling can be present in features prior to stress migration testing. In this situation, stress migration testing can be a sensitive measurement of fill quality because the fill related voids will randomly migrate during testing to the via base or sidewall leading to failure.

16.4.13.4 Defects

Defects related to copper electroplating can be classified as pitting or missing metal, abnormal copper growth, and particles. Most serious are pitting or missing metal defects which are the result of plated copper failing to deposit on the copper seed layer [92,93]. These defects can lead to opens in the damascene circuitry following CMP. Several examples of missing metal defects in plated copper films are shown in Figure 16.29. Causes for pit-type defects include incomplete initial wetting of the copper surface, air bubbles adhering to the plated surface, contamination of the seed with suppressor-additive-related polymer agglomerates, foams, micelles, or other particulates that deposit on the seed during entry into the plating bath, pre-existing contamination of the seed, and highly variable of severe oxidation of the copper seed which limits wetting. The size of pit-type defects can range from approximately 0.1 μm , to several microns in diameter. Defects related to air bubbles, poor wetting, or failure to displace air from the copper seed are usually circular and frequently appear in lines corresponding to wetting fronts or air bubble movement across the wafer surface. Pitting defects are reduced by controlling the exposure time of the wafers to ambient air between seeding and plating [92], selection of non-agglomerating suppressor additives with good wetting and low surface tension behavior [94,95], and selection of methods for wafer entry into the plating solution which create a single splash-free wetting interface across the wafer [94].

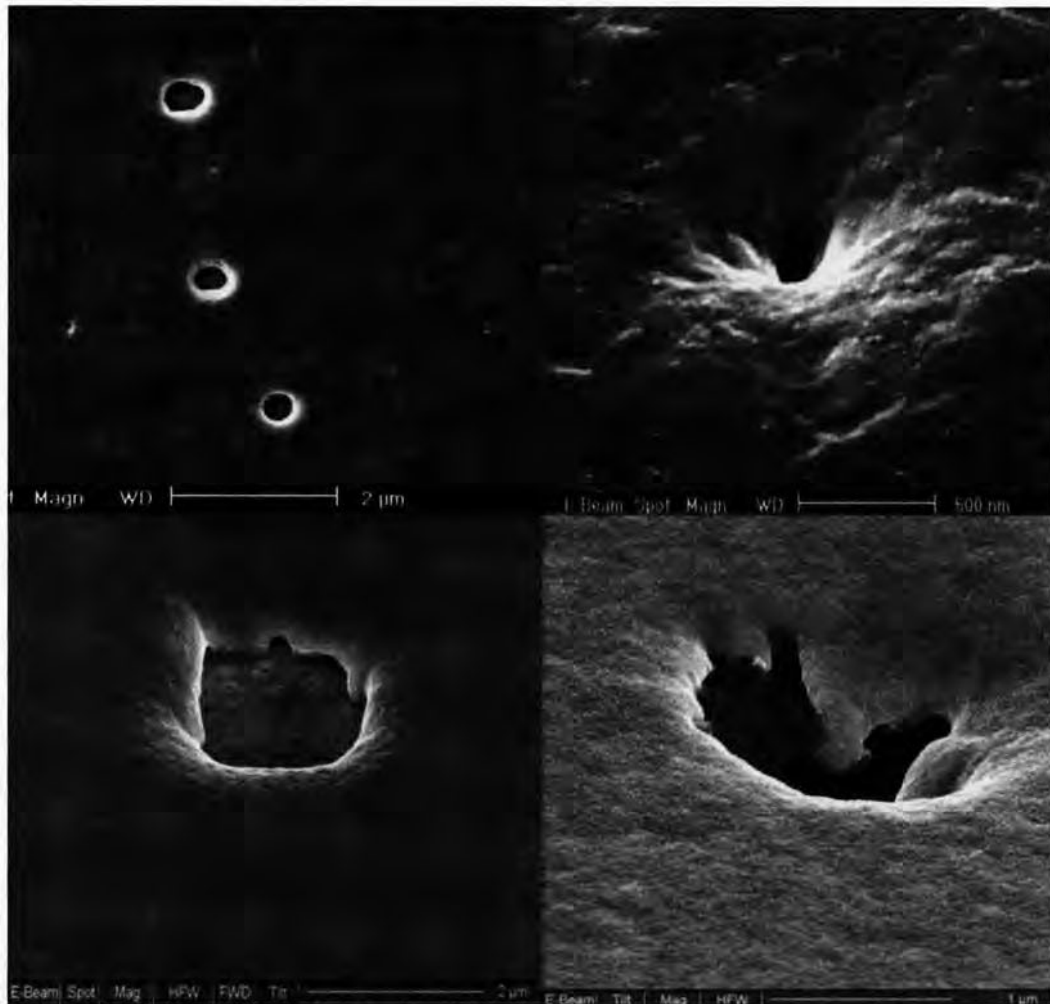


FIGURE 16.29 Missing metal and pitting defects observed after copper plating.

Missing metal defects which become apparent only after CMP can result from formation of microvoids during post-plate copper anneal or from galvanic corrosion during CMP processing.

Abnormal copper growth defects can be detected using various optical light inspection methods following copper plating [5]. In most cases, these defects will be removed during CMP processing and not result in a yield impact. Defect inspection methods do not normally differentiate between pitting and abnormal growth defects, so beyond the desire to have an imperfection-free film, these defects need to be eliminated to facilitate post plating wafer inspection to detect pitting. Abnormal growth defects are usually the result of either non-homogeneous additive adsorption or adherence of small conductive particles to the wafer surface during plating. These particles act as nucleation sites for excessive growth. Defects related to non-homogeneous additive adsorption are usually addressed by the proper selection of additive types, plating currents, and mass transfer rates. Defects related to small particles are most commonly the result of nanometer scale fragments of copper dislodging from the plating cell contact hardware or from the copper anode, and their subsequent transfer to the wafer surface. To prevent anode related particles from reaching the wafer surface, low porosity or ion selective membranes to prevent

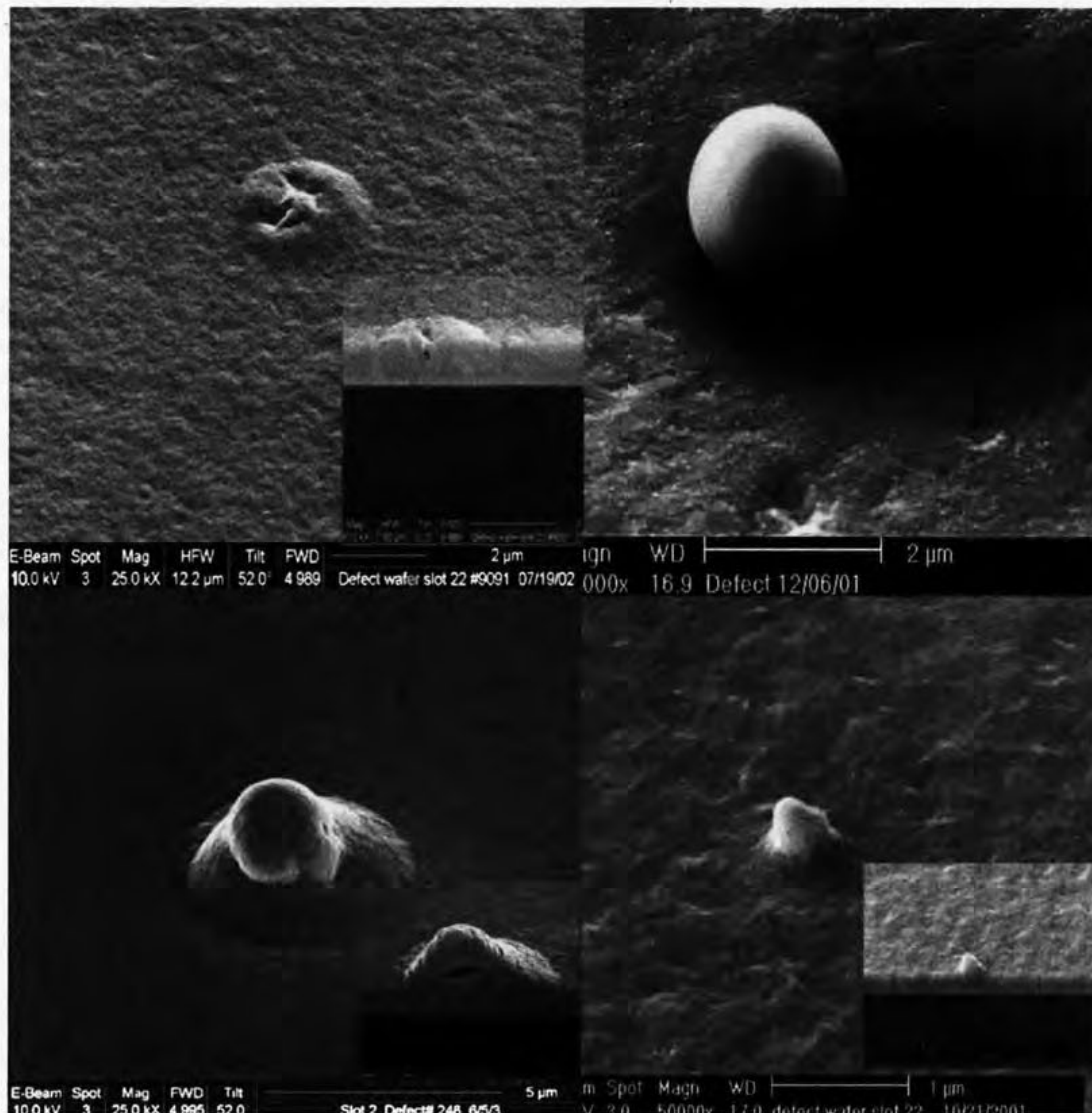


FIGURE 16.30 Abnormal growth defects observed after copper plating.

unfiltered solution from reaching the wafer surface. Examples of irregular copper growth type defects are shown in Figure 16.30.

Particles such as dislodged anode films or extraneous contamination can be incorporated in, or be present on, the plated copper film. To reduce particle defects, the plating solution is normally filtered using 0.05 μm filters immediately before reaching the plating cell and the anode is isolated from the wafer as discussed above. Plating cell material selection and design and adequate filter replacement frequency are also critical for particle free plating performance.

16.5 Modeling Capabilities

The across wafer thickness distribution of copper can be modeled based on plating bath resistivity, plating cell dimensions, seed resistivity, seed type, pattern density, electrical contact pattern, deposition

kinetics, and mass transfer. Several models have been developed which account for some or all of these factors [96–99]. In general, it has been found that seed resistivity, cell dimensions, and bath resistivity are critical in accurately predicting the thickness distribution. Items such as contact position around the perimeter of the wafer and pattern density can be shown to have increasing impact on the thickness distribution as the seed thickness decreases. Mass transfer and deposition kinetics are more difficult to model accurately and are usually less critical in predicting experimental thickness distributions. Mass transfer is relatively complex and usually turbulent due to the combination of wafer rotation and solution flow. This necessitates a full 3D simulation which makes accurate modeling across the full wafer time consuming. Deposition kinetics are influenced by additive adsorption behavior, mass transfer of the additives, and behaviors of the additives on the surface which are not fully understood making modeling based on fundamental principles difficult. Polarization curves at known mass transfer rates can be used to determine an interfacial resistance, which can represent mass transfer and deposition kinetic effects in models.

The fill behavior during damascene plating has been successfully modeled based on surface area loss within features leading to accelerator accumulation [100,101]. In addition, the degree of acceleration capability has been related in models to the degree of hysteresis between anodic and cathodic branches of polarization curves measured for the bath used for filling [101]. Other models have been developed to predict fill based on a lack of suppressor diffusion to the base of high aspect ratio features [102,103]. Although both types of models can predict bottom-up filling, the accelerator accumulation model assumptions are more consistent with the actual chemistries and conditions currently used for damascene filling.

16.6 Process Integration

16.6.1 Feature Profile and Seed Interactions

The performance of the damascene copper plating process is strongly influenced by the characteristics of the incoming PVD seed layers and the etch profile of the underlying dielectric. An ideal seed provides continuous coverage of slightly oxidized copper of uniform thickness within a feature. The physical characteristics of PVD processes, however, tend to result in thicker seed coverage near the top of the feature and thinner coverage near the feature base. This behavior is accentuated when dielectric profiles are re-entrant and result in shadowing of the lower feature sidewalls during seeding. As the seed becomes

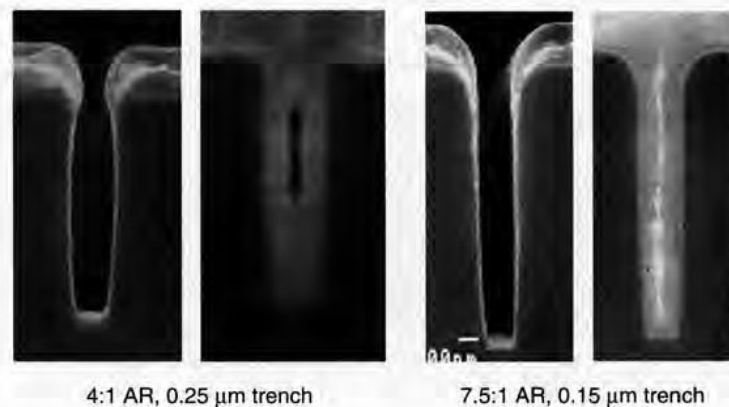


FIGURE 16.31 Profiles of trenches following copper seed layers with excessive overhang and vertical profiles and the resulting fill performance.

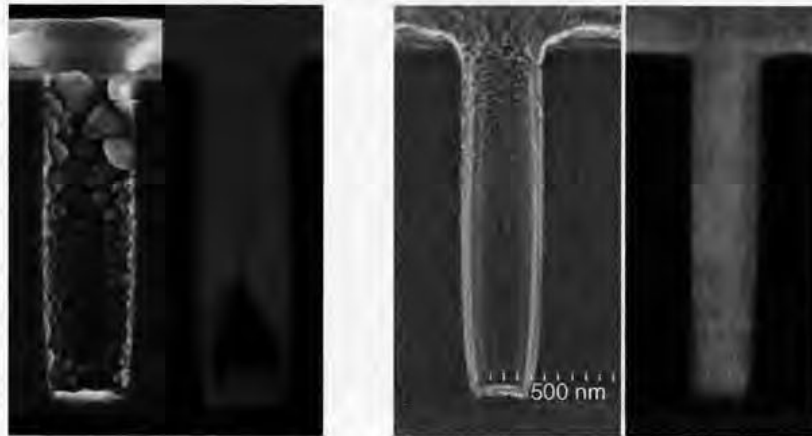


FIGURE 16.32 Topography of copper seed layers on via sidewalls for highly agglomerated and for smooth continuous seeds and the resulting fill performance.

thinner, coverage can become discontinuous or the seed can become fully oxidized, usually near the base of high aspect ratio features [61].

When the seed thickness near the top of the feature becomes too great, the aspect ratio of the remaining open area within the feature increases dramatically and fill without a top center void becomes difficult. Figure 16.31 compares fill in a typical damascene bath for a trench showing significant seed overhang with fill in a higher dielectric aspect ratio trench without overhang. Void free fill is achieved in the feature without seed overhang, while a center void is formed in the trench with excessive seed overhang. Typical pre-plate aspect ratio's which include seed coverage are normally kept under 10 in production to avoid top center void formation.

When seed discontinuity near the feature base occurs due to either agglomeration of the seed copper, because the seed thickness is too low, or due to excessive seed oxidation, bottom voids are observed following plating. Via fill results on an agglomerated seed are shown in Figure 16.32 along with results on a smooth continuous seed layer. Following plating on the agglomerated seed a large bottom void is observed, while deposition on the continuous seed yields void free fill. Seed repair processes utilizing electroless and electrolytic deposition from alkaline solutions were found to be capable of improving fill on discontinuous seed layers [104,105], however, barrier/seed technology improvements have resulted in continuous seed layers with little overhang near the top of the feature. Complete fill of trenches with aspect ratio of up to 20:1 and widths as small as 0.06 μm has been reported in cases where a slight "V" shape exists in the dielectric profile. Improved PVD technology and advancements such as atomic layer deposition result in both an improvement in the seed thickness uniformity within features as well as a reduction in the pre-plate aspect ratio. These developments should allow fill of 32 nm generation or smaller interconnects using existing plating baths, or chemistries modified to more rapidly initiate bottom-up filling.

16.7 Process Control Approaches

In order to maintain consistent process performance, damascene plating equipment normally operates using a large reservoir of plating solution, which is re-circulated through several plating cells. Reservoir volumes of approximately 200 L and plating cell volumes of 5–15 L are typical. The large reservoir volume improves bath stability by acting as a buffer with respect to unexpected dilution, evaporation, or additive consumption variations. During continuous copper deposition, additive chemicals decompose to form by-products, which impact bath performance [106] and result in a finite bath lifetime. To reduce

the impact of additive degradation, plating baths can either be fully replaced prior to a significant change in process performance, or a fraction of the plating solution in the reservoir can regularly be exchanged for fresh electrolyte [107] allowing process operation in a near steady-state condition. An alternative approach, in which the plating solution reservoir is eliminated and small volumes of plating solution are circulated through the plating cells and replaced after a relatively short period of use, has also been implemented [5]. To help maintain process stability, most commercial plating systems use automated dosing of additive components to replace additives consumed during plating.

In all systems, monitoring the concentrations of the plating solution components is required for process verification and correction of concentration deviations. Most damascene plating equipment includes on-line concentration monitoring, and in some cases feedback for dosing of bath components to correct for concentration deviations [108]. Concentrations of inorganic bath components can be monitored using titrations, electrochemical methods [109–111], UV spectroscopy, and other methods. Typical control ranges are less than 2% relative standard deviation. Monitoring of additive components is generally carried out using electrochemical methods such as cyclic voltammetric stripping (CVS) or real time analysis (RTA) [112]. These methods yield analysis accuracy on the order of $\pm 5\%$ relative standard deviation.

Using CVS methods, the voltage is cycled to deposit and strip copper on an electrode in solutions containing bath samples and various standards. The amount of copper stripped during the voltage cycles is measured and related to the concentration of a given additive component. A unique set of bath sample solutions and voltage cycles is normally required for analysis of each additive component, and samples must be discarded after analysis.

Using RTA methods, complex waveforms are applied to an electrode immersed in the plating bath. The current response is measured and related directly to the additive concentration [112]. The plating solution is not consumed during the analysis.

Alternative methods for additive analysis include high performance ion or liquid chromatography [113,114], and mass spectroscopy. These methods provide more direct chemical information such as molecular structure, molecular weight distribution, and inert and active breakdown product concentrations, but are not widely implemented at this time.

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References

1. Edelstein, D. C., Y. J. Mii, and G. A. Sai-Halasz. "VLSI On-Chip Interconnection Performance Simulations and Measurements." *IBM J. Res. Dev.* 39 (1995): 383.
2. Andricacos, P. C., et al. "Damascene Copper Electroplating for Chip Interconnections." *IBM J. Res. Dev.* 42 (1998): 567.
3. Edelstein, D. C., et al. "Full Copper Wiring in a Sub 0.25 μm CMOS ULSI Technology." Technical Digest, IEE International Electron Devices Meeting, 773. 1997.
4. Andricacos, P. C. "Copper On-Chip Interconnections: A Breakthrough in Electrodeposition to Make Better Chips." *Interface* 8 (1999): 32.
5. Beaudry, C. L., and J. O. Dukovic. "Faraday in the Fab: A Look at Copper Plating for On-Chip Wiring." *Interface* (2004): 40.
6. Misawa, N. et al. "High Performance Planarized CVD-Cu Multi-Interconnection." *VMIC Conf. Proc.* (1993): 353.

7. Nguyen, T., et al. "Electrical Characteristics of CVD Copper Interconnects and Vias." *Electrochem. Soc. Proc.* 97 (1997): 120.
8. Shacham-Diamand, Y., and V. M. Dubin. "Copper Electroless Deposition for ULSI Metallization." *Microelect. Eng.* 33 (1997): 47.
9. Shacham-Diamand, Y., and S. Lopatin. "High Aspect Ratio Quarter-Micron Electroless Copper Integrated Technology." *Microelect. Eng.* 37 (1997): 77.
10. Nguyen, T., L. J. Charneski, and D. R. Evans. "Temperature Dependence of the Morphology of Copper Sputtered Deposited on TiN Coated Substrates." *J. Electrochem. Soc.* 144 (1997): 3634.
11. Shibuki, S., S. Kanao, and T. Akahori. "Copper Film Formation Using Electron Cyclotron Resonance Plasma and Reflow Method." *J. Vac. Sci. Tech. B.* 15 (1997): 60.
12. Schlessinger, M., and M. Panouvic., *Modern Electroplating*. 4th ed, New York: Wiley, 1980.
13. Vereecken, P. M., et al. "The Chemistry of Additives in Damascene Copper Plating." *IBM J. Res. Dev.* 49 (2005): 3.
14. Takahashi, K. M. "Electroplating Copper onto Resistive Barrier Films." *J. Electrochem. Soc.* 147 (2000): 1414.
15. Dukovic, J. O. "Current Distribution and Shape Change in Electrodeposition of Thin Films for Microelectronic Fabrication." *Adv. Echem. Sci. Eng.* 3 (1994): 117.
16. Alkire, R. "Transient Behavior During Electrodeposition onto a Metal Strip of High Ohmic Resistance." *J. Electrochem. Soc.* 118 (1935): 1971.
17. Landau, U., J. J. D'Urso, and D. B. Rear. Electrodeposition chemistry. U.S. Patent 6,113,771, Issued Sept. 5, 2000.
18. Reid, J. D. "Copper Electrodeposition: Principles and Recent Progress." *Jpn. J. Appl. Phys.* 40 (2001): 2650.
19. Reid, J. D., and S. Mayer. "Factors Influencing Fill of IC Features Using Electroplated Copper." In *Materials Research Society Journal 1999 Advanced Metallization Conference Proceedings Red Book Series*, edited by M. Gross, 53–62. Warrenton PA: MRS Press, 2000.
20. Moffat, T. P., D. Wheeler, and D. Josell. "Superfilling and the Curvature Enhances Accelerator Coverage Mechanism." *Interface* (2004): 46.
21. Osterwald, J. "Leveling and Roughening by Inhibitors and Catalysts." *Oberflache-Surface* 17, no. 5 (1976): 89.
22. Bard, A. J., and L. R. Faulkner., *Electrochemical Methods Fundamentals and Applications*. New York: Wiley, 1980.
23. Reid, J. D., and A. P. David. "Impedance Behavior of a Sulfuric Acid—Copper Sulfate/Copper Cathode Interface." *J. Electrochem. Soc.* 134 (1987): 1389.
24. Alkire, R., and D. B. Reiser. "Electrode Shape Change during Deposition onto an Array of Parallel Strips." *Electrochimica. Acta* 28 (1983): 1309.
25. Kessler, T., and R. Alkire. "A Model for Copper Electroplating Multilayer Boards." *J. Electrochem. Soc.* 123 (1976): 990.
26. Dukovic, J. O. "Feature-Scale Simulation of Resist Patterned Electrodeposition." *IBM J. Res. Dev* 37 (1993): 125.
27. Gauvin, W. H., and C. A. Winkler. "The Effect of Chloride Ions on Copper Electrodeposition." *J. Electrochem. Soc.* 99 (1952): 71.
28. Jovic, V. D., and B. M. Jovic. "Copper Electrodeposition from a Copper Acid Bath in the Presence of PEG and NaCl." *J. Serbian. Chem. Soc.* 66 (2001): 935.
29. Healy, J. P., D. Pletcher, and M. Godelough. "The Chemistry of the Additives in an Acid Copper Electroplating Bath, Part 1. Polyethylene Glycol and Chloride Ion." *J. Electroanal. Chem.* 338 (1992): 155.
30. Goldbach, S., et al. "Coupled Effects of Chloride Ions and Branched Polypropylene Ether LP-1 on the Electrochemical Deposition of Copper from Sulfate Solution." *Electrochim. Acta* 44 (1998): 323.
31. Yokoi, M., S. Konishi, and T. Hayashi. "Mechanism of the Electrodeposition and Dissolution of Copper in an Acid Copper Sulfate Bath IV: Acceleration Mechanism in Presence of Cl⁻ Ions." *Denki Kagaku* 51 (1983): 460.

32. Tan, M., and J. N. Harb. "Additive Behavior during Copper Electrodeposition in Solutions Containing Cl⁻, PEG and SPS." *J. Electrochem. Soc.* 150 (2003): 420.
33. Sarma, R. L., and S. Nageswar. "Electrodeposition of Copper in the Presence of 2-Mercaptoethanol." *Surf. Technol.* 12 (1981): 377.
34. Farndon, E. E., F. C. Walsh, and S. A. Campbell. "Effect of Thiourea, Benzotriazole, 4,5-Dithiooctane-1,8-Disulfonic Acid on the Kinetics of Copper Deposition from Dilute Sulphate Solutions." *J. Appl. Electrochem.* 25 (1995): 574.
35. Zhukauskaite, N., and A. Malinauskas. "Mechanism of the Brightening Effect of the Disulfide of Dipropanedisulfonic Acid in Acid Copper Plating Electrolytes." *Protect. Met.* 25 (1989): 132.
36. Moffat, T. B., et al. "Accelerator Aging Effects during Copper Electrodeposition." *Electrochem. Solid State Lett.* 6 (2003): C59.
37. Lichusina, S. B., et al. "Electrodeposition of Cu in Acidic CuSO₄ Solutions Containing Accelerating Additive-Sulfite. 4 GALVANOSTATIC Transients for Cu Cathode." *Chemija* 4 (1996): 29.
38. Simkunaite, D., and A. Steponavicius. "Chronopotentiometric Investigation of Acidic CuSO₄ Solution Containing Accelerating Additive—DDDS." *Chemija* 3 (1996): 42.
39. Reid, J. D., C. Gack, and S. H. Hearne. "Cathodic Depolarization Effect during Electroplating on Patterned Wafers." *Electrochem. Solid State Lett.* 6 (2003): C26.
40. Frank, A., and A. J. Bard. "The Decomposition of the Sulfonate Additive Sulfopropyl Sulfonate in Acid Copper Electroplating Chemistries." *J. Electrochem. Soc.* 150 (2003): C244.
41. Reid, J. D. "An HPLC Study of Acid Copper Brightener Properties." *Printed Circuit Fabrication* 65 (1987): 65–71.
42. Reid, J. D., and A. P. David. "Effects of Polyethylene Glycol on the Electrochemical Characteristics of Copper Cathodes in an Acid Copper Medium." *Plat. Surf. Finish.* 74 (1987): 66–70.
43. Kelly, J., and A. West. "Copper Deposition in the Presence of Polyethylene Glycol II. Electrochemical Impedance Spectroscopy." *J. Electrochem. Soc.* 45 (2000): 3477.
44. Kelly, J., and A. West. "Copper Deposition in the Presence of Polyethylene Glycol I. Quartz Microbalance Study." *J. Electrochem. Soc.* 145 (1998): 3472.
45. Hebert, K. R., S. Adhikari, and E. Houser. "Chemical Mechanism of Suppression of Electrodeposition by Poly(Ethylene Glycol)." *J. Electrochem. Soc.* 152 (2005): C324.
46. Hope, G., and G. Brown. "A Study of the Adsorption of Polymeric Additives at a Copper Electrode and the Incorporation into Copper Deposits by Electrodeposition." *Electrochem. Soc. Proc.* 96 (1996): 215.
47. Kelly, J., C. Tian, and A. C. West. "Leveling and Microstructure Effects of Additives for Copper Electrodeposition." *J. Electrochem. Soc.* 146 (1999): 2540.
48. Franklin, T. C. "Some Mechanisms of the Action of Additives in Electrodeposition Processes." *Surf. Coat. Tech.* 30 (1987): 415.
49. Jordan, K. G., and C. W. Tobias. "The Effect of Inhibitor Transport on Leveling in Electrodeposition." *J. Electrochem. Soc.* 138 (1991): 1251.
50. Tindall, G. W., and S. Bruckenstein. "Determination of Heterogeneous Equilibrium Constants by Chemical Stripping at Ring Disk Electrode: $\text{Cu} + \text{Cu}_2 + -2\text{Cu} +$ in Sulfuric Acid." *Analytical. Chem.* (1968): 1402.
51. Cheng, X., and B. Hisky. "Fundamental Studies of Copper Anode Passivation during Electrorefining: Part 2 Surface Morphology." *Metall. Mat. Trans. B* 27B (1996): 610.
52. Demedts, G., and A. P. Van Peteghem. "The Corrosion of Copper a Tool in the Investigation of the Reaction Kinetics." *Corros. Sci.* 18 (1978): 1041.
53. Frankel, G. S., et al. "Behavior of Cu(P) and Oxygen Free High Conductivity Cu Anodes under Electrodeposition Conditions." *J. Electrochem. Soc.* 140 (1993): 959.
54. Rashkov, V. S., G. Raichevski, and L. Vuchkov. "Influence of Anodic Films on the Kinetics and Mechanism of the Dissolution of Copper Anodes in Bright Acid Copper Plating." *Bulg. Acad. Sci., Comm. Dept. Chem.* 11 (1978): 459.
55. Reid, J. D., and A. P. David. "Kinetics of Copper Dissolution at Oxygen Free and Phosphorized Anodes." *AIChE Symp.* 83 (1987): 1 (Series 254).

56. Walker, C. T. "Copper Anode Area for High Speed Plating." *PC Fab.* 8-8 (1985): 30.
57. Mayer, S. T., et al. Copper electroplating apparatus. U.S. Patent 6527920, issued Mar. 4, 2003.
58. Ting, C. H., et al. Copper replenishment technique for precision copper plating system. U.S. patent 5997712, issued Dec. 7, 1999.
59. Zhu, M., et al. "Recent Advances in Gap Filling Cu Electroplating Technology." *Electrochem. Soc. Proc.* 99 (1999): 38.
60. Thies, A., et al. "A Novel Electrolyte for Wafer Plating." Materials Research Society Journal 1999 AMC Proceedings Red Book Series. 15,69. Warrenton PA: MRS Press, 2000.
61. Reid, J., et al. "Factors Influencing Damascene Feature Fill Using Copper PVD and Electroplating." *Solid State Technol.* July (2000): 86-103.
62. Moffat, T. P., et al. "Superconformal Electrodeposition of Copper." *Electrochem. Solid-State Lett.* 4 (2001): C26.
63. Josell, D., et al. "A Simple Equation for Predicting Superconformal Electrodeposition in Sub-Micron Trenches." *J. Electrochem. Soc.* 148 (2001): 767.
64. Moffat, T., et al. "Superconformal Electrodeposition of Copper in 500 to 75 nm Features." *J. Electrochem. Soc.* 147 (2000): 4524.
65. Josell, D., et al. "Superconformal Electrodeposition in Sub-Micron Features." *Phys. Rev. Lett.* 87 (2001): 16102.
66. West, A. C. "Theory of Filling High-Aspect Ratio Trenches and Vias in Presence of Additives." *J. Electrochem. Soc.* 147 (2000): 227.
67. Georgiadou, M., et al. "Simulation of Shape Evolution during Electrodeposition of Copper in the Presence of Additive." *J. Electrochem. Soc.* 148 (2001): 54.
68. Gill, W. N., D. J. Duquette, and D. Varadarajan. "Mass Transfer Models for the Electrodeposition of Copper with a Buffering Agent." *J. Electrochem. Soc.* 148 (2001): 289.
69. West, A. C., C. C. Cheng, and B. C. Baker. "Pulse Reverse Copper Electrodeposition in High Aspect Ratio Trenches and Vias." *J. Electrochem. Soc.* 145 (1998): 3070.
70. Hayase, M., et al. "Copper Bottom-Up Deposition by Breakdown of PEG-Cl Inhibition." *Electrochem. Solid-State Lett.* 5 (2002): 99.
71. Lee, C., and D. Duquette. "Pulsed Electrodeposition of Copper from Alkaline and Acid Baths for Metallization of Integrated Circuits." *Electrochem. Soc. Proc.* 99-31 (2000): 111.
72. Bason, B. Plating method and apparatus that creates a differential between additive disposed on a top surface and a cavity surface of a workpiece using an external influence. U.S. Patent 6402923, issued June 11, 2002.
73. Mayer, S. T., et al. Method and apparatus for uniform of thin metal seeded wafers using multiple segmented virtual anode sources. U.S. Patent 6773571, issued August 10, 2004.
74. Mayer, S. T., et al. Method and apparatus for uniform electroplating of integrated circuits using a variable field shaping element. U.S. Patent 6402923, issued June 11, 2002.
75. Reid, J. D., et al. Method of electroplating semiconductor wafer using variable currents and mass transfer to obtain uniform plated layer. U.S. Patent 6074544, issued June 13, 2000.
76. Link, C., M. Gross, and W. Brown. "X-Ray Diffraction Pole Figure Evidence for (111) Sidewall Texture of Electroplated Cu in Submicron Damascene Trenches." *Appl. Phys. Lett.* 74 (1999): 682.
77. Oshida, Y., P. C. Chen, and J. D. Reid. "Time-Dependent Ductility of Electrodeposited Copper." *J. Electronic Packaging (ASME)* 114 (1992): 448.
78. Harper, J. M., et al. "Mechanisms for Microstructure Evolution in Electroplated Copper Thin Films Near Room Temperature." *J. Appl. Phys.* 86 (1999): 2516.
79. Malhotra, S. P., et al. "Copper Room Temperature Resistance Transients as a Function of Electroplating Parameters." Materials Research Society Journal 1999 AMC Proceedings Red Book Series. 15. Warrenton PA: MRS Press, 2000.
80. Kozlov, V. M. "Influence of Annealing on the Structure and Macrohardness of Electrolytic Copper." *Phys. Met. Metall.* 45 (1979): 184.
81. Sekiguchi, A., et al. "Void Formation by Thermal Stress Concentration at Twin Interfaces in Cu Thin Films." *Appl. Phys. Lett.* 79 (2001): 1.

82. Hu, C. K., et al. "Electromigration in On-Chip Single/Dual Damascene Cu Interconnections." *J. Electrochem. Soc.* 149 (2002): 408.
83. Mallikarjunan, A., S. Sharma, and S. Murarka. "Resistivity of Copper Films at Thicknesses Near the Mean Free Path of Electrons in Copper." *Electrochem. Solid-State Lett.* 3 (2000): 437.
84. Alers, G. B., et al. "Influence of Copper Purity on Microstructure and Electromigration." *2000 IITC Conf. Digest Tech. Pap.* 45 (2000): 2000.
85. Parikh, S., et al. "Defect and Electromigration Characterization of a Two Level Copper Interconnect." *2001 IITC Conf. Digest Tech. Pap.* 183 (2001): 2001.
86. Padhi, D., et al. "Electrodeposition of Copper-Tin Alloy Thin Films for Microelectronic Applications." *Electrochimica. Acta* 48 (2003): 935.
87. Lee, K. H., C. K. Hu, and K. N. Tu. "Insitu Electron Microscope Comparison Studies on Electromigration of Cu and Cu(Sn) Alloys for Advanced Chip Interconnects." *J. Appl. Phys.* 78 (1995): 4428.
88. Aoyagi, M. "Stress-Induced Migration Model Based on Atomic Migration." *J. Mater. Res.* 19 (2004): 2349.
89. Ogawa, E. T., et al. "Stress-Induced Voiding under Vias Connected to Wide Cu Metal Lines." *Int. Reliability Phys. Symp. Proc.* (2002): 312.
90. Alers, G., et al. "Stress Migration and Mechanical Properties of Copper." *Int. Reliability Phys. Symp. Proc.* (2005): 36-111.
91. Shih, C. H. "Design of ECP Additive for 65 nm-node Technology BEOL Reliability." *IITC Conf. Digest Tech. Pap.* 102 (2005): 2005.
92. Varadajaran, S., D. Kalakad, and T. Cacouris. "Understanding and Reducing Copper Defects." *Semicond. Int.* 25 (2002): 125-130.
93. Shaw, J. B., et al. "Voids, Pits, and Copper." *Yield Manage. Solutions* 4 (2002): 8.
94. Lu, J., et al. "Understanding and Eliminating Defects in Electroplated Cu Films." *IITC Conf. Digest Tech. Pap.* 280 (2001): 2001.
95. Lee, D. W., et al. "Effect of Acidity on Defectivity and Film Properties of Electroplated Copper." *J. Electrochem. Soc.* 151 (2004): 204.
96. Deligianni, H., et al. "Model of Wafer Thickness Uniformity in an Electroplating Tool." *Proc. Electrochem. Soc.* 99-1 (1999): 83.
97. Kobayashi, K. "Trench and Via Fill Profile Simulations for Copper Electroplating Process." *IITC Conf. Digest Tech. Pap.* 34 (2000): 2000.
98. Broadbent, E. K., et al. "Experimental and Analytical Study of Seed Layer Resistance for Copper Damascene Electroplating." *J. Vac. Sci. Technol. B* 17 (1999): 2584.
99. Gochberg, L. A. "Modeling of Uniformity and Scale-up in a 300 mm Copper Electroplating Tool." *Proceedings of the International Symposium on Fundamental Aspects of Electrochemical Deposition and Dissolution. Electrochemical Society Proceedings*, edited by M. Matlosz, et al., Vol. 99-33, 421-31. Pennington, NJ: Electrochemical Society, 2000.
100. West, A. C., J. D. Reid, and S. T. Mayer. "A Superfilling Model That Predicts Bump Formation." *Electrochem. Solid State Lett.* 4 (2001): C50.
101. Josell, D., et al. "Superconformal Electrodeposition in Sub-Micron Features." *Phys. Rev. Lett.* 87 (2001): 16102.
102. Cao, Y., et al. "Three Additive Model of Superfilling of Copper." *J. Electrochem. Soc.* 148 (2001): 466.
103. Soukane, S., S. Sen, and T. Cale. "Feature Superfilling in Copper Electrochemical Deposition." *J. Electrochem. Soc.* 149 (2002): C74.
104. Webb, E., et al. "Integration of Thin Electroless Copper Films in Copper Interconnect Metallization." *J. Appl. Electrochem.* 34 (2004): 291.
105. Sukamto, J. H., et al. "An Evaluation of Electrolytic Repair of Discontinuous PVD Copper Seed Layers in Damascene Vias." *J. Appl. Electrochem.* 34 (2004): 283.
106. Jiang, Q., R. Mikkola, and B. Carpenter. "Critical Influence of Plating Bath Temperature on Cu Damascene Electrodeposits." *J. Vac. Sci. Technol. B* 17 (1999): 2361.
107. Andricacos, P. C., J. O. Dukovic, and L. T. Romankiw. Method for controlling chemical species concentration. U.S. Patent 5352350, issued Oct. 4, 1994.

108. Contolini, R., et al. "Use of On-Line Chemical Analysis for Copper Electrodeposition." In *Materials Research Society Journal 1999 Advanced Metallization Conference Proceedings Red Book Series*, edited by M. Gross, 117. Warrenton PA: MRS Press, 2000.
109. Freitag, W. O., et al. "Determination of the Individual Additive Components in Acid Copper Plating Baths." *Plat. Surf. Finish.* 70 (1983): 55.
110. Haak, R., R. Teench, and C. Ogden. "Cyclic Voltammetric Stripping Analysis of Acid Copper Sulfate Plating Baths Part 2: Sulfoniumalkanesulfonate-Base Additives." *Plat. Surf. Finish.* 69 (1982): 62.
111. Mansfeld, F. "The Copper Plating Bath Monitor." *Plat. Surf. Finish.* 65 (1978): 60.
112. Wikiel, H. and K. Wikiel. "On-line Monitoring of Copper Interconnect Deposition Processes." AESF SUR/FIN 2000 Proceedings. Orlando, FL: AESF1, 2000.
113. Reid, J. D. "An HPLC Study of Acid Copper Brightener Properties." *Printed Circuit Fabrication* 11 (1987): 65.
114. Heberling, S. S., S. Carson, and D. Campbel. "Monitoring Acid Copper Plating Baths." *Printed Circuit Fabrication* 12 (1989): 72.