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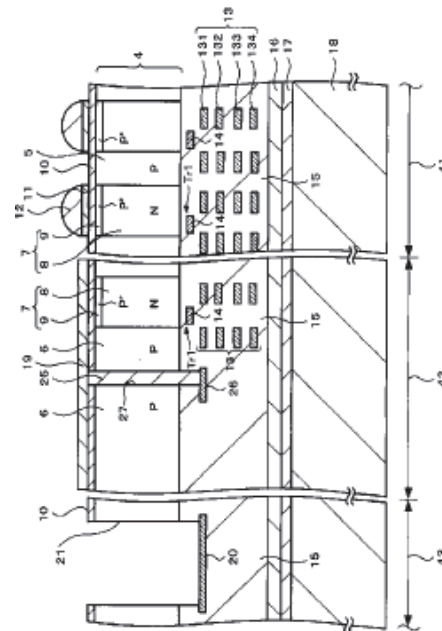
(54) (Title of the Invention) Solid-state Image Sensor, Solid-state Image Pickup Device, and Process for Producing a Solid-state Image Sensor

(57) (Abstract)

(Object) Provide a solid-state image pickup device constructed to allow the minority carriers generated in the photoelectric conversion elements to be easily extracted.

(Construction) A solid-state image pickup device is constructed with a solid-state image sensor 1 having photoelectric conversion elements 7 formed in a semiconductor substrate 4, wiring layers 13 formed in the insulating layer 15 disposed on the front face side of the semiconductor substrate 4, light being irradiated against the photoelectric conversion elements 7 from the back face side of the semiconductor substrate 4, a semiconductor region 6 formed in the semiconductor substrate 4 at the periphery of the photoelectric conversion elements 7, and a conductive material layer 25 formed at least in one section of the semiconductor region 6 from the back face side of the semiconductor substrate 4; and a means for applying a voltage to the solid-state image sensor 1, the means applying the ground potential to the conductive material layer 25.

(Elected Drawing) FIG. 2



(Claims)

(Claim 1)

A solid-state image sensor comprising
photoelectric conversion elements formed in a semiconductor substrate, and
wiring layers formed in the insulating layer disposed on the front face side of said semiconductor substrate,
light being irradiated against said photoelectric conversion elements from the back face side of said semiconductor substrate,
said solid-state image sensor being characterized by having
a semiconductor region formed in said semiconductor substrate at the periphery of said photoelectric conversion elements, and
a conductive material layer formed at least in one section of said semiconductor region from the back face side of said semiconductor substrate.

(Claim 2)

A solid-state image sensor according to claim 1 characterized such that said conductive material layer is embedded in a hole formed to penetrate from the back face side of said semiconductor region to the front face side of said semiconductor substrate.

(Claim 3)

A solid-state image pickup device characterized by comprising:
a solid-state image sensor having
photoelectric conversion elements formed in a semiconductor substrate,
wiring layers formed in the insulating layer disposed on the front face side of said semiconductor substrate,
light being irradiated against said photoelectric conversion elements from the back face side of said semiconductor substrate,
a semiconductor region formed in said semiconductor substrate at the periphery of said photoelectric conversion elements, and
a conductive material layer formed at least in one section of said semiconductor region from the back face side of said semiconductor substrate; and
a means for applying a voltage to said solid-state image sensor,
said means applying the ground potential to said conductive material layer.

(Claim 4)

A solid-state image pickup device according to claim 3 characterized such that said conductive material layer is embedded in a hole formed to penetrate from the back face side of said semiconductor region to the front face side of said semiconductor substrate.

(Claim 5)

A solid-state image pickup device characterized by comprising:
a solid-state image sensor having
photoelectric conversion elements formed in a semiconductor substrate,
wiring layers formed in the insulating layer disposed on the front face side of said semiconductor substrate,
light being irradiated against said photoelectric conversion elements from the back face side of said semiconductor substrate,
a semiconductor region formed in said semiconductor substrate at the periphery of said photoelectric conversion elements, and
a conductive material layer formed at least in one section of said semiconductor region from the back face side of said semiconductor substrate; and
a means for applying a voltage to said solid-state image sensor,
said means applying to said conductive material layer a positive or negative potential capable of extracting minority carriers.

(Claim 6)

A solid-state image pickup device according to claim 5 characterized such that said conductive material is embedded in a hole formed to penetrate from the back face side of said semiconductor region to the front face side of said semiconductor substrate.

(Claim 7)

A process for producing a solid-state image sensor constructed with an image pickup region, an optical black region, and a pad region, photoelectric conversion elements formed in the semiconductor substrate in said image pickup region and said optical black region, a wiring layer formed in the insulating layer disposed on the front face side of said semiconductor substrate, light being irradiated against said photoelectric elements from the back face side of said semiconductor substrate, said process for producing a solid-state image sensor being characterized by having

- a step of forming a semiconductor region in said semiconductor substrate,
- a step of forming photoelectric conversion elements in said semiconductor region,
- a step of forming wiring layers and an insulating layer covering said wiring layers while forming an electrode layer in said pad region to be covered by said insulating layer,
- a step of simultaneously forming an opening reaching said electrode layer in said pad region and a hole reaching said wiring layer penetrating said semiconductor region, and
- a step of embedding a metal material film in said hole.

(Detailed Explanation of the Invention)

(Field of the Invention)

(0001)

The present invention relates to solid-state image sensors, solid-state image pickup devices, and processes for producing solid-state image sensors.

(Background Art)

(0002)

Conventional solid-state image sensors are constructed with photoelectric conversion elements, an electrode layer, such as a readout electrode, and a color filter or on-chip lens which are formed on the front face side of the semiconductor substrate to capture images by allowing light to enter from the front face side.

(0003)

In a solid-state image sensor having such a construction, the minority carriers generated in the photoelectric conversion elements are extracted through the semiconductor well region formed at the periphery of the photoelectric conversion elements, for example, by allowing the region to achieve the ground potential via the wiring disposed from the front face side of the semiconductor substrate (single crystal silicon layer), i.e., the front face side of the semiconductor well region.

A potential gradient is formed in the photoelectric conversion elements so that the minority carriers generated in the photoelectric conversion elements naturally flow into the semiconductor well region.

(0004)

Incidentally, in the case of a solid-state image sensor having such a construction (the so-called surface irradiation type), the incident light is absorbed or reflected by the electrode layer or the like disposed on the front face side, giving rise to problems, such as reduced photoelectric conversion efficiency and reduced sensitivity with respect to incident light.

(0005)

Accordingly, in recent years, as a construction to solve these problems, a so-called backside irradiation type solid-state image sensor has been introduced to increase the aperture ratio for photoreception and suppress absorption or reflection of incident light by forming an electrode layer, such as a readout electrode, on the front face side of the semiconductor substrate while forming a color filter or on-chip lens on the back face side of the semiconductor substrate to capture images by allowing light to enter from the back face side of the semiconductor substrate (see, for example, Patent Document 1).

(0006)

(Patent Document 1) Japanese Unexamined Patent Application Publication No. 2003-031785

(Disclosure of the Invention)

(Problems to be Solved by the Invention)

(0007)

Incidentally, the thickness of the semiconductor substrate (single crystal silicon layer) in a backside irradiation type solid-state image sensor having such a construction is thin, about several μ (for example, 5 μ), as compared to a surface irradiation type, the resistance within the single crystal silicon layer is high.

(0008)

However, with a backside irradiation type solid-state image sensor, if the minority carriers generated in the photoelectric conversion elements were extracted using the same construction as that of a surface irradiation type solid-state image sensor described above, i.e., if the semiconductor well region formed at the periphery of the photoelectric conversion elements were grounded via the wiring disposed from the front face side of the single crystal silicon layer as discussed above, the following problems would result.

(0009)

Among the light entering the photoelectric conversion elements from the back face side of the single crystal silicon layer, for example, the holes generated by long wavelength light (infrared light) reaching the deep regions of the photoelectric conversion elements (front face side) would flow into the semiconductor well region to be readily extracted from the front face side of the single crystal silicon layer via the wiring.

On the other hand, in the case of the holes generated by short wavelength light (ultraviolet light) reaching only the back face side of the photoelectric conversion elements, for example, the holes flowing into the semiconductor well region must be moved from the back face side to the front face side of the semiconductor well region. The high resistance in the semiconductor well region would affect this, inhibiting the extraction.

In this case, holes gradually accumulate in the semiconductor well region, extending the residence time of the holes in the semiconductor well region. This inhibits the flow of holes from the photoelectric conversion elements into the semiconductor well region, allowing the holes to easily accumulate in the photoelectric conversion elements. This affects and weakens the electric field being applied to the photoelectric conversion elements, making it impossible for the majority carriers, i.e., electrons (signal charges), accumulated in the photoelectric conversion elements to be correctly read out.

(0010)

This does not allow the saturation charge quantity (Q_s) in the photoelectric conversion elements to remain constant, causing the occurrences of transient phenomena, such as time-dependent property changes and reduced sensitivity.

(0011)

In view of the above problems, the invention provides a solid-state image sensor, a solid-state image pickup device, and a process for producing the solid-state image sensor capable of allowing the minority carriers generated in the photoelectric conversion elements to be easily extracted.

(Means for Solving the Problems)

(0012)

The solid-state image sensor according to the invention comprises photoelectric conversion elements formed in a semiconductor substrate, and wiring layers formed in the insulating layer disposed on the front face side of the semiconductor substrate, light being irradiated against the photoelectric conversion elements from the back face side of the semiconductor substrate, wherein the solid-state image sensor is constructed with a semiconductor region formed in the semiconductor substrate at the periphery of the photoelectric conversion elements, and a conductive material layer formed at least in one section of the semiconductor region from the back face side of the semiconductor substrate.

(0013)

According to the solid-state image sensor of the invention described above, since a semiconductor region is formed in the semiconductor substrate at the periphery of the photoelectric conversion elements, and a conductive material layer is formed at least in one section of the semiconductor region (e.g., a semiconductor well region or an element separation region) from the back face side of the semiconductor substrate, the minority carriers generated in the photoelectric conversion elements on the back face side can be extracted via the conductive material layer formed in the semiconductor region. When constructed, for example, to apply the ground potential, or a positive or negative potential capable of

extracting minority carriers, to the conductive material layer using an externally disposed voltage application means, the minority carriers can easily be extracted.

(0014)

The solid-state image pickup device according to the invention comprises a solid-state image sensor having photoelectric conversion elements formed in a semiconductor substrate, wiring layers formed in the insulating layer disposed on the front face side of the semiconductor substrate, light being irradiated against said photoelectric conversion elements from the back face side of said semiconductor substrate, a semiconductor region formed in the semiconductor substrate at the periphery of the photoelectric conversion elements, and a conductive material layer formed at least in one section of the semiconductor region from the back face side of the semiconductor substrate; and a means for applying a voltage to the solid-state image sensor, the means applying the ground potential to the conductive material layer.

(0015)

According to the solid-state image pickup device of the invention described above, since it is constructed with a solid-state image sensor having a semiconductor region formed in the semiconductor substrate at the periphery of the photoelectric conversion elements and a conductive material layer formed at least in one section of the semiconductor region from the back face side of the semiconductor substrate, and a means for applying a voltage to the solid-state image sensor, which applies the ground potential to the conductive material layer, the minority carriers generated in the photoelectric conversion elements can easily be extracted via the conductive material layer formed in the semiconductor region. This can prevent the accumulation of minority carriers in the photoelectric conversion elements. Since it is constructed to apply the ground potential, minority carriers can be extracted with a simplified structure.

(0016)

The solid-state image pickup device according to the invention comprises a solid-state image sensor having photoelectric conversion elements formed in a semiconductor substrate, wiring layers formed in the insulating layer disposed on the front face side of the semiconductor substrate, light being irradiated against said photoelectric conversion elements from the back face side of said semiconductor substrate, a semiconductor region formed in the semiconductor substrate at the periphery of the photoelectric conversion elements, and a conductive material layer formed at least in one section of the semiconductor region from the back face side of the semiconductor substrate; and a means for applying a voltage to the solid-state image sensor, wherein a positive or negative potential capable of extracting minority carriers is applied by this means to the conductive material layer.

(0017)

According to the solid-state image pickup device of the invention, since it is constructed with a solid-state image sensor having a semiconductor region formed in the semiconductor substrate at the periphery of the photoelectric conversion elements and a conductive material layer formed at least in one section of the semiconductor region from the back face side of the semiconductor substrate, and a means for applying a voltage to the solid-state image sensor, which applies a positive or negative potential capable of extracting minority carriers to the conductive material layer, the minority carriers generated in the photoelectric conversion elements can easily be extracted via the conductive material layer formed in the semiconductor region. This can prevent the accumulation of minority carriers in the photoelectric conversion elements. Since it is constructed to apply a positive or negative potential capable of extracting minority carriers, minority carriers can be efficiently extracted by controlling the voltage.

(0018)

The solid-state image sensor production process according to the invention is a process for producing a solid-state image sensor having an image pickup region, an optical black region, and a pad region, photoelectric conversion elements formed in the semiconductor substrate in the image pickup region and the optical black region, wiring layers formed in the insulating layer disposed on the front face side of the semiconductor substrate, light being irradiated against the photoelectric elements from the back face side of the semiconductor substrate, wherein the production process has a step of forming a semiconductor region in the semiconductor substrate, a step of forming photoelectric conversion elements in the semiconductor region, a step of forming wiring layers and an insulating layer covering the wiring layers while forming an electrode layer in the pad region to be covered by the insulating layer, a step of simultaneously forming an opening reaching the electrode layer in the pad region and a hole reaching the

wiring layer penetrating the semiconductor region, and a step of embedding a metal material film in the hole.

(0019)

According to the solid-state image sensor production process of the invention, which has a step of forming a semiconductor region in the semiconductor substrate, a step of forming photoelectric conversion elements in the semiconductor region, a step of forming wiring layers and an insulating layer covering the wiring layers while forming an electrode layer in the pad region to be covered by the insulating layer, a step of simultaneously forming an opening reaching the electrode layer in the pad region and a hole reaching the wiring layer penetrating the semiconductor region, and a step of embedding a metal material film in the hole, performing the step of simultaneously forming an opening reaching the electrode layer in the pad region and a hole in the semiconductor region can form the opening in the pad region and the hole for embedding a conductive material layer at the same time. This can combine the step of forming a resist mask for forming an opening and the step of forming a resist mask for forming a hole as one step.

(Effect of the Invention)

(0020)

According to the solid-state image sensor and the solid-state image pickup device of the invention, accumulation of minority carriers in the photoelectric conversion elements can be prevented, always maintaining a constant saturation signal quantity within the photoelectric conversion elements.

This can suppress the transient phenomena from occurring and suppress the degradation of sensitivity, enabling the production of, for example, a solid-state image sensor and a solid-state image pickup device capable of handling a video over an extended period of time.

This can thus achieve a highly reliable, high performance solid-state image sensor and a solid-state image pickup device.

(0021)

According to the process for producing the solid-state image sensor of the invention, the resist mask formation step can be simplified, reducing the manufacturing steps for the solid-state image sensor.

(Best Mode for Carrying Out the Invention)

(0022)

Embodiments of the invention will be explained below with reference to the drawings.

(0023)

First, as a first embodiment of the invention, the construction of a backside irradiation type solid-state image sensor, for example, a CMOS type solid-state image sensor, will be explained with reference to FIGS. 1 and 2.

FIG. 1 is a schematic plan view of a backside irradiation type solid-state image sensor, for example, a CMOS type solid-state image sensor. FIG. 2 is an enlarged sectional view along line X-X indicated in FIG. 1.

(0024)

The CMOS type solid-state image sensor 1 comprises an image pickup region 41 in which pixels are arranged in a matrix, an optical black region 42 formed at the periphery of the image pickup region 41, and a pad region 43 formed at the periphery of the optical black region 42.

The optical black region 42 is constructed with the pixels for dark current correction arranged at the periphery of the pixels in the image pickup region 41, and a principle face side of the pixels are covered with a light shielding film. Noise, such as dark current, is removed by correcting the signals output by the image pickup region 41 using the signals output by the optical black region 42 as a reference. The pad region 43 is where pads to be connected to external wiring, for example, are disposed. In addition to the image pickup region 41 and the optical black region 42, a peripheral circuit region, not shown, made of a transistor or the like is formed.

(0025)

In the image pickup region 41, as shown in FIG. 2, photoelectric conversion elements 7 comprising N-type semiconductor regions are formed in unit pixel regions divided by the element separation regions 5 formed in the semiconductor substrate (e.g., single crystal silicon layer) 4. The photoelectric conversion elements 7 is each formed with a charge accumulation region 8 comprising an N-type

semiconductor region, and a positive charge accumulation region 9 comprising a high concentration P-type semiconductor region.

(0026)

On one principal face side of the single crystal silicon layer 4, i.e., the back face side (upper side in the figure), a color filter 11 is formed via an antireflective film (oxide film and nitride film) 10, and on-chip lenses 12 are formed on the color filter 11 at the positions corresponding to the photoelectric conversion elements 7.

On the other principal face side of the single crystal silicon layer 4, i.e., the front face side (lower side in the figure), MOS type transistors Tr1, for example, are formed in correspondence to the photoelectric conversion elements 7, and multilayer wiring layers 13 are formed on the transistors Tr1.

(0027)

In the image pickup region 41, although not shown in the figure, floating diffusion sections are formed to convert the signal charges accumulated in the photoelectric conversion regions into voltages. Furthermore, output sections (output amplifiers) for outputting the voltages converted by the floating diffusion sections, and reset gate sections to discharge the signal charges accumulated in the floating diffusion sections are formed. These floating diffusion sections, output sections, and reset gate sections are formed per photoelectric conversion element.

(0028)

The MOS type transistor Tr1 comprises a gate electrode 14 formed via a gate insulating film on the front face side between a pair of source and drain regions formed in the single crystal silicon layer 4. The source region, drain region, and channel region of the transistor Tr1 are formed at prescribed positions within the single crystal silicon layer 14, although not shown in the figure.

(0029)

The wiring layer 13 has four layers of wiring.

More specifically, it is formed, in the insulating layer 15 formed on the front face side of the single crystal silicon layer 4, with wiring 131 which is the first layer, wiring 132 which is the second layer formed on the first layer wiring 131 via the insulating layer 15, wiring 133 which is the third layer formed on the second layer wiring 132 via the insulating layer 15, and wiring 134 which is the fourth layer formed on the third layer wiring 133 via the insulating layer 15.

(0030)

On the insulating layer 15, a flattening film 16 is formed, onto which a support substrate 18 is pasted via an adhesive layer 17.

(0031)

In the optical black region 42, a light shielding film 19 is formed on the back face side of the single crystal silicon layer 4 via the antireflective film 10. Even in the optical black region 42, photoelectric conversion elements 7, transistors Tr1, and wiring layers 26 are formed in the similar manner as in the case of the image pickup region 41.

The light shielding film 19 is formed so as to cover all the photoelectric conversion elements formed in the optical black region 42.

(0032)

In the peripheral section of the optical black region 42, a semiconductor well region 6 comprising a P-type semiconductor region is formed. The semiconductor well region 6 is formed at least in the image pickup region 41 and the optical black region 42 overall.

(0033)

In the pad region 43, an electrode layer 20 is formed in the insulating layer 15 on the front face side of the single crystal silicon layer 4 on the same plane as for the wiring 131 and the wiring 26 of the image pickup region 41 and the optical black region 42, respectively, and an opening 21 reaching the electrode layer 20 is formed from the back face side of the single crystal silicon layer 4. On the inner wall of the opening 21, an insulating film is formed although not shown in the figure.

(0034)

A potential gradient is formed in the photoelectric conversion elements 7 to allow the minority carriers generated in the photoelectric conversion elements 7 to naturally flow into the semiconductor well region 6.

(0035)

In the CMOS type solid-state image sensor 1 constructed as above, light for imaging enters from the back face side of the single crystal silicon layer 3.

(0036)

In this embodiment, in particular, a conductive material layer 25 is formed in the semiconductor well region 6 located in the peripheral section of the optical black region 42. The conductive material layer 25 is formed by being embedded in the hole 27 created to penetrate from the back face side to the front face side in the semiconductor well region 6 reaching the wiring 26 formed in the insulating layer 15 on the front face side of the semiconductor well region 6.

(0037)

For the conductive material layer 25, a conductive material, for example, metal materials, such as AlCu, Al, AlSi, or W can be used. When such a metal material is used, the resistance of the conductive material layer 25 will be lower than that within the semiconductor well region 6.

(0038)

The conductive material layer 25 is constructed such that a voltage is applied thereto using an externally disposed voltage application means not shown in the figure. In other words, a solid-state image pickup device is constructed with the solid-state image sensor 1 having the above described construction and a voltage application means disposed outside the solid-state image sensor 1.

The voltage application means is disposed, for example, on the outside or the inside of the solid-state image sensor 1, and comprises a voltage control circuit for generating a voltage to be applied to the conductive material layer 25 from the voltage from the power supply, and wiring (wire and the wiring layer within the solid-state image sensor 1) for applying the voltage generated by the voltage control circuit to the conductive material layer 25.

(0039)

As a solid-state image pickup device having such a construction, in this embodiment, the means for applying a voltage to the conductive material layer 25 is constructed by using the wiring 26 formed within the insulating layer 15 on the front face side of the single crystal silicon layer 4, and the electrode layer 20 of the pad region 43 connected to the wiring 26. It is adapted to apply a voltage to the conductive material layer 25 via the electrode layer 20. The wiring 26 and the electrode layer 20 are connected in the region not shown in the figure.

(0040)

As an embodiment of the solid-state image pickup device described above, the ground voltage (0 V) is applied to the conductive material layer 25 by the voltage application means.

(0041)

When the solid-state image pickup device is constructed to apply the ground voltage to the conductive material layer 25 as described above, the minority carriers (holes) generated in the photoelectric conversion elements 7 in the solid-state image sensor 1 can be easily extracted through the conductive material layer 25 located in the semiconductor well region 6.

At this time, since the conductive material layer 25 is formed to penetrate from the back face side to the front face side of the semiconductor well region 6, and is formed with a metal material, as described earlier, there is no difficulty in extracting the holes generated particularly from short wavelength incident light on the back face side of the photoelectric conversion elements, i.e., the holes can be easily extracted by the conductive material layer 26 which has lower resistance than that of the semiconductor well region 6.

(0042)

Accordingly, in the solid-state image sensor 1, accumulation of holes within the photoelectric conversion elements 7 can be prevented, and a constant saturation signal quantity can always be maintained in the photoelectric conversion elements 7.

Since this can suppress the saturation charge quantity (Qs) from fluctuating, maintain a constant saturation charge quantity (Qs) in the photoelectric conversion elements 7, for example, the time-dependent problems, such as color changes occurring over time, can be solved. This can also prevent the degradation of sensitivity.

(0043)

Grounding the conductive material layer 25 allows for the extraction of the holes with a simplified construction.

(0044)

Incidentally, the construction that also grounds the light shielding film formed in the optical black region has been contemplated, and in this case, for example, wiring for grounding was connected to the light shielding film from the outside after forming the light shielding film.

In the solid-state image sensor 1 in this embodiment, in contrast, the conductive material layer 25 is formed to reach the grounding wiring 26 formed in the insulating layer 15, and thus the light shielding film 19 is also grounded through the conductive material layer 25 and the wiring 26. This eliminates the need for connecting grounding wiring to the light shielding film 19.

(0045)

Moreover, as another embodiment of the solid-state image pickup device described above, it can be constructed to have the voltage application means apply a positive or negative voltage capable of extracting the minority carriers to the conductive material layer 25.

(0046)

In the solid-state image sensor 1 shown in FIGS. 1 and 2, the photoelectric conversion elements 7 are formed with N-type semiconductor regions, and the semiconductor well region 6 is formed with a P-type semiconductor region. Accordingly, the voltage application means applies a negative voltage to the conductive material layer 25. The negative voltage is set at a level which would not affect the properties of the solid-state image sensor 1, for example, a lower voltage than the readout voltage.

(0047)

When the solid-state image pickup device is constructed to apply a negative voltage to the conductive material layer 25, in addition to achieving the same effect as in the case of applying the ground voltage, minority carriers can be efficiently extracted by controlling the voltage.

(0048)

When using a solid-state image sensor constructed with photoelectric conversion elements comprising P-type semiconductor regions, and a semiconductor well region comprising an N-type semiconductor region, the same effect as in the case of applying a negative voltage described above can be achieved by applying a positive voltage to the conductive material layer 25 formed in the semiconductor well region. It goes without saying that the positive voltage applied in this case is also of a level which would not affect the properties of the solid-state image sensor 1.

(0049)

Moreover, as another embodiment of the solid-state image pickup device described above, it can be constructed to apply the ground voltage or a negative voltage to the conductive material layer 25 from the back face side (upper side in FIG. 1) of the single crystal silicon layer 4.

More specifically, for example, a wire or the like is connected to the light shielding film 19 of the optical black region 42 to apply a voltage to the conductive material layer 25 via the light shielding film 19.

Even when the solid-state image pickup device is constructed to apply the ground voltage or a negative voltage to the conductive material layer 25 from the back face side of the single crystal silicon layer 4 described above, the same effect can result as in the case of applying the ground voltage or a negative voltage from the front face side (lower side in FIG. 1) of the single crystal silicon layer 4.

(0050)

This construction where a voltage is applied from the back face side of the single crystal silicon layer 4 can be applied to the solid-state image sensors described later in which a conductive material layer is formed in an element separation region in the optical black region, or the conductive material layer is formed partway from the back face side interface of the semiconductor well region. In other words, it can be applied to a solid-state image sensor having a construction other than those in which a conductive material layer 25 is formed in the section on the back face side of the single crystal silicon layer 4 where the formation of voltage applying wiring and electrode is difficult as in the case of the image pickup region 41 where the color filter 11 and the on-chip lenses 12 are formed on the back face side of the single crystal silicon layer 4.

(0051)

As explained above, in the solid-state image pickup device of this embodiment, because the conductive material layer 25 is formed in the semiconductor well region 6 in the peripheral section of the optical black region 42, and the ground voltage or a voltage capable of extracting minority carriers (positive or negative voltage) is applied to the conductive material layer 25 by the voltage application means from the front or back face side of the single crystal silicon layer, accumulation of minority carriers within the photoelectric conversion elements 7 can be prevented, and a constant saturation signal quantity can always be maintained within the photoelectric conversion elements.

(0052)

When the solid-state image pickup device is constructed to apply a voltage to the conductive material layer 25 from the back face side of the single crystal silicon layer 4, the conductive material layer 25 may not necessarily be connected to the wiring 26 on the front face side as shown in FIG. 2. For example, the conductive material layer 25 may be formed from the back face side interface to the front face side interface of the single crystal silicon layer 4. Even with this construction, holes can be extracted from the front face side and the back face side of the semiconductor well region 6 via the conductive material layer 25 and the light shielding film 19.

(0053)

Next, the process for producing the solid-state image sensor 1 shown in FIGS. 1 and 2 will be explained with reference to FIGS. 3-6. FIGS. 3-6 are schematic sectional views of the image pickup region 41, the optical black region 42, and the vicinity of the optical black region 42 of the solid-state image sensor 1 shown in FIG. 1. The sections corresponding to those in FIGS. 1 and 2 are denoted with the same reference numerals.

The production steps described below will be performed by using the alignment markings as a reference, which are formed to penetrate the single crystal silicon layer at the predetermined positions although not shown in the figure.

(0054)

First, as shown in FIG. 3A, an SOI substrate 30 is prepared by forming a single crystal silicon layer 4 on a silicon substrate 2 via an embedded oxide film (the so-called BOX layer) 3, for example.

The thicknesses of the embedded oxide film 3 and the single crystal silicon layer 4 can be set as desired.

(0055)

Next, in the image pickup region 41 to the optical black region 42, a P-type semiconductor well region 6 is formed in the single crystal silicon layer 4 by using a known technique, followed by forming element separation regions 5 at prescribed positions of the semiconductor well region 6 by using a known technique. Then, N-type semiconductor regions (charge accumulation regions) 8 which form the photoelectric conversion elements are formed at prescribed positions within the element formation regions divided by the element separation regions 5 by using a known technique (see FIG. 3B).

(0056)

Next, as shown in FIG. 3C, on the single crystal silicon layer 4 in the image pickup region 41 and the optical black region 42, MOS type transistors Tr1 each comprising a gate electrode 14 and a pair of source and drain regions are formed via an insulating layer.

The channel, source, and drain regions of the transistors Tr1 are not shown in the figure, but are formed at prescribed positions within the single crystal silicon layer 4.

(0057)

Then, as shown in FIG. 4D, multilayer wiring layers 13 are formed via the insulating layer 15 on the single crystal silicon layer 4.

(0058)

More specifically, after performing a flattening treatment by forming an insulating layer 15 on the single crystal silicon layer 4, a first layer wiring 131 is formed to a prescribed pattern.

Then, after performing a flattening treatment by forming an insulating layer 15 again across the entire surface, including the first layer wiring 131, a second layer wiring 132 is formed to a prescribed pattern.

The same step is repeated to achieve a prescribed number of layers.

The example shown in FIG. 4D has four layers to make up a wiring layer 13. If more layers than four layers are formed, the same step is repeated.

Moreover, a flattening film made of an SiN film or SiON film, for example, is formed on the insulating layer 15.

(0059)

In the step of forming the wiring 13, a grounding wiring 26 is formed to a prescribed pattern in the peripheral section of the optical black region 42 on the same plane as that for the first layer wiring 131 at the same time the wiring 131 is formed in the image pickup region 41 and the optical black region 42. Moreover, although not shown in the figure, in the pad region, an electrode layer is formed to a prescribed pattern on the same plane as that for the wiring 131 and the wiring 26.

(0060)

Next, as shown in FIG. 4E, the flattening film is coated with an adhesive layer 17, and the support substrate 18 is pasted thereto. The support substrate 18 is pasted to the front face side of the SOI substrate 30 in order to ensure the mechanical strength required when the SOI substrate 30 is thinned down in the step described later.

(0061)

Next, the SOI substrate 30 is flipped upside down, and the silicon substrate 2 is now on top. Then, by sequentially removing the silicone substrate 2 and the embedded oxide film 3, the single crystal silicon layer 4 of the SOI substrate 30 is exposed as shown in FIG. 4F.

Then, on the back face side of the charge accumulation regions 8, positive charge accumulation regions 9 comprising high purity P-type semiconductor regions are formed by using known techniques (e.g., forming a thin oxide film on the upper face of the single crystal silicon layer 4, followed by resist mask formation and ion implantation). This thus forms photoelectric conversion elements 7. The step of forming positive charge accumulation regions 9 is not limited to that performed in the state shown in FIG. 4F, i.e., they can be formed in various other ways, such as forming them from the front face side of the single crystal silicon layer 4 as in the case of the charge accumulation regions 8.

(0062)

Next, as shown in FIG. 5G, an opening 21 reaching the electrode layer 20 is formed in the pad region 43 for connecting an external contact wiring to the electrode layer 20 embedded in the insulating layer 15 by sequentially etching off the single crystal silicon layer 4 and the insulating layer 15.

At this point, in this embodiment, a hole 27 reaching the wiring 26 is simultaneously formed in the semiconductor well region 6.

The electrode layer 20 of the pad region 43, as described above, is formed on the same plane as that for the wiring 131 and the wiring 26 of the image pickup region 41 and the optical black region, respectively. Accordingly, the hole 27 reaching the wiring 26 in the optical black region 42 can be created at the same time the opening 21 reaching the electrode layer 20 is created in the pad region 43.

(0063)

More specifically, in the state where the single crystal silicon layer 4 of the SOI substrate 30 is exposed (see FIG. 4F), an antireflective film is formed on the single crystal silicon layer 4, then a photoresist film is formed on the antireflective film, and then the resist mask having the pattern for forming the opening and the hole is formed by a known lithography process.

The hole 27 and the opening 21 can be formed at prescribed positions in the single crystal silicon layer in the optical black region 42 and the pad region 43, respectively, by etching off the single crystal silicon layer using the resist mask as a mask as shown in FIG. 5G.

(0064)

Then, a conductive material layer 25 is formed on the single crystal silicon layer 4, including the hole 27. Removing only the conductive material layer 25 formed on the surface of the single crystal silicon layer 4 results in the conductive material layer 25 embedded in the hole 27 as shown in FIG. 5H.

(0065)

Next, as shown in FIG. 6I, a light shielding film 19 is formed on the single crystal silicon layer 4 in the optical black region 42. During this step, the single crystal silicon layer 4 in the image pickup region 41 is covered with a mask. The light shielding film 19 is formed to cover up to the peripheral section of the optical black region 42.

(0066)

Subsequently, as shown in FIG. 6J, in the image pickup region 41, on-chip microlenses 12 are formed in the sections of the single crystal silicon layer 4 corresponding to the photoelectric conversion elements 7 via the color filter 11.

(0067)

The backside irradiation type CMOS solid-state image sensor 1 with the construction shown in FIGS. 1 and 2 can thus be produced.

(0068)

According to the production process described above, since the hole 27 for embedding the conductive material layer 25 is formed in the peripheral section of the optical black region 42 at the same time the hole 21 for connecting an external contact wiring to the electrode layer 20 is formed in the pad region 43, the step of forming a resist mask for the hole 27 and the step of forming a resist mask for the opening 21 can be performed in one step. This can simplify the resist mask formation step.

(0069)

In the production process explained above, moreover, the present invention was applied to the case of producing a solid-state image sensor 1 from a multilayer SOI substrate 30 where a single crystal silicon layer 4 was stacked on the silicon substrate 2 via an embedded oxide film 3. The present invention, however, is also applicable, for example, to the cases where the solid-state image sensor having the construction described above is formed from a single layer semiconductor substrate (single crystal silicon layer) having a small layer thickness.

(0070)

The production process described above showed the case of exposing the single crystal silicon layer 4 of the SOI substrate 30 by removing the silicon substrate 2 and the embedded oxide film 3 in the steps shown in FIGS. 4E-4F. However, the embedded oxide film 3 can be retained by removing only the silicon substrate 2.

(0071)

Next, another embodiment of the solid-state image sensor according to the invention will be explained.

In the solid-state image sensor 1 of the embodiment described above, the conductive material layer 25 was formed in the semiconductor well region 6 formed in the peripheral section of the optical black region 42 as shown in FIG. 2, whereas in the solid-state image sensor 31 in this embodiment, as shown in FIG. 7, the conductive material layer 25 is formed in an element separation region 5 comprising a P-type semiconductor region which separates adjacent photoelectric conversion elements 7 in the image pickup region 41.

The construction is otherwise the same as that of the solid-state image sensor 1 in the embodiment described above, including the materials used for the conductive material layer 25, and thus redundant explanations will be omitted.

(0072)

In cases where a solid-state image pickup device is constructed by employing the solid-state image sensor 31 in which a conductive material layer 25 is formed in an element separation region 5 of the image pickup region 41, a voltage application means is constructed to apply a voltage to the conductive material layer 25 from the front face side of the single crystal silicon layer 4 because the color filter 11 and the on-chip lenses 12 are formed on the back face side of the single crystal silicon layer 4 of the image pickup region 41. As described above, it is constructed so that the ground voltage or a voltage capable of extracting minority carriers is applied by the voltage application means.

In other words, as described above, it is constructed to apply a voltage to the conductive material layer 25 by an externally disposed voltage application means via the wiring 26, and the electrode layer 20 of the pad region 43, for example.

(0073)

In cases where a solid-state image pickup device is constructed by employing the solid-state image sensor 31 in which a conductive material layer 25 is formed in an element separation region 5 of the image pickup region 41, as discussed earlier, accumulation of holes within the photoelectric conversion elements 7 in the solid-state image sensor 31 can be prevented, always maintaining a constant saturation signal quantity within the photoelectric conversion elements 7. This suppresses the saturation charge

quantity (Q_s) from fluctuating, maintaining a constant saturation charge quantity (Q_s), thereby solving the time-dependent problems, such as color changes occurring over time. This also prevents the sensitivity from degrading.

(0074)

Yet another embodiment of the solid-state image sensor of the invention will be explained next.

In the solid-state image sensor 32 of this embodiment, a conductive material layer 25 is formed in an element separation region comprising a P-type semiconductor region which separates adjacent photoelectric conversion elements 7 in the optical black region 42.

The construction is otherwise the same as that of the solid-state image sensor 1 in the embodiment described above, including the materials used for the conductive material layer 25, and thus redundant explanations will be omitted.

(0075)

In cases where a solid-state image pickup device is constructed by employing the solid-state image sensor 32 in which a conductive material layer 25 is formed in an element separation region 5 of the optical black region 42, a voltage application means is constructed to apply a voltage to the conductive material layer 25 from the front face side of the single crystal silicon layer 4. As described above, it is constructed so that the ground voltage or a voltage capable of extracting minority carriers is applied by the voltage application means.

In other words, as described above, it is constructed to apply a voltage to the conductive material layer 25 by an externally disposed voltage application means via the wiring 26, and the electrode layer 20 of the pad region 43, for example.

In the case of a solid-state image pickup device constructed in this way, the voltage application means can alternatively be constructed to apply a voltage to the conductive material layer 25 from the back face side of the single crystal silicon layer 4, not from the front face side of the single crystal silicon layer 4. In this case, as described above, a wire is connected to the light shielding film 19 of the optical black region 42 so that a voltage can be applied to the conductive material layer 25 via the light shielding film 19, for example.

(0076)

Even when a solid-state image pickup device is constructed by employing the solid-state image sensor 32 in which a conductive material layer 25 is formed in an element separation region 5 of the optical black region 42, accumulation of holes within the photoelectric conversion elements 7 in the solid-state image sensor 32 can be prevented, always maintaining a constant saturation signal quantity within the photoelectric conversion elements 7. This suppresses the saturation charge quantity (Q_s) from fluctuating, maintaining a constant saturation charge quantity (Q_s), thereby solving the time-dependent problems, such as color changes occurring over time. This also prevents the sensitivity from degrading.

(0077)

When a conductive material layer 25 is formed in an element separation region 5 as shown in FIGS. 7 or 8, the conductive material layer 25 can also be formed in each of the plural element separation regions 5 that separate the photoelectric conversion elements 7.

(0078)

In each of the embodiments described above, the conductive material layer 25 was formed to penetrate from the back face side to the front face side of the semiconductor well region 6, but the conductive material layer 25, for example, can be formed partway from the interface of the back face side of the semiconductor well region 6 as shown in FIG. 9. FIG. 9 is an enlarged sectional view of the vicinity of the conductive material layer 25.

When forming a conductive material layer 25 having such a construction, the hole 27 is formed under the conditions set so as not to reach the front face side of the single crystal silicon layer 4 in the step for forming a hole 27 shown in FIG. 5G.

(0079)

When constructing a solid state image pickup device using such a solid image sensor, since the conductive material layer 25 does not reach the front face side of the single crystal silicon layer 4, it cannot be adapted to apply a voltage to the front face side of the single crystal silicon layer 4. Thus, it is constructed to apply a voltage to the back face side of the single crystal silicon layer 4.

(0080)

Even when a solid-state image pickup device is constructed by employing the solid-state image sensor in which a conductive material layer 25 is formed partway from the back face side of the semiconductor well region 6, accumulation of holes within the photoelectric conversion elements 7 in the solid-state image sensor can be prevented, always maintaining a constant saturation signal quantity within the photoelectric conversion elements 7. This suppresses the saturation charge quantity (Qs) from fluctuating, maintaining a constant saturation charge quantity (Qs), thereby solving the time-dependent problems, such as color changes occurring over time. This also prevents the sensitivity from degrading.

(0081)

In the embodiments described above, the instances in which the semiconductor well region 6 and the element separation regions 5 were formed in the groundable regions were explained, but in cases where the semiconductor well region 6 and the element separation regions 5 are formed in the regions that cannot be grounded, for example, insulation is provided by forming, for example, an insulating film or a PN junction region at the borders between the regions 5 or 6 and the conductive material layer 25.

This, for example, can prevent the peripheral circuit section or the like formed at the periphery of the image pickup region 41 or the optical black region 42 from being affected.

(0082)

In the embodiments described above, moreover, a metal material was used as the conductive material layer 25, but the materials for the conductive material layer 25 are not limited to the aforementioned metal materials, so long as they are highly conductive materials. Since metal materials have low resistance as described above, they can easily extract minority carriers.

When a metal material is used, for example, the metal material embedded in the hole 27 could diffuse into the single crystal silicon layer 4. Accordingly, it can be constructed with a barrier metal film 33 on the lateral wall of the hole 27, as shown in FIG. 10, to prevent the metal from diffusing.

(0083)

In the embodiments described above, a single conductive material layer 25 was formed in the semiconductor well region 6 or the element separation region 5, but plural conductive material layers 25 may be formed.

(0084)

The invention is not limited to the embodiments described above, and various other constructions can be achieved without departing from the scope of the invention.

(Brief Explanation of the Drawings)

(0085)

FIG. 1 is a schematic representation (plan view) of the solid-state image sensor according to one example of the invention.

FIG. 2 is a schematic sectional view (enlarged view) of the image pickup region and the optical black region in FIG. 1.

FIGS. 3A-C are production step diagrams (part 1) showing the process for producing the solid-state image sensor shown in FIGS. 1 and 2.

FIGS. 4D-F are production step diagrams (part 2) showing the process for producing the solid-state image sensor shown in FIGS. 1 and 2.

FIGS. 5G-H are production step diagrams (part 3) showing the process for producing the solid-state image sensor shown in FIGS. 1 and 2.

FIGS. 6I-J are production step diagrams (part 4) showing the process for producing the solid-state image sensor shown in FIGS. 1 and 2.

FIG. 7 is a schematic sectional view (enlarged view) of another embodiment of the solid-state image sensor according to one embodiment of the invention.

FIG. 8 is a schematic sectional view (enlarged view) of yet another embodiment of the solid-state image sensor according to one embodiment of the invention.

FIG. 9 is a schematic sectional view of yet another embodiment of the solid-state image sensor according to one embodiment of the invention.

FIG. 10 is an enlarged sectional view of another embodiment of the conductive material layer.

(Explanation of Reference Numerals)

(0086)

1, 31, 32 --- solid-state image sensor, 2 --- silicon substrate, 3 --- embedded oxide film, 4 --- single crystal silicon layer (semiconductor substrate), 5 --- element separation region, 6 --- P-type semiconductor well region, 7 --- photoelectric conversion element, 8 --- charge accumulation region, 9 --- positive charge accumulation region, 10 --- antireflective film, 11 --- color filter, 12 --- on-chip lens, 13 (131, 132, 133) --- wiring layer, 14 --- gate electrode, 15 --- insulating layer, 16 --- flattening film, 17 --- adhesive layer, 18 --- support substrate, 19 --- light shielding film, 20 --- electrode layer, 21 --- opening, 25 --- conductive material layer, 26 --- wiring, 27 --- hole, 33 --- barrier metal film, 41 --- image pickup region, 42 --- optical black region, 43 --- pad region

FIG. 1

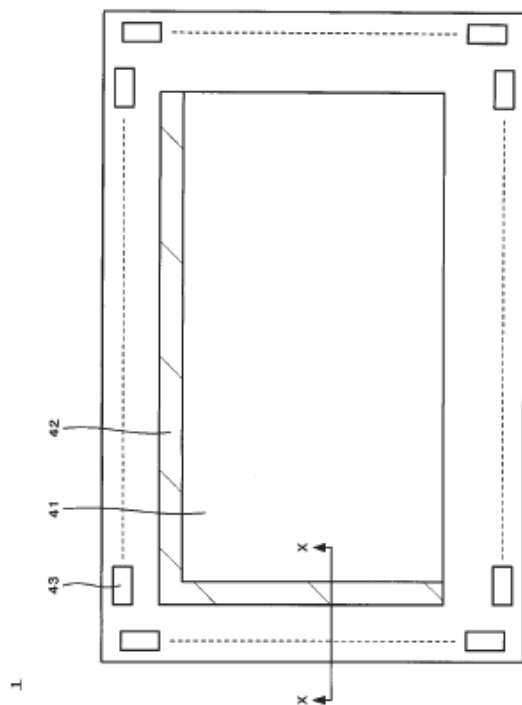


FIG. 2

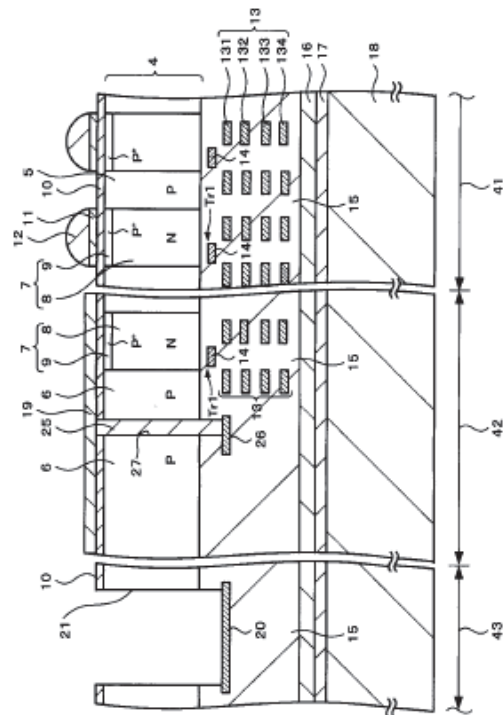


FIG. 3

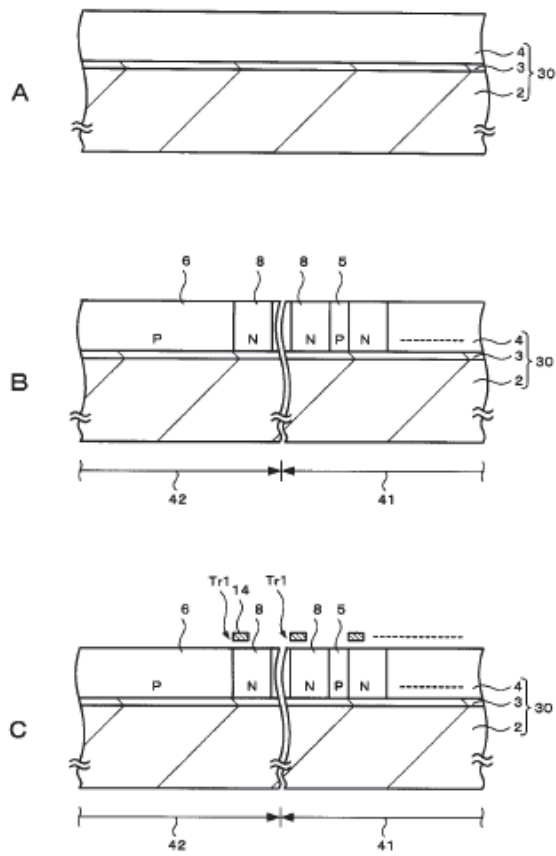


FIG. 4

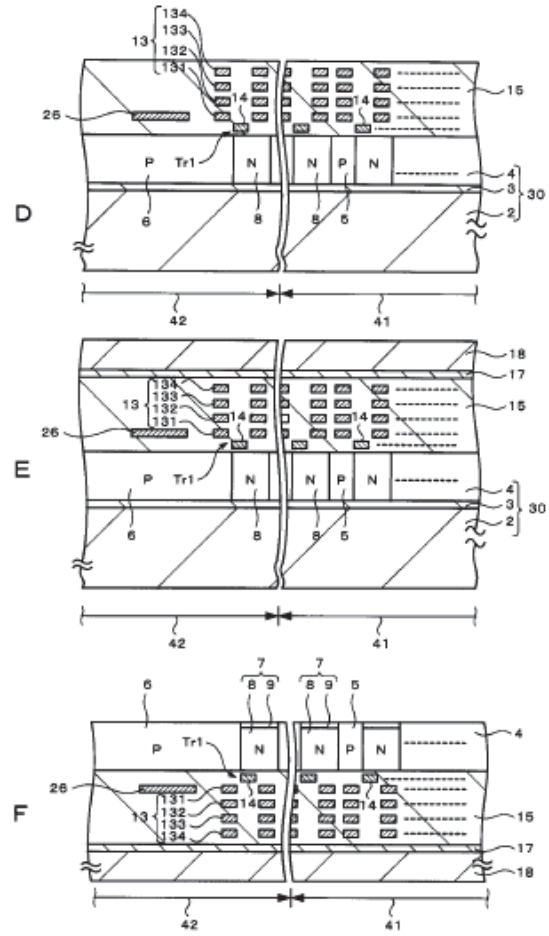


FIG. 5

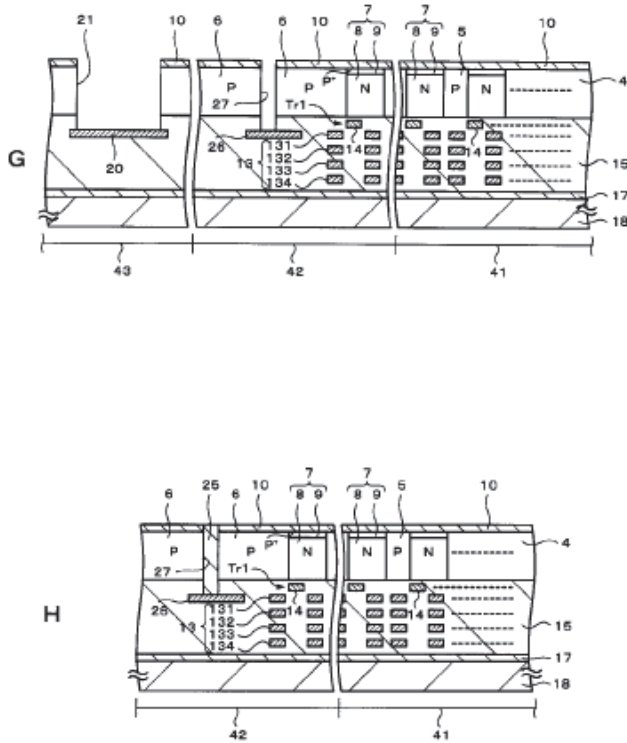


FIG. 6

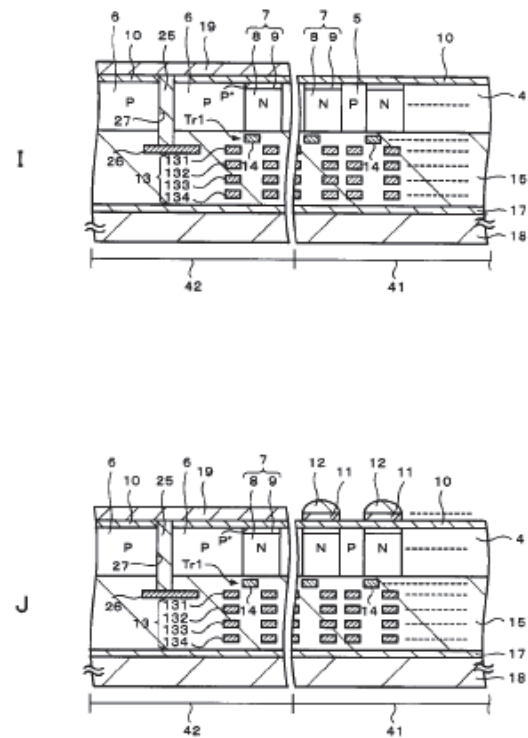


FIG. 7

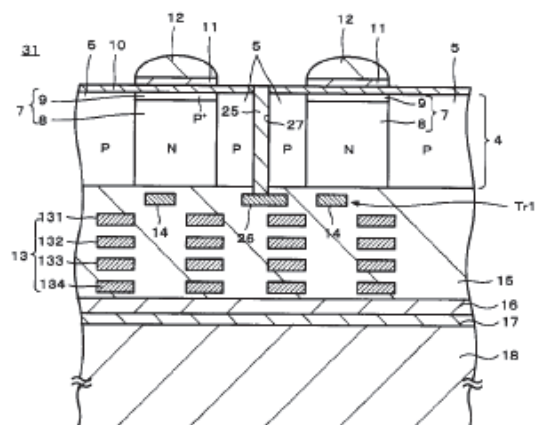


FIG. 8

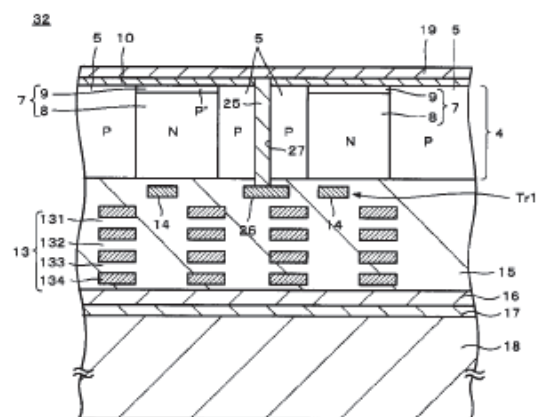


FIG. 9

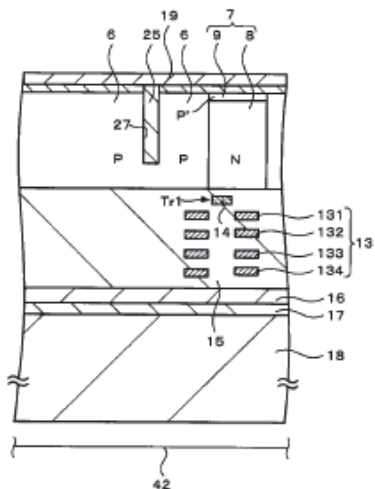
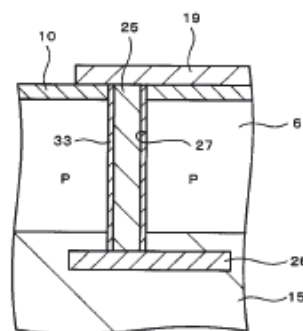


FIG. 10





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CERTIFICATION OF TRANSLATION

I, Asami Isomichi, hereby declare:

1. I am a Japanese language translator.
2. I have over 25 years experience translating technical, legal, and business documents from Japanese to English, and from English to Japanese.
3. I certify that the English translation of the document identified below is a true and correct translation, to the best of my knowledge and ability, of the original Japanese document:

- Japanese Unexamined Patent Application Publication No. 2006-032497

I hereby certify under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed this 7th day of March, 2016.

By: _____

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