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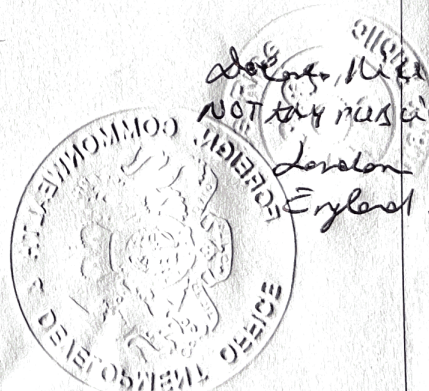
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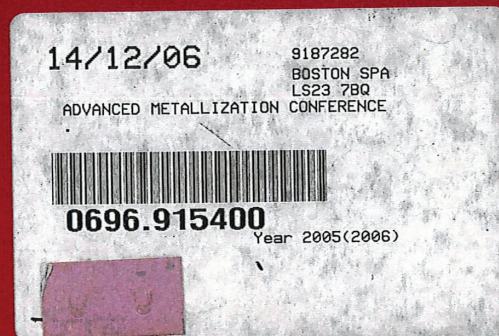
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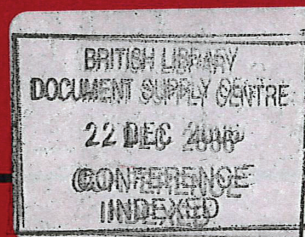


**Advanced Metallization
Conference 2005
(AMC 2005)**



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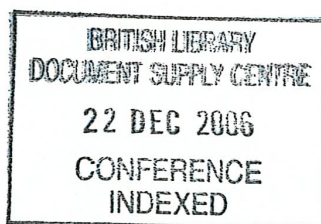


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**Advanced Metallization
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Optimization of Cu Interconnect Layers for CMOS Image Sensor Technology

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ABSTRACT

A 0.18 μm CMOS imager sensor technology is described that uses Cu interconnects. Copper wiring results in a thinner dielectric stack compared to Al wiring, which provides an improved angular response of the photodiode. However, the SiN capping layers on top of the Cu wires increase reflectivity, which can reduce the sensitivity of the photodiodes. A number of approaches are described for eliminating the SiN capping layers over the photodiodes, including a self-aligned CoWP passivation layer.

INTRODUCTION

CMOS image sensors are increasingly being used in consumer products instead of charge-coupled devices, because of lower power consumption, lower system cost, and the ability to randomly access image data [1]. Aluminum interconnects are generally used in image sensors because the technology uses relaxed ground rules; typically 0.18 μm or larger [2].

Copper interconnects have gained wide acceptance in the microelectronics industry, owing to improved resistivity and reliability compared to Al interconnects [3]. For image sensors, Cu interconnect technology again offers advantages. The pixel performance is improved in two ways: First, Cu interconnect technology improves the uniformity of the optical path by reducing the polishing of the interconnect dielectric [4]. Second, the reduction in metal thickness allows thinning of the optical path. As pixel size is reduced, the optical stack height critically determines the angle response of the detector. However, just as for the high-performance applications, introduction of Cu interconnects for an image sensor leads to unique challenges and specialized fabrication.

EXPERIMENT

CMOS imagers with Cu interconnects and associated test structures have been fabricated using a 0.18 μm foundry process [5]. The imagers have four levels of metal; M1 through M3 are Cu, with an undoped SiO_2 dielectric, and the last metal level is Al. The minimum M1 and M2 pitches are 0.44 and 0.56 μm , respectively, while the minimum via diameter is 0.28 μm . Changes to the base process have been made to (1) optimize the photodiode, (2) optimize the optical path through the dielectric stack, and (3) to add color filters and microlenses.

MICROLENSSES AND COLOR FILTERS

The CMOS imager consists of an array of pixels that detect the incident light. A commonly used pixel is the four transistor or "4T" cell (Fig. 1) [2,6]. To capture an image, the

photodiode is first reversed biased (set to V_{dd}) using the reset gate and transfer gate. When the shutter of the camera is opened, light that is incident on the photodiode will generate electron-hole pairs. To sense the charge in the photodiode, the transfer gate is turned on and the charge is moved to the floating diffusion. This changes the potential on the gate of the source-follower circuit, and the resulting signal is detected at the output of the pixel by turning on the row select transistor.

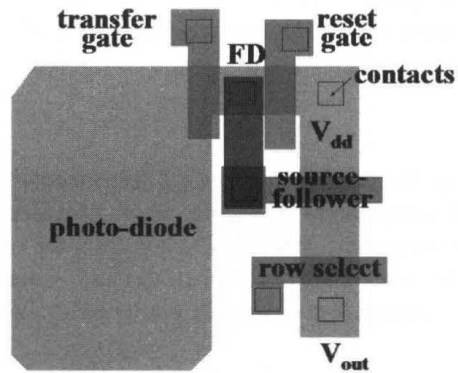


Fig. 1. Example of pixel layout for four-transistor CMOS imager [ref. 6]. Note that the photo-diode area is much smaller than the pixel area.

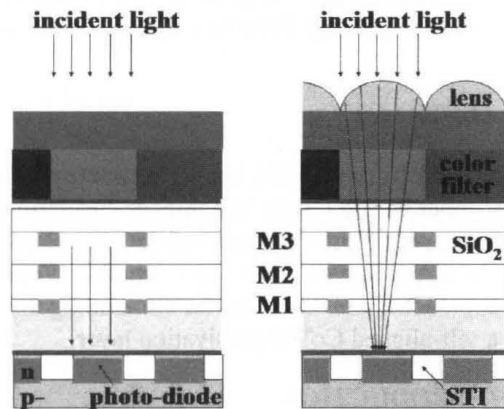


Fig. 2. Schematic of light collection with and without microlenses. By using microlenses, light that is not directly over the photo-diode can be captured, resulting in higher sensitivity.

The photo-diode area is much smaller than the total area of the pixel. Any light that is not directly above the photo-diode will not be collected, or may even be scattered to neighboring pixels by the wiring over the transistors, resulting in increased noise. To overcome this loss of sensitivity, microlenses are used to focus light on the photo-diodes (Fig. 2) [7,8]. The microlenses are fabricated from clear photoresist. After patterning, the resist is flowed to achieve the desired lens shape (Fig. 3). The quantum efficiency (i.e., the percentage of photo-generated carriers that are detected for each incoming photon) is greatly improved by using microlenses (Fig. 4).

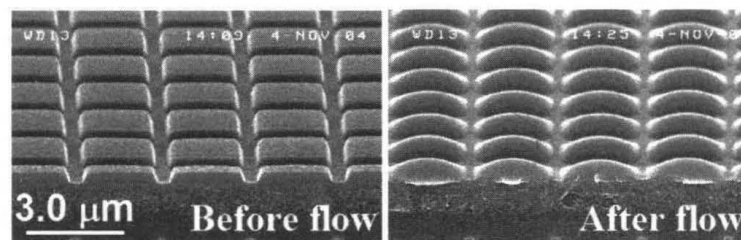


Fig. 3. Angled top-down SEMs of microlenses. Microlenses are formed using patterned photoresist and reflow.

Silicon-based image sensors are sensitive to light with wavelengths up to 1050 nm (Fig. 5) [9]. In order to capture color information from the broad bandwidth incident light, color filters are used so that each pixel captures mainly one color of light (i.e., red, green, or blue). The color filters consist of dyed photoresist that is arranged in alternating rows of either green and blue or green and red [10,11](Fig. 6). These are printed in three lithography steps, one for each color. There are twice as many “green pixels” (i.e. pixels with green color filters) as “red pixels” or “blue pixels”, because the human eye is more sensitive to green light than red or blue light. While the color filters reduce the light intensity from the other colors, they do not eliminate it. For example, the green pixel has considerable quantum efficiency at 480 nm, corresponding to blue light (Fig. 4). The high quality images that can be achieved with CMOS image sensors are largely due to the data processing by the logic circuits at the periphery of the array.

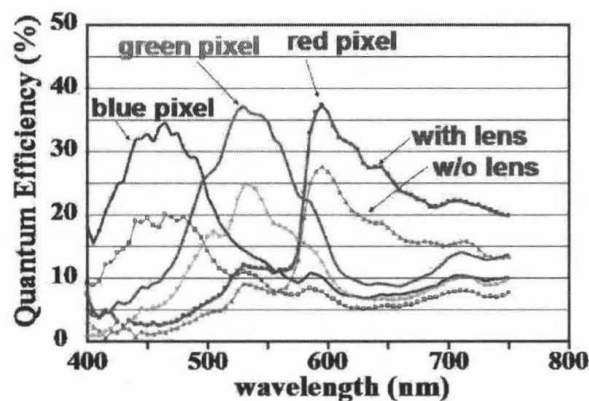


Fig. 4. Measured quantum efficiency of 2.7 μm pixel with red, green, and blue filters, for imager arrays with and without microlenses. Solid lines correspond to data from imager array with microlenses. Dashed lines (with lower quantum efficiency) correspond to data from imager array without microlenses.

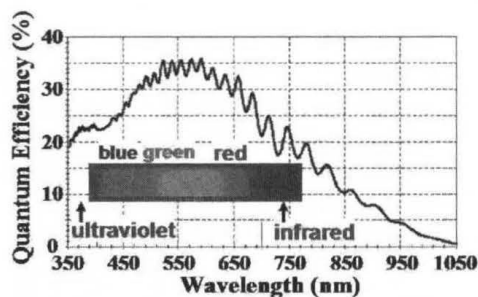


Fig. 5. Quantum efficiency of Si-based image sensor without color filters [ref. 9]. Color filters are required to generate a color image.

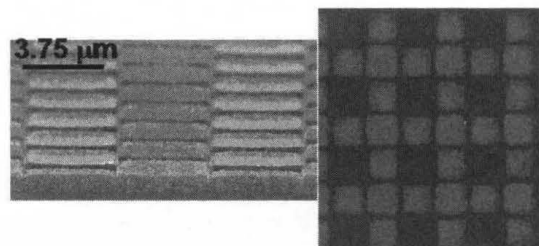


Fig. 6. SEM and optical micrograph of color filters. Color filters are formed using photoresist that is dyed with either green, red, or blue pigments.

INTEGRATION OF COPPER WIRING

The most significant advantage of Cu wiring in an image sensor is the reduction of the stack height. A comparison of three different 0.18 μm metallization technologies is shown in Fig. 7,

consisting of standard Al, standard Cu (same resistance as Al), and thin Cu. For a four-level metal wiring process, the Al stack height is more than 30% thicker than the Cu. Using these BEOL options, we modeled the angle response of a representative $2.7\text{ }\mu\text{m}$ pixel (Fig. 8). The angular response of the photodiode is greater as the thickness of the BEOL stack decreases.

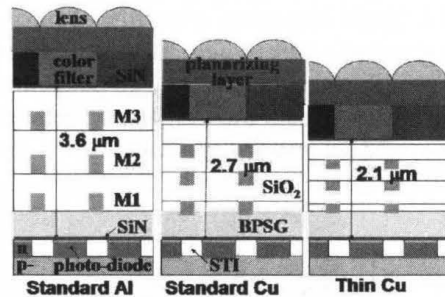


Fig. 7. Schematic comparing thicknesses of optical path with either standard $0.18\text{ }\mu\text{m}$ Al, standard $0.18\text{ }\mu\text{m}$, Cu, or thin Cu metallization.

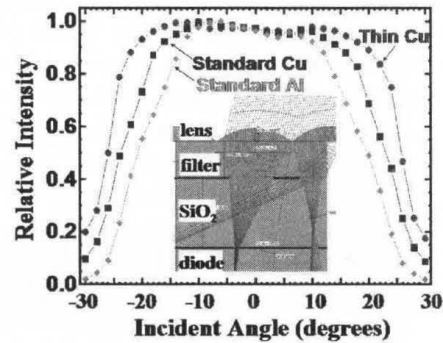


Fig. 8. Simulated angle response for a $2.7\text{ }\mu\text{m}$ pixel with standard Al, standard Cu, or thin Cu metallization.

The SiN passivation layer on top of the Cu introduces a discontinuity in the refractive index as the light travels to the detection area. Reflections from these layers degrade the spectral response (Fig. 9). With the nitrides present, the reflectance can reach 60% at some wavelengths. These reflections cannot be corrected because of the inherent variability in the manufacturing process.

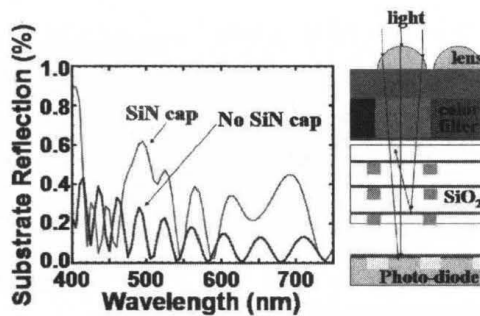


Fig. 9. Simulated reflectance of the optical path for 3 levels of Cu wiring in the array and 80 nm of SiN on top of the silicon, with and without SiN capping layers on Cu. The SiN capping layers have high reflectance, which reduces the light intensity at the photo-diodes.

The passivating SiN must be removed from the optical path in order to have acceptable optical performance. A number of methods are available to eliminate the nitride-induced reflections. The simplest approach preserves the nitrides over the copper layers, but uses a mask to eliminate them in the optical path (Fig. 10a). The experimental quantum efficiency from two pixel arrays (without microlenses or color filters), with and without the SiN layers in the optical path, is shown in Fig. 11. When the SiN layers are present, the quantum efficiency is degraded at a number of wavelengths, in particular, near 520 nm , 590 nm , and 650 nm . By removing the SiN layers, high quantum efficiency is maintained at all wavelengths.

The masked method of removing the nitrides, while solving the reflectance problem, is expensive and can potentially add defects that degrade yield. A more cost-effective solution is to use a self-aligned deposition of a barrier metal to protect the copper features. CoWP can be selectively deposited on the Cu features using an electroless plating technique after the copper polish (Fig. 10b). CoWP layers have been used in conjunction with dielectric capping layers to improve the electromigration lifetime of Cu interconnects [12]. However, the integration of CoWP without a dielectric capping layer is difficult. The CoWP must be thick enough to protect the copper during oxidizing processes, such as the deposition of SiO₂ by plasma enhanced chemical vapor deposition (PECVD), and the via and trench patterning processes [13,14]. If the CoWP is too thin, high via resistance and short stress migration lifetime will result [14, 15].

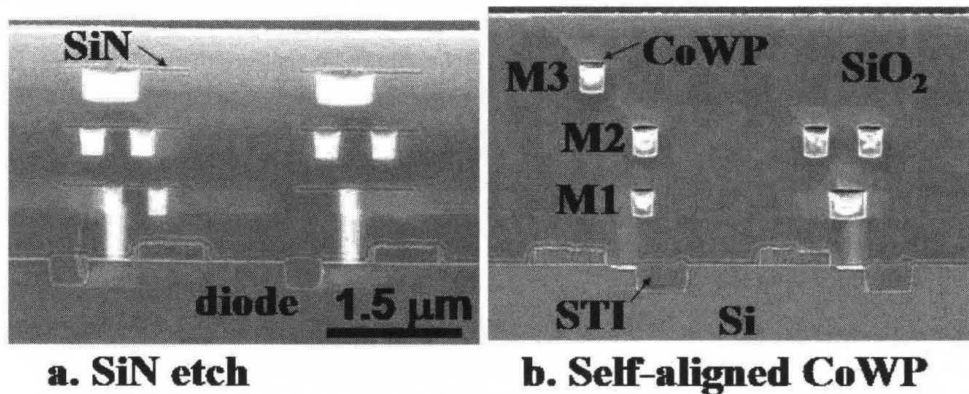


Fig. 10. SEM cross-sections of array fabricated with two different methods for eliminating SiN capping layers from optical path; (a) SiN etch and (b) self-aligned CoWP cap.

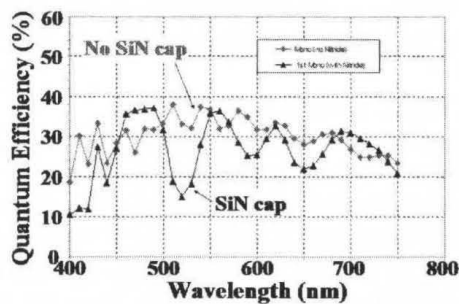


Fig. 11. Measured quantum efficiency versus wavelength for an image sensor (without color filters or microlenses) with 3 levels of Cu wiring in array, with and without SiN capping layers.

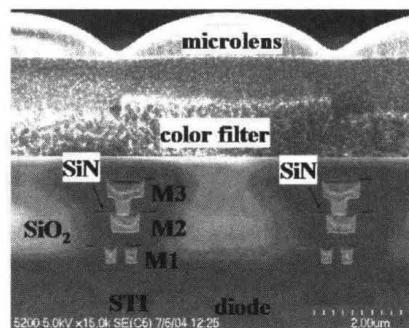


Fig. 12. SEM cross-section of array fabricated with SiN etch process, including color filters and microlenses.

We fabricated a 5M pixel imager with 2.7 μm pixels in a four-transistor architecture using the standard Cu interconnect process (Fig. 12). The angle response is in good agreement with the simulations in Fig. 8. Beyond the Cu interconnect stack-height reduction, we optimized barrier nitride layers on top of the pixel to serve as an anti-reflection coating for blue response [16]. In addition, we used a p-type layer to passivate the surface of the photodetector. Both the blue and red quantum efficiency continue to be improved by a combination of silicon processing and lens optimization (Fig. 4).

CONCLUSION

A 0.18 μm CMOS imager sensor technology is described that uses Cu interconnects. Copper wiring results in a thinner dielectric stack compared to Al wiring, which provides an improved angular response of the photodiode. However, the SiN capping layers on top of the Cu wires increase reflectivity, which can reduce the sensitivity of the photodiodes. A number of approaches are described for eliminating the SiN capping layers over the photodiodes, including a self-aligned CoWP passivation layer.

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REFERENCES

1. B. Dipert, Electronic Design News, Sept. 2004, p. 40
2. H. Rhodes, G. Agranov, C. Hong, U. Boettiger, R. Mauritzson, J. Ladd, I. Karasev, J. McKee, E. Jenkins, W. Quinlin, I. Patrick, J. Li, X. Fan, R. Panicacci, S. Smith, C. Mouli, J. Bruce, 2004 IEEE Workshop on Microelectronics and Electron Devices, 2004, p. 7.
3. D. Edelstein, J. Heidenreich, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, P. Roper, T. McDevitt, W. Motsiff, A. Simon, J. Dukovic, R. Wachnik, H. Rathore, R. Schulz, L. Su, S. Luce, J. Slattery, IEDM Proc., 1997, p. 773.
4. A.K. Stamper, M.B. Fuselier, X. Tian, IITC Proc., 1998, p. 62.
5. B. Agarwala, M. Armacost, S. Biesemans, L. Burrell, B. Chen, K. Han, D. Harmon, J. Heidenreich, K. Holloway, N. Rovedo, S. Kapur, T. Kebede, D. Kiesling, P. Kim, G. Matusiewicz, J. Lukaitis, P. Nguyen, N. Prabhakara, S. Rauch, G. Friese, F. Grellner, E. Kaltalioglu, M. Hoinkis, C. Lin, R. Mahnkopf, O. Prigge, T. Schafbauer, T. Schiml, K. Schrufer, S. Srinivasan, M. Stetter, M. Unger, R. Zoeller, ESSDERC'99, 1999, p. 632.
6. H.I. Kwon, I.M. Kang, B.-G. Park, J.D. Lee, S.S. Park, IEEE Trans. Elec. Dev., **51**, 178 (2004).
7. Y.-T. Fan, C.-S. Peng, C.-Y. Chu, Applications of Digital Image Processing XXIII, Proc. SPIE, vol. 4115, 2000, p. 263.
8. M. Deguchi, T. Maruyama, F. Yamasaki, T. Hamamoto, A. Izumi, IEEE Trans. Consumer. Elec., **38**, 583 (1992).
9. www.kodak.com/go/imagers

10. D.J. Guerrero, B. DiMenna, T. Flaim, R. Mercado, S. Sun, Sensors and Camera Systems for Scientific, Industrial, and Digital Photography Applications IV, Proc. SPIE, vol. 5017, 2003, p. 298.
11. H. Miller, IEEE/SEMI Advanced Semiconductor Manufacturing Conf., 1996, p. 192.
12. C.-K. Hu, L. Gignac, R. Rosenberg, E. Liniger, J. Rubino, C. Sambucetti, A. Stamper, A. Domenicucci, X. Chen, Microelec. Eng., **70**, 406 (2003).
13. J. Gambino, S. Smith, S. Mongeon, D. Meatyard, F. Chen, P. DeHaven, from Materials, Technology, and Reliability of Advanced Interconnects – 2005, MRS Proc., Spring 2005, B6.11.
14. J. Gambino, J. Wynne, S. Smith, S. Mongeon, P. Pokrinchak, D. Meatyard, IITC Proc. , 2005.
15. J. Gambino, C. Johnson, J. Therrien, D. Hunt, J. Wynne, S. Smith, S. Mongeon, P. Pokrinchak, T.M. Levin, Proc. 12th Int. Symp. Physical & Failure Analysis of Integrated Circuits, 2005, p. 92.
16. M. Furumiya, H. Ohkubo, Y. Muramatsu, S. Kurosawa, F. Okamoto, Y. Fujimoto, Y. Nakashiba, IEEE Trans. Elec. Dev., **48**, 2221 (2001).