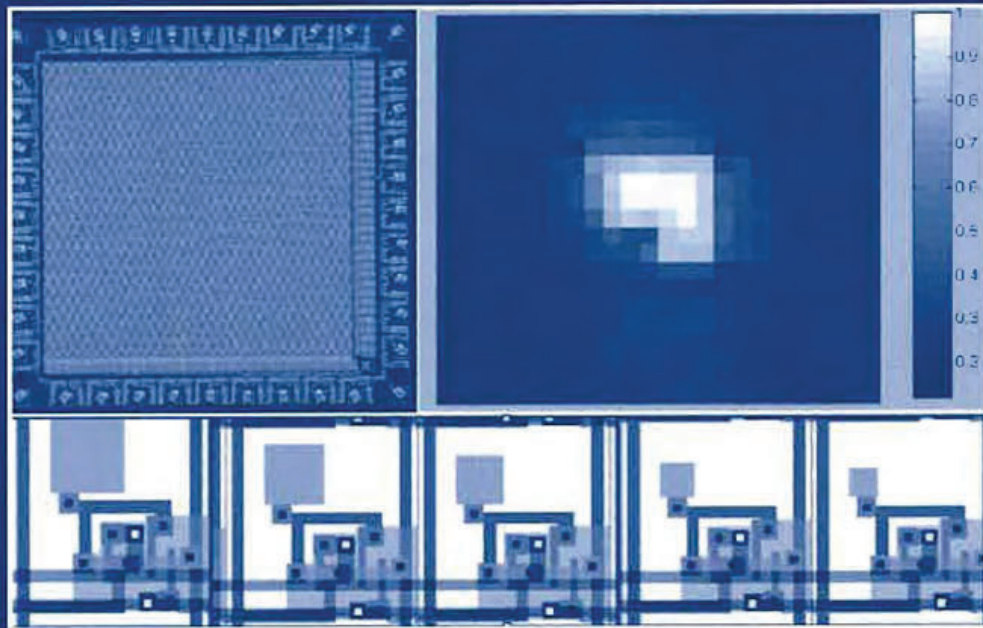


CMOS IMAGERS: FROM PHOTOTRANSDUCTION TO IMAGE PROCESSING

Orly Yadid-Pecht and Ralph Etienne-Cummings (Eds.)



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CMOS Imagers

From Phototransduction to Image Processing

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Chapter 3

PHOTORESPONSE ANALYSIS AND PIXEL SHAPE OPTIMIZATION FOR CMOS APS

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Abstract: A semi-analytical model has been developed for the estimation of the photoresponse of a photodiode-based CMOS active pixel sensor (APS). This model, based on a thorough analysis of experimental data, incorporates the effects of substrate diffusion as well as geometrical shape and size of the photodiode active area. It describes the dependence of pixel response on integration photocarriers and on conversion gain. The model also demonstrates that the tradeoff between these two conflicting factors gives rise to an optimum geometry, enabling the extraction of a maximum photoresponse. The dependence of the parameters on the process and design data is discussed, and the degree of accuracy for the photoresponse modeling is assessed.

Key words: CMOS image sensor, active pixel sensor (APS), diffusion process, quantum efficiency, parameter estimation, optimization, modeling.

3.1 Introduction

This work is a logical continuation of the pixel response analysis published by Yadid-Pecht et al. [1]. In this chapter, a pixel photoresponse is analyzed and quantified to provide the information necessary for its optimization. A novel way for the determination and prediction of the imager quantum efficiency (QE) is also presented. In this method, the QE is broadly interpreted to be dependent on the process and design data, i.e., on the pixel geometrical shape and fill factor. It is worth noting that QE, which is one of the main figures of merit for imagers, has been considered a whole pixel characteristic without any specific attention to the internal pixel geometry. However, it is useful to divide it into the main and diffusion parts. Even though the active area has the most effect on the output, the substrate

parts could account for up to 50% of the total output signal. The derived expression exhibits excellent agreement with the actual measurements obtained from a 256×256 CMOS active pixel sensor (APS) imager. The simplicity and the accuracy of the model make it a suitable candidate for implementation in photoresponse simulation of CMOS photodiode arrays.

This chapter presents the proposed photoresponse model and shows the correspondence between the theory and the experimental data. The model is then used to predict a design that will enable maximum response in different scalable CMOS technologies.

3.1.1 General remarks on photoresponse

Single-chip electronic cameras can be fabricated using a standard CMOS process; these cameras have the advantages of high levels of integration, low cost, and low power consumption [2–13]. However, getting an acceptable response from the currently available CMOS structures is a major difficulty with this technology.

A particular problem encountered by designers of vision chips in standard CMOS technologies is that foundries do not deliver characterization data for the available photosensors. Thus, designers are forced to use simplistic behavioral models based on the idealized descriptions of CMOS-compatible photosensors descriptions. This may be enough for chips intended to process binary images. However, the characteristics of real devices largely differ from their idealized descriptions, being, on the other hand, strongly dependent on the fabrication process. Consequently, using these idealized models yields very inaccurate results whenever the analog content of the incoming light (regarding both intensity and wavelength) is significant for signal processing; i.e., chips whose behavior is anticipated on the basis of such simplified models most likely will not accomplish the specifications. In this scenario, designers of vision chips are confronted by the necessity to fully characterize the CMOS-compatible photosensors by themselves. This is not a simple undertaking and requires expertise that is not common among chip designers. This chapter is intended to help designers acquire the skills to accomplish this task.

In order to predict the performance of an image sensor, a detailed understanding is required of the photocurrent collection mechanism in the photodiodes that comprise the array.

The response of the detectors can be affected by different parameters that are dependent on the process or on the layout. Process-dependent parameters (such as junction depths and doping concentration) cannot be modified by the designer, whereas layout-dependent parameters (detector size and shape)

are under the designer's control. Both types of parameters have to be considered when designing a test chip for characterizing visible-light detectors. All possible devices or structures available in the technology to detect visible light have to be included in the chip so that their actual behavior can be measured. In addition, these detectors should each be tested in different sizes and shapes to account for the layout-dependent parameters. Each detector should ideally be tested in as many sizes as possible, with a range of different perimeters (shapes) for each size. Furthermore, the chip should include as many copies of each detector configuration as possible to obtain statistical information on their response. Since detectors must be connected to bonding pads to have direct access to the detected signal, the cost of fabrication of such a chip would be very high.

A more realistic approach would use a limited number of discrete detectors with different sizes and shapes, but still covering all the possible device structures; several arrays of these detectors would be tested to provide the statistical information. Accordingly, the experimental data in this chapter were acquired from several APS chips fabricated in standard, scalable CMOS technology processes (e.g., standard $0.5\ \mu\text{m}$ and $0.35\ \mu\text{m}$ CMOS processes). Various topologies of the photosensitive area were implemented. All the pixels had a common traditional three-transistor type of readout circuitry (see *Figure 3-1*), enabling behavior identification for the different pixel types. Deviations in the device geometry were demonstrated to affect overall performance and thus these dependencies can be used as a predictive tool for design optimization.

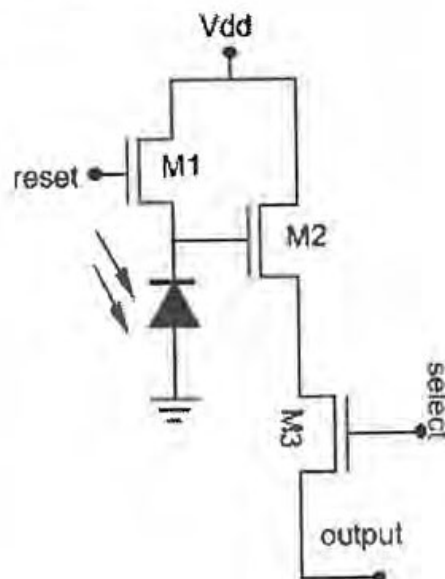


Figure 3-1. Traditional pixel readout circuitry. Transistor M2 is used as a source follower and the M2 gate is used to read out the photodiode voltage.

When light is incident on a diode (APS systems usually consist of photodiode or photogate arrays on a silicon substrate), photons absorbed in the depletion region of the p-n junction create electron-hole pairs that are separated by the high internal electric field. These new charges can be detected as an increase in the reverse current of the device or as a change in the voltage across it. Carriers generated in the bulk of the silicon, if they are less than a minority-carrier diffusion length away from the depletion region, can also contribute to the detected signal and thus increase the sensitive volume of the detector. The collection of photocarriers along the lateral edge of the photodiode is known as the peripheral photoresponse or the lateral photocurrent [14–17]. The overall signal generated by a pixel is therefore proportional to its geometry; i.e., the signal grows as photodiode dimensions increase. The total signal can be represented as the sum of the main (photodiode) response and the periphery response (due to the successfully collected diffusion carriers).

Figure 3-2 schematically shows cross-section of imager sites and indicates their depletion-region boundaries.

The response of these detectors is also affected by other parameters, such as technology scaling and detector size and shape. It is important to characterize all possible detectors for a range of sizes and shapes (independent of the circuitry) to obtain the photogenerated current levels for each case. All possible detectors also have to be characterized for each technology in order to find the optimum device and match the requirements of the signal processing circuitry.

In the case of CMOS APS, the charge-to-voltage conversion gain is typically dominated by the photodiode junction capacitance, which is composed of the bottom and sidewall capacitances. This capacitance can be expressed as

$$C_{jdp} = \frac{C_{j0B} A_D}{\left[1 - \left(\frac{V_d}{\phi_B}\right)\right]^{m_j}} + \frac{C_{j0sw} P_D}{\left[1 - \left(\frac{V_d}{\phi_{Bsw}}\right)\right]^{m_{jsw}}} \quad (3.1)$$

where

- C_{jdp} represents the depletion capacitance of the p-n junction;
- C_{j0B} and C_{j0sw} represents zero-bias capacitances of the bottom and the sidewall components, respectively;
- V_d is the voltage applied to the photodiode;
- ϕ_B and ϕ_{Bsw} stand for the build-in potential of the bottom and the sidewalls respectively;

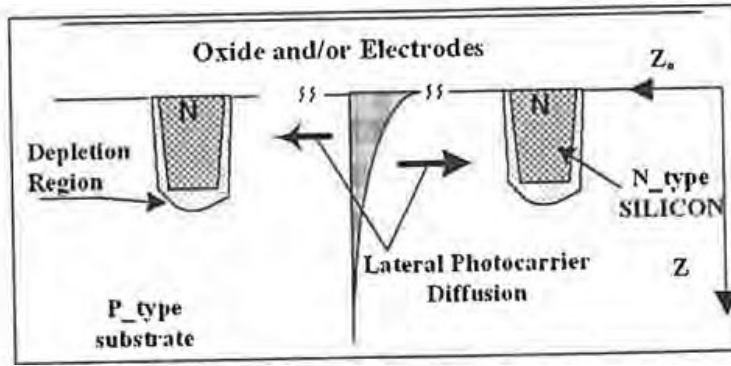


Figure 3-2. Cross-sections of imager sites and their depletion-region boundaries.

- m_j and m_{jsw} stand for the grading coefficients of the bottom and the sidewalls respectively;
- A_D represents the photodiode area (bottom component); and
- P_D represents the photodiode perimeter.

The conversion factor, $C_{gain} = q_{el}/C_{jdep}$ (in $\mu V/e^-$), is inversely proportional to the pixel geometry. The factor q_{el} is the electron charge.

The basic transfer characteristics of a photodetector are usually described by its quantum efficiency, which depends on the wavelength and describes the number of electrons generated and collected per incident photon. The quantum efficiency is related to the spectral response (in A/W) according to the equation:

$$SR(\lambda) = \frac{\lambda q}{hc}(\lambda) \quad (3.2)$$

If a photodiode is exposed to a spectral power density $\Phi(\lambda)$, the collected photocharge can be expressed as

$$Q = A_{eff} t_{int} \int SR(\lambda) \Phi(\lambda) d\lambda \quad (3.3)$$

with A_{eff} denoting the effective photoactive area of a pixel and t_{int} the integration time. Illumination is assumed to be constant during the exposure time.

The voltage swing that is obtained from the collected photocharge is inversely proportional to the integration capacitance, C_{int} (which equals the depletion capacitance C_{jdep} in CMOS APS), as follows:

$$V = \frac{Q}{C_{int}} = \frac{A_{eff} t_{int} q}{C_{int}} \int \frac{\lambda}{hc} \eta(\lambda) \Phi(\lambda) d\lambda \quad (3.4)$$

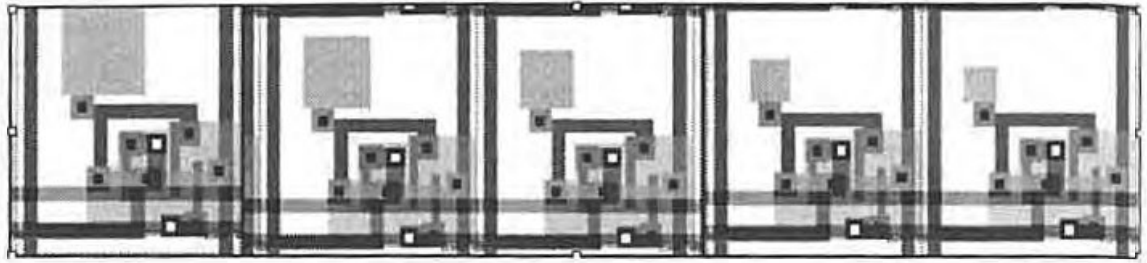


Figure 3-3. A sample from an otherwise identical square-shaped pixel set with decreasing active area (photodiode) dimensions. The photodiode areas in the full pixel set vary from $40\ \mu\text{m}^2$ down to $5.5\ \mu\text{m}^2$ and their perimeters from $23\ \mu\text{m}$ down to $9.3\ \mu\text{m}$.

Consequently, pixel signal output is proportional to the product of the integrated photocarriers and the conversion gain. The tradeoff between these two conflicting parameters is most important. Indeed, it has already been shown that a lower active area contributes to a higher output signal. This is mainly due to an increase in conversion gain, but the active-area surroundings probably have an affect as well [1, 5, 10, 18]. However, a lower active area reduces the fill factor, which directly influences the signal and the signal-to-noise ratio. Both the active area and the fill factor should therefore be as large as possible.

3.2 Photoresponse model

Figure 3-3 shows a sample from a set of pixels of identical square shape but decreasing active area (photodiode) dimensions. The photodiode areas vary from $40\ \mu\text{m}^2$ down to $5.5\ \mu\text{m}^2$, and their perimeters vary from $23\ \mu\text{m}$ down to $9.3\ \mu\text{m}$.

Figure 3-4 displays the signal output obtained for illumination at three different wavelengths with the various photodiode geometries of the pixel set represented in *Figure 3-3*.

The curves share the same behavior, each displaying a pronounced maximum in the response. Pixel sets of different photodiode active-area geometrical shapes were tested, including circular, rectangular, and L-shaped. For each shape, a similar phenomenon was observed: each type of pixel gives a maximum response for particular illumination conditions. Note that for each wavelength (λ was changed from $450\ \text{nm}$ to $650\ \text{nm}$) the measurements were performed under uniform light (an integrating sphere was used). The tradeoff between the two conflicting factors, integrated photocarriers and conversion gain, give rise to an optimum geometry and thus the maximum photoresponse.

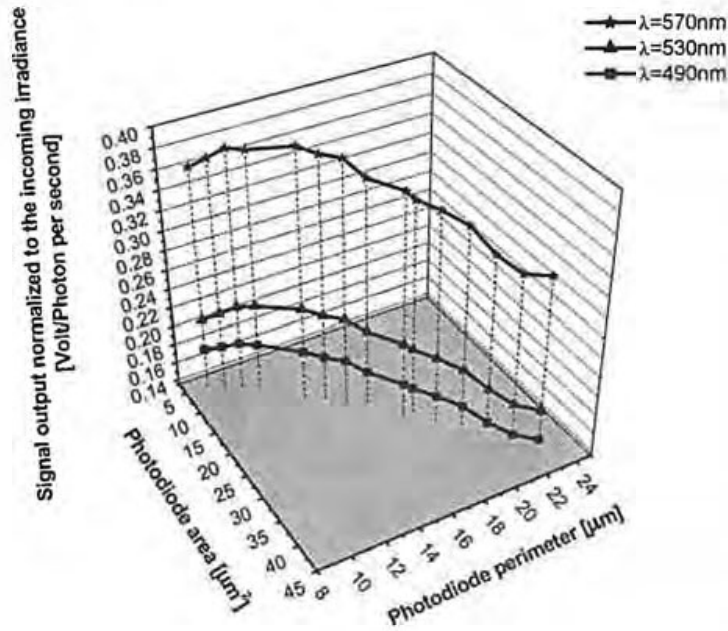


Figure 3-4. The signal output of the pixel set represented in Figure 3-3 with illumination at three different wavelengths and with changes in the linear dimensions of the photodiodes.

A semi-analytical expression has been derived for a diffusion-limited pixel photosignal in a closely spaced photodiode array. In this expression each one of the parameters determining the signal output depends on the photodiode area and perimeter:

$$\frac{V_{out}(\lambda)}{N_{p\lambda}} = (\text{integration photocarriers} \times \text{conversion gain}) \quad (3.5)$$

$$= \frac{k_1 A + k_2 P d \left(\frac{S-A}{S} \right) \left(1 - \frac{4Pi-P}{8L_{diff}} \right)}{k_3 A + k_4 P}$$

The left part of this equation, $V_{out}(\lambda)/N_{p\lambda}$, corresponds to the pixel output voltage signal related to the number of incoming photons (in a time unit).

On the right side of equation (3.5), the denominator represents the conversion factor and the numerator represents the integrated photocarriers. The term in the denominator, $1/(k_3 A + k_4 P)$, represents the conversion gain, which depends on both the photodiode area and perimeter. The numerator

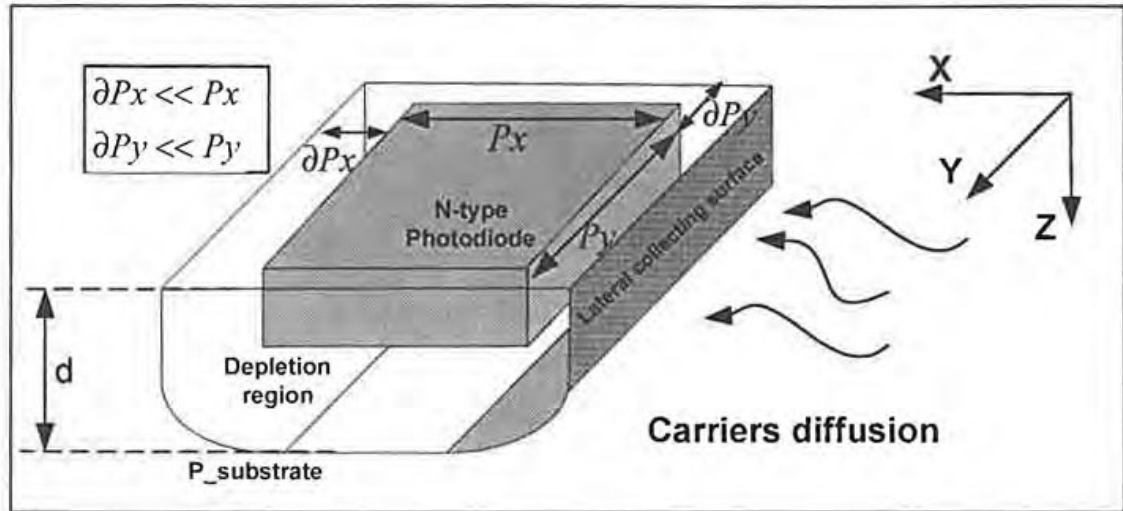


Figure 3-5. The sidewall or lateral collecting surface, built up from the junction bottom and sidewall depletion capacitances. P (in μm) is the photodiode perimeter; P_x and P_y are its dimensions in the x and y directions; d (in μm) is the junction depth; and ∂P_x and ∂P_y are the lateral depletion stretches.

consists of two terms that contribute to the total number of carriers collected by the imager. The first term, $k_1 A$, represents the contribution of the photocarriers created within the photodiode itself, i.e., the contribution of the active area. The second term

$$k_2 P d \left(\frac{S - A}{S} \right) \left(1 - \frac{4P_i - P}{8L_{diff}} \right)$$

represents the contribution of the periphery or the “lateral diffusion current”, i.e., the carriers that had been created in the area surrounding the photodiode, had successfully diffused towards the photodiode, and had been collected.

Pd (in μm^2) represents the lateral collecting surface or the interaction cross-section for lateral diffusion, where P (in μm) is the photodiode perimeter, and d (in μm) is the junction depth. Since $\partial P_x \ll P_x$ and $\partial P_y \ll P_y$ (where ∂P_x and ∂P_y are the lateral depletion stretches of the photodiode), ∂P_x and ∂P_y can be neglected. Therefore, it can be assumed that the perimeter P (in μm) itself defines the boundary of lateral interaction area (see Figure 3-5).

The term $((S - A)/S)$ is dimensionless. Since the optical generation rate is relatively uniform throughout the substrate, this multiplier is proportional to the relative number of carriers created within the pixel substrate around the photodiode. Here, $(S - A)$ (in μm^2) represents the substrate area, i.e., the unoccupied area surrounding the photodiode within the pixel, whereas A

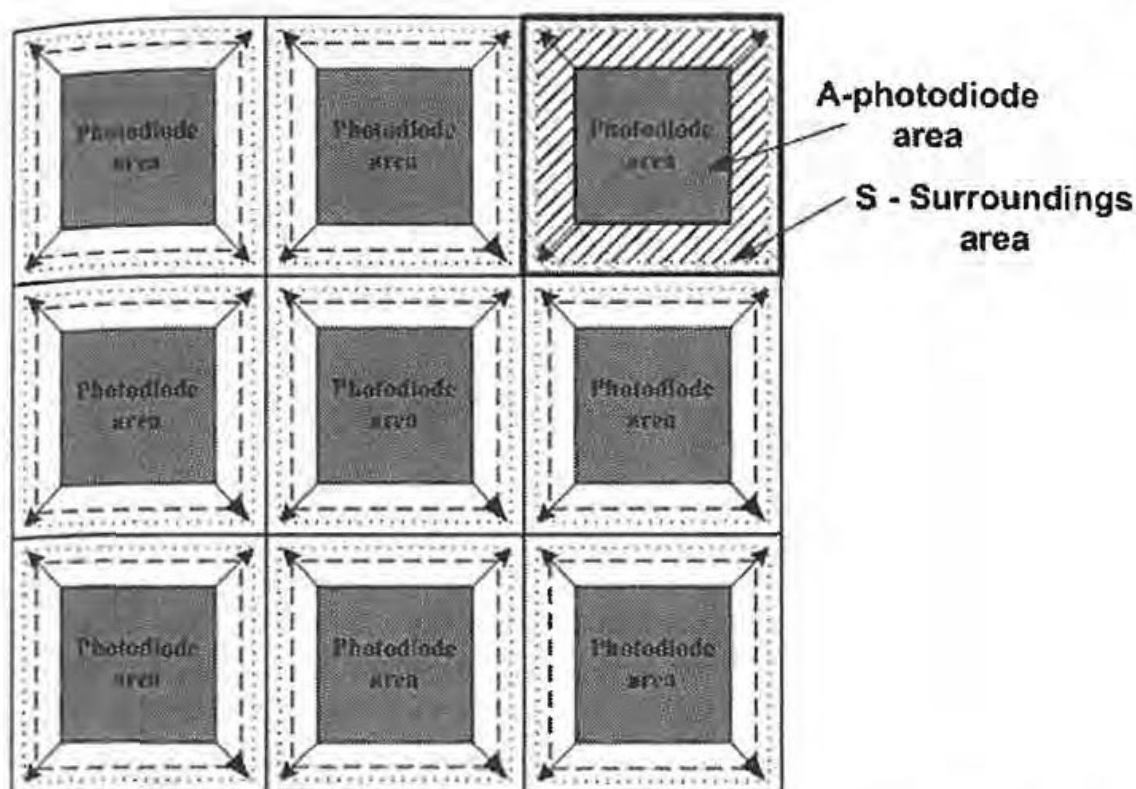


Figure 3-6. A schematic illustration of the boundary condition where the active area is increased to the maximum possible and reaches the pixel boundary (i.e., $A = S$ for all the pixels in the array). When this occurs, the diffusion contribution will equal zero.

(in μm^2) is the photodiode active area. The lower the fill factor, the higher the number of the carriers created within the photodiode surroundings that can diffuse and contribute to the total signal. It is clear that this multiplier represents the array influence on the pixel photodiode, and the boundary condition, i.e., as the active area increases to the pixel boundary and $A = S$ is approached for all the pixels in array, the diffusion contribution to the signal approaches zero. Figure 3-6 illustrates the situation where the diffusion equals zero as a result of maximum expansion of the photodiode area for all pixels in the array. Therefore, the multiplier $((S - A)/S)$ represents the relative number of the potential diffusion contributors.

The term $(1 - (4Pi - P)/8L_{diff})$ is dimensionless and indicates the approximate relative distance that the prospective contributor has to pass before it is trapped in the depletion region. In this term, L_{diff} (in μm) is the characteristic diffusion length and Pi (in μm) is the pixel pitch. As the photodiode dimensions and the perimeter P (in μm) increase, the maximum distance that a carrier created within the substrate has to diffuse before it is collected by the peripheral sidewall collecting surface Pd decreases. Thus, the diffusion contribution increases. This multiplier is obtained from a series

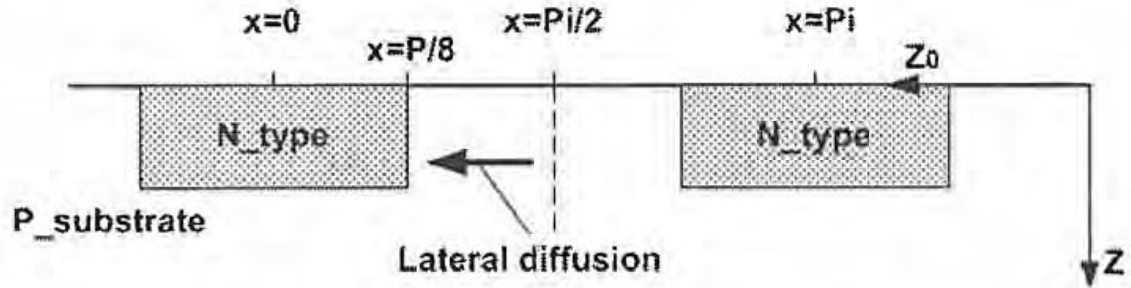


Figure 3-7. A schematic cross-section of two imager sites, illustrating the dependence of diffusion distance on the photodiode geometry. Pi is the pixel pitch.

expansion of the expression $\exp[-(4Pi - P)/8L_{diff}]$, which represents the solution to the one-dimensional diffusion equation [19–21]. Since the distances between the photodiodes in the array—and therefore the maximum carrier path—are small compared to the minority carrier diffusion length, it is sufficient to consider only the first two terms of the expansion. Figure 3-7 illustrates the dependence of diffusion distance on the photodiode geometry.

Also in equation (3.5), $V(\lambda)$ (in volts) is the pixel signal output for a particular wavelength.

$N_{p\lambda}$ (in photons/sec) is the photon irradiance. Since watts are joules per second, one watt of monochromatic radiation at wavelength λ corresponds to $N_{p\lambda}$ photons per second. The general expression is

$$\frac{dN_{p\lambda}}{dt} = 5.03 \times 10^{15} P_{\lambda} \lambda$$

where P_{λ} is in watts and λ is in nm.

The coefficient k_1 (in μm^{-2}) describes the unit active-area contribution to the total number of electrons collected by the imager, i.e., the number of electrons collected by the unit photodiode area in a time unit.

The coefficient k_2 (in μm^{-2}) describes the photodiode unit peripheral-area contribution to the total number of electrons collected by the imager, i.e., the number of electrons collected by the sidewall collecting surface within the substrate. Figure 3-5 illustrates the sidewall or lateral collecting surface, which is built up from junction bottom and sidewall depletion capacitances.

The coefficients k_3 and k_4 (in $\text{aF} \cdot \mu\text{m}^{-2}$ and $\text{aF} \cdot \mu\text{m}^{-1}$, respectively) describe the bottom and sidewall capacitances in the regular junction capacitance sense (see equation (3.1)) and are defined by the particular process data.

In summary, the diffusion contribution to the overall signal is proportional to the lateral collecting area, the number of possible contributors, and the distance that the carrier has to pass before its collection

by the photodiode. All parameters, with the exception of the coefficients k_1 and k_2 , are defined by the process and design data. The expression agrees well with experimental results, as shown in the following section.

3.3 Comparison with experimental results

We have performed a functional analysis of experimental data obtained from a $14 \times 14 \mu\text{m}$ pitch CMOS APS array by means of scientific analysis software. Pixel sets with square, rectangular, circular, and L-shaped active areas of different sizes have been tested. The response was analyzed for different wavelengths in the visible spectrum. Example results for a photodiode pixel with a square-shaped active area have been presented here.

The solution (in the minimum variance sense) of equation (3.5) for different pixel sets and different wavelengths enabled the extraction of the missing coefficients k_1 and k_2 . The combination of these coefficients determined the contributions to the total pixel output signal and remained constant for all pixels at certain wavelength exposures.

It is evident from *Figure 3-4* that a longer wavelength enabled better response; for example, the signal obtained at 570 nm was almost two times the one obtained at 490 nm. This can be related to better absorption of red visible radiation within the semiconductor depth and thus better quantum efficiency. Moreover, the curves in *Figure 3-4* are shifted approximately in parallel. Since this output change was defined only by k_1 and k_2 (all other terms are wavelength independent), it was to be expected that the coefficients are wavelength dependent and that there was an increase in their values for longer wavelengths. As mentioned earlier, these coefficients represented the number of electrons collected by the photodiode via its upper and lateral faces respectively. Since the output signal was normalized to the number of photons impinging the pixel for uniform incident illumination, k_1 and k_2 was interpreted as the quantum efficiency per unit area for the upper and lateral faces respectively.

As the output signal for 570 nm was approximately double that for 490 nm, it was predicted that the QE for 570 nm would be double that the QE for 490 nm. The values obtained for the coefficients k_1 and k_2 confirmed this result: k_1/k_2 (570 nm) $\approx 0.468/0.229$, and k_1/k_2 (490 nm) $\approx 0.215/0.107$.

It is worth noting that QE, which is one of the main figures of merit for imagers, was considered only as a whole-pixel characteristic; i.e., no specific attention was paid to the photodiode shape and fill factor [1, 13, 22–23]. The work in this chapter demonstrates the merit of dividing QE into its main and diffusion portions according to the pixel geometrical shape and fill factor. This chapter also introduces a method (solving equation (3.5)) for the

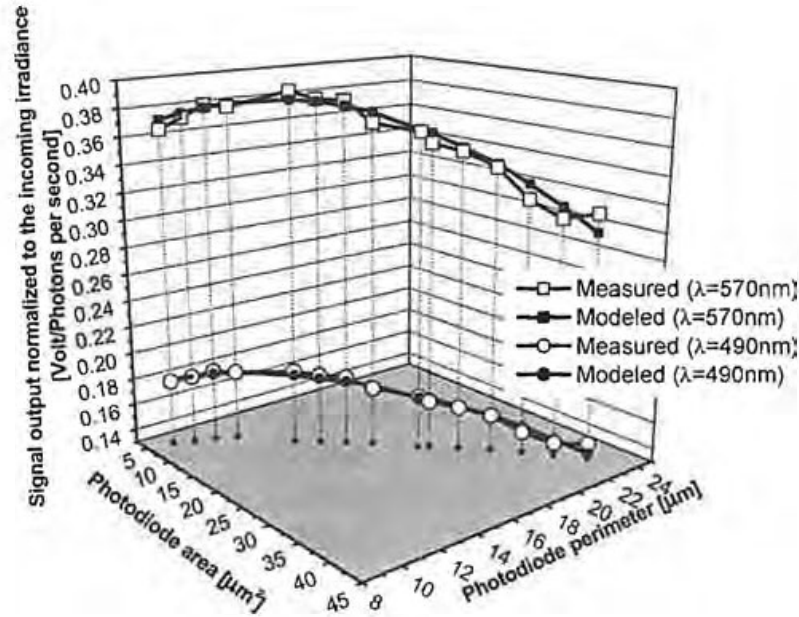


Figure 3-8. Comparisons at two different wavelengths of the derived expression, equation (3.5), with the actual pixel measurements presented in Figure 3-3 and Figure 3-4.

determination and prediction of QE based on the process and design data. The result obtained for the presented pixel sets is $k_1/k_2 \approx 2.7$. This demonstrates that even though the active area is the primary source of the output, the substrate could account for up to 50% of the total output signal.

A 3-D graph presented in Figure 3-8 shows example comparisons at two different wavelengths of the derived expression, equation (3.5), and the actual pixel measurements presented in Figure 3-3 and in Figure 3-4. It illustrates the correspondence between the measured and the modeled output signal as the pixel area and perimeter are varied. Furthermore, the modeled function reaches its maximum exactly at the point marked by the measurements, confirming the proposed assumption that a compromise between integration photocarriers and conversion gain results in an optimum photodiode geometry. Thus, the model enables the successful prediction of a geometry that provides maximum output signal. Based on equation (3.5) and the specific process data, it is possible to select the photodiode shape and size that will provide the highest outcome.

The functional analysis of equation (3.5) enables the determination of the variables (area A and perimeter P) corresponding to the maximum value of the argument. It should be noted that area and perimeter are not independent; the function describing their dependence is implicit and must be taken into

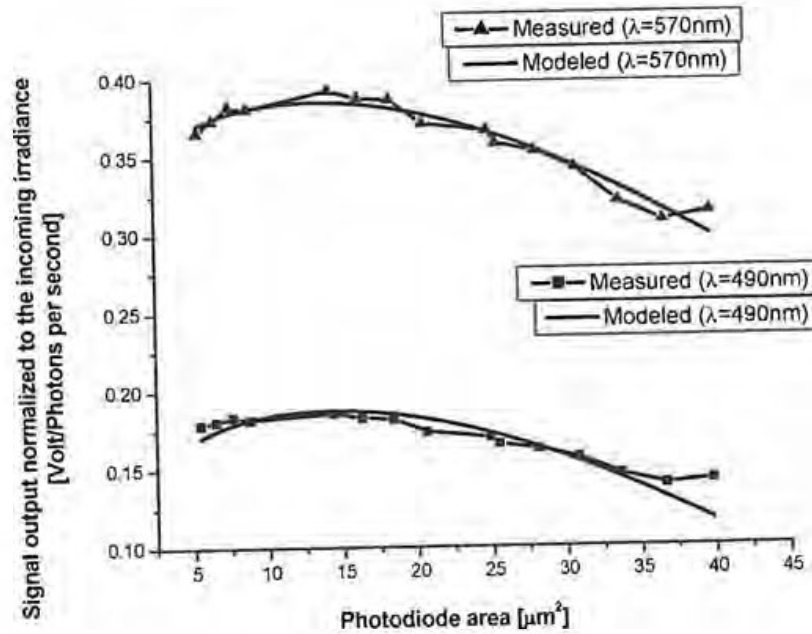


Figure 3-9. A comparison of the dependence of the modeled and experimental pixel output signal on the photodiode area for the square-shaped pixel data set of Figure 3-8.

consideration. In the case of a symmetrical photodiode shape, the function connecting area and perimeter can be easily obtained. equation (3.5) thus reduces to the case of only one independent variable; for example, the expression $P = 4A^{1/2}$ relates area and perimeter for the square-shaped photodiode. This result is confirmed in Figure 3-9, which presents a 2-D comparison of the dependence of the modeled and the experimental output signal on the photodiode area for the square-shaped pixel data set of Figure 3-8. A more complicated photodiode shape could always be represented as an aggregate of the elementary symmetrical parts [17, 24] and investigated in order to obtain a relation with only one independent variable as above.

Good correspondence of the model with the data is seen when the maximum divergence of the model result is constrained to 5%. It should be noted that surface leakage and the non-ideal transmission rate of the overlayers are not included in the present analysis and are considered to be second order effects [25].

3.4 CMOS APS pixel photoresponse prediction for scalable CMOS technologies

This section describes a semi-analytical diffusion-limited CMOS APS pixel photoresponse model use for maximum pixel photosignal prediction in scalable CMOS technologies.

3.4.1 Impact of technology scaling on sensitivity

Over the last twenty years, the evolution of CMOS technology has followed Moore's Law: a new generation of technology has been developed every three years, and between generations, memory capacity increased by a factor of four and logic circuit density increased by a factor of between two and three. Furthermore, every six years (two generations), the feature size decreased by a factor of two and transistor density, clock rate, chip area, chip power dissipation and the maximum number of pins has doubled. This continuous development has led to a reduction in the state-of-the-art commercially available minimum lithographic feature size from $3\text{ }\mu\text{m}$ in 1977 to $0.25\text{ }\mu\text{m}$ in 1998 and $0.1\text{ }\mu\text{m}$ in 2003. It is anticipated that it is technically possible to maintain the pace shown in *Table 3-1* [26].

CMOS process development is funded by high-volume sales of standard CMOS logic and memory chips. Hence, CMOS imaging technology does not have to bear the process development costs and consequently has cheaper process costs than CCD imagers.

Decreases in pixel size much beyond $5 \times 5\text{ }\mu\text{m}$ have not been considered to be of much interest due to camera lens diffraction issues. However, in a common Bayer patterned RGB color sensor, 2×2 pixels define an effective color pixel; further downscaling of single pixels may prove useful for fitting an entire effective color pixel within the optical lens resolution limit. Therefore, pixel sizes below $5 \times 5\text{ }\mu\text{m}^2$ can be expected for all imagers, contrary to an assumption made by Wong [27].

The predicted downscaling of the supply voltage (see *Table 3-1*) will lead to a reduction of usable signal range and, together with increased noise components, will limit the overall dynamic range. Sources of detrimentally high leakage currents that generate shot noise and flood the pixel are discussed by Wong [27]. Examples include dark current, p-n junction tunneling current, transistor off current, gate oxide leakage, and hot carrier effects.

As Wong [27] noted, the diffusion collection behavior is modified by increasing doping levels through the reduction of mobility and lifetime. Under strong absorption conditions, the absorption coefficient $\alpha(\lambda)$ and the

Table 3-1. Technology parameters for different process generations (after [26]).

Process	0.8 μm	0.5 μm	0.35 μm	0.25 μm	0.18 μm	0.1 μm
Supply voltage (V)	5-3.3	5-3.3	5-3.3	2.5-1.8	1.8-1.5	1.2-0.9
Interconnect levels	2	2-3	4-5	5-6	6-7	8-9
Substrate doping (cm^{-3})	8×10^{16}	1.2×10^{17}	2.5×10^{17}	3.4×10^{17}	5×10^{17}	1×10^{18}
Junction depth d/S (nm)	350-450	300-400	200-300	50-100	36-72	20-40
Depletion region (μm)	0.71	0.57	0.39	0.24	0.19	0.1
Mobility ($\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$)	825	715	550	485	425	345
Lifetime (μs)	3.6	2.3	1.1	0.8	0.6	0.3
Diffusion length (μm)	88	68	41	33	25	15

diffusion length L_n are both much smaller than the width of the substrate. Further effects on spectral sensitivity result from the shallower drain/source diffusion and the shrinkage of the depletion widths. Figure 3-10 demonstrates that the scaling effect on diffusion collection efficiency works in favor of CMOS imagers. The influence on mobility and lifetime are not very strong, so the loss of sensitivity in the infrared range is not very pronounced. On the other hand, the shallower diffusions promote the collection of blue light in the silicon material. This improves performance for visible light applications, especially for color sensors, as was shown above. These effects of technology scaling apply directly to the photodiode. However, the losses caused by the overlying layers must also be included and reduce the total QE considerably.

The lens diffraction limit of 5 μm has been reached with the 0.35 μm process. The increased number of routing levels leads to an increasing

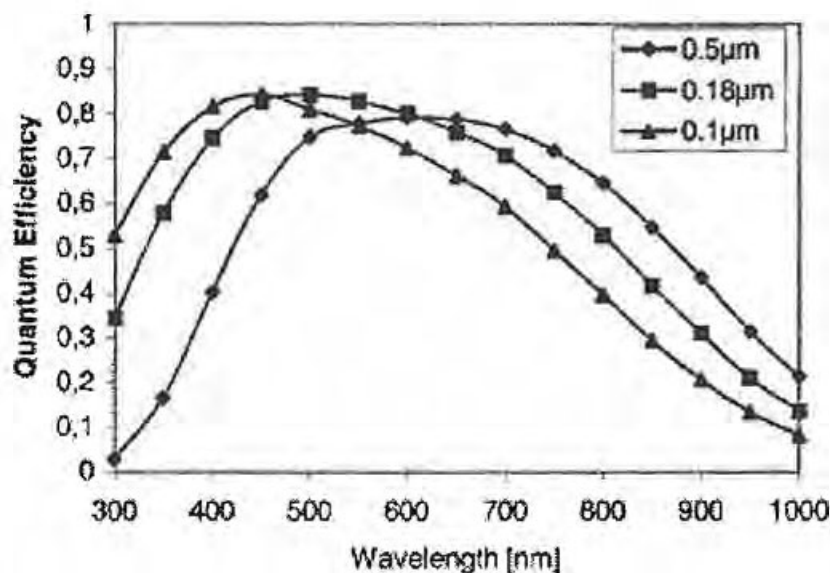


Figure 3-10. Internal carrier collection efficiency for different process generations (after [26]).

Table 3-2. Scaling trends of CMOS sensor parameters for a standard photodiode (after [26]).

Technology	0.8 μm	0.35 μm	0.25 μm	0.18 μm
Sensor type	standard	standard	standard	standard
A_{pix} (μm^2)	14 $\times$ 14	7 $\times$ 7	5 $\times$ 5	5 $\times$ 5
Fill factor (%)	60	60	60	80
A_{diode} (μm^2)	117.6	29.4	15	20
C_{diff} (fF)	5.75	2.7	1.87	0.65
C_{gate} (fF)	2.06	1.1	0.67	0.48
C_{diode} (fF)	94.4	37.8	38.3	24.2
C_{tot} (fF)	102.2	41.6	40.8	25.3
q/C ($\mu\text{V}/\text{e}^-$)	1.5	3.8	3.9	6.4
S ($\text{V}\cdot\mu\text{J}^{-1}\cdot\text{cm}^{-2}$)	1.8	1.1	0.57	1.2

thickness of the layer system on top of the diode, which aggravates the problems of absorption, reflection, diffraction, and even light guidance into distant pixels. In addition, the accuracy requirements for microlenses become very strict as the sensitive spot in the pixels becomes smaller and moves further away from the lens. Below 0.35 μm , only those processes that allow blocking of silicide layers on diffusions can be employed. The shrinkage of capacitances does not generally compensate sufficiently for the reduction of sensitive area. On the contrary, the area-specific capacitance increases due to increased doping concentrations, which automatically reduces the sensitivity. For a given fill factor, the overall sensitivity remains low, as shown by the results presented in Table 3-2 [26].

3.4.2 CMOS APS pixel photoresponse predictions for scalable CMOS technologies

It has recently been shown ([28] and section 3.2) that for any pixel active-area shape, a reliable estimate of the degradation of image performance is possible. The tradeoff between conflicting factors (such as integrated photocarriers and conversion gain) can be compared for each pixel design, allowing the optimum overall sensor performance in a particular technology process to be determined. The present work is based on a thorough study of the experimental data acquired from several pixel chips fabricated in two different technology processes, 0.5 μm and 0.35 μm CMOS processes. Using this data, the analysis is extended to show the efficacy and the suitability of this photoresponse model in scalable CMOS processes. Calculations based on this model only require readily available process and design data to make possible the selection of designs with maximum output signal.

Figure 3-3 and Figure 3-11 show two subsets of pixels (square and rectangular active-area shape, respectively) with decreasing photodiode dimensions and fabricated in a standard CMOS 0.5 μm process.

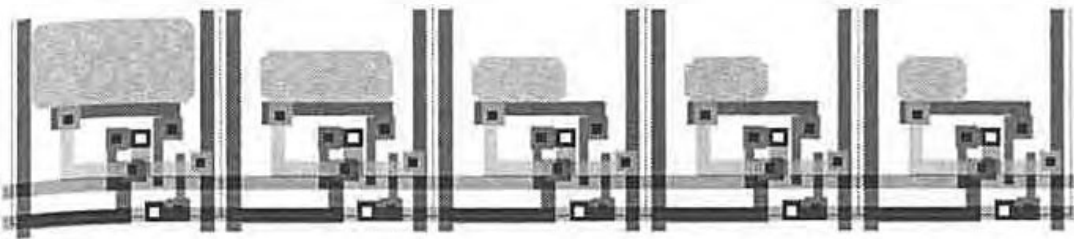


Figure 3-11. A sample from an otherwise identical set of rectangular active-area pixels (CMOS 0.5 μm technology) with decreasing photodiode dimensions. The photodiode areas in the full pixel set vary from $63 \mu\text{m}^2$ to $13 \mu\text{m}^2$ and their perimeters from $34 \mu\text{m}$ to $15.5 \mu\text{m}$.

Figure 3-4 and Figure 3-12 show the corresponding output curves for several wavelengths of illumination. These curves share the same behavior; i.e., Figure 3-4 curves display a pronounced maximum response location, while in Figure 3-12 the curves tend to an extremum.

The photoresponse model enables the extraction of the unit “main area” and unit peripheral contributions to the output signal, and in turn the identification and modeling of pixel behavior (see Figure 3-8).

The fact that the combination of these two contributions remains invariable for all pixels at a specific wavelength of illumination (for a

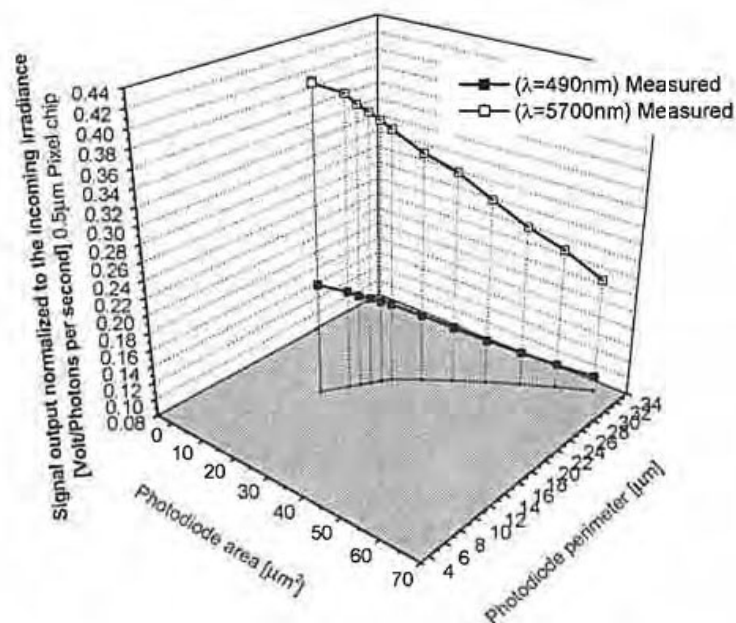


Figure 3-12. Measured signal output obtained for the pixel set presented in Figure 3-11 as functions of the photodiode linear dimensions for two different wavelength illuminations.

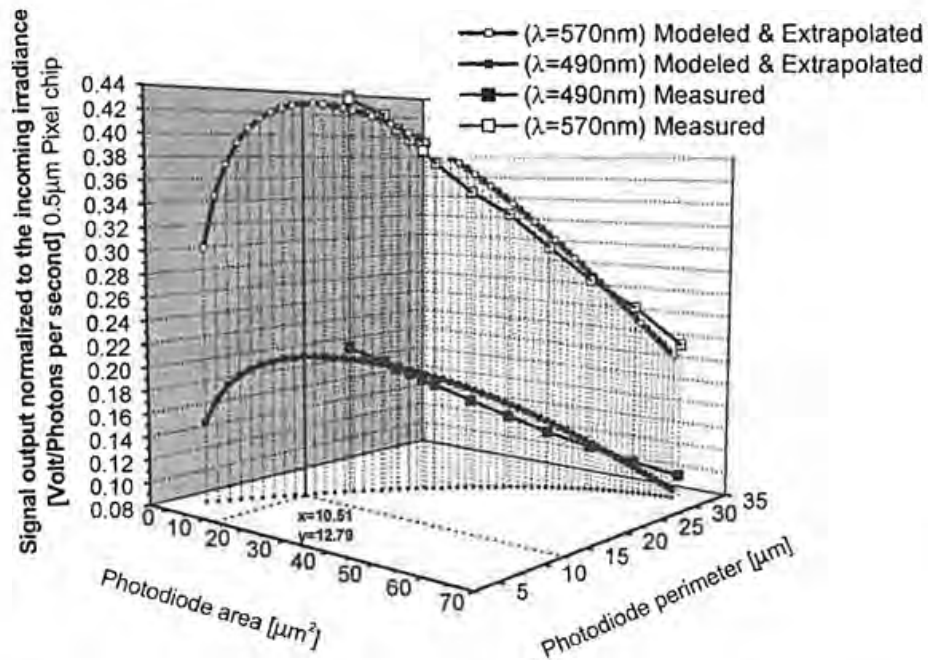


Figure 3-13. A comparison of the modeled results and the measured data at two different wavelengths for the pixel set represented in Figure 3-11. Extrapolation of the model predicted a photodiode area and perimeter corresponding to a pixel design that would enable maximum photoresponse. Note that the optimal pixel was not actually designed and measured, but rather its existence and geometric dimensions were revealed by extrapolation of the model.

specific process) enables the extrapolation of the modeled function and in turn the identification of the optimal photodiode geometry (for the rectangular pixel case, see Figure 3-13). Thus, the model theoretically predicts both the existence and the properties of the optimal geometry; (the optimal dimensions) based on the investigated process and the specific design data.

The total “main area” and total periphery contributions to the output signal have been examined separately as a function of the change in the photodiode dimensions. With a increase in the dimensions, the “main area” contribution drops and the periphery contribution rises such that they intercept. The interception point is at the exact location where the maximum output signal was predicted by extrapolation in Figure 3-13 for the particular scalable CMOS process (see Figure 3-14).

The overall influence of scaling on the device sensitivity is very complicated and depends on a large variety of parameters. An analytical expression that uniquely determines the general scaling trends has not yet been developed [26, 27]. An approximation is proposed to describe the scaling influence: it is assumed that the ratio between the unit “main area” and the unit “periphery” contributions has a slight upward trend, due

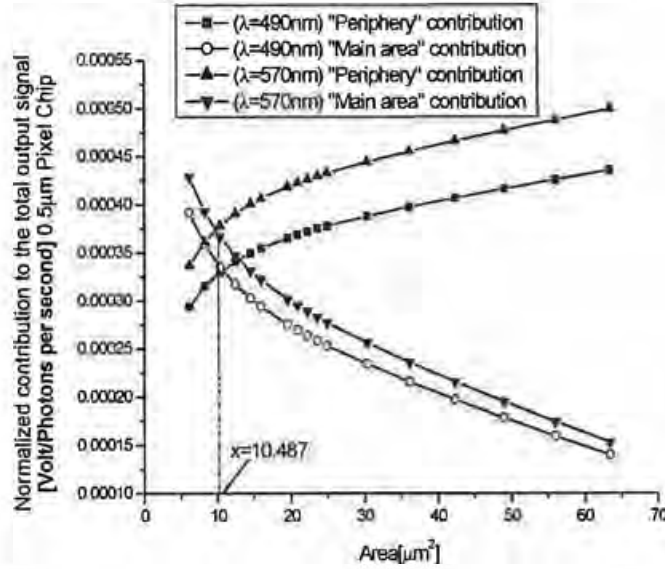


Figure 3-14. Total “main area” and periphery contributions to the output signal as a function of the change in the (rectangular) photodiode dimensions for the 0.5 μm CMOS pixel set presented in Figure 3-11. The interception point is at the exact location where the maximum output signal was predicted by extrapolation in Figure 3-13.

mostly to the reduction of mobility and lifetime with increasing doping levels and to shrinkage of the depletion widths. Under strong absorption conditions where the diffusion coefficient $\alpha(\lambda)$ and the diffusion length L_n are both much smaller than the substrate width, the photocurrent density due to diffusion in the substrate can be derived [26] as $J_{ph} = q \Phi / (1 + 1/\alpha(\lambda) L_n)$, where Φ is the photon flux entering the quasi-neutral p-substrate region and q is the electron charge. With technology downscaling, the unit “periphery” contribution to the output signal decreases. The depletion width shrinkage means that carriers are collected more through the bottom facet of the depletion region rather than through its lateral facets, intensifying therefore the relative “main area” contribution. In addition, the junction depth for advanced processes is small in comparison to the absorption depth, such that most photocarriers are collected through the bottom depletion facet. Based on the assumption above and using the process data and the extracted results (the coefficients k_1 and k_2 , i.e., determining the unit “main area” and the unit “periphery” contributions for each particular wavelength), it is possible to determine the coefficients k_1 and k_2 for the more advanced scalable CMOS technology. It is predicted that

$$\begin{aligned} k_1 / k_2 \Big|_{CMOS\ 0.35\mu m}^{570nm} &\approx k_1 / k_2 \Big|_{CMOS\ 0.5\mu m}^{570nm} \\ &\times \left(d_{CMOS\ 0.5\mu m} / d_{CMOS\ 0.35\mu m} \right) \cdot \left(L_{nCMOS\ 0.35\mu m} / L_{nCMOS\ 0.5\mu m} \right) \approx 1.12 \end{aligned} \quad (3.6)$$

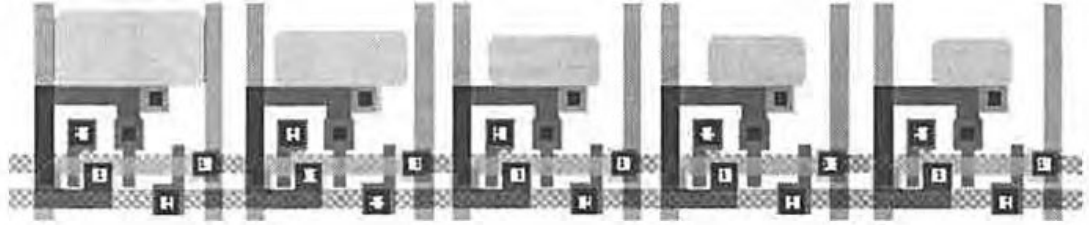


Figure 3-15. A subset of a rectangular-shaped active area pixel set with decreasing photodiode dimensions (CMOS 0.35 μm technology). The photodiode areas vary from 13.4 μm^2 down to 4.3 μm^2 and their perimeters vary from 15 μm down to 8.1 μm .

and

$$\begin{aligned} k_1 / k_2 \Big|_{\text{CMOS } 0.35 \mu\text{m}}^{490\text{nm}} &\approx k_1 / k_2 \Big|_{\text{CMOS } 0.5 \mu\text{m}}^{490\text{nm}} \\ &\times \left(d_{\text{CMOS } 0.5 \mu\text{m}} / d_{\text{CMOS } 0.35 \mu\text{m}} \right) \cdot \left(L n_{\text{CMOS } 0.35 \mu\text{m}} / L n_{\text{CMOS } 0.5 \mu\text{m}} \right) \approx 1.07 \end{aligned} \quad (3.7)$$

where d is the depletion depth.

An example calculation was performed for set of pixels of a rectangular photodiode shape designed according to the CMOS 0.35 μm rules and obeying the same mathematical guidelines as the older technology of pixels presented in Figure 3-12. An example subset of these newer pixels is shown in Figure 3-15. All the pixels share a common traditional three-transistor-type readout circuitry, enabling identification of the behavior of different pixel types.

The predictions of equations (3.6) and (3.7) were used to find a pixel that enabled maximum response. In Figure 3-16, the interception point of the calculated total “main area” and the total “periphery” contributions envisaged the maximum photoresponse pixel geometry for the pixel set designed and fabricated in the more advanced CMOS 0.35 μm technology design (shown in Figure 3-15).

Figure 3-17 shows the comparison between the measured and theoretically modeled output curves for several wavelengths of illumination where obvious maximum response geometry was indicated. Note that the modeled function (based on available process and design data) reaches its maximum exactly at the point marked by the measurements. Moreover, the values obtained from the measurements of the contributions ratio are

$$k_1 / k_2 \Big|_{\text{CMOS } 0.35 \mu\text{m}}^{570\text{nm}} \approx 1.13 \quad (3.8)$$

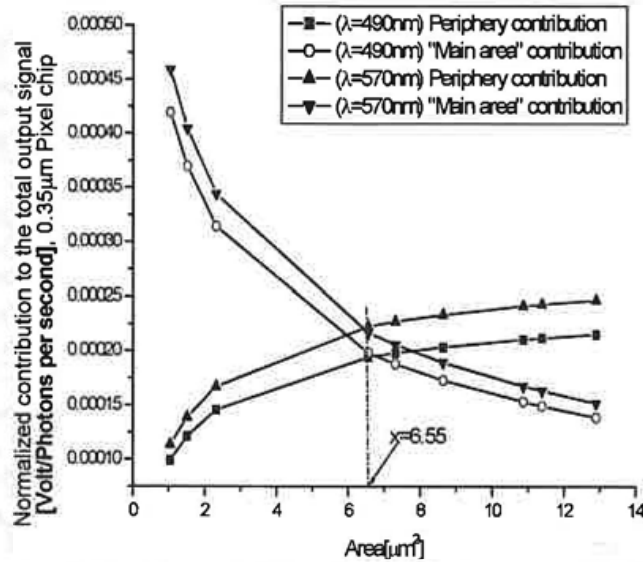


Figure 3-16. Total “main area” and periphery contributions to the output signal as a function of the changes in the photodiode dimensions for the 0.35 μm CMOS pixel set presented in Figure 3-15. Note that this result is obtained theoretically, based only on the experimental results obtained from an older CMOS process and scaling considerations.

and

$$k_1 / k_2 \Big|_{CMOS, 0.35 \mu m}^{490 nm} \approx 1.068 \quad (3.9)$$

These are similar to our theoretical results in equations (3.6) and (3.7). The maximum occurs exactly at the previously predicted interception point (Figure 3-16).

The theoretical result described here was obtained for the 0.35 μm CMOS design based only on the parameters extracted from the available design and process data; i.e., there was no need for an actual study with a 0.35 μm test chip. The optimum geometry, or the pixel that enabled the maximum photoresponse, was predicted theoretically based only on the experimental results obtained from older process data and scaling considerations. The measurements confirmed the theoretical prediction.

This model for photoresponse estimation of a photodiode based CMOS APS field of applicability does not appear to be constrained by a specific technology process. It can therefore be used as a predictive tool for design optimization of each potential application in scalable CMOS technologies.

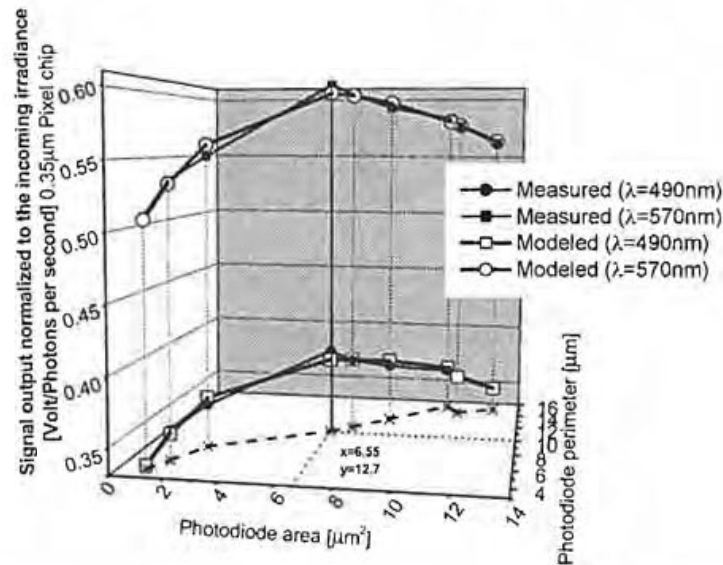


Figure 3-17. A comparison of the modeled and the measured results obtained for the pixels presented in Figure 3-15 at two different wavelengths of illumination. The geometry of the pixel that enabled maximum photoresponse is indicated. The maximum occurred exactly at the interception point indicated in Figure 3-16; i.e., the theoretically predicted result was confirmed by the measurements.

3.5 Summary

A closed-form semi-analytical expression has been presented for diffusion-limited CMOS APS pixel photosignal in a closely spaced photodiode array. This expression represents the pixel photosignal dependence on the pixel geometrical shape and fill factor, i.e., the photodiode active area and perimeter. It enables identification of the behavior of different pixel types and shows how changes in the device geometry affect its overall performance. In addition, the expression introduces a method for the determination and prediction of CMOS photodiode quantum efficiency based on the process and design data.

The results indicate that the tradeoffs between conflicting factors (such as integration photocarriers and conversion gain) can be compared for each potential pixel design, and a reliable estimate for optimum overall sensor performance is possible.

The model clearly makes possible the theoretical prediction of pixel designs that enable the extraction of maximum output signal for any selected photodiode shape. This prediction is based only on the usual process and design data available for different scalable CMOS technologies, and thus can be a practical tool for design optimization.

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Chapter 4

ACTIVE PIXEL SENSOR DESIGN: FROM PIXELS TO SYSTEMS

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Abstract: Since active pixel sensors (APS) are fabricated in a commonly used CMOS process, image sensors with integrated "intelligence" can be designed. These sensors are very useful in many scientific, commercial and consumer applications. Current state-of-the-art CMOS imagers allow integration of all functions required for timing, exposure control, color processing, image enhancement, image compression, and ADC on the same die. In addition, CMOS imagers offer significant advantages and rival traditional charge coupled devices (CCDs) in terms of low power, low voltage and monolithic integration. This chapter presents different types of CMOS pixels and introduces the system-on-a-chip approach, showing examples of two "smart" APS imagers. The camera-on-a-chip approach is introduced, focusing on the advantages of CMOS sensors on CCDs. Different types of image sensors are described and their modes of operation briefly explained. Two examples of CMOS imagers are presented, a smart vision system-on-a-chip and a smart tracking sensor. The former is based on a photodiode APS with linear output over a wide dynamic range, made possible by random access to each pixel and by the insertion of additional circuitry into the pixels. The latter is a smart tracking sensor employing analog non-linear winner-take-all (WTA) selection.

Key words: CMOS image sensor, active pixel sensor (APS), charge-coupled devices (CCD), passive pixel (PS), system-on-a-chip, smart sensor, dynamic range (DR), winner-take-all (WTA) circuit.

4.1 Introduction

Driven by the demands of multimedia applications, image sensors have become a major category of high-volume semiconductor production. The introduction of imaging devices is imminent in consumer applications such

as cell phones, automobiles, computer-based video, smart toys and both still and video digital cameras.

In addition to image capture, the electronics in a digital camera must handle analog-to-digital (ADC) conversion as well as a significant amount of digital processing for color imaging, image enhancement, compression control and interfacing. These functions are usually implemented with many chips fabricated in different process technologies.

The continuous advances in CMOS technology for processors and DRAMs have made CMOS sensor arrays a viable alternative to the popular charge-coupled devices (CCD) sensor technology. New technologies provide the potential for integrating all imaging and processing functions onto a single chip, greatly reducing the cost, power consumption and size of the camera [1–3]. Standard CMOS mixed-signal technology allows the manufacture of monolithically integrated imaging devices: all the functions for timing, exposure control and ADC can be implemented on one piece of silicon, enabling the production of the so-called “camera-on-a-chip” [4]. *Figure 4-1* is a diagram of a typical digital camera system, showing the difference between the building blocks of commonly used CCD cameras and the CMOS camera-on-a-chip. The traditional imaging pipeline functions—such as color processing, image enhancement and image compression—can also be integrated into the camera. This enables quick processing and exchanging of images. The unique features of CMOS digital cameras allow many new applications, including network teleconferencing, videophones, guidance and navigation, automotive imaging systems, and robotic and machine vision.

Most digital cameras currently use CCDs to implement the image sensor. State-of-the-art CCD imagers are based on a mature technology and present excellent performance and image quality. They are still unsurpassed for high sensitivity and long exposure time, thanks to extremely low noise, high quantum efficiency and very high fill factors. Unfortunately, CCDs need specialized clock drivers that must provide clocking signals with relatively large amplitudes (up to 10 V) and well-defined shapes. Multiple supply and bias voltages at non-standard values (up to 15 V) are often necessary, resulting in very complex systems.

Figure 4-2 is a block diagram of a widely used interline transfer CCD image sensor. In such sensors, incident photons are converted to charge, which is accumulated by the photodetectors during exposure time. In the subsequent readout time, the accumulated charge is sequentially transferred into the vertical and horizontal CCDs and then shifted to the chip-level output amplifier. However, the sequential readout of pixel charge limits the readout speed. Furthermore, CCDs are high-capacitance devices and during

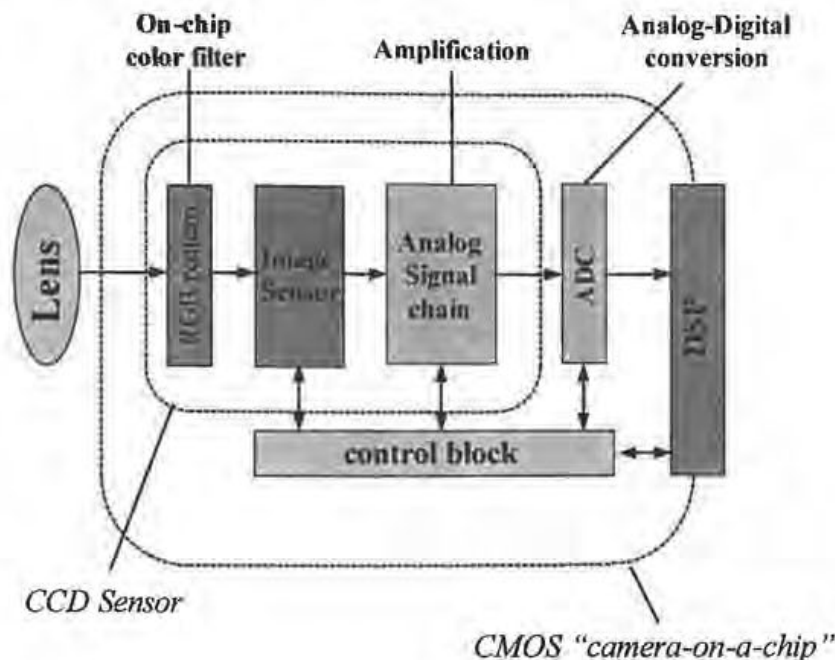


Figure 4-1. Block diagram of a typical digital camera system.

readout, all the capacitors are switched at the same time with high voltages; as a result, CCD image sensors usually consume a great deal of power. CCDs also cannot easily be integrated with CMOS circuits due to additional fabrication complexity and increased cost. Because it is very difficult to integrate all camera functions onto a single CCD chip, multiple chips must be used. A regular digital camera based on CCD image sensors is therefore burdened with high power consumption, large size and a relatively complex design; consequently, it is not well suited for portable imaging applications.

Unlike CCD image sensors, CMOS imagers use digital memory style readout, using row decoders and column amplifiers. This readout overcomes many of the problems found with CCD image sensors: readout can be very fast, it can consume very little power, and random access of pixel values is possible so that selective readout of windows of interest is allowed. *Figure 4-3* shows the block diagram of a typical CMOS image sensor.

The power consumption of the overall system can be reduced because many of the supporting external electronic components required by a CCD sensor can be fabricated directly inside a CMOS sensor. Low power consumption helps to reduce the temperature (or the temperature gradient) of both the sensor and the camera head, leading to improved performance.

An additional advantage of CMOS imagers is that analog signal processing can be integrated onto the same substrate; this has already been demonstrated by some video camera-on-a-chip systems. Analog signal

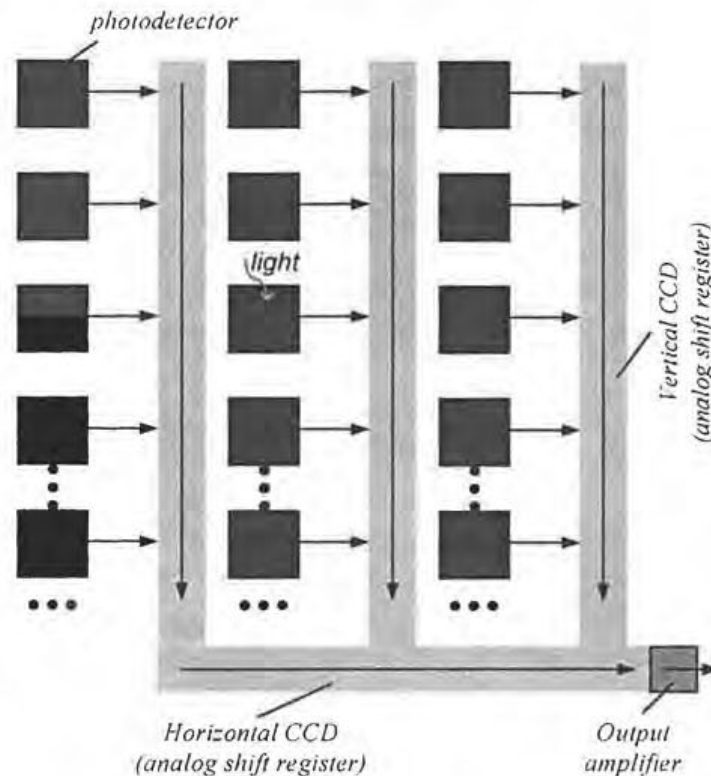


Figure 4-2. Block diagram of a typical interline transfer CCD image sensor.

processing can include widening the dynamic range of the sensor, real-time object tracking, edge detection, motion detection and image compression. These functions are usually performed by nonlinear analog circuits and can be implemented inside the pixels and in the periphery of the array. Offloading signal processing functions makes more memory and DSP processing time available for higher-level tasks, such as image segmentation or tasks unrelated to imaging.

This chapter presents a variety of implementations of CMOS image sensors, focusing on two examples of system-on-a-chip design: an image sensor with wide dynamic range (DR) [5] and a tracking CMOS imager employing analog winner-take-all (WTA) selection [6].

4.2 CMOS image sensors

CMOS pixels can be divided into two main groups, passive pixel sensors (PPS) and active pixel sensors (APS).

Each individual pixel of a PPS array has only a photosensing element (usually a photodiode) and a switching MOSFET. The signal is detected

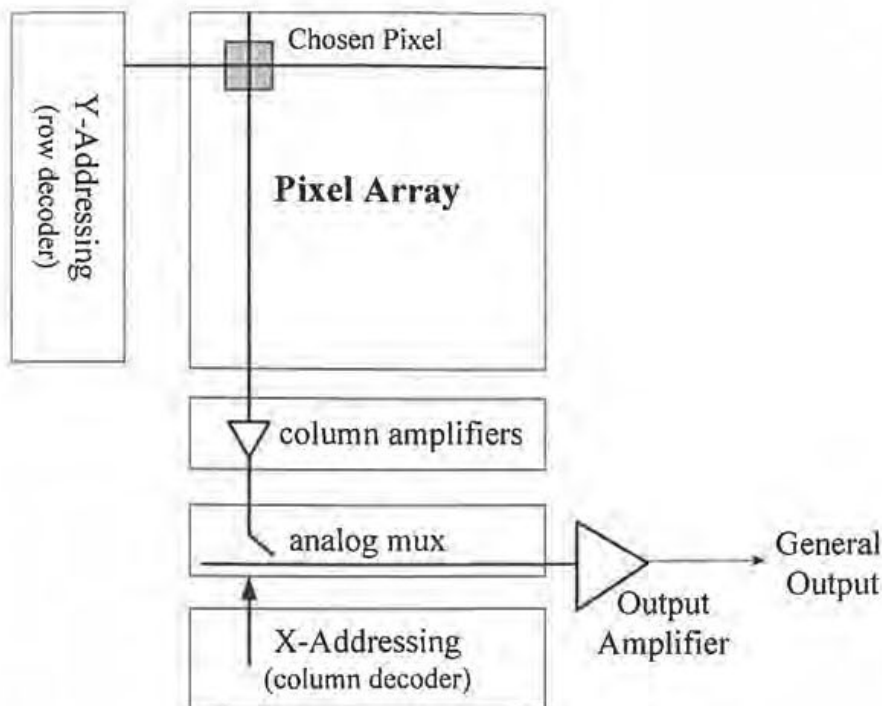


Figure 4-3. Block diagram of a typical CMOS image sensor.

either by an output amplifier implemented in each column or by a single output for the entire imaging device. These conventional MOS-array sensors operate like an analog DRAM, offering the advantage of random access to the individual pixels. They suffer from relatively poor noise performance and reduced sensitivity compared to state-of-the-art CCD sensors.

APS arrays are novel image sensors that have amplifiers implemented in every pixel; this significantly improves the noise parameter.

4.2.1 Passive Pixel Sensors

The PPS consists of a photodiode and just one transistor (labeled *TX* in Figure 4-4). *TX* is used as a charge gate, switching the contents of the pixel to the charge integration amplifier (CIA). These passive pixel CMOS sensors operate like analog DRAMs, as shown in Figure 4-5.

More modern PPS implementations use a CIA for each column in the array, as shown in Figure 4-6. The CIA readout circuit is located at the bottom of each column bus (to keep the voltage on that bus constant) and uses just one addressing transistor. The voltage V_{ref} is used to reset the photo-diode to reverse bias. Following the reset, this switch is opened, for a period of integration time (T_{int}). During this period, the photodiode discharges at a rate approximately proportional to the amount of incident

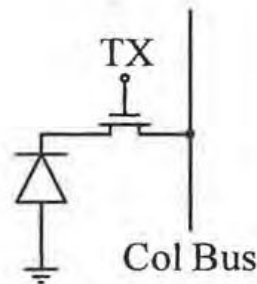


Figure 4-4. Passive pixel sensor structure.

illumination. When the MOS switch is closed again to reset the photodiode once more, a current flows via the resistance and capacitance of the column bus due to the difference between V_{ref} and the voltage on the diode (V_{diode}). The total charge that flows to reset the pixel is equal to that discharged during the integration period. This charge is integrated on the capacitor C_{int} and output as a voltage. When the final bus and diode voltages return to V_{ref} via the charge amplifier, the address MOS switch is turned off, the voltage across C_{int} is removed by the *Reset* transistor, and the integration process starts again.

The passive pixel structure has major problems due to its large capacitive loads. Since the large bus is directly connected to each pixel during readout,

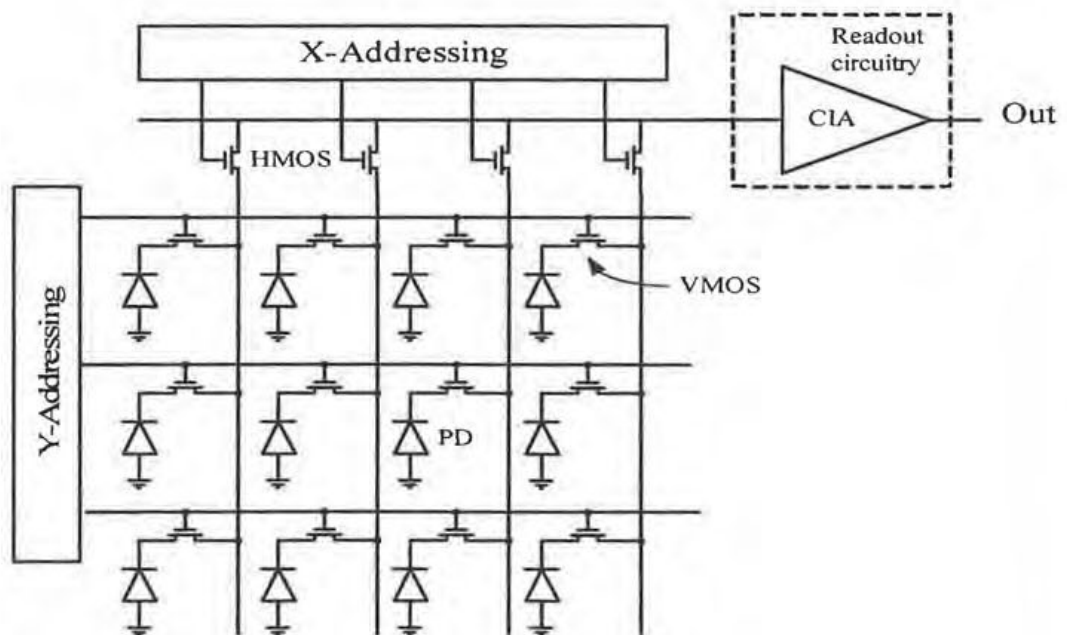


Figure 4-5. Basic PPS architecture.

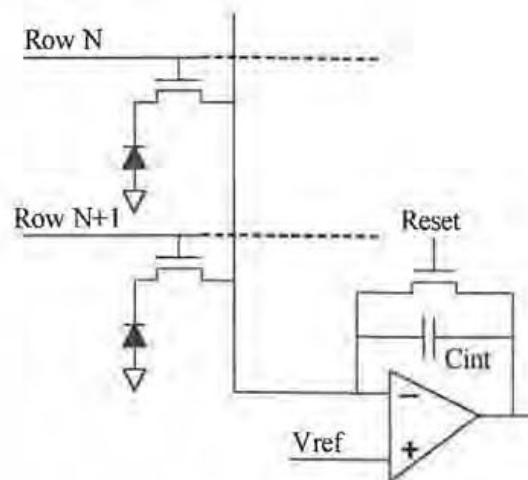


Figure 4-6. PPS implementation with a separate CIA for each column in the array (after [13]).

the RC time constant is very high and the readout is slow. In addition, passive pixel readout noise is typically high—on the order of 250 electrons rms compared to less than 10 electrons rms for commercial CCDs. Because of these factors, PPS does not scale well to larger array sizes or faster pixel readout rates. Furthermore, differences between the individual amplifiers at the bottoms of the different columns will cause fixed pattern noise (FPN). FPN is time-independent and arises from component mismatch due to variations in lithography, doping and other manufacturing processes.

PPS also offers advantages. For a given pixel size, it has the highest design fill factor (the ratio of the light sensitive area of a pixel to its total area), since each pixel has only one transistor. In addition, its quantum efficiency (QE)—the ratio between the number of generated electrons and the number of impinging photons—can be quite high due to this large fill factor.

4.2.2 Active Pixel Sensors

The passive pixel sensor was introduced by Weckler in 1967 [7]. The problems of PPS were recognized, and consequently a sensor with an active amplifier (a source follower transistor) within each pixel was proposed [8]. The current term for this technology, active pixel sensor, was first introduced by Fossum in 1992 [1]. Figure 4-7 shows the general architecture of an APS array and the principal pixel structure. A detailed description of the readout procedure will be presented later in this chapter.

Active pixels typically have a fill factor of only 50–70%, which reduces the photon-generated signal. However, the reduced capacitance in each pixel

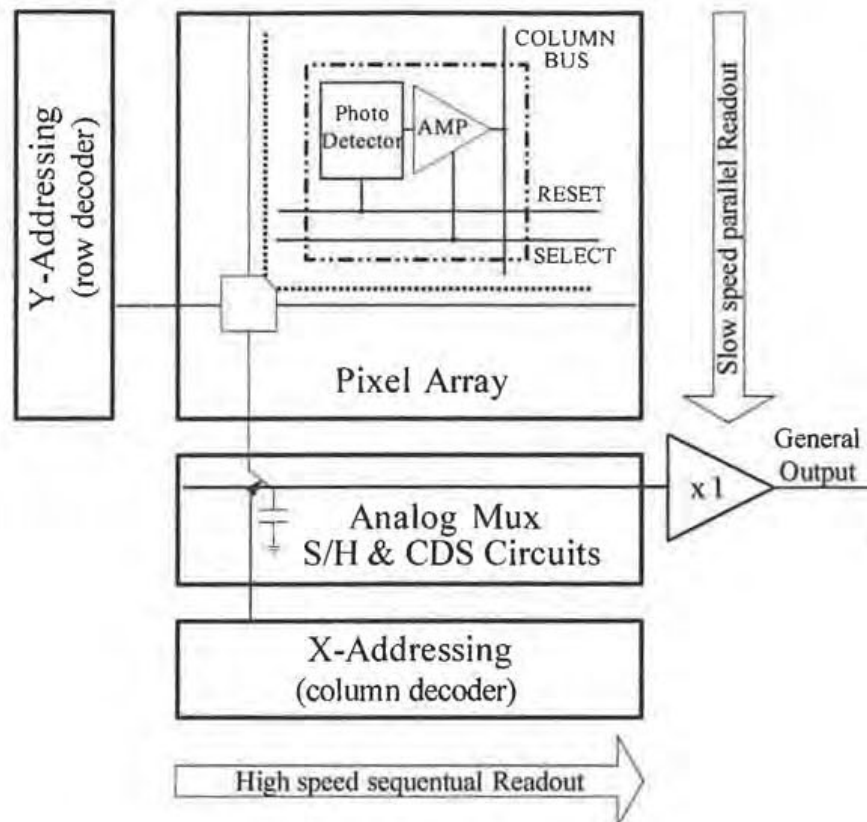


Figure 4-7. General architecture of an APS array.

leads to lower read noise for the array, which increases both the dynamic range and the signal-to-noise ratio (SNR).

The pixels used in these sensors can be divided into three types: photodiodes, photogates, and pinned photodiodes. The most popular is currently the photodiode.

4.2.3 Photodiode APS

The photodiode APS was described by Noble in 1968 [8] and has been under investigation by Andoh since the late 1980s [9]. A novel technique for random access and electronic shuttering with this type of pixel was proposed by Yadid-Pecht in the early 1990s [12].

The basic photodiode APS employs a photodiode and a readout circuit of three transistors: a photodiode reset transistor (*Reset*), a row select transistor (*RS*) and a source-follower transistor (*SF*). The scheme of this pixel is shown in Figure 4-8.

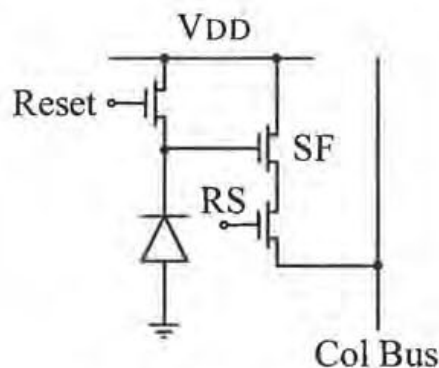


Figure 4-8. Basic photodiode APS pixel.

The charge-to-voltage conversion occurs at the sense node capacitance, which comprises the photodiode capacitance and all other parasitic capacitances connected to that node. In this case, these are the source capacitance of the *Reset* transistor and the gate capacitance of the *SF* transistor. The *SF* transistor acts as a buffer amplifier to isolate the sensing node; the load of this buffer (the active-current-source load) is located on each column rather than on each pixel to keep the fill factor high and to reduce pixel-to-pixel variations. The *Reset* transistor controls an integration time and is usually implemented with an NMOS transistor. Since no additional well is required for NMOS implementation, this allows a higher fill factor. However, an NMOS transistor with V_{DD} on both gate and drain can only reach a source voltage (at the photodiode node) of $V_{DD} - V_T$, thereby decreasing the dynamic range of the pixel. An example of a mask layout for this pixel architecture is shown in Figure 4-9.

Photodiode APS operation and readout are described here with reference to both Figure 4-7 and Figure 4-8. Generally, pixel operation can be divided into two main stages, reset and phototransduction.

(a) *The reset stage.* During this stage, the photodiode capacitance is charged to a reset voltage by turning on the *Reset* transistor. This reset voltage is read out to one of sample-and-hold (S/H) in a correlated double sampling (CDS) circuit. The CDS circuit, usually located at the bottom of each column, subtracts the signal pixel value from the reset value. Its main purpose is to eliminate fixed pattern noise caused by random variations in the threshold voltage of the reset and pixel amplifier transistors, variations in the photodetector geometry and variations in the dark current. In addition, it should eliminate the $1/f$ noise in the circuit.

(b) *The phototransduction stage.* During this stage, the photodiode capacitor is discharged through a constant integration time at a rate

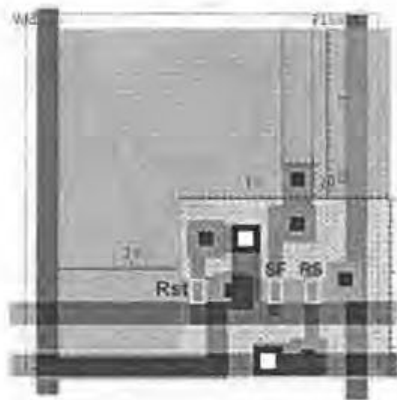


Figure 4-9. An example of a pixel layout with an L-shaped active area, which is the most common pixel design.

approximately proportional to the incident illumination. Therefore, a bright pixel produces a low analog signal voltage and a background pixel gives a high signal voltage. This voltage is read out to the second S/H of the CDS by enabling the row select transistor of the pixel. The CDS outputs the difference between the reset voltage level and the photovoltage level.

Because the readout of all pixels cannot be performed in parallel, a rolling readout technique is applied. All the pixels in each row are reset and read out in parallel, but the different rows are processed sequentially. *Figure 4-10* shows the time dependence of the rolling readout principle. A given row is accessed only once during the frame time (T_{frame}). The actual pixel operation sequence is in three steps: the accumulated signal value of the previous frame is read out, the pixel is reset, and the reset value is read out to the CDS. Thus, the CDS circuit actually subtracts the signal pixel value from the reset value of the next frame. Because CDS is not truly correlated without frame memory, the read noise is limited by the reset noise on the photodiode. After the signals and resets of all pixels in the row are read out to S/H, the outputs of all CDS circuits are sequentially read out using X-addressing circuitry, as shown in *Figure 4-7*.

The output photodiode signal is supposedly independent of detector size, because the lower pixel capacitance of smaller detectors causes an increase in conversion gain that compensates for the decrease in detector size. However, peripheral capacitances from the perimeters of the detector increase the total capacitance of the sensing node and thus decrease the conversion gain. As the pixel size scales down, photosensitivity decreases and the reset noise scales as $C^{1/2}$, where C is the photodiode capacitance. These tradeoffs must be considered when designing pixel fill factor, DR, SNR and conversion gain.

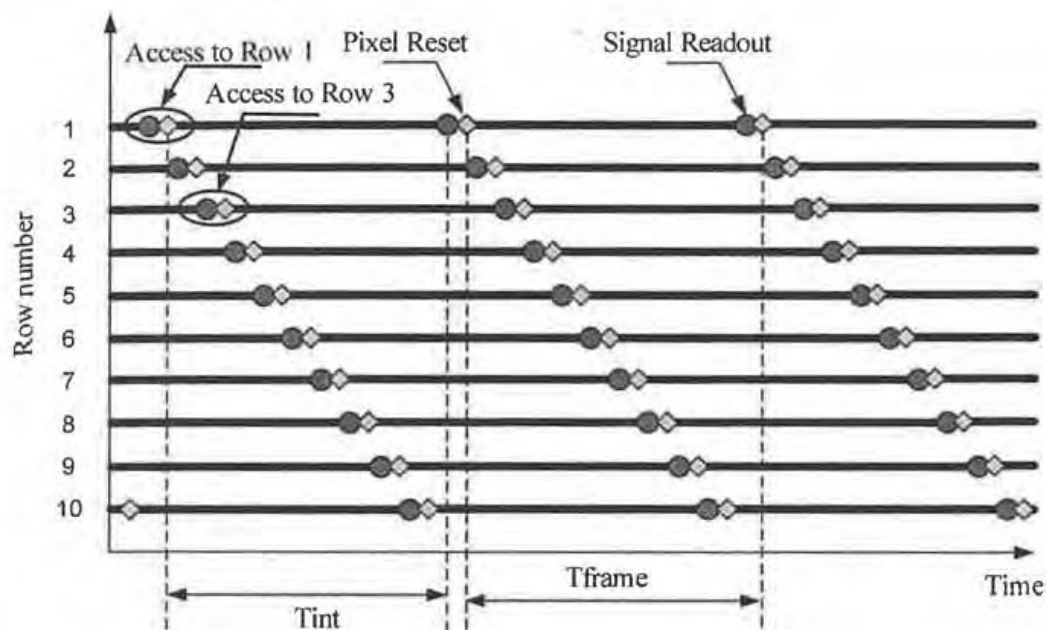


Figure 4-10. Rolling readout principle of the photodiode APS.

4.2.4 Photogate APS

Figure 4-11 shows the common photogate pixel architecture [10]. The basic concept for the photogate pixel arose from CCD technology. While photon-generated charge is integrated under a photogate with a high potential well, the output floating node is reset and the corresponding voltage is read out to the S/H of the CDS. When the integration is completed, the charge is transferred to the output floating node by pulsing the signal on the photogate. Then the corresponding voltage from the

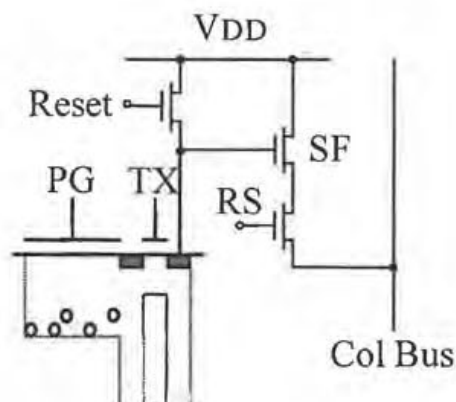


Figure 4-11. Basic photogate pixel architecture.

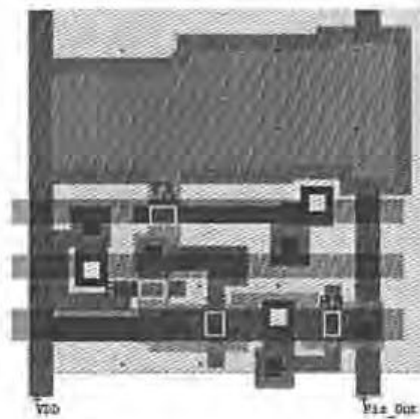


Figure 4-12. Example layout of a photogate pixel design.

integrated charge is read by the source follower to the second S/H of the CDS. The CDS outputs the difference between the reset voltage level and the photo-voltage level.

As mentioned above, the CDS can suppress reset noise, $1/f$ noise and FPN due to V_T and lithographic variations in the array. The reduction of noise level increases the total dynamic range and the SNR. The primary noise source for the photogate APS is photon shot noise, which cannot be suppressed by any means.

The photogate has a pixel pitch typically equal to 20 times the minimum size of the technology, since there are five transistors in each pixel. Due to the overlaying polysilicon, however, there is a reduction in QE, particularly in the blue region of the spectrum. The photogate pixel architecture is shown as a mask layout in Figure 4-12.

4.2.5 Pinned photodiode APS

The pinned photodiode pixel consists of a pinned diode (p^+n-p), where the photon collection area is dragged away from the surface in order to reduce surface defect noise (such as that due to dark current) [13]. Photon-generated charge is integrated under a pinned diode and transferred to the output floating diffusion for the readout. As in the photogate APS, the sense node and integration node are separated to minimize noise. However, the primary difference is that the potential well for charge collection in a pinned diode is generated by a buried intrinsic layer (or an n -type layer) instead of a pulsed gate voltage as in the photogate. Each pinned diode pixel has four transistors and five control lines, resulting in a fill factor higher than in the photogate pixel, but lower than in the photodiode pixel. However, the small photon collection area of the pinned diode results in a very small full well

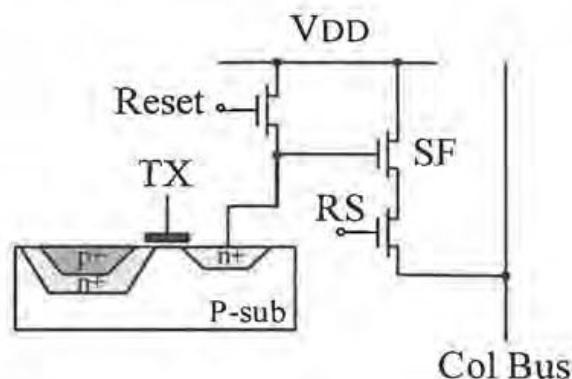


Figure 4-13. Basic pinned photodiode pixel architecture.

for photon-generated charge collection and lower QE compared to the photodiode pixel. Figure 4-13 shows a basic pinned photodiode pixel structure.

4.2.6 Logarithmic Photodiode APS

Another type of APS is a logarithmic photodiode sensor [11]. This three-transistor pixel enables logarithmic encoding of the photocurrent, thus increasing the dynamic range of the sensor; i.e., the same range of sensor output voltage is suitable for a wider range of illumination. The implementation of the basic logarithmic photodiode pixel is described in Figure 4-14.

This pixel does not require reset and operates continuously. The voltage on the photodiode (V_{PH}) is approximately equal to V_{DD} , causing the load transistor to operate in the subthreshold region ($V_{DD} = V_{PH} + \Delta V_{PH}$). The

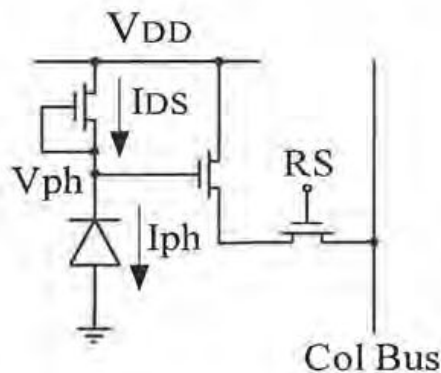


Figure 4-14. Basic logarithmic photodiode pixel architecture.

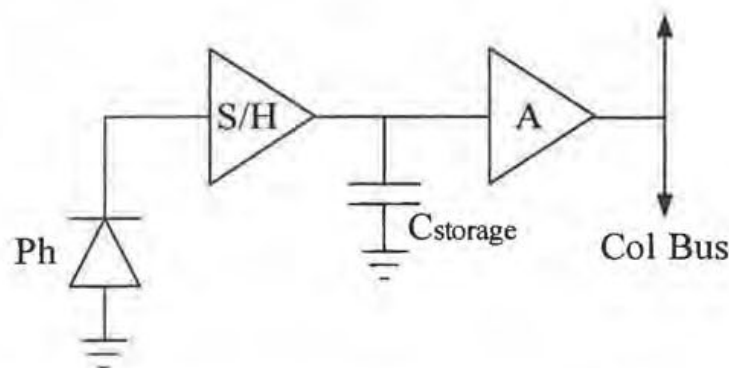


Figure 4-15. Architecture of a snapshot photodiode APS (after [12]).

photocurrent (I_{PH}) is equal to the subthreshold current (I_{DS}). The voltage on the photodiode decreases logarithmically with linear increases in illumination (and thus photocurrent) following the equation

$$V_{PH} = V_{DD} - \Delta V_{PH} = V_{DD} - \frac{KT}{q} \cdot \ln \left(\frac{I_{PH}}{I_0} \right) \quad (4.1)$$

where KT/q is 0.026 V at $T=300$ K and I_0 represents all constant terms. While the logarithmic APS has the above-mentioned advantages, it suffers from serious drawbacks such as significant temperature dependence of the output, low swing of the output (especially for relatively low illumination levels) and high FPN. Accordingly, the logarithmic APS is not commonly used.

4.2.7 Snapshot pixels

Most CMOS imagers feature the rolling shutter readout method (also known as the rolling readout method) shown in Figure 4-10. In the rolling shutter approach, the start and end of the light collection for each row is slightly delayed from the previous row; this leads to image deformity when there is relative motion between the imager and the scene. The ideal solution for imaging objects moving at high speed is the snapshot imager, which employs the electronic global shutter method [12]. This technique uses a memory element inside each pixel and provides capabilities similar to a mechanical shutter: it allows simultaneous integration of the entire pixel array and then stops the exposure while the image data is read out. The principal scheme of snapshot photodiode APS was introduced by Yadid-Pecht in 1991, and is shown in Figure 4-15.

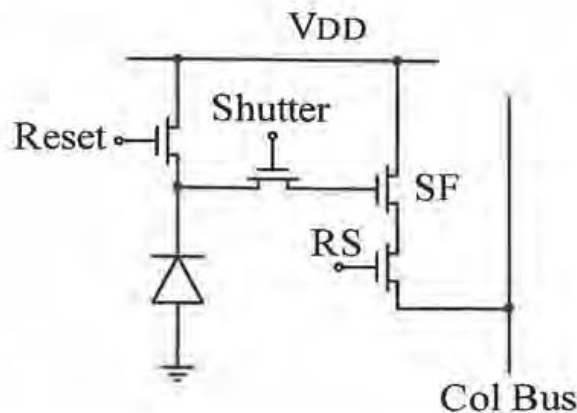


Figure 4-16. Transistor scheme of a commonly used snapshot pixel.

The snapshot pixel includes a sample-and-hold (S/H) switch with analog storage, which consists of all parasitic capacitances in the amplifier input. The in-pixel amplification is performed by a source follower amplifier, identical to that in a rolling shutter pixel. The full transistor scheme of a commonly used global shutter pixel is shown in *Figure 4-16*.

In contrast to the rolling shutter technique, a sensor with global shutter architecture exposes all its pixels at the same time. After the integration time T_{int} , the signal charge is stored in an in-pixel sample-and-hold capacitance until readout. One of the problems that should be addressed in the snapshot pixels is the shutter efficiency. The light exposure of the S/H stage, shutter leakage and the limited storage capacitance lead to signal loss. *Figure 4-16* shows a pixel that employs an NMOS transistor as a shutter. This implementation allows a small pixel area, but it has a low shutter efficiency. Shutter efficiency can be increased using a PMOS transistor as a shutter, if it is well separated from the photodiode. Unfortunately, a PMOS shutter decreases the fill factor and, due to increased parasitic capacitances, also decreases the conversion gain.

4.3 APS system-on-a-chip approach

CMOS image sensors allow implementations of complex sensing systems on a single silicon die. For example, almost all CMOS imagers employ analog to digital conversion on the same die. There are three general approaches to implementing ADC with active pixel sensors:

1. *Chip-level ADC*, where a single ADC circuit serves the whole APS array. This method requires a very high-speed ADC, especially if a very large array is used.
2. *Column-level ADC*, where an array of ADCs is placed at the bottom of the APS array and each ADC is dedicated to one or more columns

of the APS array. All these ADCs are operated in parallel, so a low-to-medium-speed ADC design can be used, depending on the APS array size. The disadvantages of this approach are the necessity of fitting each ADC within the pixel pitch (i.e., the column width) and the possible problems of mismatch among the converters on different columns.

3. *Pixel-level ADC*, where every pixel has its own converter. This approach allows parallel operation of all ADCs in the APS array, so a very low speed ADC is suitable. Using one ADC per pixel has additional advantages, such as higher SNR, lower power and simpler design.

In this section, two examples of CMOS imagers are described. The first implements a “smart vision” system-on-a-chip based on a photodiode APS with linear output over a wide dynamic range. An increase in the dynamic range of the sensors is enabled by random access to the pixel array and by the insertion of additional circuitry within each pixel. The second example is a smart tracking sensor employing analog nonlinear winner-take-all selection.

In the design of a “smart” sensing system, an important step is to decide whether computation circuitry should be inserted within the pixel or placed in the periphery of the array. When processing circuitry is put within the pixel, additional functions can be implemented, simple 2-D processing is possible, and neighboring pixels can be easily shared in neural networks. These systems are also very useful for real-time applications. On the other hand, the fill factor is drastically reduced, making these systems unsuitable for applications where high spatial resolution and very high image quality are required. In all systems presented later in this chapter, most of the processing circuitry is placed in the periphery of the array to avoid degradation of image quality.

4.3.1 Autoscaling APS with customized increase of dynamic range

This section introduces the reader to the dynamic range problem in CMOS imagers, showing possible existing solutions. Then an advanced autoscaling CMOS APS with customized linear increase of DR is explained.

4.3.1.1 Dynamic range problem and possible solutions

Scenes imaged with electronic cameras can have a wide range of illumination. Levels can range from 10^{-3} lux for night vision to 10^5 lux for scenes illuminated with bright sunlight, and even higher levels can occur with the direct viewing of light sources such as oncoming headlights. The

intrascene dynamic range capability of a sensor is measured as

$$DR = 20 \cdot \log(S/N) \quad (4.2)$$

where S is the saturation level and N is the root mean square (rms) read noise floor measured in electrons or volts. The human eye has a dynamic range of about 90 dB and camera film of about 80 dB, but typical CCDs and CMOS APS have a dynamic range of only 65–75 dB. Generally, dynamic range can be increased in two ways: the first one is noise reduction and thus expanding the dynamic range toward darker scenes. The second method is incident light saturation level expansion, thus improving the dynamic range toward brighter scenes.

Bright scenes and wide variations in intrascene illumination can arise in many situations: driving at night, photographing people in front of a window, observing an aircraft landing at night, and imaging objects for studies in meteorology or astronomy. Various solutions have been proposed in both CCD and CMOS technologies to cope with this problem [13–37]. Methods for widening the dynamic range can be grouped into five areas:

1. *Companing sensors*, such as logarithmic compressed-response photodetectors;
2. *Multi-mode sensors*, where operation modes are changed;
3. *Frequency-based sensors*, where the sensor output is converted to pulse frequency;
4. *Sensors with external control over integration time*, which can be further divided into global control (where the integration time of the whole sensor can be controlled) and local control (where different areas within the sensor can have different exposure times); and
5. *Sensors with autonomous control over integration time*, in which the sensor itself provides the means for different integration times.

Companing sensors. The simplest solution to increase DR is to compress the response curve using a logarithmic photodiode sensor, as described in section 4.2.6. Another type of companing sensor for widening the DR was introduced by Mead [16], where a parasitic vertical bipolar transistor with a logarithmic response was used. The logarithmic function there is again a result of the subthreshold operation of the diode-connected MOS transistors, added in series to the bipolar transistor. The voltage output of this photoreceptor is logarithmic over four or five orders of magnitude of incoming light intensity. It has been used successfully by Mahowald and Boahen [17]. This detector operates in the subthreshold region and has a low output voltage swing. A disadvantage of these pixels is that this form of

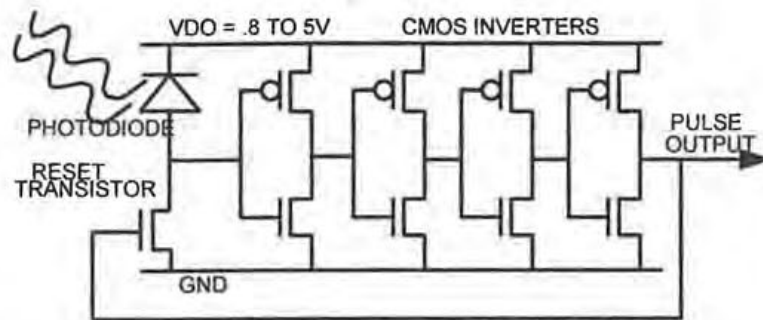


Figure 4-17. A pulse photosensor with reset circuitry (after Yang).

compression leads to low contrast and loss of details; adaptation, where linearity around the operation point is exploited, was proposed to alleviate this problem [19–20]. In addition, the response of the logarithmic pixels with this kind of readout is light dependent. This means that for low light intensities the readout time would be very slow, depending also on the photodiode capacitance.

Multimode sensors. A multisensitivity photodetector was proposed by Ward et al. [21]. The detector is a parasitic vertical bipolar transistor between diffusion, well and substrate. By connecting a MOS transistor to the base and the emitter of the bipolar transistor in a Darlington structure, the current gain can be boosted further. Thus, both bipolar transistors can be activated at very low light intensities and inactivated at higher intensities. For moderate levels, only one bipolar transistor is activated. Two selection transistors are required within the pixel for choosing the mode. This pixel occupies a relatively large area.

Frequency-based sensors. In 1994, Yang [22] proposed a pulse photosensor that uses simple integrate-and-reset circuitry to directly convert optical energy into a pulse frequency output. The output of this photosensor can vary over 5–6 orders of magnitude and is linearly proportional to optical energy. A diagram of the circuitry is presented in Figure 4-17.

The pixel fill factor is much decreased with this approach, since the inverter chain resides next to the photodiode. In addition, the pulse timing relies on the threshold voltages of the inverters. Since threshold voltage mismatches exists between different transistors, there will be a different response for each pixel. This makes this sensor worse in terms of noise, since the threshold mismatch translates to a multiplicative error (the output frequency of the pulses is affected) and not just constant FPN.

Sensors with external control over integration time. A multiple-integration-time photoreceptor has been developed at Carnegie Mellon University [23]. It has multiple integration periods, which are chosen

depending upon light intensity to avoid saturation. When the charge level nears saturation, the integration is stopped at one of these integration periods and the integration time is recorded. This sensor has a very low fill factor.

Sensors with autonomous control over integration time. The automatic wide-dynamic-range sensor was proposed by Yadid-Pecht [24, 25]. This imager consisted of a two-dimensional array of sensors, with each sensor capable of being exposed for a different length of time with autonomous on-chip control. Reset enable pulses are generated at specific times during the integration period. At each reset enable point, a nondestructive readout is performed on the sensor and compared to a threshold value. A conditional reset pulse is generated if the sensor value exceeds the threshold voltage. The main drawback with this solution is the extent of the additional circuitry, which affects spatial resolution.

In the following sections, we describe an APS with an in-pixel autoexposure and a wide-dynamic-range linear output. Only a minimum additional area above the basic APS transistors is required within the pixel, and the dynamic range enhancement is achieved with minimal effects on the temporal resolution.

4.3.1.2 System architecture

The architecture of the DR approach is shown in *Figure 4-18*. As in a traditional rolling-shutter APS, this imager is constructed of a two-dimensional pixel array, here of 64 columns and 64 rows, with random pixel access capability. Each pixel contains an optical sensor to receive light, a reset input and an electrical output representing the illumination received. The pixel used here is not a classic pixel, since it enables individual pixel reset via an additional transistor [5]. The outputs of a selected row are read through the column-parallel signal chain, and at certain points in time are also compared with an appropriate threshold in the comparison circuits. If a pixel value exceeds the threshold, a reset is given at that time to that pixel. The binary information concerning the reset (i.e., applied or not) is saved in digital storage for the later calculation of the scaling factor. The pixel value can then be determined as a floating-point number, where the exponent comes from the scaling factor for the actual integration time and the mantissa from the regular A/D output. Therefore, the actual pixel value would be

$$Value = Man \cdot \left(T / \left(T / X^{EXP} \right) \right) = Man \cdot X^{EXP} \quad (4.3)$$

where *Value* is the actual pixel value, *Man* (mantissa) is the analog or

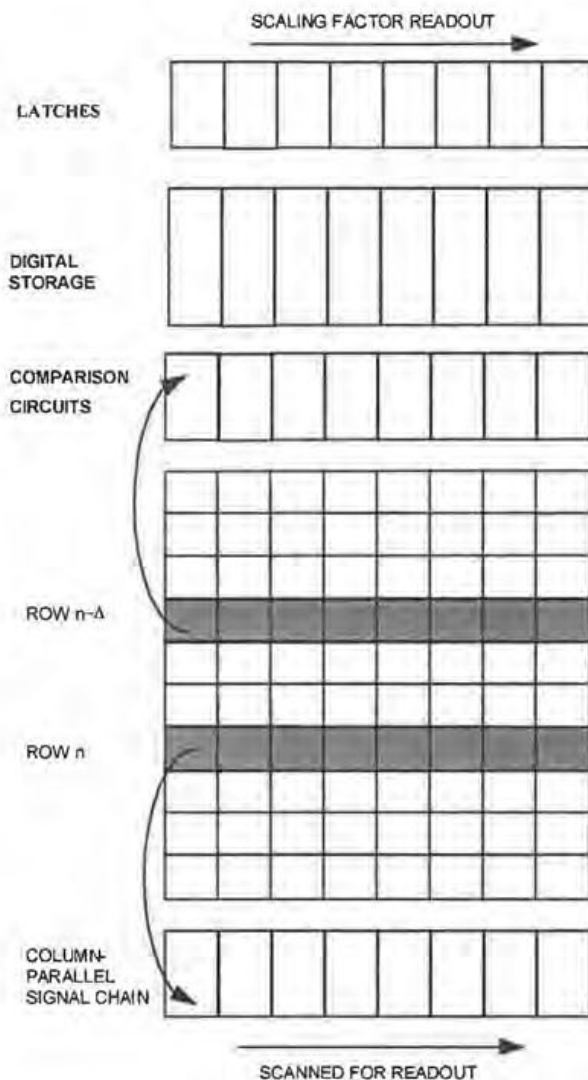


Figure 4-18. General architecture description of the autoscaling CMOS APS.

digitized output value that has been read out at the time T , X is a constant greater than one (for example, 2), and EXP is the exponent value describing the scaling factor. This digital value is read out at the upper part of the chip. For each pixel, only the last readouts of a certain number of rows are kept to enable the correct output for the exponent bits.

The idea of having a floating-point presentation per pixel via real-time feedback from the pixel has been proposed before by Yadid-Pecht [36]. However, the previous design required an area in the pixel that substantially affected the fill factor, so it was then proposed that the control for a group of pixels should be shared. In the currently proposed solution, however, the necessary additional hardware will be placed in the periphery; as a result, the

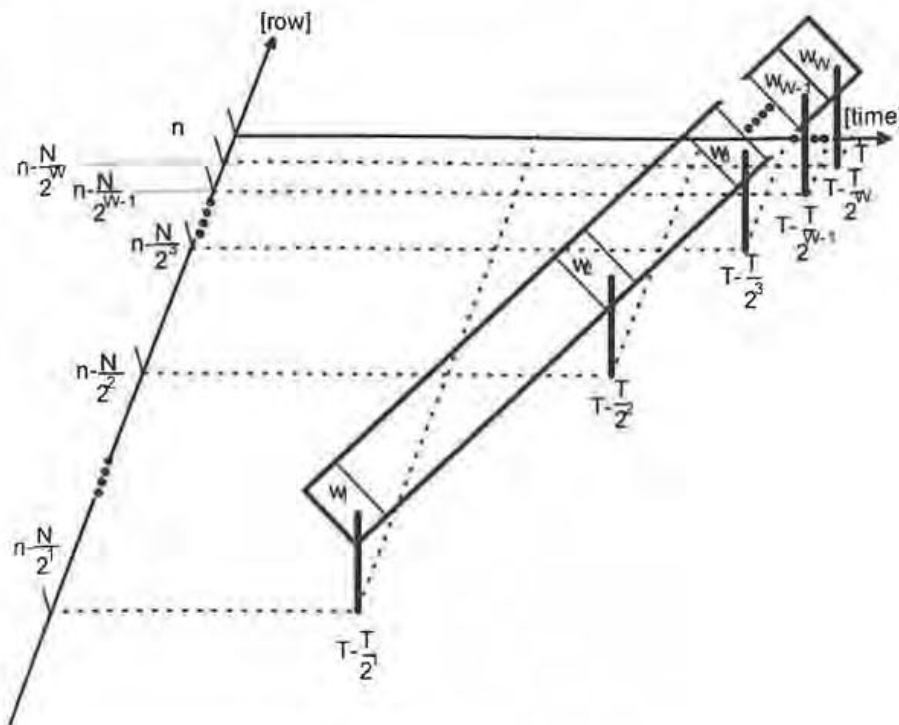


Figure 4-19. Combined time-space diagram.

information can be output with minimal effect on spatial or temporal resolution. The spatial resolution is slightly modified, since the desired ability to independently reset each pixel requires an additional transistor per pixel [37]. The temporal resolution should be assessed: a pixel should be checked at different time points to get the exponential (scaling) term. Equivalently, the pixels of different rows could be checked to get the same information. In the latter case, row n at time zero would provide the mantissa for row n (either through an on-chip or an off-chip A/D output), while the pixels in row $n - N/2$ (where N is the total number of rows that set the frame time) would provide the first exponent bit (W_1) as a result of the logic circuit decision for that row. Row $n - N/4$ would provide the second bit (W_2) for that row, row $n - N/8$ would provide the third bit, and so on. Thus, at the cost of a customized number of comparisons, the required information can be obtained automatically and the mantissa scaled accordingly.

Figure 4-19 describes this approach via a combined time-space diagram where the axes represent the row number and time, respectively. $W_1, W_2, \dots, W_w$, represent the exponent bits; i.e., W_1 represents the first point of decision $T - T/2$ (whether to reset or not for the first time), W_2 for the next point and so forth. The equivalent is shown at point $n - N/2$ in the spatial domain, which is the row that should be used for the decision concerning W_1 .

For example, an imaging device consisting of a square pixel array of 64 rows and 64 columns may be assumed, and it is desired to expand the dynamic range by 3 bits due to a high illumination level. Therefore, $W = 3$ and $N = 64$ in this case. For each pixel from the selected row n , three comparisons (W_1 , W_2 and W_3) are carried out at three corresponding time points ($T - T/2$, $T - T/4$, $T - T/8$). The first comparison, which is with the threshold, is carried out at row $n - 32$ (32 rows before regular readout of that pixel). This leaves an integration time of $T/2$ with a comparison result of $W_1 = "1"$, and this pixel is reset. The second comparison is carried out at row $n - 16$ (16 rows before regular readout of that pixel), leaving an integration time of $T/4$ with a comparison result of $W_2 = "1"$; this pixel is also reset. The third comparison is carried out at row $n - 8$ (8 rows before regular readout of that pixel), leaving an integration time of $T/8$ with a comparison result of $W_3 = "1"$. This pixel is reset as well. The autoscaling combination for the pixel in this example is therefore (1 1 1): this means that the pixel has been reset three times during the frame time, and the regular readout for this pixel should be scaled (multiplied) by a factor of $2^3 = 8$.

The frame time of a pixel array consisting of N rows and N columns may be calculated. Readout time for each row is composed of a copying time (T_{copy} = the time needed to copy one row into the readout buffer) and a scanning time (T_{scan} = the time needed to scan each pixel). Since there are N pixels in each row, the total time for row readout (T_{row}) is given by

$$T_{\text{row}} = T_{\text{copy}} + N \times T_{\text{scan}} \quad (4.4)$$

and the frame time (T_{frame}) is given by

$$T_{\text{frame}} = N \times T_{\text{scan}} \quad (4.5)$$

By adding W comparisons (for W different integration times) for each row, the row readout time is slightly modified and is given by

$$\begin{aligned} T'_{\text{row}} &= W \times T_{\text{comp}} + T_{\text{row}} \\ &= W \times T_{\text{comp}} + T_{\text{copy}} + N \times T_{\text{scan}} \end{aligned} \quad (4.6)$$

where T_{comp} is the time for comparison to the threshold level. Since $W \ll N$ then

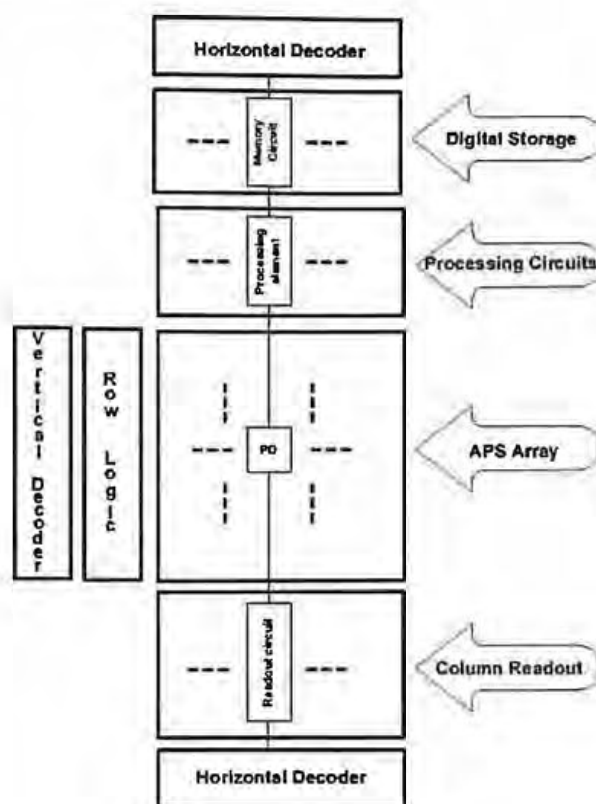


Figure 4-20. Block diagram of the proposed design.

$$W \times T_{comp} \ll N \times T_{scan} \quad (4.7)$$

and $T'_{row} = T_{row}$. Hence, the frame time T_{frame} is insignificantly affected by autoscaling. This enables the imager to process scenes without degradation in the frame rate.

4.3.1.3 Design and implementation

A block diagram of the proposed design is shown in Figure 4-20. The design makes use of a column parallel architecture to share the processing circuits among the pixels in a column. The pixel array, the memory array and the processing elements are separated in this architecture. Each pixel contains an additional transistor (in series with the row reset transistor) that is activated by a vertical column reset signal; this allows the independent reset of the pixel. Integration time can be adjusted for each pixel with this reset, and nondestructive readout of the pixel can be performed at any time

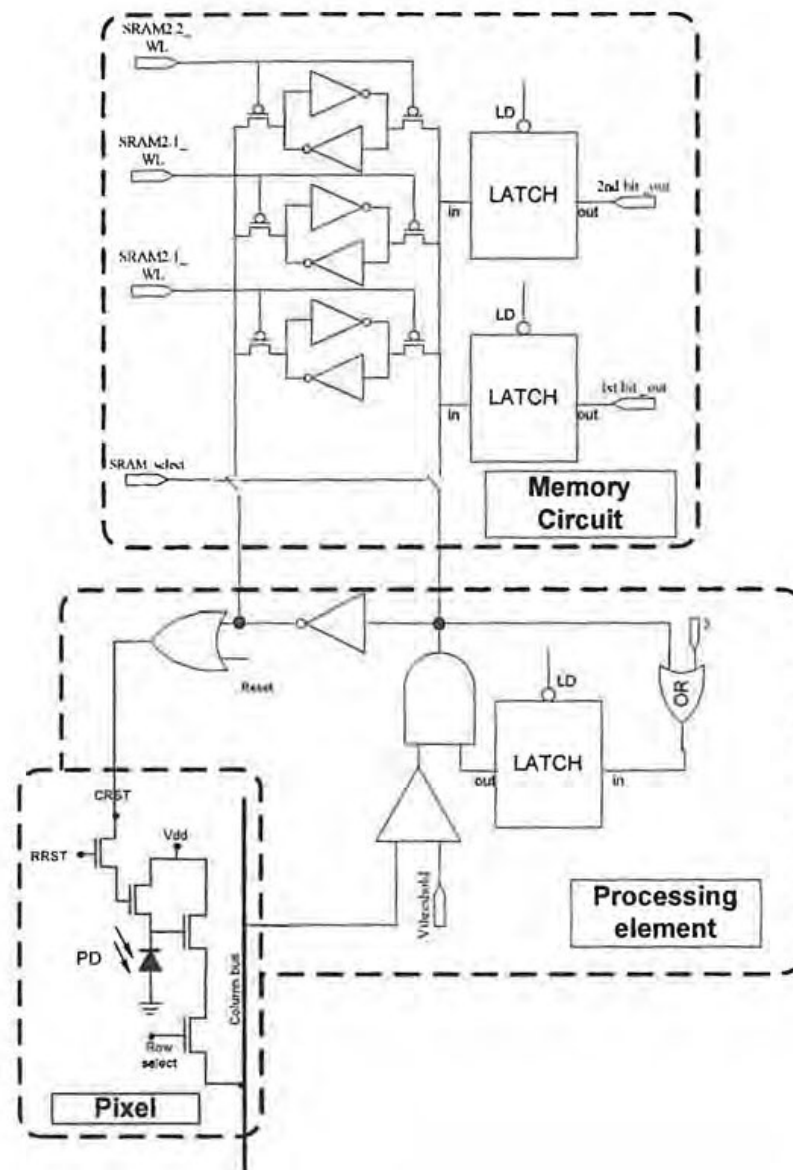


Figure 4-21. Electrical description of one column of an autoscaling CMOS APS.

during the integration period by activating the row select transistor and reading the voltage on the column bus.

The processing element contains the saturation detection circuit, which is shared by all pixels in a column. Because of the column parallel architecture, the pixel array contains a minimum amount of additional circuitry and sacrifices little in fill factor. The memory array contains the SRAMs and latches. Two horizontal decoders—one each for the pixel array and the memory array—work in parallel and are used to retrieve the mantissa and exponent, respectively. The vertical decoder is used to select the rows in order.

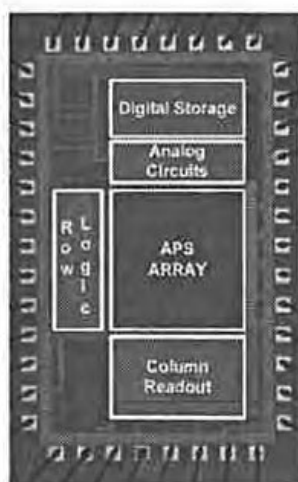


Figure 4-22. Photograph of the fabricated autoscaling CMOS APS test chip.

The electrical scheme for a single column is presented in *Figure 4-21*. In this circuit, the pixel output signal is evaluated at the comparator, where it is compared with an appropriate threshold. If its signal exceeds a predetermined threshold, the pixel is detected as saturated. Using this information and the binary information concerning the pixel (stored in the memory during different parts of the integration), a decision whether to reset the pixel is made. If the decision is positive, the column reset (*CRST*) and row reset (*RRST*) lines must both be precharged at a logical high voltage to activate the reset transistor; the photodiode then restarts integration. If the decision is negative, the reset is not active and the pixel continues to integrate. The binary information (whether the reset was applied or not) is saved in the SRAM memory storage and output to the latches in due time. After the row is read through the regular output chain, this additional information is retrieved from the memory through the latches.

4.3.1.4 Experimental results

A 64×64 pixel chip was successfully fabricated using the HP $0.5 \mu\text{m}$ n-well process. The chip photograph is shown in *Figure 4-22*. The sensor was quantitatively tested for relative responsivity, conversion gain, saturation level, noise, dynamic range, dark current, and fixed pattern noise. The results are presented in *Table 4-1*.

The conversion gain was in general agreement with the design estimate of photodiode capacitance. The saturation level was approximately 1.33 V; fixed pattern noise (FPN) was measured to be approximately 0.15% saturation; dark current was measured to be on the order of 30–35 mV/sec, output referred, or 0.61 pA/cm^2 ; and the inherent dynamic range was

Table 4-1. Attributes of the autoscaling CMOS APS test chip.

Chip format	64 × 64 pixels
Chip technology	HP 0.5 μm
Chip size	1.878 mm × 2.9073 mm
Pixel size	14.4 μm × 14.4 μm
Pixel type	Photodiode
Pixel fill factor	37%
Conversion gain	12 $\mu\text{V}/\text{e}^-$
Fixed pattern noise (FPN)	0.15%
Dark current (room temp)	35 mV/sec (0.61 pA/cm ²)
Power	3.71 mW (5 MHz)
Inherent dynamic range	71.4 dB (~11 bit)
Extended dynamic range	2 additional bits
Saturation level	1.33 V
Quantum efficiency (QE)	20%

71.4 dB, or 11 bits. The extended dynamic range provided two additional bits to the inherent dynamic range. No smear or blooming was observed due to the lateral overflow drain inherent in the APS design. The chip was also functionally tested.

Figure 4-23 shows a comparison between an image captured by a traditional CMOS APS and by the autoexposure system presented here. In the Figure 4-23(a), a scene is imaged with a strong light on the object; hence, some of the pixels are saturated. At the bottom of Figure 4-23(b), the capability of the autoexposure sensor for imaging the details of the saturated area in real time may be observed. Since the display device is limited to eight bits, only the most relevant eight-bit part (i.e., the mantissa) of the thirteen-bit range of each pixel is displayed here. The exponent value, which is different for different areas, is not displayed. This concept in its present form suits rolling-shutter sensors, and a first prototype following this concept has been demonstrated here.

4.3.2 CMOS smart tracking sensor employing WTA selection

This section presents an example of a smart APS sensor suitable for tracking purposes. The system employs an analog winner-take-all circuit to find and track the brightest object in the field of view (FOV). This system-on-a-chip employs adaptive spatial filtering of the processed image, with elimination of bad pixels and with reduction of false alarm when the object is missing. The circuit has a unique adaptive spatial filtering ability that allows the removal of the background from the image, and this occurs one stage before the image is transferred to the WTA detection circuit. A test chip of 64 × 64 array has been implemented in 0.5 μm CMOS technology. It

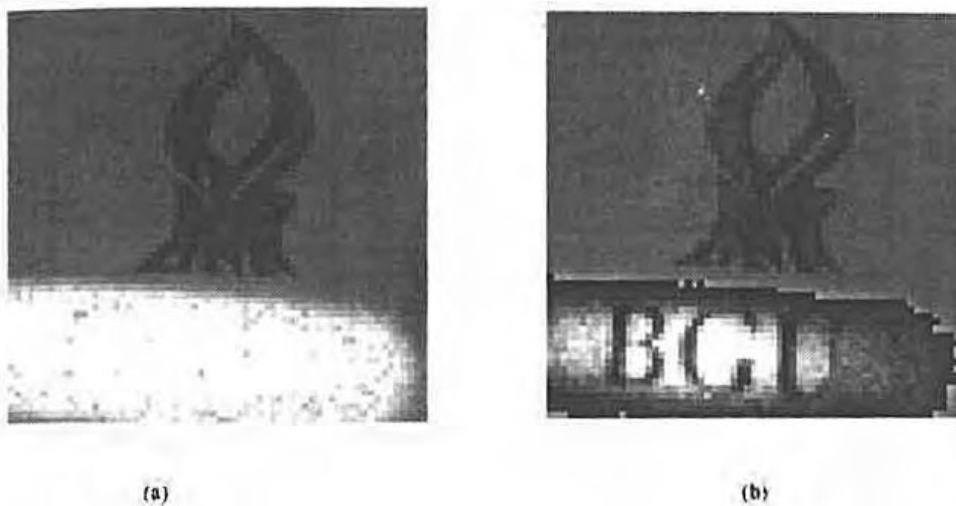


Figure 4-23. (a) Scene observed with a traditional CMOS APS sensor.(b) Scene observed with the in-pixel autoexposure CMOS APS sensor.

has a 49% fill factor, it is operated by 3.3 V supply, and it dissipates 36 mW at video rate. The system architecture and operation are described, together with measurements from a prototype chip.

4.3.2.1 Motivation

Many scientific, commercial and consumer applications require spatial acquisition and tracking of the brightest object of interest. A winner-take-all function has an important role in these kinds of systems: it selects and identifies the highest input (which corresponds to the brightest pixel of the sensor) and inhibits the rest. The result is a high digital value assigned to the winner pixel and a low one assigned to the others. CMOS implementations of WTA networks are an important class of circuits widely used in neural networks and pattern-recognition systems [42, 44]. Many WTA circuit implementations have been proposed in the literature [40–52]. A current-mode MOS implementation of the WTA function was first introduced by Lazzaro [40]. This very compact circuit optimizes power consumption and silicon area usage. It is asynchronous, responds in real time and processes all input currents in parallel.

Most of the existing WTA circuits can be integrated with APS sensors. Usually, when WTA circuits are used in two-dimensional tracking and visual attention systems, the image processing circuitry is included in the pixel; however, there are penalties in fill factor or pixel size and resolution. Here we show an implementation of a 2-D tracking system using 1-D WTA circuits. All image processing is performed in periphery of the array without influencing imager quality.

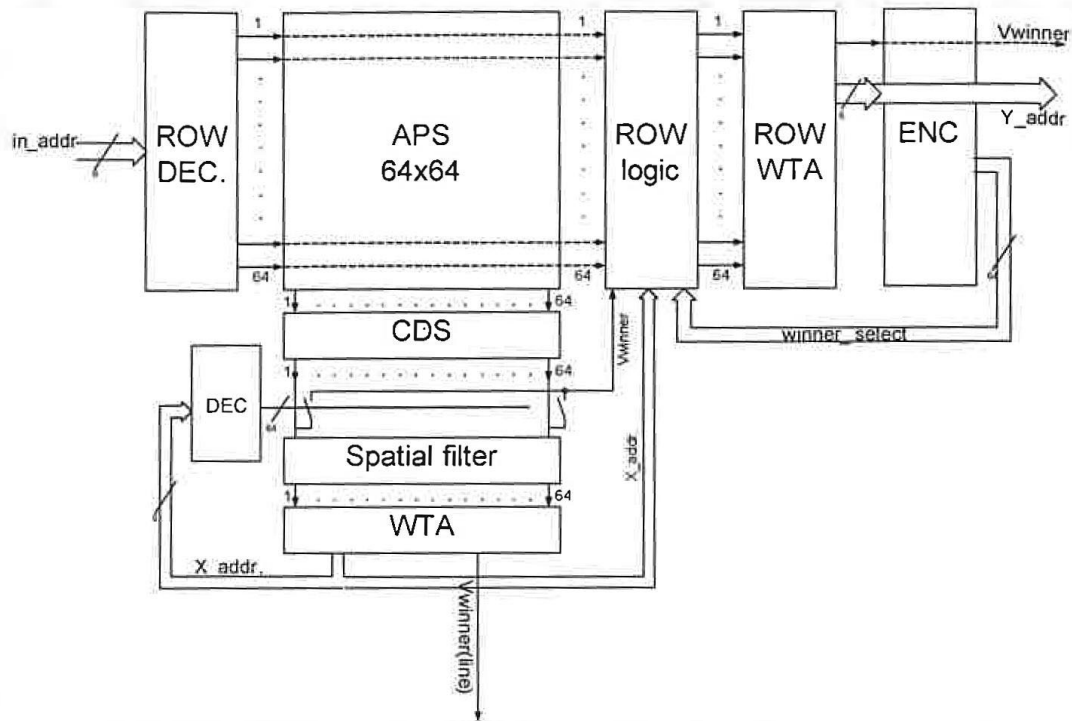


Figure 4-24. Block diagram of the proposed CMOS smart tracking sensor system.

As mentioned above, the regular WTA circuit chooses a winner from a group of input signals. When an APS with WTA selection system is used for object selection, a number of problems can occur. If the object of interest disappears from the processed image, the WTA will compare input voltages that represent intensity levels in the image background; hence, the circuit will output the coordinates of some background pixel instead of the missing object of interest and cause a false alarm. Background filtering and false alarm reduction is therefore necessary. Another problem that can disrupt proper operation of the system is a bad pixel. Since the bad pixel has a high value, it can be selected as the winner regardless of other pixel values.

The simplest technique for background filtering is signal comparison against a globally set threshold, above which pixels qualify as object pixels. The disadvantage of this kind of filtering is that it is necessary to choose the value of this threshold in advance; in the case where the background is overly bright (i.e., above the chosen threshold), the circuit will not be able to cope with the task. The problem is most severe if the object of interest disappears from the processed image and the background is bright.

The system described here is a 64×64 element APS array with two-dimensional WTA selection. A spatial adaptive filtering circuit allows adaptive background filtering and false alarm reduction if the object is missing from the scene.

4.3.2.2 System architecture

Figure 4-24 shows the block diagram of the system. There is no penalty in spatial resolution using the proposed architecture, since the processing is done at the periphery of the array.

The process of phototransduction in the APS is done row-by-row in two phases: reset (where a photodiode capacitor is charged to a high reset voltage) and phototransduction (where the capacitor is discharged after a constant integration time). A commonly used CDS circuit is implemented on the chip to subtract the signal pixel value from the reset one; the output is high for a bright pixel and low for a dark one. The subsequent stage is adaptive background filtering of all pixels for which the CDS values are less than a threshold value. This threshold corresponds to the average of the outputs from all row sensors, with the addition of a small variable epsilon value. Only the signals that pass the filter are transmitted to the WTA selection circuit. When there is no detectable object (i.e., only background signals exist), no signals pass this filter, and so the “no object” output becomes high and false alarm reduction is achieved. A detailed description of this filtering technique is presented in section 4.3.2.3.

The next stage is the winner-take-all selection, which is done with a simple voltage-mode WTA after Donckers et al. [48]. The main factor for choosing this WTA circuit is its simplicity; generally any kind of voltage- or current-mode WTA can be integrated with this system [53]. The winner selection is done row-by-row. The winner of each row is found, its value is stored into an analog memory (a capacitor), and its address is deposited in the digital storage. If there is more than one input with the same high value, the WTA chooses the leftmost one using a simple logic. The result is a column of N analog pixel values of row winners with their column addresses. From all the row winners, a global winner is selected using an identical WTA circuit. The 1-D winner selection array was designed to consist of eight identical blocks of eight-input WTA cells to achieve better resolution and reduce matching problems. The row winner value is stored in the analog memory that corresponds to the actual row and its column address is stored in the corresponding digital memory; these analog and digital memories are in the *ROW logic* block displayed in Figure 4-24. In the case of “no object” in a row, the value transmitted to the memory is zero. Following a full frame scan, the WTA function is activated on all 64 row winners (in the *ROW WTA* block in Figure 4-24) and the location of the global frame winner is found. Its analog value and its address are then read out of the memory by an encoder (the *ENC* block in Figure 4-24).

This architecture allows the enlargement of the proposed system to any size of $N \times N$ pixel array without affecting the system properties.

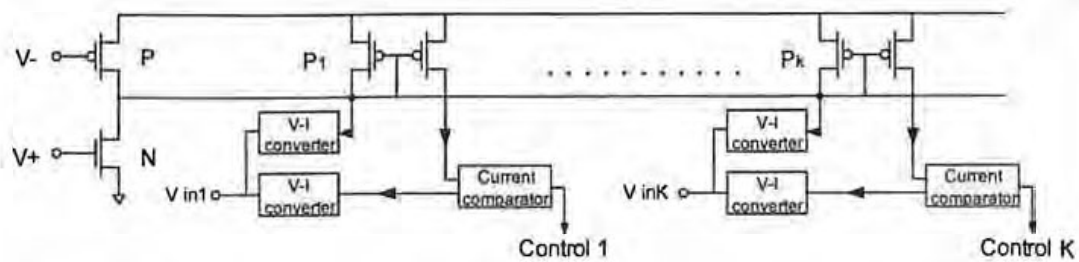


Figure 4-25. Principal scheme of the spatial filter circuit in the CMOS smart tracking sensor.

4.3.2.3 Descriptions of the circuits

4.3.2.3.1 The adaptive spatial filter

The principal scheme of the adaptive 1-D filter circuit used in the CMOS smart tracking sensor system is shown in Figure 4-25. The inputs to the filter correspond to the CDS values, and the outputs are the control signals. As mentioned earlier, this circuit filters all pixels for which the CDS values are less than a threshold value. This threshold corresponds to the average of the outputs from all the row sensors, with the addition of a small variable epsilon value. The *Control* output of the filter is high for an object pixel and low for a pixel that is imaging the background. The advantage of this filtering is that this epsilon value is adaptive and not constant for different input vectors. The value of epsilon depends inversely on the average current value: it increases when the average current decreases and decreases when current increases. This results in a small epsilon value for a high background and a high epsilon for a low background. The filtering process is thus more sensitive when a high background is present and the input voltage of the object is very similar to that of the background. The epsilon value can be controlled manually by setting suitable V_- and V_+ voltage values (see Figure 4-25).

If V_+ is zero and V_- is V_{DD} , then the epsilon value is zero and all $I_{average} + \epsilon$ currents of the circuit are equal to the average current of the n inputs in an n -sized array. The non-zero epsilon value can be added to this average by increasing the V_+ value. The epsilon value can also be subtracted from the average by decreasing the V_+ value. A positive epsilon value is usually of interest here, so V_- is V_{DD} in this case. Note that the voltages to the current converters have a pull configuration (the current direction is shown by arrows in Figure 4-25).

The adaptive functionality can be achieved by operation of transistor N in the linear region. With an average current increase (reflecting an increase in background), the V_{gs} values of the $P_1 \dots P_k$ transistors are increased as well,

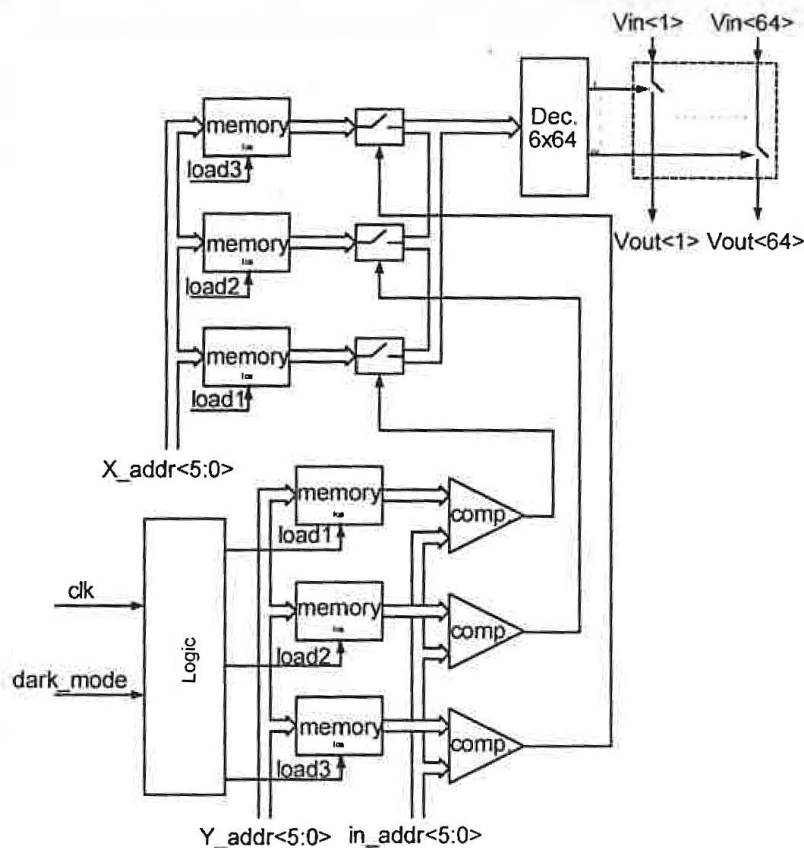


Figure 4-26. Principal scheme for bad pixel elimination in the CMOS smart tracking sensor.

which causes a reduction in the V_{ds} voltage of transistor N. The result is a fall in current at transistor N and a reduction of epsilon. Note that if a constant epsilon value is required, a stable current source (independent of the V_{sg} of $P_1 \dots P_k$) can be used instead of transistor N.

Instead of using a transistor N, another simple option is to connect two parallel transistors, one with a relatively large W/L value operating in saturation and another with a small W/L operating in the linear region. This arrangement can achieve a constant epsilon by cutting off the transistor that is usually operated in the linear region and using only the saturation transistor. Alternatively, an adaptive epsilon value can be achieved by using the transistor operating in the linear region and cutting off the transistor that is in saturation.

In addition to background filtering, the circuit enables “no object” notification. If the control values of all pixels are “0”, the “no object” output is high and false alarms are reduced. However, noise levels vary with the background level and shot noise is higher at a higher background level. To achieve proper operation of the “no object” function, the minimum value of epsilon must therefore be limited.

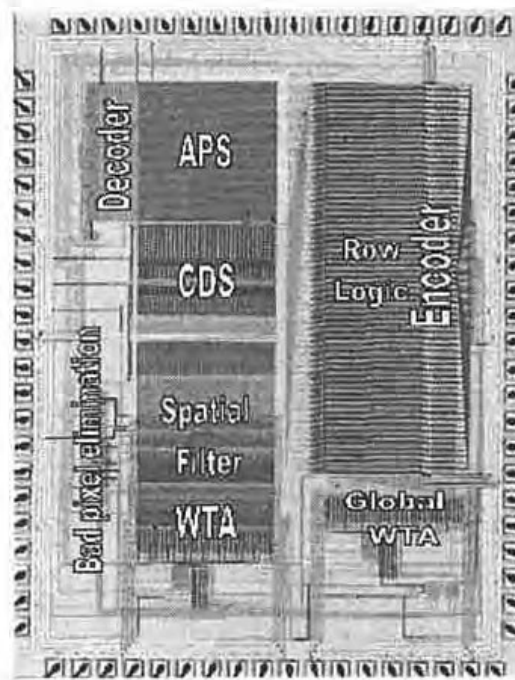


Figure 4-27. Photograph of the CMOS smart tracking sensor test chip.

The inputs to the WTA circuit depend on the filter control values: zero for a background pixel and pixel intensity level for an object pixel.

4.3.2.3.2 Elimination of bad pixels

Bad pixels can disrupt proper operation of the system. A bad pixel can have a high value, so it may be selected as the winner regardless of other pixel values. In the proposed CMOS smart tracking sensor system, bad pixels are disabled with a special “dark mode” in which a dark image is input. Figure 4-26 shows the principal scheme for bad pixel elimination.

Bad pixels are eliminated in two stages. In the first stage (the dark mode), the *dark_mode* signal in Figure 4-26 is “1” and the system processes a dark image—a very low background without an object of interest. The circuit finds bad bright pixels, using a regular WTA algorithm as described before. The frame must be scanned (processed) N times in order to find N bad pixels. After each additional frame scanning, a new bad pixel is found and its address is stored in the memory (using the *X_addr* and *Y_addr* buses in Figure 4-26).

In the second stage (regular system operation), the *dark_mode* signal is “0” and a real image is processed. For the “bad” pixels that were found in the dark mode stage, however, only ground values are transmitted to the filter and the WTA circuits. This is accomplished by comparing the address of every processed row (*in_addr* in Figure 4-26) with the *Y_addr* stored in

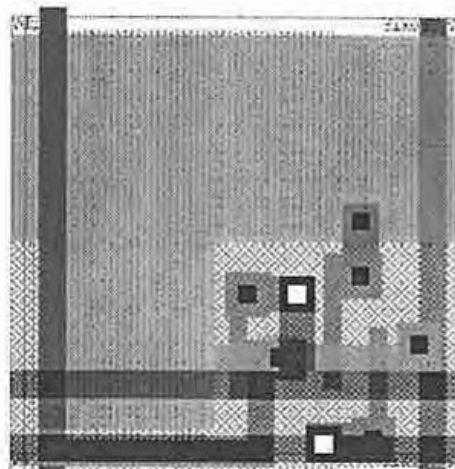


Figure 4-28. Layout of a single photodiode pixel of the CMOS smart tracking sensor.

the memory. If their values are equal, the comparator will output “1” and the X_addr of the bad pixel of this row is transferred to the $Dec. 6 \times 64$ block. In the array, the input bad pixel voltage is replaced with a ground value. The values of all bad pixels are replaced by ground, and thus bad pixels cannot be chosen as winners.

The fabricated prototype chip allows the elimination of up to three bad pixels. Adding more logic can easily increase this capacity.

4.3.2.4 Performance and test chip measurements

The CMOS smart tracking sensor system was designed and fabricated in a $0.5 \mu\text{m}$, n-well, 3-metal, CMOS, HP technology process supported by MOSIS. The supply voltage was 3.3 V. A photograph of the test chip is shown in Figure 4-27. The test chip includes an APS array, row decoders, correlated double sampling circuit, an adaptive spatial filter, eight identical eight-input voltage WTA circuits, logic, a global winner selection circuit and a bad pixel elimination block.

The test chip was designed to allow separate modular testing of every functional block of the chip as well as measurements of the chip as a unit. The main separate blocks of the chip (the APS with CDS, the adaptive filter and the eight-input WTA circuit) were tested, as was the whole chip to check the functionality.

4.3.2.4.1 APS with CDS

The layout of a single photodiode pixel of the CMOS smart tracking sensor is shown in Figure 4-28.

As mentioned before, there is no penalty in spatial resolution for this architecture since the processing is done at the periphery. The pixel size is

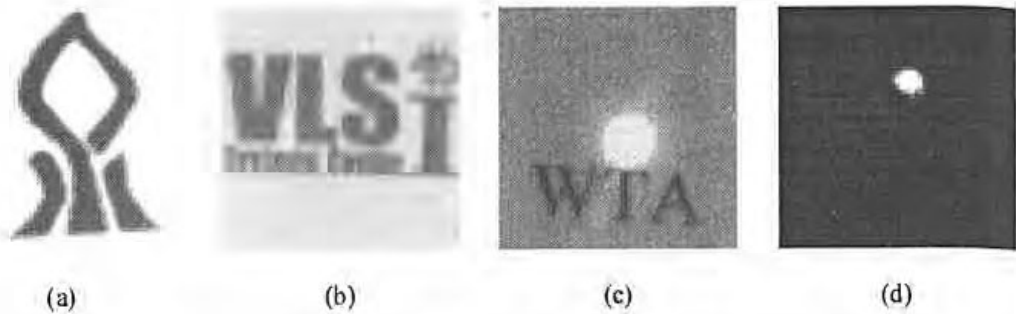


Figure 4-29. Four images as captured by the APS: (a) the Ben-Gurion University logo on a high illumination background; (b) the VLSI Systems Center logo; (c) WTA with a laser beam spot; and (d) a laser beam spot on a dark background.

$14.4\ \mu\text{m} \times 14.4\ \mu\text{m}$ and the fill factor is 49%. Figure 4-29 shows four images as captured by the sensor under different background illumination levels.

4.3.2.4.2 Adaptive filter measurements

Measurements were carried out at both low and high background levels to determine the properties of the filter. These measurements check the ability of the circuit to filter background regardless of its level and also check the dependence of the ε value on the background level. Figure 4-30(a) and (b) show the response of the filter to low and high backgrounds, respectively.

In the first test, the average of the input voltages for a low background was 820 mV; this is represented by the horizontal solid line in Figure 4-30(a). One of the filter inputs ranged from 0 V to 3.3 V; these inputs corresponded to the background in the case of a low value and the object in the case of a high value. They are represented by the sloped sawtooth lines in Figure 4-30. The pulsed voltage in Figure 4-30 is the filter control output (see Figure 4-25). This square wave is low for $V_{in3} < 1.6\ \text{V}$ and high for $V_{in3} > 1.6\ \text{V}$. This value represents $V_{\text{average}} + \varepsilon$ when $V_{in3} = 1.6\ \text{V}$. In this case, the ε value is 780 mV. As mentioned earlier, the ε value can be changed for this input vector by changing the $V+$ and $V-$ control voltages.

The same procedure was performed to test the high background case, where the average was 1.54 V and the ε value was found to be 360 mV.

The filter responded as expected: a high epsilon value was generated for a low background level and a low epsilon value for a high background.

Figure 4-31 plots the epsilon value as function of background levels for different $V+$ values. As expected, an increase in $V+$ bias at a constant background level gives a higher epsilon value. On the other hand, the epsilon value decreases with background increase.

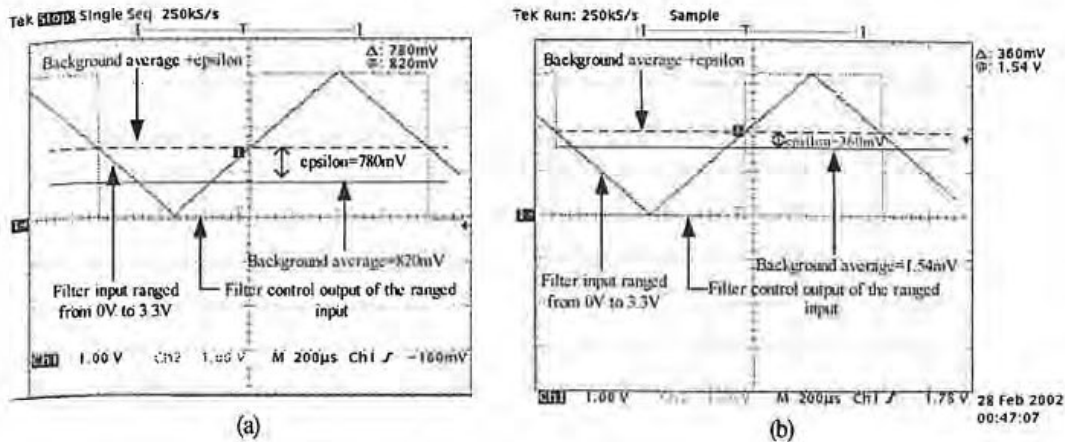


Figure 4-30. Adaptive filter response for (a) a low background and (b) a high background.

4.3.2.4.3 Measurements of the filter response and false alarm reduction

Figure 4-32 shows the filter response to four different images. The column beside each image shows the "no object" outputs for every row: white corresponds to "1" in "no object" output and black to "0". Figure 4-32(a) and Figure 4-32(b) present the same object of interest (a laser beam spot) but with two different background levels, a high background in Figure 4-32(a) and a low background in Figure 4-32(b).

Because of the adaptive properties of the filter, the epsilon value is higher for the low backgrounds in Figure 4-32(b) and (d), so the filtering is more aggressive and only very high values pass the filter. For the high backgrounds in Figure 4-32(a) and (c), the epsilon value is lower and relatively lower voltage values can pass the filter. The filtering process is thus more sensitive when a high background is present and the object input

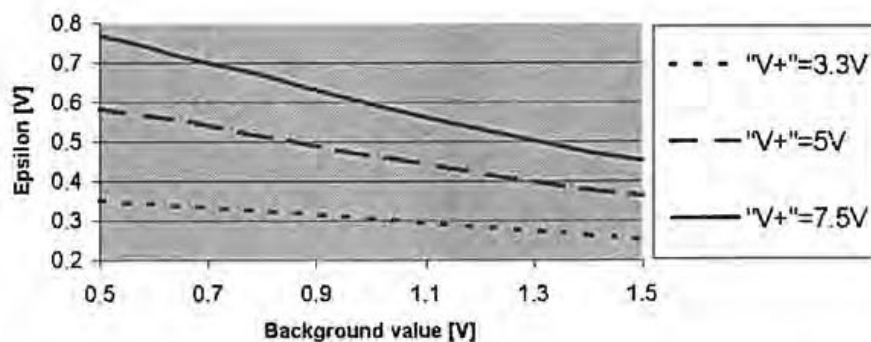


Figure 4-31. Epsilon value as function of background levels for different V_+ values.

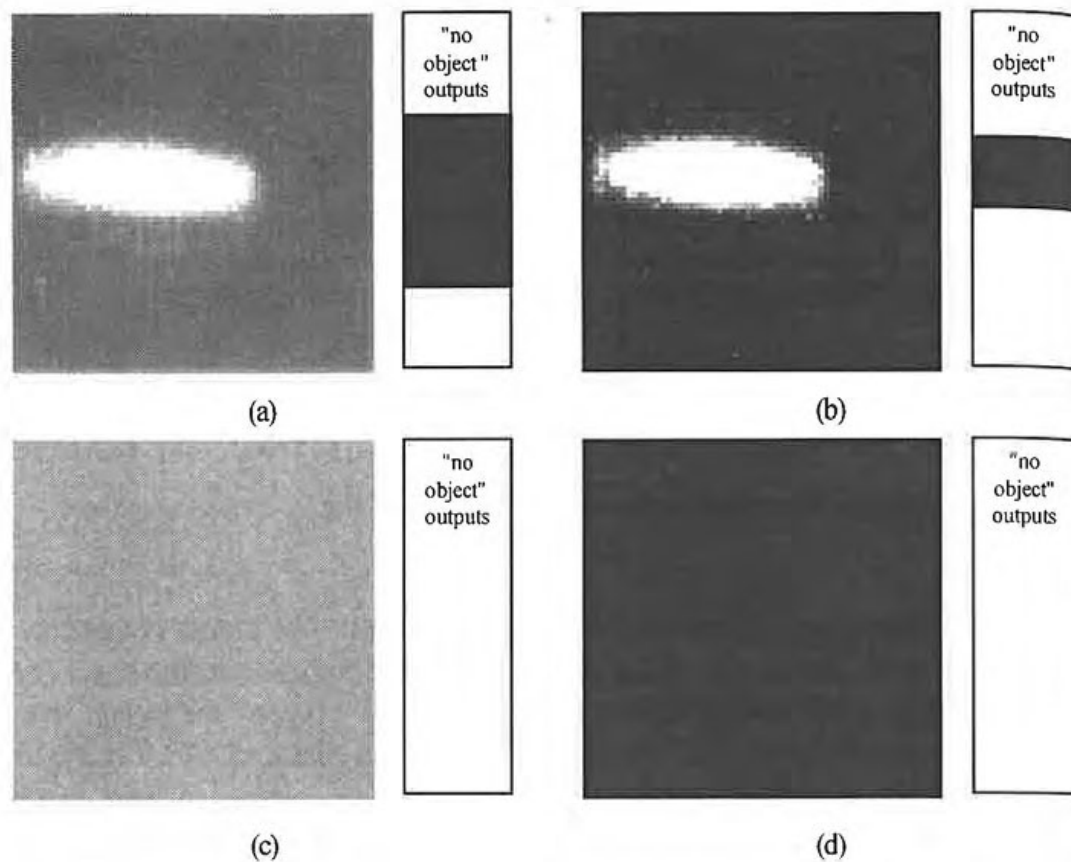


Figure 4-32. Adaptive filter response to four different images: (a) laser beam with a high background; (b) laser beam with a low background; (c) high background only; and (d) low background only.

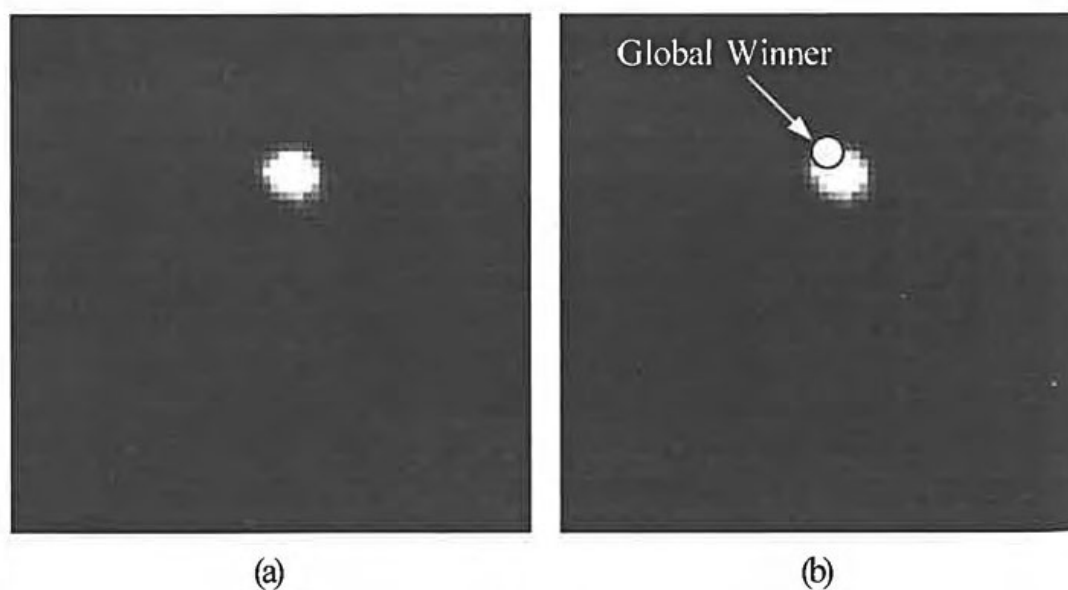


Figure 4-33. Global winner selection: (a) the processed image; and (b) the winner location.

Table 4-2. Chip attributes for the CMOS smart tracking sensor.

Technology	HP 0.5 μm
Voltage supply	3.3 V
Array size	64 $\times$ 64
Pitch width	14.4 μm
Fill factor	49%
WTA mode	Voltage
WTA resolution	40 mV
Chip size (mm)	3.5 $\times$ 4.3
Frame scanning frequency	30 Hz
Minimum power dissipation (low background without object)	$\sim$ 28 mW
Typical power dissipation (the laser beam is $\sim$ 10% of the frame)	$\sim$ 36 mW
FPN (APS)	0.15%
Conversion gain (APS)	7.03 $\mu\text{V}/\text{e}^-$
Dark response (APS output)	5.77 mV/s
Dynamic range	65 dB
Output voltage range	1.47 V

voltage is close to the background level. However, there is more freedom in filtering when a low background is present. In both cases, the object of the interest passes the filter. With a high background (small epsilon value), however, some pixels of the background succeed in passing the filter, while for a low background (high epsilon value) only the object pixels pass the filter. This effect can be seen in *Figure 4-32(a)* and *(b)*, where the “no object outputs” flags show the number of rows that succeed to pass the filter. As expected, *Figure 4-32(a)* has more “object” rows than *Figure 4-32(b)*. *Figure 4-32(c)* and *(d)* examine the false alarm reduction for low and high backgrounds. In both cases, the object of interest is not in the processed image and thus no signal passes the filter. The “no object” output is fixed on “1” when the object of interest disappears from the processed image, and therefore a false alarm is prevented for both levels of background.

4.3.2.4.4 The global winner measurements.

To examine the ability of the system to find the coordinates of the global winner, a focused laser beam was used as object of interest. *Figure 4-33(a)* shows the processed image; *Figure 4-33(b)* presents the winner as found by the system. As expected, the winner is the pixel farthest to the upper left in the first row of the object of interest.

Table 4-2 summarizes the chip specifications for the CMOS smart tracking sensor.

4.4 Summary

In this chapter, the area of CMOS imagers was briefly introduced. CMOS technologies, CCD technologies and different CMOS pixels were described and compared. The system-on-a-chip approach was presented, showing two design examples. The main advantages of CMOS imagers—low cost, low power requirements, fabrication in a standard CMOS process, low voltage and monolithic integration—rival those of traditional charge coupled devices. With the continuous progress of CMOS technologies, especially the decreasing minimum feature size, CMOS imagers are expected to penetrate into various fields such as machine vision, portable devices, security, biomedical and biometric areas, and other applications where custom sensors and smart pixels are required. More systems on chips will definitely be seen in the near future.

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