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Paper No. ____

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY GROUP CORPORATION,
Petitioner,

v.

VISIONX TECHNOLOGIES, LLC,
Patent Owner.

Case No. TBD
Patent No. 7,868,366

**PETITION FOR INTER PARTES REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1 et seq**

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APPENDIX LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 7,868,366 (“ 366 patent ”)
1002	Prosecution History of U.S. Patent No. 7,868,366
1003	Declaration of R. Michael Guidash (“ Guidash ”)
1004	Curriculum Vitae of R. Michael Guidash
1005	Certified English Translation of Korean Unexamined Patent Application Publication No. 10-2006-0077132 (“ Pyo ”)
1006	Certified English Translation of Japanese Patent No. 3800335 (“ Imaoka ”)
1007	U.S. Patent Publication No. 2005/0012166 A1 (“ Choi ”)
1008	U.S. Patent No. 5,695,810 (“ Dublin ”)
1009	U.S. Patent No. 6,576,550 (“ Brase ”)
1010	Reid, Jonathan, Chapter 16, Handbook of Semiconductor Manufacturing Technology, 2nd Ed., Doering, Robert et al. eds., (2008) (“ Doering ”)
1011	Declaration of Rachel J. Watters authenticating: Edelstein, D., et al., Full Copper Wiring in a Sub-0.25 μ m CMOS ULSI Technology, 1997 International Electron Devices Meeting Technical Digest, 773-776 (1997) (“ Edelstein ”)
1012	U.S. Patent No. 6,429,120 (the “’120 patent”)
1013	Declaration of Nathaniel E. Frank-White authenticating: Pratt, Annabelle, Overview of the Use of Copper Interconnects in the Semiconductor Industry (2004) (“ Pratt ”)
1014	Quirk, Michael and Julian Serda, Semiconductor Manufacturing Technology, 257-333 (2001) (“ Quirk ”)
1015	Certified English Translation of Japanese Unexamined Patent Application 2004-206377 (“ Yanagida ”)

Exhibit	Description
1016	Japanese Unexamined Patent Application 2004-206377 (original Japanese language version)
1017	Certified English Translation of Korean Registered Patent 10-0664864 (“ Yun ”)
1018	Certified English Translation of Undated Response to a February 21, 2008, Office Action from the Korea Intellectual Property Office regarding Korean Patent Application No. 10-2007-0024914
1019	Certified English Translation of February 21, 2008, Office Action from the Korea Intellectual Property Office regarding Korean Patent Application No. 10-2007-0024914
1020	U.S. Patent No. 7.651,941 (the “’941 patent”)
1021	Complaint, <i>VisionX Technologies LLC v. Sony Group Corporation, et al.</i> , No. 2-22-cv-00178, Dkt. No. 1 (E.D. Tex. May 26, 2022)
1022	U.S. Patent Publication No. 2004/0245649 A1 (the “’649 Pub.”)
1023	Gambino, J., et al., Optimization of Cu Interconnect Layers for CMOS Image Sensor Technology, Conference Proceedings AMC XXI, 151-157 (2006) (“ Gambino ”)
1024	Yadid-Pecht, Orly and Ralph Etienne-Cummings (Eds.), CMOS Imagers: From Phototransduction to Image Processing, 75-139 (2004) (“ Yadid-Pecht ”)
1025	International Publication No. WO 2006/008637 A1
1026	Springer History, https://www.springer.com/us/about-springer/history (accessed October 12, 2022)
1027	Plaintiff’s Infringement Contentions, <i>VisionX Technologies LLC v. Sony Group Corporation, et al.</i> , No. 2-22-cv-00178 (E.D. Tex. Sept. 8, 2022)
1028	Certified English Translation of International Publication No. WO 2006/129762 A1 (“ Iwabuchi ”)

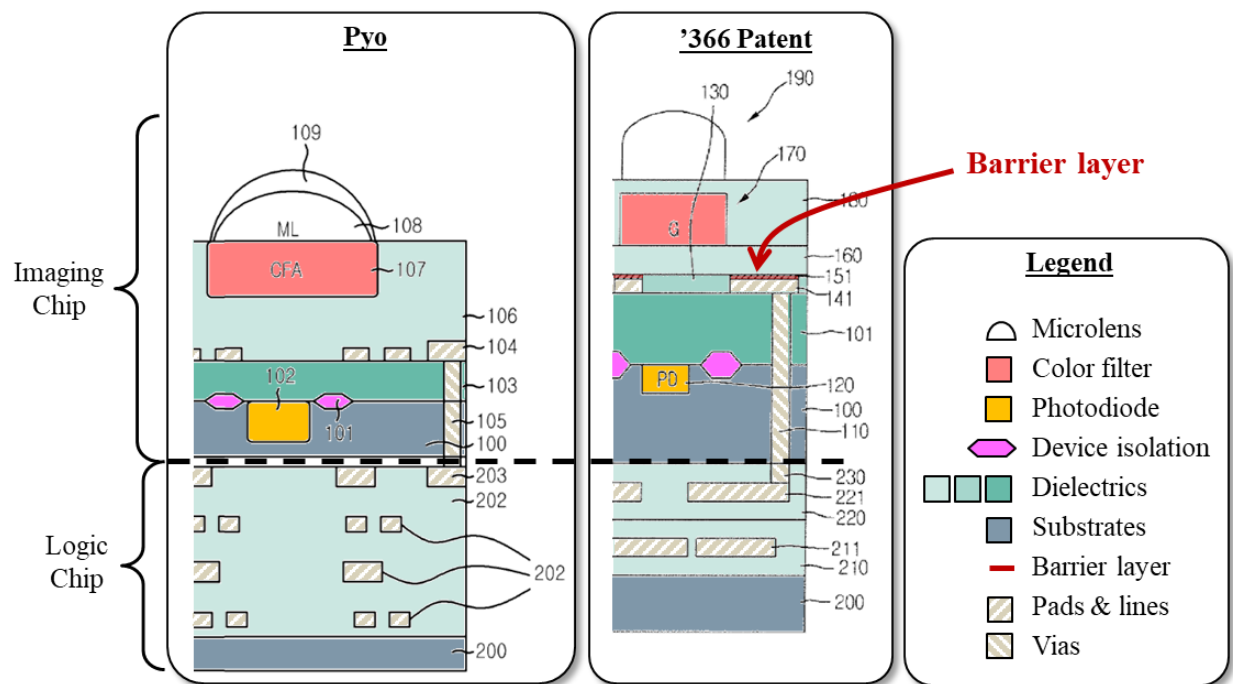
APPENDIX LISTING OF ABBREVIATIONS

Abbreviation	Description
'366 patent	U.S. Patent No. 7,868,366
Challenged Claims	Claims 1-8 of the '366 patent
CMOS	Complementary Metal–Oxide–Semiconductor
CMP	Chemical Mechanical Polishing
ILD	Interlayer dielectric
KR '914	KR 10-2007-0024914 (foreign priority application to the '366 patent)
Memo	The Office's June 21, 2022 memorandum (https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf)
Petitioner	Sony Group Corporation
PMD	Pre-metal dielectric
POSA	Person having ordinary skill in the art
Texas Litigation	<i>VisionX Technologies, LLC v. Sony Group Corporation et al.</i> , Case No. 2:22-cv-00178 (E.D. Tex.)
TSV	Thru-silicon via
UWM	University of Wisconsin-Madison

I. INTRODUCTION

Sony Group Corporation (“Petitioner”) requests cancellation of claims 1-8 (“Challenged Claims”) of U.S. Patent No. 7,868,366 (Ex. 1001, “’366 patent”).

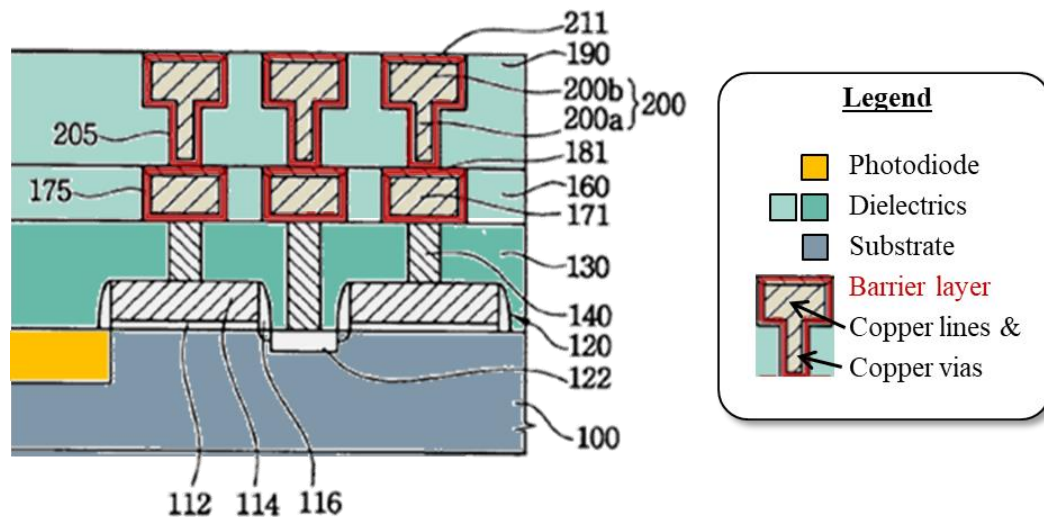
The Challenged Claims cover image sensors having a logic chip bonded to an imaging chip, below right. ’366 patent, Figure 8;¹ Guidash, ¶148. Pyo is indisputable prior art and discloses a stacked design just like the one claimed except that Pyo’s metal lines (104) lack a conductive barrier layer. Pyo, Figure 3 (below left). *Id.*



Pyo does not identify the metal used to fabricate lines (104), but discloses other metal lines (201)—mislabeled as “202” in Figure 3—can be copper.

¹ Images are annotated throughout unless otherwise noted.

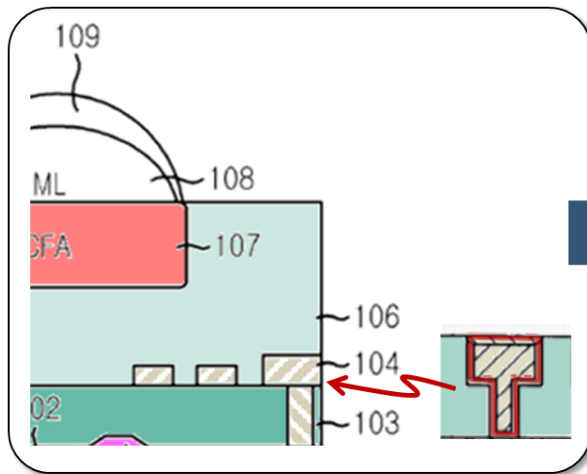
In 2005, Choi disclosed copper interconnections had advantages over aluminum interconnections when fabricating CMOS image sensors, but copper required barrier layers. Choi therefore disclosed methods of fabricating copper interconnections with metal barrier layers. Choi's methods, commonly known as the damascene and dual-damascene processes, were commonplace in CMOS manufacturing by 2007.



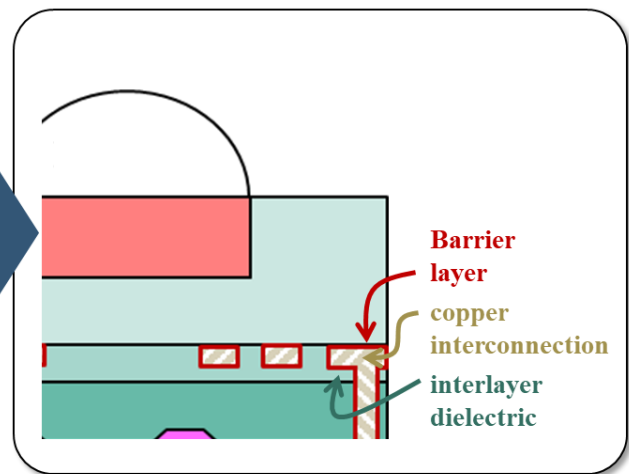
Choi, Fig. 5G; Guidash, ¶150.

Copper's advantages over aluminum—the only other natural choice—would have made it a natural choice for Pyo's metal lines (104) when implementing Pyo's design in 2007. Doing so using Choi's well-known methods would have resulted in conductive metal barrier layers, on copper interconnections, on an interlayer dielectric ("ILD"), as required by the Challenged Claims.

Pyo + Choi



Pyo-Choi



Indeed, during prosecution of the '366 patent's Korean priority application, the Korean examiner rejected similar apparatus claims over Pyo. In response, the Applicant presented no contrary argument, but canceled the rejected claims and instead pursued **method** claims analogous to the '366 patent's method claims, which are not challenged here.

During U.S. prosecution, the Applicant submitted Pyo, but in its original Korean language. The Applicant provided the U.S. Examiner an English translation of Pyo's *abstract*, but the abstract fails to disclose material aspects of Pyo's design. Without a complete translation of Pyo or the Korean file history (i.e., the Korean examiner's rejection of the sensor claims over Pyo and the Applicant's subsequent cancelling of those claims), the U.S. Examiner apparently misapprehended the significance of the Korean-language Pyo reference. Instead, the U.S. Examiner allowed the Challenged Claims without rejection.

Pyo is not the only reference that discloses sensors comparable to the Challenged Claims. Imaoka was not before the Examiner and anticipates the Challenged Claims.

II. MANDATORY NOTICES – 37 C.F.R. §42.8

A. Real Party-In-Interest – §42.8(b)(1)

Petitioner is a Real Party-in-Interest. Co-defendants in the Texas Litigation, Sony Corporation, Sony Semiconductor Manufacturing Corporation, and Sony Semiconductor Solutions Corporation, are Real Parties-in-Interest. In an abundance of caution, Petitioner states that other Sony affiliates could be Real Parties-in-Interest, and in particular Petitioner identifies Sony Corporation of America (SCA) and Sony Electronics Inc. (SEL) as Real Parties-in-Interest.

B. Related Matters – §42.8(b)(2)

A decision in this proceeding could affect or be affected by the following:

VisionX Technologies, LLC v. Sony Group Corporation et al., Case No. 2:22-cv-00178 (E.D. Tex.) (“Texas Litigation”).

C. Counsel and Service Information - §42.8(b)(3), (4)

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A power of attorney is submitted with the Petition. Counsel for Petitioner consent to service of all documents via electronic mail.

III. REQUIREMENTS FOR *IPR* – 37 C.F.R. §42.104

A. Grounds for Standing – §42.104(a)

Petitioner certifies pursuant to 37 C.F.R. §42.104(a) that the '366 patent is available for *inter partes* review and Petitioner is not barred or estopped from requesting such review as to the Challenged Claims.

B. Identification of Challenged Claims – §42.104(b)(1)

Petitioner requests cancellation of claims 1-8 of the '366 patent.

C. Grounds of Challenge – §42.104(b)(2)

Grounds of unpatentability presented in this Petition are as follows.

Ground		Claim(s)	Basis
1	Obvious over Pyo in view of Choi	1-2 and 4-8	§103
2	Obvious over Pyo in view of Choi and Dublin	3	§103
3	Anticipated by Imaoka	1-2 and 4-8	§102
4	Obvious over Imaoka in view of Dublin	3	§103
5	Obvious over Imaoka in view of Choi	1-2 and 4-8	§103
6	Obvious over Imaoka in view of Choi and Dublin	3	§103

Petitioner relies upon expert testimony of R. Michael Guidash (Ex. 1003, hereinafter “Guidash”) and the following primary and secondary references:

1. Pyo (Ex. 1005)

Pyo, Korean Unexamined Patent Application Publication No. 10-2006-0077132, published on July 05, 2006, “more than one year prior to the date of the application for [the ’366 patent] in the United States” (*i.e.*, March 14, 2008), making it §102(b) prior art.² Pyo, 2. Pyo was published in Korean. *Id.*, 11-19. A certified English translation is provided. *Id.*, 2-10.

2. Imaoka (Ex. 1006)

Imaoka, Japanese Patent No. 3800335, published on July 26, 2006, making it §102(b) prior art. Imaoka was published in Japanese. *Id.*, 19-35. A certified English translation is provided. *Id.*, 2-18.

3. Choi (Ex. 1007)

Choi, U.S. Publication No. 2005/0012166A1, published on January 20, 2005, making it §102(b) prior art. Choi, face.

4. Dublin (Ex. 1008)

Dublin, U.S. Patent No. 5,695,810, issued on December 9, 1997, making it §102(b) prior art. Dublin, face.

² All citations are to pre-AIA 35 U.S.C. unless otherwise noted.

5. Background References

Petitioner also relies on the following references (among others) to establish the state of the art and POSAs' knowledge.

Doering (Ex. 1010), an excerpt of “Handbook of Semiconductor Manufacturing Technology,” published by “CRC Press,” bears a 2008 copyright date. Doering, 1-2. Doering is only relied upon as evidence of the state of the art. *Yeda Rsch. v. Mylan Pharms.*, 906 F.3d 1031, 1041 (Fed. Cir. 2018) (“Board can rely on evidence other than just prior art.”).

Edelstein (Ex. 1011), a paper entitled “Full Copper Wiring in a Sub-0.25 μm CMOS ULSI Technology,” was published by IEEE in its 1997 International Electron Devices Meeting Technical Digest. Edelstein, 7-8. Edelstein is cited by U.S. Patent No. 6,429,120, which issued on August 6, 2002. Ex. 1012, 1:40-46. A UWM library received Edelstein on March 4, 1998, and was “catalogued and available to library patrons within a few days or at most 2 to 3 weeks after March 4, 1998.” Edelstein, 2, 6.³ Edelstein is therefore §102(b) prior art. *Tetra Tech Canada v. Georgetown Rail Equip.*, IPR2019-01581, Paper 17, 20-22 (PTAB Feb. 11, 2021) (crediting testimony from same declarant concerning public accessibility of publication from UWM library system).

³ A copy as found in the library is included in Ex. 1011 at 9-12.

Pratt (Ex. 1013), a paper entitled “Overview of the Use of Copper Interconnects in the Semiconductor Industry,” bears a 2004 copyright date and states “Printed in U.S.A.” Pratt, 23. The “Wayback Machine” archived Pratt as early as June 21, 2006. *Id.*, 1-2.⁴ Pratt therefore constitutes §102(b) prior art. *Valve Corp. v. Ironburg Inventions Ltd.*, 8 F.4th 1364, 1375-76 (Fed. Cir. 2021) (upholding reliance on Wayback Machine to establish public accessibility).

Quirk (Ex. 1014), an excerpt of “Semiconductor Manufacturing Technology,” was published by “Prentice-Hall” and bears a 2001 copyright date. Quirk, 1-2. The Board has recognized Prentice-Hall as “a well-known publisher.” *Intel. v. Qualcomm*, IPR2018-01429, Paper 8, 15 (PTAB Feb. 15, 2019); *Arista Networks v. Cisco Sys.*, IPR2016-00303, Paper 53, 18 (PTAB May 25, 2017) (finding “book published by a well-known publisher, i.e., Prentice Hall” prior art as of its copyright date). For established publishers such as Prentice-Hall, “absent some indication that the reference was not publicly available, demonstrating a date of publication is alone sufficient for showing accessibility to the public.” *Microsoft v. IPA Techs.*, IPR2018-00794, Paper 11, 10-11 (PTAB Oct. 15, 2018); *see also Arista* at 21 (“[I]t serves the interest of justice to allow the Petitioners to rely on the

⁴ A copy as archived is included in Ex. 1013 at 4-23.

copyright date of technical references published by a well-known publisher....”).

Quirk therefore constitutes §102(b) prior art.

Gambino (Ex. 1023), a paper entitled “Optimization of Cu Interconnect Layers for CMOS Image Sensor Technology” (Gambino, 21), was first presented at the Advanced Metallization Conference 2005 held on September 27- 29, 2005, in Colorado Springs, Colorado (*id.*, 5), and was subsequently published by the Materials Research Society in 2006 (*id.*, 6). The British Library received a copy of Gambino, cataloged it, and made it available for public use on December 22, 2006. *Id.*, 1.⁵ Petitioner’s expert, Mr. Guidash, was personally involved in the 2003-2005 project culminating in Gambino’s publication. Guidash, ¶17. Gambino therefore constitutes §102(b) prior art.

Yadid-Pecht (Ex. 1024), an excerpt of “CMOS Imagers: From Phototransduction to Image Processing,” published by “Kluwer Academic Publishers” and bears a 2004 copyright date. Yadid-Pecht, 1-3. International Publication No. WO 2006/008637 A1, which published on January 26, 2006, cites Yadid-Pecht. Ex. 1025, 5-6; *see also* Guidash, ¶142 (explaining how Kluwer Academic Publishers merged into Springer, “producing the world’s second-largest academic publishing house,” citing Ex. 1026, 2). Yadid-Pecht therefore constitutes §102(b) prior art. *Microsoft* at 10-11; *Arista* at 21.

⁵ A copy as found in the library is included in Ex. 1023 at 21-27.

IV. THE '366 PATENT

The '366 patent, filed on March 14, 2008, claims benefit of KR 10-2007-0024914 ("KR '914"), itself filed on March 14, 2007. Without conceding priority entitlement, for purposes of this Petition only, it is assumed the Challenged Claims were effectively filed as of March 14, 2007. The Grounds herein render the Challenged Claims unpatentable as of that date.

A. Embodiment

The '366 patent discloses and claims an image sensor with a cross-sectional view shown in Figure 8 (original, below). Guidash, ¶72.

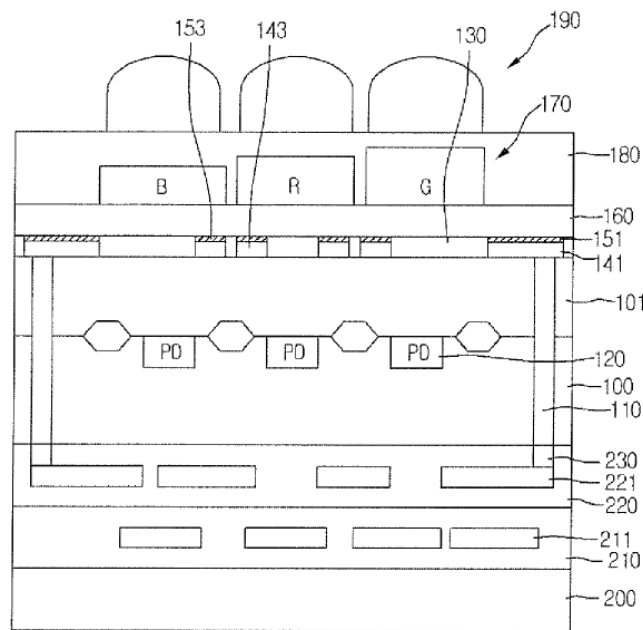


FIG. 8

Photodiodes in the pixel region are connected to interconnections on the first substrate (141, 143) by “a contact (not shown).” '366 patent, 2:43-44; Guidash,

¶73. Interconnections are connected to the first via (110), which penetrates the pre-metal dielectric (“PMD”) (101) and the first substrate (100) to be exposed at the bottom surface of the first substrate. *Id.*, 2:35-43. A second substrate is bonded to the first, allowing the signal from the first via (110) to a second via (230) and into the interconnections of the second substrate (221). *Id.*, 2:63-67, 3:1-4, 3:26-31.

B. Person of Ordinary Skill in the Art

Person having ordinary skill in the art (“POSA”) in the 2007 timeframe would have had at least a Bachelor’s degree in electrical engineering, physics, microelectronics, or material science and approximately 3-5 years of industrial experience or equivalent research or teaching experience, or a Master’s degree in the same fields and 1-3 years of industrial experience or equivalent research or teaching experience in the field of semiconductor image sensor design and fabrication. Guidash, ¶¶67-69. The levels of education, experience and knowledge can trade off against one another. *Id.*

C. Prosecution History

1. Korean Priority Application

KR ’914 was filed with 15 claims: 1-6 recited an image sensor and 7-15 recited a method of manufacturing an image sensor. Ex. 1018, 4-8.

The Korean examiner rejected claim 1 because it was “***similar to the configuration*** in [Pyo].”⁶ Ex. 1019, 2-3. The Korean examiner identified only one difference: “***the conductive barrier film*** on the metal wiring.” *Id.* However, the Korean examiner noted such film “***is commonly used*** in this field” and cited a Japanese application “in which a barrier metal is formed on the wiring layer.” *Id.*, 3. The Korean examiner rejected dependent claims 2-6 because “these limitations limit simple materials or are merely structural changes, and it is not technically difficult to apply these limitations.” *Id.*

The Applicant presented no contrary argument and cancelled the image sensor claims. Ex. 1018, 4-8.⁷ Those rejected and subsequently cancelled claims are substantially the same as the Challenged Claims. *Compare id.*, 4-5, with ’366 patent, claims 1 and 3-5; Guidash, ¶76.

2. The ’366 Patent

Applicant filed the ’366 patent’s application on March 14, 2008—three weeks after the Korean examiner rejected substantially similar claims (Ex. 1019, 2). Applicant filed an IDS listing Pyo and provided an English-language translation of its abstract but submitted Pyo only in its original Korean. Ex. 1002, 29-39, 53-

⁶ Emphasis is added throughout unless otherwise noted.

⁷ By contrast, the Applicant amended method claims 7-15 to traverse the rejection.

54. Pyo's abstract fails to disclose material aspects of Pyo's sensor design including (1) a first and a second ILDs, (2) a PMD, (3) a first metal interconnection⁸, and (4) a color filter. *Compare* claim 1 with Ex. 1002, 30; Guidash, ¶79. Applicant did not submit a copy of the Korean examiner's rejection or Applicant's cancelation of the sensor claims.

Apparently unaware of Pyo's significance, and without the Korean examiner's rejection as a guide, the U.S. Examiner allowed the Challenged Claims without rejection over any prior art. Ex. 1002, 97-104.

D. Challenged Claims

Claim 1 is the only independent Challenged Claim. It recites:

[1.pre⁹] An image sensor, comprising:

[1.1] a second semiconductor substrate including a second metal interconnection and a second interlayer dielectric;

[1.2] a second via penetrating the second interlayer dielectric so that the second via is connected to the second metal interconnection;

[1.3] a first semiconductor substrate on the second interlayer dielectric, the first semiconductor substrate having a unit pixel;

[1.4] a pre-metal dielectric on the first semiconductor substrate;

⁸ The abstract only discloses metal lines on the **second** substrate. Guidash, ¶79.

⁹ Reference numbers have been added.

[1.5] a first via penetrating the pre-metal dielectric and the first semiconductor substrate, the first via being connected to the second via;

[1.6] a first interlayer dielectric on the pre-metal dielectric including the first via;

[1.7] a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel;

[1.8] a conductive barrier layer on the first metal interconnection; and

[1.9] a color filter and a microlens on the first interlayer dielectric on the unit pixel.

Claims 2-8 depend directly from claim 1. Some specify particular material(s) for interconnections (claims 2 and 5), barrier layer (claim 3), or vias (claim 7). Others specify relationships of the surfaces of metal interconnections (claim 4) or barrier layers (claim 6). Claim 8 requires “the second semiconductor substrate provides metal interconnections for connection to a power line and an external signal line.”

V. CLAIM INTERPRETATION

Claim terms are interpreted in accordance with “the ordinary and customary meaning” as understood by POSAs. 37 C.F.R. §42.100(b). The Board need only interpret terms to the extent necessary to resolve disputes between parties.¹⁰ *Niddec*

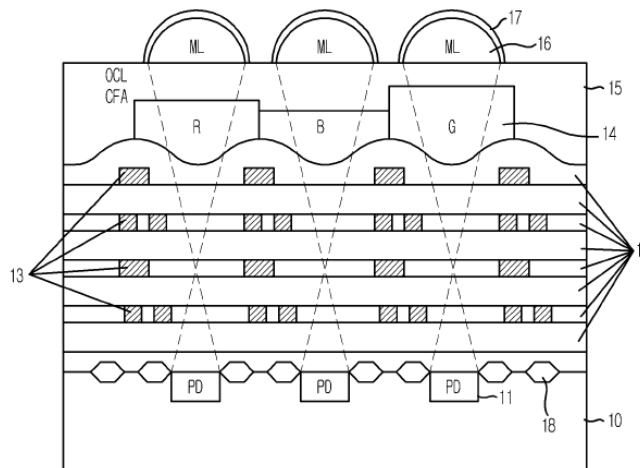
¹⁰ Petitioners are not waiving any arguments concerning claim scope necessary for resolving other proceedings.

Motor v. Zhongshan, 868 F.3d 1013, 1017 (Fed. Cir. 2017); 83 Fed. Reg. 51,340, at 51,353. As explained in §VI, the Challenged Claims use several terms consistently with how they are used in the art, for which Petitioner provides definitions. *AFG Indus. v. Cardinal IG*, 239 F.3d 1239, 1248 (Fed. Cir. 2001). As the terms are used consistently with how they are used in the art, Petitioner does not believe any term requires construction for purposes herein.

VI. PRECISE REASONS FOR RELIEF REQUESTED

In the mid-2000s, some CMOS image sensors had a single substrate with interconnections above photodiodes. Ex. 1017 (“Yun”), Fig. 1; Guidash, ¶39.

Yun, Fig. 1



As image resolution increased, however, “the size of the unit pixel is gradually reduced,” thereby also reducing “the area ratio of the photodiode 11 per unit pixel.” Yun, 8. This “reduced sensitivity with respect to incident light.” Yanagida, [0004]. One known solution was relocating the interconnections below

the photodiodes in a stacked design such as disclosed by Pyo (Grounds 1-2) and Imaoka (Grounds 3-6). Guidash, ¶43.

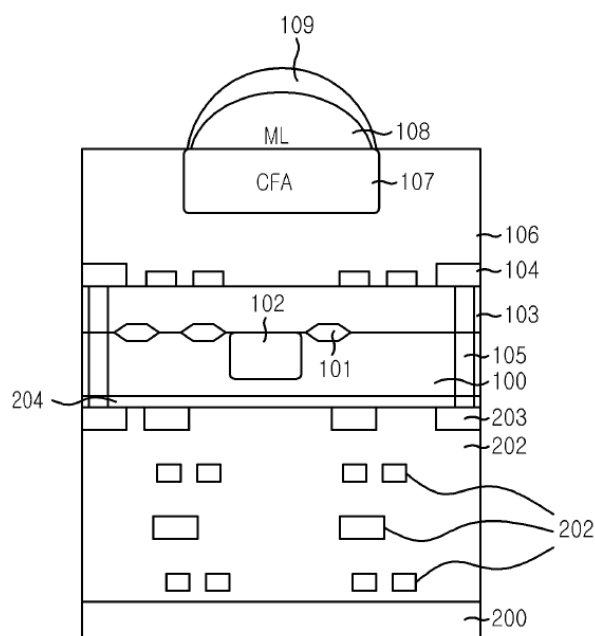
A. GROUND 1: Pyo in view of Choi Renders Claims 1-2 and 4-8 Obvious

Pyo discloses a stacked design just like the one claimed except that Pyo’s metal lines (104) lack a conductive barrier layer. Guidash, ¶148. But Pyo discloses metal interconnections can be copper. Choi discloses that copper interconnections had advantages over aluminum ones (the alternative), but that copper required barrier layers. Choi disclosed a method for fabricating copper interconnections with barrier layers, commonly known as damascene processes. *Id.*, ¶150. POSAs would have been motivated to use copper for Pyo’s interconnections and would have had a reasonable expectation of success in doing so because by 2007, the damascene processes had become ubiquitous in CMOS manufacturing. *Id.*, ¶151.

1. Pyo’s Sensor

Pyo’s design uses “two chips,” separating the “image chip” from the “logic chip.” Pyo, 2. By omitting metal lines atop photodiodes, “the distance between the photodiode and the microlens is reduced to dramatically reduce the optical path, thereby improving the photosensitivity.” Pyo, 2, Fig. 3 (original, below); Guidash, ¶106.

FIG. 3



Pyo's metal lines (104) serve a "light-shielding function" and connects unit pixels to metal lines (201)¹¹ through vias (105). Pyo, 5; Guidash, ¶152. Pyo does not disclose materials for lines (104) but discloses metal lines (201) are "aluminum or copper." Pyo, 5. Aluminum and copper were each well-known options for interconnections in CMOS manufacturing, and each would achieve light-shielding and interconnection functions of Pyo's metal lines (104) because each is opaque and conductive. Guidash, ¶152.

¹¹ The metal lines 201 are mis-labeled in Figure 3 as 202. Guidash, ¶107.

A “connecting portion 105” is “connected to the metal line 104 through the rear surface of the first substrate 100,” and may be “tungsten, aluminum, copper, or the like.” Pyo, 6.

A “pad 203 [is] connected to the metal line 201” on the second substrate. *Id.*, 6. A connection between layers (such as between Pyo’s pad 203 and lines 201) is called a via. *Id.* (connecting portion 105 formed using a “super via process”); Quirk, 54 (a via is a hole filled with a metal plug to “form an electrical pathway” from one metal layer to another); Guidash, ¶¶95-97.

2. Reasons to Use Copper Throughout Pyo’s Sensor

Pyo does not disclose materials for lines (104) but teaches metal lines (201) are “copper or aluminum.” Pyo, 5. Both metals would serve “light-shielding” and interconnection functions Pyo discloses for lines (104), but POSAs would have had reasons to pick copper over aluminum. Guidash, ¶152.

a. Aluminum Was “No Longer Satisfactory” For Pattern Sizes Below 0.13 μm

A significant benefit of CMOS image sensors is that they are manufactured using the same equipment as other CMOS chips. Pyo, 3 (desirable to use “CMOS technology *that has previously been set-up*”); Yadid-Pecht, 30-31 (image sensors “are fabricated in a commonly used CMOS process”); Guidash, ¶¶154-157. By 2007, that meant using 0.13 – 0.045 μm design rules. Pyo, 5 (design “can be loaded with core logic technology of 130 nm and 90 nm or less *as it is*”); Pratt, 5, 10 (by

2004, manufacturers were offering tools for copper interconnections “extendable beyond the 65 nm node” and “[s]everal advanced chipmakers ha[d] announced breakthrough technologies down to 45 nm”). POSAs would have understood Pyo’s sensor was compatible with at least 0.13 – 0.09 μm design rules. Pyo, 5; Guidash, ¶¶154-157.

Choi discloses that “[w]hen manufacturing semiconductor devices having a pattern size less than about 0.13 μm , *aluminum is no longer satisfactory*.” Choi, [0007]; see also Doering, 5 (“*aluminum etch to circuit dimensions below 0.10 μm has been difficult*”). Using copper avoided this limitation. Guidash, ¶55; Choi, [0139] (disclosing “multi-layered interconnections [using] *copper* ... under a process condition having *a design rule of about 0.13 micrometer*.”); see also Quirk, 54 (2001 text noting ongoing “transition” from aluminum to “copper metallization”).

Using then-current fabs in 2007 would have thus meant employing copper interconnections in Pyo’s design. Guidash, ¶¶154-157.

b. Choi Disclosed Copper’s Low Resistivity

Copper also had performance advantages over aluminum-based materials including “low resistance, thereby minimizing problems.” Choi, [0139] (touting benefits of copper for “multi-layered interconnections”).

POSAs indeed would have known copper's low resistivity offered advantages over aluminum. Quirk, 59 (“[I]nterconnect wiring resistivity reduces from 2.65 $\mu\Omega$ -cm for aluminum to 1.678 $\mu\Omega$ -cm at 20°C for copper, reducing RC signal delay.”); Edelstein, 9 (“Cu wiring has advantages of significantly lower resistance”); Pratt, 5-7; Doering, 4; Brase, 1:15-22; Guidash, ¶153.

c. Other Advantages Known to POSAs

POSAs would also have known additional advantages of copper interconnections over aluminum ones:

- 1. Reduction in power consumption.** Lower resistivity permitted narrower lines, which “consume less power.” Quirk, 59; Doering, 4-5 (“the resistivity advantage of copper over aluminum ... allowed for smaller line dimensions”); Pratt, 8 (“copper results in a power consumption reduction of 30%”); *see also* Guidash, ¶48.
- 2. Tighter packing density.** POSAs sought to enable “miniaturization” of CMOS sensors. Pyo, 3. “Narrower lines permit tighter circuitry packing.” Quirk, 60. “As wafer fabrication design rules reduce to 0.15- μ m linewidths and below, the increased packing density ... leads to improved chip performance” (*id.*) by permitting more light to reach photodiodes (Guidash, ¶51).

3. **Resistance to electromigration.** “Electromigration causes transport of the conductor material as a result of high current densities, which can ultimately lead to a void in the conductor.” Pratt, 8. “[C]opper has ten to 100 times more resistance to electromigration failures than aluminum.” *Id.*; Quirk, 60; Doering, 5; Brase, 1:22-24; *see also* Guidash, ¶49.
4. **Fewer processing steps resulting in higher yields relative to aluminum.** Narrower lines simplifies “interconnect routing,” thus “reducing the number of interconnect levels and resulting in fewer process steps.” Pratt, 8; Doering, 5 (“the advantages of copper interconnects result in ... fewer interconnect metal levels”); Quirk, 82 (“Reducing process steps ... improv[es] the yield....”); Gambino, 21 (“Cu interconnect technology ... reduc[es] the polishing of the interconnect dielectric”); *see also* Guidash, ¶50, 158-159.

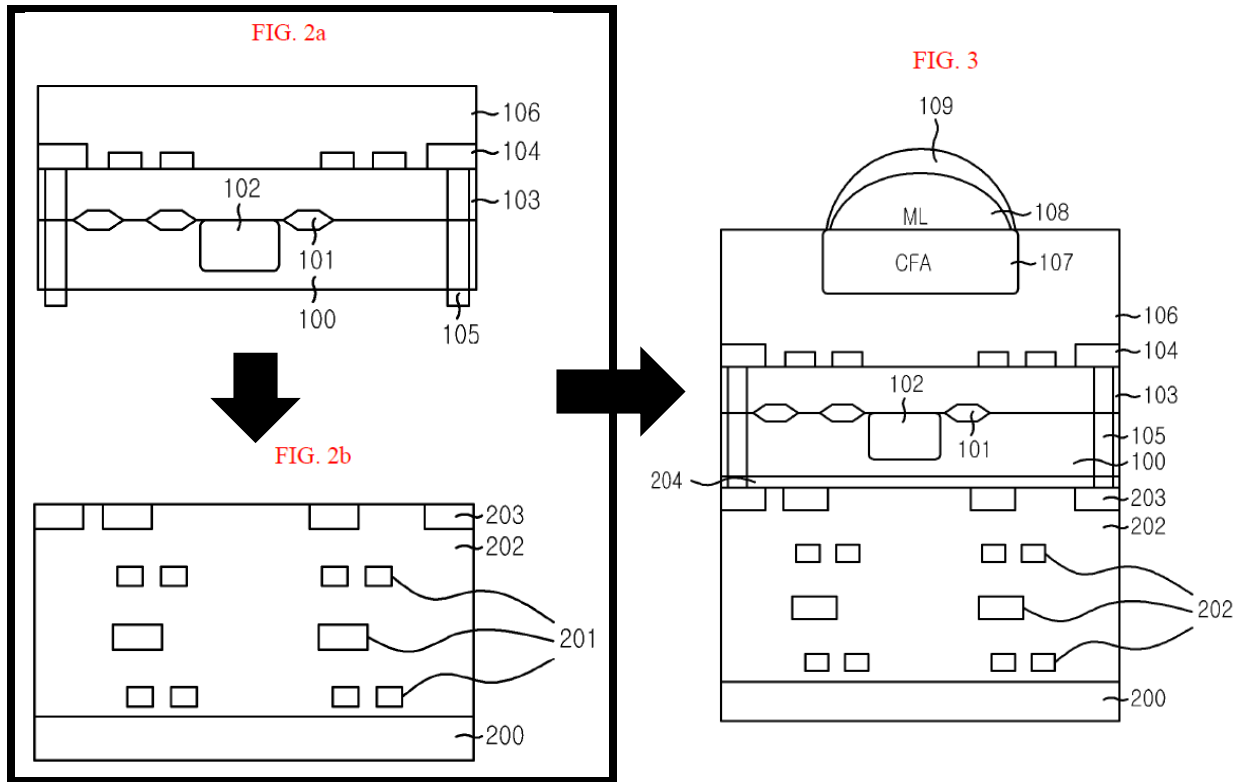
These advantages made copper interconnections commonplace in CMOS manufacturing by 2004 (Doering, 5), and they had been incorporated in CMOS image sensors by 2005 (Gambino, 21). By 2007, POSAs would have had reason to use copper in Pyo’s design too. Guidash, ¶¶152-159.

d. Obvious to Try

The Supreme Court endorsed an “obvious to try” analysis where “there are a finite number of identified, predictable solutions,” and POSAs had “good reason to pursue the known options within [their] technical grasp.” *KSR Int’l v. Teleflex*, 550 U.S. 398, 421 (2007). Here, Pyo discloses two possibilities for metal lines: “copper or aluminum.” Pyo, 5. It would have been obvious to try copper as one of the two. Guidash, ¶160; *Uber Techs. v. X One*, 957 F.3d 1334, 1339 (Fed. Cir. 2020) (reversing Board and noting that claim element would have been obvious to try when record “reflect[ed] only two possible methods”). Given the extensive prior-art teachings concerning copper interconnections, this is not a situation that would have required “try[ing] every available option until one succeeds” or “explor[ing] a new technology ... [with] only general guidance.” *In Re: Copaxone*, 906 F.3d 1013, 1025 (Fed. Cir. 2018) (obvious to try one of two disclosed doses).

3. Resulting Pyo-Choi Sensor

Pyo separately fabricates logic and image chips before bonding them together. Pyo, 5-6, Figs. 2a-2b, 3 (below); Guidash, ¶196.

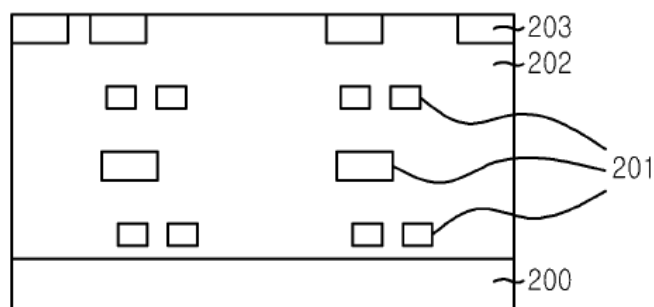


POSAs would do the same for Pyo-Choi. Guidash, ¶197.

a. Fabricating the Logic Chip

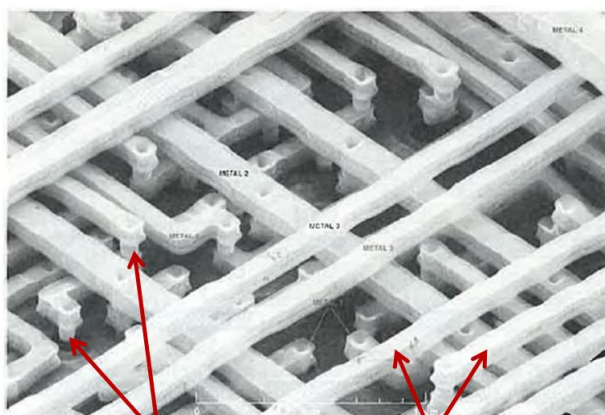
Pyo discloses its logic chip has a “a **plurality** of metal lines 201”; the figures show four levels of wiring, and Pyo also discloses “it is possible to form a logic element with 6-layer wiring or more.” Pyo, 5, Figs. 2b (below, original) and 3. Pyo also describes “pads 203” as “**connected** to the plurality of metal lines 201.” *Id.*, 5. POSAs would therefore recognize the existence of a connection from pad 203 to metal lines 201 even though not expressly reflected in Pyo’s figures. Guidash, ¶163.

FIG. 2b



POSAs would similarly recognize Pyo's logic chip had connections between layers of wiring (201) even though not expressly reflected in Pyo's figures. *Id.*, ¶164. Such simplifications were commonplace in such figures; for example, a two-dimensional cross-section does not illustrate all the vias and lines in the network shown in a three-dimensional micrograph. *Id.*; Quirk, 14, 55.

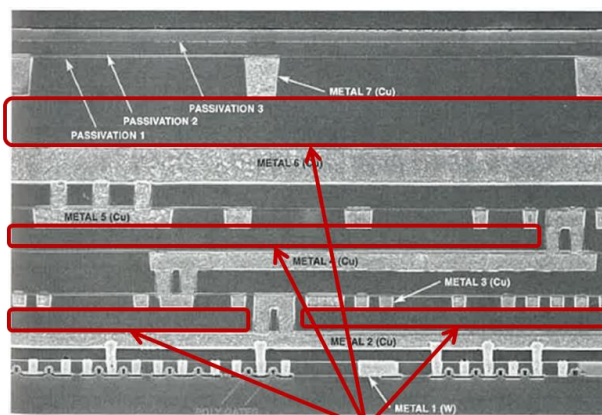
Three-Dimensional View



Vias

Lines / wires

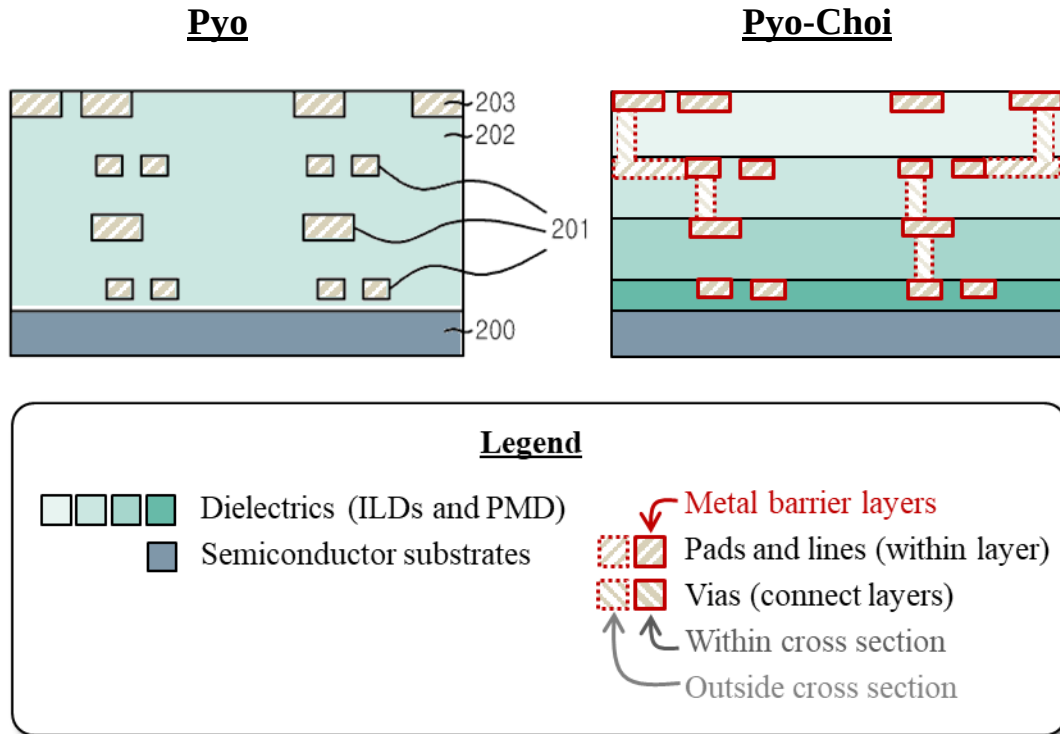
Cross-Section



Vias Connecting Wires Not Shown

POSAs would understand Pyo's design had interconnections between levels of metal lines (201) even though Pyo's figures do not illustrate such details. Guidash, ¶165. Such interconnections are required for Pyo's sensor to function. *Id.*

Exemplary lines and vias outside the cross section are thus illustrated below, right, to better depict Pyo’s sensor’s “three-dimensional structure.” *Id.*; Pyo, 4, Fig. 2b (below left).



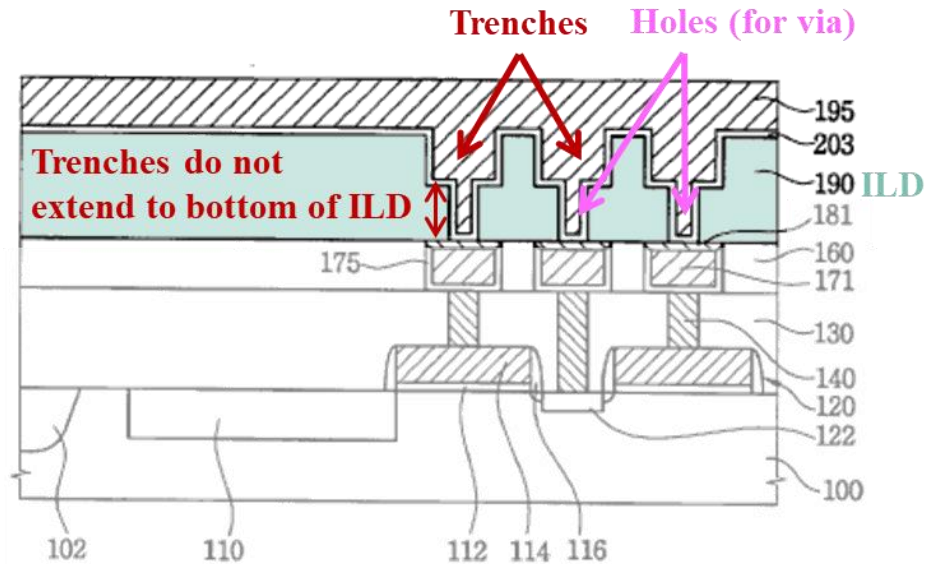
i. Choi’s Fabrication Method

Choi discloses image sensors in which copper-based lines and vias are fabricated together—a technique commonly known as the dual-damascene process. Choi, [0124]-[0132], Figs. 5E – 5G; Guidash, ¶166.

(1) ILD and Patterning

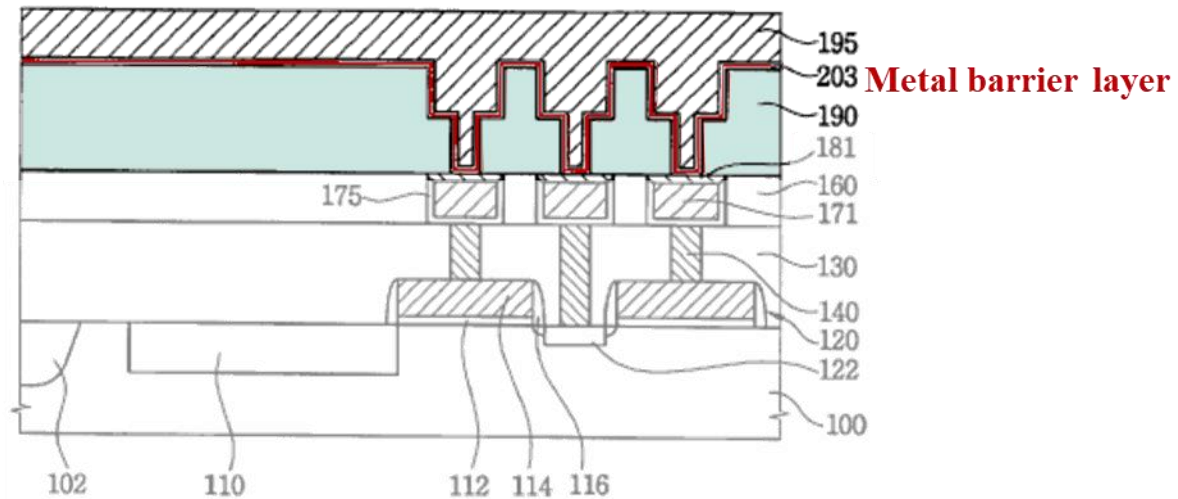
First, an “insulating interlayer 190” is formed and then “partially removed, e.g., etched using photolithography.” Choi, [0124]-[0125], Figure 5E; Guidash, ¶167. While Choi patterns trenches and holes in one etching step, POSAs would

have known multiple etches could be used in various orders interchangeably (see, *e.g.*, Quirk, 80-82, Brase, 1:47-2:10)—yielding the same results. Guidash, ¶167. Choi teaches trenches for lines would not extend to the bottom of the ILD layer. *Id.*; Choi, Fig. 5E (below).



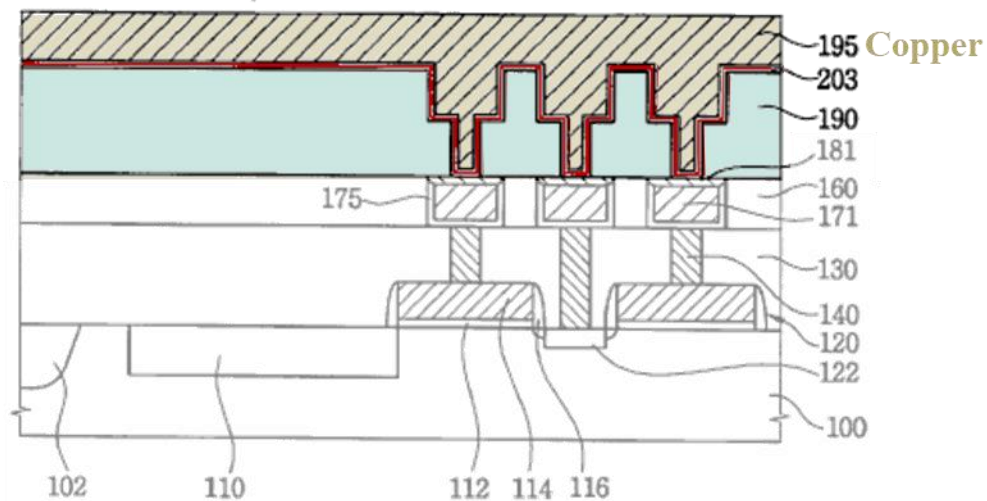
(2) Bottom Metal Barrier Layer

Choi deposits a metal barrier layer over the patterned ILD. Choi, [0126], Fig. 5E (below); Guidash, ¶168. This barrier “prevent[s] diffusion of the copper into surrounding materials.” Choi, [0008]. Choi discloses tantalum (Ta) and tantalum nitride (TaN) as suitable. *Id.*, [0066]. Each is a conductive metal. Guidash, ¶168 (citing Quirk, 62-63).



(3) Copper Deposition

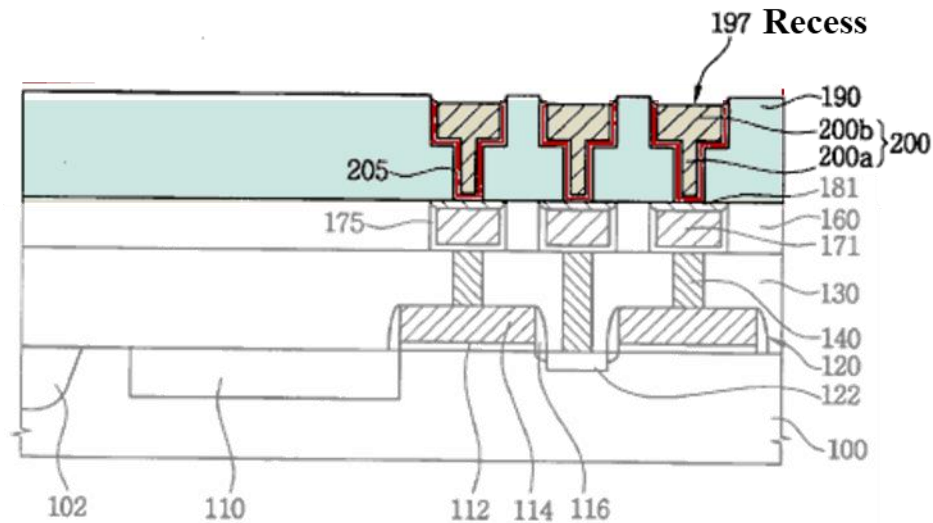
Next, trenches and holes (“vias”) are filled with copper. Choi, [0126], Fig. 5E (below); Guidash, ¶169.



(4) Chemical Mechanical Polishing (“CMP”)

“[C]opper layer 195 is removed, e.g., using CMP, so that the first copper interconnection 200 ... is formed” with “upper surface of the first copper interconnection 200 ... positioned ... lower than the upper surface of the second

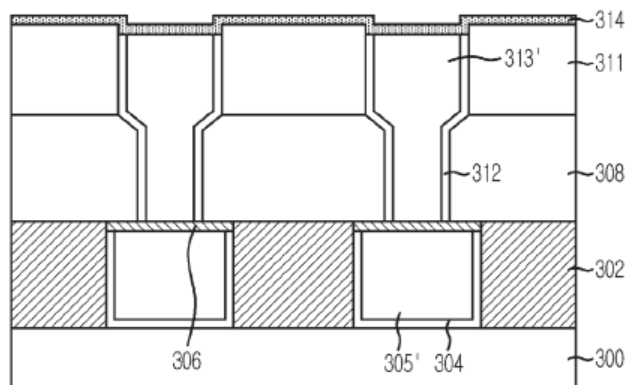
insulating interlayer 190, so a second recess 197 ... is formed.” Choi, [0128], Fig. 5F (below); Guidash, ¶170.



Creating a recess as Choi does was common in CMOS manufacturing.

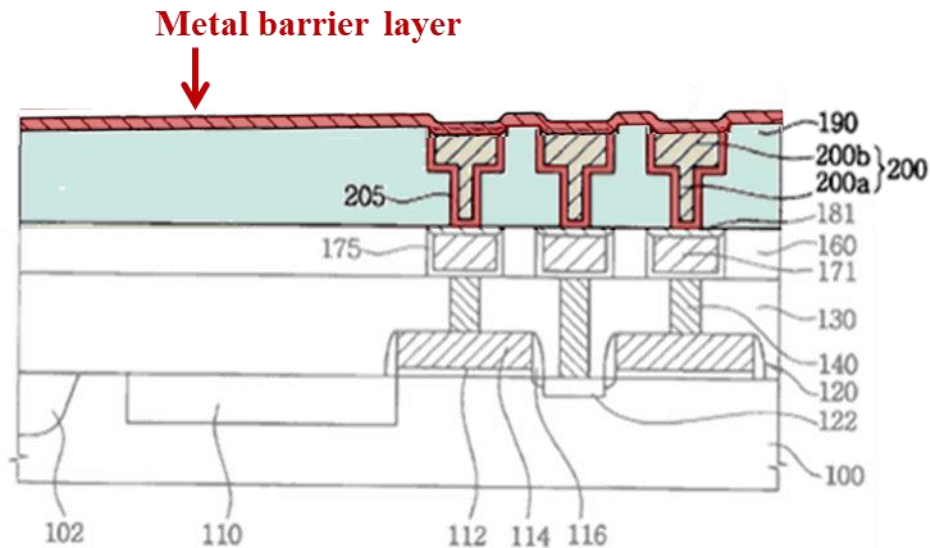
Guidash, ¶171; Yun, 13 (“excessive polishing is performed so that the copper layer 313 and the third barrier layer 312 filled in the upper trench are recessed”), Fig. 3i (below).

FIG. 3i



(5) Top Metal Barrier Layer

A metal barrier layer is next deposited across the surface. Choi, [0121]-[0122], [0129], Fig. 5C. The metal barrier layer applied to Choi's Figure 5F would appear as shown below. Guidash, ¶¶172-173.



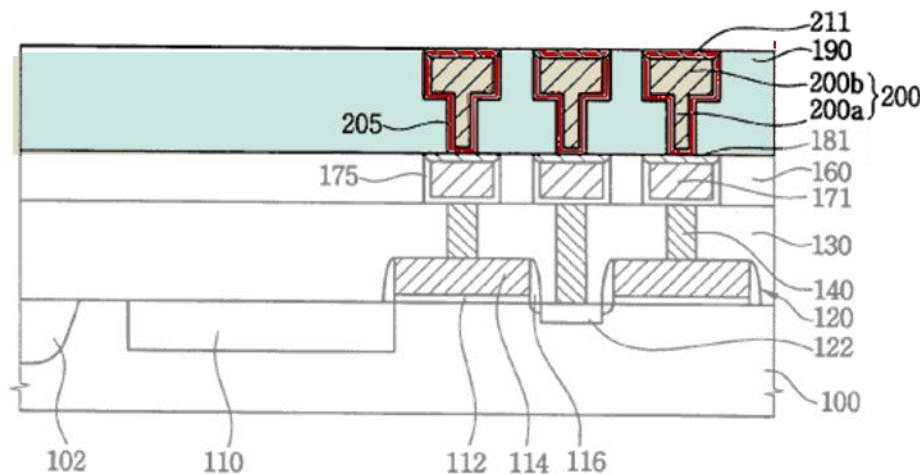
POSAs would understand Choi's "diffusion preventing pattern" prevents copper from diffusing into surrounding materials (Choi, [0007]) and subsequent layers from oxidizing the copper (Dublin, 2:16-24), making it a barrier layer. Guidash, ¶174. Choi discloses tungsten and tungsten nitride are suitable (Choi, [0122]); each are conductive metals. Guidash, ¶174.

While also disclosing insulators as alternative barrier materials, Choi cautions that insulators "may negatively impact the performance of image devices" (Choi, [0008]) and need to "be removed during the etching" (*id.*, [0125]). POSAs

would have thus preferentially used conductive metals, not insulators. Guidash, ¶175; Quirk, 62-63; Gambino, 21.

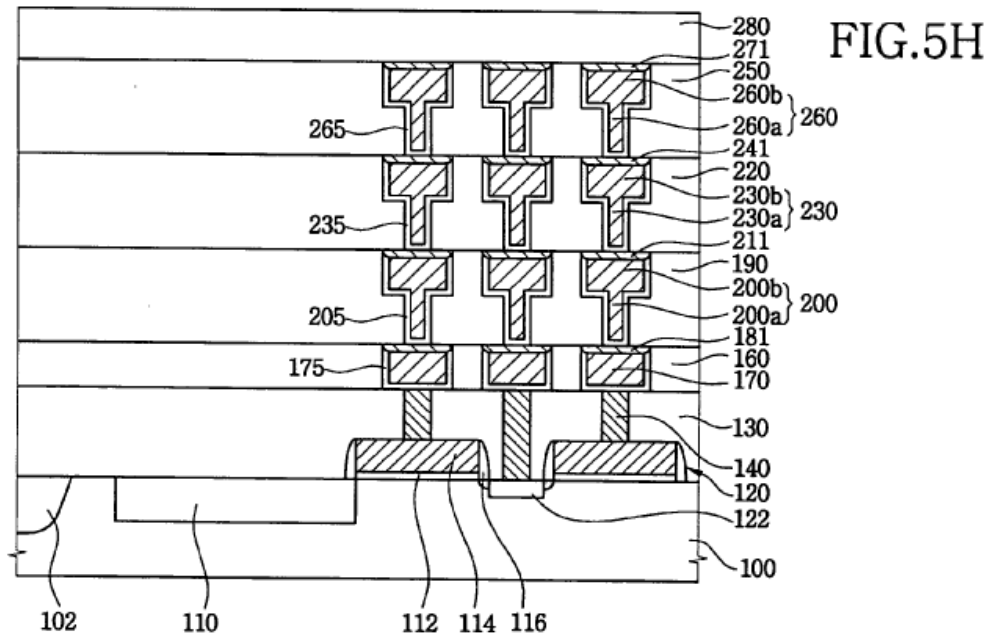
(6) Planarization

Choi then planarizes the barrier layer “by CMP, such that [it] remains only in the second recess 197.” Choi, [0129], Fig. 5G (below); Guidash, ¶176.



(7) Subsequent Levels

Choi repeats steps (1) through (6) to form subsequent metal layers. Choi, [0130]-[132] (“a multi-layered structure” may be formed “by repeatedly performing the processes described”), Figure 5H (below); Guidash, ¶177. Notably, when using metal barrier layers as discussed above, they need not be etched away for subsequent levels. Choi, [0125]; Guidash, ¶177.



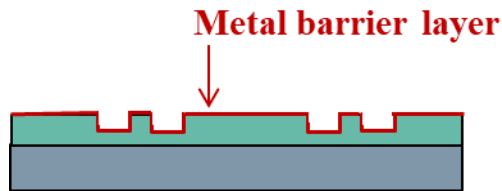
ii. Applying Choi's Process to Fabricate the Pyo-Choi Logic Chip

As of at least 2001, “*the dual-damascene process became the consensus process for copper metallurgy*” and thus a routine means for incorporating copper interconnections. Quirk, 80; Guidash, ¶178. It would thus have been an obvious choice when implementing Pyo’s sensor with copper interconnections. Guidash, ¶178. Starting with second substrate 200, POSAs would have applied Choi’s process as follows to create the first layer of metallization. *Id.*

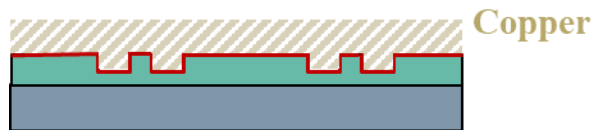
1. **Deposit ILD and pattern** trenches for lines (201) and holes for vias (not shown). §VI.A.3.a.i.(1).



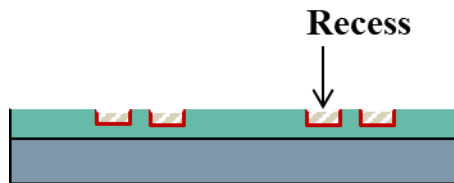
2. **Deposit bottom metal barrier layer.** §VI.A.3.a.i.(2).



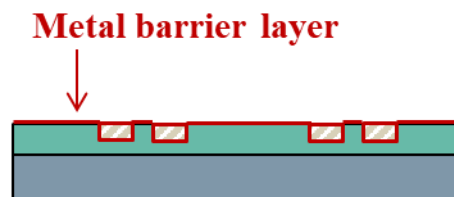
3. **Deposit copper.** §VI.A.3.a.i.(3).



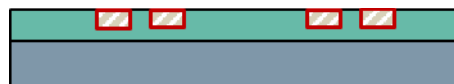
4. **Polish to create recess.** §VI.A.3.a.i.(4).



5. **Deposit top metal barrier layer.** §VI.A.3.a.i.(5).

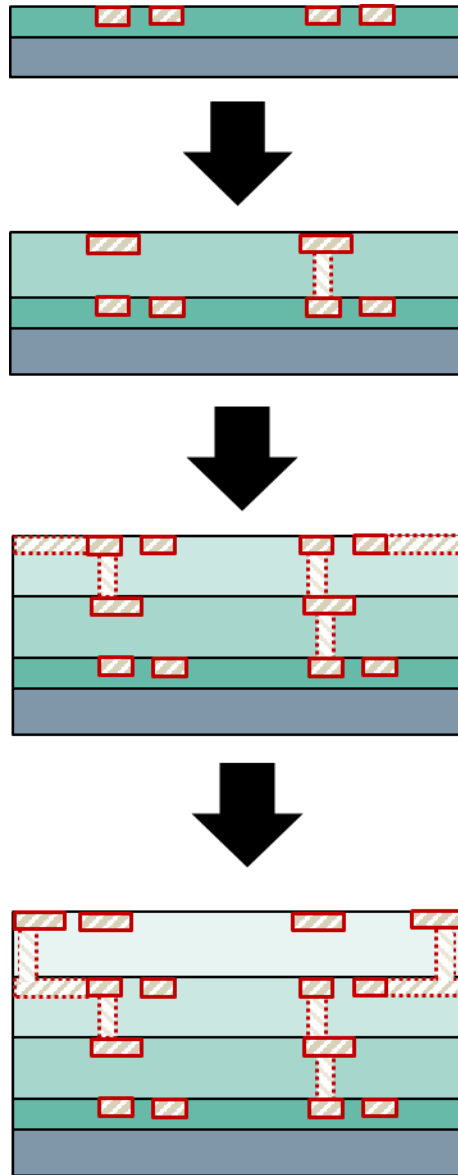


6. **Planarize.** §VI.A.3.a.i.(6).



See also Guidash, ¶¶179-184.

POSAs would have repeated these steps to fabricate each subsequent metal layer. §VI.A.3.a.i.(7); Guidash, ¶185.

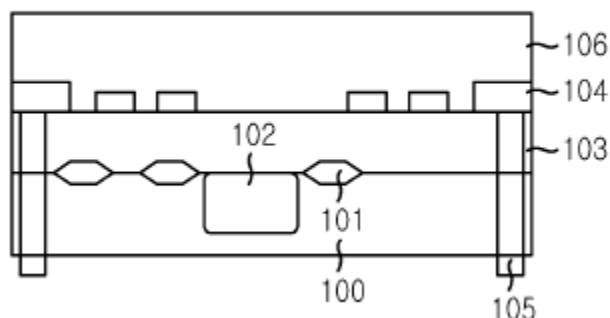


b. Fabricating the Image Chip

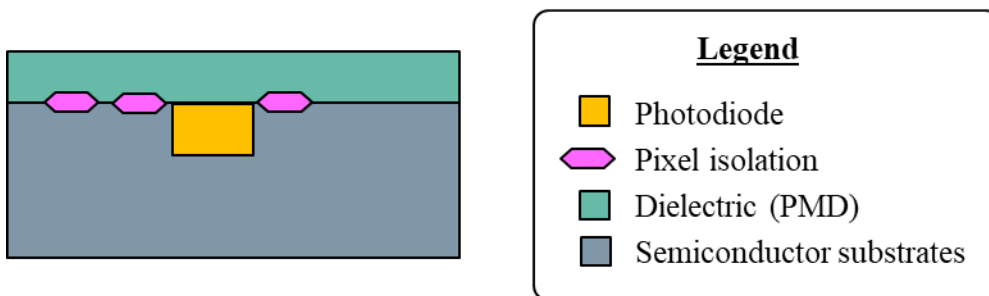
Pyo's image chip included "a field oxide layer 101" "on the first substrate 100," a "photodiode 102," "a plurality of transistors constituting a unit pixel," "an insulating film 103," and a "metal line 104" "connected to the gate electrode or source/drain of the transistor through a contact," where "a connecting portion 105

[is] connected to the metal line 104” using a “super via process.” Pyo, 5-6, Fig. 2a (below, original); Guidash, ¶186.

FIG. 2a

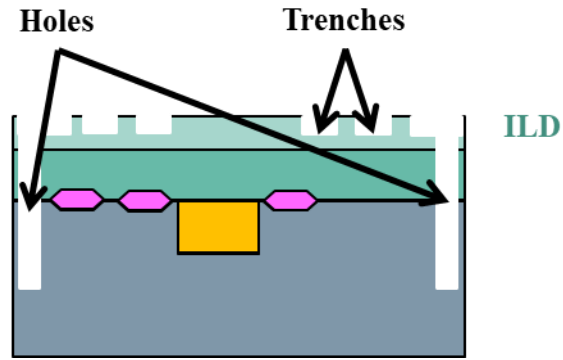


POSAs would understand applying the same dual-damascene process as described for the logic chip would have been an obvious way to implement copper interconnections for Pyo’s image chip. Guidash, ¶187.

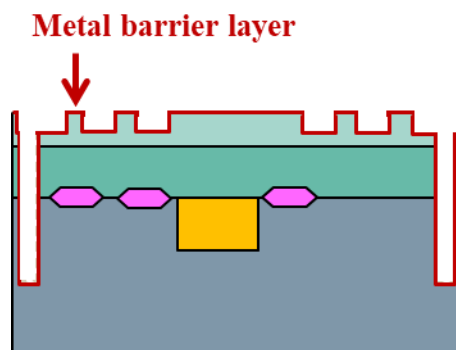


Starting with Pyo’s image chip after insulating film 103 is deposited (above), POSAs would have applied the following steps to create lines (104) and vias (105) in the image chip. *Id.*, ¶188.

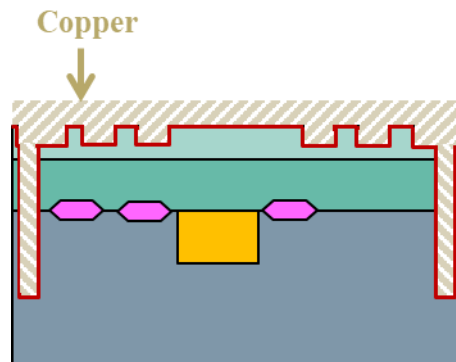
1. **Deposit ILD and pattern** trenches for lines (104) and holes for vias (105). §VI.A.3.a.i.(1). Using Choi’s method, trenches would not extend to the bottom of the ILD layer, below. Choi, Fig. 5E; Guidash, ¶189.



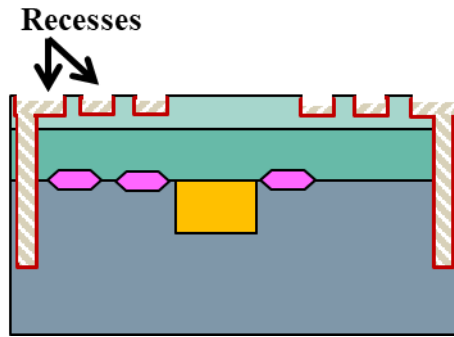
2. **Deposit bottom metal barrier layer.** §VI.A.3.a.i.(2).



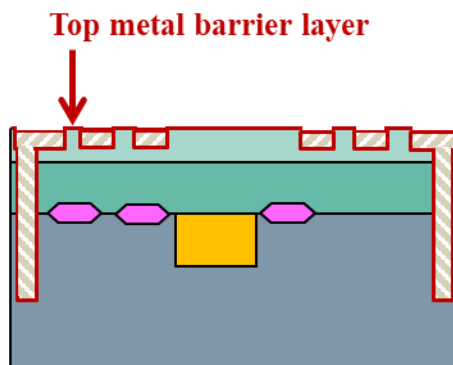
3. **Deposit copper.** §VI.A.3.a.i.(3).



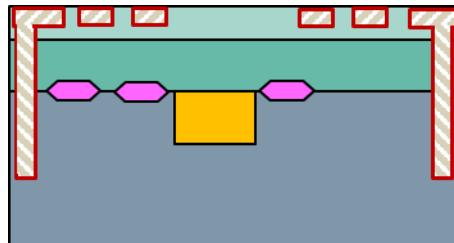
4. **Polish to create recess.** §VI.A.3.a.i.(4).



5. **Deposit top metal barrier layer.** §VI.A.3.a.i.(5).



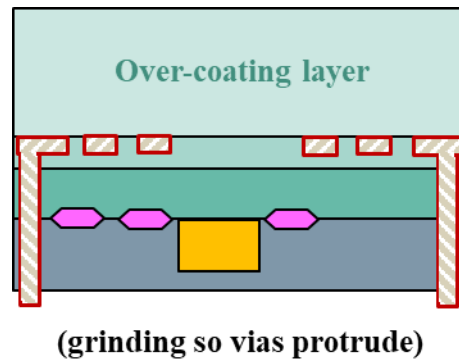
6. **Planarize.** §VI.A.3.a.i.(6).



See also Guidash, ¶¶190-194.

Pyo completes the image chip by depositing “an over-coating layer 106” (Pyo, 5, Fig. 2a) and “grinding the rear surface of the first substrate 100 so that the connecting portion 105 protrudes” (*id.*, 6, Fig. 2a). Guidash, ¶195. POSAs would

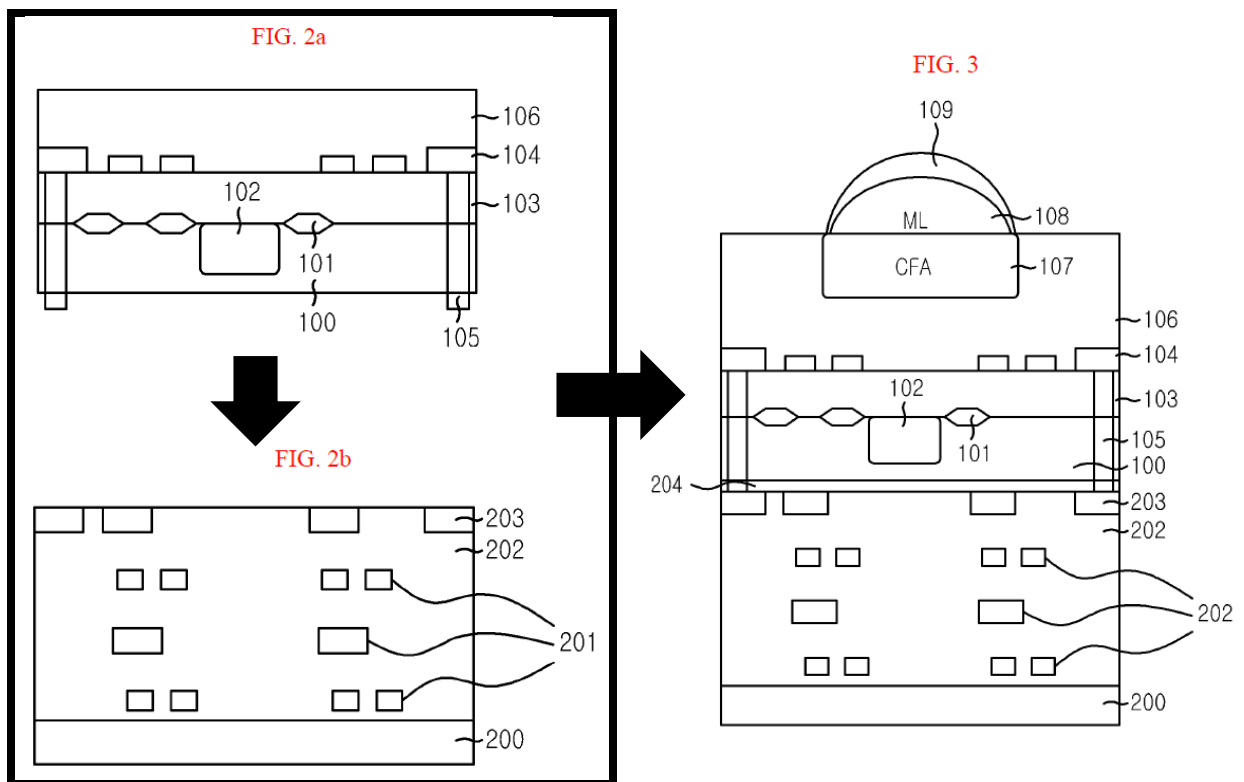
perform these same steps to finish the Pyo-Choi image chip too, below. Guidash,
¶195.



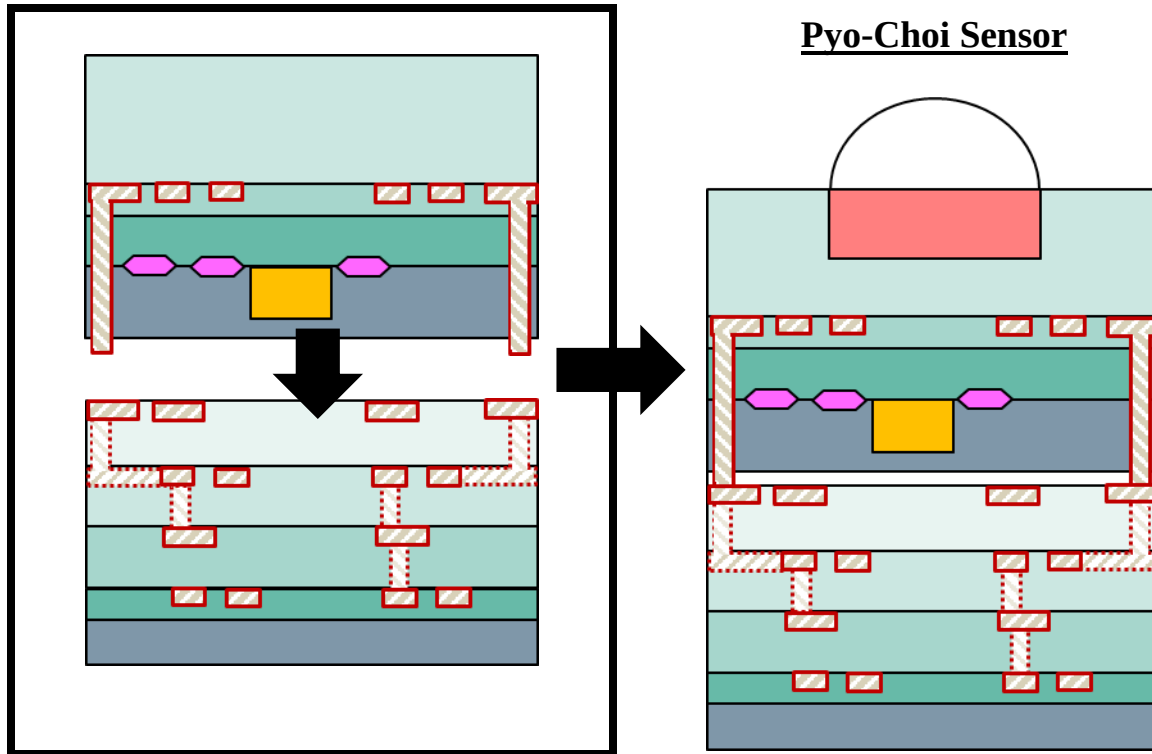
c. Bonding

Pyo discloses bonding the logic chip to the image chip and thereafter forming the “color filter array 107, the microlens 108, and the protective film 109.”

Pyo, 5-6, Figs. 2a-2b, 3; Guidash, ¶196.



POSAs would have done the same for the Pyo-Choi Sensor, below. Guidash, ¶197 (see legend on page 1).



4. Reasonable Expectation of Success

POSAs would have had a reasonable expectation success in modifying Pyo's sensor as described above. *Id.*, ¶198. Pyo identified copper as suitable for interconnections. Pyo, 5. POSAs would have had a reasonable expectation of using copper-based interconnections that Pyo disclosed as being suitable. Guidash, ¶199. And as of at least 2001, "***the dual-damascene process became the consensus process for copper metallurgy***" and thus a routine means for incorporating copper interconnections. Quirk, 80; Doering, 4 ("A variation of the damascene process,

known as the dual-damascene process, has been **widely implemented as the most cost-effective means of producing copper interconnect circuitry.**”); Guidash, ¶200. Barrier layers for copper interconnections were also well known. Quirk, 62, 81 (“7. Deposit barrier **metal**”); Dublin, 3:1-7; Guidash, ¶62. And CMOS image sensors with copper interconnections were known since at least 2005. Gambino, 21. POSAs would thus have had a reasonable expectation of implementing copper interconnections in Pyo’s CMOS image sensor using Choi’s well-known materials and process. Guidash, ¶200.

5. Claim-by-Claim Analysis

The Pyo-Choi Sensor meets every element of claims 1-2 and 4-8, rendering those claims obvious given the above-discussed reasons for modification. Guidash, ¶201.

a. Claim 1

i. [1.pre]

[1.pre] An image sensor, comprising:

To the extent the preamble is limiting, the Pyo-Choi Sensor satisfies the preamble because Pyo’s device is an image sensor. Pyo, 2 (“The present invention is a ... solution to the **next-generation CMOS image sensor.**”), 3 (“The present invention relates to **an image sensor....**”). This aspect would be unchanged after modification. Guidash, ¶203.

ii. [1.1]

[1.1] a second semiconductor substrate including a second metal interconnection and a second interlayer dielectric;

The Pyo-Choi Sensor satisfies limitation [1.1] because Pyo’s “logic chip [is] disposed on a **second substrate**,” which POSAs would understand is a **semiconductor** substrate as Pyo’s sensor is a “**semiconductor** device.” Pyo, 4; Guidash, ¶205.

The second substrate includes second metal interconnections. Pyo discloses “[a] plurality of metal lines 201 ... formed on the second substrate 200” and “a pad 203” formed “on the upper portion of [a] metal line.” Pyo, 4, Fig. 3; Guidash, ¶206. POSAs would understand “metal lines 201” and “pad 203” as interconnections because “interconnection” “describes the conductor materials, ... that create the metal wiring that carries electrical signals to different parts of the chip.” Quirk, 54. Such materials include:

- (i) “lines” extending parallel to the chip’s top surface;
- (ii) “vias” that “form an electrical pathway” from one metal layer to another (i.e., perpendicular to the chip’s top surface); and
- (iii) contacts (a.k.a. pads) at the chip’s surface.

Guidash, ¶¶91-92, citing, Quirk, 54; Brase, 1:40-45. The '366 patent uses “interconnection” consistently with its meaning in the art. For example, in claim 1, the unit pixel is connected to the first metal interconnection, which is connected to the first via, which is connected to the second via, which is connected to the second metal interconnection—thereby allowing signals generated when light strikes the unit pixel on the image chip to propagate to the second metal interconnections on the logic chip. Guidash, ¶92. Metal lines 201 and pads 203 thus each are “interconnections.” *Id.*, ¶206.

The second substrate includes second ILDs. Pyo describes lines (201) and pads (203) as in an “insulating layer 202.” Pyo, 6, Fig. 3; Guidash, ¶207. POSAs would understand each level of the “insulating layer 202” is an ILD because each is “an insulating film between two conducting metals or adjacent metal lines.” Quirk, 14; Guidash, ¶¶93-94. The '366 patent uses “interlayer dielectric” consistently with its meaning in the art. For example, as seen in Figure 8 (below, original), ILD (130) electrically insulates the space between first and second metal interconnections (141 and 143) (i.e., adjacent metal lines). '366 patent, 2:32-44; Guidash, ¶94. Similarly, ILD (210) electrically insulates the space between metal lines (211 and 221). '366 patent, 3:10-14, Fig. 8; Guidash, ¶94.

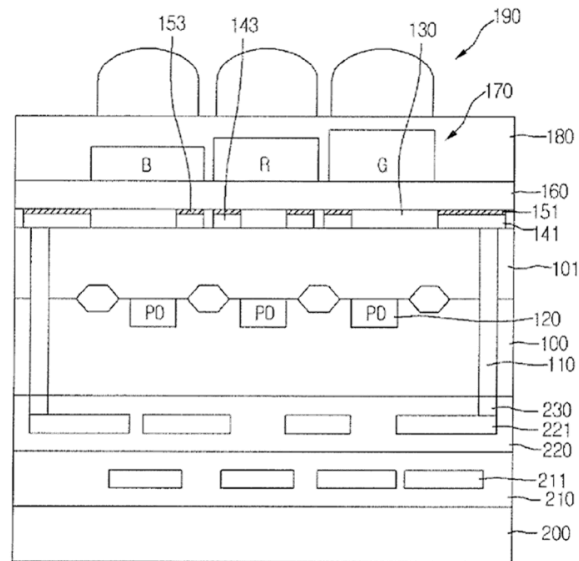
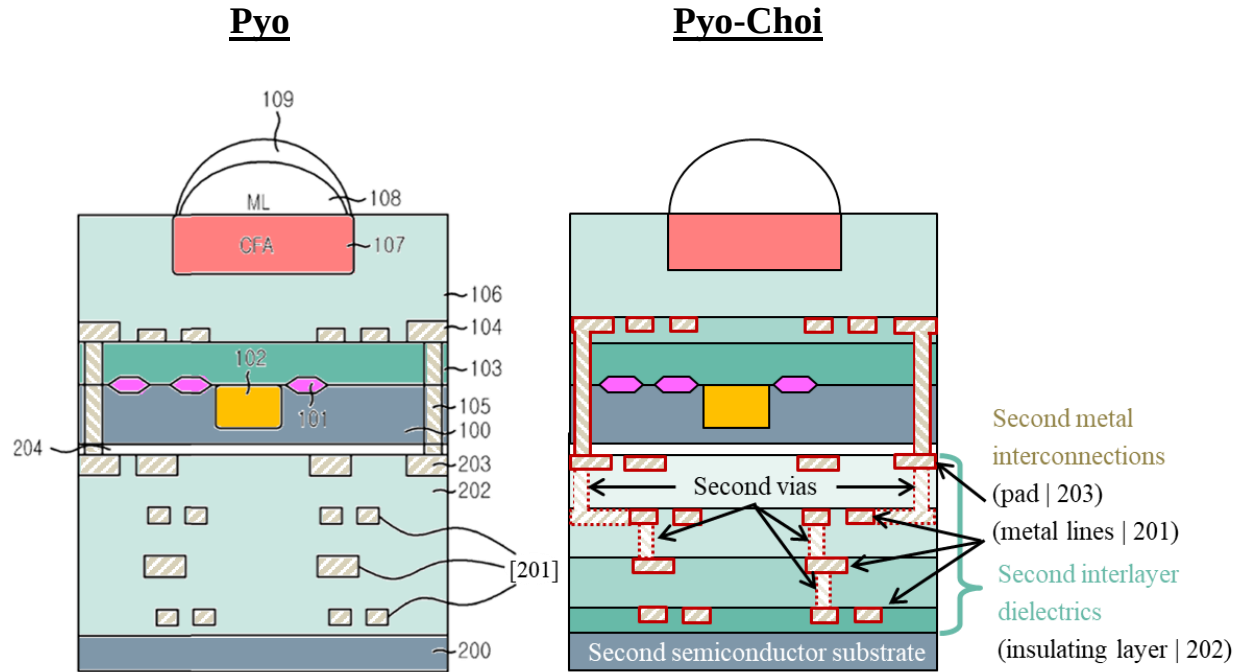


FIG. 8

Pyo's levels of "insulating layer 202" are thus ILDs within the ordinary meaning of that term, as confirmed by the '366 patent. Guidash, ¶207.

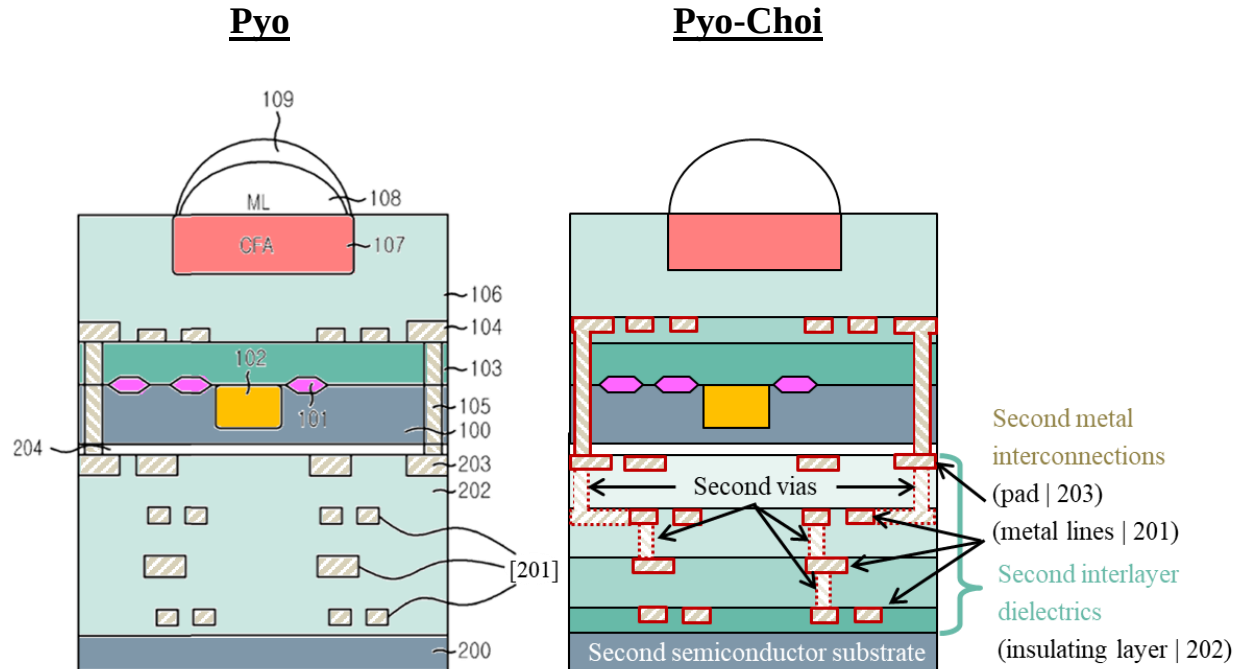
The modification of Pyo (i.e., using copper) would keep the above aspects of Pyo unchanged while incorporating metal barrier layers, not relevant to limitation [1.1]. *Id.*, ¶204.



iii. [1.2]

[1.2] a second via penetrating the second interlayer dielectric so that the second via is connected to the second metal interconnection;

The Pyo-Choi Sensor satisfies limitation [1.2] because Pyo’s logic chip has vias, each penetrating the insulating layer (202) to connect the pad (203) to the metal lines (201) or between layers of metal lines (201). Guidash, ¶208. Pyo discloses “pads 203 are **connected** to the plurality of metal lines 201” and the logic chip has “6-layer[s] [of] wiring or more.” Pyo, 4-5, Fig. 3; Guidash, ¶209. POSAs would have understood pads (203) and metal lines (201) are connected by one or more vias, which are interconnections to “form an electrical pathway” from one metal layer to another. Quirk, 54; Brase, 1:40-45; Guidash, ¶¶163-165.



The '366 patent uses “via” consistently with this meaning. For example, claim 1 specifies the first via connects the first metal interconnection to the second via, each on different levels. Claim 7 requires the “first via and the second via comprise the *same material*,” meaning the via is the conductor, not the “via hole.” '366 patent, 3:65-4:6; Guidash, ¶¶95-97. And the specification describes vias providing electrical connections between layers. '366 patent, Abstract (“first via being *electrically* connected to the second via”), 1:42-44 (similar), 2:65-3:4 (“first semiconductor substrate 100 and the second semiconductor substrate 200 can be *electrically* connected together”).

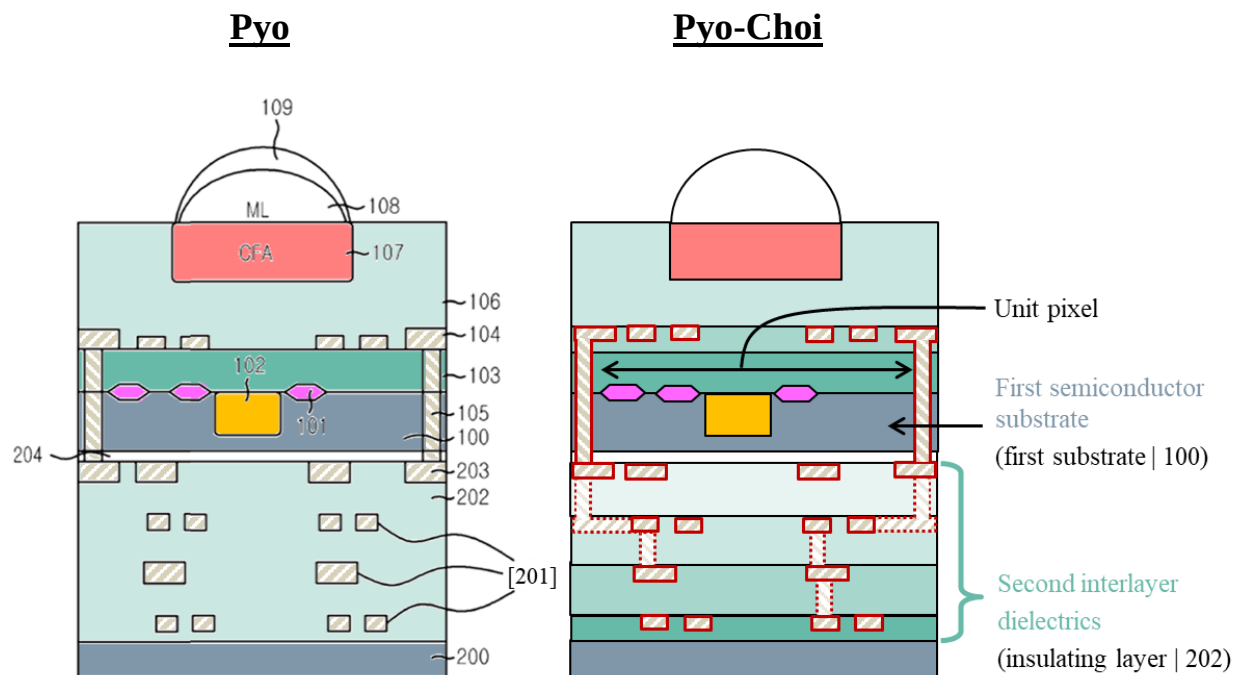
In Pyo’s logic chip, vias *penetrate* the insulating layer (202) (second ILD) to connect pads (203) to the first level of metal lines (201) or between the layers of

metal lines (201). Guidash, ¶211. The modification of Pyo would leave these aspects unchanged. *Id.*, ¶208.

iv. [1.3]

[1.3] a first semiconductor substrate on the second interlayer dielectric, the first semiconductor substrate having a unit pixel;

The Pyo-Choi Sensor satisfies limitation [1.3] because Pyo’s “image chip [is] disposed on a **first substrate**,” which POSAs would understand is a semiconductor because Pyo’s sensor is a “**semiconductor** device.” Pyo, 4; Guidash, ¶213. The substrate includes a unit pixel. Pyo, 5 (“plurality of transistors **constituting a unit pixel**,... are formed” “on the first substrate 100” and “transistor[s] **constitute[] the unit pixel**.”).



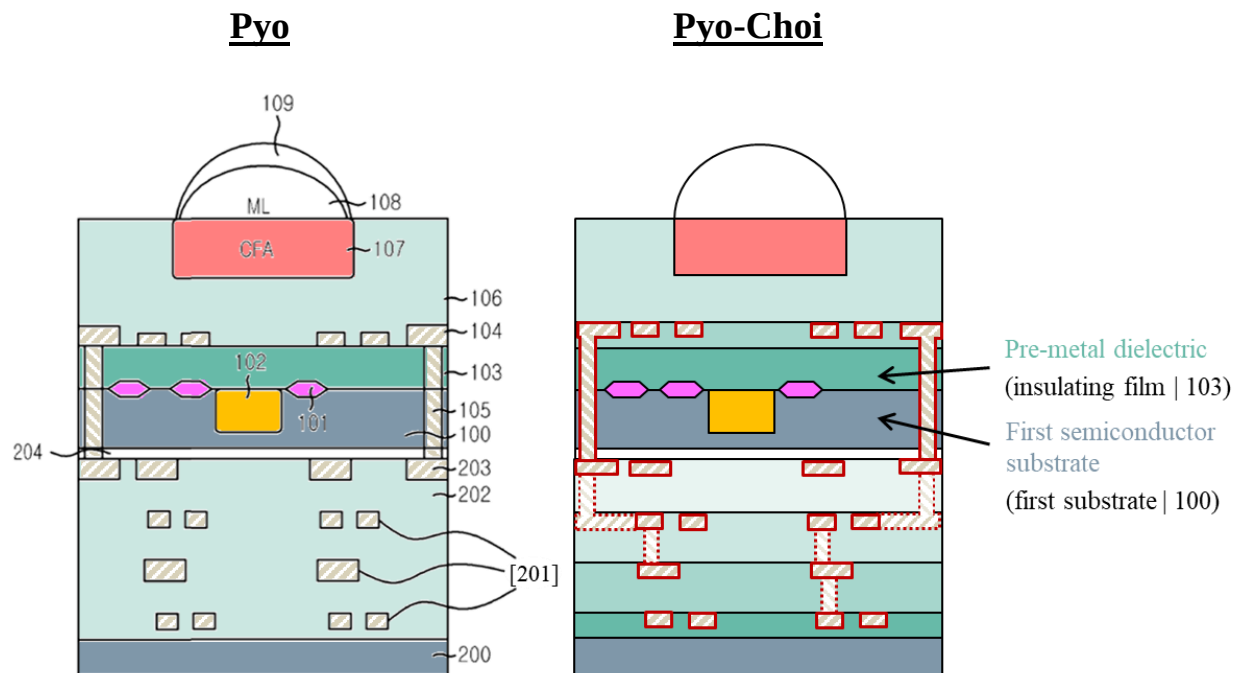
The first substrate is located “on” the second ILD within the meaning of “on” in the ’366 patent despite the intervening bonding layer (204). The ’366 patent explains one layer or structure is “on” another even if “intervening layers, regions, patterns, or structures” are also present. ’366 patent, 2:17-22; Guidash, ¶214.

The modification to Pyo would leave these aspects unchanged. *Id.*, ¶212.

v. [1.4]

[1.4] a pre-metal dielectric on the first semiconductor substrate;

The Pyo-Choi Sensor satisfies limitation [1.4] because Pyo discloses “an insulating film 103.” Pyo, 6, Fig. 3; Guidash, ¶217.



POSAs would understand insulating film 103 is a PMD because it is between active devices (i.e. photodiodes and unit pixel transistors) and metal lines 104,

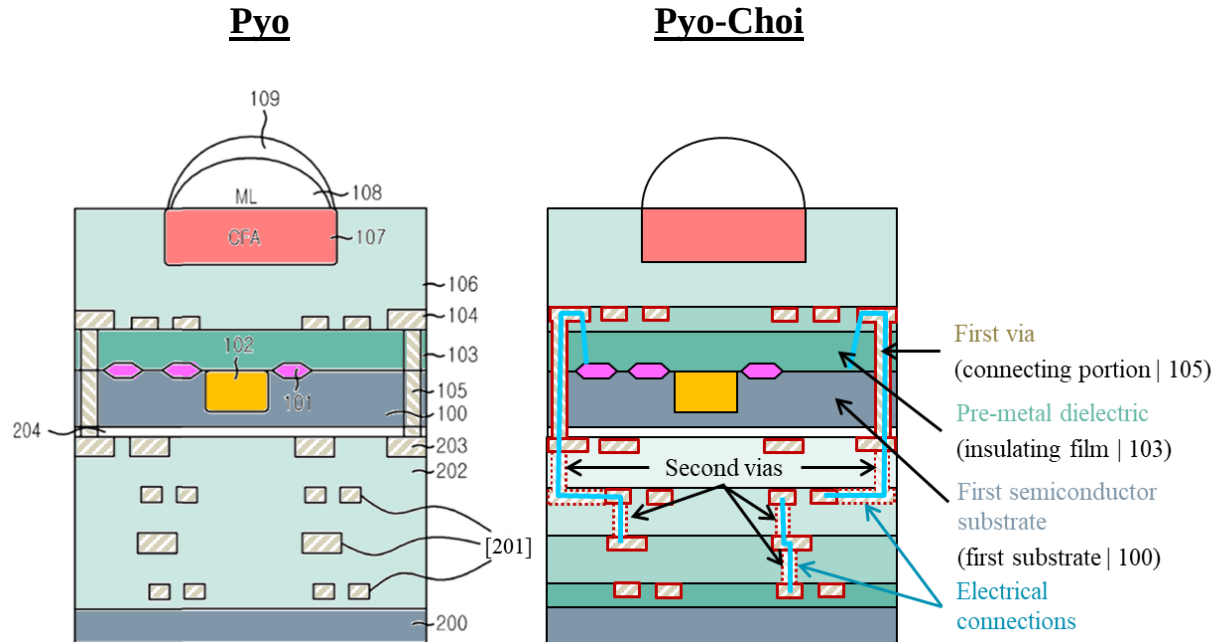
above. Guidash, ¶217. An insulating layer “between the active devices in silicon and the first metal layer ... is also called *the premetal dielectric (PMD)*.” Quirk, 13; Guidash, ¶¶101-102. The ’366 patent uses “pre-metal dielectric” consistently with its meaning in the art. For example, claim 1 requires a PMD located between the first semiconductor substrate (i.e., where the active devices are located) and the first metal interconnection. Guidash, ¶102.

Pyo’s PMD on the first semiconductor substrate would remain unchanged after modifications elsewhere in the sensor. *Id.*, ¶216.

vi. [1.5]

[1.5] a first via penetrating the pre-metal dielectric and the first semiconductor substrate, the first via being connected to the second via;

The Pyo-Choi Sensor satisfies limitation [1.5] because Pyo’s sensor has “a connecting portion 105 connected to metal line 104 through the rear surface of the first substrate 100” penetrating the insulating film (103) and first substrate (100). Pyo, 6, Fig. 3; Guidash, ¶219. POSAs would recognize portion 105 as a via because it electrically connects different layers. §VI.A.5.a.iii (meaning of “via”).



Specifically, Pyo discloses part 105 (first via) is electrically connected to the pad (203) and metal lines (201) (second metal interconnects) of the logic chip.

Guidash, ¶219, citing Pyo, 5 (“plurality of transistors are **connected** to the pads 203 ... through the connecting portion 105 ...”, and the pads 203 are **connected** to the plurality of metal lines 201.”), 6 (“105 needs to be **connected** to the logic chip,” “pad 203 must be **connected** to the connecting portion 105,” and “pad 203 [is] connected to the metal line[s] 201”). The above figure, right, illustrates these connections in blue. Guidash, ¶220.

POSAs would understand “connected” encompasses electrical connections as the ’366 patent itself discloses. Guidash, ¶221 (citing ’366 patent, Abstract (“the first via being **electrically connected** to the second via”), 1:42-44 (“first via ... to **electrically connect** with the second via”), 2:65-3:4 (similar)). And at least one

embodiment connects vias “using polymer,” meaning they would not physically touch—permitting **only** an electrical connection. ’366 patent, 7:5-8; Guidash, ¶221.

An interpretation excluding a preferred embodiment is rarely, if ever, correct.

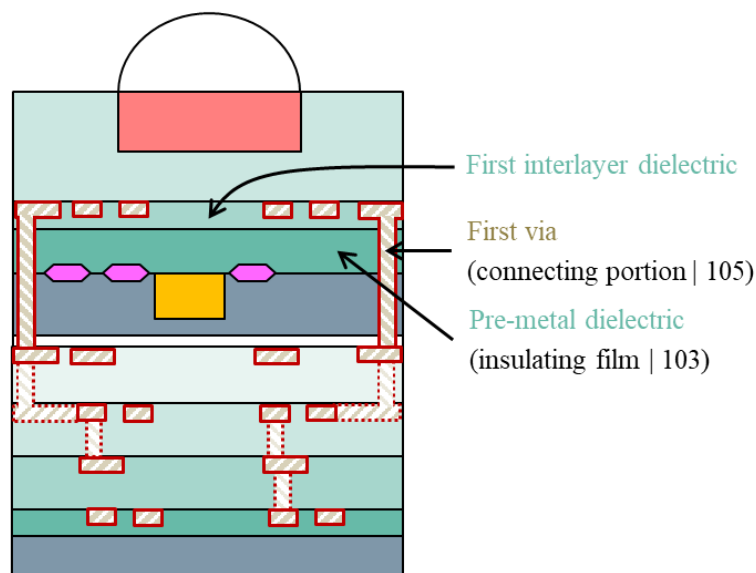
Vitronics. v. Conceptronic, 90 F.3d 1576, 1583 (Fed. Cir. 1996).

These aspects of Pyo would remain unchanged after the above-discussed modifications elsewhere in the sensor. Guidash, ¶218.

vii. [1.6]

[1.6] a first interlayer dielectric on the pre-metal dielectric including the first via;

The Pyo-Choi Sensor satisfies limitation [1.6] because it has a ILD on the PMD including the first via as a result of the above-discussed dual-damascene process for incorporating copper-based interconnections. §VI.A.3.b; Guidash, ¶¶222-224.

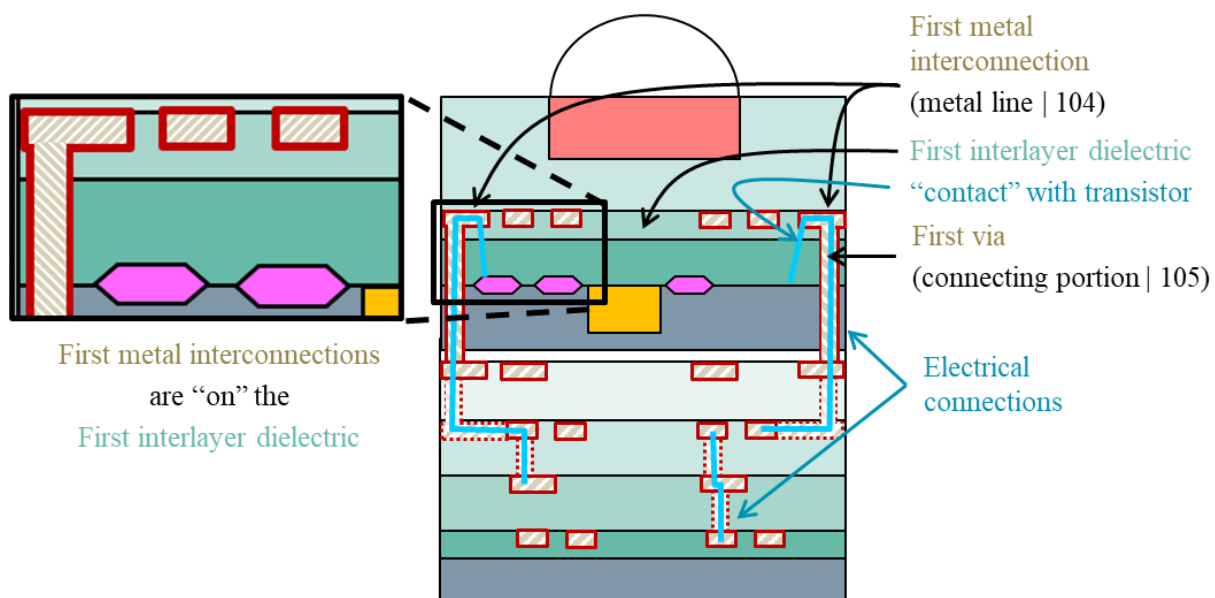


Pyo even discloses using “an inter-metal dielectric (IMD).” Pyo, 4 (“the metal line process ... using an “IMD (Inter-Metal Dielectric)””), 6. POSAs would understand inter-metal dielectrics are ILDs because they insulate two adjacent lines. §VI.A.5.a.ii (meaning of ILD).

viii. [1.7]

[1.7] a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel;

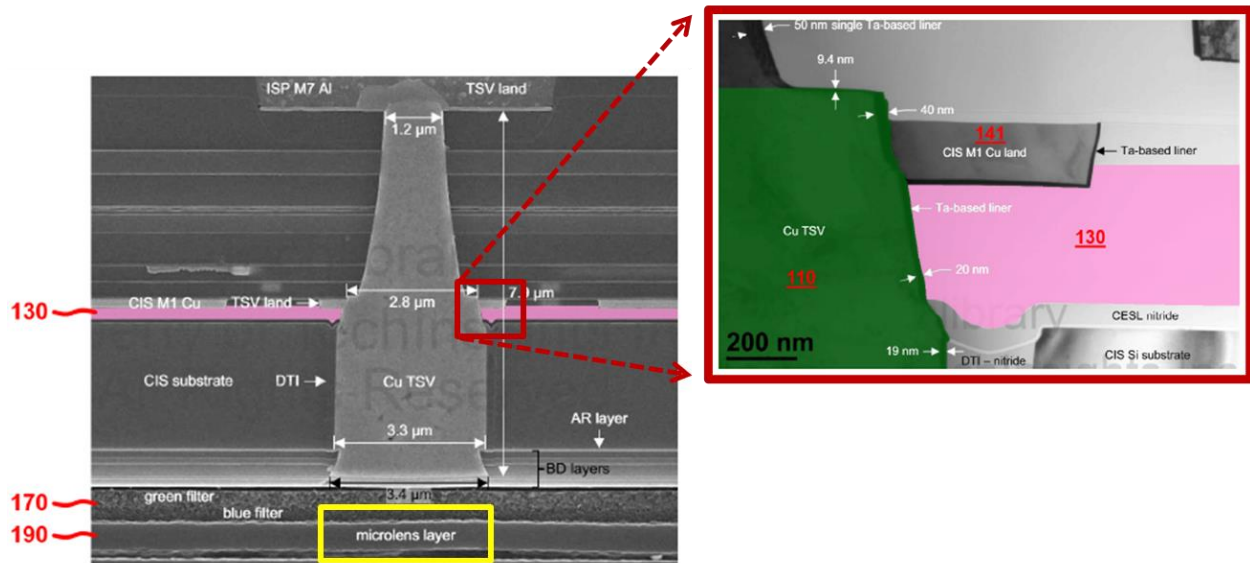
The Pyo-Choi Sensor satisfies limitation [1.7] because it has a first metal interconnection on the first ILD (as shown below) given the above-discussed dual-damascene process for incorporating copper-based interconnections. §VI.A.3.b; Guidash, ¶¶225-226.



Pyo describes “[r]eference number ‘104’” as “a metal line.” Pyo, 5. POSAs would understand “metal line 104” is a metal interconnection because it is “for **interconnecting** the transistor constituting the unit pixel and the lower portion metal line 201,” that it “is **connected** to the pad 203 through the connecting portion 105,” and is also “**connected** to the gate electrode or source/drain of the transistor through a contact.” *Id.*, 5-6; §VI.A.5.a.ii (meaning of “interconnection”); Guidash, ¶¶91-92. These connections are shown in blue, above. Guidash, ¶227.

While the “dual-damascene process became the consensus process for copper metallurgy” (Quirk, 80), even if a single-damascene process were used instead, where no portion of the metal interconnections (104) would be above the ILD (as shown in Figure 3 of Pyo), the Pyo-Choi Sensor would still satisfy limitation [1.7] under Patent Owner’s construction of “on.” Guidash, ¶231.

In the co-pending Texas Litigation, Patent Owner depicts an accused product with the microlens layer at the bottom of the image (below). Ex. 1021, 35-36.

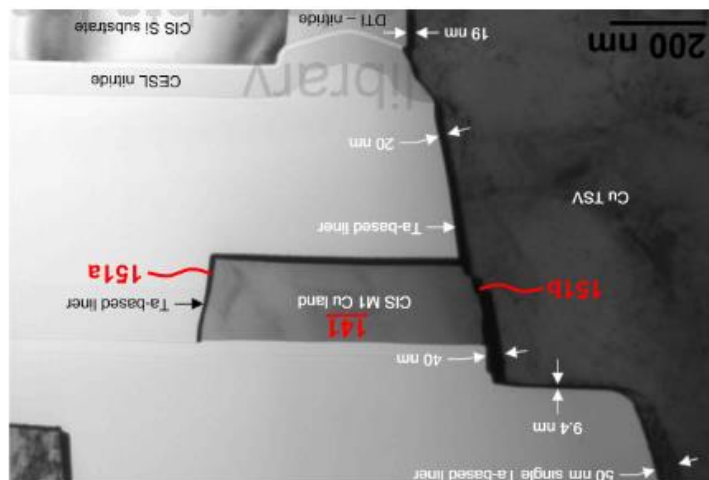


Re-orienting the images 180-degrees matches the orientation of Figure 8 of the '366 patent (microlens up). Guidash, ¶¶87-88.

Patent Owner alleges interconnection 141 is “on” alleged ILD 130 even though interconnection 141 is partly *adjacent to* and partly *below* the first ILD but *not above* any part of it. Ex. 1021, 35 (below, re-orientated to match that of Figure 8 of the '366 patent); Guidash, ¶88.

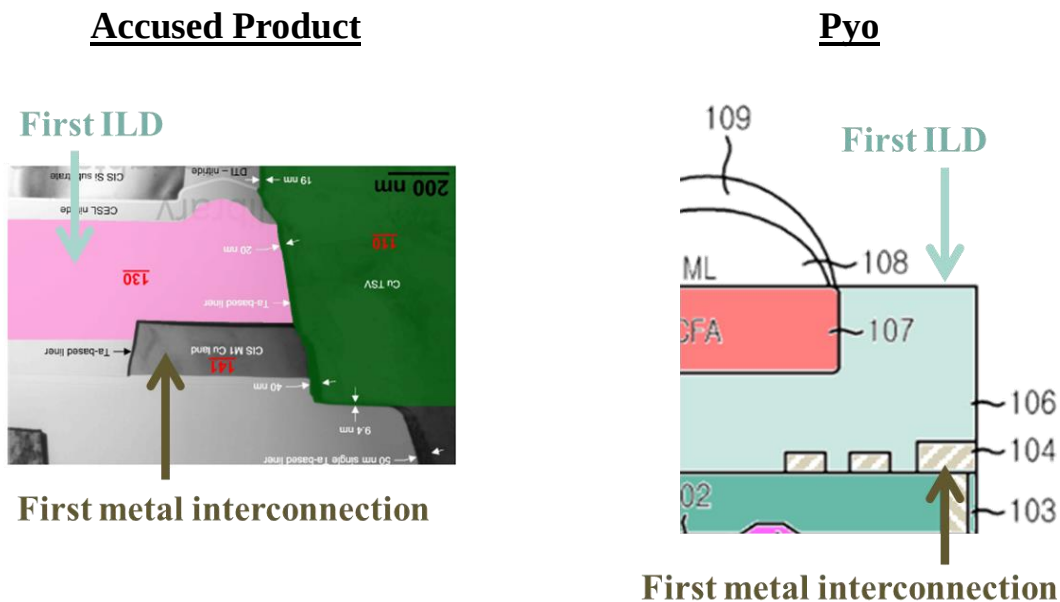


Likewise, as to limitation [1.8] Patent Owner alleges barrier layer (151a and 151b) is above, and thus “on” the alleged interconnection (141). *Id.*, 36 (below, re-orientated to match that of Figure 8 of the ’366 patent); Guidash, ¶89.



While Petitioner reserves its rights to challenge Patent Owner’s interpretation of “on,” for the purposes of this Petition only, it is assumed an element is “on” a corresponding element when the element is above, adjacent to, or below the corresponding element. *10X Genomics v. Bio-Rad Lab ’ys.*, IPR2020-00086, Paper 8, 19-20 (PTAB Apr. 27, 2020) (instituting review, citing 35 U.S.C. §301(a)(2): “[W]e see no problem with Petitioner relying on statements by Patent Owner in the related district court action in which Patent Owner took a position on the scope of a challenged claim....”); *Western Digital, v. SPEX Techs.*, IPR2018-00084, Paper 14, 11 (PTAB Apr. 25, 2018) (instituting review: “37 C.F.R. §104(b)(3) does not require Petitioner to express its subjective agreement regarding correctness of its proffered claim constructions.”).

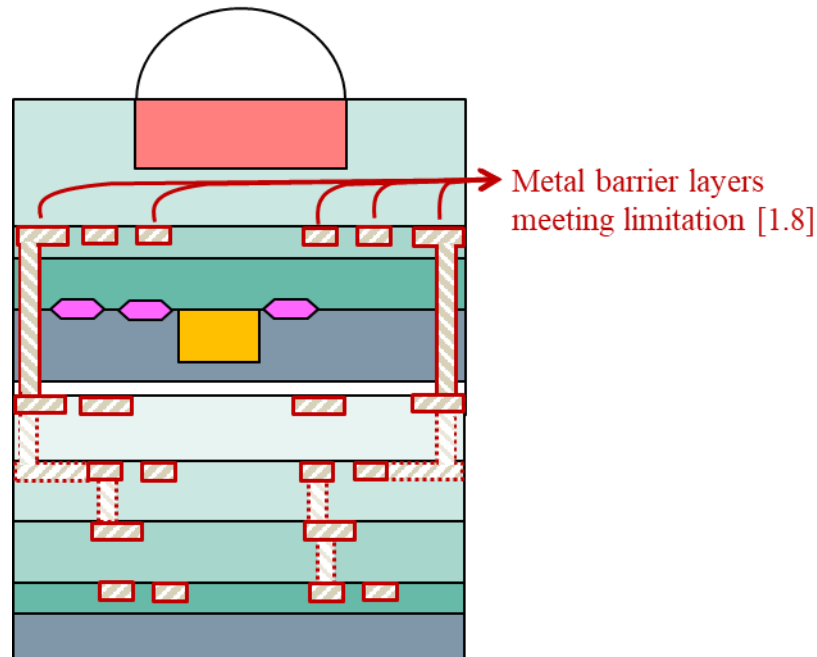
The Pyo-Choi Sensor's first metal interconnections are “on” the first ILD because Pyo discloses its wires 104 are at least adjacent to dielectric 106 pursuant to Patent Owner's claim construction, and that would remain the same even after modification. Guidash, ¶231.



ix. [1.8]

[1.8] a conductive barrier layer on the first metal interconnection; and

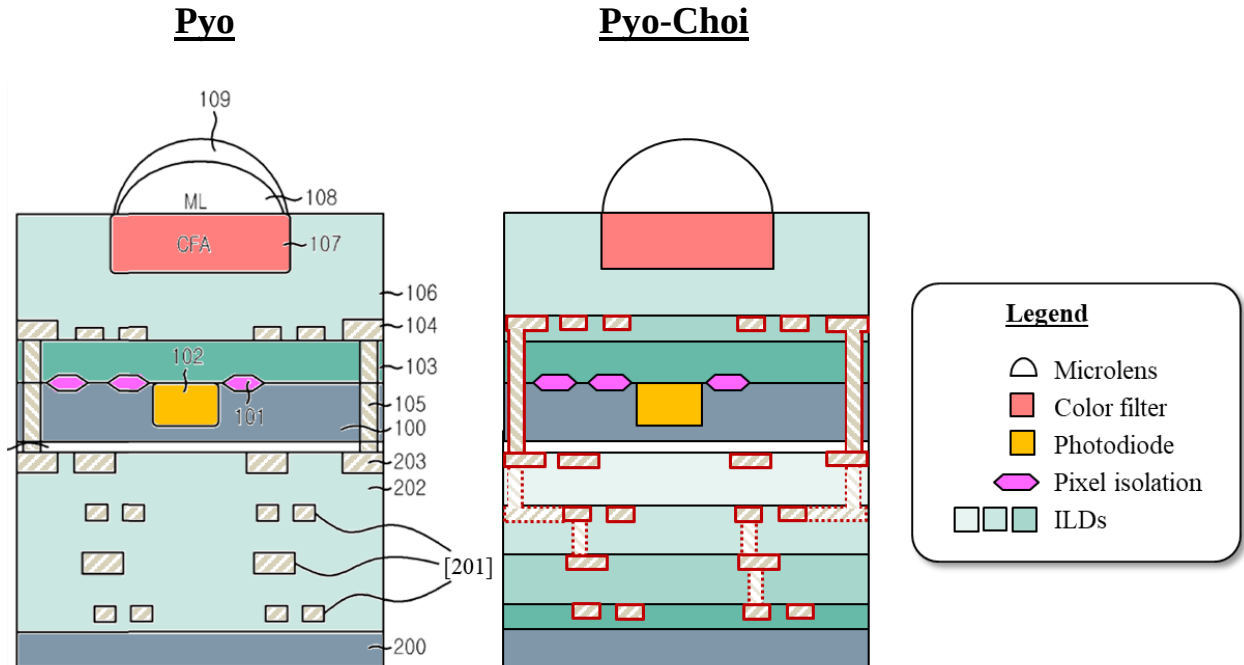
The Pyo-Choi Sensor satisfies limitation [1.8] because POSAs following Choi would have encapsulated the copper interconnections with a conductive metal barrier layer (shown below) as a result of the above-discussed dual-damascene process for incorporating copper-based interconnections. §VI.A.3.b, referencing VII.A.3.a.i.(5); Guidash, ¶¶193. The top metal barrier layer is “on” the first metal interconnection. Guidash, ¶232.



x. [1.9]

[1.9] a color filter and a microlens on the first interlayer dielectric on the unit pixel.

The Pyo-Choi Sensor satisfies limitation [1.9] because Pyo's sensor has "a color filter array and a microlens." Pyo, 4, 5 (noting "color filter array 107" and "microlens 108" in Figure 3). The color filter array and microlens are "on" the first ILD and unit pixel despite "intervening layers." '366 patent, 2:17-22. These aspects of Pyo would remain unchanged after the above-discussed modifications elsewhere in the sensor. Guidash, ¶233.



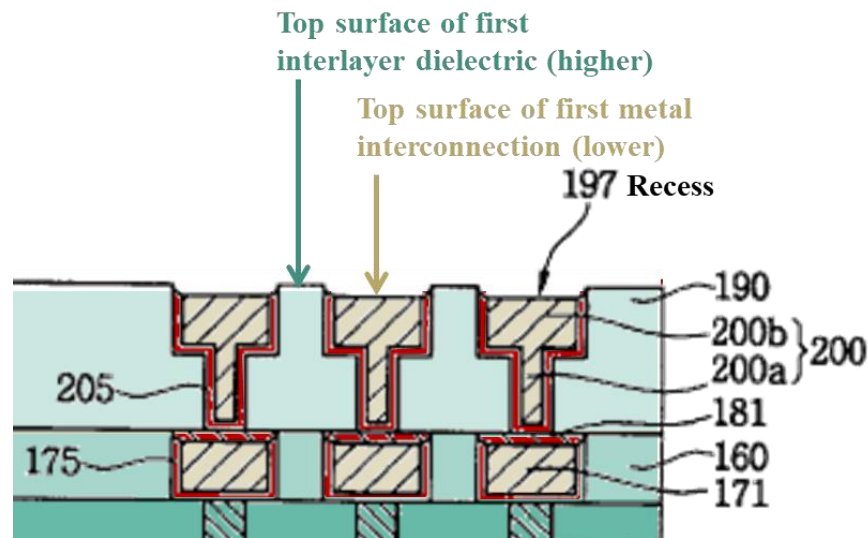
b. Claim 2

The Pyo-Choi Sensor satisfies claim 2’s additional limitation that the first metal interconnection is copper because POSAs would have selected copper for interconnections in implementing Pyo’s design. §VI.A.2 (motivation to use copper); §VI.A.3.b (fabrication of copper interconnections); Guidash, ¶235. Claim 2 is thus unpatentable as obvious.

c. Claim 4

The Pyo-Choi Sensor satisfies claim 4’s additional limitation that the first metal interconnection has a top surface lower than that of the first ILD, such that there is a “height difference” between the two, because Choi discloses creating a recess on the copper for a top barrier layer—a commonplace practice per the above-discussed dual-damascene process, and one that would have been obvious

when implementing copper interconnections in Pyo's sensor with Choi's processes. §VI.A.3.a.i.(4) (CMP creating a recess); §VI.A.3.b (fabricating image chip, cross referencing the earlier Section); Choi, [0128]-[0129], Figs. 5E, 5F (excerpted, below), and 5G; Guidash, ¶¶236-237. Claim 4 is thus unpatentable as obvious.

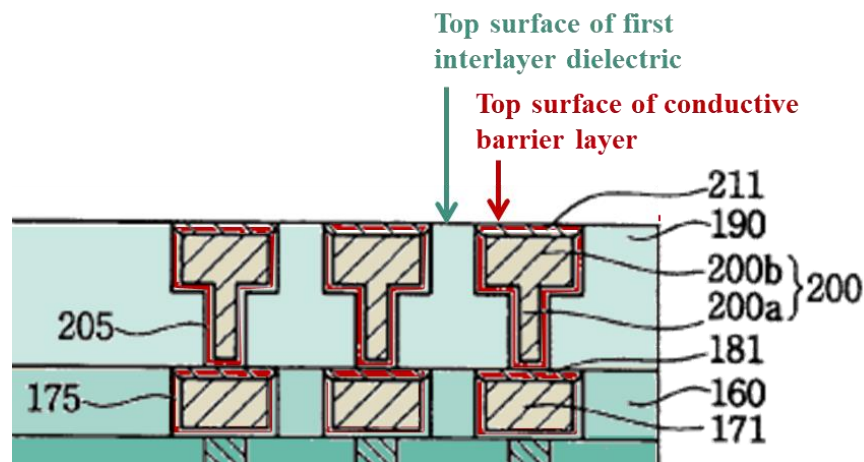


d. Claim 5

The Pyo-Choi Sensor satisfies claim 5's additional limitation that the second metal interconnection comprises copper or aluminum because Pyo describes "metal line 201" (the second metal interconnection) as "formed using copper or aluminum." Pyo, 5. POSAs would have used copper interconnections for the Pyo-Choi Sensor. §VI.A.2 (motivation to use copper); Guidash, ¶238. Claim 5 is thus unpatentable as obvious.

e. Claim 6

The Pyo-Choi Sensor satisfies claim 6's additional limitation that the conductive barrier layer has at top surface substantially even with the top surface of the first ILD because Choi discloses depositing a barrier layer in a recess above the copper interconnections and planarizing such that the top surface of the barrier layer is even with the top surface of the first ILD—a commonplace practice per the above-discussed dual damascene process, and one that would have been obvious when implementing copper interconnections in Pyo's sensor with Choi's processes. §VI.A.3.a.i.(6) (planarizing); §VI.A.3.b (fabricating image chip, cross referencing those earlier Sections); Choi, [0129] (referencing back to [0122]-[0123]), Fig. 5G (excepted, below); Guidash, ¶¶239-240. Claim 6 is thus unpatentable as obvious.



f. Claim 7

The Pyo-Choi Sensor satisfies claim 7's additional limitation that the first via and the second via comprise the same material because POSAs would have modified Pyo's sensor to use copper vias. §VI.A.2 (motivation to use copper); §VI.A.3.a.ii (using copper for vias in logic chip); §VI.A.3.b (using copper for vias in image chip); Guidash, ¶241. Claim 7 is thus unpatentable as obvious.

g. Claim 8

The Pyo-Choi Sensor satisfies claim 8's additional limitation that the second semiconductor substrate provides metal interconnections for connection to a power line and an external signal line because POSAs would have desired to make the Pyo-Choi Sensor operational by connecting it to power and external signal lines. Guidash, ¶242; Edelstein, 10 (requiring "DC power distribution, [and] off-chip I/O"); Imaoka, [0049] (requiring a "power supply terminal" and an "input/output terminal"); Choi, [0005] ("A complementary MOS image sensor (CIS) converts an optical image into an electrical signal."). POSAs would have been motivated to locate these interconnections on the "logic chip" to improve sensor performance. Guidash, ¶243; Pyo, 5 ("by removing the ... plurality of metal lines 201 and an insulating film 202 [from the image chip], it is possible to maximize photosensitivity"). Claim 8 is thus unpatentable as obvious.

B. GROUND 2: Pyo in view of Choi and Dublin Renders Claim 3 Obvious

Claim 3 depends from claim 1 and further requires cobalt (Co) or nickel (Ni) alloy for the conductive barrier layer. Dublin disclosed a cobalt tungsten phosphide (CoWP) alloy as preferred for a conductive barrier layer for copper interconnections. Claim 3 would therefore have been obvious over Pyo in view of Choi (as previously discussed concerning claim 1) and further in view of Dublin.

1. Reasons to Use CoWP Barrier Layer

POSAs would have been motivated to combine Pyo and Choi to obtain the Pyo-Choi Sensor. §VI.A.2; §VI.A.3.

POSAs would have been further motivated to use Dublin's CoWP as the barrier material in lieu of options disclosed in Choi because Dublin acknowledges Choi's options,¹² but discloses CoWP was "preferred" over them because it "significantly enhances the barrier properties." Dublin, 3:1-7. CoWP alloy allows for "increased thermal stability, improved corrosion resistance and mechanical properties (such as wear resistance)." *Id*, 5:17-23. POSAs would thus have been motivated to use CoWP. Guidash, ¶¶248.

¹² Compare Dublin, 2:25-57 (disclosing Ta, W, TaN, and WN as copper barrier materials) with Choi, [0066] and [0071] (same); Guidash, ¶248.

Moreover, Dublin discloses CoWP can be selectively deposited on copper, eliminating need for Choi's final planarizing step (§VI.A.3.i.(6)). Guidash, ¶249; Dublin, 8:66-9:3; Choi, [0122]-[0123], [0129]. Using CoWP would thus simplify manufacturing. Guidash, ¶249; Quirk, 82 ("Reducing process steps in wafer fabrication is important for improving the yield.").

Finally, using CoW would have been nothing more than simple substitution. *KSR*, 550 U.S. at 416 ("combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results."). Dublin discloses CoWP for barrier layers in damascene processes, achieving the same function as barrier materials disclosed in Choi. Dublin, 8:1-65; Guidash, ¶250. POSAs could thus readily replace Choi's barrier materials. Guidash, ¶250. Using CoWP instead would have been simple substitution. *Agrizap v. Woodstream*, 520 F.3d 1337, 1344 (Fed. Cir. 2008); *Daikin Indus. v. Chemours*, 846 F. App'x 907, 911-12 (Fed. Cir. 2021) (affirming Board's reliance on "substitution" theory given evidence that new chemical had improved properties). Gambino shows such substitution worked. Gambino, 25.

2. Resulting Sensor and Reasonable Expectation of Success

The resulting sensor would be structurally identical to the Pyo-Choi Sensor of Ground 1 except the barrier layer would comprise CoWP. Guidash, ¶251.

POSAs would have had a reasonable expectation of successfully making such a sensor for the same reasons as discussed in §VI.A.4, and because CoWP is compatible with the damascene process like Choi's. *Compare* §VI.A.3 with Dublin, 8:1-65; Guidash, ¶252. Indeed, Gambino successfully used CoWP in place of silicon nitride in a CMOS sensor. Gambino, 25.

3. Claim 3 Analysis

The resulting sensor includes a conductive metal barrier layer comprising a cobalt (Co) alloy (i.e., CoWP), thereby fulfilling claim 3's additional element and rendering the claim obvious. Guidash, ¶253; Dublin, 2:63-66, 3:53-55.

C. GROUND 3: Imaoka Anticipates Claims 1-2 and 4-8

Imaoka's sensor meets every element of claims 1-2 and 4-8 under Patent Owner's claim interpretations in the Texas Litigation, anticipating those claims. Guidash, ¶254.

1. Claim 1

a. [1.pre]

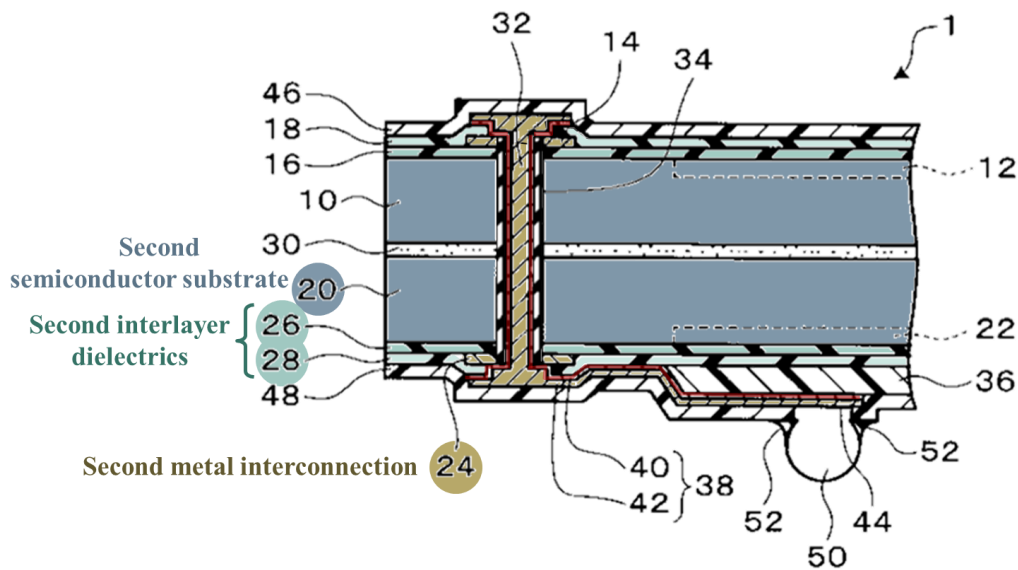
[1.pre] An image sensor, comprising:

To the extent the preamble is limiting, Imaoka's device is an image sensor. Imaoka, [0006] ("In this optical device, ... [the] light-receiving elements may be arrayed for *image sensing*."), [0011] ("the optical device may be an *image sensor* (for example, ... a CMOS *image sensor*)"); Guidash, ¶255.

b. [1.1]

[1.1] a second semiconductor substrate including a second metal interconnection and a second interlayer dielectric;

Imaoka includes “second semiconductor substrate 20” with “pad 24” and “passivation films 26 and 28.” Imaoka, [0010], Fig. 3 (below).



POSAs would understand pad 24 is a metal interconnection because it is “aluminum” or “a copper type of metal.” Imaoka, [0009], [0010] (noting “contents of the second semiconductor substrate 20 may be the same as the above-mentioned first semiconductor substrate 10”). Pad 24 connects with electrical connection 44 and pad 14, through part 38. *Id.*, [0018] (“[C]onductive part 38 is electrically connected to at least one (both in Fig. 3) of the first and the second pad 14 and 24.”), [0019] (“electrical connection part 44 may ... overlap the second pad 24”);

Guidash, ¶257. POSAs would have thus understood pad 24 is an interconnection. §VI.A.5.a.ii (meaning of “interconnection”); Guidash, ¶257.

POSAs would understand passivation films 26 and 28 are insulators because pads 24 are in direct contact with films 26 and 28 (Imaoka, Figures 2, 3); if the films were not insulators, there would be a short circuit. Guidash, ¶258. Moreover, films 26 and 28 are made from “SiO₂, SiN, [and] a polyimide resin” (*id.*, [0009], [0010]), each an insulator. Guidash, ¶258. POSAs would understand films 26 and 28 are ILDs because each insulates pads 24 from one another. §VI.A.5.a.ii (meaning of ILD); Guidash, ¶258.

c. [1.2]

[1.2] a second via penetrating the second interlayer dielectric so that the second via is connected to the second metal interconnection;

While Imaoka discloses only a single part 38 to connect the first and second substrates, in the co-pending Texas Litigation, Patent Owner asserts that a single thru-silicon via (“TSV”) satisfies both the claimed first **and** second vias. Ex. 1021, ¶¶64-66, Fig. 6 (below). Patent Owner asserts claims 1, 2 and 4-8 are infringed by “**any** back-illuminated and stacked CMOS image sensors utilizing TSVs.” Ex. 1027, 3.

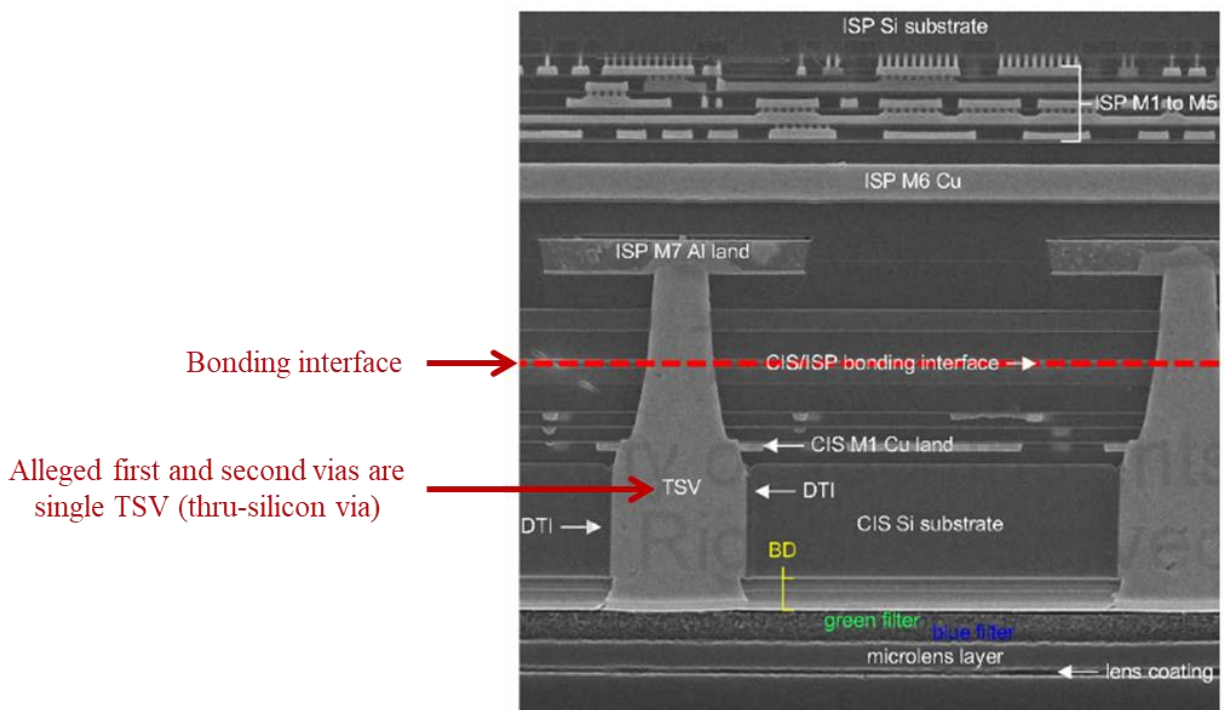
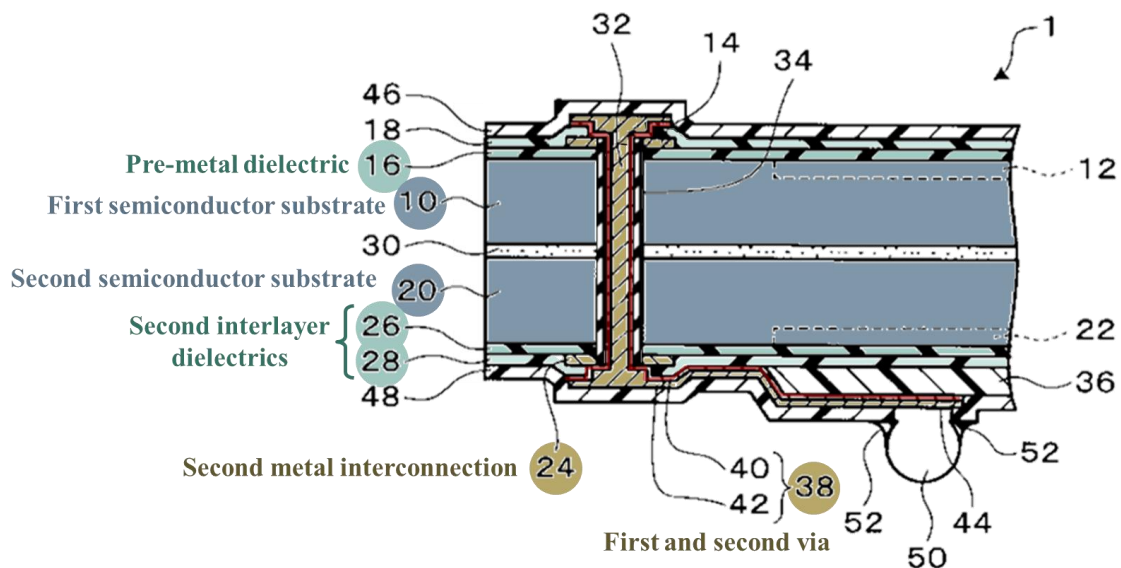


Figure 6

While Petitioner reserves its rights to challenge that construction, for the purposes of this Petition only, it is assumed that a single via may meet both first and second vias if it otherwise meets the claimed requirements. *10X Genomics* at 19-20; *Western Digital* at 11. Under Patent Owner’s interpretation, part 38 satisfies every claimed requirement of the first and second vias. Guidash, ¶261.

Part 38 satisfies limitation [1.2] because it penetrates the second ILDs (26 and 28) (below figures) and is “electrically connected to at least one (both in Fig. 3) of the first and the second pad 14 and 24” (first and second interconnections). Imaoka, [0018]-[0020], Fig. 3; Guidash, ¶261; §VI.A.5.vi (an *electrical* connection meets the “connected” requirement). Guidash, ¶261.

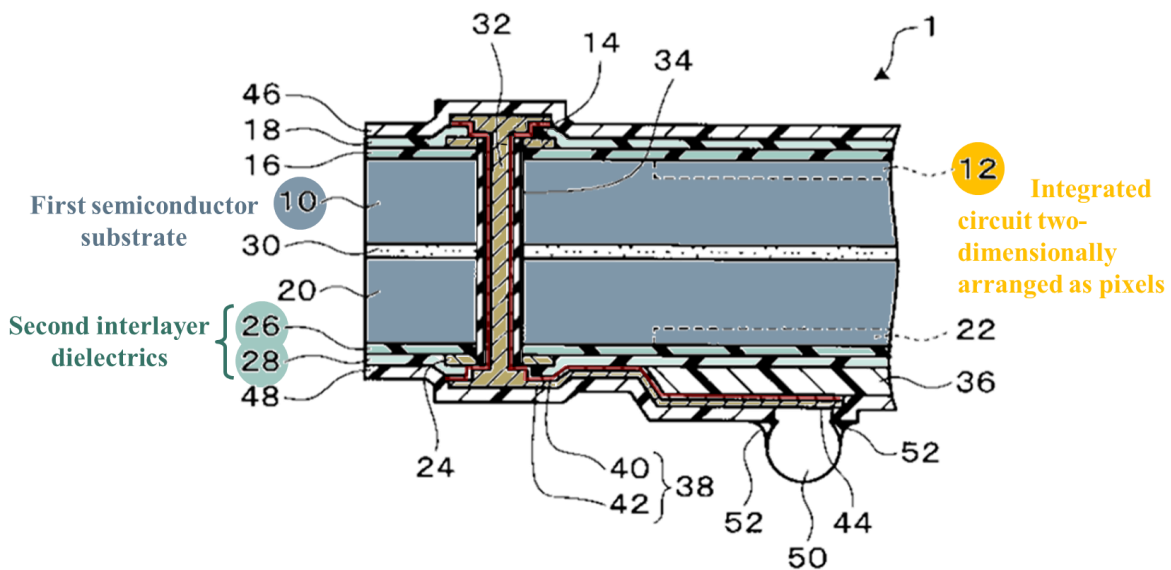
Part 38 satisfies limitation [1.5], which requires it “penetrating the pre-metal dielectric and the first semiconductor substrate, the first via being connected to the second via,” because it penetrates the PMD (16) and first substrate (10) and is “connected” to the second via because it is a single structure. Guidash, ¶261; Imaoka, [0018]-[0020], Fig. 3. Part 38 also performs the functions of the first and second vias because it forms an electrical pathway from the first metal interconnection to the second metal interconnection. Guidash, ¶261; Imaoka, [0018]-[0020]; Fig. 3. And POSAs would understand part 38 is a via because it forms an electrical pathway from one metal layer to another. §VI.A.5.a.iii (meaning of “via”); Guidash, ¶261.



d. [1.3]

[1.3] a first semiconductor substrate on the second interlayer dielectric, the first semiconductor substrate having a unit pixel;

Imaoka's first and second substrates (10 and 20) are "bonded to each other" (Imaoka, [0015]) with first substrate (10) located above the second ILDs (films 26 and 28) (Figure 3 (below)), making it "on" the second ILDs notwithstanding intervening layers ('366 patent, 2:17-22). Guidash, ¶262.

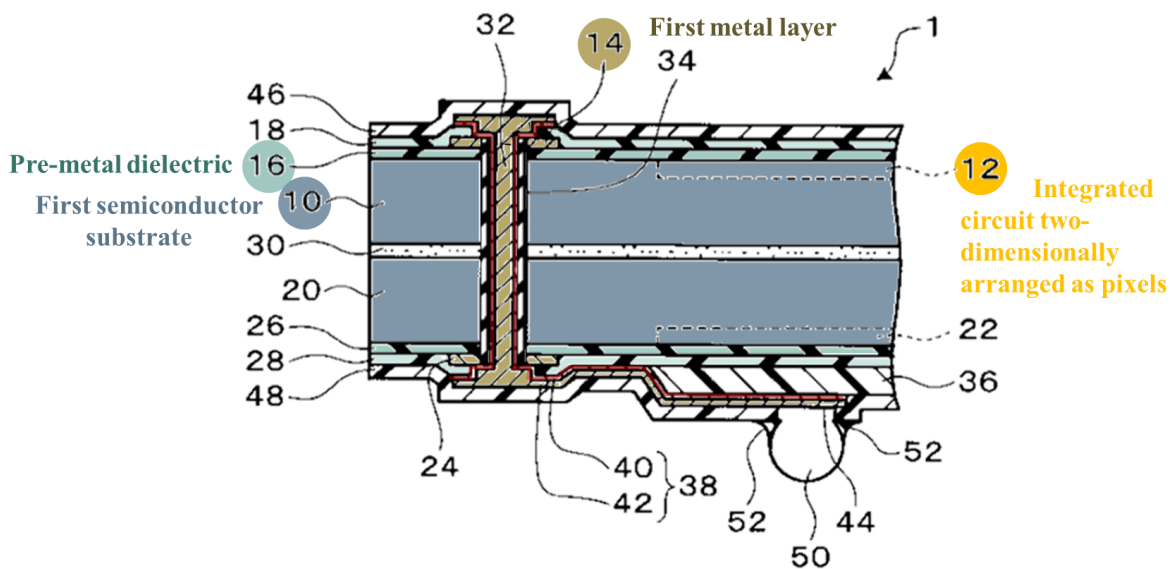


And first substrate (10) has a unit pixel (12). Imaoka, [0011], [0052] ("the first semiconductor substrate 10 has an optical part 13," "the optical part 13 has at least one energy converter," and the "energy converter ... is a part of the first integrated circuit 12" and corresponds to "a plurality of *pixels* two-dimensionally arrayed."); Guidash, ¶263.

e. [1.4]

[1.4] a pre-metal dielectric on the first semiconductor substrate;

Imaoka has “passivation film[] 16 ... **on** the first semiconductor substrate 10.” Imaoka, [0009], Fig. 3 (below); Guidash, ¶264. POSAs would understand film 16 is a PMD because it insulates adjacent pads to prevent electrical shorts (*id.*, Figs. 2 and 3), is made from insulators (*id.*, [0009] (“SiO₂, SiN, [and] a polyimide resin”)), and is located between active devices in substrate 12 and first metal layer 14. §VI.A.5.a.v (meaning of PMD); Guidash, ¶264.



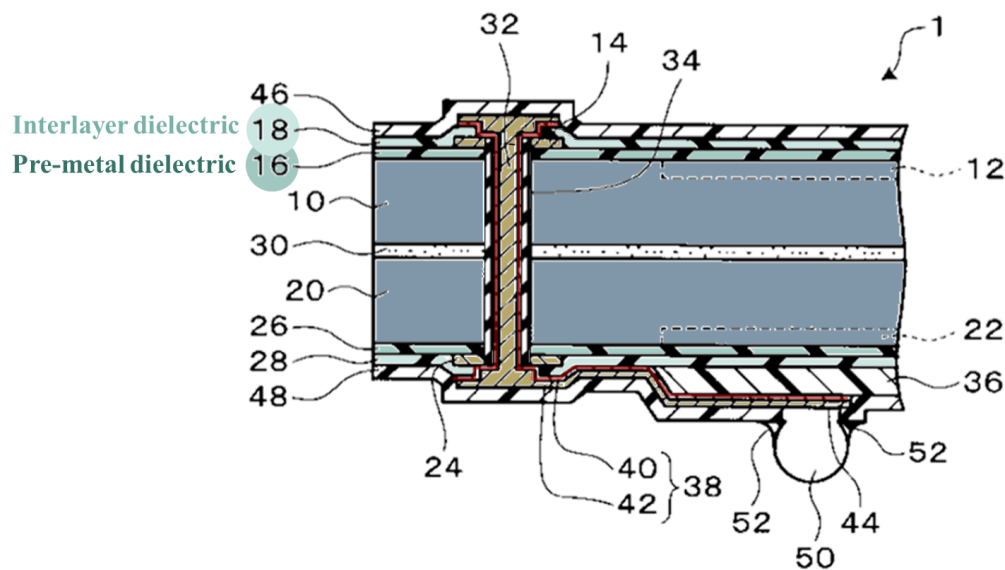
f. [1.5]

Imaoka’s “part 38” meets the requirements of both first and second vias.
§VI.C.1.c.

g. [1.6]

[1.6] a first interlayer dielectric on the pre-metal dielectric including the first via;

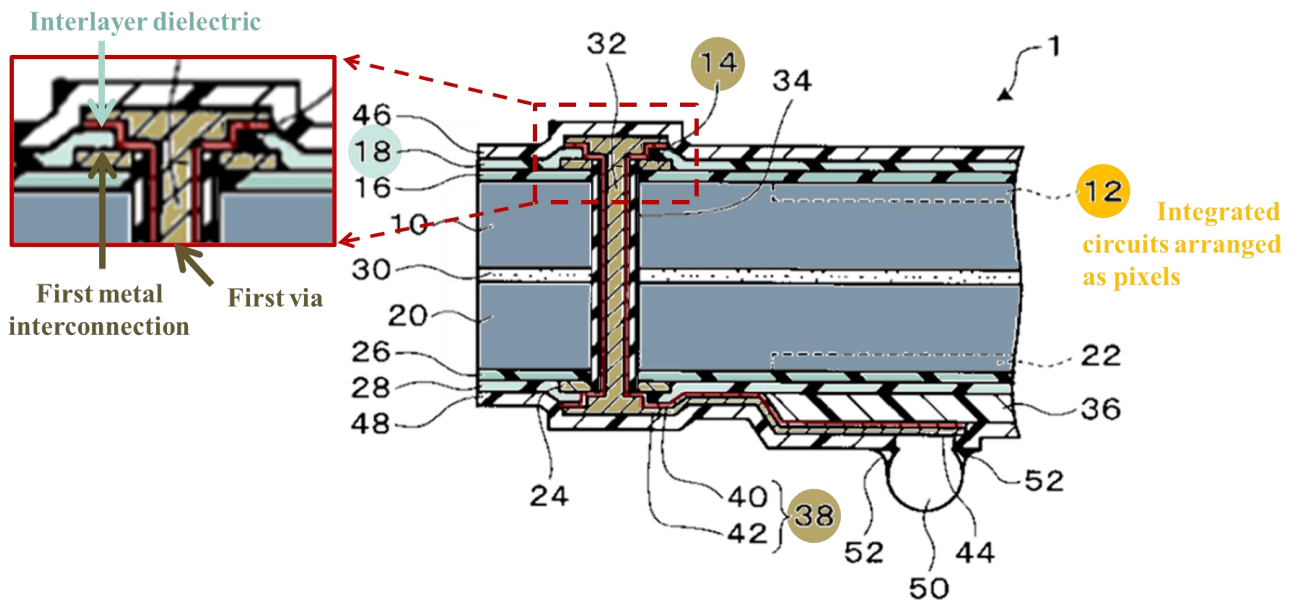
Imaoka has “passivation films 16 and **18** ... *on* the first semiconductor substrate 10.” Imaoka, [0009], Fig. 3 (below); Guidash, ¶266. POSAs would understand film 18 is an ILD because it insulates adjacent pads (14) to prevent electrical shorts (*id.*, Figs. 2-3) and is made from insulators (*id.*, [0009] (“SiO₂, SiN, [and] a polyimide resin”)). §VI.A.5.a.ii (meaning of ILD); Guidash, ¶266.



h. [1.7]

[1.7] a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel;

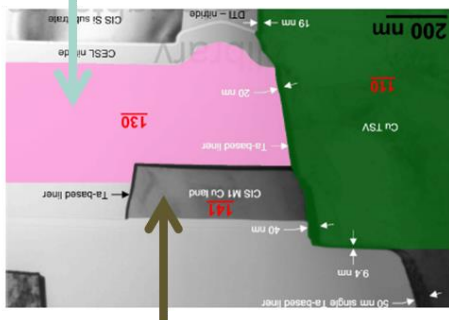
POSAs would understand Imaoka's pads (14) are metal interconnections because they are "aluminum" or "a copper type of metal" that are electrically connected to first and second vias (part 38) (Imaoka, [0018]) and "to the first semiconductor circuit" (12) (*id.*, [0009]), which contains the unit pixel (*id.*, [0011]). Guidash, ¶267; §VI.A.5.a.ii (meaning of "interconnection").



Pads (14) would be "on" ILD (18) under Patent Owner's claim construction in the co-pending Texas Litigation. See §VI.A.5.viii (according to Patent Owner, an element is "on" a corresponding element when the element is above, adjacent to, or below the corresponding element). Imaoka's pads 14 are "on" ILD 18 because they are below and adjacent to dielectric 18 pursuant to Patent Owner's claim construction. Guidash, ¶269.

Accused Product

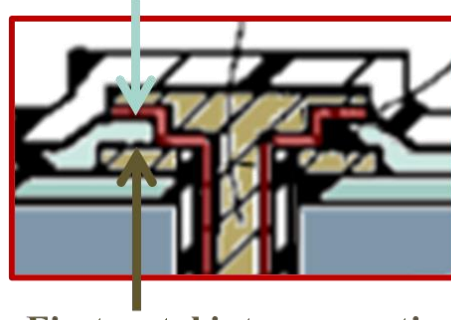
First ILD



First metal interconnection

Imaoka

First ILD

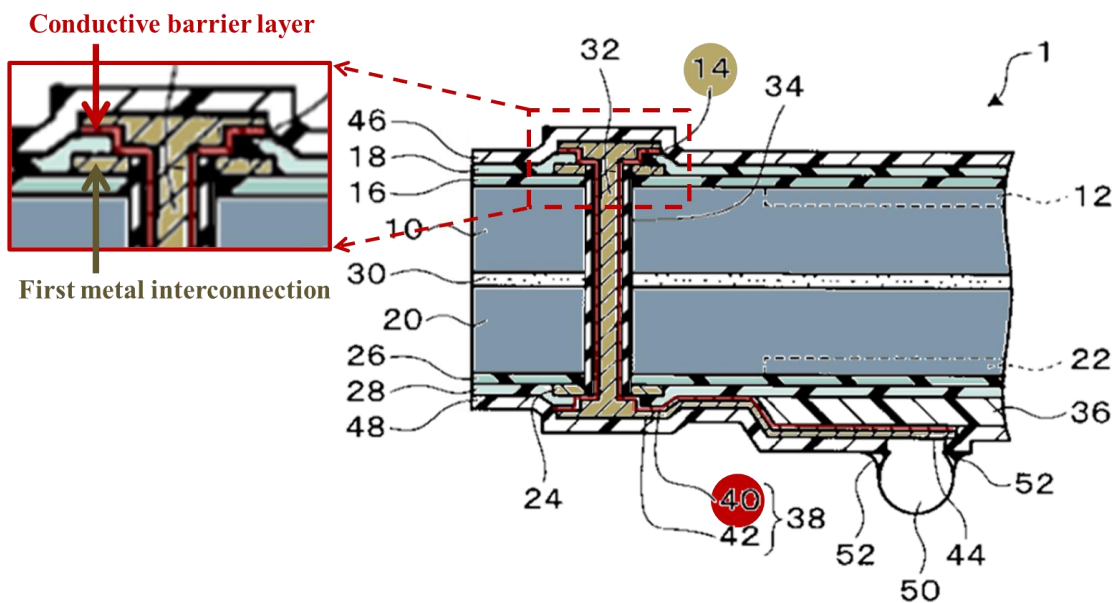


First metal interconnection

i. [1.8]

[1.8] a conductive barrier layer on the first metal interconnection; and

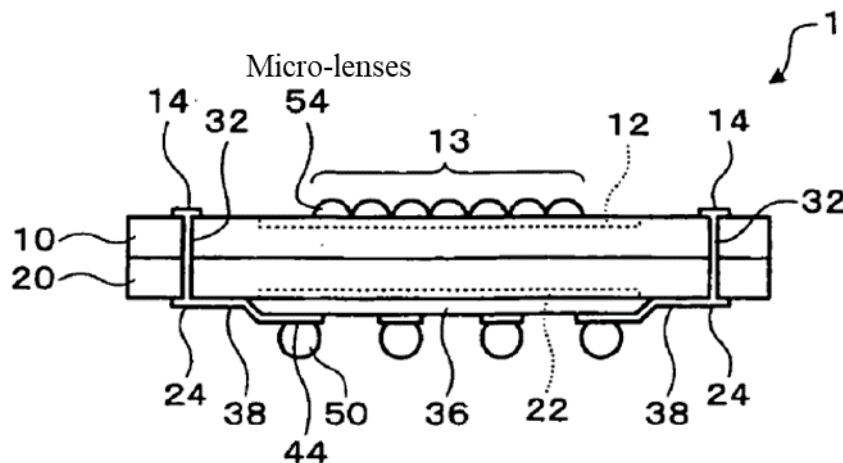
Imaoka has “a first **conductive** layer 40” that “may at least include a **barrier layer**,” which according to Figure 3 is disposed partly above (i.e. “on”) pad 14 (i.e. the “first metal interconnection”). Imaoka, [0041], Fig. 3; Guidash, ¶270.



j. [1.9]

[1.9] a color filter and a microlens on the first interlayer dielectric on the unit pixel.

Imaoka discloses “optical part 13” with a “*color filter (not illustrated)*,” “formed between the micro-lenses 54 and the light-receiving elements.” Imaoka, [0013], Fig. 1; Guidash, ¶271. “[O]ptical part 13 may be equipped with a plurality of *micro-lenses 54*” “corresponding to each of the plurality of the light-receiving elements,” “placed on the side of the surface on which the first integrated circuit 12 on the first semiconductor substrate 10 is formed.” Imaoka, [0012]-[0013], Fig. 1 (below); Guidash, ¶272.



2. Claim 2

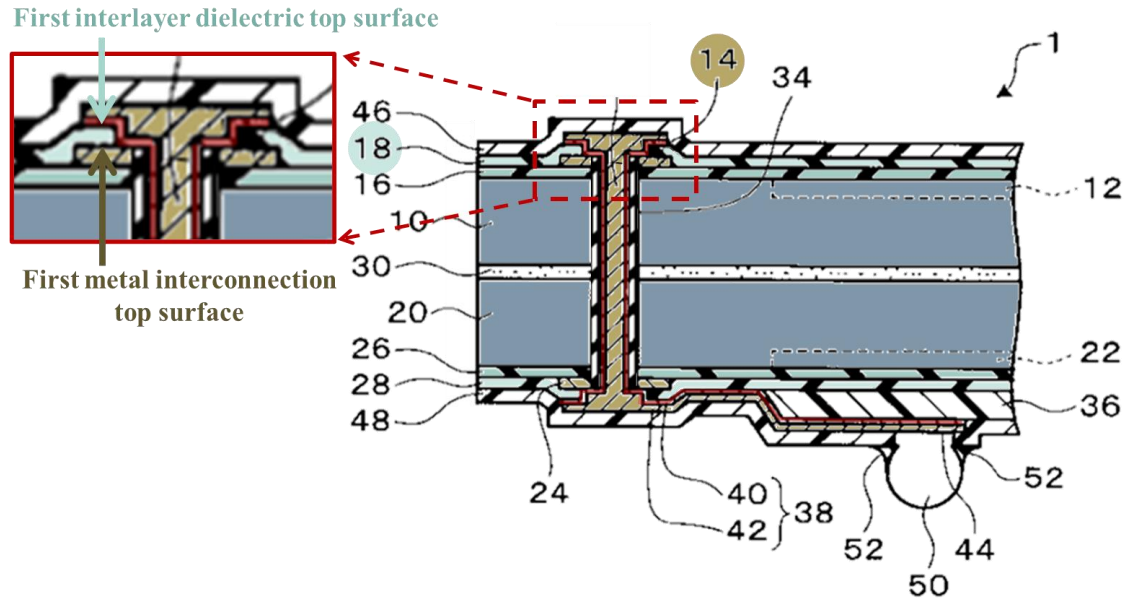
Imaoka satisfies claim 2’s additional limitation of the first metal interconnection being copper because pads 14 are formed from “an aluminum type

or ***a copper type of metal.***”¹³ Imaoka, [0009]. Thus, one embodiment has copper pads. Guidash, ¶273; *Kennametal v. Ingersoll Cutting Tool*, 780 F.3d 1376, 1382–83 (Fed. Cir. 2015) (number of prior art combinations was not so large that each “would not be immediately apparent to [POSAs]”).

3. Claim 4

Imaoka satisfies claim 4’s additional limitation that the first metal interconnection has a top surface lower than that of the first ILD, such that there is a “height difference” between the two because Figure 3 shows the claimed height difference. Imaoka, Fig. 3; Guidash, ¶274.

¹³ U.S. Patent Publication No. 2004/0245649 (“’649 Pub.”) claims priority to Imaoka. Ex. 1022, face. While the ’649 Pub. discloses pads 14 may be “steel type of metal” (*id.*, [0050]), POSAs would understand that as an error because steel is not used for interconnections in semiconductors. Guidash, ¶273.



4. Claim 5

Imaoka satisfies claim 5's additional limitation that the second metal interconnection comprises copper or aluminum because Imaoka discloses its pads may be "aluminum" or "copper." Imaoka, [0009], [0010] (structures on the second substrate "may be the same as" the first); Guidash, ¶275.

5. Claim 6

Imaoka satisfies claim 6's additional limitation that the conductive barrier layer has at top surface "substantially even" with the top surface of the first ILD because Figure 3 shows the barrier layer (40) having top surface "substantially even" with the top surface of the first ILD (18). Imaoka, Fig. 3; Guidash, ¶276.

external connections for the circuit's power and external signal line. Guidash, ¶278. POSAs would thus understand from Imaoka's disclosure that the "external terminal 50" are metal interconnections for connection to a power line and an external signal line that is part of the second substrate. Guidash, ¶278.

D. GROUND 4: Imaoka in view of Dublin Renders Claim 3 Obvious

1. Reasons to Use CoWP Barrier Layer

Claim 3 depends from claim 1 and further requires cobalt (Co) or nickel (Ni) alloy for the conductive barrier layer. POSAs would have used CoWP (an alloy having cobalt) as Imaoka's conductive barrier layer because Imaoka does not disclose the material for its barrier layer and CoWP had better performance than other known materials. §VI.B.1; Guidash, ¶¶280-282.

2. Resulting Sensor and Reasonable Expectation of Success

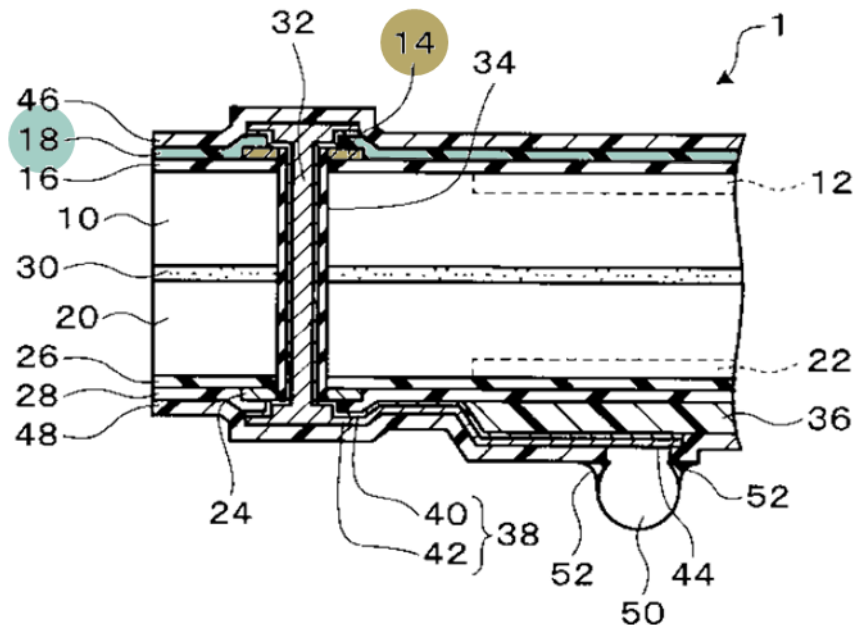
The resulting sensor would be identical to Imaoka's except using CoWP as the conductive barrier material. Guidash, ¶283. POSAs would have had a reasonable expectation of successfully using CoWP as a barrier material because Imaoka discloses its part 38 is made of copper (Imaoka, [0041]) and Dublin discloses CoWP is for copper interconnections in semiconductor devices. Dublin, 2:63-3:7; Guidash, ¶284. Moreover, Gambino successfully used CoWP in place of silicon nitride as a copper interconnection barrier layer in a CMOS sensor. Gambino, 25.

3. Claim 3 Analysis

The resulting sensor includes a conductive metal barrier layer comprising a cobalt (Co) alloy (i.e., CoWP), thereby fulfilling the additional element of claim 3 and rendering the claim obvious. Guidash, ¶285; Dublin, 2:63-66, 3:53-556.

E. GROUND 5: Imaoka in view of Choi Renders Claims 1-2 and 4-8 Obvious

Imaoka's pads 14 are formed from "an aluminum type or *a copper type of metal.*" Imaoka, [0009]. Nevertheless, POSAs would infer the sensor in Imaoka's Figures 1-4 uses aluminum rather than copper for pad 14 because film 18 overcoats pad 14; a copper structure would instead normally be disposed within film 18. Guidash, ¶286; Imaoka, Fig. 3 (below).



However, POSAs would have had reason to fabricate Imaoka's sensor using copper rather than aluminum, and in particular would have had reason to use

Choi's damascene process for such fabrication. The resultant sensor would satisfy all elements of claims 1-2 and 4-8 even if interpreting "on" more narrowly than Patent Owner's suggestion in the Texas Litigation.

1. Reasons to Pick Copper for Pad 14

POSAs would have had reason to pick copper instead of aluminum for pad 14 given its lower resistivity, reduced power consumption, resistance to electromigration, and tighter packing density. §VI.A.2. In addition, because Imaoka discloses part 38 can be copper (Imaoka, [0041]), POSAs implementing Imaoka's Figures 1-4 would naturally also select copper for pad 14 to fill both the vias and the interconnections in a single step—reducing the number of processing steps. §VI.A.2.c; Guidash, ¶288. Fewer processing steps lead to higher yields. §VI.A.2.c. As Imaoka does not disclose a structure specific to copper pads, POSAs would have consulted references such as Choi. Guidash, ¶289; Quirk, 80; Pratt, 8-10; Doering, 4.

POSAs would have also had reason to make pad 24 and electrical connection part 44 out of copper for the same reasons as for pad 14. However, for purposes of the analysis herein, it is immaterial whether POSAs would have taken that additional step, which would have required removing or modifying Imaoka's resin layer (36) to apply Choi's copper interconnection process and in particular Choi's planarization step. Guidash, ¶290.

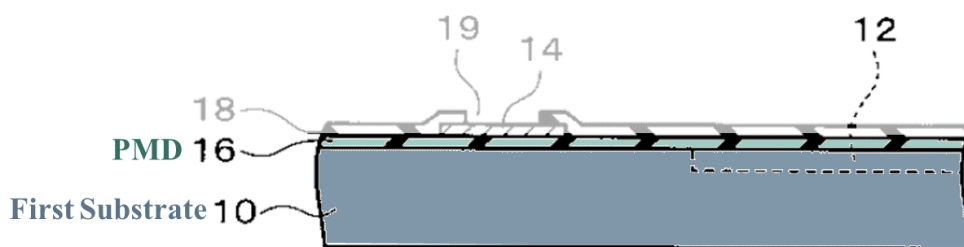
2. Resulting Imaoka-Choi Sensor

Imaoka discloses stacking the semiconductor substrates (Imaoka, [0034]-[0035]) prior to fabricating the interconnections (*id.*, [0036]-[0044]), but POSAs would have understood a straightforward way of fabricating pads 14 from copper without altering the structure of the second substrate would be to fabricate the interconnections on the two substrates first, then bond them together thereafter. Guidash, ¶292; Pyo, 4 (disclosing separately fabricating image and logic chips before bonding them together); Iwabuchi, [0095]-[0096], Figs. 34A-34B (similar).

Using this approach, POSAs would have fabricated the interconnections on the second substrate as disclosed by Imaoka (*see* [0036]-[0044]), fabricated the interconnections on the first substrate and bonded together the first and second substrates as described below. Guidash, ¶¶293-295.

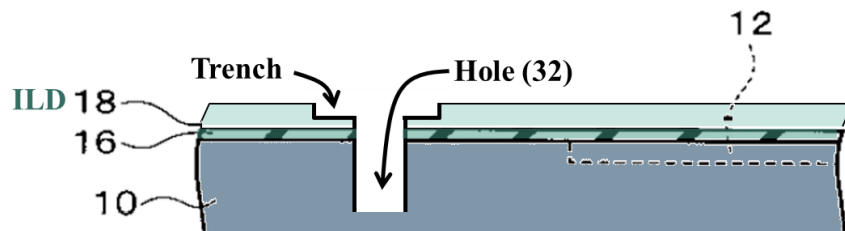
a. Deposit PMD

POSAs would have first deposited passivation film 16. Imaoka, [0036], Fig. 5(A) (below). Passivation film 16 is a PMDs because it insulates the active devices (12) from the first metal layer. Guidash, ¶296; Quirk, 13.



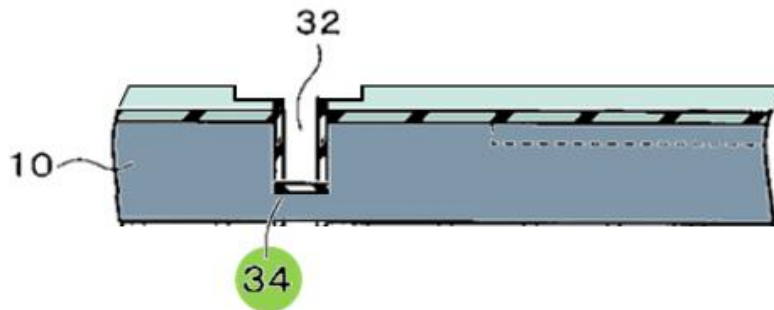
b. Deposit ILD and Pattern

POSAs would have next deposited an ILD layer and etched it to form trenches for pad 14 and a hole (32) for part 38. §VI.A.3.a.i.(1); Imaoka, [0036]-[0037] (using a “YAG laser, a CO₂ laser, an excimer laser and the like” to form the hole), Fig. 5B (below, modified); Guidash, ¶297.



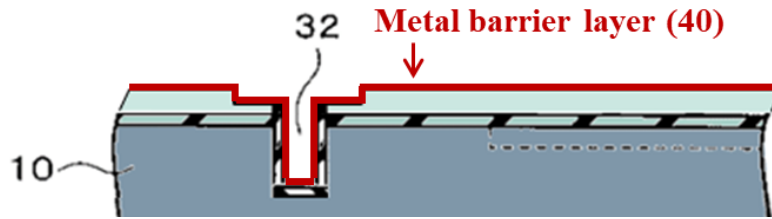
c. Insulating Layer

POSAs would have next fabricated an “insulating layer 34” inside the hole. Imaoka, [0038], Fig. 5C (below, modified); Guidash, ¶298.



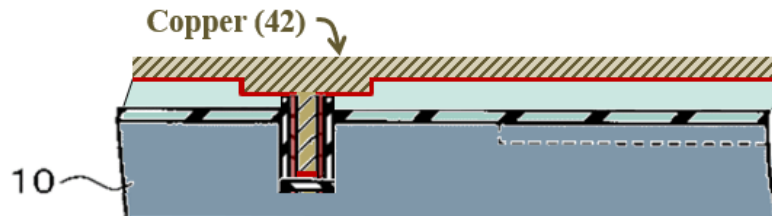
d. Metal Barrier Layer

POSAs would have next deposited a metal barrier layer. §VI.A.3.a.i.(2); Imaoka, [0041] (a “barrier layer may be formed ... (for example, TiW or TiN)”), Fig. 6(B) (below, modified); Guidash, ¶299.



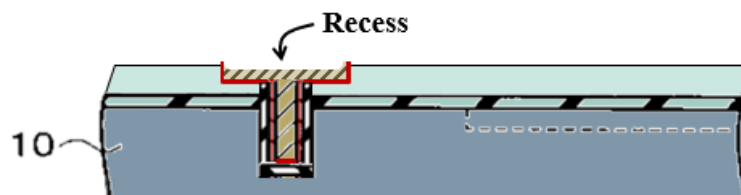
e. Copper Deposition

POSAs would have deposited a “seed layer” (Imaoka, [0041]) and deposited copper (§VI.A.3.a.i.(3); Imaoka, [0041]-[0042], Figure 6(C) (below, modified)). Guidash, ¶300.



f. CMP

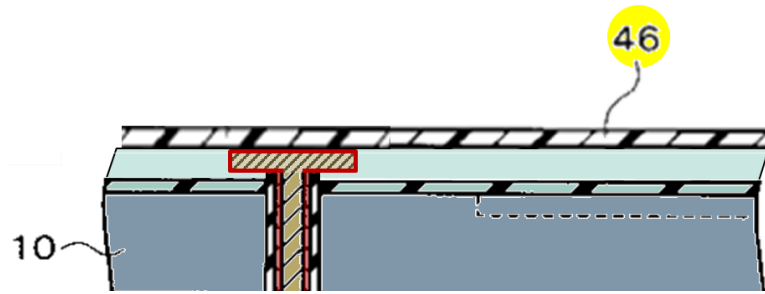
POSAs would next perform CMP to create a recess above the interconnection, below. §VI.A.3.a.i.(4), citing Yun, 13 (“excessive polishing is performed so that the copper layer 313 and the third barrier layer 312 filled in the upper trench are recessed”), Fig. 3i; Guidash, ¶301.



g. Top Metal Barrier Layer; Planarization

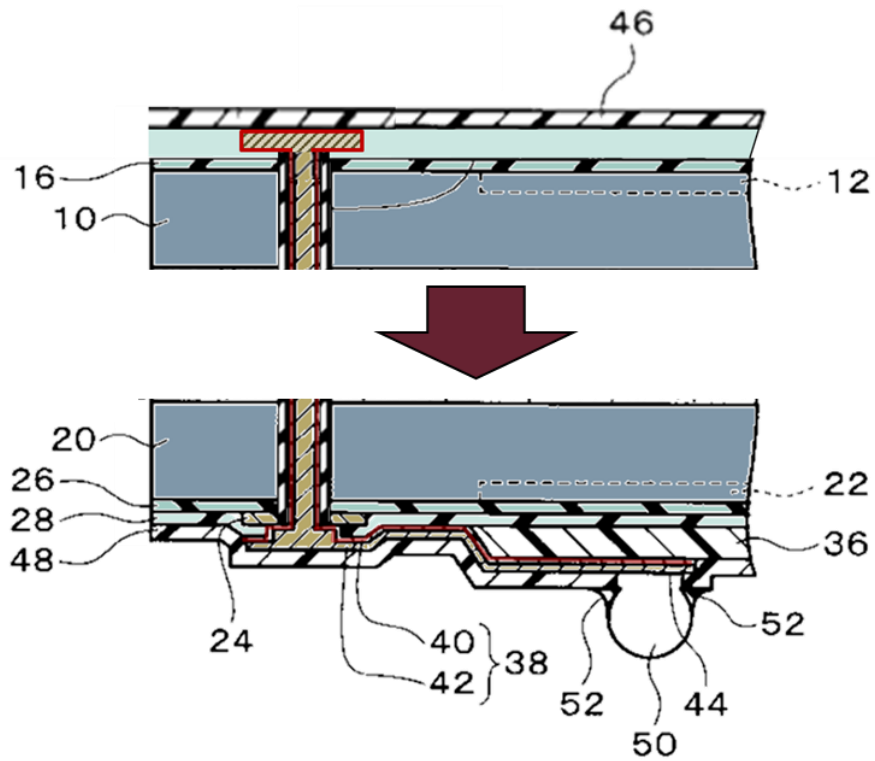
POSAs would next deposit a top metal barrier layer (§VI.A.3.a.i.(5)) and planarize (§VI.A.3.a.i.(6)). Guidash, ¶302. POSAs would deposit insulating layer

46, below. Imaoka, [0044], Fig. 7(B) (below, modified); Guidash, ¶302. POSAs would thin the back side of the substrate to expose the via for connection to the via in the second substrate. Guidash, ¶302; Pyo, 6 (“grinding the rear surface of the first substrate”).

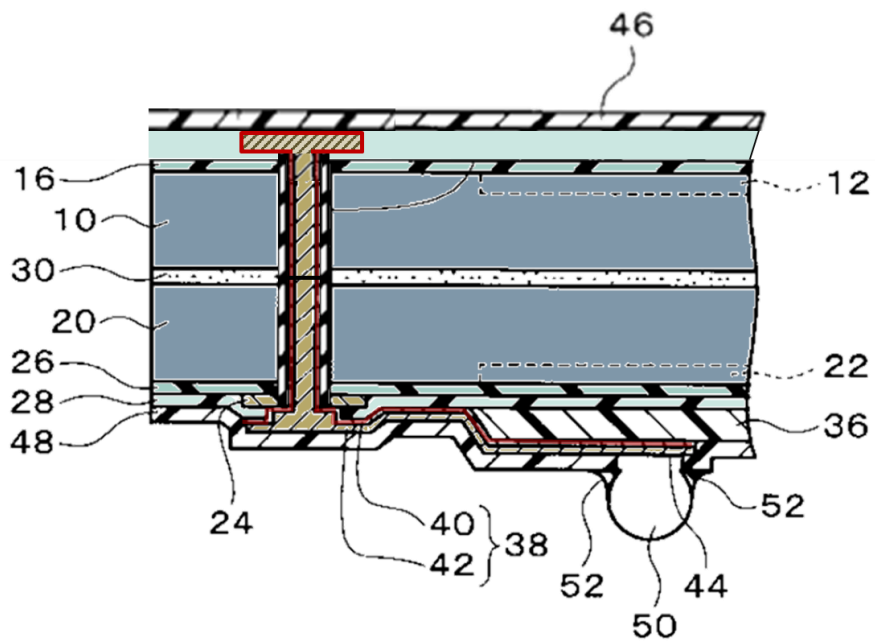


h. Bonding

302. POSAs would next bond the first substrate (as described above) to the second substrate (described by Imaoka, [0036]-[0044]). Guidash, ¶303; Pyo, 4; Iwabuchi, [0095]-[0096], Figs. 34A-34B.



The sensor resulting from modifying Imaoka's design for use of copper in pads 14 ("Imaoka-Choi Sensor") is shown below. Guidash, ¶291.



3. Reasonable Expectation of Success

POSAs would have had a reasonable expectation of success implementing copper for pad 14. Guidash, ¶304. Fabricating the pads 14 and part 38 on the first substrate is a straight-forward application of Choi's well-known dual-damascene process, which Choi itself and Gambino had already applied to image sensors. *Id.* Bonding the first and second substrates is a straight-forward application of known bonding techniques. *Id.*; Pyo 4; Iwabuchi, [0095]-[0096], Figs. 34A-34B.

4. Claim-by-Claim Analysis

a. Claim 1

The Imaoka-Choi Sensor meets every element of claims 1-2 and 4-8, rendering those claims obvious given the above-discussed reasons for the modification. Guidash, ¶305.

i. [1.pre]

[1.pre] An image sensor, comprising:

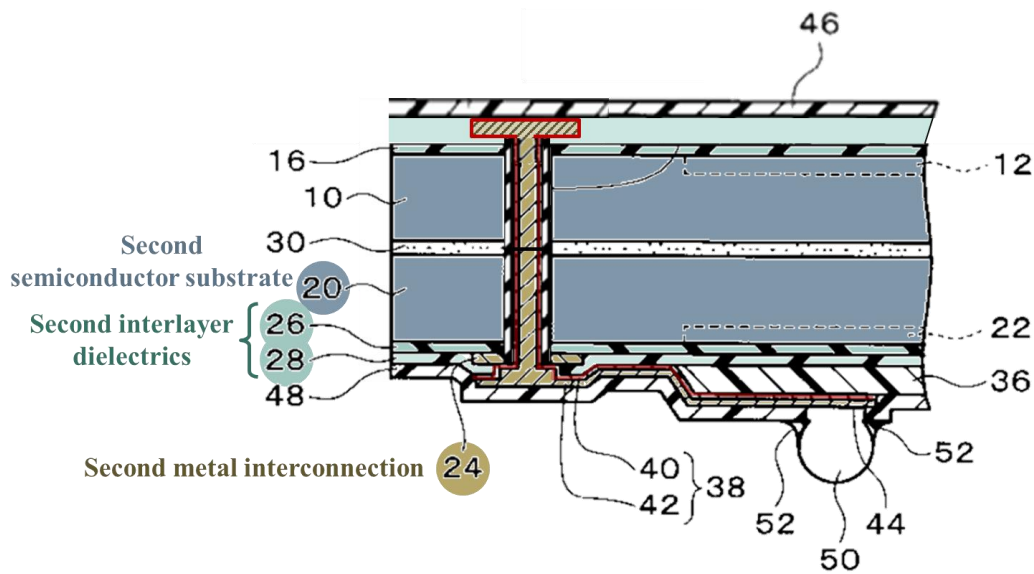
To the extent the preamble is limiting, the Imaoka-Choi Sensor satisfies the preamble because Imaoka's device is an image sensor (§VI.C.1.a) and the modification would leave this aspect unchanged. Guidash, ¶306.

ii. [1.1]

[1.1] a second semiconductor substrate including a second metal interconnection and a second interlayer dielectric;

The Imaoka-Choi Sensor satisfies limitation [1.1] because Imaoka's sensor does (§VI.C.1.b) and these aspects would remain unchanged after modification. Guidash, ¶307.

After Modification

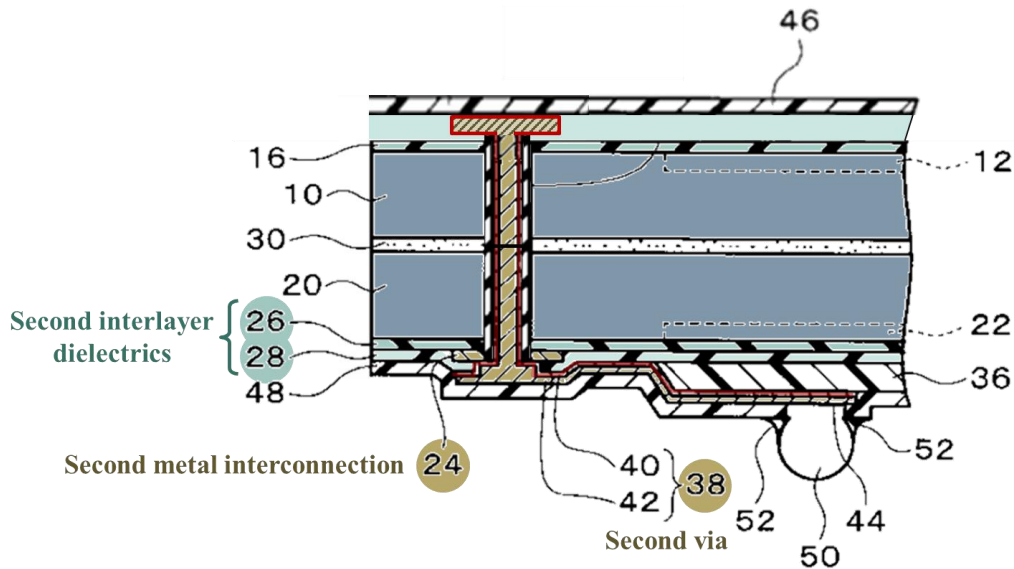


iii. [1.2]

[1.2] a second via penetrating the second interlayer dielectric so that the second via is connected to the second metal interconnection;

The Imaoka-Choi Sensor satisfies limitation [1.2] because Imaoka's sensor does (§VI.C.1.c) and these aspects would remain unchanged after modification. Guidash, ¶308.

After Modification

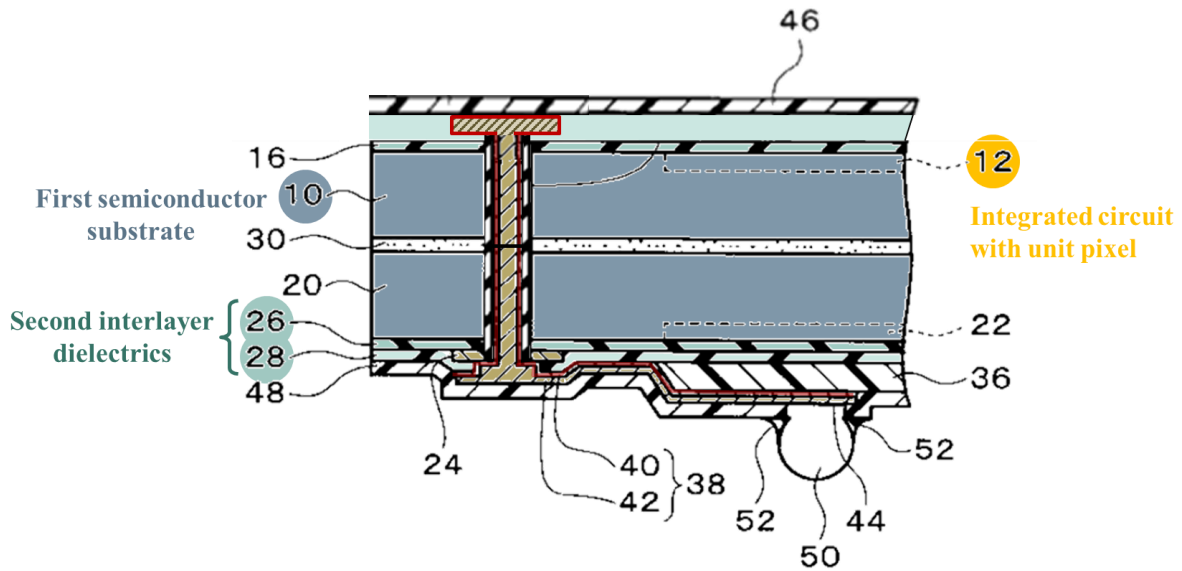


iv. [1.3]

[1.3] a first semiconductor substrate on the second interlayer dielectric, the first semiconductor substrate having a unit pixel;

The Imaoka-Choi Sensor satisfies limitation [1.3] because Imaoka's sensor does (§VI.C.1.d) and these aspects would remain unchanged after modification. Guidash, ¶309.

After Modification

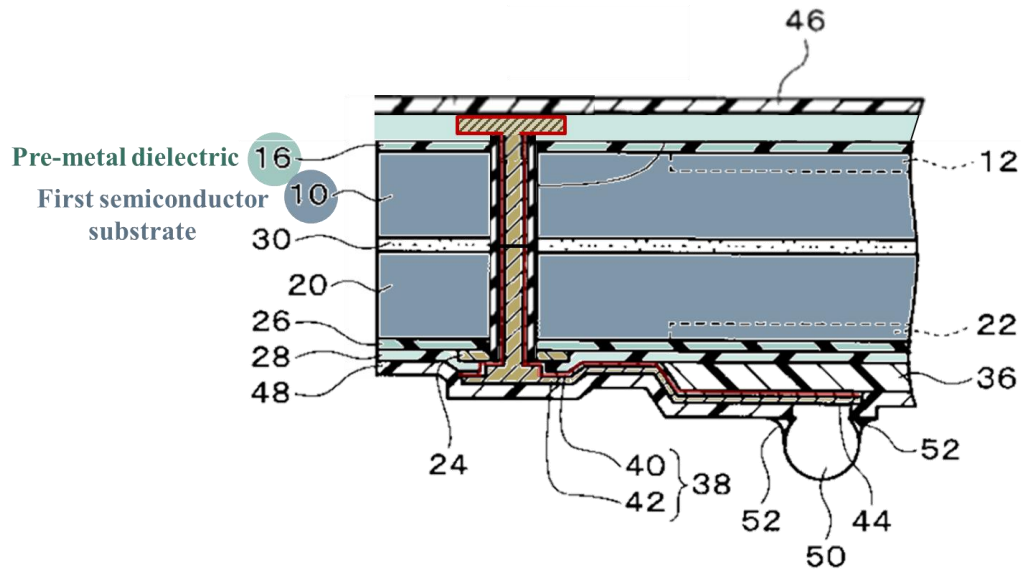


v. [1.4]

[1.4] a pre-metal dielectric on the first semiconductor substrate;

The Imaoka-Choi Sensor satisfies limitation [1.3] because Imaoka's sensor does (§VI.C.1.e) and these aspects would remain unchanged after modification. Guidash, ¶310.

After Modification

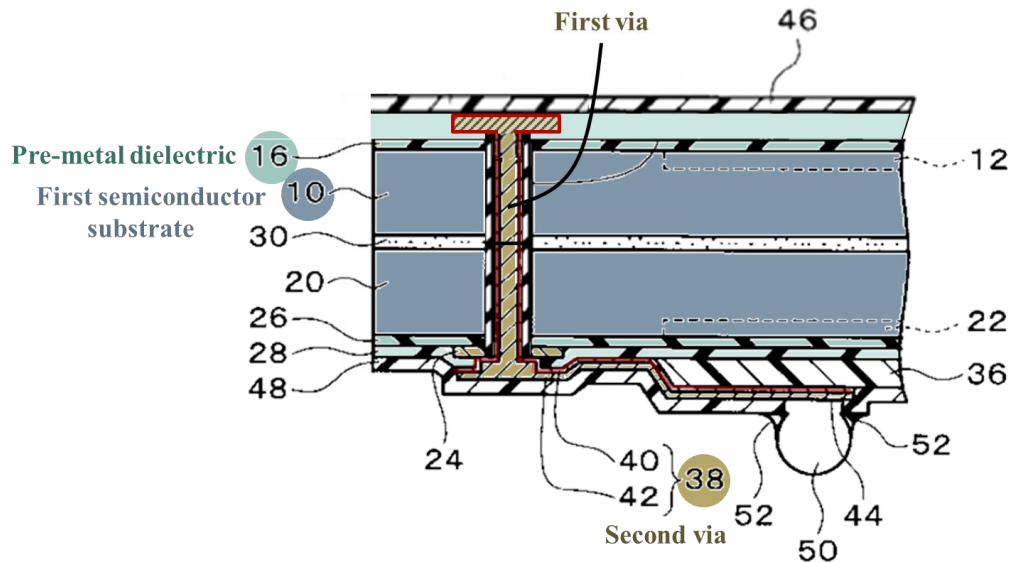


vi. [1.5]

[1.5] a first via penetrating the pre-metal dielectric and the first semiconductor substrate, the first via being connected to the second via;

The Imaoka-Choi Sensor satisfies limitation [1.5] under Patent Owner's interpretation because the "conductive part 38" would be fabricated in the first substrate separately from the second substrate before both substrates are bonded together, thus connecting the first and second substrates. §VI.E.2.

After Modification



vii. [1.6]

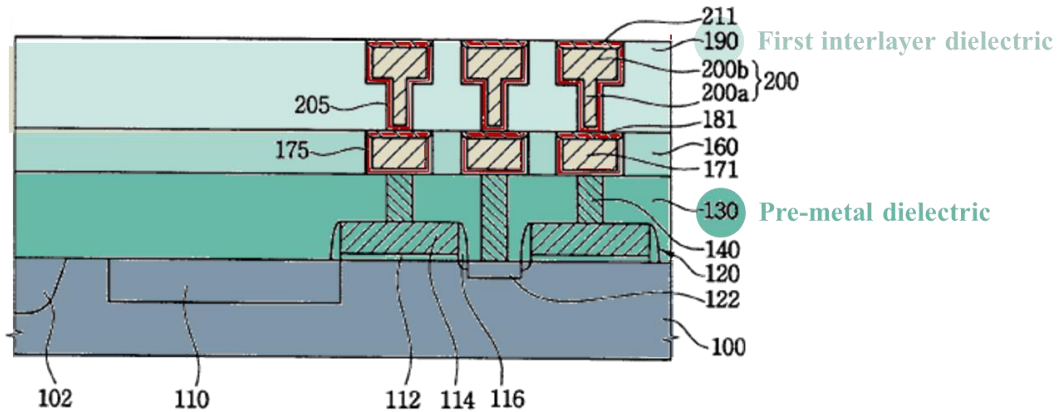
[1.6] a first interlayer dielectric on the pre-metal dielectric including the first via;

The Imaoka-Choi Sensor satisfies limitation [1.6] because, when implementing pads 14 in copper using Choi’s process, it has a first ILD on the PMD (that includes the first via), below. §VI.E.2; Guidash, ¶312.

After Modification



Specifically, Choi requires an ILD (“interlayer 190”) on a PMD (“lower insulation layer 130”). Choi, [0115], [0124], Fig. 5E (below); Guidash, ¶313.

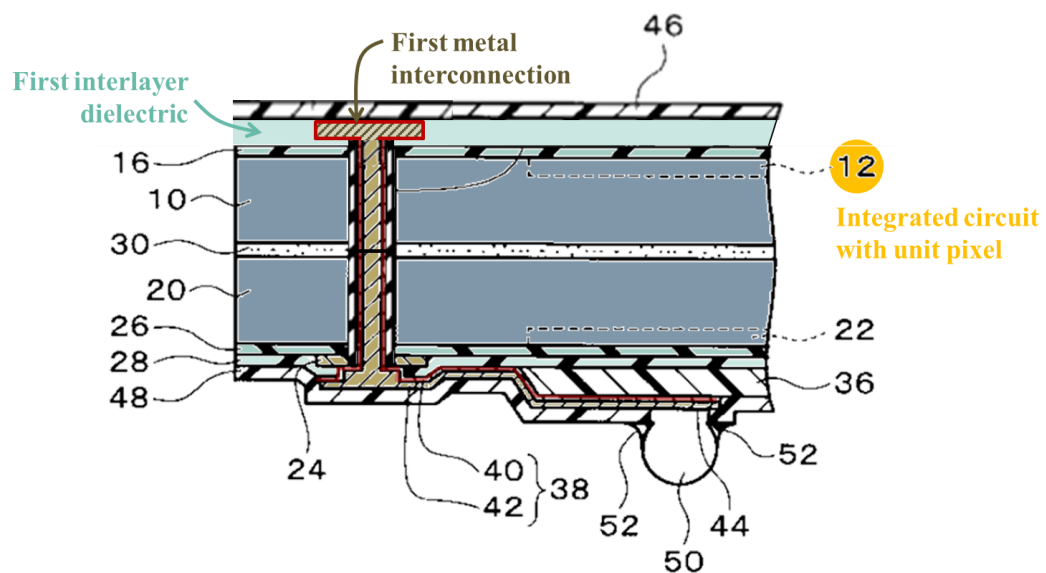


viii. [1.7]

[1.7] a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel;

The Imaoka-Choi Sensor satisfies limitation [1.7] because when implementing pads 14 in copper using Choi's processes, the pad would be located "on" a first ILD, below. §VI.E.2; Guidash, ¶314.

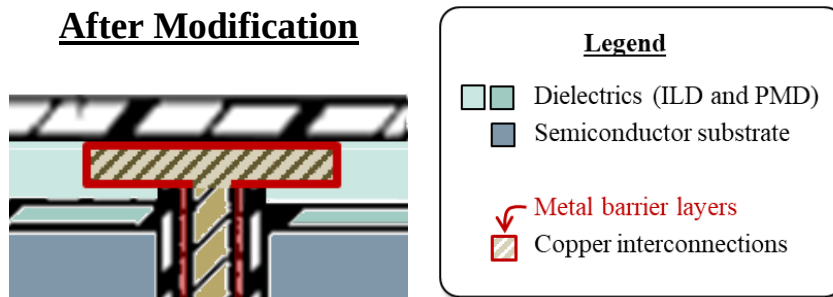
After Modification



ix. [1.8]

[1.8] a conductive barrier layer on the first metal interconnection; and;

The Imaoka-Choi Sensor satisfies limitation [1.8] because when implementing pads 14 in copper using Choi's processes, POSAs would have encapsulated the copper pads with a conductive barrier layer, including "on" the pads, shown below. §VI.E.2; Guidash, ¶315.



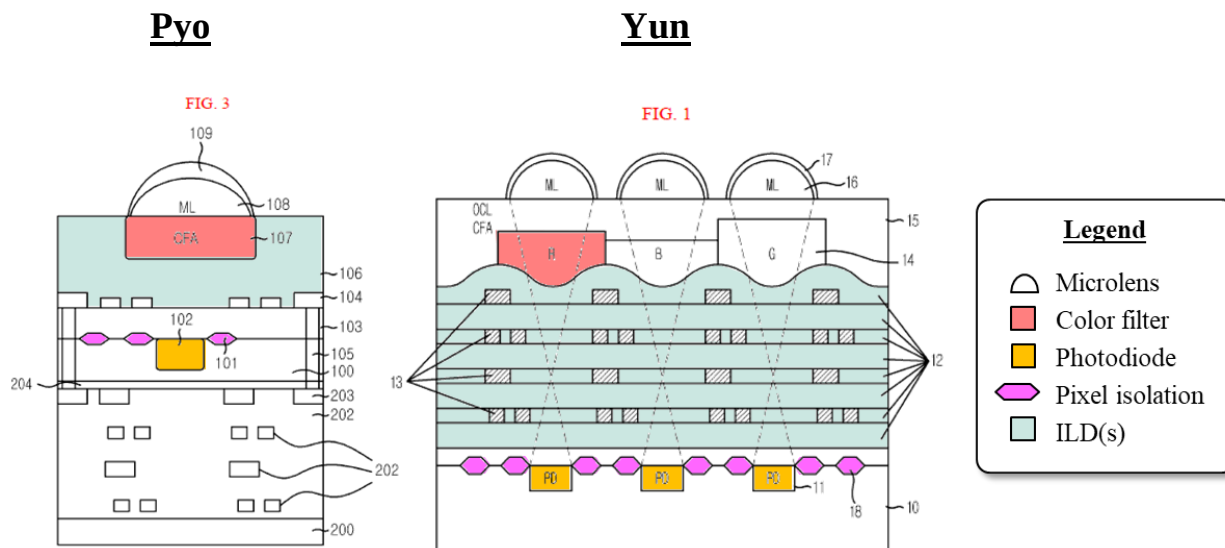
x. [1.9]

[1.9] a color filter and a microlens on the first interlayer dielectric on the unit pixel.

The Imaoka-Choi Sensor satisfies limitation [1.9] because Imaoka's sensor does (§VI.C.1.j) and these aspects would remain unchanged after modification. Guidash, ¶316.

Moreover, an obvious place to locate a color filter and microlens for the Imaoka-Choi Sensor would have been "on" the first ILD on the unit pixel because each would naturally have been fabricated on the first substrate *after* the unit pixel

and ILD layer had already been formed, a common location to put the microlens and color filter. *E.g.* Pyo, Fig. 3 (below); Yun, Fig. 1 (below); Guidash, ¶317.



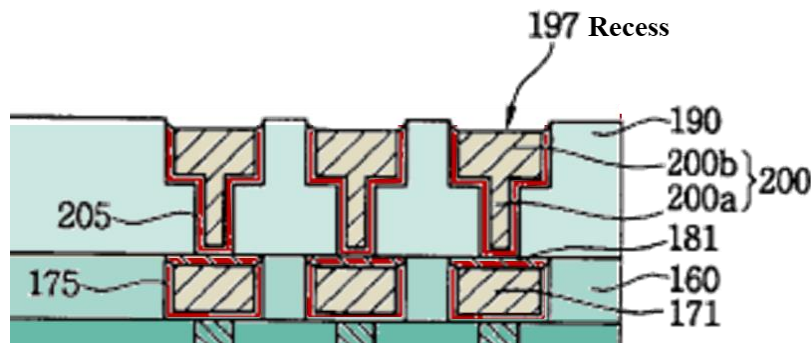
The color filter and microlens would be “on” the first ILD and the unit pixel in the Imaoka-Choi Sensor notwithstanding any intervening layers. Guidash, ¶318; ’366 patent, 2:17-22 (allowing for “intervening layers”).

b. Claim 2

Imaoka’ sensor satisfies claim 2’s additional limitation of the first metal interconnection being copper. §VI.C.2. POSAs would have selected copper in the Imaoka-Choi Sensor too. §VI.E.1 (motivation to use copper); §VI.E.2 (fabrication of first metal interconnection); Guidash, ¶319. Claim 2 is thus unpatentable as obvious.

c. Claim 4

The Imaoka-Choi Sensor satisfies claim 4's additional limitation that the first metal interconnection has a top surface lower than that of the first ILD, such that there is a "height difference" between the two, because Choi discloses creating a recess for a top barrier layer, a common practice and would have been an obvious when implementing copper interconnections in Imaoka's sensor with Choi's processes. §VI.E.2.f (use of CMP to create a recess); Choi, [0128]-[0129], Figs. 5E, 5F (excerpted, below), and 5G; Guidash, ¶320. Claim 4 is thus unpatentable as obvious.

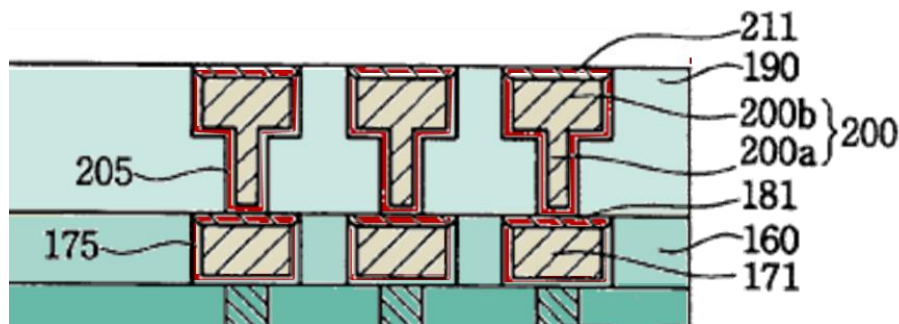


d. Claim 5

Imaoka's sensor satisfies claim 5's additional limitation that the second metal interconnection comprises copper or aluminum. §VI.C.4. This aspect would remain unchanged after modification. §VI.E.2.e; Guidash, ¶321. Claim 5 is thus unpatentable as obvious.

e. Claim 6

The Imaoka-Choi Sensor satisfies claim 6's additional limitation that the conductive barrier layer has at top surface substantially even with the top surface of the first ILD because Choi discloses depositing a barrier layer in a recess above the copper interconnections and planarizing so the top surface of the barrier layer is even with the top surface of the first ILD, a common practice, and would have been obvious when implementing copper interconnections in Imaoka's sensor with Choi's processes. §VI.E.2.g (planarizing); Choi, [0129] (referencing back to [0122]-[0123]), Fig. 5G (excerpted below); Guidash, ¶322. Claim 6 is thus unpatentable as obvious.



f. Claim 7

Imaoka's sensor satisfies claim 7's additional limitation that the first via and the second via comprise the same material. §VI.C.6. This aspect would remain unchanged after modification. §VI.E.2; Guidash, ¶323. Claim 7 is thus unpatentable as obvious.

g. Claim 8

Imaoka's sensor satisfies claim 8's additional limitation that the second semiconductor substrate provides metal interconnections for connection to a power line and an external signal line. §VI.C.7. This aspect would remain unchanged after modification. §VI.E.2. Claim 8 is thus unpatentable as obvious.

F. GROUND 6: Imaoka in view of Choi and Dublin Renders Claim 3 Obvious

When implementing the Imaoka-Choi Sensor discussed in Ground 5, it would have been obvious to use a CoWP alloy for the conductive barrier layer as disclosed in Dublin—thereby also rendering obvious claim 3, which depends from claim 1 and further requires cobalt or nickel alloy for the conductive barrier layer.

1. Reasons to Use CoWP Barrier Layer

POSAs would have used CoWP as the conductive barrier layer for the same reasons discussed in §VI.B.1; Guidash, ¶326.

2. Resulting Sensor and Reasonable Expectation of Success

The resulting sensor would be identical to the Imaoka-Choi Sensor described in Ground 5 except using CoWP as the conductive barrier material. Guidash, ¶327. POSAs would have had a reasonable expectation of successfully using CoWP as a barrier material because it is fabricated using the industry-standard dual-damascene process. *Compare* §VI.E.2 with Dublin, 8:1-65; Guidash, ¶327. Moreover,

Gambino successfully used CoWP in place of silicon nitride as a copper interconnection barrier layer in a CMOS sensor. Gambino, 25.

3. Claim 3 Analysis

The resulting sensor includes a conductive metal barrier layer comprising a cobalt (Co) alloy (i.e., CoWP), thereby satisfying claim 3's additional element and rendering it obvious. Guidash, ¶328; Dublin, 2:63-66, 3:53-55.

VII. DISCRETIONARY DENIAL IS NOT WARRANTED

A. Discretionary Denial Not Warranted Under *Fintiv*

There is no basis to deny institution under 35 U.S.C. §314(a) given the Texas Litigation and the factors identified in *Apple v. Fintiv*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential).

1. Factor 1: Potential for litigation stay

The “litigation stay” factor is neutral because neither party “has requested a stay thus far.” *Autostore Sys. v. Ocado Innovation*, IPR2022-00673, Paper 7, 9-10 (PTAB Sept. 14, 2022) (citing *Apple v. Fintiv*, IPR2020-00019, Paper 15, 12 (PTAB May 13, 2020) (informative)). Petitioner intends to seek a stay should review be instituted. *E.g.*, *Arbor Glob. v. Samsung Elecs.*, No. 219CV00333JRGRSP, 2021 WL 66531, at *3 (E.D. Tex. Jan. 7, 2021) (staying litigation pending instituted IPRs).

2. Factor 2: Trial date relative to FWD deadline

Per the Office’s June 21, 2022 memorandum¹⁴ (“Memo”), “the PTAB will consider the median time from filing to disposition of the civil trial for the district in which the parallel litigation resides.” The median time in this case is currently 24.5 months, thereby projecting trial in June 2024—after the anticipated date for a final written decision here. This factor therefore favors institution, notwithstanding the slightly earlier (March 2024) trial date currently scheduled. *Apple v. Scramoge Tech.*, IPR2022-00573, Paper 12, 8-9 (PTAB Sept. 13, 2022) (citing median statistics and instituting review, notwithstanding earlier scheduled trial).

3. Factor 3: Investment in parallel proceedings

The “investment” factor favors institution because the Texas “court has yet to hold a claim construction hearing [scheduled for September 6, 2023] or issue a claim construction order, and the parties have not begun expert discovery or work on dispositive motions.” *Autostore*, IPR2022-00673, Paper 7, 11-12. Further, Petitioner exercised reasonable diligence by filing the Petition less than three months after receipt of Patent Owner’s infringement contentions and six months after Patent Owner filed suit.

¹⁴ https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf

4. Factor 4: Issue overlap

The “issue overlap” factor favors institution because Petitioner stipulates that, should the Board institute review, Petitioner and the other defendants will not rely upon any invalidity grounds based on Pyo and/or Imaoka (i.e., the primary references herein). *Sand Revolution II v. Cont’l Intermodal Group-Trucking*, IPR2019-01393, Paper 24, 11–12 (PTAB June 16, 2020) (informative).

5. Factor 5: Parties

The “parties” factor is neutral because while Petitioner is a “defendant[] in the parallel litigation ... there is uncertainty as to whether the district court will go to trial before the final written decision is due in this proceeding.” *Samsung Elecs. v. Jawbone Innovations*, IPR2022-00630, Paper 10, 13-14, 17 (PTAB Sept. 13, 2022) (citing median time-to-trial).

6. Factor 6: Other considerations

Aside from the above-noted factors, discretionary denial would be inappropriate because the above-noted grounds present “a compelling unpatentability challenge”—that is, a “meritorious” challenge “in which the evidence, if unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable by a preponderance of the evidence.” *Nokia of Am. Corp. v. TQ Delta*, IPR2022-00664, Paper 10, 8-9 (PTAB Sept. 27, 2022) (quoting Memo). The cancellation of the Korean counterparts to the Challenged Claims following the Korean examiner’s rejection over Pyo (a Korean-language reference

the Korean examiner could understand but the U.S. examiner could not) confirms the compelling nature of the challenge herein.

7. Conclusion

Discretionary denial under §314(a) would be inappropriate, as three of the primary five *Fintiv* factors favor institution while the other two are neutral. Petitioner’s compelling unpatentability challenge is a separate basis for institution.

B. Discretionary Denial Not Warranted Under Section 325(d)

Under the Board’s two-part framework under *Advanced Bionics v. Med-El Elektromedizinsche Gerate*, IPR2019-01469, Paper 6, 8 (PTAB Feb. 13, 2020) (precedential), the Board first determines “(1) whether the same or substantially the same art...or...arguments previously were presented to the Office.” If the answer is no, the inquiry ends there. But if the answer is yes, the Board then determines “whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.” *Id.*

1. The References Cited Were Not “Presented to the Office”

Of the cited references herein, none were before the Office except for a Korean-language version of Pyo and an English translation of its Abstract, provided in an IDS. Ex. 1002, 30. The Examiner, however, never cited or otherwise discussed Pyo.

The Board has “consistently held that a reference that was neither applied against the claims nor discussed by the Examiner does not weigh in favor of

exercising our discretion under §325(d).” *Solvay USA v. WorldSource Enterprises*, PGR2019-00046, Paper 7, 14 (PTAB Aug. 13, 2019). This includes “[m]ere citation in an IDS.” *Id.*; *Zip Top v. Stasher*, IPR2018-01216, Paper 14, 35 (PTAB Jan. 17, 2019) (“mere citation to a reference by the Examiner does not establish that the Examiner substantively considered the merits of” the reference).

Further, the English translation of the Pyo Abstract fails to disclose several elements disclosed by Pyo, including at least, (1) a first and a second ILD (limitations [1.1] and [1.6]), (2) a PMD (limitation [1.5]), (3) a first metal interconnection (the abstract only discloses metal lines on the second substrate) (limitation [1.7]), and (4) a color filter (limitation [1.9]). *Compare* claim 1 with Ex. 1002, 30; Guidash, ¶79. Nor does the Pyo Abstract disclose the possibility of copper lines and vias—a significant aspect of the above-discussed obviousness grounds. The English translation of the Pyo Abstract thus fails to disclose the features Pyo discloses; the abstract is not cumulative of Pyo.

Moreover, the Korean examiner’s rejection and the Applicant’s subsequent cancellation of the device claims over Pyo in the related Korean prosecution was also not provided to the Office. Guidash, ¶78; Ex. 1002; §IV.C.1, above.

2. Even if Pyo Was “Presented to the Office,” the Office Materially Erred by Overlooking Its Impact

Even if the Board finds Pyo was previously “presented to the Office,” the Examiner “misapprehend[ed] or overlook[ed] specific teachings of the relevant

prior art [i.e., Pyo] where those teachings impact patentability of the challenged claims.” *Cellco P'ship v. Huawei Device*, IPR2020-01117, Paper 10, 12 (PTAB Feb. 3, 2021). Here, the Examiner never cited Pyo. Thus, the Examiner overlooked specific teachings of Pyo impacting the patentability of the claims challenged in this Petition. *Id.* Similarly, the “fact that [the references in the Petition were] not the basis of rejection weighs strongly against exercising [the Board’s] discretion to deny institution under 35 U.S.C. §325(d).” *Id.*, 13.

The Petition is supported by an English translation of the entirety of Pyo—not just its abstract—and an expert declaration explaining how POSAs would have understood Pyo. Guidash, ¶¶104-110. This new evidence weighs against discretionary denial. *Puma North America v. Nike*, IPR2019-01058, Paper 10, 19 (PTAB Oct. 31, 2019) (instituting where petition presented “new non-cumulative evidence.... probative to issues of patentability and helpful to our consideration of a prior art combination that was not before the Examiner”); *Apple v. MPH Techs. Oy*, IPR2019-00819, Paper 10, 16-17 (PTAB Sept. 27, 2019) (similar).

Moreover, the Examiner never had the opportunity to consider Pyo in combination with Choi, which was not of record. Thus, there is no overlap between the grounds in this Petition and anything considered during prosecution. *Cellco P'ship*, Paper 10, 14 (declining to exercise §325(d) discretion where the combination “as asserted in the Petition has not been substantively evaluated by

the Office”); *Asetek Danmark A/S v. Coolit Sys.*, IPR2019-00705, Paper 19, 9-11 (PTAB Sept. 6, 2019) (granting institution where “the same art may have been considered during examination, [but] the Examiner did not evaluate Petitioner’s [arguments].”).

3. Conclusion

The Office never had a full English translation of Pyo, the abstract of which fails to disclose all the features of Pyo’s sensor. And this Petition combines Pyo with Choi, which was not of record. Further, Grounds 3-6 rely entirely on art never of record in any form. The Board should decline to deny institution under §325(d).

VIII. CONCLUSION

The Board should institute review and cancel claims 1-8.

Dated: December 2, 2022

Respectfully submitted,
Sony Group Corporation

/Jason W. Balich/

Jason W. Balich, Reg. No. 67,110

CERTIFICATE OF SERVICE UNDER 37 C.F.R. §42.6 (E)(4)

I certify that on December 2, 2022, I will cause a copy of the foregoing document, including any exhibits or appendices filed therewith, to be served via Overnight FedEx at the following correspondence address of record for the patent:

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

Date: December 2, 2022

/MacAulay Rush/
MacAulay Rush
Paralegal
WOLF, GREENFIELD & SACKS, P.C.

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24, the undersigned certifies that the foregoing Petition for *Inter Partes* Review contains 13,997 words excluding a table of contents, a table of authorities, Mandatory Notices under §42.8, a certificate of service or word count, or appendix of exhibits or claim listing, but including a table of abbreviations and annotations added to figures. Petitioner has relied on the word count feature of the word processing system used to create this paper in making this certification, manually adding to that the number of words present in annotations to figures.

Date: December 2, 2022

/MacAulay Rush/
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