

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY GROUP CORPORATION,
Petitioner

v.

VISIONX TECHNOLOGIES, LLC,
Patent Owner

IPR2023-00298
U.S. Patent No. 7,868,366

**PATENT OWNER'S PRELIMINARY RESPONSE
TO PETITION FOR *INTER PARTES* REVIEW
*37 C.F.R. §42.107***

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PATENT OWNER’S CURRENT EXHIBIT LIST¹

Exhibit	Brief Description
2001	Comprehensive Dictionary of Electrical Engineering
2002	Oxford Dictionary of Electrical Engineering
2003	Tutorial on Forming TSVs
2004	Consent to Proceed Before Magistrate Judge Payne
2005	Amended Docket Control Order
2006	U.S. Dist. Courts—National Judicial Caseload Profile
2007	VisionX Notice re Infringement Contentions
2008	Sony Notice re Invalidity Contentions
2009	Sony Invalidity Contentions & ID of Doc Production
2010	IDS
2011	IDS Foreign Reference Pyo and English Abstract
2012	IDS Foreign Reference Sugimoto and English Abstract
2013	IDS References Considered by Examiner

¹ Relevant portions of exhibits may be highlighted to help the Board locate cited sections.

I. INTRODUCTION

Pursuant to 35 U.S.C. §313 and 37 C.F.R. §42.107, Patent Owner, VisionX Technologies, LLC, hereby provides a Preliminary Response to the Petition for *Inter Partes* Review (IPR) filed December 2, 2022 (Paper 2, herein “Petition” or “Pet.”). A Notice dated January 26, 2023 (Paper 5) set April 26, 2023 as the deadline for this Preliminary Response, which is timely filed.

Petitioner Sony Group Corporation filed the Petition challenging claims 1-8 of the ‘366 patent (Ex. 1001, U.S. Patent No. 7,868,366) on six grounds. Pet. 5. For each of the six grounds, the relied upon references fail to disclose key limitations of the challenged claims. For example, claim 1 specifically recites “a second via penetrating the second interlayer dielectric so that the second via is connected to the second metal interconnection.” Despite relying on two different primary references—Pyo and Imaoka—Sony’s Petition fails to show that this element is found in the prior art.

As detailed in this Preliminary Response, Pyo does not show or discuss a second via or how and where it is connected. Moreover, in Petitioner’s combined “Pyo-Choi” drawing which shows second vias manually added by Petitioner, any alleged second via terminates below “pad 203” and never penetrates “insulating layer 202,” Petitioner’s purported second interlayer dielectric. As a result, the

most that can be said of Pyo is that any purported second via (even as inserted in the modified drawings by Petitioner) is within the second interlayer dielectric. Further, claim element “the first via being connected to the second via” is not disclosed by Pyo.

Similarly, as discussed below, Imaoka fails to disclose a first via and a second via. Petitioner seemingly recognizes this problem by stating that “Imaoka discloses only a single part 38 to connect the first and second substrates.” Pet. 64. Specifically, Imaoka discloses only a *single* “through-hole 32” that extends through the first and second semiconductor substrates that is subsequently filled with “conductive part 38.” Because Petitioner identifies this single through-hole (and conductive material) as both the “first via” and the “second via” of claim 1, Petitioner’s reliance on Imaoka is misplaced. Imaoka also fails to disclose the claim element “a first metal interconnection on the first interlayer dielectric.”

Finally, the Board should exercise its discretion to deny this Petition because the same invalidity arguments will be addressed, and resolved, in the co-pending district court proceedings before the Board would issue a final written decision here. As discussed below, not only do the factors for discretionary denial weigh in Patent Owner’s favor, but Petitioner’s Pyo reference was previously disclosed and considered during prosecution.

II. PETITIONER’S IMPROPER RELIANCE ON THE “KOREAN EXAMINER’S REJECTION OVER PYO”

The Petition states that a “meritorious challenge” is presented since the “cancellation of the Korean counterparts [*sic*] to the Challenged Claims following the Korean examiner’s rejection over Pyo (*a Korean-language reference the Korean examiner could understand but the U.S. examiner could not*) confirms the compelling nature of the challenge herein.”² Pet. 98-99. However, contrary to Petitioner’s contention, the claims in the Korean application (the Korean priority application or “KR ‘914”) were substantially different from, not substantially the same as, the claims pending before the U.S. Examiner.

A side by side comparison of the claims in KR ‘914 and claim 1 of the ‘366 patent shows that the U.S. application claims were in fact substantially different from the Korean application claims. As one example, the following element of claim 1 of the ‘366 patent is not present in any of the listed claims 1-5 of KR ‘914: *“a first via penetrating the pre-metal dielectric and the first semiconductor substrate, the first via being connected to the second via.”* See claims 1-5 of KR ‘914 listed in Guidash, ¶76. Nor are the following elements of claim 1 of the ‘366

² Emphasis is added throughout unless otherwise noted.

patent present in any of the listed claims 1-5 of KR ‘914: “*a pre-metal dielectric on the first semiconductor substrate*” and “*a first interlayer dielectric on the pre-metal dielectric including the first via.*” *Id.*

Despite the clear and substantial differences in the claims, Petitioner’s expert declares that: “Claims 1-5 rejected by the Korean examiner (as translated into English in a certified English translation) were *substantially the same* as claims 1 and 3-5 of the ‘366 patent.” Guidash, ¶76. This statement is manifestly incorrect. Claims 1-5 rejected by the Korean examiner were *substantially different from (not substantially the same as)* claims 1 and 3-5 of the ‘366 patent. Not only is Guidash’s testimony devoid of support in many of its assertions, it is also remarkably similar to the Petition. Many of the paragraphs in the declaration are nothing more than statements that appear to be identical in their operative wording to paragraphs in the Petition. This is a reason to give Petitioner’s expert testimony little or no weight. *See Kinetic Techs. Inc. v. Skyworks Solutions, Inc.*, IPR2014-00530, Paper 8 at 13 (PTAB Sept. 29, 2014) (giving “the cited evidence of [petitioner’s expert] Declaration no probative weight” because “[m]erely repeating an argument from the Petition in the declaration of a proposed expert does not give that argument enhanced probative value.”).

Moreover, the Guidash declaration has quite incorrectly equated the “*interlayer insulating film*” appearing in the Korean application claim element “an interlayer insulating film comprising a metal wiring and a conductive barrier film formed on the first semiconductor substrate” to “*a pre-metal dielectric on the first semiconductor substrate*” in claim element [1.4] of the ‘366 patent. Guidash, ¶76. An “*interlayer* insulating film” is between metal layers and not a “pre-metal dielectric.” In fact, in the same Guidash declaration, the same “*interlayer insulating film*,” has been also equated to the “*first interlayer dielectric*” of the ‘366 patent claim elements [1.7] and [1.9]. *Id.* Clearly, the “interlayer insulating film” *cannot be equated to two different claim elements* in claim 1 of the ‘366 patent at the same time, i.e., it cannot be both the “pre-metal dielectric” and the “first interlayer dielectric.”

Following the incorrect statement that the Korean and U.S. claims were substantially the same, the Petition advances the speculation that the U.S. Examiner “*misapprehended*” Pyo, even though Pyo and all its drawings, and its translated abstract were brought to the Examiner’s attention.

Importantly, the abstract of the translated Pyo presented in the Petition is different from the abstract that was submitted to the U.S. Examiner by the Applicant. The abstract submitted to the U.S. Examiner appears in the IDS in the

prosecution history of the '366 patent (Ex. 1002, 30), and has several reference numerals referring to various elements in Pyo's main drawing that would have very well aided the U.S. Examiner in determining the relevance of Pyo.

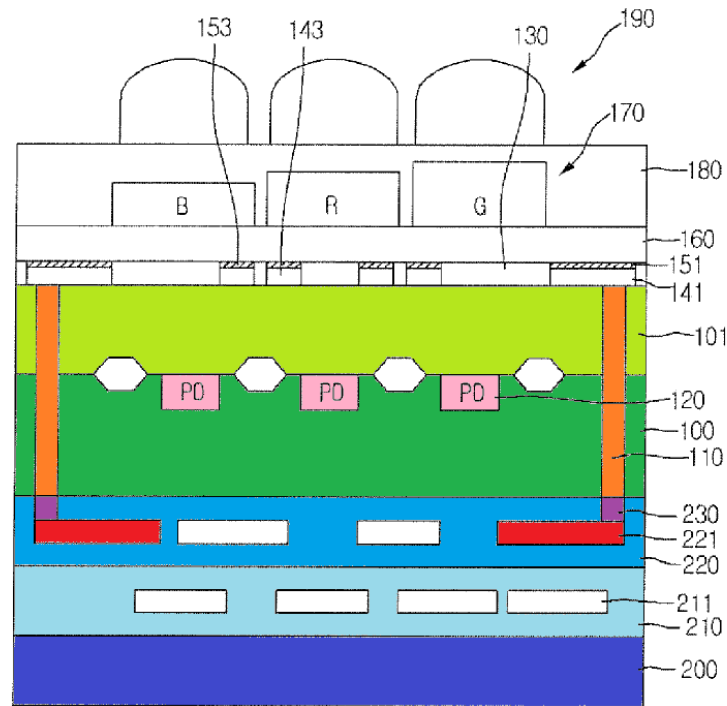
The Pyo reference was in fact before the U.S. Examiner as only one of two references cited in the IDS for consideration. Instead of Petitioner's unsupported speculation that the U.S. Examiner "misapprehended" Pyo, a better explanation is that the Examiner deemed Pyo to be sufficiently different than claim 1 of the '366 patent, and decided to allow the claim.

III. BACKGROUND

A. THE '366 PATENT

The '366 patent is generally directed to an image sensor comprising a first semiconductor substrate (100) having a unit pixel (comprising photodiode 120) and a pre-metal dielectric (101), and a second semiconductor substrate (200) having a metal interconnection (221) and an interlayer dielectric (220). A first via (110) penetrates the pre-metal dielectric and the first semiconductor substrate and a second via (230) penetrates the interlayer dielectric so that the second via is connected to the metal interconnection. The first via and the second via are connected allowing signals from the unit pixel to be communicated to the metal

interconnection of the second semiconductor substrate. An embodiment described in the '366 patent is illustrated and labeled below:



'366 Patent Fig. 8 (colorized)

The use of a first via and a second via in the manner disclosed and claimed plays an important role. For example, the use of a second via may alleviate the need for extra pads, which would have been necessary to provide an indirect connection between the image sensor and logic circuitry. The use of such additional features not only requires additional masking steps, which increases expense and reduces manufacturing throughput in the fabrication process, it would

consume additional space on the chip and reduce flexibility in routing other interconnections. For example, the footprint required for using a connection pad may be significantly larger than the area required to etch a via, thus limiting design optimization. Similarly, by using a first via and a second via, an image sensor manufacturer is better able to tailor the corresponding etch processes to account for fabrication concerns—such as undercut—and different materials that the via profiles may extend through.

The advantage of a first and second via, in accordance with the claim language, is a feature is that is lacking in all of the art references relied upon by Petitioner. Accordingly, institution of *Inter Partes* Review should be denied.

B. ART REFERENCES RELIED UPON

Petitioners assert six grounds of invalidity based on four references:

Ground	Claims	Statute	References
1	1-2 and 4-8	§103	Pyo+Choi
2	3	§103	Pyo+Choi+Dublin
3	1-2 and 4-8	§102	Imaoka
4	3	§103	Imaoka+Dublin
5	1-2 and 4-8	§103	Imaoka+Choi
6	3	§103	Imaoka+Choi+Dublin

Pet. at 5.³

1. PYO

Pyo is an English translation of Korean Unexamined Patent Application Publication No. 10-2006-0077132, titled “CMOS Image Sensor of 3D Integrated Structure and Manufacturing Method Thereof.” Ex. 1005. According to Petitioner’s translation, Pyo is directed to “us[ing] a single pad to three-dimensionally integrate an image chip ... by separating it into a logic chip consisting of a logic array that can bestow driver IC and other additional functions to drive it, and a logic chip.” *Id.*, Abstract. Pyo is not directed to the use of a first via and a second via that penetrates an interlayer dielectric to connect an image sensor chip to a logic chip, and thus Pyo does not recognize the problem that is solved by the ‘366 patent. Indeed, Patent Owner notes that Pyo was one of only two art references that were disclosed to the Examiner during prosecution (Ex.

³ For this preliminary response, Patent Owner has addressed independent claim 1, which is sufficient to show that Petitioner has failed to demonstrate a reasonable likelihood of success with respect to all challenged claims 1-8. However, Patent Owner reserves the right to address the deficiencies in the Petition with respect to dependent claims 2-8.

2010), and the Examiner was fully able to consider Pyo's Figure 3, which forms the backbone of Petitioner's "Pyo-Choi" combination drawing. Instead of disclosing the novelty of the '366 patent, Pyo and its Figure 3 are directed generally to "omitting the plurality of metal lines on the photodiode" itself and are not focused on the interconnection of the image sensor and logic chips. *See, e.g., id.*, 4 and Fig. 3.

2. IMAOKA

Imaoka is an English translation of Japanese Patent No. 3800335, titled "Optical Device, Optical Module, Semiconductor Device and Electronic Equipment." Ex. 1006. According to Petitioner's translation, Imaoka is directed to "forming an integrated circuit on both surfaces of a semiconductor chip." *Id.*, Background of Invention. Imaoka is not directed to the use of a first via and a second via that penetrates an interlayer dielectric to connect an image sensor chip to a logic chip, and thus Imaoka does not recognize the problem that is solved by the '366 patent. Instead, Imaoka is directed generally to the use of a single "through-hole" etched from a top surface of an upper semiconductor substrate to a bottom surface of a lower semiconductor substrate to connect a power supply terminal from the lower semiconductor substrate to the upper semiconductor substrate. *See, e.g., id.*, Fig 3.

3. CHOI

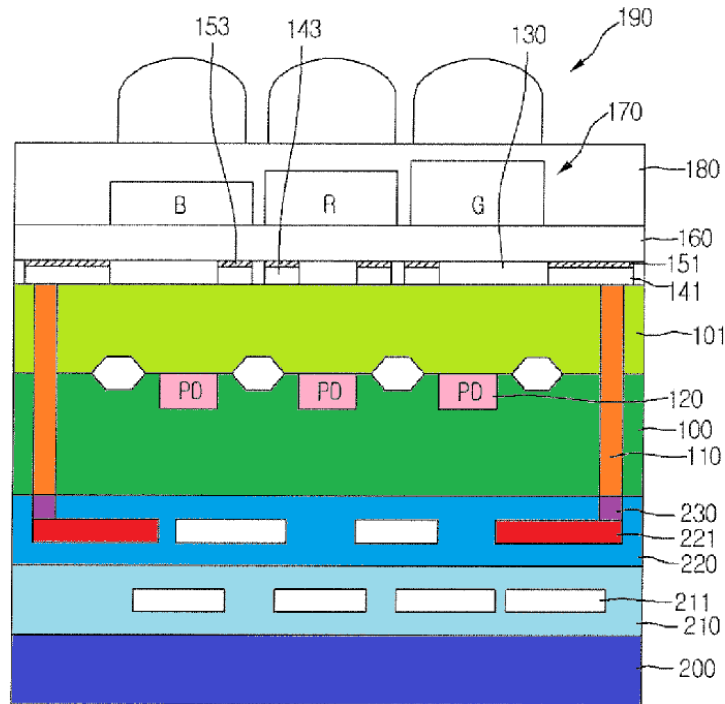
Choi is U.S. Patent Application Publication No. 2005/0012166A1 and is titled “Image Sensor.” Ex. 1007. Choi is directed to a “diffusion barrier layer” that prevents diffusion of copper into surrounding areas of an image sensor chip. *Id.*, [0008]. Choi is a single-substrate reference and is not directed to the use of a first via and a second via that penetrates an interlayer dielectric to connect an image sensor chip to a logic chip. Thus, Choi does not recognize the problem that is solved by the ‘366 patent. Instead, Petitioner relies on Choi for disclosing use of copper in dual-damascene and a conductive metal barrier layer. *See* Pet. 54.

IV. CLAIM CONSTRUCTION

Petitioner suggests that “[a]s the terms are used consistently with how they are used in the art, Petitioner does not believe any term requires construction for purposes herein.” Pet. 15. Although Patent Owner agrees that the terms are used consistently with how they are used in the art and, as a result, do not require any construction, Patent Owner disagrees with Petitioner’s application of the plain language to its analysis of the cited references.

Importantly, for purposes of the Petition, claim 1 recites “a second via ***penetrating*** the second interlayer dielectric so that the second via is connected to the second metal interconnection.” ‘366 patent, 7:62-64. With respect to the term

“penetrating,” the ‘366 patent states that “[t]he first via 110 can be formed to *penetrate* through both the first semiconductor substrate 100 and a pre-metal dielectric (PMD) 101 formed on the first semiconductor substrate 100. That is, the first via 110 can be exposed at the bottom surface of the first semiconductor substrate 100.” *Id.*, 2:35-39. Similarly, elsewhere the ‘366 patent states that “the second via 230 can *penetrate* the third interlayer dielectric 220 and be exposed.” *Id.*, 3:21-22. These disclosures of the ‘366 patent are reflected, for example, in Figure 8 (reproduced and colorized below). As shown, the first via 110 (orange) penetrates the first substrate 100 (green) and the pre-metal dielectric 101 (light green), while the second via 230 (purple) penetrates the interlayer dielectric 220 (blue) so that the second via is connected to metal interconnection 221 (red):

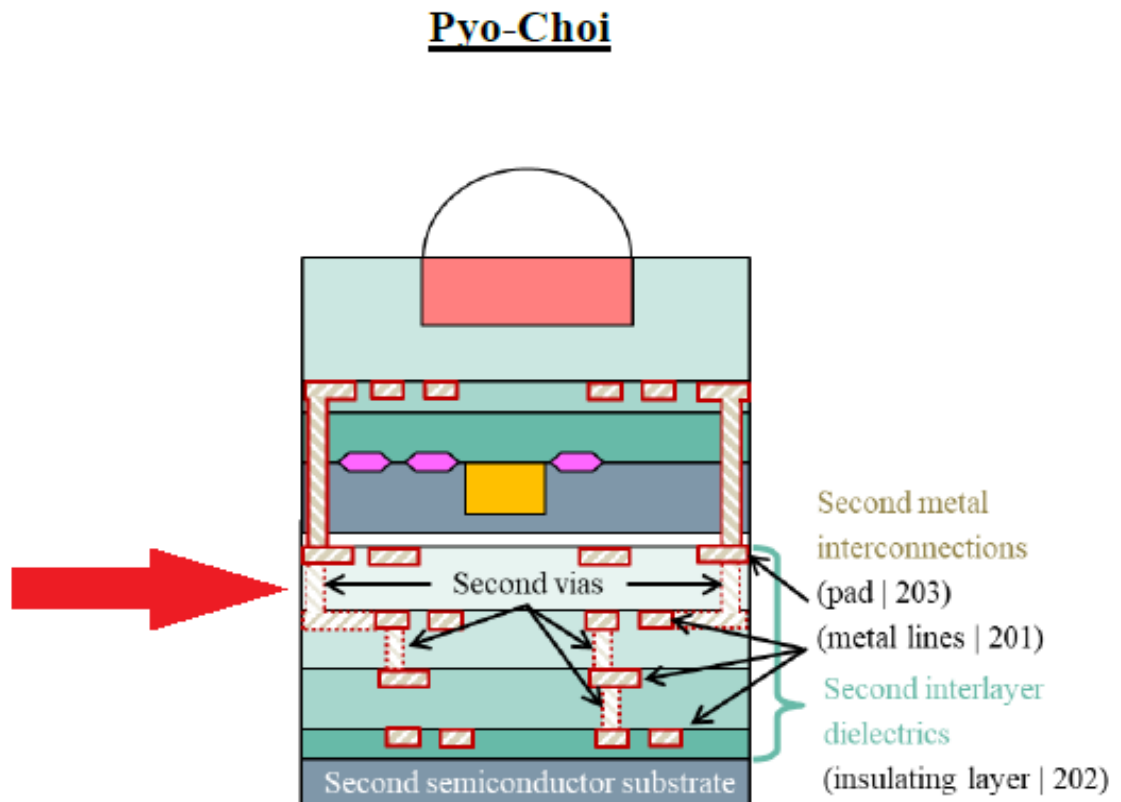


‘366 Patent Fig. 8 (colorized)

This comports with the natural plain-and-ordinary understanding of the term “penetrate,”—*i.e.*, a doctor’s needle penetrating a patient’s upper arm in the course of giving a flu shot. In contrast, the patient’s humerus—the upper arm bone—would not be considered (in the normal sense) to be “penetrating” the patient’s arm.

As discussed below, the Petition’s analysis of the claim elements overlooks the ‘366 patent’s use of the term “penetrating.” Not only does Petitioner never address this particular aspect of the claim language head-on, but Petitioner’s treatment of the term in connection with its “Pyo-Choi” combination drawing

(reproduced below) reflects its understanding that the alleged “second via” (see red arrow) is entirely internal to the identified second interlayer dielectric—i.e., Pyo’s “insulating layer 202”—terminating below Pyo’s “pad 203.” *See* Pet. 44.



As a result, Petitioner’s conclusory assertion that this specific claim language is met by Pyo is insufficient to prevail on at least Grounds 1 and 2.

Similarly, Petitioner’s failure to request a specific claim construction that would deviate from the term’s plain and ordinary meaning is a failure to follow the Board’s rules, which require that Petitioners set forth “how the challenged claim is

to be construed” and “how the construed claim is unpatentable.” 37 C.F.R.

§42.104(b)(3)-(4). The purpose of this Board’s rule is to prevent a party from engaging in gamesmanship and pursuing competing positions in both the IPR and in the underlying litigation.

V. ARGUMENT

The Petition should be denied for at least the following reasons:

(A) Grounds 1 and 2 should be denied because the proposed combinations, which are based on the Pyo reference, fail to disclose claim 1’s limitations of: (1) “a second via penetrating the second interlayer dielectric so that the second via is connected to the second metal interconnection”; and (2) “the first via being connected to the second via.”

(B) Grounds 3-6 should be denied because the proposed combinations, which are based on the Imaoka reference, fail to disclose claim 1’s limitations of: (1) “a first via” and “a second via”; and (2) “a first metal connection on the first interlayer dielectric.”

(C) The Board should exercise its discretion to deny this Petition because the same invalidity arguments will be addressed, and resolved, in the co-pending district court proceedings before the Board would issue a final written decision

here and because the Pyo reference, which Petitioner relied on for Grounds 1 and 2, was previously before the Examiner during prosecution.

A. GROUND 1 AND 2 FAIL TO DISCLOSE ALL ELEMENTS OF CLAIM 1

Grounds 1 and 2 should be denied because the proposed combinations, which are based on the Pyo reference, fail to disclose claim 1's limitations of: (1) "a second via penetrating the second interlayer dielectric so that the second via is connected to the second metal interconnection"; and (2) "the first via being connected to the second via."

1. GROUND 1 AND 2 FAIL TO DISCLOSE "A SECOND VIA PENETRATING THE SECOND INTERLAYER DIELECTRIC"

Claim 1 of the '366 patent recites "a second via penetrating the second interlayer dielectric so that the second via is connected to the second metal interconnection."

a. PYO DOES NOT DISCLOSE A "SECOND VIA"

As an initial matter, the Petition has repeatedly acknowledged that a via refers to a via hole and conductive material therein, and not merely to the conductive material: A "*via is a hole filled with a metal plug* to 'form an electrical pathway' from one metal layer to another." Pet. 18. The Petition again states:

“Next, trenches and *holes* (*‘vias’*) are filled with copper.” *Id.*, 27 (quoting Guidash, ¶169). The art references provided by Petitioner confirm this definition. *See, e.g.*, Brase (Ex. 1009), 1:40-45: “*vias are holes*, typically extending normal to the surface, that are patterned to connect the metal lines from layer to layer.”

Despite its own definition and usage of via to include both a via hole and conductive material therein, the Petition has later changed course to assert that a via means an electrical connection, whether or not there is a via hole, i.e. that a via refers to only an electrical connection, and not the fact that a via hole is required. This change of course is in order to overcome the deficiencies in its proposed combination of Pyo and Choi. The Petition’s definition is quite incorrect as well as illogical and, as illustrated above, is belied by the Petition’s own earlier usage and definition.

In order to support its fit-the-present-argument definition of “via,” the Petition states that: “Claim 7 requires the ‘first via and the second via comprise the *same material*,’ meaning the via is the conductor, not the ‘via hole.’” Pet. 44 (emphasis in original). The Petition’s argument is logically flawed and is also contrary to common use of language and contrary to technical definition of “via” in the art. To state that the vias comprise the same material does not mean that the term “via” excludes the via hole. To the contrary, the via comprises both the

conductive material and the hole that has to exist to allow the conductive material to be situated therein. As such, a claim in a patent can call for two vias to comprise the same conductive material, without in any way meaning or implying that the vias do not comprise via holes in addition to the conductive material. The ‘366 patent has done the same, and has not changed the well-understood definition of via, that is that a via includes both a via hole and the conductive material therein, a definition that has been understood and acknowledged by Petitioner itself.

The Petition’s other purported support for its changed definition of “via” fares no better. The Petition states that: “And the specification describes vias providing electrical connections between layers. ‘366 patent, Abstract (‘first via being *electrically* connected to the second via’), 1:42-44 (similar), 2:65-3:4 (‘first semiconductor substrate 100 and the second semiconductor substrate 200 can be *electrically* connected together’).” Pet. 44 (emphases in original). The ‘336 patent states a truism that vias are used, among other reasons, for electrical connections. These statements in no way mean that a via refers *only* to the conductive material inside the via, and do not exclude the existence of a via hole that is a defining feature of a via.

In addition to the Petition's own earlier definition of the term "via," the following are merely a few examples of how the term via is commonly defined in the art to mean a via hole including the conductive material therein:

- (1) The "*Comprehensive Dictionary of Electrical Engineering*," CRC Press, 2nd ed., 2005, defines the term "**via**" as: "a **hole** in the insulator between two metal layers on a multilayer integrated circuit that is etched and **filled with a conducting material** so that the two metal layers are electrically connected." Ex. 2001 at 35.
- (2) The "*Dictionary of Electronics and Electrical Engineering*," Oxford University Press, 5th ed., 2018, defines the term "**via**" as: "A **plated hole** used to provide low-inductance connections on an integrated circuit." Ex. 2002 at 1.
- (3) A "*Tutorial on forming through-silicon vias*," Journal of Vacuum Science & Technology A, Volume 38, Issue 3, 2020, defines TSV [through-silicon via] as: "**a hole** in a silicon (Si) substrate that is **filled with a conducting material** to allow 3D electrical routing." Ex. 2003 at 3.

Thus, it is clear that the term "via" is a short-hand way of referring to both a via hole and conductive material therein.

With the above correct and common definition of via in mind, it is clear that Pyo does not discuss or show a second via. *Pyo merely shows and discusses “pads 203” and does not show or mention “a via” in relation to any interlayer dielectric of second semiconductor substrate 200.* Similarly, Choi is completely silent on a “second via” since Choi is a single-substrate reference and does not disclose a second semiconductor substrate.

Pyo’s recitation of the term “via” is limited to a single vague reference to “connecting portion 105”: “a super via process through the rear surface of the first substrate 100, a process of filling the same to form the connecting portion 105, and a process of grinding the rear surface of the first substrate 100 so that the connecting portion 105 protrudes.” Pyo, 6. Thus, Pyo’s mention of the term “via” is limited to *only one occurrence in first substrate 100* (and not second substrate 200). Pyo does not mention “via” in any other place or any other context.

Petitioner has stated that “the insulating layer (202)” in Pyo is the “second ILD” in the ‘366 patent. *See, e.g.,* Pet. 44 (“vias penetrate the insulating layer (202) (second ILD) to connect pads (203) ...”). Thus, as an initial matter, Pyo does not mention the term “via” nor does it show a via in reference to “insulator layer (202).”

The Petition itself acknowledges a clear distinction between a “pad” (such as pad 203 in Pyo) and a “via” (such as via 230 in the ‘366 patent): “POSAs would understand *‘metal lines 201’ and ‘pad 203’* as interconnections because ‘interconnection’ ‘describes the conductor materials, ... that *create the metal wiring* that carries electrical signals to different parts of the chip.” Pet. 40. The Petition further notes that: “*Metal lines 201 and pads 203 thus each are ‘interconnections.’*” Pet. 41 (quoting Guidash).

The Petition has in fact set forth a formal distinction between a “pad” and a “via” by the following definitions:

- “(i) *‘lines’ extending parallel to the chip’s top surface;*
- (ii) *‘vias’* that ‘form an electrical pathway’ from one metal layer to another (*i.e., perpendicular to the chip’s top surface*); and
- (iii) contacts (*a.k.a. pads*) *at the chip’s surface.*” Pet. 40-41 (quoting Guidash citing Quirk and Brase).

Thus, while pads are admittedly at the chip’s surface, exist in a single layer, and are analogous to metal lines that extend parallel to the chip’ top surface, also within a single layer, vias are perpendicular to the chip’s top surface.

Petitioner has not argued or suggested, as it cannot, that a pad is analogous to a via. Moreover, none of the art references relied upon suggests that

a pad is analogous to a via. In stark contrast, a via is commonly defined as “a *hole* in the insulator *between two metal layers* on a multilayer integrated circuit that is etched and *filled with a conducting material* so that the two metal layers are electrically connected.” See, e.g., *supra*, The “*Comprehensive Dictionary of Electrical Engineering*.”

In summary, Pyo illustrates a pad instead of a second via. Petitioner cannot propose, and has not proposed, that pad 203 is equivalent to the second via. Patent Owner submits that based on these facts alone, it should be determined that claim 1 is not obvious over Pyo in view of Choi.

Since Petitioner cannot argue that pad 203 is equivalent to a second via, it has improperly relied on its expert to fill gaps in what the prior art actually discloses, instead of relying on its expert to clarify technical matters. For example, Petitioner’s expert has manually inserted into Pyo’s drawings a “second via,” and has indirectly “connected” it to not only to the “first via,” but also to a “second metal interconnection,” without any supporting disclosure or suggestion by Pyo or Choi.⁴

⁴ Nevertheless, as discussed below, even the purported “second via,” manually inserted into Pyo, is not equivalent to second via 230 in the ‘366 patent.

For support for its manual insertion of a “second via” into Pyo’s drawings, Petitioner relies on its expert’s declaration. However, “because an *inter partes* review may only be requested ‘on the basis of prior art consisting of patents or printed publications,’ 35 U.S.C. §311(b), ***expert testimony cannot take the place of disclosure from patents or printed publications.*** In other words, ***expert testimony may explain ‘patents and printed publications,’ but is not a substitute for disclosure in a prior art reference itself.***” *Patent Trial and Appeal Board Consolidated Trial Practice Guide* (Nov. 2019) at 36. *See also Oakley, Inc. v. Sunglass Hut Int’l*, 316 F.3d 1331, 1343 (Fed. Cir. 2003) (explaining that unsupported expert testimony is “facially deficient”); *Monsanto Co. v. Pioneer Hi-Bred Int’l, Inc.*, IPR2013-00023, Paper 32 at 7-8 (PTAB Apr. 11, 2013) (denying institution of trial where petitioner’s expert’s opinions were unsupported).

There is no support in either Pyo or Choi for Petitioner’s expert to manually draw arbitrary boundary lines inside Pyo’s “insulating film 202” and add into Pyo’s drawings a “second via,” and have it “electrically connected” to the “first via” and also to a “second metal interconnection.” The expert has in effect asserted that several inserted and indirect interconnections and vias are sufficient to meet the claimed limitation of “the first via being connected to the second via.” *See* Pet. 48 (citing Guidash ¶221). However, this assertion does not provide a basis

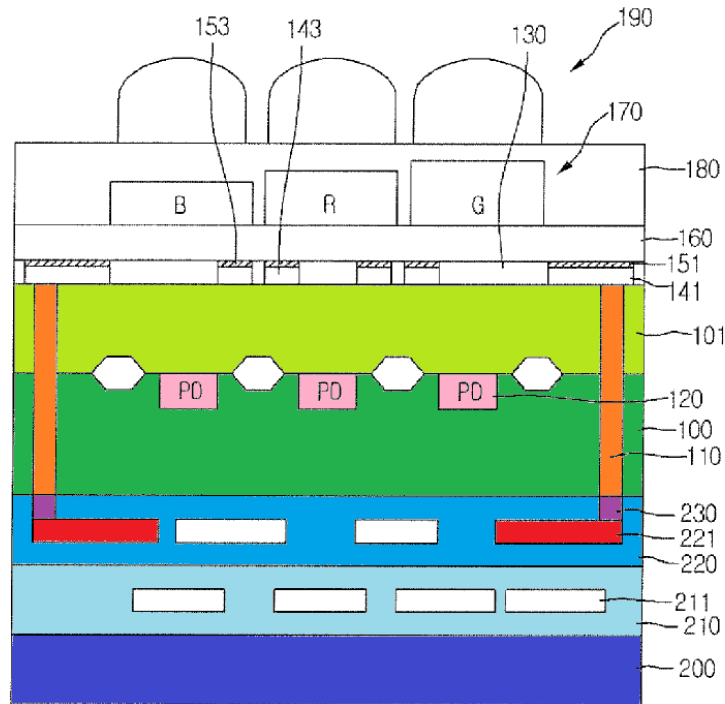
for the insertion of various interconnect lines and second vias and connecting them in the manner shown in the manually created “Pyo-Choi” drawing. *See, e.g.,* Pet. 48 (Pyo-Choi drawing in the upper right of the page). That is just speculation by Petitioner. That is legally wrong. *See Bettcher Indus., Inc. v. Bunzl USA, Inc.*, 661 F.3d 629, 640 (Fed. Cir. 2011) (“[T]he speculative notion that by happenstance the [prior art feature] might, under hypothetical circumstances, be capable of operating as [claimed] is an insufficient basis” for inherency).

As equally speculative approaches that are not set forth in the Petition, pad 203 in Pyo could have been connected to a resistive or an inductive element before being connected to a “second via.” As another speculative example, pad 203 could have been connected to “metal lines 201” by a direct capacitive connection, without a need to use a “second via” at all. However, Petitioner’s expert has avoided discussion of these other equally speculative approaches. Thus, Petitioner’s expert testimony has clearly exceeded its function to “explain the patents and printed publications,” and has substituted itself as a “disclosure in a prior art reference itself.”

b. PYO DOES NOT DISCLOSE “A SECOND VIA *PENETRATING* THE SECOND INTERLAYER DIELECTRIC”

Claim 1 element “a second via *penetrating* the second interlayer dielectric” uses the term “penetrating” in a manner consistent with its plain and ordinary meaning. For example, the ‘366 patent states that “[t]he first via 110 can be formed to *penetrate* through both the first semiconductor substrate 100 and a pre-metal dielectric (PMD) 101 formed on the first semiconductor substrate 100. That is, the first via 110 can be exposed at the bottom surface of the first semiconductor substrate 100.” ‘366 patent, 2:35-39. Elsewhere the ‘366 patent states that “the second via 230 can *penetrate* the third interlayer dielectric 220 [i.e., the “second interlayer dielectric” in claim 1] and be exposed.” *Id.*, 3:21-22.

The ‘366 patent explains that “[s]ince the second via 230 exposed in the top surface of the second semiconductor substrate 200 is disposed under the first via 110 exposed in the bottom surface of the first semiconductor substrate 100, the first semiconductor substrate 100 and the second semiconductor substrate 200 are electrically connected to each other.” *Id.* at 3:26-31. This relationship can be seen in Figure 8 (reproduced below), which shows both the first via (orange) and the second via (purple):



‘366 Patent Fig. 8 (colorized)

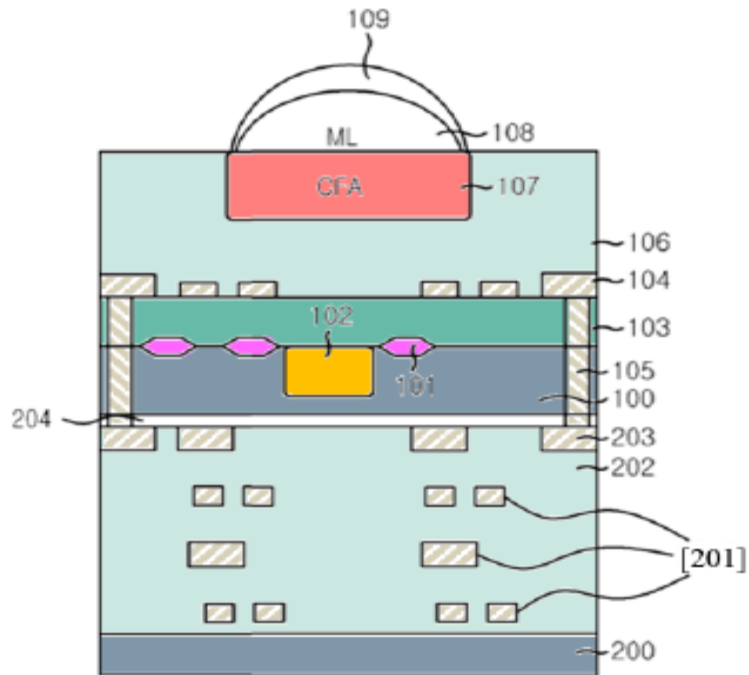
The notion that an object “penetrating” something would become exposed at that boundary—*i.e.*, break the surface—comports with the plain-and-ordinary understanding of the term “penetrate.” Common usage is replete with examples: a doctor’s needle *penetrating* a patient’s arm in the course of giving a shot; a bullet *penetrating* an armored plate or bullet-proof vest; or a humpback whale *penetrating* the surface of the ocean when it breaches.



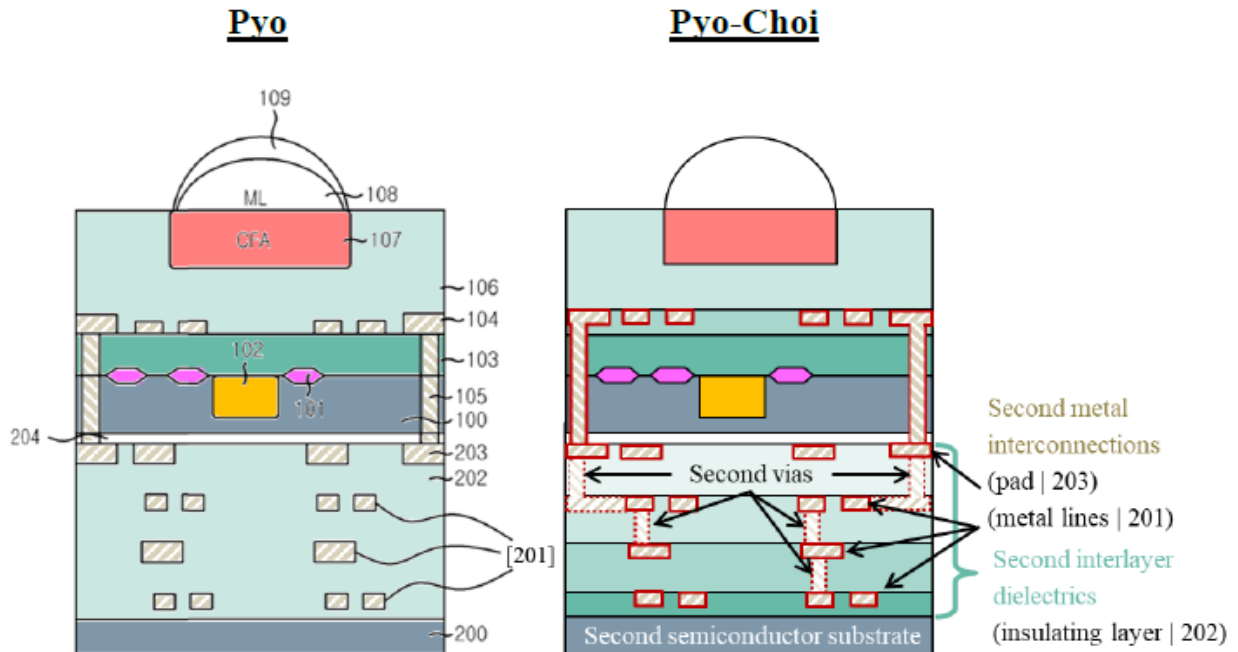
In contrast, Pyo does not show nor disclose a second via penetrating the second interlayer dielectric.

First, as effectively conceded by Petitioner, Pyo merely states that “pads 203 are connected to the plurality of metal lines 201.” *See* Pet. 43. Pyo does not disclose any via structure or provide any detail on how pads 203 are connected to the plurality of metal lines. Pyo’s limited disclosure is illustrated by its own Figure 3, which omits any relevant details showing any alleged second via:

Pyo



See Pet. 44 (colorizing Pyo's Figure 3). Instead, Petitioner modified Pyo to add detail that is not present to create what it calls the "Pyo-Choi" drawing:



See Pet. 44 (Petitioner’s “Pyo-Choi” drawing).

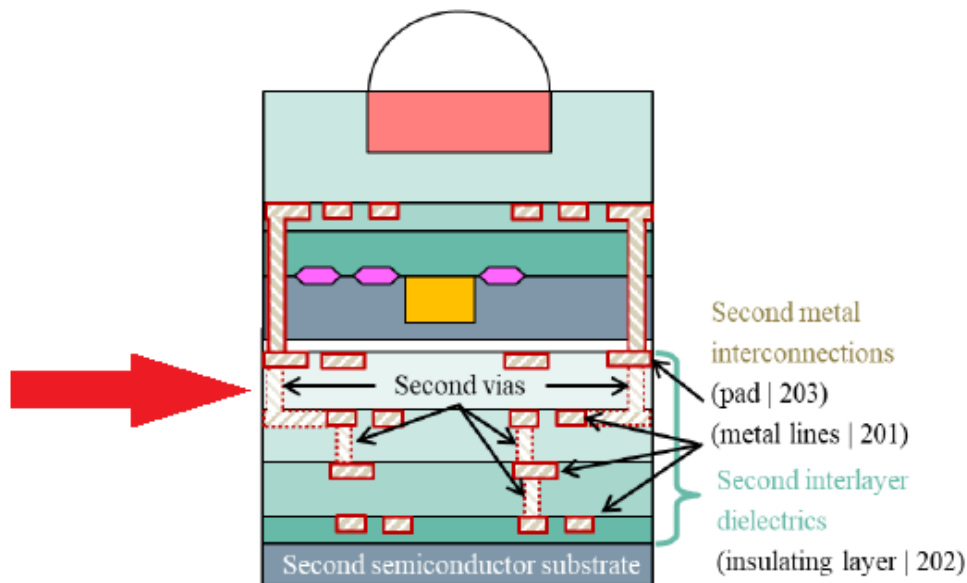
For example, despite vaguely identifying Pyo’s “insulating film 202” as the “second interlayer dielectric” required by the prior claim element, Petitioner proceeds to draw arbitrary boundary lines within that film to define “each level of the ‘insulating layer 202.’” Pet. 41. The arbitrary boundary lines are determined in a manner solely to aid Petitioner’s arguments. But there is no disclosure in *Pyo* that how “insulating film 202” is made of multiple layers, how many layers there are, or that how any such layers match the arbitrary boundary lines drawn by Petitioner. In other words, even if Petitioner is correct that “insulating film 202” is composed of multiple layers, there is nothing in *Pyo* that says whether metal lines

201 sit on top of the underlying layer or are instead etched into or embedded into that underlying layer.

Similarly, there is no disclosure of how pads 203 are connected to metal lines 201. Although, Petitioner adds two sets of dotted red lines to Pyo's Figure 3 in an attempt to illustrate two "second vias," there is nothing in Pyo that even suggests that Petitioner's modification is taught in the reference. For example, not only is Pyo silent on how pads 203 are connected to metal lines 201, but Pyo does not even specify which of the "pads 203" are connected to what "metal lines 201." Instead, despite Petitioner's attempt to illustrate a specific via connecting a specific pad 203, Pyo merely states that "pads 203 are connected to the plurality of metal lines 201." *See* Pet. 43; Pyo, 5.

Second, even if the Board were to credit Petitioner's additions to Pyo, the Petitioner ***still*** fails to establish that its modified Figure 3 shows "a second via ***penetrating*** the second interlayer dielectric so that the second via is connected to the second metal interconnection." As clearly shown in Petitioner's drawing, the alleged second via terminates beneath pad 203 and does not penetrate the identified second interlayer dielectric ("insulating film 202") (see red arrow):

Pyo-Choi



See Pet. 44 (Petitioner’s “Pyo-Choi” drawing).

As alluded to above, Petitioner’s argument is akin to saying that a bullet has “penetrated” an armored plate even if it is stopped by another layer. But even under Petitioner’s own reading of Pyo, it would—at best—only disclose the use of the intervening pad 203 (not a second via) to penetrate the second interlayer dielectric and indirectly connect a first and a second via. Accordingly, Petitioner’s reliance on Pyo is misplaced.

Patent Owner further notes that the Petition does not rely on either Choi or Dublin to supply this missing limitation. Instead, Petitioner states that “[t]he

modification of Pyo would leave these aspects unchanged.” Pet. 44-45. As a result, neither Ground 1 nor Ground 2 discloses every element of independent claim 1. For this reason, the Board should deny the Petition’s first two grounds.

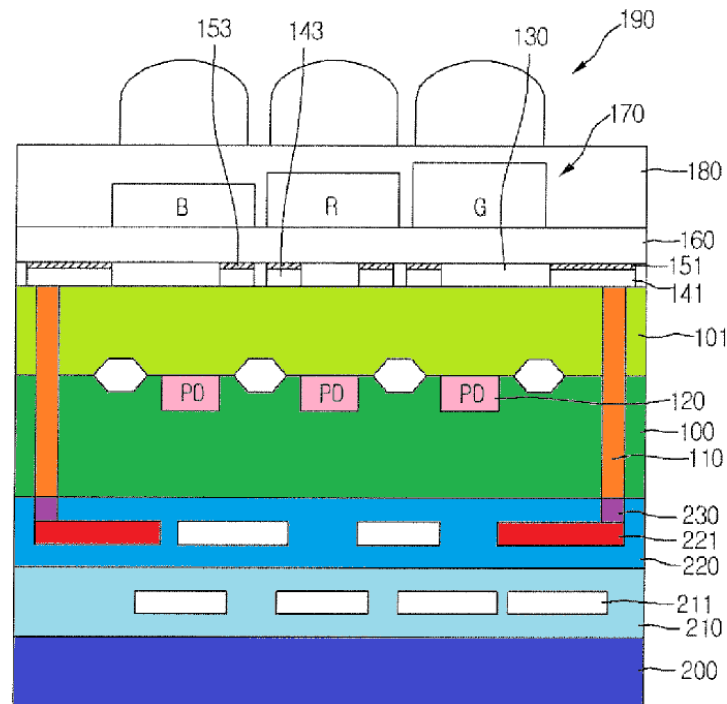
2. GROUNDS 1 AND 2 FAIL TO DISCLOSE “THE FIRST VIA BEING CONNECTED TO THE SECOND VIA”

Claim 1 of the ‘366 patent recites “*a second via penetrating the second interlayer dielectric,*” and it further recites “*a first via penetrating the pre-metal dielectric and the first semiconductor substrate, the first via being connected to the second via.*” The ‘366 patent’s use of the term “penetrating” in reference to the first and second vias implicitly involves a direct connection of the vias. As stated in the patent: “[i]n one embodiment, the second via 230 can penetrate the third interlayer dielectric 220 and be exposed” (‘366 patent, 3:21-22) and that “[s]ince the second via 230 exposed in the top surface of the second semiconductor substrate 200 is disposed under the first via 110 exposed in the bottom surface of the first semiconductor substrate 100, the first semiconductor substrate 100 and the second semiconductor substrate 200 are electrically connected to each other.” *Id.*, 3:26-31.

Because this embodiment results in *two penetrating vias*, the vias are physically connected to each other rather than connected through various paths or

structures. In other words, since both the first and second vias penetrate through, there is no intervening material left between the two vias to interfere with or inhibit a physical connection between them.

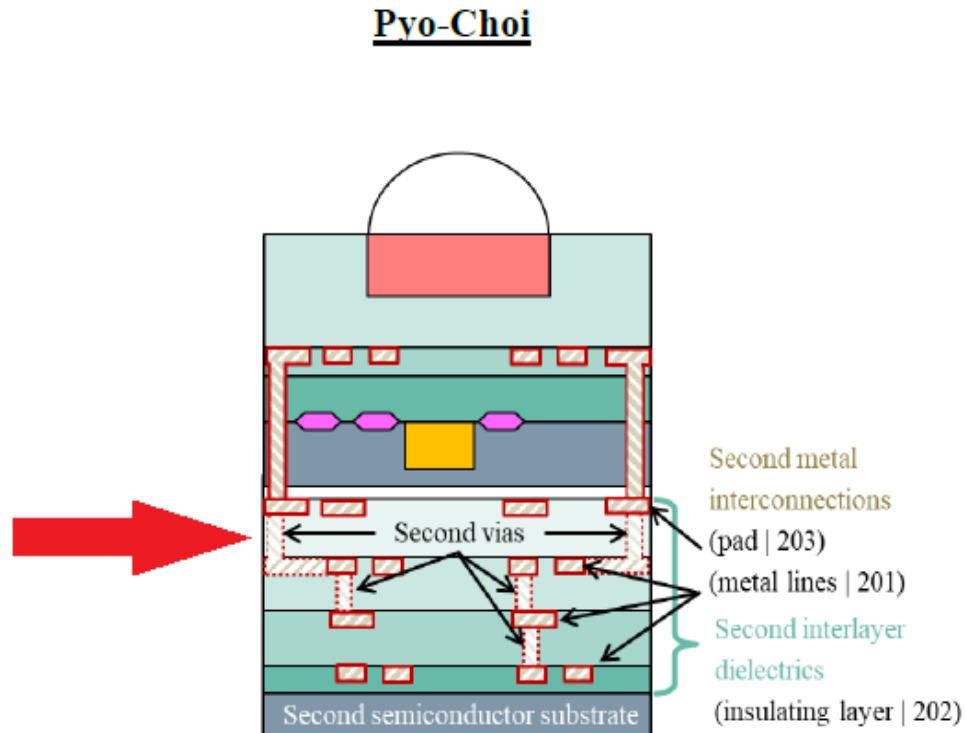
This relationship between the first via (orange) and the second via (purple) can be seen in the '366 patent:



'366 Patent Fig. 8 (colorized)

However, just as Pyo's pad 203 poses a problem for the claim element "***second via penetrating*** the second interlayer dielectric," it poses a similar problem for the subsequent element "a first via penetrating the pre-metal dielectric and the first semiconductor substrate, ***the first via being connected to the second***

via.” Namely, even in Petitioner’s modified version of Figure 3, Pyo clearly discloses an intervening pad 203 such that the vias are not connected (see red arrow):



See Pet. 44 (Petitioner’s “Pyo-Choi” drawing).

Not only is this inconsistent with the claim language, but the use of an intervening pad to make a connection between the two substrates is inconsistent with the goals of reducing costly fabrication steps and maximizing the use of available real estate in a chip.

Significantly, there is no description anywhere in the ‘366 patent as to how to electrically connect first via 110 and second via 230 without a physical connection of the two vias, and Figure 8 of the ‘366 patent (above) illustrates this physical connection between first via 110 and second via 230. Petitioner’s logic in adding the term “electrical” to the claim is faulty. The Petition states that “POSAs would understand ‘connected’ encompasses electrical connections as the ‘366 patent itself discloses. Guidash, ¶221 (citing ‘366 patent, Abstract (‘the first via being *electrically connected* to the second via’), 1:42-44 (‘first via ... to *electrically connect* with the second via’), 2:65-3:4 (similar)).” Pet. 48. Of course, since the ‘366 patent discloses the first and second vias as being physically connected, they are also electrically connected. Being electrically connected does not mean that the connection is not a direct one. As such, the quoted portions of the ‘366 patent simply state a truism, that is the two vias are electrically connected. Indeed, the quoted portions of the ‘366 patent actually point to a distinction being drawn by the patent in excluding the term “electrically” from claim 1 while maintaining the term “connected.”

To try to overcome the fact that a combination of Pyo and Choi does not disclose or suggest a second via in a second ILD that is physically connected to a first via in a first semiconductor substrate, the Petition makes an incomprehensible

statement that, according to the ‘366 patent, “one embodiment connects vias ‘using polymer,’ *meaning they would not physically touch* – permitting only an electrical connection.” Pet. 48-49 (underlined emphasis in original).

First, the referenced portion of the ‘366 patent that the Petition has twisted out of shape states in full: “In an embodiment, *the first semiconductor substrate 100 and the second semiconductor substrate 200 can be electrically connected to each other using polymer such as polyimide or benzocyclobutene.*” ‘366 patent, 7:5-8. There is no logical connection between this quoted portion and the asserted conclusion that the first and second vias “would not physically touch.” And there is certainly no mention of “connect[ing] vias ‘using polymer’” as inexplicably proclaimed by the Petition and repeated by Petitioner’s expert (Guidash ¶221).

Second, the only other place where the term “polymer” appears in the ‘366 patent is in method claim 19, which claims in relevant part: “bonding the first semiconductor substrate and the second semiconductor substrate together by performing a *polymer bonding*, a silicon fusion bonding, a copper-to-copper bonding, or an eutectic bonding.” It is amply clear that “polymer” is one of the options used for bonding the two semiconductor substrates.

In fact, using polymer in bonding semiconductor substrates 100 and 200 emphasizes the need for the first and second vias to pierce through the layer of

intervening polymer utilized for bonding in order for the two vias to physically touch and connect to each other. If the first and second vias did not physically touch, as the Petition appears to vaguely propose, the two vias would not be electrically connected due to the intervening polymer and, further, no indirect electrical connection for the two vias is described in the detailed description or shown in the drawings. Thus, the term “connected” in claim 1 of the ‘366 patent would be devoid of meaning when the two vias do not physically touch.

Patent Owner notes that the Petition does not rely on either Choi or Dublin to supply the missing claim limitation “the first via being connected to the second via.” Instead, Petitioner states that “[t]hese aspects of Pyo would remain unchanged after the above-discussed modifications elsewhere in the sensor.” Pet. 48-49. As a result, neither Ground 1 nor Ground 2 discloses every element of independent claim 1. For this reason, the Board should deny the Petition’s first two grounds.

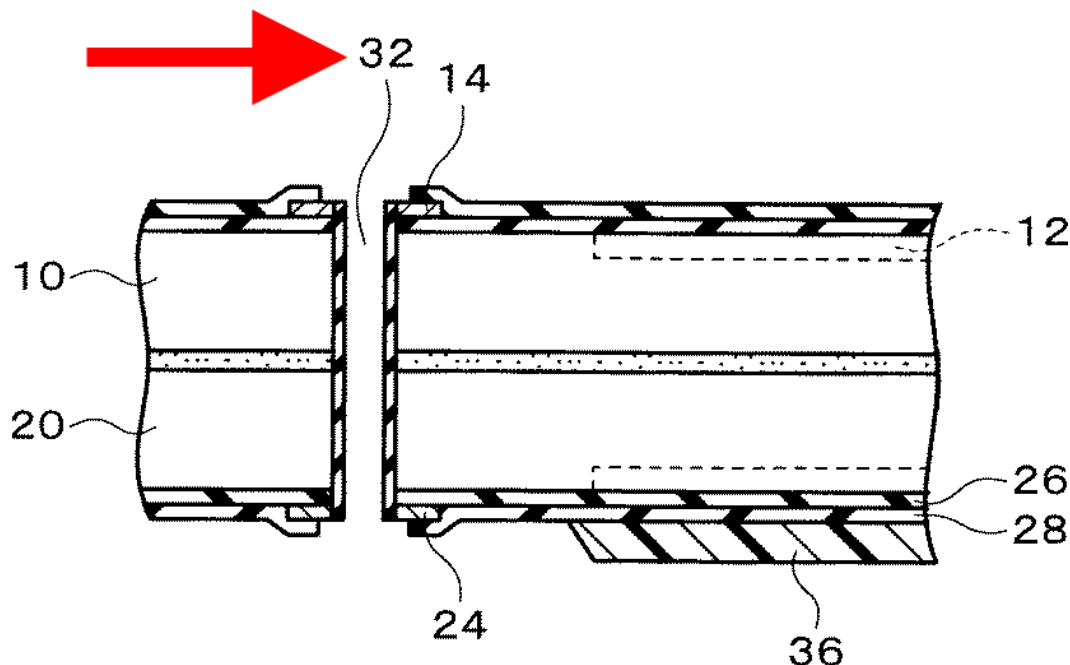
B. GROUNDS 3-6 FAIL TO DISCLOSE ALL ELEMENTS OF CLAIM 1

Grounds 3-6 should be denied because the proposed combinations, which are based on the Imaoka reference, fail to disclose claim 1’s limitations of: (1) “a

first via” and “a second via;” and (2) “a first metal interconnection on the first interlayer dielectric.”

1. GROUNDS 3-6 FAIL TO DISCLOSE “A FIRST VIA” AND “A SECOND VIA”

Claim 1 of the ‘366 patent recites “a first via” and “a second via.” With respect to these elements, Petitioner concedes that “Imaoka discloses only a single part 38 to connect the first and second substrates.” Pet. 64. Specifically, Imaoka states that “[a] through-hole 32 is formed in the first and second semiconductor substrates” and that “[i]n particular, the through-hole 32 extends continuously (integrally) through the first and second semiconductor substrates.” Imaoka, [0016]. This is shown, for example, in Figure 6(A) of Imaoka:



Imaoka, Figure 6(A)

Subsequently, “[a] conductive part 38 is formed inside the through-hole 32.”

Id. As a result, Imaoka’s process of creating a single through-hole discloses, at most, one via running through the two substrates.

Nonetheless, Petitioner bases Grounds 3-6 on its “assum[ption] that a single via may meet both first and second vias.” *Id.*, 65. Petitioner’s argument with respect to these grounds is fatally flawed for multiple reasons.

First, as a procedural matter, Petitioner does not even try to support a claim construction that would allow for a single through-hole to create two vias.

However, in situations where a petitioner is departing from the plain and ordinary meaning of a term, the PTAB rules require that the petition sets forth how the challenged claim is to be construed and how the construed claim is unpatentable.

The purpose of this rule is to prevent gamesmanship whereby a petitioner raises one construction in the IPR and a conflicting construction in a related litigation.

But here, it appears that Petitioner intends to do just that by “reserving its right to challenge” the very construction that it seeks to advance in its Petition. *See* Pet. 65.

The Board has previously recognized that such gamesmanship cannot result in a reasonable likelihood of success in challenging the patented claims. *See, e.g.,*

Orthopediatrics Corp. v. K2M Inc., IPR2018-01546, Paper 10 at 10-12 (PTAB Feb. 14, 2019) (“Petitioner’s failure to provide a claim construction is...further compounded by the fact that Petitioner takes an inconsistent position before the District Court ... By failing to reconcile its proffered claim construction here with its very different construction proffered in District Court ... Petitioner fails to satisfy [its] burden”); *Samsung Elecs. Co., Ltd. v. Ancora Techs., Inc.*, IPR2020-01184, Paper 11 at 27 (PTAB Jan. 5, 2021) (“Significantly, Petitioner’s [claim construction] argument...seems to be inconsistent with its position advanced in the parallel litigation and the Federal Circuit’s interpretation.”).

Petitioner’s argument raises the specter that this Board will make a legal ruling that is inconsistent with the claim construction ruling that Petitioner will seek and could receive from the district court. *See KioSoft Tech. LLC v. PayRange Inc.*, CBM2020-00026, Paper 11 at 17 (PTAB Mar. 22, 2021) (“If we were to adopt Petitioner’s claim construction as presented in the Petition, and if the district court were to adopt Petitioner’s claim constructions as proposed there, the subsequent decisions issued in reliance on these inconsistent claim constructions may lack ‘uniformity’ between us and the district court and may undermine the ‘predictability’ of the [] patent’s claim scope and the ‘integrity of the patent system’ overall.”). For at least this reason, the Petition should be denied.

Second, Petitioner’s attempt to shift the blame for its own gamesmanship onto Patent Owner is undermined by its own Petition. Although Petitioner claims that its interpretation of “via” is motivated by Patent Owner’s infringement contentions in the underlying litigation, Petitioner provides the Board with only a partial and misleading view of the issue.

Patent Owner is ***not*** claiming that a “single thru-silicon via”—as suggested by Petitioner—satisfies both the first and second vias of claim 1. *See* Pet. 64. Indeed, Petitioner’s screenshot of Patent Owner’s infringement contentions is shockingly duplicitous. Specifically, the red text to the left of the image (fully reproduced below) was ***added by Petitioner***, a fact that Petitioner deliberately failed to disclose to the Board:

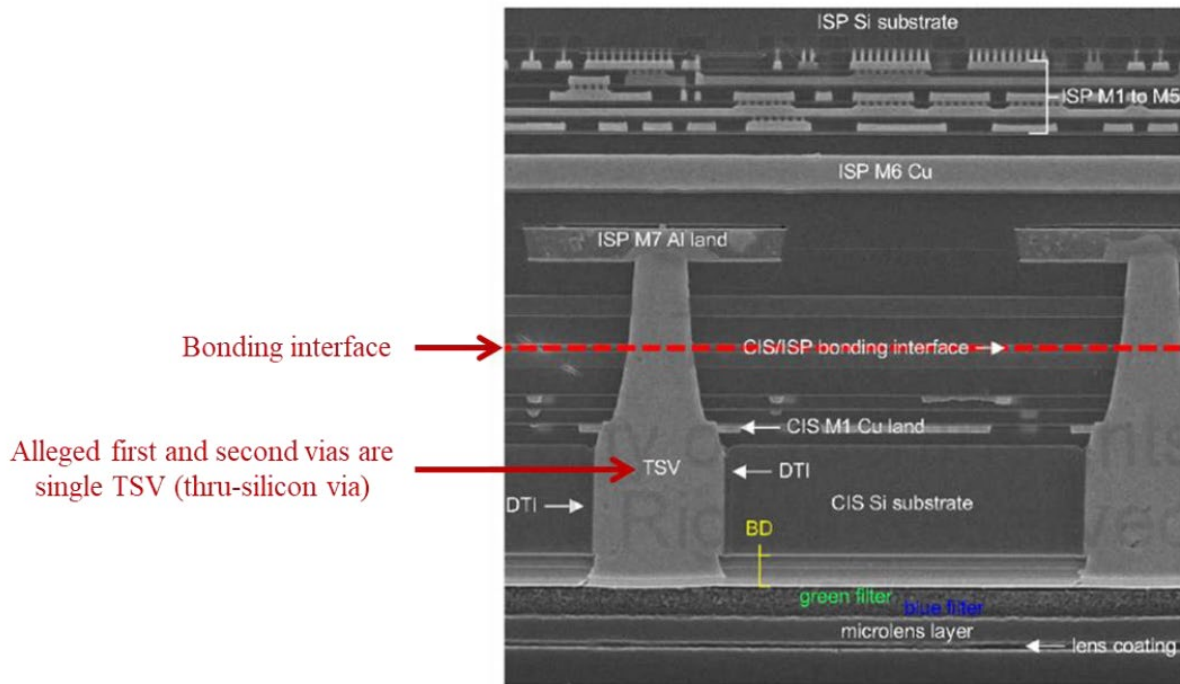


Figure 6

See Pet. 65 (citing Figure 6 from Ex. 1021). As clearly evidenced in the cited passages of Patent Owner’s Complaint (Ex. 1021), Patent Owner makes no assertion that a “single thru-silicon via” satisfies the claim language, and the paragraph immediately below the cited figure explicitly states that the Sony “CIS and ISP dies are electrically connected by two vias corresponding to two distinct holes.” See Ex. 1021 at ¶65 and Figures 6 and 7.

Indeed, nowhere in Patent Owner’s contentions does it claim that only a “single thru-silicon via” satisfies both the first and second vias of claim 1. Rather, what Petitioner fails to explain to the Board is that in manufacturing the accused

sensors, it etches two different via profiles in connecting the ISP and CIS chips. Petitioner's *own* cited references recognize that a via, logically, is defined in part by the hole created: "*a via is a hole* filled with a metal plug to form an electrical pathway from one metal layer to another." Pet. at 18 (citing Quirk). Similarly, Petitioner itself states that "trenches and *holes ('vias')* are filled with copper." Pet. 27 (quoting Guidash, ¶169). Those statements, combined with Petitioner's knowledge of its own manufacturing process, make its mischaracterization of Patent Owner's infringement theory a transparent attempt to game the IPR process.

Third, as a matter of logic, the single "through-hole 32" and its "conductive part 38" cannot meet claim 1's requirement of a first and second via. Indeed, it is a basic tenet of Patent Law that different terms refer to different parts of the claimed invention. If the Applicant intended for the second via to refer to the first via, the Applicant would have used one term and referred back to that term with the proper antecedent basis. Similarly, claim 1 elsewhere recites "the first via being connected to the second via," which would become meaningless if the first via and second via were both met by a single via. As a result, as effectively conceded by Petitioner, Imaoka does not disclose the required elements of claim 1.

Petitioner's half-hearted reliance on Imaoka is a transparent attempt to effectively pursue two competing claim constructions in both the IPR process and

the underlying litigation. In doing so, Petitioner is seeking facially inconsistent results: an excessively broad construction for its invalidity challenge and a narrower construction for purposes of infringement. But this is exactly why the PTAB rules require a Petitioner in such circumstances to affirmatively stake out a position on claim construction. For the above reasons, the Board should reject Petitioner's reliance on Imaoka to satisfy the first and second via limitations.

Fourth, Petitioner cannot fix Imaoka's lack of disclosure by combining it with Choi. Imaoka is about fabricating a single through-hole in two semiconductor substrates, without any suggestion as to the possibility of fabricating a first via and a second via. Choi is a single-substrate device that does not disclose a "second via" as it lacks a second substrate (as a result, Choi does not disclose a number of other claim 1 elements). The proposed combination of Choi and Imaoka results in several inexplicable incongruities which point to fundamental deficiencies in any purported combination of Imaoka with Choi. As discussed below, POSAs would not have a reason or motivation to combine Imaoka with Choi.

Petitioner states that "POSAs would have had reason to pick copper instead of aluminum for pad 14 given its lower resistivity, reduced power consumption, resistance to electromigration, and tighter packing density." Pet. 78. However, realizing that to "pick copper instead of aluminum" would result in a problem for

semiconductor substrate 20 in that it “would have required removing or modifying Imaoka’s resin layer (36) to apply Choi’s copper interconnection process and in particular Choi’s planarization step” (Pet. 78), the Petition envisions a completely different scheme for Imaoka by using copper in semiconductor substrate 10, but using aluminum in semiconductor substrate 20.

Petitioner states that “[t]he combination of the ease of fabricating narrow copper interconnects and the difficulty of fabricating aluminum interconnects of the same dimensions meant that *nearly all high performance logic devices have made the transition to copper*, as of 2004.” Guidash, ¶56. However, according to the Petition, even though copper would have all the purported advantages listed in the Petition (Pet. 78 and Guidash, ¶¶55-56), POSAs would choose to use copper for semiconductor substrate 10, *but not for semiconductor substrate 20*.

The Petition proposes an enigmatic use of copper in Imaoka for only the upper half of the device, i.e. substrate 10, while maintaining aluminum for the lower half of the device, i.e. substrate 20, even though according to Petitioner copper offers “ease of fabricating” and there is “difficulty [in] fabricating aluminum interconnects.” Thus, POSAs would have to employ separate and additional manufacturing chambers and different etchants and use different process

recipes and fabrication steps for using copper in the upper substrate while using aluminum in the lower substrate.

Furthermore, conductive part 38 that is disclosed as one contiguous conductive material in Imaoka, would be split in the middle of through-hole 32 such that it would consist of copper in semiconductor substrate 10 and aluminum in semiconductor substrate 20.

In addition, Petitioner would strategically alter the fabrication process of Imaoka without citing any reason or motivation: ***Imaoka discloses bonding the two semiconductor substrates first and then making a single through-hole 32.*** See Imaoka, Figs. 5A-5B. Single-through hole 32 is filled in with conductive part 38 ***after the bonding*** of the two semiconductor substrates. See *id.*, Fig. 6C. Further, according to Imaoka, many of the remaining dielectric and interconnect layers are fabricated after bonding the two semiconductor substrates. See *id.*, Figs. 5B-5C, 6A-6C, and 7A-7B.

Perplexingly, the Petition proposes a complete strategic reversal of Imaoka's disclosure. The Petition proposes making semiconductor substrate 10 using copper interconnect and using copper in a "first via" ***and separately making*** semiconductor substrate 20 using aluminum interconnect and using aluminum in a "second via." ***After*** the two vias are already in place and already filled in with

conductive materials, the Petition proposes ***bonding the two semiconductor substrates and the first and second vias***. See Pet. 83 and the drawings therein. Thus, instead of first bonding the two substrates, then making a single uniform through-hole and then filling the uniform single hole with conductive material, Petitioner proposes a complete departure from Imaoka by first making via holes in two separate substrates, separately filling each via hole with conductive material, and thereafter bonding the two substrates and the two vias.

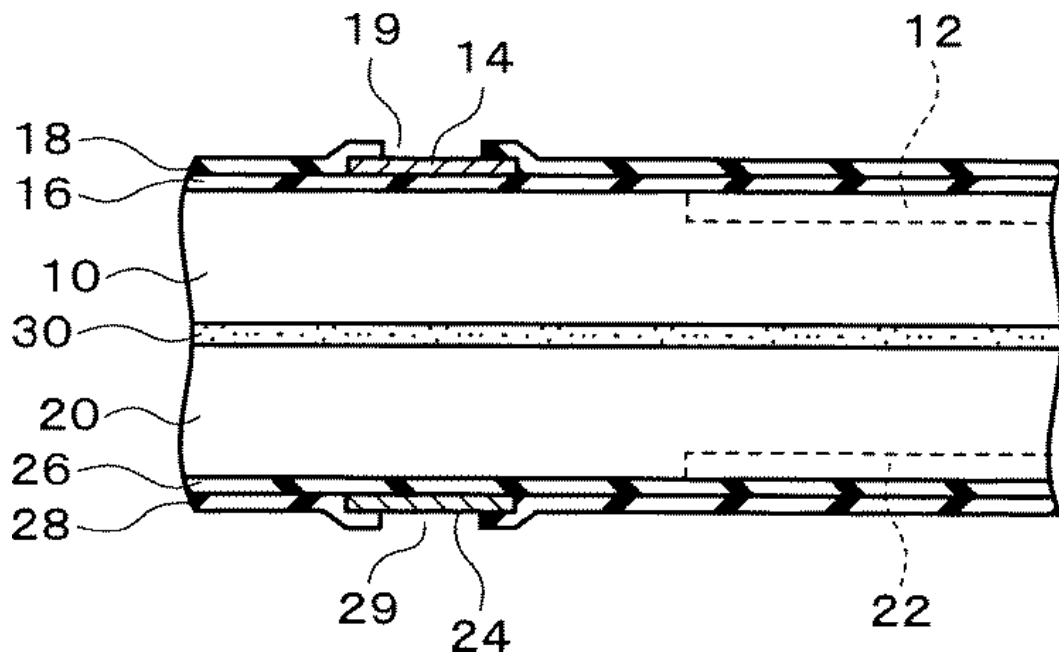
In addition, the Petition assumes that the numerous additional steps for bonding two completed semiconductor substrates would not dissuade the POSAs. For example, the Petition casually states that “POSAs would ***thin the back side of the substrate*** to expose the via for connection to the via in the second substrate.” Guidash, ¶302. However, the Petition does not provide a reason or motivation for applying such additional step to Imaoka’s process.

With respect to the first and second vias, Petitioner puzzlingly claims that “POSAs would have understood ***a straightforward way*** of fabricating pads 14 from copper without altering the structure of the second substrate would be to fabricate the interconnections on two substrates first, then bond them together afterward.” Pet. 79. However, nowhere in Petitioner’s conclusory assertion is there any disclosure of such a “straightforward way” in Imaoka or Choi. Indeed,

Petitioner does not appear to even rely on Imaoka or Choi for disclosing this alleged “straightforward” manufacturing process. *See id.*, 79-83.

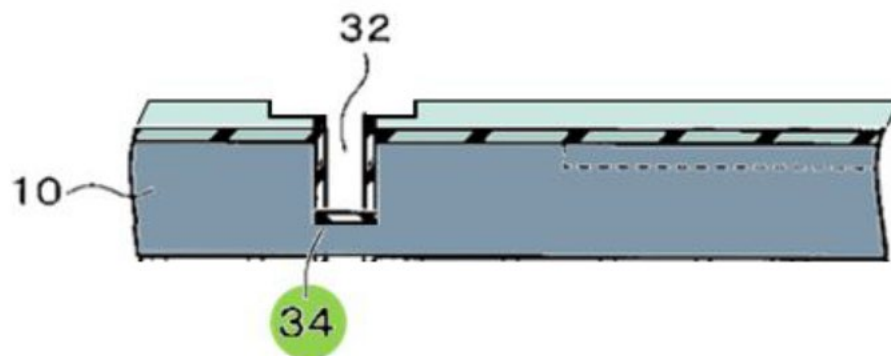
Even worse, according to the Petitioner itself, this “straightforward way” of modifying Imaoka is comprised of no less than eight major steps, most of which diverge from Imaoka’s actual teachings. *See id.* For example, with respect to “step b” of this modified process, Petitioner claims that “POSAs would have next deposited an ILD layer and etched it to form trenches for pad 14 and a hole 32 for part 38.” *Id.*, 80. But in Imaoka, there is no disclosure of etching to form pad 14 and, as noted above, POSAs would have no reason or motivation to combine with Choi.

Instead, Imaoka simply states that “a passivation film 16 is formed on a surface of the first semiconductor substrate 10 on which the first integrated circuit is formed, and the first pad 14 is formed thereon.” Imaoka, [0036]. This is shown, for example, in Figure 5(A) of Imaoka:



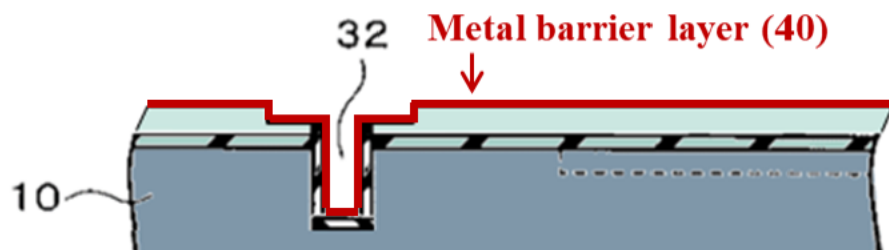
Imaoka, Figure 5(A)

Similarly, for “step c” of Petitioner’s modified process, Petitioner claims that “POSAs would have next fabricated an ‘insulating layer 34’ inside the hole [32].” Pet. 80. But there is no disclosure in Imaoka of how to deposit Petitioner’s illustrated insulating layer inside Petitioner’s trench/hole structure, which as shown below does not extend through the entire substrate:



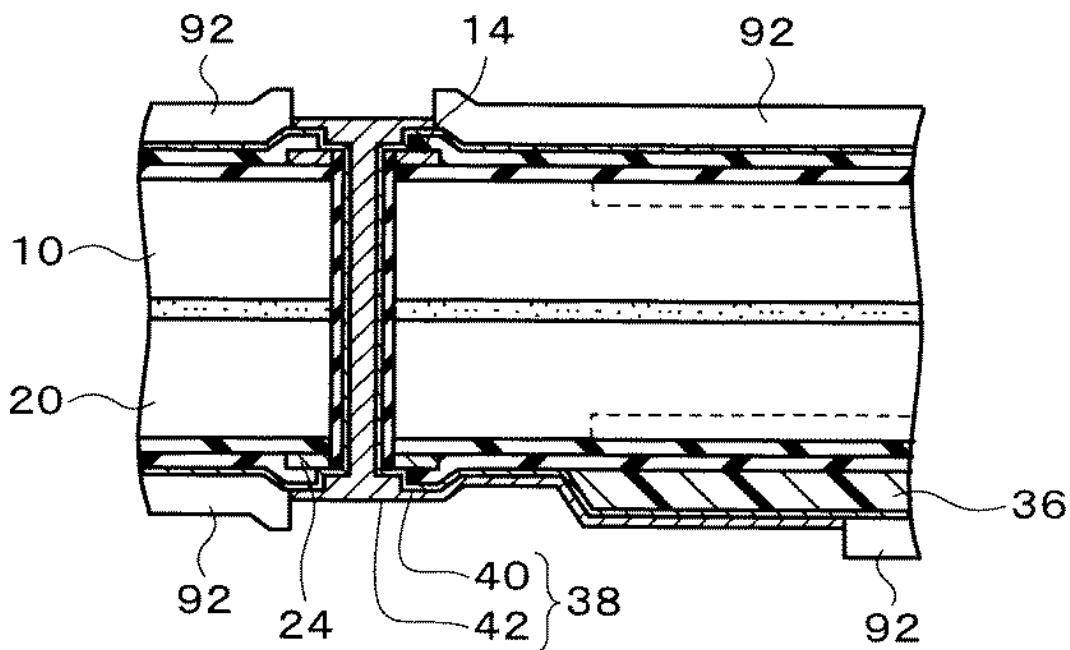
See Pet. 80. Instead, Imaoka only discloses depositing an insulating layer 34 inside through-hole 32 and states that it is “formed so as to not clog the through-hole 32.” Imaoka, [0038]. Petitioner fails to explain how a process that is taught not to clog a through-hole can be applied to suitably coat (and clog) the bottom of Petitioner’s trench/hole structure, or how this Imaoka’s process can be combined with Choi’s process, especially in the absence of a reason or motivation for a combination with Choi.

The same problem applies equally to Petitioner’s “step d” in which the modified trench/hole structure is then filled with a “metal barrier layer (40).” Pet. 81. Petitioner ignores the fact that Imaoka does not disclose this step, and in contrast, explicitly cautions that “conductive layer 40 is set up so as not to bury the inside of the through-hole 32.” *Id.*, [0041].



See Pet. 81. As a result, Petitioner’s unsupported “step d” is explicitly warned against by Imaoka.

Petitioner’s “step f”—which involves polishing copper layer 42—also has no connection with Imaoka. For this step, Petitioner relies on Choi and Yun, which states that “excessive polishing is performed so that the copper layer 313 and the third barrier layer 312 filled in the upper trench are recessed.” Pet. 81. In contrast, Imaoka uses photoresist layer 92 to pattern the second conductive layer 42 without any reference to or use of a polishing step. *See* Figure 6(C) below:



Imaoka, Fig. 6(C)

Id., [0042] (“[a]s shown in Fig. 6(C), a photoresist layer 92 for patterning the second conductive layer 42 may be formed” and “a conductive material is supplied to an opening part of the photoresist layer 92 to from the second conductive layer

42”). Moreover, as with the other steps, there is no reason or motivation to combine with Choi.

Petitioner then compounds its error in “step g” by claiming that “POSAs would thin the back side of the substrate to expose the via for connection to the via in the second substrate.” Pet. 82. Recognizing that there is no such disclosure in Imaoka or Choi, Petitioner cites to yet another different reference: Pyo. But as explained above, Pyo does not disclose “expos[ing] the via for connection to the via in the second substrate” as claimed by Petitioner. There is no disclosure in Pyo of the “penetrating” language required by the challenged claims.

Additionally, Petitioner’s stated bases for Grounds 3-6 were that the challenged claims were anticipated by Imaoka or obvious in view of Imaoka and Choi.⁵ Petitioner’s efforts to ignore the deficiencies in Imaoka and Choi by trying to cobble together disparate passages from multiple other references improperly turns its Petition into a futile game of whack-a-mole. Petitioner’s argument is that the challenged claims are invalid in view of Imaoka and Choi, only if you look—in

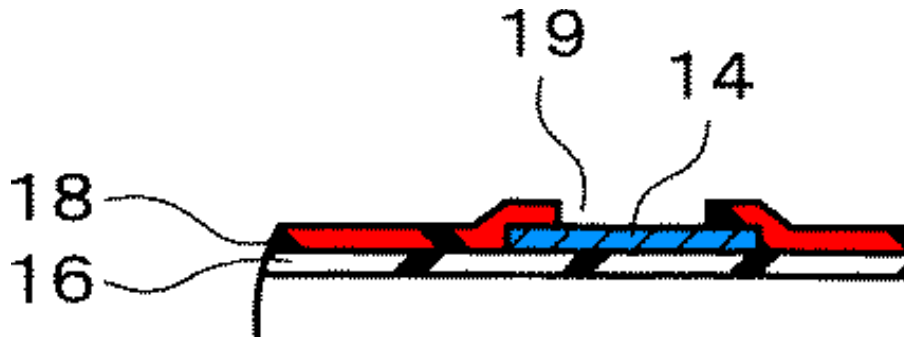
⁵ For Grounds 4 and 6, Petitioner combines Imaoka and/or Choi with Dublin for purposes of dependent claim 3. Petitioner does not purport to rely on Dublin to cure the above deficiencies in Grounds 3 and 5. *See* Pet. 76-77 and 95-96.

hindsight—to a variety of *other* references to piece together a specific CMOS sensor design that did not exist in the prior art. That formulation cannot legitimately form the basis for an invalidity challenge and is contrary to what is required for a Petition, which must explicitly set forth its grounds for consideration.

Because the combination of Imaoka and Choi does not cure the deficiencies in Imaoka, Petitioner has no likelihood of success with respect to its Grounds 3-6.

2. GROUND 3-6 FAIL TO DISCLOSE “A FIRST METAL INTERCONNECTION ON THE FIRST INTERLAYER DIELECTRIC”

Claim 1 of the ‘366 patent recites “a first metal interconnection on the first interlayer dielectric.” With respect to this element, Petitioner identifies pad 14 as the metal interconnection and passivation film 18 as the interlayer dielectric. Pet. 70. However, according to Imaoka, passivation film 18 (red) is formed on pad 14 (blue), not vice versa: “the passivation film is formed by covering the surface of the first pad 14.” Imaoka, [0036]. This is shown below:

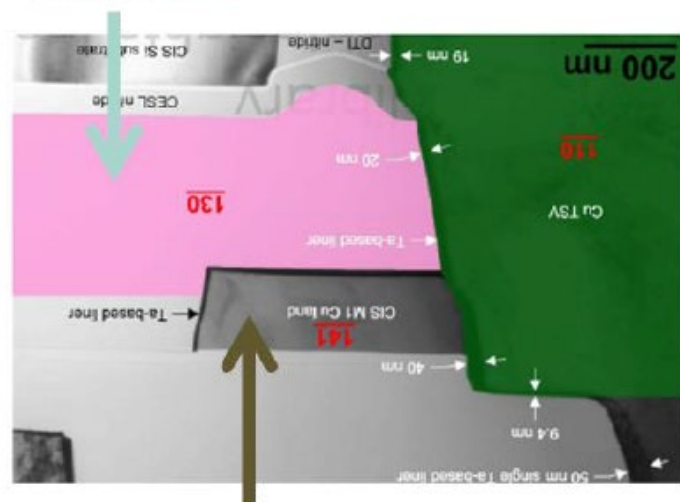


Imaoka, Fig. 5(A) (Colorized and Shown in Part)

As with some of its other positions, Petitioner seeks to pursue conflicting constructions in the IPR and litigation, using Patent Owner's contentions as an excuse for this gamesmanship. However, a cursory view of the Petition will show this to be misleading. Specifically, the screenshot from Patent Owner's contentions on the top right of Page 71 of the Petition has been flipped upside down (as evidenced by the upside-down letters and numbers):

Accused Product

First ILD



First metal interconnection

See Pet. 71.

Similarly, Petitioner has neglected to submit any evidence that the identified interlayer dielectric (part 130) is formed on the identified metal interconnection (part 141) in a manner equivalent to Imaoka. As a result, Petitioner's attempt to apply Patent Owner's contentions should not change the recited relationship between the first metal interconnection and the first interlayer dielectric. Because Imaoka does not disclose this element, Petitioner's reliance on this reference is misplaced.

Patent Owner further notes that the Petition does not actually rely on either Choi or Dublin to supply this missing limitation. Instead, Petitioner argues—as discussed above—that a POSA could have applied a “straightforward” 8-step modification to Imaoka in order to create two vias. As part of this complete rewrite of Imaoka, Petitioner claims that “POSAs would have next deposited an ILD layer and etched it to form trenches for pad 14” Pet. 80. But, as detailed above, Choi simply describes the use of a copper process and does not purport to provide a solution for combining two substrates.

When viewed as a whole, Petitioner is attempting to rewrite Imaoka to add structures—and problems—that simply do not exist in the reference in order to justify Grounds 4-6.

As detailed above, Petitioner has not shown that all of the elements of independent claim 1 are disclosed in any of its asserted Grounds. Accordingly, the Board should reject Petitioner’s arguments and deny institution.

C. THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION UNDER 35 U.S.C. §314(a)

As detailed below, the factors listed in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15, at 7-8 (May 13, 2020) (informative) favor discretionary denial under §314(a).

Factor 1: The “EDTX Proceeding” (*VisionX Tech., LLC. v. Sony et al.*, Case No. 2:22-cv-00178, filed May 26, 2022 (E.D. Tex.)) is ongoing in front of Magistrate Judge Payne in the Eastern District of Texas.⁶ Sony has not moved to stay the case pending the resolution of this IPR, nor is there evidence that such a stay would be granted. For example, in a recent denial issued by Judge Payne, the Court noted that the Supreme Court’s decision in *SAS Inst., Inc. v. Iancu*, 138 S.Ct. 1348 (2018), “precluded the PTAB from instituting only a portion of the patent claims, so any institution decision occurring after *SAS* provides a weaker inference that the PTAB will determine that all challenged claims are unpatentable.” *Peloton Interactive, Inc. v. Flywheel Sports, Inc.*, Case No. 2:18-cv-390, 2019 WL 3826051, at *2 (E.D. Tex. Aug. 14, 2019) (Payne, J.) (holding that “SAS alters the analysis and makes institution decisions less indicative that all claims will be found unpatentable”); *see also Arbor Global Strategies LLC v. Samsung Elec. Co., Ltd.*, Case No. 2:19-cv-333, 2020 WL 6305883, at *3 (E.D. Tex. Aug. 10, 2020) (Payne,

⁶ During the parties’ scheduling conference on September 26, 2022, the Sony Defendants and Patent Owner consented to trial before the Magistrate Judge, further increasing the likelihood that the EDTX Proceeding will reach trial before the Board issues any final written decision. Ex. 2004.

J.) (holding that a movant “may need to show that the Board is likely to invalidate every asserted claim—a showing that may require more than just pointing to a successful petition”).

Similarly, in evaluating motions to stay pending an IPR proceeding, Judge Payne also considers whether the Board has granted institution with respect to all asserted patents. *See Peloton Interactive, supra*, at *2 (noting that “the simplification factor weighed against a stay where the PTAB had not instituted IPR proceedings for all asserted patents”). In the EDTX Proceedings, Patent Owner has asserted three patents against Sony, each targeting different features of Sony’s CMOS image sensors. Each of the asserted patents are subject to a Petition for IPR filed by Sony: IPR2023-00298 (Patent 7,868,366); IPR2023-00296 (Patent 7,867,808); and IPR2023-00389 (Patent 8,035,143).

As a result, in order to prevail on a motion to stay, Sony would have to show not only that the Board is likely to invalidate every asserted claim, but that the Board is likely to invalidate every asserted claim from every asserted patent.

Accordingly, this factor favors denial of institution because Petitioner has not sought a stay pending outcome of this IPR, and evidence exists that the EDTX Proceeding Judge would not grant a stay even if institution were to occur.

Factor 2: If the Board reaches its institution decision within three months of receiving the preliminary response, 35 U.S.C. §314(b), and issues a final written decision within 1 year of institution, 35 U.S.C. §316(a)(11), a final written decision would likely not issue until around late July 2024—4 months after the scheduled trial date of March 18, 2024 (Ex. 2005 at 1) and 2 months after the median statistics for Judge Payne suggest the trial would occur. Ex. 2006 at 35. As a result, a final written decision here is highly unlikely to issue early enough to avoid duplication or simplify any issues for trial (which would be projected to occur the same month). Thus, this factor favors denial.

Factor 3: The investment in the parallel proceedings is significant. In the EDTX Proceeding, the parties have exchanged discovery, including technical, marketing and sales materials relating to Sony’s CMOS image sensor products. Similarly, both infringement and invalidity contentions have already been served. Ex. 2007; Ex. 2008. The parties are also on the eve of the claim construction process, with deadlines for exchanging terms and proposed constructions coming up next month in May and claim construction briefing starting in July of 2023. Ex. 2005 at 4-5.

Factor 4: All of Sony’s asserted grounds in this proceeding are also part of its preliminary invalidity contentions in the EDTX Proceeding. *See* Ex. 2009 at

114 (stating that “Sony incorporates by reference its IPR petition” and identifying the same six grounds of invalidity). Thus, instituting this proceeding would lead to entirely duplicative efforts here and in the EDTX Proceeding.

Petitioner Sony argues that this factor weighs against denial because it stipulates that, “should the Board institute review, Petitioner and the other defendants will not rely upon any invalidity grounds based on Pyo and/or Imaoka (*i.e.*, the primary references herein).” Pet. 98. However, such a narrow stipulation still favors exercising discretionary denial. As the Board noted in its precedential opinion in *Sotera Wireless, Inc. v. Masimo Corporation*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020), what is important is whether the “Petitioner broadly stipulates to not pursue ‘any ground raised ***or that could have been reasonably raised.***’” *Id.* at 19; *see also* Director’s Guidance at 7-8.

Petitioner’s offer to conditionally litigate one set of invalidity theories in the PTAB and a separate set of invalidity theories in the EDTX Proceeding does little to provide an “inexpensive resolution of every proceeding.” *See* 37 C.F.R. §42.1(b). In fact, Petitioner’s approach simply increases the costs for all parties, creating a duplication of litigation rather than the desired “cost-effective alternative to litigation.” *See* 77 Fed. Reg. 48680-01 (Aug. 14, 2012).

Even worse, Sony's narrow stipulation to not rely on the Pyo reference would not cover Sony's reliance on the Pyo2 reference, which Sony raised in its invalidity contentions in the EDTX Proceeding. *See* Ex. 2009 at 18. Like for Pyo, Sony's invalidity contentions rely on Pyo2 in combination with the Choi and/or Dublin references as a basis for invalidity. *See* Ex. 2009 at 105. As a result, Sony's stipulation, on its face, does nothing to avoid the duplication of issues in this IPR and the EDTX Proceeding.

Factor 5: Sony concedes that it is a party to the Litigation. Pet. at 98. Under the Board's precedential *Sotera* opinion, when the parties are the same, this factor supports denying institution. *Sotera, supra*, at 19.

Factor 6: As discussed above, the merits of this Petition are particularly weak: although Petitioner purports to rely on the plain and ordinary meaning for each of the claim terms, Petitioner's combinations fail to disclose all of the elements of at least independent claim 1. Instead, Petitioner's arguments are based on overly broad *de facto* constructions that were not properly raised under the PTAB rules and fail to reflect the common meanings of key terms. Such flaws are readily apparent in Petitioner's complete failure to address the term "penetrating" with respect to the first and second vias (Grounds 1-2), and Petitioner's attempt to identify the same "through-hole 32" as satisfying those two vias (Grounds 3-6).

Additionally, as mentioned above, Petitioner is pursuing two additional IPR petitions against the other asserted patents from the underlying litigation. As with the instant Petition, those Petitions are also particularly weak. For example, in IPR2023-00296, the Patent Owner's Preliminary Response illustrates how various claim elements are missing in each asserted ground. Similarly, in IPR2023-00389, the Patent Owner's Preliminary Response illustrates how various claim elements are missing in each asserted ground and, moreover, in contravention of 37 C.F.R. §42.104(b)(4), the Petition has not specified where each element of the challenged independent claim is found in the prior art relied upon.

On balance, the *Fintiv* factors favor discretionary denial.

D. THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION UNDER 35 U.S.C. §325(d)

Under §325(d), the Board uses the following two-part framework: “(1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) ... whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims. If a condition in the first part of the framework is satisfied and the petitioner fails to make a showing of material error, *the Director generally will exercise discretion*

not to institute inter partes review.” *Advanced Bionics, LLC v. Med-El Elektromedizinische*, IPR2019-01469, Paper 6, at 8-9 (Feb. 13, 2020) (precedential).

Turning to the first part of the *Advanced Bionics* framework, the combination of Pyo and Choi relied upon in the Petition is substantially the same art previously presented to the Office. During prosecution of the ‘143 patent, the Applicant submitted Pyo and a complete English translation of its Abstract (Ex. 2011), as well as another foreign reference, Sugimoto, and a complete English translation of its Abstract (Ex. 2012), with an Information Disclosure Statement (IDS) (Ex. 2010).⁷ The Examiner confirmed the submissions by initialing the IDS and adding a note that both art references were considered. Ex. 2013.

The Petition asserts that Pyo was “not ‘presented to the Office’” because “the English translation of the Pyo Abstract fails to disclose several elements disclosed by Pyo, ...” Pet. 100. As an initial matter, the Board considers filing an IDS as presenting a reference to the Office. *See, e.g., Advanced Bionics*, 7-8

⁷ Pyo is identified by its application number KR 10-2004-0115928 in the IDS (Ex. 2010), whereas it is identified by its publication number 10-2006-0077132 in the Petition (Pet. ix).

(“***Previously presented art*** includes ... art provided to the Office by an applicant, ***such as on an Information Disclosure Statement (IDS)***”). Further, an applicant is not required to provide a full English translation of a foreign language art reference as part of an IDS. According to 37 C.F.R. §1.98(a), “[a]ny information disclosure statement ... shall include ... [a] copy of the translation ***if a written English-language translation*** of a non-English-language document, ***or portion thereof*** is within the possession, custody, or control of, or is readily available”

The Office requires only a ***concise*** English explanation of the ***relevance*** of a foreign language art reference in an IDS, and not a detailed statement of which claim elements applicant contends are present and which are missing from the foreign language art. See M.P.E.P. §609.04(a)(III) (“Each information disclosure statement must further include ***a concise explanation of the relevance*** ... about the content of the information listed ***that is not in the English language.***”).

Furthermore, an English language Abstract may satisfy the requirement of a concise explanation of the relevance of the foreign art: “***Submission of an English language abstract of a reference***, such as one generated by a foreign patent office, ***may fulfill the requirement for a concise explanation.***” *Id.*

The English language Abstract together with the drawings having English numerals filed with the IDS provide a concise representation of Pyo and its

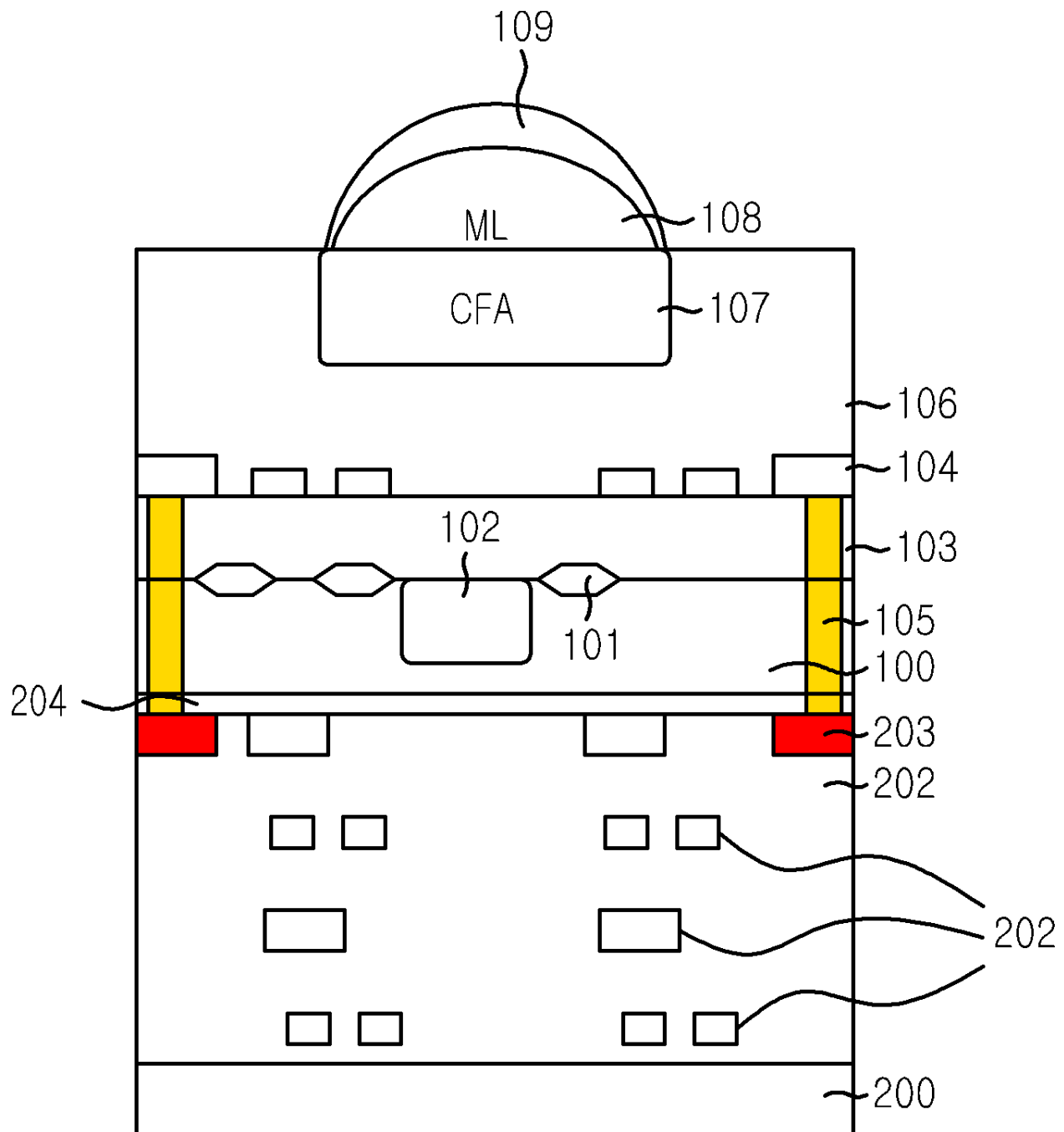
relevance. The Examiner did not ask for additional explanation or a full translation of Pyo, and instead noted that the reference was “considered” (Ex. 2013), indicating that the Examiner determined that Pyo was sufficiently presented.

Petitioner contends that “the English translation of the Pyo Abstract fails to disclose several elements disclosed by Pyo” Pet. 100. Even assuming Petitioner’s contention is accurate (and it is not), the elements Petitioner contends are not disclosed have no bearing on the fact that a reasonable Examiner may determine that Pyo fails to disclose “*a second via*” and “*the first via being connected to the second via*” based on the English language Abstract together with the drawings having English numerals filed with the IDS.

For example, Pyo filed with the IDS does not show or disclose “a second via.” The Petition refers to connecting portion 105 in first substrate 100 as “first via.” See, e.g., Pet. 47-49. Connecting portion 105 is shown in first substrate 100 in the Abstract and Figures 2a, 2c, 2d, and 3 filed with the IDS. Ex. 2011 at 1, 8-10. The Abstract discloses “first substrate (100)” (*id.*, 1), and “[a] connection part (105) is formed on a back surface of the first substrate.” *Id.* The Abstract also discloses “second substrate (200).” *Id.* Thus, while the Abstract shows and discloses a “first via” (“connecting portion 105”), a second via is not shown or disclosed. Thus, the Examiner may very reasonably determine that Pyo fails to

disclose “*a second via.*” It follows that the Examiner may then quite reasonably determine that Pyo fails to disclose limitations such as “*a second via penetrating the second interlayer dielectric so that the second via is connected to the second metal interconnection*” and “*the first via being connected to the second via.*”

In fact, the Abstract and its drawing (and other Pyo’s drawings) filed with the IDS disclose that connecting portion 105 (the “first via” in the Petition) is connected to pad 203, and not to a second via. “A connection part (105) is formed on a back surface of the first substrate. ... A *pad (203) is formed on the metal lines to correspond to the connection part.* The back side of the first substrate is joined to a front side of the second substrate, thereby the pad correspond [sic] the connection part.” Ex. 2011 at 1. Thus, even if Pyo disclosed “a second via” (which it does not), the Examiner may very reasonably determine that Pyo still lacks the claim element “*the first via being connected to the second via,*” since connecting portion 105 is connected to pad 203 and not a second via. The colorized Abstract Figure in the IDS (below) shows connecting portions 105 (yellow) and pads 203 (red).



Pyo Fig. 3 (colorized Abstract Figure filed with IDS)

Therefore, the Examiner may quite reasonably conclude that claim elements in [1.2] (Pet. 13) and [1.5] (Pet. 14) are missing from Pyo's Abstract, and indeed

missing from all Pyo's drawings that were before the Examiner with English numerals.

Any differences between the Pyo filed with the IDS and the full translation of Pyo do not alter the Examiner's reasonable conclusion. Like Pyo filed with the IDS, the full translation of Pyo does not show or disclose a second via, and also discloses that connection part 105 (the "first via") is connected to pad 203, and not to a purported second via. The claim elements that were missing in the art that was before the Examiner are also missing in the art presented in the Petition in a similar manner, as discussed *supra* §V.A.

Petitioner contends that only the fully translated Pyo discloses (1) a first and a second ILD; (2) a PMD; (3) a first metal interconnection; and (4) a color filter. Pet. 100. However, even if Petitioner's contention was accurate (and it is not), the contention is not directed to claim elements "***a second via penetrating the second interlayer dielectric*** so that the second via is connected to the second metal interconnection" and "a first via penetrating the pre-metal dielectric and the first semiconductor substrate, ***the first via being connected to the second via.***" These claim elements are missing from both the full translation of Pyo (*supra* §V.A), and the Pyo filed with the IDS. As such, in all material respects, substantially the same art was previously presented to the Office.

Petitioner asserts that “the Examiner never had the opportunity to consider Pyo in combination with Choi, which was not of record. Thus, there is no overlap between the grounds in this Petition and anything considered during prosecution.” Pet. 101. Contrary to Petitioner’s assertion, Grounds 1 and 2 in the Petition significantly overlap with Pyo’s Abstract and drawings considered by the Examiner during prosecution.

Petitioner relies on Choi for disclosing the claim element “a conductive barrier layer on the first metal interconnection.” Pet. 54. Choi is a single-substrate reference that is not concerned with a “second via.” Petitioner does not rely on Choi for disclosing “*a second via penetrating the second interlayer dielectric* so that the second via is connected to the second metal interconnection” and “a first via penetrating the pre-metal dielectric and the first semiconductor substrate, *the first via being connected to the second via*” that are missing in Pyo. *Id.*

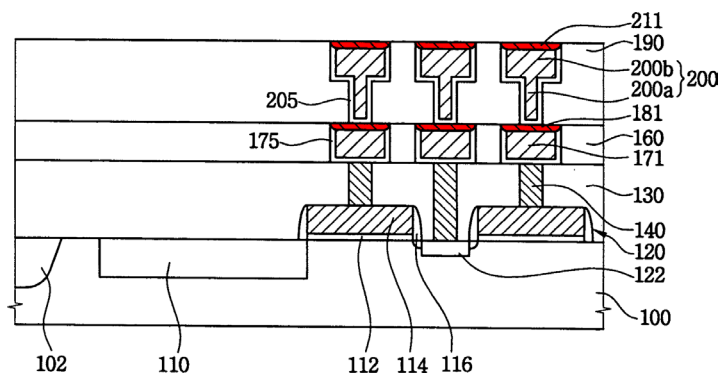
Moreover, Choi is merely cumulative as to Sugimoto (Japanese Application No. JP20020001936) that was disclosed in the same IDS as Pyo and considered during prosecution. The Petition relies on the top metal barrier layers 181 and 211 on respective copper interconnections 171 and 200 in Figure 5G of Choi (below, colorized) for the purported “conductive barrier layer.” *See, e.g.*, Pet. 29-30; 54 (“The top metal barrier layer is ‘on’ the first metal interconnection.”); *id.*, 55

(“metal barrier layers meeting limitation [1.8]” in the annotated drawing).

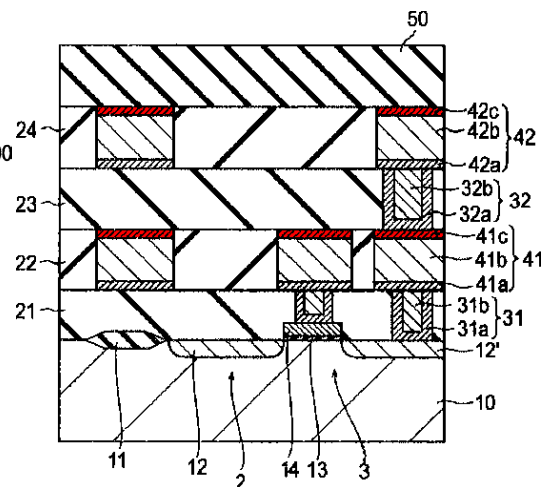
Sugimoto filed with the IDS discloses barrier metals 41c and 42c similar to top metal barrier layers 181 and 211 of Choi. Sugimoto’s Abstract discloses “barrier metals 41a, 41c, 42a, 42c” and “main wiring layers 41b, 42.” Ex. 2012 at 1.

Sugimoto’s representative drawing Figure 2 in the Abstract (below, colored) shows barrier metals 41c and 42c on respective main wiring layers 41b and 42b.

Id. In the figures below, top metal barrier layers 181 and 211 of Choi and barrier metals 41c and 42c of Sugimoto are colored red.



Choi Fig. 5G (Colorized)



**Sugimoto Fig. 2 (Colorized)
Abstract Figure filed with IDS)**

As seen above, Choi is cumulative as to Sugimoto that was considered during prosecution.

Setting aside that Choi is cumulative as to Sugimoto, there are no material differences between the combination of Pyo and Choi asserted in the Petition and

Pyo individually. The combination of Pyo and Choi is the same as Pyo individually in failing to disclose “*a second via penetrating the second interlayer dielectric* so that the second via is connected to the second metal interconnection” and “a first via penetrating the pre-metal dielectric and the first semiconductor substrate, *the first via being connected to the second via*” as discussed *supra* §V.A. Accordingly, the combination of Pyo and Choi is not materially different than Pyo individually, which was previously presented to the Office.

Thus, the first part of *Advanced Bionics* is satisfied, and the combination of Pyo and Choi relied upon in the Petition is substantially the same art previously presented to the Office.

Under the second part of the *Advanced Bionics* framework, Petitioner fails to make a showing of material error by the Office with respect to Pyo or Sugimoto presented in the IDS. The Petition makes a conclusory and speculative assertion that “the Examiner ‘misapprehend[ed] or overlook[ed] specific teachings of the relevant prior art [i.e., Pyo] where those teachings impact patentability of the challenged claims.’ ... Here, the Examiner never cited Pyo. Thus, the Examiner overlooked specific teachings of Pyo impacting the patentability of the claims challenged in this Petition.” Pet. 100-101. First, the Examiner did in fact cite Pyo, as seen in the “References Cited” on the front page of the ‘366 patent, and on the

list of references considered by the Examiner (Ex. 2013). Second, the Petition completely fails to identify any specific teaching of Pyo that the Examiner purportedly misapprehended or overlooked. Pet. 100-101. Petitioner mentions that “[t]he Petition is supported by an English translation of the entirety of Pyo—not just its abstract—and an expert declaration explaining how POSAs would have understood Pyo.” *Id.*, 101. However, the Petition also completely fails to identify any specific part of its translation or new expert declaration it considers applicable. *Id.*

This is not a situation where the Examiner miscited or misquoted key language from a reference. Instead, the Examiner had an opportunity to consider it against the pending claims and, presumably, concluded that its failure to disclose key claim elements was dispositive. Contrary to Petitioner’s assertion that “the Examiner never cited Pyo. Thus, the Examiner overlooked ...” (Pet. 101), it is by no means an error to avoid issuing an Office Action affirmatively relying on a reference that fails to disclose key claim elements.

“If reasonable minds can disagree regarding the purported treatment of the art or arguments, it cannot be said that the Office erred in a manner material to patentability.” *Advanced Bionics*, 9. Indeed, it would have been quite reasonable for the Examiner, after due consideration, to conclude that Pyo fails to disclose

claim elements [1.2] (Pet. 13) and [1.5] (Pet. 14). The Examiner need not determine whether additional claim elements were missing or other claim elements were present. It is enough for the Examiner to conclude that at least some claim elements, such as claim elements [1.2] and [1.5], were missing based on the Abstract and the drawings filed with the IDS.

Thus, it cannot at all be said that the Office materially erred. “At bottom, this framework reflects a commitment to defer to previous Office evaluations of the evidence of record unless material error is shown.” *Advanced Bionics*, 9. Petitioner fails to make a showing of material error by the Office. Under *Advanced Bionics* reconsidering the Office’s previous evaluation of the art filed with the IDS is unwarranted.

The Petition has repeatedly and improperly referred to the “Korean counterpart” of the ‘143 patent. For example, Petitioner states that “cancellation of the Korean counterparts [*sic*] to the Challenged Claims following the Korean examiner’s rejection over Pyo (*a Korean-language reference the Korean examiner could understand but the U.S. examiner could not*) confirms the compelling nature of the challenge herein.” Pet. 98-99. As another example, Petitioner states that: “Moreover, the Korean examiner’s rejection and the Applicant’s subsequent cancellation of the device claims over Pyo in the related

Korean prosecution was also not provided to the Office.” *Id.* 100. Similar improper references to the “Korean counterpart” and its purported relevance to the ‘143 patent has been made throughout the Petition. *See id.*, 3, 11-13, 98-100.

The basic premise of Petitioner is that the claims in the Korean counterpart application were substantially the same as the claims in the U.S. application. However, as illustrated *supra* §II, the opposite is true, that is the claims **were substantially different, not substantially the same**. A side by side comparison of claim 1 of the ‘366 patent with claims 1-5 in the Korean counterpart speaks for itself and shows the substantial differences. *See supra* §II. Some of these differences were specifically discussed *supra* §II.

As such, the basic premise in the Petition is untenable. Therefore, Petitioner’s repeated references to the Korean counterpart application are improper and misleading. Moreover, Petitioner’s insinuation that the U.S. Examiner failed due to lack of understanding the Korean language (itself a speculation) is improper. Further, Petitioner’s reliance on the Korean counterpart application in discussing the *Fintiv* factors (Pet. 98-99), and the *Advanced Bionics* factors (*id.*, 100) are also improper and irrelevant.

The Board should exercise discretion under §325(d) not to institute *Inter Partes* Review.

VI. CONCLUSION

For at least the foregoing reasons, Patent Owner respectfully requests that the Board deny the Petition and not institute trial.

Respectfully submitted,

/michael farjami/

Michael Farjami

Reg. No. 38,135

Lead Counsel for Patent Owner VisionX

Date: April 21, 2023

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24, the undersigned certifies that the paper, Patent Owner's Preliminary Response, contains 13,576 words excluding a table of contents, a table of authorities, a certificate of service, a certificate of word count, or exhibit list, but including annotations added to figures. In making this certification, Patent Owner has relied on the word count feature of the word processing system used to prepare the paper, and manually adding the number of words present in annotations to figures.

April 21, 2023

/michael farjami/
Michael Farjami
Reg. No. 38,135

CERTIFICATE OF SERVICE

I hereby certify that on April 21, 2023 copies of the foregoing PATENT OWNER'S PRELIMINARY RESPONSE and all documents filed with it were served via electronic mail, as agreed to by counsel, upon the following counsel for the Petitioner:

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