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via

A plated hole used to provide low-inductance connections on an *integrated circuit. A via may be formed through the dielectric layer on the top of a wafer to interconnect two metallization patterns. A via may also be formed through the back of a wafer containing FETs where a low-inductance earth is required; this is especially useful for microwave or power FETs, and metal plating is used on the back of the wafer to provide a heat sink and earth plane simultaneously (see diagram)....

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