

Tutorial on forming through-silicon vias

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ABSTRACT

Through-silicon vias (TSVs) are a critical technology for three-dimensional integrated circuit technology. These through-substrate interconnects allow electronic devices to be stacked vertically for a broad range of applications and performance improvements such as increased bandwidth, reduced signal delay, improved power management, and smaller form-factors. There are many interdependent processing steps involved in the successful integration of TSVs. This article provides a tutorial style review of the following semiconductor fabrication process steps that are commonly used in forming TSVs: deep etching of silicon to form the via, thin film deposition to provide insulation, barrier, and seed layers, electroplating of copper for the conductive metal, and wafer thinning to reveal the TSVs. Recent work in copper electrochemical deposition is highlighted, analyzing the effect of accelerator and suppressor additives in the electrolyte to enable void-free bottom-up filling from a conformally lined seed metal.

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I. INTRODUCTION

While Moore's law has fueled growth in the electronics industry for more than five decades, there has been an increase in both the cost and development time required to miniaturize transistors. This gives indications that Moore's law may no longer be the appropriate economic driver for continued growth in the microelectronics industry. Heterogeneous integration (HI) and advanced packaging approaches, such as three-dimensional (3D) integration, have been identified as paths for continuing the push for increased bandwidth and functionality, while decreasing cost per system volume. Gordon Moore predicted "It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically."¹ HI can add increased value and performance, similar to the motivation behind system on a chip integration, without the associated costs and yield fallout associated with Moore's law scaling.¹ Integration of sophisticated electronics at the system level and the many approaches used to achieve this integration are well described

in published review articles.^{2–6} Through-silicon vias (TSVs) are a key enabling technology for many HI systems as they are required for 3D chip stacking in advanced microelectronic packaging approaches and have been used in many applications over the last several years such as biomedical, optoelectronic, photonic, display technologies, and microelectromechanical systems (MEMSs). TSVs allow direct signal routing vertically between chips as opposed to routing to the periphery and wirebonding to an interposer or printed circuit board. This vertical routing results in shorter electrical path lengths, which translates to reduced electrical parasitics such as resistive-capacitive (RC) delay time delays. In addition to electrical improvements, TSVs enable an increased number of inputs and outputs because they can be arrayed throughout the area of a chip as opposed to utilizing only the perimeter of the chip. Furthermore, TSVs can improve thermal management throughout the chip. TSVs enable the stacking of multiple semiconductor chips resulting in packaging microelectronic devices with increased functionality per volume. Packaging these sophisticated electronic systems is difficult, and examples of these technical challenges are well described in the literature, especially in the areas of thermal management,^{7,8} interconnect compatibility,⁹ reliability,¹⁰ and failure modes.¹¹

This article reviews some of the processing steps associated with fabricating TSVs. A TSV is a hole in a silicon (Si) substrate that is filled with a conducting material to allow 3D electrical routing. There are several approaches for TSV integration depending on the design and fabrication requirements, and they are categorized into via-first, via-middle, or via-last approach.² Via-first, -middle, or -last designation describes TSV integration before CMOS front-end of line (FEOL) processes, in the middle of the full process flow, or after CMOS back-end of line (BEOL) processing is complete, respectively. In a via-first integration scheme, TSVs are inserted into the substrate prior to any other processing (including FEOL processing such as ion implantation). This has the benefit of process flexibility during the TSV module (etch, line, and fill) but has the drawback of setting thermal budget constraints for subsequent processing depending on what materials are utilized in the TSV module. Via-middle integration approaches generally insert the TSV module after the FEOL steps are complete, which consist of numerous high temperature processes, but before BEOL processing where the multilayer metal routing is performed. Via-last integration schemes insert TSVs after both the FEOL and BEOL processes are complete. This review focuses primarily on the processes and materials most often associated with via-middle and via-last integration. Two previous articles review the formation of TSVs in detail^{12,13} with attention to the considerations for integrating TSVs with existing circuitry as well as manufacturing challenges and considerations required for these specific applications. This field has evolved significantly over the last 20 years and yet several challenges remain. Specifically, this review highlights recent studies in the area of copper (Cu) electrochemical deposition (ECD) providing a summary of the mechanisms associated with electrolyte

additives that enable void-free bottom-up feature filling from a conformally deposited conductive seed metal.

Figure 1 illustrates a typical via-middle or via-last process flow with a series of cross-sectional schematics.¹⁴ The first step in the process is to form the vias through photolithography and reactive ion etching (RIE). The angle of the etch profile can be intentionally tailored (straight or with a positive taper) to accommodate the deposition of subsequent insulating, barrier, and seed layers. Controlling the etch profile is important for conformal continuous coverage of the materials that line the via. In this integration approach, blind vias (not etched entirely through the wafer) are formed. After the via is etched, an insulating liner is deposited to electrically isolate the Cu TSV from the substrate. The insulating liner is most often silicon dioxide (SiO_2) deposited using plasma enhanced chemical vapor deposition (PECVD). Other materials such as silicon nitride (SiN_x) or alumina (Al_2O_3) can also be used and deposited by a number of deposition techniques. An important deposition technique used for conformally lining geometries that are nonaccessible by line-of-site deposition approaches is atomic layer deposition (ALD), which has extremely high conformality. A barrier material is needed between the insulating layer and the electroplating seed metal to prevent electromigration or diffusion of Cu, which result from high current densities or operation at elevated temperatures, respectively. This barrier material is commonly tantalum nitride (TaN) deposited by reactive sputtering or by directly sputtering from a TaN target.¹⁵ As stated previously, other materials can be used for this barrier film such as platinum (Pt) deposited by physical vapor deposition (PVD) or ALD. On top of the barrier layer, a thin Cu seed metal is deposited by PVD. One benefit of utilizing Pt as the barrier layer is that it can also serve as

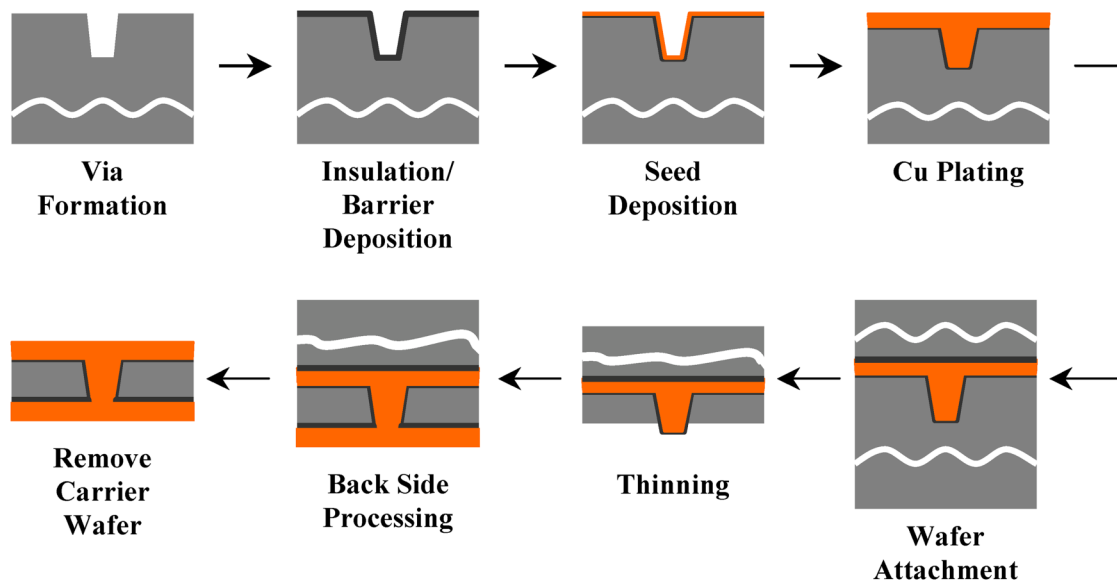


FIG. 1. Series of schematics illustrating a common process flow for fabricating TSVs. The schematic was modified slightly from the original publication (Ref. 14). Adapted with permission from Abhulimen *et al.*, J. Vac. Sci. Technol. B 26(6), 1834 (2008). Copyright 2008, American Vacuum Society.

the seed metal for subsequent ECD.¹⁶ The via is filled by ECD in an electrolyte with organic additives that promote a more rapid growth front at the bottom of the feature, as compared to the sidewall or the top surface of the feature. After frontside processing is complete, a carrier wafer is attached to the topside of the device with a temporary bonding media and the backside of the silicon wafer is thinned to reveal the via. After revealing the via, backside photolithography and metal deposition are performed to fabricate the flip chip bond pad and then the carrier wafer can be removed. Sections II–V in this paper provide additional details for each of these key process steps, specifically etching, liner deposition, Cu electroplating, and wafer thinning.

II. ETCHING

Formation of the vias used for TSVs is done utilizing dry etching techniques. This paper provides a conceptual foundation of the function of deep reactive ion etching (DRIE) equipment, as well as traditional etching/passivating mechanisms used to form high-aspect ratio features like TSVs. For more depth on the development of Si DRIE processes, there are a number of topical reviews available.^{17–22}

Inductively coupled plasma (ICP) etch tools have many advantages for DRIE. These tools have the ability to independently control plasma density, ion energy, and gas chemistry. Thus, there are many process parameters that can be tuned in order to etch Si with tapered, vertical, or reentrant sidewall profiles. Understanding of the operation of ICP etch tools is crucial for successful development of the etch. Depending on the model, ICP etch tools often supply gas species to the chamber using a shower head or an annular ring in order to improve areal uniformity of plasma and radical distributions. A strike step is used to ignite the plasma and then ICP coils are used to induce a magnetic field. This field interacts with free electrons to form a high density plasma. The process gases moving through this inductively coupled plasma region become at least partially dissociated and ionized, thus forming the

chemically reactive and physically energetic species that enable etching. The chuck, that is holding the wafer, is biased independently of the plasma through a separate RF supply. The ions generated by the ICP coil are driven into the wafer by this bias. The density of ions (and thus ion current to the wafer) is proportional to the RF power applied to the inductive coil, while the energy of those ions incident on the wafer is proportional to the RF power applied to the chuck.

Typically to achieve high speed, high-aspect ratio DRIE of silicon, a combination of both etching and sidewall passivation is required. Etching occurs using reactive ion species that bombard a surface. The impingement of ions on the surface can create damage in the form of unsatisfied bonds. The gas species used for etching can react with this surface to form volatile byproducts, thus removing the material from the substrate. Therefore, there is both a physical (ion bombardment) and chemical component to reactive ion etching, which in combination will etch the wafer much faster than either mechanism alone.²³ Several gases are capable of Si etching including most halogens; however, fluorine based etches are preferred because of their high etch rates and toxicity concerns with Cl_2 and HBr .¹⁷

Passivation of the sidewalls during a DRIE process helps control the etch to achieve anisotropic profiles. This is most commonly achieved utilizing a pulsed-mode process (Bosch), where the etching and polymerizing gases are cycled on and off, or using a mixed-mode process in which both passivation and etching gases are present simultaneously.¹⁷

In a pulsed-mode or Bosch process, there are two steps, an etching step and a passivation step, that are cycled.²⁴ This is sometimes extended to three steps by the addition of a separate directional physical etching step to clean the horizontal surfaces' passivating polymer as depicted in Fig. 2. The etch step utilizes SF_6 , which dissociates in the plasma to form atomic fluorine (F), a silicon etchant. At low bias, F etches Si at a high rate, while also being chemically selective to the etch mask. The F etch is isotropic

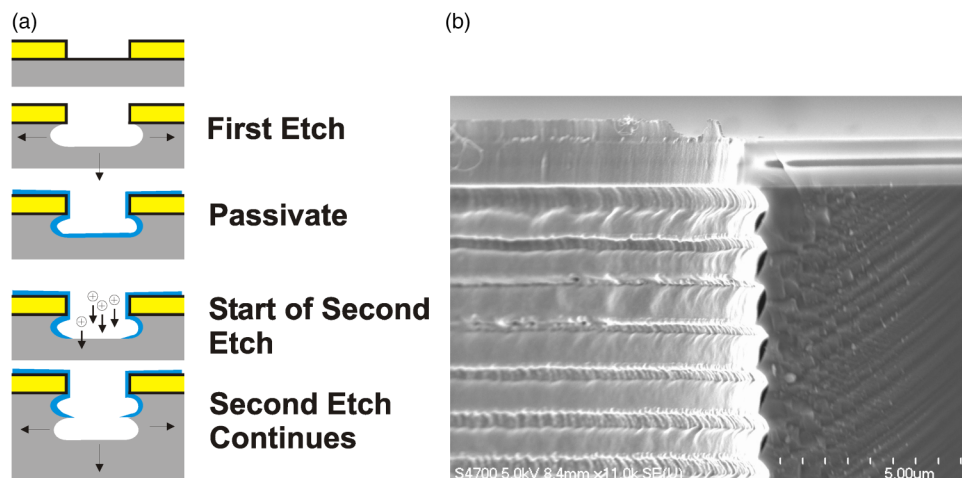


FIG. 2. (a) Schematic illustration of Bosch etch cycling demonstrating the isotropic nature of the chemical etch and passivation and the anisotropic nature of the ion bombardment. This cycling leads to sidewall scallops which are shown in (b).

and, therefore, a trade-off exists between the speed of the etch and the amount of lateral etching, referred to as scalloping, caused during this primary etch step. Following the Si etch step, a separate process gas, often C_4F_8 , is used to form a protective polymer coating on the sidewalls of the trench or via. C_4F_8 forms a polymer similar to polytetrafluoroethylene (PTFE) on all surfaces of the substrate, though process parameters are optimized to prevent excessive polymer deposition. To remove the polymer at the bottom of the feature and achieve an anisotropic etch front, the chemistry is then cycled between this polymerizing gas and the etch gas with sufficient bias applied to remove polymer on surfaces normal to incident ions (horizontal surfaces in a cross-sectional view), while leaving the polymer in place on surfaces parallel to the incident ions (vertical surfaces in a cross-sectional view). The etch/passivation cycle results in characteristic sidewall scallops as seen in Fig. 2. This process can be tuned to be highly anisotropic and obtain a vertical etch profile. Following the Bosch etch process, both dry and wet cleans using oxygen plasma and PRS 3000 are used to remove the residual polymer from the sidewall of the etched feature. Removing this residual polymer is important for the adhesion of subsequent thin film liners as well as defect prevention from undesired redistribution of this polymer during subsequent processing.

In a mixed-mode process, the passivating species and the etching species are supplied to the chamber at the same time. One method is to utilize SF_6 in combination with O_2 gas to provide the etching and passivation. The fluorinated species will etch Si, just as with pulsed-mode etching, and the addition of oxygen promotes an SiO_xF_y passivation layer, which is volatile at room temperature. In order to maintain the passivating reaction products, cryogenic wafer cooling is used to freeze them in place.^{17,25–27} This is done utilizing a liquid nitrogen cryostat achieving wafer temperatures typically between -80 and -160 °C. The inhibiting layer can be modified by changing the temperature or the amount of oxygen in the gas flow, with as a general rule lowering the temperature by 10 °C requires 10 SCCM less O_2 to achieve the same profile.¹⁷ The effect of oxygen on the etch profile can be seen in Fig. 3.²⁸

There are several trade-offs to consider when choosing between a Bosch and a mixed-mode process. First, because the mixed-mode process does not cycle between etching and passivating, the sidewall scallops are eliminated. However, cryogenic temperatures can induce unwanted stress and the cooling/warming cycles can increase the overall process time.¹⁷ The thick fluorocarbon polymer deposited using a Bosch process must be removed prior to further processing; however, its thickness in comparison to the SiO_xF_y layer deposited using a mixed-mode process is helpful in limiting ion bowing caused by an image field.^{17,20} Finally, Bosch processes are less sensitive to aspect ratio dependent etching (ARDE), also referred to as RIE lag, as well as etch chamber conditioning with respect to mixed-mode processes.¹⁷

There are several issues that can arise from improperly tuned DRIE processes, each having negative impacts on downstream TSV processing; these include poor etch sidewall profile control,²⁴ non-uniform etch depth arising from feature density and/or feature size variation across the wafer,²⁹ and notch formation at the bottom corners of the etched feature.²¹ Etch depth uniformity is affected by both microloading, where local etch rates vary as a function of the local exposed silicon area fraction and, therefore, F:Si ratio, and

ARDE, where narrow features etch at a lower rate than wide features as a result of Knudsen-limited transport of reactants to the bottom of deep trenches or the ion angular distribution.^{17,21,22} Both of these sources of etch rate nonuniformity can be minimized by careful etch parameter selection within certain bounds or by incorporating a buried dielectric or other landing film in the process integration scheme. There is a trade-off to using buried insulating films as etch stops as the films do not efficiently dissipate local charging from the etch chemistry. This results in increased lateral etching at the bottom of the feature leading to a notched profile. These notches are extremely difficult to coat in downstream film deposition processes. Strategies for minimizing notch formation include low frequency bias pulsing, bias duty cycle modulation, and/or changing etch chemistry during the end of the etch process.^{21,22}

A tapered etch profile is helpful with depositing the insulating liner, barrier layer, and plating seed metals. These liners are typically deposited by PVD, which is a line-of-sight deposition approach and thus it is difficult for these films to conformally line a feature with a perfectly vertical or reentrant sidewall profile. Positive sidewall taper in the etch profile can be achieved in mixed-mode etching by varying the temperature or the oxygen content.^{25,28} With a pulsed etch, a tapered sidewall profile can be achieved by proper balance of the relative amounts of etching and deposition in the individual steps of the Bosch cycle. Generally, excessive etching will result in lateral undercut and/or a reentrant sidewall profile, while excessive deposition will lead to positively tapered sidewalls or stop etching altogether. An example of intentionally inducing a slightly positive sidewall to alleviate the challenges associated with line-of-sight PVD is highlighted in Fig. 4.³⁰ The figure shows an example scanning electron micrograph in which an 85° taper is obtained in $10\mu m$ diameter TSVs etched $50\mu m$ deep into the substrate. The slight angle was achieved with a modified DRIE process in which the etch and passivation times, during the Bosch etch, are changed as the via depth increases.

III. THIN FILM LINER DEPOSITION

Once the via is etched, thin films are deposited to electrically insulate the vias from the surrounding silicon, prevent copper diffusion into the substrate, and provide a seed layer for the electrochemical deposition of Cu. Each of these films have particular constraints, either for their material properties or how they are deposited. For the insulating liner, the material must exhibit a sufficiently high breakdown voltage relative to the performance needs of the circuit and all three of these films (liner, barrier, and seed metal) must be deposited conformally and with good adhesion in order to completely line the via. As previously mentioned, one benefit to having tapered sidewalls for the Si etch is to reduce the conformality requirements of these deposition approaches.

For a via-first integration, high temperature deposition processes may be utilized for the insulating liner. Processes based on tetraethyl orthosilicate (TEOS) precursors and thermal oxidation approaches can be used and result in highly conformal SiO_2 . In a via-middle or via-last integration, liner deposition at low temperatures is required for compatibility with BEOL materials. Commonly, a maximum deposition temperature of 400 – 450 °C is utilized after

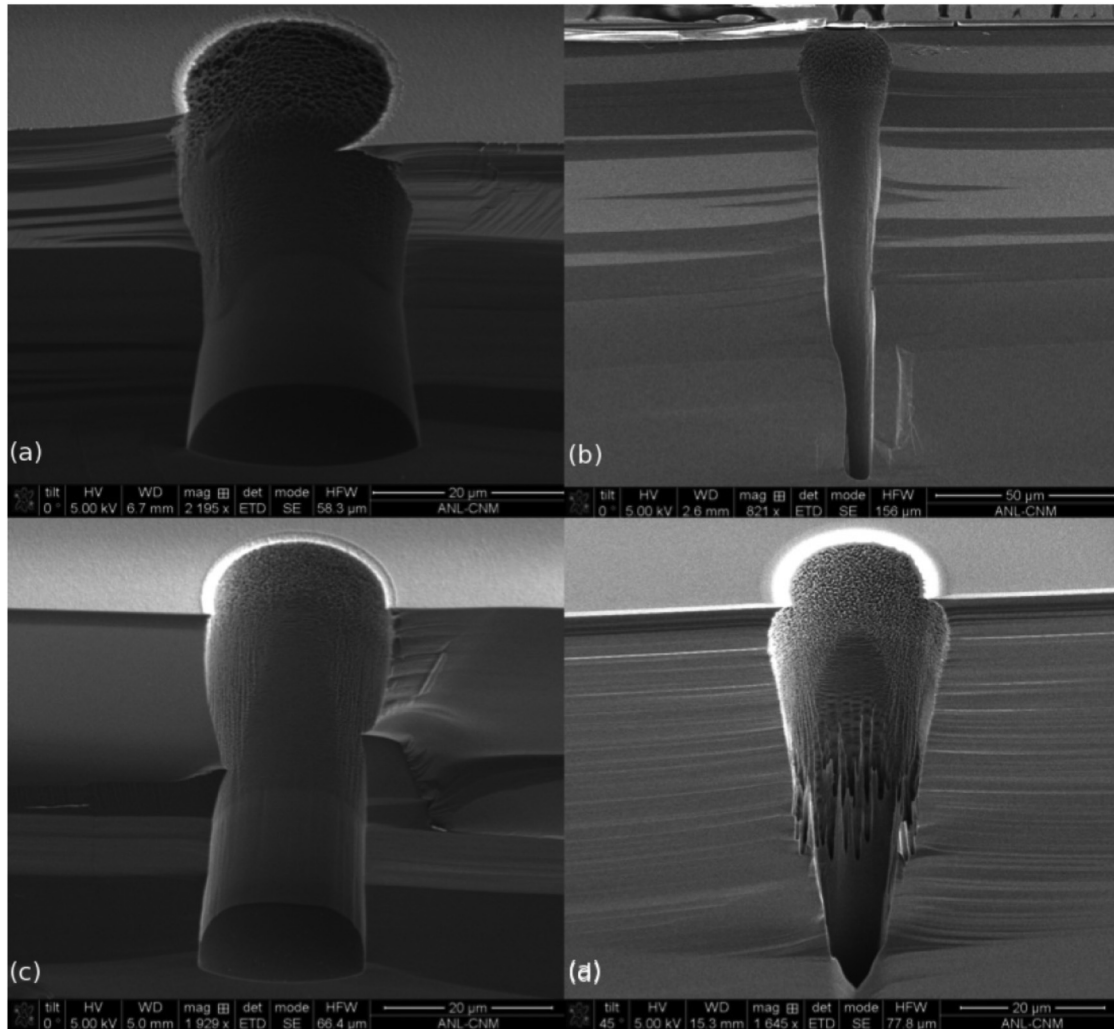


FIG. 3. Cleaved cross sections of the mixed-mode ICP cryoetching of Si with different amounts of oxygen. Etch was done at -90°C with SF_6 and (a) 8% O_2 for 20 min, (b) 10% O_2 for 40 min, (c) 12% O_2 for 20 min, (d) 14% O_2 flow for 20 min. This demonstrates the change in sidewall taper and the advent of Si grass at the highest O_2 flow. The effect of the oxide hardmask on ion bowing is evident in (b). Reprinted with permission from M. B. Jordan, "Fabrication of carbon nanotube filled blind vias and the investigation of carbon nanotubes embedded in a copper matrix for three-dimensional chip stacking applications," M.S. Thesis (The University of Alabama, 2013).

BEOL materials are integrated with the device. For via-middle and via-last integration approaches, the insulating liner is frequently either SiO_2 or SiN_x deposited by PECVD. ALD can also be used to deposit alumina (Al_2O_3) when a more conformal coverage is needed, such as lining a notch feature at the bottom of an etch. In many cases, PECVD provides adequate step coverage for the via liner; however, careful process optimization is required to utilize nonconformal methods such as this.³¹ In some approaches, a combination of PECVD and thermal CVD can be utilized to yield appropriate step coverage and electrical performance.³²

After the insulating layer, a barrier layer is deposited to minimize Cu diffusion. Titanium nitride (TiN) or tantalum nitride (TaN) are routinely used as this barrier layer to prevent Cu migration.^{15,33,34}

TaN films as thin as 8 nm can serve as adequate barriers in temperatures up to 700°C . Furthermore, TaN films exhibit excellent adhesion to many oxides and nitrides³⁵ and Ta-based films deposited by PVD show better step coverage inside small features as compared to Ti-based PVD films.³⁶ In a study comparing TiN and TaN,³⁴ both materials exhibited good adhesion to Cu but galvanic corrosion was observed when utilizing TiN in the postplating chemical mechanical polishing (CMP) step but not when TaN was used. In addition to the diffusion resistance at high temperatures and lack of Cu corrosion, TaN also serves as an excellent CMP stop layer when removing the Cu overburden that results during ECD.

Most commonly, the barrier layer is deposited by either chemical vapor deposition (CVD) or PVD, however other techniques

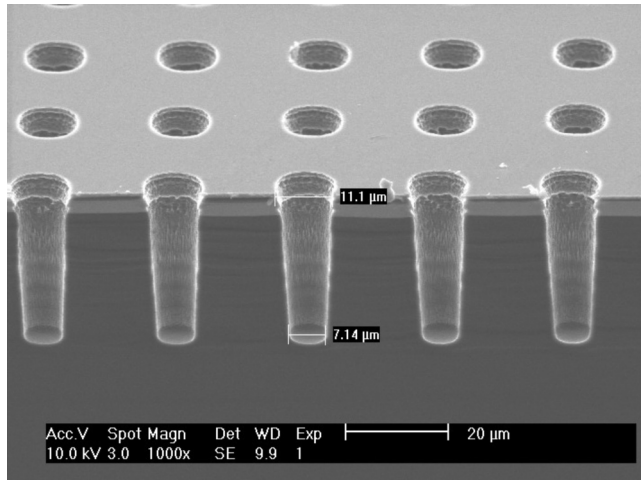


FIG. 4. SEM photo showing an array of vias etched by a modified Bosch process (10 μm in diameter, aspect ratio of 5, and sidewall taper of 85°). Reprinted with permission from Spiesshoefer *et al.*, *J. Vac. Sci. Technol. A* **24** (4), 1277(2006). Copyright 2006, American Vacuum Society.

such as metallorganic CVD^{37–39} and ALD^{40,41} can be used with excellent conformality within deep features. An early study compared the properties of TaN thin films deposited by CVD and PVD.⁴² TaN films prepared by PVD were shown to have smaller grain size, lower resistivity, and lower impurity percentages compared to films prepared by CVD. In the same study, PVD films were found to withstand 50 °C higher temperatures before failure than those of CVD films, both in terms of Cu diffusion and leakage current. In addition, PVD deposition temperatures are much lower than CVD temperatures, which is particularly important for integration schemes with thermal budget constraints.

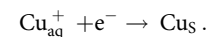
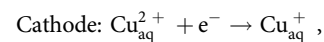
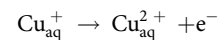
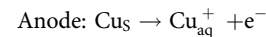
An atomic ratio of 1:1 N:Ta is the desired stoichiometry for TaN and can be achieved through reactive sputtering.⁴³ Rutherford backscattering spectroscopy has been used to investigate the effect of deposition power on the N:Ta ratio and found the highest power (2500 W) resulted in an N:Ta ratio slightly over 1:1, but it is noted that the optimum power level is dependent on the design and configuration of the sputtering tool.³⁰ Following insulation and barrier layer depositions, a conductive seed layer is required for the subsequent ECD process used to fill the TSV. This seed layer is often Cu, deposited by PVD but can be other metals such as Pt deposited by ALD.¹⁶ Recent work has highlighted the use of sputtered ruthenium⁴⁴ and cobalt⁴⁵ for damascene like processes at advanced technology nodes due to the resistivity size effect compared to copper. When the seed metal is deposited through PVD, often a thin (tens of nanometers) adhesion layer is required to prevent the Cu layer from delaminating and is commonly either titanium, tantalum, or chromium.

IV. ELECTROCHEMICAL DEPOSITION

TSVs are filled with a variety of materials including doped polysilicon, conformal tungsten, carbon nanotubes, and ECD Cu.^{46–56}

This review focuses on ECD for void-free bottom-up filling of blind-TSVs with Cu. Cu has higher electrical and thermal conductivity compared to polysilicon and tungsten and ECD results in a relatively low stress material deposition. Void-free filling of high-aspect ratio structures with ECD Cu is challenging, but process parameters can be tailored to accommodate different via geometries.

An electrochemical cell including an electrolyte, power supply, and electrodes used for copper electroplating is illustrated in Fig. 5. In this simplified model, applied potential removes electrons from the anode, leaving the positively charged chemical species solvated in the electrolyte. Electrons arriving at the cathode combine with the Cu ions in the solution at the cathode boundary to deposit solid Cu on the wafer surface. This is depicted algebraically by



The electrolyte contains Cu ions and is a medium for transport of cations and anions toward the two electrodes. The conductive seed layer on the TSV substrate is the cathode in the cell. In practice, electroplating additives, ion exchange membranes, and other factors lead to more complex interactions.

Three deposition regimes for ECD are outlined in Fig. 6, (a) subconformal, (b) conformal, and (c) superconformal deposition. Subconformal deposition results from a gradient of metal ion depletion down the feature due to insufficient Cu^{2+} ion replenishment caused by the geometric confinement of the electrolyte within the feature. Conformal deposition can be achieved through a balance of ion consumption and replenishment at the bottom of a feature. To minimize reactant depletion, plating may be done at a slow rate or, alternatively, pulsed plating may be used where depletion effects are relaxed during the off or reverse cycle. Superconformal growth,

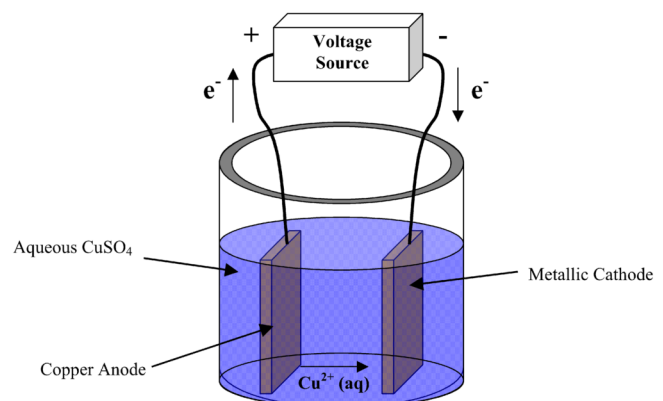


FIG. 5. Schematic illustration of a basic Cu ECD system.

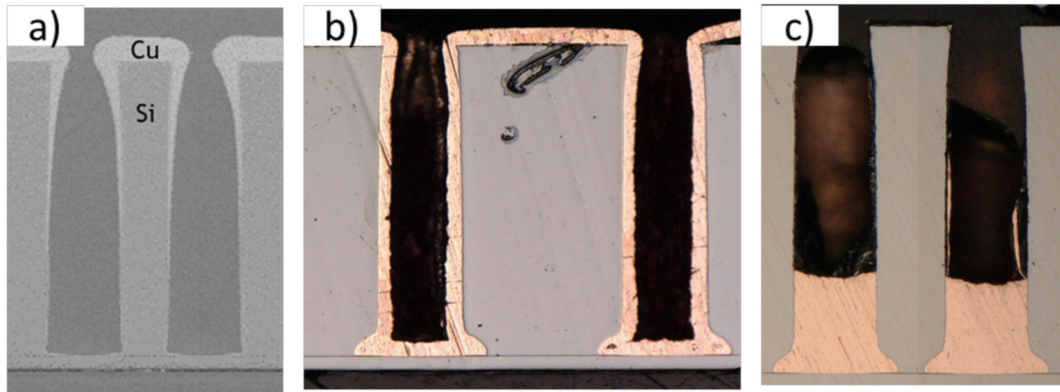


FIG. 6. (a) SEM cross section of subconformal TSV plating; optical microscope cross sections of (b) conformal TSV plating and (c) superconformal plating.

where deposition preferentially grows from the bottom of the vias, is achieved through the use of additives, which either accelerate the deposition at the bottom of the feature or suppress deposition at the top field and sidewall of the feature. Void-free filling of blind vias relies on superconformal deposition regimes. Pulsed plating regimes, such as periodic pulse reverse plating (PPR), in conjunction with additives, have been used to achieve void-free filling, but the underlying mechanisms behind the preferential growth at the bottom of the feature rely heavily on finely tuned additive concentrations. Two models for superconformal growth based on plating with additives exist, the curvature enhanced adsorbate concentration (CEAC) model based on an accelerator additive^{57–62} and the S-shaped negative differential resistance (S-NDR) model, which relies on a suppressor additive.^{16,63–65}

A. Periodic pulse reverse plating

PPR plating can be used in conjunction with electrolyte additives to achieve void-free filling.^{66–71} In PPR, a forward bias is used to deposit a thin layer of materials, a reverse pulse is used to strip Cu from the surface of the via and modify the additive concentrations within the via, and then a short rest period is used to allow time for ion replenishment within the feature. Typical time lengths for the forward and off times are around 100 ms. The reverse pulse is applied for a significantly shorter duration, around 10 ms, and at a higher current density, three to five times greater in magnitude than the forward pulse. An example of subconformal filling using PPR for a sample is shown in Fig. 7. This is a result obtained before optimizing the additive concentrations and pulse plating parameters.

Figure 8 shows cross-sectional views of (a) a superconformal filling profile for a via and (b) a set of vias filled successfully with Cu. To achieve void-free filling, either the additives can be adjusted and a direct current (DC) bias used or the pulse regime can be optimized to still achieve void-free filling with a nonideal concentration of additives.^{66,73–75} For PPR, optimization requires adjusting parameters such as current density in forward and reverse directions as well as forward, reverse, and off pulse times. It is important to note that the additives in the chemistry can react at the anode as

well as be consumed during deposition so it is necessary to replenish the additives to maintain a specific concentration. Alternatively, ion exchange membranes may be employed to separate the anode from the plating additives to avoid additive aging effects. As stated earlier, a modified etch process can be used to achieve a slightly

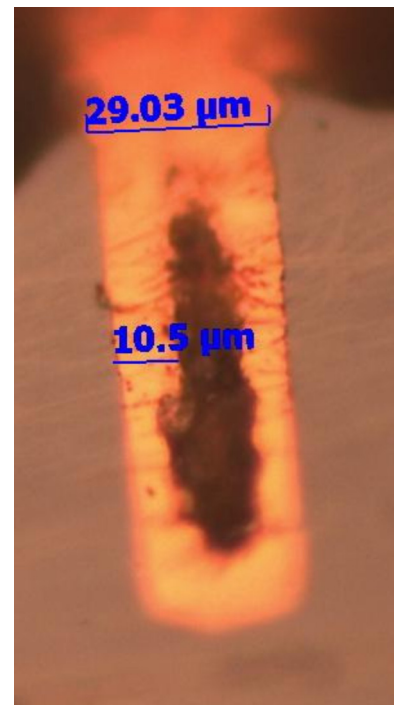


FIG. 7. Optical micrograph showing a cross-sectional view of a subconformal Cu-filled via illustrating a large void. Via diameter is $\sim 30 \mu\text{m}$, and via depth is $90 \mu\text{m}$.

tapered sidewall at the via opening to allow the via lining materials and Cu seed to promote complete filling of the via.

B. CEAC model

Cu plating solutions used in the microelectronics industry typically rely on additives such as chloride ions, a polyether, such as polyethylene glycol, poloxamer (Pluronic), or poloxamine (Tetronics) as a suppressor, bis(3-sulfopropyl)disulfide as an accelerator, and Janus Green B as a leveling agent. These four additives were carried over from printed circuit board manufacturing into dual damascene routing and then TSV filling.^{57,58} Over the past two decades, further understanding on the effects of these additives and other additives exhibiting similar properties in aqueous ECD chemistries has been developed and a few resultant models have been derived. Recent studies have shown that bottom-up growth can be achieved without all four plating additives, for example, a combination of halide and suppressor, or just accelerator additives can be sufficient. The CEAC model describes the mechanism in which an accelerator additive can be used to achieve superconformal fill of trenches and vias.^{58–62}

Two assumptions are made in electrolyte compositions that contain accelerator additives: (1) the local growth velocity is related to the concentration of the adsorbed accelerator and (2) the accelerator floats along the growth interface and is neither strongly incorporated into the deposit nor entirely desorbed back into the plating bath.⁵⁸ These assumptions lead to three stages of ECD as characterized by the growth front location and velocity as depicted in Fig. 9. The first stage has nearly conformal growth and Cu is deposited on all surfaces including the sidewalls of the via and top field of the substrate. As the Cu growth proceeds, area change leads to increased concentrations of accelerator at the bottom of the feature which leads to the second stage, which is superconformal growth.

As shown in Fig. 9(b), positive curvature of the growth front at the bottom of the feature leads to enrichment of the adsorbed accelerator with area change. Finally, when the deposit reaches the top of the etched feature, the third stage, the locally enriched accelerator leads to momentum plating, which eventually weakens the inflection of the curvature. The subsequent increase in surface area as the growth front expands beyond the top of the trench or via is accompanied by some dilution of the accelerator coverage. The excess plating on the surface is referred to as overburden and momentum plating may result in a thicker deposit above the filled features, which must be accounted for when the overburden is removed. The magnitude of momentum plating can be reduced by the addition of a leveling agent, which is accounted for in the extended CEAC model.^{59,66,77}

The CEAC model has been studied extensively, including the development of a growth front tracking algorithm,⁷⁸ which can assist in the bottom-up filling of a wide array of TSV and damascene geometries, but this filling mechanism is geometry dependent as it relies on area change within the feature. For more information on the application of these models to particular TSV geometries, the authors recommend the papers by Moffat and Josell.^{58–62,78}

C. S-NDR model

As mentioned above, superconformal bottom-up filling is also possible in chemistries containing only chloride and suppressor additives. The suppressor based mechanism is dependent on applied overpotential, additive concentrations, and solution replenishment, which influences additive diffusion throughout the features.^{16,63–79} For Cu electroplating, the halide concentration (typically chloride ions) and the concentration of the suppressing additive (typically a polyether molecule), in particular, are instrumental in defining the process window where superconformal filling can occur due

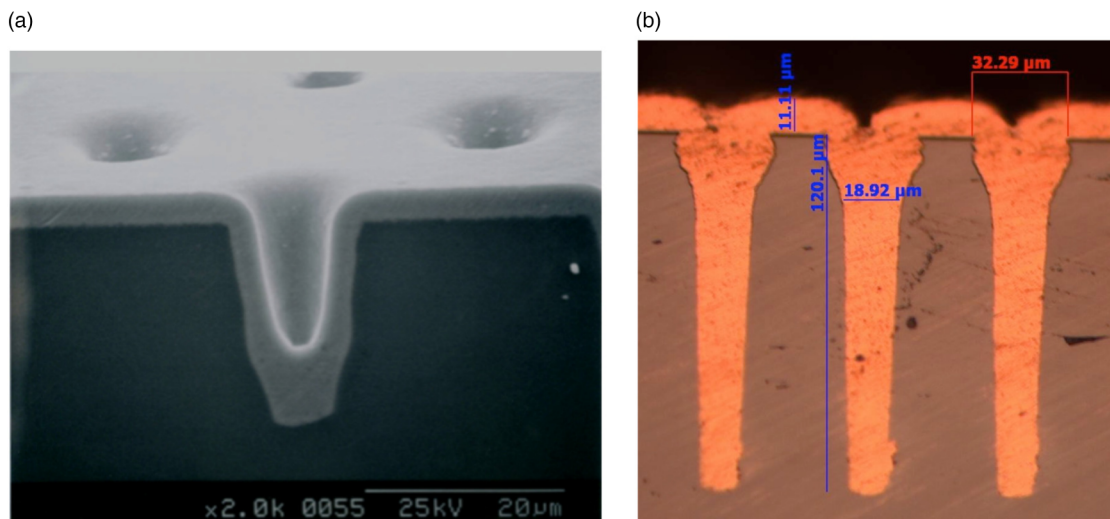


FIG. 8. (a) Scanning electron micrograph showing a superconformal filling profile for a Cu-filled via. (Ref. 72). Reproduced with permission from Spiesshoefer *et al.*, *J. Vac. Sci. Technol. A* **23**(4), 824 (2005). Copyright 2005, American Vacuum Society. (b) Optical micrograph showing cross-sectional views of a set of Cu-filled vias. Via diameter is $\sim 20 \mu\text{m}$, and via depth is $120 \mu\text{m}$.

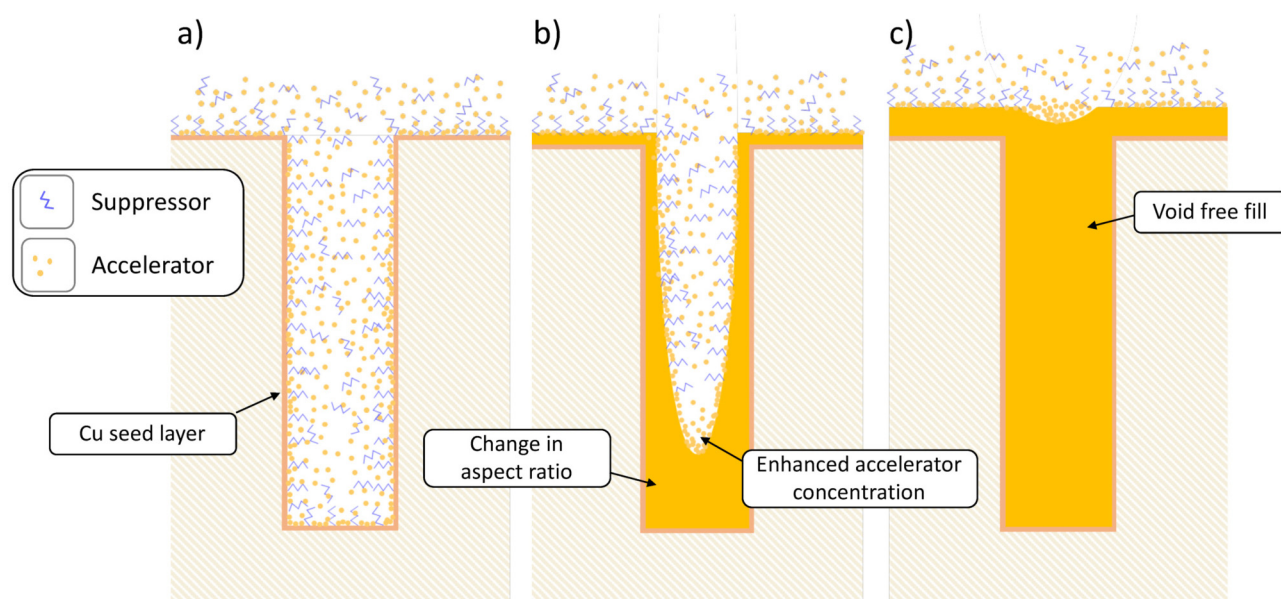


FIG. 9. Schematic representation of the CEAC mechanism: (a) the incubation period where deposition begins conformally; subsequent area change leads to the build-up of accelerator coverage on the bottom high curvature segments of the U-shaped region of the trench leading to (b) superconformal growth as a result of increased accelerator concentration at the center of the via. (c) Excess accelerator concentration collected above the filled features results in overburden bumps. Adapted from Lee and Chen, *Metals* **8**, 338 (2018). Copyright 2018 Author(s), licensed under a Creative Commons Attribution 4.0 License (Ref. 76).

to interaction between the adsorption of the chloride and the polyether compound.^{64,80}

The addition of suppressor additives to the electrolyte affects the relationship between potential and current in the cell. The effects of suppressor molecules are typically analyzed using cyclic voltammetry, in which the voltage is swept from the open circuit potential (OCP) to more negative potential and then back to OCP while measuring the resultant current. In an electrolyte without suppressor additives, there is a relatively linear relationship between current and potential that does not exhibit hysteresis. A schematic of a postexperiment IR corrected voltammogram for a chemistry containing suppressor additives is shown in Fig. 10. In this schematic, the potential is swept from the OCP [near Fig. 10(a)] to a point where suppressor breakdown begins to occur (b). At that point, a large reductive current begins to flow (c) and is a representative of metal deposition. A higher current is measured on the positive return sweep back to OCP when compared to the negative sweep. When the plot is corrected for IR loss in the electrochemical cell, the hysteresis exhibits negative differential resistance and the shape of the curve resembles an “S” leading to the term S-NDR.^{63,64} In the S-NDR system, deposition occurs where the suppression layer is disrupted because of overpotential driven transitions in the halide adlayer.^{63,64}

Bottom-up growth is achieved by applying a potential within the region between Figs. 10(b) and 10(c). At this point, it is possible to achieve a bifurcating behavior where deposition occurs within the vias and no deposition occurs on the surface.⁶³ Some effects of this bistable system in which deposition is suppressed in

some areas and active in others are the emergence of Turing patterns on electrode surfaces.^{16,63}

The amount of suppression within the TSV is dependent on the transport characteristics of the suppressor molecule and as a result, this process is sensitive to initial conditions.⁶³ The location at which deposition initiates depends on the additive concentrations and the applied overpotential. At higher overpotentials, deposition initiates further up in the TSV as is shown in Fig. 11.⁶⁵ For a given suppressor concentration, too low of a voltage results in no deposition. As more negative voltage is applied, localization of the deposition at the bottom of the feature can be achieved. Moving to even more negative potential can lead to conformal deposition and then finally further negative potential pushes the deposition high up in the feature, which ultimately results in pinch off and void formation.

The different filling profiles are highly dependent on chemistry composition as well as feature geometry. For some combinations of electrolyte and geometry, a single potential can be applied to result in bottom-up growth from a positive feedback interaction between the chloride, suppressor, and Cu reduction. Other combinations of chemistry and geometry result in a passive and active deposition profile.^{64,79,81} In a system that exhibits the passive and active fill profile, the deposition initiates as a position within the via and will grow from the outside of the feature to the center but not progress up the via. This quenching of the deposition results from a combination of metal ion depletion or over suppression. To overcome this effect, potential stepping can be used to sequentially advance the location of deposition higher and higher up the TSV.^{16,64,82} Figure 12 depicts potential stepping at 1 h intervals and

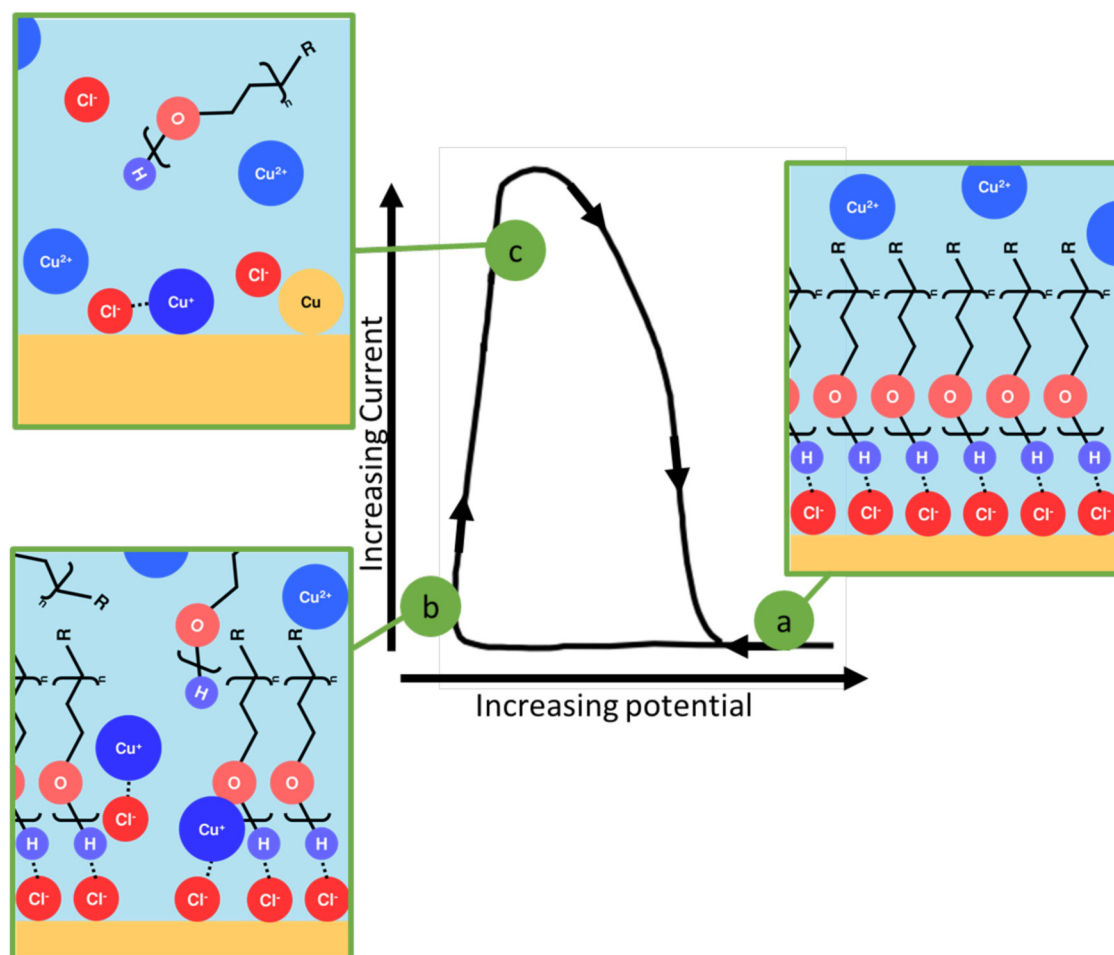


FIG. 10. Schematic representation of the S-shaped negative differential current mechanism. The curve represents a cyclic voltammogram. From positions (a) and (b), Cu plating is suppressed. At (b), suppressor breakdown occurs. Between (b) and (c), negative differential resistance is observed after correcting for IR loss in the bath. Hysteresis results from a positive feedback mechanism between the suppressor and chloride, reducing the overpotential needed for deposition after the suppressor breakdown potential has been achieved. Note that this representation is meant to illustrate the S-NDR mechanism and the angle between the polymer backbone and copper surface may be inaccurate.

1.5 h intervals to control the advancement of localized deposition and fill millimeter sized TSVs.⁷⁹

Over the past couple of decades, the understanding of the underlying mechanisms behind superconformal Cu deposition through plating with additives has evolved. Originally, all four additives were carried over into TSV plating in addition to pulsed plating, but recent development of the CEAC and S-NDR models have led to the realization that single additive systems with DC plating can result in void-free Cu filling. Pulsed plating, such as PPR, can be used to affect the fill profile in a plating system with a given chemical composition, but the most efficient way to achieve void-free filling is through tailoring the additive concentrations for a given feature geometry. The CEAC mechanism can be used to achieve superconformal growth but void-free filling with this approach is dependent on the aspect ratio and overall geometry of

the vias. The S-NDR model can be used to achieve void-free filling by understanding the relationship between feature geometry, applied overpotential, and additive concentrations.

V. WAFER THINNING

After the blind vias are filled by ECD, excess Cu needs to be removed from the front and the vias need to be opened from the back. Generally, this occurs through a series of CMP, wafer grinding, and dry etch processes.

ECD typically results in excess metal deposited on the surface of the wafer referred to as overburden. This excess material is removed by a series of CMP steps that are thoroughly covered in the literature.^{83,84} Before removing the overburden, there is a thermal annealing step to relieve stress associated with the coefficient of thermal

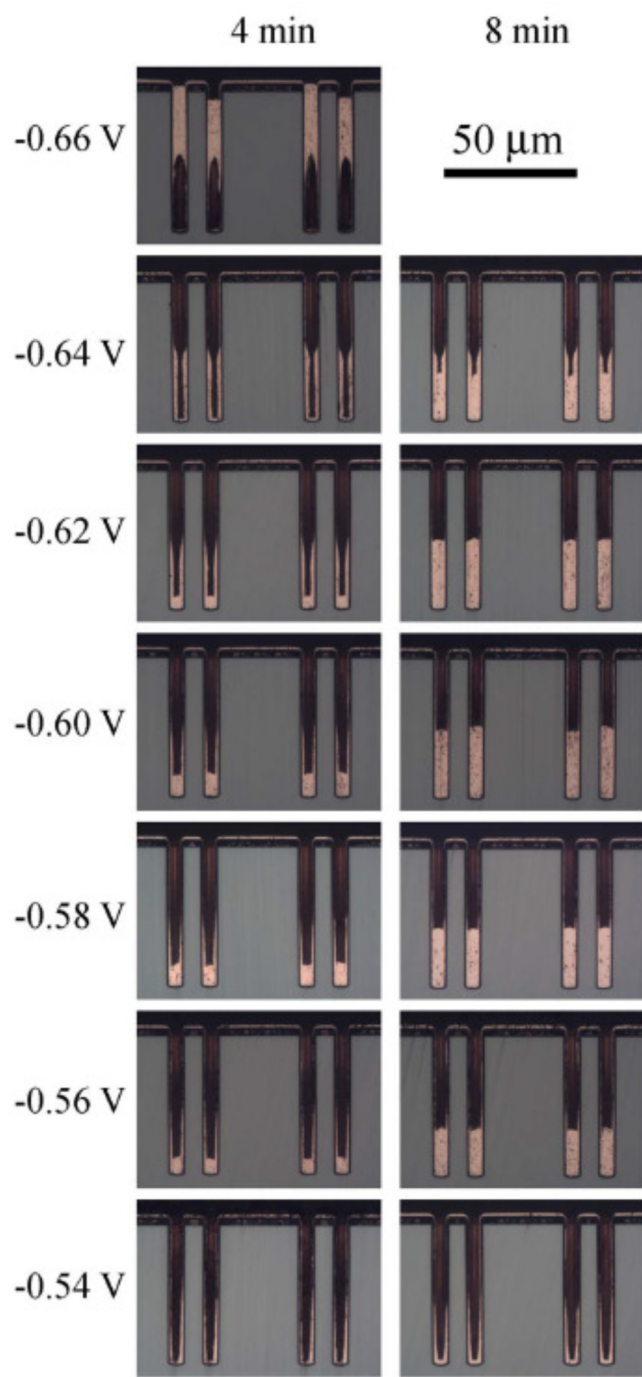


FIG. 11. Cross-sectional micrographs of Cu plating initiating in TSVs at different potentials. At higher overpotentials (lower potentials at the top of the figure), plating initiates higher up in the TSV than at the lower overpotentials in the bottom of the figure. Reprinted with permission from Josell and Moffat, *J. Electrochem. Soc.* **165**, D23 (2018). Copyright 2018, The Electrochemical Society.

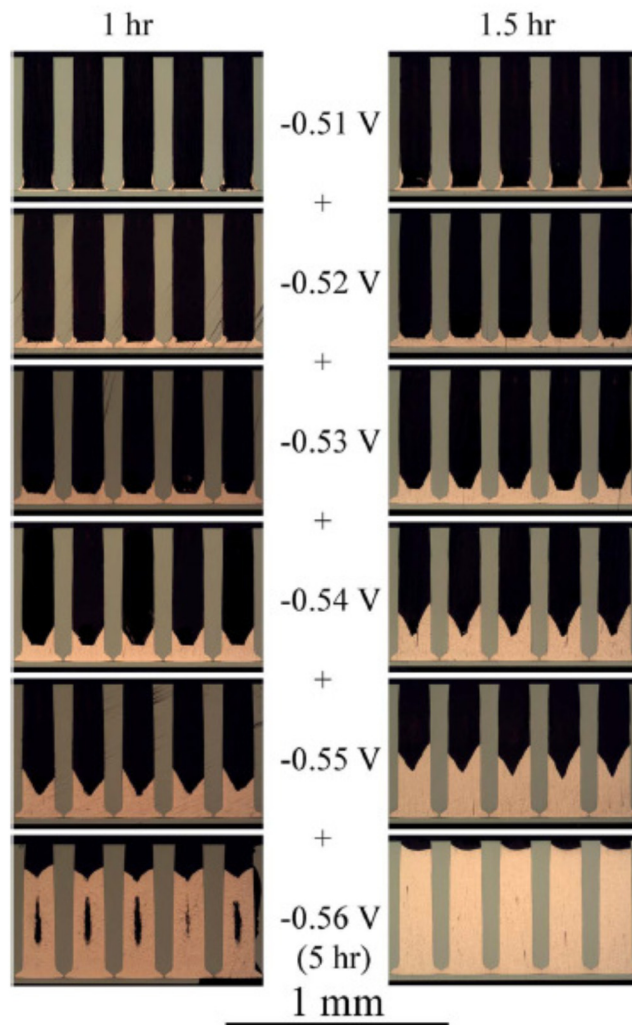


FIG. 12. Potential stepping at 1 h intervals and 1.5 h intervals to fill and increase the deposition rate of large TSVs. Reprinted with permission from Josell *et al.*, *J. Electrochem. Soc.* **166**, D3254 (2019). Copyright 2019, The Electrochemical Society.

expansion (CTE) mismatch between the Si and the Cu-filled TSVs. If Cu is not annealed, the CTE mismatch can lead to Cu swelling during subsequent process steps or during device operation which can result in stress, dielectric cracking, delamination, and other reliability concerns.^{2,85} This annealing step is referred to as Cu pumping and is often performed after the TSV overburden is removed so that Cu has a free surface to expand into. During the anneal, Cu protrudes from the surface of the via. This protrusion is a plastic deformation process in which the grain size and structure are reordered within the via such that the protrusion becomes permanent until it is later eliminated with an additional CMP step.⁸⁵ In addition to the anneal, design rules on the volume of Cu, pitch of the TSVs, and the distance

between active circuitry sensitive to stress are often utilized to avoid performance and reliability issues.

After removing the overburden and annealing Cu, wafer thinning is performed to reveal the TSV from the backside of the substrate. This is done in two phases: bulk and fine material removal. A carrier wafer is used for handling with a temporary bonding adhesive sandwiched between the process and carrier wafers. After bonding, the process wafer is thinned from the backside using a wafer grinding or lapping tool. These mechanical thinning tools are capable of removing material very quickly, while maintaining wafer planarity. Endpointing of the coarse removal can be done by targeting a specific wafer thickness, based on measured removal rates, or by incorporating large etched patterns or blaret holes in the front side of the wafer. ARDE is used to form the blaret holes at the same time as the TSVs are etched. The blaret holes are intentionally patterned as

larger features than the TSVs resulting in the RIE proceeding deeper into Si. These deeper blaret holes are opened by the mechanical polish before the TSVs allowing for an accurate end point.⁸⁶ For fine material removal, mechanical polishing is performed to remove surface damage created by the grinding step and reduce surface roughness for subsequent backside patterning. Chemical etching can also be used to relieve the stresses caused by grinding. The etchant spray is often a mixture of hydrofluoric, nitric, and phosphoric acids, where the nitric acid oxidizes the surface of the Si and hydrofluoric acid removes this oxide.

Further backside processing of the thinned wafer is performed to form a pad compatible with flip chip bonding. One possible integration scheme is outlined in Fig. 13.¹⁴ In this case, the final interconnection of the backside of the vias is made utilizing a Cu fill and etch back process.

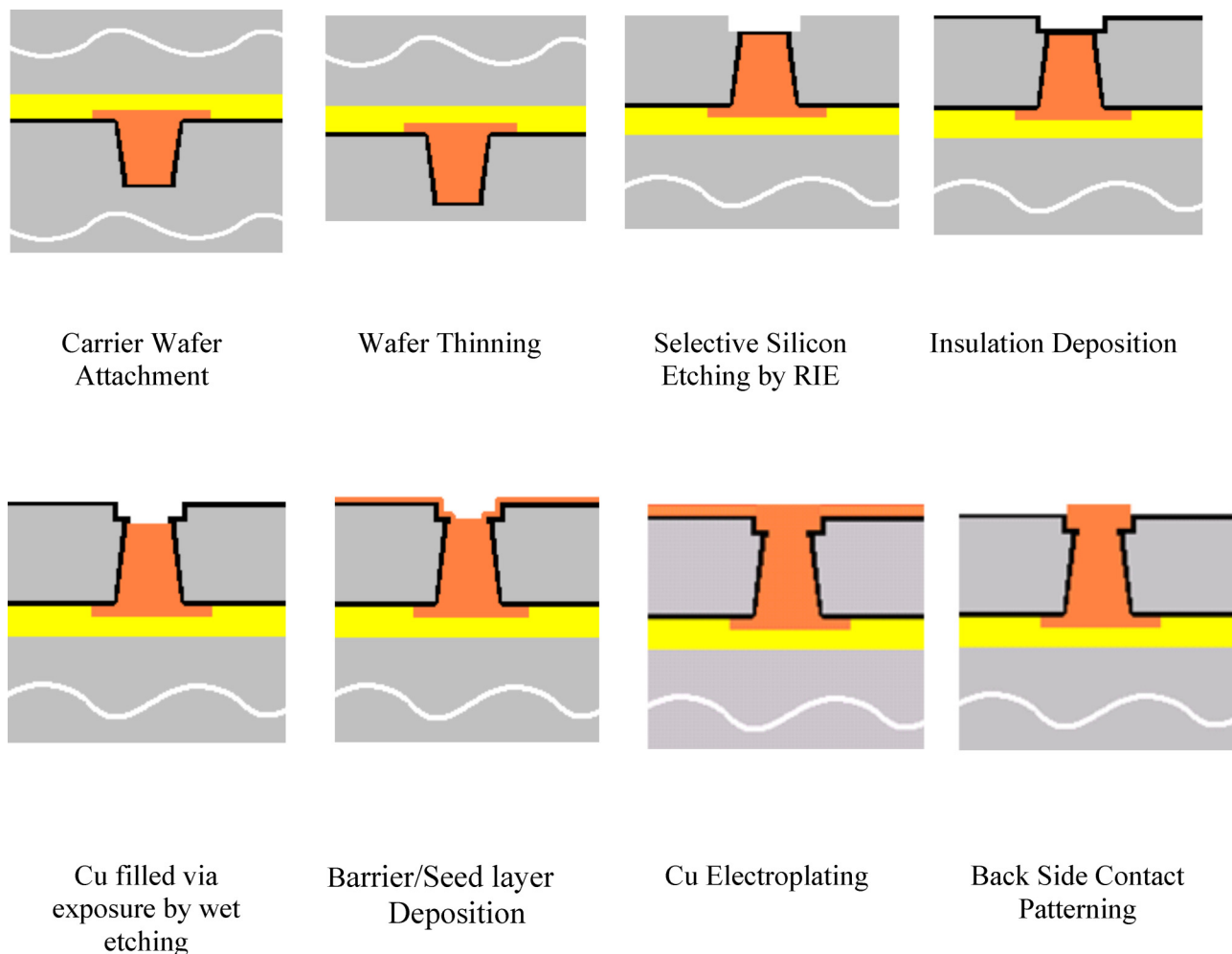


FIG. 13. Schematic illustrating the process flow used in processing the backside when fabricating TSVs for contact to the bottom side.

VI. SUMMARY

In this paper, a tutorial is provided for the general process steps necessary to fabricate through-silicon vias, an enabling technology for microelectronics integration. The processes include DRIE of silicon to form the via, thin film deposition to line the via sidewall, ECD of Cu to fill the vias from the bottom up, and wafer thinning to reveal the TSV from the wafer backside. The importance for controlling the DRIE process is highlighted to create a sidewall taper to assist with liner, barrier, and seed layer deposition. Three ECD mechanisms are summarized including periodic pulse PPR, a CEAC model related to the accelerator additive, and an S-NDR model related to suppressor coverage and breakdown. Finally, an overview of wafer thinning is presented.

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