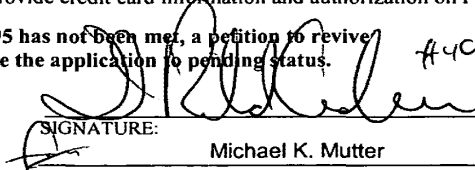


FORM PTO 1390 (REV 10-2003)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 0365-0601PUS1
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371			U.S. APPLICATION NO. (If known, see 37 CFR 1.5) 10/502336
INTERNATIONAL APPLICATION NO. PCT/FI03/00065	INTERNATIONAL FILING DATE 28 January 2003	PRIORITY DATE CLAIMED 31 January 2002	
TITLE OF INVENTION METHOD FOR EMBEDDING A COMPONENT IN A BASE			
APPLICANT(S) FOR DO/EO/US Risto TUOMINEN			
Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:			
1. ☒ This is a FIRST submission of items concerning a filing under 35 U.S.C. 371. 2. ☐ This is a SECOND or SUBSEQUENT submission of items concerning a filing 35 U.S.C. 371. 3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371 (f)). The submission must include items (5), (6), (9) and (21) indicated below. 4. ☒ The US has been elected (Article 31). 5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c)(2)) a. ☐ is attached hereto (required only if not communicated by the International Bureau). b. ☒ has been communicated by the International Bureau. c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US). 6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371 (c)(2)). a. ☒ is attached hereto. b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4). 7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3)) a. ☐ are attached hereto (required only if not communicated by the International Bureau). b. ☐ have been communicated by the International Bureau. c. ☐ have not been made; however, the time limit for making such amendments has NOT expired. d. ☒ have not been made and will not be made. 8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)). 9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)). 10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).			
Items 11 to 20 below concern document(s) or information included:			
11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98. 12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included. 13. ☐ A preliminary amendment. 14. ☒ An Application Data Sheet under 37 CFR 1.76. 15. ☐ A substitute specification. 16. ☐ A power of attorney and/or change of address letter. 17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 37 CFR 1.821 - 1.825. 18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4). 19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4). 20. ☒ Other items or information: Drawings - Twelve (12) Sheets			

JT12 Rec'd PCT/PTO 23 JUL 2004

U.S. APPLICATION NO. (if known, see 37 CFR 1.49) 107502336		INTERNATIONAL APPLICATION NO. PCT/FI03/00065		ATTORNEY'S DOCKET NUMBER 0365-0601PUS1	
21. ☒ The following fees are submitted:				CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):					
☒ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO \$1080.00					
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO \$920.00					
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO \$770.00					
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) \$730.00					
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) \$100.00					
ENTER APPROPRIATE BASIC FEE AMOUNT =					
Surcharge of \$130.00 for furnishing the oath or declaration later than 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).				\$ 1,080.00	
				\$ 130.00	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	29-20 =	9	x 18.00	\$ 162.00	
Independent claims	1-3 =		x	\$ 0.00	
MULTIPLE DEPENDENT CLAIM(s) (if applicable)			+ 290.00	\$ 290.00	
TOTAL OF ABOVE CALCULATIONS =				\$ 1,662.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.					
SUBTOTAL =				\$ 1,662.00	
Processing fee of \$130.00 for furnishing the English translation later than 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).					
TOTAL NATIONAL FEE =				\$ 1,662.00	
Fee for recording the enclosed assignment (37 CFR 1.21 (h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property				+ \$	
TOTAL FEES ENCLOSED =				\$ 1,662.00	
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b. ☐ Please charge my Deposit Account No. _____ in the amount of \$ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.					
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d. ☐ Fees are to be charged to a credit card. WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.					
NOTE: Where an appropriate time limit under 37 CFR 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.					
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CUSTOMER NUMBER: 02292 July 23, 2004 /clb				SIGNATURE:  NAME: Michael K. Mutter	
				29,680	
REGISTRATION NUMBER					

METHOD FOR EMBEDDING A COMPONENT IN A BASE

The present invention relates to a method for embedding one or more components in a base.

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The bases that are processed using the methods to which the present invention relates are used as bases for electrical components, typically semiconductor components and particularly microcircuits, in electronic products. The task of the base is to provide a mechanical attachment base for the components and the necessary electrical connections to the other components on the base and outside the base. The base can be a circuit board, so that the method that is the object of the invention is closely related to circuit-board manufacturing technology. The base can also be some other base, for example, a base used for packaging a component or components, or the base of an entire functional module.

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Circuit-board manufacturing technologies differ from microcircuit manufacture in, among other things, the fact that the substrate used in microcircuit manufacturing technologies is a semiconductor material, whereas the base material of a circuit board is an insulator. Microcircuit manufacturing technologies are also typically considerably more expensive than circuit-board manufacturing technologies.

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Circuit-board manufacturing technologies differ from packaging techniques in that packaging techniques are intended to form a package around a semiconductor component, which will facilitate its handling. The surface of a package of a semiconductor component has contact parts, typically protrusions, which allow the packaged component to be easily installed on a circuit board. A semiconductor package also contains conductors, through which voltage can be connected to the actual semiconductor, connecting the protruding contact parts outside the package to the contact areas on the surface of the semiconductor component.

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However, the packages of components manufactured using conventional technologies take up a considerable amount of space. The miniaturization of electronic devices has

led to an attempt to eliminate the packaging of semiconductor components. For this purpose, the so-called flip-chip technology for instance, has been developed, in which a semiconductor component without a package is assembled directly onto the surface of the circuit board. There are, however, many difficulties in flip-chip technology. For example, problems can arise with the reliability of connections, especially in applications in which mechanical stresses arise between the circuit board and the semiconductor component. Mechanical stresses must be evened by adding a suitable underfill between the chip and the circuit board. This procedure slows down the process and increases manufacturing costs. Stresses arise particularly in applications in which a flexible circuit board is used and the circuit board is flexed strongly.

Object of the invention is to create a method, by means of which unpacked microcircuits can be embedded to a base reliably but economically.

The invention is based on embedding the semiconductor components, or at least some of them, in a base, such as a circuit board, during the manufacture of the board, whereby part of the base structure is, as it were, manufactured around the semiconductor components. According to the invention, feed-throughs for semiconductor components are made in the base in such a way that the holes extend between the first and second surfaces of the base. After the holes have been made, a polymer film is spread over the second surface of the base structure in such a way that the polymer film also covers the feed-throughs made for the semiconductor components, from the second side of the base structure. Before the hardening of the polymer film, or after partial hardening, the semiconductor components are placed, from the direction of the first side of the base, in the holes that have been made. The semiconductor components are pressed against the polymer film so that they adhere to the polymer film. After this, the final hardening of the polymer film is carried out. According to the invention, a conductive pattern is made in the base, before a component is placed in the holes, and the component is placed in the hole in such a way that the component is aligned in relation to the conductive patterns made on the baseboard.

More specifically, the method according to the invention is characterized by what is

stated in the characterizing portion of Claim 1.

Considerable advantages are gained with the aid of the invention. This is because, with the aid of the invention, a circuit board can be manufactured with the semiconductor components embedded inside it. The invention also makes it possible to manufacture a small and reliable component package around a component.

The invention also permits a large number of embodiments, which provide significant additional advantages.

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For example, with the aid of preferred embodiments of the invention, the component's packaging stage, the circuit board's manufacturing stage, and the assembly and contact-making stage of the semiconductor components can be combined to form a single totality. The combination of the various process stages brings important logistic benefits and permits the manufacture of a smaller and more reliable electronic module. There is the further advantage that such a manufacturing method can largely exploit circuit board manufacturing and assembly technologies that are in general use.

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According to a preferred embodiment of the invention, the totality of the composite process is simpler than, for example, using flip-chip technology to manufacture a circuit board and attach the components to the circuit board. By means of such preferred embodiments, the following advantages over the conventional solution are obtained:

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- Soldering is not required to form contacts with the components, instead an electrical contact can be manufactured by growing conductors on top of the contact areas of a semiconductor component. This means that there is no need to use molten metal to connect the components, so that compounds are not formed between metals. Compounds between metals are generally brittle, so that reliability is improved compared to connections made by soldering. Particularly in small connections, the brittleness of the metal compounds in the connections causes great problems. According to a preferred embodiment, it is possible to achieve clearly smaller structures in a solderless solution than in soldered

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solutions. The solderless contact-making method also has the advantage that high temperatures are not required to form contacts. A lower process temperature permits greater choice when selecting other materials of the circuit board, the component package, or the electronics module. In the method, the temperature of the circuit board, the component, and the conductive layer directly connected to the component can be kept in the range 20 - 85°C. Higher temperatures, for example, of about 150°C, may be needed only when curing (polymerizing) the polymer films used. However, the temperature of the baseboard and the components can be kept under 200°C during the entire process. If the method employs polymer films that are hardened in other ways than due to the effect of a high temperature, for example, chemically, or by electromagnetic radiation, the temperature of the baseboard and the components can, in a preferred embodiment, be kept under 100°C during the entire process.

- Because the use of the method permits the manufacture of smaller structures, the components can be spaced more closely. The conductors between the components can then also be shorter while the electrical properties of the electronic circuit improve, for example, by reducing losses, interference, and delay times.

- The method also permits the manufacture of three-dimensional structures, as the bases and the components embedded in the bases can be assembled on top of each other.

- In the method, it is also possible to reduce the interfaces between different metals.

- The method permits a lead-free process.

The invention also permits other preferred embodiments. In connection with the invention, flexible circuit boards, for instance, can be used. Further, the process permits

circuit boards to be assembled on top of each other.

With the aid of the invention, it is also possible to manufacture extremely thin structures, in which the semiconductor components are, despite its thinness, entirely protected
5 within a base, such as a circuit board.

Because the semiconductor components can be placed entirely inside the circuit board, the joints between the circuit board and the semiconductor components are mechanically durable and reliable.

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In the following, the invention is examined with the aid of examples and with reference to the accompanying drawings.

Figure 1 shows a series of cross-sections of one process according to the invention.

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Figure 2 shows a series of cross-sections of a second process according to the invention.

Figure 3 shows a schematic diagram of one possible contact-forming method.

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Figure 4 shows a series of cross-sections of a third process according to the invention.

The series of illustrations shown in Figure 1 show one possible process according to the invention. In the following, the process of Figure 1 is examined in stages:

25 **Stage A (Figure 1A):**

In stage A, a suitable baseboard 1 is selected for the circuit-board manufacturing process. The baseboard 1 can be, for example, a glass-fibre reinforced epoxy board, such as an FR4-type board. In the example process, the baseboard 1 can thus be an organic
30 board, as the example process does not require high temperatures. A flexible and cheap organic board can thus be selected for the baseboard 1. Typically a board that is already coated with a conductive material 2, usually copper, is selected for the baseboard 1. Of

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course, an inorganic board can also be used.

Stage B (Figure 1B):

- 5 In stage B, through holes 3 are made in the baseboard for electrical contacts. The holes 3 can be made, for example, with some known method used in circuit-board manufacture, such as mechanical drilling.

Stage C (Figure 1C):

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In stage C, metal is grown into the through holes made in stage B. In the example process, the metal 4 is also grown on top of the circuit board, thus also increasing the thickness of the conductive layer 2.

- 15 The conductive material 4 to be grown is copper, or some other material with sufficient electrical conductivity. Copper metallizing can take place by coating the holes with a thin layer of chemical copper and then continuing the coating using an electrochemical copper-growing method. Chemical copper is used in the example, as it will also surface on top of a polymer and act as an electrical conductor in electrochemical coating. The
20 metal can thus be grown using a wet-chemical method, so that the growth is cheap. Alternatively, the conductive layer 4 can be made, for example, by filling the through holes with an electrically conductive paste.

Stage D (Figure 1D):

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In stage D, the conductive layer on the surface of the circuit board is patterned. This can be done by utilizing generally known circuit-board manufacturing methods. The patterning of the conductive layer is aligned, for example, on the holes made in stage B.

- 30 The manufacture of the conductor pattern can take place, for example, by laminating, on the surface of the metal 4, a photolithographic polymer film, on which the desired conductive pattern is formed by directing light through a patterned mask. After

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- exposure, the polymer film is developed, when the desired areas are removed from it and the copper 4 under the polymer is revealed. Next, the copper revealed under the film is etched away, leaving the desired conductive pattern. The polymer acts as a so-called etching mask and openings 5, at the foot of which the baseboard of the circuit board is revealed, are formed in the metal layer 4. After this, the polymer film is also removed from on top of the copper 4.

Stage E (Figure 1E):

- 10 In stage E, holes 6 are made in the baseboard for the microcircuits. The holes extend through the entire baseboard, from the first surface 1a to the second surface 1b. The holes may be made, for example, mechanically milling by means of a milling machine. The holes 6 can also be made, for example, by stamping. The holes 6 are aligned relative to the conductive patterns 4 of the circuit board. The holes 3 made during stage B can
15 also be used to aid alignment, but then too the alignment is relative to the conductive patterns 4, as the conductive patterns 4 have a specific position in relation to the holes 3.

Stage F (Figure 1F):

- 20 In stage F, a polymer film 7 forming an electrical insulation is made on the second surface 1b of the baseboard and over the holes 6. The polymer film 7 is made in such a way that it is sufficiently rigid to retain the main features of its shape, but, however, not hardened, so that components can be attached by pressing them into the film. The polymer film should also be sufficiently rigid to be able to hold the components pressed
25 into the film essentially immovable in relation to the base, during the following process stages.

The polymer film made in Stage F can be, for example, a pre-preg-type film.

- 30 If desired, a metal coating 8 can also be made on top of the polymer film 7 in stage F.

In the example process, stage F is carried out by laminating a thin polymer film (e.g., c.

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40 μm) on the surface of the circuit board, on top of which is a layer of copper (e.g., c. 5 μm). Lamination takes place with the aid of pressure and heat. In the example process, the film is thus an RCC (Resin Coated Copper) foil. The lamination must then be carried out to be uncompleted, so that the polymer is not completely hardened. This is achieved
5 by setting the laminating temperature sufficiently low and/or by shortening the duration of the heat treatment.

Stage G (Figure 1G):

- 10 In stage G, the microcircuits 18 are assembled in the holes 6, from the side of the first surface 1a of the baseboard. Assembly can take place using a precision assembly machine, the microcircuits 18 being aligned relative to the conductive patterns of the circuit board. As in stage E, the holes made in stage B can be used to aid alignment.
- 15 The microcircuits 18 are assembled in such a way that they adhere to polymer film 7 in the 'bottoms' of the holes 6. The most suitable way to carry out assembly is to use such a force that the microcircuits 18 push slightly inside the polymer film 7, so that the microcircuits are made to remain in place better. It is also advantageous to the process, if the microcircuits being assembled have contact protrusions 9, which penetrate inside the
20 polymer film 7.

Figure 3 shows an interesting alternative embodiment, in which the contact protrusions 9 of the microcircuits are so long that they extend right through the polymer film 7 to the metal coating 8. In that case, there is no need to make holes in the polymer film 7 (Stage
25 K) for making contacts in the microcircuits, as the holes are formed in connection with the assembly of the components. In addition, the metallizing stage (Stage L) of the holes can be simplified, as the contact protrusions 9 automatically form conductor columns through the polymer film 7. In the embodiment of Figure 3, the contact protrusions can also be given a sharp shape, so that their penetration ability improves. If the contact
30 protrusions 9 are sufficiently long and sharp, they can also penetrate the metal coating 8 and in principle form an electrical contact between the microcircuit 18 and the metal

coating 8.

Stage H (not shown):

- 5 In stage H, the polymer film 7 is hardened with the aid of curing. Curing generally comprises a heat treatment, but the process can also employ some treatment other than heat to harden the polymer. If desired, stage H can also be omitted, particularly in connection with polymers cured by heat treatment. However, hardening the polymer at this stage prevents the microcircuit from moving relative to the base during stage I.

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Stage I (Figure 1D):

- In stage I, the microcircuits are secured to the baseboard of the circuit board by filling the holes made for the microcircuits with a filler material 10. In the example process, this stage is carried out by spreading casting epoxy into the holes from the first surface (1a) of the circuit board and on top of the microcircuits. The epoxy is smoothed with a spatula and hardened by curing in an autoclave. At the same time, the polymer film 7 is also hardened, if the process does not include stage H.

20 **Stage J (Figure 1J):**

- In stage J, a polymer film 11 is formed on the first surface (1a) of the circuit board, followed by a thin metal coating 12 on top of the polymer film.
- 25 In the example process, stage J is carried out by laminating a thin polymer film (e.g., c. 40 μm) on the surface of the circuit board, on top of which is a layer of copper (e.g., c. 5 μm). Lamination takes place with the aid of pressure and heat. In the example process, the film is thus an RCC (Resin Coated Copper) foil.
- 30 The polymer film can also be made by, for example, spreading polymer in a liquid form on the circuit board. Thus lamination is not essential in stage J. What is essential is that

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an insulating layer, typically a polymer film, is made on the circuit board, which contains the embedded components, particularly embedded microcircuits. The polymer film itself can be, according to the embodiment, a filled or unfilled polymer film. The polymer film can also be coated with metal, but this is not essential, as the conductive surface can also be made later, on top of a polymer layer that is already attached to the circuit board.

Stage J makes it possible to use conventional manufacturing methods and work stages used in circuit board manufacture in the example process and nevertheless to be able to bury microcircuits and other components inside the circuit board.

Stage K (Figure 1K)

In stage K, holes 13 are made in the polymer films 7 and 11 (and at the same time in the conductive foils 8 and 12), through which it is possible to create contacts with the conductive patterns and feed-throughs (conductive material 4) of the circuit board and with the microcircuits.

The holes 13 can be made, for example, using a laser, or some other suitable method. The conductive patterns made in stage D, or the through holes made in stage B can be used for alignment.

Stage L (Figure 1L):

Stage L corresponds to stage C. In stage L, a conductive layer 14 is made in the holes 13 and on the surfaces of the circuit board.

In the example process, the feed-throughs (holes 13) are first of all cleaned using a three-stage desmear treatment. After this, the feed-throughs are metallized by first forming a catalysing SnPd surface on the polymer and after that depositing a thin layer (about 2 Fm) of chemical copper onto the surface. The thickness of the copper 14 is increased by electrochemical deposition.

Alternatively, the feed-throughs can be filled with an electrically conductive paste or made using some other suitable micro-via metallizing method.

5 **Stage M (Figure 1M):**

In stage M, a conductive pattern is formed in the same way as in stage D.

10 **Stages N and O (Figures 1N and 1O):**

In stages N and O, a photolithographic polymer 14 is spread on the surface of the circuit board and the desired pattern is formed in the polymer 14 (in a manner similar to that in stages D and M). The exposed polymer film is developed, but the polymer film pattern remaining on the circuit board is not removed.

15 **Stage P (Figure 1P):**

In stage P, the connection areas of the polymer film pattern formed in the previous stage are coated 16. The coating 16 can be made with, for example, a Ni/Au coating, or an
20 OSP (organic surface protection).

The example of Figure 1 depicts one process, which can be used to exploit our invention. Our invention is thus in no way restricted to the process described above, but
25 instead the invention covers a large group of different process and their end products, to the full extent of the Claims and allowing for equivalency interpretations. In particular, the invention is in no way restricted to the layout shown in the example, instead it will be obvious to one versed in the art that the processes according to our invention can be used to manufacture many kinds of circuit boards, which differ greatly from the
30 examples disclosed here. Thus, the microcircuits and connections of the figures are only shown to illustrate the manufacturing process.

A great many changes can thus be made to the process of the example disclosed above, without nevertheless deviating from the idea according to the invention. The changes can relate to the manufacturing techniques depicted in the various stages, or, for example, to the mutual sequence of the stages. For example, stage B can equally well be carried out after stage D, i.e. the procedure can be to align the drill on the pattern, instead of aligning the pattern on the drilled holes. Correspondingly, the order of stages D and E can also be reversed. The component holes 6 are then made before the conductive patterns are formed. In that case, the conductive pattern is aligned relative to the holes 6 (and also the holes 3). Irrespective of the order in which stages B, D, and E are carried out, the polymer film 7 to be made in stage F covers the holes 6 and the conductive pattern formed on the second surface 1b of the baseboard.

Stages that are felt to be required can also be added to the process of the example disclosed above. For example, a foil that protects the surface of the circuit board during the casting taking place in stage H can be laminated onto the first side (1a) of the circuit board. Such a protective foil is manufactured so that it covers all the other areas except for the holes 6. The protective foil keeps the surface of the circuit board clean when the casting epoxy is spread with the spatula. The protective foil can be made in a suitable stage before stage I and removed from the surface of the circuit board immediately after the casting.

With the aid of the method, it is also possible to manufacture component packets to be attached to the circuit board. Such packets can also include several semiconductor components, which are connected electrically to each other.

The method can also be used to manufacture entire electrical modules. The process shown in Figure 1 can also be applied in such a way that the conductive structure is made only on the second side (1b) of the circuit board, to which the contact surfaces of the microcircuit are oriented.

The method makes it possible to manufacture, for example, circuit boards or electrical modules, in which the thickness of the baseboard used is in the range 50 - 200 microns

and the thickness of the microcircuit and microcircuits is in the range 50 - 150 microns. The pitch of the conductors can vary, for example, in the range 50 - 250 microns while the diameter of the micro-feed-throughs can be, for example, 15 - 50 microns. Thus, the total thickness of a single board in a one-layer construction will be about 100 - 300
5 microns.

The invention can also be applied in such a way that circuit boards are assembled on top of each other, thus forming a multi-layer circuit structure, in which there are several circuit boards manufactured according to Figure 1 set on top of each other and connected
10 electrically to each other. The circuit boards set on top of each other can also be circuit boards in which the conductive structure is formed only on the second side 1b of the circuit board, but which nevertheless include feed throughs, through which an electrical contact can also be formed to the microcircuits from the first side of the circuit board. Figure 2 shows one such process.

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Figure 2 shows the connection of circuit boards to each other. In the following, the process is described in stages.

Stage 2A (Figure 2A):

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Stage 2A depicts the circuit boards being set on top of each other. The lowest circuit board can be obtained, for example, after stage J of a modified process of Figure 1. In this case, the process of Figure 1 is then modified by omitting stage 1C.

25 The middle and upper circuit boards in turn can be obtained after stage M of a modified process of Figure 1, for instance. In this case, the process of Figure 1 is modified by omitting stage 1C and performing stages J, K, and L on only the second side (1b) of the circuit board.

30 In addition to the circuit boards, Figure 2A also shows pre-preg epoxy layers 21 placed between the circuit boards.

Stage 2B (Figure 2B):

In stage 2B, the circuit boards are laminated together with the aid of pre-preg epoxy layers 21. In addition, a metal-coated polymer film 22 is made on the upper surface of the circuit board. The process corresponds to stage J of the process of Figure 1. In the example process, a metal-coated polymer film 22 is already on the under surface of the circuit board.

Stage 2C (Figure 2C):

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In stage 2C, holes 23, for the formation of contacts, are drilled in the circuit board.

After Stage 2C, the process can be continued for example as follows:

15 **Stage 2D:**

In stage 2D, conductive material is grown on top of the circuit board and in the through holes 23, in the same way as in stage 1C.

20 **Stage 2E:**

In stage 2E, the conductive layer on the surface of the circuit board is patterned in the same way as in stage 1D.

25 **Stage 2F:**

In stage 2F, a photolithographic polymer is spread on the surfaces of the circuit board and the desired pattern is formed in the polymer in the same way as in stages 1N and 1O. The exposed polymer film is developed, but the polymer film pattern remaining on the circuit board is not removed.

Stage 2G:

In stage 2G, the connection areas of the polymer film pattern formed in the previous stage are metallized in the same way as in stage 1P.

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On the basis of the example of Figure 2, it is obvious that the method can also be used to manufacture many kinds of three-dimensional circuit structures. For example, the method can be used in such a way that several memory circuits are placed on top of each other, thus forming a packet containing several memory circuits, in which the memory
10 circuits are connected to each other to form an operational totality. Such a packet can be termed a three-dimensional multichip module. The chips in such modules can be selected freely and the contacts between the chips can be easily made according to the selected circuits.

15 The invention also permits electromagnetic protection to be made around the component embedded in the base. This is because the method of Figure 1 can be modified in such a way that the holes 6 depicted in stage 1E can be made in connection with the making of the holes 3 carried out in stage 1B. In that case, the conductive layer 4 to be made in stage 1C will also cover the side walls of the holes 6 made for the components. Figure
20 4A shows a cross-section of the base structure as it is after stage 1F in the process modified in the aforesaid manner.

After the intermediate stage shown in Figure 4A, the process can be continued by assembling the microcircuits in a similar way to stage 1G, the polymer film being
25 hardened as in stage 1H, and the microcircuits being attached similarly to stage 1I. After this, polymer and metal foils can be formed on the first surface of the circuit board similarly to stage 1J. Figure 4B shows an example cross-section of the base structure after these process stages.

30 After the intermediate stage shown in Figure 4B, the process can be continued by making holes, similar to those of stage 1K, in the polymer film, for making contacts. After this, a conductive layer is made in the holes and on the surfaces of the board

similarly to stage 1L. Figure 4C shows an example cross-section of the base structure after these process stages. For reasons of clarity, the conductive layer made similarly to stage 1L in the holes and on the board surfaces is highlighted in black.

- 5 After the intermediate stage shown in Figure 4C, the process can be continued by patterning a conductive layer on the surfaces of the board as in stage 1M and by coating the surfaces of the board as in stage 1N. After these stages, the microcircuits are surrounded by a nearly unbroken metal foil, which forms an effective protection against interference caused by electromagnetic interaction. This construction is shown in Figure 10 4D. After the intermediate stage shown in Figure 4D, stages corresponding to stages 1O and 1P are carried out, in which a protective foil and connections are made on the surface of the circuit board.

- In Figure 4D, the cross-sections of the metal layers protecting the microcircuits are 15 highlighted in black. In addition, the background of the microcircuits is highlighted with cross-hatching. The cross-hatching is intended to be a reminder that all the sides of a hole made for a microcircuit are covered by a metal foil. Thus the microcircuit is surrounded laterally with an unbroken metal foil. In addition to this, a metal plate can be designed above the microcircuit, which is made in connection with the making of the 20 circuit board's conductive pattern. Similarly, a metal foil that is as complete as possible is made below the microcircuit. The making of contacts below the microcircuit means that small gaps must be made in the metal foil, as shown in Figure 4D, for instance. These gaps can, however, be made so narrow laterally, or, correspondingly, so thin vertically, that they do not weaken the protective effect obtained against electromagnetic 25 interference.

- When examining the example of Figure 4D, it must also be take into account that the final structure also contains parts extending at right angles to the plane shown in the figure. Such a structure extending at right angles is shown by the conductor connected to 30 the contact bump on the left-hand side of the left-hand microcircuit of Figure 4D, which runs towards the viewer from between the metal foil surrounding the microcircuit laterally and the conductive layers below the microcircuit.

The solution shown by Figure 4D thus provides the microcircuit with excellent protection against electromagnetic interference. As the protection is made immediately around the microcircuit, the construction also protects against mutual interference
5 arising between the components contained in the circuit board. Most of the electromagnetic protective structure can also be earthed, as the metal foil surrounding the microcircuits laterally can be connected electrically to the metal plate above the circuit. The connections of the circuit board, can, in turn, be designed in such a way that the metal plate is earthed through the conductive structure of the circuit board.

10

Claims:

1. A method for embedding at least one component in a base, which component has contact areas on its first surface, the method comprising
 - 5 - taking a baseboard of the base, the baseboard having a first surface and a second surface,
 - making conductive patterns on the baseboard and at least one hole for the at least one component, in such a way that each hole extends through the baseboard between the first surface and the second surface,
 - 10 - spreading an insulating polymer layer on the second surface of the baseboard, in such a way that the insulating polymer layer covers the at least one hole made for the component,
 - placing the at least one component in the at least one hole, in such a way that the component is aligned in relation to the conductive patterns made on the
 - 15 baseboard and the first surface of the component presses against the insulating polymer layer, and
 - hardening the insulating polymer layer.
2. A method according to Claim 1, in which the first surface of the component is pressed
20 into the unhardened insulating polymer layer.
3. A method according to Claim 1, in which the first surface of the component is pressed into the partly hardened insulating polymer layer.
- 25 4. A method according to any of Claims 1 - 3, in which the insulating polymer layer is manufactured by placing an RCC foil on the second surface of the baseboard.
- 30 5. A method according to any of Claims 1 - 3, in which the insulating polymer layer is manufactured by spreading a pre-preg epoxy film on the second surface of the baseboard.

19

6. A method according to any of Claims 1 - 5, in which insulating material is grown on the side walls of the hole made for a component, in order to create interference protection around the component.

5 7. A method according to any of Claims 1 - 6, in which the contact areas of the component have contact protrusions connected to them, and the component is placed in the hole in such a way that the contact protrusions push inside the insulating polymer layer.

10 8. A method according to any of Claims 1 - 6, in which the contact areas of the component have contact protrusions connected to them, the height of the contact protrusions being at least as great as the thickness of the insulating polymer layer, and the component is placed in the hole in such a way that the contact protrusions penetrate through the insulating polymer layer.

15

9. A method according to any of Claims 1 - 7, in which

- contact openings for the component are made in the hardened insulating polymer layer, and

20 - conductors for forming electrical contacts with the component are made in the contact openings and on top of the insulating polymer layer.

10. A method according to any of Claims 1 - 9, in which conductive patterns are made on at least the second surface (1b) of the baseboard, and in which the insulating polymer layer to be spread on the second surface (1b) of the baseboard is spread in such a way
25 that it covers the conductive patterns made on the second surface (1b).

11. A method according to any of Claims 1 - 10, in which the first surface of the component is pushed into the insulating polymer layer, which is in contact with the conductive patterns, which are formed from the conductive layer.

30

12. A method according to any of Claims 1 - 11, in which at least one set of conductive patterns are located between the insulating polymer layer, against which the first surface

20

of the component is pushed, and the baseboard of the circuit board.

13. A method according to any of Claims 1 - 12, in which the baseboard is of an insulating material.

5

14. A method according to any of Claims 1 - 13, in which the component is secured in place by filling a hole, made in the baseboard, with a filler material.

15. A method according to any of Claims 1 - 14, in which the component is a microcircuit and an electrical contact is formed with the microcircuit from the direction of the first surface of the baseboard, after the microcircuit has been placed in the hole made in the baseboard.

16. A method according to any of Claims 1 - 15, in which an electrical contact is formed with the component by growing conductive material in the contact areas of the component, or on top of its contact protrusions.

17. A method according to any of Claims 1 - 16, in which the electrical contact with the microcircuit is formed without solder using a circuit-board manufacturing technology.

20

18. A method according to any of Claims 1 - 17, in which more than one component is embedded in the base and in which a separate hole is made in the baseboard for each component to be embedded in the base and each component to be embedded in the base is located in its own hole.

25

19. A method according to any of Claims 1 - 18, in which a multi-layer structure is manufactured, in which there are at least four conductive layers on top of each other.

20. A method according to any of Claims 1 - 19, in which a first base, into which at least two microcircuits are embedded, and at least one second base, in which at least two microcircuits are embedded, are manufactured, and the bases are assembled and secured on top of each other in such a way that the bases are aligned in relation to each other.

30

21. A method according to any of Claims 1 - 19, in which

- a first and a second base and an intermediate layer are manufactured,
- the second base is placed above the first base and the second base is aligned in
5 relation to the first base,
- the intermediate layer is placed between the first and the second bases, and
- the first and second bases are laminated to each other with the aid of the
intermediate layer.

10 22. A method according to Claim 21, in which

- at least one third base and an intermediate layer for every third base are
manufactured,
- each third base is placed in turn above the first and second bases and each third
base is aligned in relation to one of the lower bases,
- 15 - an intermediate layer is placed beneath each third base, and
- the first, second, and each third base are laminated to each other with the aid of
the intermediate layers.

20 23. A method according to any of Claims 20 - 22, in which holes for feed-throughs are
drilled through the bases secured on top of each other and conductors are made in the
drilled holes for connecting the electronic circuits of each base to each other to form an
operational totality.

25 24. A method according to any of Claims 1 - 23, in which the temperature of a
baseboard, component, or conductive layer connected directly to a component, is, during
the process, less than 200°C and preferably in the range 20 - 85°C.

30 25. An electronic module, which is manufactured using a method according to any of
Claims 1 - 24.

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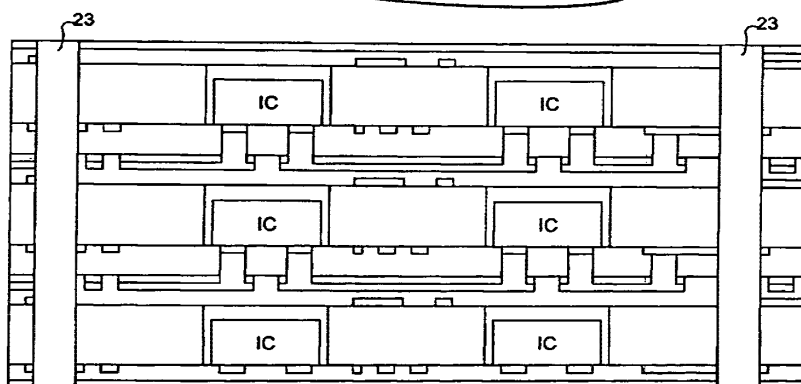
Published:

— with international search report

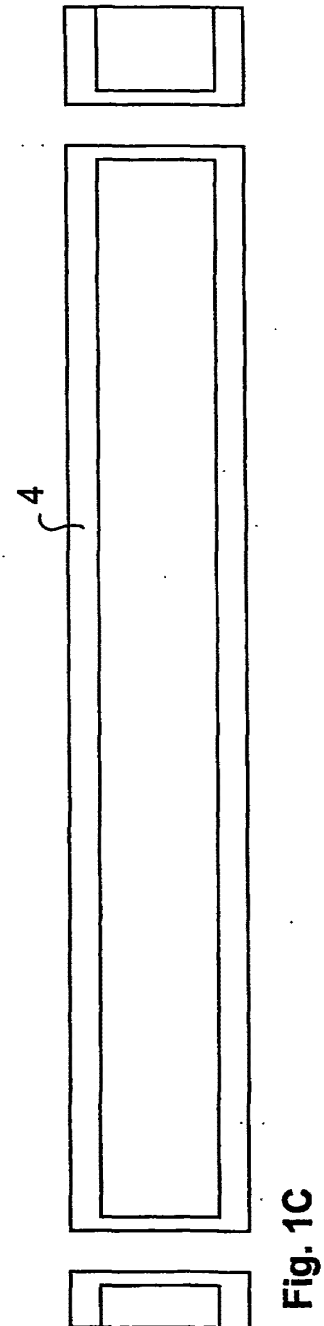
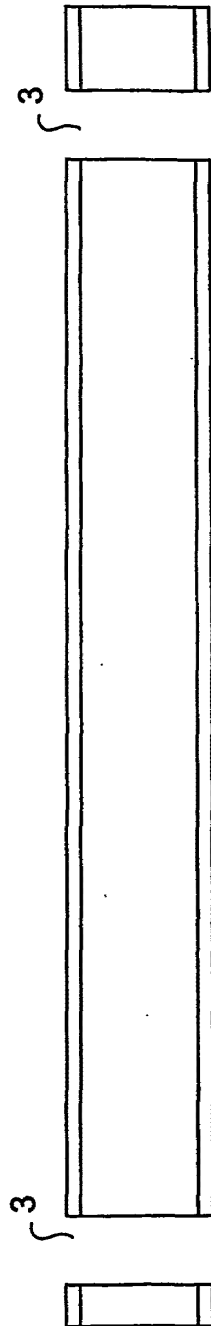
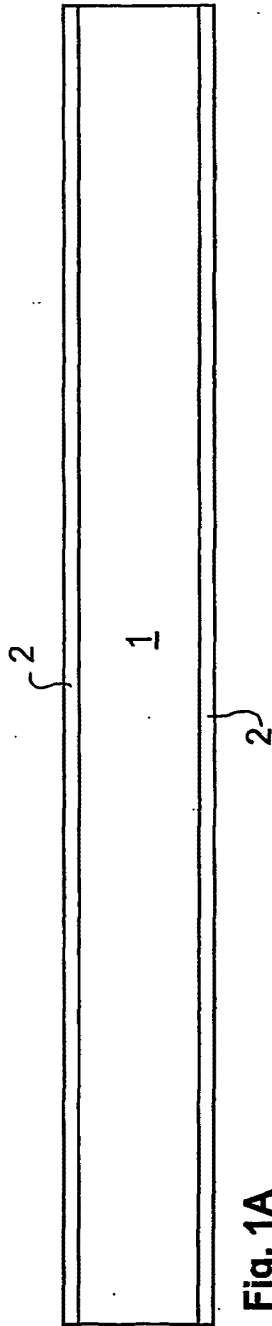
(74) Agent: SEPPO LAINE OY; Itämerenkatu 3 B,
FIN-00180 Helsinki (FI).

For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.

(54) Title: METHOD FOR EMBEDDING A COMPONENT IN A BASE



(57) Abstract: This publication discloses a method, in which the semiconductor components forming part of an electronic circuit, or at least some of them, are embedded in a base, such as a circuit board, during the manufacture of the base, when part of the base structure is, as it were, manufactured around the semiconductor components. According to the invention, through-holes for the semiconductor components are made in the base, in such a way that the holes extend between the first and second surface of the base. After the making of the holes, a polymer film is spread over the second surface of the base structure, in such a way that the polymer film also covers the through-holes made for the semiconductor components from the side of the second surface of the base structure. Before the hardening, or after the partial hardening of the polymer film, the semiconductor components are placed in the holes made in the base, from the direction of the first surface of the base. The semiconductor components are pressed against the polymer film in such a way that they adhere to the polymer film. After this, the final hardening of the polymer film is carried out.



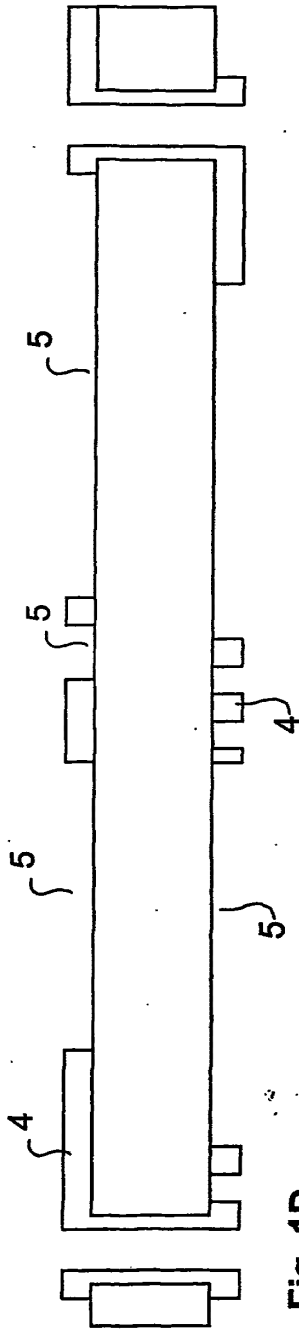


Fig. 1D

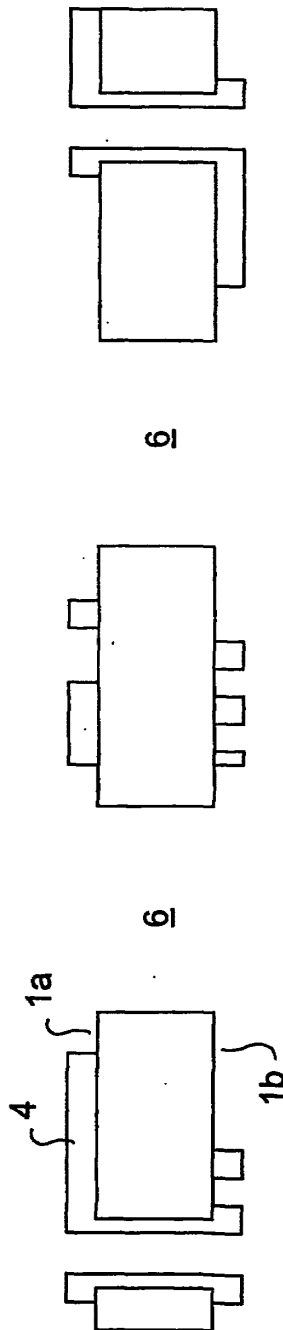


Fig. 1E

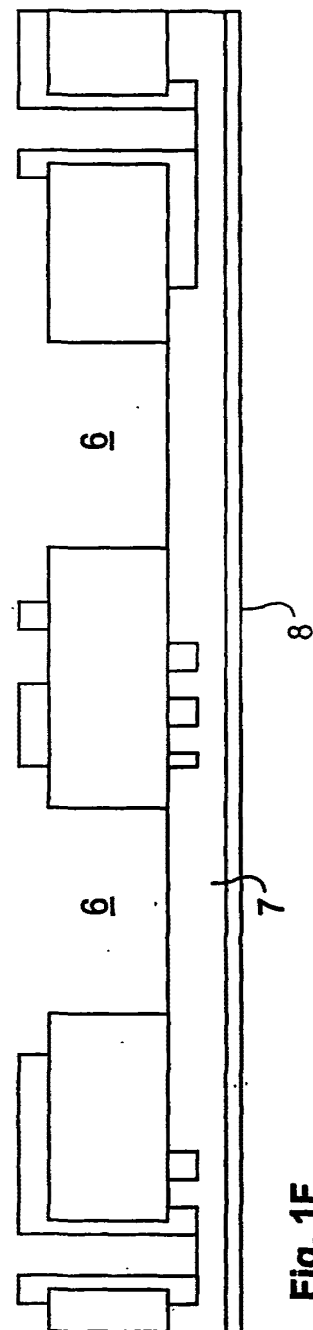
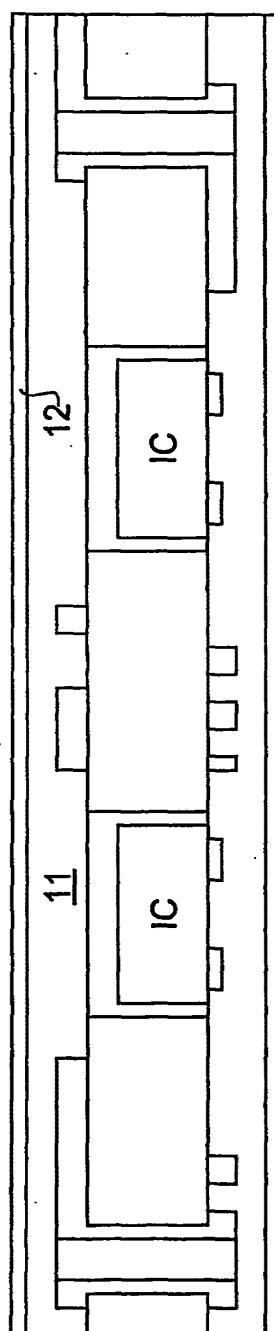
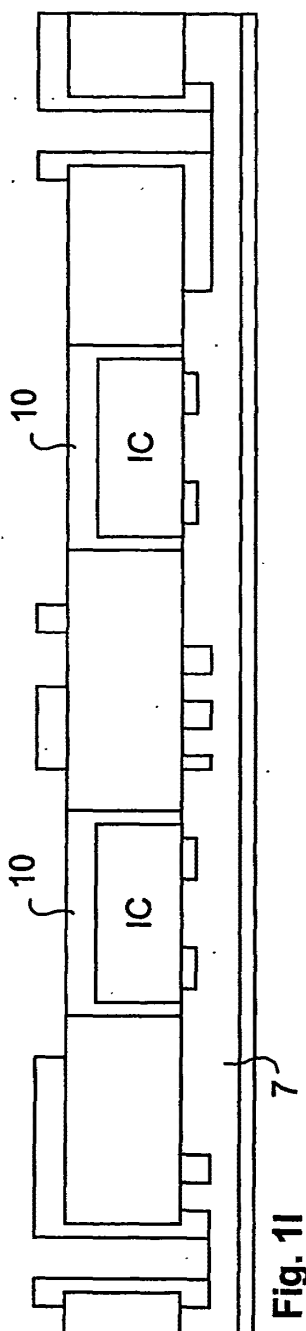
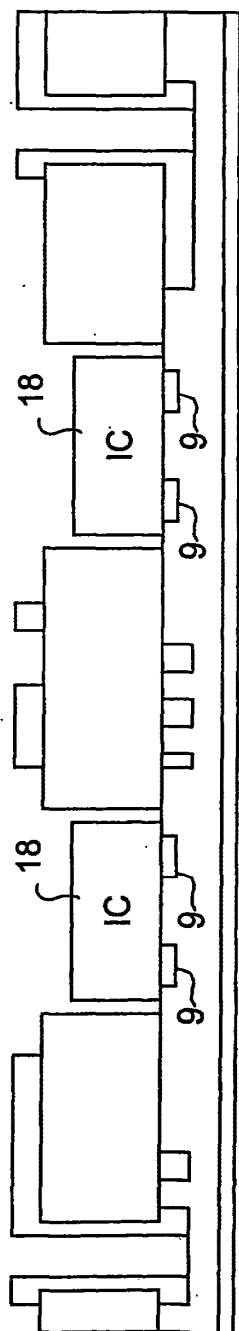


Fig. 1F



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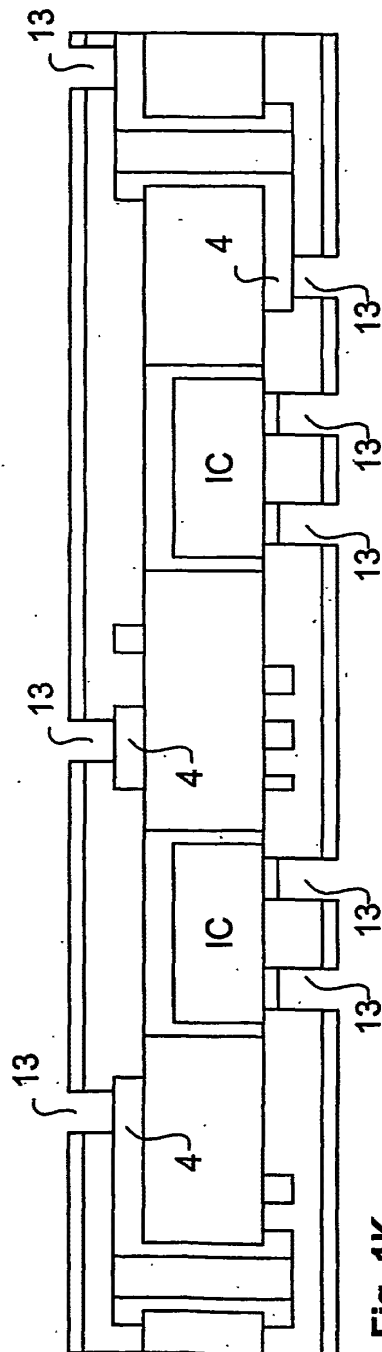


Fig. 1K

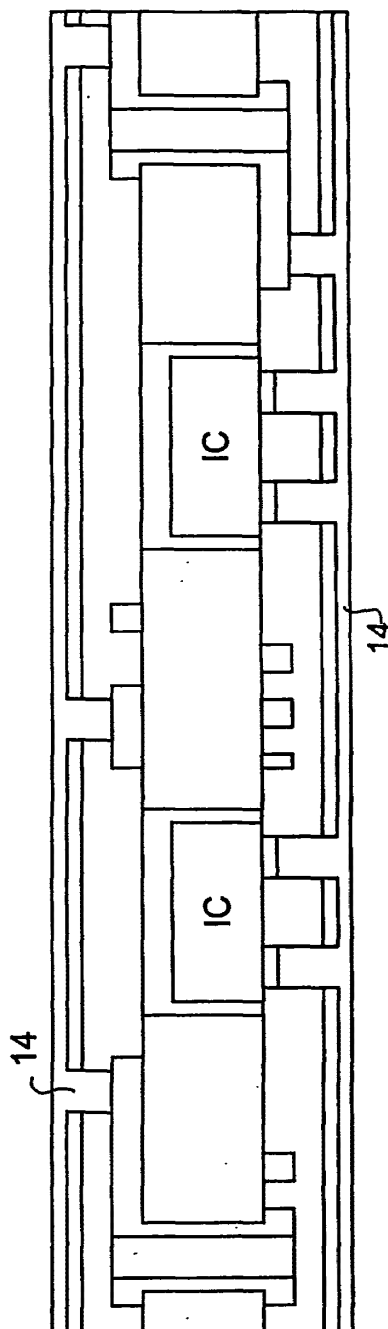
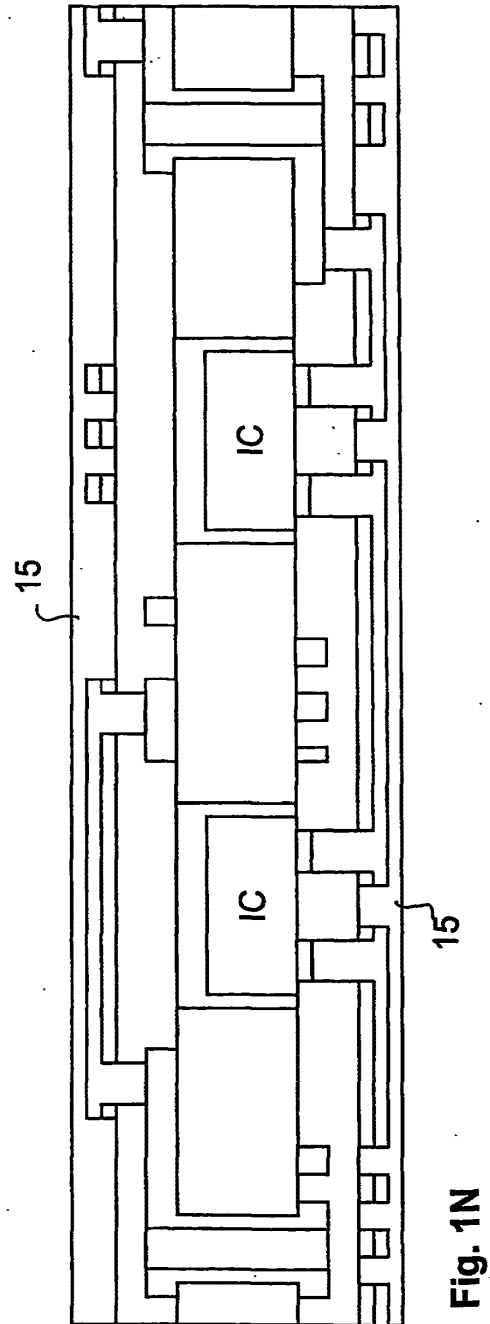
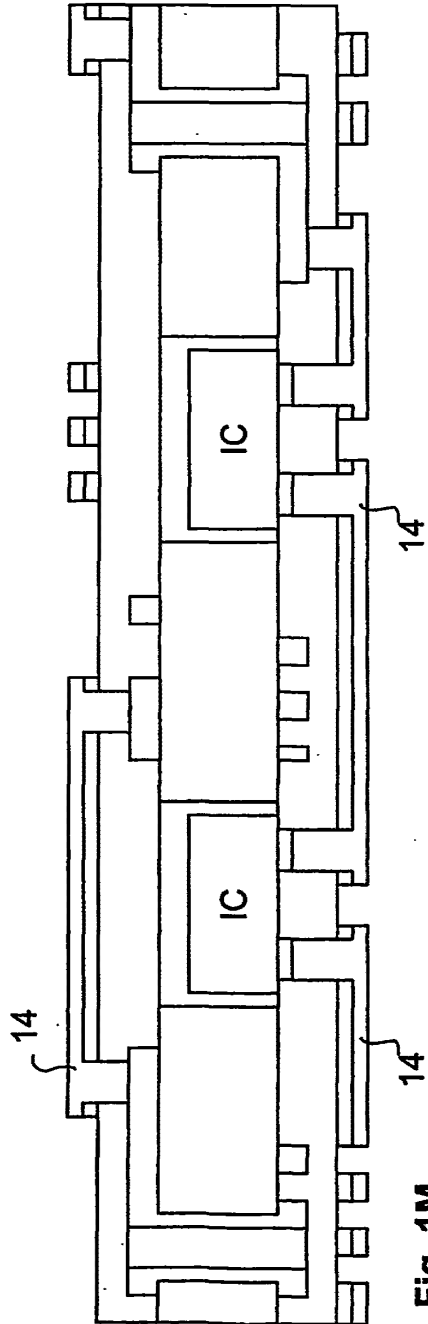


Fig. 1L



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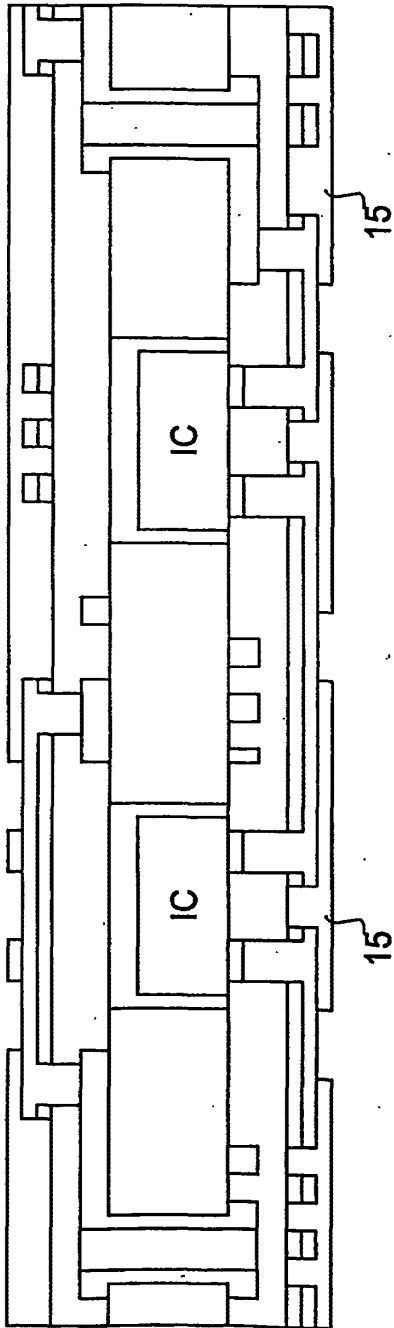


Fig. 10

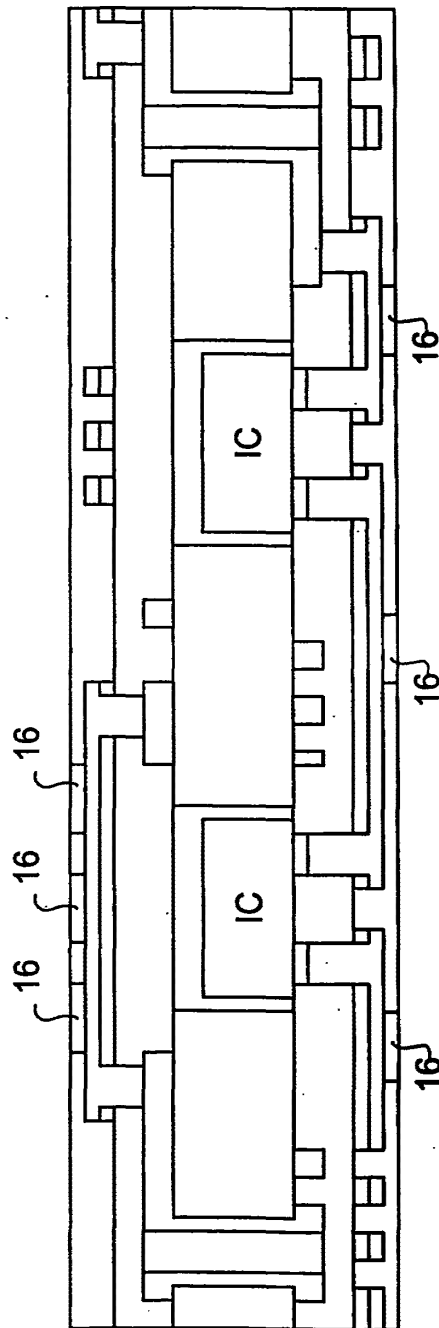


Fig. 1P

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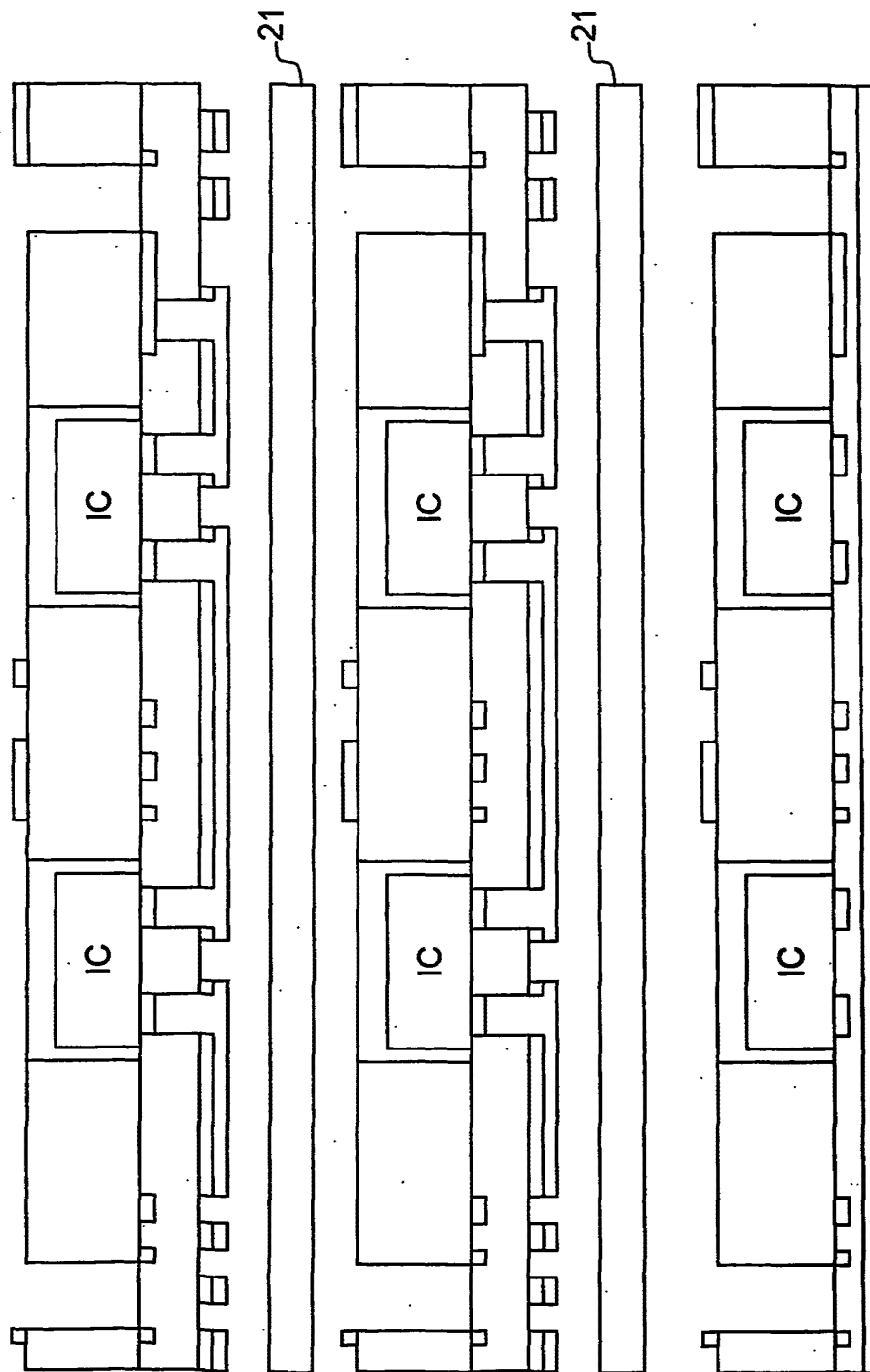


Fig. 2A

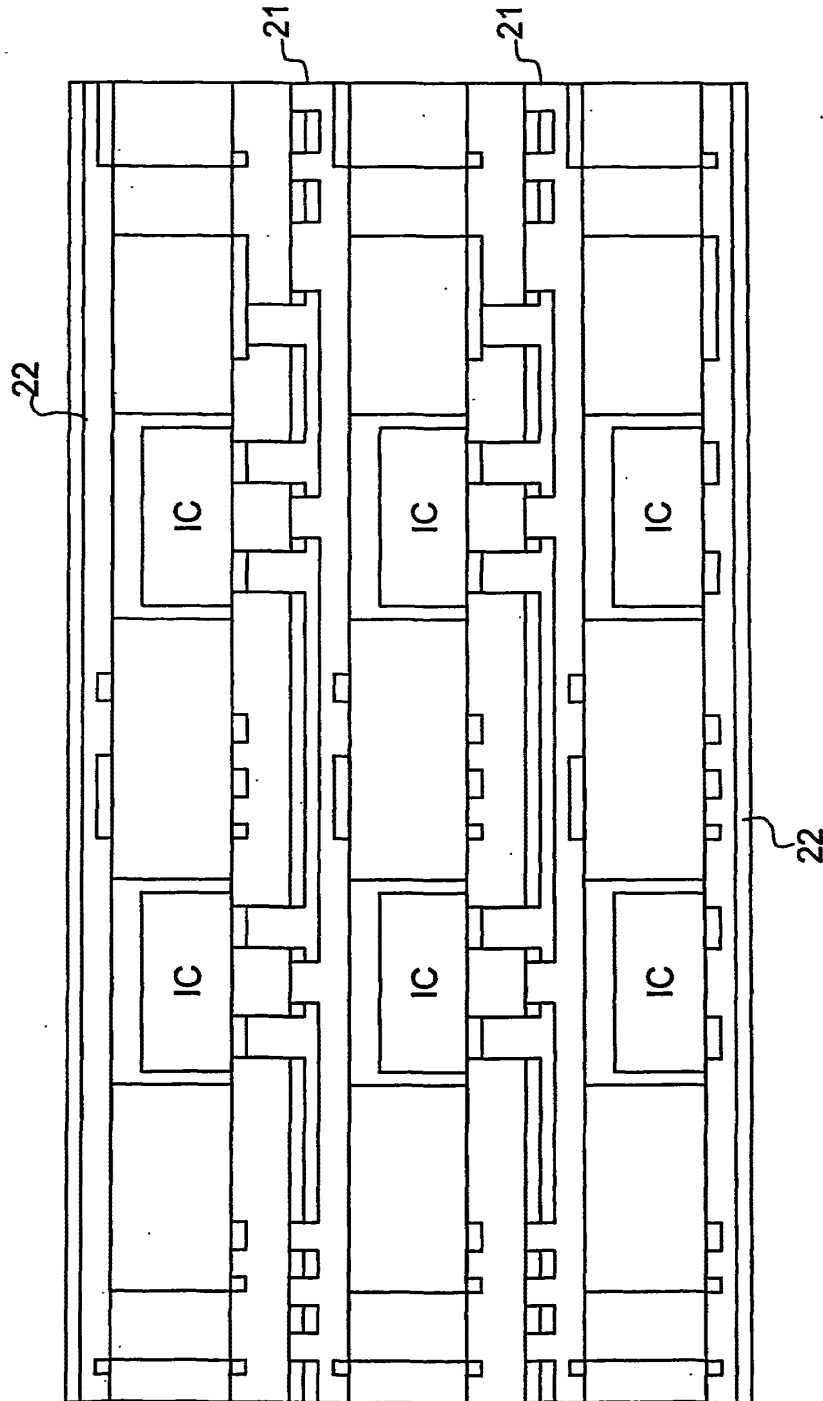


Fig. 2B

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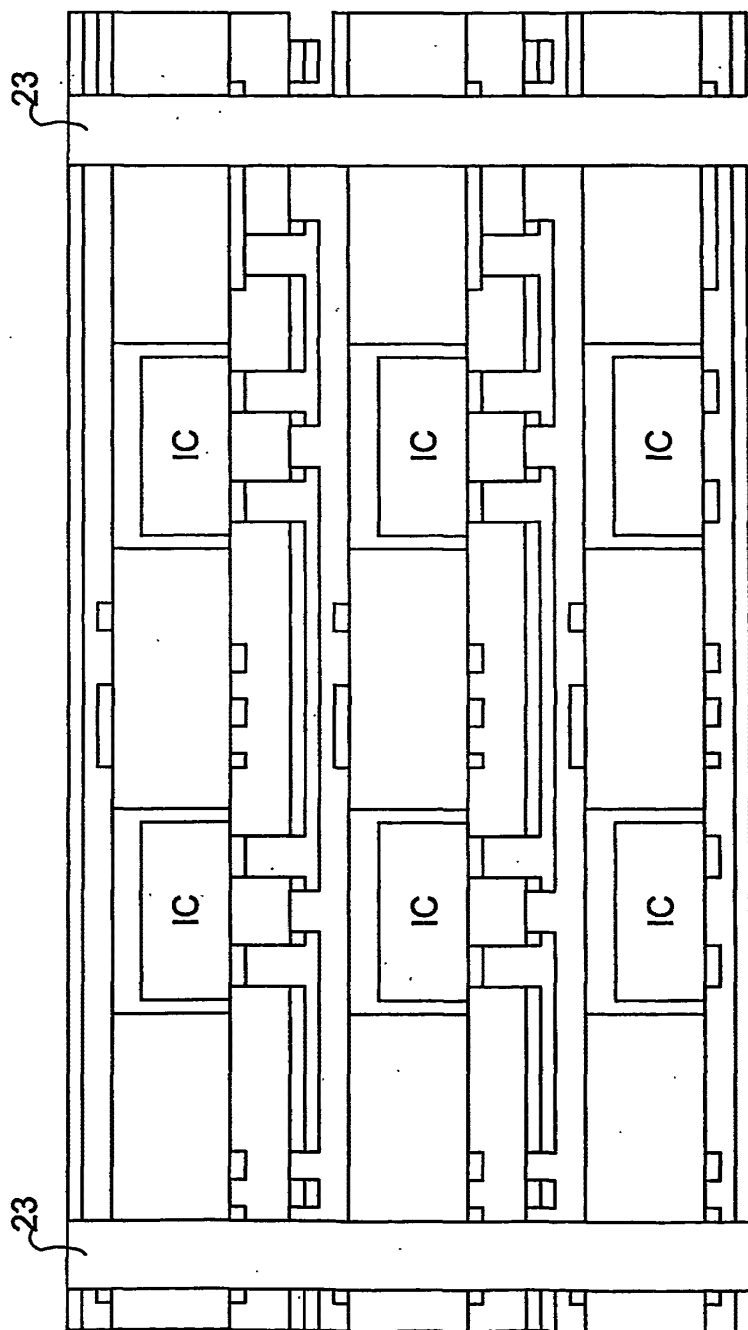


Fig. 2C

10/12

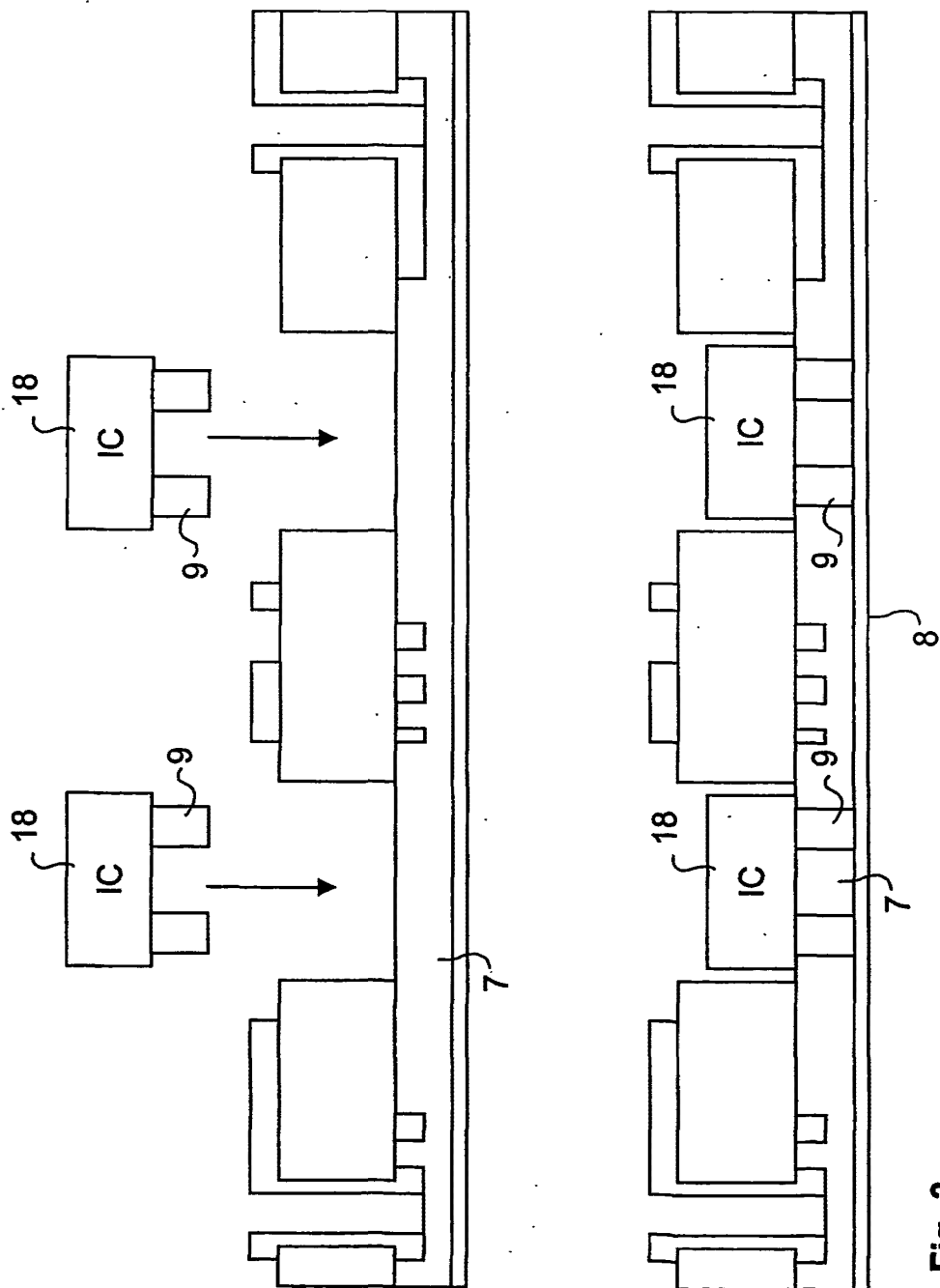


Fig. 3

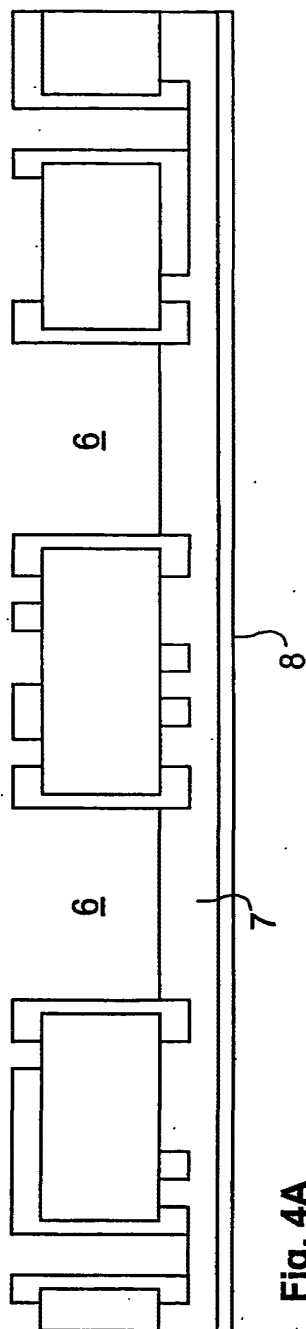


Fig. 4A

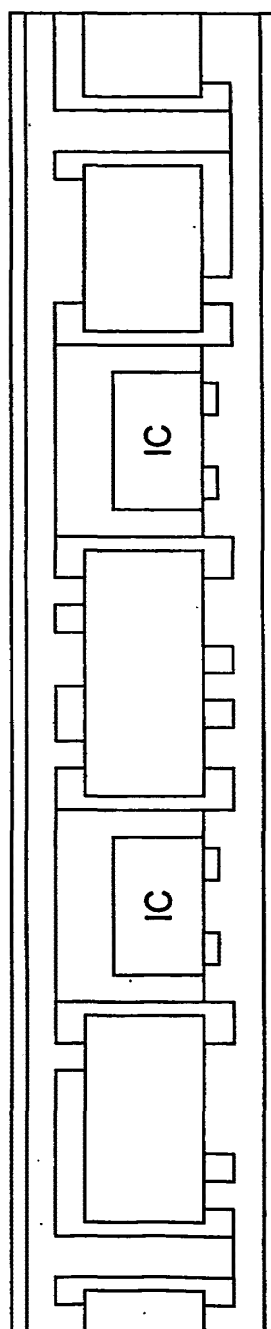


Fig. 4B

12/12

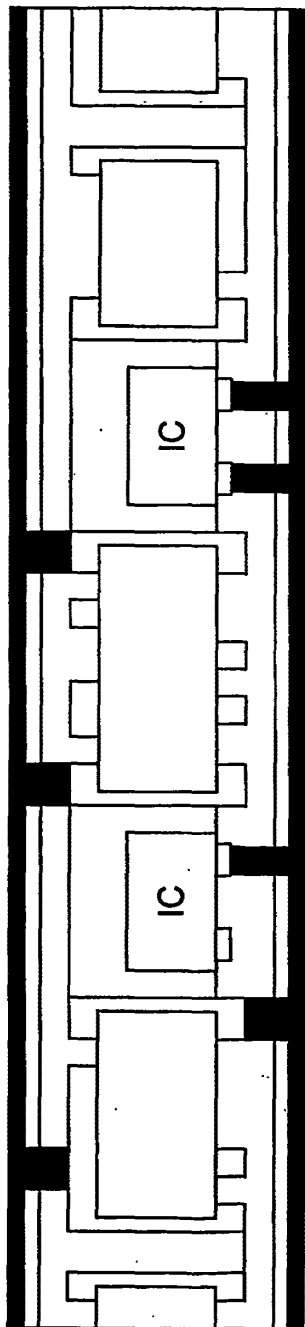


Fig. 4C

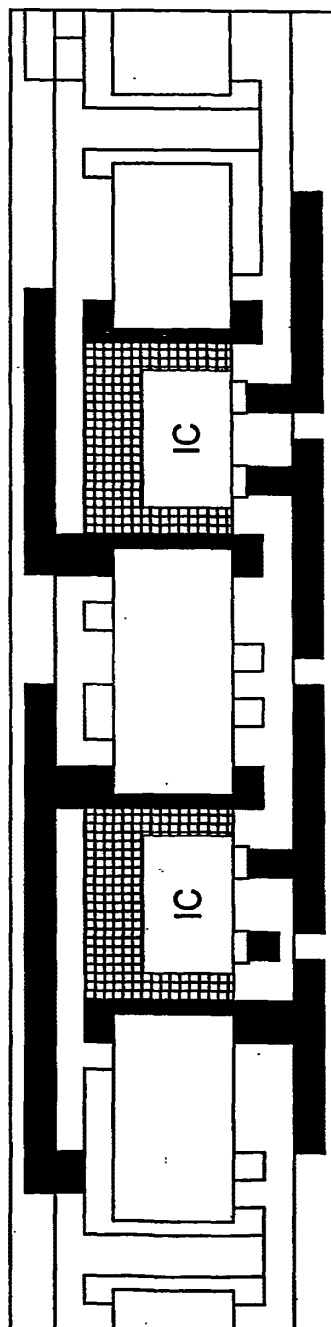


Fig. 4D

**MULTIPLE DEPENDENT CLAIM
FEE CALCULATION SHEET**
(FOR USE WITH FORM PTO-875)

SERIAL NO.

10/502 16

FILING DATE

APPLICANT(S)

CLAIMS

	AS FILED		AFTER 1 st AMENDMENT		AFTER 2 nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
1						
2						
3		1				
4		3				
5		3				
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7		(1)				
8		(1)				
9		(1)				
10		(1)				
11		(1)				
12		(1)				
13		(1)				
14		(1)				
15		(1)				
16		(1)				
17		(1)				
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19		(1)				
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TOTAL IND.	1	↓		↓		↓
TOTAL DEP.	28	←		←		←
TOTAL CLAIMS	29					

	AS FILED		AFTER 1 st AMENDMENT		AFTER 2 nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
51						
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100						
TOTAL IND.		↓		↓		↓
TOTAL DEP.		←		←		←
TOTAL CLAIMS						

PATENT APPLICATION SERIAL NO. 10/502336

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

07/29/2004 LLANDGRA 00000002 10502336

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02 FC:1617	130.00 OP
03 FC:1615	162.00 OP
04 FC:1616	290.00 OP

PTO-1556
(5/87)

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 2004

Application or Docket Number

10/502336

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	29 minus 20 =	9
INDEPENDENT CLAIMS	1 minus 3 =	
MULTIPLE DEPENDENT CLAIM PRESENT ☒		

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY
TYPE ☐

OR

OTHER THAN
SMALL ENTITY

RATE	FEE
BASIC FEE	
X \$ 9 =	
X \$ 44 =	
+ \$ 150 =	
TOTAL	

OR

RATE	FEE
BASIC FEE	1080
X \$ 18 =	162
X \$ 88 =	
+ \$ 300 =	290
TOTAL	1532

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total *	Minus **	=
	Independent *	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

RATE	ADDITIONAL FEE
X \$ 9 =	
X \$ 44 =	
+ \$ 150 =	
TOTAL ADDIT. FEE	

OR

RATE	ADDITIONAL FEE
X \$ 18 =	
X \$ 88 =	
+ \$ 300 =	
TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total *	Minus **	=
	Independent *	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

RATE	ADDITIONAL FEE
X \$ 9 =	
X \$ 44 =	
+ \$ 150 =	
TOTAL ADDIT. FEE	

OR

RATE	ADDITIONAL FEE
X \$ 18 =	
X \$ 88 =	
+ \$ 300 =	
TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total *	Minus **	=
	Independent *	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

RATE	ADDITIONAL FEE
X \$ 9 =	
X \$ 44 =	
+ \$ 150 =	
TOTAL ADDIT. FEE	

OR

RATE	ADDITIONAL FEE
X \$ 18 =	
X \$ 88 =	
+ \$ 300 =	
TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than "20", enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than "3", enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Application Data Sheet

Application Information

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Subject Matter::	PCT
Suggested Group Art Unit::	N/A
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Sequence submission?::	None
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Attorney Docket Number::	0365-0601PUS1
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Request for Non-Publication?::	No
Total Drawing Sheets::	12
Small Entity?::	No
Petition included?::	No
Secrecy Order in Parent Appl.?::	No

Applicant Information

Applicant Authority Type::	Inventor
Primary Citizenship Country::	Finland
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City of mailing address::	Helsinki
Country of mailing address::	Finland
Postal or Zip Code of mailing address::	FI-00610

Correspondence Information

Correspondence Customer Number:: 02292

Representative Information

Representative Customer Number:: 02292

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Finland	20020191	01/31/02	Yes

Assignee Information

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City of mailing address:: Espoo

Country of mailing address:: Finland

Postal or Zip Code of mailing address:: FI-02151

10/502336
DT1 c'd PCT/PTO 23 JUL 2004

Docket No.: 0365-0601PUS1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Risto TUOMINEN

Application No.: Not Yet Assigned

Confirmation No.: N/A

Filed: July 23, 2004

Art Unit: N/A

For: METHOD FOR EMBEDDING A
COMPONENT IN A BASE

Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT (IDS)

MS PCT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement accompanies the new patent application submitted herewith.

A summary/abstract translation of the non-English language references is enclosed.

A copy of each reference on the PTO/SB/08 is attached.

Application No.: Not Yet Assigned

10/502336
DT12 PCT/PTO 23 JUL 2004
Docket No.: 0365-0601PUS1

A concise explanation of relevance of the items listed on form PTO/SB/08 is in the form of an English language copy of a Search Report from a foreign patent office, issued in a counterpart application, which refers to the relevant portions of the references.

In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure statement shall not be construed to be an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

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MKM/clb

Respectfully submitted,

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		Application Number	Not Yet Assigned		
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U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	AA**	US-4,246,595-A1	01-20-1981	NOYORI et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
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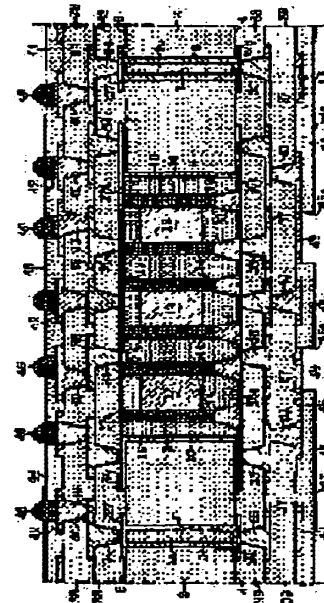
(54) WIRING BOARD AND ITS MANUFACTURING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a wiring board and its manufacturing method that prevent electronic components incorporated into an insulating board from being easily affected by an external electromagnetic wave, at the same time, can reduce influence by noise generated by a circuit being composed of the electronic components, and can stabilize electric characteristics inside the wiring board and continuity with an IC chip or the like that is mounted onto a wiring layer and a first main surface.

SOLUTION: In a wiring board 1, on the inner surface of a through hole 8 that is provided on an insulating board (core board) 2 and at the same time

incorporates an electronic component 12, a shield layer 10 made of a copper-plated film for shielding the electromagnetic wave is formed, and at the same time a chip capacitor (electronic component) 12 inserted into the through hole 8 is stuck via a resin 16, thus carrying out incorporation into the insulating board 2, and at the same time forming wiring layers 26 and 27 being continuous to electrodes 13 and 14 of the capacitor 12 at the upper and lower parts of the insulating board 2.



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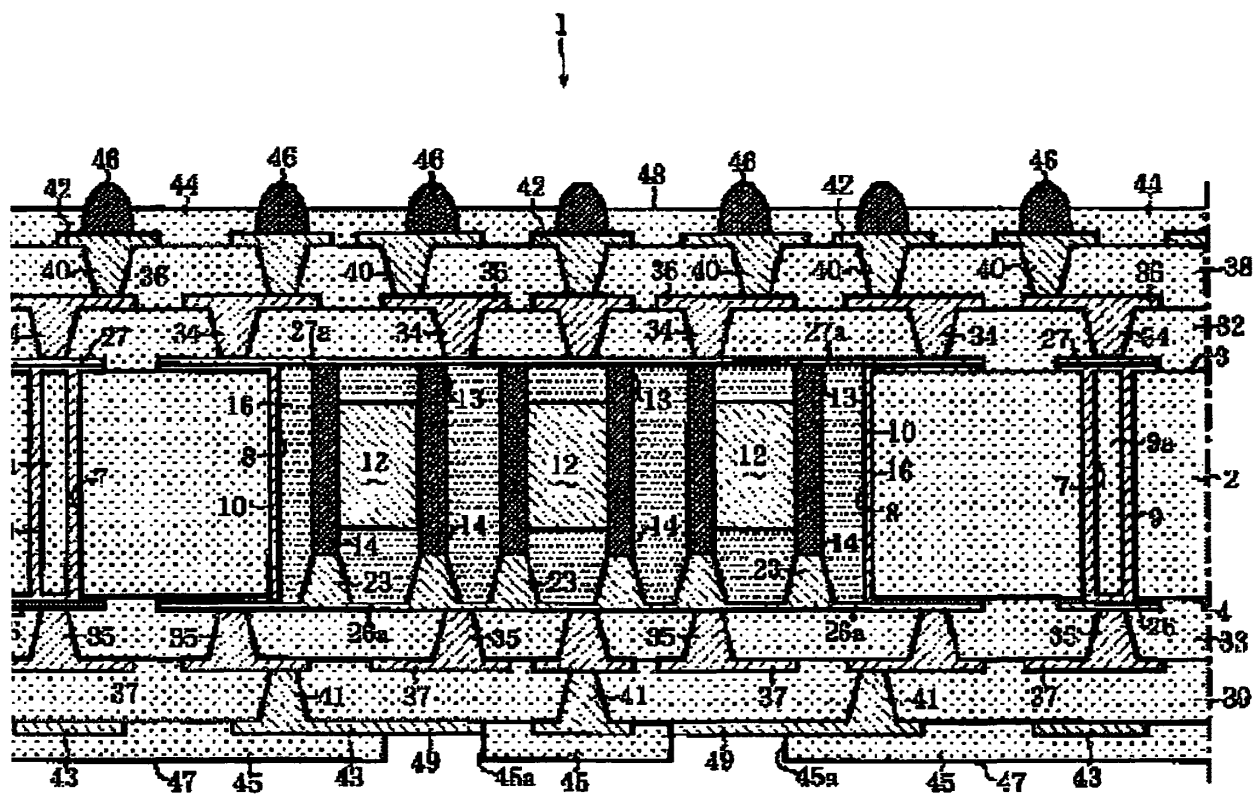
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DETAILED DESCRIPTION

Detailed Description of the Invention]

[0001]

The technical field to which invention belongs] this invention relates to the wiring substrate which fixes and builds in electronic parts in an insulating substrate, and its manufacture method.

[0002]

Description of the Prior Art] Since it corresponds to the miniaturization of the wiring substrate in recent years, and the densification of the wiring in a wiring substrate, it not only carries electronic parts, such as IC chip, on the 1st principal plane of a wiring substrate, but the wiring substrate which builds electronic parts in the interior of an insulating substrate is proposed. For example, the wiring substrate 100 shown in drawing 8 (A) inserted the chip capacitor (electronic parts) 103 in the breakthrough 102 which penetrates an insulating substrate 101, and has connected it with the land 107 which formed the electrode 104 of the ends through the pewter 108 between the insulating layers 106 which adjoin the above-mentioned substrate 101. The viscus of the capacitor 103 are fixed and carried out by being filled up with a resin 109 in the above-mentioned breakthrough 102. The internal electrode 105 is installed inside in this capacitor 103.

[0003] Moreover, the wiring substrate 110 shown in drawing 8 (B) plugs up one opening of the breakthrough 112 which penetrates the insulating substrate 111 with the adhesive temporary fixed film which is not illustrated beforehand, it is in the state which stuck the chip capacitor (electronic parts) 113 which has an internal electrode 115 on this temporary fixed film, and after being filled up with a resin 119 in a breakthrough 112 and making it solidify, it removes the above-mentioned temporary fixed film. This wiring substrate 110 is connected to the land 117,117 which formed the electrode 114 located in the ends of the above-mentioned capacitor 113 between the insulating layers 116 which adjoin the above-mentioned insulating substrate 111 and this beforehand through a pewter 118.

[0004] However, in the wiring substrate 100 of drawing 8 (A), since the breakthrough 102 which carried out the viscus of the capacitor 103 was surrounded by the insulating substrate 101 and the insulating layer 106 through the resin 109, it had the case where became easy to cause a malfunction by the electric wave and magnetic field (for it to consider as an electromagnetic wave hereafter) from the outside, and the electrical property in the interior of the wiring substrate 100 became unstable. Moreover, also by the wiring substrate 110 of drawing 8 (B), since the breakthrough 112 which carried out the viscus of the chip capacitor 113 was surrounded by the insulating substrate 111 and the insulating layer 116 through the resin 119, it tended to invite a malfunction like the above and had a possibility that the electrical property in the interior of the wiring substrate 110 might become unstable. Furthermore, when the viscus of the electronic parts with which switching is performed by the RF in the aforementioned breakthrough 102,112 are carried out, the noise of an electrical power system is revealed outside. This affected IC chip mounted in the front face of the wiring substrate 100,110, or IC chip mounted in other wiring substrates on the mother board in which wiring substrate 100,110 the very thing is mounted, and there was also a possibility of causing a malfunction.

[0005]

[Problem(s) to be Solved by the Invention] the circuit which the trouble in the Prior art explained above is solved, and the electronic parts which carried out viscus to the insulating substrate cannot

be easily influenced by the electromagnetic wave from the outside, and these electronic parts constitute generates this invention -- the influence by the noise can be reduced the [and / the electrical property inside a wiring substrate, a wiring layer, and] -- let it be a technical problem to offer the wiring substrate which may stabilize a flow with IC chip etc. and the above-mentioned electronic parts which are carried on 1 principal plane, and its manufacture method

[0006]

[Means for Solving the Problem] this invention is hit on an idea of it and accomplished to give the shield function for electromagnetic wave cover to the inside of the breakthrough which carries out the internal organs of the electronic parts, or a crevice in order to solve the above-mentioned technical problem. That is, the wiring substrate (claim 1) of this invention is characterized by what the shield layer was formed in the inside of the breakthrough or crevice where it is prepared in an insulating substrate, and electronic parts are built in for. If it adds, the above-mentioned wiring substrate can also be expressed as the wiring substrate which formed the shield layer in the inside of the breakthrough or crevice where the electronic parts prepared in the insulating substrate are built in. According to this, since the circumference is surrounded by the shield layer, the above-mentioned breakthrough or a crevice can reduce the leakage by the exterior of the noise generated from the circuit which can shield the electronic parts built in this breakthrough or crevice from an external electromagnetic wave, and the above-mentioned electronic parts constitute. For this reason, while operating normally IC chip carried in the above-mentioned electronic parts or the 1st principal plane, an internal electrical property can also be stabilized like the ability to reduce the cross talk noise in a wiring substrate. In addition, although what active parts, such as passive components, such as a capacitor, an inductor, a filter, and resistance, and low noise amplifier (LNA), a transistor, a semiconductor device, FET, or an SAW filter, the LC filter, the antenna switch module, the coupler, the diplexer, etc. were contained, and made these the letter of a chip is contained in the above-mentioned electronic parts, it does not restrict to these. Furthermore, you may carry out the internal organs of the electronic parts of a different kind to the same breakthrough or the same crevice among these.

[0007] Moreover, the wiring substrate (claim 2) by which the aforementioned electronic parts are built in the aforementioned breakthrough or the crevice through the resin is also contained in this invention. According to this, while electronic parts are firmly built in in a breakthrough or a crevice, being surrounded by the resin and insulating, they are surrounded by the shield layer and shielded also from an external electromagnetic wave. For this reason, the electronic parts built in the insulating substrate of a wiring substrate can be operated correctly and certainly. Since the noise which the circuit which the built-in electronic parts constitute simultaneously generates can be covered, the bad influence to parts, such as IC chip mounted in the wiring substrate concerned, can be prevented, or it can decrease. Furthermore, the wiring substrate (claim 3) by which the shield layer is formed also in opening of the aforementioned breakthrough or a crevice is also contained in this invention. According to this, since a shield layer (a ground layer or power supply layer) surrounds the perimeter enclosure, the electronic parts built in an insulating substrate can operate these electronic parts much more correctly and certainly, or can shield the noise to generate certainly.

[0008] Moreover, the wiring substrate (claim 4) in which the flowing wiring layer of the upper part of the aforementioned insulating substrate and a lower part is formed with the electrode of the aforementioned electronic parts is also contained in this invention at least at either. According to this, through this wiring layer, the flow with IC chip carried on the 1st principal plane of a wiring substrate, the mother board by the side of the 2nd principal plane, etc. is also stabilized by the flow between electronic parts and a wiring layer, and it can be taken from a basis. Furthermore, the wiring substrate (claim 5) to which the wiring which is in a wrap position about the breakthrough of the aforementioned insulating substrate or opening of a crevice among the aforementioned wiring layers serves as the aforementioned shield layer is also contained. While the above-mentioned wiring layer itself shields electronic parts according to this, without preparing the shield layer of exclusive use, the flow of electronic parts, the above-mentioned IC chip, etc. can also be taken, and it can respond also to the request of the miniaturization to a wiring substrate, and densification.

[0009] On the other hand, the manufacture method (claim 6) of the wiring substrate of this invention is characterized by what the process which forms the breakthrough or crevice for building electronic

parts in an insulating substrate, and the process which forms a shield layer in the inside of this breakthrough or a crevice by plating are included for. While being able to shield the electronic parts built in the above-mentioned breakthrough or a crevice from an external electromagnetic wave according to a few process according to this, the wiring substrate which can prevent the disclosure to the substrate inside and outside of the noise which the circuit which these electronic parts constitute generates can be offered easily and certainly.

[0010] Moreover, the manufacture method (claim 7) of a wiring substrate of having the process which inserts electronic parts into the aforementioned breakthrough or a crevice, and the process which is filled up with a resin and solidified in the breakthrough or crevice where the above-mentioned electronic parts were inserted is also included in this invention after the process which forms the aforementioned shield layer. According to this, the wiring substrate which can prevent disclosure of the noise which the circuit where the electronic parts built in the above-mentioned breakthrough or the crevice can be shielded from an external electromagnetic wave, insulating, and these electronic parts constitute them generates can be offered certainly. Furthermore, the manufacture method (claim 8) of a wiring substrate of having further the process which forms the electrode of the electronic parts by which built-in was carried out [aforementioned], and the flowing wiring layer in at least the upper part of the aforementioned insulating substrate and downward one side is also included in this invention after the process which is filled up with the aforementioned resin and solidified. According to this, the wiring substrate stabilized by the flow with the flow between electronic parts and a wiring layer, IC chip carried on the 1st principal plane of a wiring substrate through a wiring layer, the mother board by the side of the 2nd principal plane, etc. can be manufactured certainly. And since a shield layer can also be formed, a manufacturing process can be lessened and it also becomes possible to cut down the cost, at the same time it forms electronic parts and the flowing wiring layer.

[0011]

[Embodiments of the Invention] The suitable form for operation of this invention is explained with a drawing below. Drawing 1 shows the cross section of the principal part in the wiring substrate 1 of this invention (claims 3-5) which has the size of every 40mm of every direction by plane view. The wiring substrate 1 contains an insulating substrate (core substrate) 2 and the shield layer 10 formed in the inside of the breakthrough 8 which penetrates the table and the rear faces 3 and 4 of this insulating substrate 2, as shown in drawing 1. Moreover, it has the wiring layers 26 and 27 including the wiring 26a and 27a which serves as the shield layer formed in two or more chip capacitors (electronic parts) 12 built in through the resin 16 in the breakthrough 8, and opening of the upper and lower sides of a breakthrough 8. The wiring layers 26 and 27 are used as a grand layer or a power supply layer.

[0012] An insulating substrate 2 is a plate with a thickness of about 0.8mm which presents an abbreviation square by plane view, for example, it consists of a composite of a glass-epoxy resin, and the breakthrough 8 whose one side plane view is 12mm with an abbreviation square is punched by carrying out punching of the center section. moreover, it is shown in drawing 1 -- as -- the both sides of the breakthrough 8 of an insulating substrate 2 -- through holes 7 and 7 -- penetrating -- the interior -- a through hole -- a conductor 9 and restoration resin 9a are formed Furthermore, the shield layer 10 with a thickness of about 25 micrometers formed by copper coating mentioned later is formed in the inside of 4 rounds of a breakthrough 8. The chip capacitor 12 built in through a resin 16 in a breakthrough 8 is a ceramic capacitor which carried out the laminating of the dielectric layer which has the electrodes 13 and 14 of the product made from Cu, and plurality at the vertical edge, for example, makes a barium titanate a principal component, and the nickel layer by turns. This chip capacitor 12 has 3.2mmx1.6mmx0.7mm size.

[0013] As shown in drawing 1, the wiring layers 26 and 27 which include the wiring 26a and 27a which flows with the electrodes 13 and 14 of each chip capacitor 12, and serves as a shield layer in opening of the upper and lower sides of a breakthrough 8 are formed along table and rear face 3, and 4 top. [of an insulating substrate 2] in addition, the beer connected with each electrode 14 of the above-mentioned capacitor 12 at wiring 26a by the side of a rear face 4 -- the conductor (field beer) 23 is formed moreover, the beer with which the laminating of the insulating layers 32, 38, and 44 and the wiring layers 36 and 42 made from Cu which consist of an epoxy resin is carried out by

turns, and they connect between the wiring layer 27 and 36 and between the wiring layer 36 and 42 to insulating layers 32 and 38 as shown in drawing 1 above the front face 3 of an insulating substrate 2 -- conductors (field beer) 34 and 40 are formed. An insulating layer (solder resist layer) 44 is penetrated in the position in the wiring layer 42 of the best layer, and two or more pewter bumps 46 who project more highly than the 1st principal plane 48 of the front face are formed in it. Each bump 46 is connected with IC chip which is carried on the 1st principal plane 48 and which is not illustrated.

[0014] furthermore, the beer with which the laminating of the insulating layers 33, 39, and 45 and the wiring layers 37 and 43 which consist of the same resin as the above is carried out by turns, and they connect between the wiring layer 26 and 37 and between the wiring layer 37 and 43 to insulating layers 33 and 39 down the rear face 4 of an insulating substrate 2 as shown in drawing 1 -- conductors (field beer) 35 and 41 are formed. In open cibarium 45a prepared in the 2nd principal plane 47 under the insulating layer (solder resist layer) 45 of the lowest layer, and 45a, a part of above-mentioned wiring layer 43 is exposed, respectively, and the end-connection child 49 who had nickel and Au plating film covered by the front face is formed. These end-connection children 49 are used for connection with printed circuit boards, such as a mother board in which wiring substrate 1 the very thing is carried and which is not illustrated. in addition -- while the wiring layers 26 and 27 which sandwiched the insulating substrate 2 flow through each chip capacitor 12 -- each through hole -- it has flowed through the conductor 9

[0015] According to the above wiring substrates 1, each chip capacitor (electronic parts) 12 has flowed with the electrodes 14 and 13 of each capacitor 12, opening of the upper and lower sides of a breakthrough 8 also being covered by the wiring 26a and 27a in the wiring layer 26 and 27, while being built in the breakthrough 8 which fixed to the resin 16 and formed the shield layer 10 in the inside, as shown in drawing 1. For this reason, it is stabilized with IC chip which flows with the wiring layers 26 and 27 etc., and is carried on the 1st principal plane 48 through these, the mother board by the side of the 2nd principal plane 47, etc., and it can be flowed through it while it can demonstrate an original function, without producing a malfunction, since each chip capacitor 12 is certainly shielded from the electromagnetic wave from the outside.

[0016] Therefore, according to the wiring substrate 1, a chip capacitor (electronic parts) 12 operates normally, and an electrical property is also improved and stabilized like the ability to reduce the cross talk noise in the interior of the wiring substrate 1. And the noise generated when the above-mentioned capacitor 12 switches by the RF cannot affect, and can carry out influence to IC chip carried in other wiring substrates on the mother board in which IC chip and wiring substrate 1 the very thing carried on the 1st principal plane 48 is carried. In addition, in the form of the above-mentioned implementation, the form which does not restrict it to this although the insulating layer (core substrate 2) of a monolayer is used for an insulating substrate 2, and carried out the laminating of two or more insulating layers (a core substrate is included), and the form which carried out the laminating of two or more insulating layers, and formed the wiring layer among these are also included. Furthermore, one kind or two or more kinds of material may be used for two or more insulating layers mentioned above.

[0017] Drawing 2 and drawing 3 are related with the manufacture method of the wiring substrate 1 shown in aforementioned drawing 1. As shown in drawing 2 (A), copper foil 5 and 6 of 10 micrometers of thickness numbers is beforehand covered by the table and the rear faces 3 and 4 of the insulating substrate 2 with a thickness of about 0.8mm. As shown in drawing 2 (B), by carrying out punching of the center of abbreviation of an insulating substrate 2, the breakthrough 8 of every 12mm of every direction is formed, and through holes 7 and 7 are punched by the drill at the both sides. Next, after adhering catalyst nuclei for plating, such as Pd, to the inside of the above-mentioned breakthrough 8 and a through hole 7 beforehand, non-electrolytic-copper plating and electrolytic-copper plating are given. consequently, as shown in drawing 2 (C), the shield layer 10 which consists of a copper-coating layer with a thickness of 25 micrometers forms in the inside of 4 rounds of a breakthrough 8 -- having -- and -- the inside of a through hole 7 -- a through hole -- the wiring substrate 11 in which the conductor 9 was formed is obtained. This wiring substrate 11 is equivalent to the claim 1 of this invention. in addition, it is shown in drawing 2 (D) -- as -- a cylinder-like through hole -- restoration resin 9a is formed inside a conductor 9

[0018] Subsequently, as shown in drawing 2 (E), the tape 15 which turned the adhesive face to the breakthrough 8 side is stuck on the rear face 4 of an insulating substrate 2, and opening by the side of the rear face 4 of a breakthrough 8 is closed. in order that [in addition,] a tape 15 may close all of the breakthroughs 8 and 8 of a large number in the aggregate (panel) of insulating substrates 2 and 2 and the insulating substrate containing --, and -- illustration -- like -- the whole of a rear face 4 --
 ***** attachment ***** In this state, as shown in drawing 2 (E), two or more chip capacitors 12 are inserted into a breakthrough 8, and the position on the adhesive face of a tape 15 is pasted, respectively. This insertion work is done by the chip mounter etc. The above-mentioned capacitor 12 protrudes two or more electrodes 14 and 13 on a vertical edge, and the end face of the electrode 13 by the side of a soffit pastes it up on the adhesive face of a tape 15.

[0019] Furthermore, as shown in drawing 3 (A), after being filled up with the melted resin 16 which makes an epoxy resin a principal component in a breakthrough 8 from a front-face 3 side, cure processing held about 60 minutes at about 100 degrees C is performed. Consequently, like illustration, when a resin 16 solidifies, except for the end face of the electrode 13, the internal organs of each capacitor 12 are carried out to the position in a breakthrough 8 through a resin 16. Moreover, as shown in drawing 3 (A), the front face 17 of the solidified resin 16 is curved, rises, and lays the electrode 14 of each capacitor 12 underground. On the other hand, the rear face 18 of a resin 16 turns into a flat side which imitated the tape 15, and the end face of the electrode 14 of each capacitor 12 exposes it. In this stage, the installation position and the short existence of each capacitor 12 laid underground into the resin 16 are inspected. In addition, the above-mentioned cure processing removes the air bubbles of the resin 16 interior, and makes a resin 16 a precise organization. Moreover, the above-mentioned tape 15 has the thermal resistance which is equal to this cure processing.

[0020] Next, as shown in drawing 3 (B), after exfoliating a tape 15, where an insulating substrate 2 is fixed, counter etching of the front face 17 of a resin 16 is carried out by buffing. Consequently, the wiring substrate 20 from which the front face 19 of the resin 16 newly formed turned into the same flat surface as the copper foil 5 on the front face 3 of an insulating substrate 2 like illustration is obtained. This wiring substrate 20 is equivalent to the claim 2 of this invention. Subsequently, as shown in drawing 3 (C), Laser L is irradiated from the front-face 19 side of a resin 16 at a perpendicular. The irradiation position of Laser L is set up right above the electrode 14 of each capacitor 12 upper limit. Consequently, like illustration, right above each electrode 14, the beer hall 22 of a cross-section trapezoidal shape is formed for a bore by about 100 micrometers, and the end face of an electrode 14 is exposed to the bottom. In addition, CO2, YAG, an excimer laser, etc. are used for Laser L.

[0021] Furthermore, the aforementioned catalyst nucleus is made to adhere to the inside of each beer hall 22, and the table and rear faces 19 and 18 of a resin 16, and non-electrolytic-copper plating and electrolytic-copper plating are given on a table, rear faces 19 and 18 and copper foil 5, and 6. consequently, it is shown in drawing 3 (D) -- as -- the front-face 3 side of an insulating substrate 2 -- beer -- the copper-coating layer 24 containing a conductor 23 is formed, and the flat copper-coating layer 25 is formed in a rear-face 4 side each beer -- a conductor 23 is connected with the electrode 14 of a capacitor 12, and the copper-coating layer 25 is connected with each electrode 13 of a capacitor 12

[0022] In this state, the layer of the photopolymer which is not illustrated is formed, and the exposure and development by the predetermined pattern are performed, and a pattern resist is formed on the copper-coating layer 24 and in the bottom of the copper-coating layer 25. Furthermore, after *****ing the copper-coating layers 24 and 25 through the gap in this resist, the above-mentioned resist is exfoliated. consequently, it is shown in drawing 3 (E) -- as -- the front-face 3 side of an insulating substrate 2 -- a breakthrough 8 and a resin 16 -- a wrap -- beer -- the wiring layer 26 containing wiring 26a which has a conductor 23 is formed, and the wiring layer 27 containing wiring 27a that it is the same as that of the above and flat is formed in a rear-face 4 side Thereby, the wiring substrate 28 equivalent to the claim 3 of this invention is obtained.

[0023] The above-mentioned wiring 26a and 27a serves also as the shield layer which shields each capacitor 12 from an external electromagnetic wave with the aforementioned shield layer 10. moreover, it is shown in drawing 3 (E) -- as -- a through hole on either side -- the wiring layers 26

and 27 are formed also in the ends side of a conductor 9 therefore -- while the wiring layers 26 and 27 flow mutually through each capacitor 12 -- a through hole -- it flows through a conductor 9 the state where the table and the rear face of the above-mentioned wiring substrate 28 were made reverse -- the upper and lower sides of the wiring layers 27 and 26 -- beer, such as the wiring layers 36 and 37, such as insulating layers 32 and 33, -- the pewter bumps (flip chip bump) 46, such as conductors 34 and 35, etc. are formed with well-known build-up technology The wiring substrate 1 which has by this the multilayer structure shown in aforementioned drawing 1 can be obtained. in addition, the technology which laminates the shape of a film, and a liquefied resin insulating layer on the above-mentioned build-up technology and the technology which drill a beer hall with a photolithography or laser beam machining -- further -- a semi additive process , a full additive process , or a subtractive process -- beer -- although the technology which form a conductor and a wiring layer be include , it do restrict to these

[0024] Drawing 4 shows the cross section of the principal part in the wiring substrate 50 of this invention (claims 3-5) which has a gestalt which has the same size as the aforementioned wiring substrate 1, and is different. The wiring substrate 50 contains an insulating substrate (core substrate) 52, the crevice 58 which carries out opening to the front-face 53 side of this insulating substrate 52, and the shield layers 60a and 60b formed in the inside of this crevice 58, as shown in drawing 4 . Moreover, it has the wiring layer 72 containing wiring 72a which serves as the shield layer formed in two or more chip capacitors (electronic parts) 62 built in through the resin 64 in the above-mentioned crevice 58, and opening of a crevice 58. The wiring layer 72 is used as a grand layer or a power supply layer. When the above-mentioned insulating substrate 52 also consists of the same size and same quality of the material as the aforementioned insulating substrate 2 and carries out router processing of the center section, the crevice 58 whose one side plane view is 12mm with an abbreviation square is formed. moreover, it is shown in drawing 4 -- as -- the both sides of the crevice 58 of an insulating substrate 52 -- through holes 57 and 57 -- penetrating -- the interior -- a through hole -- a conductor 59 and restoration resin 59a are formed

[0025] Furthermore, the shield layers 60a and 60b with a thickness of about 25 micrometers formed with copper coating are formed in the inside of four peripheral surfaces of a crevice 58, and a base. Although the chip capacitor 62 built in through a resin 64 in this crevice 58 has the electrode 63 made from Cu which projected only in the upper limit, it is the same as that of the aforementioned capacitor 12. [of others] As shown in drawing 4 , the wiring layer 72 which contains in opening of the crevice 58 upper part wiring 72a which flows with the electrode 63 of each chip capacitor 62, and serves as a shield layer is formed along the front-face 53 top of an insulating substrate 52. the beer connected with each electrode 63 of a chip capacitor 62 at wiring 72a -- the conductor (field beer) 69 is formed

[0026] moreover, the beer which connects between the wiring layers 72 and 80 and 86 to insulating layers 76 and 82 while the laminating of the insulating layers 76, 82, and 88 which consist of an epoxy resin, and the wiring layers 80 and 86 made from Cu is carried out by turns, as shown in drawing 4 above the front face 53 of an insulating substrate 52 -- conductors (field beer) 78 and 84 are formed An insulating layer (solder resist layer) 88 is penetrated in the position in the wiring layer 86 of the best layer, and two or more pewter bumps 92 who project more highly than the 1st principal plane 90 are formed in it. Each bump 92 is connected with IC chip which is carried on the 1st principal plane 90 and which is not illustrated.

[0027] Furthermore, down the rear face 54 of an insulating substrate 52, as shown in drawing 4 , the laminating of the insulating layers 77, 83, and 89 which consist of the same resin as the above, and the wiring layers 73, 81, and 87 is carried out by turns. the beer which connects between the wiring layers 73 and 81 and 87 to insulating layers 77 and 83 -- conductors (field beer) 79 and 85 are formed In the open cibarium 93 prepared in the 2nd principal plane 91 under the insulating layer (solder resist layer) 89 of the lowest layer, and 93, a part of wiring layer 87 is exposed, respectively, and the end-connection child 94 who had nickel and Au plating film covered by the front face is formed. These end-connection children 94 are also used for connection with printed circuit boards, such as a mother board in which wiring substrate 50 the very thing is carried and which is not illustrated. in addition, the wiring layers 72 and 73 which sandwiched the insulating substrate 52 -- a through hole -- it connects through the conductor 59

[0028] According to the above wiring substrates 50, as shown in drawing 4, while being built in the crevice 58 which fixed to the resin 64 and formed the shield layers 60a and 60b in the inside, opening on a crevice 58 was covered by wiring 72a in the wiring layer 72, and this wiring 72a and electrode 63 have flowed through each chip capacitor (electronic parts) 62. For this reason, also between IC chip which flows with the wiring layer 72 etc. and is carried on the 1st principal plane 90 through these, the mother board by the side of the 2nd principal plane 91, etc., it is stabilized and it can flow through it while it demonstrates an original function, without producing a malfunction, since each chip capacitor 62 is certainly shielded from the electromagnetic wave from the outside.

[0029] Therefore, in the wiring substrate 50, the chip capacitor 62 which carried out viscous operates normally, and the electrical property of being able to reduce the cross talk noise in the interior is also improved and stabilized. And since the situation where the noise which the circuit which a capacitor 62 constitutes generates leaks to the crevice 58 shell exterior can also be prevented, having a bad influence on the above-mentioned IC chip etc. can also be prevented. In addition, in the gestalt of the above-mentioned implementation, although the insulating layer (core substrate 52) of a monolayer was used for the insulating substrate 52, it is not restricted to this. That is, the gestalt which carried out the laminating of two or more insulating layers (a core substrate is included), and the gestalt which carried out the laminating of two or more insulating layers, and formed the wiring layer among these are also included. Moreover, when a part of two or more above-mentioned insulating layers are punched beforehand and the laminating of the breakthrough is carried out to it with other insulating layers, you may make it form the aforementioned crevice 58. Furthermore, one kind or two or more kinds of material may be used for two or more above-mentioned insulating layers. In addition, in the gestalt of the above-mentioned implementation, although opening of the opening of a crevice 58 was carried out to the pewter bump 92 side who mounts IC chip etc., it is still better also as a gestalt which carries out opening to the end-connection child [who is not restricted to this] 94 side by whom opening of a crevice 58 is used for connection with a mother board etc.

[0030] Drawing 5 and 6 are related with the manufacture method of the wiring substrate 50 shown in aforementioned drawing 4. As shown in drawing 5 (A), copper foil 55 and 56 of 10 micrometers of thickness numbers is beforehand covered by the same table and rear faces 53 and 54 of an insulating substrate 52 as the above. As shown in drawing 5 (B), the crevice 58 which carried out router processing of the center of abbreviation of an insulating substrate 52, and carried out opening to the front-face 53 side is formed, and a drill punches through holes 57 and 57 at the both sides. Next, copper coating is performed to the inside of the above-mentioned crevice 58 and a through hole 57 like the above. consequently, as shown in drawing 5 (C), the shield layers 60a and 60b which consist of a copper-coating layer with a thickness of 25 micrometers form in the wall surface (inside) of 4 rounds and base (inside) of a crevice 8 -- having -- the inside of a through hole 57 -- a through hole -- the wiring substrate 61 in which the conductor 59 was formed is obtained This wiring substrate 61 is also equivalent to the claim 1 of this invention.

[0031] furthermore, it is shown in drawing 5 (D) -- as -- a through hole -- restoration resin 59a is formed inside a conductor 59 in addition, a through hole -- a conductor 59 and the shield layers 60a and 60b are following copper foil 55 and 56 Subsequently, as shown in drawing 5 (E), two or more chip capacitors 62 are inserted into a crevice 58, and it arranges to the position on shield layer 60b, respectively. The above-mentioned capacitor 62 protrudes two or more electrodes 63 only on a upper limit. The upper-limit side of each electrode 63 is located rather than the front face of copper foil 55 in a low position. Furthermore, as shown in drawing 6 (A), after being filled up with the same melted resin 64 as the above in a crevice 58 from a front-face 53 side, the same cure processing as the above is performed. Consequently, like illustration, when a resin 64 solidifies, the viscous of each capacitor 62 are carried out to the position in a crevice 58 through a resin 64. In addition, as shown in drawing 6 (A), the front face 65 of the solidified resin 64 rises, and lays the electrode 63 of each capacitor 62 underground.

[0032] Next, where an insulating substrate 52 is fixed, counter etching of the front face 65 of a resin 64 is carried out by buffing. Consequently, as shown in drawing 6 (B), the wiring substrate 67 from which the front face 66 of the resin 64 newly formed turned into the same flat surface as the copper foil 55 on the front face 53 of an insulating substrate 52 can be obtained. This wiring substrate 20 is also equivalent to the claim 2 of this invention. Furthermore, as shown in drawing 6 (C), the same

laser L as the above to a perpendicular is irradiated right above the electrode 63 of each capacitor 62 upper limit from the front-face 66 side of a resin 64. Consequently, like illustration, right above each electrode 63, the beer hall 68 of a cross-section trapezoidal shape is formed for a bore by about 100 micrometers, and the upper-limit side of an electrode 63 is exposed to the pars basilaris ossis occipitalis.

[0033] Subsequently, the aforementioned catalyst nucleus is made to adhere to the inside of each beer hall 68, and the front face 66 of a resin 64, and the same copper coating as the above is performed on a front face 66 and copper foil 55, and 56. consequently, it is shown in drawing 6 (D) - as -- the front-face 53 side of an insulating substrate 52 -- beer -- the copper-coating layer 70 containing a conductor 69 is formed, and the flat copper-coating layer 71 is formed in a rear-face 54 side each beer -- the conductor 69 is connected with the electrode 63 of a capacitor 62 In this state, the layer of the photopolymer which is not illustrated is formed, and the exposure and development by the predetermined pattern are performed, and a pattern resist is formed on the copper-coating layer 70 and in the bottom of the copper-coating layer 71. Furthermore, after *****ing the copper-coating layers 70 and 71 through the gap in this resist, the above-mentioned resist is exfoliated.

[0034] consequently, it is shown in drawing 6 (E) -- as -- the front-face 53 top of an insulating substrate 52 -- a crevice 58 and a resin 64 -- covering -- and beer -- the wiring layer 72 containing wiring 72a which has a conductor 69 is formed, and the wiring layer 73 is formed on a rear face 4 Thereby, the wiring substrate 75 equivalent to the claim 3 of this invention is obtained. The above-mentioned wiring 72a serves also as the shield layer which shields each capacitor 62 from an external electromagnetic wave with the aforementioned shield layers 60a and 60b. moreover, it is shown in drawing 6 (E) -- as -- a through hole on either side -- since the wiring layers 72 and 73 are formed also in the ends side of a conductor 59 -- the wiring layers 72 and 73 -- a through hole -- it flows through a conductor 59 and the wiring layer 72 and 73 top in the wiring substrate 75 or the bottom -- beer, such as the wiring layers 80 and 81, such as insulating layers 76 and 77, -- the wiring substrate 50 which has the multilayer structure which showed the pewter bumps (flip chip bump) 92, such as conductors 78 and 79, etc. to aforementioned drawing 4 by forming with the well-known build-up technology mentioned above can be obtained

[0035] Each chip capacitor 12 by which drawing 7 (A) is a cross section corresponding to aforementioned drawing 3 (B), and viscus were carried out into the breakthrough 8 of an insulating substrate 2 is exposing the end face of the electrodes 14 and 13 of a vertical edge at the table and the rear face 19 and 18 of a resin 16. After forming the same copper-coating layer as the above on these table and rear faces 19 and 18 and the copper foil 5 of an insulating substrate 2, and 6 and forming an etching resist, it *****s like the above. Thereby, as shown in drawing 7 (B), the wiring substrate 97 which has the wiring layers 95 and 96 including the wiring 95a and 96a linked to the electrodes 14 and 13 of each capacitor 12 at a table and the rear face 3 and 4 can be obtained. Wiring 95a and 96a serves also as the shield layer which shields each capacitor 12 with the shield layer 10 of breakthrough 8 inside. since [moreover,] the electrodes 14 and 13 of each capacitor 12 are connectable with Wiring 95a and 96a soon in the wiring substrate 97 -- a manufacturing process -- decreasing -- and the flow of a capacitor 12, the wiring layer 95, etc. -- the aforementioned beer -- it becomes what was stabilized compared with the wiring substrate 28 between which a conductor 23 is made to be placed

[0036] Each chip capacitor 62 by which drawing 7 (C) is a cross section corresponding to aforementioned drawing 6 (B), and viscus were carried out into the crevice 58 of an insulating substrate 52 is exposing the end face of the electrode 63 of a upper limit on the front face 66 of a resin 64. After forming the same copper-coating layer as the above on this front face 66 and the copper foil 55 of an insulating substrate 52, and 56 and forming an etching resist, it *****s like the above. Thereby, as shown in drawing 7 (D), the wiring substrate 99 which has the wiring layer 98 containing wiring 98a linked to the electrode 63 of each capacitor 62 in a front-face 53 side, and has the wiring layer 73 in a rear-face 54 side can be obtained. The above-mentioned wiring 98a serves also as the shield layer which shields each capacitor 62 with the shield layers 60a and 60b of crevice 58 inside. since [moreover,] the electrode 63 of each capacitor 62 is soon connected with wiring 98a in the wiring substrate 99 -- a manufacturing process -- decreasing -- and the flow of each

chip capacitor 62, the wiring layer 98, etc. -- the aforementioned beer -- it is made to what was stabilized compared with the wiring substrate 75 between which a conductor 69 is made to be placed

[0037] this invention is not limited to each form explained above. For example, only one electronic parts built in in the aforementioned breakthrough 8 or a crevice 58 are good. On the contrary, you may form two or more breakthroughs 8 and crevices 58 in one product [take a large number and] unit containing two or more insulating substrates 2 and 52 in the panel of business (insulating substrates 2 and 52). Moreover, it is also possible to build in electronic parts like the aforementioned capacitor 62 which has an electrode 63 only in a upper limit in the breakthrough 8 of the aforementioned insulating substrate 2. Furthermore, it can consider as the unit which pasted up beforehand two or more letter electronic parts of a chip between the mutual sides, and this can also be inserted and built in in the aforementioned breakthrough 8 or a crevice 58. Moreover, while active parts, such as passive components, such as the inductor and resistance which were made into the letter of a chip besides being the aforementioned chip capacitor 12 etc., and a filter, and a transistor, memory, low noise amplifier (LNA), are also contained in the letter electronic parts of a chip, it is also mutually possible to put side by side and build in electronic parts of a different kind in the same breakthrough or a crevice.

[0038] Furthermore, the glass fiber-resin material which is composite material with resins, such as a glass cloth which has the same thermal resistance besides the composite material of the aforementioned glass-epoxy resin, mechanical strength, flexibility, processing ease, etc., and glass fibers, such as a glass cloth, an epoxy resin, polyimide resin or BT resin, may be used for the quality of the materials, such as an insulating substrate 2. Or it is also possible to use the composite material of the resin-resin into which resins, such as an epoxy resin, were infiltrated etc. for the fluorine system resin of the 3-dimensional network structures, such as composite material of organic fiber, such as polyimide fiber, and a resin and PTFE which has continuation pore. Moreover, the quality of the materials, such as the shield layers 10, 60a, and 60b and the wiring layers 26 and 72, are good as for others, nickel, nickel-Au, etc., or can also be formed by the method of applying conductive resin not using metal plating. [copper coating / aforementioned] furthermore, the aforementioned beer -- a conductor 34 etc. is good also as a form of the shape of a cone which imitated not only the form of the aforementioned field beer which fills the inside of a beer hall but the beer hall

[0039] Moreover, although the quality of the materials, such as insulating layers 32 and 76, make the aforementioned epoxy resin a principal component, they can also use the composite material of the resin-resin into which resins, such as an epoxy resin, were infiltrated etc. for the fluorine system resin of the 3-dimensional network structures, such as PTFE which has the polyimide resin which has others, the same thermal resistance, a pattern moldability, etc., BT resin, a PPE resin, or continuation pore. And the method of carrying out thermocompression bonding of the insulating film besides the method of applying a liquefied resin by the roll coater can also be used for formation of an insulating layer. Furthermore, you may use the thing in which the flip chip pad, the wirebonding pad, or the pad for TAB connection other than the aforementioned flip chip bumps (pewter bump) 46 and 92 was formed etc. for the 1st principal plane 48 of the wiring substrates 1 and 50, and an end-connection child with IC chip carried on 90. Moreover, although the high dielectric ceramic which makes BaTiO₃ a principal component was used by capacitors 12 and 62 PbTiO₃, PbZrO₃, TiO₂, SrTiO₃, CaTiO₃, MgTiO₃, KNbO₃, NaTiO₃, KTaO₃, PbTaO₃, TiO (Na_{1/2}Bi_{1/2})₃, and Pb (Mg_{1/2}W_{1/2}) -- O₃, TiO (K_{1/2}Bi_{1/2})₃, etc. You may use what is made into a principal component.

[0040] Furthermore, although the quality of the materials, such as the electrodes 13, such as the aforementioned capacitor 12, made Cu the principal component, Pt, Ag, Ag-Pt and Ag-Pd which have conformity with electronic parts, Pd, Au, nickel, etc. can be used for them. in addition, the beer which serves as an electrode layer which the capacitor 12 of the aforementioned electronic parts etc. becomes from the dielectric layer which makes a high dielectric ceramic a principal component, Ag-Pd, etc. from a resin, Cu plating, nickel plating, etc. -- it is good also as a capacitor which compounded the conductor and the wiring layer In addition, it is also possible to form two or more loading area on the 1st principal plane 48 of the aforementioned wiring substrates 1 and 50 and 90, and to carry two or more IC chips in each area individually.

[0041]

[Effect of the Invention] According to the wiring substrate (claim 1) of this invention explained above, since the circumference is surrounded by the shield layer, a breakthrough or a crevice can shield the electronic parts built in this breakthrough etc. from an external electromagnetic wave, or can reduce the situation where the noise of the circuit which electronic parts constitute conversely leaks within and without a wiring substrate. For this reason, while operating the above-mentioned electronic parts, IC chip, etc. normally, the electrical property of being able to reduce the cross talk noise in a wiring substrate can also be stabilized. Moreover, according to the wiring substrate of a claim 3, the electronic parts built in an insulating substrate can operate much more correctly and certainly IC chip which mounts the perimeter enclosure in these electronic parts itself and the wiring substrate concerned since it is surrounded by the shield layer, or IC chip mounted in other wiring substrates which flow through a mother board. Furthermore, according to the wiring substrate of claims 4 and 5, in addition to the above, the flow with IC chip mounted in the front face of a wiring substrate through this wiring layer, the mother board by the side of the 2nd principal plane, etc. is also stabilized by flow with the electronic parts and the wiring layer which are built in, and it can be taken from a basis.

[0042] On the other hand, according to the manufacture method (claim 6) of the wiring substrate of this invention, the electronic parts built in the above-mentioned breakthrough or a crevice can be shielded from an external electromagnetic wave according to a few process, or the wiring substrate which can prevent that the noise of the circuit which electronic parts constitute leaks within and without a wiring substrate can be offered easily and certainly. Moreover, the wiring substrate which the noise which the circuit which shields from an external electromagnetic wave, insulating the electronic parts built in the breakthrough or the crevice according to the manufacture method of the wiring substrate of a claim 7, and electronic parts constitute generates does not reveal can be offered certainly. Furthermore, according to the manufacture method of the wiring substrate of a claim 8, in addition to the above, the wiring substrate which is stabilized by the flow with the flow between the electronic parts and the wiring layers to build in, IC chip carried on the 1st principal plane of a wiring substrate through a wiring layer, the mother board by the side of the 2nd principal plane, etc., and can take it can be manufactured certainly.

[Translation done.]

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"Menetelmä komponentin upottamiseksi alustaan"

Hakemus on hakemusdiaariin 29.09.2002 tehdyn merkinnän mukaan siirtynyt Imbera Electronics Oy:lle, kotipaikka Espoo.

The application has according to an entry made in the register of patent applications on 29.09.2002 been assigned to Imbera Electronics Oy, Espoo.

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Menetelmä komponentin upottamiseksi alustaan

Keksinnön kohteena on menetelmä yhden tai useamman komponentin upottamiseksi alustaan.

- 5 Keksinnön kohteena olevilla menetelmillä käsiteltäviä alustoja käytetään elektroniikka-
tuotteissa sähköisten komponenttien, tyypillisesti puolijohdekomponenttien ja erityisesti
mikropiirien alustana. Alustan tehtävänä on tarjota komponentille mekaaninen
kiinnitysalusta sekä tarvittavat sähköiset yhteydet alustalla oleviin muihin
komponentteihin ja alustan ulkopuolelle. Alusta voi olla piirilevy, jolloin keksinnön
10 kohteena oleva menetelmä liittyy läheisesti piirilevynvalmistustekniikkaan. Alusta voi
olla myös muu alusta, esimerkiksi komponentin tai komponenttien paketoimisessa
käytettävä alusta tai kokonaisen toiminnallisen moduulin alusta.

- Mikropiirien valmistuksesta piirilevynvalmistustekniikat poikkeavat mm. siten, että
mikropiirien valmistustekniikoissa substraattina on puolijohdemateriaali, kun taas
15 piirilevyn perusmateriaali on eriste. Mikropiirien valmistustekniikat ovat myös
tyypillisesti huomattavasti kalliimpia kuin piirilevynvalmistustekniikat.

- Pakkaustekniikoista piirilevynvalmistustekniikat poikkeavat siten, että pakkaus-
tekniikoiden tarkoituksena on muodostaa puolijohdekomponentin ympärille pakkaus,
joka helpottaa komponentin käsittelyä. Puolijohdekomponentin pakkauksen pinnalla on
20 kontaktiosia, tyypillisesti ulokkeita, joiden avulla pakattu komponentti on helppo asettaa
piirilevyille. Puolijohdepakkaus sisältää lisäksi johteet, jotka yhdistävät pakkauksen
ulkopuolelle ulottuvat kontaktiosat puolijohdekomponentin pinnalla oleviin kontakti-
alueisiin, joiden kautta jännite voidaan kytkeä varsinaiseen puolijohteeseen.

- Perinteisellä tekniikalla valmistetut komponenttien pakkaukset vievät kuitenkin
25 huomattavasti tilaa. Elektroniikkalaitteiden pientyessä onkin pyritty eroon
puolijohdekomponenttien pakkaamisesta. Tätä tarkoitusta varten on kehitetty mm. flip-
chip -teknologiaa, jossa pakkaamaton puolijohdekomponentti ladotaan suoraan
piirilevyn pinnalle. Flip-chip -tekniikassa on kuitenkin monia vaikeuksia. Esimerkiksi
ongelmia voi aiheutua liitosten luotettavuuden kanssa erityisesti sellaisissa
30 sovelluksissa, joissa piirilevyn ja puolijohdekomponentin välille syntyy mekaanisia

jännityksiä. Mekaanisia jännityksiä joudutaan tasoittamaan lisäämällä chipin ja piirilevyn väliin soveltuva kiinnitysainetta (underfill). Tämä menetelmävaihe hidastaa prosessia ja lisää valmistuskustannuksia. Jännityksiä syntyy erityisesti sellaisissa sovelluksissa, joissa käytetään taipuisaa piirilevyä ja piirilevyä taivutetaan voimakkaasti.

Tämän keksinnön tarkoituksena on aikaansaada menetelmä, jonka avulla pakkaamattomia mikropiirejä on mahdollista upottaa alustaan luotettavasti mutta edullisesti.

Keksintö perustuu siihen, että puolijohdekomponentit tai ainakin osa niistä upotetaan alustaan, kuten piirilevyyn, alustan valmistamisen aikana, jolloin osa alustarakenteesta ikään kuin valmistetaan puolijohdekomponenttien ympärille. Keksinnön mukaan alustaan valmistetaan läpireiät puolijohdekomponentteja varten siten, että reiät ulottuvat alustan ensimmäisen ja toisen pinnan välillä. Reikien valmistamisen jälkeen ja alustarakenteen toisen pinnan yli levitetään polymeerikalvo siten, että polymeerikalvo peittää myös puolijohdekomponentteja varten valmistetut läpireiät alustarakenteen toisen pinnan puolelta. Ennen polymeerikalvon kovettamista tai osittaisen kovettamisen jälkeen puolijohdekomponentit sijoitetaan alustaan valmistettuihin reikiin alustan ensimmäisen pinnan suunnasta. Puolijohdekomponentit painetaan polymeerikalvoa vasten siten, että ne kiinnittyvät polymeerikalvoon. Tämän jälkeen suoritetaan polymeerikalvon lopullinen kovetus.

Täsmällisemmin sanottuna keksinnön mukaiselle menetelmälle on tunnusomaista se, mikä on esitetty patenttivaatimuksessa 1.

Keksinnön avulla saavutetaan huomattavia etuja. Keksinnön avulla voidaan nimittäin valmistaa piirilevy, jonka sisään on upotettu puolijohdekomponentteja. Keksinnön avulla voidaan myös valmistaa komponentin ympärille pienikokoinen ja luotettava komponenttipakkaus.

Keksintö mahdollistaa myös runsaasti edullisia sovellusmuotoja, jotka tuovat merkittäviä lisäetuja.

Keksinnön edullisten sovellusmuotojen avulla on esimerkiksi mahdollista yhdistää komponentin pakkausvaihe, piirilevyn valmistusvaihe ja puolijohdekomponenttien

ladonta ja kontaktointivaihe yhdeksi kokonaisuudeksi. Erillisten prosessivaiheiden yhdistäminen tuo merkittäviä logistisia etuja ja mahdollistaa pienemmän ja luotettavamman elektronisen moduulin valmistamisen. Edelleen lisätuna on se, että tällainen elektronisen moduulin valmistusmenetelmä voi pääosin käyttää hyväksi yleisesti käytössä olevia piirilevynvalmistus- ja ladontatekniikoita.

Keksinnön edullisen sovellusmuodon mukainen yhdistelmäprosessi on kokonaisuutena yksinkertaisempi kuin piirilevyn valmistaminen ja komponenttien liittäminen piirilevyyn esim. flip-chip-tekniikalla. Tällaisilla edullisilla sovellusmuodoilla saavutetaan perinteiseen ratkaisuun verrattuna seuraavia etuja:

- 10 - Komponenttien kontaktimisessa ei tarvita juottamista, vaan sähköinen kontakti voidaan valmistaa kasvattamalla johteet puolijohdekomponentin kontaktialueiden päälle. Tämä tarkoittaa sitä, että komponentin liittämisessä ei tarvitse käyttää sulaa metallia, joten metallien välisiä yhdisteitä ei muodostu. Metallien väliset yhdisteet ovat yleensä hauraita, joten luotettavuus paranee juottamalla tehtyihin liitoksiin verrattuna. Erityisesti pienissä liitoksissa metalliyhdisteiden hauraus aiheuttaa suuren ongelman. Edullisen sovellusmuodon mukaisessa juotteettomassa ratkaisussa voidaankin päästä juotteellisia ratkaisuja selvästi pienempiin rakenteisiin. Juotteettoman kontaktointimenetelmän etuna on myös se, että kontaktoinnissa ei tarvita korkeita lämpötiloja. Matalampi prosessilämpötila mahdollistaa suuremman valinnanvaran piirilevyn, komponenttipaketin tai elektroniikkamoduulin muita materiaaleja valittaessa. Menetelmässä pohjalevyn, komponentin ja komponenttiin välittömästi liittyvän johdekerroksen lämpötila voidaan pitää välillä 20 – 85 °C. Ainoastaan käytettävien polymeerikalvojen kovettamiseen (polymerisointiin) saatetaan tarvita korkeampia lämpötiloja, esimerkiksi noin 150 °C lämpötilaa. Pohjalevyn ja komponenttien lämpötila voidaan kuitenkin pitää alle 200 °C:n kautta koko prosessin. Mikäli menetelmässä käytetään polymeerikalvoja, jotka kovetetaan muuten kuin lämpötilan vaikutuksesta, esimerkiksi kemiallisesti tai sähkömagneettisen säteilyn avulla, pohjalevyn ja komponenttien lämpötila voidaan edullisessa sovellusmuodossa pitää koko prosessin ajan alle 100 °C:ssa.
- 30 - Koska menetelmällä pystytään valmistamaan pienempiä rakenteita, komponentit voidaan sijoittaa lähemmäs toisiaan. Tällöin myös komponenttien väliset johtimet

jäävät lyhemmiksi ja elektroniikkapiirin sähköiset ominaisuudet paranevat, esim. häviöt, häiriöt ja kulkuaikaviiveet voivat pienentyä.

- Menetelmä mahdollistaa myös kolmedimensionaalisten rakenteiden valmistamisen, sillä alustoja ja alustoihin upotettuja komponentteja voidaan latio päällekkäin.

- 5
- Menetelmässä voidaan myös vähemmän eri metallien välisiä rajapintoja.
 - Menetelmä mahdollistaa lyijyttömän prosessin.

Keksintö mahdollistaa myös muita edullisia sovellusmuotoja. Keksinnön yhteydessä voidaan mm. käyttää taipuisaa piirilevyä. Edelleen prosessi mahdollistaa piirilevyjen latomisen päällekkäin.

- 10
- Keksinnön avulla on myös mahdollista valmistaa erittäin ohuita rakenteita, joissa puolijohdekomponentit ovat rakenteen ohuudesta huolimatta kauttaaltaan suojattuna alustan, kuten piirilevyn, sisällä.

Koska puolijohdekomponentit voidaan sijoittaa kokonaan piirilevyn sisälle, piirilevyn ja puolijohdekomponentin välisestä liitoksesta tulee mekaanisesti kestävä ja luotettava.

- 15
- Keksintöä tarkastellaan seuraavassa esimerkkien avulla ja oheisiin piirustuksiin viitaten.

Kuvio 1 esittää poikkileikkauskuvasarjan yhdestä keksinnön mukaisesta prosessista.

Kuvio 2 esittää poikkileikkauskuvasarjan toisesta keksinnön mukaisesta prosessista.

Kuvio 3 esittää periaatekuvan yhdestä mahdollisesta kontaktinmuodostusmenetelmästä.

Kuvio 4 esittää poikkileikkauskuvasarjan kolmannesta keksinnön mukaisesta prosessista.

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Kuvion 1 esittämässä kuvasarjassa on kuvattu yksi mahdollinen keksinnön mukainen prosessi. Seuraavassa tarkastellaan kuvion 1 prosessia vaiheittain:

Vaihe A (kuvio 1A):

Vaiheessa A valitaan piirilevyn valmistusprosessia varten sopiva pohjalevy 1. Pohjalevy 1 voi olla esim. lasikuituvahvistettu epoksilevy, kuten FR4 -tyyppinen levy. Pohjalevy 1 voi esimerkkiprosessissa siis olla orgaaninen levy, sillä esimerkkiprosessissa ei tarvita

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korkeita lämpötiloja. Pohjalevyksi 1 voidaan siis valita taipuisa ja halpa orgaaninen levy. Tyypillisesti pohjalevyksi 1 valitaan levy, joka on jo valmiiksi pinnoitettu johdemateriaalilla 2, tavallisimmin kuparilla. Toki voidaan käyttää myös epäorgaanista levyä.

5 Vaihe B (kuvio 1B):

Vaiheessa B pohjalevyyn valmistetaan läpireiät 3 sähköistä kontaktia varten.. Reiät 3 voidaan valmistaa esim. jollakin tunnetulla piirilevynvalmistuksessa käytetyllä menetelmällä, esim. mekaanisesti poraamalla.

Vaihe C (kuvio 1C):

- 10 Vaiheessa C kasvatetaan metallia 4 vaiheessa B valmistettuihin läpireikiin. Esimerkkiprosessissa metallia 4 kasvatetaan samalla myös piirilevyn päälle, joten myös johdekerroksen 2 paksuus kasvaa.

- 15 Kasvatettava johdemateriaali 4 on kuparia tai jotain muuta riittävästi sähköä johtavaa materiaalia. Kuparimetallointi voidaan tehdä pinnoittamalla reiät ohuella kerroksella kemiallista kuparia ja tämän jälkeen pinnoitusta voidaan jatkaa sähkökemiallisella kuparinkasvatusmenetelmällä. Kemiallista kuparia käytetään esimerkissä siksi, koska se pinnoittuu myös polymeerin päälle ja toimii sähkönjohtajana sähkökemiallisessa pinnoituksessa. Metallin kasvatus voidaan siis suorittaa märkäkemiallisella menetelmällä, joten kasvattaminen on halpaa. Vaihtoehtoisesti johdekerros 4 voidaan
- 20 valmistaa esim. täyttämällä läpireiät sähköä johtavalla pastalla.

Vaihe D (kuvio 1D):

Vaiheessa D piirilevyn pinnalla oleva johdekerros kuvioidaan. Tämä voidaan tehdä yleisesti tunnettuja piirilevynvalmistusmenetelmiä hyväksikäyttäen. Johdekerroksen kuviointi kohdistetaan esimerkiksi vaiheessa B valmistettuihin reikiin.

- 25 Johdinkuvion valmistus voidaan suorittaa esim. siten, että metallin 4 pinnalle laminoidaan valokuvioitava polymeerikalvo, johon muodostetaan haluttu johdinkuvio johtamalla valoa kuvioidun maskin lävitse. Valotuksen jälkeen polymeerikalvo kehitetään, jolloin siitä poistetaan halutut alueet ja polymeerin alla oleva kupari 4 paljastuu. Tämän jälkeen filmin alta paljastunut kupari syövytetään pois ja jäljelle jää

haluttu johdinkuvio. Polymeeri toimii ns. etsausmaskina ja metallikerrokseen 4 muodostuu aukkoja 5, joiden kohdalta paljastuu piirilevyn pohjalevy. Tämän jälkeen polymeerikalvo poistetaan myös kuparin 4 päältä.

Vaihe E (kuvio 1E):

- 5 Vaiheessa E pohjalevyyn valmistetaan reiät 6 mikropiirejä varten. Reiät ulottuvat koko pohjalevyn läpi ensimmäiseltä pinnalta 1a toiselle pinnalle 1b. Reiät 6 voidaan valmistaa esim. mekaanisesti jyrsimällä erotusjyrsimen avulla. Reiät 6 voidaan valmistaa myös esim. lyömällä. Reiät 6 kohdistetaan piirilevyn johdinkuvioiden 4 suhteen. Kohdistamisessa voidaan käyttää apuna myös vaiheessa B valmistettuja reikiä
- 10 3, mutta tällöinkin on kysymyksessä kohdistus johdinkuvioiden 4 suhteen sillä johdinkuvioilla 4 on tietty asema reikiin 3 nähden.

Vaihe F (kuvio 1F):

- Vaiheessa F pohjalevyn toiselle pinnalle 1b ja reikien 6 yli valmistetaan sähköeristeen muodostava polymeerikalvo 7. Polymeerikalvo 7 valmistetaan siten, että se on riittävän
- 15 jäykkä pitämään pääpiirteittäisen muotonsa mutta kuitenkin kovettumaton siten, että kalvoon voidaan painamalla kiinnittää komponentteja. Polymeerikalvon tulee olla jäykkä myös siinä mielessä, että se kykenee pitämään kalvoon painetut komponentit alustan suhteen olennaisesti liikkumattomina seuraavien prosessivaiheiden aikana.

Vaiheessa F valmistettava polymeerikalvo voi olla esim. pre-preg-tyyppinen kalvo.

- 20 Vaiheessa F voidaan haluttaessa valmistaa polymeerikalvon 7 päälle myös ohut metallipinnoite 8.

- Esimerkkiprosessissa vaihe F tehdään laminoimalla piirilevyn pinnalle ohut polymeerikalvo (esim. n. 40µm), jonka päällä on kerros kuparia (esim. n. 5µm). Laminointi tapahtuu paineen ja lämmön avulla. Esimerkkiprosessissa kalvo on siis
- 25 RCC-kalvo (Resin Coated Copper). Tällöin laminointi täytyy tehdä vaillinaisesti siten, että polymeeri ei täysin kovetu. Tähän päästään asettamalla laminoinnissa käytettävä lämpötila sopivan matalaksi ja/tai lyhentämällä lämpökäsittelyn kestoaikaa.

Vaihe G (kuvio 1G):

Vaiheessa G reikiin 6 ladotaan pohjalevyn ensimmäisen pinnan 1a puolelta mikropiirit 18. Ladonta voidaan suorittaa tarkan ladontakoneen avulla ja mikropiirit 18 kohdistetaan piirilevyn johdinkuvioiden suhteen. Kohdistuksessa voidaan vaiheen E tapaan käyttää apuna vaiheessa B valmistettuja reikiä.

- 5 Mikropiirit 18 ladotaan siten, että ne tarttuvat reikien 6 ”pohjalla” olevaan polymeerikalvoon 7. Sopivimmin ladonta suoritetaan sellaisella voimalla, että mikropiirit 18 painautuvat hieman polymeerikalvon 7 sisään, jolloin mikropiirit saadaan paremmin pysymään paikallaan. Prosessille on eduksi myös se, jos ladottavissa mikropiireissä on kontaktiulokkeet 9, jotka työntyvät polymeerikalvon 7 sisään.
- 10 Kuviossa 3 on esitetty mielenkiintoinen vaihtoehtoinen sovellusmuoto, jossa mikropiirien kontaktiulokkeet 9 ovat niin pitkät, että ne ulottuvat polymeerikalvon 7 lävitse aina metallipinnoitteeseen 8 saakka. Tällöin mikropiirin kontaktoimista varten ei välttämättä tarvitse valmistaa reikiä polymeerikalvoon 7 (vaihe K), sillä reiät muodostuvat komponenttien ladonnan yhteydessä. Lisäksi voidaan yksinkertaistaa reikien metallointivaihetta (vaihe L), sillä kontaktiulokkeet 9 muodostavat automaattisesti johdepatsaat polymeerikalvon 7 lävitse. Kuvion 3 sovellusmuodossa kontaktiulokkeet voidaan muotoilla myös teräviksi, jolloin niiden läpäisykyky paranee. Mikäli kontaktiulokkeet 9 ovat riittävän pitkät ja terävät, ne voivat tunkeutua myös metallipinnoitteeseen 8 ja periaatteessa muodostaa sähköisen kontaktin mikropiiriin 18 ja metallipinnoitteen 8 välille.
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Vaihe H (ei esitetty):

- Vaiheessa H kovetetaan polymeerikalvo 7 kovetuskäsittelyn avulla. Kovetuskäsittely sisältää yleensä lämpökäsittelyn, mutta prosessissa voidaan käyttää myös muuten kuin lämpökäsittelyn avulla kovetettavaa polymeeriä. Vaihe H voidaan haluttaessa myös jättää pois, erityisesti lämpökäsittelyllä kovettavien polymeerien yhteydessä. Kovettamalla polymeeri tässä vaiheessa voidaan kuitenkin estää se, että mikropiiri liikkuu alustan suhteen vaiheen I aikana.
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Vaihe I (kuvio 1I):

- Vaiheessa I mikropiirit kiinnitetään piirilevyn pohjalevyyn täyttämällä mikropiirejä varten valmistetut reiät täyteaineella 10. Esimerkkiprosessissa tämä vaihe tehdään
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levittämällä piirilevyn ensimmäisen pinnan (1a) puolelta reikiin ja mikropiirien päälle valuepoksia. Epoksi tasoitetaan lastalla ja kovetetaan paistamalla sitä uunissa. Samalla kovettuu myös polymeerikalvo 7, mikäli prosessi ei sisällä vaihetta H.

Vaihe J (kuvio 1J):

- 5 Vaiheessa J piirilevyn ensimmäiselle pinnalle (1a) valmistetaan polymeerikalvo 11 sekä polymeerikalvon päälle ohut metallipinnoite 12.

Esimerkkiprosessissa vaihe J tehdään laminoimalla piirilevyn pinnalle ohut polymeerikalvo (esim. n. 40µm), jonka päällä on kerros kuparia (esim. n. 5µm). Laminointi tapahtuu paineen ja lämmön avulla. Esimerkkiprosessissa kalvo on siis
10 RCC-kalvo (Resin Coated Copper).

Polymeerikalvo voidaan valmistaa myös esim. levittämällä polymeeri piirilevylle nestemäisessä muodossa. Laminointi ei siten ole olennaista vaiheelle J. Olennaista on sen sijaan se, että piirilevylle, joka sisältää upotettuja komponentteja, erityisesti upotettuja mikropiirejä, valmistetaan eristerakos, tyypillisesti polymeerikalvo. Itse
15 polymeerikalvo voi olla sovelluksen mukaan täytetty tai täyttämätön polymeerikalvo. Polymeerikalvo voi olla myös metallipinnoitettu, mutta tämä ei ole välttämätöntä, sillä johdepinta on mahdollista valmistaa myös myöhemmin jo piirilevyyn kiinnitetyn polymeerikalvon päälle.

Vaihe J mahdollistaa sen, että esimerkkiprosessissa voidaan käyttää tavanomaisia
20 piirilevynvalmistuksessa käytettyjä valmistusmenetelmiä ja työvaiheita ja silti haudata piirilevyn sisään mikropiirejä ja muita komponentteja.

Vaihe K (kuvio 1K):

Vaiheessa K polymeerikalvoihin 7 ja 11 (ja samalla johdekalvoihin 8 ja 12) valmistetaan reiät 13, joiden kautta voidaan muodostaa kontaktit piirilevyn
25 johdinkuvioihin ja läpivienteihin (johdemateriaali 4) sekä mikropiireihin.

Reiät 13 voidaan valmistaa esim. laserilla tai jollakin muulla sopivalla menetelmällä. Kohdistukseen voidaan käyttää vaiheessa D valmistettua johdinkuviota tai vaiheessa B valmistettuja läpäreikiä.

Vaihe L (kuvio 1L):

Vaihe L vastaa vaihetta C. Vaiheessa L reikiin 13 ja piirilevyn pinnoille valmistetaan johdekerros 14.

- 5 Esimerkkiprosessissa läpiviennit (reiät 13) puhdistetaan ensin kolmivaiheisella desmear käsittelyllä. Tämän jälkeen läpiviennit metalloidaan siten, että ensin muodostetaan polymeerin katalysoiva SnPd-pinnoite ja tämän jälkeen pinnalle saostetaan kemiallista kuparia ohut kerros (noin 2µm). Kuparin 14 paksuutta kasvatetaan sähkökemiallisella saostuksella.

Vaihtoehtoisesti läpiviennit voidaan täyttää sähköä johtavalla pastalla tai valmistaa jollakin muulla soveltuvalla mikroläpivientien metallointimenetelmällä.

10 **Vaihe M (kuvio 1M):**

Vaiheessa M valmistetaan johdinkuvio samaan tapaan kuin vaiheessa D.

Vaiheet N ja O (kuviot 1N ja 1O):

- Vaiheissa N ja O piirilevyn pinnoille levitetään valokuvioitava polymeeri 15 ja muodostetaan polymeeriin 15 haluttu kuvio (vastaavalla tavalla kuin vaiheissa D ja M).
15 Valotettu polymeerikalvo kehitetään, mutta piirilevylle jäävää polymeerikalvokuviota ei poisteta.

Vaihe (kuvio 1P):

- Vaiheessa P päällystetään 16 edellisessä vaiheessa muodostetun polymeerikalvon kuvion liitosalueet. Päällystys 16 voidaan tehdä esim. Ni/Au-pinnoitteella tai OSP:llä (orgaaninen suojapinnoite).
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- 25 Kuvion 1 esimerkki kuvaa yhden sellaisen prosessin, jonka avulla keksintöämme voidaan käyttää hyväksi. Keksintöämme ei siis mitenkään rajoitu edellä esitettyyn prosessiin vaan keksintö kattaa suuren joukon erilaisia prosesseja ja näiden lopputuotteita patenttivaatimusten täydessä laajuudessa ja ekvivalenssitulkinta huomioon ottaen. Erityisesti keksintö ei mitenkään rajoitu esimerkin kuvaamaan layoutiin vaan alan ammattihenkilölle on selvää, että keksintöämme mukaisilla prosesseilla voidaan valmistaa hyvin monenlaisia piirilevyjä, jotka poikkeavat

suurestikin tässä esitetyistä esimerkeissä. Kuvioden mikropiirit ja johdotukset on siis esitetty ainoastaan valmistusprosessin havainnollistamistarkoituksessa. Edellä esitetyn esimerkin prosessiin voidaan tehdä siis runsaasti muutoksia poikkeamatta silti keksinnön mukaisesta ajatuksesta. Muutokset voivat liittyä eri vaiheissa kuvattuihin valmistustekniikoihin tai esim. vaiheiden keskinäiseen järjestykseen. Esimerkiksi vaihe 5 B voidaan aivan hyvin suorittaa vaiheen D jälkeen, eli menetellä siten, että pora kohdistetaan kuvioon sen sijaan että kuvio kohdistettaisiin porattuihin reikiin.

Edellä esitetyn esimerkin prosessiin voidaan myös lisätä tarpeelliseksi katsottuja vaiheita. Piirilevyn ensimmäiselle puolelle (1a) voidaan esimerkiksi laminoida kalvo, 10 joka suojaa piirilevyn pintaa vaiheessa I tehtävän valun aikana. Tällainen suojakalvo valmistetaan siten, että se peittää kaikki muut alueet paitsi reiät 6. Suojakalvon ansiosta piirilevyn pinta jää puhtaaksi, kun valuepoksi levitetään lastalla. Suojakalvo voidaan valmistaa soveltuvassa vaiheessa ennen vaihetta I ja se poistetaan piirilevyn pinnasta välittömästi valun jälkeen.

15 Menetelmän avulla voidaan myös valmistaa komponenttipaketteja piirilevylle liittämistä varten. Tällaiset paketit voivat sisältää myös useampia puolijohdekomponentteja, jotka on kytketty sähköisesti toisiinsa.

Menetelmällä voidaan valmistaa myös kokonaisia sähköisiä moduuleja. Kuvion 1 esittämää prosessia voidaan soveltaa myös siten, että johderakenne valmistetaan 20 ainoastaan piirilevyn toiselle puolelle 1b, eli sille puolelle, jonne mikropiirin kontaktipinnat suuntautuvat.

Menetelmällä voidaan valmistaa esimerkiksi sellaisia piirilevyjä tai sähköisiä moduuleja, joissa käytetyn pohjalevyn paksuus on välillä 50-200 mikrometriä ja mikropiirin ja mikropiirien paksuus on välillä 50-150 mikrometriä. Johtimien väli 25 (pitch) voi vaihdella esim. välillä 50 – 250 mikrometriä ja mikroläpivientien halkaisija voi olla esim. 15 – 50 mikrometriä. Tällä tavalla yhden levyn kokonaispaksuus yksikerroksisessa rakenteessa on noin 100-300 mikrometriä.

Keksintöä voidaan soveltaa myös siten, että piirilevyjä ladotaan päällekkäin ja näin muodostetaan monikerroksinen piirilevyrakenne, jossa on useita kuvion 1 kaltaisesti 30 valmistettuja piirilevyjä päällekkäisesti ja kytkettynä sähköisesti toisiinsa. Päällekkäin liitettävät piirilevyt voivat olla myös sellaisia piirilevyjä, joissa johderakenne on

valmistettu ainoastaan piirilevyn toiselle puolelle 1b, mutta joka kuitenkin käsittää läpiviennit, joiden kautta mikropiireihin voidaan muodostaa sähköinen kontakti myös piirilevyn ensimmäiseltä pinnalta käsin. Kuviossa 2 on esitetty 1 tällainen prosessi.

5 Kuvio 2 kuvaa piirilevyjen liittämistä yhteen. Seuraavassa prosessia kuvataan vaiheittain.

Vaihe 2A (kuvio 2A):

Vaihe 2A kuvaa piirilevyjen asettamista päällekkäin. Alimmainen piirilevy voidaan saada esim. modifioidusta kuvion 1 prosessista vaiheen J jälkeen. Kuvion 1 prosessia on tällöin modifioitu siten, että vaihe 1C on jätetty pois.

10 Keskimmäinen ja ylimmäinen piirilevy voidaan puolestaan saada esim. modifioidusta kuvion 1 prosessista vaiheen M jälkeen. Kuvion 1 prosessia on tällöin modifioitu siten, että vaihe 1C on jätetty pois ja vaiheet J, K ja L on suoritettu ainoastaan piirilevyn toiselle puolelle (1b).

15 Piirilevyjen lisäksi kuviossa 2A on esitetty piirilevyjen väliin asetetut pre-preg-epoksikerrokset 21.

Vaihe 2B (kuvio 2B):

20 Vaiheessa 2B piirilevyt on laminoitu yhteen pre-preg-epoksikerrosten 21 avulla. Lisäksi piirilevyn yläpinnalle valmistetaan metallipinnoitettu polymeerikalvo 22. Prosessi vastaa kuvion 1 prosessin vaihetta J. Esimerkkiprosessissa piirilevyn alapinnalla on jo valmiiksi metallipinnoitettu polymeerikalvo 22.

Vaihe 2C (kuvio 2C):

Vaiheessa 2C piirilevyyn porataan läpireiät 23 kontaktien muodostamista varten.

Vaiheen 2C jälkeen prosessia voidaan jatkaa esim. seuraavasti:

Vaihe 2D:

25 Vaiheessa 2D piirilevyn päälle ja läpireikiin 23 kasvatetaan johdemateriaalia vaiheen 1C tapaan.

Vaihe 2E:

Vaiheessa 2E piirilevyn pinnalla oleva johdekerros kuvioidaan vaiheen 1D tapaan.

Vaihe 2F:

- 5 Vaiheessa 2F piirilevyn pinnoille levitetään valokuvioitava polymeeri ja muodostetaan polymeeriin haluttu kuvio vaiheiden 1N ja 1O tapaan. Valotettu polymeerikalvo kehitetään, mutta piirilevylle jäävää polymeerikalvokuviota ei poisteta.

Vaihe 2G:

Vaiheessa 2G metalloidaan edellisessä vaiheessa muodostetun polymeerikalvon kuvion liitosalueet vaiheen 1P tapaan.

- 10 Kuvion 2 esimerkin perusteella on selvää, että menetelmää voidaan käyttää myös monenlaisten kolmedimensionaalisten piirirakenteiden valmistamiseen. Menetelmää voidaan käyttää esim. siten, että useita muistipiirejä sijoitetaan päällekkäin ja näin muodostetaan useita muistipiirejä sisältävä paketti, jossa muistipiirit on kytketty toisiinsa yhdeksi toiminnalliseksi kokonaisuudeksi. Tällaista pakettia voidaan kutsua
- 15 kolmedimensionaaliseksi multichip-moduuliksi. Tällaisessa moduulissa chipit voidaan valita vapaasti ja eri chippien väliset kontaktit voidaan helposti valmistaa valittujen piirien mukaisesti.

- 20 Keksintö mahdollistaa myös sähkömagneettisen suojan valmistamisen alustaan upotetun komponentin ympärille. Kuvion 1 menetelmää voidaan nimittäin modifioida siten, että vaiheessa 1E kuvattu reikien 6 valmistus suoritetaan vaiheessa 1B tehtävän reikien 3 valmistuksen yhteydessä. Tällöin vaiheessa 1C valmistettava johdekerros 4 peittää myös komponentteja varten valmistettujen reikien 6 sivuseinämät. Kuviossa 4A on esitetty alustarakenteen poikkileikkaus sellaisena kuin se on vaiheen 1F jälkeen edellä mainitulla tavalla modifioidussa prosessissa.

- 25 Kuvion 4A esittämän välivaiheen jälkeen prosessia voidaan jatkaa siten, että reikiin ladotaan mikropiirit vaiheen 1G kaltaisesti, polymeeri kovetetaan vaiheen 1H tapaan ja mikropiirit kiinnitetään vaihetta 1I vastaavasti. Tämän jälkeen piirilevyn ensimmäiselle pinnalle voidaan valmistaa polymeeri- ja metallikalvot vaihetta 1J vastaavalla tavalla.

Kuvio 4B esittää alustarakenteen esimerkinomaisen poikkileikkauksen näiden prosessivaiheiden jälkeen.

5 Kuvion 4B esittämän välivaiheen jälkeen prosessia voidaan jatkaa siten, että polymeerikalvoon valmistetaan vaiheen 1K kaltaisesti reiät kontaktointia varten. Tämän jälkeen reikiin ja levyn pinnoille valmistetaan johdekerros vaihetta 1L vastaavalla tavalla. Kuvio 4C esittää alustarakenteen esimerkinomaisen poikkileikkauksen näiden prosessivaiheiden jälkeen. Reikiin ja levyn pinnoille vaihetta 1L vastaavasti valmistettu johdekerros on selvyuden vuoksi korostettu mustalla värillä.

10 Kuvion 4C esittämän välivaiheen jälkeen prosessia voidaan jatkaa kuvioimalla levyn pinnoilla oleva johdekerros vaiheen 1M tapaan ja päällystämällä levyn pinnat vaiheessa 1N esitetyn kaltaisesti. Näiden vaiheiden jälkeen mikropiirejä ympäröi lähes yhtenäinen metallikalvo, joka muodostaa tehokkaan suojan sähkömagneettisen vuorovaikutuksen aiheuttamia häiriöitä vastaan. Tätä rakennetta on kuvattu kuviossa 4D. Kuvion 4D esittämän välivaiheen jälkeen suoritetaan vielä vaiheita 1O ja 1P vastaavat vaiheet, 15 joissa valmistetaan piirilevyn pinnalle suojakalvo ja liitokset.

Kuviossa 4D mikropiirejä suojaavien metallikerrosten poikkileikkaukset on korostettu mustalla värillä. Lisäksi kuviossa on korostettu ruutukuviolla mikropiirin tausta. Ruutukuvion tarkoitus on muistuttaa siitä, että mikropiiriä varten valmistetun reiän kaikkia sivuja peittää metallikalvo. Sivusuunnassa mikropiiriä siis ympäröi yhtenäinen 20 metallikalvo. Tämän lisäksi mikropiirin yläpuolelle voidaan suunnitella metallilaatta, joka valmistetaan piirilevyn johdekuvioiden valmistamisen yhteydessä. Vastaavalla tavalla myös mikropiirin alapuolelle valmistetaan mahdollisimman kattava metallikalvo. Mikropiirin kontaktoinnin johdosta alapuolen metallikalvoon joudutaan valmistamaan pieniä rakoja esim. kuviossa 4D esitettyyn tapaan. Nämä raot voidaan 25 kuitenkin valmistaan leveyssuunnassa niin kapeiksi tai vastaavasti korkeussuunnassa niin ohuiksi, että ne eivät heikennä sähkömagneettisia häiriöitä vastaan saatavaa suojavaikutusta.

30 Kuvion 4D esimerkkiä tarkasteltaessa on myös otettava huomioon se, että lopullinen rakenne sisältää myös sellaisia osia, jotka ulottuvat kuvion esittämää tasoa vastaan kohtisuorassa suunnassa. Tällaista kohtisuorassa suunnassa ulottuvaa rakennetta esittää kuvion 4D vasemmanpuoleisen mikropiirin vasemmanpuoleiseen kontaktinystyyn

yhdistetty johde, joka kulkee mikropiiriä sivusuunnassa ympäröivän metallikalvon ja mikropiirin alapuolella olevien johdetasojen välistä katsojaa kohti.

- 5 Kuvion 4D kuvaama ratkaisu tarjoaa siis mikropiirille erittäin hyvän suojan sähkömagneettista häiriösäteilyä vastaan. Koska suoja valmistetaan välittömästi mikropiirin ympärille, rakenne tarjoaa suojaa myös piirilevyn sisältämien komponenttien toisilleen aiheuttamia keskinäisiä häiriöitä vastaan. Sähkömagneettinen suojarakenne voidaan myös suurimmaksi osaksi maadoittaa, sillä mikropiiriä sivusuunnassa ympäröivä metallikalvo voidaan yhdistää sähköisesti piirin yläpuolella olevaan metallilaattaan. Piirilevyn johdotus taas voidaan suunnitella siten, että
- 10 metallilaatta maadoitetaan piirilevyn johderakenteen välityksellä.

Patenttivaatimukset:

1. Menetelmä ainakin yhden komponentin, jonka ensimmäisellä pinnalla on kontaktialueita, upottamiseksi alustaan, jossa menetelmässä

- otetaan alustan pohjalevy, jolla on ensimmäinen pinta ja toinen pinta,
- 5 — valmistetaan pohjalevyyn ainakin yksi reikä ainakin yhtä komponenttia varten siten, että kukin reikä ulottuu pohjalevyn läpi ensimmäisen pinnan ja toisen pinnan välillä,
- levitetään pohjalevyn toiselle pinnalle eristepolymeerikerros siten, että eristepolymeerikerros peittää ainakin yhden komponenttia varten valmistetun reiän,
- 10 — asetetaan ainakin yhteen reikään ainakin yksi komponentti siten, että komponentin ensimmäinen pinta painautuu eristepolymeerikerrokseen, ja
- kovetetaan eristepolymeerikerros.

15 2. Patenttivaatimuksen 1 mukainen menetelmä, jossa komponentin ensimmäinen pinta painetaan kovettamattomaan eristepolymeerikerrokseen.

3. Patenttivaatimuksen 1 mukainen menetelmä, jossa komponentin ensimmäinen pinta painetaan osittain kovetettuun eristepolymeerikerrokseen.

20

4. Jonkin patenttivaatimuksen 1 - 3 mukainen menetelmä, jossa eristepolymeerikerros valmistetaan asettamalla pohjalevyn toiselle pinnalle RCC-kalvo.

25

5. Jonkin patenttivaatimuksen 1 - 3 mukainen menetelmä, jossa eristepolymeerikerros valmistetaan levittämällä pohjalevyn toiselle pinnalle pre-preg-epoksikalvo.

6. Jonkin patenttivaatimuksen 1 - 5 mukainen menetelmä, jossa komponenttia varten valmistetun reiän sivuseinille kasvatetaan johdemateriaalia häiriösuojan valmistamiseksi komponentin ympärille.

5 7. Jonkin patenttivaatimuksen 1 - 6 mukainen menetelmä, jossa komponentin kontaktialueisiin liittyy kontaktiulokkeet, ja komponentti asetetaan reikään siten, että kontaktiulokkeet painautuvat eristepolymeerikerroksen sisään.

10 8. Jonkin patenttivaatimuksen 1 - 6 mukainen menetelmä, jossa komponentin kontaktialueisiin liittyy kontaktiulokkeet, joiden korkeus on vähintään yhtä suuri kuin eristepolymeerikerroksen paksuus, ja komponentti asetetaan reikään siten, että kontaktiulokkeet läpäisevät eristepolymeerikerroksen.

9. Jonkin patenttivaatimuksen 1 - 7 mukainen menetelmä, jossa

- 15
- kovetettuun eristepolymeerikerrokseen valmistetaan kontaktiaukot komponenttia varten, ja
 - kontaktiaukkoihin ja eristepolymeerikerroksen päälle valmistetaan johteet sähköisten kontaktien muodostamiseksi komponenttiin.

20 10. Jonkin patenttivaatimuksen 1 - 9 mukainen menetelmä, jossa ennen komponentin asettamista reikään pohjalevyllä valmistetaan johdinkuvioita, ja jossa komponentti asetetaan reikään siten, että komponentti kohdistetaan pohjalevyllä valmistettujen johdinkuvioiden suhteen.

25 11. Jonkin patenttivaatimuksen 1 - 10 mukainen menetelmä, jossa komponentti kiinnitetään paikalleen pohjalevyyn valmistettuun reikään täyttämällä reikä täytemateriaalilla.

12. Jonkin patenttivaatimuksen 1 - 11 mukainen menetelmä, jossa komponentti on mikropiiri ja mikropiiriin muodostetaan sähköinen kontakti pohjalevyn ensimmäisen pinnan suunnasta sen jälkeen kun mikropiiri on asetettu pohjalevyyn tehtyyn reikään.

5

13. Jonkin patenttivaatimuksen 1 - 12 mukainen menetelmä, jossa komponenttiin muodostetaan sähköinen kontakti kasvattamalla komponentin kontaktialueiden tai kontaktiulokkeiden päälle johtavaa materiaalia.

10

14. Jonkin patenttivaatimuksen 1 - 13 mukainen menetelmä, jossa sähköinen kontakti mikropiiriin muodostetaan juotteettomasti piirilevynvalmistustekniikalla.

15

15. Jonkin patenttivaatimuksen 1 - 14 mukainen menetelmä, jossa alustaan upotetaan useampi kuin yksi komponentti ja jossa pohjalevyyn valmistetaan oma reikä kullekin alustaan upotettavalle komponentille ja kukin alustaan upotettava komponentti sijoitetaan omaan reikäänsä.

20

16. Jonkin patenttivaatimuksen 1 - 15 mukainen menetelmä, jossa valmistetaan monikerrosrakenne, jossa on ainakin neljä päällekkäistä johdinkerrosta.

25

17. Jonkin patenttivaatimuksen 1 - 16 mukainen menetelmä, jossa valmistetaan ensimmäinen alusta, johon on upotettu ainakin kaksi mikropiiriä, ja ainakin yksi toinen alusta, johon on upotettu ainakin kaksi mikropiiriä, ja ladotaan ja kiinnitetään alustat päällekkäin siten, että alustat tulevat kohdistetuiksi toistensa suhteen.

18. Jonkin patenttivaatimuksen 1 - 16 mukainen menetelmä, jossa

- valmistetaan ensimmäinen ja toinen alusta sekä välikerros,
 - asetetaan toinen alusta ensimmäisen alustan yläpuolelle ja kohdistetaan toinen alusta ensimmäisen alustan suhteen,
 - tuodaan välikerros ensimmäisen ja toisen alustan väliin, ja
- 5 – laminoidaan ensimmäinen ja toinen alusta toisiinsa välikerroksen avulla.

19. Patenttivaatimuksen 18 mukainen menetelmä, jossa

- valmistetaan ainakin yksi kolmas alusta sekä välikerros kutakin kolmatta alustaa varten,
- 10 – asetetaan vuorollaan kukin kolmas alusta ensimmäisen ja toisen alustan yläpuolelle ja kohdistetaan kukin kolmas alusta jonkin alemman alustan suhteen,
- tuodaan välikerros kunkin kolmannen alustan alle, ja
 - laminoidaan ensimmäinen, toinen ja kukin kolmas alusta toisiinsa välikerrosten avulla.

15

20. Jonkin patenttivaatimuksen 17 - 19 mukainen menetelmä, jossa päällekkäin kiinnitettyjen alustojen läpi porataan reikiä läpivientejä varten ja valmistetaan porattuihin reikiin johteet kullakin alustalla olevien elektroniikkapiirien kytkemiseksi toisiinsa toiminnalliseksi kokonaisuudeksi.

20

21. Jonkin patenttivaatimuksen 1 - 20 mukainen menetelmä, jossa pohjalevyn, komponentin ja komponenttiin välittömästi liittyvän johdekerroksen lämpötila on prosessin aikana alle 200 °C ja edullisesti välillä 20 – 85 °C.

- 25 22. Elektroniikkamoduuli, joka on valmistettu jonkin patenttivaatimuksen 1 - 21 mukaisella menetelmällä.

64
(57) Tiivistelmä:

Tässä julkaisussa on kuvattu menetelmä, jossa elektroniikka-piiriin tulevat puolijohdekomponentit tai ainakin osa niistä upotetaan alustaan, kuten piirilevyyn, alustan valmistamisen aikana, jolloin osa alustarakenteesta ikään kuin valmistetaan puolijohdekomponenttien ympärille. Keksinnön mukaan alustaan valmistetaan läpireiät puolijohdekomponentteja varten siten, että reiät ulottuvat alustan ensimmäisen ja toisen pinnan välillä. Reikien valmistamisen jälkeen ja alustarakenteen toisen pinnan yli levitetään polymeerikalvo siten, että polymeerikalvo peittää myös puolijohdekomponentteja varten valmistetut läpireiät alustarakenteen toisen pinnan puolelta. Ennen polymeerikalvon kovettamista tai osittaisen kovettamisen jälkeen puolijohdekomponentit sijoitetaan alustaan valmistettuihin reikiin alustan ensimmäisen pinnan suunnasta. Puolijohdekomponentit painetaan polymeerikalvoa vasten siten, että ne kiinnittyvät polymeerikalvoon. Tämän jälkeen suoritetaan polymeerikalvon lopullinen kovetus.

(Kuvio 2C)

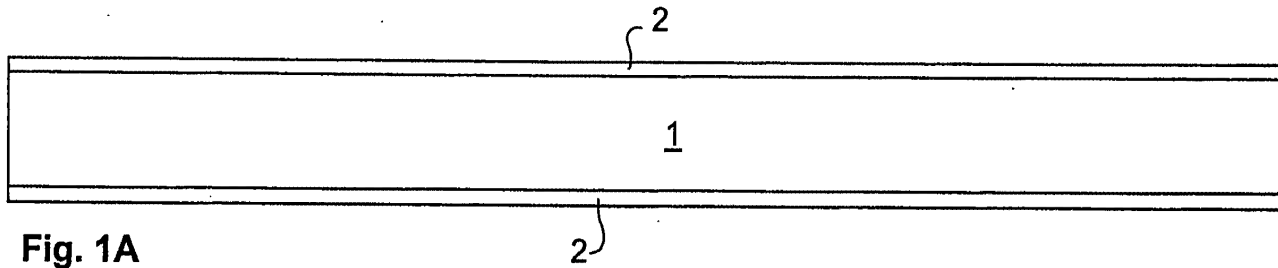


Fig. 1A

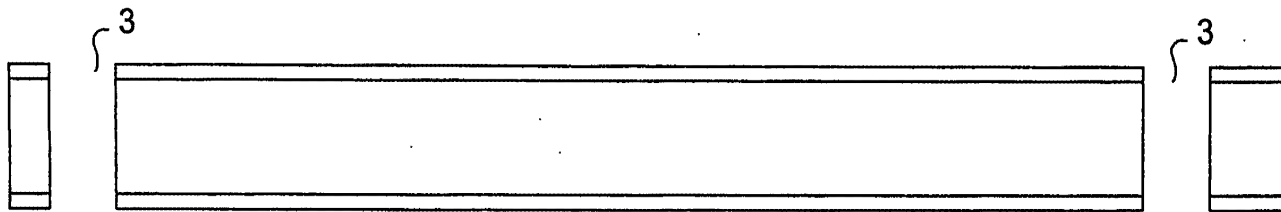


Fig. 1B

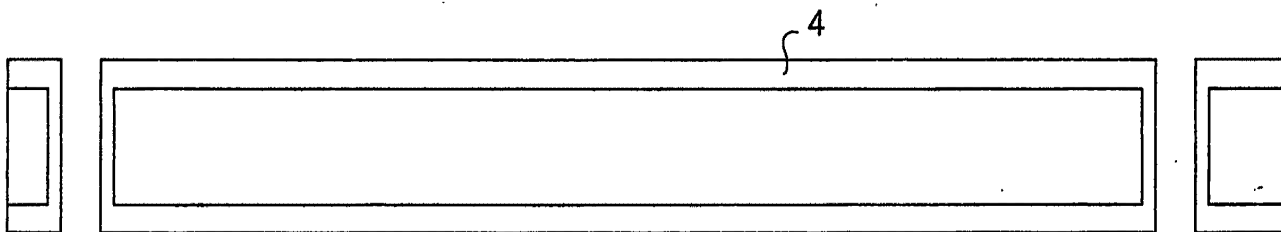


Fig. 1C

FIG. 1D

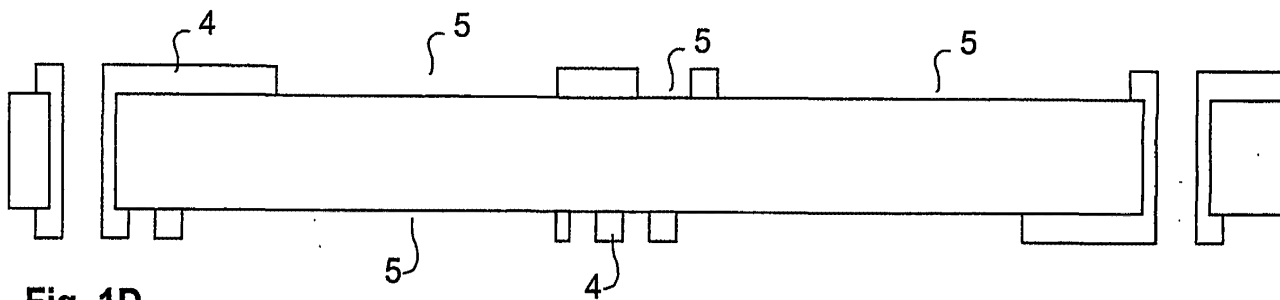


Fig. 1D

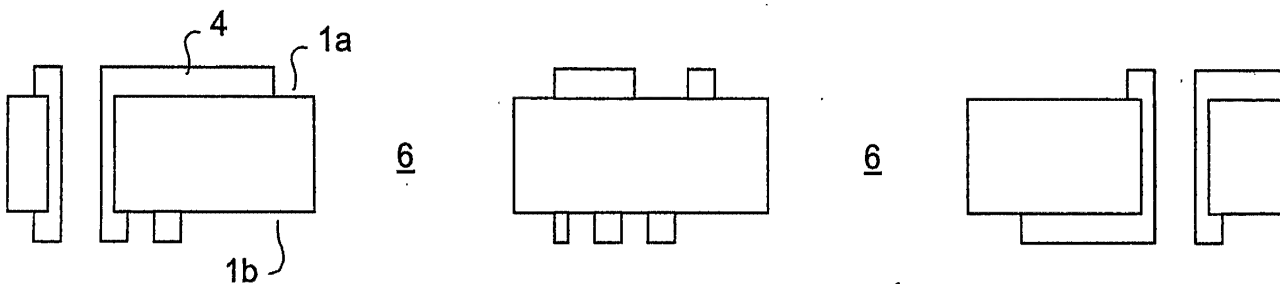


Fig. 1E

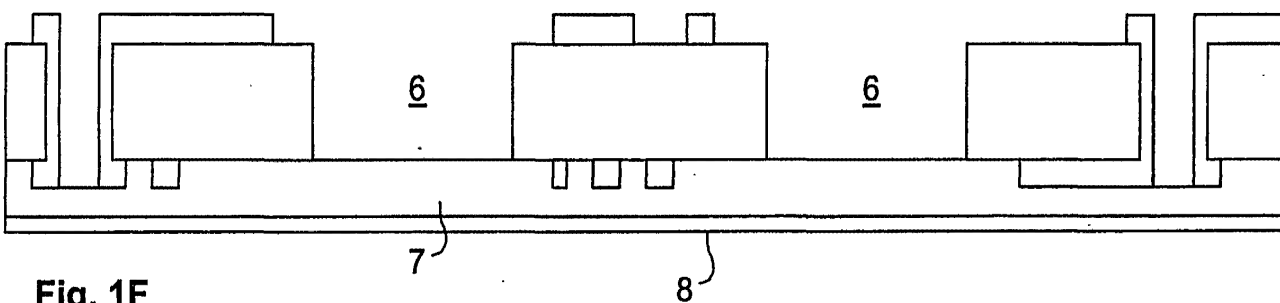


Fig. 1F

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26

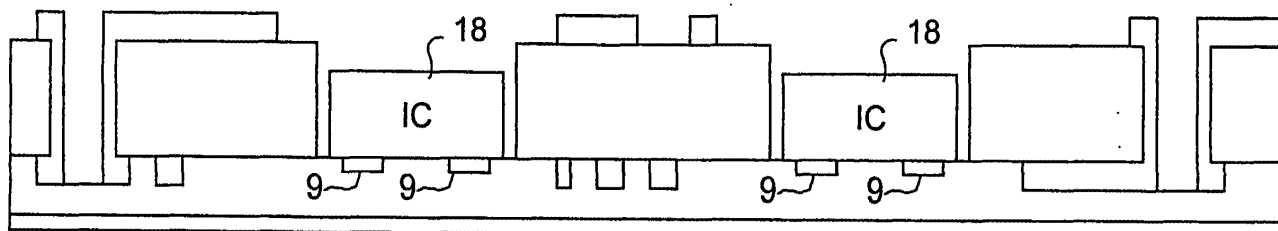


Fig. 1G

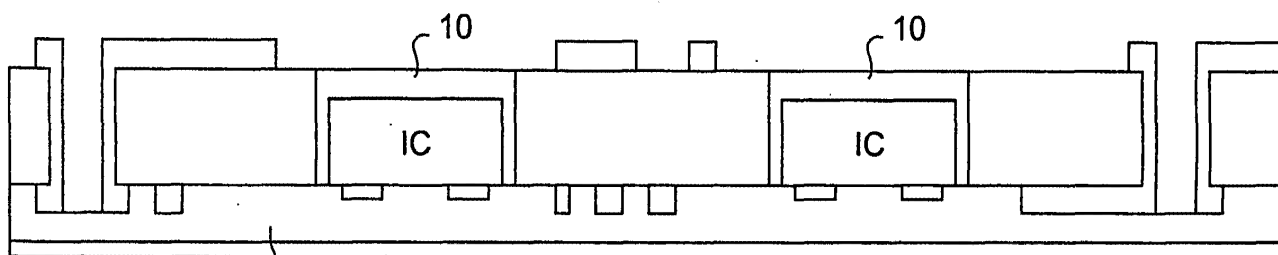


Fig. 1I

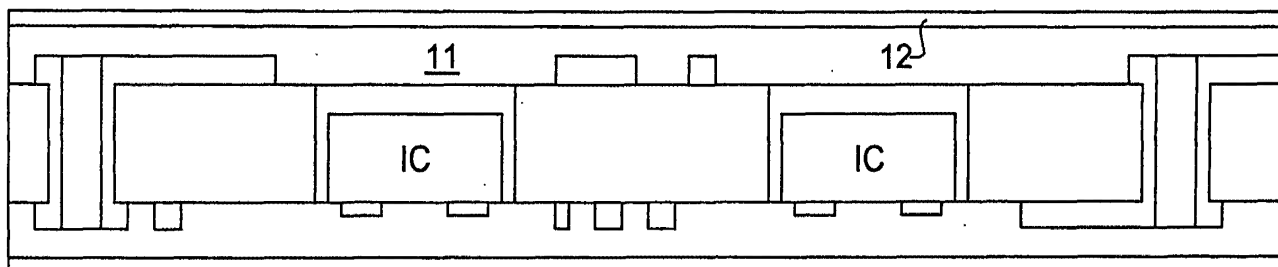


Fig. 1J

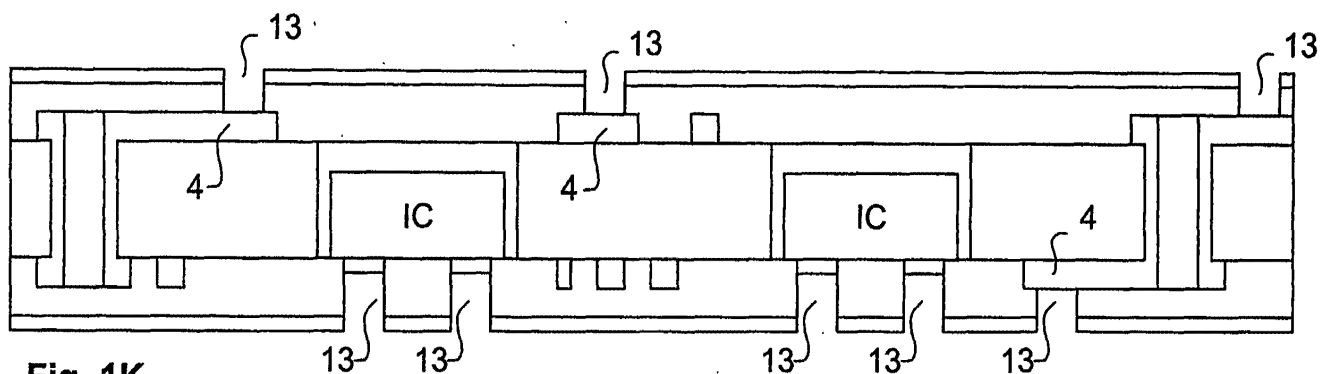


Fig. 1K

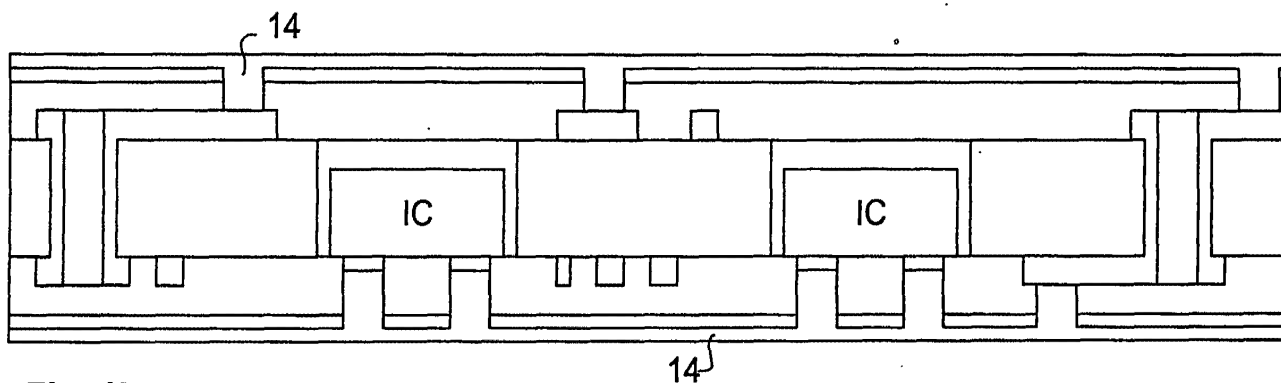
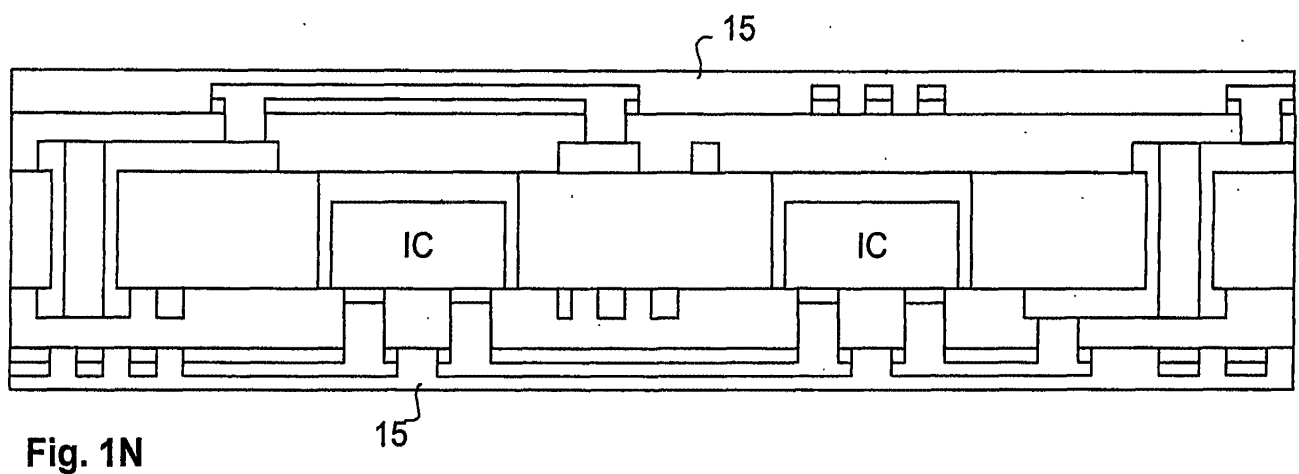
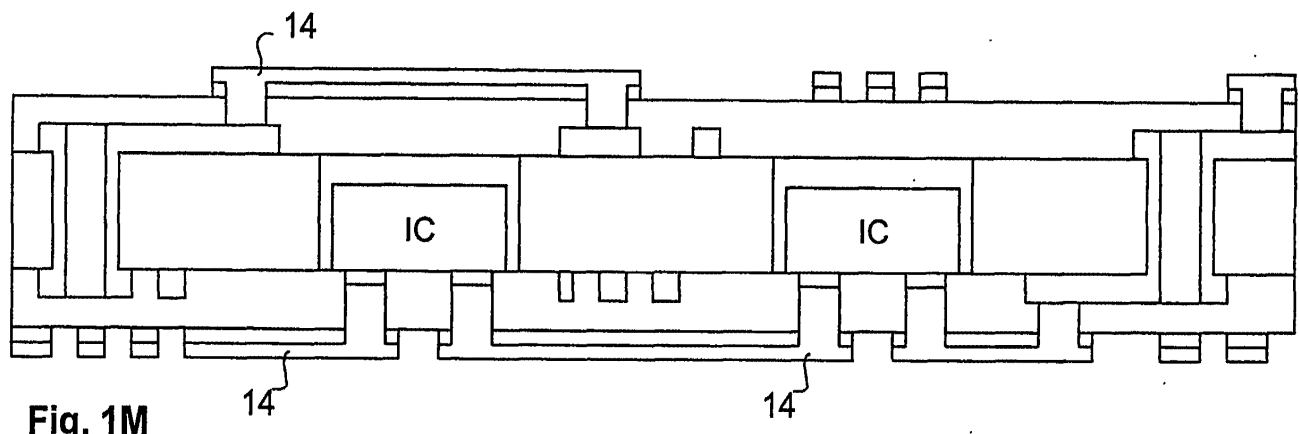


Fig. 1L

11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100



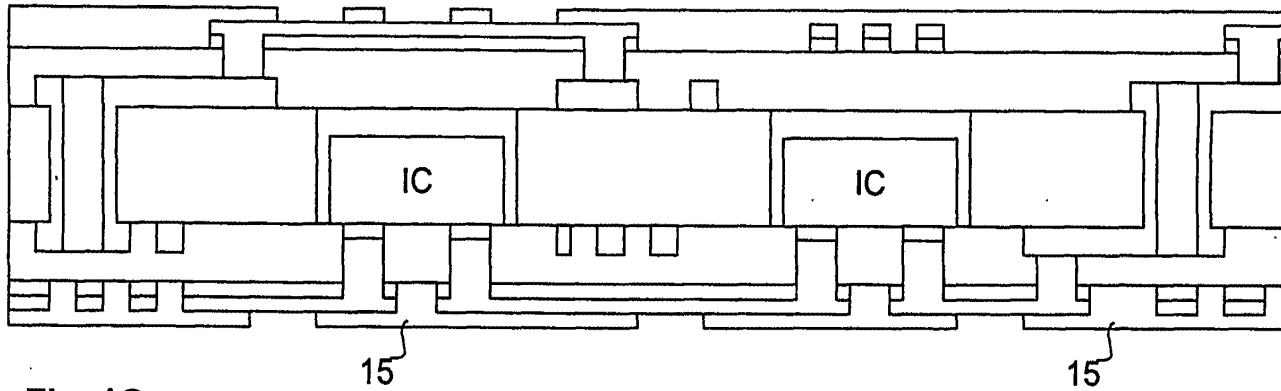


Fig. 10

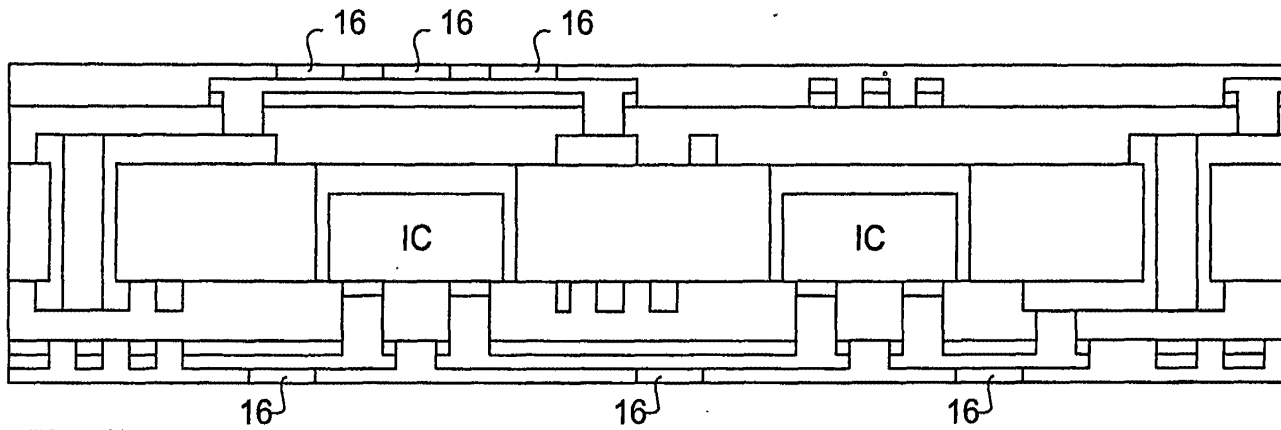


Fig. 1P

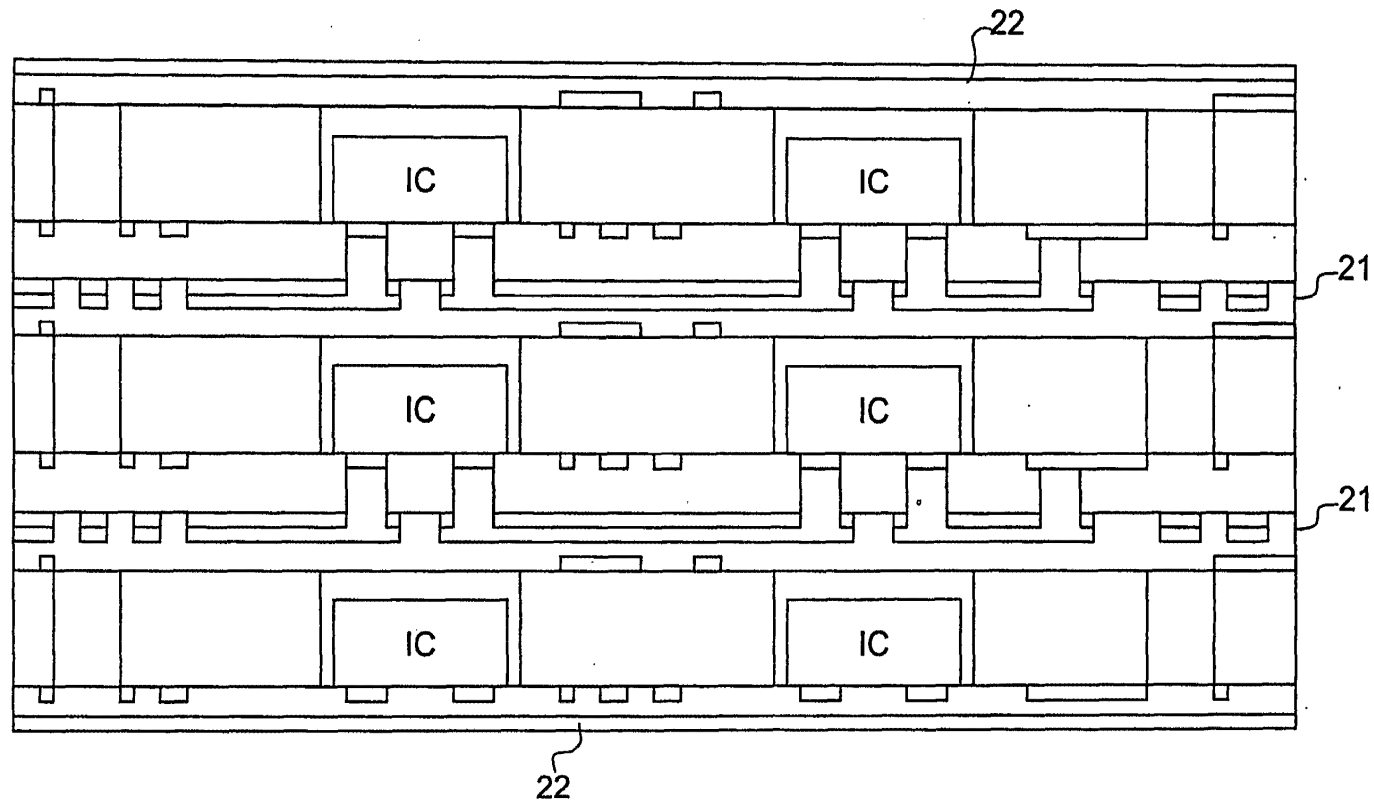


Fig. 2B

FIG. 2C

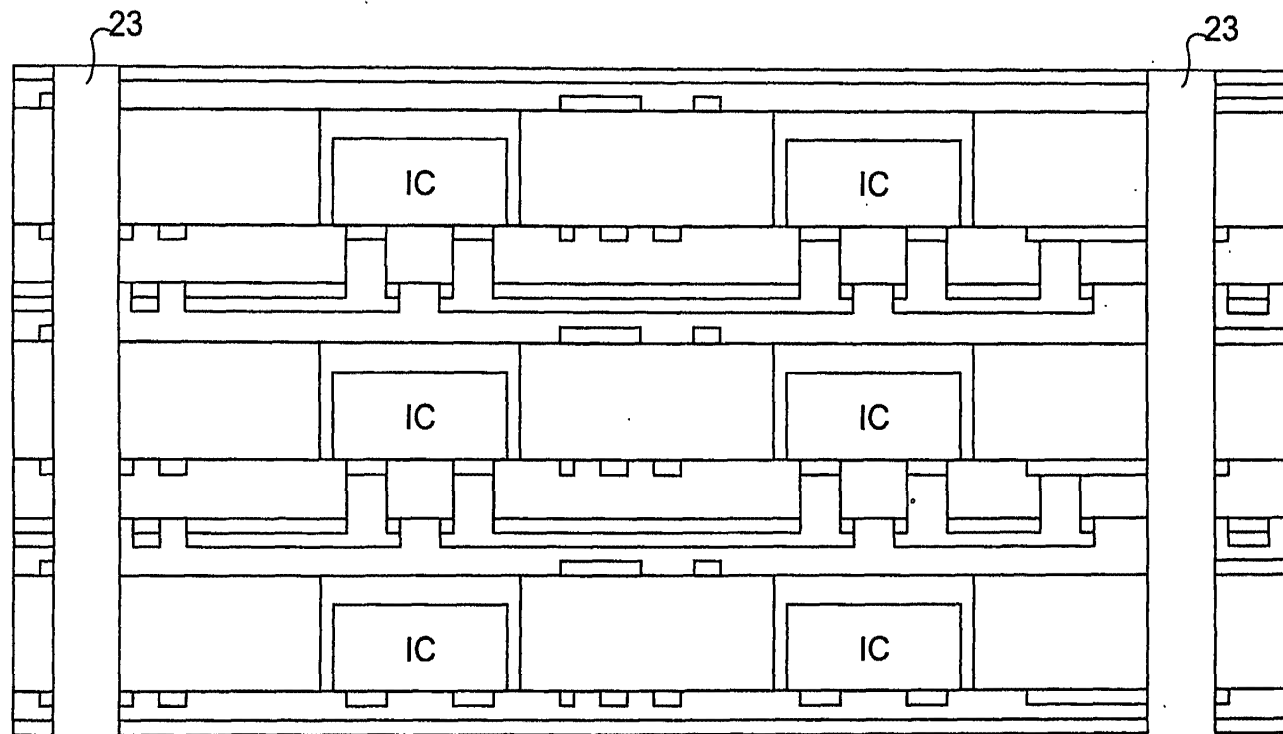


Fig. 2C

2.5

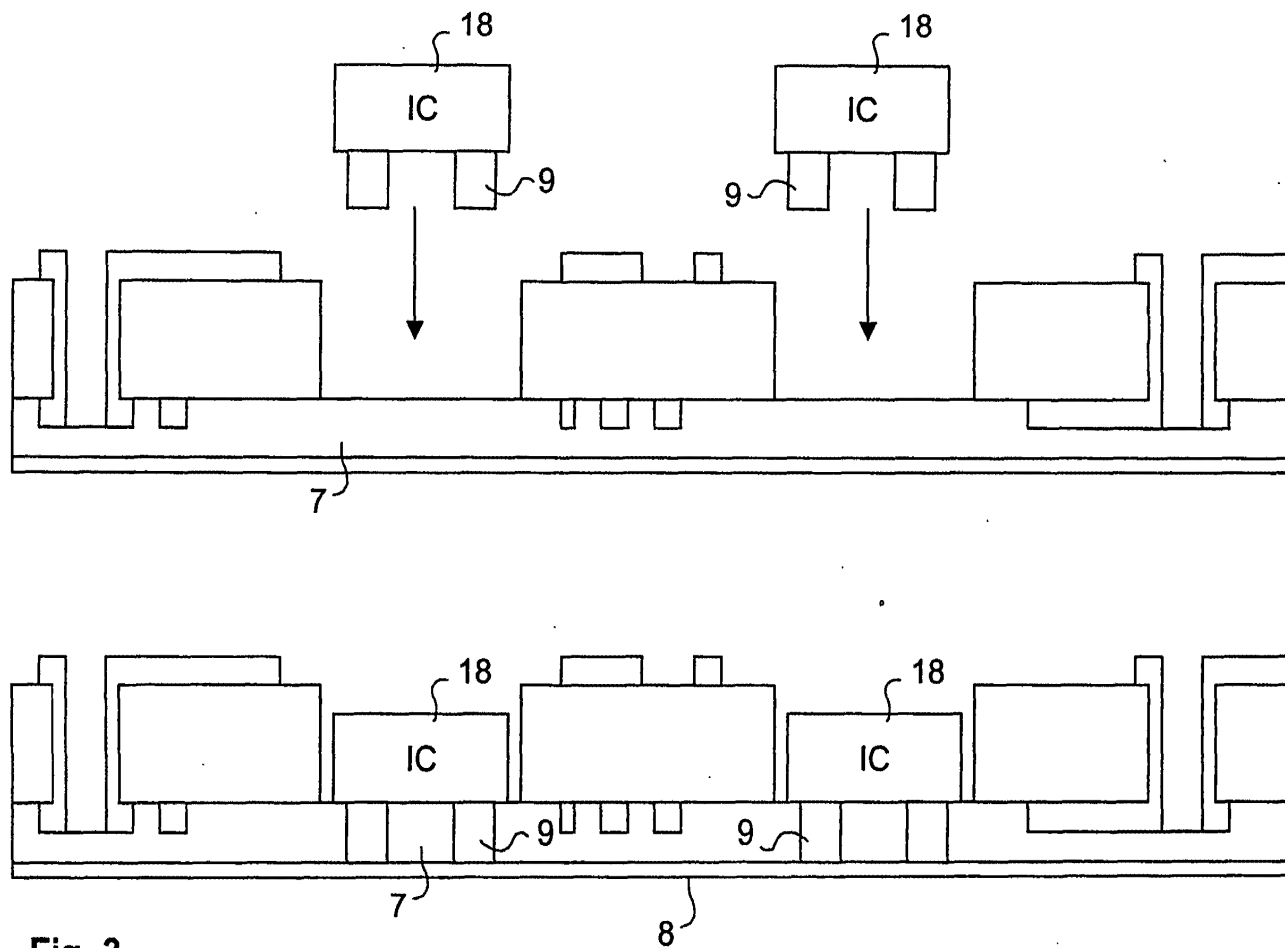
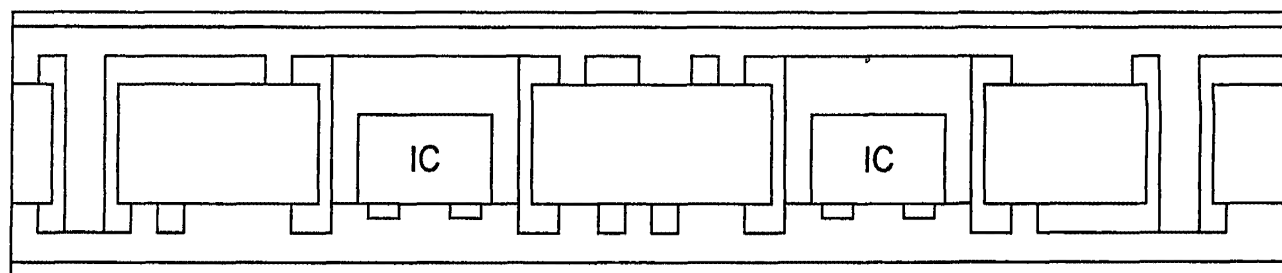
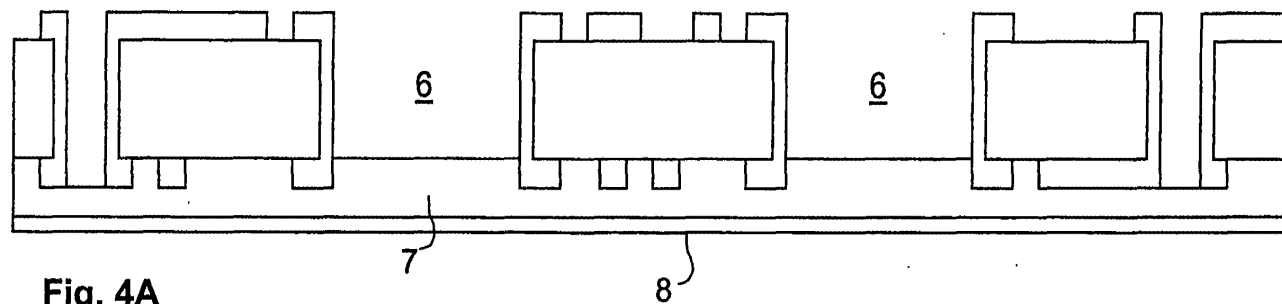


Fig. 3



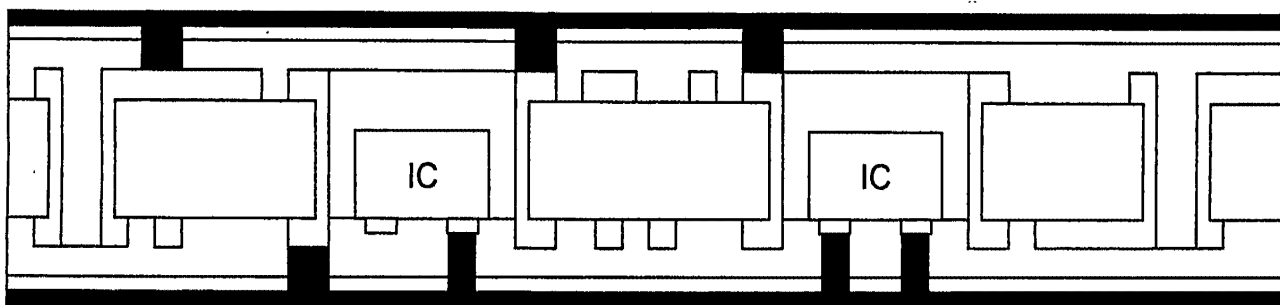


Fig. 4C

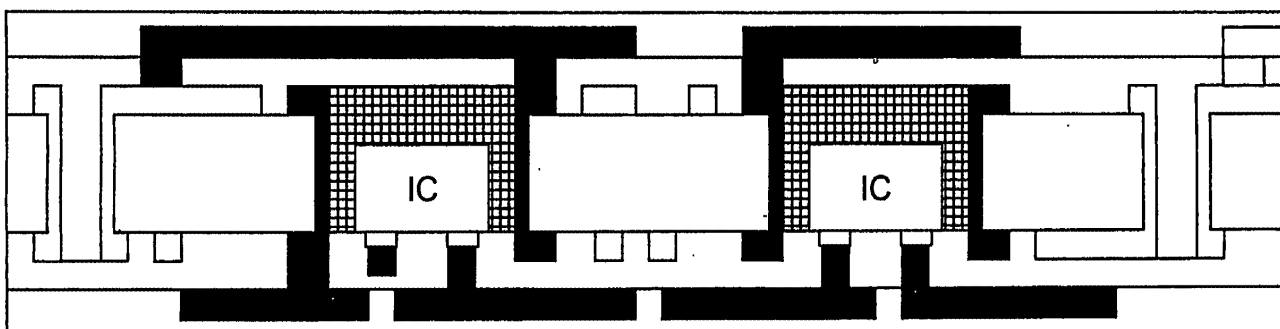


Fig. 4D

INTERNATIONAL STAGE WORKSHEET (DO/EO)

U.S. APPL. NO. 10/502336 INTERNATIONAL APPL. FI03/00065

APPLICATION FILED BY: 20 MOS. _____ OR 30 MOS. _____ SCREENED BY SK

INTERNATIONAL APPLICATION PAPERS IN THE APPLICATION FILE:

- ☒ International application
- ☐ Article 19 amendments
- ☒ Priority Document(s) No. (1)
- ☐ Request Form PCT/RO/101
- ☐ PCT/IB/302
- ☐ PCT/IB/304
- ☐ PCT/IB/306
- ☐ PCT/IB/308
- ☐ PCT/IB/331
- ☐ OTHER PCT/IB/ _____
- ☐ PCT/PEPA/409 also 416

- ☐ 409 annexes to IPR
- ☒ PCT/ISA/210 (Search report)
- ☐ Search report References
- ☒ Other Papers filed AOS

WIPO PUBLICATION
PUBLICATION NO. WO 03/065779
PUBLICATION DATE 7 Aug 03
PUBLICATION LANG. English
NOT PUBLISHED
U.S. only _____ Requested

RECEIVED FROM THE APPLICANT: (other than checked above)

- ☒ National application basic fee paid
- ☐ Express Processing Requested
- ☐ Translation of the International Application
- ☐ Used the IB copy of the IA
- ☒ Description
- ☒ Claims (12)
- ☒ Drawings
- ☐ Foreign Language in drawing
- ☐ Article 19 Amendments
- ☐ Amendment used in application
- ☐ Article 34 Amendment
- ☐ Amendment used in application
- ☐ DNA
- ☐ I194 transaction done

- ☐ Preliminary Amendment(s) filed _____
- ☐ second submission
- ☒ Information Disclosure Statement 23 July 04
- ☒ second submission 23 July 04
- ☐ Assignment
- ☐ Forward to Assignment Branch
- ☐ Substitute Specification
- ☐ Small Entity Statement
- ☐ type _____
- ☒ Oath/Declaration (date submitted 23 Sep 04)
- ☐ Not executed
- ☒ Executed
- ☐ Power of Attorney
- ☐ Change of Address

(prepared surcharge)

(30)

35 USC Receipt of Request (PTO - 1399 Transmittal Letter)

Date Acceptable oath/declaration received

102(e) Date

Date complete 35 USC 371 requirements met

DATE NOTICE COMPLETED

DO/EO 903 Notice of Acceptance

DO/EO 905 Notice of Missing Requirements

DO/EO 917 Notice of A defective oath or declaration

DO/EO 916 Notice of defective response

DO/EO 913 Notice of defective translation

DO/EO 909 Notification of Abandonment

INTERNATIONAL SEARCH REPORT

Rec'd PCT/PTO 23 JUL 2004

International Application No.

PCT/FI/00065

A. CLASSIFICATION OF SUBJECT MATTER

10/502336

IPC7: H05K 1/18, H05K 3/46

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI DATA, EPO-INTERNAL, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4246595 A (MASAHARU NOYORI ET AL), 20 January 1981 (20.01.81), column 4, line 29 - line 36; column 8, line 34 - column 9, line 23; column 11, line 8 - line 10, figures 8a-8f, column 11, line 38 - line 43	1-25
	--	
A	PATENT ABSTRACTS OF JAPAN vol.2002, no 05, 3 May 2002 (2002.05.03) & JP 2002 016327 A (NGK SPARK PLUG CO LTD) 18 January 2002 (2002-01-18) abstract	1-25
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☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

Date of mailing of the international search report

8 May 2003

14-05-2003

Name and mailing address of the ISA/
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INTERNATIONAL SEARCH REPORT

Information on patent family members

29/03/03

International application No.

PCT/JP03/00065

Patent document cited in search report			Publication date	Patent family member(s)		Publication date
US	4246595	A	20/01/81	CA	1108305 A	01/09/81
				DE	2810054 A,C	14/09/78
				GB	1588377 A	23/04/81
				JP	1192560 C	29/02/84
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				US	4356374 A	26/10/82
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				JP	53124976 A	31/10/78
				JP	59029145 B	18/07/84
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				JP	58006951 B	07/02/83

19/10/04

1

METHOD FOR EMBEDDING A COMPONENT IN A BASE

The present invention relates to a method for embedding one or more components in a base.

5

The bases that are processed using the methods to which the present invention relates are used as bases for electrical components, typically semiconductor components and particularly microcircuits, in electronic products. The task of the base is to provide a mechanical attachment base for the components and the necessary electrical connections to the other components on the base and outside the base. The base can be a circuit board, so that the method that is the object of the invention is closely related to circuit-board manufacturing technology. The base can also be some other base, for example, a base used for packaging a component or components, or the base of an entire functional module.

15

Circuit-board manufacturing technologies differ from microcircuit manufacture in, among other things, the fact that the substrate used in microcircuit manufacturing technologies is a semiconductor material, whereas the base material of a circuit board is an insulator. Microcircuit manufacturing technologies are also typically considerably more expensive than circuit-board manufacturing technologies.

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Circuit-board manufacturing technologies differ from packaging techniques in that packaging techniques are intended to form a package around a semiconductor component, which will facilitate its handling. The surface of a package of a semiconductor component has contact parts, typically protrusions, which allow the packaged component to be easily installed on a circuit board. A semiconductor package also contains conductors, through which voltage can be connected to the actual semiconductor, connecting the protruding contact parts outside the package to the contact areas on the surface of the semiconductor component.

25
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However, the packages of components manufactured using conventional technologies take up a considerable amount of space. The miniaturization of electronic devices has

led to an attempt to eliminate the packaging of semiconductor components. For this purpose, the so-called flip-chip technology for instance, has been developed, in which a semiconductor component without a package is assembled directly onto the surface of the circuit board. There are, however, many difficulties in flip-chip technology. For example, problems can arise with the reliability of connections, especially in applications in which mechanical stresses arise between the circuit board and the semiconductor component. Mechanical stresses must be evened by adding a suitable underfill between the chip and the circuit board. This procedure slows down the process and increases manufacturing costs. Stresses arise particularly in applications in which a flexible circuit board is used and the circuit board is flexed strongly.

Object of the invention is to create a method, by means of which unpacked microcircuits can be embedded to a base reliably but economically.

The invention is based on embedding the semiconductor components, or at least some of them, in a base, such as a circuit board, during the manufacture of the board, whereby part of the base structure is, as it were, manufactured around the semiconductor components. According to the invention, feed-throughs for semiconductor components are made in the base in such a way that the holes extend between the first and second surfaces of the base. After the holes have been made, a polymer film is spread over the second surface of the base structure in such a way that the polymer film also covers the feed-throughs made for the semiconductor components, from the second side of the base structure. Before the hardening of the polymer film, or after partial hardening, the semiconductor components are placed, from the direction of the first side of the base, in the holes that have been made. The semiconductor components are pressed against the polymer film so that they adhere to the polymer film. After this, the final hardening of the polymer film is carried out. According to the invention, a conductive pattern is made in the base, before a component is placed in the holes, and the component is placed in the hole in such a way that the component is aligned in relation to the conductive patterns made on the baseboard.

More specifically, the method according to the invention is characterized by what is

stated in the characterizing portion of Claim 1.

Considerable advantages are gained with the aid of the invention. This is because, with the aid of the invention, a circuit board can be manufactured with the semiconductor components embedded inside it. The invention also makes it possible to manufacture a small and reliable component package around a component.

The invention also permits a large number of embodiments, which provide significant additional advantages.

10

For example, with the aid of preferred embodiments of the invention, the component's packaging stage, the circuit board's manufacturing stage, and the assembly and contact-making stage of the semiconductor components can be combined to form a single totality. The combination of the various process stages brings important logistic benefits and permits the manufacture of a smaller and more reliable electronic module. There is the further advantage that such a manufacturing method can largely exploit circuit board manufacturing and assembly technologies that are in general use.

According to a preferred embodiment of the invention, the totality of the composite process is simpler than, for example, using flip-chip technology to manufacture a circuit board and attach the components to the circuit board. By means of such preferred embodiments, the following advantages over the conventional solution are obtained:

- Soldering is not required to form contacts with the components, instead an electrical contact can be manufactured by growing conductors on top of the contact areas of a semiconductor component. This means that there is no need to use molten metal to connect the components, so that compounds are not formed between metals. Compounds between metals are generally brittle, so that reliability is improved compared to connections made by soldering. Particularly in small connections, the brittleness of the metal compounds in the connections causes great problems. According to a preferred embodiment, it is possible to achieve clearly smaller structures in a solderless solution than in soldered

solutions. The solderless contact-making method also has the advantage that high temperatures are not required to form contacts. A lower process temperature permits greater choice when selecting other materials of the circuit board, the component package, or the electronics module. In the method, the temperature of the circuit board, the component, and the conductive layer directly connected to the component can be kept in the range 20 - 85°C. Higher temperatures, for example, of about 150°C, may be needed only when curing (polymerizing) the polymer films used. However, the temperature of the baseboard and the components can be kept under 200°C during the entire process. If the method employs polymer films that are hardened in other ways than due to the effect of a high temperature, for example, chemically, or by electromagnetic radiation, the temperature of the baseboard and the components can, in a preferred embodiment, be kept under 100°C during the entire process.

- Because the use of the method permits the manufacture of smaller structures, the components can be spaced more closely. The conductors between the components can then also be shorter while the electrical properties of the electronic circuit improve, for example, by reducing losses, interference, and delay times.

- The method also permits the manufacture of three-dimensional structures, as the bases and the components embedded in the bases can be assembled on top of each other.

- In the method, it is also possible to reduce the interfaces between different metals.

- The method permits a lead-free process.

The invention also permits other preferred embodiments. In connection with the invention, flexible circuit boards, for instance, can be used. Further, the process permits

circuit boards to be assembled on top of each other.

With the aid of the invention, it is also possible to manufacture extremely thin structures, in which the semiconductor components are, despite its thinness, entirely protected within a base, such as a circuit board.

Because the semiconductor components can be placed entirely inside the circuit board, the joints between the circuit board and the semiconductor components are mechanically durable and reliable.

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In the following, the invention is examined with the aid of examples and with reference to the accompanying drawings.

Figure 1 shows a series of cross-sections of one process according to the invention.

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Figure 2 shows a series of cross-sections of a second process according to the invention.

Figure 3 shows a schematic diagram of one possible contact-forming method.

Figure 4 shows a series of cross-sections of a third process according to the invention.

The series of illustrations shown in Figure 1 show one possible process according to the invention. In the following, the process of Figure 1 is examined in stages:

25 **Stage A (Figure 1A):**

In stage A, a suitable baseboard 1 is selected for the circuit-board manufacturing process. The baseboard 1 can be, for example, a glass-fibre reinforced epoxy board, such as an FR4-type board. In the example process, the baseboard 1 can thus be an organic board, as the example process does not require high temperatures. A flexible and cheap organic board can thus be selected for the baseboard 1. Typically a board that is already coated with a conductive material 2, usually copper, is selected for the baseboard 1. Of

30

course, an inorganic board can also be used.

Stage B (Figure 1B):

- 5 In stage B, through holes 3 are made in the baseboard for electrical contacts. The holes 3 can be made, for example, with some known method used in circuit-board manufacture, such as mechanical drilling.

Stage C (Figure 1C):

10

In stage C, metal is grown into the through holes made in stage B. In the example process, the metal 4 is also grown on top of the circuit board, thus also increasing the thickness of the conductive layer 2.

- 15 The conductive material 4 to be grown is copper, or some other material with sufficient electrical conductivity. Copper metallizing can take place by coating the holes with a thin layer of chemical copper and then continuing the coating using an electrochemical copper-growing method. Chemical copper is used in the example, as it will also surface on top of a polymer and act as an electrical conductor in electrochemical coating. The
20 metal can thus be grown using a wet-chemical method, so that the growth is cheap. Alternatively, the conductive layer 4 can be made, for example, by filling the through holes with an electrically conductive paste.

Stage D (Figure 1D):

25

In stage D, the conductive layer on the surface of the circuit board is patterned. This can be done by utilizing generally known circuit-board manufacturing methods. The patterning of the conductive layer is aligned, for example, on the holes made in stage B.

- 30 The manufacture of the conductor pattern can take place, for example, by laminating, on the surface of the metal 4, a photolithographic polymer film, on which the desired conductive pattern is formed by directing light through a patterned mask. After

exposure, the polymer film is developed, when the desired areas are removed from it and the copper 4 under the polymer is revealed. Next, the copper revealed under the film is etched away, leaving the desired conductive pattern. The polymer acts as a so-called etching mask and openings 5, at the foot of which the baseboard of the circuit board is revealed, are formed in the metal layer 4. After this, the polymer film is also removed from on top of the copper 4.

Stage E (Figure 1E):

10 In stage E, holes 6 are made in the baseboard for the microcircuits. The holes extend through the entire baseboard, from the first surface 1a to the second surface 1b. The holes may be made, for example, mechanically milling by means of a milling machine. The holes 6 can also be made, for example, by stamping. The holes 6 are aligned relative to the conductive patterns 4 of the circuit board. The holes 3 made during stage B can
15 also be used to aid alignment, but then too the alignment is relative to the conductive patterns 4, as the conductive patterns 4 have a specific position in relation to the holes 3.

Stage F (Figure 1F):

20 In stage F, a polymer film 7 forming an electrical insulation is made on the second surface 1b of the baseboard and over the holes 6. The polymer film 7 is made in such a way that it is sufficiently rigid to retain the main features of its shape, but, however, not hardened, so that components can be attached by pressing them into the film. The polymer film should also be sufficiently rigid to be able to hold the components pressed
25 into the film essentially immovable in relation to the base, during the following process stages.

The polymer film made in Stage F can be, for example, a pre-preg-type film.

30 If desired, a metal coating 8 can also be made on top of the polymer film 7 in stage F.

In the example process, stage F is carried out by laminating a thin polymer film (e.g., c.

- 40 μm) on the surface of the circuit board, on top of which is a layer of copper (e.g., c. 5 μm). Lamination takes place with the aid of pressure and heat. In the example process, the film is thus an RCC (Resin Coated Copper) foil. The lamination must then be carried out to be uncompleted, so that the polymer is not completely hardened. This is achieved
- 5 by setting the laminating temperature sufficiently low and/or by shortening the duration of the heat treatment.

Stage G (Figure 1G):

- 10 In stage G, the microcircuits 18 are assembled in the holes 6, from the side of the first surface 1a of the baseboard. Assembly can take place using a precision assembly machine, the microcircuits 18 being aligned relative to the conductive patterns of the circuit board. As in stage E, the holes made in stage B can be used to aid alignment.
- 15 The microcircuits 18 are assembled in such a way that they adhere to polymer film 7 in the 'bottoms' of the holes 6. The most suitable way to carry out assembly is to use such a force that the microcircuits 18 push slightly inside the polymer film 7, so that the microcircuits are made to remain in place better. It is also advantageous to the process, if the microcircuits being assembled have contact protrusions 9, which penetrate inside the
- 20 polymer film 7.

- Figure 3 shows an interesting alternative embodiment, in which the contact protrusions 9 of the microcircuits are so long that they extend right through the polymer film 7 to the metal coating 8. In that case, there is no need to make holes in the polymer film 7 (Stage
- 25 K) for making contacts in the microcircuits, as the holes are formed in connection with the assembly of the components. In addition, the metallizing stage (Stage L) of the holes can be simplified, as the contact protrusions 9 automatically form conductor columns through the polymer film 7. In the embodiment of Figure 3, the contact protrusions can also be given a sharp shape, so that their penetration ability improves. If the contact
- 30 protrusions 9 are sufficiently long and sharp, they can also penetrate the metal coating 8 and in principle form an electrical contact between the microcircuit 18 and the metal

coating 8.

Stage H (not shown):

- 5 In stage H, the polymer film 7 is hardened with the aid of curing. Curing generally comprises a heat treatment, but the process can also employ some treatment other than heat to harden the polymer. If desired, stage H can also be omitted, particularly in connection with polymers cured by heat treatment. However, hardening the polymer at this stage prevents the microcircuit from moving relative to the base during stage I.

10

Stage I (Figure 1I):

- In stage I, the microcircuits are secured to the baseboard of the circuit board by filling the holes made for the microcircuits with a filler material 10. In the example process, this stage is carried out by spreading casting epoxy into the holes from the first surface (1a) of the circuit board and on top of the microcircuits. The epoxy is smoothed with a spatula and hardened by curing in an autoclave. At the same time, the polymer film 7 is also hardened, if the process does not include stage H.

20 **Stage J (Figure 1J):**

- In stage J, a polymer film 11 is formed on the first surface (1a) of the circuit board, followed by a thin metal coating 12 on top of the polymer film.
- 25 In the example process, stage J is carried out by laminating a thin polymer film (e.g., c. 40 μm) on the surface of the circuit board, on top of which is a layer of copper (e.g., c. 5 μm). Lamination takes place with the aid of pressure and heat. In the example process, the film is thus an RCC (Resin Coated Copper) foil.
- 30 The polymer film can also be made by, for example, spreading polymer in a liquid form on the circuit board. Thus lamination is not essential in stage J. What is essential is that

an insulating layer, typically a polymer film, is made on the circuit board, which contains the embedded components, particularly embedded microcircuits. The polymer film itself can be, according to the embodiment, a filled or unfilled polymer film. The polymer film can also be coated with metal, but this is not essential, as the conductive surface can also be made later, on top of a polymer layer that is already attached to the circuit board.

Stage J makes it possible to use conventional manufacturing methods and work stages used in circuit board manufacture in the example process and nevertheless to be able to bury microcircuits and other components inside the circuit board.

Stage K (Figure 1K)

In stage K, holes 13 are made in the polymer films 7 and 11 (and at the same time in the conductive foils 8 and 12), through which it is possible to create contacts with the conductive patterns and feed-throughs (conductive material 4) of the circuit board and with the microcircuits.

The holes 13 can be made, for example, using a laser, or some other suitable method. The conductive patterns made in stage D, or the through holes made in stage B can be used for alignment.

Stage L (Figure 1L):

Stage L corresponds to stage C. In stage L, a conductive layer 14 is made in the holes 13 and on the surfaces of the circuit board.

In the example process, the feed-throughs (holes 13) are first of all cleaned using a three-stage desmear treatment. After this, the feed-throughs are metallized by first forming a catalysing SnPd surface on the polymer and after that depositing a thin layer (about 2 Fm) of chemical copper onto the surface. The thickness of the copper 14 is increased by electrochemical deposition.

Alternatively, the feed-throughs can be filled with an electrically conductive paste or made using some other suitable micro-via metallizing method.

5 **Stage M (Figure 1M):**

In stage M, a conductive pattern is formed in the same way as in stage D.

Stages N and O (Figures 1N and 1O):

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In stages N and O, a photolithographic polymer 14 is spread on the surface of the circuit board and the desired pattern is formed in the polymer 14 (in a manner similar to that in stages D and M). The exposed polymer film is developed, but the polymer film pattern remaining on the circuit board is not removed.

15

Stage P (Figure 1P):

In stage P, the connection areas of the polymer film pattern formed in the previous stage are coated 16. The coating 16 can be made with, for example, a Ni/Au coating, or an
20 OSP (organic surface protection).

The example of Figure 1 depicts one process, which can be used to exploit our invention. Our invention is thus in no way restricted to the process described above, but
25 instead the invention covers a large group of different process and their end products, to the full extent of the Claims and allowing for equivalency interpretations. In particular, the invention is in no way restricted to the layout shown in the example, instead it will be obvious to one versed in the art that the processes according to our invention can be used to manufacture many kinds of circuit boards, which differ greatly from the
30 examples disclosed here. Thus, the microcircuits and connections of the figures are only shown to illustrate the manufacturing process.

A great many changes can thus be made to the process of the example disclosed above, without nevertheless deviating from the idea according to the invention. The changes can relate to the manufacturing techniques depicted in the various stages, or, for example, to the mutual sequence of the stages. For example, stage B can equally well be carried out after stage D, i.e. the procedure can be to align the drill on the pattern, instead of aligning the pattern on the drilled holes. Correspondingly, the order of stages D and E can also be reversed. The component holes 6 are then made before the conductive patterns are formed. In that case, the conductive pattern is aligned relative to the holes 6 (and also the holes 3). Irrespective of the order in which stages B, D, and E are carried out, the polymer film 7 to be made in stage F covers the holes 6 and the conductive pattern formed on the second surface 1b of the baseboard.

Stages that are felt to be required can also be added to the process of the example disclosed above. For example, a foil that protects the surface of the circuit board during the casting taking place in stage H can be laminated onto the first side (1a) of the circuit board. Such a protective foil is manufactured so that it covers all the other areas except for the holes 6. The protective foil keeps the surface of the circuit board clean when the casting epoxy is spread with the spatula. The protective foil can be made in a suitable stage before stage I and removed from the surface of the circuit board immediately after the casting.

With the aid of the method, it is also possible to manufacture component packets to be attached to the circuit board. Such packets can also include several semiconductor components, which are connected electrically to each other.

The method can also be used to manufacture entire electrical modules. The process shown in Figure 1 can also be applied in such a way that the conductive structure is made only on the second side (1b) of the circuit board, to which the contact surfaces of the microcircuit are oriented.

The method makes it possible to manufacture, for example, circuit boards or electrical modules, in which the thickness of the baseboard used is in the range 50 - 200 microns

and the thickness of the microcircuit and microcircuits is in the range 50 - 150 microns. The pitch of the conductors can vary, for example, in the range 50 - 250 microns while the diameter of the micro-feed-throughs can be, for example, 15 - 50 microns. Thus, the total thickness of a single board in a one-layer construction will be about 100 - 300
5 microns.

The invention can also be applied in such a way that circuit boards are assembled on top of each other, thus forming a multi-layer circuit structure, in which there are several circuit boards manufactured according to Figure 1 set on top of each other and connected
10 electrically to each other. The circuit boards set on top of each other can also be circuit boards in which the conductive structure is formed only on the second side 1b of the circuit board, but which nevertheless include feed throughs, through which an electrical contact can also be formed to the microcircuits from the first side of the circuit board. Figure 2 shows one such process.

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Figure 2 shows the connection of circuit boards to each other. In the following, the process is described in stages.

Stage 2A (Figure 2A):

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Stage 2A depicts the circuit boards being set on top of each other. The lowest circuit board can be obtained, for example, after stage J of a modified process of Figure 1. In this case, the process of Figure 1 is then modified by omitting stage 1C.

25 The middle and upper circuit boards in turn can be obtained after stage M of a modified process of Figure 1, for instance. In this case, the process of Figure 1 is modified by omitting stage 1C and performing stages J, K, and L on only the second side (1b) of the circuit board.

30 In addition to the circuit boards, Figure 2A also shows pre-preg epoxy layers 21 placed between the circuit boards.

Stage 2B (Figure 2B):

5 In stage 2B, the circuit boards are laminated together with the aid of pre-preg epoxy layers 21. In addition, a metal-coated polymer film 22 is made on the upper surface of the circuit board. The process corresponds to stage J of the process of Figure 1. In the example process, a metal-coated polymer film 22 is already on the under surface of the circuit board.

Stage 2C (Figure 2C):

10

In stage 2C, holes 23, for the formation of contacts, are drilled in the circuit board.

After Stage 2C, the process can be continued for example as follows:

15 **Stage 2D:**

In stage 2D, conductive material is grown on top of the circuit board and in the through holes 23, in the same way as in stage 1C.

20 **Stage 2E:**

In stage 2E, the conductive layer on the surface of the circuit board is patterned in the same way as in stage 1D.

25 **Stage 2F:**

30 In stage 2F, a photolithographic polymer is spread on the surfaces of the circuit board and the desired pattern is formed in the polymer in the same way as in stages 1N and 1O. The exposed polymer film is developed, but the polymer film pattern remaining on the circuit board is not removed.

Stage 2G:

In stage 2G, the connection areas of the polymer film pattern formed in the previous stage are metallized in the same way as in stage 1P.

5

On the basis of the example of Figure 2, it is obvious that the method can also be used to manufacture many kinds of three-dimensional circuit structures. For example, the method can be used in such a way that several memory circuits are placed on top of each other, thus forming a packet containing several memory circuits, in which the memory
10 circuits are connected to each other to form an operational totality. Such a packet can be termed a three-dimensional multichip module. The chips in such modules can be selected freely and the contacts between the chips can be easily made according to the selected circuits.

15 The invention also permits electromagnetic protection to be made around the component embedded in the base. This is because the method of Figure 1 can be modified in such a way that the holes 6 depicted in stage 1E can be made in connection with the making of the holes 3 carried out in stage 1B. In that case, the conductive layer 4 to be made in stage 1C will also cover the side walls of the holes 6 made for the components. Figure
20 4A shows a cross-section of the base structure as it is after stage 1F in the process modified in the aforesaid manner.

After the intermediate stage shown in Figure 4A, the process can be continued by assembling the microcircuits in a similar way to stage 1G, the polymer film being
25 hardened as in stage 1H, and the microcircuits being attached similarly to stage 1I. After this, polymer and metal foils can be formed on the first surface of the circuit board similarly to stage 1J. Figure 4B shows an example cross-section of the base structure after these process stages.

30 After the intermediate stage shown in Figure 4B, the process can be continued by making holes, similar to those of stage 1K, in the polymer film, for making contacts. After this, a conductive layer is made in the holes and on the surfaces of the board

similarly to stage 1L. Figure 4C shows an example cross-section of the base structure after these process stages. For reasons of clarity, the conductive layer made similarly to stage 1L in the holes and on the board surfaces is highlighted in black.

- 5 After the intermediate stage shown in Figure 4C, the process can be continued by patterning a conductive layer on the surfaces of the board as in stage 1M and by coating the surfaces of the board as in stage 1N. After these stages, the microcircuits are surrounded by a nearly unbroken metal foil, which forms an effective protection against interference caused by electromagnetic interaction. This construction is shown in Figure 10 4D. After the intermediate stage shown in Figure 4D, stages corresponding to stages 1O and 1P are carried out, in which a protective foil and connections are made on the surface of the circuit board.

- In Figure 4D, the cross-sections of the metal layers protecting the microcircuits are 15 highlighted in black. In addition, the background of the microcircuits is highlighted with cross-hatching. The cross-hatching is intended to be a reminder that all the sides of a hole made for a microcircuit are covered by a metal foil. Thus the microcircuit is surrounded laterally with an unbroken metal foil. In addition to this, a metal plate can be designed above the microcircuit, which is made in connection with the making of the 20 circuit board's conductive pattern. Similarly, a metal foil that is as complete as possible is made below the microcircuit. The making of contacts below the microcircuit means that small gaps must be made in the metal foil, as shown in Figure 4D, for instance. These gaps can, however, be made so narrow laterally, or, correspondingly, so thin vertically, that they do not weaken the protective effect obtained against electromagnetic 25 interference.

- When examining the example of Figure 4D, it must also be take into account that the final structure also contains parts extending at right angles to the plane shown in the figure. Such a structure extending at right angles is shown by the conductor connected to 30 the contact bump on the left-hand side of the left-hand microcircuit of Figure 4D, which runs towards the viewer from between the metal foil surrounding the microcircuit laterally and the conductive layers below the microcircuit.

The solution shown by Figure 4D thus provides the microcircuit with excellent protection against electromagnetic interference. As the protection is made immediately around the microcircuit, the construction also protects against mutual interference
5 arising between the components contained in the circuit board. Most of the electromagnetic protective structure can also be earthed, as the metal foil surrounding the microcircuits laterally can be connected electrically to the metal plate above the circuit. The connections of the circuit board, can, in turn, be designed in such a way that the metal plate is earthed through the conductive structure of the circuit board.

10

Claims:

1. A method for embedding at least one component in a base, which component has contact areas on its first surface, the method comprising
 - 5 - taking a baseboard of the base, the baseboard having a first surface and a second surface,
 - making conductive patterns on the baseboard and at least one hole for the at least one component, in such a way that each hole extends through the baseboard between the first surface and the second surface,
 - 10 - spreading an insulating polymer layer on the second surface of the baseboard, in such a way that the insulating polymer layer covers the at least one hole made for the component,
 - placing the at least one component in the at least one hole, in such a way that the component is aligned in relation to the conductive patterns made on the
 - 15 baseboard and the first surface of the component presses against the insulating polymer layer, and
 - hardening the insulating polymer layer.
2. A method according to Claim 1, in which the first surface of the component is pressed
20 into the unhardened insulating polymer layer.
3. A method according to Claim 1, in which the first surface of the component is pressed into the partly hardened insulating polymer layer.
- 25 4. A method according to any of Claims 1 - 3, in which the insulating polymer layer is manufactured by placing an RCC foil on the second surface of the baseboard.
5. A method according to any of Claims 1 - 3, in which the insulating polymer layer is manufactured by spreading a pre-preg epoxy film on the second surface of the
30 baseboard.

6. A method according to any of Claims 1 - 5, in which insulating material is grown on the side walls of the hole made for a component, in order to create interference protection around the component.
- 5 7. A method according to any of Claims 1 - 6, in which the contact areas of the component have contact protrusions connected to them, and the component is placed in the hole in such a way that the contact protrusions push inside the insulating polymer layer.
- 10 8. A method according to any of Claims 1 - 6, in which the contact areas of the component have contact protrusions connected to them, the height of the contact protrusions being at least as great as the thickness of the insulating polymer layer, and the component is placed in the hole in such a way that the contact protrusions penetrate through the insulating polymer layer.
- 15 9. A method according to any of Claims 1 - 7, in which
- contact openings for the component are made in the hardened insulating polymer layer, and
 - conductors for forming electrical contacts with the component are made in the
- 20 contact openings and on top of the insulating polymer layer.
10. A method according to any of Claims 1 - 9, in which conductive patterns are made on at least the second surface (1b) of the baseboard, and in which the insulating polymer layer to be spread on the second surface (1b) of the baseboard is spread in such a way
- 25 that it covers the conductive patterns made on the second surface (1b).
11. A method according to any of Claims 1 - 10, in which the first surface of the component is pushed into the insulating polymer layer, which is in contact with the conductive patterns, which are formed from the conductive layer.
- 30 12. A method according to any of Claims 1 - 11, in which at least one set of conductive patterns are located between the insulating polymer layer, against which the first surface

of the component is pushed, and the baseboard of the circuit board.

13. A method according to any of Claims 1 - 12, in which the baseboard is of an insulating material.

5

14. A method according to any of Claims 1 - 13, in which the component is secured in place by filling a hole, made in the baseboard, with a filler material.

15. A method according to any of Claims 1 - 14, in which the component is a microcircuit and an electrical contact is formed with the microcircuit from the direction of the first surface of the baseboard, after the microcircuit has been placed in the hole made in the baseboard.

16. A method according to any of Claims 1 - 15, in which an electrical contact is formed with the component by growing conductive material in the contact areas of the component, or on top of its contact protrusions.

17. A method according to any of Claims 1 - 16, in which the electrical contact with the microcircuit is formed without solder using a circuit-board manufacturing technology.

20

18. A method according to any of Claims 1 - 17, in which more than one component is embedded in the base and in which a separate hole is made in the baseboard for each component to be embedded in the base and each component to be embedded in the base is located in its own hole.

25

19. A method according to any of Claims 1 - 18, in which a multi-layer structure is manufactured, in which there are at least four conductive layers on top of each other.

20. A method according to any of Claims 1 - 19, in which a first base, into which at least two microcircuits are embedded, and at least one second base, in which at least two microcircuits are embedded, are manufactured, and the bases are assembled and secured on top of each other in such a way that the bases are aligned in relation to each other.

30

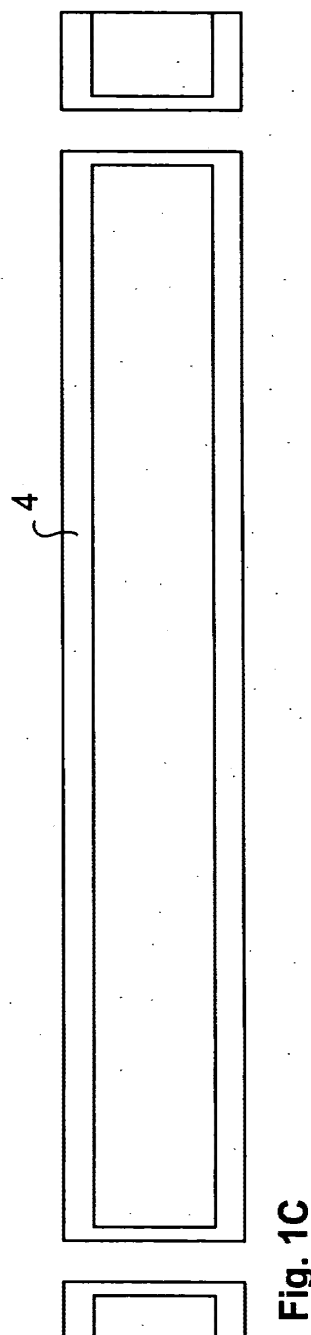
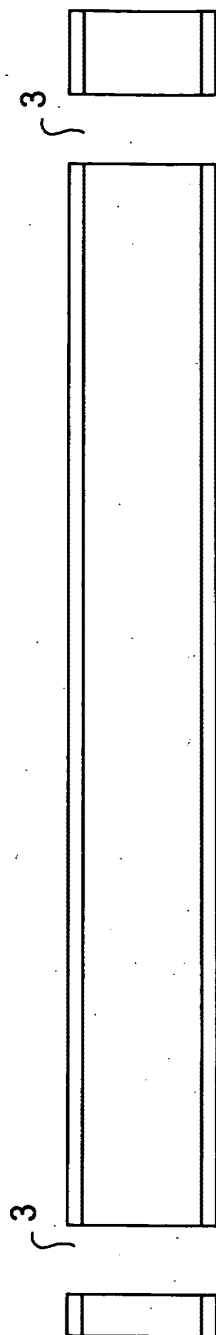
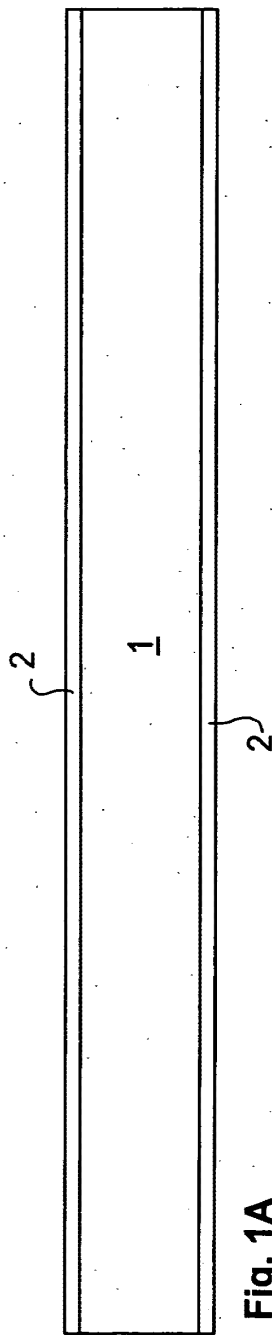
21. A method according to any of Claims 1 - 19, in which
- a first and a second base and an intermediate layer are manufactured,
 - the second base is placed above the first base and the second base is aligned in
5 relation to the first base,
 - the intermediate layer is placed between the first and the second bases, and
 - the first and second bases are laminated to each other with the aid of the intermediate layer.
- 10 22. A method according to Claim 21, in which
- at least one third base and an intermediate layer for every third base are manufactured,
 - each third base is placed in turn above the first and second bases and each third
base is aligned in relation to one of the lower bases,
 - 15 - an intermediate layer is placed beneath each third base, and
 - the first, second, and each third base are laminated to each other with the aid of the intermediate layers.
- 20 23. A method according to any of Claims 20 - 22, in which holes for feed-throughs are drilled through the bases secured on top of each other and conductors are made in the drilled holes for connecting the electronic circuits of each base to each other to form an operational totality.
24. A method according to any of Claims 1 - 23, in which the temperature of a
25 baseboard, component, or conductive layer connected directly to a component, is, during the process, less than 200°C and preferably in the range 20 - 85°C.
25. An electronic module, which is manufactured using a method according to any of
Claims 1 - 24.

30

(57) Abstract:

This publication discloses a method, in which the semiconductor components forming part of an electronic circuit, or at least some of them, are embedded in a base, such as a circuit board, during the manufacture of the base, when part of the base structure is, as it were, manufactured around the semiconductor components. According to the invention, through-holes for the semiconductor components are made in the base, in such a way that the holes extend between the first and second surface of the base. After the making of the holes, a polymer film is spread over the second surface of the base structure, in such a way that the polymer film also covers the through-holes made for the semiconductor components from the side of the second surface of the base structure. Before the hardening, or after the partial hardening of the polymer film, the semiconductor components are placed in the holes made in the base, from the direction of the first surface of the base. The semiconductor components are pressed against the polymer film in such a way that they adhere to the polymer film. After this, the final hardening of the polymer film is carried out.

(Figure 2C)



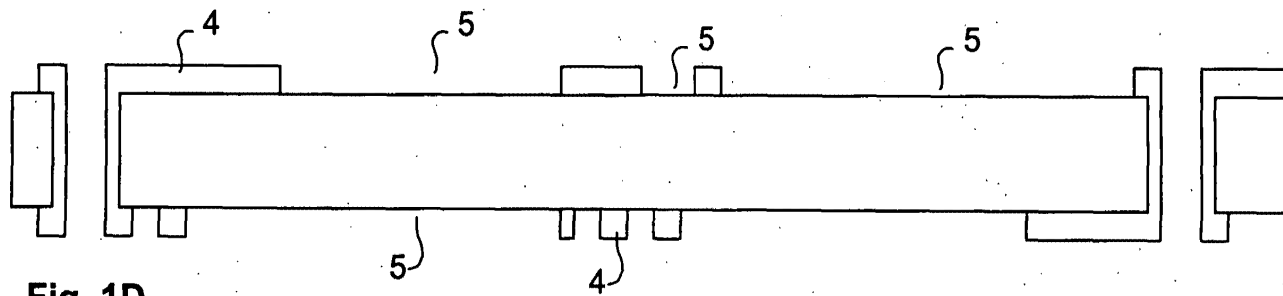


Fig. 1D

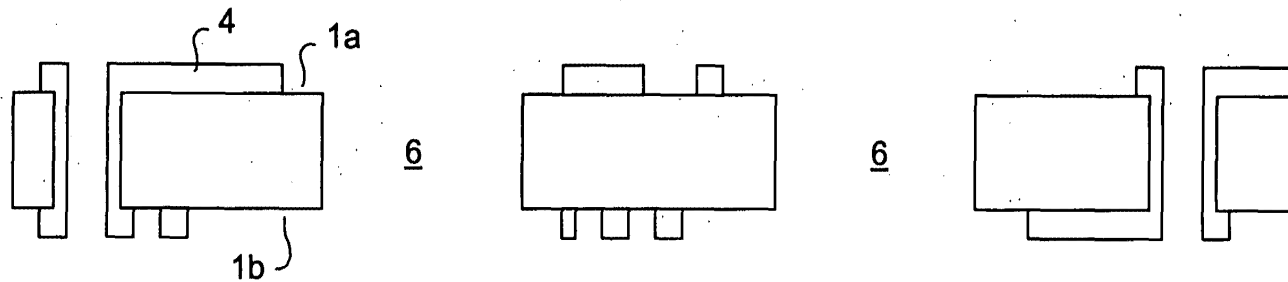


Fig. 1E

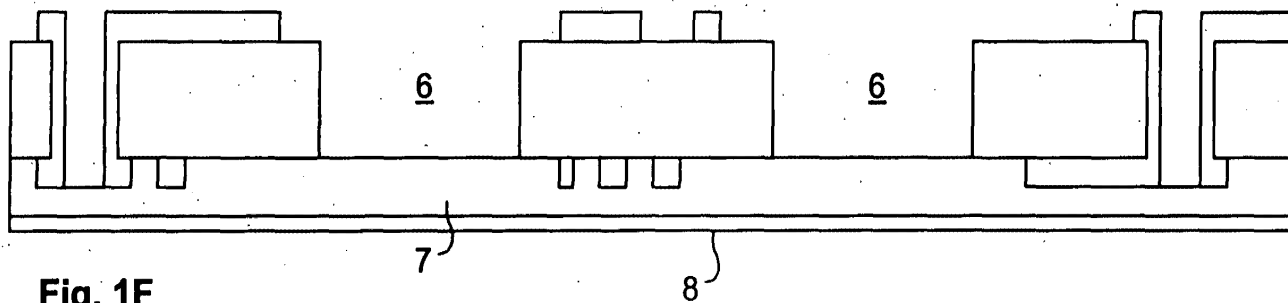


Fig. 1F

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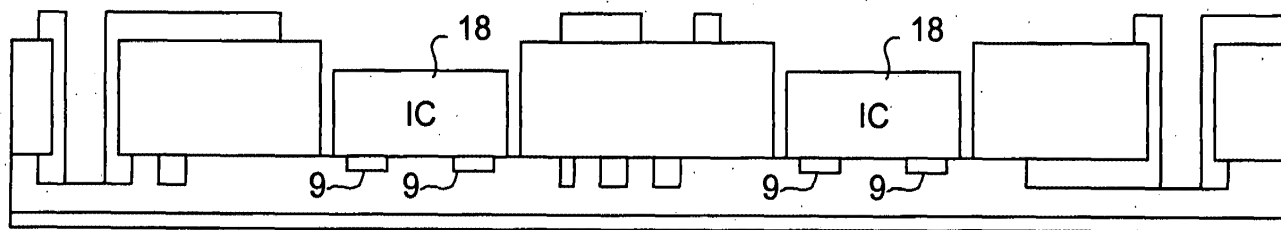


Fig. 1G

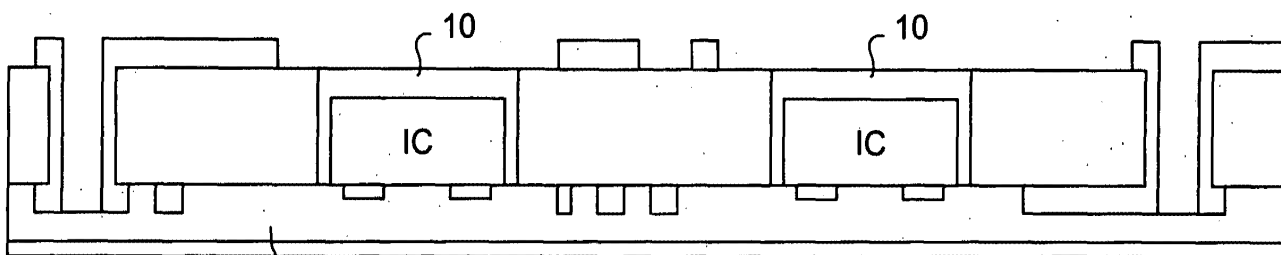


Fig. 1I

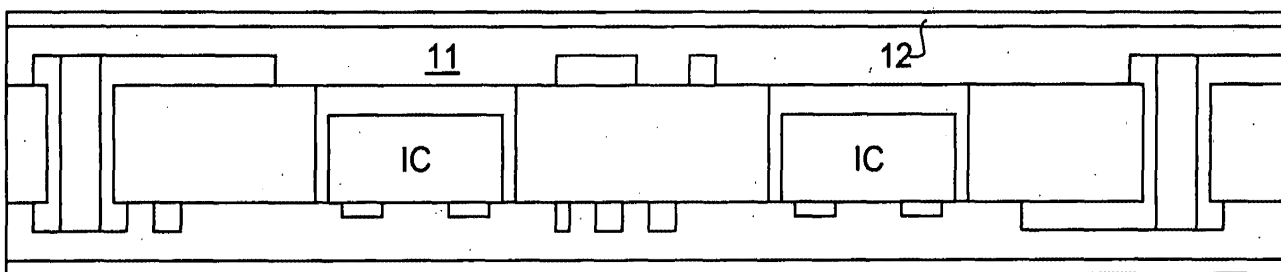


Fig. 1J

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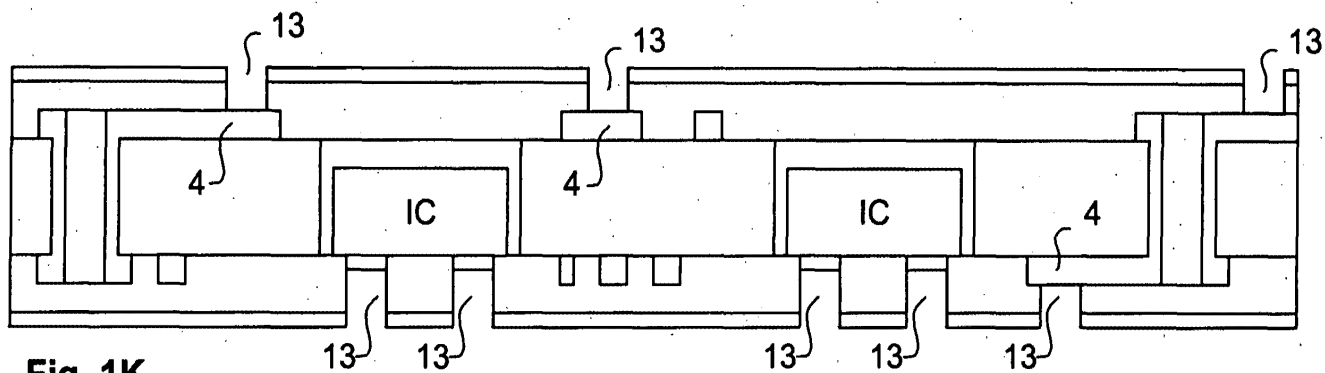


Fig. 1K

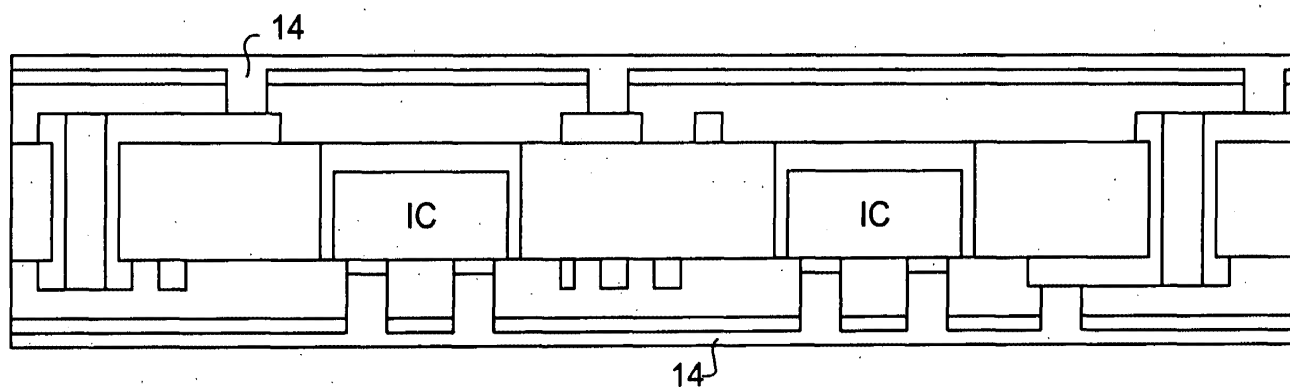
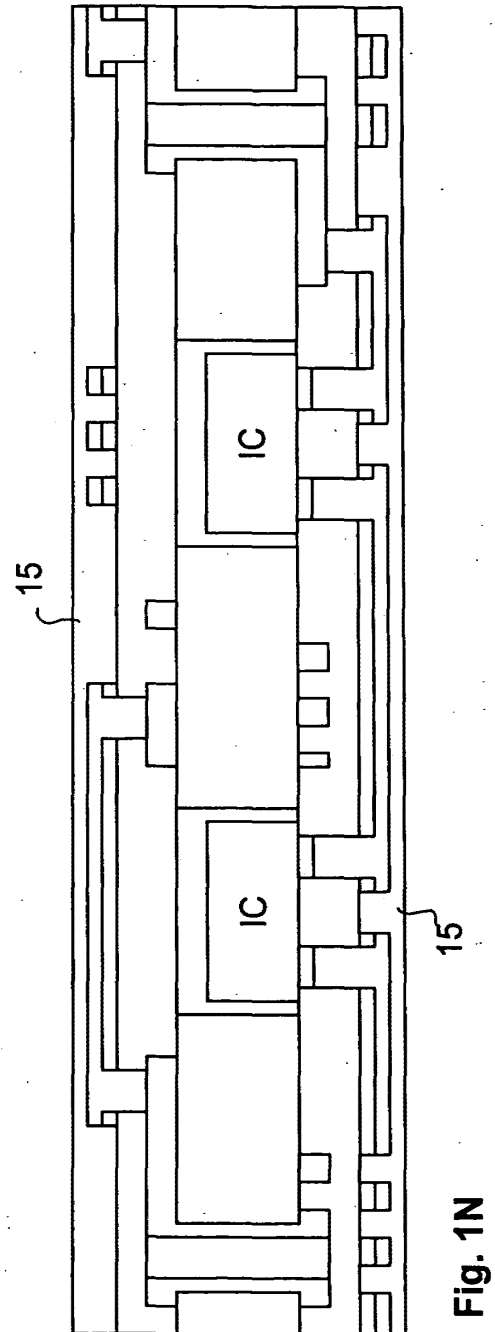
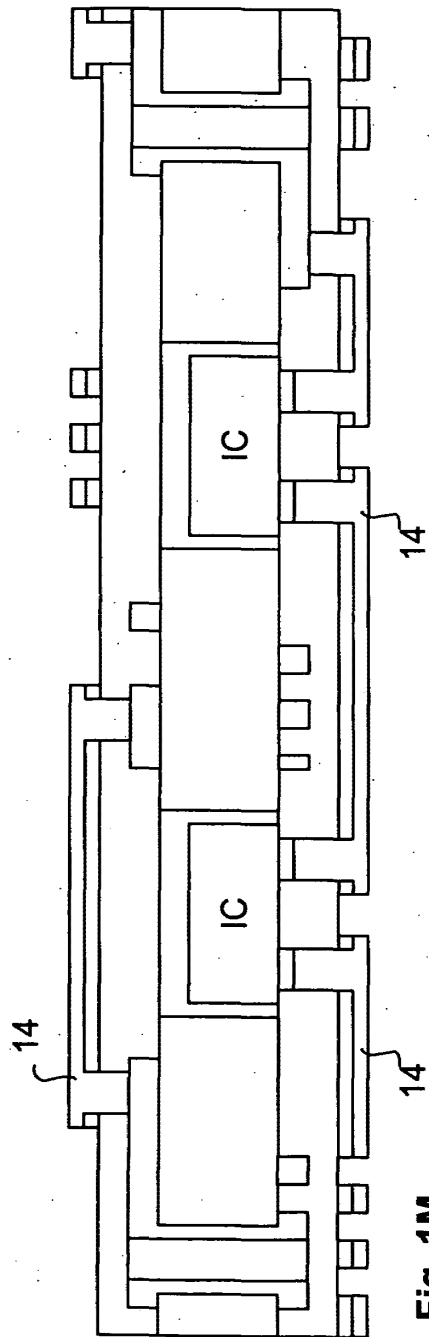


Fig. 1L

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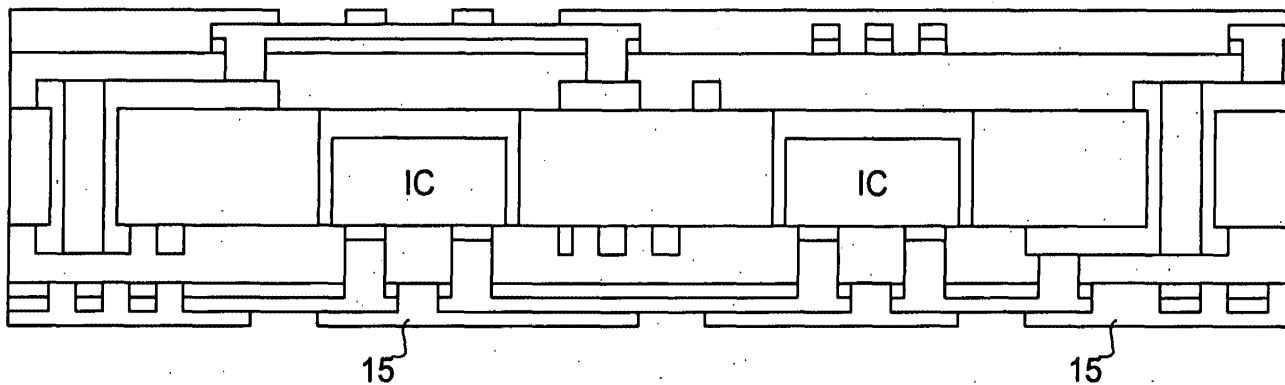


Fig. 10

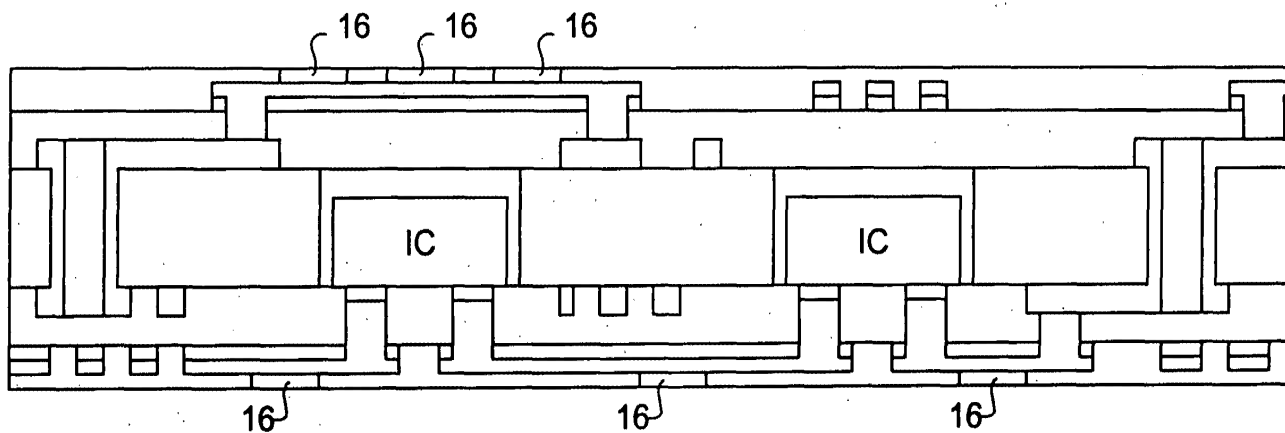


Fig. 1P

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10/502336

7/12

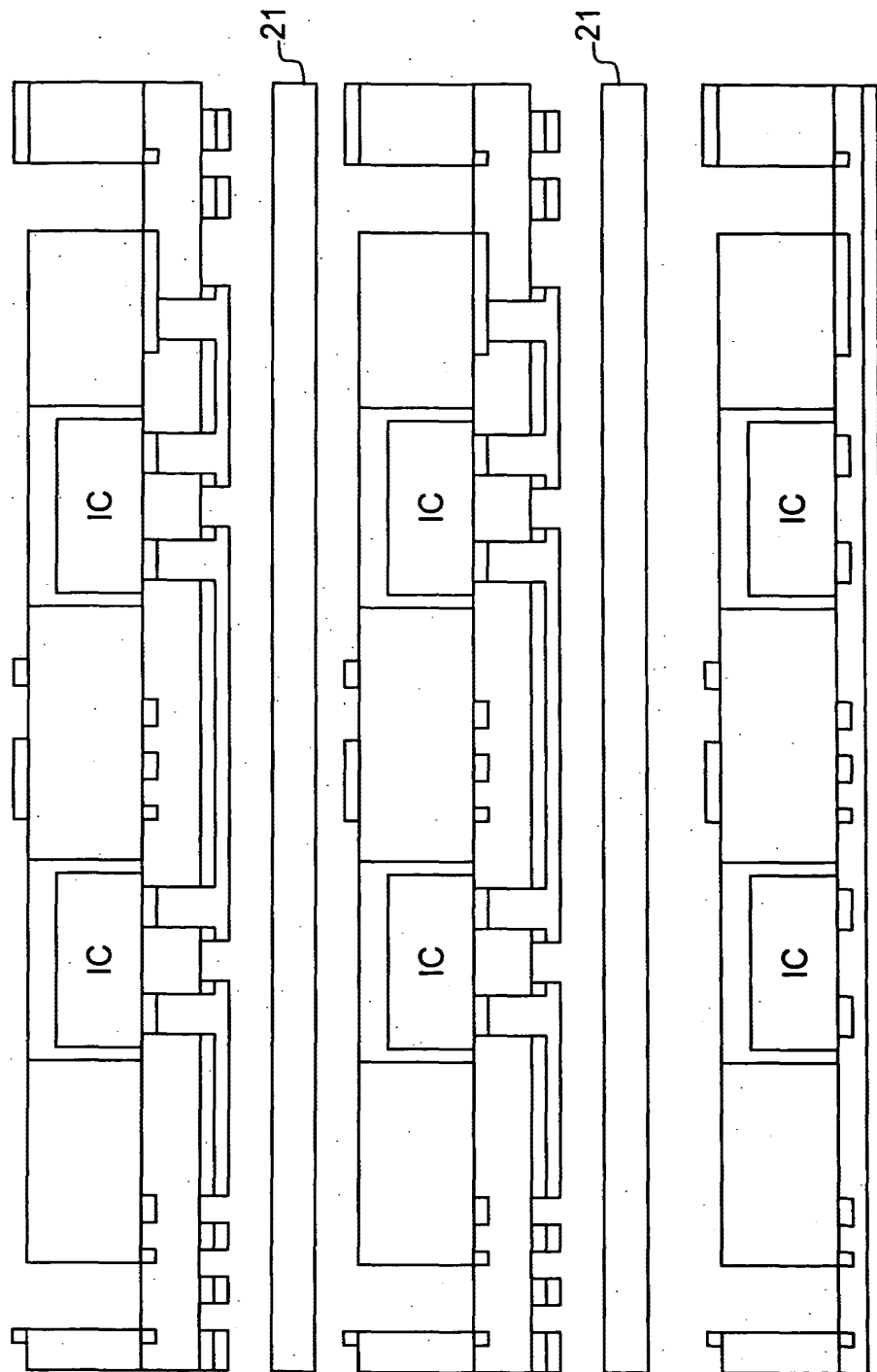


Fig. 2A

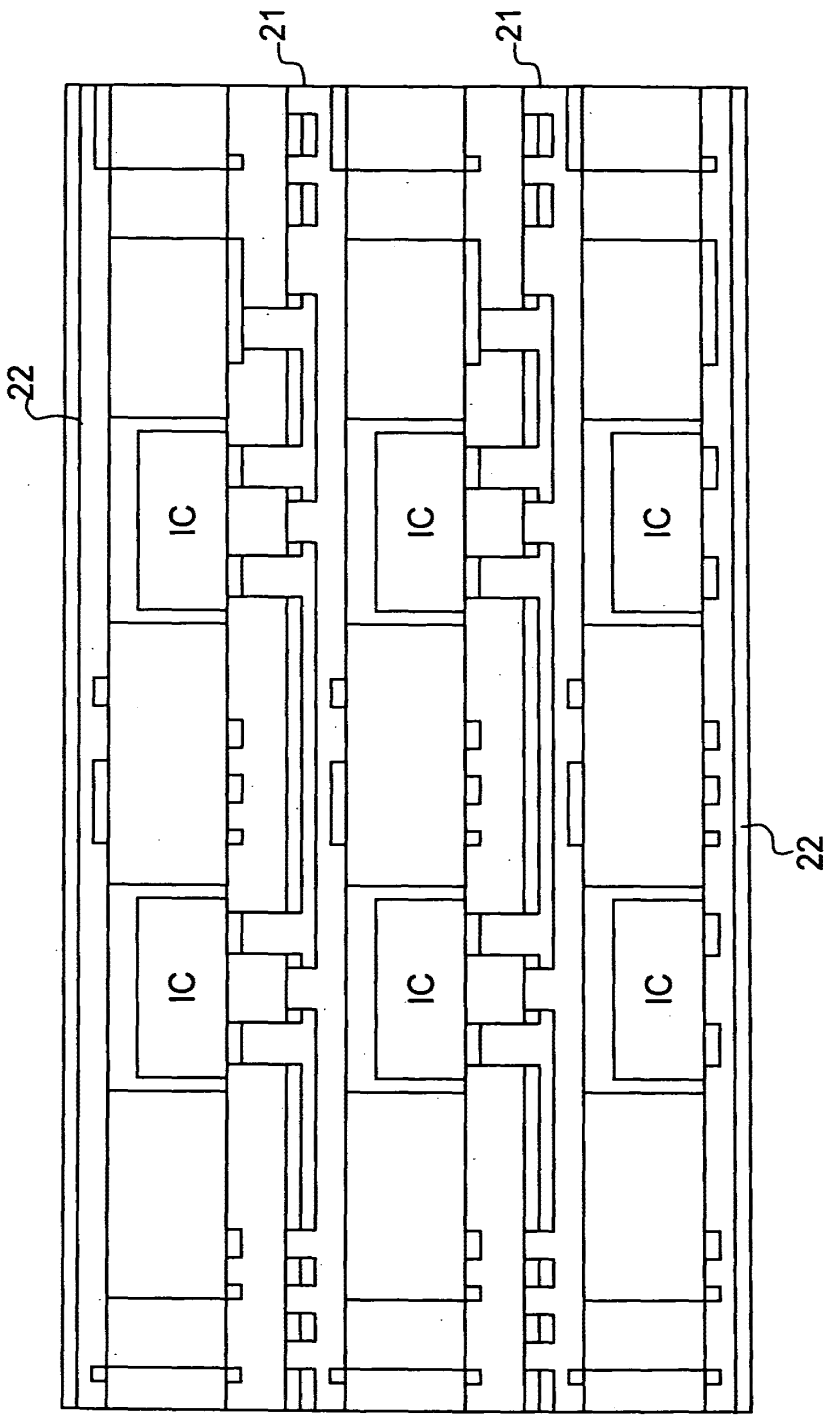


Fig. 2B

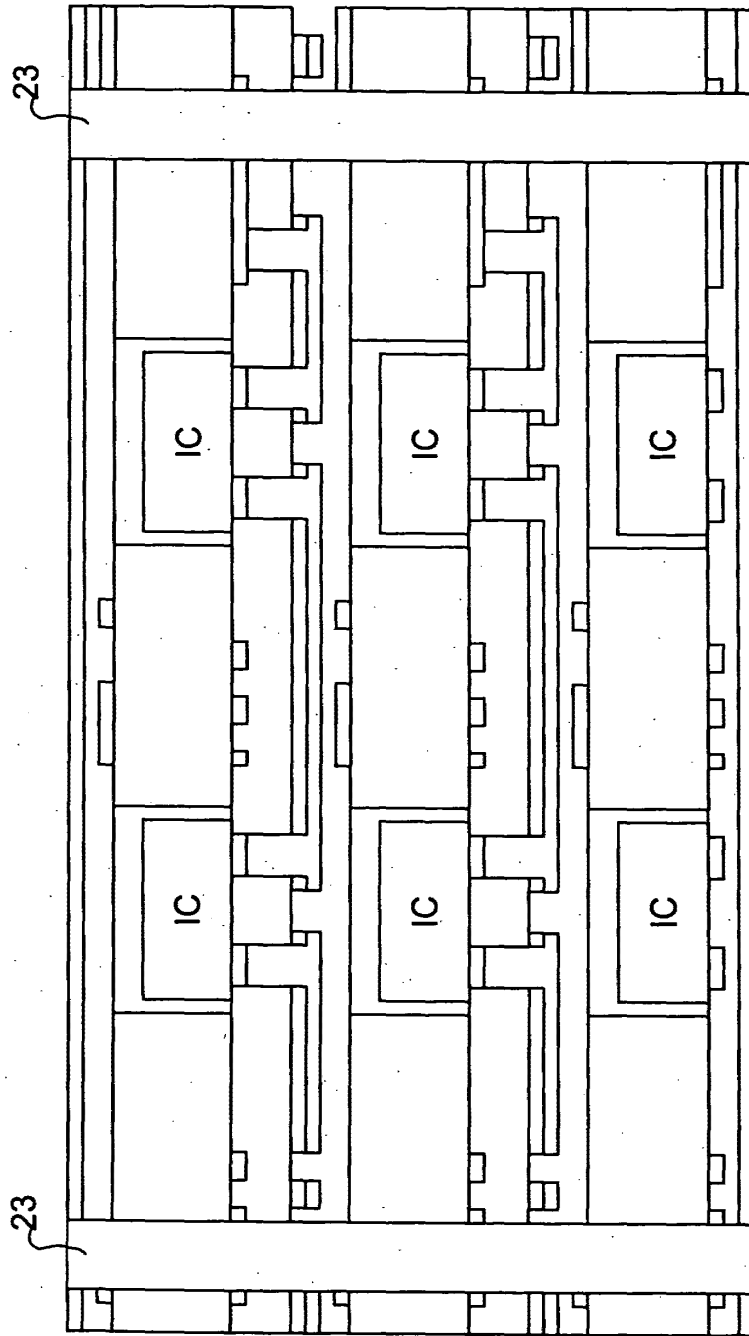


Fig. 2C

10/12

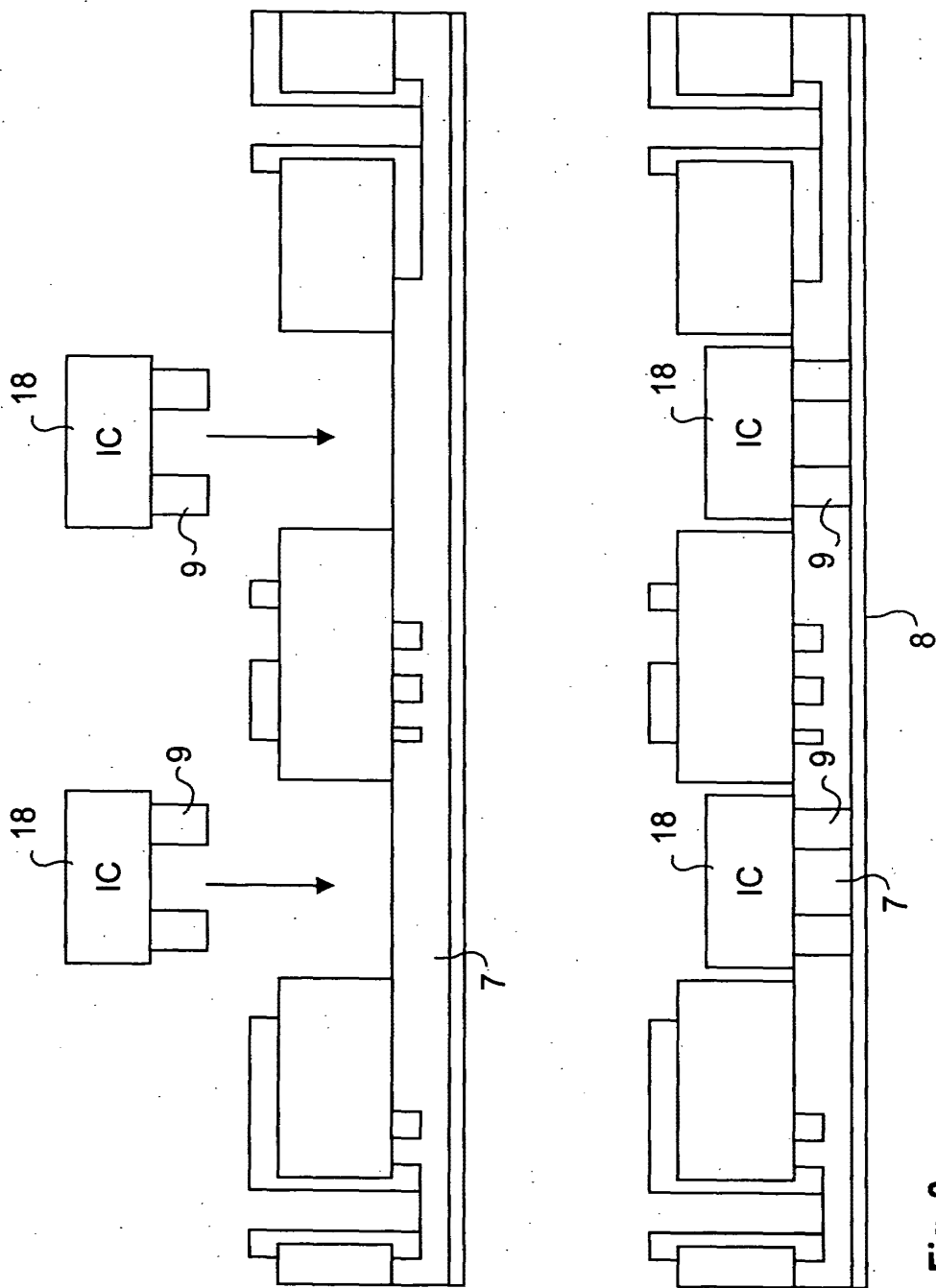


Fig. 3

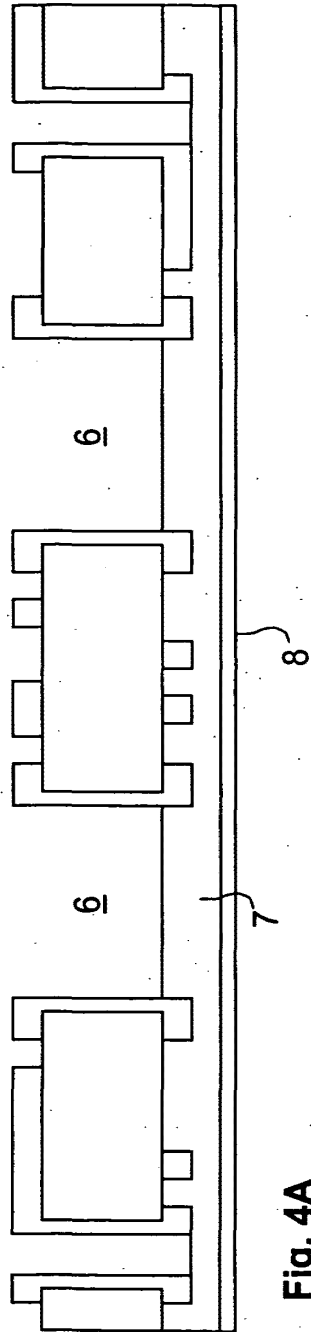


Fig. 4A

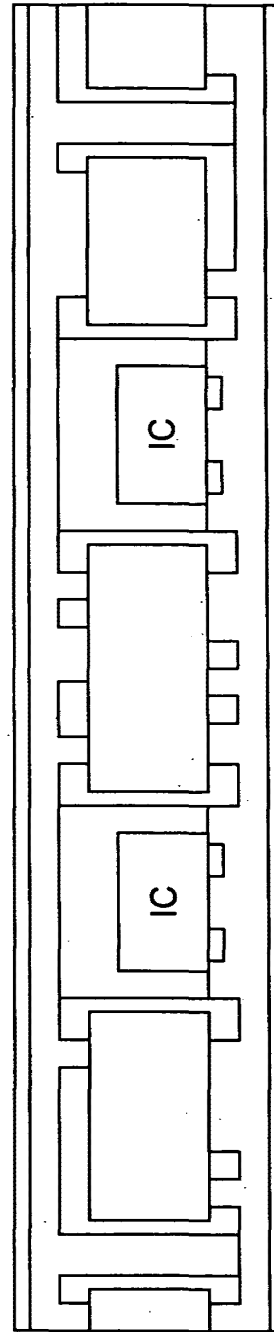


Fig. 4B

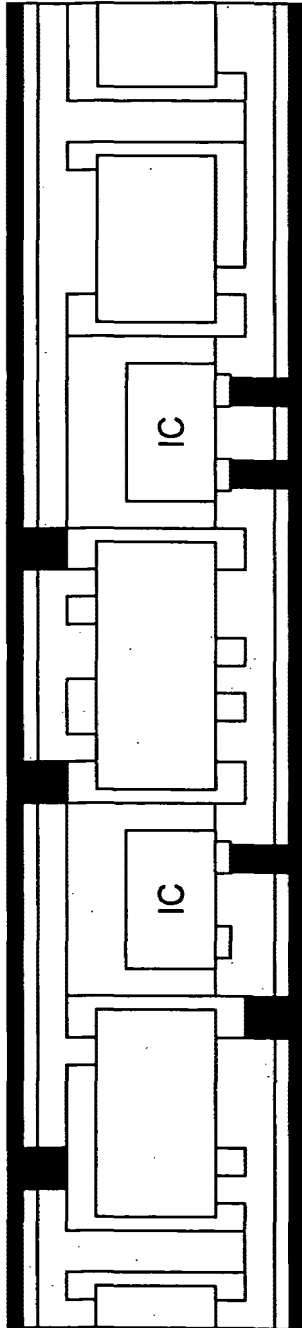


Fig. 4C

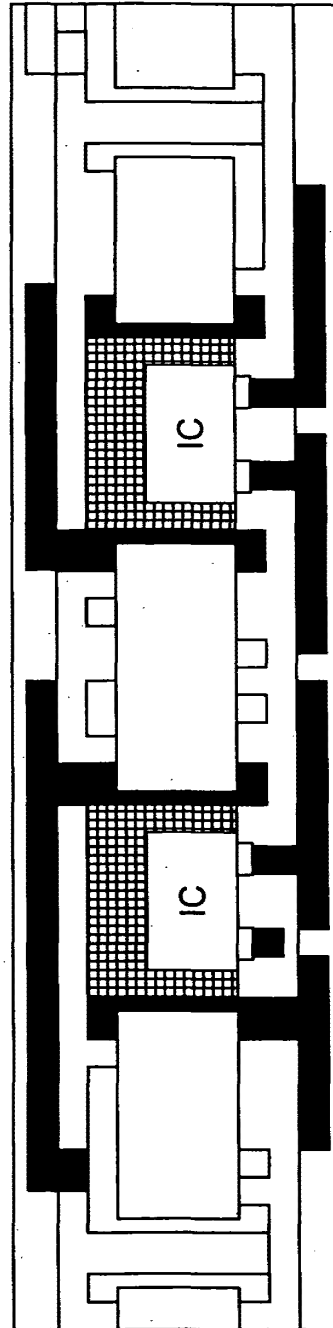
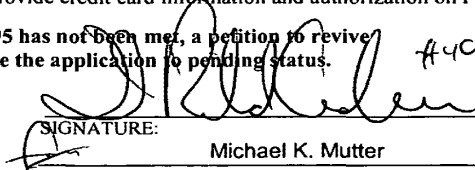


Fig. 4D

FORM PTO 1390 (REV 10-2003)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 0365-0601PUS1
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371			U.S. APPLICATION NO. (If known, see 37 CFR 1.5) 10/502336
INTERNATIONAL APPLICATION NO. PCT/FI03/00065	INTERNATIONAL FILING DATE 28 January 2003	PRIORITY DATE CLAIMED 31 January 2002	
TITLE OF INVENTION METHOD FOR EMBEDDING A COMPONENT IN A BASE			
APPLICANT(S) FOR DO/EO/US Risto TUOMINEN			
Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:			
1. ☒ This is a FIRST submission of items concerning a filing under 35 U.S.C. 371. 2. ☐ This is a SECOND or SUBSEQUENT submission of items concerning a filing 35 U.S.C. 371. 3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371 (f)). The submission must include items (5), (6), (9) and (21) indicated below. 4. ☒ The US has been elected (Article 31). 5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c)(2)) a. ☐ is attached hereto (required only if not communicated by the International Bureau). b. ☒ has been communicated by the International Bureau. c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US). 6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371 (c)(2)). a. ☒ is attached hereto. b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4). 7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3)) a. ☐ are attached hereto (required only if not communicated by the International Bureau). b. ☐ have been communicated by the International Bureau. c. ☐ have not been made; however, the time limit for making such amendments has NOT expired. d. ☒ have not been made and will not be made. 8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)). 9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)). 10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).			
Items 11 to 20 below concern document(s) or information included:			
11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98. 12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included. 13. ☐ A preliminary amendment. 14. ☒ An Application Data Sheet under 37 CFR 1.76. 15. ☐ A substitute specification. 16. ☐ A power of attorney and/or change of address letter. 17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 37 CFR 1.821 - 1.825. 18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4). 19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4). 20. ☒ Other items or information: Drawings - Twelve (12) Sheets			

JT12 Rec'd PCT/PTO 23 JUL 2004

U.S. APPLICATION NO. (if known, see 37 CFR 1.41) 107502336		INTERNATIONAL APPLICATION NO. PCT/FI03/00065		ATTORNEY'S DOCKET NUMBER 0365-0601PUS1	
21. ☒ The following fees are submitted:				CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):					
☒ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO \$1080.00					
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO \$920.00					
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO \$770.00					
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) \$730.00					
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) \$100.00					
ENTER APPROPRIATE BASIC FEE AMOUNT =					
Surcharge of \$130.00 for furnishing the oath or declaration later than 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).				\$ 1,080.00	
				\$ 130.00	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	29-20 =	9	x 18.00	\$ 162.00	
Independent claims	1-3 =		x	\$ 0.00	
MULTIPLE DEPENDENT CLAIM(s) (if applicable)			+ 290.00	\$ 290.00	
TOTAL OF ABOVE CALCULATIONS =				\$ 1,662.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.					
SUBTOTAL =				\$ 1,662.00	
Processing fee of \$130.00 for furnishing the English translation later than 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).					
TOTAL NATIONAL FEE =				\$ 1,662.00	
Fee for recording the endorsed assignment (37 CFR 1.21 (h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property				+ \$	
TOTAL FEES ENCLOSED =				\$ 1,662.00	
				Amount to be refunded: \$	
				charged: \$	
a. ☒ A check in the amount of \$ 1,662.00 to cover the above fees is enclosed.					
b. ☐ Please charge my Deposit Account No. _____ in the amount of \$ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.					
c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 02-2448. A duplicate copy of this sheet is enclosed.					
d. ☐ Fees are to be charged to a credit card. WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.					
NOTE: Where an appropriate time limit under 37 CFR 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.					
SEND ALL CORRESPONDENCE TO:					
CUSTOMER NUMBER: 02292 July 23, 2004 /clb				SIGNATURE:  NAME: Michael K. Mutter	
				29,680	
REGISTRATION NUMBER					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov



Bib Data Sheet

CONFIRMATION NO. 5376

SERIAL NUMBER 10/502,336	FILING OR 371(c) DATE 09/23/2004 RULE	CLASS 438	GROUP ART UNIT 2812	ATTORNEY DOCKET NO. 0365-0601PUS1	
APPLICANTS Risto Tuominen, Helsinki, FINLAND; ** CONTINUING DATA ***** This application is a 371 of PCT/FI03/00065 01/28/2003 ** FOREIGN APPLICATIONS ***** FINLAND 20020191 01/31/2002					
Foreign Priority claimed ☐ yes ☐ no 35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance Verified and Acknowledged _____ Examiner's Signature _____ Initials _____		STATE OR COUNTRY FINLAND	SHEETS DRAWING 12	TOTAL CLAIMS 24	INDEPENDENT CLAIMS 1
ADDRESS 02292					
TITLE Method for embedding a component in a base					
FILING FEE RECEIVED 1662	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

#3

BIRCH, STEWART, KOLASCH & BIRCH, LLP

P.O. Box 747 • Falls Church, Virginia 22040-0747

Telephone: (703) 205-8000 • Facsimile: (703) 205-8050

ATTORNEY DOCKET NO.

0365-0601PUS1

PLEASE NOTE:
YOU MUST
COMPLETE THE
FOLLOWING:

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT AND DESIGN APPLICATIONS

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Insert Title: Method for embedding a component in a base

the specifications of which is attached hereto. If not attached hereto, the application is identified by the attorney docket number as set forth above and/or the following:

Fill in Appropriate
Information -
For Use
Without
Specification
Attached:

the specification was filed on _____ as
United States Application Number _____;
and amended on _____ (if applicable); and/or
the specification was filed on January 28, 2003 as PCT
International Application Number PCT/FI03/00065; and was
amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Insert Priority
Information:
(if appropriate)

Prior Foreign Application(s)

(Number)	(Country)	(Month / Day / Year Filed)	Priority Claimed
<u>20020191</u>	<u>Finland</u>	<u>01/31/2002</u>	☒ Yes ☐ No
_____	_____	_____	☐ Yes ☐ No
_____	_____	_____	☐ Yes ☐ No
_____	_____	_____	☐ Yes ☐ No

Insert Provisional
Application(s):
(if any)

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
_____	_____
_____	_____

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed more than 12 months (6 months for designs) Prior to the Filing Date of this Application:

Insert Requested
Information:
(if appropriate)

Country	Application Number	Date of Filing (Month / Day / Year)
_____	_____	_____
_____	_____	_____

I hereby claim the benefit under Title 35, United States Code, §120 of any United States and/or PCT application(s), including for continuation-in-part application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States and/or PCT application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to the patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Insert Prior U.S.
Application(s):
(if any)

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
_____	_____	_____
_____	_____	_____

I hereby appoint the practitioners at **CUSTOMER NO. 02292** as my attorneys or agents to prosecute this application and/or an international application based on this application and to transact all business in the Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the practitioners, unless the inventor(s) or assignee provides said practitioners with a written notice to the contrary:

Send Correspondence to:

BIRCH, STEWART, KOLASCH & BIRCH, LLP or **CUSTOMER NO. 02292**
P.O. Box 747 • Falls Church, Virginia 22040-0747
Telephone: (703) 205-8000 • Facsimile: (703) 205-8050

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

**PLEASE NOTE:
YOU MUST
COMPLETE THE
FOLLOWING:**

Full Name of First or
Sole Inventor:
Insert Name of Inventor
Insert Date This
Document is Signed

Insert Residence
Insert Citizenship

Insert Mailing
Address

Full Name of Second
Inventor, if any:

see above

Full Name of Third
Inventor, if any

see above

Full Name of Fourth
Inventor, if any

see above

Full Name of Fifth
Inventor, if any

see above

GIVEN NAME		FAMILY NAME		INVENTOR'S SIGNATURE		DATE*	
Risto		Tuominen		<i>[Signature]</i>		July 9, 2004	
Residence (City, State & Country)						CITIZENSHIP	
Helsinki, Finland						Finnish	
MAILING ADDRESS (Complete Street Address including City, State & Country)							
Väinölänkatu 17 B 18, FI-00610 Helsinki, Finland							
GIVEN NAME		FAMILY NAME		INVENTOR'S SIGNATURE		DATE*	
Residence (City, State & Country)						CITIZENSHIP	
MAILING ADDRESS (Complete Street Address including City, State & Country)							
GIVEN NAME		FAMILY NAME		INVENTOR'S SIGNATURE		DATE*	
Residence (City, State & Country)						CITIZENSHIP	
MAILING ADDRESS (Complete Street Address including City, State & Country)							
GIVEN NAME		FAMILY NAME		INVENTOR'S SIGNATURE		DATE*	
Residence (City, State & Country)						CITIZENSHIP	
MAILING ADDRESS (Complete Street Address including City, State & Country)							

* DATE OF SIGNATURE



DT10 Rec'd PCT/JP 23 SEP 2004
10/02336 #3

MS PCT
PATENT
0365-0601PUS1

IN THE U.S. PATENT AND TRADEMARK OFFICE

APPLICANT: TUOMINEN, Risto
INTERNATIONAL APPL. NO.: PCT/FI03/00065
APPL. NO.: 10/502,336 ✓
CONF.: UNASSIGNED
FILED: July 23, 2004
FOR: METHOD FOR EMBEDDING A
COMPONENT IN A BASE

LETTER SUBMITTING ADDITIONAL DOCUMENTS FOR
ENTERING NATIONAL PHASE FOR A PCT APPLICATION

MS PCT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

September 23, 2004

Sir:

Under the provisions of 37 C.F.R. § 1.494 or 37 C.F.R. § 1.495, attached hereto are the following additional items necessary for entering the national phase in connection with the above-identified PCT international application.

DOCUMENTATION

- ☒ Executed Declaration and Power of Attorney
☒ Original ☐ Photocopy
- ☐ The specification attached to the executed Declaration and Power of Attorney is a true copy of the specification that was filed in the U.S. Patent and Trademark Office on July 23, 2004, including any amendments thereto (if applicable) filed on even date therewith.

- ☒ The undersigned hereby declares that "Attorney Docket No. 0365-0601PUS1" on page 1 of the attached inventors' Declaration corresponds to Appl. No. 10/502,336 filed July 23, 2004 entitled "METHOD FOR EMBEDDING A COMPONENT IN A BASE."
- ☐ Attached is a copy of the Notification of Missing Requirements (371 Formalities Letter).
- ☐ Attached is an English language translation of the above-identified application that was filed in a foreign language, which should be used as the copy for examination purposes.
- ☐ See the attached Translator's Verification; or
- ☐ The undersigned states that the English translation attached hereto is a true and correct translation of the application as originally filed in a foreign language.
- ☐ Attached are _____ (____) sheet(s) of formal drawings. Please substitute these corrected drawings for the corresponding _____ (____) sheets of drawings on file in the above-identified application.
- ☐ Attached are substitute claims commencing on a separate sheet in accordance with 37 C.F.R. § 1.75(h).
- ☐ Attached is a substitute abstract commencing on a separate sheet in accordance with 37 C.F.R. § 1.72(b).
- ☐ Attached is a substitute specification that complies with 37 C.F.R. § 1.52. The substitute specification does not contain new matter.
- ☐ Applicant claims small entity status under 37 C.F.R. § 1.27.
- ☒ Submitted concurrently herewith **under separate cover** for recording is an Assignment.
- ☐ _____

FEES

- ☒ The Government Filing Surcharge for late filing of oath and/or declaration in the amount of \$130.00 in accordance with 37 C.F.R. §§ 1.494 and 1.492 was previously paid for concurrently with the filing of the application on July 23, 2004.
- ☐ The Government Filing Surcharge for late filing of the English translation in the amount of \$0.00 in accordance with 37 C.F.R. § 1.492 was previously paid for concurrently with the filing of the application on .
- ☐ Additional claim fee(s) under 37 C.F.R. § 1.16(b)-(d) in the amount of \$0.00; which have been calculated as follows:

	CURRENT NUMBER OF CLAIMS		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA	RATES	ADDITIONAL FEE
TOTAL		-	20	=	0	\$18 (large)	\$0.00
INDEPENDENT		-	3	=	0	\$86 (large)	\$0.00
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM						\$290 (large)	\$0.00
TOTAL							\$0.00

- ☒ No extension fee is required because the undersigned has not yet received the Notification of Missing Requirements (Formalities Letter). However, if for some reason it is determined that an extension of time is necessary, applicant hereby respectfully petitions for an extension of time for the filing of the present paper in accordance with the provisions of 37 C.F.R. § 1.136 and 37 C.F.R. § 1.17.
- ☐ Applicant(s) hereby respectfully petitions for () month(s) extension of time for the filing of the present paper in accordance with the provisions of 37 C.F.R. § 1.136 and 37 C.F.R. § 1.17. The required fee of \$0.00 is attached hereto.

- ☐ Check(s) in the amount of \$0.00 to cover the above-mentioned fees is/are enclosed.
- ☐ Please charge Deposit Account No. 02-2448 in the amount of \$0.00. A triplicate copy of this transmittal form is enclosed.
- ☒ No fee(s) required.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fee required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By

Michael K. Mutter, #29,680

MKM/slb
0365-0601PUS1

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

Attachment(s)

(Rev. 04/16/2004)



DT07 Rec'd PCT/PTO 0 5 NOV 2004

PCT

PATENT
0365-0601PUS1

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant: Risto TUOMINEN Conf.: UNASSIGNED
Appl. No.: 10/502,336 Group: UNASSIGNED
Filed: July 23, 2004 Examiner: UNASSIGNED
For: METHOD FOR EMBEDDING A COMPONENT IN A
BASE

INFORMATION DISCLOSURE STATEMENT
(SUBMISSION AFTER FILING OF AN APPLICATION
BUT BEFORE FINAL REJECTION OR NOTICE OF ALLOWANCE
OR CONCURRENTLY WITH A RULE 1.114 RCE APPLICATION)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

November 4, 2004

Sir:

Pursuant to 37 C.F.R. §§ 1.97 and 1.98, applicant(s) hereby submit(s) an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on the PTO-1449(s), attached hereto.

II. COPIES (check at least one box)

- a. ☐ This application was filed before June 30, 2003. Accordingly, submitted herewith is a legible copy of (i) each U.S. and foreign patent; (ii) each publication or that portion which caused it to be listed; and (iii) all other information or that portion which caused it to be listed.
- b. ☒ This application was filed on or after June 30, 2003. Accordingly, copies of cited U.S. patents and patent application publications therefore are not included. Copies of foreign patent documents and non-patent literature are included.

- c. ☐ Some or all of the documents listed on the PTO-1449 are not enclosed because they were cited in the International Search Report and copies should already be in the PTO file. If copies are needed, please contact the undersigned.

III. CONCISE EXPLANATION OF THE RELEVANCE
(check at least one box)

- a. ☒ **DOCUMENTS IN THE ENGLISH LANGUAGE**

The patents, publications, or other information listed on the attached PTO 1449 are in the English language and therefore, do not require a statement of relevancy.

- b. ☐ **DOCUMENTS NOT IN THE ENGLISH LANGUAGE**

A concise explanation of the relevance of all patents, publications, or other information listed that is not in the English language is as follows:

- c. ☐ **ENGLISH LANGUAGE SEARCH REPORT**

An English language version of the search report or action that indicates the degree of relevance found by the foreign office is attached, thereby satisfying the requirement for a concise explanation. See MPEP 609(III)(A)(3).

- d. ☐ **OTHER**

The following additional information is provided for the Examiner's consideration.

FEEES

IV. ☒ THIS IDS IS BEING FILED UNDER 37 C.F.R. § 1.97(b):
(check one box)

- a. ☐ within three months of the filing date of a national application (37 C.F.R. § 1.97(b)(1)). No fee or statement is required. *(This section is not to be used with RCE's.)*
- b. ☐ within three months of the date of entry of the national stage as set forth in § 1.491 in an international application (37 C.F.R. § 1.97(b)(2)). No fee or statement is required.
- c. ☐ concurrently with the filing of a Request for Continued Examination under § 1.114 (37 C.F.R. § 1.97(b)(4)). No fee or statement is required.
- d. ☒ before the mailing date of a first Action on the merits (37 C.F.R. § 1.97(b)(3)). No fee or statement is required.
In the event that a first Office Action on the merits has been issued, please consider this IDS under 37 C.F.R. § 1.97(c) and see the statement under 37 C.F.R. § 1.97(e) below, or, if no statement has been made, charge our deposit account in the amount of \$180.00 as required by 37 C.F.R. § 1.17(p).

V. ☐ THIS IDS IS BEING FILED UNDER 37 C.F.R. § 1.97(c):
(check one box)

before the mailing date of a Final Office Action under 37 C.F.R. § 1.113 (See 37 C.F.R. § 1.97(c)(1)) or before the mailing date of a Notice of Allowance under 37 C.F.R. § 1.311 (See 37 C.F.R. § 1.97(c)(2)).

- a. ☐ No statement; therefore, a fee in the amount of \$180.00 as required by 37 C.F.R. § 1.17(p).
or
- b. ☐ See the statement below. No fee is required.

VI. STATEMENT UNDER 37 C.F.R. § 1.97(e) (check only one box)

The undersigned hereby states that

- a. ☐ each item of information contained in the IDS was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than 30 days prior to the filing of this IDS; or
- b. ☐ each item of information contained in the IDS was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this IDS; or
- c. ☐ no item of information contained in the IDS was cited in a communication from a foreign Patent Office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of IDS was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of the IDS.
- d. ☐ Some of the items of information were cited in a communication from a foreign Patent Office. As to this information, the undersigned states that each item of information contained in the IDS was first cited in a communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this IDS. As to the remaining information, the undersigned hereby states that no item of this remaining information contained in the IDS was cited in a communication from a foreign Patent Office in a counterpart foreign application and, to the best of my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this statement.

VII. PAYMENT OF FEES (check one box)

- ☐ A check in the amount of \$180.00 as required by 37 C.F.R. § 1.17(p) is enclosed for the above-identified fee.
- ☐ Please charge Deposit Account No. 02-2448 in the amount required by 37 C.F.R. § 1.17(p) for the above-indicated fee. This paper is submitted in triplicate.
- ☒ No fee is required.

If the Examiner has any questions concerning this IDS, he/she is requested to contact the undersigned. If it is determined that this IDS has been filed under the wrong rule, the PTO is requested to consider this IDS under the proper rule and charge the appropriate fee to Deposit Account No. 02-2448.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under § 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By

Michael K. Mutter, #29,680

MKM/slb
0365-0601PUS1

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

Attachment(s): ☒ PTO-1449
☐ Documents
☐ Foreign Search Report
☐ Fee
☐ Other:

MKM/slb

MKM/slb



UNITED STATES PATENT AND TRADEMARK OFFICE

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U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
10/502,336	Risto Tuominen	0365-0601PUS1

INTERNATIONAL APPLICATION NO.

PCT/FI03/00065

02292
 BIRCH STEWART KOLASCH & BIRCH
 PO BOX 747
 FALLS CHURCH, VA 22040-0747

LA. FILING DATE

01/28/2003

PRIORITY DATE

01/31/2002

CONFIRMATION NO. 5376

371 ACCEPTANCE LETTER



OC000000016022855

Date Mailed: 05/16/2005

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office in its capacity as a Designated / Elected Office (37 CFR 1.495), has determined that the above identified international application has met the requirements of 35 U.S.C. 371, and is ACCEPTED for national patentability examination in the United States Patent and Trademark Office.

The United States Application Number assigned to the application is shown above and the relevant dates are:

09/23/2004

DATE OF RECEIPT OF 35 U.S.C. 371(c)(1), (c)(2) and
 (c)(4) REQUIREMENTS

09/23/2004

DATE OF COMPLETION OF ALL 35 U.S.C. 371
 REQUIREMENTS

A Filing Receipt (PTO-103X) will be issued for the present application in due course. **THE DATE APPEARING ON THE FILING RECEIPT AS THE " FILING DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371 (c)(1), (c)(2) and (c)(4) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN ABOVE.** The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363). Once the Filing Receipt has been received, send all correspondence to the Group Art Unit designated thereon.

The following items have been received:

- Copy of the International Application filed on 07/23/2004
- Copy of the International Search Report filed on 07/23/2004
- Information Disclosure Statements filed on 07/23/2004
- Oath or Declaration filed on 09/23/2004
- U.S. Basic National Fees filed on 07/23/2004
- Priority Documents filed on 07/23/2004

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed

to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

KAYA L LEWIS BALTIMORE
Telephone: (703) 308-9100 EXT 202

PART 3 - OFFICE COPY

FORM PCT/DO/EO/903 (371 Acceptance Notice)

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	8418	((438/107,118,126) or (257/e23.005, e23.126,e23.128,e23.182,e21.5,e21.503,e21.505,e21.511)).CCLS.	US-PGPUB; USPAT	OR	OFF	2006/12/10 19:30
L2	57	(257/e21.5).CCLS.	US-PGPUB; USPAT	OR	OFF	2006/12/10 19:17
L3	672619	chip or die	US-PGPUB; USPAT	OR	OFF	2006/12/10 19:31
L4	1516176	opening "through-hole"	US-PGPUB; USPAT	OR	OFF	2006/12/10 19:31
L5	1236031	tape or resin or polymer	US-PGPUB; USPAT	OR	OFF	2006/12/10 19:31
L6	2961	3 with 4 with 5	US-PGPUB; USPAT	OR	OFF	2006/12/10 19:32
L7	233	1 and 6	US-PGPUB; USPAT	OR	OFF	2006/12/10 19:32
L8	25	(US-20060105500-\$ or US-20060110851-\$ or US-20010026010-\$ or US-20020180010-\$ or US-20030100142-\$ or US-20030162326-\$ or US-20040178510-\$ or US-20040266067-\$ or US-20050012032-\$ or US-20050067715-\$ or US-20050104211-\$ or US-20050285244-\$ or US-20060172464-\$).did. or (US-5216806-\$ or US-5637919-\$ or US-5162613-\$ or US-5208188-\$ or US-6537848-\$ or US-6607943-\$ or US-6710458-\$ or US-6717248-\$ or US-6790712-\$ or US-6964888-\$ or US-6979596-\$ or US-7033862-\$).did.	US-PGPUB; USPAT	OR	OFF	2006/12/10 21:53
L9	1	("4246595").PN.	US-PGPUB; USPAT	OR	OFF	2006/12/10 21:53
S1	65379	"438"/\$.ccls.	US-PGPUB; USPAT	OR	OFF	2004/03/31 19:04
S2	0	semiconductor or ic or "integrated circuit" or microelectronic	US-PGPUB; USPAT	OR	OFF	2003/05/29 17:11
S3	855	("438/for.227").CCLS.	EPO; JPO; DERWENT	OR	OFF	2005/12/07 16:56
S5	105811	"438"/\$.ccls.	US-PGPUB; USPAT	OR	OFF	2006/03/24 09:36
S6	196566	"257"/\$.ccls.	US-PGPUB; USPAT	OR	OFF	2006/03/24 09:36

EAST Search History

S7	746088	semiconductor or ic or "integrated circuit" or microelectronic	US-PGPUB; USPAT	OR	OFF	2006/03/24 09:36
S8	771582	S5 or S6 or S7	US-PGPUB; USPAT	OR	OFF	2006/04/12 11:51
S9	221599	S5 or S6	US-PGPUB; USPAT	OR	OFF	2006/04/12 11:50



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/502,336	09/23/2004	Risto Tuominen	0365-0601PUS1	5376

2292 7590 12/12/2006

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER

FOURSON, III, GEORGE R

ART UNIT PAPER NUMBER

2823

DATE MAILED: 12/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/502,336	TUOMINEN, RISTO	
	Examiner	Art Unit	
	George Fourson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on ____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-25 is/are pending in the application.

 4a) Of the above claim(s) ____ is/are withdrawn from consideration.

5) ☒ Claim(s) 1-5 is/are allowed.

6) ☐ Claim(s) ____ is/are rejected.

7) ☒ Claim(s) 6-25 is/are objected to.

8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date 7/23/04, 11/5/04.

4) ☐ Interview Summary (PTO-413)
 Paper No(s)/Mail Date. ____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: ____.

Art Unit: 2823

This application is in condition for allowance except for the following formal matters:

Claims 6-25 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim can not depend from another multiply dependent claim . See MPEP § 608.01(n).

Accordingly, the claims 6-25 have not been further treated on the merits.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

The following is an examiner's statement of reasons for allowance: The prior art taken alone or in combination neither discloses nor makes obvious the instant invention including hardening the insulating polymer layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Fourson whose telephone number is (571) 272-1860. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2823

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'George Fourson', written in a cursive style.

George Fourson
Primary Examiner
Art Unit 2823

GFourson
December 10, 2006

10/502336

JTI2004 PCT/PTO 23 JUL 2004

PTO/SB/08a/b (08-03)

Approved for use through 07/31/2008. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Application Number	Not Yet Assigned 10/502336
		Filing Date	July 23, 2004
		First Named Inventor	Risto TUOMINEN
		Art Unit	~~N/A~~ 2823
		Examiner Name	Not Yet Assigned- Fourson
Sheet 1 of 1	Attorney Docket Number	0365-0601PUS1	

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
GF	AA**	US-4,246,595-A1	01-20-1981	NOYORI et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
GF	BA	JP-A-2002-016327	1/18/2002		Translation Only	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 801.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
GF	CA	PATENT ABSTRACTS OF JAPAN, vol. 2002; no 05, May 3, 2002.	

MKM/clb

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature	/George Fourson/	Date Considered	12/10/2006
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(Use several sheets if necessary)

GROUP	UNKNOWN 2823
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EXAMINER INITIAL	DOCUMENT NUMBER	Kind	DATE	NAME	CLASS	SUP CLASS	FILING DATE IF APPROPRIATE
GF	US 4,246,595		1981-01-20	NOYORI et al.			
GF	US 6,038,133	A	2000-03-14	NAKATANI et al.			
GF	US 6,154,366	A	2000-11-28	MA et al.			
GF	US 6,271,469	A	2001-08-07	MA et al.			
GF	US 6,292,366	B1	2001-09-18	PLATT			
GF	US 6,475,877	B1	2002-11-05	SAIA et al.			
GF	US 6,489,685	B2	2002-12-03	ASAHI et al.			
GF	US 6,538,210	B2	2003-03-25	SUGAYA et al.			
GF	US 2002/0117743	A1	2002-08-29	NAKATANI et al.			
GF	US 2002/0185303	A1	2002-12-12	TAKEUCHI et al.			

[illegible]

OTHER DOCUMENTS (Include Name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.

EXAMINER: Initial if citation considered, whether or not citation is in conformance with W.P.B.P. 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Petitioner Samsung Ex-1006, 0152

U.S. PATENT DOCUMENTSFOREIGN PATENT DOCUMENTS

OTHER DOCUMENTS (Include Name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.

MM/81b

Notice of References Cited	Application/Control No. 10/502,336	Applicant(s)/Patent Under Reexamination TUOMINEN, RISTO	
	Examiner George Fourson	Art Unit 2823	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2006/0105500	05-2006	Chang, Wen-Yuan	438/121
*	B	US-5,216,806	06-1993	Lam, Ken	29/848
*	C	US-5,637,919	06-1997	Grabbe, Dmitry G.	257/690
*	D	US-2003/0100142	05-2003	Shin et al.	438/110
*	E	US-2004/0266067	12-2004	Bai, Jin-Chuan	438/126
*	F	US-2005/0285244	12-2005	Chen, Chi-Ming	257/678
*	G	US-5,162,613	11-1992	Schoenthaler, David	174/88R
*	H	US-5,208,188	05-1993	Newman, Robert A.	156/310
*	I	US-6,537,848	03-2003	Camenforte et al.	438/106
*	J	US-6,607,943	08-2003	Kinsman, Larry D.	438/124
*	K	US-6,710,458	03-2004	Seko, Toshiharu	257/778
*	L	US-6,790,712	09-2004	Bai, Jin-Chuan	438/126
*	M	US-6,979,596	12-2005	Corisis et al.	438/118

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/502,336	TUOMINEN, RISTO	
	Examiner	Art Unit	
	George Fourson	2823	

SEARCHED			
Class	Subclass	Date	Examiner
438	107	12/9/2006	GF
	118		
	126		
257	e23.004		
	e23.126		
	e23.128		
	e23.182		
	e21.5		
	e21.503		
	e21.505		
	e21.511		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST results attached	12/9/2006	GF



Docket No.: 0365-0601PUS1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Risto TUOMINEN

Application No.: 10/502,336

Confirmation No.: 5376

Filed: September 23, 2004

Art Unit: 2823

For: METHOD FOR EMBEDDING A
COMPONENT IN A BASE

Examiner: M. S. Smith

AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated December 12, 2006, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.

AMENDMENTS TO THE CLAIMS

1. (Original) A method for embedding at least one component in a base, which component has contact areas on its first surface, the method comprising

- taking a baseboard of the base, the baseboard having a first surface and a second surface,
- making conductive patterns on the baseboard and at least one hole for the at least one component, in such a way that each hole extends through the baseboard between the first surface and the second surface,
- spreading an insulating polymer layer on the second surface of the baseboard, in such a way that the insulating polymer layer covers the at least one hole made for the component,
- placing the at least one component in the at least one hole, in such a way that the component is aligned in relation to the conductive patterns made on the baseboard and the first surface of the component presses against the insulating polymer layer, and
- hardening the insulating polymer layer.

2. (Original) A method according to Claim 1, in which the first surface of the component is pressed into the unhardened insulating polymer layer.

3. (Original) A method according to Claim 1, in which the first surface of the component is pressed into the partly hardened insulating polymer layer.

4. (Original) A method according to any of Claims 1 - 3, in which the insulating polymer layer is manufactured by placing an RCC foil on the second surface of the baseboard.

5. (Original) A method according to any of Claims 1 - 3, in which the insulating polymer layer is manufactured by spreading a pre-preg epoxy film on the second surface of the baseboard.

6. (Currently amended) A method according to ~~any of Claims 1—5~~ Claim 1, in which ~~insulating—conducting~~ material is grown on the side walls of the hole made ~~for a~~ for the component, in order to create interference protection around the component.

7. (Currently amended) A method according to ~~any of Claims 1—6~~ Claim 1, in which the contact areas of the component have contact protrusions connected to them, and the component is placed in the hole in such a way that the contact protrusions push inside the insulating polymer layer.

8. (Currently amended) A method according to ~~any of Claims 1—6~~ Claim 1, in which the contact areas of the component have contact protrusions connected to them, the height of the contact protrusions being at least as great as the thickness of the insulating polymer layer, and the component is placed in the hole in such a way that the contact protrusions penetrate through the insulating polymer layer.

9. (Currently amended) A method according to ~~any of Claims 1—7~~ Claim 1, in which

- contact openings for the component are made in the hardened insulating polymer layer, and
- conductors for forming electrical contacts with the component are made in the contact openings and on top of the insulating polymer layer.

10. (Currently amended) A method according to ~~any of Claims 1—9~~ Claim 1, in which conductive patterns are made on at least the second surface (1b) of the baseboard, and in which the insulating polymer layer to be spread on the second surface (1b) of the baseboard is spread in such a way that it covers the conductive patterns made on the second surface (1b).

11. (Currently amended) A method according to ~~any of Claims 1—10~~ Claim 1, in which the first surface of the component is pushed into the insulating polymer layer, which is in contact

with the conductive patterns, which are formed from the conductive layer.

12. (Currently amended) A method according to ~~any of Claims 1—11~~ Claim 1, in which at least one set of conductive patterns are located between the insulating polymer layer, against which the first surface of the component is pushed, and the baseboard of the circuit board.

13. (Currently amended) A method according to ~~any of Claims 1—12~~ Claim 1, in which the baseboard is of an insulating material.

14. (Currently amended) A method according to ~~any of Claims 1—13~~ Claim 1, in which the component is secured in place in the at least one hole made for the component by filling a ~~hole the hole, made in the baseboard,~~ with a filler material.

15. (Currently amended) A method according to ~~any of Claims 1—14~~ Claim 1, in which the component is a microcircuit and an electrical contact is formed with the microcircuit from the direction of the first surface of the baseboard, after the microcircuit has been placed in the hole made in the baseboard.

16. (Currently amended) A method according to ~~any of Claims 1—15~~ Claim 1, in which an electrical contact is formed with the component by growing conductive material in the contact areas of the component, ~~or on top of its contact protrusions.~~

17. (Currently amended) A method according to ~~any of Claims 1—16~~ Claim 15, in which the electrical contact with the microcircuit is formed without solder using a circuit-board manufacturing technology.

18. (Currently amended) A method according to ~~any of Claims 1—17~~ Claim 1, in which ~~more than one component is embedded in the base and in which a separate hole is made comprising making a plurality of holes~~ in the baseboard for a plurality of components ~~each~~

~~component to be embedded in the base~~ base, and embedding each component to be embedded in the base is located in its own hole of said components in a separate hole of said plurality of holes.

19. (Currently amended) A method according to ~~any of Claims 1—18~~ Claim 1, in which a multi-layer structure is manufactured, in which there are at least four conductive layers on top of each other.

20. (Currently amended) A method according to ~~any of Claims 1—19~~ Claim 1, ~~in which a first base, into which~~ wherein at least two microcircuits are embedded in the base, and wherein at least one second base, in which at least two microcircuits are embedded, ~~are~~ is manufactured, and the bases are assembled and secured on top of each other in such a way that the bases are aligned in relation to each other.

21. (Currently amended) A method according to ~~any of Claims 1—19~~ Claim 1, in which

- a first and a second base and an intermediate layer are manufactured,
- the second base is placed above the first base and the second base is aligned in relation to the first base,
- the intermediate layer is placed between the first and the second bases, and
- the first and second bases are laminated to each other with the aid of the intermediate layer.

22. (Original) A method according to Claim 21, in which

- at least one third base and an intermediate layer for every third base are manufactured,
- each third base is placed in turn above the first and second bases and each third base is aligned in relation to one of the lower bases,
- an intermediate layer is placed beneath each third base, and
- the first, second, and each third base are laminated to each other with the aid of the intermediate layers.

23. (Original) A method according to any of Claims 20 - 22, in which holes for feed-throughs are drilled through the bases secured on top of each other and conductors are made in the drilled holes for connecting the electronic circuits of each base to each other to form an operational totality.

24. (Currently amended) A method according to ~~any of Claims 1—23~~ Claim 1, in which the temperature ~~of a~~ of the baseboard, component, ~~or~~ and conductive layer connected directly to ~~a component~~ the component, is, during the process, less than 200°C ~~and preferably in the range 20—85°C~~.

25. (Currently amended) An electronic module, which is manufactured using ~~a method according to any of Claims 1—24~~ the method of claim 1.

26. (New) The method according to Claim 1, in which the contact areas of the component have contact protrusions connected to them, and an electrical contact is formed with the component by growing conductive material on top of the contact protrusions.

27. (New) The method according to Claim 1, in which the temperature of the baseboard, component, and conductive layer connected directly to the component, is in the range 20 - 85°C during the process.

28. (New) The electronic module of Claim 25, comprising
the baseboard having the first surface and the second surface,
the conductive patterns on the baseboard and the at least one hole for the at least one component, wherein the at least one hole extends through the baseboard between the first surface and the second surface,
the hardened insulating polymer layer on the second surface of the baseboard, the insulating polymer layer covering the at least one hole made for the component,
the at least one component in the at least one hole, the at least one component having

contact areas on its first surface and the first surface of the component being against the hardened insulating polymer layer.

29. (New) The electronic module of Claim 25, comprising
conducting material on the side walls of the at least one hole for the at least one
component, in order to create interference protection around the component.

30. (New) The electronic module of Claim 25, comprising
contact openings for the component in the hardened insulating polymer layer, and
conductors for forming electrical contacts with the component in the contact openings
and on top of the hardened insulating polymer layer.

31. (New) The electronic module of Claim 25, wherein the at least one component is at
least one microcircuit.

32. (New) The electronic module of Claim 25, comprising a plurality of holes in the
baseboard and a plurality of components embedded each in the individual ones of said plurality
of holes.

33. (New) The electronic module of Claim 25, comprising at least four conductive layers.

34. (New) The electronic module of Claim 25, comprising at least two bases each having
at least one component embedded therein and said bases being secured on top of each other.

35. (New) The electronic module of Claim 26, wherein at least one of the bases has at
least two microcircuits embedded therein.

36. (New) The electronic module of Claim 25, comprising at least one intermediate layer
between said at least two bases secured on top of each other.

37. (New) The electronic module of Claim 25, comprising feed-throughs for electrically connecting the components of the bases to each other.

REMARKS

Claims 1-37 are pending in the above application. By the above amendment, claims 26-37 have been added.

The Office Action dated December 12, 2006, has been received and reviewed. In that Office Action it was indicated that claims 1-5 had been allowed and that claims 6-25 had not been treated on the merits because they were improperly multiple dependent claims. By the above amendment, the dependencies of claims 6-25 have been corrected to ensure that no multiple dependent claim depends from another multiple dependent claim. Minor changes to dependent claims 6-25 have also been made to more clearly define aspects of the present invention. In addition, new dependent claims 26-37 have been added.

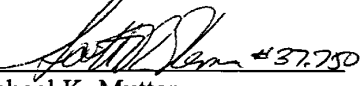
In view of the above amendments, it is respectfully submitted that claims 1-37 are in condition for allowance, and the allowance of these claims is earnestly solicited.

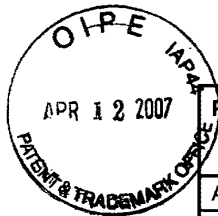
Should there be any outstanding matters that need to be resolved in the present application, the examiner is respectfully requested to contact Scott Wakeman (Reg. No. 37,750) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.14; particularly, extension of time fees.

Dated: April 12, 2007

Respectfully submitted,

By  #37,750
Michael K. Mutter
Registration No.: 29,680
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant



IFU

PTO/SB/22 (09-06)
Approved for use through 03/31/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)
FY 2006
(Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).)

Docket Number (Optional)
0365-0601PUS1

Application Number 10/502,336-Conf. #5376

Filed September 23, 2004

For METHOD FOR EMBEDDING A COMPONENT IN A BASE

Art Unit 2823

Examiner M. S. Smith

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	
☐ One month (37 CFR 1.17(a)(1))	\$120	\$60	\$
☒ Two months (37 CFR 1.17(a)(2))	\$450	\$225	\$ 450.00
☐ Three months (37 CFR 1.17(a)(3))	\$1020	\$510	\$
☐ Four months (37 CFR 1.17(a)(4))	\$1590	\$795	\$
☐ Five months (37 CFR 1.17(a)(5))	\$2160	\$1080	\$

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☒ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 02-2448. I have enclosed a duplicate copy of this sheet.

I am the ☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☒ attorney or agent of record. Registration Number 29,680

☐ attorney or agent under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34

Michael K. Mutter 437,750
Signature

April 12, 2007
Date

Michael K. Mutter
Typed or printed name

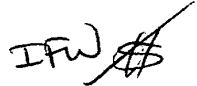
(703) 205-8000
Telephone Number

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☐ Total of 1 forms are submitted.

04/13/2007 YPOLITE1 00000000 022448
01 FC:1252 450.00 DA

10502336



Effective on 12/08/2004. Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818). FEE TRANSMITTAL For FY 2007 ☐ Applicant claims small entity status. See 37 CFR 1.27		Complete if Known <table border="1"> <tr> <td>Application Number</td> <td>10/502,336-Conf. #5376</td> </tr> <tr> <td>Filing Date</td> <td>September 23, 2004</td> </tr> <tr> <td>First Named Inventor</td> <td>Risto TUOMINEN</td> </tr> <tr> <td>Examiner Name</td> <td>M. S. Smith</td> </tr> <tr> <td>Art Unit</td> <td>2823</td> </tr> <tr> <td>Attorney Docket No.</td> <td>0365-0601PUS1</td> </tr> </table>		Application Number	10/502,336-Conf. #5376	Filing Date	September 23, 2004	First Named Inventor	Risto TUOMINEN	Examiner Name	M. S. Smith	Art Unit	2823	Attorney Docket No.	0365-0601PUS1
Application Number	10/502,336-Conf. #5376														
Filing Date	September 23, 2004														
First Named Inventor	Risto TUOMINEN														
Examiner Name	M. S. Smith														
Art Unit	2823														
Attorney Docket No.	0365-0601PUS1														
TOTAL AMOUNT OF PAYMENT	(\$) 450.00														

☐ Check
 ☐ Credit Card
 ☐ Money Order
 ☐ None
 ☐ Other (please identify): _____

☒ Deposit Account
 Deposit Account Number: 02-2448
 Deposit Account Name: Birch, Stewart, Kolasch & Birch, LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below
 ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17
 ☒ Credit any overpayments

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		<u>Small Entity</u>		<u>Small Entity</u>		<u>Small Entity</u>	
<u>Application Type</u>	<u>Fee (\$)</u>	<u>Fee (\$)</u>	<u>Fee (\$)</u>	<u>Fee (\$)</u>	<u>Fee (\$)</u>	<u>Fee (\$)</u>	<u>Fees Paid (\$)</u>
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

Fee Description	Fee (\$)	Fee (\$)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

HP = highest number of total claims paid for, if greater than 20.

HP = highest number of independent claims paid for, if greater than 3.

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

4. OTHER FEE(S)		Fees Paid (\$)
Non-English Specification, \$130 fee (no small entity discount)		
Other (e.g., late filing surcharge): 1252 Extension for response within second month		450.00

04/13/2007 XPOLITE1 00000037 022448 10502336
 Sale Ref: 00000090 DAN: 022448 10502336
 01 FC1252 456.00 DA

10/502,336

INDEX OF CLAIMS

✓ Rejected - (Through numeral) ... Canceled N Non-elected A Appeal
 = ... Allowed + ... Restricted I Interference O Objected

Claim	Date	Claim	Date	Claim	Date
1		51		101	
2		52		102	
3		53		103	
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33		83		133	
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48		98		148	
49		99		149	
50		100		150	

If more than 150 claims or 9 actions staple additional sheet here

182-44 05-27-03

PATENT APPLICATION FEE DETERMINATION RECORD

Effective Date: October 1, 2004

Application or Docket Number

10/502336

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	29	minus 20 = 9
INDEPENDENT CLAIMS	1	minus 3 =
MULTIPLE DEPENDENT CLAIM PRESENT ☒		

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY
TYPE ☐ OROTHER THAN
SMALL ENTITY

RATE	FEE
BASIC FEE	
X \$ 9 =	
X \$ 44 =	
+ \$ 150 =	
TOTAL	

RATE	FEE
BASIC FEE	1080
X \$ 18 =	162
X \$ 88 =	
+ \$ 300 =	290
TOTAL	1532

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	4/12/07	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR
Total	37	Minus	29 = 8
Independent	1	Minus	3 =
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

RATE	ADDITIONAL FEE
X \$ 9 =	
X \$ 44 =	
+ \$ 150 =	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X \$ 18 =	
X \$ 88 =	
+ \$ 300 =	
TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR
Total		Minus	=
Independent		Minus	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

RATE	ADDITIONAL FEE
X \$ 9 =	
X \$ 44 =	
+ \$ 150 =	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X \$ 18 =	
X \$ 88 =	
+ \$ 300 =	
TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR
Total		Minus	=
Independent		Minus	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

RATE	ADDITIONAL FEE
X \$ 9 =	
X \$ 44 =	
+ \$ 150 =	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X \$ 18 =	
X \$ 88 =	
+ \$ 300 =	
TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than "20", enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than "3", enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.



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NOTICE OF ALLOWANCE AND FEE(S) DUE

2292 7590 07/03/2007

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER

FOURSON III, GEORGE R

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 07/03/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/502,336	09/23/2004	Risto Tuominen	0365-0601PUS1	5376
TITLE OF INVENTION: METHOD FOR EMBEDDING A COMPONENT IN A BASE				

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$0	\$1700	10/03/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. **PROSECUTION ON THE MERITS IS CLOSED.** THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN **THREE MONTHS** FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. **THIS STATUTORY PERIOD CANNOT BE EXTENDED.** SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.
- B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

- A. Pay TOTAL FEE(S) DUE shown above, or
- B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

2292 7590 07/03/2007

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PO BOX 747
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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/502,336	09/23/2004	Risto Tuominen	0365-0601PUS1	5376

TITLE OF INVENTION: METHOD FOR EMBEDDING A COMPONENT IN A BASE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$0	\$1700	10/03/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
FOURSON III, GEORGE R	2823	438-106000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____
 Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/502,336	09/23/2004	Risto Tuominen	0365-0601PUS1	5376
2292	7590	07/03/2007	EXAMINER	
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			FOURSON III, GEORGE R	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 07/03/2007

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 353 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 353 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability**Application No.**

10/502,336

Applicant(s)

TUOMINEN, RISTO

Examiner

George Fourson

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed 4/12/07.
2. ☒ The allowed claim(s) is/are 1-37.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some* c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

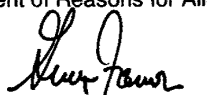
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____


George Fourson
Primary Examiner
Art Unit: 2823

Issue Classification 	Application/Control No. 10/502,336	Applicant(s)/Patent under Reexamination TUOMINEN, RISTO
	Examiner George Fourson	Art Unit 2823

ISSUE CLASSIFICATION									
ORIGINAL					INTERNATIONAL CLASSIFICATION				
CLASS		SUBCLASS			CLAIMED			NON-CLAIMED	
438		107			H	01	L	21	/58
CROSS REFERENCES									/
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)								/
438	118	126							/
257	e21.5	e23.126	e23.182	e21.511					/
									/
									/
									/
					Total Claims Allowed: 37				
(Assistant Examiner) (Date)					O.G. Print Claim(s) 1				
(Legal Instruments Examiner) (Date) <i>Heena Sept 26/28/07</i>					O.G. Print Fig. 3				
George Fourson Primary Examiner (Primary Examiner) (Date) <i>6/21/07</i>									

☒ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47	
Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		121
	2		32		62		122
	3		33		63		123
	4		34		64		124
	5		35		65		125
	6		36		66		126
	7		37		67		127
	8		38		68		128
	9		39		69		129
	10		40		70		130
	11		41		71		131
	12		42		72		132
	13		43		73		133
	14		44		74		134
	15		45		75		135
	16		46		76		136
	17		47		77		137
	18		48		78		138
	19		49		79		139
	20		50		80		140
	21		51		81		141
	22		52		82		142
	23		53		83		143
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	25		55		85		145
	26		56		86		146
	27		57		87		147
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							210

[illegible]

George Fourson

2823

Class	Subclass	Date	Examiner
438	107	6/21/2007	GF
	118		
	126		
257	e23.004		
	e23.126		
	e23.128		
	e23.182		
	e21.5		
	e21.503		
	e21.505		
	e21.511		

Class	Subclass	Date	Examiner
438	107	6/21/2007	
	118		
	126		
PG Pub Text Search		6/21/2007	GF

[illegible]



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov



Bib Data Sheet

CONFIRMATION NO. 5376

SERIAL NUMBER 10/502,336	FILING OR 371(c) DATE 09/23/2004 RULE	CLASS 438	GROUP ART UNIT 2823	ATTORNEY DOCKET NO. 0365-0601PUS1
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APPLICANTS

Risto Tuominen, Helsinki, FINLAND;

** CONTINUING DATA *****

G This application is a 371 of PCT/FI03/00065 01/28/2003

** FOREIGN APPLICATIONS *****

G FINLAND 20020191 01/31/2002

Foreign Priority claimed 35 USC 119 (a-d) conditions met Verified and Acknowledged	☒ yes ☐ no ☒ yes ☐ no ☐ Met after Allowance Examiner's Signature <u>Fourson</u> Initials <u>GF</u>	STATE OR COUNTRY FINLAND	SHEETS DRAWING 12	TOTAL CLAIMS 24	INDEPENDENT CLAIMS 1
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ADDRESS

2292

TITLE

Method for embedding a component in a base

FILING FEE RECEIVED 1662	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit
------------------------------------	---	---

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

2292 7590 07/03/2007

BIRCH STEWART KOLASCH & BIRCH, LLP
 PO BOX 747
 FALLS CHURCH, VA 22040-0747

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/502,336	09/23/2004	Risto Tuominen	0365-0601PUS1	5376

TITLE OF INVENTION: METHOD FOR EMBEDDING A COMPONENT IN A BASE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$0	\$1700	10/03/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
FOURSON III, GEORGE R	2823	438-106000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 BIRCH, STEWART, KOLASCH
 & BIRCH, LLP
 2
 3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.111. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

IMBERA ELECTRONICS OY

(B) RESIDENCE: (CITY AND STATE OR COUNTRY).

ESPOO, FINLAND

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies 4

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 02-2448 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature [Signature] # 37,750

Date OCTOBER 1, 2007

Typed or printed name MICHAEL K. MUTTER

Registration No. #29,680

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		10502336		
Filing Date:		23-Sep-2004		
Title of Invention:		METHOD FOR EMBEDDING A COMPONENT IN A BASE		
First Named Inventor/Applicant Name:		Risto Tuominen		
Filer:		Michael Keith Mutter/Tenika Askew		
Attorney Docket Number:		0365-0601PUS1		
Filed as Large Entity				
U.S. National Stage under 35 USC 371 Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1440	1440
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	4	3	12
Total in USD (\$)				1752

Electronic Acknowledgement Receipt	
EFS ID:	2265581
Application Number:	10502336
International Application Number:	
Confirmation Number:	5376
Title of Invention:	METHOD FOR EMBEDDING A COMPONENT IN A BASE
First Named Inventor/Applicant Name:	Risto Tuominen
Customer Number:	2292
Filer:	Michael Keith Mutter/Tenika Askew
Filer Authorized By:	Michael Keith Mutter
Attorney Docket Number:	0365-0601PUS1
Receipt Date:	01-OCT-2007
Filing Date:	23-SEP-2004
Time Stamp:	17:57:55
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	\$ 1752
RAM confirmation Number	2787
Deposit Account	022448
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	20071001IssueFee.pdf	69723 40e0a9ab549549feb37cd0c4b3d61a8f b3415777	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	8477 230d0c9fec9791afed18258872122784 e97b63c8	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			78200		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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Alexandria, Virginia 22313-1450
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/502,336	11/13/2007	7294529	0365-0601PUS1	5376

2292 7590 10/24/2007
BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 353 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Risto Tuominen, Helsinki, FINLAND;

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT5948335

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
Name		Execution Date
GE EMBEDDED ELECTRONICS OY		01/13/2020
RECEIVING PARTY DATA		
Name:	IMBERATEK, LLC	
Street Address:	13921 PARK CENTER RD, SUITE 380	
City:	HERNDON	
State/Country:	VIRGINIA	
Postal Code:	20171	
PROPERTY NUMBERS Total: 26		
Property Type	Number	
Patent Number:	6991966	
Patent Number:	7294529	
Patent Number:	7299546	
Patent Number:	7673387	
Patent Number:	7696005	
Patent Number:	8062537	
Patent Number:	8225499	
Patent Number:	8238113	
Patent Number:	8240032	
Patent Number:	8286341	
Patent Number:	8547701	
Patent Number:	8581109	
Patent Number:	8631566	
Patent Number:	8659134	
Patent Number:	8699233	
Patent Number:	8735735	
Patent Number:	8964409	
Patent Number:	8984746	
Patent Number:	9301394	
Patent Number:	9420694	

Property Type	Number
Patent Number:	9425158
Patent Number:	9999136
Patent Number:	8076586
Patent Number:	8704359
Patent Number:	9363898
Patent Number:	8240033

CORRESPONDENCE DATA

Fax Number: (703)643-9789
Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 4349062975
Email: yoon@capitoliplaw.com
Correspondent Name: YEASUN YOON
Address Line 1: 20319 KIAWAH ISLAND DR
Address Line 4: ASHBURN, VIRGINIA 20147

ATTORNEY DOCKET NUMBER:	PA01GETOIMBERATEK
NAME OF SUBMITTER:	YEASUN YOON
SIGNATURE:	/yoon/
DATE SIGNED:	02/05/2020
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 7
source=imbera assignment#page1.tif
source=imbera assignment#page2.tif
source=imbera assignment#page3.tif
source=imbera assignment#page4.tif
source=imbera assignment#page5.tif
source=imbera assignment#page6.tif
source=imbera assignment#page7.tif

CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS

This CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS (this “**Assignment**”) is made this 13th day of January 2020, by **GE Embedded Electronics Oy**, a Finnish company (“**Assignor**”), in favor of **ImberaTek, LLC**, a Delaware limited liability company (“**Assignee**”).

WHEREAS, Assignor and Assignee are party to that certain patent sale agreement of December 19, 2019 (the “**Patent Sale Agreement**”); capitalized terms used but not otherwise defined in this Assignment shall have the respective meaning assigned thereto in the Patent Sale Agreement; and

WHEREAS, pursuant to the Patent Sale Agreement, Assignor has agreed to sell, convey, transfer, assign and deliver to Assignee all right, title and interest, including, without limitation, Patent Rights, in and to the patents, provisional patent applications, and patent applications listed on Schedule A hereto (collectively, the “**Patents**”).

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged by Assignor, Assignor hereby sells, conveys, transfers, and assigns to Assignee, its successors, legal representatives, and assigns all right, title and interest in the United States and throughout the world in and to:

the Patents and any and all letters patent that are or may be granted thereon, and any legal equivalent and counterpart thereof that may be granted in any country or countries foreign to the United States, in each case including without limitation any extensions, substitutes, continuations, continuations-in-part, divisions, reissues, reexaminations, and renewals thereof, or other equivalents thereof, and further, all rights and privileges pertaining to the Patents and any and all letters patent that are or may be granted thereon, and any legal equivalent thereof that may be granted in any country or countries foreign to the United States as well as all inventions, invention disclosures, and discoveries described in any of the foregoing and including, without limitation, the right, if any, to petition, sue or otherwise seek and recover damages, profits and any other remedy (monetary, injunctive, declaratory or other relief or remedy of any kind) in the United States and anywhere throughout the world for any past, present and future infringement thereof, conversion or misappropriation of, or other injury, offense, violation, breach of duty or wrong relating to, any of the Patents, or any license, agreement, contract or other matter relating thereto.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks of the United States of America and the appropriate officers of all other jurisdictions in which the Patents are or may be registered or in which applications included among the Patents are pending, to record the title of Assignee, its successors, legal representatives and assigns, as owner of all right, title and interest in and to the Patents, and to issue to Assignee, its successors, legal representatives and assigns, all letters patent and any legal equivalent thereof that may be granted in any country or countries foreign to the United States and recordings of patent rights resulting from any application included among the Patents, according to this instrument.

Except to the extent that federal law preempts state law with respect to the matters covered hereby, this Assignment shall be governed by and construed in accordance with the laws of the State of Delaware, without giving effect to any of the principles of conflicts of laws thereof that would result in the application of the laws of another jurisdiction to this Assignment.

This Assignment will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

Assignor has the full power and authority, and has obtained all Third-Party consents, approvals and/or other authorizations required to enter into this Assignment and to carry out its obligations hereunder.

IN WITNESS WHEREOF, Assignor has caused this Assignment to be executed by its duly authorized officer, as of the date first written above.

ASSIGNOR:

GE Embedded Electronics Oy

By: 

Name: Patrick K. Patnode

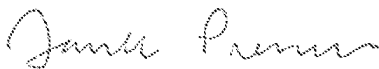
Title: Authorized Signatory

Acknowledgement:

State of New York)

ss.

County of Schenectady)


SANDRA PREISMAN
Notary Public, State of New York
Reg. No. 8022402
Qualified in Schenectady County
Commission Expires February 10, 2023

On this 13 day of January 2020, before me appeared Patrick K. Patnode, the person who signed this instrument, who acknowledged that he/she signed it as a free act on his/her own behalf or on behalf of the Assignor with authority to do so.

**SCHEDULE A
TO
CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS
PATENTS**

Number	Title	Applicant	Current Assignee	filing date	Family	Estimated Expiration
<u>EP01104647B</u> 1	Method for Manufacturing Solderless High-Density Electronic Modules	Imbera Electronics Oy		2000.04.17	FR, DE, GB	2020.04.17
<u>US6991966</u>	Method for embedding a component in a base and forming a contact	Imbera Electronics Oy	GE Embedded Electronics Oy	2003.01.28	BRPI0307364B1, CN100566511C, DE60300619T2, EP1474959B1 (AT, FR, DE, IT, IE) (not GB), FI115285B, HK1077151A1, IL163238A, IN224711, KR1013325B1, SG105702, RU2297736C2	2023.01.28
<u>US7294529</u>	Method for embedding a component in a base	Imbera Electronics Oy	GE Embedded Electronics Oy	2003.01.28	CN102348324B, CN1625926B, EP1477048 (GB, AT, FR, DE), FI119215B, IN241345, RU2327311C2, US7732909B2, US7989944B2, US8368201B2, US8455994B2	2024.01.16
<u>US7299546</u>	Method for manufacturing an electronic module	Imbera Electronics Oy	GE Embedded Electronics Oy	2004.02.25	EP1597947(GB, FR, DE) FI119583B, US10085345B2, US2018376597A1, US7609527B2, US8817485B2	2024.03.20
<u>US7673387</u>	Manufacture of a layer including a component	Imbera Electronics Oy	GE Embedded Electronics Oy	2005.08.04	AT503718B1, CN100543983C, FI117812B, JP4630333B2, US8487194B2	2026.08.09

<u>US7696005</u>	Method for manufacturing an electronic module in an installation base	Imbera Electronics Oy	GE Embedded Electronics Oy	2004.09.15	CN1853451B, DE11200400172 7T5, GB2422054B, JP4977464B2, US2015124411A 1, US9232658B2	2025.06.12
<u>US8062537</u>	Method for manufacturing an electronics module	Imbera Electronics Oy	Imbera Electronics Oy	2005.11.23	CN101065843B, FI117369B, JP5160895B2, KR101101603B1	2027.06.27
<u>US8225499</u>	Method for manufacturing a circuit board structure, and a circuit board structure	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.16	CN101199244B, DE11200600150 6 FI121134B, GB2441265B	2028.08.19
<u>US8238113</u>	Electronic module with vertical connector between conductor patterns	Imbera Electronics Oy	Imbera Electronics Oy	2010.07.23		2031.02.11
<u>US8240032</u>	Method for manufacturing an electronics module comprising a component electrically connected to a conductor-pattern layer	Imbera Electronics Oy	Imbera Electronics Oy	2005.06.13	CN101010994B, DE11200500141 4T5, FI117814B, JP4796057B2, KR101034279B1	2028.03.15
<u>US8240033</u>	Method for manufacturing a circuit board	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.15	BR PI0612060-1 CN101199242B, FI122128B, IN269884 JP5175719B2, KR101455234B1 , SG138149	2029.02.21
<u>US8286341</u>	Method of manufacturing a wiring board	Imbera Electronics Oy	Imbera Electronics Oy	2009.04.08	CN102007825B, EP2274962B1 (AT, DE, GB) FI121909B, IN306150B, JP5551680B2, KR101260908B1	2030.09.07
<u>US8547701</u>	Electronics module and method for manufacturing the same	Imbera Electronics Oy	Imbera Electronics Oy	2005.11.24		2026.06.12
<u>US8581109</u>	Method for manufacturing a circuit board structure, and a circuit board structure	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.16	CN100596258C, EP1891845(AT, DE, FR, GB), FI119714B, IN271174 JP5025644B2, KR101090423B1 , US2017071061A 1, US9622354B2	2028.08.19

<u>US8631566</u>	Circuit board structure comprising an electrical component and a method for manufacturing a circuit board structure comprising an electrical component	Imbera Electronics Oy	Imbera Electronics Oy	2009.08.24	FI125526B	2031.08.25
<u>US8659134</u>	Multi-chip package and manufacturing method	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2009.07.21	FI122217B, US9691724B2	2031.03.25
<u>US8699233</u>	Circuit module and method of manufacturing the same	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2009.05.11	CN102027585B, FI123205B, US9107324B2, US9324647B2, US9883587B2	2030.10.11
<u>US8735735</u>	Electronic module with embedded jumper conductor	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.07.23	US10231335B2	2030.12.18
<u>US8964409</u>	Electronic module with EMI protection	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.02.05	CN101800216B, JP6126770B2, KR101781446B1, US10010019B2, US2018352689A1	2031.02.23
<u>US8984746</u>	Manufacture of a circuit board containing a component	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2007.03.15	US10085347B2	2030.11.07
<u>US9301394</u>	Manufacturing method and electronic module with new routing possibilities	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.05.19	US15,937,967 (Reissue application of US9301394)	2033.05.29
<u>US9420694</u>	Method for controlling warpage within electronic products and an electronic product	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.08.31		2030.10.31

<u>US9425158</u>	Rigid-flex module and manufacturing method	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.01.05	CN101770959A, CN108133897A, FI122216B, JP5714231B2, KR101615955B1, US9674948B2, US9820375B2	2031.03.14
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<u>US9999136</u>	Method for fabrication of an electronic module and electronic module	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2014.12.15	AT516639B1, CN105704926A, DE10201501619 6A1, FR3030109B1, JP2016157919A, KR20160072822 A, TW201633860A, IN352016	2034.12.15
<u>KR101060856</u>	Method for manufacturing an electronic module, and an electronic module		Imbera Electronics Oy	2010.12.15	(JP 4537995 is an EPCOS patent)	2004.02.25
<u>US8076586</u>	Heat conduction from an embedded component		Imbera Electronics Oy	2011.12.13		2027.10.05
<u>US8351214</u>	Electronics module comprising an embedded microcircuit		Imbera Electronics Oy	2013.01.08	GB2429848, JP5064210, DE 112005000952.1, <u>CN101027948B</u>	2027.07.03
<u>US8034658</u> (divisional of EPCOS patent US7663215)	Electronic module with a conductive-pattern layer and a method of manufacturing same		Imbera Electronics Oy	2011.10.11	FI115601, MX262301, IN236924, KR10068797600 00, BRPI0408964-2, CA2520992, CN100556233, SG115077, IL171212, CN101546759, MX285993, HK1089328, GB1609339, FR1609339, DE1609339	2024.04.08
<u>US8222723</u>	Electric module having a conductive pattern layer		Imbera Electronics Oy	2012.07.17		2024.10.03

US8704359	Method for manufacturing an electronic module and an electronic module		GE Embedded Electronics Oy	2014.04.22		2025.04.13
<u>US9363898</u>	Method for manufacturing an electronic module and an electronic module		GE Embedded Electronics Oy	2016.06.07		2024.03.31