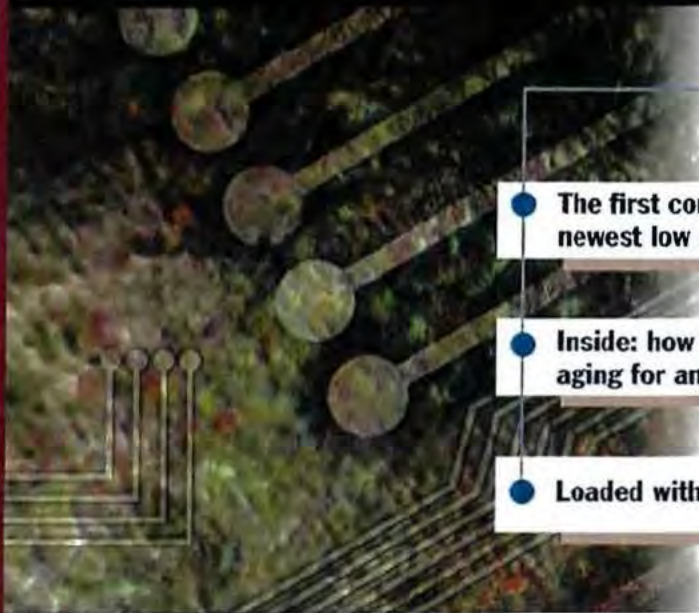


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- The first comprehensive application guide to the newest low cost flip chip technologies

- Inside: how to create effective and reliable packaging for any interconnect system

- Loaded with in-depth technical detail

Low Cost Flip Chip Technologies

for | DCA, WLCSP, and
PBGA Assemblies

JOHN H. LAU

**Low Cost
Flip Chip
Technologies**

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John H. Lau

Express Packaging Systems, Inc.

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ation (SMTA) Conference Proceedings (*Journal of Surface Mount Technology*), the National Electronic Packaging Conferences (NEPCON) and Proceedings, the *IBM Journal of Research and Development*, *Electronic Packaging and Production*, *Advanced Packaging*, *Circuits Assembly*, *Surface Mount Technology*, *Connection Technology*, *Solid State Technology*, *Circuit World*, *Microelectronics International*, and *Soldering and Surface Mount Technology*.

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JOHN H. LAU
Palo Alto, California

Integrated Circuit Packaging Trends

1.1 Introduction

The electronics industry is one of the most dynamic, fascinating, and important areas of manufacturing. In a relatively short period of time, it has become the largest and most pervasive manufacturing industry in the developed world.

The invention of the bipolar transistor by John Bardeen, Walter Brattain, and William Shockley at Bell Laboratories (now Lucent Technologies) in 1947 foreshadowed the development of generations of computers yet to come. The invention of the silicon integrated circuit (IC) by Jack Kilby of Texas Instruments in 1958 and by Robert Noyce and Gordon Moore of Fairchild Semiconductor in 1959 stimulated the development of generations of small, medium, large, very large, ultra-large, giga, and yet-to-come scale integrations (SSI, MSI, LSI, VLSI, ULSI, GSI, and . . . SI).

Fifty years ago, the average family probably owned five active electronic devices. Today, the average family owns hundreds of millions of transistors, and it is probable that by the year 2000, the figure will be more than 1 billion. This has produced a global revolution of major proportions that affects the lives of people everywhere.

The IC chip is not an isolated island. It must communicate with other IC chips in a circuit through an input/output (I/O) system of interconnects. Furthermore, the IC chip and its embedded circuitry are delicate, requiring the package to both carry and protect the chip. Consequently, the major functions of the electronics package are: (1) to provide a path for the electric current that powers the circuits on the IC chip; (2) to distribute the signals onto and off of the IC chip; (3) to

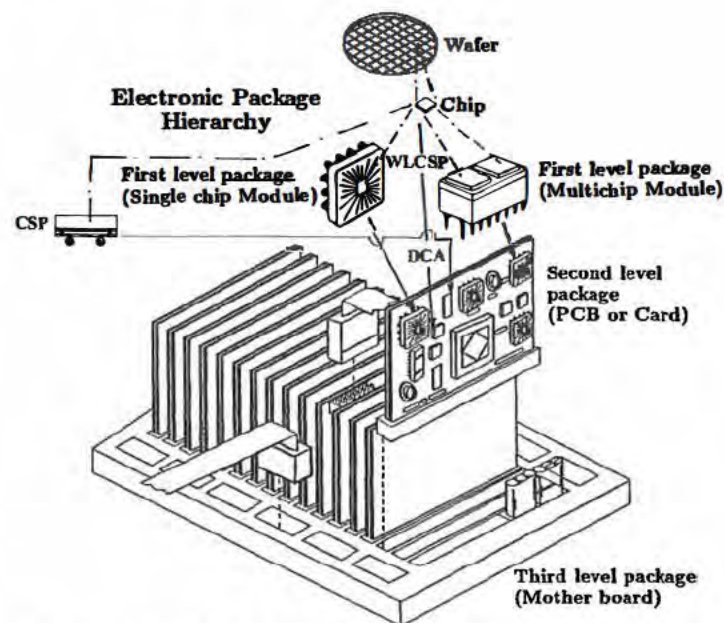


Figure 1.1 The first three levels of electronics packaging.

remove the heat generated by the circuits on the IC chip; and (4) to support and protect the IC chip from hostile environments.

Figure 1.1 shows a schematic representation of electronic package hierarchy. Packaging focuses on how a chip (or many chips) is packaged cost efficiently and reliably.¹⁷⁵ Packaging is an art based on the science of establishing interconnections ranging from zero-level packages (i.e., chip-level connections such as gold and solder bumps) to first-level packages (either single- or multichip modules), second-level packages [e.g., printed circuit board (PCB)], and third-level packages (e.g., motherboard). In this chapter, the IC trends will be briefly discussed first. Then the packaging technologies for the ICs will be briefly updated.

1.2 IC Trends

1.2.1 IC density and feature size

The past decade has witnessed an explosive growth in IC density (i.e., number of transistors per chip) and chip size. One of the key reasons for this is the advance of the complementary metal-oxide-semiconductor (CMOS) process (Fig. 1.2), which has very fine feature sizes (Fig. 1.3) and high yields. Today, 0.2- μm sizes are in volume production. According

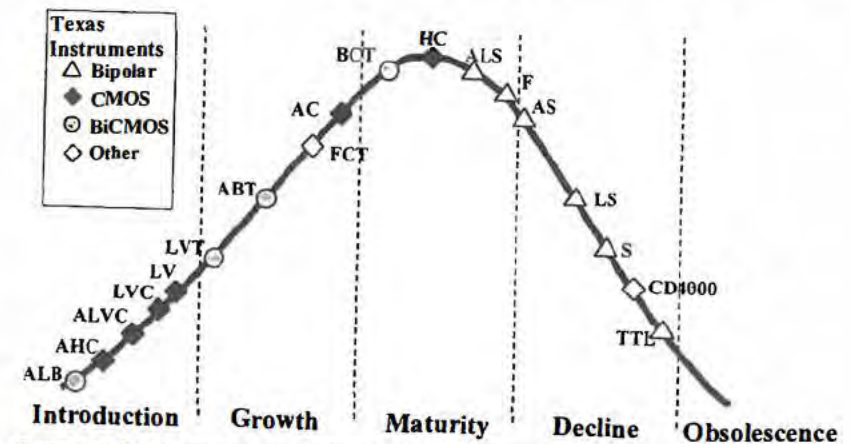


Figure 1.2 IC process technology trends. (Source: Texas Instruments)

to the Semiconductor Industry Association (SIA)'s technology road map, 1-cm² chips containing 16 million transistors are forecast to be in volume production by the year 2001 (Table 1.1).

1.2.2 IC operating voltage

Because of the explosive growth in portable electronic products, the operating voltage (power supply) on the IC chip has been reduced from

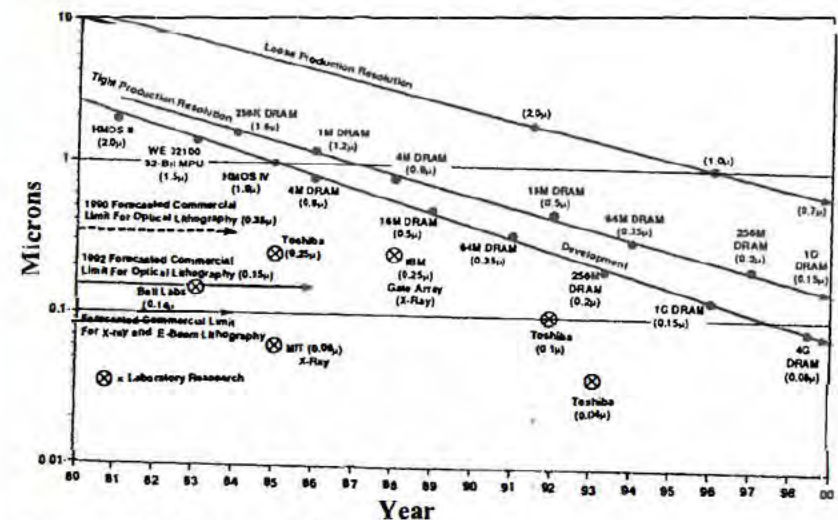


Figure 1.3 IC feature size trends.

TABLE 1.1 SIA's Overall Device Technology Trends

	1997	1999	2001	2006	2012
Memory					
Generation at production ramp	64M	256M	1G	4G	64G
Bits/cm ² at sample/introduction	96M	270M	380M	2.2B	17B
Logic (high volume, cost performance MPU)					
Logic transistors/cm ²	3.7M	6.2M	10M	39M	180M
Logic (low volume ASIC)					
Transistors/cm ²	8M	14M	16M	40M	100M
Functions/chip					
DRAM bits/chip	267M	1.07G	1.7G	17.2G	275G
Chip size (cm²)					
DRAM	2.8	4	4.45	7.9	15.8
MPU	3	3.4	3.85	5.2	7.5
ASIC (Maximum litho field area)	4.8	8	8.5	10	13
Number of chip I/Os					
Chip-to package, high-performance	1450	2000	2400	4000	7300
Chip-to-package, cost performance	800	975	1195	1970	3585
Number of package pins/balls					
ASIC, high performance	1100	1500	1800	3000	5500
MPU/controller, cost-performance	600	810	900	1500	2700
Chip frequency (MHz)					
On chip, across chip clock, high performance	750	1200	1400	2000	3000
Power supply voltage (V)					
Minimum logic voltage	1.8-2.5	1.5 1.8	1.2 1.5	0.9 1.2	0.5-0.6
Power (W)					
High performance with heat sink	70	90	110	160	175

5 V to either 3 or 3.3 V. This figure will eventually drop to 2.5 V, then 1.5 V, as shown in Fig. 1.4 and Table 1.1. One of the key reasons is that the power consumption is proportional to the square of the operating voltage, i.e., the lower the operating voltage, the longer the battery life of the portable electronic products.

1.2.3 Microprocessor, ASIC, DRAM, and SRAM

In most of the electronic products, there are four major IC devices: the microprocessor, the application-specific IC (ASIC), the cache memory, and the main memory. For example, a personal computer usually has one microprocessor; a few cache memories, e.g., fast static random access memory (SRAM); a few ASICs, e.g., video, sound, data path,

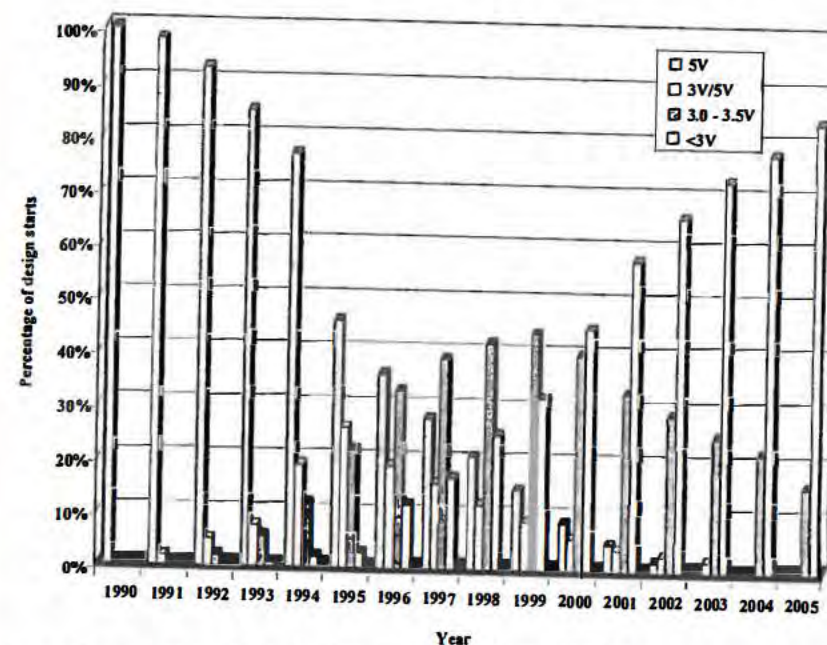


Figure 1.4 Transition of operating voltage from 5 V to less than 3 V.

high-speed memory controller, NuBus controller, and I/O controller; and many system memories, such as read only memory (ROM), which contains permanent code used by software applications, and dynamic random access memory (DRAM) to store the information while the power is turned on.

The microprocessor is the brain of a computing system. Some well-known microprocessors are Intel's complex instruction set computing (CISC)-based microprocessor family (e.g., the Pentiums); IBM, Motorola, and Apple's reduced instruction set computing (RISC)-based PowerPC microprocessors; Hewlett-Packard's RISC-based PA8000; Compaq Computer's RISC-based Alpha chipset; Silicon Graphics' RISC-based MIPS; AMD's CISC-based K5, K6, and K7; and Sun Microsystems' RISC-based UltraSparc. Both RISC-based and CISC-based microprocessors are expected to require package pin counts of over 1000 and to perform at over 500-MHz on-chip clock frequencies (Fig. 1.5).

The SRAMs for cache memories are expected to perform at high speeds similar to those of the microprocessors to prevent system data bottlenecks. Even the ASICs are expected to run at on-chip clock frequencies faster than 300 MHz and to have package pin counts of up to 900. (The ASICs of some telecommunication products need pin counts

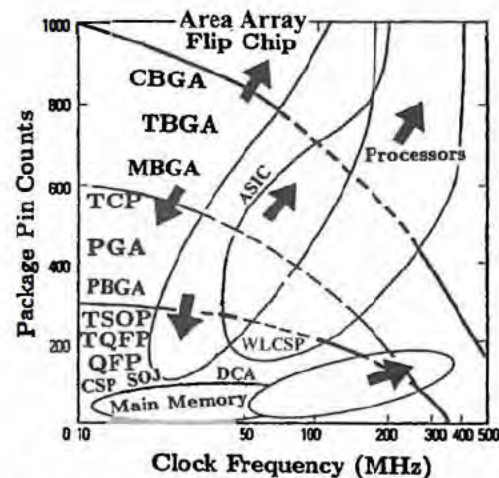


Figure 1.5 IC devices and packaging trends.

of more than 1000.) The DRAM densities are performing in accordance with Moore's law (Figs. 1.6 and 1.7), i.e., the number of transistors per chip doubles for every 18-month period.

1.2.4 Copper Interconnects

More than 99 percent of IC chips used in the world today are equipped with Al interconnects. However, IC chips with Cu interconnects are being manufactured and implemented in the products of some well-known companies. For example, IBM is shipping the 400-MHz Cu-based powerPC 750 microprocessors (with 33 percent improvement) and implementing the Cu-pad technology into its S/390, RS/6000, and AS/400 server families. Motorola's Cu-based CMOS process produces the highest-clock-frequency SRAM devices. Apple Computer uses Cu wire interconnects to enhance the performance of its Power Mac G3. Cu-based devices in the 0.18- μm generation are being offered by TSMC; Lucent is implementing these devices in the 0.16- μm generation; and Intel is planning them in the 0.13- μm generation.

The advantages of Cu-based IC devices are: (1) higher conductivity with lower resistance, (2) lower capacitive load on the interconnects, (3) lower power consumption, (4) lower crosstalk, (5) fewer metal layers, (6) fewer manufacturing steps, (7) less fabrication space, (8) shorter production cycle time, (9) fewer defects in IC devices, and (10) better electromigration performance. The disadvantages are: (1) deposition of Cu in layers only several atoms thick is more difficult, (2) contamina-

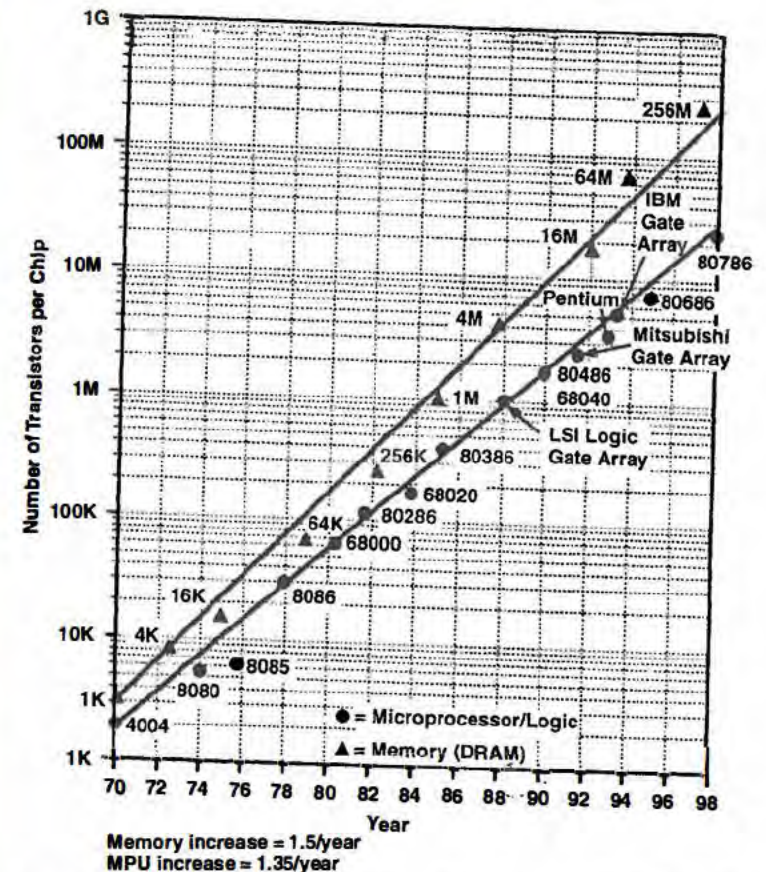


Figure 1.6 IC density trends for DRAMs and microprocessor/logic (Moore's law). (Source: ICE Corp.)

tion with the underlying silicon layer will lower transistor performance, (3) migration between Cu lines makes shorts more likely, (4) the equipment is more expensive, and (5) there is a thermal coefficient of expansion mismatch between the Si chip and the Cu pads and lines.

Some well-known equipment companies are also supporting the Cu-based technology. For example, Applied Materials provides the Copper Interconnect Equipment Set Solution (CIESS) for fabricating a complete multilevel copper interconnect structure, and the millenia electra electrochemical plating system (MEEPS) for filling vias and trenches with copper. LAM Research, Novellus, and KLA-Tencor are planning to offer a complete Cu-based production line soon.

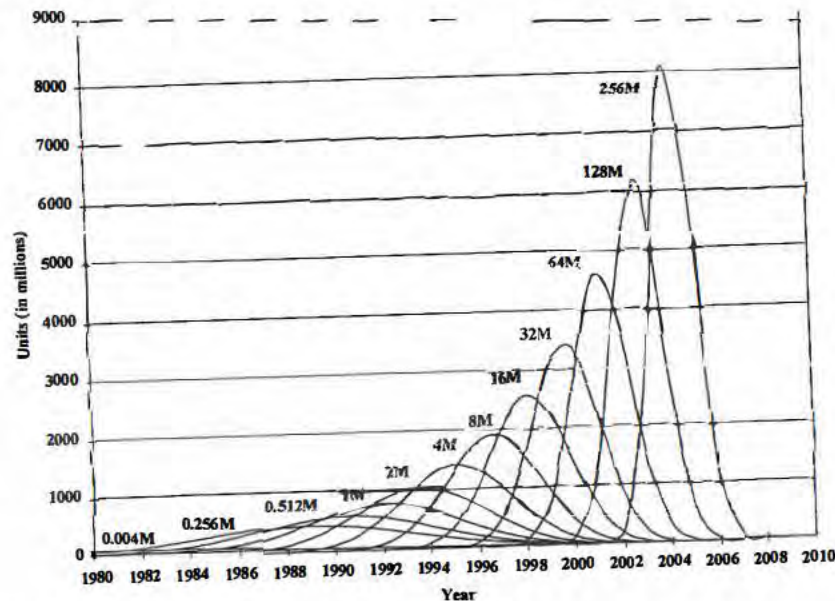


Figure 1.7 DRAM densities are tracking Moore's law.

1.2.5 Moore's Law

Since 1965, Moore's Law has been an unshakable principle for the computer industry: every 18 months, the number of transistors that will fit on a silicon chip doubles. As transistors have been scaled ever smaller, computing performance has risen exponentially while the cost of that power has been driven down. And it has been assumed (or set as a goal) in the semiconductor industry that this rate of progress would hold for at least another 10 to 15 years.

Recently, however, more and more people have reported that insurmountable barriers have forced the repeal of Moore's Law much closer at hand, perhaps early in the coming decade. It is not clear whether the most common type of silicon transistor can be scaled down beyond the generation of chips that will begin to appear in the next couple of years, because semiconductor engineers have not found ways around basic physical limits.

For example, in the current generation of semiconductors, the wires that interconnect transistors are etched as fine as $0.18\ \mu\text{m}$ and the individual insulating layers inside a transistor may be only four or five atoms thick. Semiconductor factories in Japan plan to begin mass production of chips based on $0.13\text{-}\mu\text{m}$ technology early next year, and such

chips should be in widespread use within two years. But beyond that generation, the industry's leading researchers acknowledge there remain far more questions than answers. This is because the next step would be $0.1\text{-}\mu\text{m}$ technology, a milestone that in the Moore's Law progression would be expected three to five years from now. But at that scale, transistors will be composed of fewer than 100 atoms, and statistical variations in this lilliputian world are beyond the ability of silicon semiconductor engineers to control.

Without further advances in the miniaturization of silicon-based transistors, hopes for continued progress would have to be based on technologies that are promising but unproved: new materials, new transistor designs, and advances like IBM's silicon-on-insulator and HP's molecular computing. Instead of shrinking today's CMOS technologies, IBM discovered that its silicon-on-insulator technology holds great promise at dimensions of $0.1\ \mu\text{m}$ and smaller. HP and the University of California at Los Angeles invented the Carbon 60 molecule known as the buckyball, in which single molecules act as digital on-off switches.

Thus, in order to extend the reign of Moore's Law, the industry should be prepared and accepting of new technology. Says Randall Isaac, vice president for systems technology and science at IBM's Watson Laboratory in Yorktown Heights, New York, "When a given technology saturates, it is usually replaced by a new one."

1.3 Packaging Technology Update

The major trend in electronic products today is to make them smarter, lighter, smaller, thinner, shorter, and faster, while at the same time more friendly, functional, powerful, reliable, robust, innovative, creative, and inexpensive (Fig. 1.8). As the trend toward miniature and compact products continues, the introduction of products that are more user friendly, that contain a wider variety of functions, and that can be put into a tiny box will provide growth in the market. One of the key technologies that is helping to make these goals for miniaturized and integrated product design possible is electronics packaging and assembly technology, especially low-cost flip chip technology. For example, in 1992 the typical video camera consisted of over 1800 components, with a density of 12 components per cm^2 . It occupied $2380\ \text{mm}^3$ and utilized a black-and-white charge-coupled device (CCD) array for viewing. The 1998 video camera consisted only 848 components, with a density of 21 components per cm^2 . It occupied only $1598\ \text{mm}^3$ and utilized a color liquid crystal display (LCD) for viewing (Table 1.2). The size and weight of the video camera are expected to be reduced by 50 percent by the year 2002.

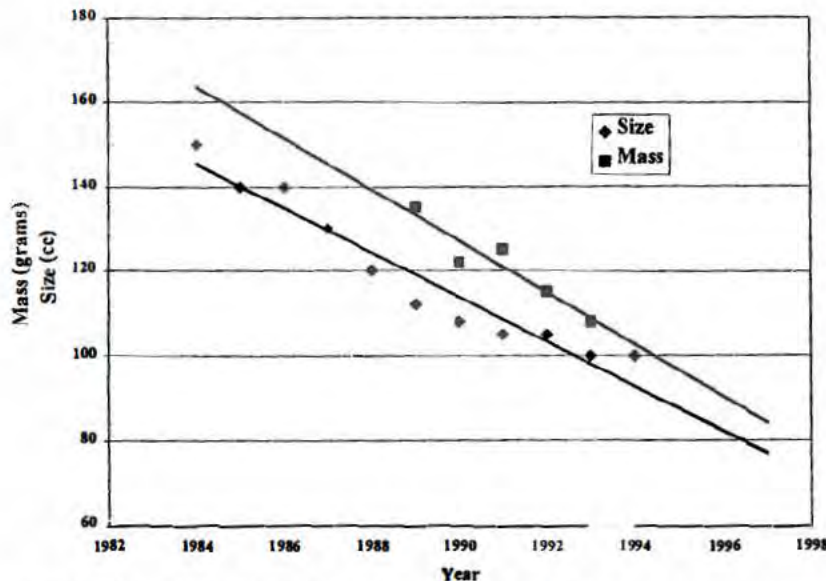


Figure 1.8 Cellular phone mass and size trends (without battery).

Different packaging technologies are required for different semiconductor IC devices and applications.^{1 174} Figure 1.5 shows some of the well-known packaging technologies for four of the major IC devices (e.g., ASIC, microprocessor, cache, and system memory).

The dashed lines in Fig. 1.5 demarcate four regions of applications. The first region is for low-pin-count IC devices; the packaging technologies are plastic quad flat pack (PQFP), Swiss outline package (SOP), Swiss outline J-leaded (SOJ), small outline IC (SOIC), plastic leaded chip carrier (PLCC), thin quad flat pack (TQFP), thin small outline package (TSOP), direct chip attach (DCA), chip scale package (CSP), and wafer level CSP (WLCSP).

The packaging technologies such as the tape carrier package (TCP), plastic pin grid array (PPGA), ceramic pin grid array (CPGA), and plastic ball grid array (PBGA) will meet the needs for the second region of applications. For higher-pin-count and higher-performance IC devices (the third region of applications), ceramic ball grid array (CBGA), tape ball grid array (TBGA), and metal ball grid array (MBGA) are cost-effective packaging technologies. For the fourth region of applications (IC devices with very high pin counts and performances), area-array solder-bumped flip chip technology is the solution.

TABLE 1.2 Electronic Product Trend Example: Video Camera

Year Model	1992 NV-S1	1998 DS7
Size		
Volume	2,380 mm ³	1,590 mm ³
Weight	900 g	690 g
Technology	Analog	Digital
Display	Black and white	Color
	CCD array	LCD
Circuit board		
Density	12 components/cm ²	21 components/cm ²
Technology	0.5 mm quad flat pack	CSP
Component technology		
Chips		
1005	115	56
1608	990	29
2124/2520	190	55
Transistor	205	58
Tantalum	130	31
Odd-form	116	60
IC		
SOP/QFP	24	38
CSP	0	10
Total components	1800	848

1.3.1 Area-array flip chip technology

For high-price and high-speed microprocessors and ASICs, the complex IC designs require very high I/O and performance packages. For these types of ICs and subsystems, area-array solder-bumped flip chip technology provides a viable answer to the needs (Fig. 1.5). Usually, these ICs are packaged in a CPGA, a PPGA, a CBGA, a TBGA, or an MBGA in a single-chip format. Recently, PBGAs with solder-bumped flip chips (Fig. 1.9) using the DCA technology have become very popular.

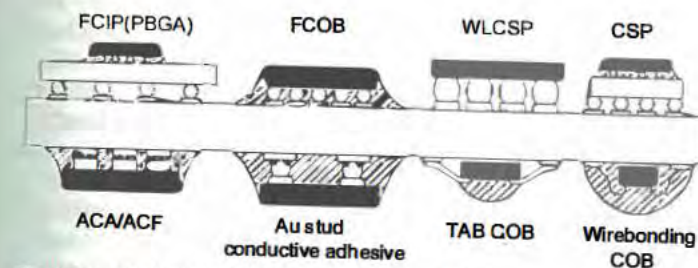


Figure 1.9 Various packaging technologies on PCB.

1.3.2 BGA technology

There are many different kinds of ball grid array (BGA) packages.^{3,5} Depending on their substrates, they are known as CBGA, MBGA, TBGA, and PBGA. Figure 1.5 shows that for high-I/O and high-performance ASICs and microprocessors, CBGA, MBGA, and TBGA could meet the high pin count (>500), power, and clock frequency requirements, but at higher costs.

Due to the fine pitch and pin count limitations of PQFP and the high cost of CBGAs, MBGAs, and TBGAs, the PBGA is cost effective at package pin counts between 250 and 600. The major difference between PQFP and PBGA is that PQFP has a leadframe and PBGA has an organic substrate. The leadframe was standardized for fanning the circuitry more than 15 years ago, while the PBGA's substrate is still custom designed. Today, the leadframe is cheaper than the organic substrate. Thus, in order for the PBGA packages to be popular, the substrate has to be standardized and lower in cost. Again, some system makers employ PBGA packages to house the solder-bumped flip chip by using the DCA technology (Fig. 1.9) for very high pin count (>1000) and performance (see Chap. 15).

1.3.3 TCP

TCP offers smaller pitches, thinner package profiles, and smaller footprints on the PCB. TCP can provide moderate-performance solutions for applications (e.g., ASICs and microprocessors) with package pin counts of up to about 600. It is noted that unless it is a very high volume production, TCP may not be cost effective due to very high development cost of these custom-designed packages. Also, TCPs suffer the same drawbacks (e.g., peripheral chip carrier, long lead length, handling, board level manufacturing yield loss) as the PQFPs.

1.3.4 TSOP and PQFP

Up to 208 pins (0.5-mm pitch and 28-mm body size), 240 pins (0.5-mm pitch, 32-mm body size), and 304 pins (0.5-mm pitch and 40-mm body size), the PQFPs are the most cost-effective packages for surface-mount technology (SMT). They have been used extensively for ASICs and low-performance and low-pin-count microprocessors. Sometimes, they are used to house one or more cache memories. Currently, the price for the PQFP packages is 0.5¢ per pin.

TSOP is a very low-profile plastic package that is specifically designed for SRAM, DRAM, and flash memory (which retains information even when the power is turned off) devices for space-limited applications. Right now, the price for TSOP is less than 1¢ per pin.

1.3.5 CSP and DCA

One of the most cost-effective packaging technologies is DCA. Some examples are shown in Figure 1.9, e.g., wire bonding chip on board,⁶ tape automated bonding (TAB) chip on board,¹⁰ flip chip with Au stud and conductive adhesive on board,⁴ flip chip with anisotropic conductive adhesive (ACA) on board, flip chip with anisotropic conductive film (ACF) on board, and solder-bumped flip chip on board. However, because of the infrastructure and the cost of supplying the known good die (KGD) and the corresponding fine line and spacing PCB, most in the industry are still working on these issues.

In the meantime, a class of new technology called CSP has surfaced. There are more than 40 different CSPs reported today;¹ most are used for SRAMs, DRAMs, flash memories, and ASICs and microprocessors without high pin counts. The unique feature of most of the CSPs is the use of a substrate (carrier or interposer) to redistribute the very fine-pitch (as small as 0.075 mm) peripheral pads on the chip to much larger-pitch (1, 0.8, 0.75, and 0.5 mm) area-array pads on the PCB.

The advantages of CSP over DCA are that with the carrier (interposer), the CSP is easier to test at speed and burn in for KGD, to handle, to assemble, to rework, and to standardize; it is easier to protect the die and to deal with die shrink; and there are fewer infrastructure constraints. On the other hand, DCA has better electrical performance and less weight, size, and cost.

1.3.6 Wafer-level packaging

Since the publications by Tsukada, et al.⁵⁸⁻⁶⁰ in 1992, the electronic packaging industry has witnessed an explosive growth in the research and development efforts devoted to solder bumped-flip chips on low-cost PCB or organic substrate,^{61 168, 175} even though Citizen was making low-end watches at very high volumes with this technology a few years earlier (Fig. 1.10). Because of the thermal expansion mismatch between the silicon chip and the epoxy substrate, underfill encapsulant is usually needed for solder joint reliability. However, due to the underfill operation, the manufacturing cost is increased and the manufacturing throughput is reduced. In addition, the rework of an underfilled flip chip on PCB is very difficult, if it is not impossible. This further complicates the KGD-related issues.

There is another reason why DCA is not very popular yet. Usually, the pitch and size of the pads on the peripheral-arrayed chips (more than 90 percent of the IC chips used in the world) are very small and pose great demands on the supporting structures (PCB or organic substrate). The high-density and fine-line-width/spacing PCBs with sequential built-up circuits with microvias are not commonly available at reasonable cost yet.

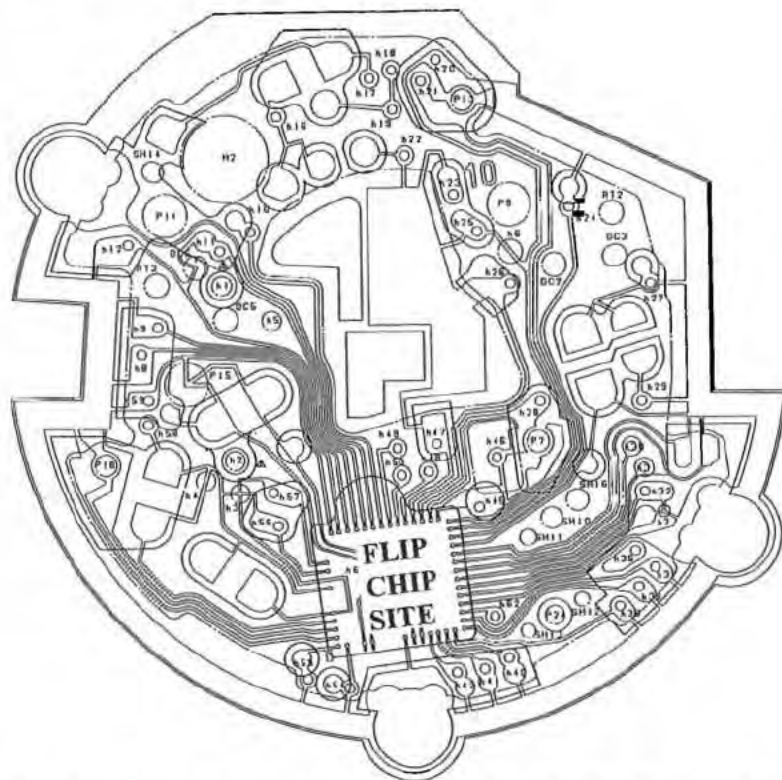


Figure 1.10 Low cost organic substrate for Citizen's watch with solder bumped flip chip with underfill.

Meantime, a new class of packaging called wafer-level chip scale package (WLCSP) provides a solution to these problems. (Lau and Lee¹ discuss the WLCSPs of eight different companies.) The unique feature of most WLCSPs is the use of a metal layer to redistribute the very fine-pitch peripheral-arrayed pads on the chip to much larger-pitch area-array pads with much larger solder joints (see Figs. 1.11 and 1.12) on the PCB. With WLCSPs, the demands on the PCB are relaxed, the underfill is not needed, and the KGD issues are much simpler. Thus, WLCSP is welcomed by system makers, because WLCSP is (potentially) lower in cost for high-yield IC chips (a necessary condition) and easier to assemble on PCB with higher yield (just like DCA but without underfill encapsulant).

There are more advantages of WLCSP compared to conventional CSP. Since the package is processed on a whole wafer before the individual

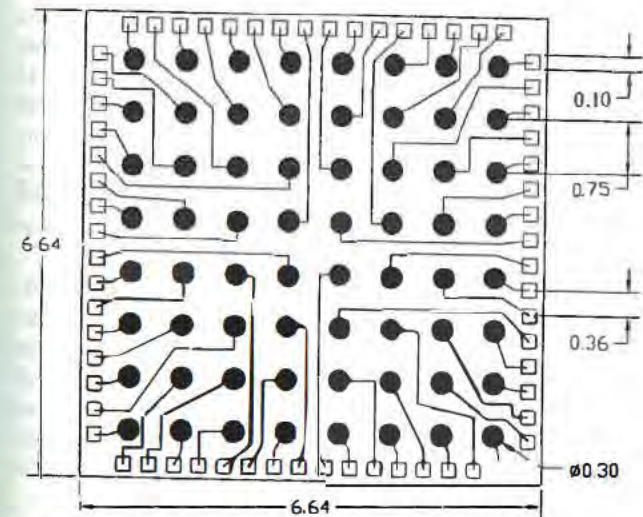


Figure 1.11 WLCSP of a peripheral-arrayed chip.

chips are separated, it may be possible to shorten the logistics chain by bringing packaging and final test back to the wafer FAB. In this case, the wafer would be functionally tested only once—after final packaging. There will be no need for a wafer probe for screening test before packaging, since the whole wafer will be packaged anyway. Also, WLCSP is not only one of the chip scale packages but a real chip size package. Finally, WLCSP enables copper interconnects on the chip. In view of Fig. 1.5,

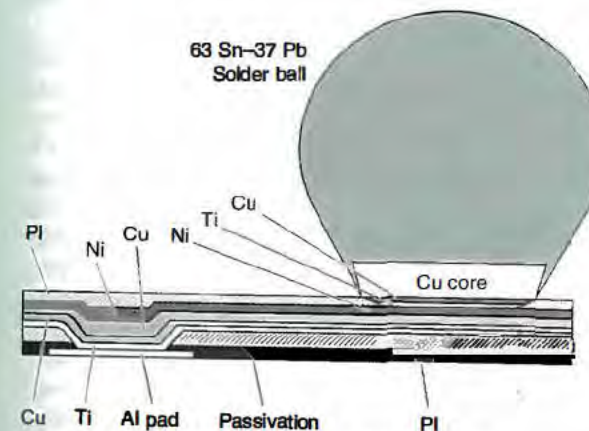


Figure 1.12 Structural cross section of the WLCSP.

WLCSP is most cost effective if the pin count is less than 250 and is perfect for DRAM devices in which the chip is large relative to its pin count.

The disadvantages of WLCSP compared to conventional CSP are: (1) high cost for poor-yield IC chips, (2) problems with system makers if the IC chip shrinks, (3) difficulty of test at speed and burn-in at high temperature on a wafer, and (4) higher-density substrates. It should be noted that even though the concept of wafer-level packaging has been used by IBM for its solder-bumped flip chip technology for more than 30 years, nevertheless, now is the exciting time for WLCSP!

It is noted that a new burn-in method that has recently been qualified at Motorola is called *wafer-level burn-in* (WLBI). This is a lower-cost method than die-level burn-in, which allows simultaneous burn-in of all die on a wafer. This process uses a sacrificial metal circuit applied to the wafer for the burn-in and test contacts, and also provides for flip chip requirements. The WLBI circuit design, burn-in process, test strategy, die preparation, and assembly requirements can be found in Beddingfield et al.¹⁷⁵

1.4 Summary

A brief overview of trends in IC devices (e.g., microprocessor, ASIC, cache memory, and system memory) has been presented. Also, various packaging technologies such as the area-array flip chip, BGA, TCP, CSP, WLCSP, and DCA for the IC devices have been briefly discussed.

The area-array solder-bumped flip chip technology is suitable for very high-I/O and high-performance single-chip modules for the microprocessors and ASICs. CBGAs, MBGAs, and TBGAs are cost-effective packages for microprocessors and ASICs with pin counts over 500 and high power dissipation. Usually, the area-array solder-bumped flip chip is packaged in a CBGA, an MBGA, or a TBGA.

In general, PBGAs are cost effective for packaging the ASICs (and sometimes the microprocessors) with pin counts of 250 to 600 and power dissipations of less than 5 W. In some cases, PBGAs with lower pin counts (less than 200) are also cost effective for housing a cache or a few fast SRAMs. For the solder-bumped flip chip in a PBGA package or the cavity-down thermal-enhanced wire bonding chip in a PBGA package, the back of the chip is attached to a heat spreader, which could be mounted with a heat sink. In that case, its power dissipation could be as high as 50 W and it could be used to house high-power microprocessors and ASICs.

CSPs are usually used to package memory and low-power (less than 1 W), low-pin-count (less than 200) ASICs, even though higher-pin-count (more than 1000), higher-power ICs have been tried in laboratories. Except for a handful of vertically integrated companies, DCAs are still

awaiting the time when the KGD and high-density microvia buildup PCBs are commonly available at reasonable costs. The wait should not be too long, and they will come in a few years. While we are waiting, WLCSP is enjoying its honeymoon.

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Chip-Level Interconnects: Wire Bonds and Solder Bumps

2.1 Introduction

The objective of chip-level connection, also called zero-level packaging, is to provide the required connections between the chip and the next level of interconnect, such as the PCB or the substrate of a package. There are many different chip-level interconnects; the most popular are wire bonds, gold bumps, and solder bumps. Today, more than 90 percent of the chips used have wire bonds. No more than 6 percent of the chips used have Au bumps through tape automated bonding (TAB). (TAB is a very interesting subject; however, it has been presented in Lau¹ and will not be discussed in this book.) Fewer than 4 percent of the chips now used have solder bumps.

Wire bonding of chips on board and on organic substrate in a package has been used for many years.²⁻¹¹ As mentioned earlier, more than 90 percent of the IC chips used in the world have wire bonds, because the high-speed automatic wire bonders meet most of the needs of the semiconductor devices for the next-level packaging interconnection. Figure 2.1 shows schematically an example of 0.1-mm-pitch wire bonding on a silicon chip. Today, however, pitches of 0.076 to 0.889 mm are used more and more in prototypes. The diameter of gold wire ranges between 20 and 33 μm , and the corresponding ball diameters are determined to be 2.5 to 4 times the wire diameter. The speed of most of the wire bonders is already four wires or eight bonds per second. The bottleneck in wire bonding is the bonding capillary (Fig. 2.2).

Figure 2.3 shows a photo of wires bonded on an organic substrate in a 1000-pin PBGA package.¹² The wires are bonded in a 50- μm -pitch staggered pattern as shown in Fig. 2.4. In order to prevent wiring short

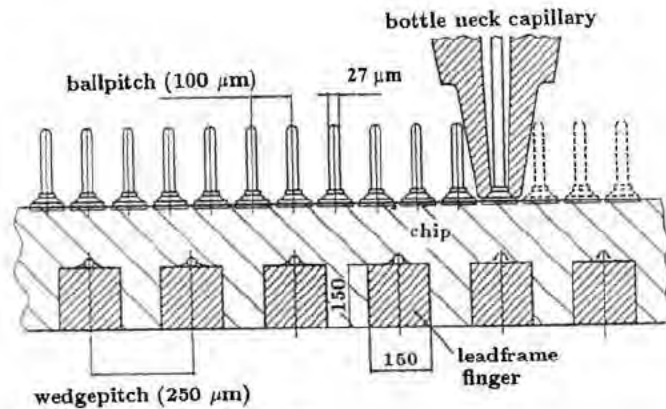


Figure 2.1 Wire bonding on chip.

circuits, the loop heights of the upper and lower wires are not the same, as shown in Fig. 2.5. Figures 2.6 and 2.7 show, respectively, photos of 60- μm -pitch in-line and staggered wire bonds.¹³ Wire bonding of chips on board has been examined extensively in Lau⁸ and Harman⁹ and will only be discussed briefly in this book. Figure 2.8 shows solder bumps on a silicon chip, which will be the focus of this book.

2.2 Wire Bonds Versus Solder Bumps

The past few years have witnessed explosive growth in the research and development efforts devoted to solder-bumped flip chips on low-cost organic substrates as a direct result of the higher requirements of package density, performance, and interconnection and the limitations of wire-bonding technology. In comparison with the popular wire-bonding

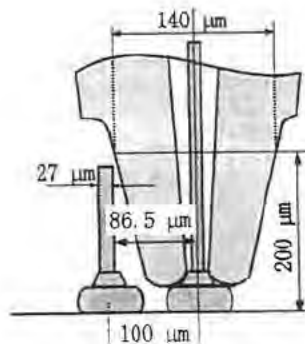
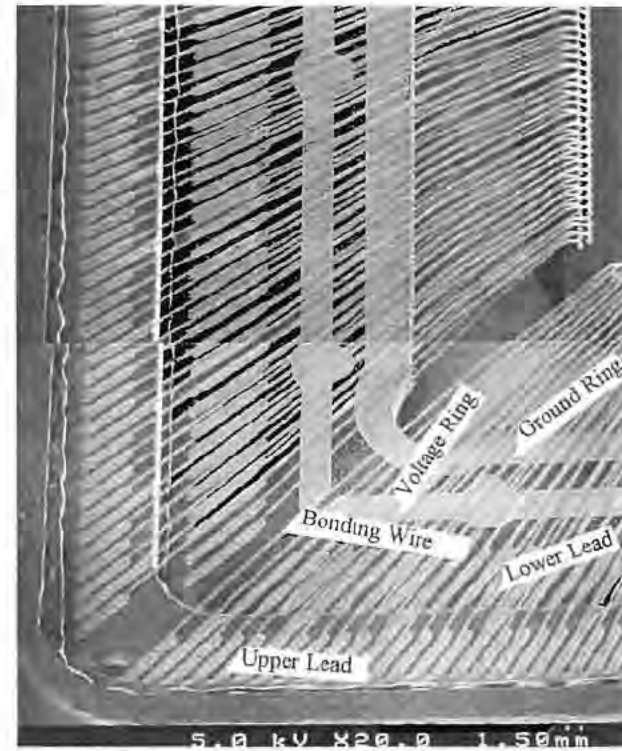


Figure 2.2 Diagram of the bonding capillary during wire bonding.

Figure 2.3 Scanning electron microscope (SEM) photograph of wires bonded in fine 50- μm pitch.

face-up technology, flip chip technology provides higher packaging density (greater I/Os) and performance (shorter possible leads, lower inductance, and better noise control), smaller device footprints, and a lower packaging profile. For example, for AC current the inductance for flip chip solder joints is about 0.4 nH, while that for wire bonding is 1.1 nH/mm. For DC current, the resistance of solder bumps is less than 1 m Ω . The advantages and disadvantages of flip chip and wire-bonding technologies are shown in Table 2.1.

Just like many other new technologies, low-cost solder-bumped flip chips still face certain critical issues. In the development of flip chips on board and in a plastic package, the following must be noted and understood in order to obtain the technology's full benefits:

- The infrastructure of flip chips is not well established.
- Flip chip expertise is not commonly available.
- Wafer bumping is still too costly.



Figure 2.4 Magnified SEM image of the bonding wires at the chip area.

- Bare die/wafer is not commonly available.
- Bare die/wafer handling is not easy.
- Pick and place is more difficult.
- Fluxing is more critical.
- Underfill decreases manufacturing throughput.

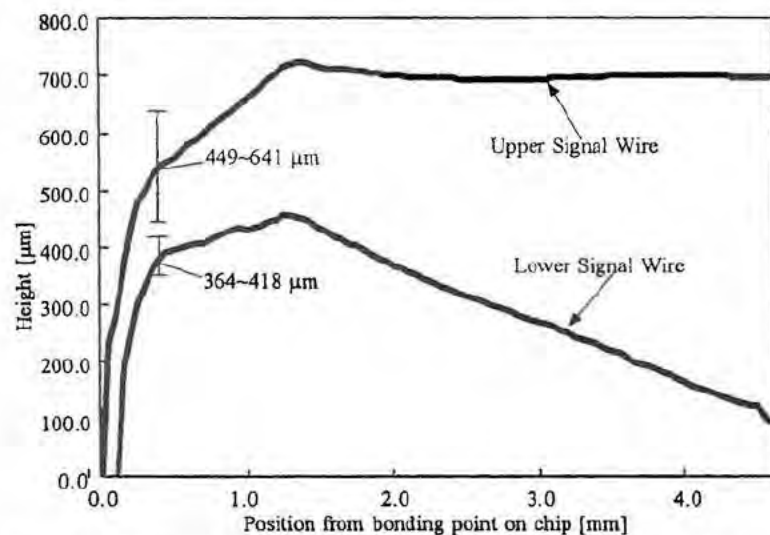


Figure 2.5 Upper and lower signal loop height. The minimum wire distance between the upper and lower signal wires is 31 μm .

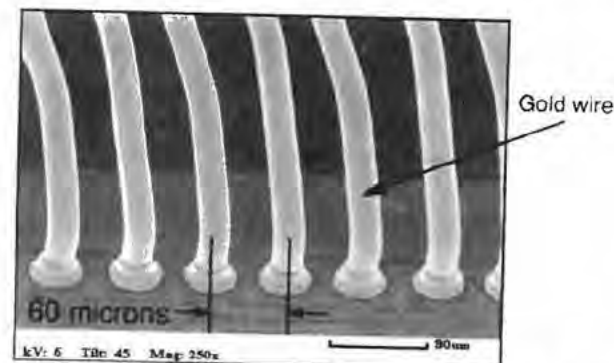


Figure 2.6 SEM photograph of 60- μm in-line pitch device side.

- Rework is more difficult.
- Solder joint reliability is more critical.
- Inspection is more difficult.
- Flip chip assembly testability is not well established.
- Die shrink and expand are troubles for system makers.
- There are known good die issues.
- Chip cracking during solder reflow has been reported.

What is the cost comparison between solder-bumped flip chip and wire bonding? This is a frequently asked question, in addition to the

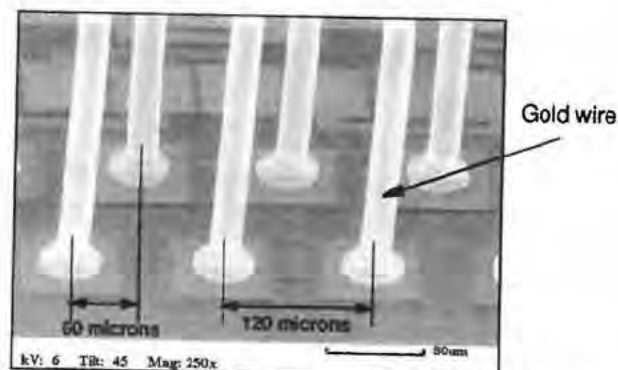


Figure 2.7 SEM photograph of 60- μm staggered pitch device side.



Figure 2.8 SEM photograph of solder bumps on chip.

critical issues just mentioned. The answer is almost impossible to determine. First of all, either flip chip or wire bonding is just an interconnect technology for connecting the IC chip to the next level of interconnection. Second, the impact of these interconnect technologies on the cost of the final product depends on the upstream (e.g., semiconductor design,

TABLE 2.1 Comparison Between Flip Chip and Wire Bonding Technologies

	Flip chip technology	Wire bonding technology
Advantages	■ High density ■ High I/Os ■ High performance ■ Noise control ■ Thin profile ■ SMT compatible ■ Area-array technology ■ Small device footprints ■ Self-alignment	■ Mature technology ■ Infrastructure exists ■ Flexible for new devices ■ Flexible for new bonding patterns
Disadvantages	■ Availability of wafers ■ Availability of dies ■ Availability of KGD ■ Wafer bumping ■ Test and burn-in ■ Underfill encapsulation ■ Additional equipment ■ Additional processes ■ Difficulty of rework after encapsulation ■ Die shrink	■ Availability of wafers ■ Availability of dies ■ Availability of KGD ■ Tests and burn-in ■ I/O limitation ■ Peripheral technology ■ Sequential process ■ Additional equipment ■ Additional processes ■ Difficulty of rework ■ Glob-top encapsulation

materials, and manufacturing)¹⁴⁻¹⁸ and downstream (e.g., substrate and printed circuit board) of this level of interconnect, and the functions of the final product. However, making some assumptions, the cost of solder-bumped flip chip and wire bonding chip on board or on substrate in a plastic package could be analyzed,¹⁹ which is the objective of this section.

2.2.1 Assembly process

Figure 2.9 shows a very simplified assembly process for wire-bonding chip and solder-bumped flip chip on either board or organic substrate. More detailed information on design, materials, processes, reliability, and applications for wire bonding and flip chip technologies can be found in Refs. 2 to 11. It should be noted that there are two ways to do the screening test for solder-bumped flip chip technology. One is to test before wafer bumping. In this case, the probe marks (damages) will be on

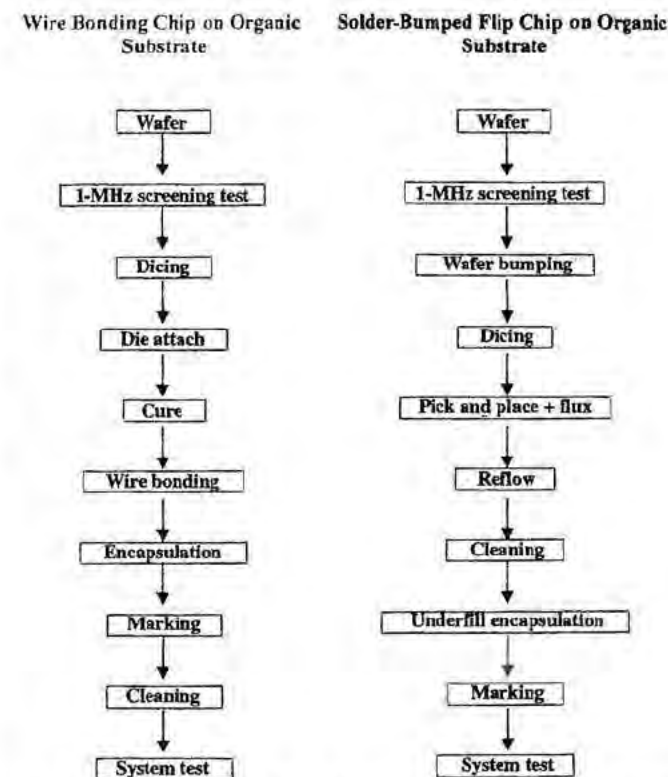


Figure 2.9 Wire bonding chip and solder-bumped flip chip on board process flows.

the pad, which could affect the integrity of the under-bump metallurgy and result in potential effects on long-term reliability. The other screening test method is to test after wafer bumping. This will contaminate the probe needles and result in shorts. Also, solder bumps could be damaged. However, better yield could be obtained because of the better electrical contact between the probe needles and the solder bumps (i.e., the number of false negatives during testing is reduced by better contacts between the probes and the bumps). For a mature wafer-bumping process, the bump yield per wafer (Y_B) is usually very high (over 98 percent).

From a cost point of view, the most important difference between wire bonding and solder-bumped flip chip is that the wire-bonding technology needs gold wire and the solder-bumped flip chip technology needs wafer bumping. The second most important difference between these two technologies is the effect on IC chip yields of the 1-MHz screening test and at-speed/burn-in system tests. Finally, different major equipment is needed for each of these interconnect methods.

2.2.2 Major equipment

The major equipment needed by wire-bonding chip and solder-bumped flip chip on board or on a plastic ball grid array (PBGA) package substrate is shown in Table 2.2. It should be noted that equipment required

TABLE 2.2 Major Equipment for Flip Chip and Wire Bonding Technologies

Flip chip		Wire bonding	
Equipment	Cost	Equipment	Cost
Pick and place + flux	3 @ \$500K = \$1500K	Die attach	\$220K
Reflow oven	\$70K	Cure oven	\$20K
Clean	\$130K	Wire bonders	35 @ \$110K = \$3850K
Underfill dispenser	5 @ 120K = \$600K	Encapsulation	\$700K (Transfer mold)
Vertical cure oven	\$100K	or	5 @ \$120K = \$600K
X-ray	\$300K	(glob-top dispenser)	
Total	\$2700K	plus vertical cure oven = \$100K	
		Total	\$4790K

- Machine utilization is 7200 hours per year.
- Machine capacity is 12 million chips per year.
- Pick and place + fluxing is assumed to be 6.5 seconds per chip.
- Underfill dispensing is assumed to be 10 seconds per chip (to completely fill the chip).
- Wire bonder speed is assumed to be 4 wires or 8 bonds per second. Also it is assumed that there are 300 pads per chip.
- Glob-top dispensing dam and encapsulant are assumed to be 10 seconds per chip.
- Equipment required by both techniques is not shown.

by both of these technologies is not shown. Also, all equipment is assumed to be utilized 300 days a year, 24 hours a day, and its capacity is assumed to be 12 million chips per year. Each chip has 300 peripheral pads.

It can be seen from Table 2.2 that expensive pick and place + fluxing machinery is necessary for flip chip technology. Even though the wire bonder is cheaper, more wire bonders are needed because their throughput is much smaller (depending on the number of pads on a chip) than that of the pick and place machine (which performs gang-bonding on a chip). Consequently, the cost of major equipment for flip chip (\$2.7 million) is lower than that for wire bonding (\$4.79 million). Also, the manufacturing floor space required for flip chip should be smaller.

It should be noted that if the number of pads per chip is doubled to 600, then 70 wire bonders are needed and the cost of equipment is even higher. On the other hand, if the pads per chip are reduced to only 30, then 4 wire bonders are more than enough to do the job, and in this case the equipment for wire bonding technology is much cheaper than that for flip chip technology. Thus, flip chip technology is cost effective if the pin count and density of the IC devices are high.

2.2.3 Cost of materials

As mentioned earlier, the largest cost differences between wire bonding and flip chip are materials and IC chip yields. The labor/operation costs for these two assembly processes are assumed to be the same.

The wafer. The physically possible number of undamaged chips (N_c) stepped from a wafer (Fig. 2.10) may be given by

$$N_c = \pi \frac{[\phi - (1 + \theta)\sqrt{A/\theta}]^2}{4A} \quad (2.1)$$

where

$$A = xy \quad (2.2)$$

and

$$\theta = \frac{x}{y} \geq 1 \quad (2.3)$$

In Eqs. 2.1 to 2.3, x and y are the dimensions of a rectangular chip (mm) with x no less than y ; θ is the ratio between x and y ; ϕ is the wafer diameter (mm); and A is the area of the chip (mm²). For example, for a 200-mm wafer with $A = 10 \times 10 = 100$ mm², then $N_c = 255$ chips.

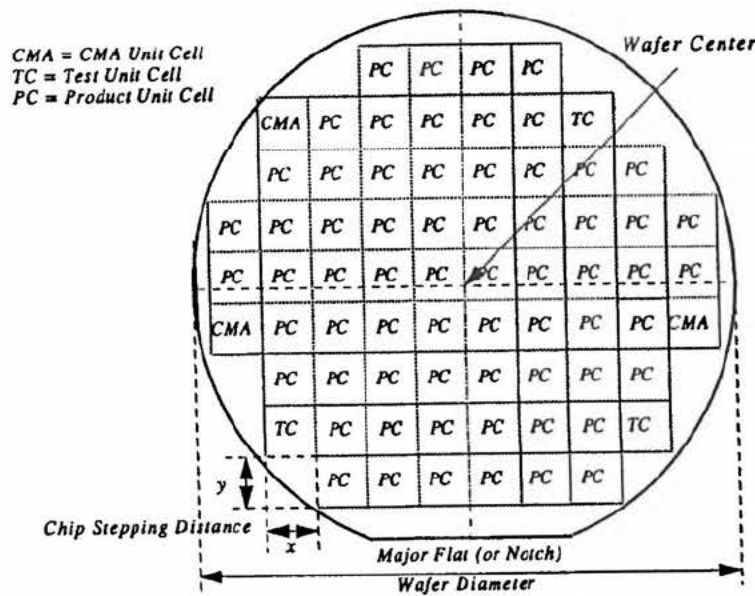


Figure 2.10 Diagram of a wafer.

For a given chip size, the physically possible number of pads (N_p) depends on the pad pitch (p) and pad configuration. The N_p on a chip surface is given as follows.

For area-array pads:

$$N_p = \left(\frac{x}{p} - 1\right) \left(\frac{y}{p} - 1\right) \quad (2.4)$$

For peripheral-array pads:

$$N_p = 2 \left(\frac{x}{p} - 1\right) + 2 \left(\frac{y}{p} - 1\right) \quad (2.5)$$

For peripheral-staggered-array pads:

$$N_p = 4 \left(\frac{x}{p} - 1\right) + 4 \left(\frac{y}{p} - 1\right) - 4 \quad (2.6)$$

For example, for a chip with $x = 10$ mm, $y = 8$ mm, and $p = 0.25$ mm, $N_p = 1209$ area-array pads, $N_p = 140$ peripheral-array pads, and $N_p = 276$ peripheral-staggered-array pads. Obviously, area array is the choice for high-density IC and packaging.

Cost per wafer for wafer bumping. Wafer bumping is the heart of solder-bumped flip chip technology. The cost of wafer bumping is affected by the true yield (Y_T) of the IC chips, the wafer-bumping yield (Y_B), and the good die cost (C_D). The actual wafer-bumping cost per wafer (C_B) is:

$$C_B = C_{WB} + (1 - Y_B)Y_T N_c C_D \quad (2.7a)$$

where C_B is the actual wafer-bumping cost per wafer, C_{WB} is the wafer-bumping cost per wafer (ranging from \$25 to \$250), Y_B is the wafer-bumping yield per wafer, C_D is the good die cost (not the cost of an individual die on the wafer), N_c is given in Eq. 2.1, and Y_T is the true IC chip yield after at-speed/burn-in system tests. It can be seen that the actual wafer-bumping cost per wafer depends not only on the wafer-bumping cost per wafer but also on the true IC chip yield per wafer, wafer-bumping yield per wafer, and good die cost.

Wafer-bumping yield (Y_B) plays a very important role in wafer bumping. The wafer-bumping yield loss ($1 - Y_B$) could be due to (1) incorrect processes, (2) different materials, (3) bump heights that are too tall or short, (5) not enough shear strength, (6) solder bridging, (7) broken wafer or dies, (8) damaged bumps, (9) missing bumps, and (10) scratching of the wafer. It should be noted that solder bumps are not reworkable. The process has to be done right the first time; otherwise, someone has to pay for it!

For example, if the die size of a 200-mm wafer is 100 mm^2 ($N_c = 255$), true IC chip yield per wafer is 80 percent, wafer-bumping yield per wafer is 90 percent, wafer-bumping cost per wafer is \$200, and good die cost is \$100 (e.g., microprocessors), then the actual wafer-bumping cost per wafer is \$2240. For the same size wafer, if the good die cost is \$1 (e.g., memory devices), then the actual wafer-bumping cost per wafer is \$220.40. On the other hand, if the wafer-bumping yield is increased from 90 percent to 99 percent, then the actual cost for bumping the microprocessor wafer is \$404 and the actual cost for bumping the memory wafer is \$202.04. Thus, wafer-bumping yield plays an important role in the cost of wafer bumping and the wafer-bumping operations should strive to make Y_B greater than 99 percent, especially for expensive good dies.

Cost per good die for wafer bumping. The wafer-bumping cost per good die ($C_{B/D}$) can be determined by

$$C_{B/D} = \frac{C_B}{Y_T N_c} \quad (2.7b)$$

Figure 2.11 shows the wafer-bumping cost per good die ($C_{B/D}$) for various Y_T values for the 200-mm wafer. It can be seen that $C_{B/D}$ increases as Y_T decreases. Also, it can be shown from Eqs. 2.1 and 2.7 that if the

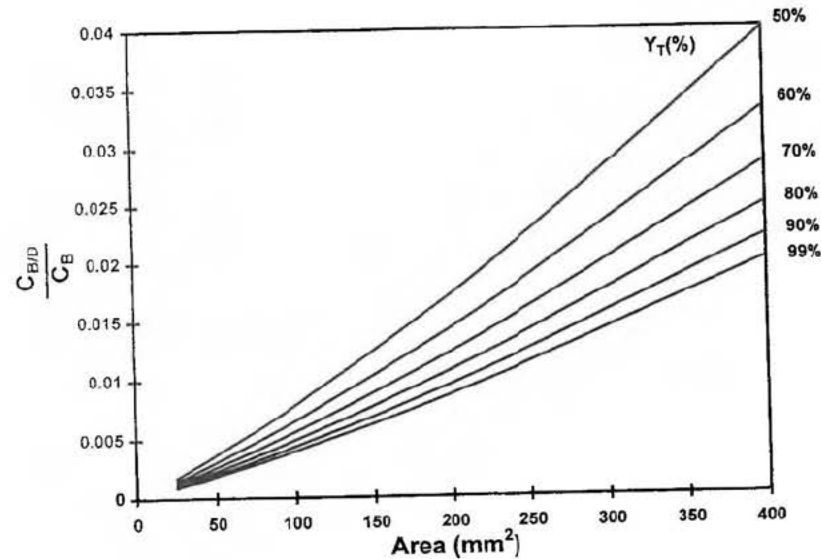


Figure 2.11 Wafer-bumping cost per die (200-mm wafer).

wafer-bumping cost (C_{WB}) of the 200-mm wafer is no more than 2 times of that of the 150-mm wafer, then the wafer-bumping cost per good die is cheaper for the larger wafer (assuming Y_B , Y_T , and good die cost are the same for both wafers). Finally, for example, for a 200-mm wafer with $A = 100 \text{ mm}^2$, $N_c \approx 255$. Assuming $C_{WB} = \$100$ and $Y_B = 100$ percent, then $C_{B/D} = \$0.44$ if $Y_T = 0.9$ and $C_{B/D} = \$0.65$ if $Y_T = 0.6$. Thus Y_T plays an important role in wafer bumping. Unless it is mandated for reasons of density, form factor, and/or performance, solder-bumped flip chip technology is not suitable for very low-yield devices.

Cost per pad on a good die for wafer bumping. The wafer-bumping cost per pad ($C_{B/P}$) on a good die can be determined by

$$C_{B/P} = \frac{C_B}{Y_T N_c N_p} \quad (2.8)$$

where N_c is given in Eq. 2.1, N_p is given in Eqs. 2.4, 2.5, or 2.6, C_B is the actual wafer-bumping cost, and Y_T is the true IC chip yield.

Figure 2.12 shows the $C_{B/P}$ for the 200-mm wafer with peripheral-area-array pads. It can be seen that $C_{B/P}$ depends on the chip size, pad pitch, C_B (C_{WB} , Y_B , C_D), and Y_T . The larger the chip size, the higher the $C_{B/P}$, and the larger the pad pitch, the higher the $C_{B/P}$. Also, $C_{B/P}$ is

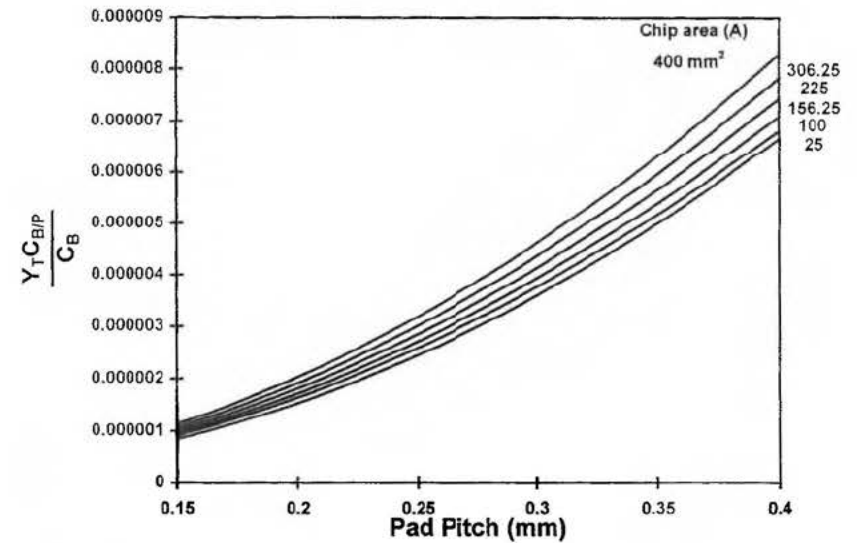


Figure 2.12 Wafer-bumping cost per pad (200-mm wafer with area-array pads).

cheaper for the 200-mm wafer if the C_B of the larger wafer is no more than twice of that of the smaller wafers.

Consider a 200-mm wafer with $A = 10 \times 10 = 100 \text{ mm}^2$ and $p = 0.25 \text{ mm}$. Assuming $C_B = C_{WB} = \$200$ ($Y_B = 100\%$) and $Y_T = 0.9$, then $C_{B/P} = \$0.00057$ for area-array pads, $C_{B/P} = \$0.00559$ for peripheral-array pads, and $C_{B/P} = \$0.00283$ for peripheral-staggered-array pads. It can be seen that the cost savings for chips with area-array pads is very compelling.

Cost per die for wire bonding. The wire-bonding cost per die ($C_{W/D}$) can be determined by

$$C_{W/D} = \frac{Y_I L_A C_W N_p}{Y_T} \quad (2.9)$$

where C_W is the wire cost (Table 2.3), L_A is the average wire length per pad, Y_I is the initial screening IC chip yield (after 1-MHz screening test), Y_T is the true IC chip yield, and N_p is given by either Eq. 2.5 or Eq. 2.6.

Figure 2.13 shows the $C_{W/D}$ for the chips with peripheral-array pads ($x = y$ has been assumed). It can be seen that $C_{W/D}$ decreases with pad pitch increase and chip size decrease.

TABLE 2.3 Cost of Gold Wire (September 1998)

Diameter (inch)	1,000 (ft)	5,000 (ft)	10,000 (ft)	25,000 (ft)
0.0007	\$485.00/LOT	\$143.70/Kft	\$ 93.70/Kft	\$ 60.00/Kft
0.001	\$375.00/LOT	\$135.30/Kft	\$ 96.50/Kft	\$ 70.30/Kft
0.0015	\$410.00/LOT	\$192.10/Kft	\$149.70/Kft	\$121.10/Kft

99.99 percent gold wire (spool: 2 inch).

Consider a chip with $x = 10$ mm, $y = 8$ mm, and $p = 0.25$ mm. Assuming $L_A = 4.572$ mm, $C_W = \$70.30/\text{Kft} = \$0.00023/\text{mm}$, $Y_I = 0.9$, and $Y_T = 0.6$, then $C_{W/D} = \$0.22$ for peripheral-array pads and $C_{W/D} = \$0.44$ for peripheral-staggered-array pads. If $Y_I = 0.7$ and $Y_T = 0.6$, then $C_{W/D} = \$0.17$ for peripheral-array pads and $C_{W/D} = \$0.34$ for peripheral-staggered-array pads. It can be seen that for wire-bonding technology it is desirable to have $Y_I \rightarrow Y_T$. Otherwise, the expensive gold wire will be bonded on the bad dies.

Cost per pad for wire bonding. The wire-bonding cost per pad ($C_{W/P}$) can be determined by

$$C_{W/P} = \frac{Y_I L_A C_W}{Y_T} \quad (2.10)$$

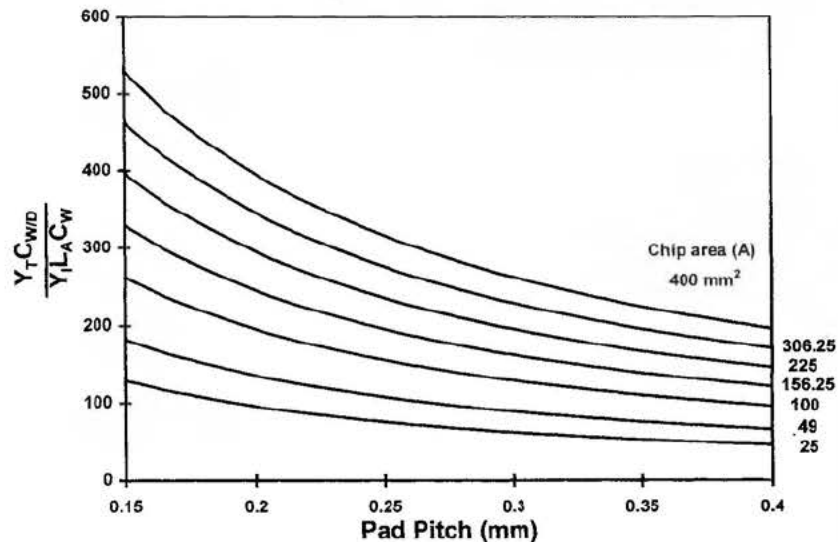


Figure 2.13 Wire bonding cost per die (wafer with peripheral-array pads).

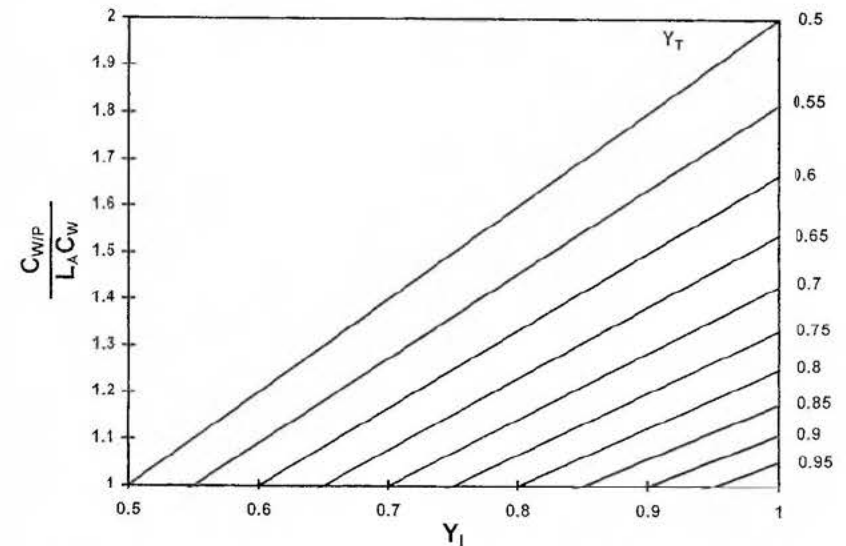


Figure 2.14 Wire bonding cost per pad.

Equation 2.10 is shown in Fig. 2.14 with various values of Y_I and Y_T . It can be seen that the higher the Y_T , the lower the $C_{W/P}$. Also, for a given Y_T , the $C_{W/P}$ increases with a higher Y_I . For example, consider a 200-mm wafer with $A = 100 \text{ mm}^2$ and $p = 0.25$ mm. Assuming $L_A = 4.572$ mm and $C_W = \$0.000231/\text{mm}$, then $C_{W/P} = \$0.001115$ if $Y_T = 0.9$ and $Y_I = 0.95$, and $C_{W/P} = \$0.001056$ if $Y_I = Y_T = 0.9$. By comparing this example with that in the section on wafer-bumping cost per good die, it can be seen that $C_{W/P}$ is smaller than $C_{B/P}$. However, flip chip technology provides the possibility for area-array pads, and in this case $C_{B/P}$ is a few times smaller than $C_{W/P}$.

Cost comparison. The cost ratio (β) between the wafer-bumping cost per die (Eq. 2.7) or pad (Eq. 2.8) and the wire-bonding cost per die (Eq. 2.9) or pad (Eq. 2.10) is given by

$$\beta = \frac{C_B}{Y_I L_A C_W N_p N_c} \quad (2.11)$$

Equation 2.11 is plotted in Fig. 2.15 for the 200-mm wafer with peripheral-array pads. It can be seen that β is larger for larger chip size and larger pad pitch. Also, β is larger for smaller Y_I . When $\beta \geq 1$, this means the costs of solder-bumped flip chip are no less than those of wire bonding.

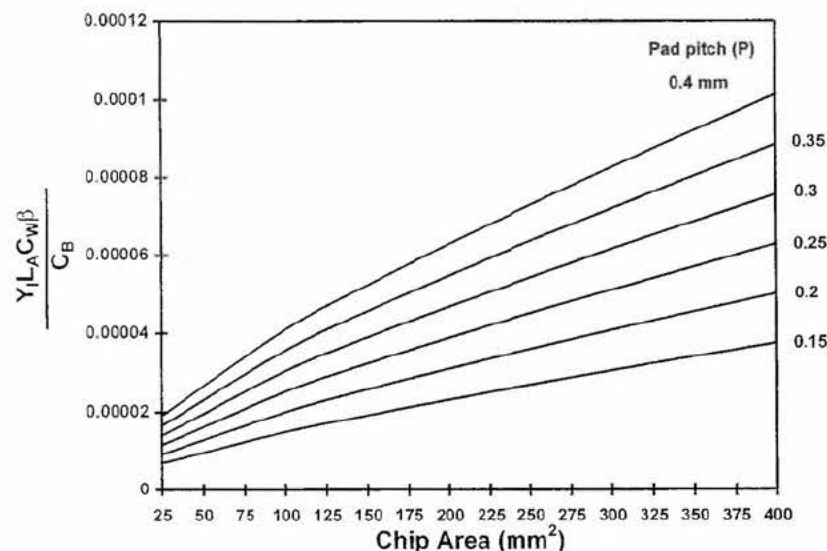


Figure 2.15 Cost ratio between wafer-bumping cost per pad and wire bonding cost per pad (200-mm wafer with peripheral-array pads).

For a 200-mm wafer with $x = y = 10$ mm and $p = 0.25$ mm on a peripheral-staggered-array pad configuration, assuming that $L_A = 4.572$ mm, $C_W = \$0.00023/\text{mm}$, $C_B = C_{W/B} = \$100$ ($Y_B = 1$), and $Y_I = 0.9$, then $\beta = 1.35$. This means that from materials, labor, and operation points of view, flip chip technology is more expensive than wire-bonding technology. It should be remembered that the major equipment cost for wire bonding is higher than that for flip chip (1.77 times). Thus, flip chip is still cheaper. If we reduce the pitch to $p = 0.16$ mm and keep everything else the same, then $\beta = 0.85$. That means flip chip is cheaper, even without counting on the major equipment cost advantage. However, for the peripheral-array pad configuration, wire bonding is cheaper.

If we reduce the chip size to $x = y = 5$ mm, then $\beta = 0.63$ for $p = 0.25$ mm on peripheral-staggered-array pads and $\beta = 0.39$ for $p = 0.16$ mm on peripheral-staggered-array pads. Thus, in this case, flip chip is cheaper even with peripheral-array pads. It should be pointed out, as shown in the section on wafer-bumping cost per die, that flip chip could be even cheaper if the area-array pad configuration is used. Unfortunately, it cannot be compared with wire bonding, since the latter cannot use area-array pads.

2.2.4 Summary

The cost analysis for wire-bonding chip and solder-bumped flip chip on board or on a PBGA substrate has been presented. Useful equations for determining the wafer-bumping and wire-bonding costs per die and per pad have also been provided. Furthermore, useful charts relating the important variables such as the wafer size, IC chip yields, wafer-bumping yield, chip dimensions, and costs are provided for engineering practice convenience. Some important results are summarized in the following list.

- The major equipment cost of wire bonding is higher than that of flip chip.
- Wire bonding occupies more manufacturing floor space than flip chip does.
- Wafer-bumping cost per die increases as Y_T decreases.
- Wafer-bumping cost per die is cheaper for larger wafers.
- Wafer-bumping cost per pad is higher for larger chip sizes.
- Wafer-bumping cost per pad is higher for larger pad pitches.
- Wafer-bumping cost per pad is cheaper for larger wafers.
- Wafer-bumping cost per pad is very low for area-array chips.
- Wire-bonding cost per die decreases as pad pitch increases.
- Wire-bonding cost per die decreases as chip size decreases.
- Wire-bonding cost per pad increases with higher ratios of Y_I and Y_T .
- Area-array solder-bumped flip chip is cheaper than wire bonding.
- For peripheral-array chip, wire bonding is cheaper than flip chip if the chip size and pad pitch are very large. Otherwise, flip chip is cheaper.
- In order for solder-bumped flip chip to be cost competitive with wire bonding, the wafer-bumping yield should be higher than 99 percent, especially for high-cost dies.
- For low-yield dies, actual wafer-bumping cost may be too high for flip chip applications, unless it is compensated for by performance, density, and form factor.

2.3 Wafer Bumping with Solders

Wafer bumping is the heart of solder-bumped flip chip technology. Today, there are many different ways to put the tiny solder bump (usu-

ally no larger than 100 μm) on the wafer. In this chapter, only the 12 best-known methods are discussed.

The most important task in wafer bumping is to put down the ball-limiting metallurgy (BLM) or under-bump metallurgy (UBM) on the aluminum pads of the wafer. Some of the UBMs for different bump materials are shown in Table 2.4. The UBM defines the region of terminal metallurgy on the top surface of the chip that is wetted by the solder.

2.3.1 Evaporation method

The most mature wafer-bumping method is evaporation, which has been perfected by IBM for more than 30 years. A detailed description of this method is beyond the scope of this book; interested readers are encouraged to read Refs. 20 to 46. However, some of the most important features of this method are briefly described in the following paragraphs.

Figure 2.16 shows the evaporation process. It can be seen that it requires two metal masks, as shown in Fig. 2.17. These masks are made of molybdenum, whose thermal coefficient of expansion is very close to that of silicon. Also, molybdenum has excellent long-term dimensional stability at high temperatures. The first metal mask with smaller openings is for the deposition through evaporation of the UBM (chrome/copper/gold), as shown in Fig. 2.18. The second metal mask with larger openings is for the deposition through evaporation of the

TABLE 2.4 Some Well-Known UBMs for Gold, Copper, Aluminum, Solder, and Nickel Bumps

Bump	UBM	Process
Gold	Cr-Cu	Electroplating
	Ti-Pd	Electroplating
	Ti-W	Electroplating
	Ti-Pt	Electroplating
Copper	Cr-Cu	Electroplating
	Al-Ni	Electroplating
Aluminum	Ti	Evaporating
	Cr	Evaporating
Solder	Cr-Cu-Au	Evaporating/printing
	Ni-Cu	Electroplating/printing
	Ti-Cu	Electroplating/printing
	TiW-Cu	Electroplating/printing
	Ni-Au	Electroless + printing
	Al-NiV-Cu	Sputtering + printing
Nickel	Ni	Electroless Ni/Au

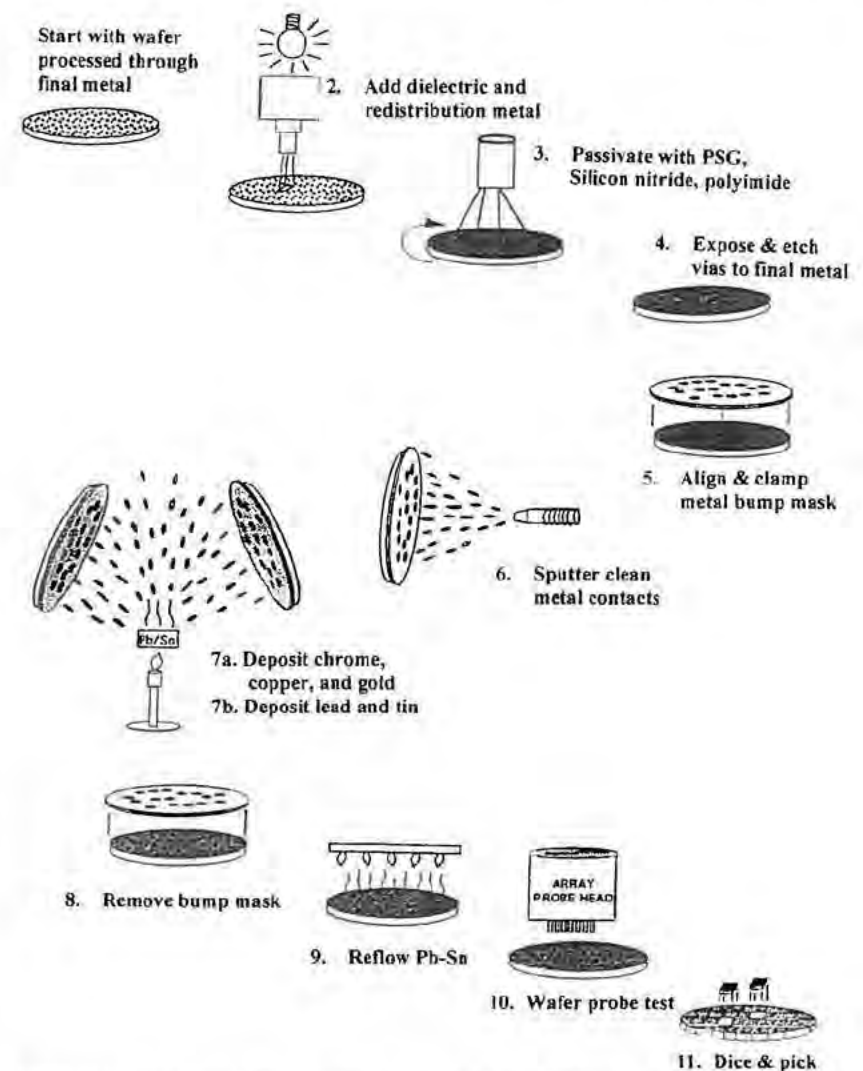


Figure 2.16 IBM's well-known evaporation wafer-bumping process.

lead-tin solder. After reflow, nice-looking truncated spherical solder bumps can be obtained, as shown in Fig. 2.17. Evaporation bumping is a dry solder buildup process.

It should be noted that because the evaporation rate of the Pb is higher than that of the Sn, this method is usually applied to high-Pb solder bumps such as the 95wt%Pb-5wt%Sn and 97wt%Pb-3wt%Sn.

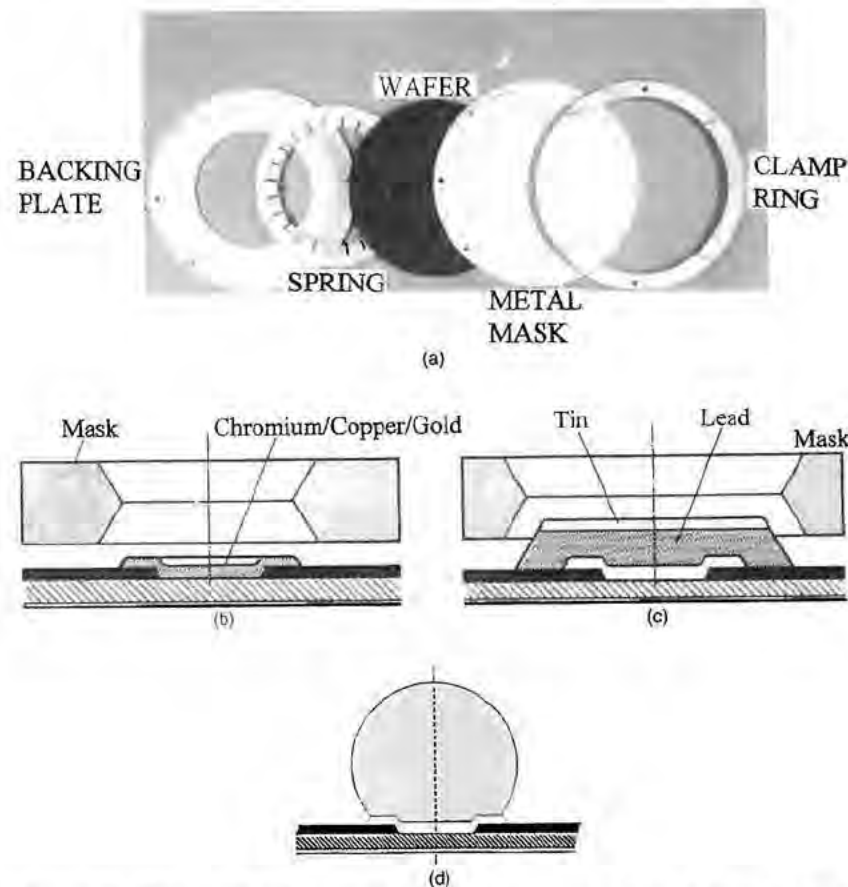


Figure 2.17 Metal mask technology. (a) Tooling for alignment of mask to wafer. (b) Masking and evaporation of chromium/copper/gold. (c) Masking and evaporation of lead and tin. (d) Reflowed solder bump.

IBM calls these controlled collapse chip connection (C4) bumps. Since two metal masks and the evaporation process are needed, this method could be expensive.

Recently, Motorola developed an E-3 (evaporated extended eutectic) wafer-bumping process⁴⁷ that also uses the evaporation method. It creates a bump with a mostly "pure" Pb column and a small amount of pure Sn at the tip. It is not reflowed prior to die attachment. Since unreflowed Pb is very soft, shipping of these bumps poses a great challenge. Interested readers are encouraged to read Chap. 6 of Lau and Pao.⁵

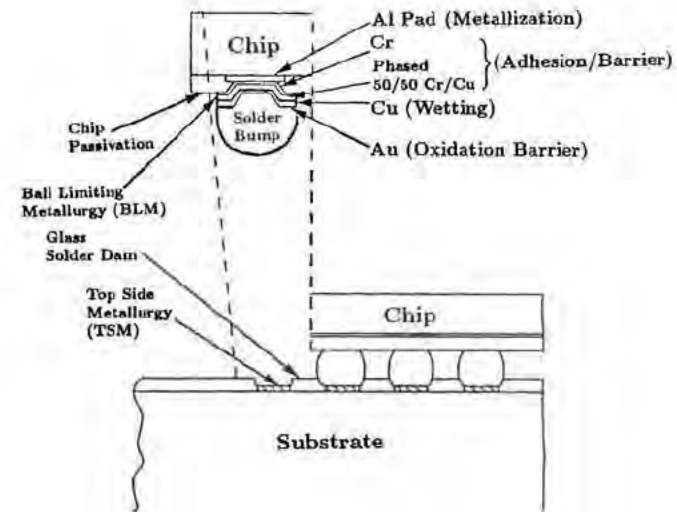


Figure 2.18 IBM's well-known Cr-Cu-Au UBM.

2.3.2 Electroplating method^{5,8}

The second most mature method in wafer bumping is electroplating, which is considered a wet solder buildup process. Figure 2.19 shows the bumping process. The most common UBM with electroplating method is either Ti-Cu or TiW-Cu. They are sputtered over the entire surface of the wafer—0.1 to 0.2 μm of Ti or TiW first, followed by 0.3 to 0.8 μm of Cu. A 40- μm layer of resist is then overlaid on the Ti-Cu or TiW-Cu and a solder bump mask is used to define the bump pattern as shown in Fig. 2.19. The openings in the resist are 7 to 10 μm wider than the pad openings in the passivation layer. A 6- to 25- μm layer of Cu is then plated over the UBM, followed by electroplating Sn-Pb solder in any combination. This is done by applying a static or pulsed current through the plating bath with the wafer as the cathode. In order to plate enough solder to achieve a final solder ball height of 100 μm , the solder is plated over the resist coating by about 15 μm to form a mushroom shape. The resist is then removed and the Ti/Cu or TiW/Cu is stripped off with a hydrogen peroxide etch. The wafer is then reflowed, which creates smooth truncated spherical solder bumps due to surface tension.

This method is very popular today because it can plate solders in any combinations, such as the 63wt%Sn-37wt%Pb eutectic solder. One of the drawbacks is bump height nonuniformity. Usually, due to the

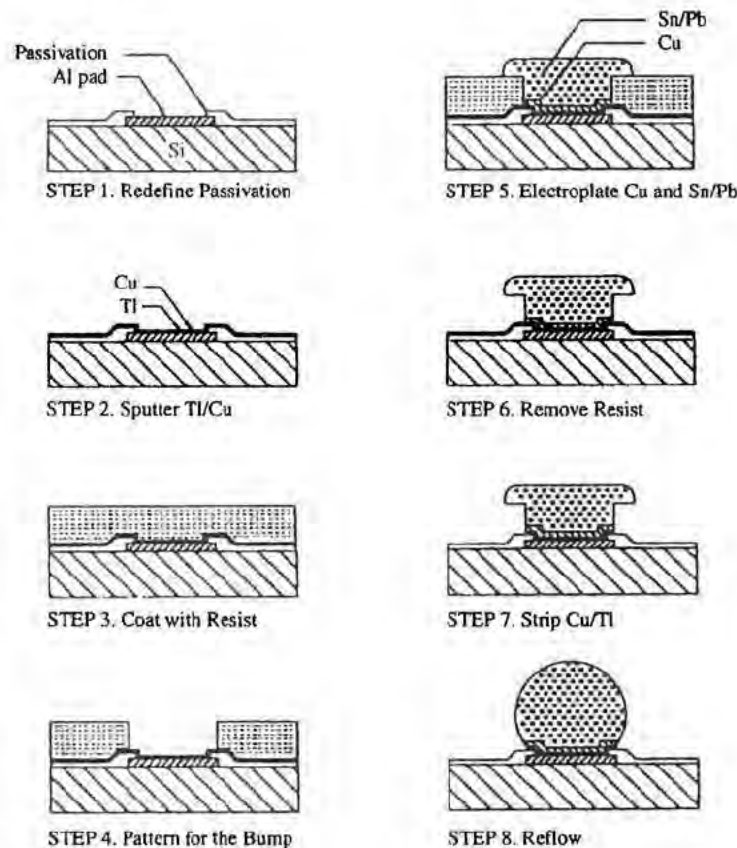


Figure 2.19 Electroplated solder wafer-bumping process.

applied electrical current at the boundary of the wafer, i.e., current density variations across the wafer during the electroplating process, the solder bumps near the edge of the wafer are taller than those near the center of the wafer. (For experimental data, please see pages 233 to 248 of Lau and Pao.⁵) The other drawback is plating time (1 to 2 min/ μm). This method is cheaper than the evaporation method, since only one bump mask is needed and the process is simpler.

2.3.3 Under-bump metallurgy (UBM)

One of the key reasons why solder-bumped flip chip technology is not commonly used today is because of the high cost of wafer bumping.

Thus, in the past few years many new and potentially low-cost wafer-bumping methods have been proposed. Almost all of these methods require a UBM: the most common are Ni-Au and Al-NiV-Cu. Since the latter has been discussed in Chap. 31 of Lau and Lee,³ in this section only the Ni-Au UBM is discussed.

The key process in making the Ni-Au UBM is shown in Fig. 2.20. It can be seen that it is a zincate process and very simple. After the wafer is cleaned, it is put into the zincate solution for less than 3 min and then rinsed in deionized (DI) water. (Very often, double-zincating is performed.) Then the wafer is put into the Ni solution for electroless plating (8 to 10 percent NiP, 85°C for 12 to 15 min) to about 5 μm thick, rinsed in DI water, immersed into the gold solution (80°C for 10 min), and then rinsed again in DI water. The function of this very thin Au layer is to prevent the Ni from oxidizing and prolong the wafer solderable shelf life. Figure 2.21 shows the Ni-Au UBM on a silicon chip.⁴⁶

The quality and uniformity of electroless Ni-Au UBM depend on the careful monitoring of each process step and the tight contamination control (every 2 h) of the zincate, Ni, and Au solution tanks. The Al-Ni adhesion and electrical resistance at the interface are strongly affected by the cleaning and activation processes.

The advantages of the Ni-Au UBM are: (1) its costs are low, (2) it is compatible with eutectic solders, (3) it has high solder wettability, (4) Al-

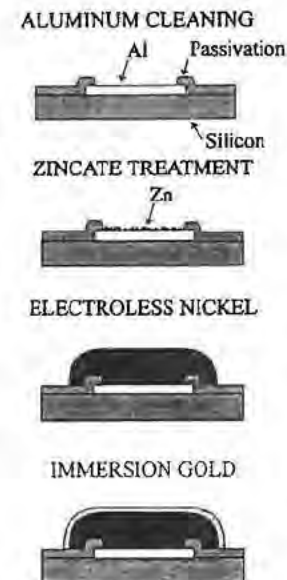


Figure 2.20 Schematic of the electroless Ni-Au bumping process (not to scale).

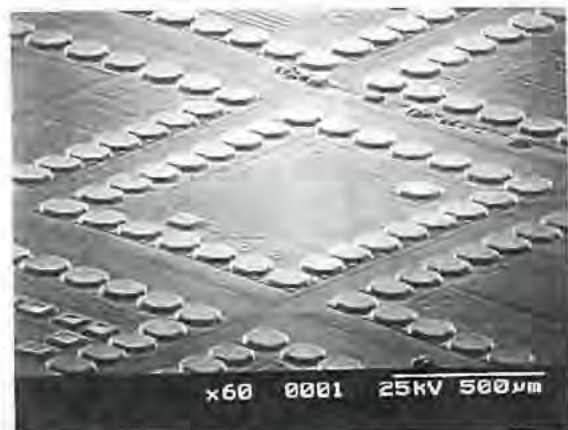


Figure 2.21 SEM photo of electroless Ni-Au UBM about 5 μm thick.

Ni adhesion is more than adequate for SMT, and (5) Ni-Sn intermetallic growth is adequate for solder thermal fatigue life.

It should be emphasized that since all the potential low-cost wafer-bumping methods discussed in Secs. 2.3.4 through 2.3.12 require UBM, logistics and infrastructure become big factors in the cost picture. Usually, truly low cost can be achieved if and only if the wafer bumpers also do UBM and at the same site. Otherwise, there would be many hidden costs.

2.3.4 Stencil printing method⁴⁹⁻⁵³

Wafer bumping by the stencil printing method is not only potentially low in cost but is also welcomed by system manufacturers, because stencil printing of solder paste is one of their most important steps in SMT. The only limitation is the very fine pitch of the pads on the chip. Today, stencil printing solder paste on the wafer in volume production is limited to 150 μm .⁴⁹

Figure 2.22 shows the key process steps for stencil printing solder paste on the wafer.^{50, 51} The first step is to put down the electroless Ni-Au UBM on the Al pads as shown in Figs. 2.23a and b.⁵² The second step is to stencil print the 63Sn-37Pb solder paste onto the UBM as shown in Fig. 2.23c⁵² and Figs. 2.24a and b. Figure 2.24b is the Ishikawa cause-and-effect (fishbone) diagram for solder paste printing. It can be seen that there are eight major categories (operator, environment, printing

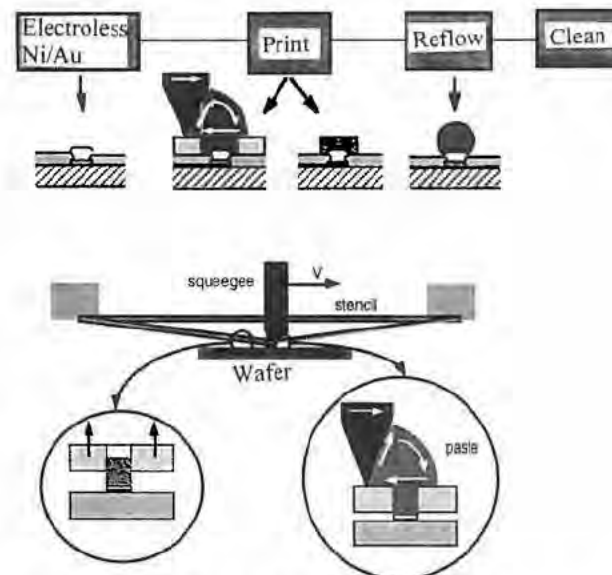


Figure 2.22 Wafer bumping by stencil printing paste process steps.

parameter, printer, stencil, wafer, squeegee, and solder paste) that influence the quality of solder paste printing on wafer. This diagram helps us to sort out the potential causes for solder paste printing defects and to organize the causes into defined categories to yield high-quality solder paste printing.

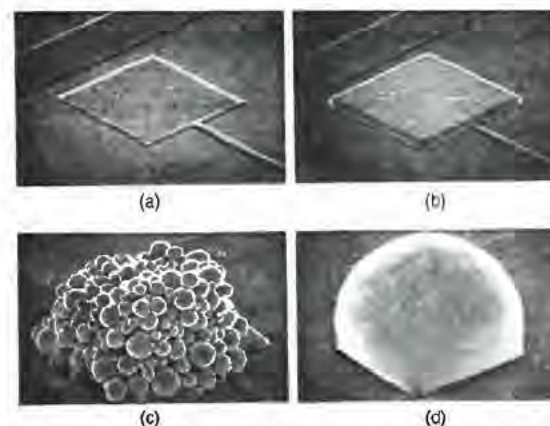


Figure 2.23 SEM photos of wafer bumping by stencil printing method. (a) Al pad; (b) 5- μm Ni-Au UBM; (c) solder paste; (d) reflowed bump.

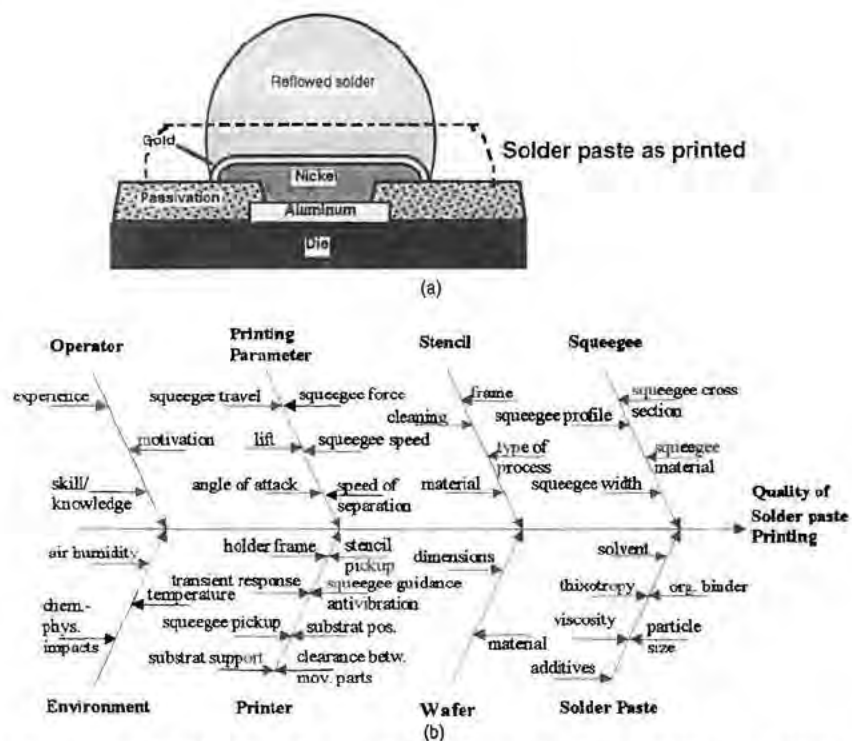


Figure 2.24 (a) Solder bump by stencil printing paste method. (b) Ishikawa (fishbone) diagram for quality solder paste printing.

The next step is to reflow the solder paste on the wafer into nice-looking solder bumps, as shown in Figs. 2.23d and 2.24a. Finally, the wafer is cleaned with DI water (Fig. 2.25). Some typical cross sections are shown in Figs. 2.26a and b.⁵⁰ It can be seen that they are very good-looking solder bumps. Also, the Ni-Au UBM looks very good. Energy dispersive spectrum (EDS) results obtained by Li et al.⁵⁰ show that a thin Ni-Sn intermetallic layer is formed at the solder-UBM interface. Also, these solder bumps are almost free of voids and have good wetting on the Ni-Au UBM.

The shear strength of the stencil printed solder bumps under certain reflow and aging conditions is also measured by Motorola and is shown in Fig. 2.27. It can be seen that there is no shear strength degradation even after 1000 h of storage at 150°C and 85°C/85% relative humidity (RH) of samples reflowed 11 times.

Figure 2.28a shows a solder bump on a Ni-Au UBM chip. The solder volume (V) of the truncated sphere solder bump with diameter = $2R$,

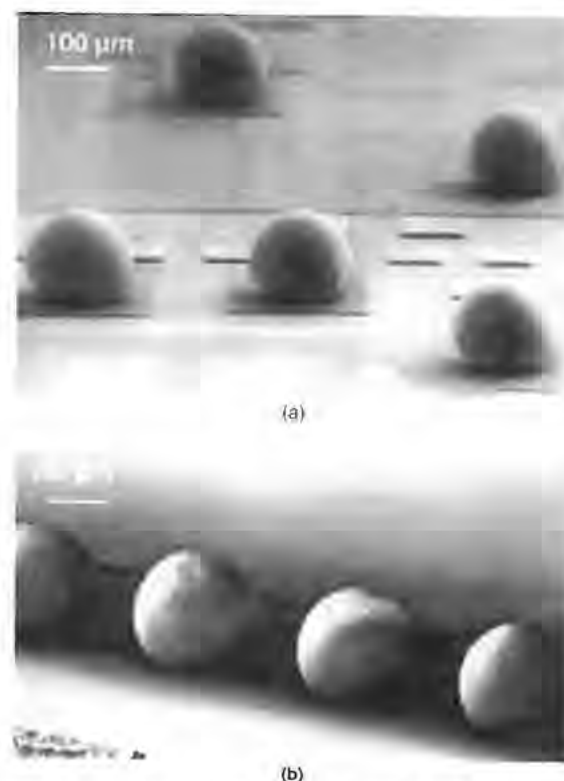
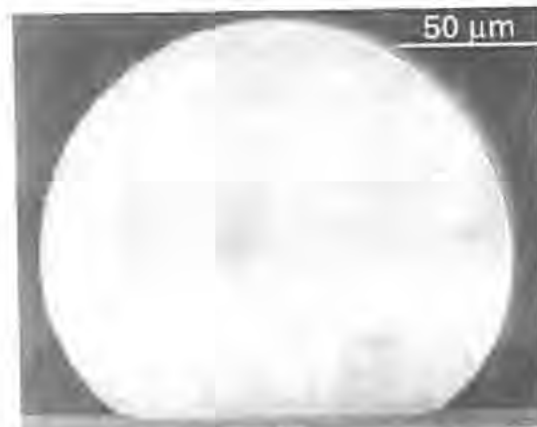


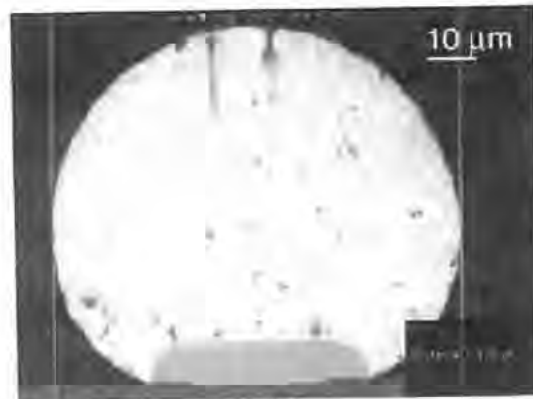
Figure 2.25 Stencil-printed solder bumps after reflow and cleaning. (a) Reflowed bumps on a 300-μm pitch device. (b) Solder bumps on a 200-μm pitch device.

based on the UBM diameter (D) and bump height (H), can be estimated with good accuracy by the equation shown in Fig. 2.28a.⁵⁰ If the wetting angle (θ) is known, then the solder volume (V) of a solder bump with height (H), radius (R), and UBM diameter (ϕ) can be obtained from the equation in Fig. 2.28b.⁵³

Figures 2.29a to c show the cross sections of untested DCA on Cu-Ni-Au PCB. These assemblies are subjected to the qualification test conditions shown in Table 2.5. All the requirements are met by Motorola. Figures 2.30a and b show the cross sections of the failure sample (liquid-to-liquid test for -55 to +125) at 1500 cycles. It can be seen that the delamination between the underfill and solder mask causes the solder joint cracks. (Also see Figs. 2.31a to c.)



(a)



(b)

Figure 2.26 Solder bump cross sections for different pitch devices. (a) 300- μ m pitch device, (b) 200- μ m pitch device.

In order to achieve a successful stencil printing method for wafer bumping, two things must be noted—the paste material and the stencil. The rheology of solder paste is critical for sufficient paste deposit without bridges. Active rosin flux containing halides should be avoided. Paste containing chemical components that create difficult-to-remove residues should not be used. The type 4 paste is adequate for stencil printing on wafer bumping even though the finer-mesh type 5 and type 6 pastes deposit more consistent solder volume. However, the latter two pastes are not commonly available at reasonable cost.

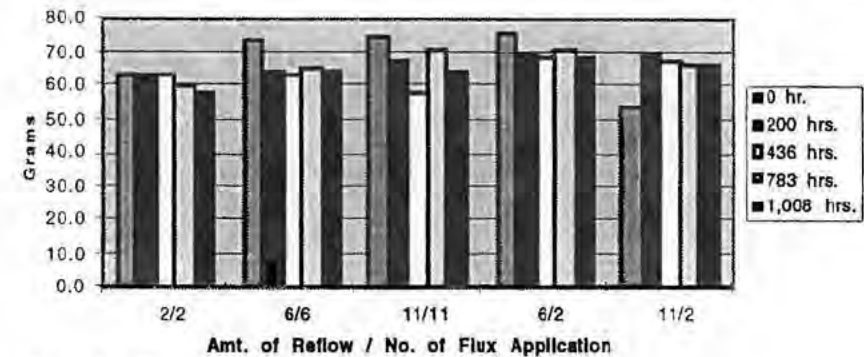


Figure 2.27 Bump shear force after 85°C/85% RH aging.

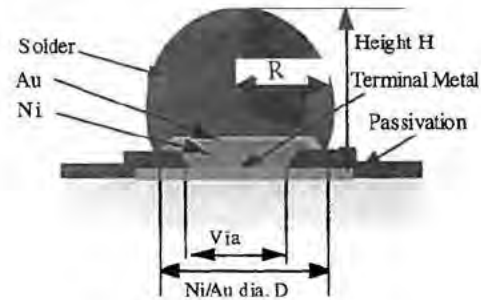
The electroformed stencil is better than the chemical-etched and laser-cut stencils. Although the chemical-etched stencils are cheaper, because of accuracy and dimension limitations they cannot meet the fine-pitch wafer-bumping requirement. Although the laser-cut stencils are accurate, the sequential processing could make costs prohibitive for wafer bumping.

2.3.5 Solder jet printing method⁵⁴⁻⁵⁶

The schematic of a demand-mode ink-jet printing system, also called solder jet technology, developed by MicroFab Technologies, Inc. is shown in Fig. 2.32.⁵⁴⁻⁵⁶ Solder jet technology is based on piezoelectric demand-mode ink-jet printing technology⁵⁴⁻⁵⁹ and is capable of producing and placing molten solder droplets 25 to 125 μ m in diameter at rates of up to 2000 per second.

In demand-mode ink-jet printing systems, a volumetric change in the fluid is induced either by the displacement of a piezoelectric material that is coupled to the fluid or by the formation of a vapor bubble in the ink caused by heating a resistive element. This volumetric change causes pressure transients to occur in the fluid, and these are directed so as to produce a drop that issues from an orifice. A droplet is created only when it is desired in demand-mode systems. Demand-mode ink-jet printing systems produce droplets that are approximately equal to the orifice diameter of the droplet generator.

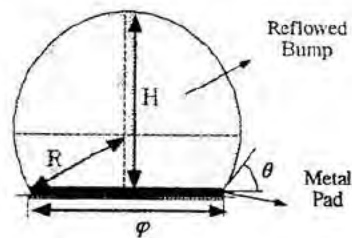
The droplet generator is incorporated into a printhead design suitable for integration into a prototype platform. Key features of the printhead include: (1) a heated inert environment localized to the tip of



$$V = \pi / 6 \times H \times (H^2 + 3(D/2)^2)$$

$$\text{Bump diameter } 2R = (D^2 + H^2) / H$$

(a)



$$V = (\pi/24) \times \phi^3 \times \{[(\cos \theta + 1) \times (2 - \cos \theta)] / [\sin \theta \times (1 - \cos \theta)]\}$$

$$H = R + R \cos \theta = [\phi \times (1 + \cos \theta)] / 2 \sin \theta$$

(b)

the droplet generator and impact area of the substrate, (2) separate heaters for the solder reservoir and droplet generator, (3) vertical dispensing capability, and (4) the ability to deposit solder droplets while the printhead is in motion.

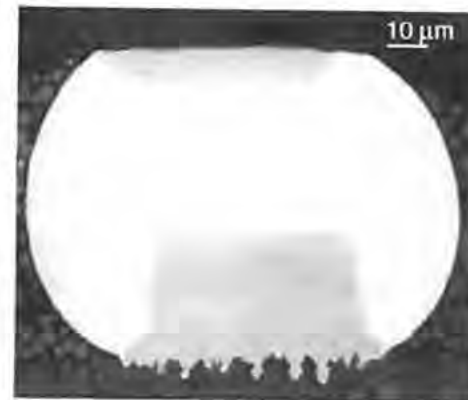
The solder jet printhead has been integrated with Universal Instruments to build the solder jet research platforms (Fig. 2.33a) that have been delivered to many companies to demonstrate fundamental capabilities in the positioning and deposition of solder droplets and to perform initial process development experiments. Figure 2.33b shows the Drop-on-Demand Metal Jet™ developed by MPM and MicroFab Technologies, Inc. Figures 2.34a and b show the solder bumps as jetted and after reflow. It can be seen that the 100-μm solder bumps look very good. The UBM on the Al pads of these chips is electroless Ni-Au, as



(a)



(b)



(c)

Figure 2.29 Cross-sectional views of solder bump assembly. (a) Overview of the assembly cross section. (b) Bump assembly cross section for the 300-μm pitch device. (c) Bump assembly cross section for the 200-μm pitch device.

TABLE 2.5 Reliability Evaluation Test Requirements

Test	Condition
Operating life	408 hr, 150°C
Power temperature cycle	1000 c, -40/+125°C
Temperature cycle	1000 c, -40/+150°C
High-temperature bake	1000 hr, 150°C
Temperature cycle	1000 c, -55/+125°C
Temperature shock	1000 c, -55/+125°C
Temperature/ humidity bias	1008 hr, 85°C/85%RH 15-V bias output pins

shown in Fig. 2.34c. The shear test results (based on the test conditions recommended on pages 239 to 241 in Lau and Pao⁶) obtained by MPM is about 35 g. The failure mode is shear fracture in the solder bump and not near the UBM, as shown in Fig. 2.34d.

2.3.6 Fly-through solder jet printing method⁶⁰

As discussed in the previous section, the drop-on-demand (DOD) solder jet technology utilizes the DOD solder ball generators along with relatively high-frequency mechanical positioning. In this section, another approach called fly-through solder joint printing (also called Continuous Stream Metal Jet™) as shown in Figs. 2.35a and b and Fig. 2.36 is presented by Rapid Analysis and Development Co. and MPM Corp. The essential components are as follows.⁶⁰

- *Solder ball generator and integrated stream angular control system:* produces uniform droplets from a constant-speed capillary stream with well-controlled breakup times relative to the disturbance waveform applied to the stream to initiate breakup. The stream from which the droplets are formed originates from a nozzle placed precisely at the center of rotation of a spherical angular control system that is used to remotely adjust the angular orientation of the system with no translational motion of the stream's origin.
- *Pressure control system:* maintains a constant effective driving pressure for the stream.
- *Charging system:* accomplishes accurate and repeatable droplet charging by means of a charging electrode and inductive charging prior to and during droplet separation from the capillary stream.



(a)



(b)

Figure 2.30 Liquid-to-liquid temperature cycling (-55 to +125°C), failed at 1500 cycles. (a) Overview of the interconnect failure modes. (b) Close-up view of the solder joint failure mode.

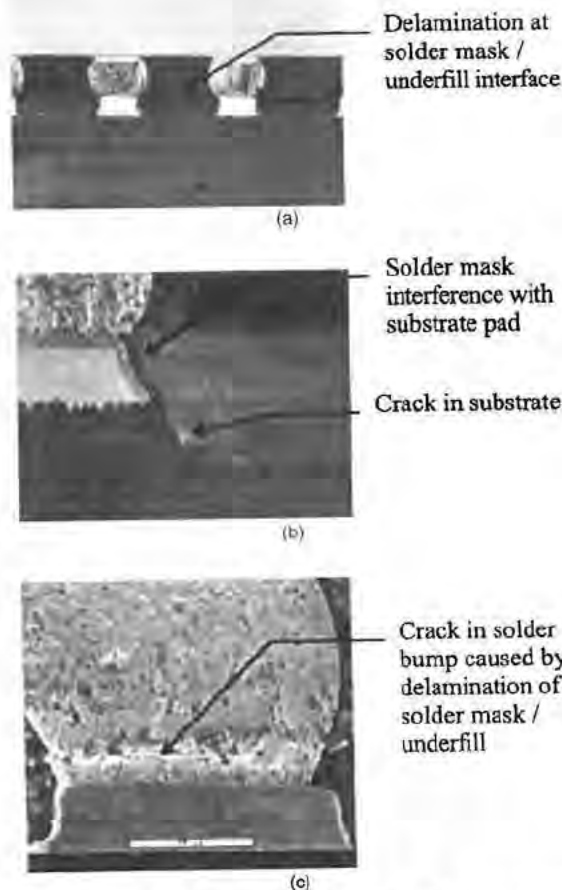


Figure 2.31 (a) Delamination between solder mask and underfill. (b) Cracks in substrate and between solder mask and underfill. (c) Cracks in solder joint.

- *Electrostatic deflection system:* permits control of the relative angular position of the plane defined by the deflected solder droplets relative to the traverse direction.
- *Environmental control system:* rejects oxygen from the vicinity of the capillary stream breakup and shields the solder droplets traveling to the target from oxygen and environmental flow disturbances; also shields the deposition sites from oxygen.

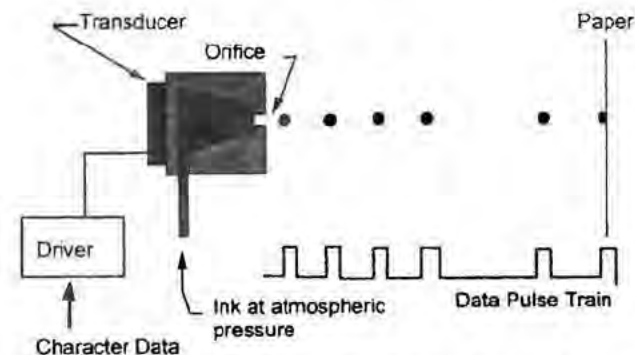


Figure 2.32 Schematic of a demand-mode ink-jet printing system.

- *Droplet stream positioning and deflection calibration system:* stream centering system permits accurate deflection calibration and null positioning of the droplet stream to a fixed home (undeflected) location.
- *Collection system:* collects solder droplets not used for printing.

Some successful printing using the system shown in Figs. 2.35 and 2.36 is demonstrated by the results in Fig. 2.37. It should be noted that the production machines for this technology have already been made. Right now, the Continuous Stream Metal Jet is up to 44,000 solder drops per second.

There are other solder jetting methods, such as the one demonstrated by Sandia National Laboratories⁶¹ and the one designed by IBM, known as micro dynamic solder pump (MDSP).⁶² However, these have not been made into commercial machines yet.

2.3.7 Micropunching method⁶³

Figure 2.38 schematically shows an overview of the micropunching mechanism developed by NEC.⁶³ The solder tape is supplied from a spool and rolled up by a motor-driven spool. A micropunch is driven by an electrical actuator and a displacement enlarging mechanism. A micropunch and die set blanks a thin solder tape and forms a small cylindrical piece. Figure 2.39 shows the punched solder pieces for four kinds of solder materials. Figure 2.40 shows the 95wt%Pb-5wt%Sn solder pieces that are punched by different diameters and thicknesses.

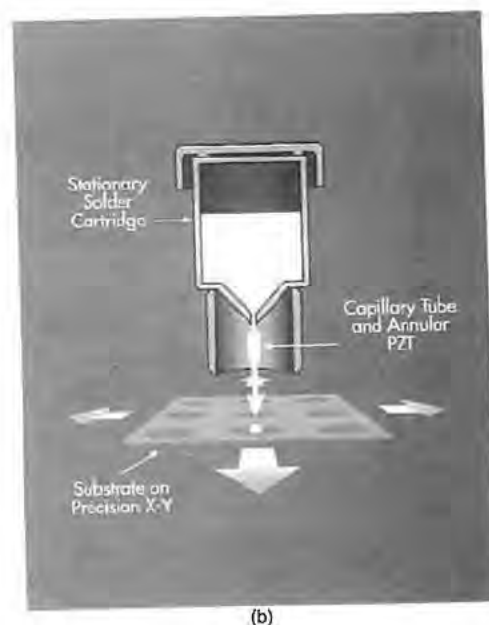
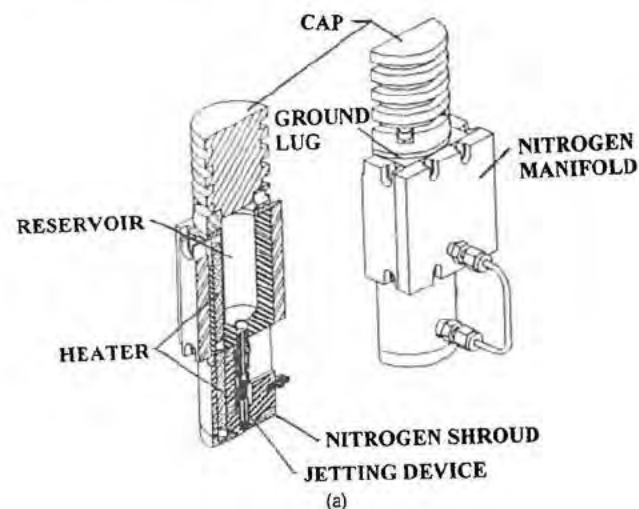
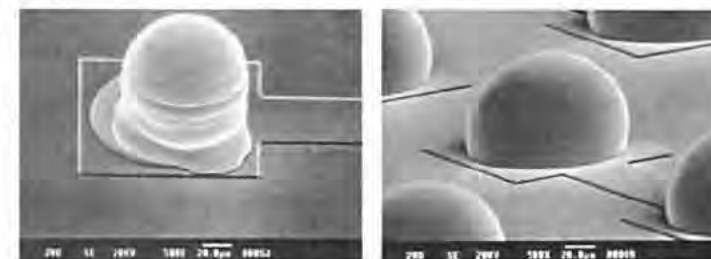


Figure 2.33 (a) Solder jet printhead employed on Universal Instruments' Solder Jet platforms. (b) Drop-on-Demand Metal Jet.



(a)



(b)



(c)



(d)

Figure 2.34 (a) SEM photo showing solder bumps as jetted and reflowed. (b) High-magnification views of as-jetted and reflowed bumps. (c) Cross section of a reflowed bump showing the UBM. (d) Sheared bump fractures (no failure at the UBM).

The characteristic of micropunching technology are as follows.⁶³

- The technology can be applied to various kinds of solders.
- Punching size diameter can be selected from 50 to 200 μm .
- The developed punching machine can create 10 bumps per second.
- The structure of the machine is simple and the price is low.
- Solder tape thickness should be less than punching diameter.

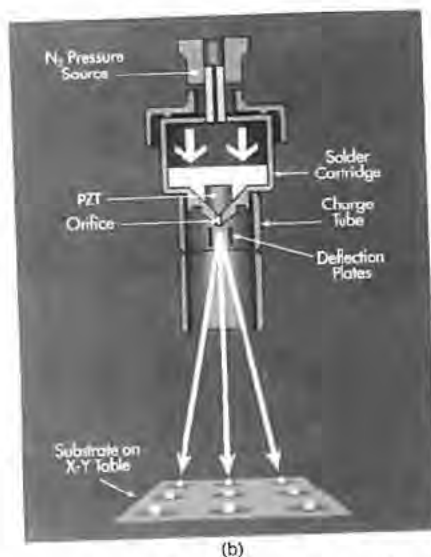
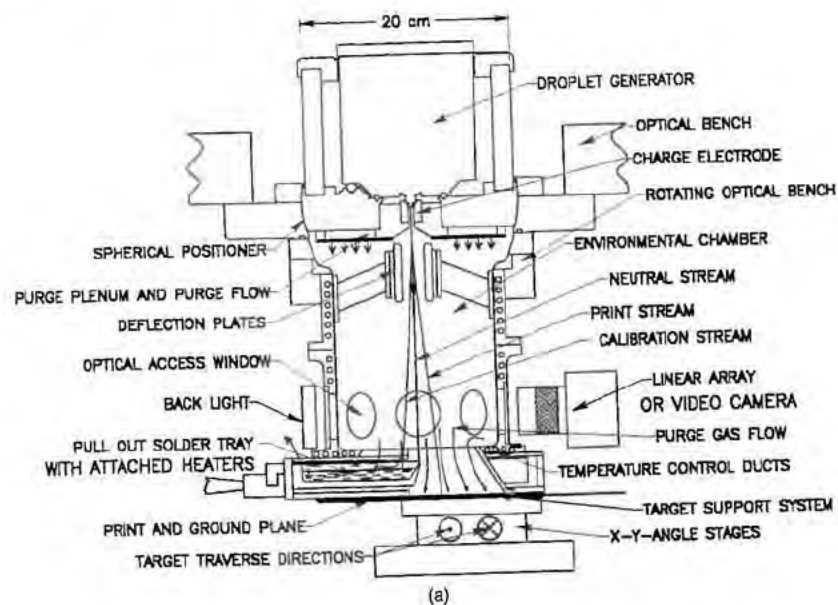


Figure 2.35 (a) Cross section of RAD fly-through printing system. (b) Continuous Stream Metal Jet.

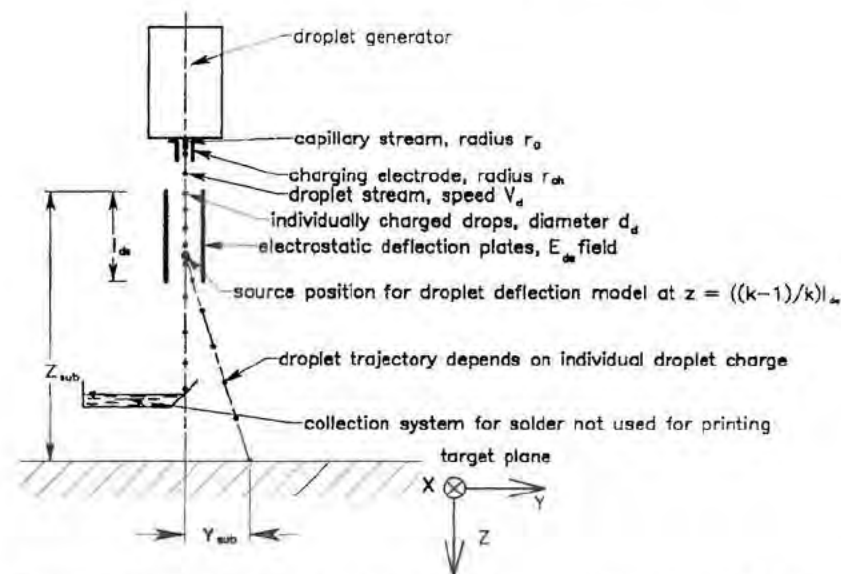


Figure 2.36 Illustration of fly-through printing with important nomenclature defined.

There are two different wafer-bumping processes for micropunch technology, namely the direct bump-forming method and the transferring bump-forming method. Figure 2.41 shows the direct bump-forming process. First, the flux is dispensed on the entire wafer. The solder pieces are punched and placed on the wafer directly. Then the whole wafer is reflowed and cleaned. Figure 2.42 shows the solder bumps on

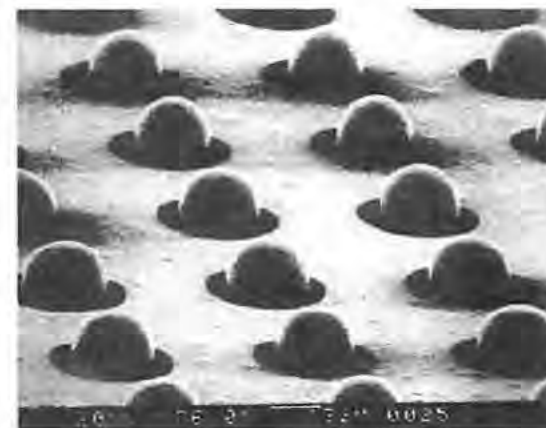


Figure 2.37 Examples from the fly-through printing system.

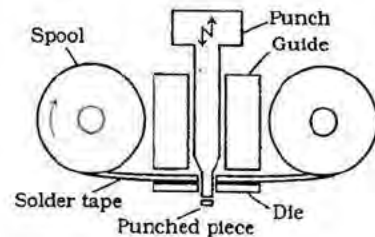


Figure 2.38 Overview of the micropunching system.

a wafer with different kinds of solders, sizes, and pad pitches. They look very good.

The micropunching technology by transferring bump-forming process is shown in Fig. 2.43. It can be seen that, instead of the solder pieces being punched on the wafer directly, they are placed on a temporary plate laminated with a special adhesive sheet that loses adhesion on heating (Fig. 2.44a). Then, the temporary plate is aligned with the fluxed wafer and a pressure (10 to 20 mN per bump) and a temperature ($<120^{\circ}\text{C}$) are applied to transfer the solder pieces to the wafer (Fig. 2.44b). Then the entire wafer is reflowed and cleaned (Fig. 2.44c).

The concept of the micropunching technology is very good. However, the infrastructure requirements for supplying the solder tape at a reasonable cost and the micropunching machine with the required accu-

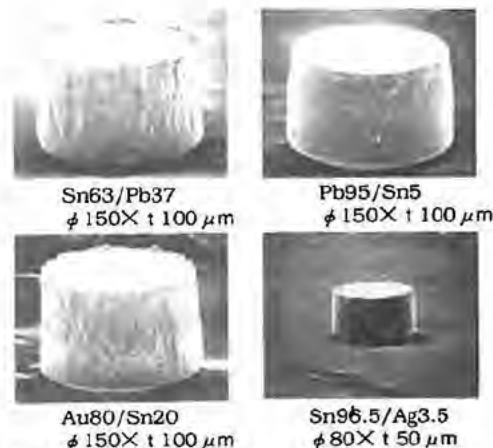


Figure 2.39 SEM photos of the punched solder pieces for four kinds of solders.

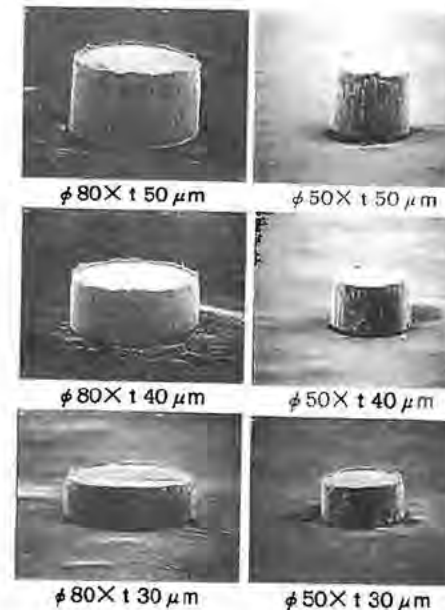


Figure 2.40 SEM photos of the 95Pb-5Sn solder pieces punched with different diameters and thicknesses.

racy are great challenges. Also, speed (10 bumps per second) could be an issue.

2.3.8 Molten solder injection method

At Yasu, Japan, IBM developed a wafer-bumping method that uses molten solder injection. Figure 2.45 shows the concept and operation pro-

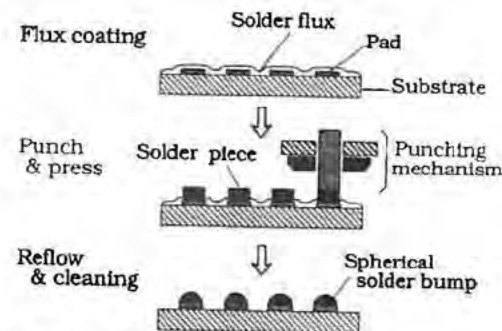


Figure 2.41 Direct solder bump-forming process.

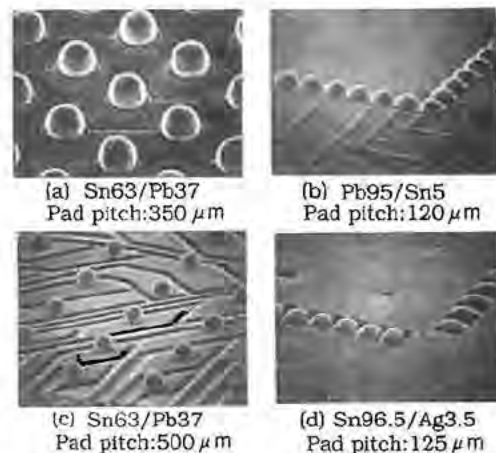


Figure 2.42 Solder bumps created by the direct solder bump-forming process.

cess. The head of this machine has a solder reservoir and a metal mask attached to its bottom. The mask has small holes whose pattern is the same as the pad pattern on the wafer. The head comes down to touch the wafer after the alignment is adjusted. When the reservoir is pressurized, the solder in the reservoir is squeezed out from the holes in the mask and

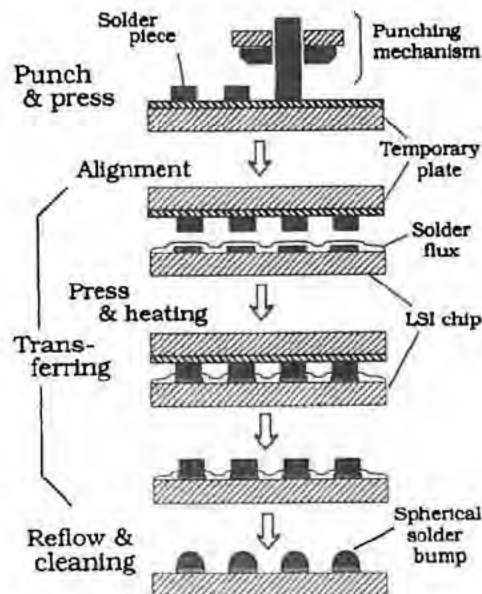


Figure 2.43 Transfer solder-bump forming process.

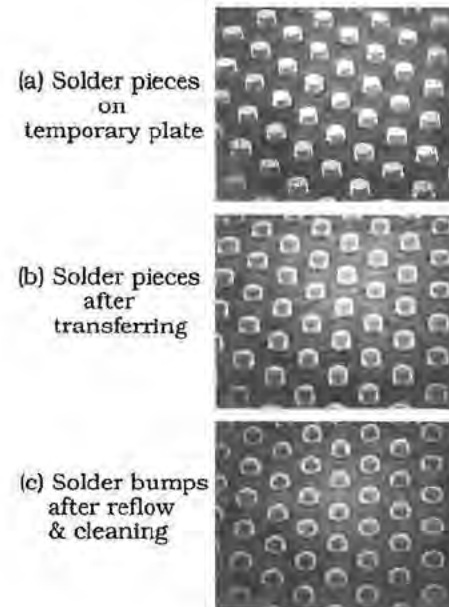


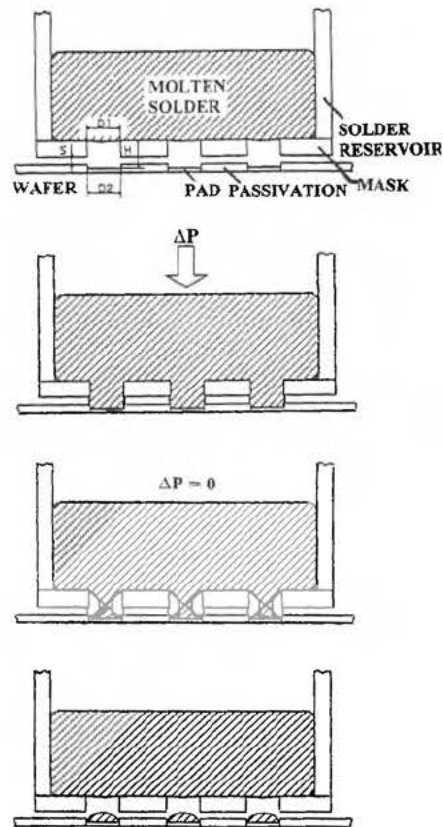
Figure 2.44 Solder bumps created by the transfer solder bump-forming process.

the solder touches the pad on the wafer. After the solder wets the pads, the increased pressure in the reservoir balances with the sum of the surface tensions of the depressed solder columns between the mask and wafer. When the pressure in the reservoir is released, the solder in the columns is pushed back into the holes by the surface tension of the molten solder itself. The solder columns are split when the condition reaches the limit to keep its form. The upper part is drawn back into the reservoir. The lower part remains on the pad and forms the solder bump. The solder bump volume is given by the equation shown in Fig. 2.45.

The concept is great. However, the pad pitch could be a limitation. It works well for 0.25-mm-pitch wafers.

2.3.9 SuperSolder method^{64,65}

The invention disclosure (No. 10941045) of low-cost solder-bumped flip chip application with SuperSolder was filed by the author with Hewlett-Packard in 1994. (The SuperSolder material is made by Furukawa Electric Co., Ltd.) Since then, Furukawa has matured it into a commercial product. SuperSolder (SS) technology works by chemically generating solder through a substitution reaction between tin and organolead salt. A paste composed of tin powder, organolead salt, and flux (SS paste) is heated, undergoing the reactions shown in Fig. 2.46.^{64,65}

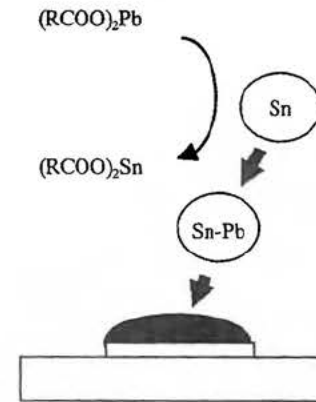


$V = \text{solder bump volume} = \pi H D_2^3 / 12 (D_1 + D_2)$
 $H = \text{height from Al-pad surface to upper surface of mask}$
 $D_1 = \text{diameter of mask opening}$
 $D_2 = \text{Al-pad diameter}$

Figure 2.45 Wafer bumping by IBM's molten solder injection process.

The application of SS for wafer bumping is shown in Fig. 2.47. It can be seen that the process steps are very simple. First, the SS paste is applied to the entire wafer or just the entire pad region. Stencils or masks are not needed since SS is not applied to individual pads. Then the whole wafer is heated and cleaned. The solder bump height is about 20 to 25 μm . Multiple SS paste applications are possible to reach the desirable bump height. However, this will increase manufacturing time and cost.

Figure 2.48 shows the secondary ion mass spectrometry (SIMS) measurement results of the oxidation near the solder bump surface using



- Step 1 Disassociation of organolead salt:
 $(\text{RCOO})_2\text{Pb} \rightarrow 2\text{RCOO}^- + \text{Pb}^{2+}$
 (heat)
- Step 2 Substitution of tin by lead:
 $\text{Pb}^{2+} + \text{Sn} \rightarrow \text{Pb} + \text{Sn}^{2+}$
 (heat)
- Step 3 Diffusion of deposited lead into metallic tin and alloying:
 $\text{Sn} + \text{Pb} \rightarrow \text{Sn-Pb alloy}$
 (heat)
- Step 4 Formation of organotin salt:
 $\text{Sn}^{2+} + 2\text{RCOO}^- \rightarrow (\text{RCOO})_2\text{Sn}$
 (cool)

Figure 2.46 SuperSolder process. A paste composed of tin powder, organolead salt, and flux (SS paste) is heated and undergoes the reaction steps.

the stencil printing, electroplating, and SS methods. It can be seen that the oxidation in SS solder bumps is lower than that in stencil printing and electroplating solder bumps. This is because in applying the SS technology, solder is melted and supplied within a reducing atmosphere. As a result, SS technology is ideal for forming solder bumps with optimal mountability. The solder supply volume (V) and the solder supply variation (ΔV) are given in Fig. 2.49. It can be seen that for the larger value of t in SS solder supply, the larger solder supply volume V can be attained; however, at the same time the solder supply variation ΔV also increases.

In order to avoid multiple applications of SS and still reach sufficient bump height, Furukawa and Motorola recommended increasing the

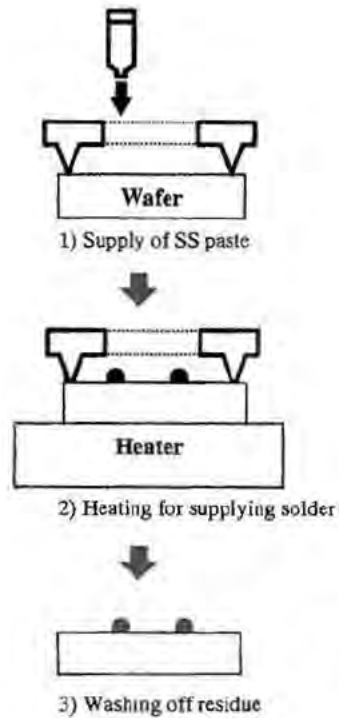


Figure 2.47 SuperSolder application steps.

electroless Ni-Au (5 μm) UBM to a 20- μm Ni-Au stud. (The diameter of the Ni-Au UBM is 113.5 μm .) In this case, with just one SS application, solder bump heights of 96 μm could be achieved (Figs. 2.50 and 2.51). It should be pointed out that for such a large Ni-Au stud, the passivation may crack (see Sec. 5.2.2 for more details). Right now, SS paste costs more than the ordinary pastes.

In order to make high-lead solder bumps, such as the C4 bumps, SMT compatible, a 63Sn-37Pb eutectic cap can be made using SS technology (Fig. 2.52). Figure 2.53 shows a cross section of a C4 bump with eutectic cap made by Hewlett-Packard in the 1994 invention disclosure with the SuperSolder provided by Furukawa.

2.3.10 Microball mounting method^{66, 67}

Solder ball mounting on PBGA package⁷ and CSP^{8, 6} substrates has been used for 10 and 6 yr, respectively. The ball sizes range from 0.3 to 0.76 mm. In recent years, micro gold (Fig. 2.54) and solder balls are becoming available. In this section, a production method for the micro solder balls

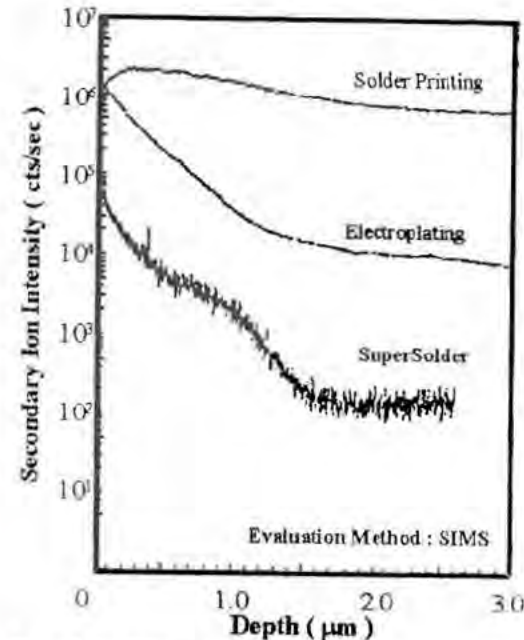
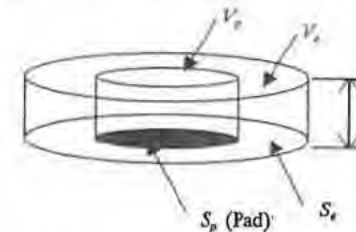


Figure 2.48 Oxidation near the solder surface.

and a gang-bonding method for forming the solder bumps on individual chips or wafers developed by Nippon Steel Corporation^{66, 67} are presented.

The micro solder balls are made by melting metal pieces previously prepared to a constant weight. The extremely uniform diameters and high sphericity are achieved by controlling the weight of the pieces pre-



$$V = V_p + x \cdot V_s = t \cdot S_p + x \cdot (t \cdot S_s)$$

$$\begin{aligned} \Delta V &= V_{\text{net}} - V_{\text{in}} \\ &= \{t \cdot S_p + (x + \Delta x) \cdot (t \cdot S_s)\} - \{t \cdot S_p + (x - \Delta x) \cdot (t \cdot S_s)\} \\ &= 2 \cdot \Delta x \cdot t \cdot S_s \end{aligned}$$

where $0 \leq x \pm \Delta x \leq 1$

Figure 2.49 SuperSolder supply volume model.

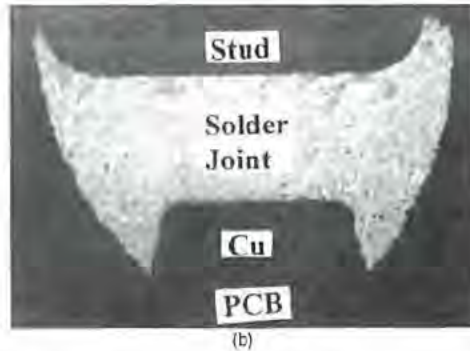
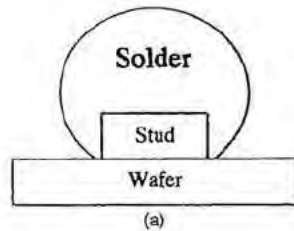


Figure 2.50 (a) Wafer with Ni-Au stud and SuperSolder. (b) Wafer assembled on PCB.

cisely and by using the surface tension of the molten metals. Micro solder balls 35 to 100 μm in diameter can be made for any solder composition, such as ternary, lead-free, and eutectic solder alloys. Figure 2.55 shows the ball size distribution of micro solder balls 100 μm in diameter.

The process of assembling the micro solder balls on a chip or wafer is shown in Fig. 2.56. It can be seen that the micro solder balls are sucked

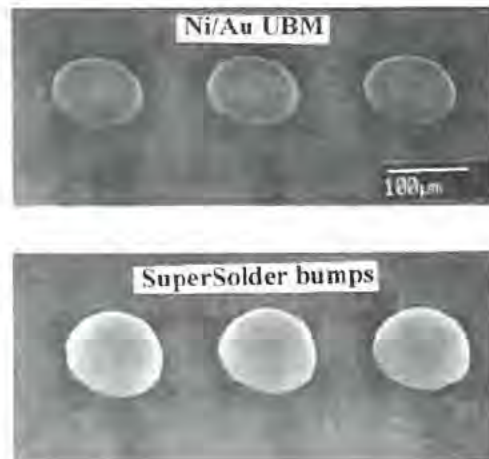


Figure 2.51 Examples of Ni-Au UBM and SuperSolder bumps.

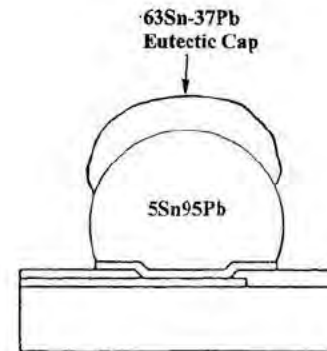


Figure 2.52 Schematic of high melt bump with eutectic cap.

onto through-holes in the arrangement plate by reducing the pressure on the other side of the plate. The through-holes are located at positions corresponding to those of the pads of the individual chip or wafer. It is possible to form bumps on a variety of chips or wafers by selecting this arrangement plate fixed on the bonding head. These arranged balls are transferred to the pads on the chip or wafer in order to form the solder bumps.

The detailed micro solder ball arrangement and transferring process is shown in Fig. 2.56: (a) bouncing the micro solder balls uniformly in the ball container by vibration; (b) lowering the bonding head with the arrangement plate toward the container and arranging the micro solder balls at the positions of the through-holes by means of vacuum suc-

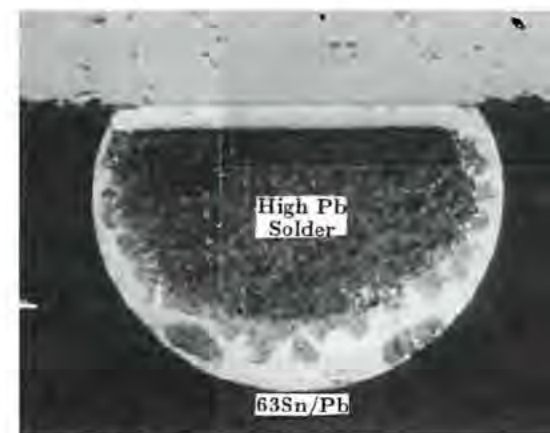


Figure 2.53 Cross section of a eutectic capped C4 solder bump with SuperSolder.



Figure 2.54 SEM image of micro gold balls (45 μm in diameter).

tion; (c) removing the excess balls adhered to the arranged balls or to the plate by vibrating the bonding head at a small amplitude; (d) inspecting the arrangement of the balls; (e) aligning the position of the balls with that of the pads on the chip or wafer; (f) transferring the balls onto the pads.

It is noted that the micro solder balls tend to adhere to each other due to (1) van der Waals forces; (2) surface adsorption of water; (3) electrostatic force; and (4) surface contamination. In order to resolve these issues, Nippon Steel Corporation has developed a micro solder ball mounter (for individual chips only), which is schematically shown in Fig. 2.57. Unique features of this mounter are the system to eliminate excess balls, the ball bouncing system, and the inspection CCD camera system. The complete process flow of micro solder bumping is shown in Fig. 2.58.

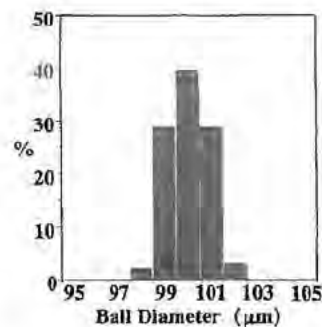


Figure 2.55 Ball size distribution of micro solder balls 100 μm in diameter.

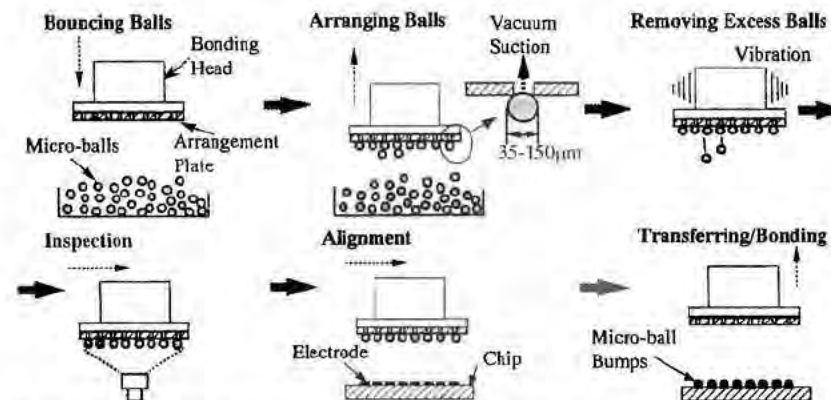


Figure 2.56 Flow chart of the microball arranging and transferring process.

Figure 2.59 shows the solder bumps, bump height distribution, and shear strength distribution of the solder bumps on a chip with 2025 pads on a 220- μm pitch. (The initial micro solder ball diameter is 150 μm .) It can be seen that the solder bumps, bump heights, and shear strengths are very uniform. Figure 2.60 shows the solder bumps on a chip with 200 pads on a 140- μm pitch. (The initial micro solder ball diameter is 80 μm .)

A high-speed automatic microball mounter for wafer bumping on a chip in a wafer is under development. Nippon Steel Corporation estimates that the cycle time should be less than 10 s for a chip in a wafer. The cost picture for micro solder ball bumping is not clear at this moment.

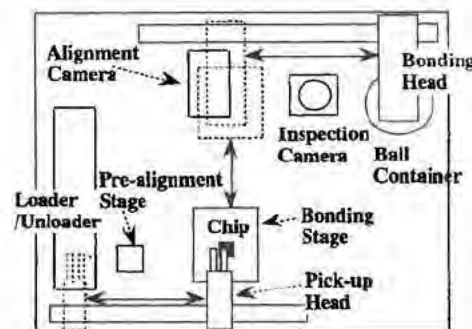


Figure 2.57 Schematic diagram of microball mounter.

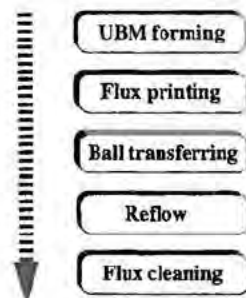
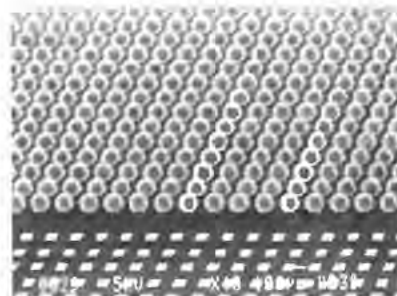


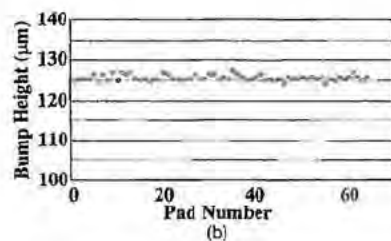
Figure 2.58 Process flow of micro solder bumping.

2.3.11 Tacky Dots™ method

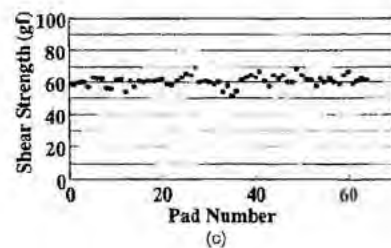
The Tacky Dot™ film is a DuPont® invention⁶⁸ produced by coating a proprietary photopolymer adhesive between a polyimide (Kapton®) carrier film and a Mylar® cover sheet. Texas Instruments (TI) joined with DuPont to codevelop Tacky Dots^{69, 70} because of its perceived



(a)



(b)



(c)

Figure 2.59 (a) SEM image, (b) bump height distribution, and (c) shear strength distribution of area-arrayed micro solder bumps (initial ball diameter: 150 μm ; number of bumps: $45 \times 45 = 2025$; bump pitch: 220 μm).



Figure 2.60 Micro solder bumps with 140- μm pitch (initial ball diameter: 80 μm ; number of bumps: 200).

advantages as a potential wafer bumping process: (1) compatibility with any metal alloy or thermoplastic composition; (2) independence from the applied UBM; (3) high throughput; (4) fine pitch; (5) cleanliness; and (6) potential low cost.

Tacky Dots is a proprietary technology system that incorporates a film of photoimageable adhesive coated on a support. The Tacky Dots assembly flow is shown in Fig. 2.61. The Tacky Dot film is imaged using

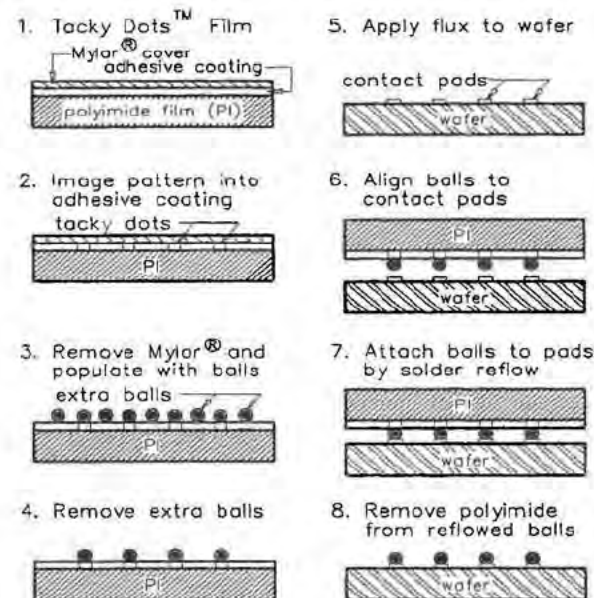


Figure 2.61 Tacky Dots™ for wafer bumping.

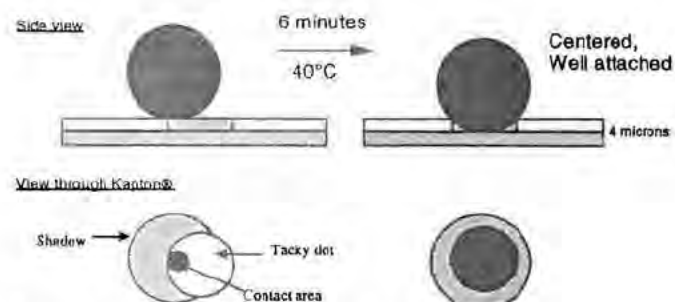


Figure 2.62 Self-centering of spheres in Tacky Dots.

a photo tool and ultraviolet (UV) light to form a pattern of Tacky Dots. The dot size is customized to hold only one particle per dot. For solder wafer bumping, the Tacky Dots are coated on Kapton and populated with conductive solder spheres of certified quality, using equipment to execute the process. The pattern, populated with the desired conductive composition, is aligned with a receiving substrate such as wafer, and the solder conductive particles are reflowed and transferred as solder bumps.

One of the important features of the Tacky Dots technology is that it is self-centering, i.e., the solder spheres are drawn to the center of the dot (Fig. 2.62). The dot size and coating thickness can be designed to perfectly match a solder sphere of a specific size.

Automated population can be accomplished by populating either single, discrete sheets or by populating discrete patterns sequentially on a continuous web. Figures 2.63 and 2.64 show, respectively, the basic elements of the fully automated population module for a single pattern of Tacky Dots mounted on a flex frame and for a roll of continuous film that has been preimagined with a sequential series of Tacky Dot patterns.

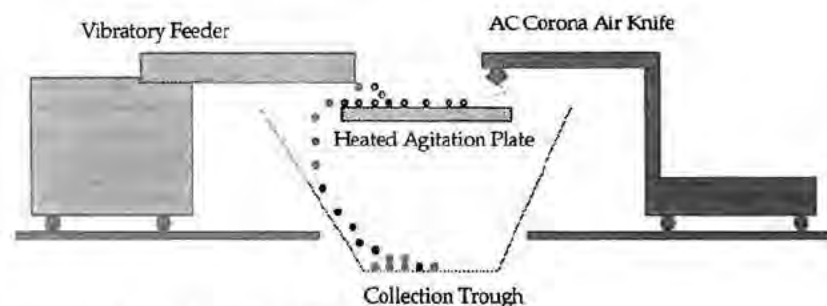


Figure 2.63 Basic elements of EPM-I population module.

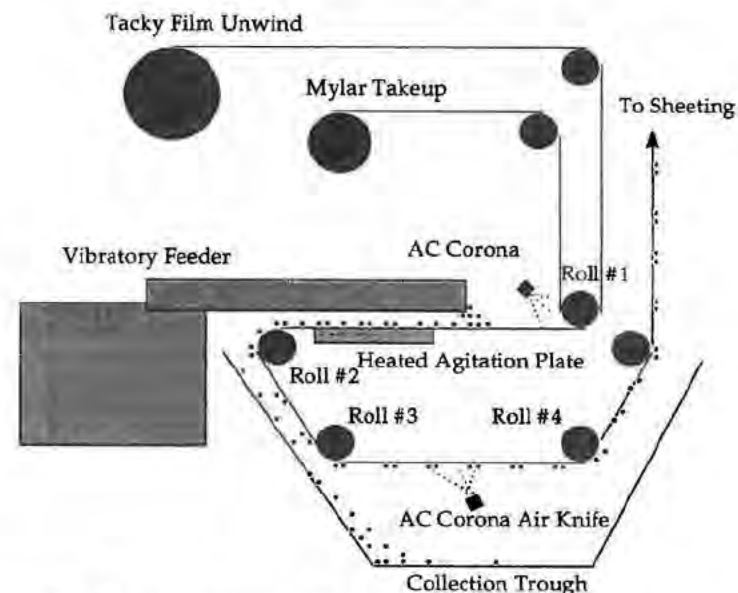


Figure 2.64 Basic elements of EPM-II population module.

The thermal coefficient of expansion for Tacky Dot Kapton film is on the order of 12 ppm/°C; that for silicon is about 2.5 ppm/°C. For 63Sn-37Pb solder and a 100-mm wafer, the Tacky Dot pattern is shrunk by 0.15 percent, allowing for the growth that will occur in the Kapton film going from 25 to 183°C. Thus, the room temperature alignment of the scaled Tacky Dot pattern is done so that all balls at the same distances from the center are equally off their corresponding targets, as shown in Fig. 2.65. As the reflow profile proceeds, the film and wafer heat up and

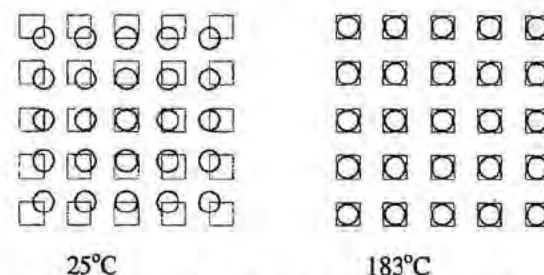


Figure 2.65 Scaled Tacky Dots pattern laid over corresponding target site pattern at 25°C and at 183°C (scale exaggerated).

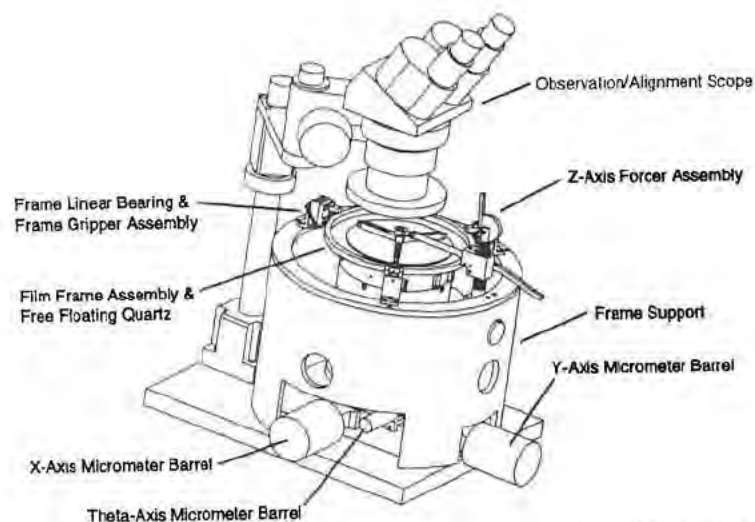


Figure 2.66 WRTP-4 prototype equipment for wafer bumping with Tacky Dots process.

grow linearly with temperature, until at 183°C the patterns match and the transfer takes place.

The Tacky Dots wafer-bumping process prototype equipment is schematically shown in Fig. 2.66.⁶⁹ It performs three major functions: film control assembly, reflector assembly, and temperature control. A

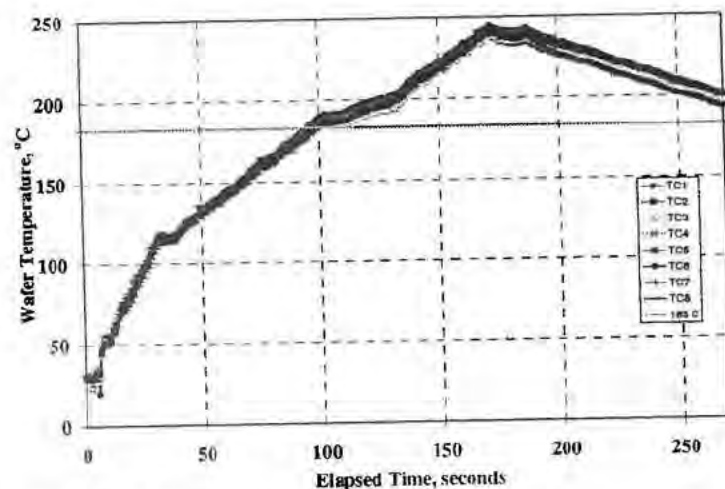


Figure 2.67 Reflow temperature profile.

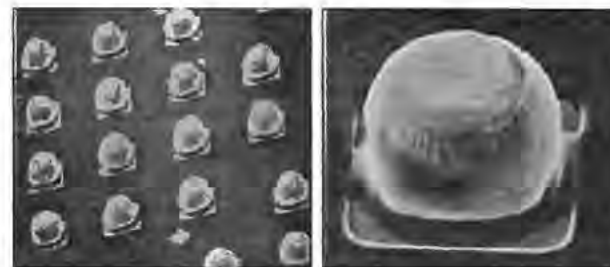


Figure 2.68 Once-reflowed Tacky Dots solder bumps.

typical solder reflow temperature profile obtained by using the prototype equipment and Tacky Dots is shown in Fig. 2.67.

Figures 2.68 and 2.69 show Tacky Dots solder bumps that have been reflowed one time. It is noted that the solder bump has a flat top surface. This is because the solder balls are solidified, with the base of the balls wetting the contact pad on the wafer and the tops of the balls constrained by the Tacky Dot carrier film. As a result, the array of transferred solder balls will all have flat tops that are coplanar and parallel to the wafer, regardless of the uniformity of the original solder ball. This flat top will disappear if it is reflowed one more time (Fig. 2.70). The UBMs of these chips are TiW-Cu, which works well with the Tacky Dots solder bumps.

The Tacky Dots technology provides a cost-effective, precise, flexible, and environmentally friendly wafer-bumping technique. It is simple, yet flexible in bump size, pitch, solder composition, and compatibility with various UBMs. One of the challenges is peeling off the Mylar cover sheet from the adhesive layer. This tends to generate a static charge and affects the handling of the tiny spheres. In addition, an agitated solder sphere bath tends to oxidize the solder sphere surface, which further aggravates the sensitivity toward static.

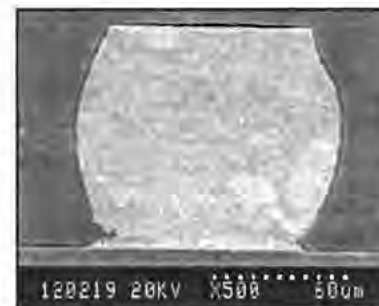


Figure 2.69 Cross section of once-reflowed Tacky Dots solder bump.



Figure 2.70 Twice-reflowed Tacky Dots solder bump.

2.3.12 Solder bumps on PCB method

Do we have to put the solder bumps on the chip/wafer in order to use the solder-bumped flip chip technology? No! However, this is more convenient for the system makers. They would consider the solder-bumped flip chip as just another SMT component and pick and place it on the PCB.

Can we put the solder bumps on the PCB and not on the chip/wafer in order to use the flip chip technology? Yes! However, in most cases the system makers hate it, because they may have only one or a few flip chip components on the PCB and they have to pay someone to put the solder bumps on the PCB. This not only adds cost but inconvenience.

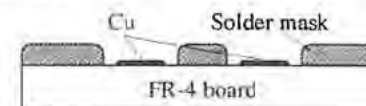
Figure 2.71 shows a way of stencil printing to make the solder bumps on PCB. Usually, printing must be repeated several times to reach the required solder bump height. The other way is by electroplating the Sn-Pb on the copper pads of the PCB. However, it will take a very long plating time to achieve certain solder bump heights on just a few flip chip sites in a large PCB. Thus, in general, it is more cost effective and convenient to put solder bumps on the wafer.

In order to make the high-lead solder bumps (e.g., C4) SMT compatible, however, a small amount of 63Sn-37Pb solder is put on the copper pads of the PCB (Fig. 2.72). For copper pads with pitches higher than 175 μm , stencil printing works fine; otherwise, electroplating⁷¹ or the molten solder injection method⁷² is needed.

2.3.13 Solder bumps on Al pads without UBM⁷³⁻⁷⁶

It is reemphasized that the low-cost wafer bumping methods discussed in Secs. 2.3.4 through 2.3.12 require UBM. Thus, logistics and infrastructure become big factors in judging the total cost of wafer bumping.

1. Manufacturing an FR-4 board with a solder mask



2. Printing solder paste into the solder mask



3. Reflowing the solder



4. Flattening the solder deposits



Figure 2.71 Stencil printing paste on board to either make solder bumps or to coat a thin layer of 63Sn-37Pb solder such that C4 is SMT compatible.

Usually, true low cost can be achieved if the bumpers also do UBM at the same site. Otherwise, there would be many hidden costs.

In this section, a very unique method to solder-bump the die without UBM is presented.⁷³⁻⁷⁶ Figure 2.73 illustrates some of the fundamental motions of the solder bump formation. The movement for bonding is provided by the conventional stud bump bonding machine, e.g., Shinkawa SBB-1. After the solder wire is inserted into a ceramic capillary, a solder ball 110 μm in diameter is formed at the tip of the wire by arc discharge in an $\text{Ar}/10\%\text{H}_2$ gas flow (1.5 l/min) introduced by means of two tubes

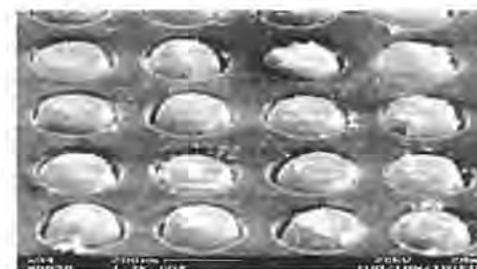


Figure 2.72 PCB with solid solder deposits.

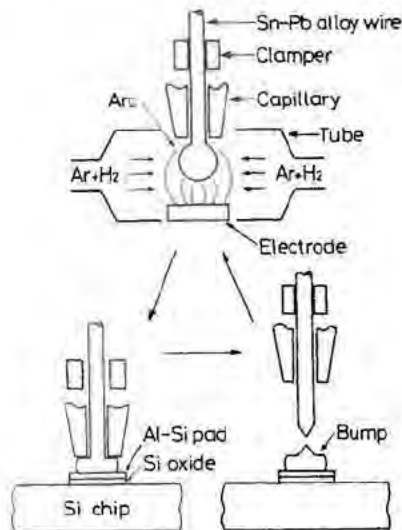


Figure 2.73 Some fundamental motions for the solder bump formation without UBM.

(inner diameter = 6 mm) positioned opposite each other. The discharge conditions are: spark voltage = 2.5 kV; discharge voltage = 60 V; current = 100 mA; time = 1.2 ms. The solder wire functions as an anode. Figure 2.74 shows the solder (Sn-Pb-Sb-Zn-Ag-Cu-Ni) alloy ball formed by arc discharge, and Fig. 2.75 shows the Auger spectra from the solder alloy ball surface before (a) and after (b) Ar ion etching for 120 s. It can be seen that Zn and O are detected near the ball surface.



Figure 2.74 SEM photo of the solder alloy ball formed by arc discharge.

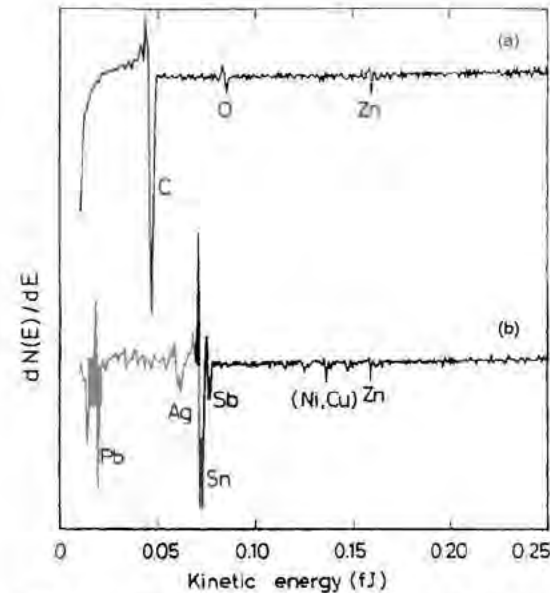


Figure 2.75 Auger spectra from the solder alloy ball surface before (a) and after (b) Ar ion etching.

The ball bonding conditions on the Al-1%Si film pad (0.8 μm), which is prepared by vapor deposition on a Si chip with a Si oxide layer of 0.5 μm , are as follows: applied power = 0.55 to 1.49 W; time = 35 ms for ultrasonic agitation; force = 0.39 to 0.51 N; chip temperature = 125°C. After the solder ball is bonded directly on the Al pad, the capillary is raised, then clamped and further raised, causing the solder wire to break at the ball-wire interface. Figure 2.76 shows the change in the shear force at various applied powers of ultrasonic agitation for the Sn-Pb-Sb-Zn-Ag-Cu-Ni alloy bump before and after reflow at 230°C.

The solder ball deformation ($2\ln D/D_0$) is fixed at 0.5 by adjusting the bonding force of the solder ball over the range of ultrasonic power from 0.55 to 1.49 W. In this examination, the D_0 and D showing the diameter of the initial ball and the bonded bump are 110 and 140 μm , respectively. The mean shear force of bonded and reflowed bumps attains a maximum value of 0.95 and 0.59 N, respectively, within a small range at 0.71 W. The bond areas at 0.71 W estimated from the areas of residual solder are $7.9 \times 10^{-3} \text{ mm}^2$ in the as-bonded state and $6.4 \times 10^{-3} \text{ mm}^2$ in the reflowed state. This results in the difference in the shear forces between bonded and reflowed states. Figure 2.77 shows the bonded

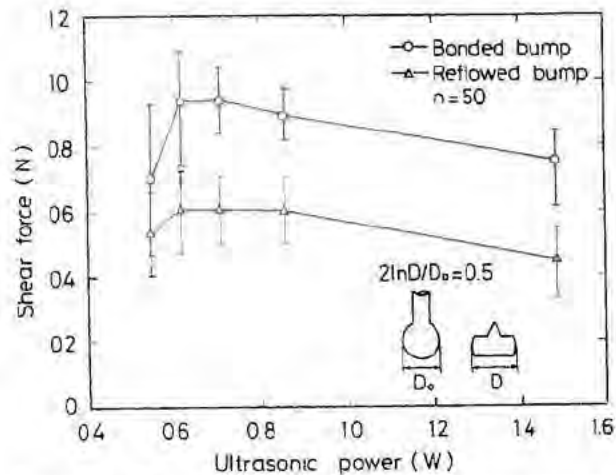


Figure 2.76 Change in the shear force with ultrasonic power for the solder alloy bump before and after reflow at 230°C.

bump shape (a) on Al-1%Si pads and the soldered interconnection and (b) before underfill encapsulation in the flip chip assembly.

The idea is great and it could be very low in cost. However, the throughput could be a big issue, since the solder bumps are formed one by one.

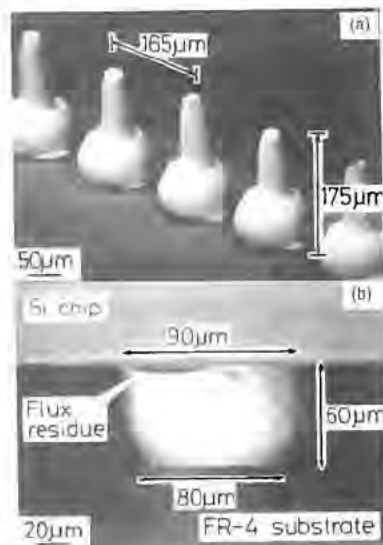


Figure 2.77 SEM photo of the bonded bump shape (a) on Al-1Si pads and the soldered interconnection and (b) before encapsulation in the flip chip assembly.

2.4 Alpha Particle

It is well known that alpha particles from thorium and uranium impurities in packaging raw materials such as lead-bearing solder alloys do not cause permanent damage to the chip but are sufficiently energetic to produce soft errors (data loss)—random, nonrecurring single-bit errors. Alpha particles produce soft errors by penetrating through the lead-bearing solder joint, UBM, Al pad, passivation, silicon, and *pn* junction and generating carriers as a result of giving up kinetic energy as they slow down. The carriers generated by alpha penetration through the junction distort the electric field and also generate charges.

The alpha emission flux is different for different materials. For example, the alpha emission from ceramic ranges from 0.1 to 1 $\alpha/\text{cm}^2 \cdot \text{h}$; the values for silicon are less than 0.1 $\alpha/\text{cm}^2 \cdot \text{h}$; and the figures for lead-bearing solder alloys vary greatly and are much higher than those from ceramic. Low-alpha lead-bearing solder alloys are available at a premium cost for applications that require purities as high as the order of parts per billion (ppb). One part per billion is equivalent to a flux of about 0.001 $\alpha/\text{cm}^2 \cdot \text{h}$.

There is a critical or escape depth, measured from the surface, below which alpha particles are internally absorbed by the emitting material and have no chance of retaining sufficient energy to emerge at the surface. For example, the escape depth for ceramic is on the order of 50 μm ; for silicon the figure is 25 μm ; and for lead-bearing solder alloys it is less than 10 μm .

Alpha particles have a limited range of penetration that varies with the energy of the particle and with the density and average mass number of the material. For example, in air, an alpha particle with ~5 MeV of energy may be stopped after traveling 5 to 6 cm. However, in polymers, the particle's range may be on the order of 0.005 to 0.01 cm. Thus, chemically inert materials such as silicone room-temperature vulcanized (RTV) rubber can be used as coatings to create barriers to alpha particles that prevent them from reaching the devices. Since the rubber itself has an average alpha activity of 0.001 $\alpha/\text{cm}^2 \cdot \text{h}$ and an alpha energy range of 2 to 8 MeV, a minimum of 2 mil of silicone rubber over the active surface of the chip is an effective barrier to alpha particles emitted from the packaging materials.

Alpha particles from lead-bearing solder alloys have been known to cause soft errors in memory devices. The alpha counts of 1 $\alpha/\text{cm}^2 \cdot \text{h}$ from solders containing lead are marginally acceptable today. However, this figure needs to be reduced to less than 0.01 $\alpha/\text{cm}^2 \cdot \text{h}$ for low-voltage and high-speed DRAM devices, since the lead-containing solder joints are the principal source of soft error. For more information about

alpha particles, readers are encouraged to consult the proceedings of the Low-Alpha Lead Symposium.⁷⁷

2.5 Wafer Bumping with Solderless Materials

The focus of this chapter is wafer bumping with solders. Discussions of wafer bumping with stud bumps can be found in Chap. 12 of Lau⁶ and Chap. 23 of Lau and Lee.³ Material on wafer bumping with Au, Cu, and Ni-Au materials can be found in Chap. 5 of this book.

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Flip Chip on Board with Solderless Materials

5.1 Introduction

Recently, for the sake of a green environment, solderless materials such as conductive adhesives¹⁻²³ have been evaluated for use in assembling flip chips on substrates. There are two different kinds of conductive adhesives: isotropic conductive adhesives and anisotropic conductive materials. Isotropic conductive adhesives, such as the Ag-Pd paste used in the stud bump bonding (SBB) flip chip on board technology given in Chapter 12 of Lau,⁴ electrically conduct in all directions and will not be discussed in this book.

Anisotropic conductive materials, also called *z*-axis conductive materials, electrically conduct only in the vertical direction. There are two groups of anisotropic conductive materials: anisotropic conductive film (ACF) and anisotropic conductive adhesive (ACA). ACF looks like paper and consists of thermosetting adhesive, conductive particles, and release film. ACA looks like paste and consists of thermosetting adhesive and conductive particles. In this chapter the design, materials, process, and reliability of flip chip assemblies with ACF and ACA will be discussed.

5.2 FCOB Assemblies with ACF²

In this section, DCA with solderless flip chip on PCB with ACF will be considered. The chip is bumped with three different metallurgies: Cu, Au, and Ni-Au. The Cu pads on the FR-4 epoxy PCB are with electroless Ni-Au and are organic coated. Hitachi's ACF^{7,8} is used for this study. The design, materials, and assembly process flow are shown in

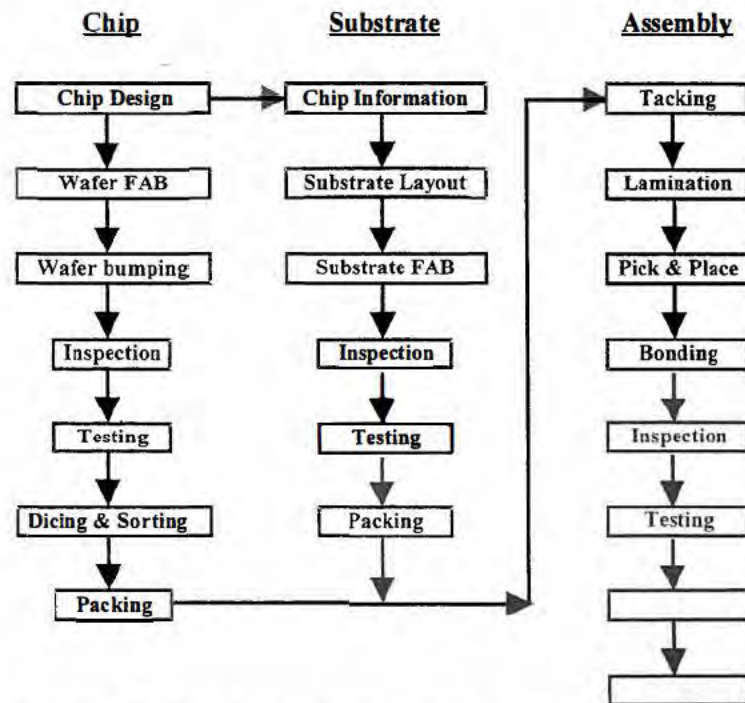


Figure 5.1 Flip chip on board with anisotropic conductive film (ACF) process.

Fig. 5.1. In the following sections some of the major steps will be discussed. Also, some thermal cycling and surface insulation resistance (SIR) test results are presented.

5.2.1 The wafer

The chip size is 0.5 in. (12.7 mm) square and 25 mils (0.64 mm) thick. The street width between all the chips is 6 mils (0.15 mm). The chip has 8-mil (0.2-mm) square pads and 14-mil (0.36-mm) pitch. All of the pads are arranged symmetrically around the perimeter of the chip and interconnected via traces on the chip in an alternating pattern so as to provide daisy-chained connections when the chip is attached to the FR-4 PCB.

The silicon wafer consists of a patterned aluminum layer on a layer of silicon dioxide that is covered with a patterned silicon nitride passivation layer. The wafer fabrication process flow starts with deposition of an 0.25- μm layer of silicon dioxide by Plasma Enhanced Chemical Vapor Deposition (PECVD) on a <111> silicon substrate. For

the metal layer, an 0.85- μm layer of Al-1%Si-0.1%Ti alloy is sputtered over the silicon dioxide. The metal pattern is then defined by coating with positive resist, exposed by projection alignment, developed, and wet-chemical-etched. After the photoresist is removed by plasma stripping, the metal pattern is sintered at 450°C to remove film stresses. For the passivation layer, a 0.75- μm layer of silicon nitride is deposited over the entire surface of the wafer by PECVD. The pad opening in the passivation layer is then defined by coating with positive resist, exposed by projection alignment, developed, and plasma-etched. Finally, the resist is removed by plasma stripping, leaving the silicon nitride passivation layer to overlap the perimeter of the Al pads by 10 μm .

5.2.2 Wafer bumping with Au, Cu, and Ni-Au

In this study, three different bumps (Au, Cu, and Ni-Au) are put on the wafers (Fig. 5.2). The materials and process for each kind of bump are briefly discussed.

Wafer bumping with Au. The wafers are Au-bumped by the electroplating method (Fig. 5.3). The under-bump metallurgies (UBMs) of the wafers are titanium (Ti) and tungsten (W). They are sputtered on the entire surface of the wafer, 0.1 to 0.2 μm of Ti first, followed by 0.3 to 0.5 μm of W. A 20- μm layer of resist is then overlaid on the Ti-W and a bump mask is used to define the bump pattern. The openings in the resist are 7 to 10 μm wider than the pad openings in the passivation layer. A 20- μm -thick layer of Au is then plated over the Ti-W. The resist is then removed and the Ti-W stripped off with a hydrogen peroxide etch. Figure 5.4 shows a cross section of the electroplated Au bump on the Si wafer. The average microhardness of the Au bumps is 120 on the Vickers scale (HVN).

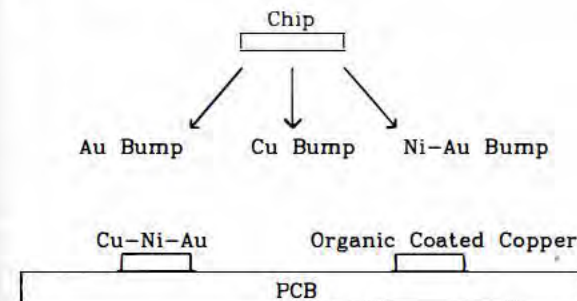


Figure 5.2 Flip chip with three different kinds of bumps on two different kinds of PCBs.

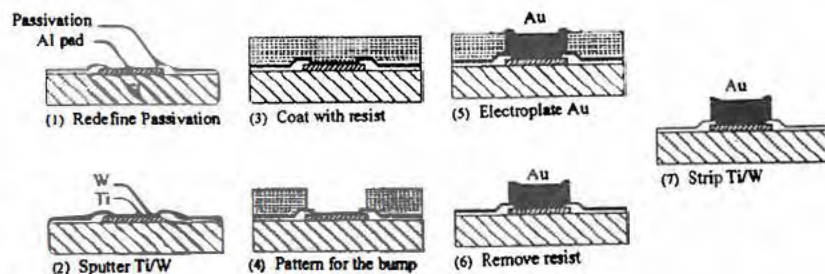


Figure 5.3 Electroplated Au wafer bumping process.



Figure 5.4 A typical Si chip with Au bump.

Wafer bumping with Cu. The wafer-bumping process with Cu is almost the same as that with Au except for the UBM, which is Ti (0.1 to 0.2 μm) and Cu (0.5 to 0.8 μm). On top of the UBM, the plated Cu thickness is 20 μm . The average microhardness of the Cu bumps is 100 (HVN). Since the copper surface oxidizes and corrodes very easily, the Cu bumps are electroless-plated with a very thin layer of Sn (i.e., immersed or simply dipped). Figure 5.5 shows a cross section of the electroplated Cu bump on the Si wafer.



Figure 5.5 A typical Si chip with Cu bump.

Wafer bumping with Ni-Au. The Ni-Au bumps on the wafers were made by PICOPAK in Finland in 1995. The average bump height is 24 μm and the average shear strength is 80 g. PICOPAK's Ni-Au process in 1995 is shown in the following list.

1. Visual inspection of wafer
2. Test runs with diced wafer samples to find optimal process conditions
3. Application of photoresist to cover possible ink dots, undesired openings in dicing lanes, etc., using a standard photolithography process
4. Application of photoresist on back side of wafer
5. Plasma cleaning of exposed surfaces (<5 min at very low wafer temperature)
6. First zincate [~2 min at room temperature (RT)], rinse in DI water
7. Zinc strip (~1 min at RT), rinse in DI water
8. Second zincate (~2 min at RT), rinse in DI water
9. Nickel plating (~1 h at <100°C), rinse in DI water
10. Visual inspection of wafer
11. Bump height measurements
12. Immersion in gold (~15 min at <100°C), rinse in DI water
13. Removal of photoresist in hot (~100°C) acidic solution

14. Visual inspection of wafer
15. Bump shear test
16. Bump wetting test (not necessary for ACF applications)
17. Documentation and shipping of goods

Figure 5.6 shows a cross section of the electroless Ni-Au bump on the Si wafer. It should be noted that for such a large Ni-Au bump (24 μm), the Ni creates a large amount of stress that could crack the passivation (Figs. 5.7 through 5.11). Great care in monitoring of all process steps and

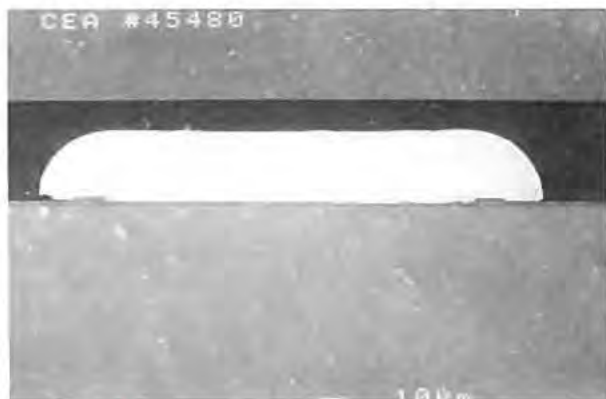


Figure 5.6 A typical Si chip with Ni-Au bump.



Figure 5.7 Ni-Au bump with a crack in the passivation.



Figure 5.8 Ni-Au bump with a crack in the passivation.



Figure 5.9 Ni Au bump with a crack in the passivation.

tight contamination control of the Zn, Ni, and Au solution tanks must be taken in order to obtain the Ni-Au bump shown in Figs. 5.6 and 5.12.

5.2.3 PCB

A matching PCB is designed along with the chip. The Cu pads are round (8 mils or 0.2 mm in diameter) and in a 14-mil (0.36-mm) pitch. In this study, two Cu pad finishings, electroless Ni-Au and organic, are

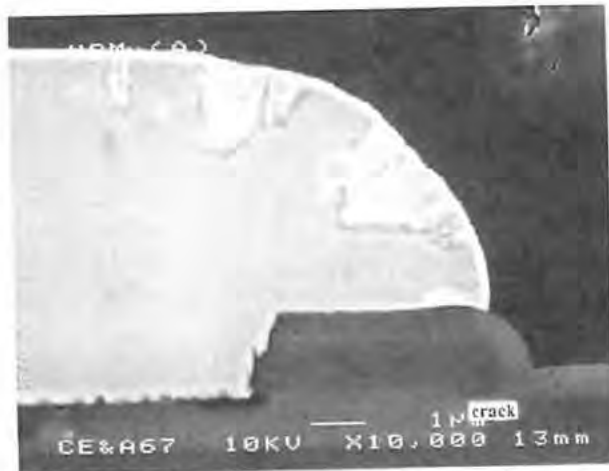


Figure 5.10 Ni Au bump with a crack in the passivation.



Figure 5.11 Ni Au bump with a crack in the passivation.

considered (Fig. 5.2). Most of the pads are interconnected via traces on the PCB in an alternating pattern so as to provide daisy-chained connections with the chip.

5.2.4 ACF^{7,8}

The ACF used for this study is Hitachi Chemical's double-layer ACF (Fig. 5.13). It consists of nonfilled thermal-setting adhesive and thermal-



Figure 5.12 Ni Au bump with no cracks (a perfect one!).

setting adhesive layers filled with Ni (2 to 5-μm) conducting particles. Each layer is about 30 μm thick. It has been shown by Hitachi Chemical that there are more conductive particles between the bumps of the chip and the pads of the substrate if the particle-filled thermal-setting adhesive layer in the ACF faces the pad of the substrate (Fig. 5.14).^{7,8} For this study, the ACF is sandwiched between two layers of release paper.

5.2.5 FCOB assembly with ACF

More than 100 chips have been bonded on the Cu-Ni-Au and organic-coated copper (OCC) FR-4 PCB. These chips have three different kinds of bumps: 20-μm Cu studs, 20-μm Au studs, and 24-μm Ni-Au bumps.

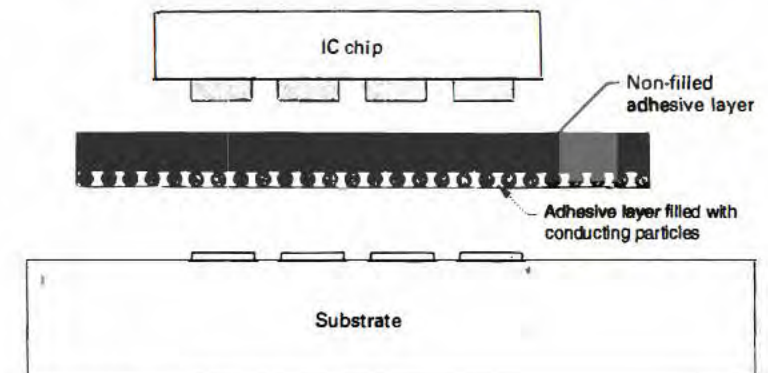


Figure 5.13 Hitachi's double layer ACF.

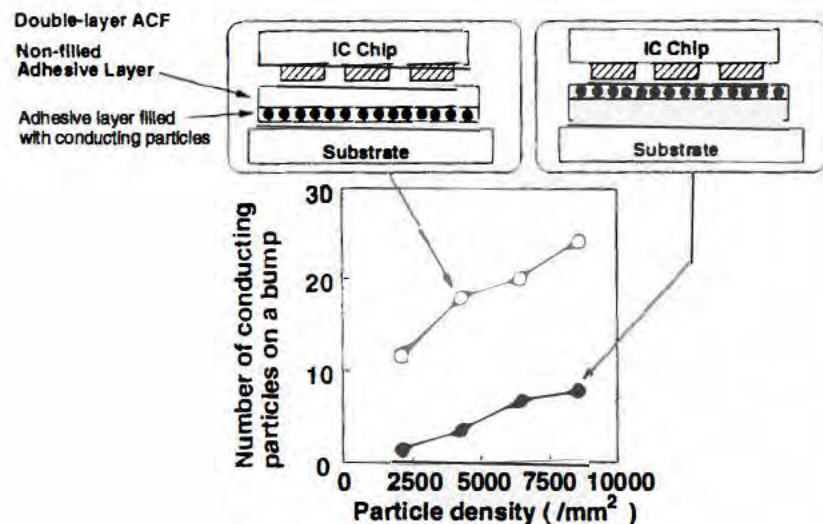


Figure 5.14 Effect of Hitachi's ACF direction on the number of conducting particles per bump.

The assembly process of the ACF is very simple and clean (fluxless). First of all, the ACF is cut to a little larger than the size of the chip and one of the release papers is removed. The ACF is then placed on the FR-4 PCB with the other release paper facing upward. This is called *tacking*.

The next step is to prepress the ACF under conditions of 80°C, 10 kg/cm², and 5 s. This is called *lamination*. In the next step, a lookup camera is used to read in some of the bumps of the chip. The release paper is removed, and then a lookdown camera is used to read in the corresponding pad locations of the PCB. After the necessary adjustment, the chip is placed on top of the ACF on the PCB. This is called *pick and place* and is done on Hitachi's aligning machine. Finally, the chip on board assembly is transported to the Hitachi bonder, which performs the *bonding* under conditions of 180°C, 5 kg/μm², and 20 s. Figure 5.15a shows a typical flip chip on PCB with ACF assembly. A typical cross section of the assembly is shown in Fig. 5.15b. There are many voids.

Figures 5.16 through 5.19 show the scanning electron microscopy (SEM) of a cross section of the ACF-bonded flip chip with Au bumps on PCB with Cu-Ni-Au pads. It can be seen that there are a few Ni conducting particles. Since the electroplated Au bump on the chip is softer than the electroless Au-Ni on the PCB, these Ni conducting particles penetrate more into the Au bump on the chip. One of the disadvantages of anisotropic conductive materials is the waste of conductive particles, as shown in Fig. 5.19.

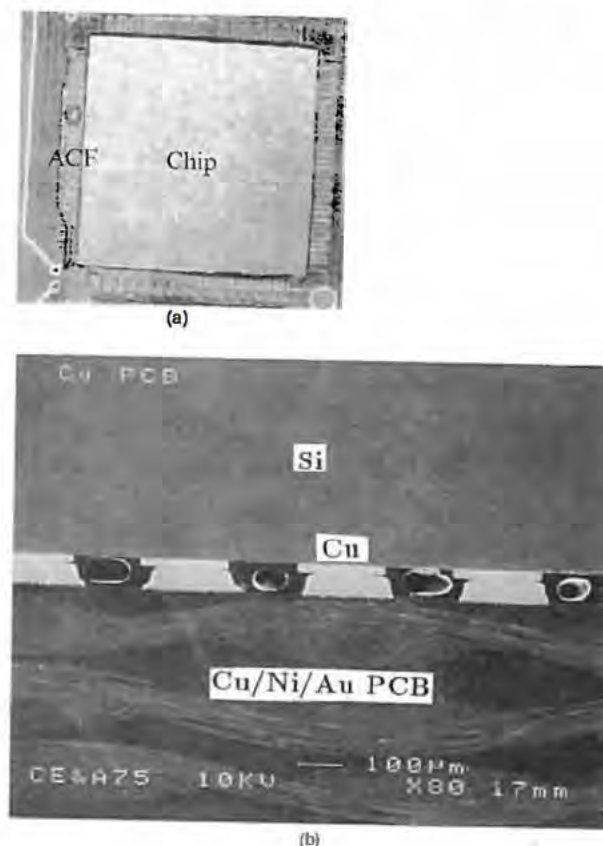


Figure 5.15 (a) An assembled FCOB with ACF. (b) A typical cross section of the ACF-bonded FCOB assembly.

Figure 5.20 shows the SEM of a cross section of the ACF-bonded flip chip with Cu bumps on PCB with Cu-Ni-Au pads. It can be seen that most of the Ni conducting particle penetrates into the electroplated Cu (with a coating of Sn) bump on the chip. Again, this is because the microhardness of the Au-Ni pads on the PCB is greater than that of the Sn-Cu bumps on the chip.

Figure 5.21 shows the SEM of a cross section of the ACF-bonded flip chip with Ni-Au bumps on PCB with Cu-Ni-Au pads. It can be seen that the penetration of the Ni conducting particles into both the Ni (with a coating of Au) bump on the chip and Au-Ni pads on the PCB is small. As a matter of fact, some of the Ni conducting particles have been badly deformed.

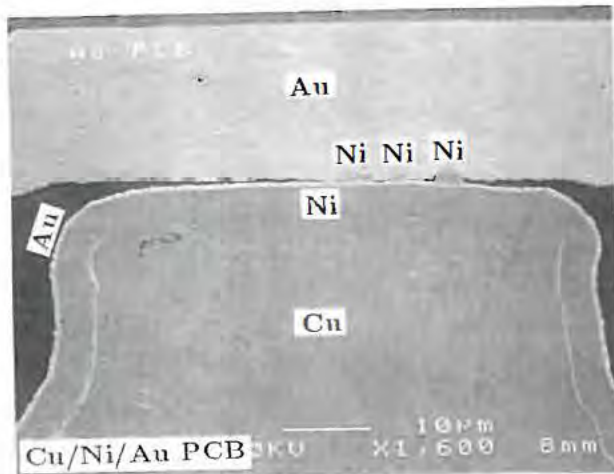


Figure 5.16 ACF-bonded flip chip with Au bump on Cu-Ni Au PCB.

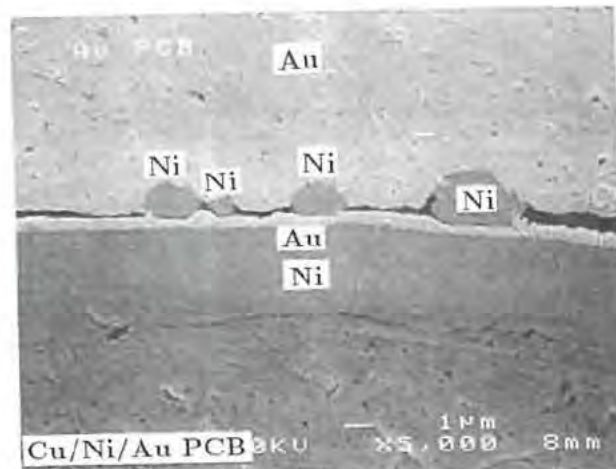


Figure 5.17 ACF-bonded flip chip with Au bump on Cu Ni Au PCB.

Figure 5.22 shows the SEM of a cross section of the ACF-bonded flip chip with Cu bumps on PCB with OCC pads. It can be seen that the Ni conducting particles penetrate into both the Cu (with a coating of Sn) bump on the chip and the OCC pad on the PCB.

In general, the ACF assembly yield is strongly affected by the kinds of bumps on the chip and the flatness of the PCBs. In our cases, chips

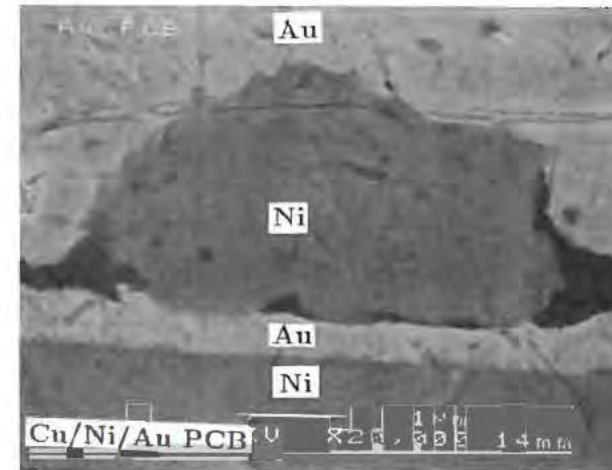


Figure 5.18 ACF-bonded flip chip with Au bump on Cu Ni Au PCB.

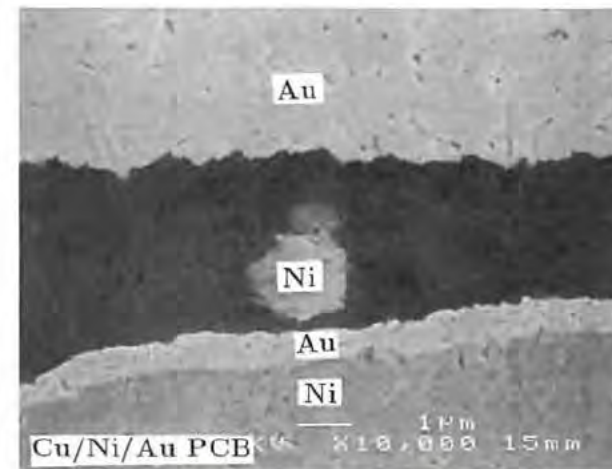


Figure 5.19 A Ni particle is wasted by not making the bond.

with Cu bumps have the highest yield and chips with Ni-Au bumps have the lowest yield. This could be due to the microhardness of the bumps, since the Cu bump is the smallest and the Ni-Au bump is the largest. Also, PCB with OCC pads leads to a better assembly yield than Cu-Ni-Au pads. This could be due to the less curved surface (greater flatness) of the OCC finishing.

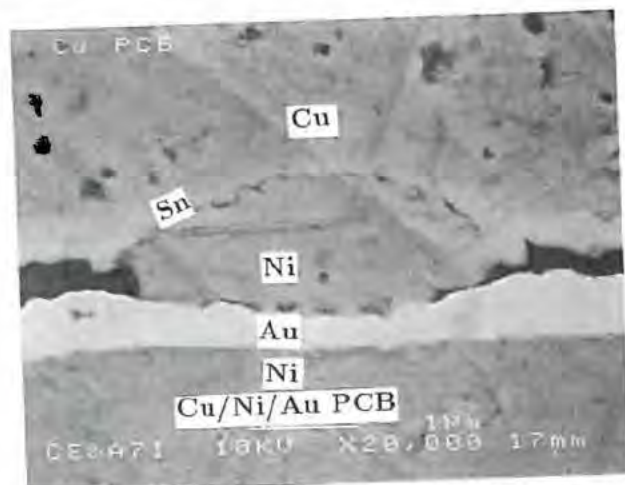


Figure 5.20 ACF bonded flip chip with Cu bump on Cu-Ni Au PCB.



Figure 5.21 ACF bonded flip chip with Ni-Au bump on Cu Ni Au PCB.

5.2.6 Thermal cycling test of FCOB assemblies with ACF²

Forty ACF-bonded flip chips (20 with Au bumps and 20 with Cu bumps) on Cu-Ni-Au PCB were subjected to thermal cycling. The temperature profile is shown in Fig. 5.23. Temperatures ranged from -20 to +110°C, and the cycle time was 1 h. The test results are shown in Fig. 5.24. It can be seen that after 1000 cycles, there was no opening in

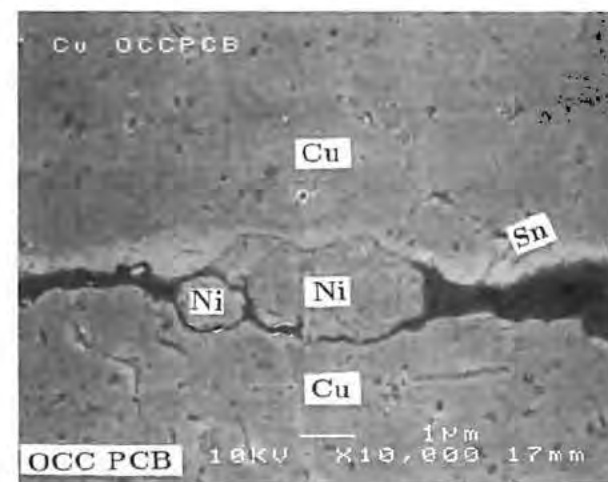


Figure 5.22 ACF bonded flip chip with Cu bump on OCC PCB.

either case. However, the resistance of the FCOB assemblies with Cu bumps increased to about 29 percent. On the other hand, the increase in resistance of the FCOB assemblies with Au bumps was only 5.3 percent. This could be due to the greater degradation of the Cu-bumped FCOB than the Au-bumped FCOB assemblies after thermal cycling.

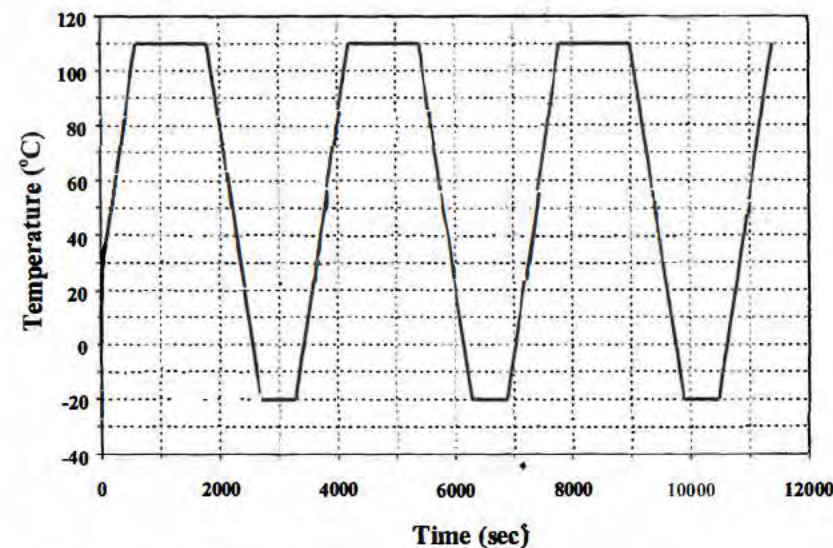


Figure 5.23 Temperature cycling profile.

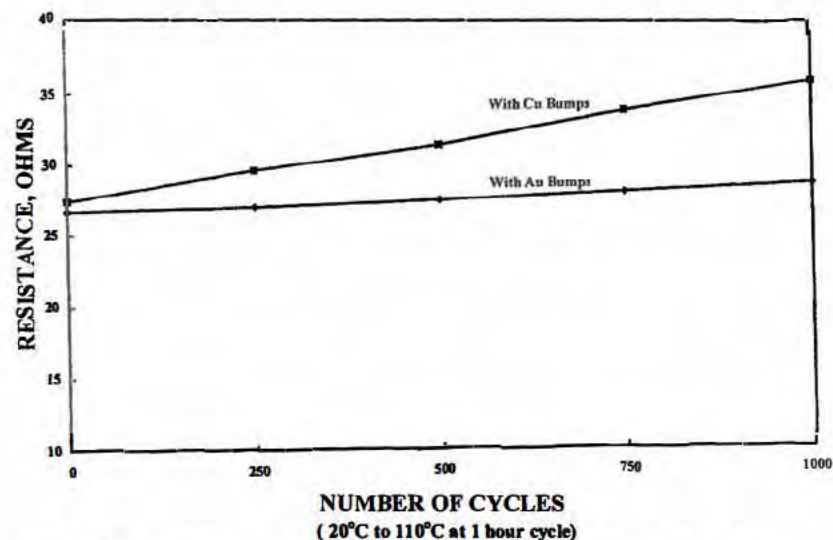


Figure 5.24 Thermal cycling results of ACF bonded flip chip on Cu-Ni Au PCB.

From the present results it is expected that the Au-bumped FCOB with ACF assemblies should have a better thermal fatigue life than the Cu-bumped FCOB with ACF assemblies.

5.2.7 SIR test results of FCOB assemblies with ACF

Surface insulation resistance testing is one of the most widely used techniques for assessing electrical performance reliability in electronic packaging. Leakage currents are monitored as a function of time at predetermined temperature, humidity, and bias voltage conditions. Leakage currents between closely spaced bumps/pads are sensitive indicators and are good signals of potential field risks. SIR values of 100 M Ω or higher are acceptable for commercial and industrial applications, and 500 M Ω is acceptable for military requirements. Figure 5.25 shows the SIR test (85°C/85%RH at 10-V bias) results for the ACF-bonded FCOB assemblies. It can be seen that ACF is acceptable for all the cases under consideration.

5.2.8 Summary

The Au-bumped, Cu-bumped, and Ni-Au-bumped flip chips have been assembled on Cu-Ni-Au and OCC PCBs with ACF. Important parameters and process steps such as the wafer; wafer bumping with Au, Cu, and Ni-Au; PCB; ACF; tacking; lamination; pick and place; and bonding have been discussed. Furthermore, the ACF-bonded FCOB assemblies

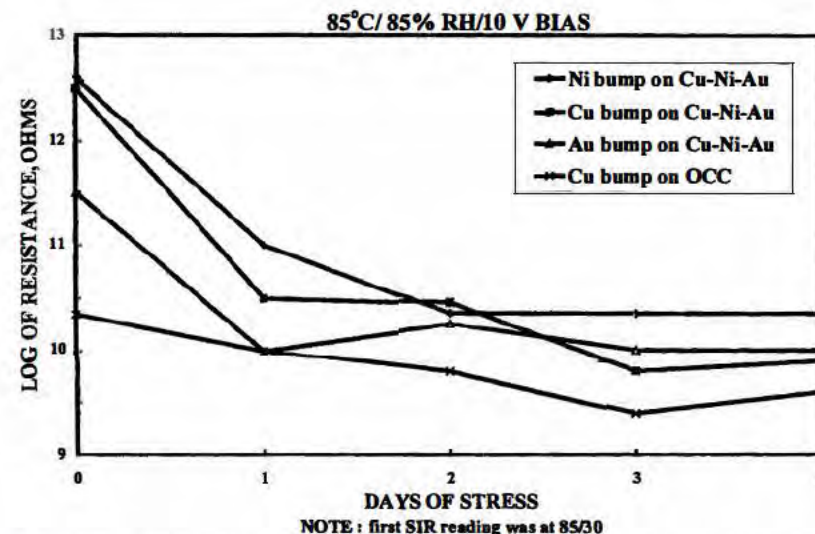


Figure 5.25 Surface insulation resistance (SIR) test results of ACF bonded flip chip on PCBs.

have been subjected to thermal cycling and SIR tests. Some important results are summarized as follows.

1. The ACF-bonded FCOB assembly yield is strongly affected by the kind of bumps (Au, Cu, or Ni-Au) on the chip. Flip chip with Cu bumps has the highest assembly yield, and that with Ni-Au bumps has the lowest.
2. The ACF-bonded FCOB assembly yield is strongly affected by the flatness of the PCB. Also, in this study, PCB with OCC pads leads to a better assembly yield than PCB with Cu-Ni-Au pads.
3. There is no opening in the ACF-bonded flip chip on Cu-Ni-Au PCB assemblies after 1000 temperature cycles (-20 to +110°C). The resistance change due to 1000 temperature cycles of the Au-bumped flip chip assemblies (5.3 percent) is smaller than that of Cu-bumped flip chip assemblies (29 percent).
4. In this study, the ACF-bonded FCOB assemblies meet SIR test requirements for commercial, industrial, and military applications.

5.3 FCOB Assemblies with ACA³

In this section, materials, process, and reliability of flip chip on PCB assemblies with different ACAs are discussed. Most of the results presented herein are provided by the Technical University of Berlin, Cen-

ter of Microperipherals Research, and Fraunhofer-Institute of Reliability and Microintegration.³

5.3.1 IC, PCB, and ACA materials

Five different ACA materials with different conductive particles are considered. Their actual curing conditions are determined by DSC and are shown in Table 5.1. Three different sizes of ICs with various daisy-chained I/Os are considered in Table 5.2. Two different bumps are considered, namely the electroless Ni-Au and Au (electroplated Au and Au stud), as shown in Table 5.2. The PCB is made of FR-4 and the Cu finishing is Ni-Au (3 μm -0.2 μm). The objective of the study is to compare the performance of different combinations of bumps and conductive particles as shown in Table 5.3.

Figures 5.26 and 5.27 show, respectively, the effect of prebaked PCB with adhesives A and B. The dark spots are voids. It can be seen that there is no void within the adhesive layer when prebaked substrates are used. (The gray treelike structures are particle sediments of filler particles used to enhance the mechanical properties of the cured adhesives.) As a matter of fact, increasing the preheat time leads to

TABLE 5.1 Properties of Processed Adhesives and Underfill Materials

Sample	Conductive filler particles	Recommended cure schedule	Investigated cure schedule
A	5.0 μm Ni	30 s @ 150°C	5 s @ 200°C
B	None	30 s @ 150°C	10 s @ 200°C
C	3.0 μm Au/Poly	30 s @ 150°C	10 s @ 200°C
D	3.7 μm Au/Poly	30 s @ 150°C	10 s @ 200°C
E	5.0 μm Ni	30 s @ 150°C	10 s @ 200°C

TABLE 5.2 Specifications of PCB and ICs

Substrate	
Material	FR 4
Size	2 × 2 in.
Electrode	Cu Ni Au: 17 3 0.2 μm
IC	
Size	5.0 × 5.0 mm ² 7.5 × 7.5 mm ² 10.0 × 10.0 mm ²
Pitch	200 μm , 300 μm
I/Os	136, 88, 184, 120
Bumps	Electroless Ni-Au: ϕ 75 μm , height 10 μm Electroplated Au: ϕ 75 μm , height 20 μm Stud Au

TABLE 5.3 Combinations of Bumps and Conductive Particles Under Study

	A	B	C	D	E
Ni Au		X	X	X	X
Stud Au	X	X			
Electroplated Au				X	X

decreased voiding. Thus, only preheated PCBs are used for further experiments.

5.3.2 FCOB with Ni-Au bumps and ACA

The flip chips with Ni-Au bumps are bonded on the PCB with forces between 50 and 150 g per bump. The contact resistance is measured and is shown in Table 5.4. Since there is no conductive particle with adhesive B, the bonds are all open for low pressure (50 g per bump). However, for greater pressures (100 and 150 g per bump), contact resistance of 4 m Ω as well as open contacts are observed. Figure 5.28 shows the cross sections of contacts for two different applied forces. It can be



Figure 5.26 C-mode images of die bonded on the original PCB (left) and prebaked PCB (right) with adhesive A.

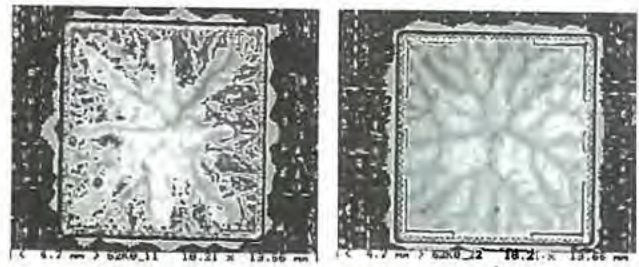


Figure 5.27 C-mode images of die bonded onto original PCB (left) and prebaked PCB (right) with adhesive B.

TABLE 5.4 Influence of Bond Force on Contact Resistance

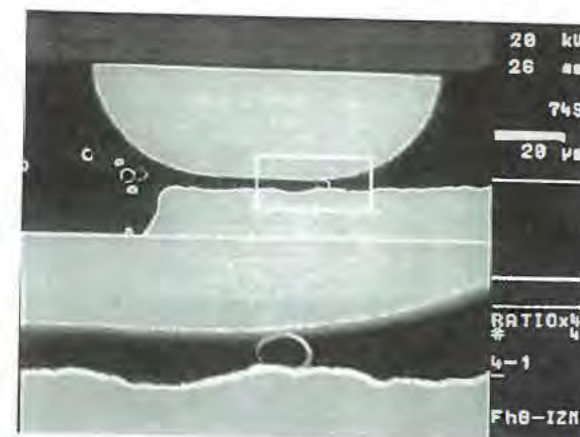
	Conductive particles	Bond force (g/bump)	Contact resistance	
			Average (mΩ)	Range (mΩ)
B	None	50	All open	—
		100	50% open	—
		150	Some open	—
C	3.0 μm Au Poly	50	80	50
		70	60	45
		100	50	20
D	3.7 μm Au Poly	50	20	10
		70	65	22
E	5.0 μm Ni	50	60	27
		100	20	5

seen on the left (50 g per bump) that because of some nonconductive fillers within the adhesive, it is difficult to have a good contact. On the other hand, the contact pads on the right (150 g per bump) are pushed downward into the substrate matrix by bending of the electrodes. The bending for this applied force is too large, which may lead to electrode cracking and die touching. Thus, bonding forces of no more than 100 g per bump will be used for the next experiments.

Figure 5.29a shows the cross section of a flip chip assembly with adhesive C (5.0-μm Au-poly) with a bond force of 50 g per bump. It can be seen that the particle deformation is not sufficient to ensure a good contact. However, with a bond force of 100 g per bump (Fig. 5.29b), it can be seen that the particles are partially crushed and the conductance is provided by direct contact between the bump and pad. For adhesive D, which has larger conductive Au/Poly particles (5.7 μm), there is a good contact resistance of 20 mΩ after bonding at 50 g per bump (Table 5.4). However, for a bond force of 70 g/bump, the contact



Figure 5.28 Bending of bond pads at bonding force of 50 g per bump (left) and 150 g per bump (right).



(a)



(b)

Figure 5.29 (a) Particle deformation at bonding force of 50 g per bump (adhesive C). (b) Particle deformation and direct contact at bonding force of 100 g per bump (adhesive C).

resistance is in the range of 65 mΩ. This means that the bond quality has been decreased by crushing the particles and forming a direct contact between the hard bump and the electrode.

As for the 5.0-μm Ni conductive particles in adhesive E, a bond force of 50 g per bump leads to a high contact resistance with large deviations. However, a bond force of 100 g per bump lowers the contact resistance to 20 mΩ with the smallest deviations of all. This is due to the large particle size, which ensures a good contact over the entire bump surface even with bent and sunk electrodes.

5.3.3 FCOB with Au bumps and ACA

Figure 5.30 shows the cross section of a Au-bumped flip chip on board with Au/polymer-filled adhesive D (bonding force of 50 g per bump). It can be seen that there are two current paths, via particles and directly between bump and electrode, because the electroplated gold bump itself is deformed and forms a direct contact with the PCB electrode. Also, the gold-coated polymer particles have not only been deformed but have penetrated into the Au bump.

Figure 5.31 shows the cross section of a Au-bumped flip chip on board with 5.0- μm Ni conductive particles of adhesive E (bonding force of 50 g per bump). It can be seen that the Ni particles penetrate into the Au bump. Also, the electrodes are bent where they are supported by the glass fibers.

5.3.4 Accelerated aging test and results

Table 5.5 shows the bonding forces and curing schedules for the samples subjected to the following accelerated aging tests: (1) high-temperature storage at 125°C, (2) temperature cycling at -55 to +125°C, (3) humidity storage at 85°C/85% RH, and (4) reflow test after humid-



Figure 5.30 Interconnection using Au coated polymer filled ACA (adhesive D).

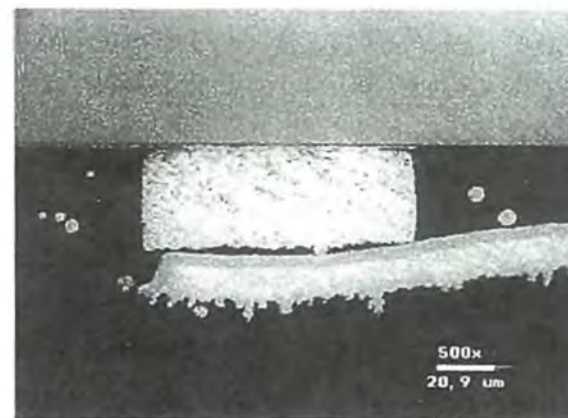


Figure 5.31 Interconnection using Ni filled ACA (adhesive E).

ity storage. Table 5.6 shows the test results. A failed contact is defined as a complete opening or a 10-fold increase in initial contact resistance. Figure 5.32 (humidity storage test) shows that Ni-filled adhesive E performs the worst. This could be due to the corrosion of the Ni particles.

Figure 5.33 (temperature cycling test) shows that most of the failures during temperature cycling tests are observed with the Ni-filled adhesive and electroplated Au bumps. The adhesive with the best performance is filled with 5.7- μm Au-coated polymer (adhesive D) with Ni-Au bumps and electroplated Au bumps.

5.3.5 Summary³

1. Unlike on polyimide, ACA materials may form voids on PCB. Either prebaking of the PCB or preheating of the ACA materials could reduce voiding to zero.

TABLE 5.5 Sample Preparation for Reliability Tests

Adhesive	Bumps	Bond force	Cure schedule
A	Au stud	70 g/bump	5 s @ 200°C
B	Au stud	70 g/bump	10 s @ 200°C
D	Ni Au	50 g/bump	10 s @ 200°C
D	Electroplated Au	50 g/bump	10 s @ 200°C
E	Ni Au	100 g/bump	10 s @ 200°C
E	Electroplated Au	50 g/bump	10 s @ 200°C

TABLE 5.6 Results of Reliability Tests

Tested combination	Results after 1000 h high temperature storage	Results after 1000 thermal cycles	Results after 1000 h humidity storage
A (stud Au bumps)	Not tested	15% failed	Not tested
B (stud Au bumps)	No increase in contact resistance	No increase in contact resistance	No increase in contact resistance
D (electroplated Au bumps)	No increase in contact resistance	No increase in contact resistance	36% failed
D (Ni Au bumps)	No increase in contact resistance	No increase in contact resistance	2× increase in contact resistance
E (electroplated Au bumps)	No increase in contact resistance	22% failed	100% failed
E (Ni Au bumps)	No increase in contact resistance	No increase in contact resistance	58% failed

- Bond forces have to be adjusted carefully according to bump metallurgies and type of conductive particles. Excess bond forces may lead to badly deformed electrodes.
- Reliability of flip chip on board strongly depends on the bump metallurgies and kind of conductive particles. The combination of hard Ni-Au bumps and soft Au-coated polymer particles performs the best through all tests.
- The combination of soft electroplated Au bumps and large (5.0- μm) Ni-filled adhesive performs the worst.

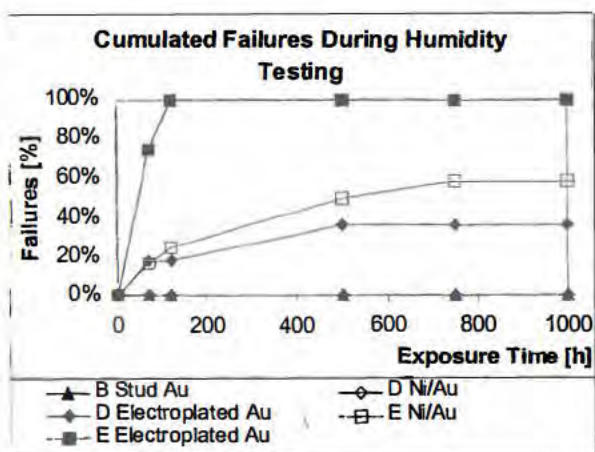


Figure 5.32 Cumulated failures during humidity storage test.

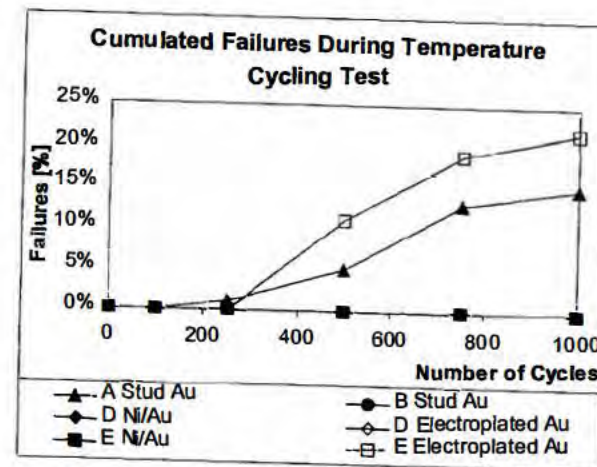


Figure 5.33 Cumulated failures during temperature cycling test.

Acknowledgments

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Flip Chip on Board with Conventional Underfills

6.1 Introduction

Flip chip is defined as a chip mounted on a substrate with various interconnect materials and methods such as TAB, wire interconnects, isotropic and anisotropic conductive adhesives, metal bumps, compliant bumps, fluxless solder bumps, and pressure contacts, as long as the chip surface (active area or I/O side) is facing the substrate.¹ Compared to the face-up chip mounting configurations, flip chip provides the shortest possible leads, the lowest inductance, the highest frequencies, the best noise control, the highest density, the greatest number of I/Os, the smallest device footprints, and the lowest profile.¹⁻²³⁹ In this chapter, the focus is on flip chips with solder-bump materials.

The solder-bumped flip chip was introduced by IBM in the early 1960s for its solid logic technology (SLT), which became the logical foundation of the IBM 360/System computer line. The so-called C4 (controlled-collapse chip connection) technology utilizes solder bumps deposited on wettable metal terminals on the chip and a matching footprint of solder wettable terminals on the substrate. The solder-bumped flip chip is aligned to the substrate, and the solder joints are made simultaneously by reflowing the solder bumps (Fig. 6.1).

In this book, the solders on the chip before it is joined to the substrate are called *solder bumps*. After the solder bumps have been reflowed on the substrate, they are called *solder joints*.

For its C4 bumps, IBM used the 5wt%Sn-95wt%Pb solder alloy, which has solid and liquid temperatures of 308 and 312°C, respectively. Sometimes, IBM also used the 3wt%Sn-97wt%Pb solder alloy, which

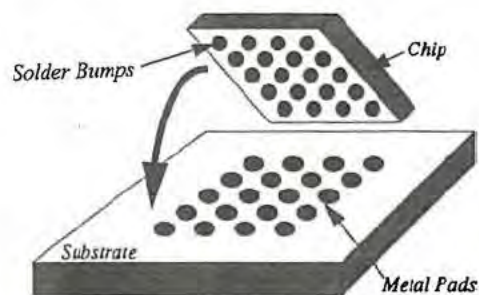


Figure 6.1 Solder bumped flip chip technology.

has solid and liquid temperatures of 314 and 320°C, respectively. The substrate materials IBM used were usually ceramics, which have a thermal expansion coefficient of about 4 to $6 \times 10^{-6}/^{\circ}\text{C}$. During reflow, because of the surface tension of the molten solder, the chip will self-align to the substrate; this leads to a very high-yield manufacturing process (Fig. 6.2). For large chips, sometimes underfill encapsulant is used to enhance solder joint reliability.

6.2 FCOB with High-Temperature Solder Bumps

IBM at Yasu, Japan, has been assembling solder-bumped flip chip on organic PCB since 1990^{33, 35} (Fig. 6.3). Applications include personal computers, personal computer memory card international association (PCMCIA) cards, and Token Ring local area network (LAN) adapter cards. IBM's results show that solder-bumped flip chip assembly technology is applicable for low-cost PCB as well as high-cost substrates such as ceramics.

The DCA technology of IBM at Yasu is based on IBM's C4 technology (Figs. 6.3 and 6.4). That means the melting temperatures of the C4 solder bumps are higher than 310°C. In order to be SMT compatible (at a maximum reflow temperature less than 240°C), the copper pads on the

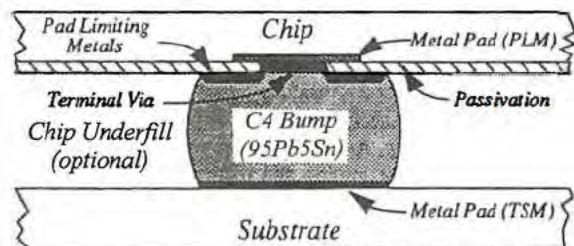


Figure 6.2 IBM's controlled collapse chip connection (C4) technology.

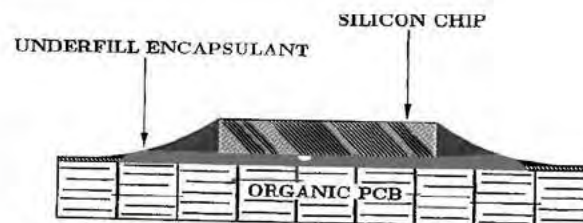


Figure 6.3 Low cost solder bumped flip chip on board.

PCB are coated with 63wt%Sn-37wt%Pb solder alloy, like those shown in Fig. 2.72, using conventional electroplating method or IBM at Yasu's molten solder injection machine, as shown in Fig. 2.45 (replacing the wafer with PCB). A typical cross section of the FCOB assembly is shown in Fig. 6.5. It should be noted that the high-temperature C4 solder bump is not reflowed.

In order to reduce the cost of substrate even further, Motorola⁷² developed E3 solder bumps (Sec. 2.3.1; Chap. 6 of Lau⁶) for FCOB assembly

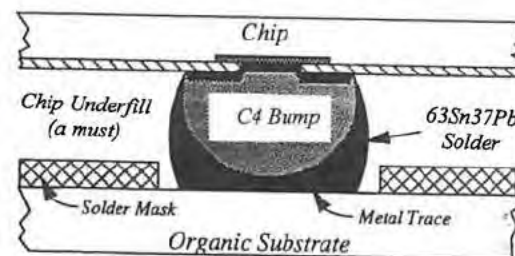


Figure 6.4 Direct chip attach with IBM's C4 technology.



Figure 6.5 Cross section of IBM's low cost FCOB.

applications. In that process, the unreflowed E3 solder bumps are placed on the OCC PCB and mass-reflowed with other SMT components.

6.3 FCOB with Low-Temperature Solder Bumps

Unlike IBM and Motorola, which use composite solder interconnects (high-lead solder bump with eutectic solder) and the evaporation method, Oki, Sharp, Hewlett-Packard, Toshiba, and many other companies use the 63Sn-37Pb eutectic solder bumps as shown in Fig. 6.6. The substrates for such non-C4 solder-bumped flip chips can be standard FR-4 or bismaleimide triazine (BT) with either Cu-Ni-Au, Sn-Pb, or OCC PCBs. These companies do not use the E-3 process or coat the PCB with eutectic solder; rather, they treat the eutectic solder-bumped chips like other SMT components, which can be mass-reflowed on the low-cost PCBs with all the other SMT components.

The non-C4 solder-bumped flip chip assemblies perform very well under thermal cycling tests. For example, Sharp's wafers are bumped with 60Sn-40Pb solder (Fig. 6.7) by electroplating. That company's substrates for the solder-bumped flip chips are standard FR-4 PCBs with a Cu-Ni-Au metal finish (Fig. 6.8). Sharp conducts thermal cycling tests (-45 to $+100^{\circ}\text{C}$ and 1 cycle per hour) of five different square flip chip assemblies (3, 6, 9, 12, and 15 mm) with underfill; no failures are observed at 1000 cycles. For the smaller flip chip assemblies (3, 6, and 9 mm) with underfill, no failures are observed even after 9000 cycles, as shown in Fig. 6.9.^{65, 66} However, without underfill, even the smaller chips failed before 300 cycles.

Another set of thermal cycling tests is performed on the chip shown in Fig. 6.10. It can be seen that the chip dimensions are 6.7×6.5 mm for a single and $\sim 14 \times 14$ mm for a quad. The chips are bumped with 63Sn-37Pb solder using the electroplating method. The bump height is about 100 μm . The chips are assembled on the OCC PCB with a thickness of 1.57 mm. The underfill materials used are the CNB11 and 4511, provided by HYSOL.

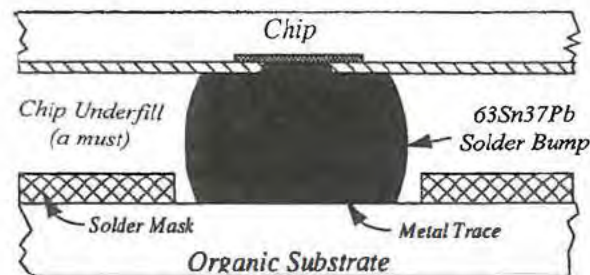


Figure 6.6 Low cost solder bumped flip chip on board with 63Sn 37Pb solder alloy.

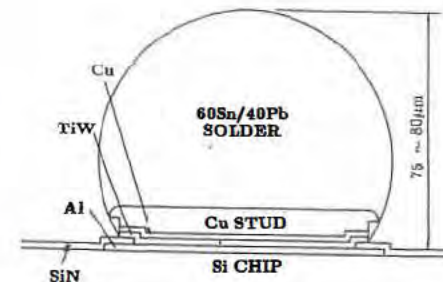


Figure 6.7 Sharp's eutectic solder bump.

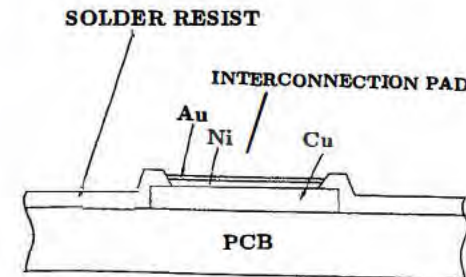


Figure 6.8 Sharp's low cost PCB.

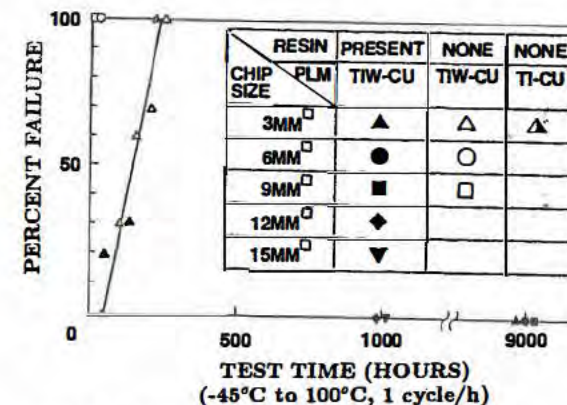
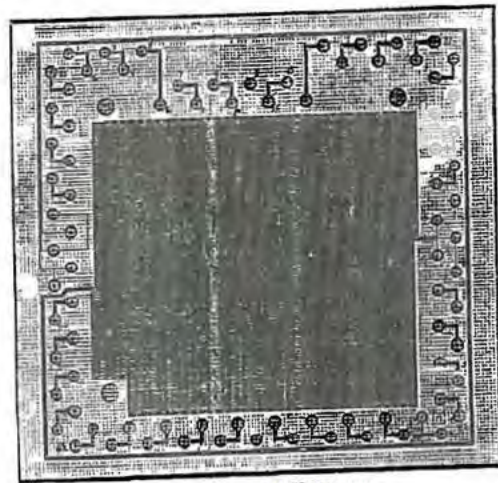


Figure 6.9 Sharp's thermal cycling test data.

The temperature loading imposed on the flip chip assemblies is shown in Fig. 6.11. It can be seen that for each cycle (60 min) the temperature is between -20 and $+110^{\circ}\text{C}$, with 15 minutes ramp, 20 minutes hold at hot, and 10 minutes hold at cold. There are two reasons for choosing this temperature profile: (1) the glass transition temperature of the PCB is 120°C and we don't want to introduce additional failure mechanisms of the solder joint due to the degradation of the PCB; and



Chip size = 6.7 X 6.5 mm
 Number of bumps = 84
 Bump diameter = 150 μ m
 Bump pitch = 250 μ m

Figure 6.10 A very useful test chip.

(2) the behavior of solder below -20°C is not very well understood. The test is run nonstop for more than 6 months.

The thermal cycling test results represented by the Weibull life distribution are shown in Figs. 6.12 and 6.13, respectively, for the single and quad flip chip assemblies. It can be seen that: (1) as expected, the smaller chip performs better than the larger chip, but not by very much, and (2) the solder joints in both cases are reliable for use in most operating conditions.

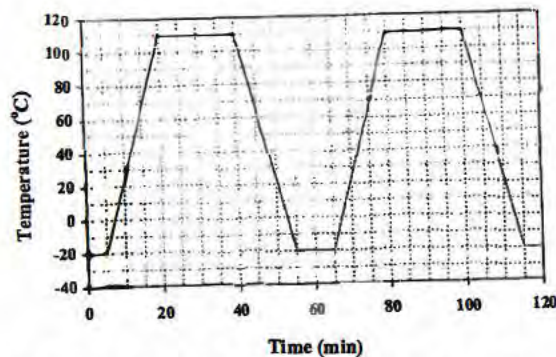


Figure 6.11 Thermal cycling temperature profile (on board).

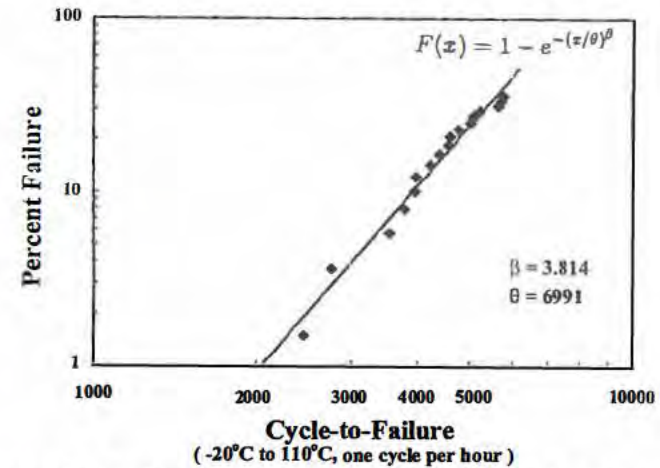


Figure 6.12 Solder joint Weibull life distribution of the single test chip.

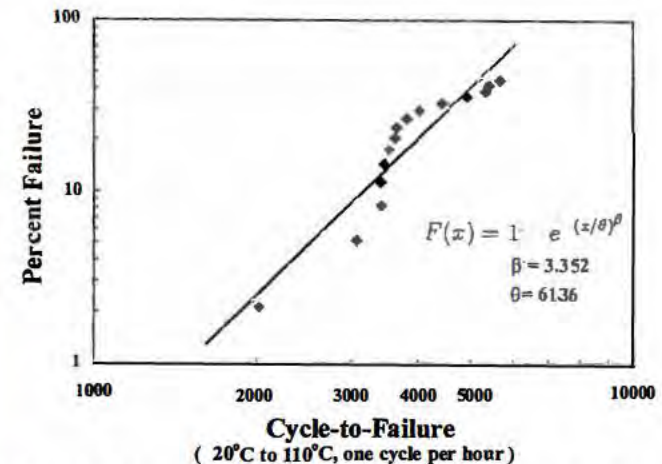


Figure 6.13 Solder joint Weibull life distribution of the quad test chip.

6.4 Most Desirable Features of Underfills¹⁸⁷

One of the major reasons why solder-bumped flip chip on low-cost PCB works is because of the underfill encapsulant. It reduces the effect of the global thermal expansion mismatch between the silicon chip ($2.5 \times 10^{-6}/^{\circ}\text{C}$) and the organic FR-4 PCB ($18.5 \times 10^{-6}/^{\circ}\text{C}$). (Since the chip, underfill, and PCB are deformed together as a unit—i.e., the relative deformation between the chip and the PCB is very small—the shear

deformation of the solder joint is very small.) The other advantages of underfill encapsulant are that it protects the chip from moisture, ionic contaminants, radiation, and hostile operating environments such as thermal and mechanical conditions, shock, and vibration. Also, without heat sink, underfill is usually the major heat path from the chip to the PCB.

The most desired features of underfill materials are:¹⁸⁷

- Low viscosity (fast flow), which can increase throughput
- Low curing temperature/fast curing time, which can reduce cost and be less harmful to other components
- Low TCE, which can reduce thermal expansion mismatch between the chip, solder bumps, and PCB
- High modulus, which leads to good mechanical properties
- High glass transition temperature, which enables endurance of higher temperature environments
- Low moisture absorption, which can extend shelf life
- Good adhesion, which can improve product life time

Some companies that provide various underfill materials are Ablestik, Alpha Metal, Dexter, Emersion, Epoxy Technology, HYSOL, Johnson Matthey, Kester, Loctite, Matsushita, Thermoset, and Zymet. It should be emphasized that the curing conditions and material properties of the underfill materials provided by the vendors are for reference purposes only. For good engineering, the end users should verify the data through measurements.

6.5 Handling and Application of Underfills

Usually, underfill materials are premixed at the supplier sites, packed in plastic syringes (5 to 10 cc), and then frozen packed at -40°C to prevent curing. Shipping of these underfill materials requires special handling to maintain the low temperature continuously. When the package is received, it should be unwrapped and the syringes should be quickly removed and stored in an uninterrupted temperature-controlled (-40°C) freezer. In this case, most of the underfill encapsulants would have approximately 1 year of storage life.

Before the underfill materials are applied, they are removed from the freezer and thawed at room temperature. It takes about 1 h to thaw a 5- to 10-cc syringe. Once thawed, most of the underfill materials have a pot life of 14 to 16 h.

Dispensing the underfill encapsulants through a syringe is accomplished with a version system (to locate the edges of chip) and a pump-

ing system (to control the amount of underfill materials). The temperature of the heating plate is around 90°C . After the underfill materials are dispensed on either one side or two adjacent sides of the chip, the chip and substrate should remain on the heating plate for about 30 to 90 s (depending on the chip size and the gap between the chip and the substrate) to enhance the flow rate of the underfill. After the underfill has flowed out from the other sides of the chip (sometimes touch-up is necessary), the chip on board will be put into a curing oven for 10 to 60 min at 130 to 170°C depending on the curing conditions of the underfill materials.

6.6 Curing Conditions of Underfills

Ten different underfill materials with different sizes and filler contents (underfills A through J) are under consideration, as shown in Table 6.1. For all these materials, the filler is silica. Most components of the underfills are bis-phenol-type epoxies and trade secret resins.

To determine the curing conditions of underfill materials, they are put into an aluminum pan (which will form a disc sample 6.4 ± 0.2 mm in diameter and 1.6 ± 0.1 mm in height), weighed, and then put into DSC equipment. Since the system is always directly measuring energy flow to or from the sample, the DSC can directly measure temperature at onset of curing. The kinetic software enables analysis of a DSC peak to obtain specific kinetic parameters that characterize a reaction process.

Figure 6.14 shows the typical DSC thermal scan curve. It can be seen that the peak curing temperatures for underfills B and F are 135.2 and 141.1°C , respectively. The exothermic peak of curve B is wider than that of curve F, which is very sharp. This means that underfill F has to be cured within a narrow temperature range while underfill B can be cured along a wide temperature range. Also, underfill B needs more time to be fully cured than underfill F (10 min at 150°C for underfill B, and 5 min at 150°C for underfill F). In general, lower temperatures and

TABLE 6.1 Average Curing Conditions for Underfills A Through J

Underfill	Filler Content and Size	Curing Temperature ($^{\circ}\text{C}$)	Curing Conditions [temperature ($^{\circ}\text{C}$)/time(min)]				Temperature ($^{\circ}\text{C}$) at 15 minutes of Curing
A	40% < $10\text{ }\mu\text{m}$	136.2	150 / 27	160 / 10	165 / 7	170 / 4	155.8
B	60% < $10\text{ }\mu\text{m}$	135.2	150 / 10	160 / 4	165 / 2	170 / 1.2	146.3
C	40% < $10\text{ }\mu\text{m}$	117	150 / 8	160 / 5	165 / 4	170 / 3	139.9
D	60% < $10\text{ }\mu\text{m}$	143.3	165 / 83	170 / 38	180 / 9	185 / 4	175.4
E	60% < $10\text{ }\mu\text{m}$	142.9	165 / 693	170 / 268	180 / 43	185 / 18	188.3
F	50% < $20\text{ }\mu\text{m}$	141.1	150 / 5	152 / 3	154 / 2	156 / 1	146.4
G	60% < $20\text{ }\mu\text{m}$	137.1	150 / 297	160 / 54	165 / 24	170 / 11	167.9
H	55% < $20\text{ }\mu\text{m}$	141.9	150 / 186	160 / 60	165 / 35	170 / 21	172.9
I	60% < $20\text{ }\mu\text{m}$	153.6	165 / 182	170 / 112	180 / 44	185 / 28	191.7
J	60% < $10\text{ }\mu\text{m}$	139.7	150 / 169	160 / 60	165 / 36	170 / 22	173.3

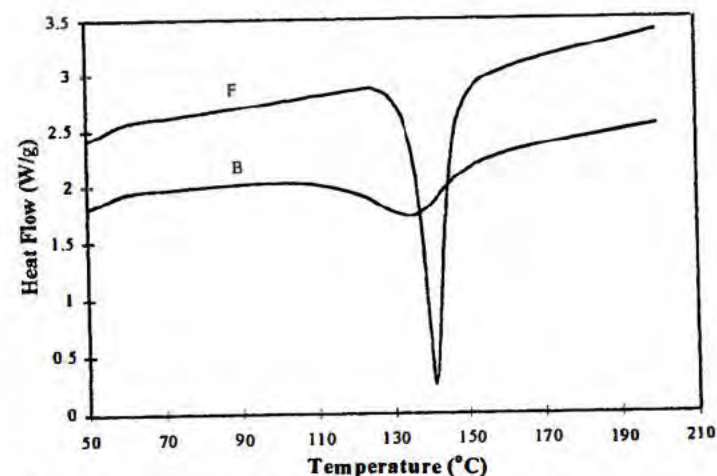


Figure 6.14 DSC thermal scan curve for underfills B and F.

longer times for full curing of underfill materials will lead to lower thermal stresses and better physical and mechanical properties. This could be due to the fact that the molecular chains have more time to reorganize and pack well.

Figure 6.15 shows the curing temperature-versus-time curves. It can be seen that underfill D cured faster than underfill E. Table 6.1 summarizes the average curing conditions for underfills A through J. It can be seen that the curing conditions varied with different underfill materials and that materials cured faster at higher temperatures.

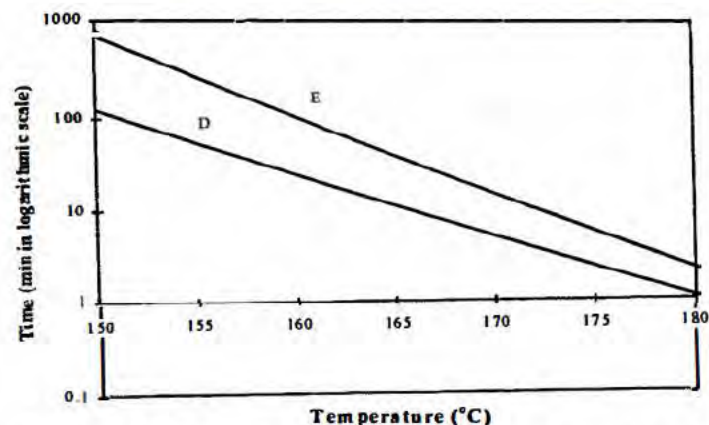


Figure 6.15 Curing temperature versus-time curves for underfills D and E.

Also, underfills B, C, and F cured faster than the others. Furthermore, the temperatures of these three materials (less than 156°C) at 15 min of curing are lower than those of the others. For most of the manufacturing environments, underfill materials that can be fully cured at 150°C within 15 min are acceptable.

6.7 Material Properties of Underfills

The values for TCE, storage modulus, tangent delta, glass transition temperature, moisture content, and flow rate of underfills A through J are obtained in this section. Also, the Young's modulus, stress-strain relations, and creep curves are provided. In addition, the fracture toughness of underfills, of underfill-FR-4 interfaces, and of underfill-passivation interfaces are presented.

6.7.1 TCE

The TCE values for underfills A through J (with sample dimensions of 6.4 ± 0.2 mm in diameter and 1.6 ± 0.1 mm in height) are determined by TMA in an expansion quartz system (50 to 200°C) at a heating rate of 5°C/min. The TCE of the material is obtained by the slope of the dimension change-versus-temperature curve, and T_g can be obtained from the onsets of the two different slopes of the curve.

Figure 6.16 shows typical expansion curves for underfills C and H. Table 6.2 summarizes the average results for underfills A through J. It

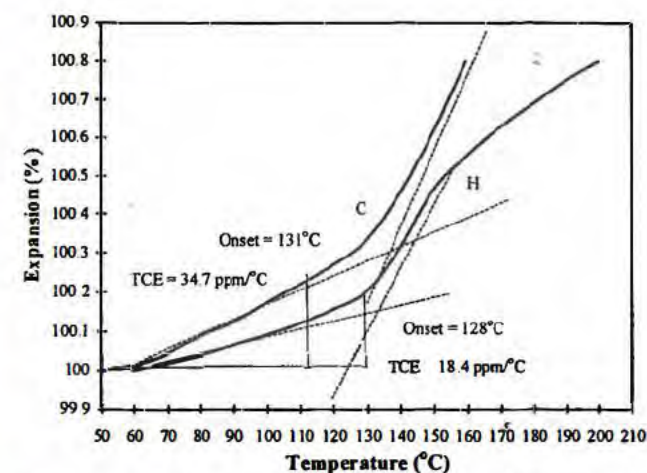


Figure 6.16 Typical expansion curves for underfills C and H for determining TCE.

TABLE 6.2 Average Material Properties of Underfills A Through J

Underfill	Filler Content and Size	TCE (ppm/°C)	T_g (°C)	Width of T_g peak (°C)	Storage Modulus (GPa)			Percent Drop from 55 to 110°C
					25°C	55°C	110°C	
A	40% < 10 μ m	37	149	18	4.62	4.56	4.22	7.5
B	60% < 10 μ m	29	162	19	4.88	4.87	4.74	2.7
C	40% < 10 μ m	34.7	140	15.8	3.4	3.3	2.93	11.2
D	60% < 10 μ m	29.8	170	24.7	3.73	3.69	3.44	6.8
E	60% < 10 μ m	32.5	124	19.5	3.78	3.76	2.7	28.2
F	50% < 20 μ m	32.5	134	58	4.4	4.34	2.45	44
G	60% < 20 μ m	17.7	155	26	4.5	4.5	4.12	8.4
H	55% < 20 μ m	18.4	142	43.2	4.5	4.45	3.69	17.1
I	60% < 20 μ m	16.7	159	36.9	2.96	2.96	2.67	9.8
J	60% < 10 μ m	14.6	127	37	4.0	3.96	2.5	36.9

can be seen that the TCE of underfill A (40 percent filler content) is the largest ($37 \times 10^{-6}/^{\circ}\text{C}$) and the TCE of underfill J (60 percent filler content) is the smallest ($14.6 \times 10^{-6}/^{\circ}\text{C}$). The T_g value obtained using the TMA method is usually about 10°C lower than that obtained with the DMA method, which will be discussed in Secs. 6.7.2 and 6.7.3.

In general, the higher the filler content, the lower the TCE value. This is because of the fact that the filler (made from silica) expands less than the epoxy resin. From solder joint thermal fatigue reliability points of view, it is preferable to use underfill materials having lower TCEs ($< 27 \times 10^{-6}/^{\circ}\text{C}$) to reduce the thermal expansion mismatch between the chip, the solder joints, and the low-cost substrate.

6.7.2 Storage modulus

The modulus values for underfills A through J are measured with a three-point bending specimen ($3.0 \pm 0.3 \text{ mm} \times 2.9 \pm 0.3 \text{ mm} \times 19 \pm 3 \text{ mm}$) in a DMA unit (50 to 200°C) at a heating rate of $5^{\circ}\text{C}/\text{min}$. For electronics packaging materials, flexural properties such as the storage modulus, loss modulus, and tangent delta ($\tan \delta$) can be obtained with DMA. In material sciences, the flexural storage modulus E_s is a measure of the energy stored per cycle of deformation.

Figure 6.17 shows typical dynamic flexural storage modulus curves for underfills B and F as a function of temperature. The stiffness of underfill B at low temperatures (less than 100°C) is temperature independent, while the stiffness of underfill F is very poor, dropping quickly when the temperature increases. The average storage modulus results for underfills A through J are reported in Table 6.2. It can be seen that the storage modulus of all the underfill materials is temperature dependent, i.e., the higher the temperature, the lower the modulus. The

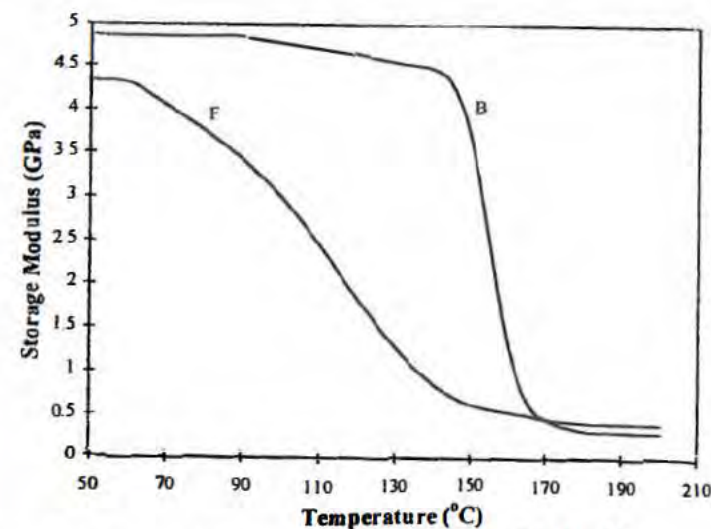


Figure 6.17 Typical storage modulus curves for underfills B and F.

percent drop in modulus from 55 to 110°C , shown in the last column of Table 6.2, can be as high as 44 percent for some underfill materials.

6.7.3 $\tan \delta$ and T_g

Mechanical energy supplied at the temperature and frequency corresponding to the transition will be absorbed by the material, then partially stored elastically and partially dissipated in the form of heat. Tangent delta ($\tan \delta$) (a measure of material-related damping properties) for underfills A and J is shown in Fig. 6.18. The temperature at the peak of a tangent delta curve is often reported in the literature as glass transition temperature (T_g).

The damping is the ratio of heat dissipation to energy storage, and is dependent on the temperature and frequency. Near the glass transition temperature, polymers display maximum values of loss modulus and $\tan \delta$, which are measures of energy dissipation—or, in other words, their “lossiness” is at a maximum. The wider range of $\tan \delta$ may involve friction between fillers or between fillers and polymer and may provide additional means of dissipating energy. Contributions from the inhomogeneous distribution of fillers and from thermal stresses may also affect damping properties. In this study, it can be seen from Fig. 6.18 that curve A is sharper than curve J (that is, the transition temperature range is smaller), indicating that the stiffness of underfill A is better than that of underfill J. The underfills will become softer during a

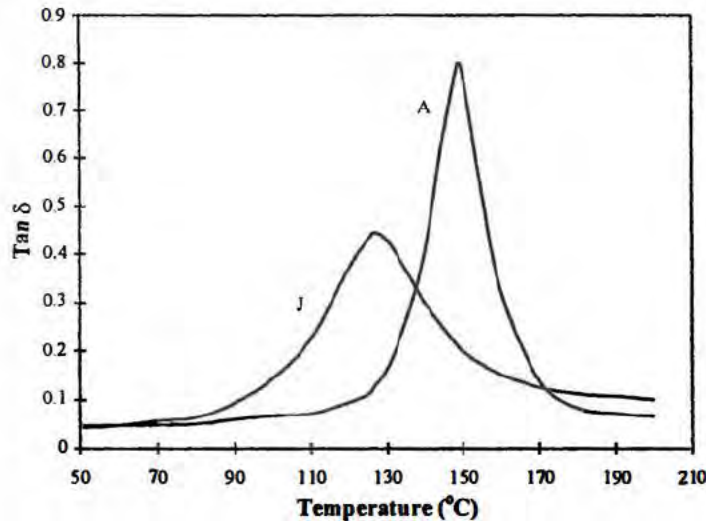


Figure 6.18 Typical tangent delta curves for underfills A and J.

wider transition temperature range. The average values of T_g for all the underfills are shown in Table 6.2.

6.7.4 Moisture content

Porosity exists in materials due to trapped air and outgasing, and is responsible for the absorption of moisture. The pores serve to concentrate stresses that may cause further growth of cracks when external loads or thermal stresses are applied. In general, the more porosity, the more moisture absorption. Three sets of tests are carried out to determine the moisture content. One is for dry specimens, the second is for moisture-soaked specimens, and the third is for steam-aged specimens. The moisture-soaked specimen is subjected to 85°C and 85 percent relative humidity for 168 h. The steam-aged specimen is prepared using steam evaporation for 20 h in a closed hot-water bath. All the specimens are 6.4 ± 0.2 mm in diameter and 1.6 ± 0.1 mm in height. Weight changes for underfills A through J are measured with the TGA equipment at 102°C for 2 h.

The change in mass during thermal scan can be expressed as $(W_f - W_i)/W_i$, where W_f is the final weight after thermal scan and W_i is the initial weight before thermal scan. Figure 6.19 shows typical percent weight change ratio (moisture content) for underfill E before and after moisture soak and after 20 h of steam aging. The average moisture contents of all the underfills are shown in Table 6.3. It can be seen that the average moisture content of all the underfills under moisture-soak con-

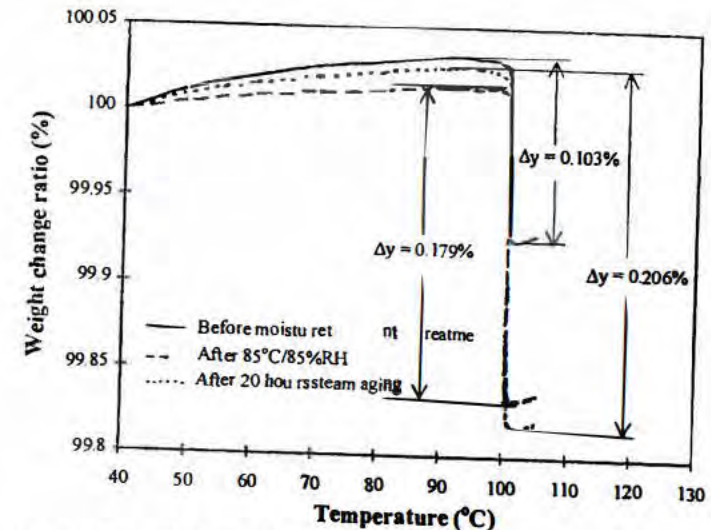


Figure 6.19 Typical weight change (moisture content) for underfill E before and after moisture soak and after 20 hours of steam aging.

ditions is very close to that after 20 h of steam aging. Based on this study, it is recommended that the acceptable moisture absorption for dry underfill materials is 0.1 percent and that for moisture-soaked underfill materials is 0.2 percent.

6.7.5 Young's modulus^{189, 223}

The Young's modulus of the HYSOL FP4526 underfill has been determined by researchers at Wayne State University.^{189, 223} The glass transi-

TABLE 6.3 Average Flow Rates for FCOB with Underfills A Through J and Moisture Content

Underfill	Filler Content and Size	Flow Rate (mm/s)	Moisture content (%)			Percent Increase After 85°C/85% RH for 168 Hours
			Dry	20 Hours of Steam Aging	85°C/85% RH for 168 Hours	
A	40% < 10 μm	0.42	0.115	0.279	0.302	162.6
B	60% < 10 μm	0.63	0.105	0.202	0.216	105.7
C	40% < 10 μm	0.42	0.153	0.855	0.686	348.4
D	60% < 10 μm	0.105	0.121	0.228	0.19	57
E	60% < 10 μm	0.21	0.103	0.206	0.179	73.8
F	50% < 20 μm	0.31	0.124	0.385	0.292	135.5
G	60% < 20 μm	0.63	0.088	0.195	0.177	101.1
H	55% < 20 μm	0.07	0.077	0.194	0.196	154.5
I	60% < 20 μm	0.07	0.075	0.142	0.15	100
J	60% < 10 μm	0.105	0.07	0.172	0.187	167.1

tion temperature of this underfill is 133°C as measured by Dexter. Figures 6.20 and 6.21 show the Young's modulus of the HYSOL FP4526 underfill at different strain rates and temperatures. It can be seen that the Young's modulus is temperature dependent; that is, the higher the temperature, the lower the Young's modulus, and the higher the strain rate, the higher the Young's modulus. It should be pointed out that, for a given underfill material, the Young's modulus is always larger than the storage modulus. The relationship between these two is not yet known.

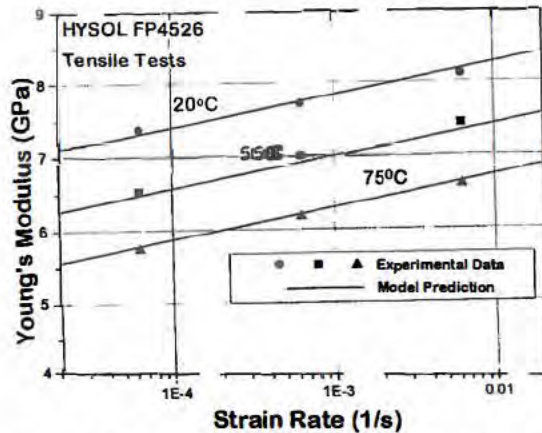


Figure 6.20 Strain rate and temperature dependence of Young's modulus of the HYSOL FP4526 underfill.

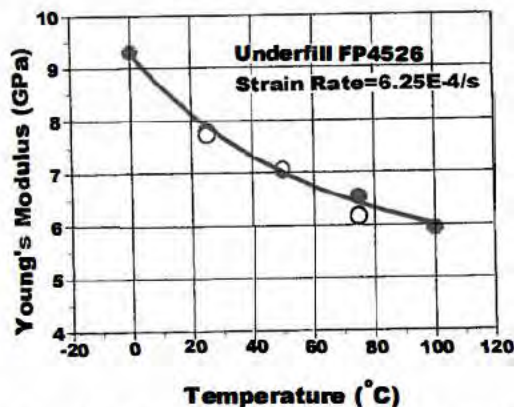


Figure 6.21 Temperature dependence of Young's modulus of the HYSOL FP4526 underfill at a certain strain rate.

6.7.6 Stress-strain relations^{189, 223}

The stress-strain relations of the HYSOL FP4526 underfill at different strain rates and temperatures have been determined.^{189, 223} Figures 6.22, 6.23, and 6.24 show the stress-strain relations of the underfill at different strain rates at 20, 50, and 75°C, respectively. For all the temperatures and strains, it can be seen that the higher the strain rates, the higher the stresses, and the higher the temperatures, the lower the stresses.

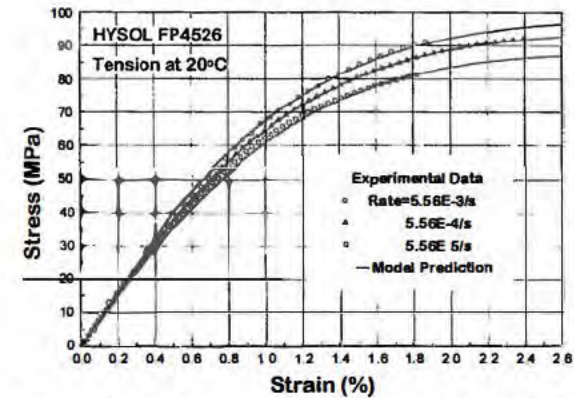


Figure 6.22 Stress strain relations of the HYSOL FP4526 underfill at different strain rates at 20°C.

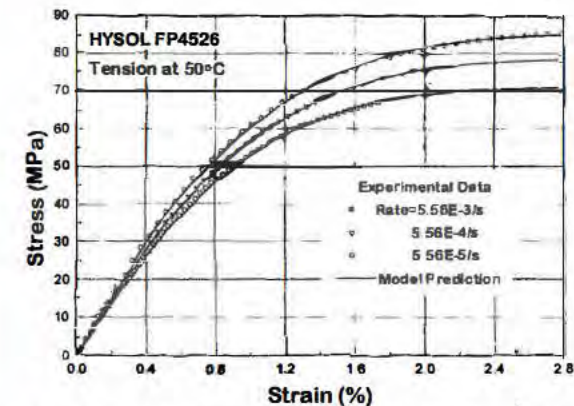


Figure 6.23 Stress strain relations of the HYSOL FP4526 underfill at different strain rates at 50°C.

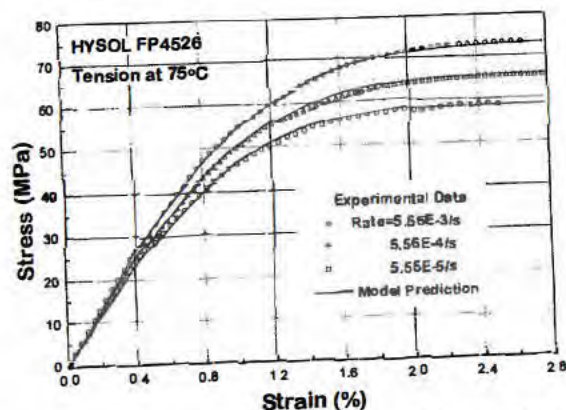


Figure 6.24 Stress-strain relations of the HYSOL FP4526 underfill at different strain rates at 75°C.

6.7.7 Creep curves^{189, 223}

The creep responses of the HYSOL FP4526 underfill at different temperatures and pressures have been obtained.^{189, 223} Figures 6.25 and 6.26 show the creep curves of the underfill at 20°C and 70 MPa, and at 75°C and 45 and 50 MPa. It can be seen that the creep responses of the HYSOL FP4526 underfill are dominated by transient (first-stage) creep. There is no tertiary-stage creep before the rupture of specimens. Also, for the same temperature, the higher the applied stresses, the higher the creep strains. Furthermore, a constitutive model for the underfill, which compares very well with the measurement data, has been developed.^{189, 223}

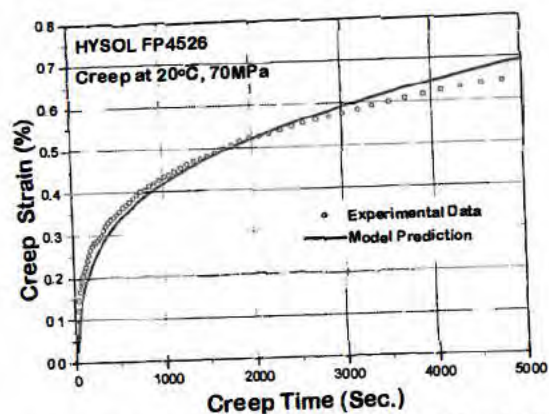


Figure 6.25 Creep curve of the HYSOL FP4526 underfill at 70 MPa and at 20°C.

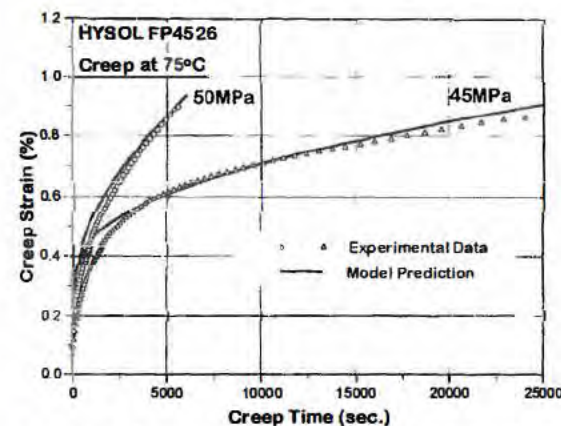


Figure 6.26 Creep curves of the HYSOL FP4526 underfill at 45 and 50 MPa and 75°C.

6.7.8 Fracture toughness of underfills²¹⁸

Fracture toughness is a material property in the same sense that yield strength is a material property. It is independent of crack length, geometry, or loading system. Physically, fracture toughness can be considered a material property that describes the inherent resistance of the material to failure in the presence of a cracklike defect (flaw). The unit for fracture toughness is $\text{MPa}\sqrt{\text{m}}$ or $\text{Psi}\sqrt{\text{in}}$.

The opening mode I (pure tensile load) fracture toughness (K_{IC}) of three different underfill materials has been determined by IBM²¹⁸ through the plane strain specimen shown in Fig. 6.27. The K_{IC} of

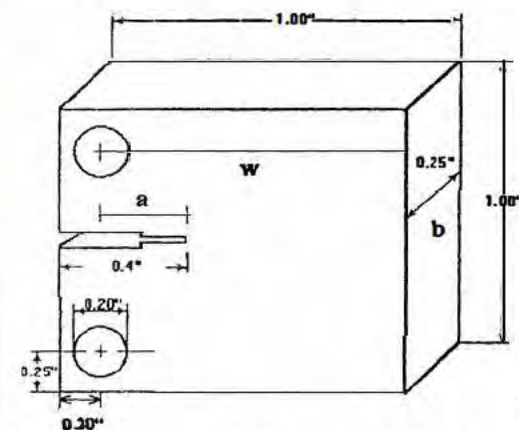


Figure 6.27 Schematics of a plane strain fracture toughness test specimen.

these underfill materials cured at temperatures between 100 and 200°C is shown in Fig. 6.28. It can be seen that, within the practice today (less than 170°C), the higher the curing temperature, the higher the K_{IC} .

Also, the fracture surfaces are different with different K_{IC} . For example, Fig. 6.29a (shown in macroscopic scale) is a typical fracture surface signified by the fanning-out river pattern for two different materials. However, on a smaller scale (Fig. 6.29b), the fracture surface of the tougher underfill material shows a consistent fish-scale pattern, which implies a localized plastic deformation as well as the directional change of crack front during propagation.²¹⁸

Furthermore, Fig. 6.30 shows the opening mode I tensile fracture surface of underfill materials with fillers. It can be seen that the weakest interface is the filler-epoxy interface, which implies that more flexible filler (absorbing more energy) or better interfacial adhesion might further improve the fracture toughness.²¹⁸

6.7.9 Fracture toughness of underfill-chip interfaces²¹⁴

Interfacial fracture toughness is a material property and is defined as the interface's resistance to decohesion. Quantitatively, it equals to the amount of energy (per unit area) required to separate a bonded inter-

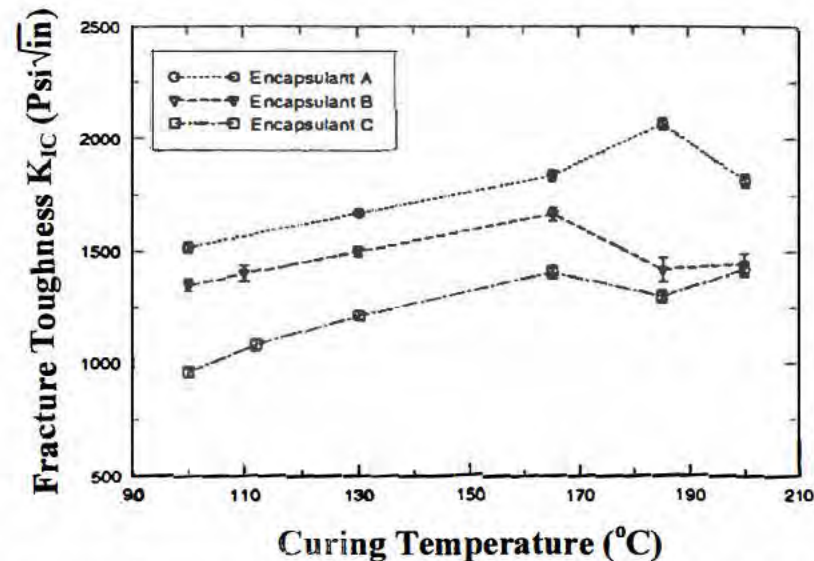
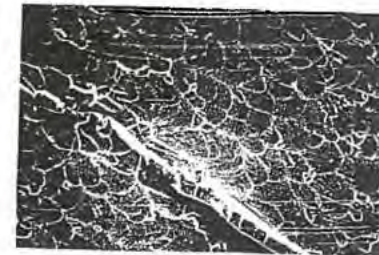


Figure 6.28 Fracture toughness under mode I loading of three underfills cured at various temperatures.



(a)



(b)

Figure 6.29 Tensile fracture surfaces on a macroscopic scale (a) and on a smaller scale (b).

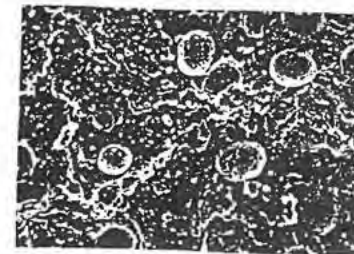


Figure 6.30 Tensile fracture surfaces of two underfills with fillers.

face between two different materials. The interfacial fracture toughness between different underfills and the chip surface and between different underfills and the PCB with solder mask surface has been determined by researchers at the Georgia Institute of Technology (GIT)²¹⁴ through four-point bending tests.

In Ref. 214, four different underfill materials are formulated by adding 1% (wt) of the selected silane coupling agents to a base resin (called Base) as shown in Table 6.4, where the storage modulus values for these materials are also given. The interfacial fracture toughness between these underfill materials and alumina, polyimide (PI), and benzocyclobutene (BCB) have been measured and are shown in Figs. 6.31 through 6.33, respectively.²¹⁴ It can be seen that, for all the cases considered (alumina, PI, and BCB), (1) underfill materials S1, S2, and S4 yield higher interfacial toughness than the base material, indicating that the silane additives in these materials enhance the interface toughness; (2) the epoxy functionalized silane has the maximum interfacial fracture toughness enhancement, and the methacrylate functionalized silane has no significant effect; and (3) the mode mixities are near 45°C (46.37 to 52.3°C), indicating that they are almost evenly mixed between open and shear modes of fractures. Also, for the interface between BCB and underfill, even the S3 material leads to higher interfacial toughness than the base material. Finally, it seems that PI yields the best results.

6.7.10 Fracture toughness of underfill-PCB interfaces²¹⁴

The interfacial toughness between the underfill materials and the FR-4 PCB with solder mask has also been obtained²¹⁴ and is shown in Fig. 6.34. It can be seen that (1) all the underfill materials containing silane additives yield higher interfacial toughness than the base material on FR-4 PCB with solder mask, and (2) just as on the chip surface, the epoxy functionalized silane has the maximum interfacial toughness enhancement, and the methacrylate functionalized silane has the minimum effect on the interface toughness of FR-4 PCB with solder mask. Also, it is interesting to note that the interface fracture toughness between the underfills and the FR-4 PCB with solder mask is greater than that between the underfills and the alumina, PI, and BCB on the chip surface.

6.8 Flow Rate of FCOB with Underfills

The flow rates of underfills A through J, discussed in Secs. 6.6 and 6.7.1 through 6.7.4, are measured underneath a solder-bumped flip chip on

TABLE 6.4 Storage Modulus of the Base Underfill and Four Underfills

	Storage Moduli (GPa)			
	Silane Coupling Agents with			
	Amine (S1)	Epoxy (S2)	Methacrylate (S3)	Vinyl Organofunctional (S4)
Base	3.03	3.18	3.17	3.43
				2.99

Underfills formulated by adding 1% (wt) of selected silane agents to the base resin.

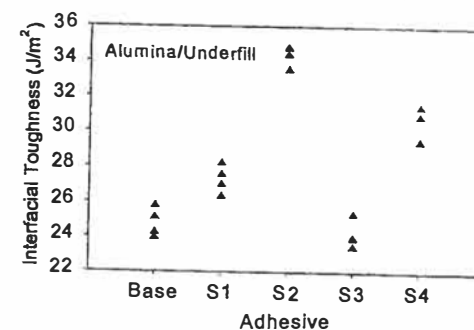


Figure 6.31 Interfacial fracture toughness of alumina/underfill interface.

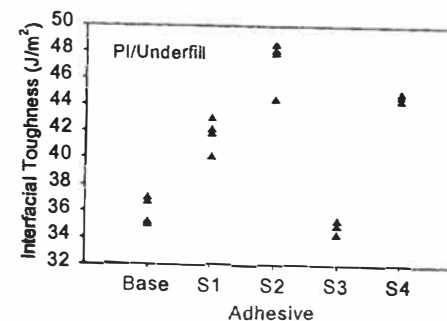


Figure 6.32 Interfacial fracture toughness of polyimide/underfill interface.

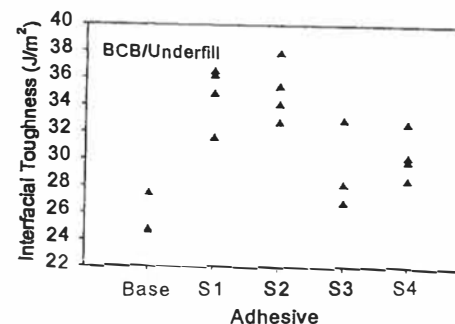


Figure 6.33 Interfacial fracture toughness of benzocyclobutene/underfill interface.

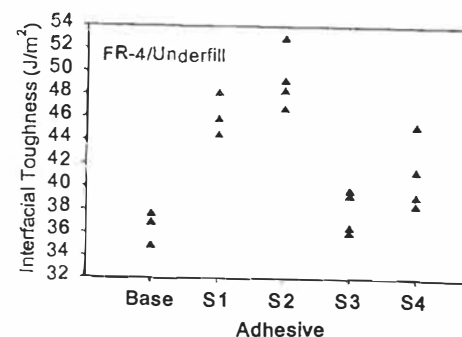


Figure 6.34 Interfacial fracture toughness of FR-4 with solder mask/underfill interface.

a BT substrate. The chips measure 6.3×3.6 mm and have 32 bumps. The BT substrate has two metal layers and 32 vias (0.254 mm in diameter). The standoff height of the solder bumps is 0.07 ± 0.02 mm.

The assembled flip chip is placed on a hot plate at 80 to 90°C. Approximately 0.025 cc of room-temperature underfill is placed around two chip sides in an L-shaped pattern. The time for the underfill to completely fill the gap is recorded. It should be pointed out that there is no flow of any underfill materials to the bottom side of the substrate. The average flow rates for underfills A through J are shown in Table 6.3. It can be seen that, in general, the smaller the filler size, the faster the flow rate.

6.9 Shear Test of FCOB with Underfills

Filler content, filler shape, filler size, and polymer type all affect the mechanical performance of underfill materials. Homogeneous mixing of fillers in epoxy is very difficult to achieve, since most of the underfill is particle-reinforced polymer. Furthermore, porosity or void absorbs moisture and serves to reduce the amount of load-bearing of the underfill materials. The Royce Instruments Model 550 is used to perform the mechanical shear tests. The shear wedge is placed very close to the substrate and against one edge of the solder-bumped flip chip with underfill on the BT substrate, which is clamped on the stage. A push of the wedge is applied to shear the chip/bumps/underfill away. The speed of the shear wedge is 0.004 in./s (0.1 mm/s).

6.9.1 Test results

Mechanical shear testing is performed on four sets of specimens: dry, steam-aged, 85°C/85 percent RH for 168 h, and level 1 precondition (reflow 3 times after 168 h at 85°C/85 percent RH). The average test results for underfills A through J are shown in Table 6.5, and shear force for different underfills in the solder-bumped flip chip on board is shown in Fig. 6.35. It can be seen from Table 6.5 that the average shear force varies with the different underfills under consideration. It can also be seen that, in most of the cases, the shear force of the solder-bumped flip chip with underfill is about the same for moisture soak and after 20 h of steam aging. Underfills E and I show better adhesion after the level 1 precondition, probably due to the reflow temperature (220°C maximum), which helps the underfills to be fully cured. (The curing temperature for underfills E and I is very high compared with the rest, Table 6.1.)

6.9.2 Failure modes

In general, there are four types of failures that occur under shear testing. The first occurs when the underfill has good adhesion with the chip

TABLE 6.5 Effects of Moisture on Mechanical Shear Test Performance of FCOB with Underfills A Through J

Underfill	Shear force (kgf)				Percent Drop After 85°C/85% RH
	Dry Conditions	85°C/85% RH	20 Hours of Steam Aging	Level 1 Precondition	
A	52.2	31.6	30.1	34.3	39.5
B	53.3	35.4	25.4	32.2	33.6
C	51.2	45	46.7	34.4	12.1
D	44.8	33	32.7	34.2	26.3
E	47.6	34.5	31.2	54.8	27.5
F	46.3	33.2	32.2	34	28.3
G	68.6	33.7	32.7	32.1	50.9
H	72.7	35	29.5	30.8	51.9
I	73.4	28.2	27.6	57.5	61.6
J	40.4	23.3	30.2	29.5	42.3

and the PCB. For example, Fig. 6.36 shows the chip with underfill A and most of the solder mask from the PCB. Figure 6.37 shows the corresponding PCB surface with very little solder mask. This phenomenon occurs for most of the samples under dry conditions. Figure 6.38 shows another example of this type of failure, in which the chip is broken into pieces and some broken chips still remain on the substrate. This happens for most of the samples under moisture conditions.

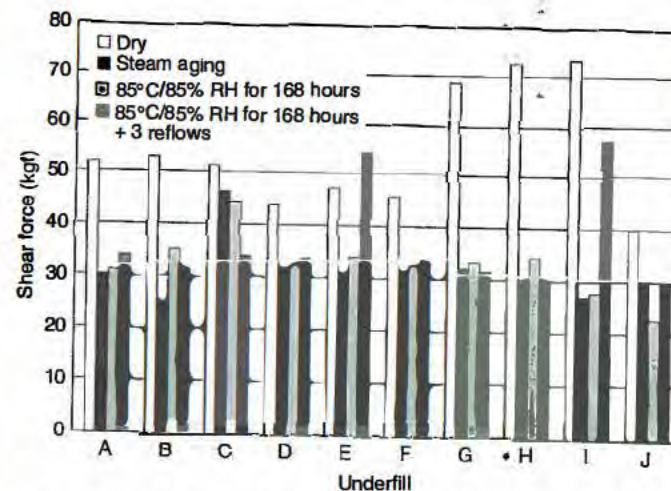


Figure 6.35 Shear force for solder bumped flip chip assemblies with different underfills under dry conditions, steam aging, 85°C/85% RH for 168 hours, and 85°C/85% RH for 168 hours + 3 SMT reflows.



Figure 6.36 Die surface with solder mask and underfill.

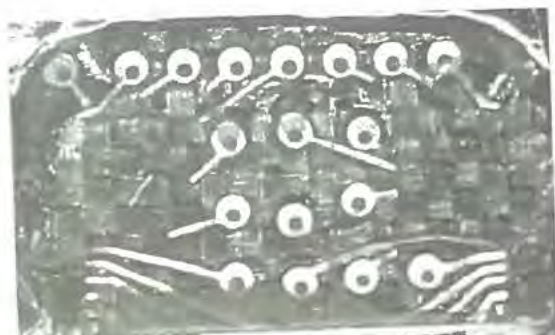


Figure 6.37 Substrate surface without solder mask.

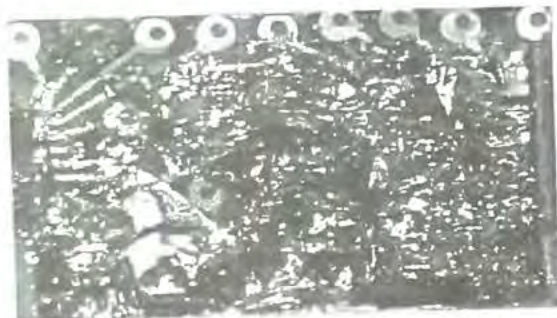


Figure 6.38 Substrate surface with partial underfill and broken chips.

The second type of failure under shear testing occurs when the underfill has good adhesion with the chip and poor adhesion with the solder mask. Figure 6.39 shows the chip with most of the underfill and very little solder mask. Figure 6.40 shows the corresponding PCB surface with most of the solder mask and very little underfill remaining. This happens for most of the samples under moisture conditions.

The third type of failure under shear testing occurs when the underfill has good adhesion with the solder mask on the PCB and poor adhesion with the passivation of the chip. Figure 6.41 shows the PCB with most of the underfill. The corresponding chip surface is clean (not shown). This means that the adhesion between the underfill and the solder mask is stronger than that between the underfill and the passivation of the chip.

The fourth type of failure under shear testing occurs when the underfill has good adhesion with the solder mask on the PCB and poor



Figure 6.39 Die surface of flip chip with most of the underfill and very little solder mask.



Figure 6.40 Substrate surface with most of the solder mask and very little underfill.



Figure 6.41 Substrate surface with most of the underfill.

adhesion with the chip due to passivation cracking. This type of failure on the PCB is very similar to that illustrated in Fig. 6.41.

It should be noted that the purpose of the destructive shear tests is to quantify the strength of these underfills. It does not mean that underfill is not reliable to use. How is an underfill material selected? The answer is not easy, since the performance of underfill depends on many factors such as, among others, the curing temperature and time, the TCE value, the storage modulus, the Young's modulus, the glass transition temperature, the moisture uptake, the flow rate, the shear strength, the fracture toughness, and the adhesion strength. However, based on the measurement data for the 10 different underfill materials under consideration, a simple method has been proposed to rank (select) the proper underfill. Interested readers are encouraged to read Ref. 170.

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