

Semiconductor Chip Underfill Materials

Flip chip interconnection of silicon devices involves inverting a chip with a two-dimensional array of solder balls and bonding the solder to a corresponding array of metal pads on a chip carrier or printed circuit card. This packaging technology is particularly important when the number of connections on a silicon die is greater than can be handled by wirebonding peripheral pads on the die to a leadframe in a conventional plastic package (see Fig. 1). The short interconnection path of the solder joints in flip chip interconnections also provides a strong electrical performance advantage over the relatively long wirebonds.

Reinforcement of the area-array solder connections in flip chip packages with a thermosetting polymeric resin has become an essential part of flip chip packaging, especially in the rapidly growing applications where the chip carrier is an epoxy laminate substrate with a coefficient of thermal expansion (CTE) significantly larger than that of silicon (Wu *et al.* 1996). The reinforcing resin is referred to as an underfill because it is applied in prepolymer form as a liquid that is allowed to fill the cavity under the chip. The underfill is needed, for without it the strain on the solder joints during device on/off cycles is sufficient to cause early package failure from solder fatigue. Thus, the underfill encapsulant provides a protective function analogous

to the epoxy molding compounds that surround the fragile wirebonds in a conventional plastic package.

1. Flip Chip Underfill Applications

The accelerating growth of portable consumer products for both information processing and communication has increasingly required miniaturization of electronic components to reduce product weight and size. Flip chip packaging with underfill is showing strong growth because it enables increased functionality without increasing product weight and size. As a comparison, a typical microprocessor chip packaged as a quad flat package, a conventional molded plastic package with wirebonds to a metal leadframe, requires $0.787\text{ in} \times 0.787\text{ in}$ ($2\text{ cm} \times 2\text{ cm}$); as a stand-alone flip chip package on an organic chip carrier, $0.334\text{ in} \times 0.384\text{ in}$ ($0.8\text{ cm} \times 1\text{ cm}$); and as a flip chip directly attached to the mother board, $0.216\text{ in} \times 0.266\text{ in}$ ($0.5\text{ cm} \times 0.7\text{ cm}$) (D. R. Gamota, Motorola Corp., unpublished data, 1997). This size reduction, along with the corresponding increase in semiconductor integration, has allowed designers to develop versatile, lightweight products for the consumer with greatly increased functionality.

2. Underfill Material Properties

To meet both processing and device protection requirements, underfill materials must have a variety of properties both in the uncured and cured states (Suryanarayana *et al.* 1993, Wang and Papathomas 1993, Koh and Ryan 1995). Some of the most important are reviewed below.

2.1 Composition

Commercial underfills are proprietary compositions from various material suppliers. Epoxy thermosetting resins are the predominant materials, but other thermosets such as cyanate esters are also used. Underfills are formulated as 100% solids compositions, i.e., liquid resins and hardeners are used without solvents or volatile additives. Thermal curing of these compositions generates a hard plastic material without appreciable weight loss.

2.2 Filler

Underfills are commonly formulated with 60–70% by weight of amorphous, fused silica. The silica is used to reduce the CTE of the underfill material because without filler the CTE of the cured polymer would cause unacceptable solder joint strain. Generally, underfill formulations have CTEs of $25\text{--}30\text{ ppm }^{\circ}\text{C}^{-1}$, which closely approximates to that of solder.

Fillers, if not chosen carefully, can increase the viscosity of the formulation to the point that it will not flow under the chip to fully encapsulate the solder

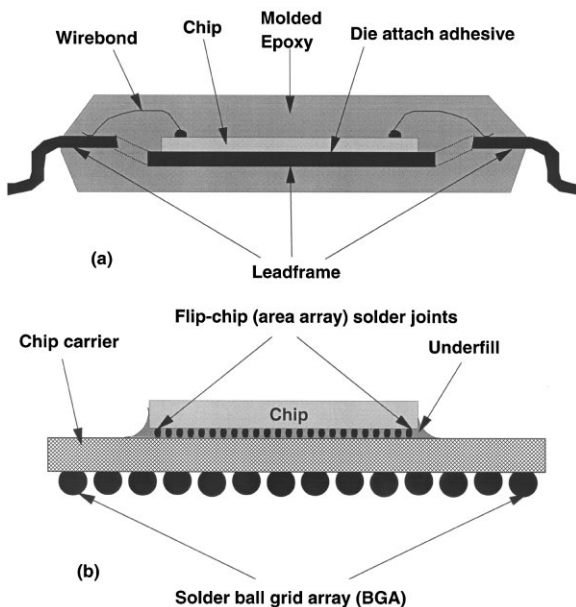


Figure 1

Schematic cross-sections of typical packages (not to scale): (a) surface mount plastic package; (b) flip chip plastic ball grid array (PBGA) package.

joints. For this reason, a special class of high-purity, spherical silica of controlled particle size distribution has been developed for underfills. Using these fillers, underfills typically are formulated to have room-temperature viscosities of 5×10^3 – 1×10^4 cPs (5 – $10 \text{ kg m}^{-1} \text{ s}^{-1}$), which allow encapsulation of the solder joints by capillary flow at a rate acceptable for manufacturing.

2.3 Cure

Underfills are formulated as thermosets rather than thermoplastics, primarily because the viscosity of solvent-free, high-performance thermoplastics is much too high for the encapsulation process. As thermosets, underfills have to be cured by heating after encapsulation, and full cure is essential to optimize properties such as adhesion, glass transition temperature (T_g), and modulus. Manufacturing throughput considerations demand short cure cycles, preferably compatible with in-line processing. However, most underfills are cured in batch curing ovens at about 150°C for one hour or more to assure acceptable reliability of the packages.

2.4 Glass Transition Temperature (T_g)

The glass transition temperature of a polymer is the temperature region of the change from a rigid “glassy” state to a flexible “rubbery” state. Most properties of thermosets, including underfills, undergo step changes at T_g . For example, the modulus of a cured underfill decreases more than ten-fold above T_g as do the cohesive and adhesive strengths. Electrical properties, heat capacity, and chemical resistance also all decrease above T_g . Accordingly, the T_g of cured underfills should be higher than any temperature experienced by the package in the field.

2.5 Elastic Modulus

The function of an underfill is to link mechanically the silicon chip to its carrier, creating a structure that eliminates or drastically reduces the strain on the individual solder joints. The optimum modulus will depend on the application, and is affected by the difference in CTE of the chip and chip carrier, the modulus of the chip carrier, and the CTE of the underfill. A typical value for underfill modulus is about 9 GPa (1.3 Mpsi) at 25°C .

2.6 Adhesion

Underfill adhesion is the most important property for maintaining reliability of flip chip assemblies. Without

durable adhesion, the solder joint reinforcement provided by the underfill is short-lived because as soon as the underfill loses adhesion to one or more surfaces, the thermal stresses are transferred directly to the solder joints. An underfill must have good adhesion to multiple surfaces: the chip passivation, the edges of the silicon chip, the surface of the chip carrier, and the solder itself. Adhesion must also be maintained despite exposure to moisture and thermal stressing.

Adhesive properties of polymers are often affected by moisture. As a small, polar molecule, water easily diffuses through polymers and can adsorb at an interface, disrupting adhesive bonding. The micro-electronic packaging industry has developed a set of criteria to classify the resistance of packages to moisture effects, called JEDEC levels 1–5 (JEDEC 1995). The levels differ in the aggressiveness of the moisture stress, which precedes other reliability testing such as simulated solder reflow and thermal shock testing.

3. Processing

An underfill material is dispensed from automatic syringe equipment as a low-viscosity suspension of silica in prepolymer, flows by capillary action between chip and chip carrier through and around the pre-formed solder joints between them, and is thermally cured in place to achieve the desired encapsulant properties. The most important consideration in this process is prevention of voids because they undermine

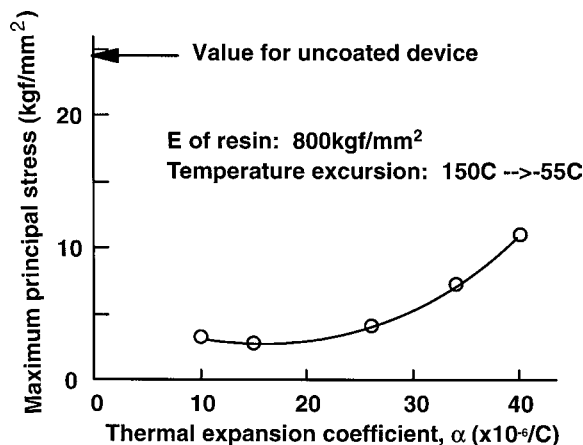


Figure 2

Relationship of maximum thermal stress of solder joints and underfill CTE and comparing stress with no underfill (reproduced by permission of the International Microelectronics and Packaging Society from ‘Proc. Int. Symp. on Microelectronics’ 1987, pp. 536–41).

solder joint reliability. Voids occur by irregularities in flow, or by trapping of volatiles during the curing step.

3.1 Underfill Flow

Underfill flow is complicated by the many variables that affect it, including viscosity, dispense pattern, temperature, surface energies of the package materials, underfill composition, chip-carrier topography, chip size and shape, and density of solder joints to be encapsulated (Schwiebert and Leong 1996, Lehmann *et al.* 1998). Consequently, development of a successful underfill flow process for manufacturing is an empirical process for each underfill and for each flip chip package. Void detection is routinely done by scanning acoustic microscopy after underfill cure.

3.2 Trapping of Volatiles

Even if an underfill is purportedly 100% solids, a fast temperature ramp during curing can cause voids if resin components evaporate before they react into the thermoset matrix. The major source of void-causing volatiles, however, is absorbed moisture from the ambient. It is routine practice to bake out laminate chip carriers no more than a few hours before underfill application in order to be sure that all absorbed moisture is removed.

4. Thermal Stressing and Reliability

Microelectronic packages experience thermal stressing as a result of power on/off cycling of the devices. The difference in CTE of the materials in the package results in strains that in the case of flip chip solder joints will eventually lead to electrical failure. By distributing the stress across the whole flip chip structure, the underfill minimizes the strains on individual solder joints. The underfill effect has been modeled by calculating the solder joint strain with and without underfill. Without underfill, the CTE mismatch generates increasing levels of strain in the solder joints as one considers joints further out from the center of the chip. In the very first publication on underfills (Nakano *et al.* 1987), the large reduction in solder joint stress offered by underfill was already recognized (see Fig. 2). Strikingly, the effect of underfill has been experimentally confirmed using microscopic Moiré interferometry (Han and Guo 1995). Figure 3 shows an order of magnitude reduction in solder joint average shear strain. The net result is that solder joints without underfill fail within a few hundred thermal cycles in cases where the CTE mismatch is large, such as when flip chips are mounted on printed circuit cards, but survive for thousands of cycles with underfill (Baggerman *et al.* 1996, Popelar 1997).

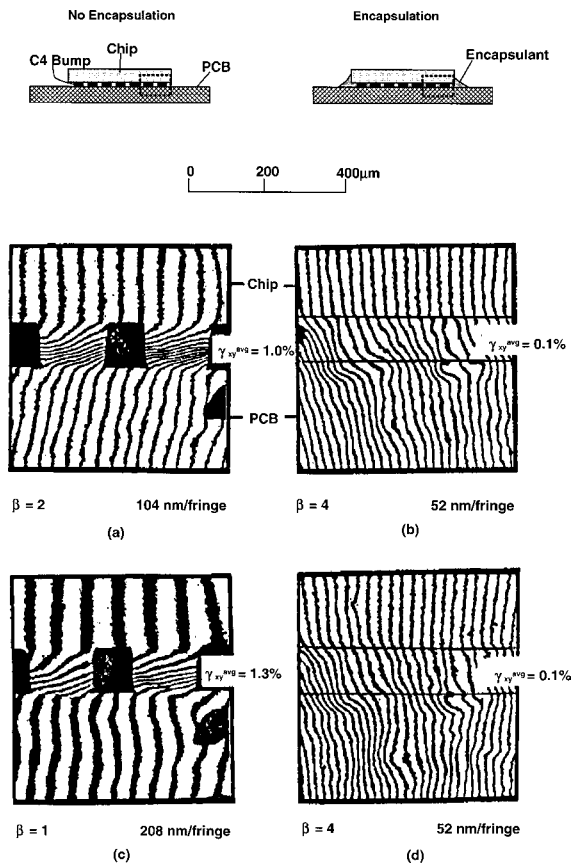


Figure 3

Moiré interferometry showing microscopic displacement field of solder joints, induced by thermal loading of $\Delta T = -60^\circ\text{C}$, (a) without underfill and (b) with underfill; and the corresponding displacement fields after 5 cycles of -40°C to 80°C (c) without underfill and (d) with underfill (reproduced by permission of the American Society of Mechanical Engineers from *J. Electron. Packaging Trans.* ASME, 1995, 117(2), 185–91).

The reinforcing effect of the underfill is completely dependent on its adhesion, however. For this reason, reliability testing of flip chip packages is largely a means of ascertaining how long the underfill adhesion at the weakest interface will survive under field conditions (Gektin *et al.* 1997).

5. Conclusions

Because of their ability to provide reliable, compact, and low-cost packaging solutions, underfills are becoming more important as applications for microelectronics proliferate along with the growth of internet appliances and wireless communication. Ongoing development of underfill materials and processes are

addressing manufacturing concerns regarding the time required for underfill flow and cure. With further improvements, flip chip packages with underfill could become the most pervasive package for semiconductors, especially for the rapidly growing applications requiring a high number of interconnections or superior electrical performance.

Bibliography

- Baggerman A F J, Caers J F J M, Wondergem J J, Wagemans A G 1996 Low cost flip chip on board. *IEEE Trans. Components, Packages, Manufact. Technol. B* **19** (4), 736–46
- Gektin V, Bar-Cohen A, Ames J 1997 Coffin–Manson fatigue model of underfilled flip chips. *IEEE Trans. Components, Packages, Manufact. Technol. A* **20** (3), 317–26
- Han B, Guo Y 1995 Thermal deformation analysis of various electronic packaging products by Moiré and microscopic Moiré interferometry. *J. Electron. Packaging Trans. ASME* **117** (2), 185–91
- JEDEC 1995 Moisture-induced stress sensitivity for plastic surface mount devices, EIA/JEDEC Standard EIA/JESD22-A112-A. Electronic Industries Association
- Koh W, Ryan L 1995 Materials used in direct chip attach (flip chip-on-board) applications. *Proc. 27th Int. SAMPE Tech. Conf. SAMPE*, pp. 96–103
- Lehmann G L, Driscoll T, Guldosh N R, Li P C, Cotts E J 1998 Underflow process for direct chip attachment packaging. *IEEE Trans. Components, Packages, Manufact. Technol. A* **21** (2), 266–74
- Nakano F, Soga T, Amagi S 1987 Resin insertion effect on thermal cycle resistivity of flip chip mounted LSI devices. *Proc. Int. Symp. Microelectronics. ISHM*, Minneapolis, MN, pp. 536–41
- Popelar S F 1997 Parametric study of flip chip reliability based on solder fatigue modelling. *Proc. IEEE/CPMT Int. Electronics Manufacturing Technology Symp.* IEEE, Austin, TX, pp. 299–307
- Schwiebert M K, Leong W H 1996 Underfill flow as viscous flow between parallel plates driven by capillary action. *IEEE Trans. Components, Packages, Manufact. Technol. C* **19**, 133–7
- Suryanarayana D, Wu T Y, Varcoe J A 1993 Encapsulants used in flip chip packages. *IEEE Trans. Components, Hybrids, Manufact. Technol.* **16** (8), 858–62
- Wang D W, Papathomas K I 1993 Encapsulant for fatigue life enhancement of controlled collapse chip connection (C4). *IEEE Trans. Components, Hybrids Manufact. Technol.* **16** (8), 863–7
- Wu T Y, Tsukada Y, Chen W T 1996 Materials and mechanics issues in flip chip organic packaging. *Proc. 46th IEEE Electronic Components Technology Conf.* IEEE, Orlando, FL, 524–34

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