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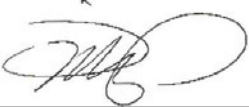
I, Alex Jo, declare:

I am a professional reviewer and coordinator specializing in translating Chinese, Japanese and Korean to English.

I have over 30 years of experience reviewing and coordinating translations of thousands of technical, legal, and business documents from Chinese to English submitted to, among others, various U.S. federal courts, the U.S. International Trade Commission (ITC), and the Patent Trial and Appeal Board (PTAB).

I certify that the following Japanese to English translation of the corresponding source text is a true, correct, and complete translation to the best of my knowledge and ability.

I hereby certify under penalty of perjury that the foregoing is true and correct. Executed this 5th day of December 2022 in the Contra Costa County of the State of California.

By: 

Alex Jo
Member, ATA

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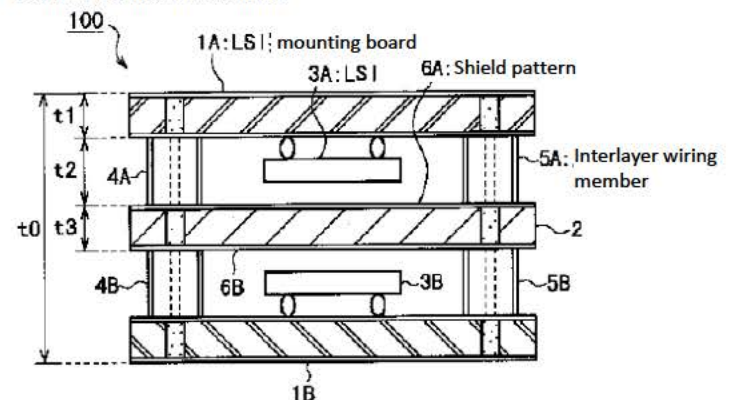
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(22) Filed:		Oct. 6, 1999				SONY CORP.	
						6-7-35 Kitashinagawa, Shinagawa-ku,	
						Tokyo	
				(72) Inventor:		Yoichi OYA	
						% SONY CORP.	
						6-7-35 Kitashinagawa, Shinagawa-ku,	
						Tokyo	
				(72) Inventor:		Emi NAKAMURA	
						% SONY MINOKAMO CORP	
						9-15-22 Hongo-cho, Minokamo, Gifu	
						Prefecture	
				(74) Agent or attorney:		100090376	
						Kunio YAMAGUCHI, patent attorney (and	
						one other)	
						Continued to last page	

(54) (TITLE) ELECTRONIC COMPONENT MOUNTING MULTILAYER BOARD AND MANUFACTURING METHOD THEREOF

(57) (ABSTRACT) To increase the mounting surface area of shielded electronic components three-dimensionally in the lamination direction.

(MEANS TO SOLVE THE PROBLEM) Provided are LSI mounting boards 1A and 1B mounted on one surface with LSI chips 3A and 3B, interlayer wiring members 4A, 4B, 5A, and 5B for interlayer connection provided between the LSI mounting boards, and shield patterns 6A and 6B of a prescribed size provided at least on an inner layer wiring board 2 on a side facing the LSI chip 3A in a region defined by the interlayer wiring members 4A, 4B, 5A, and 5B, the LSI mounting boards 1A and 1B being laminated with the interlayer wiring members 4A, 4B, 5A and 5B sandwiched therebetween, and the LSI mounting board interval being joined electrically by the interlayer wiring members 4A, 4B, 5A, and 5B to form a multilayer structure.

Structural example of the electronic component mounting multilayer board as the first embodiment



(CLAIMS)

(CLAIM 1) An electronic component mounting multilayer board characterized in being provided with a plurality of mounting boards mounted on one or both sides with electronic components, an interlayer wiring member for interlayer connection provided between the mounting boards, and a conductive member for shielding of a prescribed size provided at least on a mounting board on a side facing the electronic components in a region defined by the interlayer wiring member, and that a multilayer structure is formed by laminating the mounting boards with the interlayer wiring member sandwiched therebetween and electrically connecting the mounting board interval with the interlayer wiring member.

(CLAIM 2) The electronic component mounting multilayer board set forth in claim 1 characterized in being provided with a first mounting board mounted with the electronic components and a second mounting board laminated with the interlayer wiring member sandwiched so as to face the electronic components, a conductive member with a prescribed size being provided on a second mounting board on a side facing the electronic components, and the conductive member being grounded.

(CLAIM 3) The electronic component mounting multilayer board set forth in claim 1 characterized in that in the case where the essential parts of the interlayer wiring member are configured from an insulating material, a conductive member is provided on the inside surface, core or outside surface of the insulating material, and the conductive member is grounded.

(CLAIM 4) The electronic component mounting multilayer board set forth in claim 1 characterized in that the mounting board has a cavity structure provided with a groove or hole for housing electronic components.

(CLAIM 5) The electronic component mounting multilayer board set forth in claim 1 characterized in that in the case where the interlayer wiring member is configured from a conductive material, the conductive material has a wall, pillar, or spherical shape.

(CLAIM 6) A method for manufacturing an electronic component mounting multilayer board characterized in having a step of forming a mounting board with electronic components mounted on one or both sides and forming a conductive member for shielding of a prescribed size on another mounting board on a side facing the electronic components, a step of laminating the mounting board interval with an interlayer wiring member for interlayer connection sandwiched therebetween such that the electronic components face the conductive member, and a step of electrically joining the mounting board interval with the interlayer wiring member.

(CLAIM 7) The method for manufacturing an electronic component mounting multilayer board set forth in claim 6 characterized in that the step of laminating and joining the mounting board interval with the interlayer wiring member sandwiched therebetween and the step of electrically joining the mounting board interval with the interlayer wiring member are carried out in the same heat treatment step.

(CLAIM 8) The method for manufacturing an electronic component mounting multilayer board set forth in claim 6 characterized in that the mounting board is formed with the electronic components mounted and then

an electrical inspection is carried out on each mounting board.

(CLAIM 9) The method for manufacturing an electronic component mounting multilayer board set forth in claim 6 characterized in that an electrode for an operation inspection is lead out from the mounting board mounted with the electronic components.

(CLAIM 10) The method for manufacturing an electronic component mounting multilayer board set forth in claim 9 characterized in that the electrode for an operation inspection also serves as an electrode for electrically connecting the interlayer wiring member.

(CLAIM 11) The method for manufacturing an electronic component mounting multilayer board set forth in claim 6 characterized in that the conductive member for shielding is grounded.

(DETAILED DESCRIPTION OF THE INVENTION)**(0001)**

(TECHNICAL FIELD) The present invention relates to an electronic component mounting multilayer board favorable for application to a mobile terminal device with high-density mounting of semiconductor integrated circuit devices and electronic components such as passive elements and a manufacturing method therefor. In further detail, an interlayer wiring member for interlayer connection is provided between mounting boards mounted with electronic components opposing a conductive member for shielding, mounting boards sandwiching the interlayer wiring member are laminated, and the mounting board interval is electrically joined by the interlayer wiring member so that the mounting surface area of shielded electronic components can be increased three-dimensionally in the lamination direction.

(0002)

(PRIOR ART) In recent years, LSI mounting boards mounted with bare chip semiconductor integrated circuit devices (hereinafter referred to simply as LSI chips) have come to be used in mobile phones and mobile terminal devices such as portable personal computers. Individual LSI chips are not molded in this type of mounting board. Rather a plurality of LSI chips are arranged two-dimensionally on one surface of the mounting board, and electronic components such as resistors and capacitors are mounted on the other surface. As a measure against noise between proximate circuits, shielding is provided by covering individual LSI chips with a metal case.

(0003)

(PROBLEM THE INVENTION IS TO SOLVE) However, according to a conventional LSI mounting board, the LSI chips are arranged two-dimensionally, so a limitation has been reached in the component mounting surface area despite a need for the high-density mounting of electronic components. Accordingly, it is not possible to satisfy the demand for printed wire board miniaturization, i.e., electronic device miniaturization. In addition, with electronic device miniaturization, the problem of noise between proximate circuits has arisen.

(0004) In response to this kind of problem, "MULTILAYER ELECTRONIC CIRCUIT BOARD AND MANUFACTURING METHOD THEREOF" in Japanese Patent Application Publication No. H2-164096, which is a patent document, describes building circuit elements composing an electronic circuit between printed wiring board layers and achieving the high-density mounting of electronic circuits. Also, "MULTILAYER PRINTED WIRING BOARD AND MANUFACTURING METHOD THEREOF" of Japanese Patent Application Publication No. H5-343856 describes sandwiching a hybrid module composing an electronic circuit and the like between printed wiring boards for the high-density mounting of electronic circuits and the like.

(0005) "MULTILAYER HIGH-DENSITY MOUNTING MODULE" of Japanese Patent Application Publication No. H3-14293 describes when laminating printed wiring boards with electronic circuits and the like built into the intermediate layers, applying platinum or palladium plating to the surface in contact with the solder bumps. While the mounting surface area for electronic components is increased three-dimensionally in the lamination direction in all of these technical documents, the mounting surface area for shielded electronic components cannot be increased three-dimensionally in the lamination direction.

(0006) The present invention solves such a conventional problem, and it is an object of the present invention to provide an electronic component mounting multilayer board in which the mounting surface area of shielded electronic components can be increased three-dimensionally in the lamination direction and a manufacturing method thereof.

(0007)

(MEANS TO SOLVE THE PROBLEM) The problem described above is solved by an electronic component mounting multilayer board characterized in being provided with a plurality of mounting boards mounted on one or both sides with electronic components, an interlayer wiring member for interlayer connection provided between the mounting boards, and a conductive member for shielding of a prescribed size provided at least on a mounting board on a side facing the electronic components in a region defined by the interlayer wiring member, and that a multilayer structure is formed by laminating the mounting boards with the interlayer wiring member sandwiched therebetween and electrically joining the mounting board interval with the interlayer wiring member.

(0008) According to the electronic component mounting multilayer board of the present invention, an interlayer wiring member for interlayer connection is provided between mounting boards mounted with electronic components facing a conductive member for shielding, the mounting boards are laminated with the interlayer wiring member sandwiched therebetween, and the mounting board interval is electrically joined by the interlayer wiring member to form a multilayer structure.

(0009) Accordingly, it is possible to three-dimensionally increase in the lamination direction the mounting surface area of electronic components shielded by a conductive member of a prescribed size, and shielded electronic components can be mounted more densely than when shield-mounting electronic components two-dimensionally.

(0010) The method for manufacturing an electronic component mounting multilayer board of the present invention is characterized in having a step of forming a mounting board with electronic components mounted on one or both sides and forming a conductive member for shielding of a prescribed size on another mounting board on a side facing the electronic components, a step of laminating the mounting board interval with an interlayer wiring member for interlayer connection sandwiched therebetween such that the electronic components face the conductive member, and a step of electrically joining the mounting board interval with the interlayer wiring member.

(0011) According to the method for manufacturing an electronic component mounting multilayer board of the present invention, the mounting surface area of shielded electronic parts can be increased three-dimensionally in the lamination direction, and shielded electronic components can be mounted more densely

than when shield-mounting electronic components two-dimensionally.

(0012)

(EMBODIMENTS FOR WORKING THE INVENTION) Next, embodiments of the electronic component mounting multilayer board and the manufacturing method thereof according to the invention are described with reference to the drawings.

(1) First embodiment

FIG. 1 is a cross-section view showing a configuration example of the electronic component mounting multilayer board as a first embodiment. In this embodiment, interlayer wiring members for interlayer connections are provided between mounting boards mounted with electronic components facing conductive members for shielding, and the mounting boards are laminated with the interlayer wiring members sandwiched therebetween and the mounting board interval is electrically joined by the interlayer wiring members, making it possible to increase the mounting surface area for shielded electronic components three-dimensionally in the lamination direction.

(0013) An electronic component mounting multilayer board 100 shown in FIG. 1 is mounted in high-density with electronic components such as semiconductor integrated circuit devices (LSI chips). The LSI chips are around hundreds of μm thick, the electronic component mounting multilayer board 100 is t_0 thick, from around 1 mm to several mm depending on the electronic component lamination count. In the example shown in FIG. 1, an LSI mounting board 1A that has a thickness of t_1 and is mounted on one surface with an LSI chip 3A is laminated on one surface of an inner layer wiring board (second mounting board) 2 with interlayer wiring members 4A and 5A for interlayer connection sandwiched therebetween, the interval of the LSI mounting board 1A and the inner layer wiring board 2 is electrically joined by the interlayer wiring members 4A and 5A, another LSI mounting board 1B is mounted on the other surface of the inner layer wiring board 2 with other interlayer wiring members 4B and 5B for interlayer connection sandwiched therebetween, and the interval of the LSI mounting board 1B and the inner layer wiring board 2 are electrically joined by the interlayer wiring members 4B and 5B to form a multilayer structure.

(0014) That is, the interlayer wiring members 4A and 5A for interlayer connection are provided between the LSI mounting board 1A and the inner layer wiring board 2, the interlayer wiring members 4B and 5B are provided between the LSI mounting board 1B and the inner layer wiring board 2, and said interlayer wiring members have at least three functions, i.e., the nature of being a frame supporting the LSI mounting boards 1A and 1B and the inner layer wiring board 2, a signal line path for propagating signals and the like, and a shield wall for shielding the LSI chips 3A and 3B, signal lines and the like.

(0015) Conductive members 6A and 6B for shielding with a prescribed size are provided at least on mounting boards on the sides facing the LSI chips 3A and 3B, that is, both sides of the inner layer wiring board 2, in a region defined by the interlayer wiring members 4A, 5A, 4B and 5B. Copper foil or the like is used for the conductive members 6A and 6B, and the copper foil patterns (hereinafter called the shield patterns) 6A and 6B for shielding are grounded. The shield patterns 6A and 6B are formed at the same time as the wiring patterns during formation of the inner layer wiring board 2, leading to reduced costs due to a simpler multilayer board structure and a shortened manufacturing process.

(0016) The size of the shield patterns 6A and 6B is preferably greater than the upper projection surface area of the LSI chips 3A and 3B. That is to increase the electromagnetic and static electricity shield effects. In this example, the LSI chip 3A below the LSI mounting board 1A is electromagnetically shielded by the shield pattern 6A on the upper surface of the inner layer wiring board 2, and similarly, the LSI chip 3B on the LSI mounting board 1B is electromagnetically shielded by the shield pattern 6B on the lower surface of the inner layer wiring board 2.

(0017) The electronic components are not limited to being mounted on one surface of the mounting board, but may be mounted on both sides. For example, the LSI chips 3A and 3B may be mounted on one surface and passive elements such as a chip-like resistor and capacitor may be mounted on the other surface, or the LSI chips 3A and 3B may be mounted on both sides. This is for high-density mounting of electronic components.

(0018) In this manner, according to the electronic component mounting multilayer board 100 as the first embodiment, the LSI mounting board 1A mounted with the LSI chip 3A on one surface facing the shield pattern 6A is laminated on one surface of the inner layer wiring board 2 with the interlayer wiring members 4A and 5A for interlayer connection sandwiched therebetween, the interval of the LSI mounting board 1A and the inner layer wiring board 2 are electrically joined by the interlayer wiring members 4A and 5A, the LSI mounting board 1B mounted with the other LSI chip 3B facing the shield pattern 6B is laminated on the other surface of the inner layer wiring board 2 with the other interlayer wiring members 4B and 5B for interlayer connection sandwiched therebetween, and the interval of the LSI mounting board 1B and the inner layer wiring board 2 is electrically joined by the interlayer wiring members 4B and 5B to form a multilayer structure.

(0019) Accordingly, the mounting surface area of the LSI chips 3A and 3B electrically shielded by the shield patterns 6A and 6B of a predetermined size can be three-dimensionally increased in the lamination direction, and the shielded LSI chips 3A and 3B can be mounted at higher density than when shield-mounting two-dimensionally. Moreover, cross-talk due to noise between proximate circuits can be prevented by the shield patterns 6A and 6B provided between laminations. It is thereby possible to miniaturize and improve the reliability of electronic devices to which the electronic component mounting multilayer board 100 is applied.

(0020) Next, the method for manufacturing the electronic component mounting multilayer board 100 is described. FIG. 2 to 6 are process diagrams showing formation examples (1 to 5) of the electronic component mounting multilayer board 100. In this example, conductive members for shielding with a prescribed size are formed on both sides of the inner layer wiring board 2. Copper foil or the like is used for the conductive members. The shield patterns 6A and 6B are formed at the same time as the wiring patterns, and the shield patterns 6A and 6B of each layer are assumed to be commonly connected to the

ground line through-holes, for example, of the interlayer wiring members 4A, 5A, 4B and 5B and grounded all at once during board mounting.

(0021) With this as a premise, first the LSI chip 3A and the LSI chip 3B are mounted to one surface of the mounting board 1 shown in FIG. 2 to form the LSI mounting boards 1A and 1B. This mounting board 1 is prepared in advance by processing a double-sided copper foil board such as a glass cloth substrate epoxy resin copper clad laminate board (FR-4) and forming a prescribed wiring pattern, electrodes (round) and the like.

(0022) For example, a resist material is applied on each surface side of the double-sided copper foil board, then a reticle (e.g., a negative film or a dry plate) formed as a wiring pattern, electrode or the like is used to expose the resist material, and then the resist film is masked and the copper foil etched to form a wiring pattern, electrodes, and the like. A polyimide resin copper clad laminated board or a bismaleimide triazine (BT resin) resin copper clad laminate board may be used for the double-sided copper foil board. These boards have superior heat resistance and dimension stability. The LSI chips 3A and 3B are joined via bump electrodes to a plurality of pad electrodes or the like formed in advance. The bump electrodes compose solder balls or spherical silver, gold, or the like.

(0023) In this example, electrodes 7 and 8 for operation inspections are led out from the LSI mounting boards 1A and 1B. The electrodes 7 and 8 for operation inspections are used to impress test voltages, supply test data, and extract result data. Terminals dedicated to testing may be provided as the electrodes 7 and 8, but from the perspective of minimizing the number of terminals, the electrodes originally connected to the signal input line and the signal output line, i.e., the round electrodes 7 and 8 for electrically connecting to the through-holes provided at the core of the interlayer wiring members 4A, 5A, 4B and 5B, are used.

(0024) Next, the inner layer wiring board 2 having the shield patterns 6A and 6B is formed on both sides of the double-sided board shown in FIG. 3. Naturally, the formation order of the LSI mounting boards 1A and 1B and the inner layer wiring board 2 is not so limited, and the LSI mounting boards 1A and 1B may also be formed after the inner layer wiring board 2. The shield patterns 6A and 6B are formed in advance to a prescribed size by etching the double-sided copper foil board. For example, the resist material is applied to each side of the double-sided copper foil board, and then the resist material is exposed using a reticle with the shape of the round electrodes 9 and 11 for the through-holes, the wiring or shield patterns 6A and 6B, or the like.

(0025) The shield patterns 6A and 6B are patterned so as to reach the through-holes for ground lines. Then the copper foil is etched using the resist film as a mask. As a result, the round electrodes 9 and 11 for the through-holes, the round electrodes that reach through-holes 12 for the ground lines, the printed wiring patterns, the shield patterns 6A and 6B, and the like are formed.

(0026) When the LSI mounting boards 1A and 1B and the inner layer wiring board 2 are formed, an electrical inspection is carried out on each mounting board using an LSI tester 10 such as that shown in FIG. 4 or the like. In this example, one LSI mounting board 1 can be handled as one circuit block, and when a fault occurs in the LSI mounting board 1 after mounting on the electronic component mounting multilayer board 100, it is possible to change only the LSI mounting board 1 with the fault, making maintenance and repairs easy.

(0027) In this example, the round electrodes 7 and 8 electrically connected to the plurality of through-holes provided at the core of the interlayer wiring members 4A and 5A and the interlayer wiring members 4B and 5B are used as the electrodes for operation inspections. Probes 13 and 14 of the LSI tester 10 are brought into contact with the plurality of electrodes 7 and 8, and a local mounting test is carried out on each circuit block. Naturally, test data prepared in advance specifically for the LSI mounting board 1A, the LSI mounting board 1B and the like is used for the mounting tests.

(0028) Accordingly, before the LSI mounting boards 1A and 1B and the inner layer wiring board 2 are laminated, defective LSI mounting boards 1A and 1B can be removed early. Only the LSI mounting boards 1A and 1B and the inner layer wiring boards 2 judged to have passing test results need to be laminated via the interlayer wiring members 4A, 5A, 4B and 5B for interlayer connection. The production yield of the electronic component mounting multilayer board 100 can be improved compared to when the electrical inspections are run after laminating all of the LSI mounting boards 1A and 1B and inner layer wiring board 2.

(0029) Next, the interlayer wiring members 4A and 5A for interlayer connection and the like are prepared as shown in FIG. 5. A double-sided copper foil substrate of, for example, glass cloth substrate epoxy resin copper clad laminate board (FR-4) is cut into the rectangular shape shown in FIG. 5 to make the essential parts of the interlayer wiring members 4A and 5A from the insulating materials 4 and 5. Through-holes 15A, 16A, and the like composing the signal output line to another circuit board, the signal input line from another circuit board, other power lines, ground lines and the like are provided in the core of the insulating materials 4 and 5, and both sides (the inner and outer sides) are formed with a copper foil (conductive member) 17 for shielding and grounded with the shield patterns 6A and 6B of the inner layer wiring board 2. The through-holes 15A and 16A are formed with a well-known method. The through-holes 15A and 16A may be formed into a hollow tube and filled with another conductor such as silver.

(0030) The copper foil 17 may be provided on both sides of the interlayer wiring members 4A and 5B or on only one side. If copper foil is provided (remains) on the inner surface, electromagnetic shielding can be efficiently provided three-dimensionally for the shield patterns 6A and 6B, the LSI chip 3A and the like, but if copper foil is provided (remains) on both sides, both the electromagnetic shielding effect of the LSI chip 3A and the like and the electromagnetic shielding effect of the signal output line and signal input line passing through the core

can be obtained. A description is omitted for the interlayer wiring members 4B and 5B as a configuration similar to that of the interlayer wiring members 4A and 5A is adopted.

(0031) Then, as shown in FIG. 6, the LSI mounting board 1A, the interlayer wiring members 4A and 5A, the inner layer wiring board 2, the interlayer wiring members 4B and 5B, and the LSI mounting board 1B are aligned and laminated. When doing so, the LSI mounting board 1A, the inner layer wiring board 2 and the LSI mounting board 1B are positioned such that the LSI chip 3A faces the shield pattern 6A surface and the LSI chip 3B faces the shield pattern 6B surface. The interlayer wiring members 4A and 5A for interlayer connection are sandwiched between the LSI mounting board 1A and the inner layer wiring board 2, and the interlayer wiring members 4B and 5B for interlayer connection are sandwiched between the inner layer wiring board 2 and the LSI mounting board 1B. In this state, the LSI mounting board 1A and the inner layer wiring board 2 are electrically and structurally joined by the interlayer wiring members 4A and 5A, and the inner layer wiring board 2 and the LSI mounting board 1B are electrically and structurally joined by the interlayer wiring members 4B and 5B with the interposition of an adhesive. For this joining, a hot-melt adhesive is interposed between members and the same pressure-heating step carried out.

(0032) For example, an anisotropic conductive resin is applied between members, a laminate comprising the LSI mounting board 1A, the interlayer wiring members 4A and 5A, the inner layer wiring board 2, the interlayer wiring members 4B and 5B and the LSI mounting board 1B is pressure-heated at about 170° C. As a result, the metal particles present in the resin burst, electrically connecting the board interval, the member interval is thermally bonded, and the electronic component mounting multilayer board 100 shown in FIG. 1 is formed. Moreover, the mounting surface area of the shielded LSI chips 3A and 3B can be three-dimensionally increased in the lamination direction, and the shielded LSI chips 3A and 3B can be mounted at higher density than shield-mounting the LSI chips 3A and 3B two-dimensionally. Also, connections can be made by soldering.

(0033) The copper foil on the outside surface of the electronic component mounting multilayer board thus obtained is further etched to form a printed wire pattern and configure an external circuit, and components such as a resistor and a capacitor are further mounted on the external circuit. In this example, more electronic components can be mounted and the printed board can be miniaturized.

(0034) According to the results of the board surface area simulation carried out by the present inventors, it is clear that with the method of the present invention of incorporating five LSI chips in the board, miniaturization of 40 to 50% can be achieved compared to the conventional method of surface-mounting five LSI chips two-dimensionally on the mounting board (multichip mounting, currently chip size package (CSP): conventional method). Accordingly, it is possible to miniaturize electronic devices when applying the electronic component mounting multilayer board 100.

(0035) (Embodiments) FIG. 7 to 11 are images showing configuration examples of interlayer wiring members as embodiments. The examples shown in FIG. 7 to 9 are such that the essential parts such as the interlayer wiring members are configured from an insulating material, conductive members are provided at the inside, the core or the outside, and the conductive members are grounded.

(0036) In the example of an interlayer wiring member 41 shown in FIG. 7A, the copper foil has been removed from both sides of the insulating material 4 in the interlayer wiring member 4A shown in FIG. 5. Accordingly, the shielding effect of the interlayer wiring member 41 that is obtained is electromagnetic shielding from connecting in parallel a through-hole 15A not used in a signal line or a power line and grounding. If removing the insulating material 4 is considered, an effect of electromagnetically shielding the side surfaces and the like of the LSI chips 3A and 3B can be obtained by arranging the grounded through-holes 15A in a lattice form.

(0037) In the example of an interlayer wiring member 42 shown in FIG. 7B, the positions of through-holes 15A of the interlayer wiring member 41 shown in FIG. 7A are arranged separated left and right. The cross-section area of the through-hole 15A is 1/2, but twice as many are provided. Accordingly, the lattice portion for shielding can be completely separated from the signal line and the power line with leeway. The shielding effect when doing so is wide electromagnetic shielding obtained from connecting through-holes 15C of the shielding lattice in parallel and grounding.

(0038) In the example of an interlayer wiring member 43 shown in FIG. 7C, the through-hole for the signal line is removed from the core of the interlayer wiring member 4A shown in FIG. 5, and a printed wiring pattern 18 for the signal line and a shielding pattern 19 are formed with the conducting members on both sides. A power line and a ground line, for example, are provided at the core of the interlayer wiring member 43. Accordingly, the shielding pattern 19 can be completely separated from the signal line and the power line in a way similar to the interlayer wiring member 42 shown in FIG. 7B. Naturally, if it is clear which of the interlayer wiring members 43 on the left or right is the shielding surface from the start, the copper foil can be left there. If it's not clear which of the left and right is the shielding surface, the copper foil can be treated as the printed wiring pattern 18, the shielding surface determined, the wiring pattern 18 on the shielding surface side connected in parallel and grounded, and that used as the shielding pattern 19.

(0039) In the example of an interlayer wiring member 44 shown in FIG. 8, the interlayer wiring member itself has a frame shape, and when the essential parts are configured from the insulating material 4, the plurality of through-holes (conductive members) 15A are provided at the core of the insulating material 4, and a portion of the through-holes 15A are connected in parallel and grounded. If all of the through-holes 15A are connected in parallel, a cage-like shielding wall such as that surrounds the electronic components can be configured. Ordinarily a portion of the through-holes 15A is used in a signal line and a power line. Naturally, the conductive members may be provided on the inner surface and the outer surface of the frame-like interlayer wiring member 44 and these conductive members used as the

shield pattern 19. A shield wall is formed such as that surrounds the electronic components and a similar shielding effect is obtained.

(0040) In the example of the interlayer wiring member 45 shown in FIG. 9, the interlayer wiring member itself has a "U" shape, and one side of the frame has been removed from the frame-like interlayer wiring member 44 shown in FIG. 8. The U-shaped interlayer wiring member 45 may be used at the end of a circuit board, for example. If mounting an LSI chip or the like that releases a high amount of heat, the U-shaped interlayer wiring member 45 can be arranged so that the open portion faces the circuit board end, and the open portion is thereby used as a heat dissipation window. A plurality of through-holes 15A are provided in the core of the insulating material 5 similar to in the frame-like interlayer wiring member 44, and a portion of the through-holes 15A are connected in parallel and grounded.

(0041) When all of the through-holes 15A are connected in parallel, a shield wall with one side open can be configured such as to surround the electronic components in a U-shape. Naturally, in this example as well, conductive members may be provided on the inside surface and the outside surface of the U-shaped interlayer wiring member 45, and the conductive members used as the shield pattern 19. The shield wall is formed so as to surround the electronic components in a U-shape, obtaining a similar shielding effect.

(0042) In this manner, a shielding effect can be obtained with a simple process. In particular, when mounting the LSI chips 3A and 3B in three dimensions, an electromagnetic shield can be made from the through-holes 15A of the interlayer wiring members 41 to 45.

(0043) In the examples shown in FIG. 10 and 11, the interlayer wiring member is configured from a conductive material which has a pillar or spherical shape. Naturally, the conductive material may also have a conic, round columnar or wall shape. In the example of an interlayer wiring member 46 shown in FIG. 10, a conductive interlayer wiring member is configured from four hollow round columnar copper pipes 46A to 46D. The interlayer wiring member 46 is arranged at the four corners of the board between the LSI mounting board 1A and the inner layer circuit board 2, for example. The interlayer wiring member 46 mainly functions as a power line or a supply route for clock signals and the like and are used to support the frame of the mounting board. The arrangement of the copper pipes 46A to 46D is not limited to the four corners, but may be in three corners if there is no bending in the circuit board, or the copper pipes 46A to 46D may be arranged on the basis of the frame stress concentration portion or the signal line input/output position if there are many circuit board layers with a large surface area. The pipe material is not limited to copper but may be bronze with little resistance, or silver, gold, or an alloy thereof.

(0044) In the example of an interlayer wiring member 47 shown in FIG. 11, a conductive interlayer wiring member is configured from four spherical solder balls 47A to 47D. The interlayer wiring member 47 is arranged at the four corners of the board as described with FIG. 10 between the LSI mounting board 1A and the inside layer circuit board 2, for example. The function is the same as that of the copper pipes 46A to 46D described above.

(0045) The formation positions of the solder balls 47A to 47D are not limited to the four corners, but may be in three corners consistent with the round electrodes if there is no bending in the circuit board, or the solder balls 47A to 47D may be arranged on the basis of the frame stress concentration portion or the signal line input/output position if there are many circuit board layers with a large surface area. In order to obtain the shielding effect the examples of the interlayer wiring members 46 and 47 shown in FIG. 10 and 11, the copper pipes 46A to 46D and the solder balls 47A to 47D may be arranged at the periphery of the electronic components and electrically connected and grounded.

(0046) (2) Second embodiment

FIG. 12 is a cross-section view showing a configuration example of an electronic component mounting multilayer board 200 as a second embodiment. The electronic component mounting multilayer board 200 of this embodiment has a recessed cavity structure in which the interlayer wiring member is integrated with the LSI mounting board. The cavity structure is a groove or hole for housing electronic components. In this example, the shield patterns 6A and 6B are provided on the inner layer wiring board 2, and the mounting surface area of the shielded LSI chips 3A and 3B can be increased three-dimensionally in the lamination direction.

(0047) The electronic component mounting multilayer board 200 shown in FIG. 12 is mounted at high density with the LSI chips 3A and 3B and other electronic components. In the example shown in FIG. 12, the LSI chips 3A and 3B are mounted on a cavity-structured LSI mounting board 21, the LSI mounting board 21 is laminated on one surface of the inner layer wiring board 2, the LSI mounting board 21 and the inner layer wiring board 2 are electrically joined, the other LSI mounting board 1B and the like are laminated on the other surface of the inner layer wiring board 2 with solder balls (spherical interlayer wiring members) 23A and 23B sandwiched therebetween, and the solder balls 23A and 23B electrically join the interval of the LSI mounting board 1B and the inner layer wiring board 2.

(0048) In this example, the LSI mounting board 21 has a cavity 22 projecting in a depression, and is provided with functions such as the interlayer wiring members 4A and 4B for interlayer connection described in the first embodiment. The cavity 22 has at least three functions, i.e., the nature of being a frame supporting the LSI mounting board 21 and the inner layer wiring board 2, a signal line path for propagating signals and the like, and a shield wall for shielding the LSI chip 3A, the signal line and the like.

(0049) Also in this example, the shield pattern 6A is provided as described in the first embodiment at one of the surface of the inner layer wiring board 2 on the side facing the LSI chip 3 in a region defined by the cavity 22, and the shield pattern 6B comprising copper foil with a predetermined size is provided on the other surface of the inner layer wiring board on the side facing the LSI chip 3B in a region defined by the solder balls 23A and 23B. These shield patterns 6A and 6B are grounded. Accordingly, the LSI chip 3A of the cavity 22 of the LSI mounting

board 21 can be electromagnetically shielded by the shield pattern 6A on the upper surface of the inner layer wiring board 2, and similarly, the LSI chip 3B on the LSI mounting board 1B can be electromagnetically shielded by the shield pattern 6B on the lower surface of the inner layer wiring board 2.

(0050) In this manner, according to the electronic component mounting multilayer board 200 as the second embodiment, the LSI chip 3A is mounted on the LSI mounting board 2 with a depression-like cavity structure having the function of an interlayer wiring member, the LSI mounting board 22 is laminated on one surface of the inner layer wiring board 2, and the LSI mounting board 21 and the inner layer wiring board 2 are electrically joined. Moreover, the shield pattern 6A is provided at a prescribed position of the inner layer wiring board 2, the other LSI mounting board 6B is laminated on the other surface of the inner layer wiring board 2 with the solder balls 23A and 23B sandwiched therebetween, and the solder balls 23A and 23B are electrically joined between the LSI mounting board 1B and the inner layer wiring board 2 to form a multilayer structure.

(0051) Accordingly, the boards, such as the LSI mounting board 21 and the LSI mounting board 1B, can be connected compositely, and the lamination processing of the interlayer wiring member can be separated from the simultaneous pressure-heating joining step as in the first embodiment. The mounting surface area of the LSI chips 3A and 3B electrically shielded by the shield patterns 6A and 6B with a prescribed size can be increased three-dimensionally in the lamination direction as in the first embodiment, and the shielded LSI chips 3A and 3B can be mounted at higher density than when shield-mounting the LSI chips 3A and 3B two-dimensionally. It is thereby possible to miniaturize electronic devices when applying the electronic component mounting multilayer board 200.

(0052) Next, the method for manufacturing the electronic component mounting multilayer board 200 is described. FIG. 13 and 14 are process diagrams showing (first and second) formation examples of the electronic component mounting multilayer board 200. In these examples, it is assumed that the LSI mounting board 1B and the inner layer wiring board 2 are already prepared as explained in the first embodiment. The boards, such as the LSI mounting board 21 and the LSI mounting board 1B, are connected compositely, and the lamination processing of the interlayer wiring members is separated from the simultaneous pressure-heating joining step as in the first embodiment.

(0053) With this as a premise, the LSI mounting board 21 is formed with the cavity structure shown in FIG. 13A. The double-sided copper foil board is processed in advance to form a prescribed printed wiring pattern, electrodes (round) and the like in the LSI mounting board 21 similar to the LSI mounting board 1 described in the first embodiment, and then the cavity 22 is created in the mounting board 1. The cavity 22 can use the interlayer wiring members 4A and 5A described in the first embodiment.

(0054) For example, the interlayer wiring members 4A and 5A for interlayer connection are initially joined to the mounting board 1 and fixed as shown in FIG. 5. The fixing is carried out with thermal bonding under pressure. The through-holes 15A, 16A and the like configuring the signal output line to another circuit board, the signal input line from another circuit board, as well as a power line, a ground line and the like are provided in the core of the cavity 22 (interlayer wiring members 4A and 4B). Naturally, copper foils (conductive members) for shielding may be provided on both sides and grounded along with the shield patterns 6A and 6B of the inner layer wiring board 2 to obtain an electromagnetic shielding effect.

(0055) Then the LSI chip 3A is mounted in the depression of the mounting board 1 shown in FIG. 13B to form the LSI mounting board 21 with a cavity structure. If the LSI chip 3A is a flip-chip, for example, the LSI chip 3A is joined to a plurality of pad electrodes and the like formed in advance via bump electrodes. The LSI chip 3A is not limited to a flip-chip but may be joined with a method such as wire bonding.

(0056) In this example, the electrode for operation inspection is drawn out from the LSI mounting board 21. The through-holes 15A and 16A provided in the core of the cavity 22 also serve as electrodes for operation inspection. During an operation inspection, the through-holes 15A and 16A are used to impress a test voltage, to supply test data, and to extract the result data. A dedicated test terminal does not need to be provided.

(0057) When the LSI mounting board 21 with a cavity structure described above is formed, electrical inspection is carried out on every LSI mounting board 21 by the LIST tester shown in FIG. 4 or the like. For example, probes 13 and 14 of the LSI tester 10 not illustrated come into contact at the same time with the plurality of through-holes 15A and 16A provided at the core of the cavity 22, and a mounting test is carried out that includes the through-holes 15A and 16A of the cavity 22.

(0058) Accordingly, before laminating the LSI mounting board 21 with a cavity structure on the inner layer wiring board 2 or another LSI mounting board 1B, defective LSI mounting boards 21 can be removed early. It is possible to laminate only the LSI mounting boards 21 and inner layer wiring boards 2 determined to be passing in the inspection results. The production yield of the electronic component mounting multilayer board 200 can be improved compared to when carrying out an electrical inspection after complete lamination of the LSI mounting board 21 with a cavity structure and the inner layer wiring board 2.

(0059) Then the LSI mounting board 21 with a cavity structure, the inner layer wiring board 2, and the LSI mounting board 1B are aligned and laminated as shown in FIG. 14. When doing so,

(EFFECT OF THE INVENTION) As described above, according to the electronic component mounting multilayer board of the present invention, mounting boards mounted with electronic components facing a conductive member for shielding are laminated with an interlayer wiring member sandwiched therebetween, and the mounting board interval is electrically joined with an interlayer wiring member to form a multilayer

the LSI mounting board 21, the inner layer wiring board 2, and the LSI mounting board 1B are aligned such that the LSI chip 3A faces the shield pattern 6A surface and the LSI chip 3B faces the shield pattern 6B surface. A solder paste not illustrated is applied between the LSI mounting board 21 and the inner layer wiring board 2, and solder balls 23A and 23B are sandwiched between the LSI mounting board 1B and the inner layer wiring board 2. In this state, the LSI mounting board 21 and the inner layer wiring board 2 are electrically and structurally joined with the solder paste, and the inner layer wiring board 2 and the LSI mounting board 1B are electrically and structurally joined with the solder balls 23A and 23B. The joining is carried out with the same pressure-thermal step.

(0060) The laminate comprising the LSI mounting board 21 with a cavity structure, the inner layer wiring board 2, and the LSI mounting board 1B is, for example, soldered. It is thereby possible to form the electronic component mounting multilayer board 200 shown in FIG. 12. Moreover, the mounting surface area of the shielded LSI chips 3A and 3B can be increased three-dimensionally in the lamination direction similarly to in the first embodiment. If the number of layers of the LSI mounting board 21 is further increased to increase the circuit functions, the electronic component mounting multilayer board 200 can be configured without increasing the two-dimensional size. In this manner, it is possible to stack a desired number of LSI mounting boards 21, thereby increasing the mounting surface area and achieving miniaturization of a multifunction electronic device.

(0061) Lamination of the two LSI mounting boards 1A and 1B and the LSI mounting boards 21 and 1B was described in the embodiments, but the lamination count of the LSI mounting boards and the LSI mounting boards is not so limited. Also, the mounting surfaces for the LSI chips 3A and 3B were described as being one side of the LSI mounting boards 1A and 1B and the LSI mounting boards 21 and 1B, but the mounting surfaces are not so limited. Naturally, the LSI chips 3A and 3B can also be mounted on both sides.

(0062) For the method of connecting the circuit board intervals in the lamination process, the use of solder paste and of the solder balls 23A and 23B was described, but the invention is not so limited. Mounting is also possible with soldering widely used in component mounting, an adhesive represented by an anisotropy conductive film (ACF), a silver paste attachment method or the like. It is also possible to apply ACF to the individual boards, and the electronic component mounting multilayer boards can be manufactured easier and more inexpensively.

(0063) structure. According to this structure, the mounting surface area of the shielded electronic components can be increased three-dimensionally in the lamination direction by a conductive member of a prescribed size, and shielded electronic components can be mounted at higher density than when shield-mounting with the electronic components two-dimensionally.

(0064) According to the manufacturing method of an electronic component mounting multilayer board of the present invention, a mounting board is formed with electronic components mounted on one or both surfaces, a conductive member for shielding is formed with a prescribed size on another mounting board on a side facing the electronic components, then the mounting board interval is laminated with the interlayer wiring members for interlayer connection sandwiched therebetween, and the mounting board interval is electrically and structurally joined by the interlayer wiring members.

(0065) According to this structure, the mounting surface area of shielded electronic components can be three-dimensionally increased in the lamination direction, and shielded electronic components can be mounted at higher density than when shield-mounting the electronic components two-dimensionally. As a result, electronic devices can be miniaturized with application of the electronic component mounting multilayer board. The invention can be applied to and is extremely favorable for mobile phones and mobile terminal devices such as portable personal computers in which LSIs, resistors, capacitors and other electronic components are mounted at high density.

(BRIEF DESCRIPTION OF THE DRAWINGS)

(FIG. 1) A cross-section view showing a configuration example of the electronic component mounting multilayer board 100 as the first embodiment.

(FIG. 2) A process diagram showing a (first) formation example of the electronic component mounting multilayer board 100.

(FIG. 3) A and B are process diagrams showing a (second) formation example of the electronic component mounting multilayer board 100.

(FIG. 4) An image showing an operation inspection example of the LSI mounting board 1 during formation of the electronic component mounting multilayer board 100.

(FIG. 5) A perspective view of the interlayer wiring members 4A and 5A showing a (third) formation example of the electronic component mounting multilayer board 100.

(FIG. 6) A cross-section view showing a (fourth) formation example of the electronic component mounting multilayer board 100.

(FIG. 7) A to C are perspective views showing structural examples of interlayer wiring members 41 to 43 as embodiments.

(FIG. 8) A perspective view showing a structural example of the interlayer wiring member 44 as an embodiment.

(FIG. 9) A perspective view showing a structural example of the interlayer wiring member 45 as an embodiment.

(FIG. 10) A perspective view showing a structural example of the interlayer wiring member 46 as an embodiment.

(FIG. 11) A perspective view showing a structural example of the interlayer wiring member 47 as an embodiment.

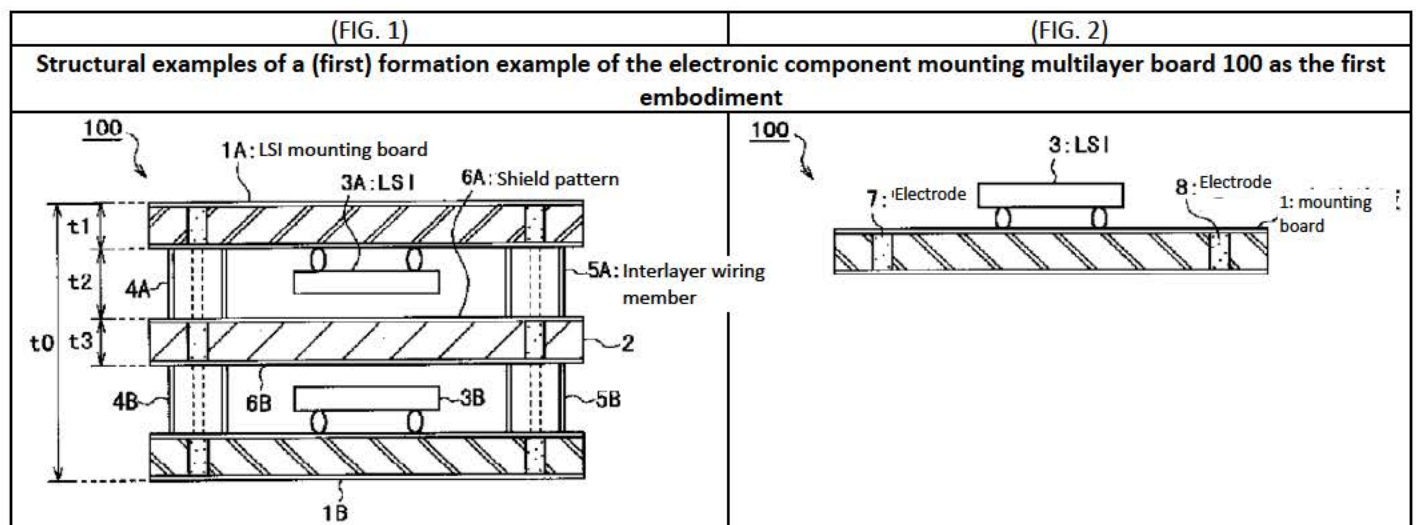
(FIG. 12) A cross-section view showing a structural example of the electronic component mounting multilayer board 200 as a second embodiment.

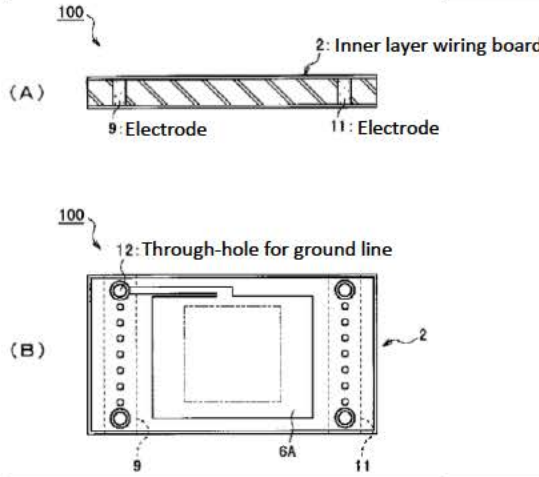
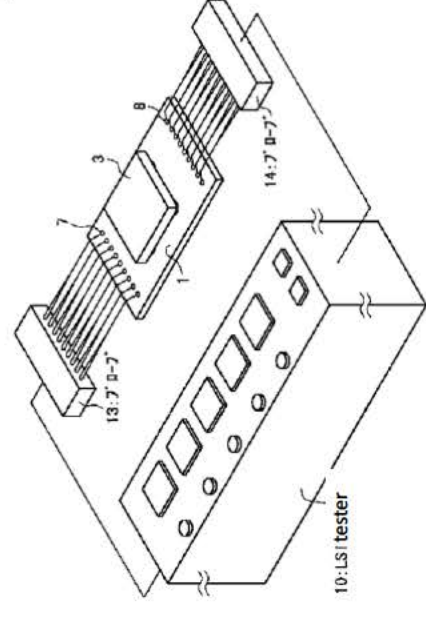
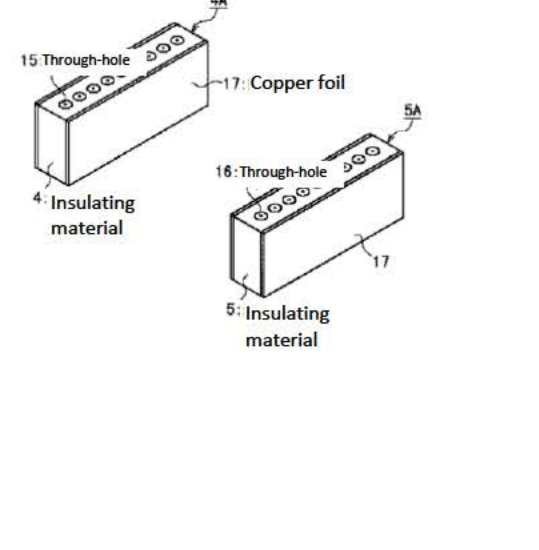
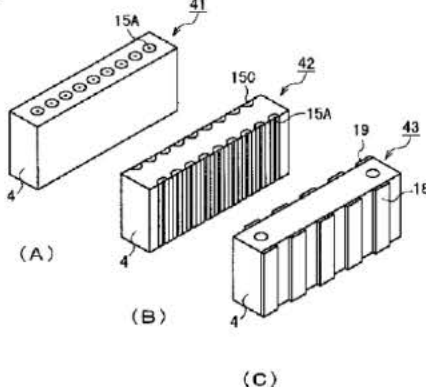
(FIG. 13) A and B are process diagrams showing a (first) formation example of the electronic component mounting multilayer board 200.

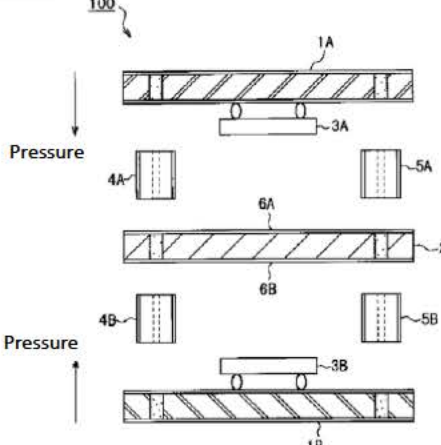
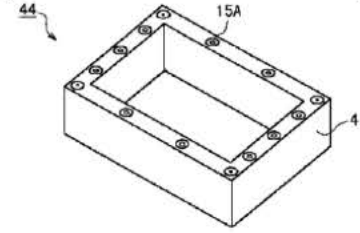
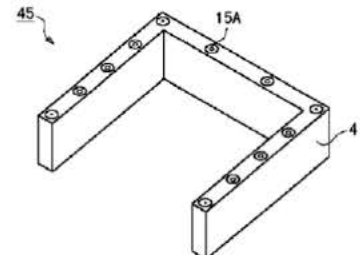
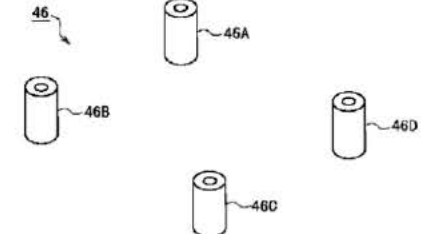
(FIG. 14) A cross-section showing a (second) formation example of the electronic component mounting multilayer board 200.

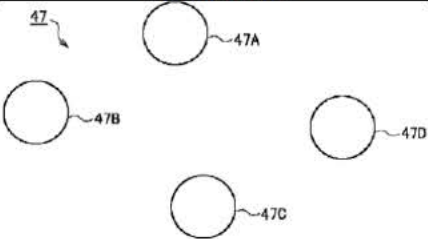
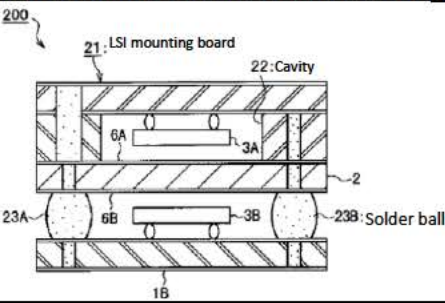
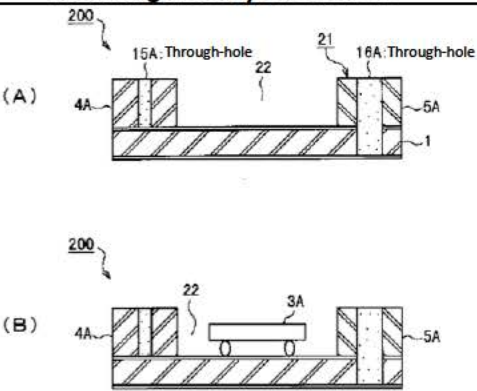
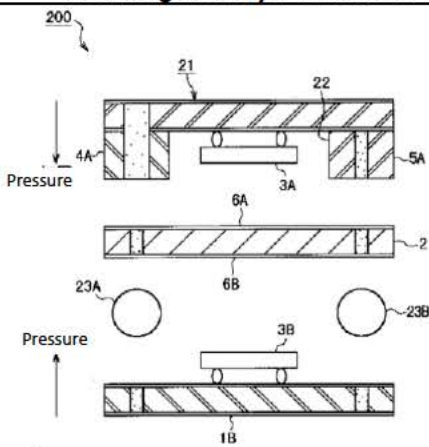
(DESCRIPTION OF THE REFERENTIAL CODES OR SYMBOLS)

1 ... mounting board; 1A, 1B, 21 ... LSI mounting board (first mounting board); 2 ... inner layer wiring board (second mounting board); 3A, 3B ... LSI chips (electronic components); 4A, 4B, 5A, 5B, 41-47 ... interlayer wiring members; 6A, 6B, 19 ... shield patterns (conductive members); 17 ... conductive member; 22 ... cavity; 23A, 23B ... solder balls (interlayer wiring members); 100, 200 ... electronic component mounting multilayer boards



(FIG. 3) (Second) formation example of the electronic component mounting multilayer board 100	(FIG. 4) Operation inspection example of the LSI mounting board 1
 (A) 100 2: Inner layer wiring board 9: Electrode 11: Electrode (B) 100 12: Through-hole for ground line 9 6A 11	 10: LSI tester
(FIG. 5) (Third) formation example of the electronic component mounting multilayer board 100	(FIG. 7) Structural examples of the interlayer wiring members 41 to 43 as embodiments
 15: Through-hole 17: Copper foil 4: Insulating material 16: Through-hole 17: Copper foil 5: Insulating material	 (A) (B) (C)

(FIG. 6)	(FIG. 8)
(Fourth) formation example of the electronic component mounting multilayer board 100	Structural example of the interlayer wiring member 44 as an embodiment
	
(FIG. 9)	(FIG. 10)
Structural example of the interlayer wiring member 45 as an embodiment	Structural example of the interlayer wiring member 46 as an embodiment
	

(FIG. 11) Structural example of the interlayer wiring member 47 as an embodiment	(FIG. 12) Structural example of the electronic component mounting multilayer board 200 as the second embodiment
	
(FIG. 13) (First) formation example of the electronic component mounting multilayer board 200	(FIG. 14) (Second) formation example of the electronic component mounting multilayer board 200
	

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