

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.;
SAMSUNG ELECTRONICS AMERICA, INC.; and
SAMSUNG AUSTIN SEMICONDUCTOR, LLC,
Petitioner

v.

IMBERATEK, LLC
Patent Owner.

**DECLARATION OF DR. BRUCE W. SMITH
IN SUPPORT OF PETITION FOR INTER PARTES REVIEW OF
U.S. PATENT NO. 7,989,944**

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I. INTRODUCTION AND BACKGROUND

1. I have been retained by Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Austin Semiconductor, LLC (collectively, “Samsung” or “Petitioner”), as an independent expert in this proceeding before the Patent Trial and Appeal Board (“PTAB” or “Board”). I understand that Samsung is requesting that the Board institute an *inter partes* review (“IPR”) proceeding of U.S. Patent No. 7,989,944 (“the ’944 Patent”) (Ex-1001), currently assigned to ImberaTek LLC (“Patent Owner” or “PO”).

2. I am not and have never been an employee of Samsung. I am being compensated at my usual and customary rate of \$550 per hour. No part of my compensation depends on the outcome of this proceeding, and I have no other interest in this proceeding.

3. I have been asked to provide my independent analysis of the ’944 Patent in light of the prior art publications cited below. I have also been asked to consider the state of the art and prior art available as of January 31, 2002. Based on the prior art discussed in this declaration, it is my opinion that Claims 1-36 of the ’944 Patent is unpatentable for the reasons provided below.

A. Qualifications

4. I am currently a Distinguished Professor of Electrical and Microelectronic Engineering at the Rochester Institute of Technology (RIT). All of

my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my over 35 years of research, academic, industry, and consulting engineering experience in IC (integrated circuit) processing, semiconductor devices, microelectronics, and microlithography.

5. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. I understand that a copy of my current curriculum vitae, which details my education and professional and academic experience, is being submitted by Petitioner as Exhibit 1003. The following provides an overview of some of my experience that is relevant to the matters set forth in this declaration.

6. I hold a Ph.D. from the Rochester Institute of Technology, which I earned in 1994 for research concentrating on semiconductor technology including thin films, materials, and lithography.

7. I have been a member of the faculty at RIT since 1988. From 2001 to 2004, I served as the Associated Dean of Graduate Programs of the Kate Gleason College of Engineering at RIT. From 2000 to 2007, I was the Intel Professor of Research and Technology. In 2008, I became Director and Professor of the Microsystems Engineering Ph.D. Program. My group's research at RIT is in areas of micro- and non-fabrication including nanolithography, semiconductor processing,

and thin film materials. Our work is directed toward leading edge electronic, photonic, micromechanical, and display devices and structures.

8. Before joining the faculty of RIT, I held R&D positions in semiconductor engineering from 1983 to 1986 at Gould AMI Semiconductor in Santa Clara, California, and from 1986 to 1988 at Digital Equipment Corporation in Hudson, Massachusetts in the Advanced Development Center.

9. I am a Fellow of the Institute of Electrical and Electronics Engineers (IEEE), a Fellow of the International Society for Optical Engineering (SPIE), and a Fellow of the Optical Society of America (OSA). I have received numerous awards including the IEEE Technology Innovation Award, the RIT Trustees Scholarship Award, the SPIE Research Mentoring Award, the RIT Creators Award, and the Rush Henrietta Outstanding Alumni Award, among others, and have been inducted into RIT's Innovator Hall of Fame.

10. I have published over 200 technical papers, articles, textbooks, and textbook chapters, and I hold 26 patents in the fields of microelectronics and semiconductor device process technology. My patented technologies have been licensed by nationally and internationally.

11. Based on my experience and education, I believe that I am qualified to opine as to the knowledge and level of skill of one of ordinary skill in the art at the

time of the alleged invention of the '944 Patent, as well as the state of the art at that time.

B. Materials Considered

12. In forming my opinions, I have reviewed the following documents:¹

Ex. No.	Description
Ex-1001	U.S. Patent No. 7,989,944 to Tuominen (“the '944 Patent”)
Ex-1004	Prosecution History of the '944 Patent (Application No. 11/878,557)
Ex-1005	U.S. Patent No. 7,294,529 to Tuominen (“the '529 Patent”)
Ex-1006	Prosecution History of the '529 Patent (Application No. 10/502,336)
Ex-1007	Certified Translation of Japanese Patent Publication No. JP2001-068624A (“Imoto”)
Ex-1008	Japanese Patent Publication No. JP2001-068624A to Imoto (“Imoto”)
Ex-1009	U.S. Patent No. 6,297,551 (“Dudderar”)
Ex-1010	U.S. Patent No. 5,306,670 (“Mowatt”)
Ex-1011	John H. Lau, <u>Low Cost Flip Chip Technologies</u> (2000).
Ex-1012	Gary L. Lehmann, T. Driscoll, N.R. Goydosh, P.C. Li, and Eric J. Cotts, <u>Underflow Process for Direct-Chip-Attachment Packaging, IEEE Transactions on Components, Packaging, and Manufacturing Technology</u> , June 1998 (“Lehmann”)
Ex-1013	U.S. Patent No. 6,404,052 (“Kurita”)
Ex-1014	U.S. Pat. No. 5,608,262 (“Degani”)

¹ Four-digit pin citations that begin with 0 are to the branded numbers added by Samsung in the bottom right corner of the exhibits. All other pin citations are to original page, column, paragraph, or line numbers.

Ex. No.	Description
Ex-1015	The IEEE Standard Dictionary of Electrical and Electronics Terms, Sixth Edition (1996) (“IEEE Dictionary”).
Ex-1016	Semiconductor Chip Underfill Materials, <u>Encyclopedia of Materials: Science and Technology</u> , 2001.
Ex-1017	U.S. Patent No. 6,469,374 (“Imoto U.S. Patent”).
Ex 1018	Certified Translation of Japanese Patent No. P3207174 (“Hayashi”)
Ex 1019	Japanese Patent No. P3207174 (“Hayashi”)
Ex-1020	U.S. Patent No. 6,459,593 (“Kwong”)
Ex-1021	Certified Translation of Japanese Patent Publication No. JP2001-237586A (“Asahi Japanese Publication”)
Ex-1022	Japanese Patent Publication No. JP2001-237586A (“Asahi Japanese Publication”)
Ex-1023	Certified Translation of Japanese Patent Publication No. JP2001-111232A (“Oya”)
Ex-1024	Japanese Patent Publication No. JP2001-111232A (“Oya”)
Ex-1025	U.S. Patent Publication No. 2003/0090833 (“Asahi U.S. Publication”)

II. LEGAL STANDARDS

13. In forming my opinions and considering the subject matter of the '944 Patent and its claim in light of the prior art, I am relying on certain legal principles that counsel in this case explained to me. My understanding of these concepts is summarized below.

14. I understand that earlier publications and patents may act to render a patent unpatentable for one of two reasons: (1) anticipation, and (2) obviousness.

A. Anticipation

15. It is my understanding that the claims of a patent are anticipated by a prior art reference if each and every element of the claim is found either explicitly or inherently in the reference. I understand that inherency requires a showing that the missing descriptive matter in the claim is necessarily present in the allegedly anticipating reference, and that it would have been so recognized by a person of ordinary skill in the art (“POSITA”).

16. I understand that when a challenged claim covers several structures, either generically or as alternatives, the claim is deemed anticipated if any of the structures within the scope of the claim is found in the prior art reference.

17. Although anticipation typically involves the analysis of a single prior art reference, I understand that additional references may be used to show that the prior art reference has enabling disclosure (i.e., allows a POSITA to make the invention without undue experimentation), to explain the meaning of a term used in the prior art reference, and/or to show that a characteristic is inherent in the prior art reference.

B. Obviousness

18. I understand that a claim is invalid as obvious if it would have been obvious to a person of ordinary skill in the art at the time the alleged invention was made. This means that even if all of the elements of the claim cannot be found in a single prior art reference that would anticipate the claim, a person of ordinary skill in the art who was aware of the prior art would have been able to come up with the claimed invention. This may be the case, for example, where the missing element represents only an insubstantial different over the prior art or a reconfiguration of a known system. I understand that in an obviousness determination, the person of ordinary skill in the art is presumed to have knowledge of all material prior art.

19. I understand that an obviousness analysis requires an understanding of the scope and content of the prior art, any differences between the alleged invention and the prior art, and the level of ordinary skill in evaluating the pertinent art.

20. I understand that when a product is available, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill in the art can implement a predictable variation, obviousness likely bars its patentability. For the same reason, if a technique has been used to improve one device and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique would have been obvious.

21. I understand that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a person of ordinary skill in the art at the time of the alleged invention. I have been told that there is not requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of one skilled in the art. In addition, I have been told that the inferences and creative steps a person of ordinary skill in the art would employ are relevant to the determination of obviousness.

22. I understand that one may consider, e.g., whether (1) the change was merely the predictable result of using prior art elements according to their known functions, or whether it was the result of true inventiveness; (2) there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; (3) the claimed innovation applies a known technique that had been used to improve a similar device or method in a similar way; (4) the claimed invention would have been obvious to try, meaning that the claimed innovation was one of a relatively small number of possible approaches to the problem with a reasonable expectation of success by those skilled in the art; (5) the invention merely substituted one known element for another known element in order to obtain predictable results; (6) the invention merely applies a known technique to

a known device, method, or product to yield predictable results; or (7) known work in one field of endeavor may have prompted variations of it for use in either the same field or a different one based on design incentives or other market forces that would have been predictable to a person of ordinary skill in the art.

23. I further understand that certain factors may support or rebut the obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the patented invention, skepticism of those having ordinary skill in the art at the time of the invention, unexpected results of the invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I understand that there must be a nexus—that is, a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

24. I am not aware of any allegations by the named inventor of the '944 Patent or any assignee of the '944 Patent that any secondary considerations tend to rebut the obviousness of the sole claim of the '944 Patent.

25. Additionally, I understand that in considering obviousness, it is important not to use the benefit of hindsight derived from the patent under consideration.

C. Level of Ordinary Skill in the Art

26. When interpreting a patent, I understand that it is important to identify the relevant art pertaining to that patent, as well as the level of ordinary skill in that art at the time of the claimed invention. The “art” is the field of technology to which the patent is related.

27. I am informed and understand that the person having ordinary skill in the art (“POSITA”) is a hypothetical person who is presumed to know the relevant prior art. I understand that the actual inventor’s skill is not determinative of the level of ordinary skill. I further understand that factors that may be considered in determining level of skill include: (i) the types of problems encountered in the art; (ii) prior art solutions to those problems; (iii) the rapidity with which innovations are made; (iv) the sophistication of the technology; and (v) the educational level of active workers in the field. I understand that not all such factors may be present in every case, and one or more of them may predominate.

28. I understand that a POSITA is one who is presumed to be aware of all pertinent art, thinks along conventional wisdom in the art, and is a person of ordinary creativity. A POSITA would have had knowledge of circuit boards and

microcircuits, including components thereof, and related technologies as of July 23, 2010.

29. A POSITA would have had a bachelor's degree in electrical engineering, material science, applied physics, or a related field, and at least three years of experience in the research, design, development, and/or testing of circuit board or microcircuit components, or the equivalent, with additional education substituting for experience and vice versa.

30. Based on my education and experience, I would have easily exceeded the criteria for a POSITA in July 23, 2010, and I still exceed it today.

D. Claim Construction

31. I understand that the United States Patent and Trademark Office interprets claim terms in an *inter partes* review proceeding under the same claim construction standard that is used in a United States federal court. I understand that under this standard, the meaning of claim terms is considered from the viewpoint of a POSITA at the time of the alleged invention.

32. I have been informed that claim terms are generally given their ordinary and customary meaning as understood by one of ordinary skill in the art in light of the specification and the prosecution history pertaining to the patent. I understand, however, that claims terms are generally not limited by the embodiments described in the specification.

33. I understand that in addition to the claims, specification, and prosecution history, other evidence may be considered to ascertain the meaning of claim terms, including textbooks, encyclopedias, articles, and dictionaries. I have been informed that this other evidence is often less significant and less reliable than the claims, specification, and prosecution history.

III. SUMMARY OF GROUNDS

34. I understand that Petitioner challenges the validity of Claims 1-36 of the '944 Patent. In particular, I understand that Petitioner asserts the following grounds for challenging the claims of the '944 Patent:

Ground	Summary
1	Claims 1-3, 8, 11, 13-26, and 29-31 are obvious in view of Imoto (Ex-1007). ²
2	Claims 4-7, 10, 27, 28, and 32-36 are obvious over Imoto in view of Dudderar (Ex-1009).
3	Claims 9 and 31 are obvious over Imoto in view of Mowatt (Ex-1010).
4	Claims 11 and 29 are obvious over Imoto in view of Lau (Ex-1011).

² Ex-1008 is a copy of Imoto; Ex-1007 is a certified translation of Imoto.

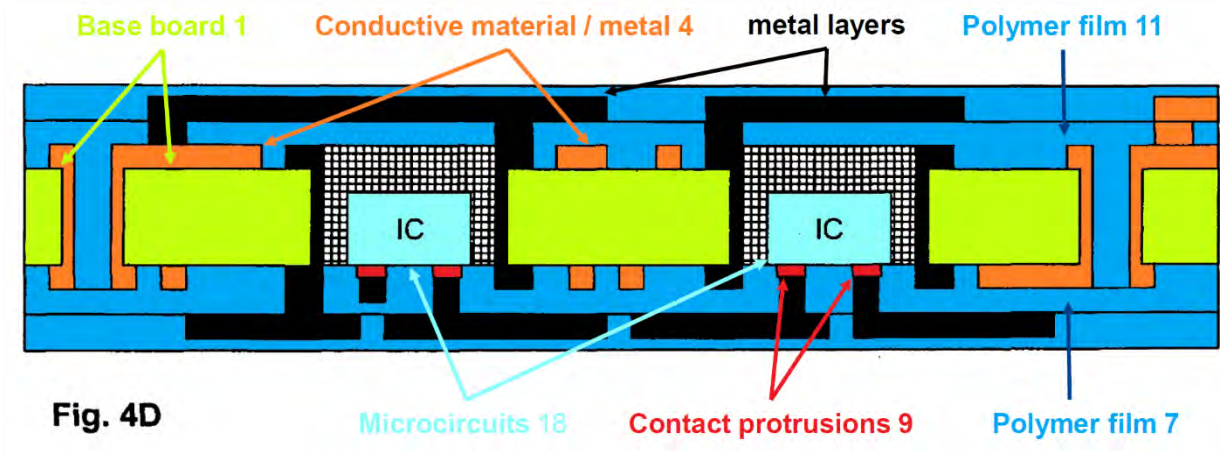
Ground	Summary
5	Claim 12 is obvious over Imoto in view of Lehmann (Ex-1012).
6	Claims 1-3, 8, 11, 13-26, and 29-31 are obvious in view of Kurita (Ex-1013).
7	Claims 4-7, 10, 27, 28, and 32-36 are obvious over Kurita in view of Dudderar.
8	Claims 9, 12, and 31 are obvious over Kurita in view of Mowatt.

IV. THE '944 PATENT

A. Overview of the '944 Patent

35. The '944 Patent describes a method of embedding a component (*e.g.*, semiconductor) in a base (*e.g.*, a circuit board). Ex-1001, Abstract. With reference to Figures 1-4, the '944 Patent describes a particular method of embedding microcircuit 18 (labeled "IC") in baseboard 1. Ex-1001, 3:32-9:41. But the challenged claims are apparatus claims directed to the final structure shown in Figure 4D.³ Ex-1001, 9:43-14:3.

³ Throughout the figures in this Declaration, all colors other than black are added for purposes of illustration.



36. The '944 Patent describes shielding microcircuits 18 with metal to protect them from electromagnetic interference. Ex-1001, 8:34-35, 64-66. In the above Figure 4D, “the cross-sections of the metal layers protecting the microcircuits are highlighted in black.” Ex-1001, 9:5-6. The '944 Patent describes “metal foil” on the lateral sides and bottom side and a “metal plate”⁴ on the top side above microcircuits 18. Ex-1001, 9:10-20.

B. Challenged Claims

37. The claim at issue are Claims 1-36 of the '993 Patent.

C. Prosecution History of the '944 Patent

38. I understand the '944 Patent was filed July 25, 2007, as a continuation of Application No. 10/502,336 (now U.S. Patent No. 7,294,529 (“the '529 Patent”)),

⁴ The claim term “metal plate” is used in the specification in only three instances—in each case, to refer to the metal *above* microcircuit 18. Ex-1001, 9:11, 38, 39-40.

claiming priority to PCT/FI03/00065 filed January 28, 2003, and further to Finish Patent No. 20020191 filed January 31, 2002.

39. I understand the prior art relied on in the Petition was not before the PTO during prosecution of the '944 Patent or during prosecution of its parent '529 Patent, with one exception—Mowatt. Ex-1001, Cover p. 2. Mowatt is used herein as a secondary reference (in combination with primary references not of record during prosecution) for three dependent claims (Claims 9, 12, and 31). *See infra* Sections VII.C, VII.H. After allowance, Applicant filed a petition to withdraw the application from issue to submit 18 new references, including Mowatt. Ex-1004, 0120-28. The petition was granted, and the Examiner signed the IDS and issued a Notice of Allowability, without any indication that the Examiner meaningfully considered Mowatt. Ex-1004, 1049. Moreover, there is no indication that the Examiner considered Mowatt in combination with Imoto, Kurita, or other substantially similar art. For example, the examiner did not apply Mowatt or any of the late-submitted prior art to the claims being examined. The record is silent on the examiner's view (if any) of Mowatt.

40. Thus, I understand that the Petition presents substantially new arguments that were not considered during prosecution.

D. Priority Date

41. I understand that for purposes of this proceeding only, Petitioner assumes that the '944 Patent is entitled to its earliest alleged priority date, January 31, 2002, and thus applies pre-AIA 35 U.S.C. § 102.

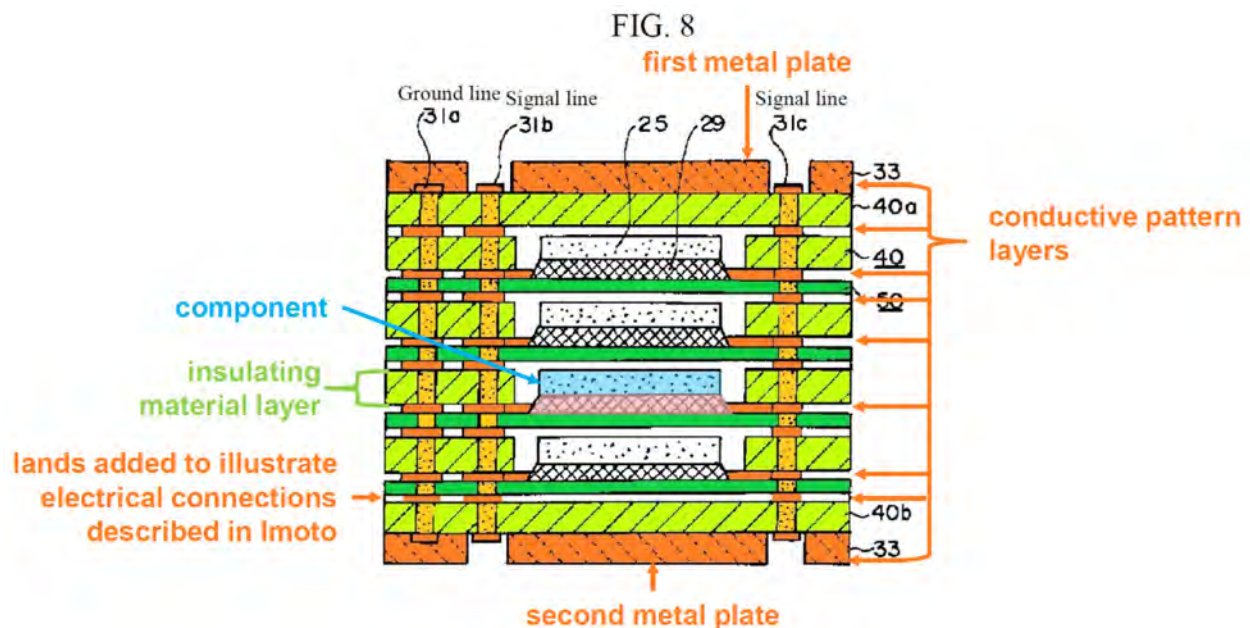
V. THE PRIOR ART

A. Imoto

42. Imoto was published March 16, 2001. Ex.-1007, cover.

43. I understand that Imoto is prior art under at least §102(b).

44. Imoto discloses a component (semiconductor 25) embedded in an insulating layer with conductive pattern layers, as shown below in Figure 8. Ex-1007, ¶0021.



45. A metal plate (metal film 33) acts as a shield above and below the component. Ex-1007, ¶0022. Imoto describes metal films 33 as electrically connected to electrode 31a, which is connected to ground to provide a shielding effect. *Id.* Based on this electrical connection, a POSITA would have understood that lands shaded orange on bottom laminated plate 40b are present, even though not depicted in Figure 8.⁵ Ex-1013, ¶0012 (describing bottom laminated plate 20(b) as including lands 3), Figs. 2b and 4a (showing lands 3 above laminated plates 20).

46. Consistent with the above interpretation of Figure 8 in Imoto, Figure 8 of U.S. Patent No. 6,469,374 (which I understand is the U.S. counterpart of Imoto and claims priority to the same Japanese patent application) shows that contact electrode 31a connects metal films 33 to one another and to ground. Ex-1017, 15:21-38.

⁵ These same lands are added to the Figure 8 illustrations throughout this Declaration.

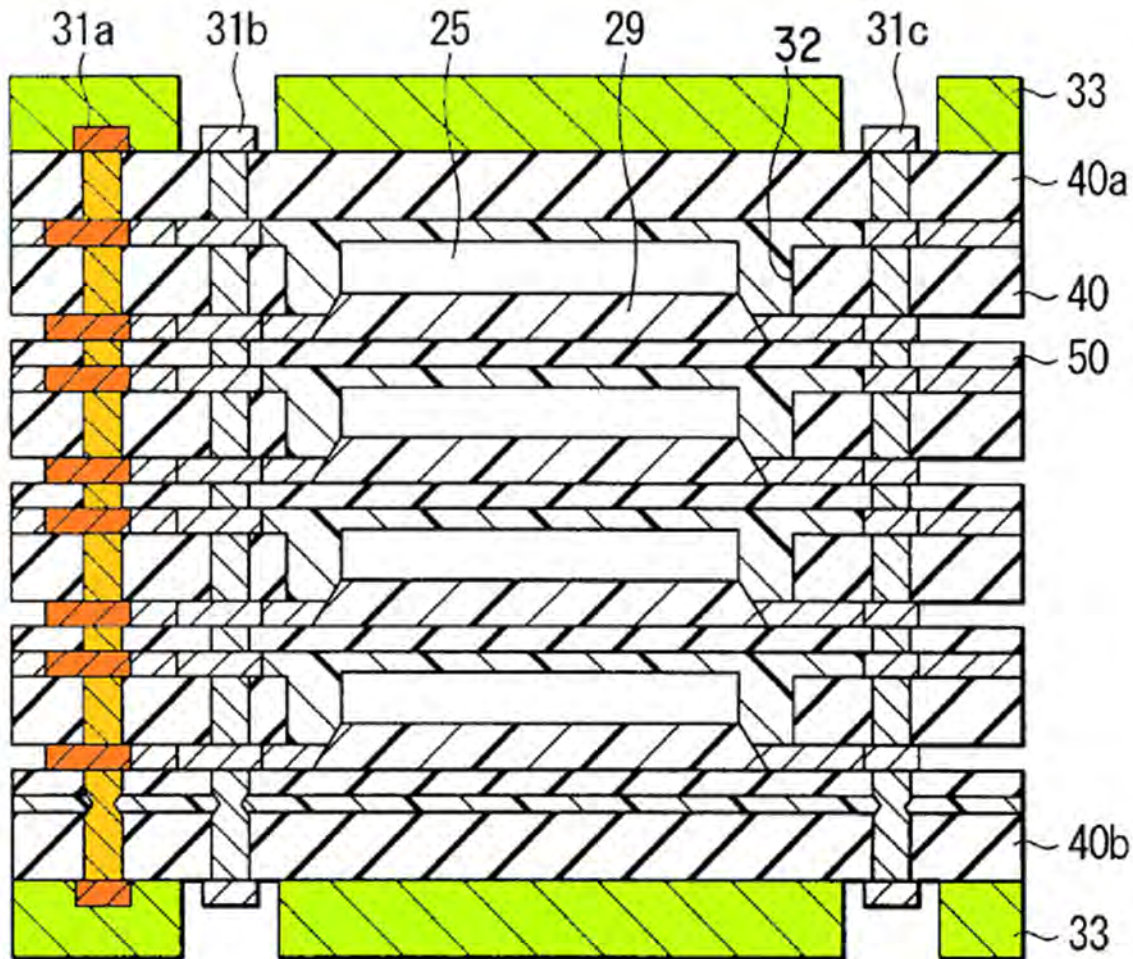


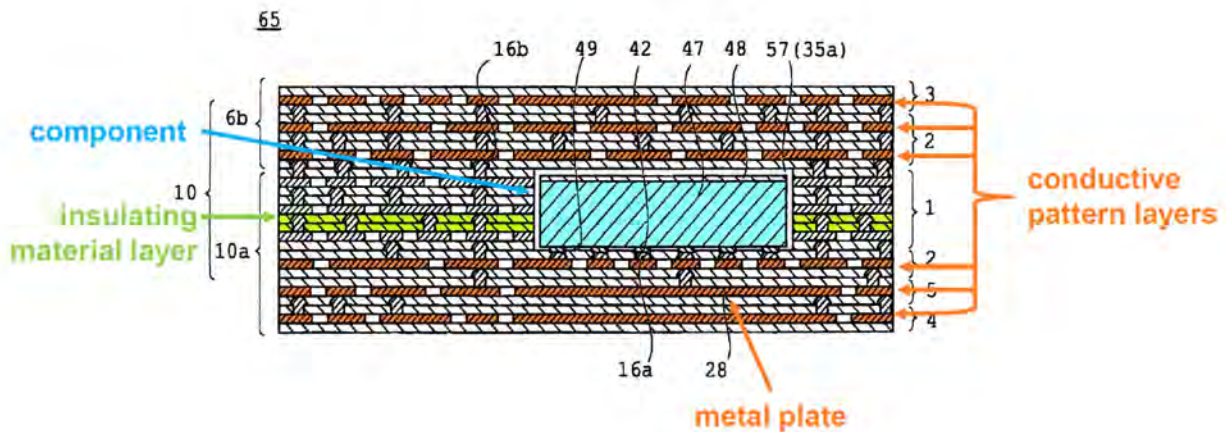
FIG. 8

B. Kurita

47. I understand that Kurita is § 102(e) prior art as of its U.S. filing date (July 7, 2000).

48. Kurita discloses a component (semiconductor device 47) embedded in multilayer substrate, as shown below in Figure 7. Ex-1013, 12:16-17.

FIG. 7



49. In other figures, the insulating layer is resin film 25, and the conductive pattern layers are wiring films 15. Ex-1013, 6:51-64, 7:25-27. A metal plate (shield section 28) acts as a shield below the component in Figure 7, but Kurita states the shield is most effective if on “both sides” of semiconductor device 47. *Id.*, 12:8-15, 12:40-50.

C. Dudderar

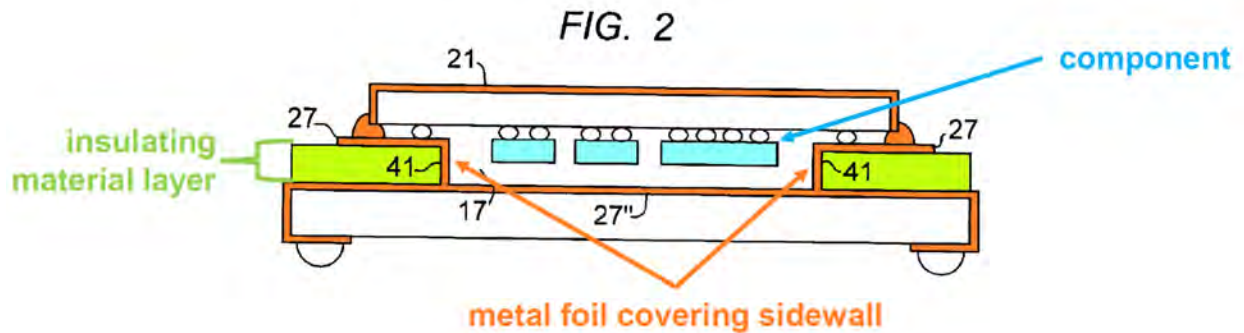
50. Dudderar was published October 2, 2001. Ex-1009, cover.

51. I understand that Dudderar is prior art under at least §102(b).

52. I understand that Dudderar incorporates by reference another patent Degani. Ex-1009, 2:15-28. Degani was published March 4, 1997 (Ex-1014, cover), and thus, I understand also is prior art under at least §102(b).

53. Dudderar discloses embedding semiconductor devices within the cavity of a printed circuit board and the use of metallization connected to ground to act as

a shield. Ex-1009, 2:53-54, 2:63-3:3. To enhance the shielding effect, Dudderar also describes extending that metallization to the inside walls of the cavity housing the semiconductor devices, as shown below in Figure 2. *Id.*, 4:45-50.

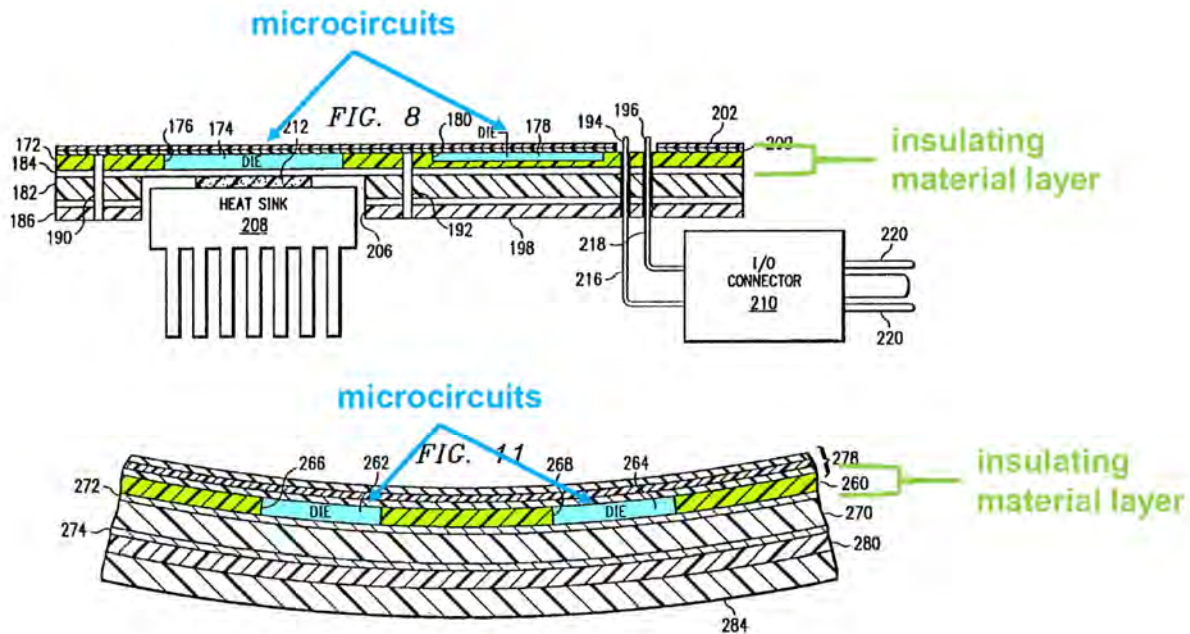


D. Mowatt

54. Mowatt was published April 26, 1994. Ex-1010, cover.

55. I understand that Mowatt is prior art under at least §102(b).

56. Mowatt also describes embedding semiconductor devices within the cavity of a circuit board. Ex-1010, 9:40-43. Mowatt discloses two microcircuits inside the same insulating material layer, as shown below in Figures 8 and 11. *Id.*, 9:40-43, 11:58-59.



E. Lau

57. Lau was published in 2000. Ex-1011, cover.
58. I understand that Lau is prior art under at least §102(b).
59. Lau describes implementation details for flip-chip, including the use of electroplated copper to make interconnections between a chip and a board. Ex-1011, 44, 47-48, 159-61, 186-87.

F. Lehmann

60. Lehmann was published in 1998. Ex-1012, ____.
61. I understand that Lehman is prior art under at least §102(b).
62. Lehmann describes directly attaching a chip to a substrate with solder balls and use of epoxy underfill resin to protect chip interconnections. Ex-1012, 266.

VI. CLAIM CONSTRUCTION

63. I do not believe that any claim term requires explicit construction to resolve the issues presented in the Petition. I apply the plain and ordinary meaning to each claim term, as that plain and ordinary meaning would have been understood by a POSITA.

64. I reserve the right to offer opinions on any claim constructions proposed in this proceeding or to offer opinions on additional constructions in the district court.

VII. DETAILED EXPLANATION OF THE UNPATENTABILITY GROUNDS

A. Grounds 1: Claims 1-3, 8, 11, 13-26, and 29-31 are rendered obvious by Imoto

1. Independent Claims 1

a. Element 1[preamble]: A circuit board comprising

65. Imoto teaches the preamble of Claim 1, to the extent it is limiting.

66. Imoto teaches a “plurality of wiring substrates” with conductive wiring patterns and vias, as illustrated in Figures 1 and 8. Ex-1007, ¶¶0004-0006, 0011, 0021-22.

FIG. 1

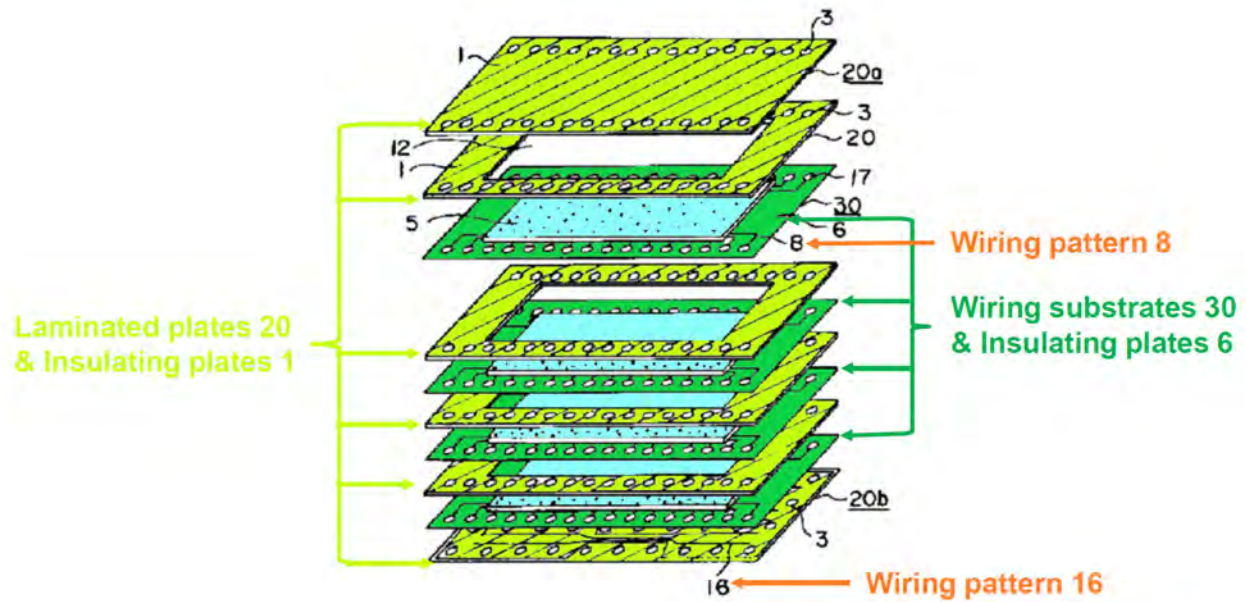
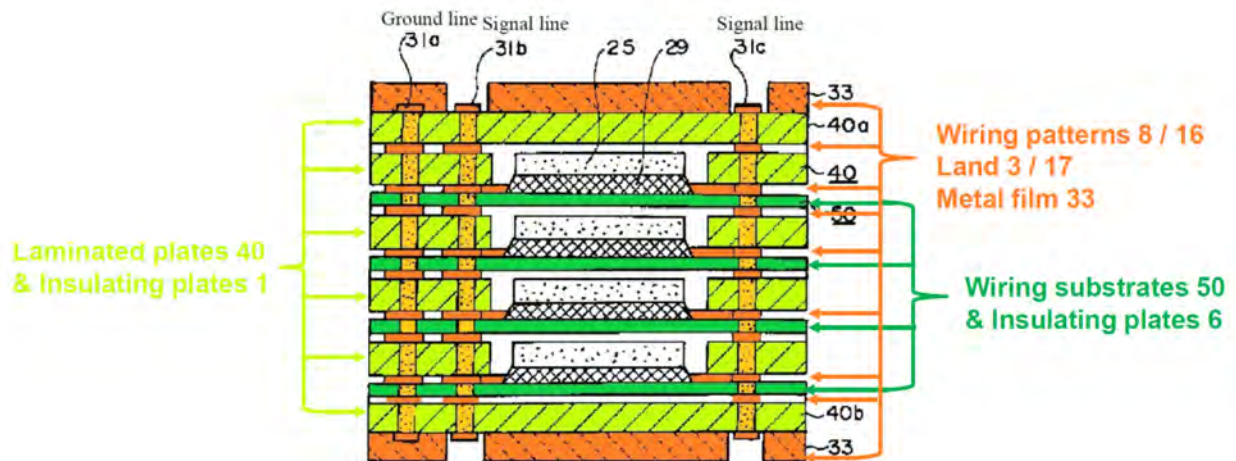


FIG. 8



67. The '944 Patent teaches that “the base material of a circuit board is an insulator.” Ex-1001 at 1:26-27. Imoto similarly teaches that the base material of

laminated plates 20/40 and wiring substrates 30/50 is an insulator (insulating plates 1 and 6). Ex-1007, ¶¶0011, 0015-16.

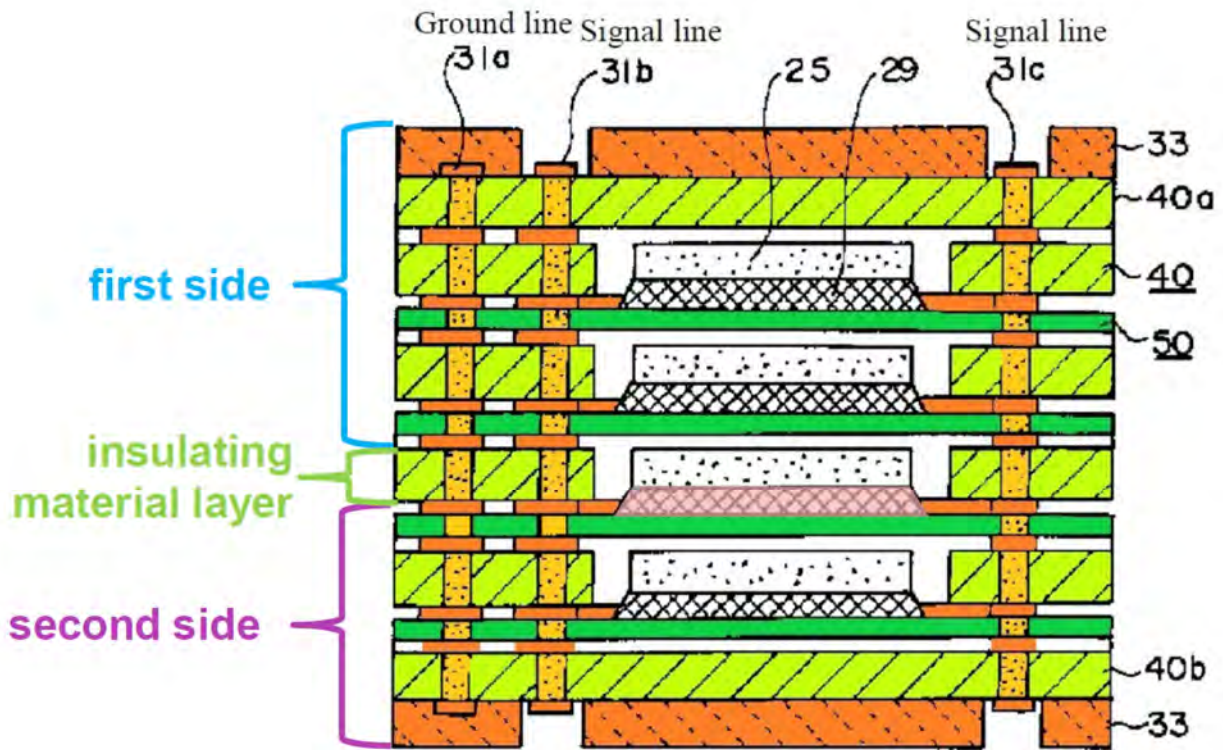
68. To the extent PO contends the preamble is limiting and Imoto does not teach a circuit board, it would have been obvious to a POSITA apply the teachings of Imoto to a circuit board. Ex 1002, ¶¶____. For example, Japanese Patent No. P3207174 (Hayashi) teaches embedding semiconductors into gap portions of the same or different layers of a multilayer wiring board. Ex 1018, ¶¶0027, 0032. Similarly, Mowatt teaches embedding semiconductor into layers of a circuit board. *See infra* Section VII.C. Thus, it would have been obvious to apply Imoto's teaching to a circuit board.

b. Element 1[a]: an insulating material layer having a first side and a second side

69. Imoto discloses Element 1[a].

70. Imoto discloses an insulating material layer with a first and second side, as shown below in Figure 8.

FIG. 8

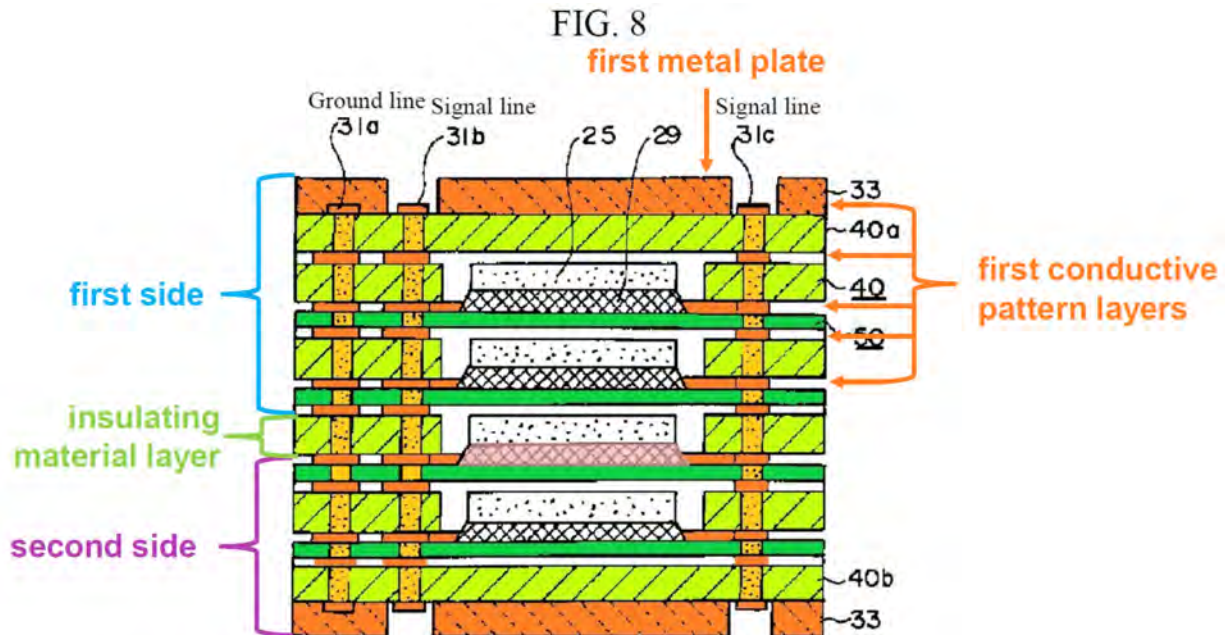


71. Laminated plate 40 is the insulating material layer. Ex-1007, ¶¶0011, 0015, 0016.

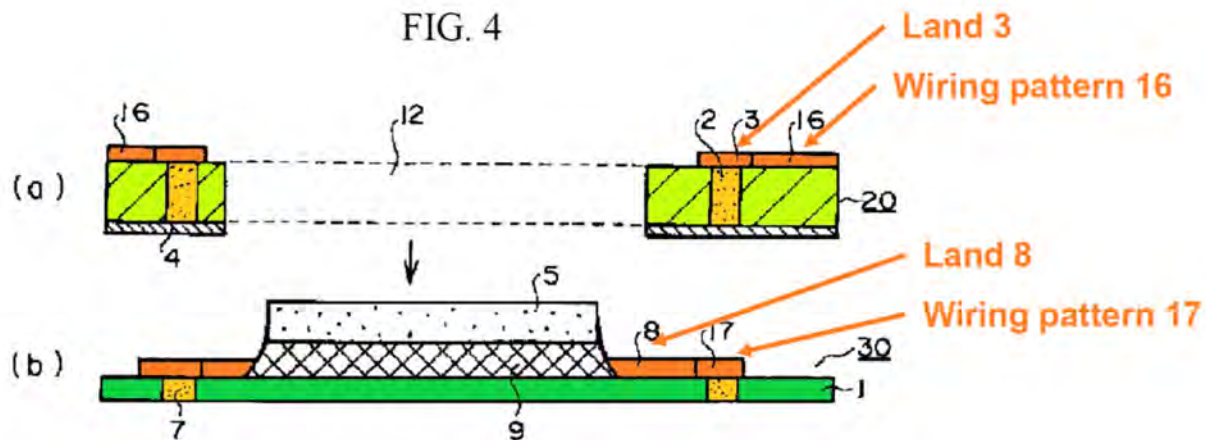
- c. **Element 1[b]: at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate**

72. Imoto discloses Element 1[b].

73. The first conductive pattern layers in Figure 8 are the combination of wiring patterns 8/16, lands 3/17, and metal film 33 above the insulating material layer, as shown below.⁶



⁶ Elements 1[b] and 1[c] require that the conductive pattern layers are on “sides” of insulating material layer as opposed to its “surface” (a term used in other limitations, such as Elements 1[d] and 1[e]). Thus, the conductive pattern layers may be above or below the surfaces of the insulating material layer as shown in Figures 4C and 4D of the '944 Patent.



74. Laminated plates 20/40 (light green) and wiring substrates 30/50 (dark green) include conductive pattern layers (orange). Each laminated plate 20/40 includes copper foil patterned to form land 3 and wiring pattern 16, and each wiring substrate 30/50 includes copper foil patterned to form land 17 and wiring pattern 8, as illustrated in Figure 4 above. Ex-1007, ¶¶0011, 0015-16 (describing these features with reference to laminated plate 20 and wiring board 30 in Figures 1-5⁷).

75. In addition, top laminated plate 40a in Figure 8 includes metal film 33, which is the claimed “first conductive pattern layer[] defining a first metal plate.” Metal film 33 may be formed by sputtering or a metal foil. Ex-1007, ¶0022. Metal film 33 is patterned to connect with ground line 31a but not to connect with signal lines 31b and 31c. *Id.* Like the metal plate described in the '944 Patent

⁷ In Figures 2(a), 3(a), 3(b), and 4(b), the reference numbers for insulating plates 1 and 6 are reversed.

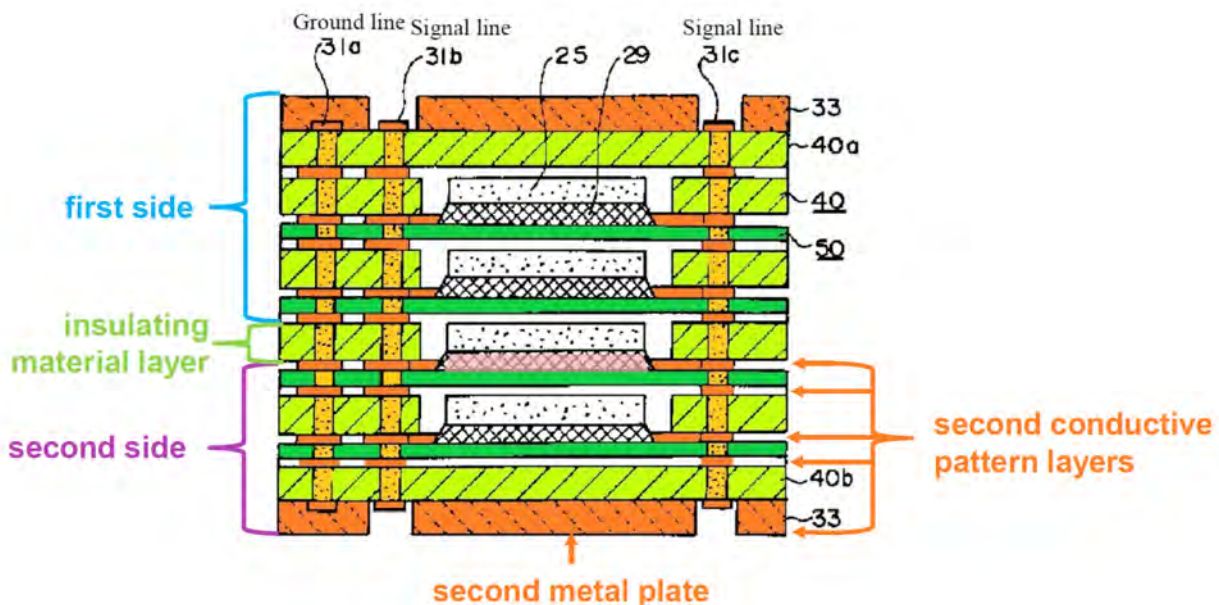
(Ex-1001, 9:30-41), metal film 33 in Imoto “has a shielding effect when connected to the ground line.” Ex-1007, ¶0022.

- d. **Element 1[c]: at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate**

76. Imoto discloses Element 1[c].

77. As shown below, the second conductive pattern layers in Figure 8 are the same features discussed above (the combination of wiring patterns 8/16, lands 3/17, and metal film 33), but on the “second side” of (below) the insulating material layer.

FIG. 8

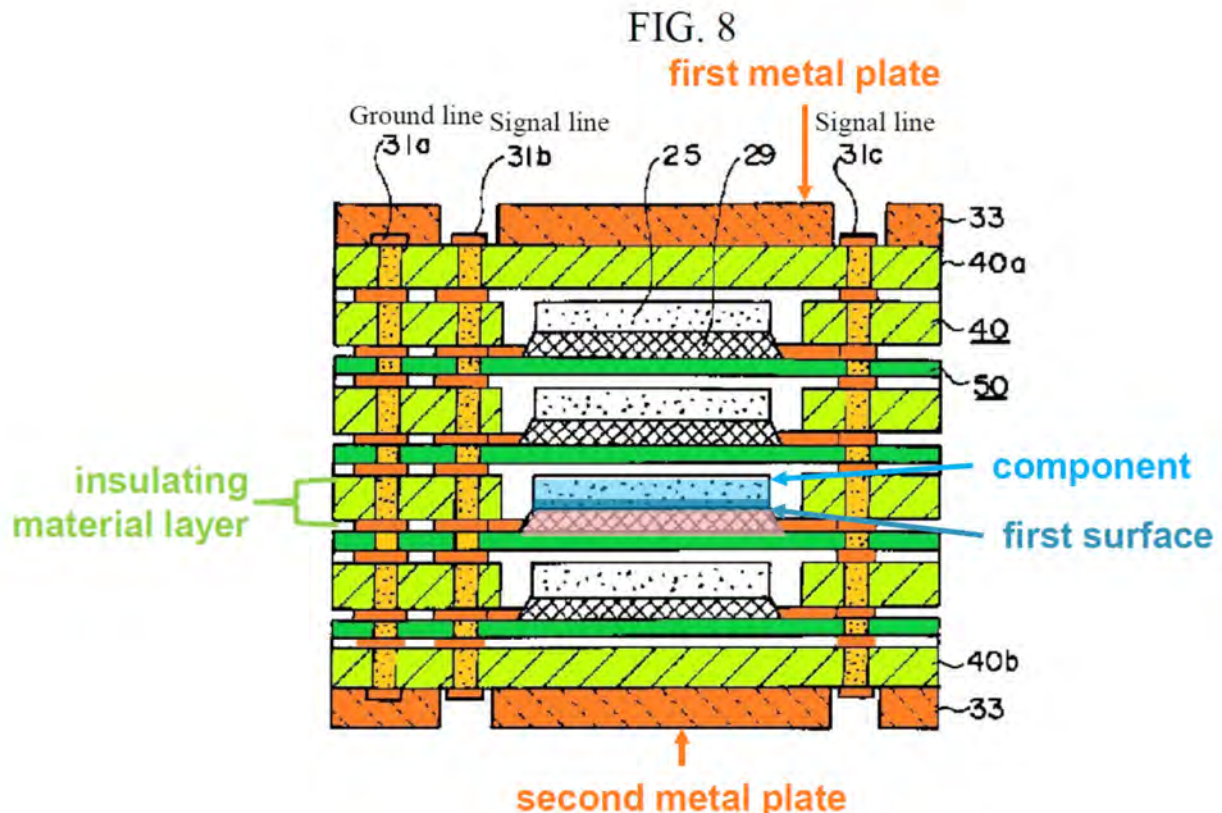


78. Bottom laminated plate 40b includes metal film 33, which is the claimed “second conductive pattern layer[] defining a second metal plate” for the same reasons discussed above in connection with the first side and first metal plate.

- e. **Element 1[d]: a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface**

79. Imoto discloses and renders obvious Element 1[d].

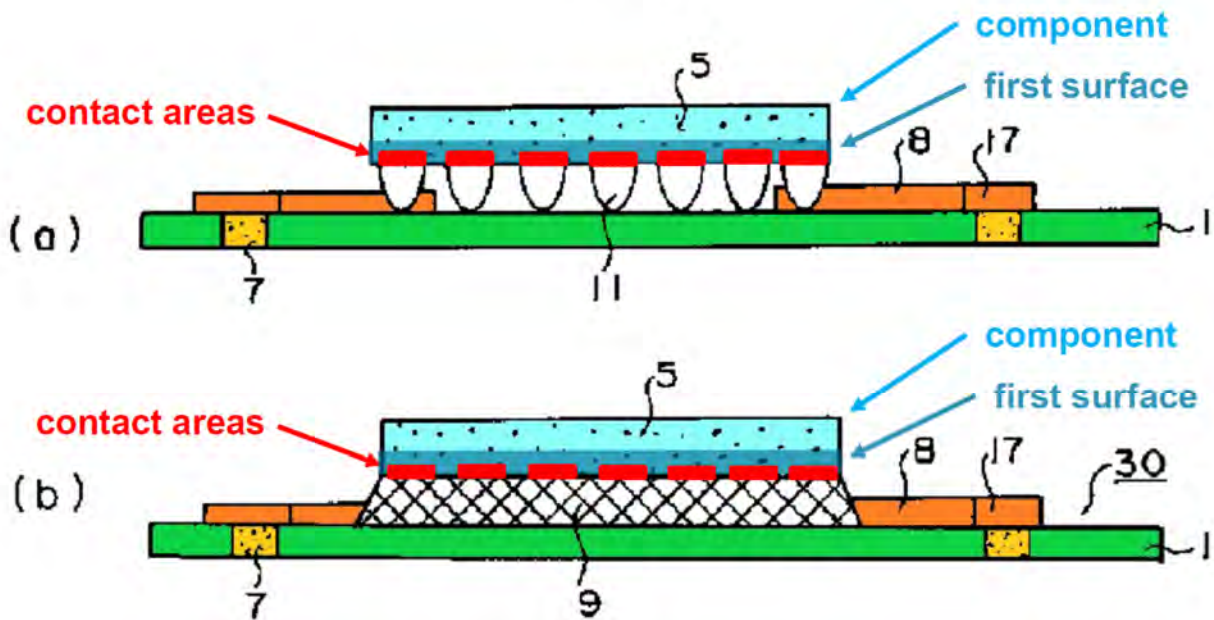
80. As shown below, the component is semiconductor element 25 (light blue), which is inside the insulating material layer and between the first and second metal plates. Ex-1007, ¶0021.



As shown above, the first surface (dark blue bottom) of semiconductor element 25 faces the second metal plate.

81. This first surface has contact areas corresponding to “connection terminals 11.” Imoto states, “In order to mount the semiconductor element 5 on the wiring substrate 30, connection terminals 11 such as a solder ball or the like are connected to the wiring pattern 8.” Ex-1007, ¶0016. A POSITA would have understood, or at least have considered it obvious, that connection terminals 11 would be electrically connected to contact areas on the first surface of semiconductor component 5/25 so that an electrical connection could be made between the semiconductor component and the wiring layers. The following Figure 3 (and later version of the same figure) shows the location of contact areas (red), although not depicted in the original figure.

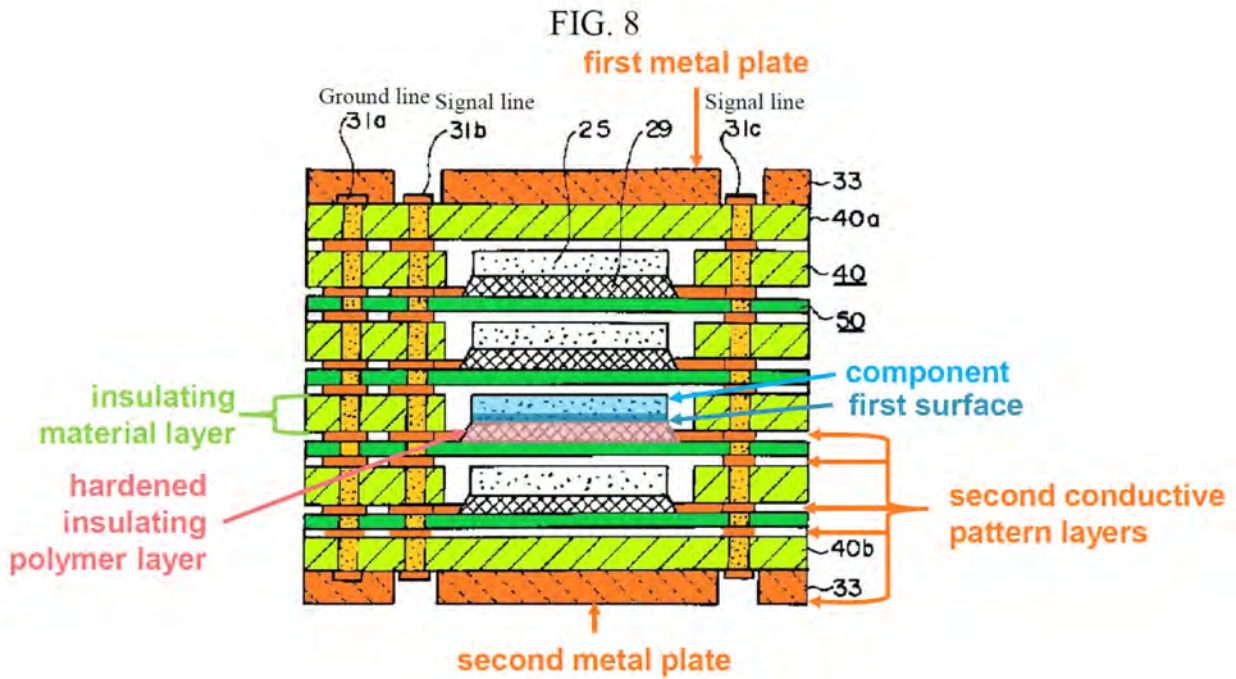
FIG. 3



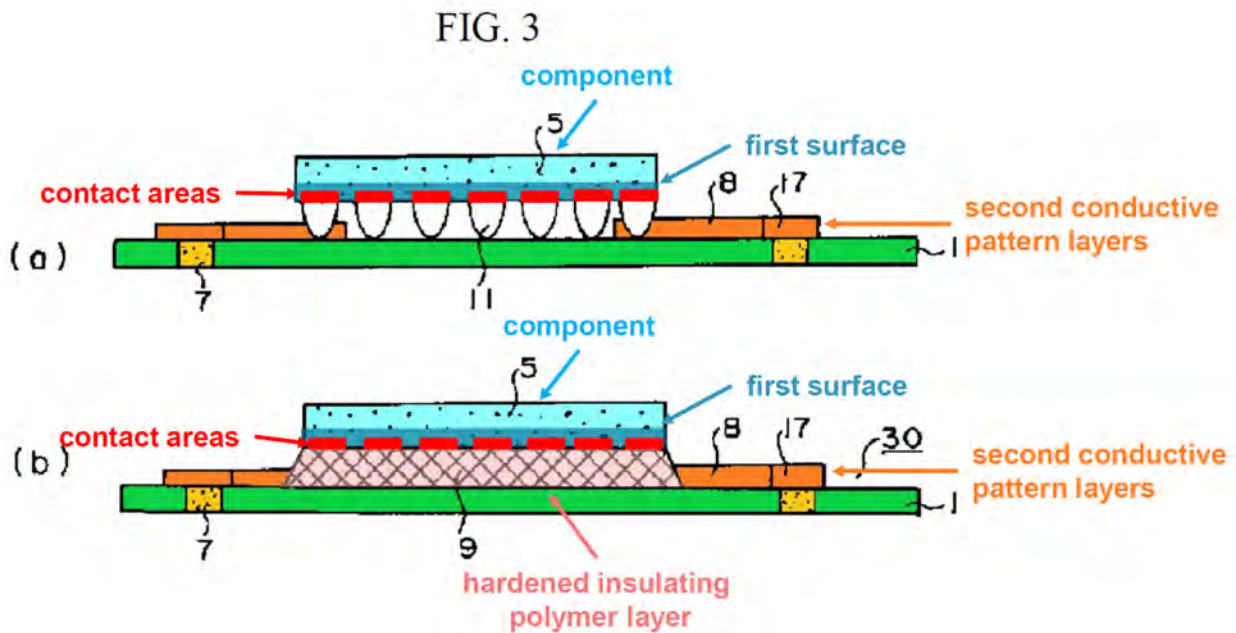
- f. **Element 1[e]: a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and**

82. Imoto discloses Element 1[e].

83. The hardened insulating polymer layer is underfill resin 29 (pink), which is located between the first surface of semiconductor component 25 (blue) and at least one second conductive pattern layer, below.



84. With reference to Figure 3 below, Imoto states that underfill resin 9/29 covers and protects connection terminal 11. Ex-1007, ¶0016.



85. A POSITA would have understood that an underfill resin is an insulating polymer that is thermally cured (*i.e.*, hardened) in place to achieve the desired encapsulant properties. For example, the Encyclopedia of Materials: Science and Technology (2001) includes a section entitled, “Semiconductor Chip Underfill Materials.” Ex-1016, 1. The section states that underfill resin is applied “in prepolymer form”:

The reinforcing resin is referred to as an underfill because it is applied ***in prepolymer form*** as a liquid that is allowed to fill the cavity under the chip. The underfill is needed, for without it the strain on the solder joints during device on/off cycles is sufficient to cause early package failure from solder fatigue. Thus, the underfill encapsulant provides a protective function analogous to the epoxy molding compounds that surround the fragile wirebonds in a conventional plastic package.

Ex-1016, 1 (emphasis added).

86. The section further describes the composition of the underfill and states that “thermal curing” generates a “hard plastic material”:

Commercial underfills are proprietary compositions from various material suppliers. Epoxy thermosetting resins are the predominant materials, but other thermosets such as cyanate esters are also used. Underfills are formulated as 100% solids compositions, *i.e.*, liquid resins and hardeners are used without solvents or volatile additives. ***Thermal curing of these compositions generates a hard plastic material*** without appreciable weight loss.

Ex-1016, 1 (emphasis added). A POSITA would have understood that a “hard plastic material” is a hardened insulating polymer.

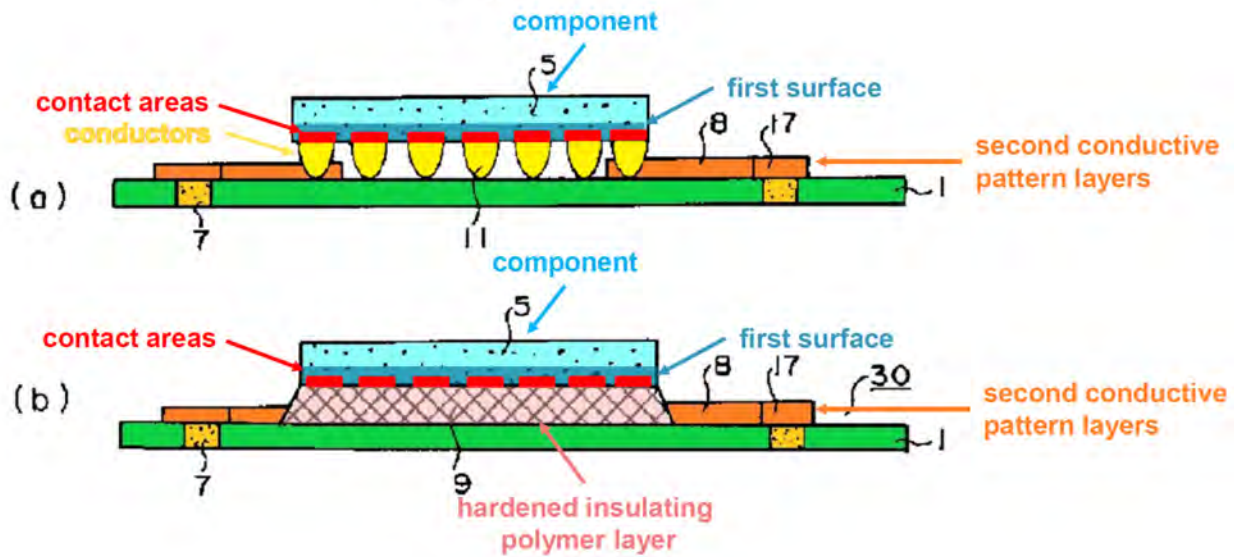
87. Imoto states that the entire structure (including underfill resin 9/29) is pressed at a curing temperature by a vacuum press or other heating compression machine. Ex-1007, ¶0016. A POSITA would have understood that, as described above, this heating cures the underfill resin to form a hardened insulating polymer layer between the first surface of component 5/25 and wiring pattern 8 of the second conductive pattern layers.

g. Element 1[f]: contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one second conductive pattern layer or layers

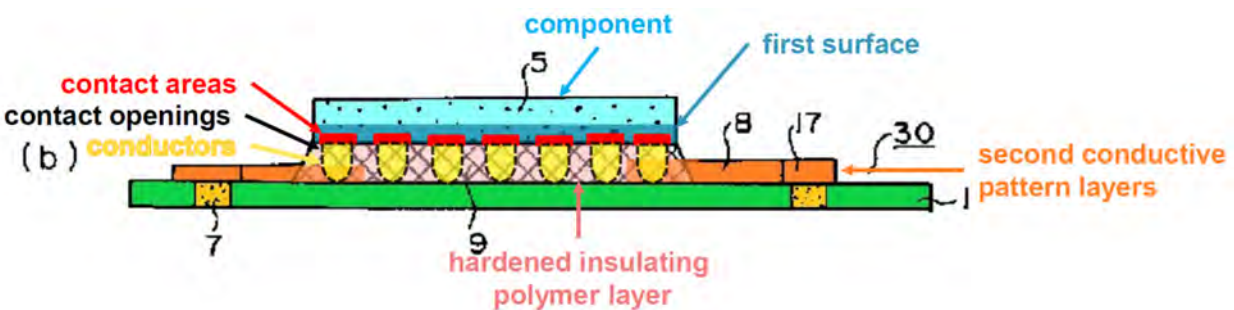
88. Imoto discloses Element 1[f].

89. In Imoto, the conductors in the contact openings are connection terminals 11 in openings in underfill resin 9/29 (the hardened insulating polymer layer). Figure 3(a) below shows connection terminals 11 (yellow) forming electrical contact between the contact areas of the semiconductor component 5/25 and wiring pattern 8. Ex-1007, ¶0016.

FIG. 3



90. Above, Figure 3(b) illustrates underfill resin 9/29 which surrounds and protects terminals 11. Ex-1007, ¶0016. The below modified version of that figure shows connection terminals 11 (which are hidden from view by underfill 9/29 in Figure 3(b)) connected to wiring pattern 8.



91. The dotted outline of terminals 11 indicates the openings in the hardened insulating polymer layer. In those contact openings, connection terminals 11 (yellow) are the conductors that electrically contact the contact areas of semiconductor component 5/25 and wiring pattern 8. Wiring pattern 8 corresponds

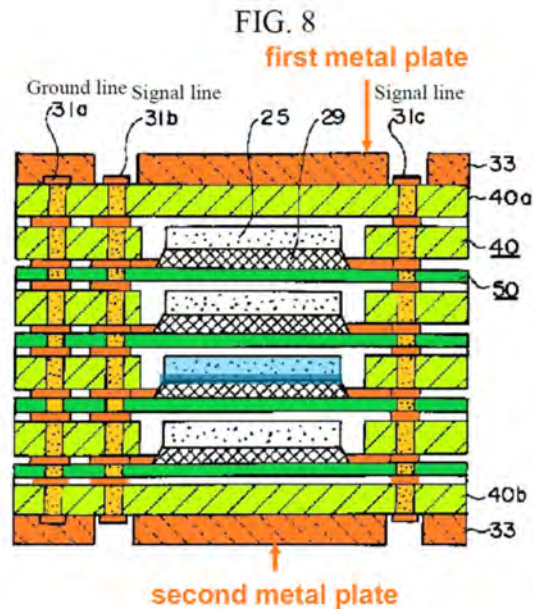
to the claimed “at least one second conductive pattern layer or layers” in Element 1[f].

2. Dependent Claim 2: The circuit board of claim 1, wherein the first and second metal plates are electrically connected to each other.

92. Imoto discloses Claim 2.

93. Imoto describes that each metal film 33 (the first and second metal plates) is connected to connection electrode 31a,⁸ which connects both metal films 33 to ground. Ex-1007, ¶0022. Thus, metal films 33 are electrically connected to each other through connection electrode 31a and to ground, as shown in Figure 8 below.

⁸ Imoto uses the term “connection electrode” for the conductors embedded in the vias. Ex-1007, ¶¶0011, 0015-16 (describing connection electrodes 2 and 7 embedded in vias and connected together by lands 3 and 17 in Figures 2-5).



3. Dependent Claim 3: The circuit board of claim 1, wherein the first and second metal plates are electrically connected to an earth connection of the circuit board.

94. Imoto discloses Claim 3.

95. As described above for Claim 2 (Section VII.A.2), metal films 33 are electrically connected to each other through connection electrode 31(a) and to ground. Ex-1007, ¶0022.

96. A POSITA would have understood this ground to be the claimed “earth connection.” Consistent with this understanding, the IEEE Dictionary defines “earth terminal” as “ground terminal.” Ex-1015, 328, 467. The IEEE Dictionary also provides the following definition of “ground” indicating that ground and earth are used interchangeably:

ground (1) (earth) (ground systems) A conducting connection, whether intentional or accidental, by which an electric circuit or equipment is connected to the earth, or to some conducting body of relatively large extent that serves in place of the earth. *Note:* It is used for establishing and maintaining the potential of the earth (or of the conducting body) or approximately that potential, on conductors connected to it, and for conducting body current to and from the earth (or the conducting body). (IA/NESC/PE/PSPD/T&D) [86], 1048-1990, 1050-1996, 1100-1992, 32-1972r, 463-1993, 524a-1993, 81-1983

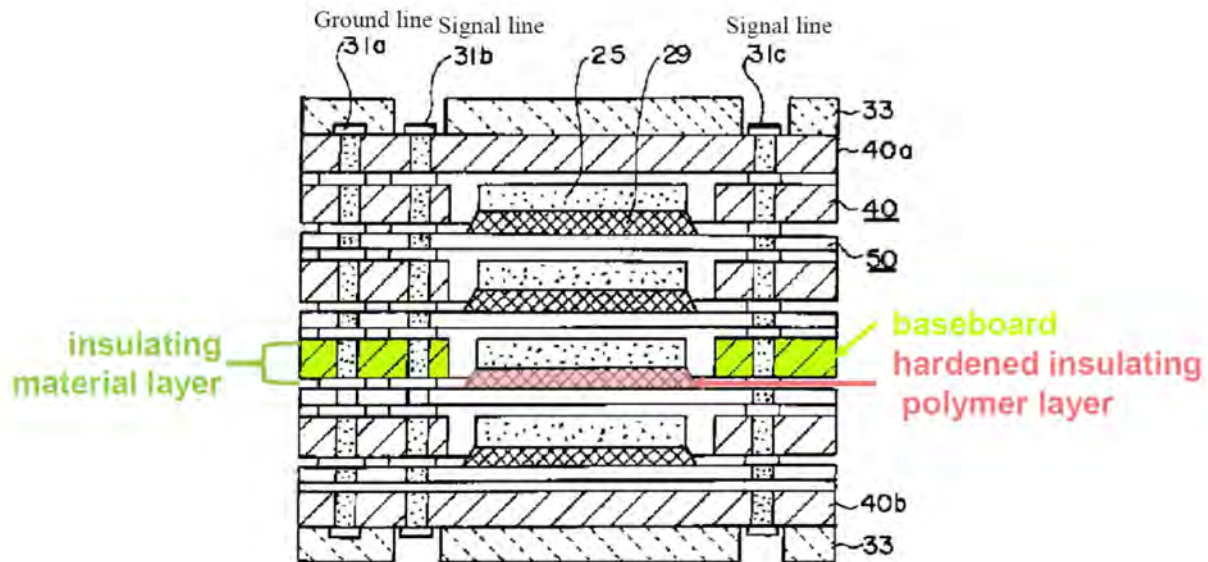
Ex-1015, 461.

4. Dependent Claim 8: The circuit board of claim 1, wherein the insulating material layer includes a baseboard and the hardened insulating polymer layer.

97. Imoto discloses Claim 8.

98. The insulating material layer includes a baseboard and the hardened insulating polymer layer, as shown below.

FIG. 8



99. As described above for Element 1[a] (Section VII.A.1.b), the insulating material layer includes laminated plate 40, which “is an insulating plate 1.” Ex-1007, ¶¶0011, 0015. Insulating plate 1 corresponds to the claimed “baseboard,” which the ’944 Patent defines baseboard broadly as encompassing organic or inorganic materials. Ex-1001, at 3:46-55. Imoto’s polyimide substrate 40 is an organic material that a POSITA thus would have considered a baseboard as described by the ’944 Patent.

100. As described above for Element 1[e] (Section VII.A.1.f), the hardened insulating polymer layer is underfill resin 29. Thus, the insulating material layer includes a baseboard and the hardened insulating material layer.

5. Dependent Claim 11: The circuit board of claim 1, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.

101. Imoto discloses or renders obvious Claim 11.

102. Imoto states, “[S]emiconductor element (chip) 5 is die-bonded and mounted on the wiring substrate 30 using a flip chip method or the like. In order to mount the semiconductor element 5 on the wiring substrate 30, connection terminals 11 such as a solder ball or the like are connected to the wiring pattern 8.” Ex-1007, ¶0016.

103. It would have been obvious to a POSITA to implement copper wiring pattern 8, to which the semiconductor element 5 is die-bonded, as at least one of electrochemically deposited copper and chemically deposited copper. For example, Imoto states, “The wiring substrate 30 on which the semiconductor element 5 is mounted is the insulating plate 6 such as a polyimide substrate with a copper foil, a printed laminated plate, or the like.” Ex-1007, ¶0016. Imoto also teaches “electroplating of copper.” Ex-1007, ¶0019; *see also id.*, ¶0015 (“copper or gold plating”), ¶0016 (same). Such electroplated copper is “electrochemically deposited copper” as recited in Claim 11. Based on these teachings, a POSITA would have been motivated to implement copper wiring pattern 8, to which the semiconductor element 5 is die-bonded, by electroplating copper because electroplating is a reliable

and efficient method of applying copper to a substrate. In so doing, the conductors in the openings of underfill resin 9/29 (hardened insulating polymer layer) would include electrochemically deposited copper.

104. For example, a POSITA would have understood that at least some of the electrochemically deposited copper would diffuse up with connection terminals 11 in the openings of underfill resin 9/29 (hardened insulating polymer layer).

6. Dependent Claim 13: The circuit board of claim 1, wherein the component is a microcircuit.

105. Imoto discloses Claim 13.

106. As described above for Element 1[d] (Section VII.A.1.4), the claimed component is semiconductor element 25. Ex-1007, ¶¶0003, 0011, 0021. The '944 Patent does not define microcircuit, but a POSITA would have understood a microcircuit to encompass an integrated circuit, such as a semiconductor chip (semiconductor 25). The IEEE Dictionary defines “microcircuit” by reference to “integrated circuit”:

microcircuit *See: integrated circuit.*

Ex-1015, 652.

107. The dictionary provides the following definition of “integrated circuit”:

integrated circuit (IC) (1) (solid state) A combination of interconnected circuit elements inseparably associated on or within a continuous substrate. *Note:* To further define the nature of an integrated circuit, additional modifiers may be prefixed. Examples are: 1) dielectric-isolated monolithic integrated circuit, 2) beamlead monolithic integrated circuit, 3) silicon-chip tantalum thin-film hybrid integrated circuit. *See also:* element; film integrated circuit; integrated electronics; multichip integrated circuit. (ED) [46], 274-1966w
(2) (A) A combination of connected circuit elements (such as transistors, diodes, resistors, and capacitors) inseparably associated on or within a continuous substrate. *Synonym:* chip. *See also:* program. **(B)** A solid-state circuit consisting of interconnected active and passive semiconductor devices diffused into a single silicon chip. *Synonyms:* chip; microcircuit. *See also:* monolithic integrated circuit; very-high-speed integrated circuit. (C) 610.10-1994

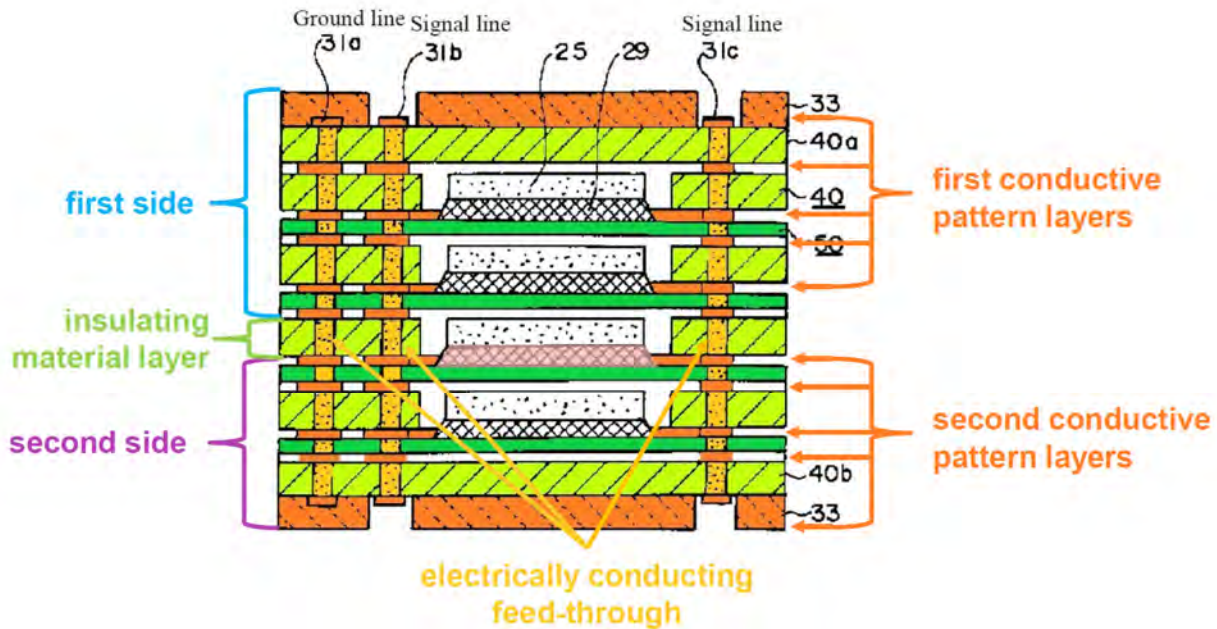
Ex-1015, 536-37.

7. **Dependent Claim 14: The circuit board of claim 1, comprising an electrically conducting feed-through between the conductive pattern layers on the both sides of the insulating material layer.**

108. Imoto discloses Claim 13.

109. As shown below, Figure 8 includes electrically conducting feed-throughs between the conductive pattern layers on both sides of the insulating material layer.

FIG. 8



110. Imoto uses the term “connection electrode” for the conductors embedded in the vias. Ex-1007, ¶¶0011, 0015-16 (Figures 2-5, describing connection electrodes 2 and 7 embedded in vias and connected together by lands 3 and 17). Figure 8 includes “connection electrode 31a that connects to the ground ... line, and connection electrodes 31b, 31c that connects to a signal line.” *Id.*, ¶0022. Any of connection electrodes 31a, 31b, or 31c discloses Claim 13.

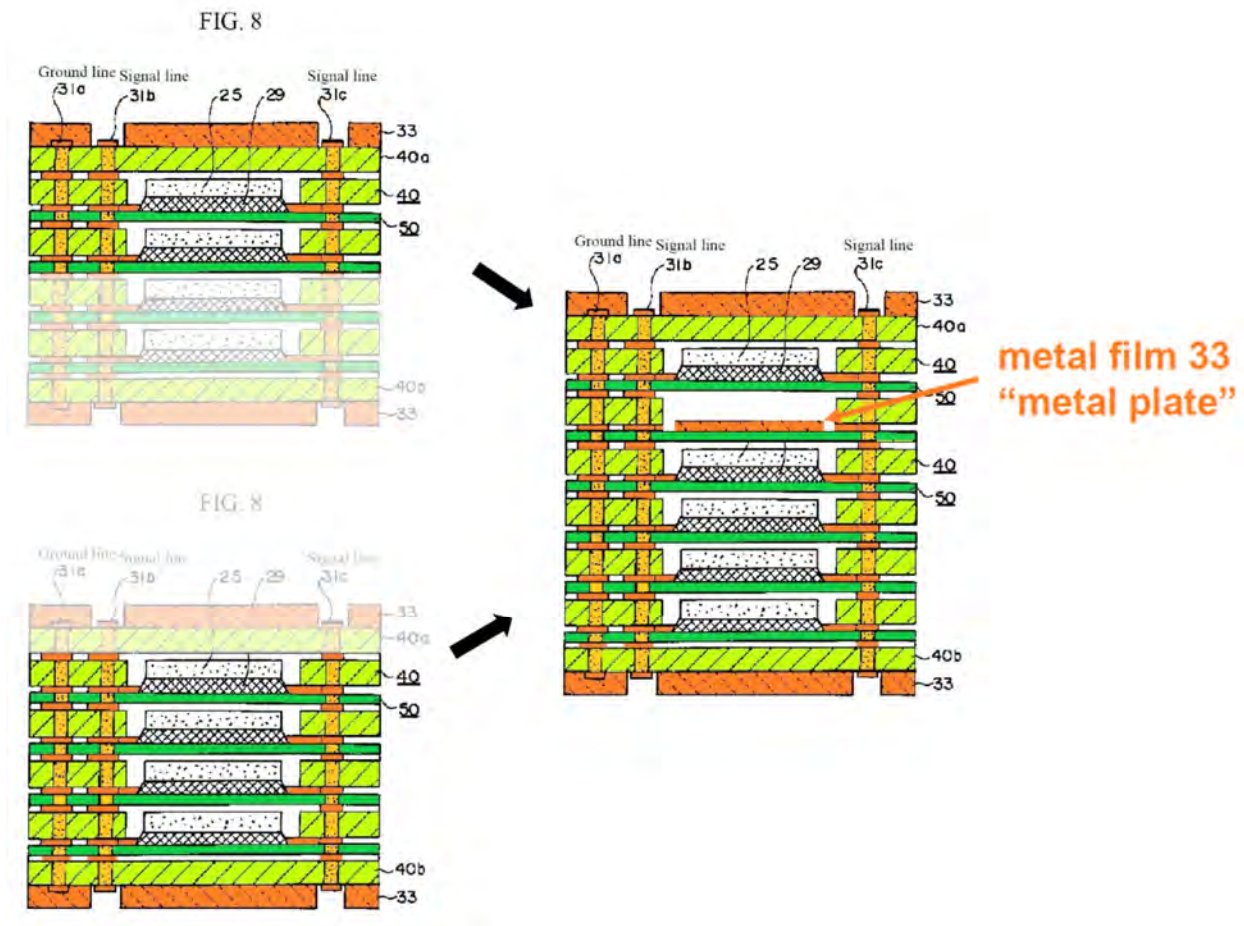
8. Independent Claim 15

111. Imoto renders obvious Claim 15.

112. Claim 15 is the same as Claim 1, except for the preamble. Claim 15 recites “a multi-layered circuit board comprising a first circuit board substructure and second circuit board substructure on top of each other, wherein at least the first

circuit board substructure comprises” the same Elements [a]-[f] as recited in Claim 1.

113. Imoto teaches the preamble of Claim 15, to the extent it is limiting. Imoto discloses a multilayer structure that includes any number of layers. Ex-1007, ¶0010; *see also* Ex-1007, Claims 1, 2, 8 (reciting “a plurality of wiring substrates” and “a plurality of conductive via insulating substrates”). To form additional layers as taught in Imoto, it would have been obvious to a POSITA to stack copies of layers from Figure 8 as shown in the modified figure below, to add functionality, reduce manufacturing cost, and save space.



114. A POSITA would have been motivated to form metal film 33 on laminated plate 50 in the middle of the stacked structure (for example, in a cavity that would otherwise include semiconductor element 25) because Imoto states that metal film 33 is grounded to provide a “shielding effect.” Ex-1007, ¶0022. A POSITA would have understood that such a grounded shield is used to protect semiconductor elements 25 from electromagnetic interference and that such interference can come from either outside or internal sources (such as other semiconductor elements 25). Thus, a POSITA would have been motivated to

include metal film 33 in the middle of the stacked structure to shield semiconductor element 25 on either side of metal film 33 from interfering with one another.

115. For example, it would have been obvious to a POSITA to put semiconductor element 25 emitting substantial electromagnetic interference (such as a high-frequency RF chip) on top and separate it from other semiconductor elements 25 by a grounded metal film 33 to shield the other semiconductor elements 25 from the electromagnetic interference.

116. Furthermore, the use of a shield between semiconductors 25 embedded in insulating layers was well known in the art. For example, Figure 2 of U.S. Patent No. 6,459,593 (“Kwong”) shows components 156 and 158 embedded in insulating layers 130 and 132 and teaches the use of shield plate 162 between components 156 and 158 to shield electromagnetic interference (EMI) between components 156 and 158. Ex-1020, 7:57-65; 8:35-41, 8:48-50. Similarly, Japanese Publication JP2001-237586A (“Asahi Japanese Publication”) teaches shield body 804 for shielding electromagnetic waves in Figure 8h, and shield body 804 includes a metal plate between insulating substrates 101 with embedded circuit components 806. Ex-1021, ¶¶119-20, 126-27.

117. As another example, Figure 10 of U.S. Patent Publication No. 2003/0090833 (“Asahi U.S. Publication”) includes shield electrode 1010 between built-in semiconductors 1006 and electronic components 1004. Ex-1025, ¶0089.

Shield electrode 1010 is made using the same materials and process as wiring patterns 1002. *Id.* Asahi U.S. Publication teaches that shield electrode 1010 is grounded and reduces interference among built-in semiconductors 1006 and electronic components 1004. *Id.* Figure 11 of Asahi U.S. Publication includes a similar electromagnetic shielding layer 1110 between semiconductors 1006 and electronic components 1004, and Asahi U.S. Publication teaches that electromagnetic shielding layer 1110 reduce the interference of electromagnetic waves among built-in semiconductors 1106 and electronic components 1104. Ex-1025, ¶¶0091-92.

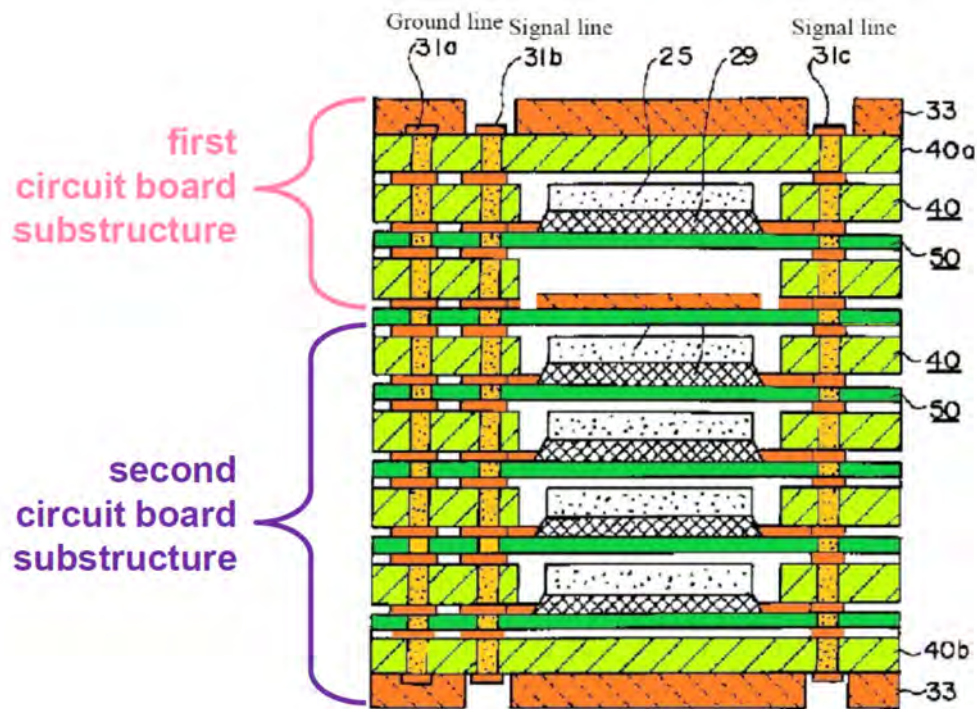
118. In addition, Japanese Publication JP2001-111232A (“Oya”) teaches shield patterns 6A and 6B on either sides of a wiring substrate 2 located between LSI chips 3A and 3B, as shown in Figure 1 and 6. Ex-1023, ¶0015. Shield patterns 6A and 6B are grounded so that LSI chips 3A and 3B are electromagnetically shielded from one another. Ex-1023, ¶¶0015-16, 0019, 0049.

119. Thus, a POSITA would have been motivated to include metal film 33 in the middle of the stacked structure to shield semiconductors 25 on either side of metal film 33 from interfering with one another.

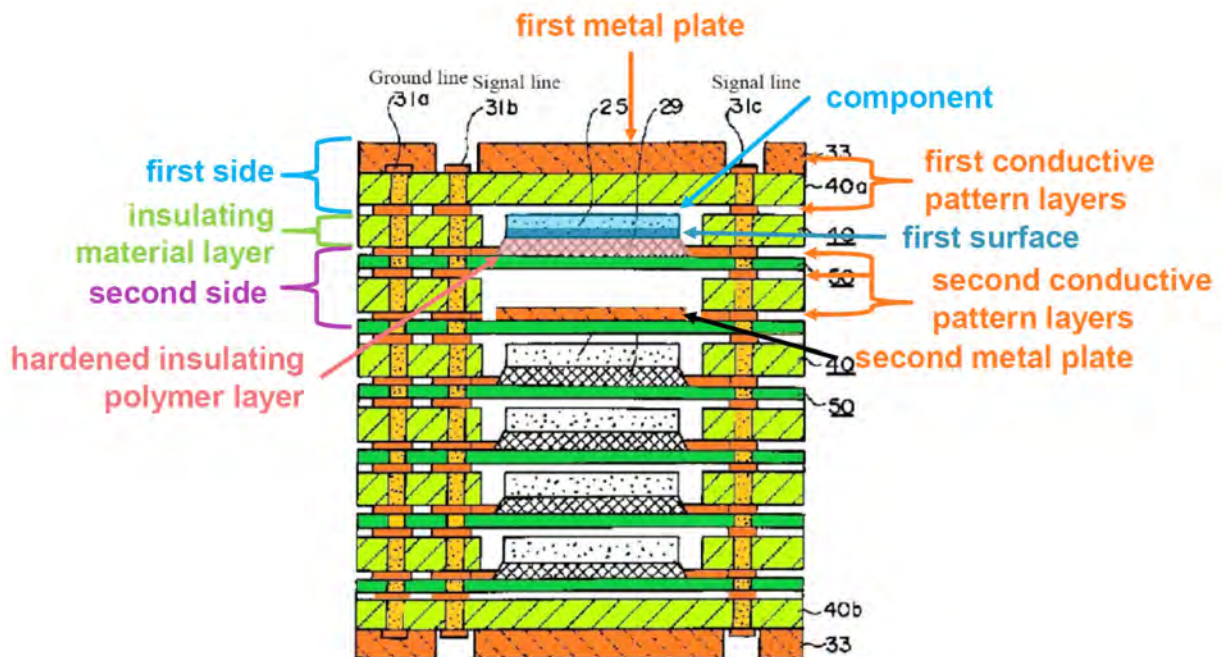
120. A POSITA would have had a reasonable expectation of success in forming metal film 33 on laminated plates 50 in the middle of the structure. Metal film 33 is formed of “metal foil” (Ex-1007, ¶0022) like the wiring pattern 8 and land

17 on laminated plates 30/50 (Ex-1007, ¶¶0011, 0015). Furthermore, Imoto teaches to “adjust[] the material and thickness of the metal film, the material and width of the connection electrodes, and the like as need[ed].” Ex-1007, ¶0022.

121. The above stacked structure discloses Claim 15. The first circuit board substructure is above the second circuit board substructure, as shown below.



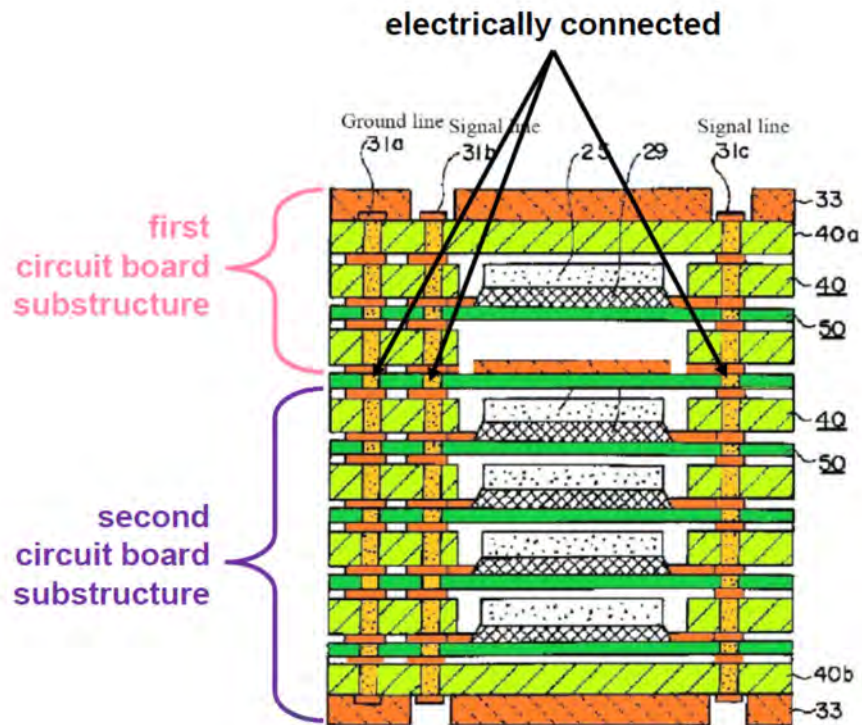
122. As shown below, the first circuit board substructure meets Elements 15[a]-15[f] as described above for corresponding Elements 1[a]-1[f] (Section VII.A.1).



9. **Dependent Claim 16:** The multi-layered circuit board of claim 15, wherein said first circuit board substructure and said second circuit board substructure are electrically connected to each other to form a multi-layered functioning totality.

123. Imoto renders obvious Claim 16.

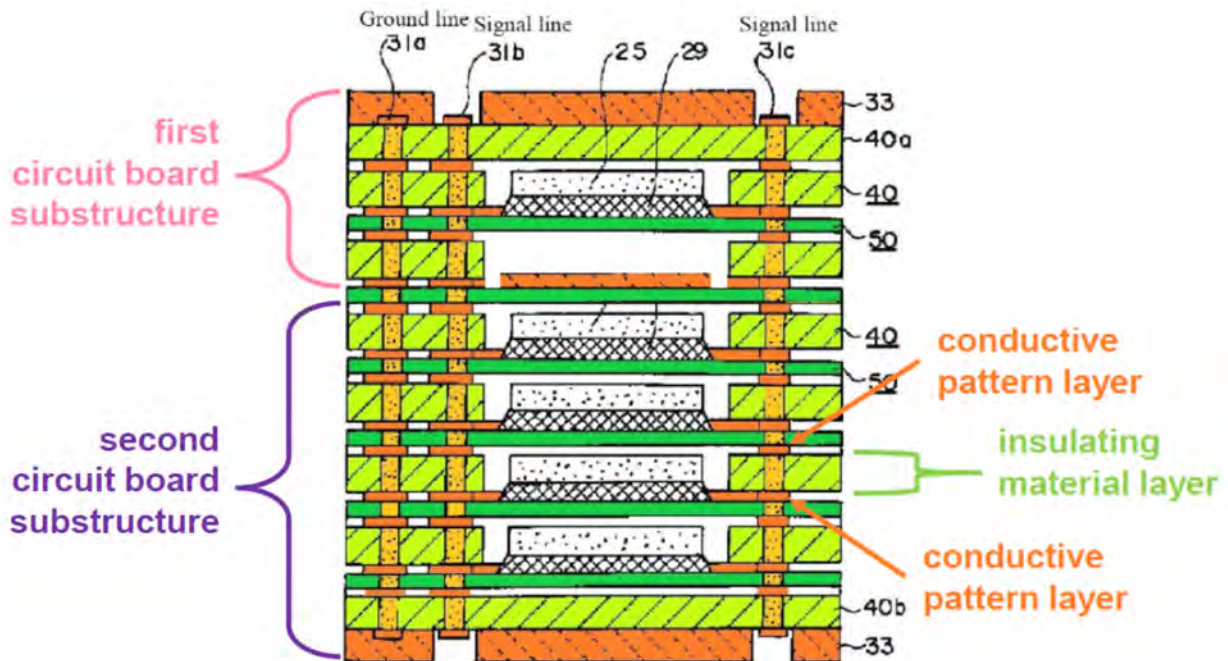
124. As described above for Claim 2 (Section VII.A.2), metal films 33 are electrically connected to each other through connection electrode 31a and to a ground line. Ex-1007, ¶0022. Thus, the two circuit board substructures “are electrically connected to each other to form a multi-layered functioning totality,” through at least connection electrodes 31a, 31b, and 31c as illustrated below.



10. **Dependent Claim 17: The multi-layered circuit board of claim 16, wherein said second circuit board substructure comprises an insulating material layer and at least one conductive pattern layer in the insulating material layer.**

125. Imoto renders obvious Claim 17.

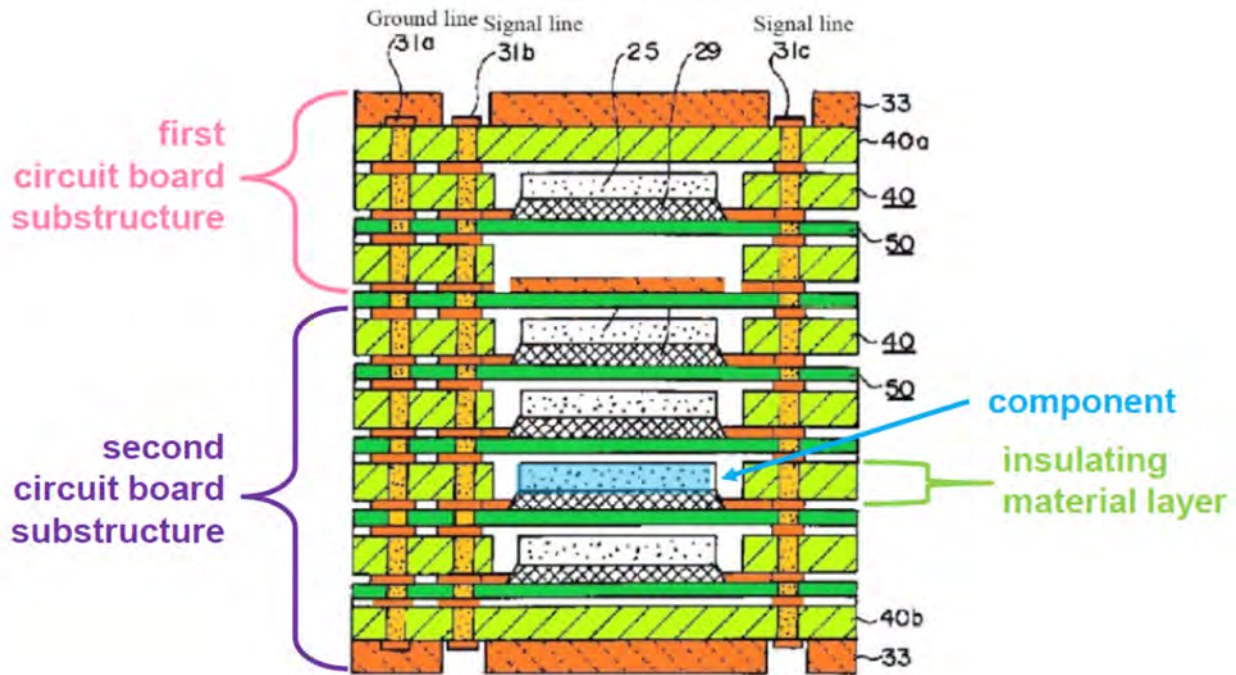
126. As shown below, the second circuit board substructure includes an insulating material layer and at least one conductive pattern layer in the insulating material layer, for the reasons described above for Element 1[a] (Section VII.A.1.b) and Element 1[b] (Section VII.A.1.c).



11. **Dependent Claim 18:** The multi-layered circuit board of claim 17, wherein said second circuit board substructure includes a component embedded in the insulating material layer.

127. Imoto renders obvious Claim 18.

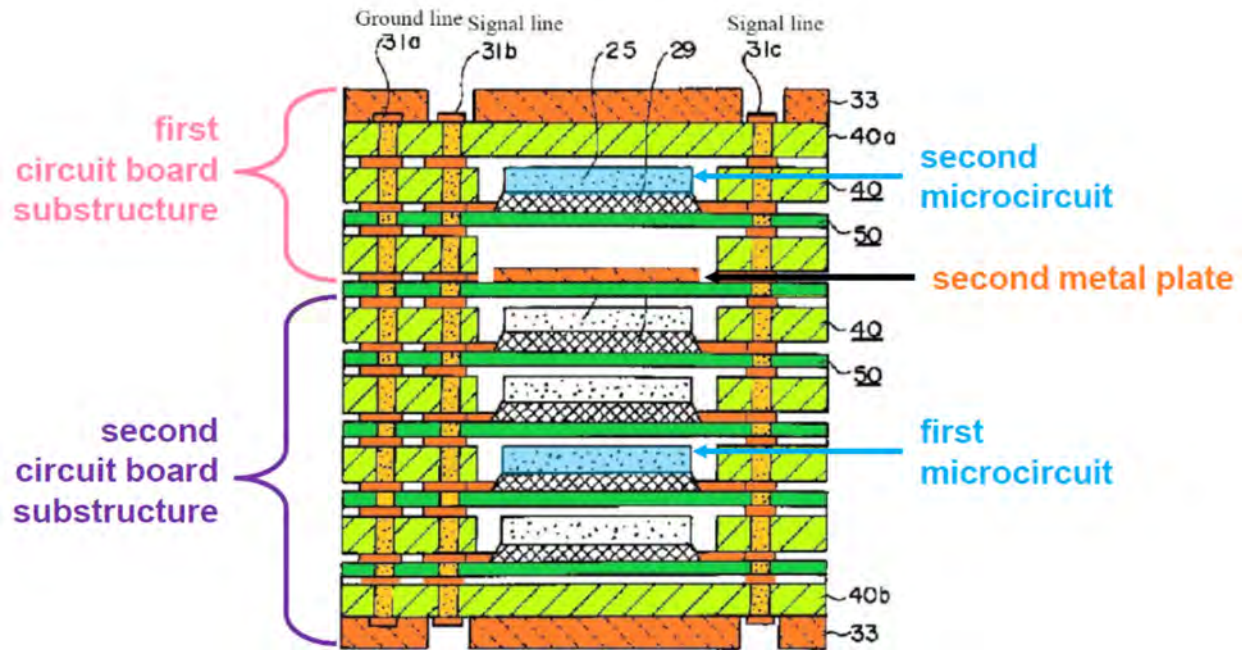
128. As shown below, the second circuit board substructure includes a component embedded in the insulating material layer, for the reasons described above for Element 1[e] (Section VII.A.1.f).



12. **Dependent Claim 19:** The multi-layered circuit board of claim 15, wherein said first circuit board substructure comprises a first microcircuit and said second circuit board substructure comprises a second microcircuit such that the first and second microcircuits are on top of each other and at least one of the first and second metal plates is located between said first and second microcircuits.

129. Imoto renders obvious Claim 19.

130. As shown below, the first circuit board substructure includes a first microcircuit, and the second circuit board substructure includes a second microcircuit on top of the first microcircuit. Metal film 33 on laminated plates 40 in the middle of the structure is the second plate, which is located between the two microcircuits.



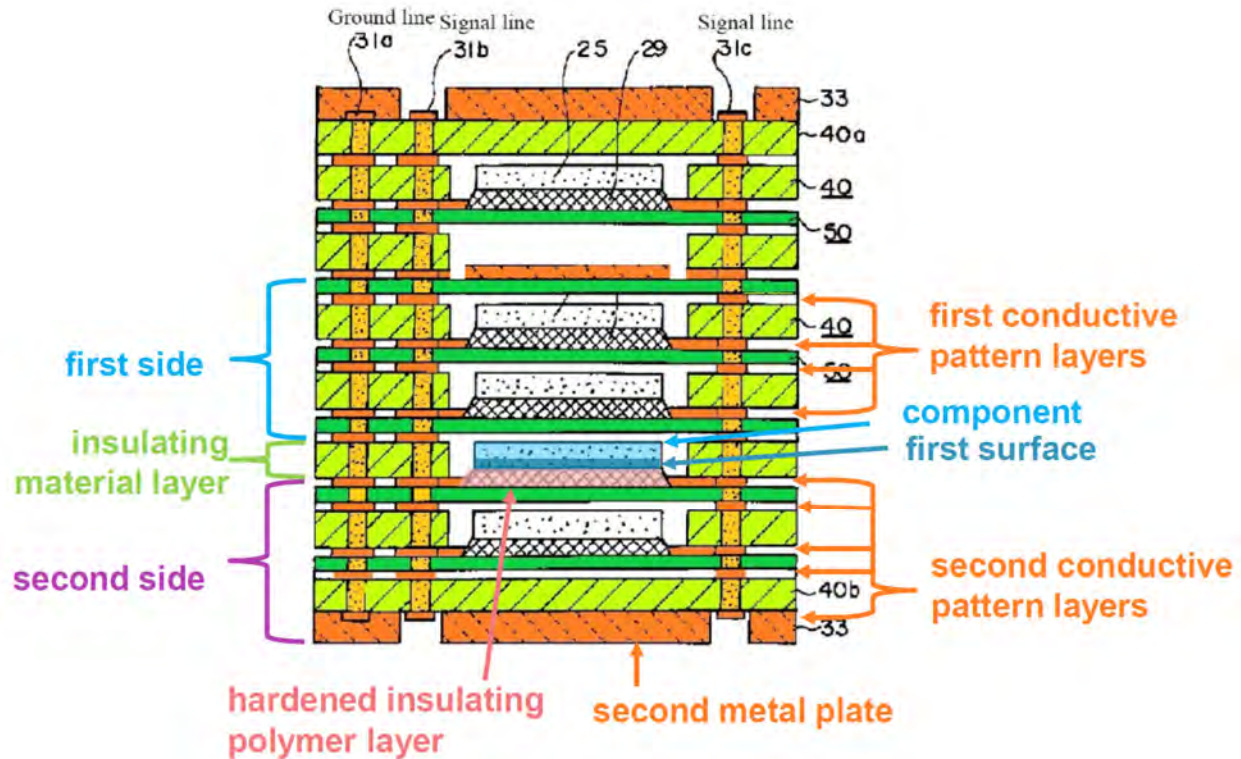
131. As explained above for Claim 13 (Section VII.A.6), a POSITA would have understood a microcircuit to encompass an integrated circuit, such as a semiconductor chip (semiconductor 25).

13. Dependent Claim 20

132. Imoto renders obvious Claim 20.

133. Claim 20 requires that the second circuit board substructure include Elements 1[a]-1[f] of Claim 1, except the **first** metal plate on the first side of the insulating material layer. *Compare* Elements 20[a]-[f] with Elements 1[a]-[f].

134. As shown below, the second circuit board substructure meets Elements 20[a]-20[f] as described above for Elements 1[a]-1[f] (Section VII.A.1). .

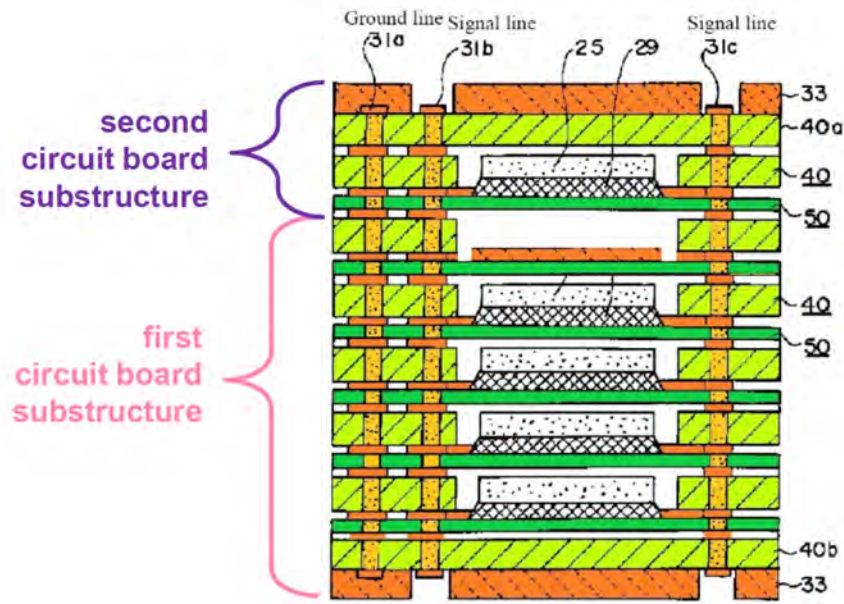


14. Dependent Claim 21

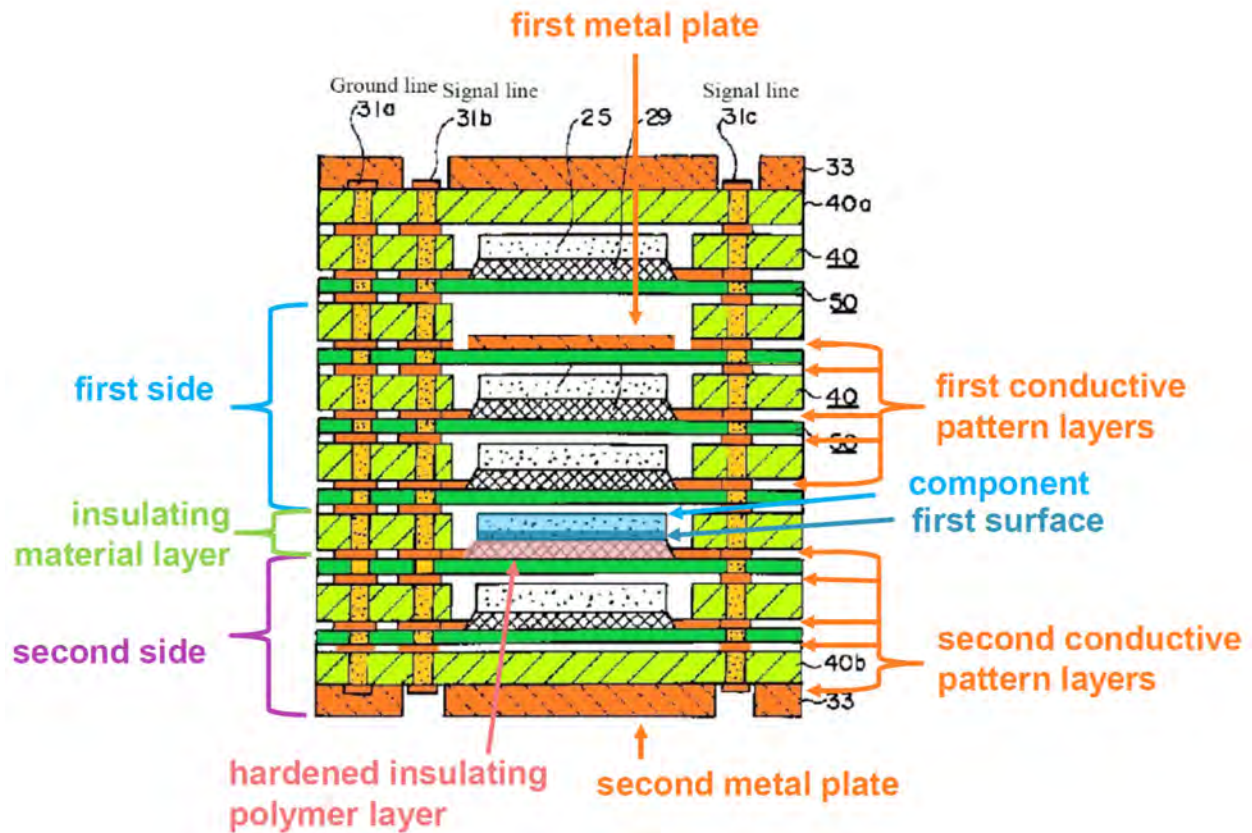
135. Imoto renders obvious Claim 21.

136. Claim 21 is like Claim 20, with one minor difference. Claim 21 requires that the second circuit board substructure include all elements of Claim 1, except the ***second*** metal plate on the second side of the insulating material layer. *Compare* Elements 21[a]-[f] to Elements 1[a]-[f].

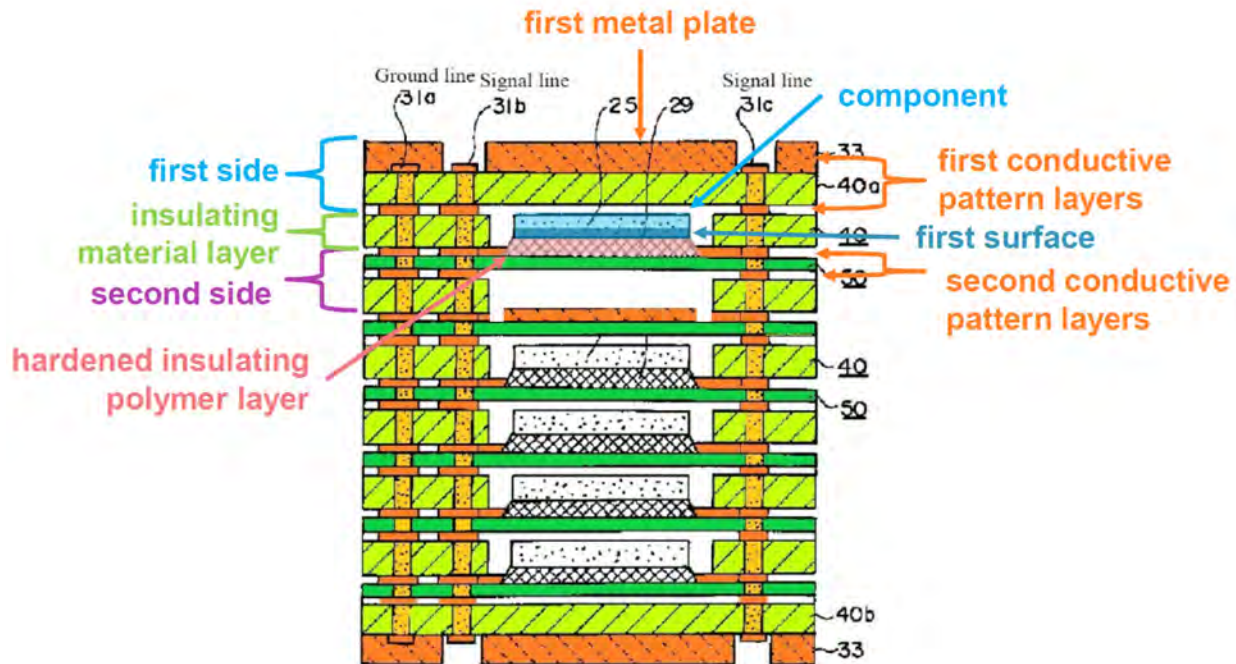
137. Imoto renders obvious Claim 21 under an alternative mapping, where the first circuit board substructure is beneath the second circuit board substructure, as shown below.



138. As shown below, the first circuit board substructure meets Elements 15[a]-15[f] as described above for Elements 1[a]-1[f] (§VII.A.1).



139. As shown below, the second circuit board substructure meets Elements 20[a]-20[f] as described above for Elements 1[a]-1[f] (Section VII.A.1).

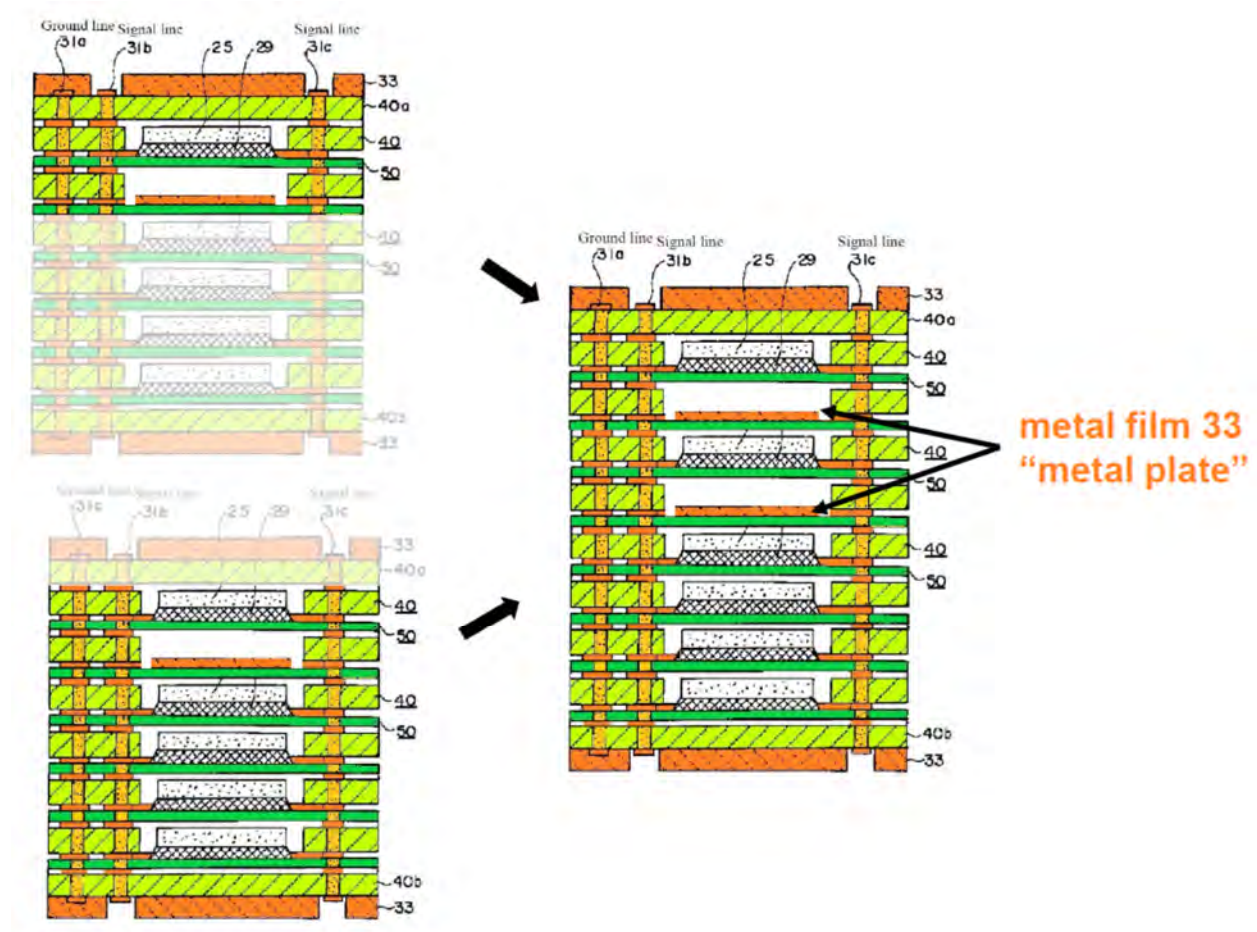


15. Dependent Claims 22: The multi-layered circuit board of claim 15, comprising a third circuit board substructure on top of the first and second circuit board substructures.

140. Imoto renders obvious Claim 22.

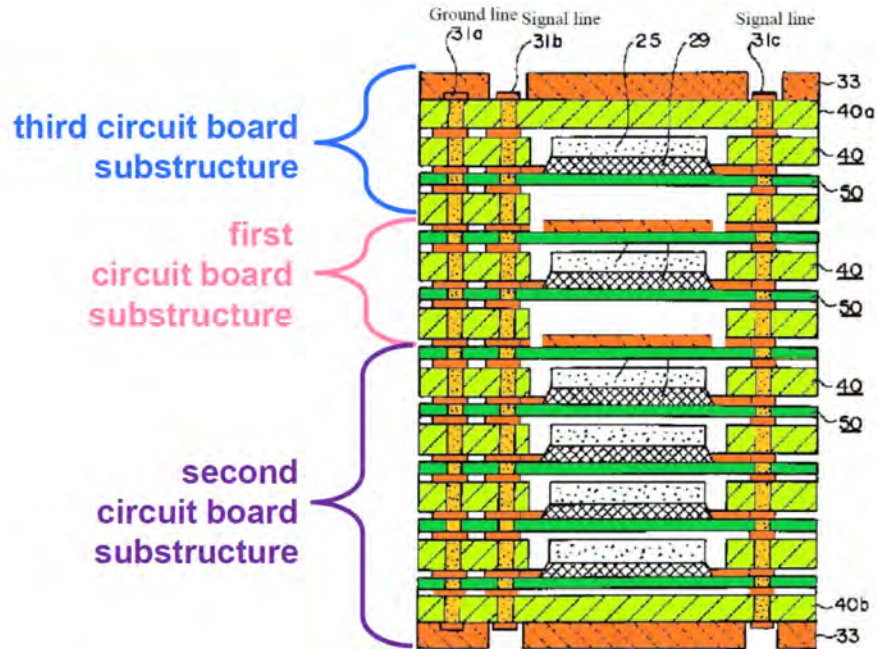
141. Claims 22 introduce a third circuit board substructure on top of the first and second circuit board substructures of Claim 15.

142. The below figure shows the structure described above for Claims 15-21, but adds more layers on top for the same reasons described above for Claim 15 (Section VII.A.8).

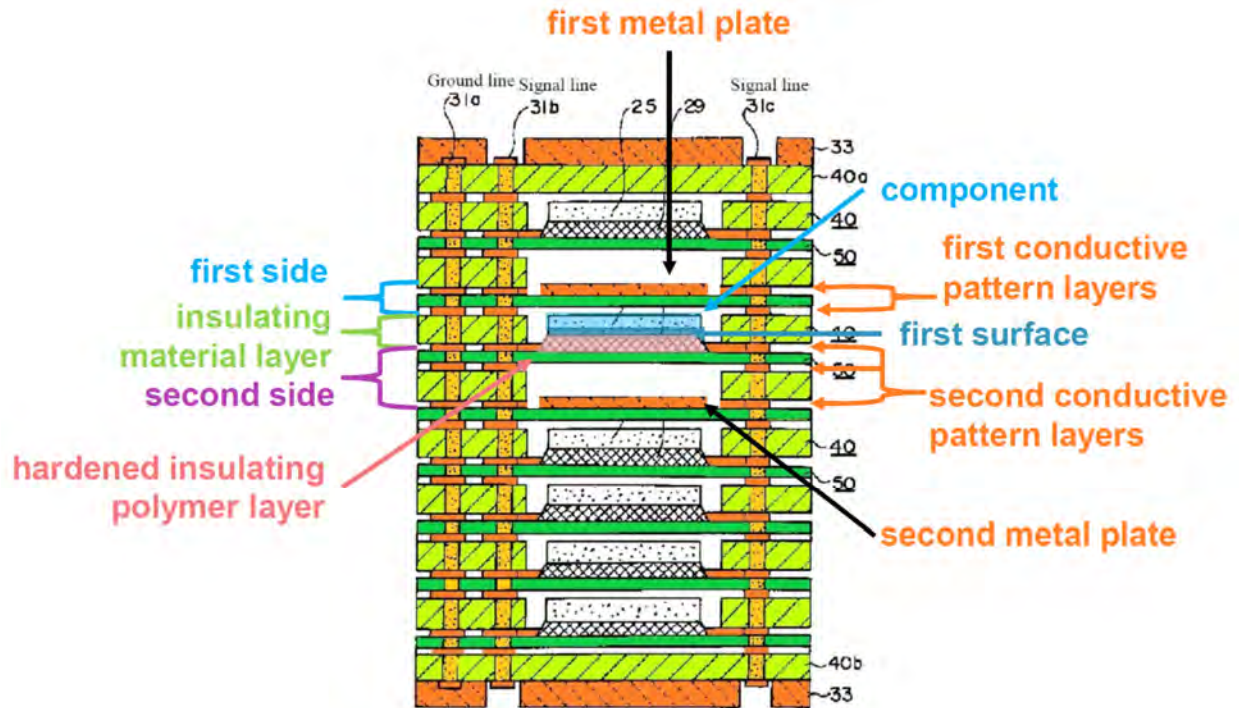


143. For the reasons described above in Claim 15 (Section VII.A.8), Imoto teaches that the structure can include additional layers and, thus, it would have been obvious to a POSITA to add layers to increase functions, reduce manufacturing costs, and save space.

144. As shown below, a third circuit board substructure is on top of the first and second circuit board substructures, as recited in Claim 22.



145. As shown below, the first circuit board substructure meets Elements 15[a]-15[f] as described above for corresponding Elements 1[a]-1[f] (Section VII.A.1).



16. **Dependent Claim 23: The multi-layered circuit board of claim 22, wherein the first circuit board substructure is between the second and third circuit board substructures.**

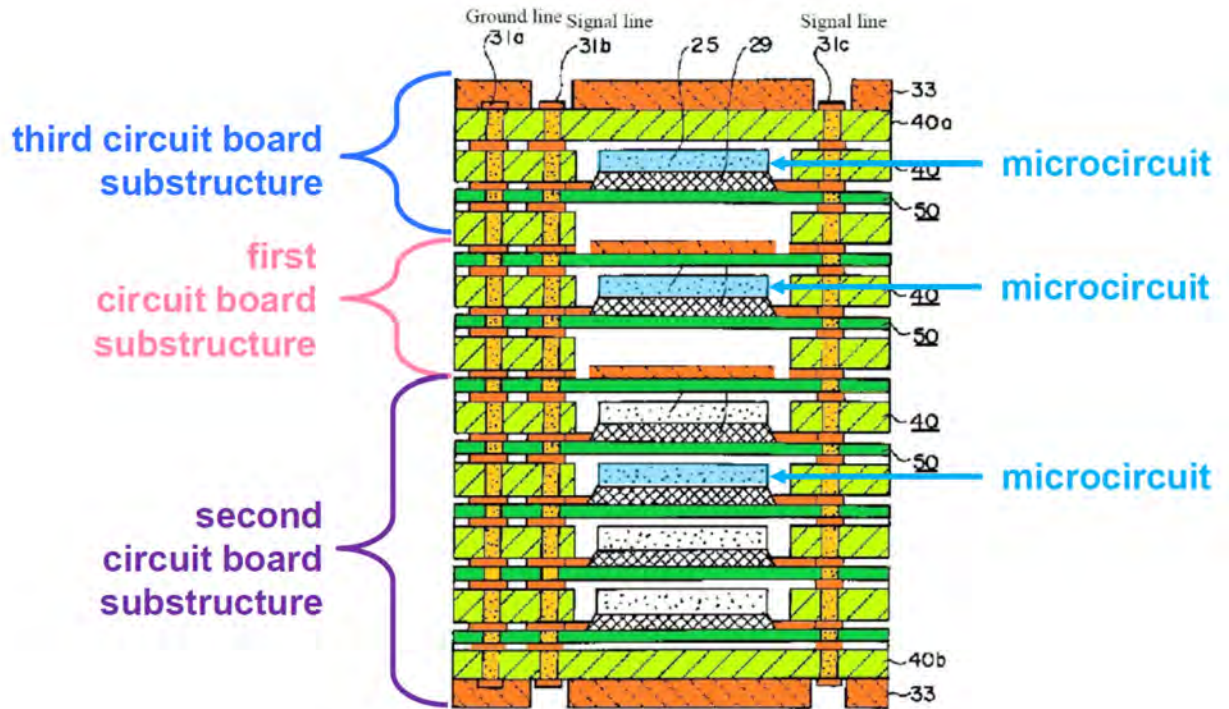
146. Imoto renders obvious Claim 23.

147. As shown above for Claim 22 (Section VII.A.15), the first circuit board substructure is between the second and third circuit board substructures.

17. **Dependent Claim 24: The multi-layered circuit board of claim 22, wherein each of the first, second and third circuit board substructures includes an embedded microcircuit.**

148. Imoto renders obvious Claim 24.

149. The first, second and third circuit board substructures identified above for Claim 22 (Section VII.A.15) include embedded microcircuits, and thus, Imoto renders obvious Claim 24, as shown below.



150. As explained above for Claim 13 (Section VII.A.6), a POSITA would have understood semiconductor elements 25 are microcircuits.

18. Dependent Claim 25: The multi-layered circuit board of claim 15, wherein the first and second metal plates are electronically connected to each other.

151. Claim 25 is the same as Claim 2 but depends from Claim 15. For the reasons described for Claim 2 (§VII.A.2) and Claim 15 (§VII.A.8), Imoto renders obvious Claim 25.

19. Dependent Claim 26: The multi-layered circuit board of claim 15, wherein the first and second metal plates are electrically connected to each other.

152. Claim 26 is the same as Claim 2 but depends from Claim 15.

153. For the reasons described above for Claim 2 (Section VII.A.2) and Claim 15 (Section VII.A.8), Imoto renders obvious Claim 26.

20. Dependent Claim 29: The multi-layered circuit board of claim 15, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.

154. Claim 29 is the same as Claim 11 but depends from Claim 15.

155. For the reasons described above for Claim 11 (Section VII.A.5) and Claim 15 (Section VII.A.8), Imoto renders obvious Claim 29.

21. Dependent Claim 30: The multi-layered circuit board of claim 15, wherein the component is a microcircuit.

156. Claim 30 is the same as Claim 13 but depends from Claim 15.

157. For the reasons described above with reference to Claim 13 (Section VII.A.6) and Claim 15 (Section VII.A.8), Imoto renders obvious Claim 30.

158. As explained above for Claim 13 (Section VII.A.6), a POSITA would have understood a microcircuit to encompass an integrated circuit, such as a semiconductor chip (semiconductor 25).

22. Dependent Claims 31: The multi-layered circuit board of claim 15, wherein the first circuit board substructure comprises at least two microcircuits inside the insulating material layer.

159. Imoto renders obvious Claim 31.

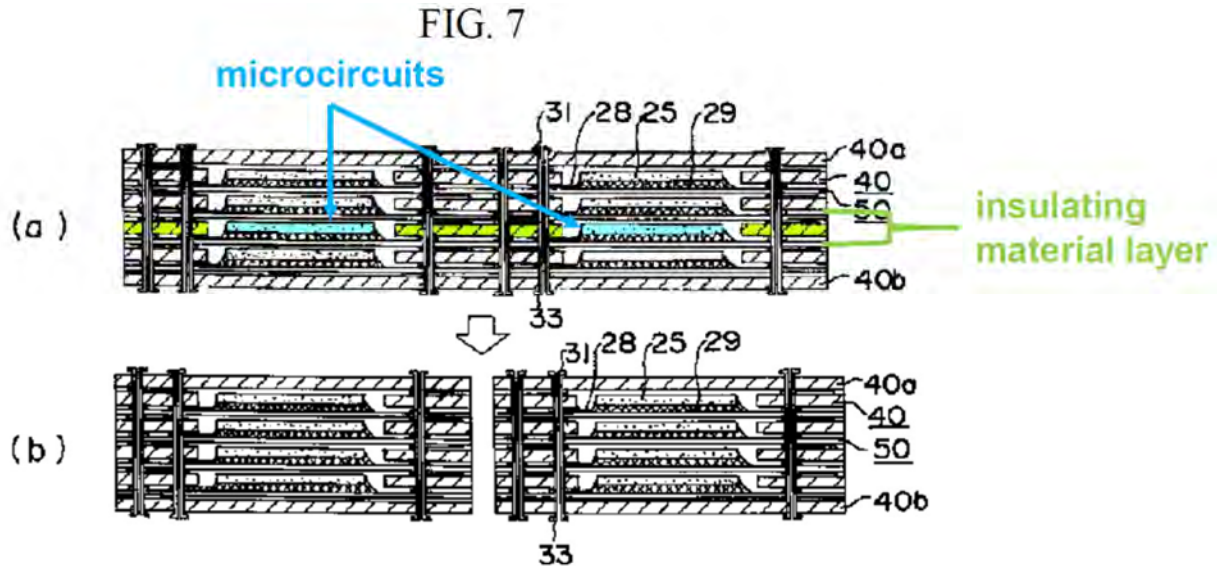
160. As described above for Claim 15 (Section VII.A.8), the first circuit board substructure includes at least two microcircuits, as recited in Claim 31.

161. As explained above for Claim 13 (Section VII.A.6), a POSITA would have understood a microcircuit to encompass an integrated circuit, such as a semiconductor chip (semiconductor 25).

162. To the extent Claim 31 is argued to require that the two microcircuits be located in a single insulating material layer, Imoto discloses that two microcircuits (semiconductor elements 25) can be embedded in each insulating material layer (laminated plate 40). Ex-1007, ¶0015 (“A region where the semiconductor elements *[plural]* are stored on the insulating plate 1 such as a printed laminated plate or the like is punched out and used as the chip cavity section 12 (FIG. 2).”). Moreover, Figure 7 of Imoto shows two microcircuits (semiconductor elements 25) in insulating material layer (laminated plate 40).⁹ *Id.*, ¶0020 (“a

⁹ Although Imoto describes cutting the structure in Figure 7 into separate pieces for packaging (Ex-1007, ¶0019), it would have been obvious to a POSITA to skip the cutting step and to use the whole structure as the final product to add functionality, to reduce manufacturing costs, and to save space.

plurality of chip cavity sections are formed in the conductive via laminated plate 40, a plurality of semiconductor elements are mounted on the wiring substrate 50”).



Thus, Imoto discloses, or at least renders obvious, the first circuit board substructure including two microcircuits inside the insulating material layer.

B. Ground 2: Claims 4-7, 10, 27, 28, and 32-36 are obvious over Imoto in view of Dudderar

- 1. A POSITA would be motivated to combine Imoto and Dudderar’s teachings and would have a reasonable expectation of success.**

163. In addition to the reasons set out below with respect to specific claim elements, a POSITA would have been motivated to combine the teachings of Imoto and Dudderar and would have had a reasonable expectation of success in doing so because each relates to the same well-known technologies. Both relate to embedding semiconductor devices within the cavity of a printed circuit board (or base).

Ex-1007, ¶¶0011-12; Ex-1009, 2:53-54. In addition, both describe using metallization connected to ground to act as a shield. Ex-1007, ¶0022; Ex-1009, 2:63-3:3. Although both provide shielding metallization above and below semiconductor devices, Dudderar further describes extending that metallization to the inside walls of the cavity housing the semiconductor devices. Ex-1009, 4:45-50.

164. A POSITA would have been motivated to apply this additional teaching of Dudderar to Imoto by using metalation on the sidewalls of the cavity as a shield. Imoto recognized the benefits of using grounded metallization as a shield, and based on Dudderar, a POSITA would have recognized that grounded metallization on the sidewalls of Imoto would have enhanced those benefits. This would produce more reliable chips, less likely to malfunction due to magnetic interference. Thus, design incentives and market forces would have motivated a POSITA to apply the teachings of Dudderar to Imoto.

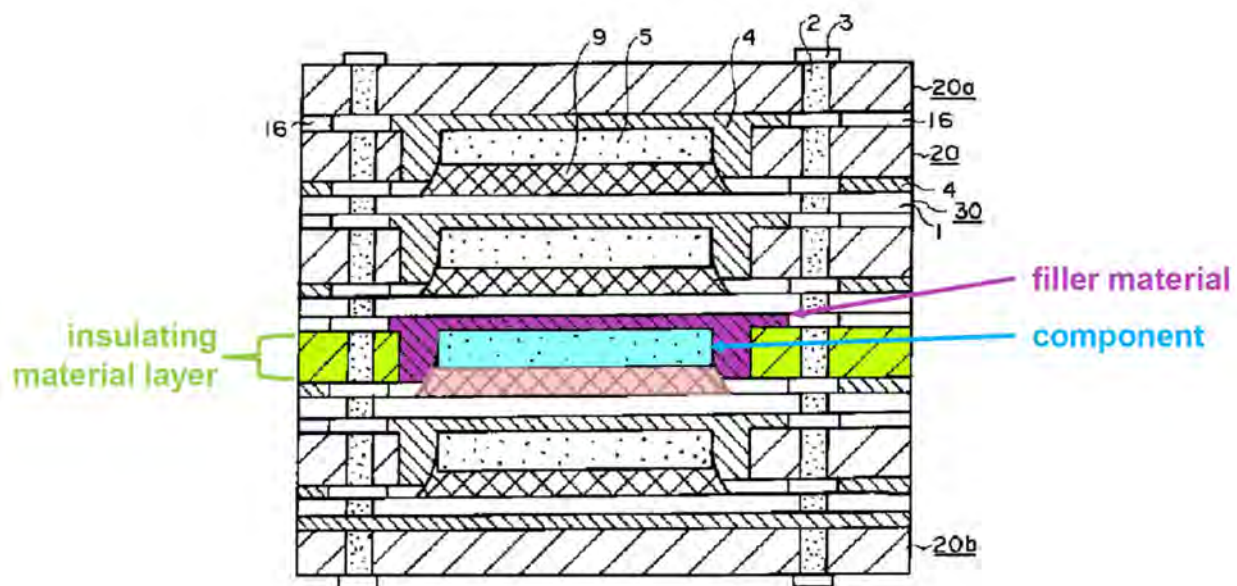
165. A POSITA would also have had a reasonable expectation of success in combining Imoto and Dudderar. A POSITA would have understood that these references disclose interrelated teachings based on routine technologies that would have been amendable to various well-understood and predictable combinations, as explained in further detail below.

2. **Dependent Claim 4: The circuit board of claim 1, wherein the component is located in a hole in the insulating material layer, and the circuit board comprises metal foil covering the sidewalls of the hole and a filler material in the hole between the metal foil and the component.**

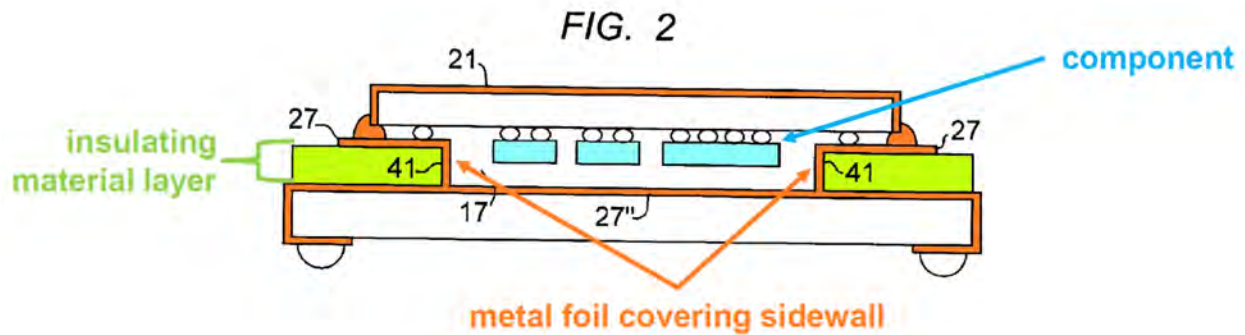
166. Imoto-Dudderar in combination teach Claim 4.

167. Imoto disclose that the component is located in a hole in the insulating material layer and that the hole includes filler material, as shown below. As described above for Element 1[d] (Section VII.A.1.e), Imoto's semiconductor element 25 is located in a hole in the insulating material layer. Imoto further describes that "adhesive material 4 fills the chip cavity section 12," as illustrated in Figure 5. Ex-1007, ¶0012; *see also* Ex-1007, ¶0013 (stating the space between the semiconductor element and the chip cavity section is "filled with a flexible adhesive material such as an elastomer").

FIG. 5



168. Dudderar discloses metal foil covering sidewalls 41 of chip cavity 17, as shown below. Ex-1009, 4:45-50.

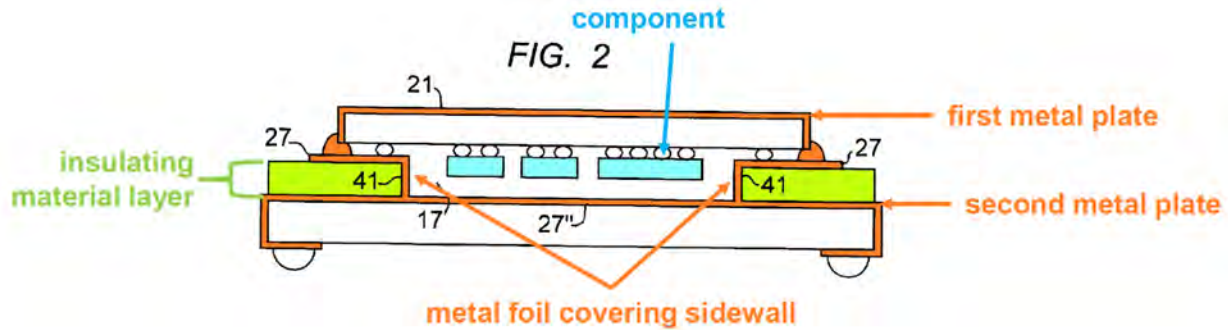


169. It would have been obvious to a POSITA to apply this teaching to the sidewalls of the chip cavity in Imoto. Imoto recognized the benefit of using metallization to shield the semiconductor element, and thus a POSITA would have been motivated to implement grounded metallization on the sidewalls of Imoto to enhance those shielding benefits, as taught in Dudderar.

3. Dependent Claim 5: The circuit board of claim 4, wherein the metal foil is electrically connected to at least one of the first and second metal plates.

170. Imoto-Dudderar in combination teaches Claim 5.

171. As described above for Claim 4 (Section VII.B.2), it would have been obvious to include metal foil on the sidewalls of Imoto as taught in Dudderar. Dudderar also teaches that the metal foil on the sidewalls is connected to the first and second metal plates and to ground, as shown below. Ex-1009, 3:28-37, 4:45-50.



172. Because Imoto also teaches that the metal plates (metal film 33) are connected together and connected to ground (*see supra* Section VII.A.2; Ex-1007, ¶10022), a POSITA would have been similarly motivated to electrically connect metal foil on the sidewalls of Imoto to the first and second metal plates and to ground.

4. Dependent Claim 6: The circuit board of claim 4, wherein the metal foil is electronically connected to an earth connection of the circuit board.

173. Imoto-Dudderar in combination renders obvious Claim 6.

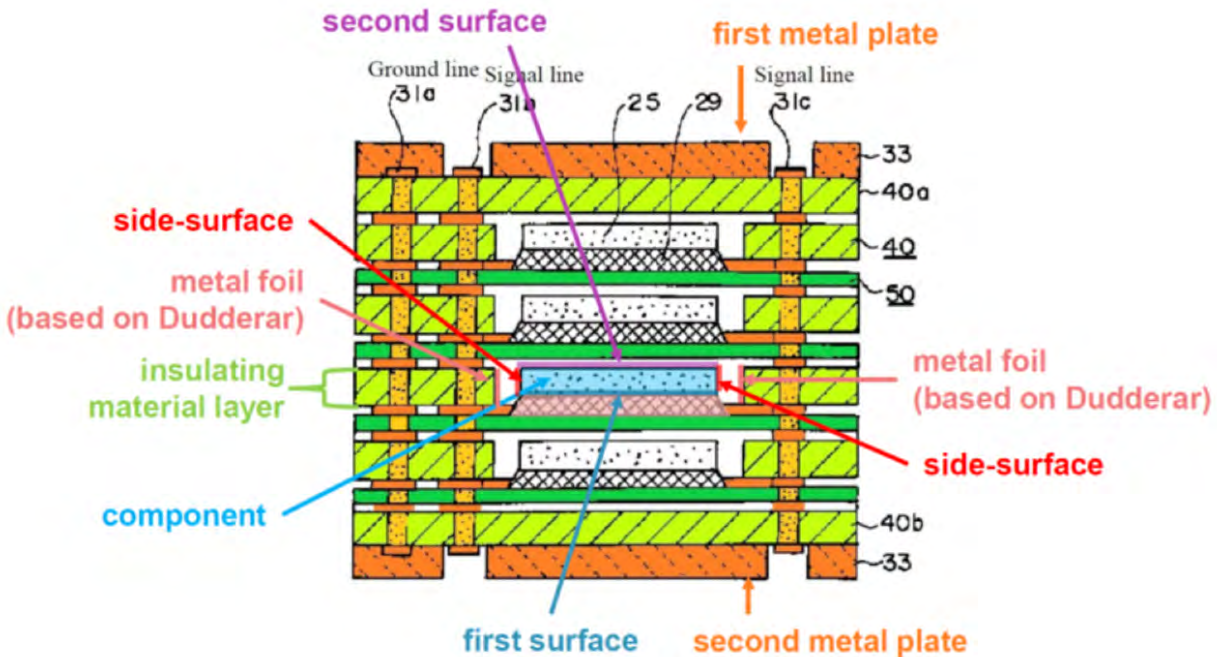
174. As explained above for Claim 5 (Section VII.B.3), Imoto and Dudderar teach connecting metallization to ground to act as a shield, and thus it would have been obvious to electronically connect metal foil on the sidewalls of Imoto to an earth connection of the circuit board.

175. As explained above for Claim 3 (Section VII.A.3), a POSITA would have understood ground to be the claimed “earth connection.”

5. **Dependent Claim 7: The circuit board of claim 4, wherein the component has a second surface opposite to the first surface and side-surfaces between the first and second surfaces, and wherein the first and second metal plates and the metal foil form an electromagnetic interference shield around the component such that the side-surfaces of the component face towards the metal foil, the first surface of the component face towards the second metal plate, and the second surface of the component face towards the first metal plate.**

176. Imoto-Dudderar in combination renders obvious Claim 7.

177. As explained above for Claim 4 (Section VII.B.2), it would have been obvious to include metal foil that forms an electromagnetic interference shield on the sidewalls of Imoto as taught in Dudderar. As shown below, the side surfaces (red) of the component face the metal foil (pink) on the sidewalls of the cavity, the first surface (dark blue bottom) of the component faces the second metal plate, and the second surface (purple top) of the component faces the first metal place.



- 6. Dependent Claim 10: The circuit board of claim 8, wherein the component is located in a hole in the baseboard; and the circuit board comprises conductive material on the sidewalls of the hole and a filler material in the hole between the metal foil and the component, wherein the metal foil creates an interference protection structure around the component.**

178. Claim 10 combines the elements of Claims 4 and 8.

179. As described above for Claim 4 (Section VII.B.2) and Claim 8 (Section VII.A.4), Imoto-Dudderar in combination renders obvious Claim 10. As taught in Dudderar, the metallization “surrounds” the component to provide electromagnetic interference (EMI) protection. Ex-1009, 3:48-51, 4:45-50.

7. **Dependent Claim 27: The multi-layered circuit board of claim 15, wherein the component is located in a hole in the insulating material layer, and the circuit board comprises metal foil covering the sidewalls of the hole and a filler material in the hole between the metal foil and the component.**

180. Claim 27 is the same as Claim 4 but depends from Claim 15.

181. As described for Claim 4 (Section VII.B.2) and Claim 15 (Section VII.A.8), Imoto-Dudderar in combination renders obvious Claim 27.

8. **Dependent Claim 28: The multi-layered circuit board of claim 15, wherein the metal foil is electronically connected to at least one of the first and second metal plates.**

182. Claim 28 is the same as Claim 5 but depends from Claim 15.

183. As described above for Claim 5 (Section VII.B.3) and Claim 15 (Section VII.A.8), Imoto-Dudderar in combination renders obvious Claim 28.

9. **Independent Claim 32**

- a. **Element 32[preamble]: An electronic module comprising**

184. Imoto's Figure 8 shows a multilayer substrate including semiconductor elements and thus teaches the preamble of Claim 1, to the extent it is limiting. Ex-1007, ¶¶00021-22.

- b. **Element 32[a]: an insulating material layer having a first side and a second side**

185. Element 32[a] is the same as Element 1[a], and thus Imoto discloses this element as described above for Element 1[a] (Section VII.A.1.b).

- c. **Element 32[b]: at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate**

186. Element 32[b] is the same as Element 1[b], and thus Imoto discloses this element as described above for Element 1[b] (Section VII.A.1.c).

- d. **Element 32[c]: at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate**

187. Element 32[c] is the same as Element 1[c], and thus Imoto discloses this element as described above for Element 1[c] (Section VII.A.1.d).

- e. **Elements 32[d], [e], [f], and [g]: a hole having sidewalls defined in the insulating material layer and located between the first and second metal plates, a metal foil covering the sidewalls of the hole, a microcircuit inside the hole and having a first surface facing towards the second metal plate, and contact areas on the first surface, a filler material in the hole between the metal foil and the microcircuit**

188. Elements 32[d], [e], [f], and [g] are the same as Elements 1[d], Element 1[e], Claims 4, and Claim 13, and thus, Imoto-Dudderar in combination renders obvious these elements as described for Element 1[d] (§VII.A.1.e), Element 1[e] (§VII.A.1.f), Claim 4 (§VII.B.2) and Claim 13 (VII.A.6).

- f. Element 32[h]: a hardened insulating polymer layer between the first surface of the microcircuit and at least one conductive pattern of said at least one second conductive pattern layer**

189. Element 32[h] is the same as Element 1[e], and thus Imoto discloses this element as described above for Element 1[e] (Section VII.A.1.f).

- g. Element 32[i]: contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the microcircuit and the at least one second conductive pattern layer or layers.**

190. Element 32[i] is the same as Element 1[f], and thus Imoto discloses this element as described above for Element 1[f] (Section VII.A.1.g).

- 10. Dependent Claim 33: The electronic module of claim 32, wherein the first and second metal plates are electronically connected to each other.**

191. Claim 33 is the same as Claim 2, but depends from Claim 32.

192. As described above for Claim 2 (Section VII.A.2) and Claim 32 (Section VII.B.9), Imoto-Dudderar in combination renders obvious Claim 33.

- 11. Dependent Claim 34: The electronic module of claim 32, wherein the first and second metal plates are electrically connected to an earth connection of the electronic module.**

193. Claim 34 is the same as Claim 3, but depends from Claim 32.

194. As described above for Claim 3 (Section VII.A.3) and Claim 32 (Section VII.B.9), Imoto-Dudderar in combination renders obvious Claim 33.

195. As explained above for Claim 3 (Section VII.A.3), a POSITA would have understood ground to be the claimed “earth connection.”

12. Dependent Claim 35: The electronic module of claim 32, wherein the metal foil is electronically connected to at least one of the first and second metal plates.

196. Claim 35 is the same as Claim 5, but depends from Claim 32.

197. As described above for Claim 5 (Section VII.B.3) and Claim 32 (Section VII.B.9), Imoto-Dudderar in combination renders obvious Claim 33.

13. Dependent Claim 36: The electronic module of claim 32, wherein the metal foil and the first and second metal plates are electronically connected to an earth connection of the electronic module.

198. Claim 36 is the same as Claims 3 and 6, but depends from Claim 32.

199. For the reasons described above with reference to Claim 3 (Section VII.A.3), Claim 6 (Section VII.B.4), and Claim 32 (Section VII.B.9), Imoto-Dudderar in combination renders obvious Claim 36.

C. Ground 3: Claims 9 and 31 are obvious over Imoto in view of Mowatt

1. A POSITA would be motivated to combine Imoto and Mowatt’s teachings and would have a reasonable expectation of success.

200. In addition to the reasons set out below with respect to specific claim elements, a POSITA would have been motivated to combine the teachings of Imoto and Mowatt and would have had a reasonable expectation of success in doing so,

because each relates to the same well-known technologies. Both relate to embedding semiconductor devices within the cavity of a laminated plate/printed wiring board. Ex-1007, ¶¶0011-12; Ex-1010, 9:40-43. A POSITA would have understood that these references disclose interrelated teachings based on routine technologies and would have been amendable to various well-understood and predictable combinations.

2. Dependent Claims 9: The circuit board of claim 8, wherein the baseboard is a glass-fibre reinforced epoxy board.

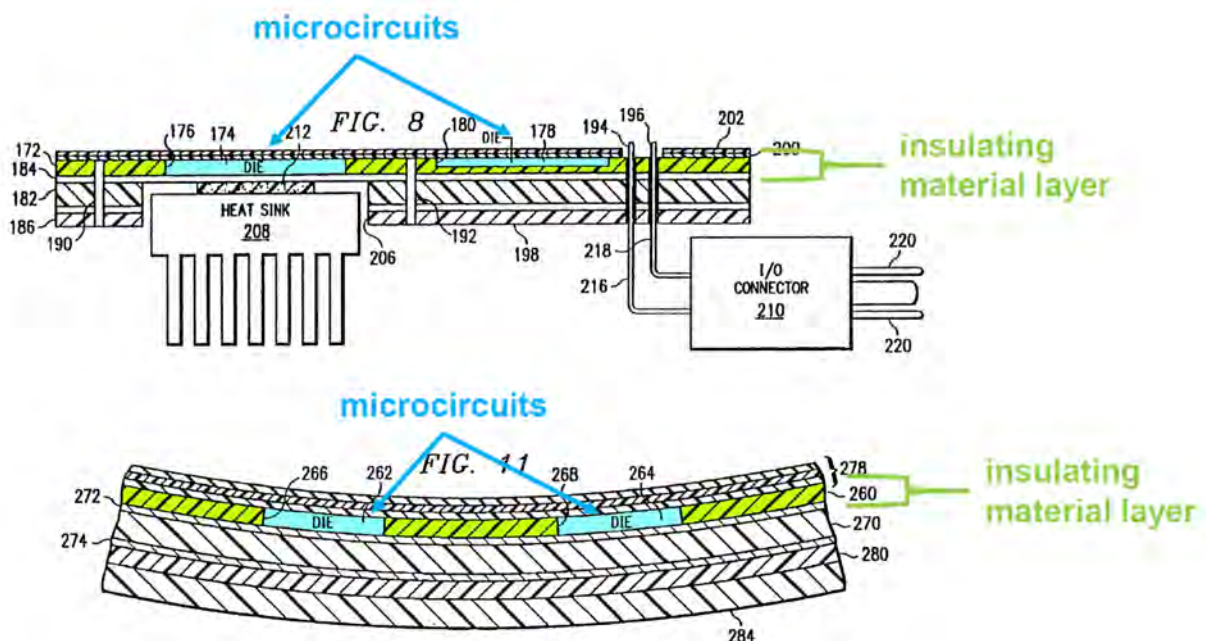
201. Imoto-Mowatt in combination renders obvious Claim 9.

202. As described above for Claim 8 (Section I.A.4), the insulating material layer in Imoto includes baseboard (plate 40), such as a “polyimide substrate.” Ex-1007, ¶¶0011, 0015. Like Imoto, Mowatt describes embedding semiconductor devices within the cavity of a laminated plate/printed wiring board. Ex-1010, 9:40-43. Mowatt teaches that the laminated plate could include “an *epoxy glass material*, or polyimide glass material, teflon or other materials commonly used in PWB fabrication.” Ex-1010, 4:40-43 (emphasis added). Based on this teaching in Mowatt, it would have been obvious to a POSITA that the baseboard in Imoto (laminated plate 40) could be a glass-fibre reinforced epoxy board. A POSITA would have been motivated to use glass-fibre reinforced epoxy boards to increase the baseboard’s rigidity and stability.

3. Dependent Claims 31: The multi-layered circuit board of claim 15, wherein the first circuit board substructure comprises at least two microcircuits inside the insulating material layer

203. As discussed above (Section VII.A.22), Imoto alone renders obvious Claim 31.

204. Alternatively, Imoto-Mowatt in combination renders obvious Claim 31. Mowatt discloses two microcircuits inside the same insulating material layer. Mowatt's Figure 8 below discloses "a primary laminate layer 172 having a first die 174 disposed in a first cavity 176 and, a second die 178 disposed in a second cavity 180." Mowatt's Figure 11 discloses "a primary laminate layer 260 for containing two die 262 and 264 within openings [266 and] 268, respectively." Ex-1010, 9:40-43, 11:58-59.



205. Mowatt refers to the dies variously as semiconductor dies, chip dies, and integrated circuit chips. Ex-1010, Abstract, 1:8, 2:64, 4:55, 6:34, 12:9-15, 12:59. For the reasons explained above for Claim 13 (Section VII.A.6), a POSITA would have understood that the dies in Mowatt are microcircuits.

206. In view of Figure 8 and 11 of Mowatt and the additional teachings of Imoto (Section VII.A.21), it would have been obvious to a POSITA that at least two microcircuits can be embedded in an insulating material layer (laminated plate 40) in Imoto. A POSITA would have been motivated to add a microcircuit to increase functionality, to reduce manufacturing costs, and to save space.

D. Ground 4: Claims 11 and 29 are obvious over Imoto in view of Lau

1. A POSITA would be motivated to combine Imoto and Lau's teachings and would have a reasonable expectation of success.

207. In addition to the reasons set out below with respect to specific claim elements, a POSITA would have been motivated to combine the teachings of Imoto and Lau and would have had a reasonable expectation of success in doing so, because each relates to the same well-known technologies. Imoto discloses that semiconductor element 5 is “die bonded and mounted on the wiring substrate 30 using flip chip method or the like.” Ex-1007, ¶0016. It describes the use of “solder balls and the like.” *Id.* Lau describes specific implementation details for flip-chip

and die bonding technologies, including the use of solder balls and underfill resins. Ex-1011, 44, 47-48, 159-61, 186-87. A POSITA would have understood that these references disclose interrelated teachings based on routine technologies and would have been amendable to various well-understood and predictable combinations, as explained in further detail below.

2. Dependent Claim 11: The circuit board of claim 1, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.

208. As discussed above (Section VII.A.5), Imoto alone renders obvious Claim 11.

209. Alternatively, Imoto-Lau in combination also renders obvious Claim 11. As described above for Element 1[f] (Section VII.A.1.g), the conductors in the contact openings in Imoto are connection terminals 11, which are surrounded by underfill resin 9/29.

210. Imoto discloses that semiconductor element 5/25 is “die bonded and mounted on the wiring substrate 30 using flip chip method or the like” and that “connection terminals 11 such as solder balls or the like are connected to the wiring pattern 9.” Ex-1007, ¶0016. A POSITA would have been motivated to implement solder balls using under-bump metallurgy (UBM) on aluminum pads (contact areas) of semiconductor elements 5/25, as taught in Lau. Ex-1011, 43-44. UBM is

necessary to define the area of the chip that is wetted by solder and to form an effective physical, metallurgical, and electrical connection between the solder and the chip. *Id.*, 43-44. As shown in Table 2.4 of Lau (Ex-1011, 44), UBM for solder typically involves copper, which can be applied by electroplating. Lau describes the use of electroplating to apply Ti-Cu or TiW-Cu and 6-25 μm of Cu (copper), as shown below. *Id.*, 47-48, 186-87.

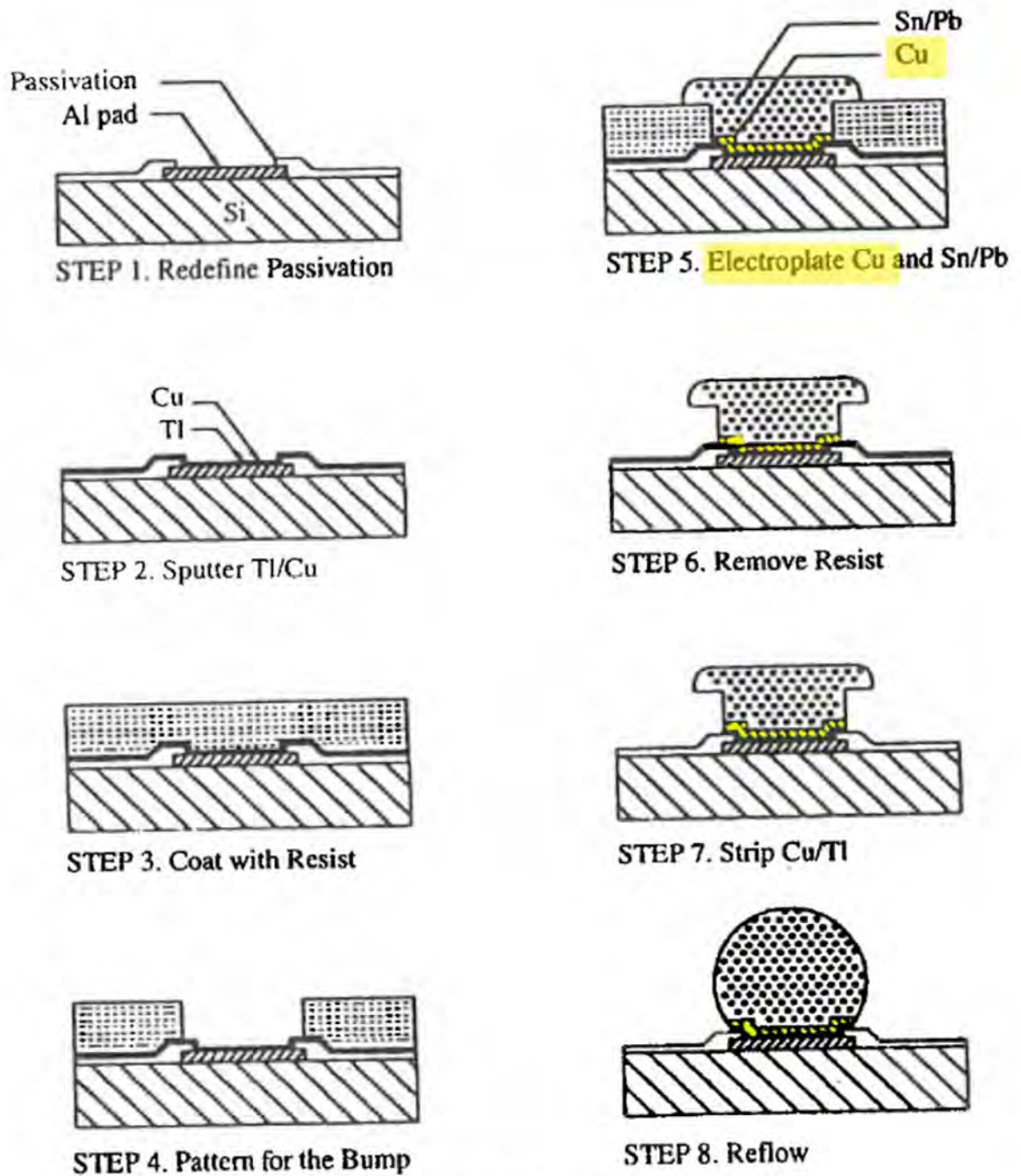


Figure 2.19 Electroplated solder wafer-bumping process.

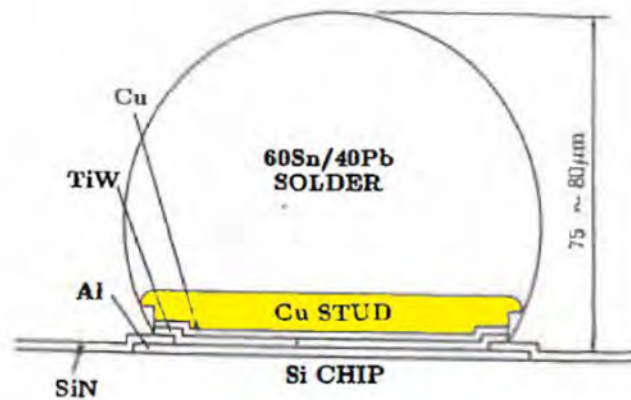


Figure 6.7 Sharp's eutectic solder bump.

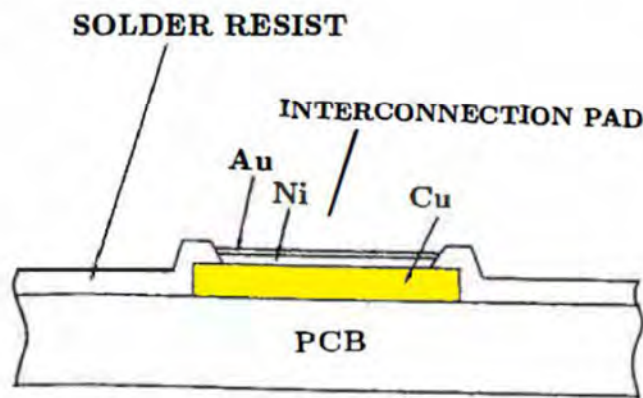


Figure 6.8 Sharp's low-cost PCB.

211. Electroplating is an electrochemical deposition process and, thus, the result is electrochemically deposited copper. In view of Lau, it would have been obvious to a POSITA that, in Imoto, the conductors in underfill resin 9/29 (hardened insulating polymer layer) include, in addition to solder, electrochemically deposited copper, as recited in Claim 11.

212. Alternatively, connection terminals 11 in Imoto could be copper bumps as opposed to solder as also taught in Lau. Imoto teaches that connection terminals 11 could be solder balls “or the like.” Ex-1007, ¶0016. Lau describes that, as an

alternative to solder, semiconductor chips are also mounted using copper bumps.

Ex-1011, 159-61.

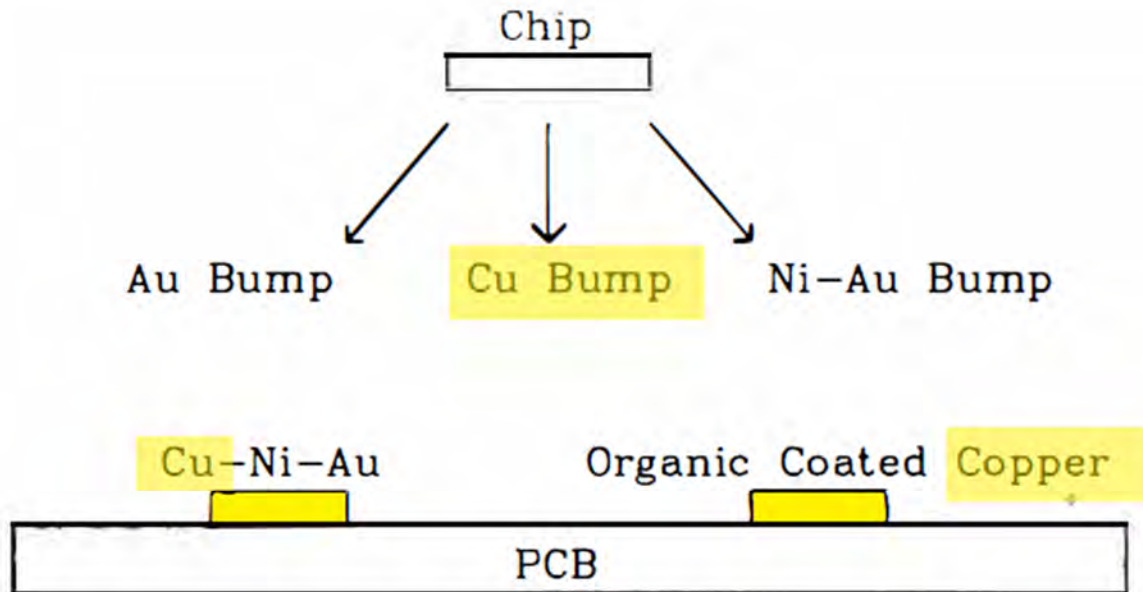


Figure 5.2 Flip chip with three different kinds of bumps on two different kinds of PCBs.

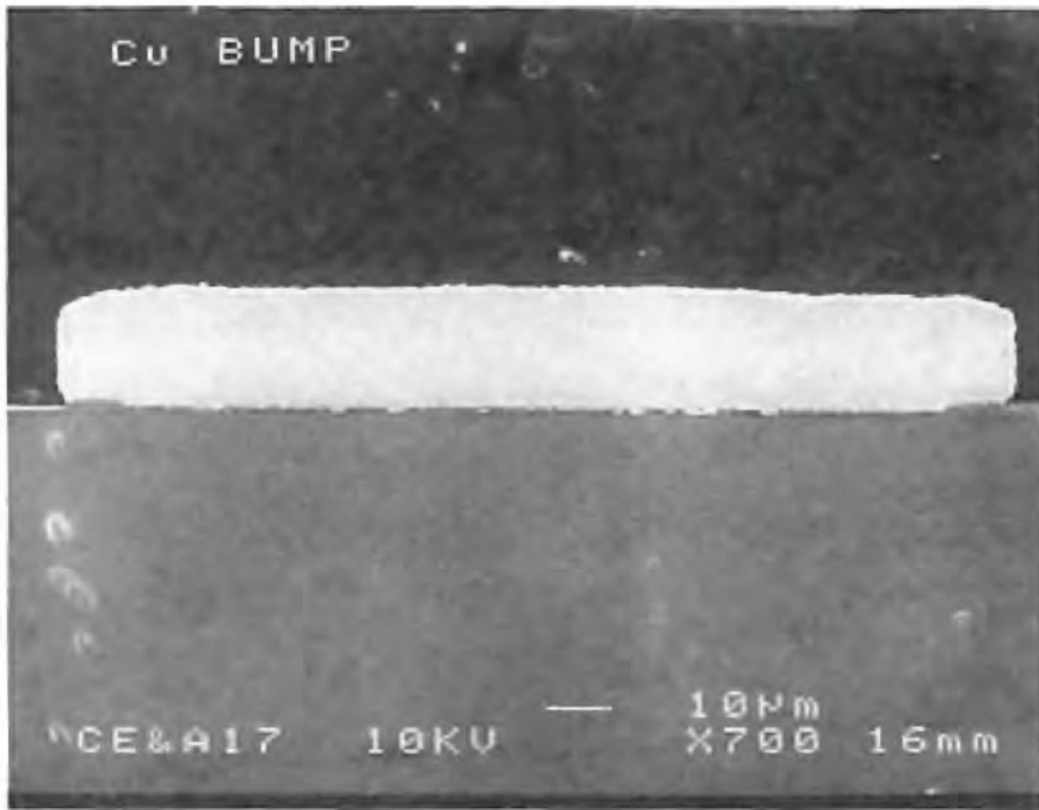


Figure 5.5 A typical Si chip with Cu bump.

213. Lau describes that the copper bumps are formed by electroplating. Ex-1011, 159 (Au bumps formed by “electroplating”), 160 (copper bump formed same way and identified as “plated Cu”). As explained in Lau, a POSITA would have been motivated to use a solderless material “for the sake of a green environment.” Ex-1011, 157. In addition, a POSITA would have understood that copper performs well because it is a highly conductive and that copper is reliable because it is widely used for interconnections in integrated circuits. Thus, in view of Lau, it would have been obvious to a POSITA that connection terminals 11 in

Imoto could be copper bumps as opposed to solder and, thus, that connection terminals 22 in underfill resin 9/29 (hardened insulating polymer layer) would include electrochemically deposited copper, as recited in Claim 11.

3. Dependent Claim 29: The multi-layered circuit board of claim 15, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.

214. Claim 29 is the same as Claim 11 but depends from Claim 15.

215. For the reasons described above for Claim 11 (Section VII.D.2) and Claim 15 (Section VII.A.8), Imoto-Lau in combination renders obvious Claim 29.

E. Ground 5: Claim 12 is obvious over Imoto in view of Lehmann

1. Dependent Claim 12: The circuit board of claim 1, wherein the hardened insulating polymer layer contains epoxy.

216. Imoto-Lehman in combination renders obvious Claim 12.

217. As described above for Element 1[e] (VII.A.1.f), the hardened insulating polymer layer in Imoto is underfill resin 9/29 between semiconductor component 5/25 and the substrate to which it attached. Like Imoto, Lehmann describes directly attaching a chip to a substrate and the use of solder balls and underfill resin. Ex-1012, 266. Lehman teaches that the underfill resin can be “epoxy resin.” *Id.* Based on this teaching in Lehmann, it would have been obvious to POSITA that to implement underfill resin 9/29 in Imoto (hardened insulating polymer layer) with an epoxy resin.

218. A POSITA would have been motivated to combine the teachings of Imoto and Lehmann and would have had a reasonable expectation of success in doing so, because each relates to the same well-known technologies. Both relate to direct attaching chips to substrates and the use of solder ball and underfill resin . Ex-1007, ¶0016; Ex-1012, 266. A POSITA would have been motivated to use epoxy resin to “protect[] both the chip and the solder joints” as taught in Lehman. Ex-1012, 266. A POSITA would also have had a reasonable expectation of success in combining Imoto and Lehmann. A POSITA would have understood that these references disclose interrelated teachings based on routine technologies and would have been amenable to various well-understood and predictable combinations.

F. Ground 6: Claims 1-3, 8, 11, 13-26, and 29-31 are rendered obvious by Kurita

1. Independent Claims 1

a. Element 1[preamble]: A circuit board comprising

219. Kurita teaches the preamble of Claim 1, to the extent it is limiting.

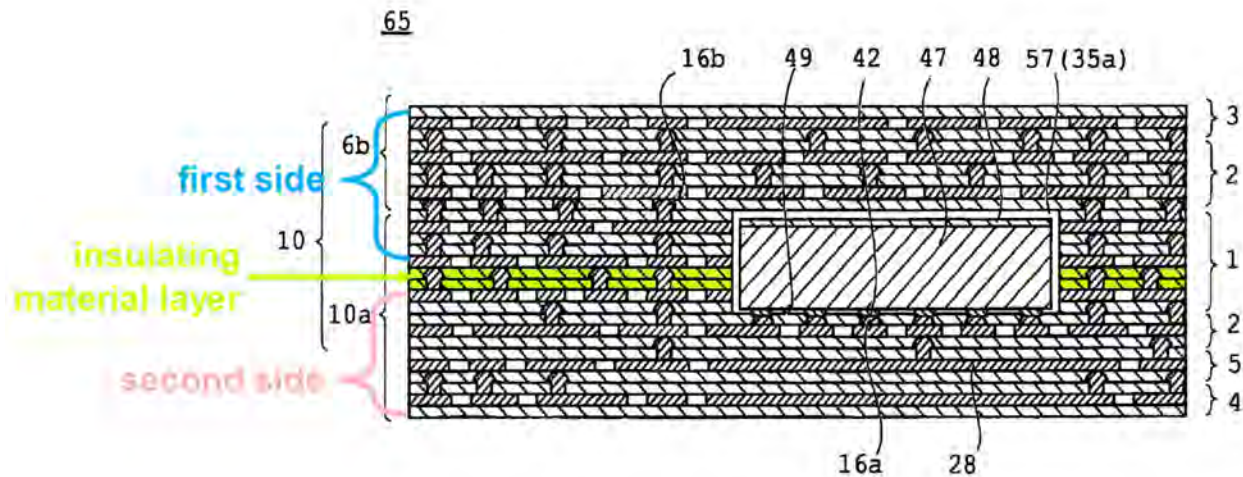
220. As indicated by its title “Multi-Layer Flexible Printed Wiring Board,” Kurita teaches a circuit board. Ex-0013, 1:6-8, 5:57-58. The circuit board in Kurita is multilayer substrate 65 in Figure 7. Ex.-0013, 11:50-56.

b. Element 1[a]: an insulating material layer having a first side and a second side

221. Kurita discloses Element 1[a].

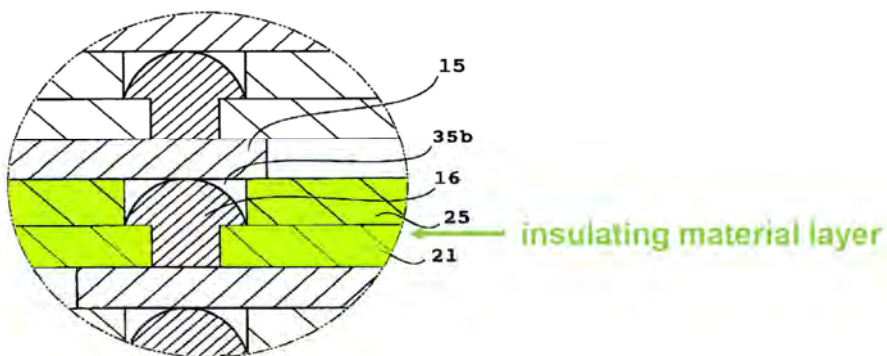
222. Kurita discloses an insulating material layer with a first and second side, as shown below.

FIG. 7



223. The insulating material layer is adhesive films 21 and resin film 25, as shown in Figure 3A.

FIG. 3A

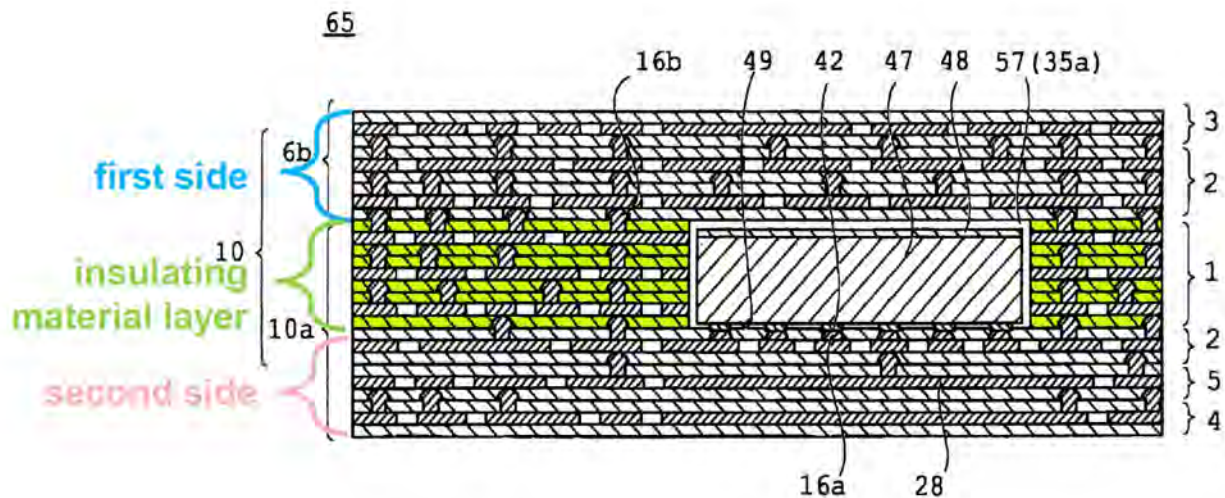


224. Adhesive layer 21 is a thermoplastic formed from heating polyimide. Ex-1013, 6:42-50, 7:62-8:6. Resin film 25 is “formed of polyimide film by

hardening of the precursor coat 23 that has been subjected to patterning.” *Id.*, 7:25-27. Thus, resin film 25 and adhesive film 21 is an insulating material layer.

225. Under an alternative mapping of the claims, the insulating material layer is the combination of resin films 25 and adhesive films 21 making up the side of housing section 57 in Figure 7, as shown below.

FIG. 7



226. Thus, the combination of resin films 25 and adhesive films 21 are an insulating material layer.¹⁰ Although the below analysis of other claim elements focuses on the prior claim mapping, the below analysis applies equally to this

¹⁰ The presence of intervening wiring films 15 is consistent with the '944 Patent, which contemplates there may be “at least one conductive pattern layer in the insulating material layer.” Ex 1001, 11:13-14 (emphasis added).

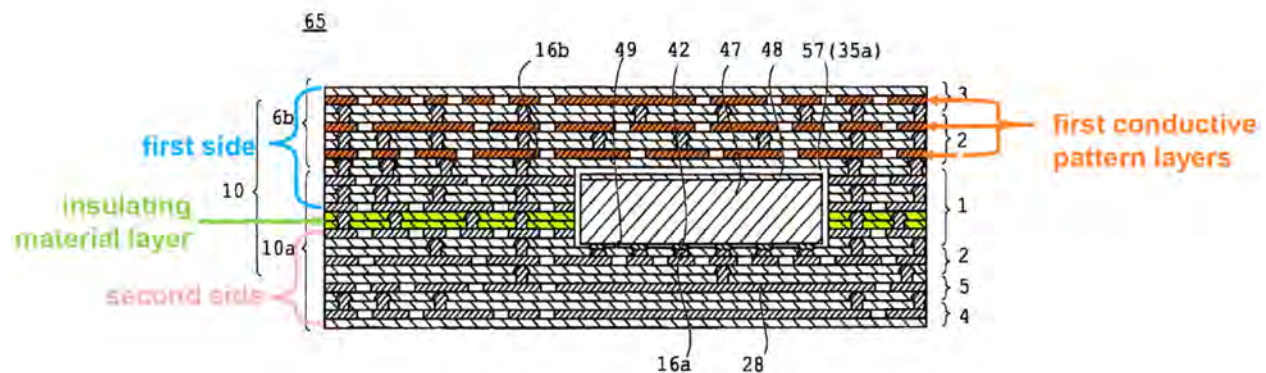
alternative mapping involving the combination of resin films 25 and adhesive films 21.

- c. Element 1[b]: at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate**

227. Kurita discloses Element 1[b].

228. As shown below, the first conductive pattern layers in Figure 7 are the layers of wiring film 15 (shaded orange) above resin film 25 (shaded green).

FIG. 7



229. The first conductive pattern layers identified above correspond to wiring films 15 in Figures 1-3. Kurita states wiring film 15 is made by “patterning” metallic foil 11, as shown in Figure 1J and 1K. Ex-1013, 6:51-64.

FIG. 1J

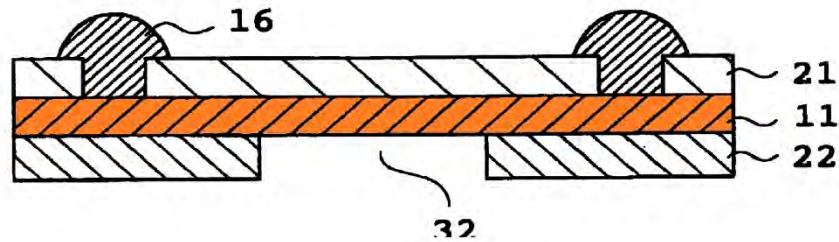
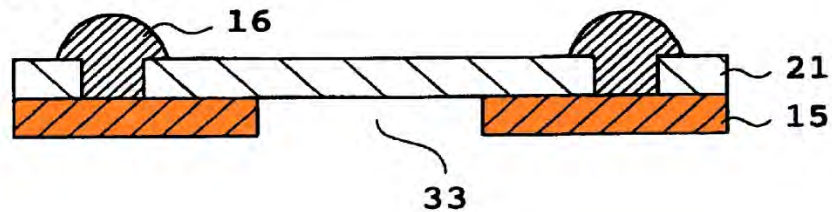
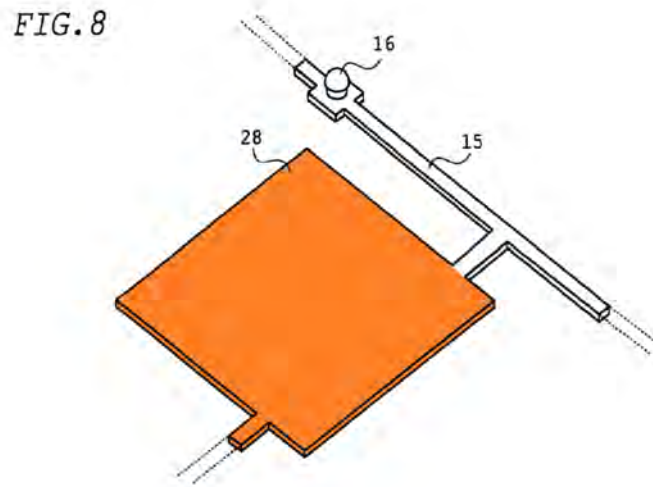


FIG. 1K



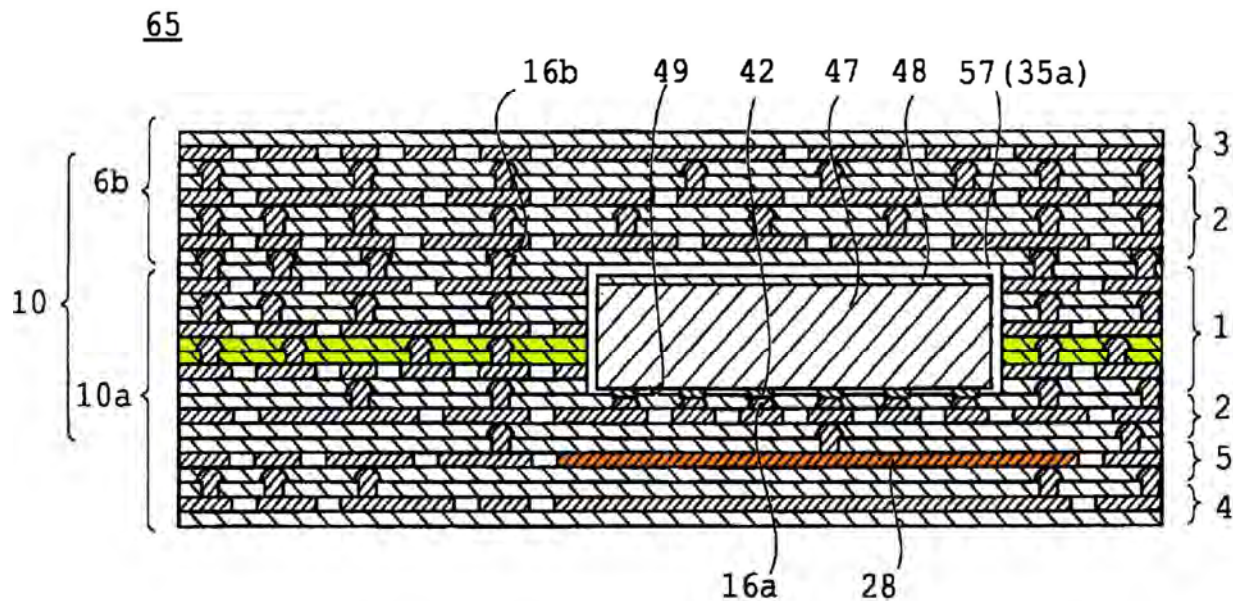
230. Kurita also discloses that wiring film 15 can be patterned to form shield section 28, which provides a larger surface area that may be connected to ground to shield semiconductor device 47 from electromagnetic noise. Ex-1013, 4:1-9, 5:24-30, 6:62-64, 11:56-63, 12:8-15, 12:40-46.

231. Figure 8 illustrates an example of shield section 28.

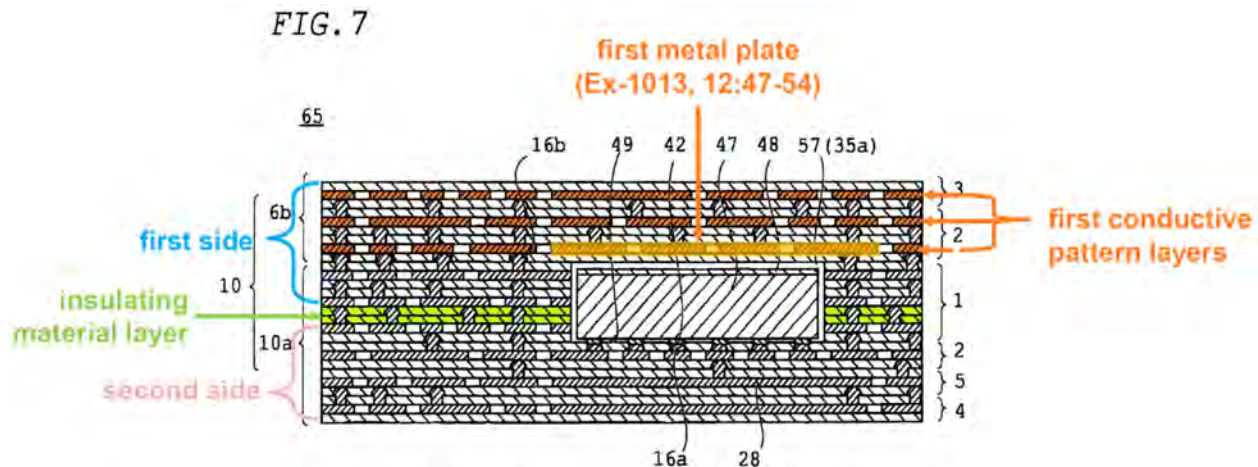


232. Figure 7 illustrates shield section 28 below semiconductor device 47, as shown below

FIG. 7



233. Kurita also explains that “it is more effective to arrange the shield sections 28 on both side [sic] of the semiconductor device 47.” Ex-1013, 12:47-54. When placed above semiconductor device 47 as taught in Kurita, shield section 28 corresponds to the claimed first metal plate. As shown below, this Declaration uses orange shading above semiconductor device 47 to identify where a first metal plate is located based on the above disclosure of Kurita.

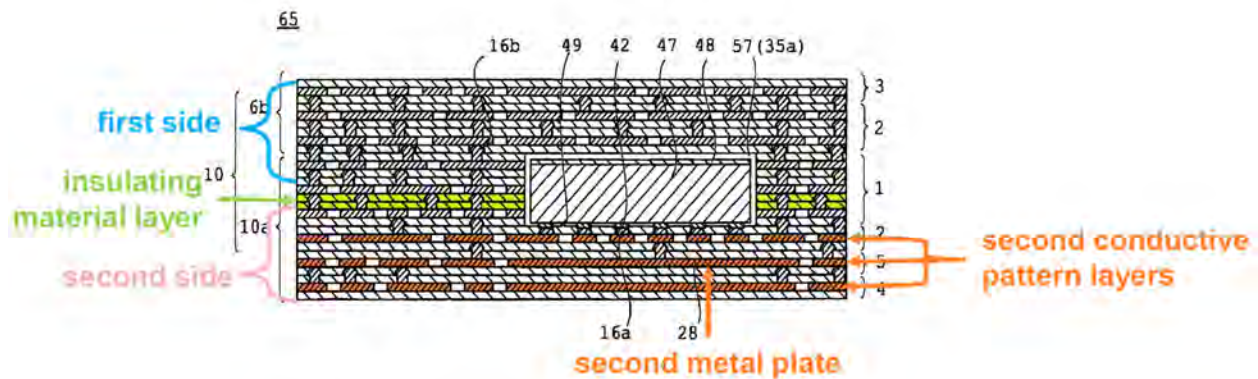


- d. **Element 1[c]: at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate**

234. Kurita discloses Element 1[c].

235. As shown below, the second conductive pattern layers in Figure 8 are the same features discussed above for first conductive pattern layers (wiring films 15) but below the insulating material layer as opposed to above it. See *supra* Section VII.F1.c. Shield section 28 corresponds to the claimed second metal plate. See *supra* Section VII.F1.c.

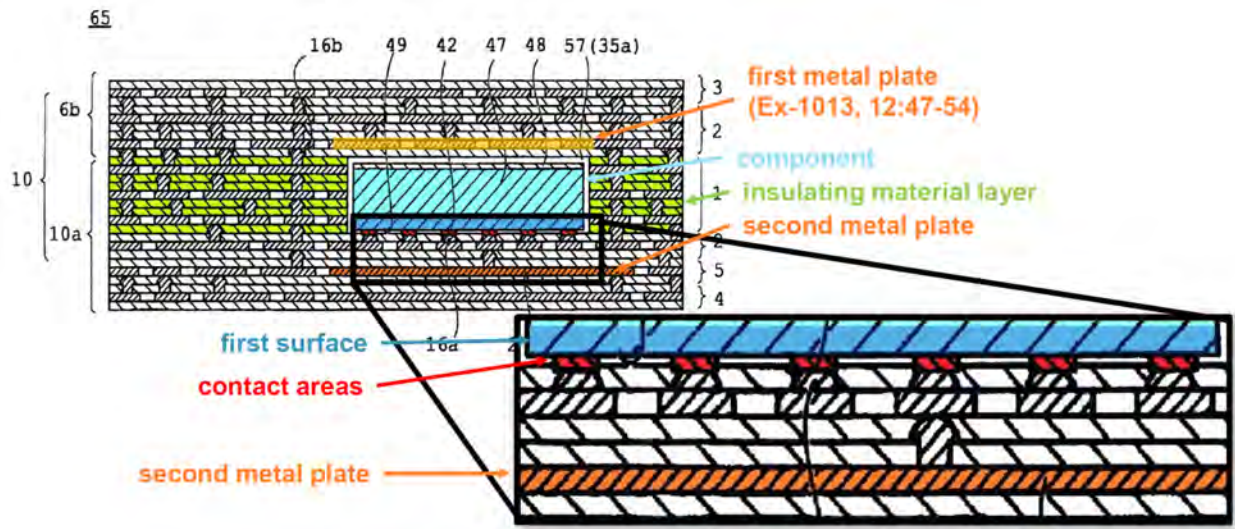
FIG. 7



- e. **Element 1[d]: a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface**

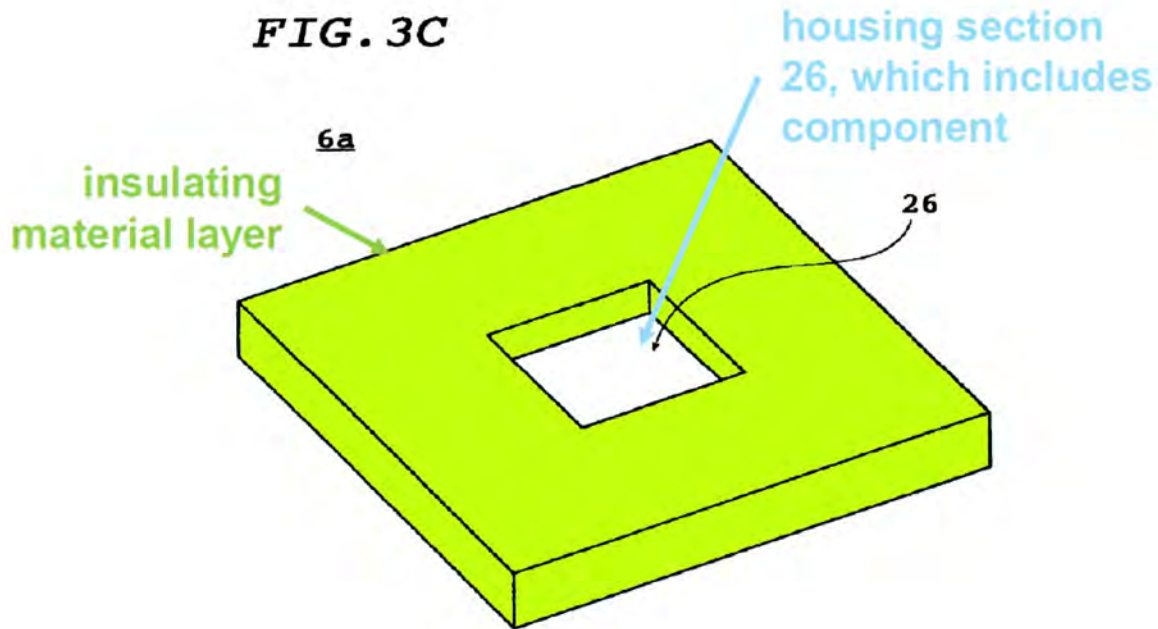
236. Kurita discloses Element 1[d].

237. As shown below in Figure 7, the component is semiconductor device 47 (light blue), which is inside insulating material layer (light green) and between first and second metal plates (orange).



238. As shown above, the first surface (dark blue) of semiconductor device 47 faces the second metal plate and includes contact areas (red). The contact areas are bonding pads 42, which face the bottom of housing 57. Ex-1013, 9:18-25.

239. The insulating material layer forms a housing section 26 as shown in Figure 3C and, thus, semiconductor device 47 (which resides in housing section 26) is located “inside the insulating material layer” as required by Element 1[d]. Ex-1013, 9:6-11, 12:16-17.

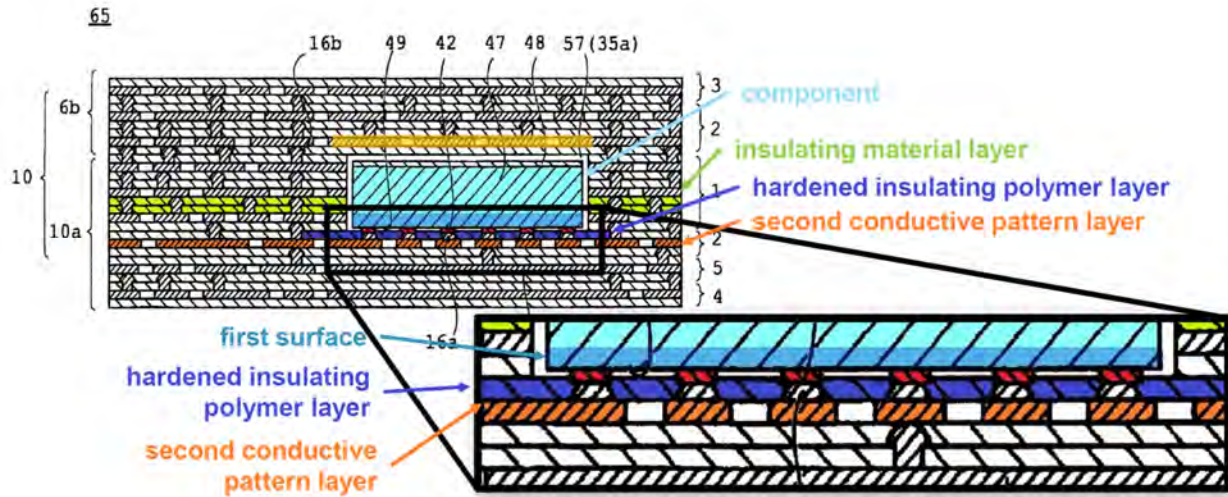


- f. **Element 1[e]: a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and**

240. Kurita discloses Element 1[e].

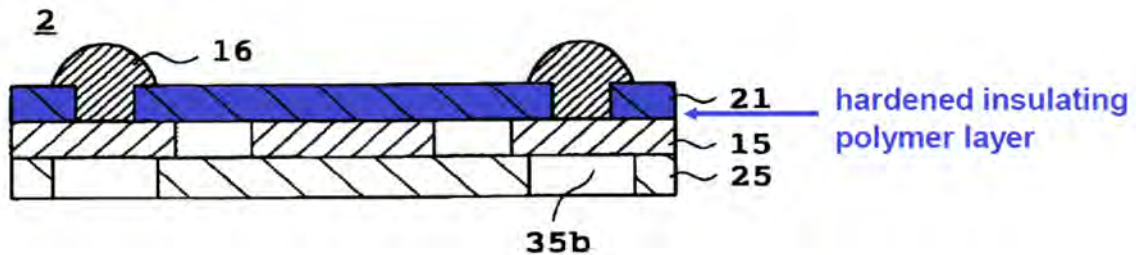
241. The hardened insulating polymer film is adhesive film 21 at the bottom of housing section 57. Ex-1013, 9:29-36, 12:16-30. As shown below, the hardened insulating polymer layer (blue) is located between the first surface of the component (semiconductor device 47) and at least one second conductive pattern layer (wiring film 15). *Id.*, 12:24-28.

FIG. 7



242. The above-identified hardened insulating polymer layer in Figure 7 corresponds to adhesive layer 21 in Figure 2A, which is a thermoplastic formed from heating polyimide resin to become adhesive. Ex-1013, 6:42-50, 7:62-8:6. Thus, adhesive layer 21 is a hardened insulating polymer film.

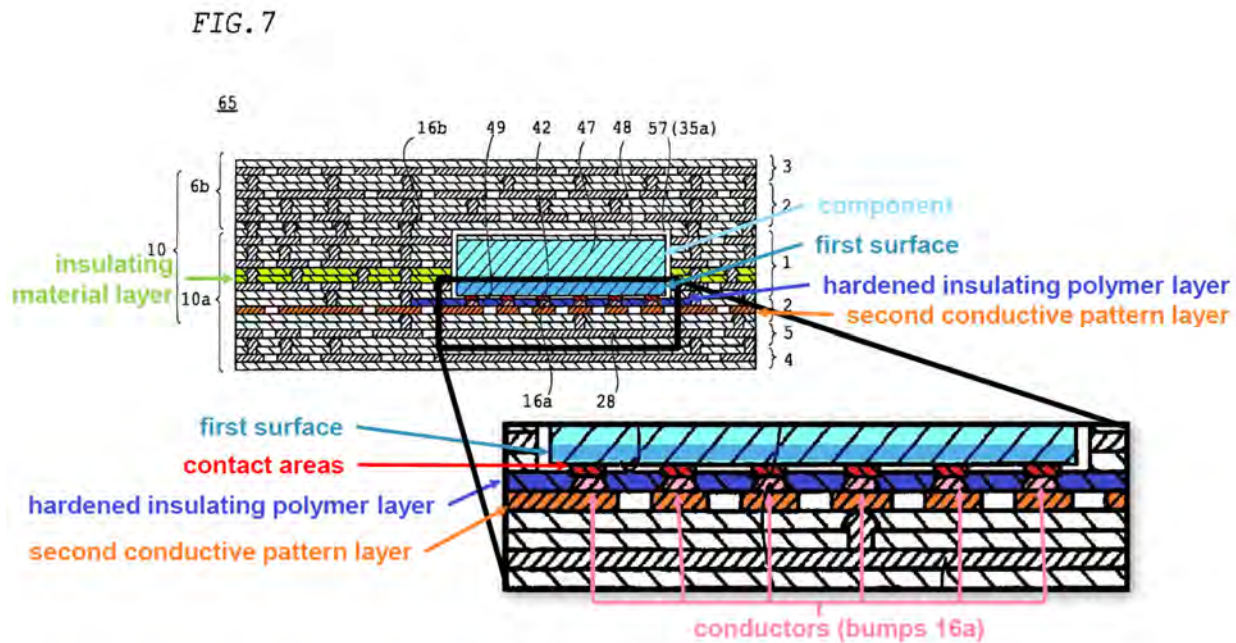
FIG. 2A



- g. **Element 1[f]: contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one second conductive pattern layer or layers**

243. Kurita discloses Element 1[f].

244. The “conductors in the contact opening” are bumps 16a in openings of adhesive layer 21 at the bottom of housing section 57. Ex-1013, 9:21-36. Bumps 16a form electrical contact between the contact areas (bonding pads 42) and at least one second conductive pattern layer (wiring film 15). *Id.*, 12:24-28.

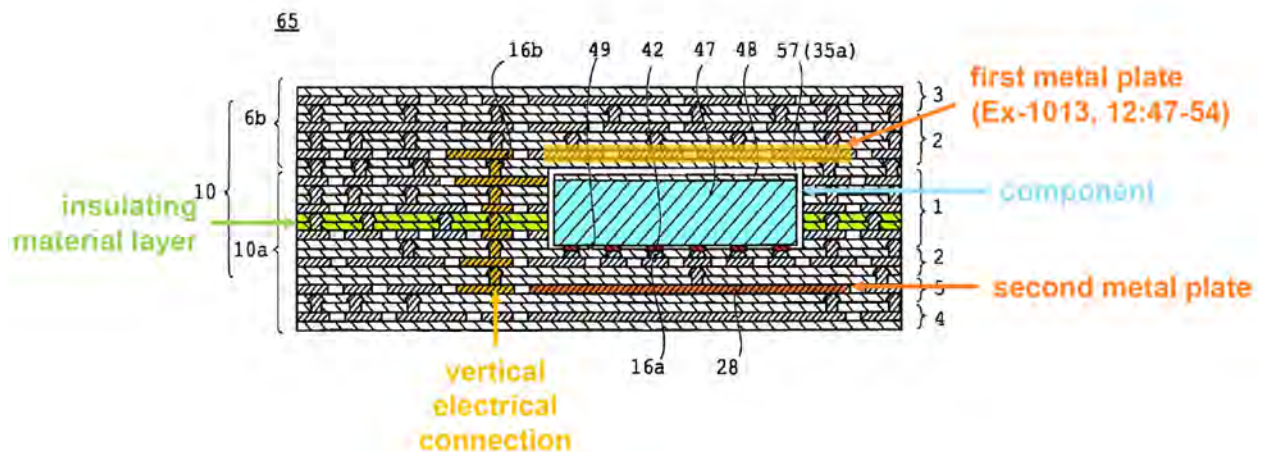


2. Dependent Claim 2: The circuit board of claim 1, wherein the first and second metal plates are electrically connected to each other.

245. Kurita renders obvious Claim 2.

246. Kurita teaches that shield sections 28 should be connected to ground to inhibit electromagnetic noise. Ex-1013, Abstract, 4:1-9, 5:24-30, 12:40-50. A POSITA would have understood that the grounded elements in Kurita's circuit board are connected to the same ground (*e.g.*, a ground plane), connecting shield sections 28 on both sides of semiconductor device 47 to the same ground and thereby connecting them to each other. A POSITA would have understood that the wiring patterns in Figure 7 could be modified to connect shield sections 28 to the vertical electrical connection identified below and thus connecting them to each other.

FIG. 7



3. Dependent Claim 3: The circuit board of claim 1, wherein the first and second metal plates are electrically connected to an earth connection of the circuit board.

247. Kurita discloses Claim 3.

248. Kurita teaches that shield sections 28 should be connected to ground to inhibit electromagnetic noise. Ex-1013, Abstract, 4:1-9, 5:24-30, 12:40-50.

249. As explained above for Claim 3 (Section VII.A.3), a POSITA would have understood ground to be the claimed “earth connection.”

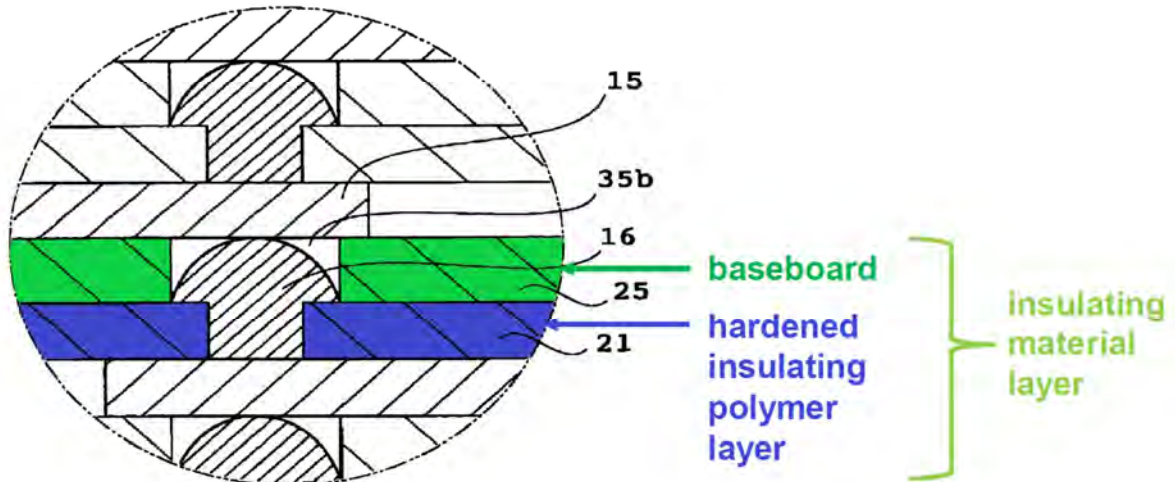
4. Dependent Claim 8: The circuit board of claim 1, wherein the insulating material layer includes a baseboard and the hardened insulating polymer layer.

250. Kurita discloses Claim 8.

251. Claim 8 redefines insulating material layer to include a baseboard and the hardened insulating polymer layer. In Kurita, the baseboard is resin film 25, and the hardened insulating polymer layer is adhesive layer 21.¹¹ These layers are stacked and adjacent to one another, as shown below in Figure 3.

¹¹ Adhesive layer 21 and resin film 25 are described above for Element 1[a] (Section VII.F.1.b).

FIG. 3A



5. **Dependent Claim 11: The circuit board of claim 1, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.**

252. Kurita discloses Claim 11.

253. As described above for Element 1[f] (Section VII.F.1.g), the “conductors in the contact opening” are bumps 16a in openings of adhesive layer 21 at the bottom of housing section 57. Kurita discloses bumps 16a are electrochemically deposited copper. Ex-1013, 6:14-24.

6. **Dependent Claim 13: The circuit board of claim 1, wherein the component is a microcircuit.**

254. Kurita discloses Claim 13.

255. As described above for Element 1[d] (Section VII.F.1.e), the claimed component is semiconductor device 47, which is a “chip-mounted semiconductor integrated circuit.” Ex-1013, 12:6-7.

256. The '944 Patent does not define microcircuit, but a POSITA would have understood a microcircuit to encompass an integrated circuit, such as a semiconductor chip (semiconductor 25). The IEEE Dictionary defines “microcircuit” by reference to “integrated circuit”:

microcircuit *See: integrated circuit.*

Ex-1015, 652.

257. The dictionary provides the following definition of “integrated circuit”:

integrated circuit (IC) (1) (solid state) A combination of interconnected circuit elements inseparably associated on or within a continuous substrate. *Note:* To further define the nature of an integrated circuit, additional modifiers may be prefixed. Examples are: 1) dielectric-isolated monolithic integrated circuit, 2) beamlead monolithic integrated circuit, 3) silicon-chip tantalum thin-film hybrid integrated circuit. *See also:* element; film integrated circuit; integrated electronics; multichip integrated circuit. (ED) [46], 274-1966w
(2) (A) A combination of connected circuit elements (such as transistors, diodes, resistors, and capacitors) inseparably associated on or within a continuous substrate. *Synonym:* chip. *See also:* program. **(B)** A solid-state circuit consisting of interconnected active and passive semiconductor devices diffused into a single silicon chip. *Synonyms:* chip; microcircuit. *See also:* monolithic integrated circuit; very-high-speed integrated circuit. (C) 610.10-1994

Ex-1015, 536-37.

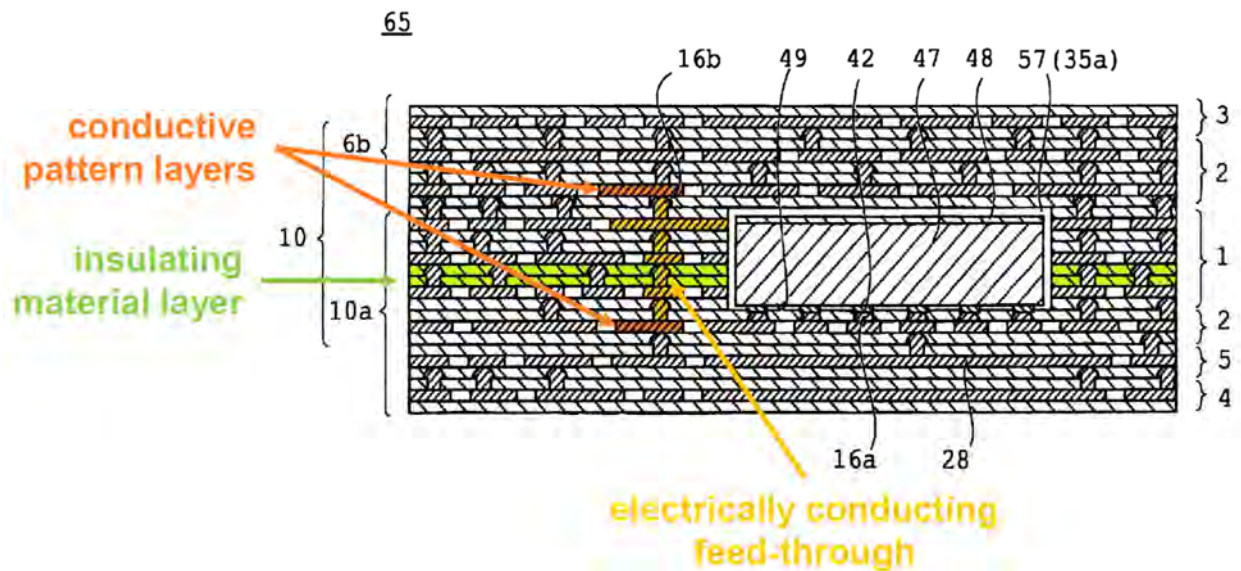
258. Thus, a POSITA would have understood that semiconductor device 47 in Kurita is a microcircuit.

7. **Dependent Claim 14: The circuit board of claim 1, comprising an electrically conducting feed-through between the conductive pattern layers on the both sides of the insulating material layer.**

259. Kurita discloses Claim 14.

260. As shown below, Figure 7 includes electrically conducting feed-throughs between the conductive pattern layers on the both sides of the insulating material layer.

FIG. 7



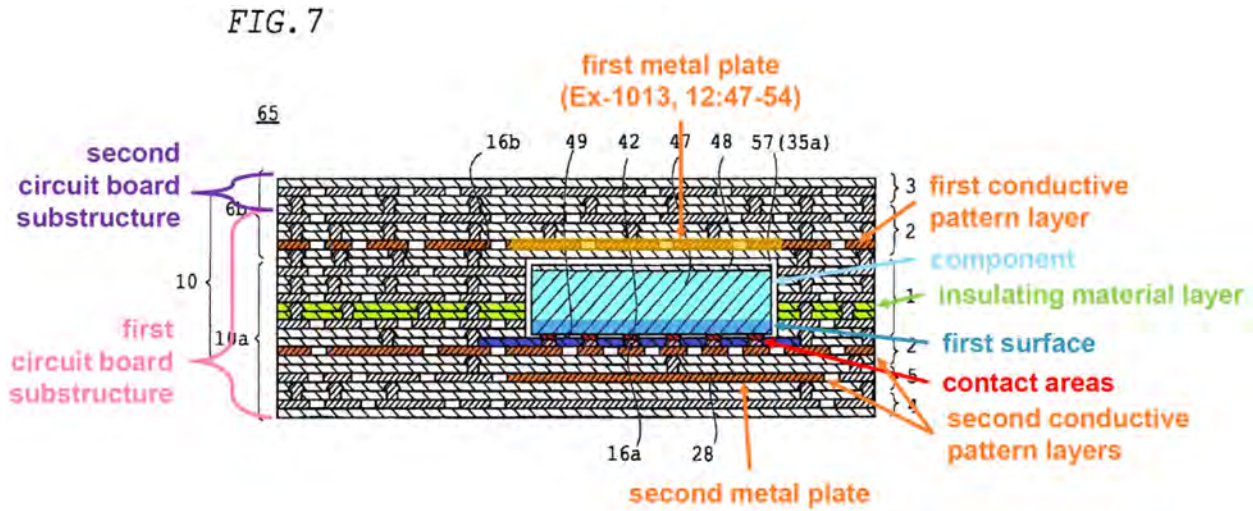
261. The electrically conducting feed-through corresponds to either bumps 16a in the insulating material layer or a combination of bumps 16a and wiring film 15 between the two conductive pattern layers.

8. Independent Claim 15

262. Kurita discloses Claim 15.

263. As explained above for Claim 15 in Ground 1 (Section VII.A.1.8), Claim 15 is the same as Claim 1, except for the preamble. Claim 15 requires “a multi-layered circuit board comprising a first circuit board substructure and second circuit board substructure on top of each other, wherein at least the first circuit board substructure comprises” the same Elements [a]-[f] as recited in Claim 1.

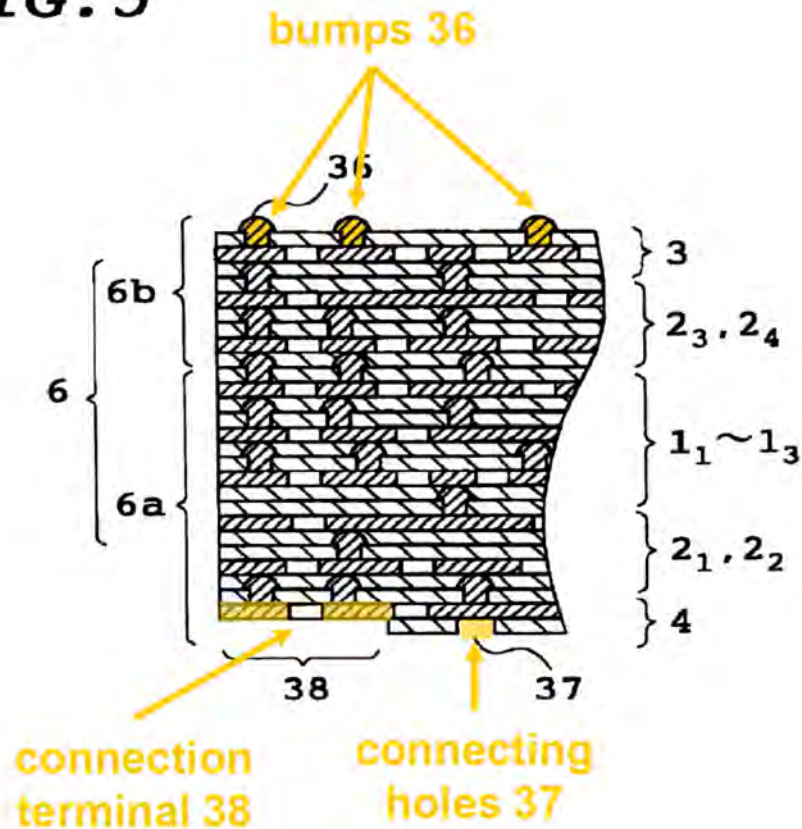
264. Even if the preamble of Claim 15 is limiting, Kurita discloses Claim 15. Because multi-layer substrate 65 of Figure 7 include multiple layers, the top layer is the second circuit board substructure, and the remaining layers are the first circuit board substructure that meets Elements 15[a]-15[f] as described for Elements 1[a]-1[f] (§VII.F.1).



265. Alternatively, the multi-layer substrate 65 of Figure 7 is the first circuit board substructure that meets Elements 15[a]-15[f] as described for Elements 1[a]-1[f] (§VII.F.1). Kurita discloses this multi-layer substrate may be connected to “other circuit substrates,” correspond to the second circuit board substructure of Claim 15. Ex-1013, 10:13-27. As shown in Figure 5, a multi-layer substrate may include bumps 36 on the top surface and connecting holes 37 or connection terminals 38 on the bottom surface to connect to these other circuit substrates.¹² *Id*, 10:13-27. A POSITA would have been motivated to add a second circuit board substructure to add functionality, reduce manufacturing cost, and save space.

¹² Kurita discloses or it would have been obvious to POSITA that this teaching for the multilayer substrate in Figure 5 also applies to the multilayer substrate of Figure 7.

FIG. 5

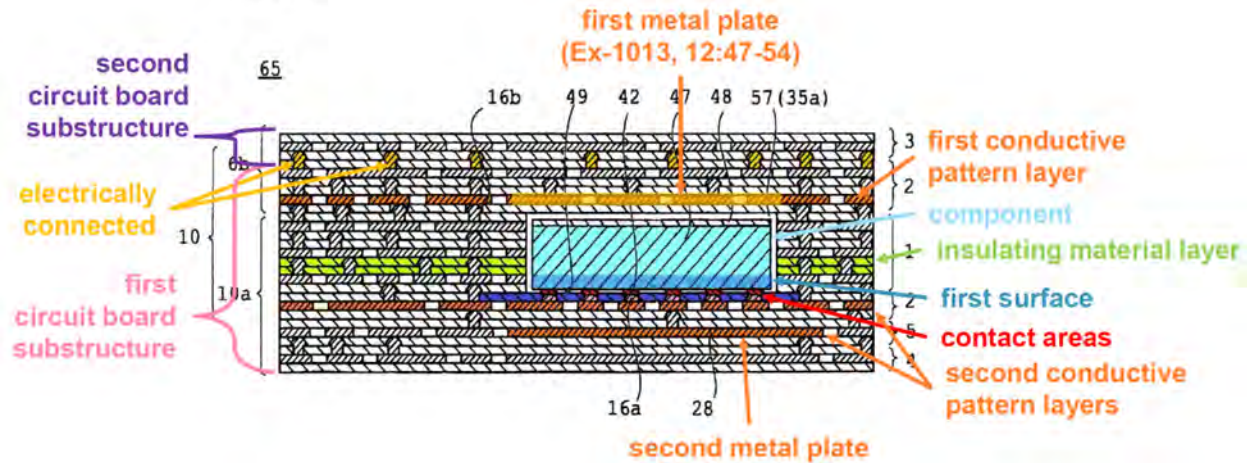


9. **Dependent Claim 16:** The multi-layered circuit board of claim 15, wherein said first circuit board substructure and said second circuit board substructure are electrically connected to each other to form a multi-layered functioning totality.

266. Kurita discloses Claim 16.

267. The first and second circuit board substructures identified for Claim 15 (§VII.F.8) are electrically connected to each other to form a multi-layered functioning totality, as shown below.

FIG. 7

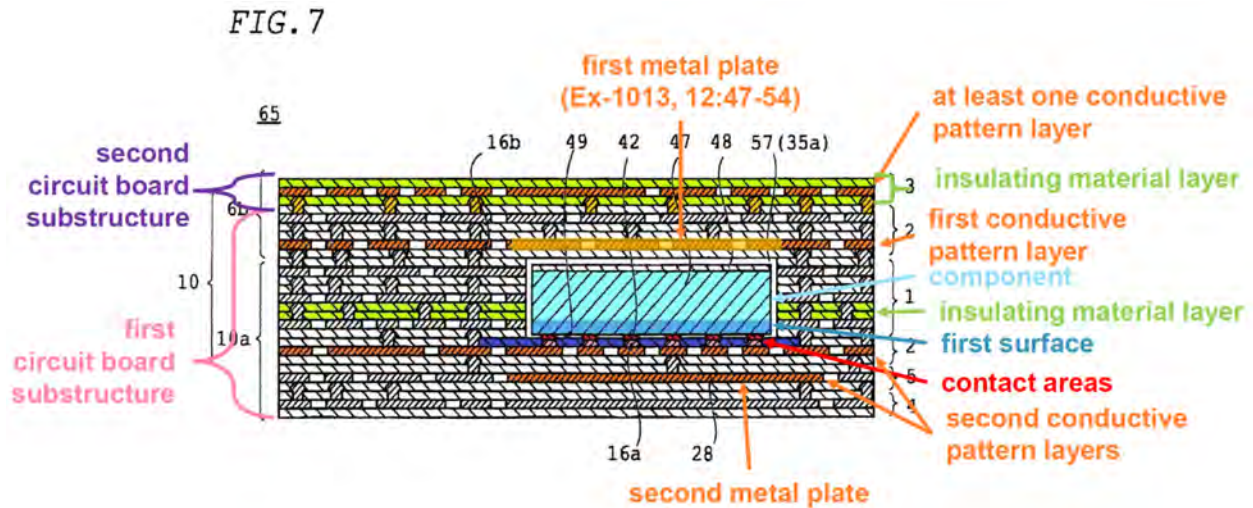


268. Alternatively, as described above for Claim 15 (Section VII.F.8), Kurita discloses that a multilayer substrate may be connected on top or bottom to “other circuit substrates.” Kurita states that semiconductor devices and wiring films 15 inside a multilayer substrate can be “electrically connected” to these other circuit substrates. Ex-1013, 10:13-22. Thus, Kurita discloses that the first circuit board substructure (multilayer substrate) and second circuit board substructure (“other circuit substrate”) are electrically connected to each other to form a multi-layered functioning totality.

- 10. Dependent Claim 17: The multi-layered circuit board of claim 16, wherein said second circuit board substructure comprises an insulating material layer and at least one conductive pattern layer in the insulating material layer.**

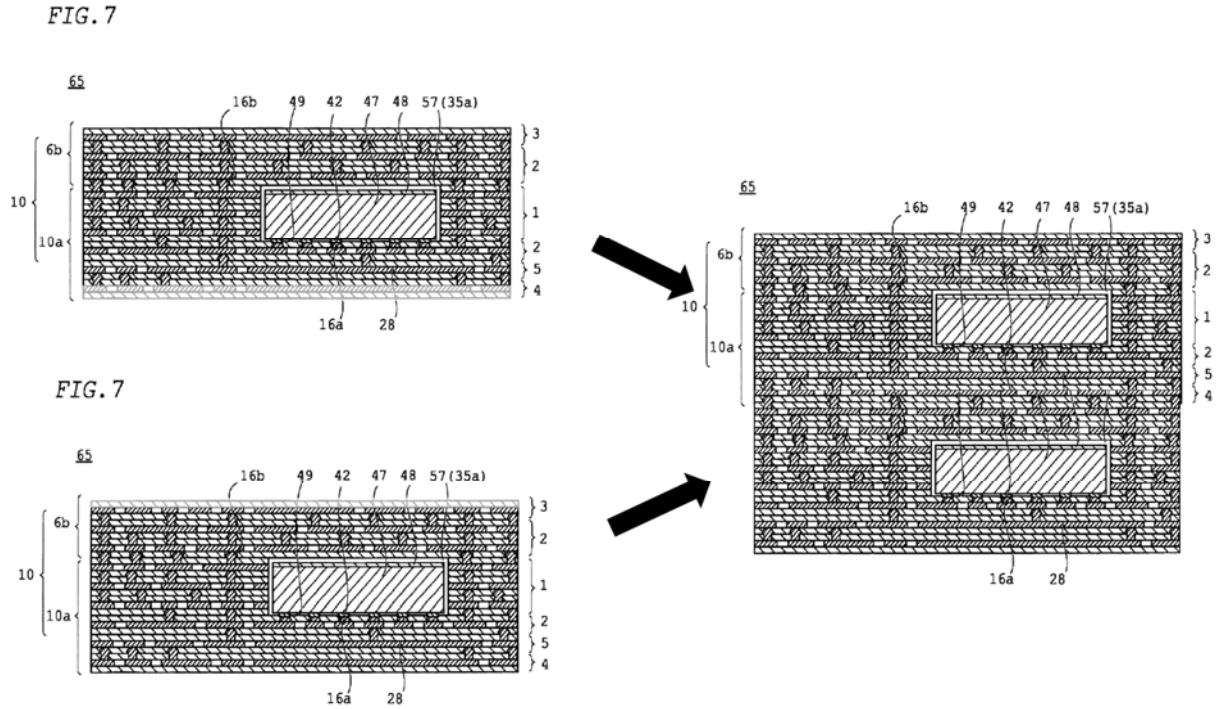
269. Kurita discloses and renders obvious Claim 17.

270. The second circuit board substructure identified for Claim 15 (§VII.F.8) includes an insulating material layer and at least one conductive pattern layer in the insulating material layer, as shown below.



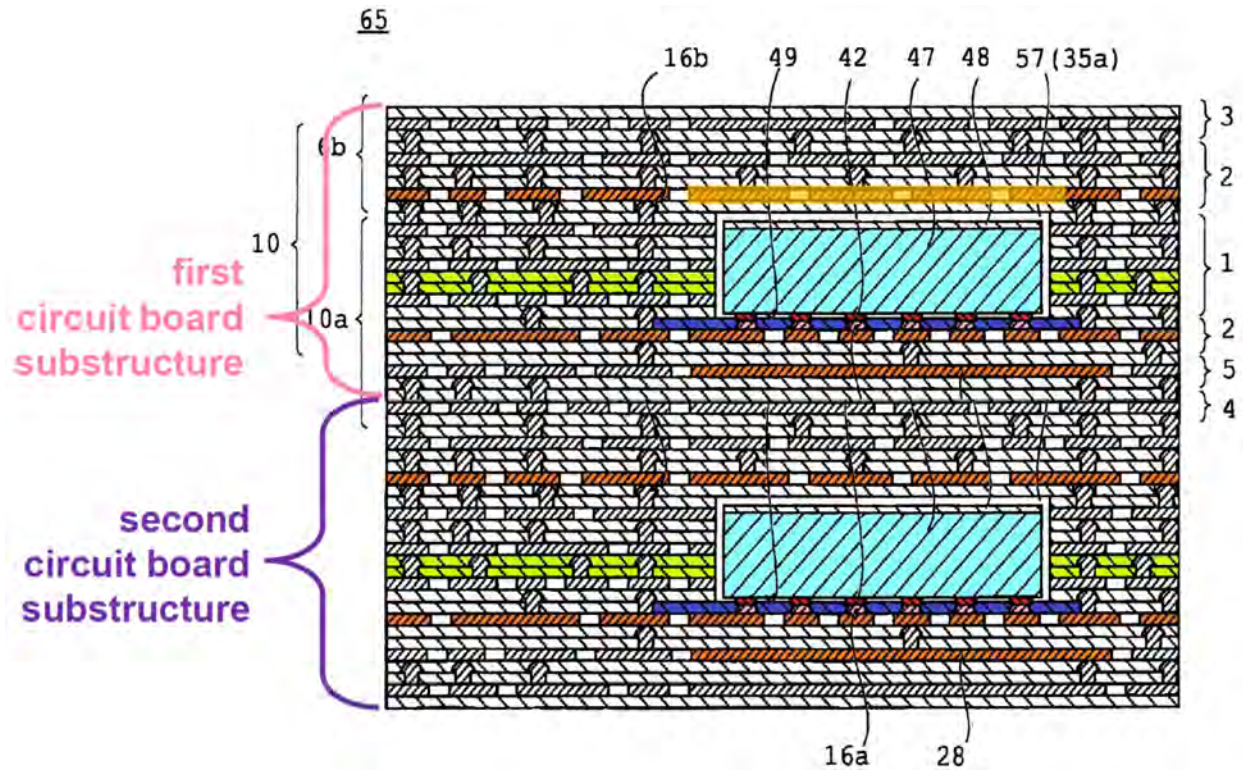
271. Alternatively, as described above for Claim 15 (Section VII.F.8), Kurita discloses that a multilayer substrate may be connected to “other circuit substrates.” Because a multilayer substrate is a “circuit substrate,” Kurita discloses that one multilayer substrate can be connected to another multilevel substrate. At the very least, it would have been obvious to a POSITA that the “other circuit substrates” could be another multilevel substrate.

272. The below diagram depicts connecting one multilayer substrate of Figure 7 to another.

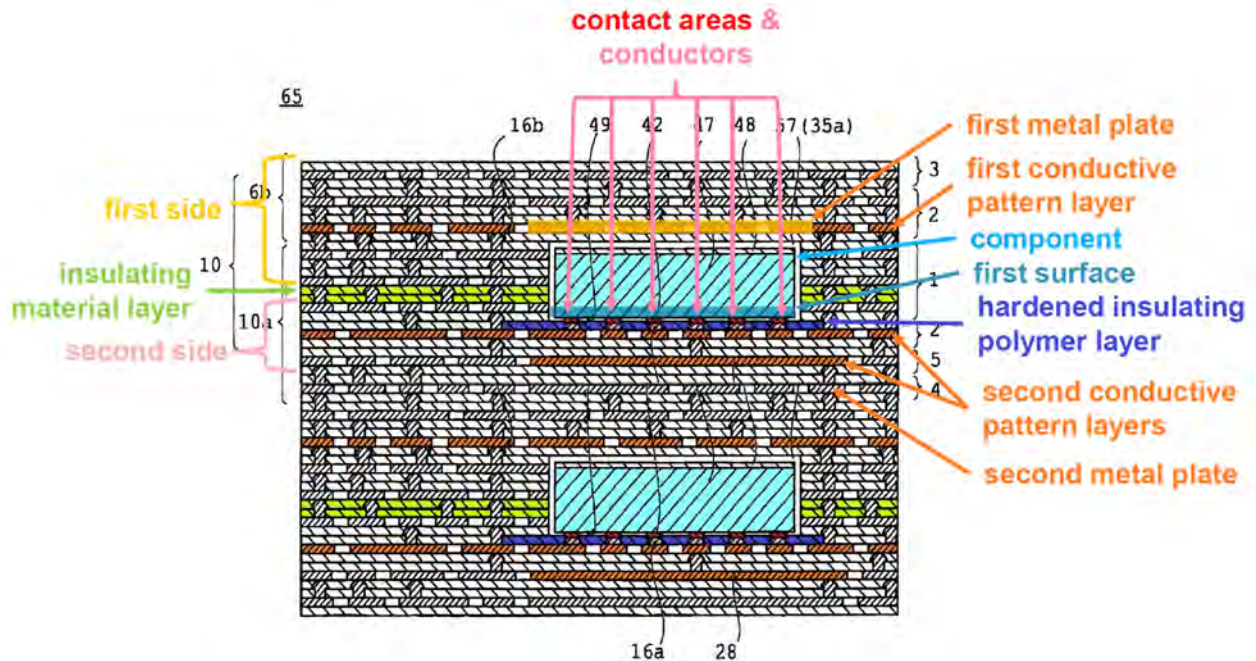


This stacked structure discloses Claim 17.

273. The following figure identifies the claimed first and second circuit board substructures in this stacked structure.

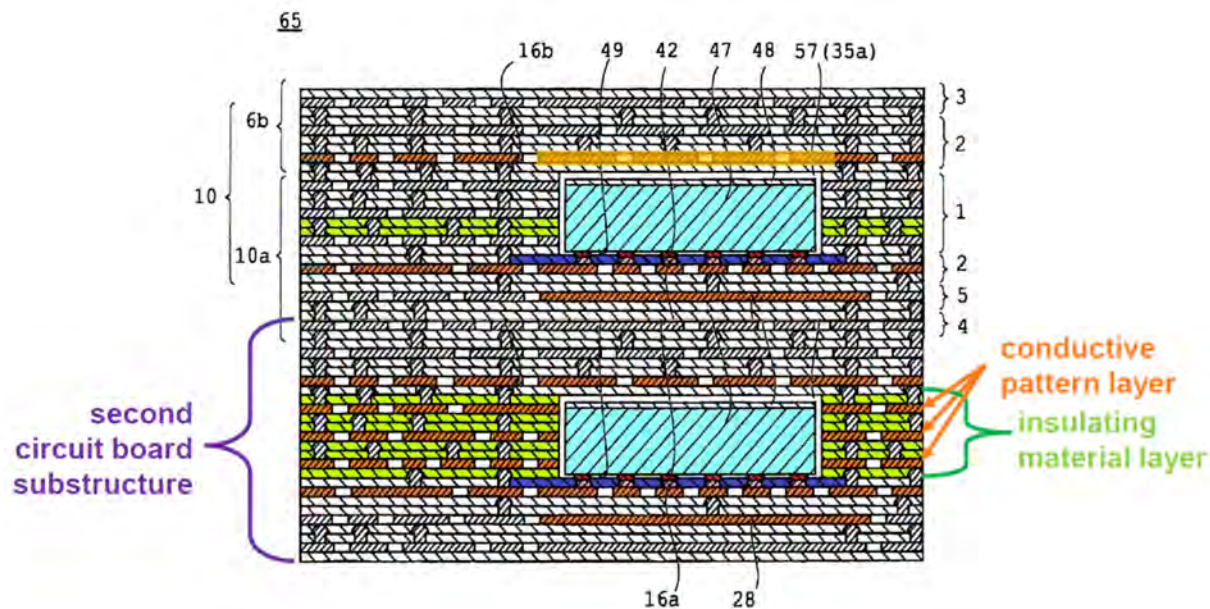


274. The first circuit board substructure meets Elements 15[a]-15[f] for the reasons described for Elements 1[a]-1[f] (§VII.F.1.a-f), as shown below.



275. The stacked structure also meets Claim 16. *See supra* VII.F.9.

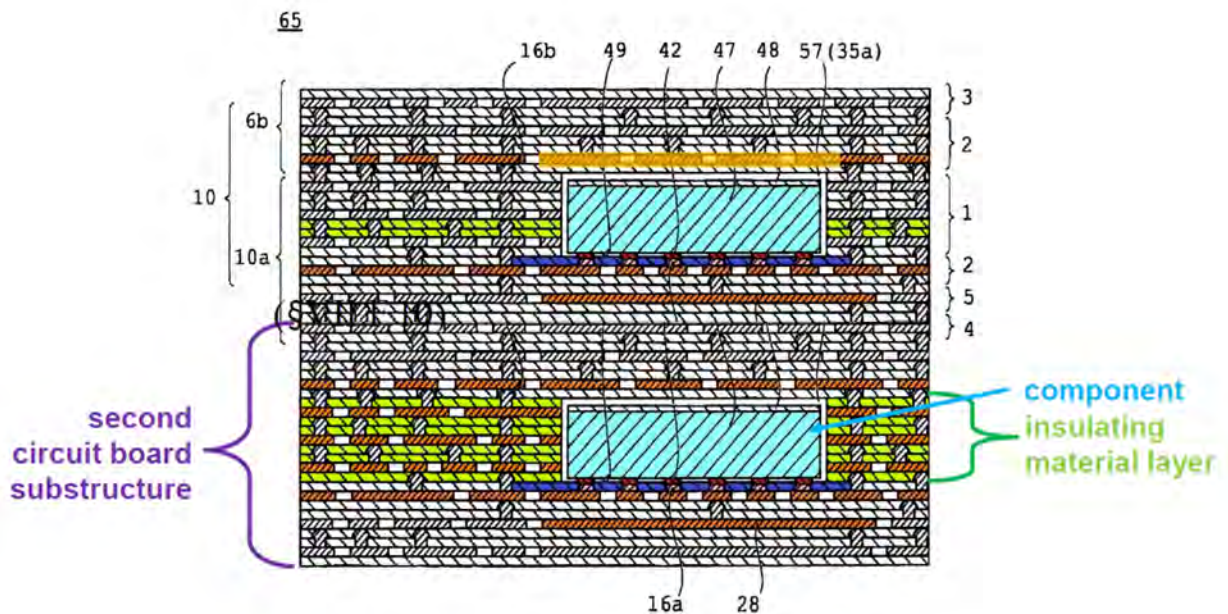
276. For the reasons described for Elements 1[a]-[c] (Sections VII.F.1.b-d), Kurita discloses and renders obvious that the second circuit board substructure comprises an insulating material layer (resin film 25) and at least one conductive pattern layer (wiring film 15) in the insulating layer, as shown below and recited in Claim 17.



- 11. Dependent Claim 18: The multi-layered circuit board of claim 17, wherein said second circuit board substructure includes a component embedded in the insulating material layer.**

277. Kurita discloses and renders obvious Claim 18.

278. For the reasons described for Element 1[d] (§VII.F.1.e), the second circuit board substructure in Claim 17 (§VII.F.10) includes a component (semiconductor device 47) embedded in the insulating material, as shown below.

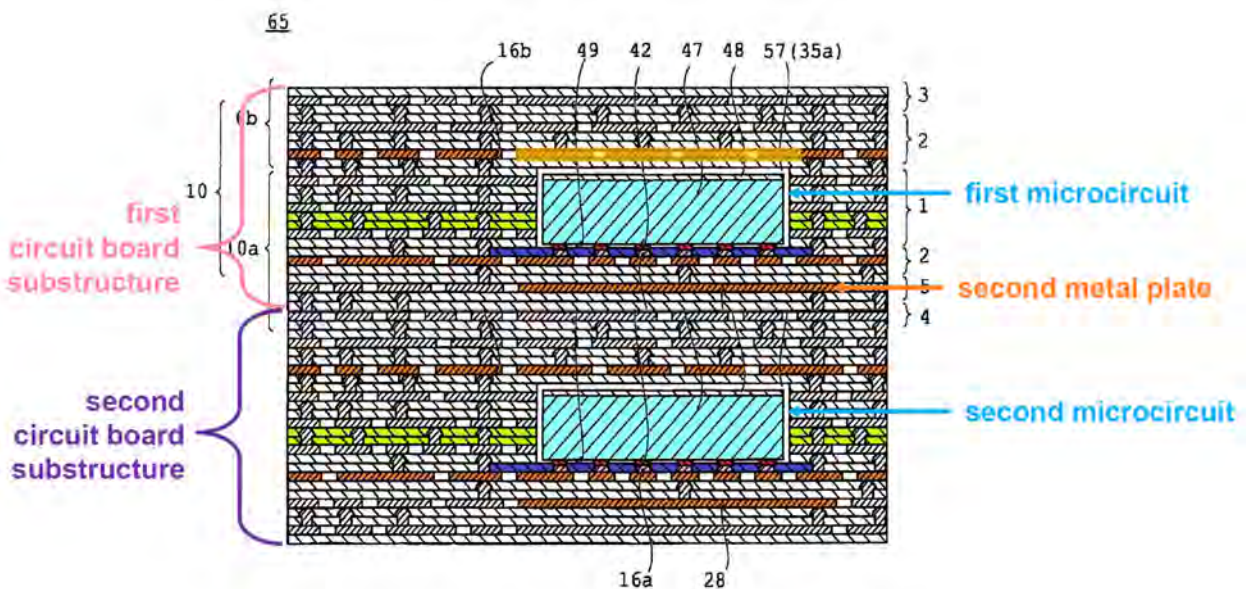


12. **Dependent Claim 19:** The multi-layered circuit board of claim 15, wherein said first circuit board substructure comprises a first microcircuit and said second circuit board substructure comprises a second microcircuit such that the first and second microcircuits are on top of each other and at least one of the first and second metal plates is located between said first and second microcircuits.

279. Kurita discloses and renders obvious Claim 19.

280. As described above for Claim 17 (Section VII.F.10), Kurita discloses or renders obvious connecting one multilayer substrate of Figure 7 to another, and the resulting stacked structure satisfies Claim 15.

281. Additionally, the first circuit board substructure comprises a first microcircuit (semiconductor device 47) and the second circuit board substructure comprises a second microcircuit (semiconductor device 47) such that the microcircuits are on top of each other and at least one of the first and second metal plates is located between the microcircuits, as recited in Claim 19.



282. As explained above for Claim 13 (Section VII.F.6), a POSITA would have understood that semiconductor device 47 in Kurita is a microcircuit.

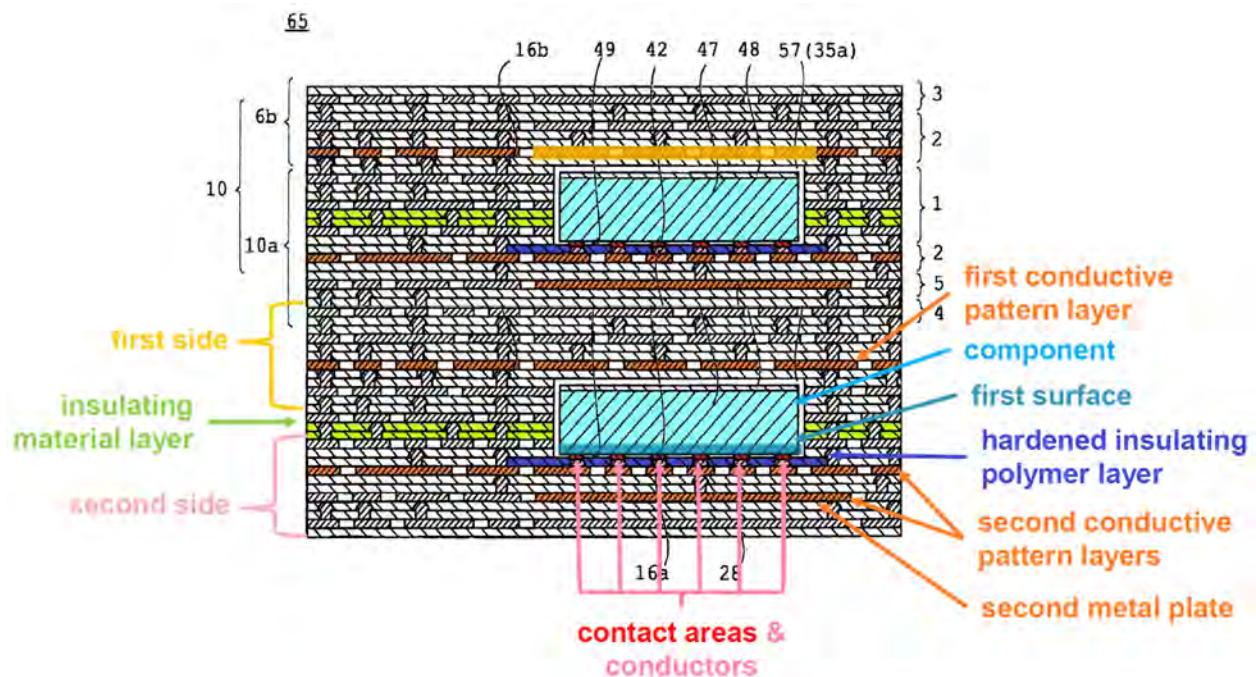
13. Dependent Claim 20

283. Kurita discloses and renders obvious Claim 20.

284. Claim 20 requires that the second circuit board substructure include all elements of Claim 1, except the first metal plate on the first side of the insulating material layer. *Compare* Elements 20[a]-[f] to Elements 1[a]-[f].

285. As described above for Claim 17 (Section VII.F.10), Kurita discloses or renders obvious connecting one multilayer substrate of Figure 7 to another, and the resulting stacked structure satisfies Claim 15.

286. Also for the reasons described above for Elements 1[a]-1[f] (Section VII.F.1.a-f), the second circuit board substructure meets Elements 20[a]-20[f], as shown below.



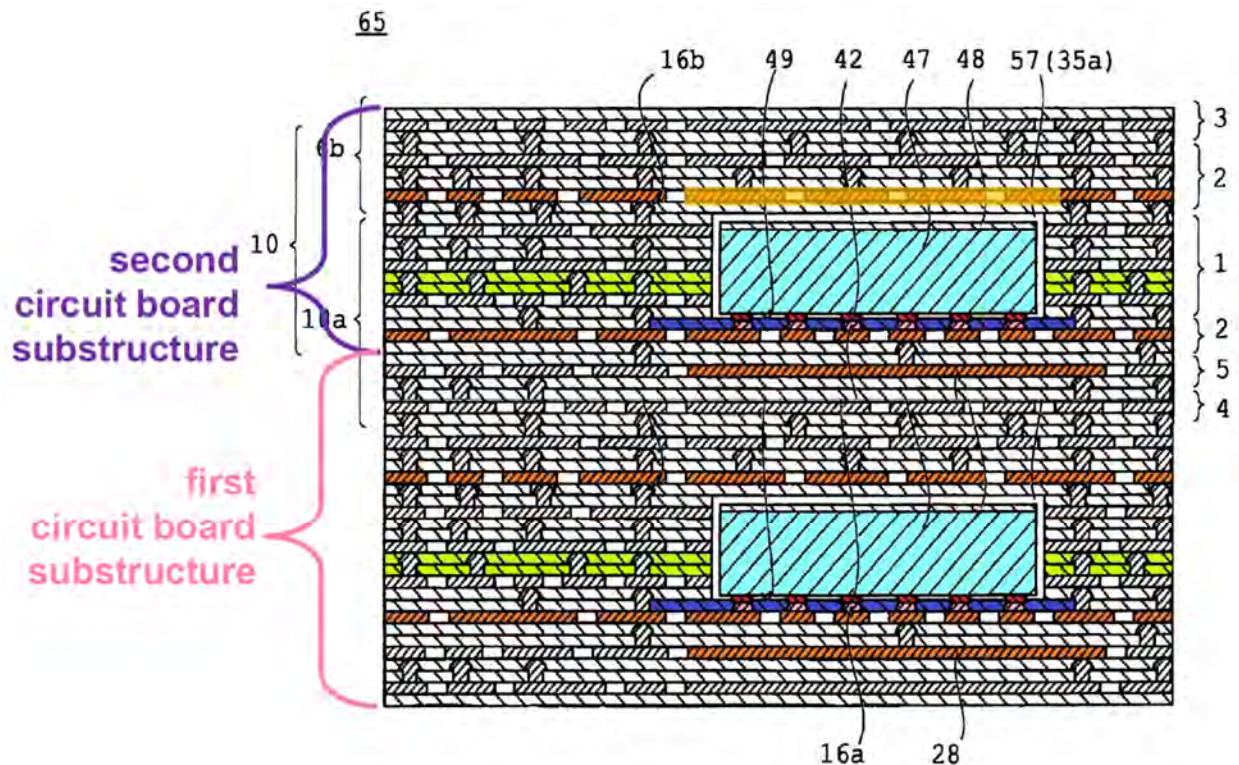
14. Dependent Claim 21

287. Kurita discloses and renders obvious Claim 21.

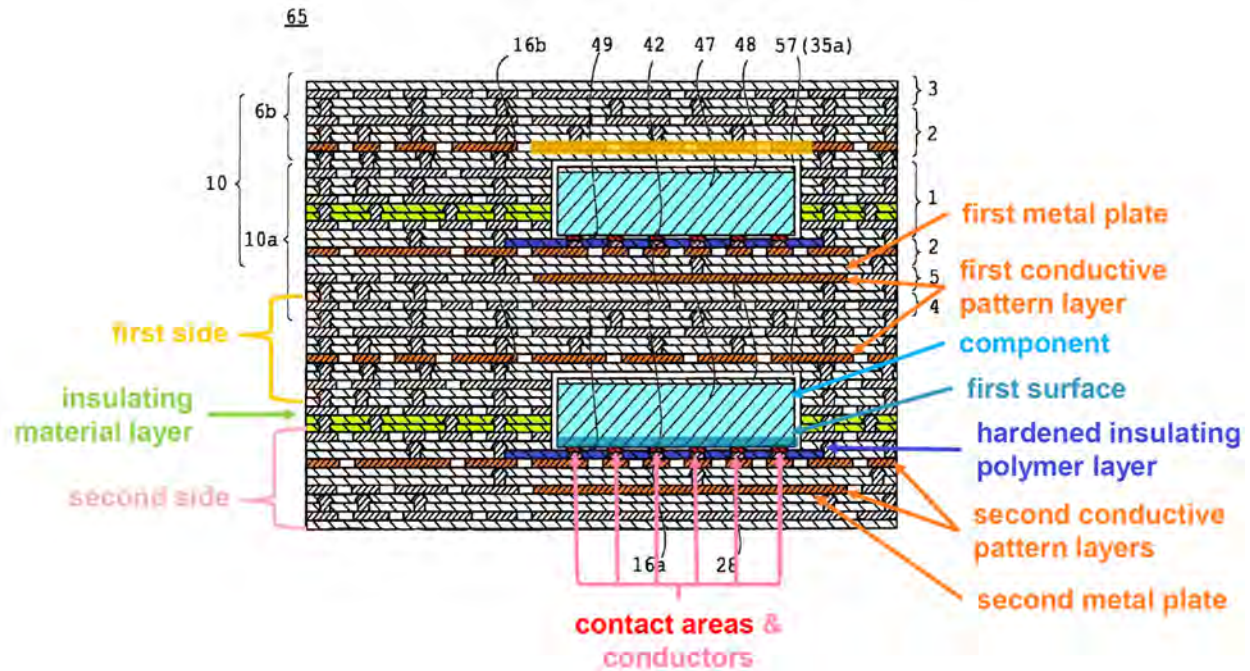
288. Claim 21 is like Claim 20, with one small difference. Claim 21 requires that the second circuit board substructure include all elements of Claim 1, except the **second** metal plate on the second side of the insulating material layer. Compare Element 21[a]-[f] to Elements 1[a]-[f].

289. As described above for Claim 17 (Section VII.F.10), Kurita discloses or renders obvious connecting one multilayer substrate of Figure 7 to another.

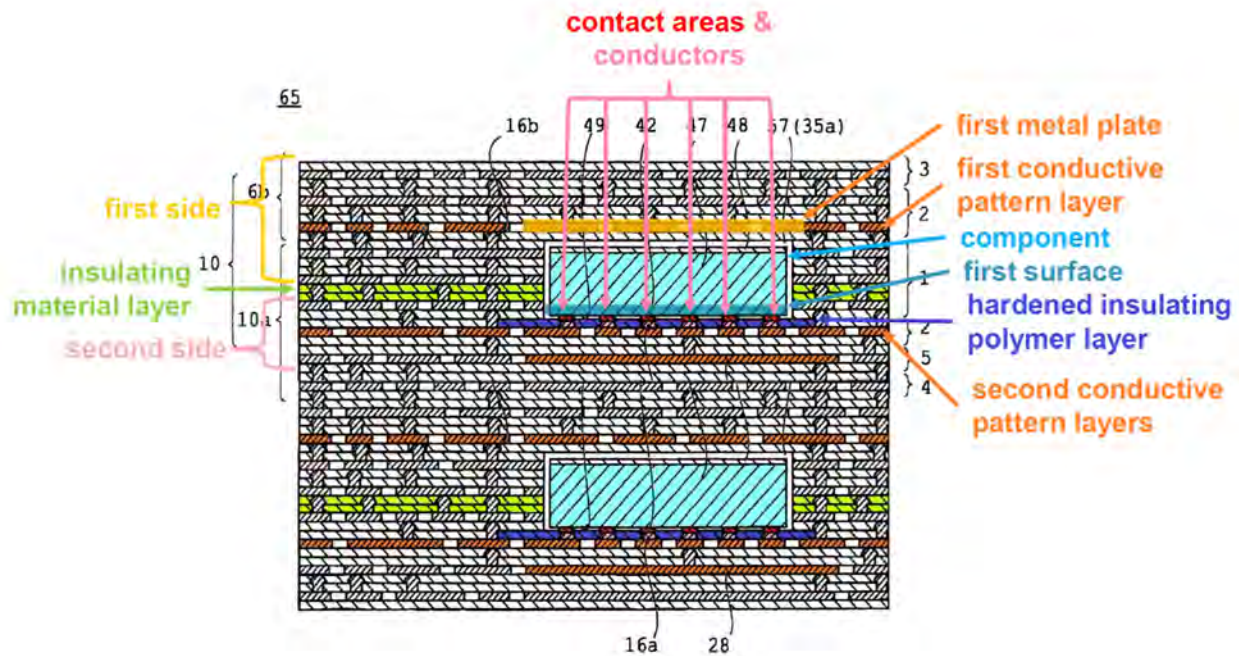
290. The following figure identifies the claimed first and second circuit board substructures under an alternative reading in which the first circuit board substructure is below the second circuit board substructure.



291. The first circuit board substructure identified above meets Elements 15[a]-15[f] for the reasons described above for Elements 1[a]-1[f] (Section VII.F.1.a-f), as shown below.



292. Also for the reasons described above for Elements 1[a]-1[f] (Section VII.F.1.a-f), the second circuit board substructure meets Elements 20[a]-20[f], as shown below.



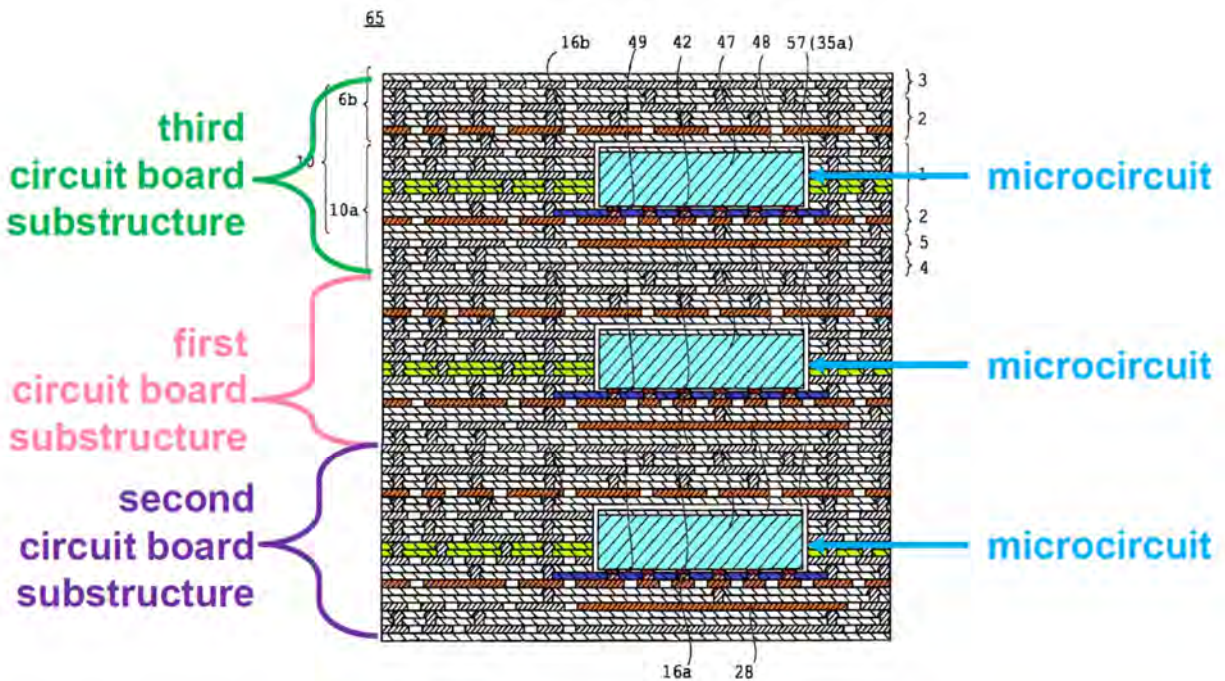
293. Accordingly, Kurita discloses and renders obvious Claim 21.

15. Dependent Claims 22: The multi-layered circuit board of claim 15, comprising a third circuit board substructure on top of the first and second circuit board substructures.

294. Kurita discloses and renders obvious Claim 22.

295. As described above with reference to Claim 17 (Section VII.F.10), Kurita discloses and renders obvious that one multilayer substrate can be connected to another multilevel substrate. Based on the same disclosures and the same motivations, Kurita discloses and renders obvious to POSITA that three multilayer substrates of Figure 7 could be stacked on top of one another.

296. The below figure shows a stack of three multilayer substrates of Figure 7.



297. As shown above, the third circuit board substructure is on top of the first and second circuit board substructures, and thus, Kurita discloses or renders obvious Claim 22.

16. Dependent Claim 23: The multi-layered circuit board of claim 22, wherein the first circuit board substructure is between the second and third circuit board substructures.

298. As shown above for Claim 22 (Section VII.F.15), the first circuit board substructure is between the second and third circuit board substructures, and thus, Kurita discloses and renders obvious Claim 23.

17. Dependent Claim 24: The multi-layered circuit board of claim 22, wherein each of the first, second and third circuit board substructures includes an embedded microcircuit.

299. As shown above in Claim 22 (Section VII.F.15), the first, second and third circuit board substructures include an embedded microcircuit, and thus, Kurita discloses and renders obvious Claim 24.

300. As explained above for Claim 13 (Section VII.F.6), a POSITA would have understood that semiconductor device 47 in Kurita is a microcircuit.

18. Dependent Claim 25: The multi-layered circuit board of claim 15, wherein the first and second metal plates are electronically connected to each other.

301. Claim 25 is the same as Claim 2 but depends from Claim 15. For the reasons described for Claim 2 (§VII.F.2) and Claim 15 (§VII.F.8), Imoto renders obvious Claim 25.

19. Dependent Claim 26: The multi-layered circuit board of claim 15, wherein the first and second metal plates are electrically connected to each other.

302. Claim 26 is the same as Claim 2 but depends from Claim 15. For the reasons described for Claim 2 (§VII.F.2) and Claim 15 (§VII.F.8), Imoto renders obvious Claims 26.

- 20. Dependent Claim 29: The multi-layered circuit board of claim 15, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.**

303. Claim 29 is the same as Claim 11 but depends from Claim 15. Thus, as described above for Claim 11 (Section VII.F.5) and Claim 15 (Section VII.F.8), Kurita discloses and renders obvious Claim 29.

- 21. Dependent Claim 30: The multi-layered circuit board of claim 15, wherein the component is a microcircuit.**

304. Claim 30 is the same as Claim 13 but depends from Claim 15. Thus, as described above for Claim 13 (Section VII.F.6) and Claim 15 (VII.F.8), Kurita discloses and renders obvious Claim 30.

- 22. Dependent Claims 31: The multi-layered circuit board of claim 15, wherein the first circuit board substructure comprises at least two microcircuits inside the insulating material layer.**

305. Kurita discloses and renders obvious Claim 22. Kurita discloses embedding “a plurality of semiconductor devices” in a multilayer substrate. Ex-1013, 10:36-44.

306. As explained above for Claim 13 (Section VII.F.6), a POSITA would have understood that semiconductor devices 47 in Kurita are microcircuits.

307. Thus, Kurita discloses or renders obvious the first circuit board substructure including at least two microcircuits inside the insulating material layer.

G. Ground 7: Claims 4-7, 10, 27, 28, and 32-36 are obvious over Kurita in view of Dudderar

- 1. A POSITA would be motivated to combine Kurita and Dudderar's teachings and would have a reasonable expectation of success.**

308. In addition to the reasons set out below with respect to specific claim elements, a POSITA would have been motivated to combine the teachings of Kurita and Dudderar and would have had a reasonable expectation of success in doing so, because each relates to the same well-known technologies. Both relate to embedding semiconductor devices within the cavity of a printed circuit board (or base). Ex-1009, 2:53-54; Ex-1013, 9:6-11, 12:16-17. In addition, both describe using metallization connected to ground to act as a shield. Ex-1009, 2:63-3:3; Ex-1013, 4:1-9, 5:24-30, 6:62-64, 11:56-63, 12:8-15, 12:40-46. Although both provide metallization above and below semiconductor devices to shield them, Dudderar further describes extending that metallization to the inside walls of the cavity housing the semiconductor devices. Ex-1009, 4:45-50.

309. A POSITA would have been motivated to apply this additional teaching of Dudderar to Kurita by using metalation on the sidewalls of the cavity as a shield. Kurita recognized the benefits of using grounded metallization as shield, and based on Dudderar, a POSITA would have recognized that grounded metallization on the sidewalls of Kurita enhances those benefits. This would produce more reliable chips, less like to malfunction due to magnetic interference. Thus, design incentives

and market forces would have motivated a POSITA to apply the teachings of Dudderar to Kurita.

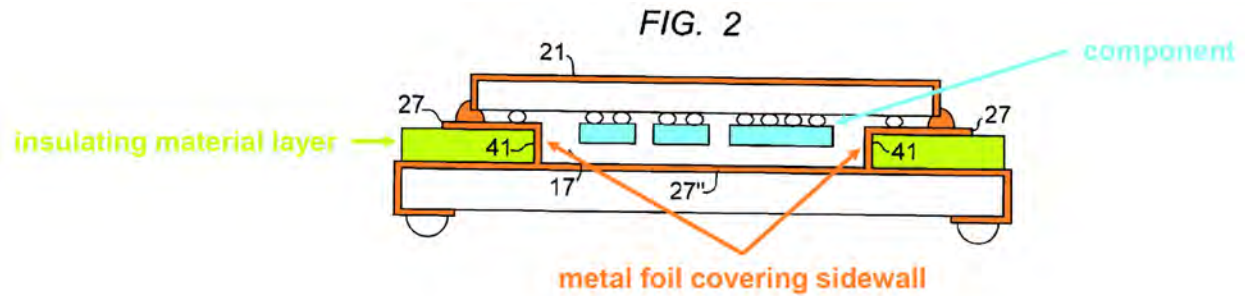
310. A POSITA would also have had a reasonable expectation of success in combining Kurita and Dudderar. A POSITA would have understood that these references disclose interrelated teachings based on routine technologies and would have been amendable to various well-understood and predictable combinations, as explained in further detail below.

2. Dependent Claim 4: The circuit board of claim 1, wherein the component is located in a hole in the insulating material layer, and the circuit board comprises metal foil covering the sidewalls of the hole and a filler material in the hole between the metal foil and the component.

311. Kurita-Dudderar in combination renders obvious Claim 4.

312. As described above with reference to Element 1[d] (Section VII.F.1.e), Kurita discloses a component (semiconductor device 47) in a hole (housing section 57) in the insulating material layer.

313. It would have been obvious to modify Kurita to include metal foil on sidewalls as described in Dudderar. Dudderar describes covering sidewalls 41 of chip cavity 17 with metallization for shielding, as shown below. Ex-1009, 4:45-50.



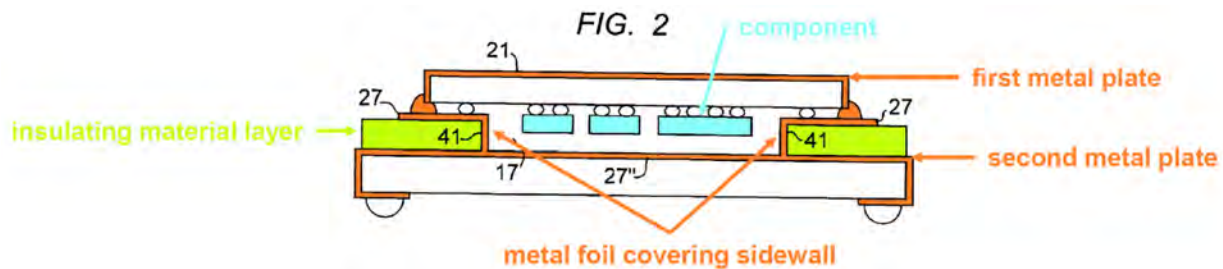
314. It would have been obvious to a POSITA to apply this teaching to the sidewalls of housing section 57 in Kurita. Kurita recognized the benefit of using metallization to shield semiconductor element, and it would have been obvious to a POSITA that grounded metallization on the sidewalls of Kurita enhances those benefits, as taught in Dudderar.

315. It also would have been obvious to modify Kurita to include filler material in housing section 57 as described in Dudderar. Dudderar incorporates by reference Degani. *See supra* Section V.C.2. Degani discloses the use of an encapsulating material 22/27 in the cavity of a substrate to protect an embedded chip and its interconnections. Ex-1014, 5:63-6:3, 5:25-27. It would have been obvious to a POSITA to apply such encapsulation material to housing section 57 in Kurita to protect semiconductor device 47 and its interconnections.

3. Dependent Claim 5: The circuit board of claim 4, wherein the metal foil is electrically connected to at least one of the first and second metal plates.

316. Kurita-Dudderar in combination renders obvious Claim 5.

317. As explained above for Claim 4 (Section VII.G.2), it would have been obvious to apply Dudderar to Kurita by covering the sidewalls of housing section 57 with metal foil for shielding purposes. Dudderar also teaches that the metal foil on the sidewalls is connected to the first and second metal plates and to ground, as shown below. Ex-1009, 3:28-37, 4:45-50.



318. Because Kurita also teaches that the metal plates (shield section 28) are connected together and connected to ground (*see supra* Section VII.F.2), it would have been obvious to electrically connect metal foil on the sidewalls of housing section 57 to the first and second metal plates and to ground.

4. Dependent Claim 6: The circuit board of claim 4, wherein the metal foil is electronically connected to an earth connection of the circuit board.

319. As explained above for Claim 5 (Section VII.G.3), both Kurita and Dudderar teach connecting metallization to ground to act as a shield. As explained above for Claim 3 (Section VII.A.3), a POSITA would have understood ground to be the claimed “earth connection.” Thus, it would have been obvious to

electronically connect metal foil on the sidewalls of Kurita to an earth connection of the circuit board.

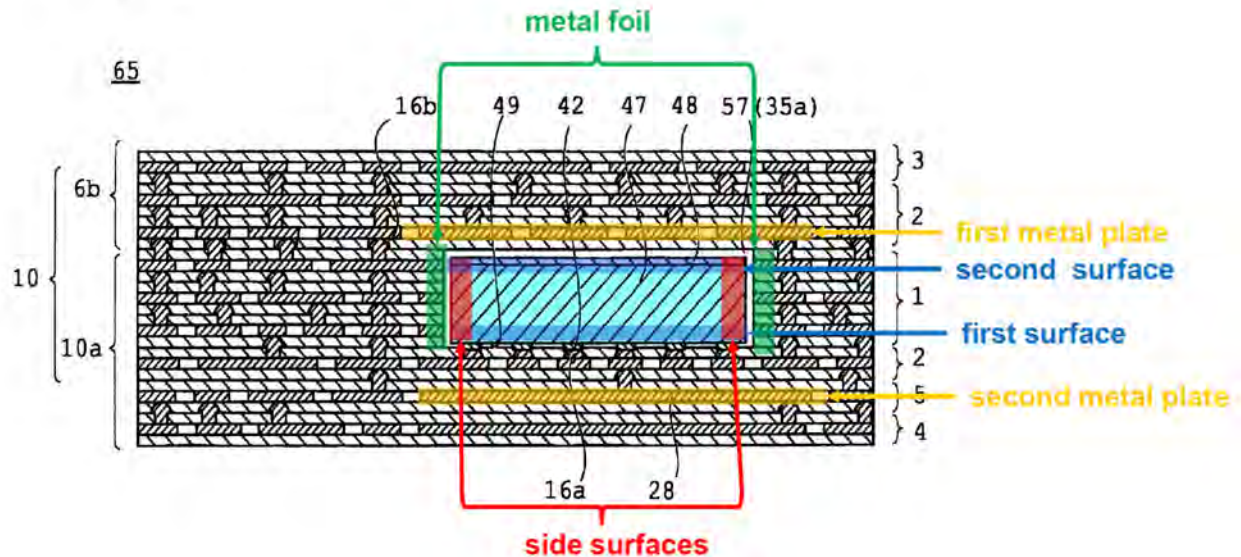
5. **Dependent Claim 7: The circuit board of claim 4, wherein the component has a second surface opposite to the first surface and side-surfaces between the first and second surfaces, and wherein the first and second metal plates and the metal foil form an electromagnetic interference shield around the component such that the side-surfaces of the component face towards the metal foil, the first surface of the component face towards the second metal plate, and the second surface of the component face towards the first metal plate.**

320. Kurita-Dudderar in combination renders obvious Claim 7.

321. As explained above for Claim 4 (Section VII.G.2), it would have been obvious to apply Dudderar to Kurita by covering the sidewalls of housing section 57 with metal foil for shielding purposes.

322. As shown below, Kurita-Dudderar in combination renders obvious Claim 7.

FIG. 7



6. **Dependent Claim 10:** The circuit board of claim 8, wherein the component is located in a hole in the baseboard; and the circuit board comprises conductive material on the sidewalls of the hole and a filler material in the hole between the metal foil and the component, wherein the metal foil creates an interference protection structure around the component.

323. Claim 10 combines the elements of Claims 4 and 8.

324. Thus, as described above for Claims 4 (Section VII.G.2) and Claim 8 (Section VII.F.4), Kurita-Dudderar in combination renders obvious Claim 10.

7. **Dependent Claim 27: The multi-layered circuit board of claim 15, wherein the component is located in a hole in the insulating material layer, and the circuit board comprises metal foil covering the sidewalls of the hole and a filler material in the hole between the metal foil and the component.**

325. Claim 27 is the same as Claim 4 but depends from Claim 15.

326. Thus, as described above for Claim 4 (Section VII.G.2) and Claim 15 (Section VII.F.8), Kurita-Dudderar in combination renders obvious Claim 27.

8. **Dependent Claim 28: The multi-layered circuit board of claim 15, wherein the metal foil is electronically connected to at least one of the first and second metal plates.**

327. Claim 28 is the same as Claim 5 but depends from Claim 15.

328. Thus, as described above for Claim 5 (Section VII.G.3) and Claim 15 (Section VII.F.8), Kurita-Dudderar in combination renders obvious Claim 27.

9. **Independent Claim 32**

- a. **Element 32[preamble]: An electronic module comprising**

329. Kurita discloses a multi-layer substrates including semiconductor devices and thus, Kurita teaches the preamble of Claim 1, to the extent it is limiting.
Ex-0013, 1:6-8, 5:57-58.

- b. **Element 32[a]: an insulating material layer having a first side and a second side,**

330. Element 32[a] is the same as Element 1[a], and thus Kurita discloses this element as described above for Element 1[a] (Section VII.F.1.b).

- c. **Element 32[b]: at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate,**

331. Element 32[b] is the same as Element 1[b], and thus Kurita discloses this element as described above for Element 1[b] (Section VII.F.1.c).

- d. **Element 32[c]: at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate,**

332. Element 32[c] is the same as Element 1[c], and thus Kurita discloses this element as described above for Element 1[c] (Section VII.F.1.d).

- e. **Elements 32[d], [e], [f], and [g]: a hole having sidewalls defined in the insulating material layer and located between the first and second metal plates, a metal foil covering the sidewalls of the hole, a microcircuit inside the hole and having a first surface facing towards the second metal plate, and contact areas on the first surface, a filler material in the hole between the metal foil and the microcircuit,**

333. Element 32[d], [e], [f], and [g] are the same as Element 1[d], Element 1[e], Claim 4, and Claim 13, and thus, Kurita-Dudderar in combination renders obvious these elements as described for Element 1[d] (§VII.F.1.e), Element 1[e] (§VII.F.1.f), Claim 4 (§VII.G.2) and Claim 13 (VII.F.6).

- f. Element 32[h]: a hardened insulating polymer layer between the first surface of the microcircuit and at least one conductive pattern of said at least one second conductive pattern layer, and**

334. Element 32[h] is the same as Element 1[e], and thus Kurita discloses this element as described above for Element 1[e] (Section VII.F.1.f).

- g. Element 32[i]: contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the microcircuit and the at least one second conductive pattern layer or layers.**

335. Element 32[i] is the same as Element 1[f], and thus Kurita discloses this element as described above for Element 1[f] (Section VII.F.1.g).

- 10. Dependent Claim 33: The electronic module of claim 32, wherein the first and second metal plates are electronically connected to each other.**

336. Claim 33 is the same of Claim 2 but depends from Claim 32. Thus, as described above for Claim 2 (Section VII.F.2) and Claim 32 (Section VII.G.9), Kurita-Dudderar in combination renders obvious Claim 33.

- 11. Dependent Claim 34: The electronic module of claim 32, wherein the first and second metal plates are electrically connected to an earth connection of the electronic module.**

337. Claim 34 is the same of Claim 3 but depends from Claim 32. Thus, as described above for Claim 3 (Section VII.F.3) and Claim 32 (Section VII.G.9), Kurita-Dudderar in combination renders obvious Claim 33.

- 12. Dependent Claim 35: The electronic module of claim 32, wherein the metal foil is electronically connected to at least one of the first and second metal plates.**

338. Claim 35 is the same of Claim 5 but depends from Claim 32. Thus, as described above for Claim 5 (Section VII.G.3) and Claim 32 (Section VII.G.9), Kurita-Dudderar in combination renders obvious Claim 33.

- 13. Dependent Claim 36: The electronic module of claim 32, wherein the metal foil and the first and second metal plates are electronically connected to an earth connection of the electronic module.**

339. Claim 36 is the same of Claim 3 and 6 but depends from Claim 32. Thus, for the reasons described above with reference to Claim 3 (Section VII.F.3), Claim 6 (Section VII.G.4), and Claim 32 (Section VII.G.9), Kurita-Dudderar in combination renders obvious Claim 36.

H. Ground 8: Claims 9, 12, and 31 are obvious over Kurita in view of Mowatt

- 1. A POSITA would be motivated to combine Kurita and Mowatt's teachings and would have a reasonable expectation of success.**

340. In addition to the reasons set out below with respect to specific claim elements, a POSITA would have been motivated to combine the teachings of Kurita and Mowatt and would have had a reasonable expectation of success in doing so, because each relates to the same well-known technologies. Both relate to embedding semiconductor devices within the cavity of a laminated plate/printed wiring board.

Ex-1010, 9:40-43; Ex-1013, 9:6-11, 12:16-17. A POSITA would have understood that these references disclose interrelated teachings based on routine technologies and would have been amendable to various well-understood and predictable combinations.

2. Dependent Claims 9: The circuit board of claim 8, wherein the baseboard is a glass-fibre reinforced epoxy board.

341. Kurita-Mowatt in combination renders obvious Claim 9.

342. As described above with reference to Claim 8 (Section VII.F.4), the baseboard in Kurita is resin film 25, which is “formed of polyimide film by hardening of the precursor coat 23.” Ex-1013, 7:25-27. Like Kurita, Mowatt describes embedding semiconductor devices within the cavity of a baseboard. Ex-1010, 9:40-43. Mowatt teaches that the baseboard could include “an ***epoxy glass material***, or polyimide glass material, teflon or other materials commonly used in PWB fabrication.” Ex-1010, 4:40-43 (emphasis added). It would have been obvious to POSITA to apply this teaching to Kurita so that the baseboard is a glass-fibre reinforced epoxy board. A POSITA would have been motivated to use glass-fibre reinforced epoxy boards to increase the rigidity and stability of the substrates.

3. Dependent Claim 12: The circuit board of claim 1, wherein the hardened insulating polymer layer contains epoxy.”

343. Kurita-Mowatt in combination renders obvious Claim 12.

344. As described above with reference to Element 1[e] (Section VII.F.1.f), the hardened insulating polymer layer in Kurita is adhesive layer 21, which is a thermoplastic formed from heating polyimide resin to become adhesive. Ex-1013, 6:42-50, 7:62-8:6.

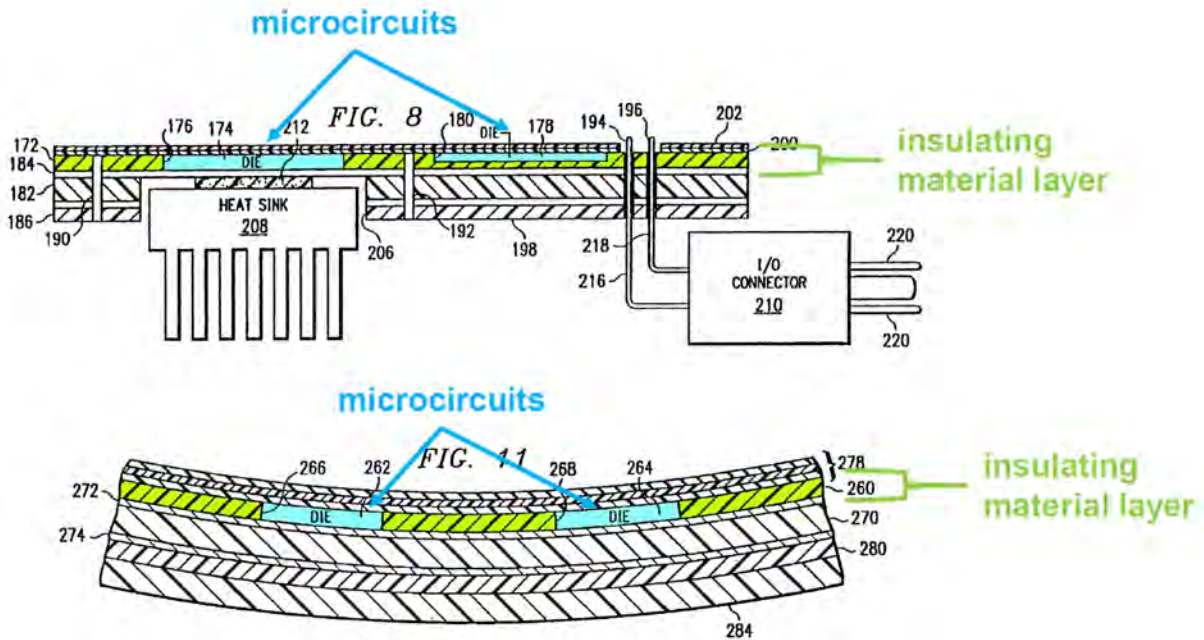
345. Like Kurita, Mowatt teaches the use of a polyimide resin between layers in a multilayer circuit board. Ex-1010, 7:18-30. In particular, Mowatt teaches the use of a “thermoset adhesive such as Siloxide Polymide epoxy.” *Id.*, 7:24-25.

346. It would have been obvious to a POSITA to apply this teaching to Kurita so that adhesive layer 2 is a polyimide resin containing epoxy. Thus, the Kurita-Mowatt combination renders obvious that the hardened insulating polymer layer (adhesive layer 21) contains epoxy.

4. Dependent Claims 31: The multi-layered circuit board of claim 15, wherein the first circuit board substructure comprises at least two microcircuits inside the insulating material layer

347. As discussed above in Ground 6 (Section VII.F.22), Kurita discloses and renders obvious Claim 31.

348. Alternatively, Kurita-Mowatt in combination also renders obvious Claim 31. As described above in Ground 3 (Section VII.C.3), Mowatt discloses two microcircuits inside the same insulating material layer, as shown below in Figures 8 and 11.



349. Mowatt refers to the dies variously as semiconductor dies, chip dies, and integrated circuit chips. Ex-1010, Abstract, 1:8, 2:64, 4:55, 6:34, 12:9-15, 12:59. For the reasons explained above for Claim 13 (Section VII.A.6), a POSITA would have understood that the dies in Mowatt are microcircuits.

350. In view of Figure 8 and 11 of Mowatt and the additional teachings of Kurita (Section VII.F.21), it would have been obvious to a POSITA that at least two microcircuits (semiconductor devices 47) can be embedded in an insulating material layer. A POSITA would have been motivated to add a microcircuit to increase functionality, to reduce manufacturing costs, and to save space.

VIII. CONCLUSION

351. For the reasons set forth above, I believe that Claims 1-36 of the '944 Patent is unpatentable in view of the prior art.

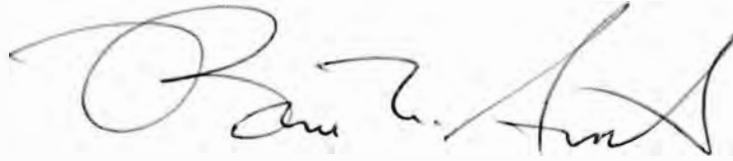
352. In signing this declaration, I recognize that it will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place in the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

353. I reserve the right to supplement my opinions in the future to respond to any arguments that the Patent Owner raises and to take into account new information as it becomes available to me.

354. I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

U.S. Patent No. 7,989,944
Declaration of Bruce W. Smith

Respectfully Submitted,

A handwritten signature in black ink, appearing to read "Bruce W. Smith", with a large, stylized initial "B" and a long, sweeping horizontal stroke.

Dr. Bruce W. Smith

Date: December 9, 2022