

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.;
SAMSUNG ELECTRONICS AMERICA, INC.; and
SAMSUNG AUSTIN SEMICONDUCTOR, LLC,
Petitioner

v.

IMBERATEK, LLC
Patent Owner.

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,989,944**

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LIST OF EXHIBITS¹

Ex. No.	Description
Ex-1001	U.S. Patent No. 7,989,944 to Tuominen (“the ’944 Patent”)
Ex-1002	Declaration of Dr. Bruce Smith
Ex-1003	Curriculum Vitae of Dr. Bruce Smith
Ex-1004	Prosecution History of the ’944 Patent (Application No. 11/878,557)
Ex-1005	U.S. Patent No. 7,294,529 to Tuominen (“the ’529 Patent”)
Ex-1006	Prosecution History of the ’529 Patent (Application No. 10/502,336)
Ex-1007	Certified Translation of Japanese Patent Publication No. JP2001-068624A to Imoto (“Imoto”)
Ex-1008	Japanese Patent Publication No. JP2001-068624A (“Imoto”)
Ex-1009	U.S. Patent No. 6,297,551 (“Dudderar”)
Ex-1010	U.S. Patent No. 5,306,670 (“Mowatt”)
Ex-1011	John H. Lau, <u>Low Cost Flip Chip Technologies</u> (2000).
Ex-1012	Gary L. Lehmann, T. Driscoll, N.R. Goydosh, P.C. Li, and Eric J. Cotts, Underflow Process for Direct-Chip-Attachment Packaging, <u>IEEE Transactions on Components, Packaging, and Manufacturing Technology</u> , June 1998 (“Lehmann”)
Ex-1013	U.S. Patent No. 6,404,052 (“Kurita”)
Ex-1014	U.S. Pat. No. 5,608,262 (“Degani”)
Ex-1015	The IEEE Standard Dictionary of Electrical and Electronics Terms, Sixth Edition (1996).

¹ Four-digit pin citations that begin with 0 are to the branded numbers added by Samsung in the bottom right corner of the exhibits. All other pin citations are to original page, column, paragraph, or line numbers.

Ex. No.	Description
Ex-1016	Semiconductor Chip Underfill Materials, <u>Encyclopedia of Materials: Science and Technology</u> , 2001.
Ex-1017	U.S. Patent No. 6,469,374 (“Imoto U.S. Patent”).
Ex-1018	Certified Translation of Japanese Patent No. P3207174 (“Hayashi”)
Ex-1019	Japanese Patent No. P3207174 (“Hayashi”)
Ex-1020	U.S. Patent No. 6,459,593 (“Kwong”)
Ex-1021	Certified Translation of Japanese Patent Publication No. JP2001-237586A (“Asahi Japanese Publication”)
Ex-1022	Japanese Patent Publication No. JP2001-237586A (“Asahi Japanese Publication”)
Ex-1023	Certified Translation of Japanese Patent Publication No. JP2001-111232A (“Oya”)
Ex-1024	Japanese Patent Publication No. JP2001-111232A (“Oya”)
Ex-1025	U.S. Patent Publication No. 2003/0090833 to Asahi (“Asahi U.S. Publication”)

I. INTRODUCTION

Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Austin Semiconductor, LLC (collectively, “Petitioner”) request inter partes review (“IPR”) of Claims 1-36 of U.S. Patent No. 7,989,944 (“the ’944 Patent”) (Ex-1001), currently assigned to ImberaTek LLC (“PO”).

II. MANDATORY NOTICES, STANDING, AND FEES

A. Mandatory Notices Under 37 C.F.R. §42.8

Real Parties-in-Interest: Petitioner identifies the following real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Austin Semiconductor, LLC.

Related Matters: PO has asserted the ’944 Patent against Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Austin Semiconductor, LLC in ImberaTek LLC v. Samsung Elec. Co., Ltd., No. 2:22-cv-00233 (E.D. Tex. Jun. 24, 2022).

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B. Grounds for Standing

Petitioner certifies that the '944 Patent is available for review, and Petitioner is not barred or estopped from requesting review.

C. Fee Authorization

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-0639.

III. RELIEF REQUESTED

For purposes of this proceeding only, Petitioner assumes that the '944 Patent is entitled to its earliest alleged priority date, January 31, 2002, and thus applies pre-AIA 35 U.S.C. § 102.

Petitioner requests review and cancellation of Claims 1-36 as unpatentable based on the following grounds, supported by a declaration from Dr. Bruce Smith. Ex-1002, ¶¶1-354; Ex-1003.

Ground	Summary
1	Claims 1-3, 8, 11, 13-26, and 29-31 are obvious in view of Imoto (Ex-1007). ²
2	Claims 4-7, 10, 27, 28, and 32-36 are obvious over Imoto in view of Dudderar (Ex-1009).

² Ex-1008 is a copy of Imoto; Ex-1007 is a certified translation of Imoto.

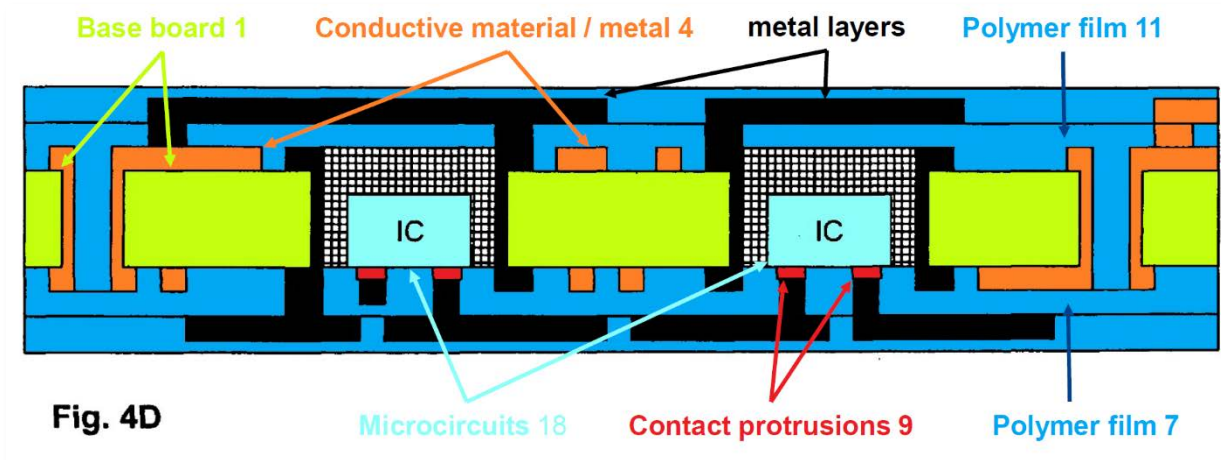
Ground	Summary
3	Claims 9 and 31 are obvious over Imoto in view of Mowatt (Ex-1010).
4	Claims 11 and 29 are obvious over Imoto in view of Lau (Ex-1011).
5	Claim 12 is obvious over Imoto in view of Lehmann (Ex-1012).
6	Claims 1-3, 8, 11, 13-26, and 29-31 are obvious in view of Kurita (Ex-1013).
7	Claims 4-7, 10, 27, 28, and 32-36 are obvious over Kurita in view of Dudderar.
8	Claims 9, 12, and 31 are obvious over Kurita in view of Mowatt.

IV. THE CHALLENGED PATENT

A. The '944 Patent

The challenged claims are apparatus claims directed to Figure 4D, which shows microcircuits 18 (labeled “IC”) in baseboard 1.³ Ex-1001, 9:43-14:3.

³ Throughout this Petition, all colors other than black are added to figures.



The '944 Patent describes surrounding microcircuits 18 with metal to shield them from electromagnetic interference (EMI). Ex-1001, 8:34-35, 64-66. The '944 Patent describes “metal foil” on the microcircuits’ sides and bottom and a “metal plate”⁴ on top. Ex-1001, 9:10-20.

B. Prosecution History of the '944 Patent

The '944 Patent was filed July 25, 2007, as a continuation of Application No. 10/502,336 (now, the '529 Patent), claiming priority to PCT/FI03/00065 (January 28, 2003), and further to Finish Patent No. 20020191 (January 31, 2002).

This Petition presents new arguments not considered during prosecution. The prior art in this Petition was not before the PTO during prosecution, with one exception, Mowatt. Ex-1001, p. 2. After allowance, Applicant filed a petition to withdraw the application from issue to submit 18 references, including Mowatt.

⁴ The claim term “metal plate” is used in the specification in only three instances—in each case, to refer to the metal *above* microcircuit 18. Ex-1001, 9:11, 38, 39-40.

Ex-1004, 0120-28. The Examiner granted the petition and signed the IDS, without any indication that the Examiner meaningfully considered Mowatt. Ex-1004, 0149. The Examiner did not apply Mowatt or any of the late-submitted prior art to the claims being examined. The record is silent on the examiner's view (if any) of Mowatt. The Examiner materially erred in failing to apply Mowatt to, at least, Claims 9, 12, and 31, since Mowatt teaches the added features of these dependent claims. *See infra* §§ VII.C and VII.H.

The Board should decline to exercise its discretion to deny institution under § 325(d). *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential).

C. Level of Ordinary Skill in the Art

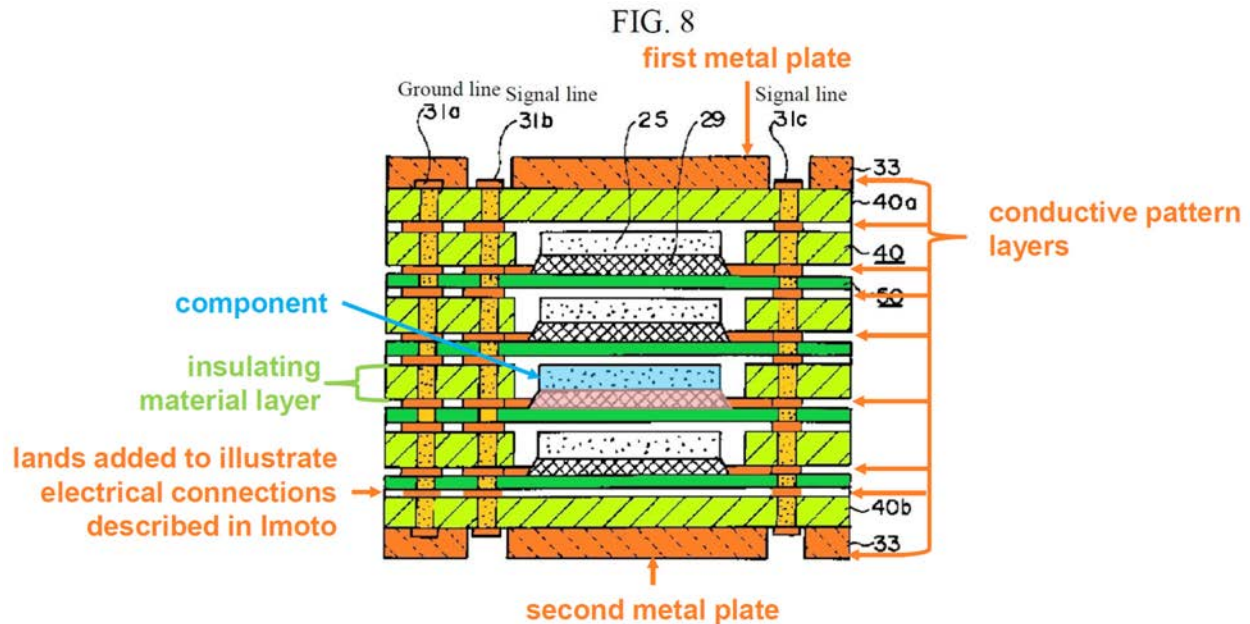
A person of ordinary skill in the art at the relevant time (“POSITA”) would have had a bachelor's degree in electrical engineering, material science, applied physics, or a related field, and at least three years of experience in the research, design, development, or testing of circuit board or microcircuit components, or the equivalent, with additional education substituting for experience and vice versa. Ex-1002, ¶¶26-30.

V. THE PRIOR ART

A. Imoto

Imoto was published March 16, 2001, and is §102(b) prior art.

Imoto discloses a component (semiconductor 25) embedded in an insulating layer with conductive pattern layers, as shown below in Figure 8. Ex-1007, ¶0021.



Above and below the component, a metal plate (metal film 33) is grounded and acts as a shield. Ex-1007, ¶0022. Imoto describes metal films 33 as electrically connected to ground through electrode 31a. *Id.* Based on this description, a POSITA would have understood that lands shaded orange on bottom laminated plate 40b are present, even though not depicted in Figure 8.⁵ Ex-1002, ¶45; see also Ex-1013, ¶0012 (describing laminated plate 20(b) as including lands 3), Figs. 2b and 4a (showing lands 3 above laminated plates 20).

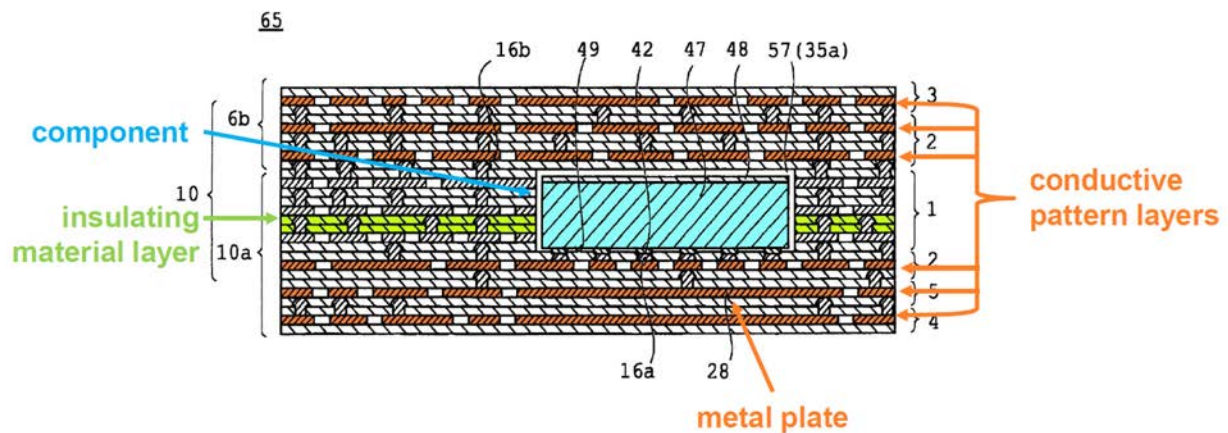
⁵ These same lands are added to the Figure 8 illustrations throughout this petition.

B. Kurita

Kurita is §102(e) prior art as of its U.S. filing date (July 7, 2000).

Kurita discloses a component (semiconductor device 47) embedded in multilayer substrate, as shown below in Figure 7. Ex-1013, 12:16-17.

FIG. 7

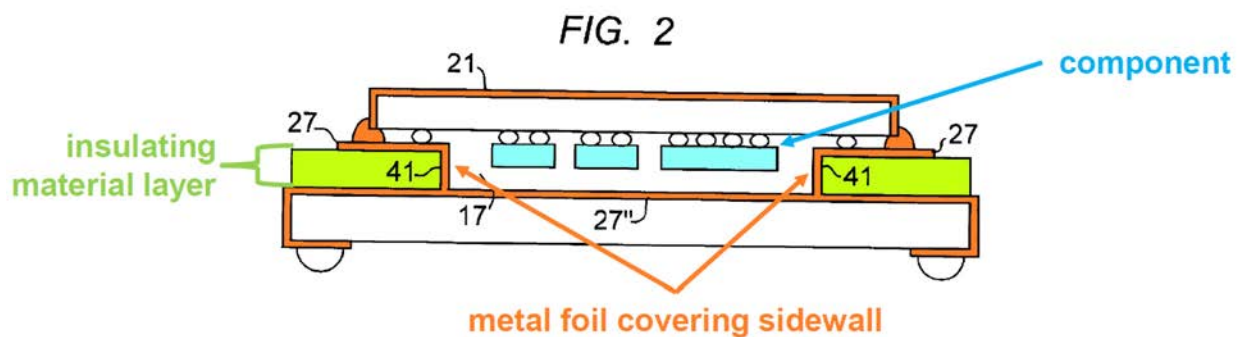


In other figures, the insulating layer is resin film 25, and the conductive pattern layers are wiring films 15. Ex-1013, 6:51-64, 7:25-27. A metal plate (shield section 28) acts as a shield below the component in Figure 7, but Kurita states the shield is most effective if on “both sides” of semiconductor device 47. *Id.*, 12:8-15, 12:40-50.

C. Dudderar

Dudderar was published October 2, 2001, and is §102(b) prior art. Dudderar incorporates by reference Degani (published March 4, 1997 and §102(b) prior art). Ex-1009, 2:15-28.

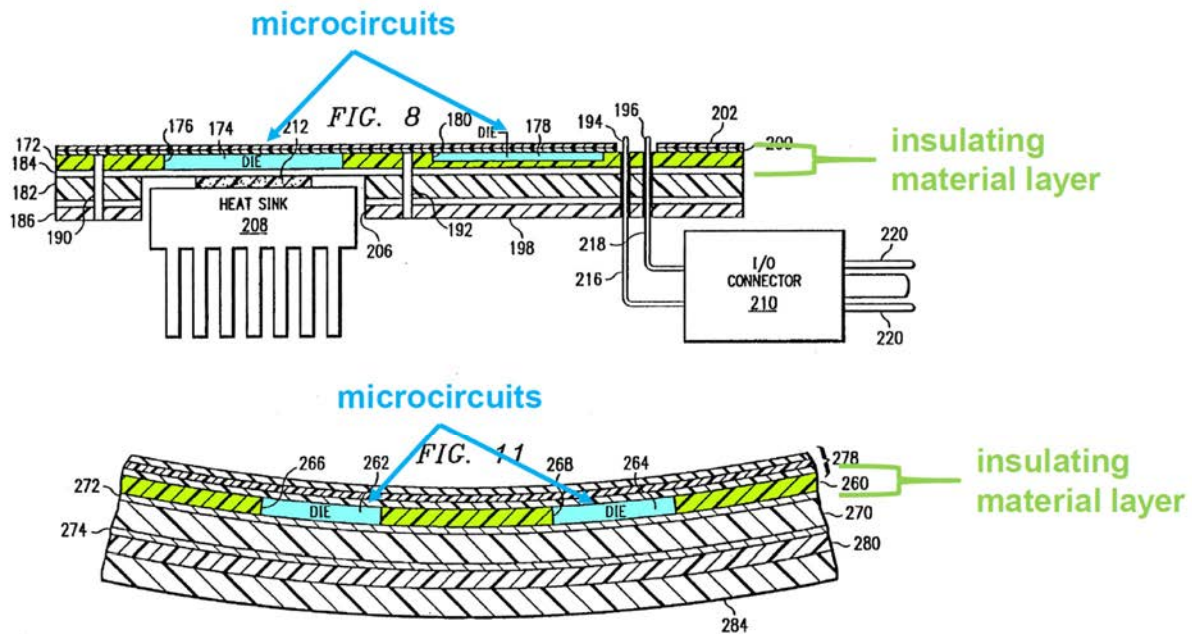
Dudderar discloses embedding semiconductors within a cavity of a printed circuit board surrounded by grounded metallization acting as a shield. Ex-1009, 2:53-54, 2:63-3:3. To enhance the shielding, Dudderar describes extending that metallization to the inside walls of the cavity, as shown below in Figure 2. *Id.*, 4:45-50.



D. Mowatt

Mowatt was published April 26, 1994, and is §102(b) prior art.

Mowatt also describes embedding semiconductors within a circuit board. Ex-1010, 9:40-43. Mowatt discloses two microcircuits inside the same insulating material layer, as shown below in Figures 8 and 11. *Id.*, 9:40-43, 11:58-59.



E. Lau

Lau was published in 2000 and is §102(b) prior art.

Lau describes implementation details for flip-chips, including the use of electroplated copper for the connections between flip-chips and boards. Ex-1011, 44, 47-48, 159-61, 186-87.

F. Lehmann

Lehmann was published in 1998 and is §102(b) prior art.

Lehmann describes directly attaching a chip to a substrate with solder balls and use of epoxy underfill resin to protect chip interconnections. Ex-1012, 266.

VI. CLAIM CONSTRUCTION

Petitioner interprets the claims according to *Phillips*. 37 C.F.R. § 42.100(b). To resolve this Petition, Petitioner does not believe that any term requires construction.⁶

VII. DETAILED EXPLANATION OF THE GROUNDS

A. Ground 1: Claims 1-3, 8, 11, 13-26, and 29-31 are rendered obvious by Imoto.

1. Independent Claims 1

a. Element 1[preamble]: A circuit board comprising

Imoto teaches the preamble, to the extent it is limiting. Ex-1002, ¶¶65-68. Imoto teaches a “plurality of wiring substrates” with conductive wiring patterns and vias, as illustrated in Figures 1 and 8. Ex-1007, ¶¶0004-0006, 0011, 0021-22.

⁶ Petitioner reserves all rights to raise claim construction and other arguments in district court. Additionally, Petitioner will request leave to submit the district court’s claim construction as soon as it becomes available.

FIG. 1

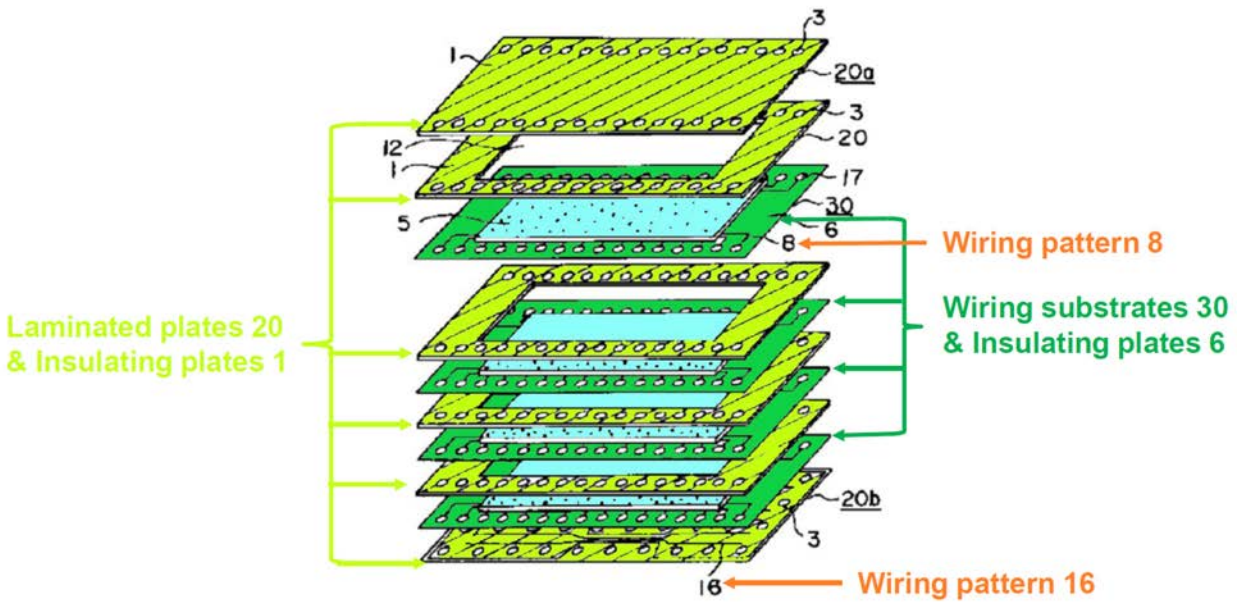
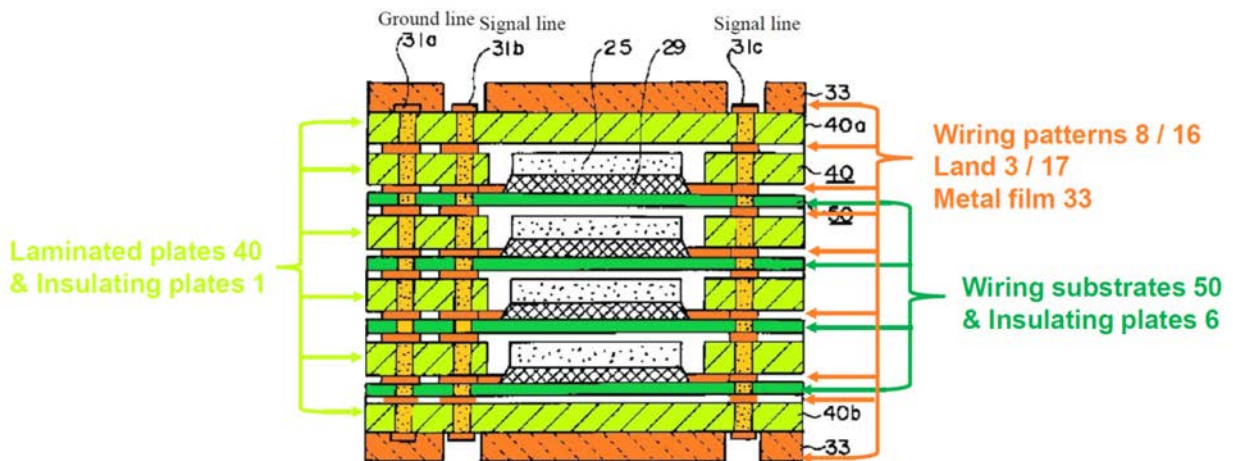


FIG. 8



Similarly, the base material of laminated plates 20/40 and wiring substrates 30/50 in Imoto is an insulator (insulating plates 1 and 6), just like the circuit boards in the '944 Patent (Ex-1001, 1:26-27). Ex-1007, ¶¶0011, 0015-16; Ex-1002, ¶67. To the

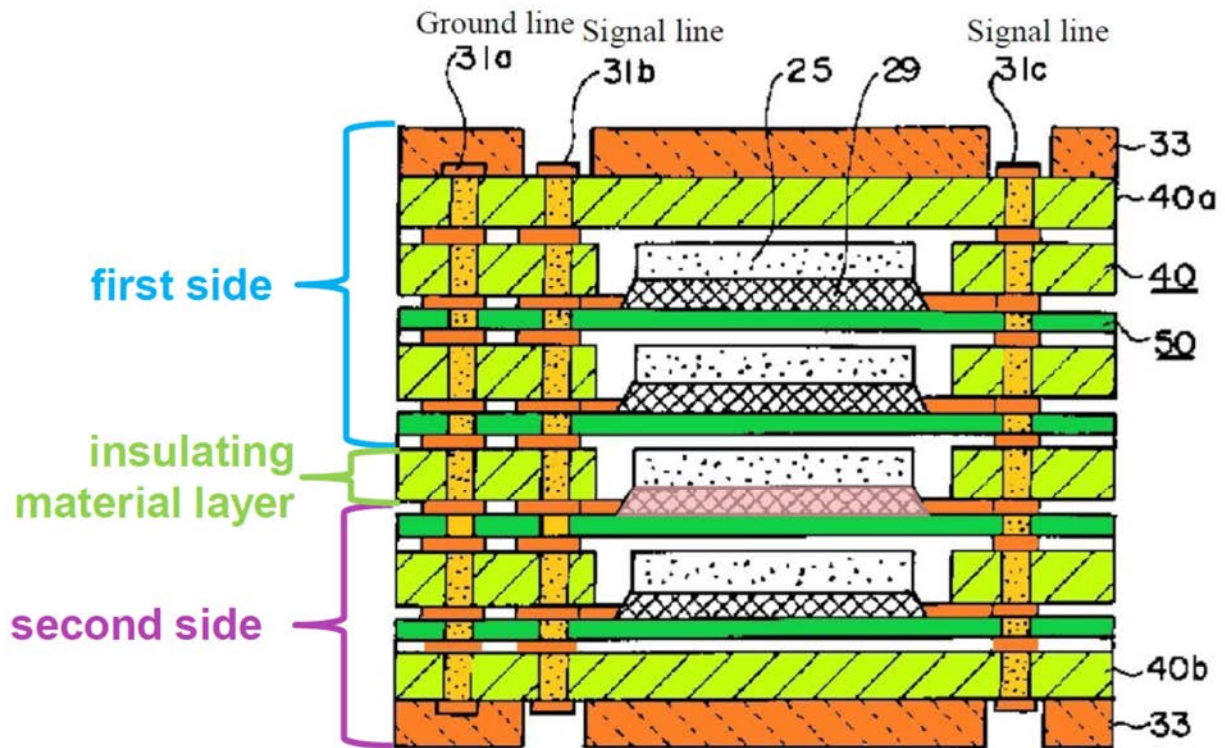
extent PO contends the preamble is limiting and Imoto does not teach a circuit board, it would have been obvious to a POSITA apply the teachings of Imoto to a circuit board. Ex-1002, ¶68. For example, Japanese Patent No. P3207174 (Hayashi) teaches embedding semiconductors into gap portions of the same or different layers of a multilayer wiring board. Ex-1018, ¶¶0027, 0032. Thus, it would have been obvious to apply Imoto's teaching to a circuit board.

b. Element 1[a]: an insulating material layer having a first side and a second side

Imoto discloses Element 1[a]. Ex-1002, ¶¶69-71.

Imoto discloses an insulating material layer with a first and second side, as shown below in Figure 8. *Id.*

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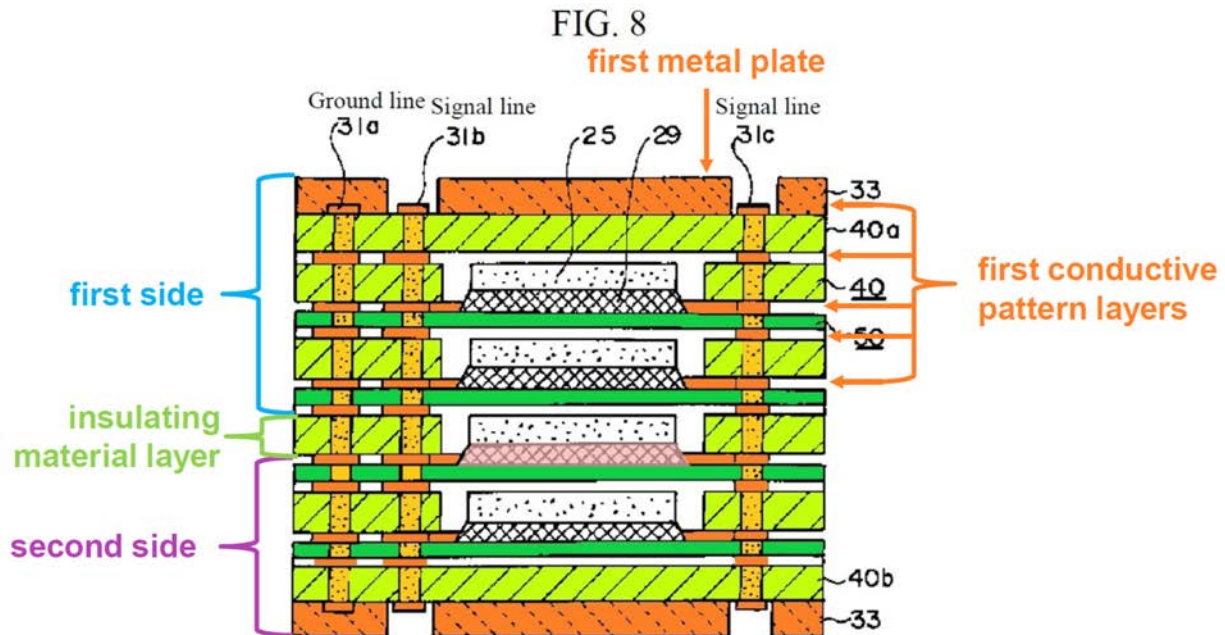
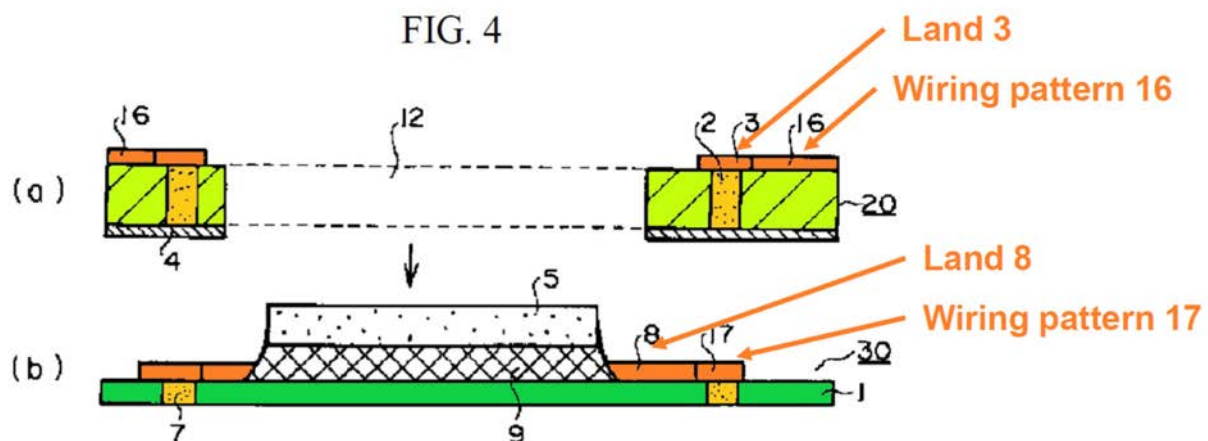
The insulating material layer includes laminated plate 20/40 which is insulating.

Ex-1007, ¶¶0011, 0015, 0016; Ex-1002, ¶71.

- c. Element 1[b]: at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate**

Imoto discloses Element 1[b]. Ex-1002, ¶¶72-75.

The first conductive pattern layers in Figure 8 are wiring patterns 8/16, lands 3/17, and metal film 33 (all, dark orange) above the insulating material layer, as shown below.⁷ Ex-1002, ¶73.



7 Elements 1[b] and 1[c] require that the conductive pattern layers are on “sides” of insulating material layer as opposed to its “surface” (a term used in Elements 1[d] and 1[e]). Thus, the conductive pattern layers may be above or below the surfaces of the insulating material layer as shown in Figures 4C and 4D of the '944 Patent.

Each laminated plate 20/40 (light green) includes copper foil patterned to form land 3 and wiring pattern 16, and each wiring substrate 30/50 (dark green) includes copper foil patterned to form land 17 and wiring pattern 8, as illustrated in Figure 4 above. Ex-1007, ¶¶0011, 0015-16 (describing these features with reference to Figures 1-5⁸).

In Figure 8, metal film 33 on top laminated plate 40a is the claimed “first conductive pattern layer[] defining a first metal plate.” Ex-1007, ¶0022; Ex-1002, ¶75. Metal film 33 is patterned to connect with ground electrode 31a but not signal electrodes 31b and 31c. Ex-1007, ¶0022. Like the metal plate in the ’944 Patent (Ex-1001, 9:30-41), metal film 33 in Imoto “has a shielding effect when connected to the ground line.” *Id.*, ¶0022.

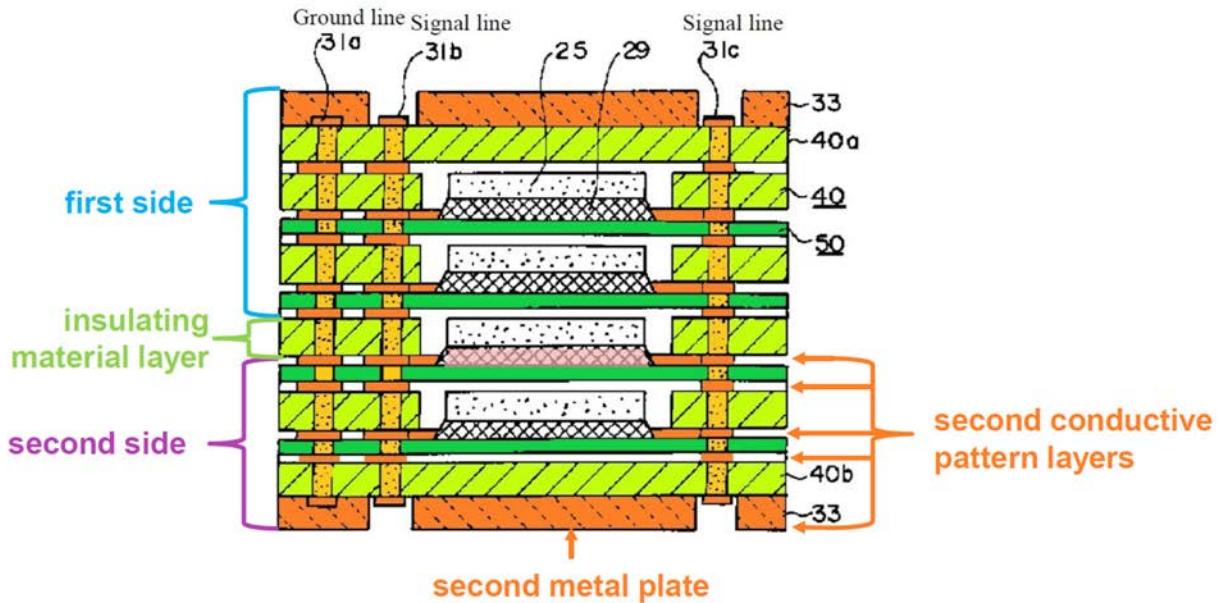
d. Element 1[c]: at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate

Imoto discloses Element 1[c]. Ex-1002, ¶¶76-78.

As shown below, the second conductive pattern layers in Figure 8 are the same features discussed above (wiring patterns 8/16, lands 3/17, and metal film 33) but below the insulating material layer. Ex-1002, ¶77.

⁸ In Figures 2(a), 3(a), 3(b), and 4(b), the reference numbers for insulating plates 1 and 6 are reversed. Ex-1002, ¶27 n.7.

FIG. 8

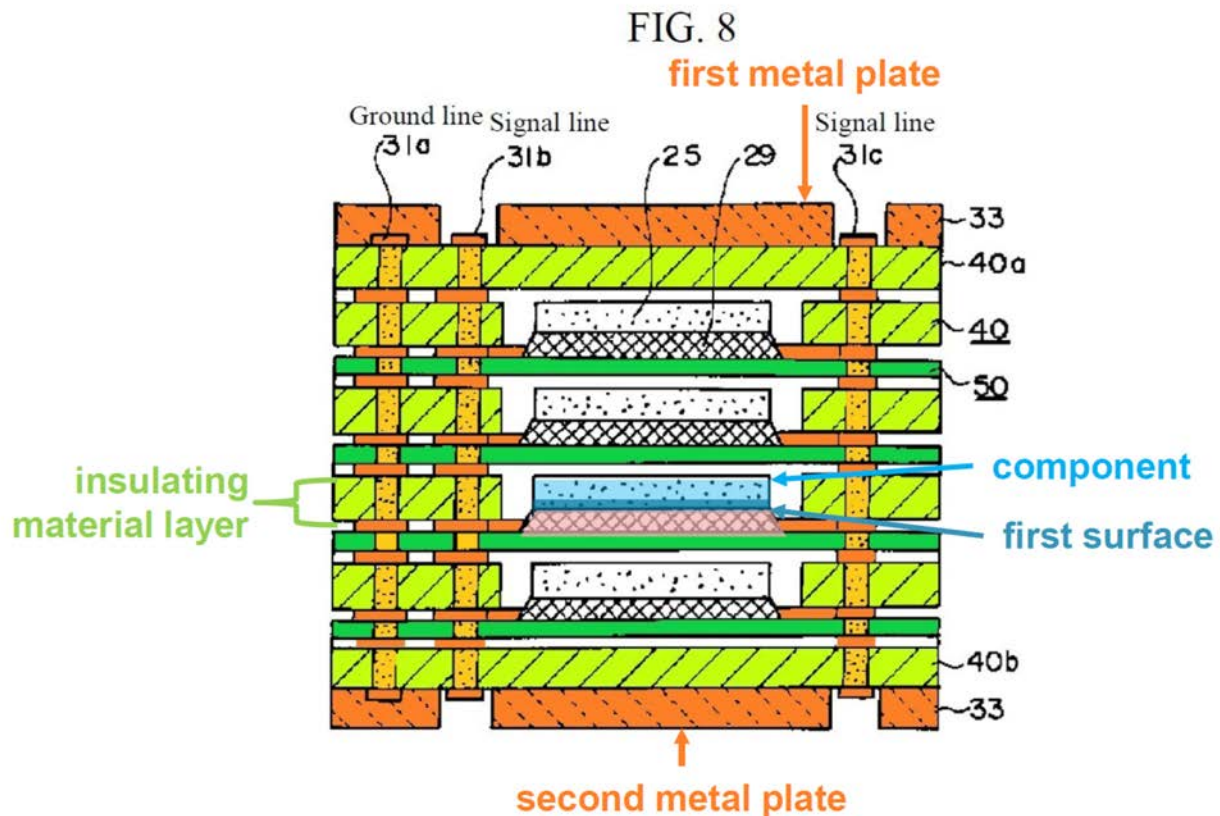


Metal film 33 on bottom laminated plate 40b is the claimed “second conductive pattern layer[] defining a second metal plate” for the same reasons that metal film 33 on top is the first metal plate (§VII.A.1.c). Ex-1002, ¶78.

- e. **Element 1[d]: a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface**

Imoto discloses and renders obvious Element 1[d]. Ex-1002, ¶¶79-81.

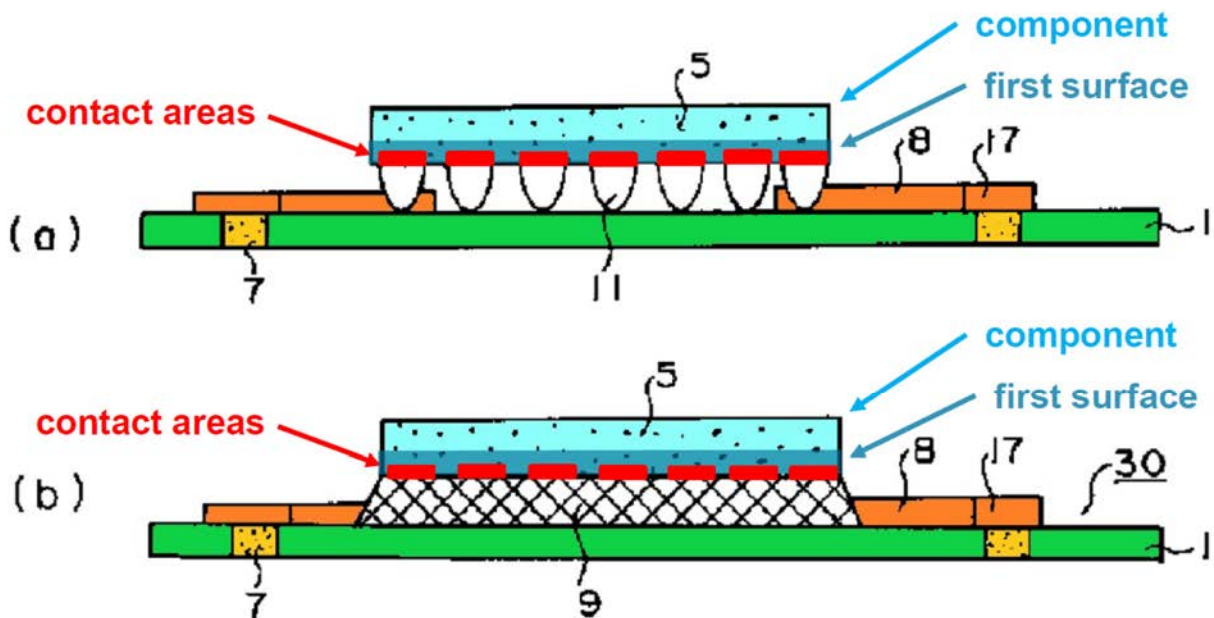
The component is semiconductor element 25 (light blue), which is inside the insulating material layer and between the first and second metal plates as shown below. Ex-1007, ¶0021; Ex-1002, ¶80.



The first surface (dark blue bottom) of semiconductor element 25 faces the second metal plate, as shown above. Ex-1002, ¶80.

Imoto states, “In order to mount the semiconductor element 5 on the wiring substrate 30, connection terminals 11 such as a solder ball or the like are connected to the wiring pattern 8.” Ex-1007, ¶0016. A POSITA would have understood, or at least have considered it obvious, that connection terminals 11 would be electrically connected to contact areas on the first surface of semiconductor component 5/25. Ex-1002, ¶81. The following Figure 3 (and later version of the same figure) shows contact areas (red), although not depicted in the original Figure. *Id.*

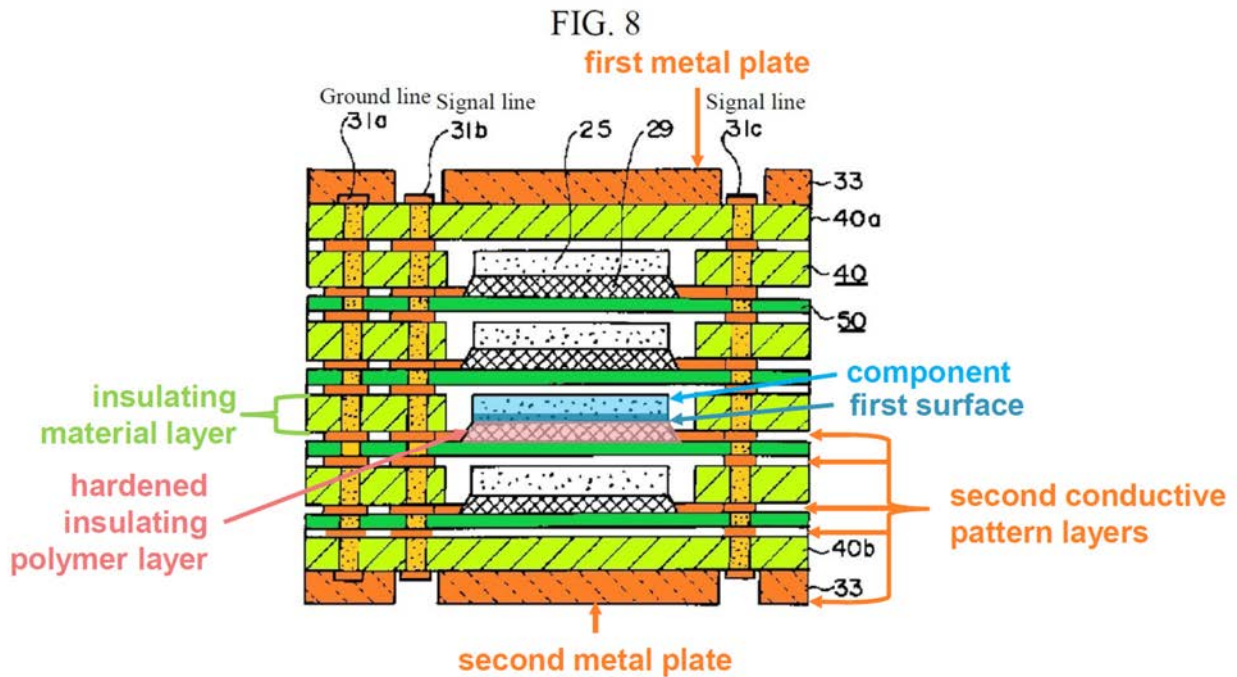
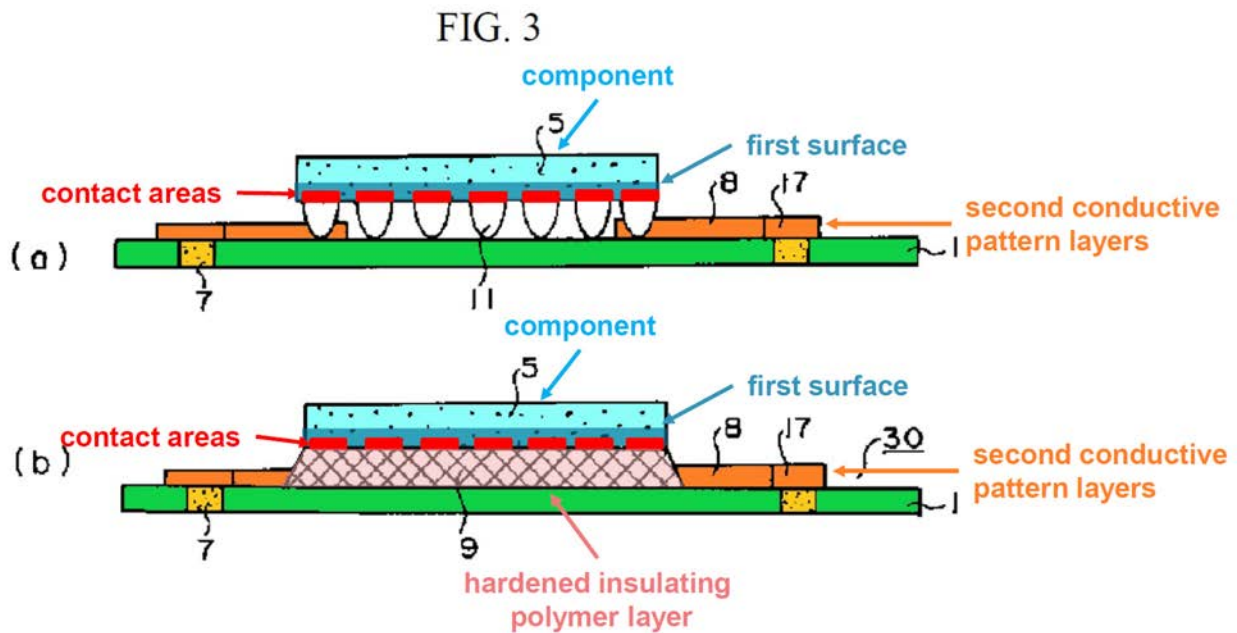
FIG. 3



- f. **Element 1[e]: a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and**

Imoto discloses Element 1[e]. Ex-1002, ¶¶82-87.

The hardened insulating polymer layer is underfill resin 9/29 (pink), which is located between the first surface of semiconductor component 5/25 (blue) and at least one second conductive pattern layer, as shown below. Ex-1002, ¶83.



Underfill resin 9/29 is an insulating polymer that is thermally cured (*i.e.*, hardened) to protect connection terminal 11. Ex-1007, ¶10016. Ex-1002, ¶¶85-87;

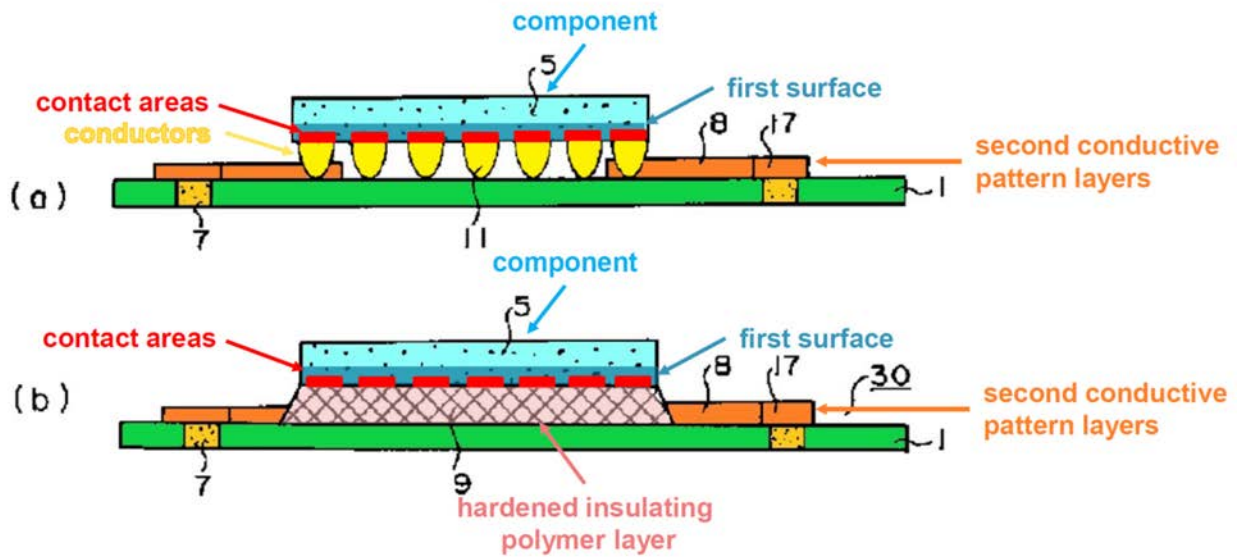
Ex-1016, 1. Imoto describes applying a “curing temperature” to the entire structure (including underfill resin 9/29). Ex-1007, ¶0016. A POSITA would have understood that this curing temperature causes underfill resin 9/29 to harden to form a hardened insulating polymer layer between the first surface of component 5/25 and wiring pattern 8 of the second conductive pattern layers. Ex-1002, ¶87.

- g. Element 1[f]: contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one second conductive pattern layer or layers**

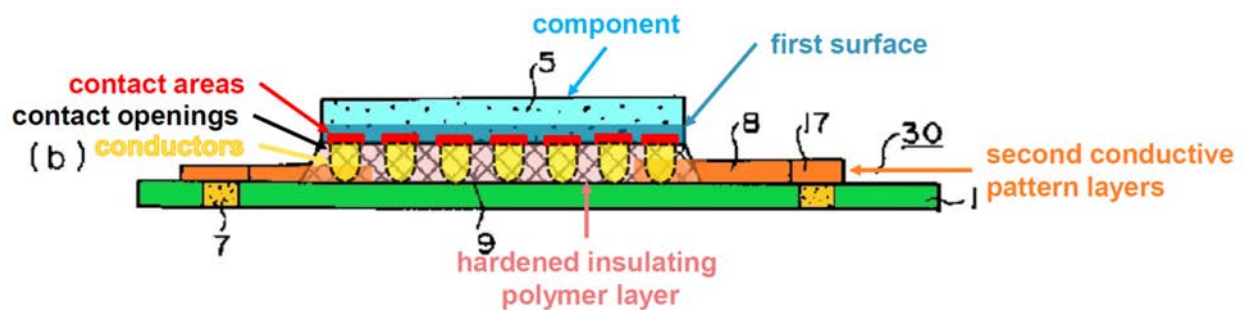
Imoto discloses Element 1[f]. Ex-1002, ¶¶88-91.

In Imoto, the conductors in the contact openings are connection terminals 11 in openings of underfill resin 9/29 (the hardened insulating polymer layer). Figure 3(a) below shows connection terminals 11 (yellow) forming electrical contact between the contact areas of the semiconductor component 5/25 and wiring pattern 8. Ex-1007, ¶0016; Ex-1002, ¶89.

FIG. 3



Above, Figure 3(b) illustrates underfill resin 9/29 which surrounds and protects terminals 11. Ex-1007, ¶0016; Ex-1002, ¶90. The below modified version figure shows connection terminals 11 (which are hidden from view by underfill 9/29 in Figure 3(b)) connected to wiring pattern 8. Ex-1002, ¶90.

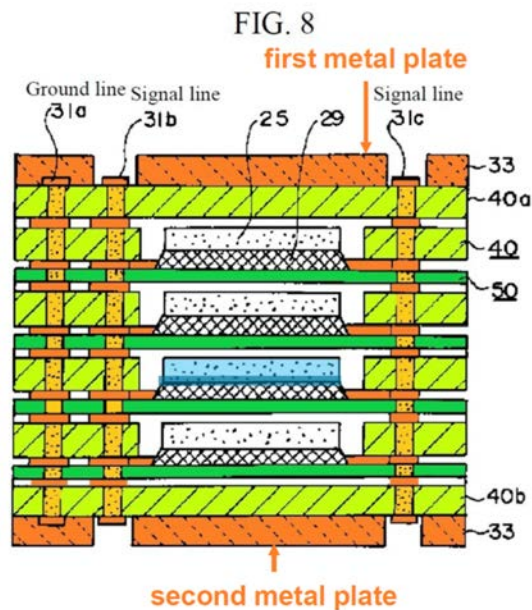


The dotted outlines of terminals 11 are the openings in the hardened insulating polymer layer. Ex-1002, ¶91. In those openings, connection terminals 11 (yellow) are conductors forming electrical contact between the contact areas of

semiconductor component 5/25 and wiring pattern 8 (the claimed “at least one second conductive pattern layer or layers”). *Id.*

2. Dependent Claim 2: The circuit board of claim 1, wherein the first and second metal plates are electrically connected to each other.

Imoto discloses Claim 2. Ex-1002, ¶¶92-93. In Imoto, each metal film 33 (the first and second metal plates) is connected to electrode 31a, which connects both metal films 33 to ground. Ex-1007, ¶0022. Thus, metal films 33 are electrically connected to each other through electrode 31a, as shown in Figure 8 below. Ex-1002, ¶93.



3. Dependent Claim 3: The circuit board of claim 1, wherein the first and second metal plates are electrically connected to an earth connection of the circuit board.

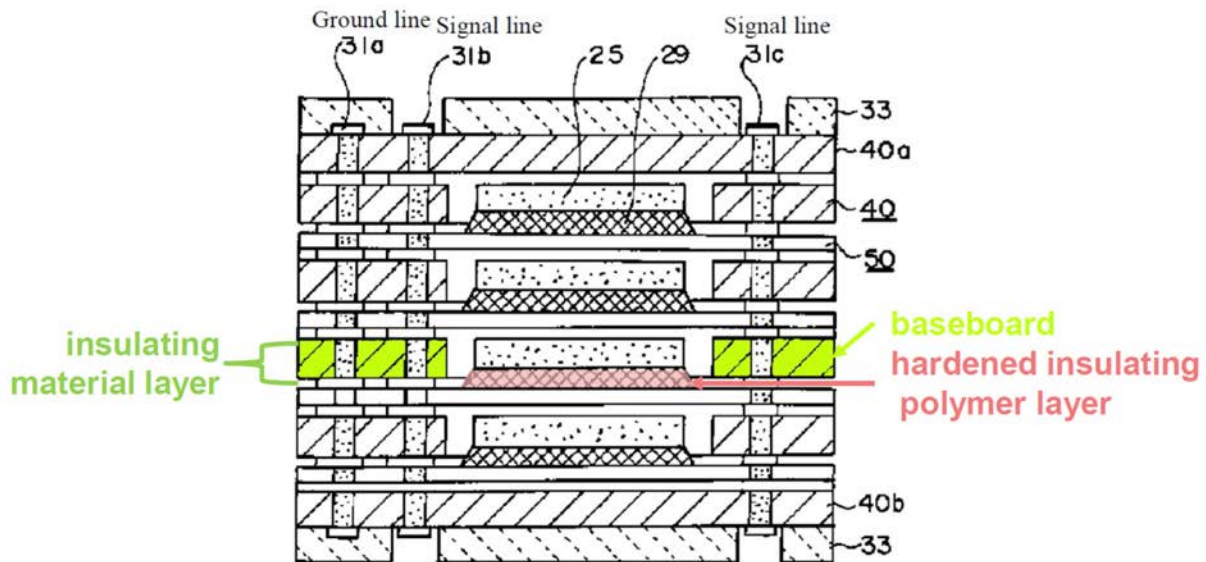
Imoto discloses Claim 3. Ex-1002, ¶¶94-96. As described for Claim 2 (§VII.A.2), metal films 33 are electrically connected to each other through connection electrode 31(a) and to ground, which a POSITA would have understood as the claimed “earth connection” of the circuit board. Ex-1007, ¶0022; Ex-1002, ¶¶95-96; Ex-1015, 328, 461, 467.

4. Dependent Claim 8: The circuit board of claim 1, wherein the insulating material layer includes a baseboard and the hardened insulating polymer layer.

Imoto discloses Claim 8. Ex-1002, ¶¶97-100.

As described for Element 1[a] (§VII.A.1.b) and Element 1[e] (§VII.A.1.f), the insulating material layer includes laminated plate 20/40 (light green) and underfill resin 9/29(pink), which are the claimed baseboard and hardened insulating polymer layer as shown below. Ex-1002, ¶99.

FIG. 8



The '944 Patent defines baseboard broadly as encompassing organic or inorganic materials. Ex-1001, 3:46-55; Ex-1002, ¶¶99. Thus, a POSITA would have considered Imoto's polyimide substrate 40 (an organic material) a baseboard. Ex-1007, ¶¶0011, 0015; Ex-1002, ¶¶99.

5. Dependent Claim 11: The circuit board of claim 1, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.

Imoto discloses or renders obvious Claim 11. Ex-1002, ¶¶101-104.

Imoto states, "[S]emiconductor element (chip) 5 is die-bonded and mounted on the wiring substrate 30 using a flip chip method or the like. In order to mount the semiconductor element 5 on the wiring substrate 30, connection terminals 11 such as a solder ball or the like are connected to the wiring pattern 8." Ex-1007, ¶¶0016.

It would have been obvious to a POSITA to implement copper wiring pattern 8, to which the semiconductor element 5 is die-bonded, as electrochemically deposited copper. Ex-1002, ¶¶103-104. For example, Imoto states that “the semiconductor element 5 is mounted [to] copper foil.” Ex-1007, ¶0016. Imoto also teaches “electroplating of copper.” Ex-1007, ¶0019; ¶0015 (“copper or gold plating”), ¶0016 (same). Such electroplated copper is “electrochemically deposited copper” as recited in Claim 11. Ex-1002, ¶103. Based on these teachings, a POSITA would have been motivated to implement copper wiring pattern 8, to which the semiconductor element 5 is die-bonded, by electroplating copper because electroplating is a reliable and efficient method of applying copper to a substrate. Ex-1002, ¶¶103. Thus, the conductors in the openings of underfill resin 9/29 (hardened insulating polymer layer) would include electrochemically deposited copper. *Id.*, ¶¶103-104.

6. Dependent Claim 13: The circuit board of claim 1, wherein the component is a microcircuit.

Imoto discloses Claim 13. Ex-1002, ¶¶105-107. As described for Element 1[d] (§VII.A.1.4), the claimed component is semiconductor element 25. Ex-1007, ¶¶0003, 0011, 0021. The '944 Patent does not define microcircuit, but a POSITA would have understood a microcircuit to encompass an integrated circuit, such as semiconductor chip 5/25. Ex-1002, ¶106; Ex-1015, 536-37, 652.

- 7. Dependent Claim 14: The circuit board of claim 1, comprising an electrically conducting feed-through between the conductive pattern layers on the both sides of the insulating material layer.**

Imoto discloses Claim 13. Ex-1002, ¶¶108-110.

As shown below, Figure 8 includes electrically conducting feed-throughs between the conductive pattern layers on both sides of the insulating material layer.

Ex-1002, ¶109.

FIG. 8

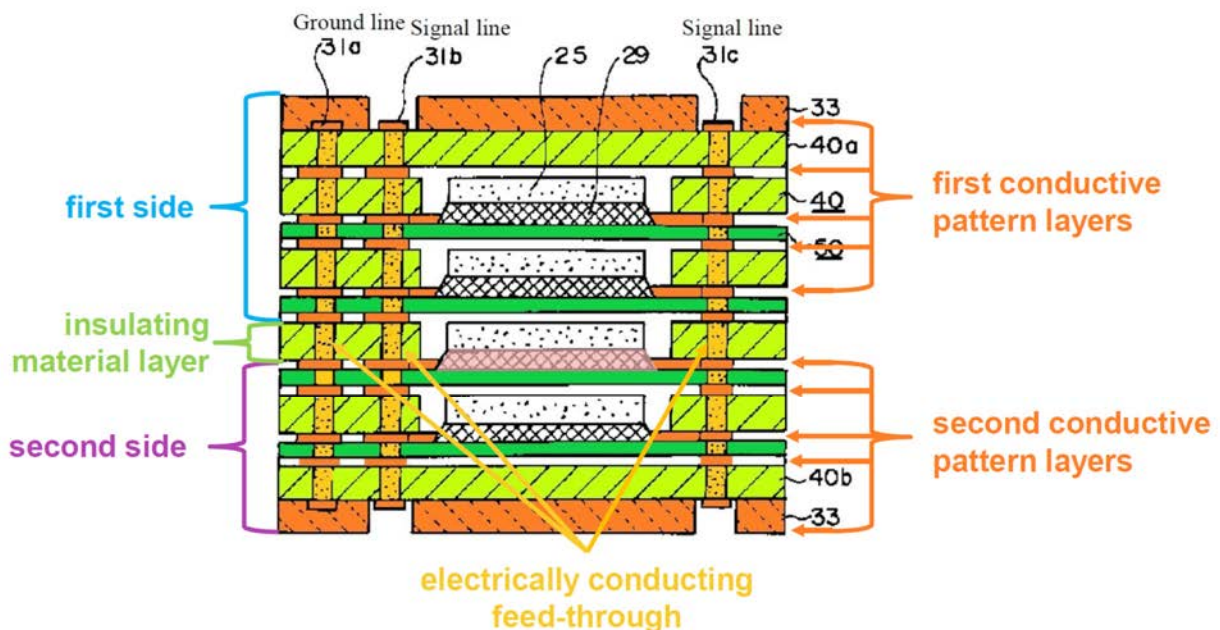


Figure 8 includes “connection electrode 31a that connects to the ground ... line, and connection electrodes 31b, 31c that connects to a signal line.” Ex-1007, ¶0022. Any

of connection electrodes⁹ 31a, 31b, or 31c discloses Claim 13. Ex-1002, ¶110; Ex-1007, ¶¶0011, 0015-16 (describing connection electrodes 2 and 7 in Figures 2-5).

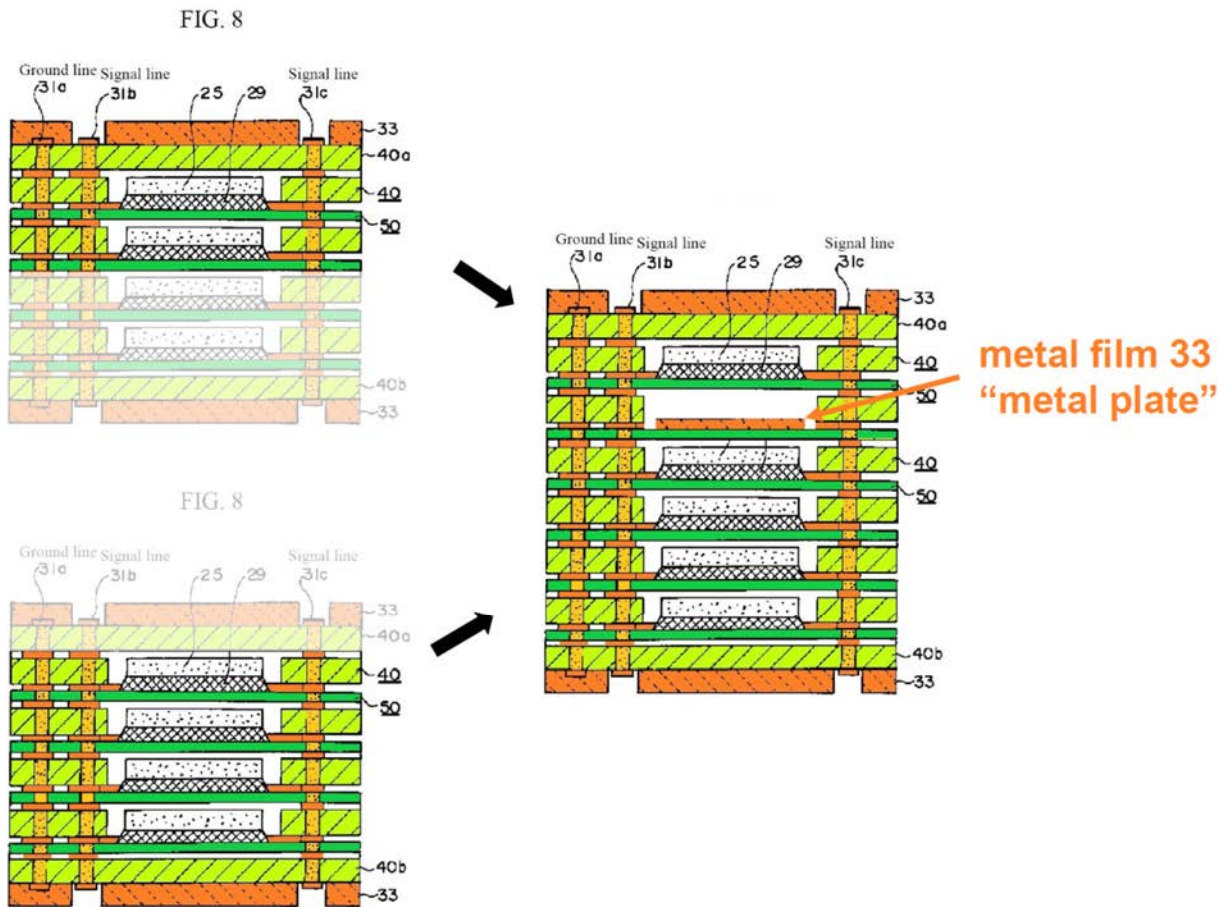
8. Independent Claim 15

Imoto renders obvious Claim 15. Ex-1002, ¶¶111-22.

Claim 15 is the same as Claim 1, except for the preamble. Claim 15 recites “a first circuit board substructure and second circuit board substructure on top of each other, wherein at least the first circuit board substructure comprises” the same Elements [a]-[f] as recited in Claim 1. Ex-1002, ¶112.

Imoto teaches the preamble of Claim 15, to the extent it is limiting. Ex-1002, ¶113. Imoto discloses a multilayer structure that includes any number of layers. Ex-1007, ¶0010; *see also* Claims 1, 2, 8 (reciting “a plurality of wiring substrates” and “a plurality of conductive via insulating substrates”). To form additional layers as taught in Imoto, it would have been obvious to a POSITA to stack layers of Figure 8 as shown below, to add functionality, reduce manufacturing cost, and save space. Ex-1002, ¶113.

⁹ Imoto uses “connection electrode” to refer to conductors embedded in the vias.

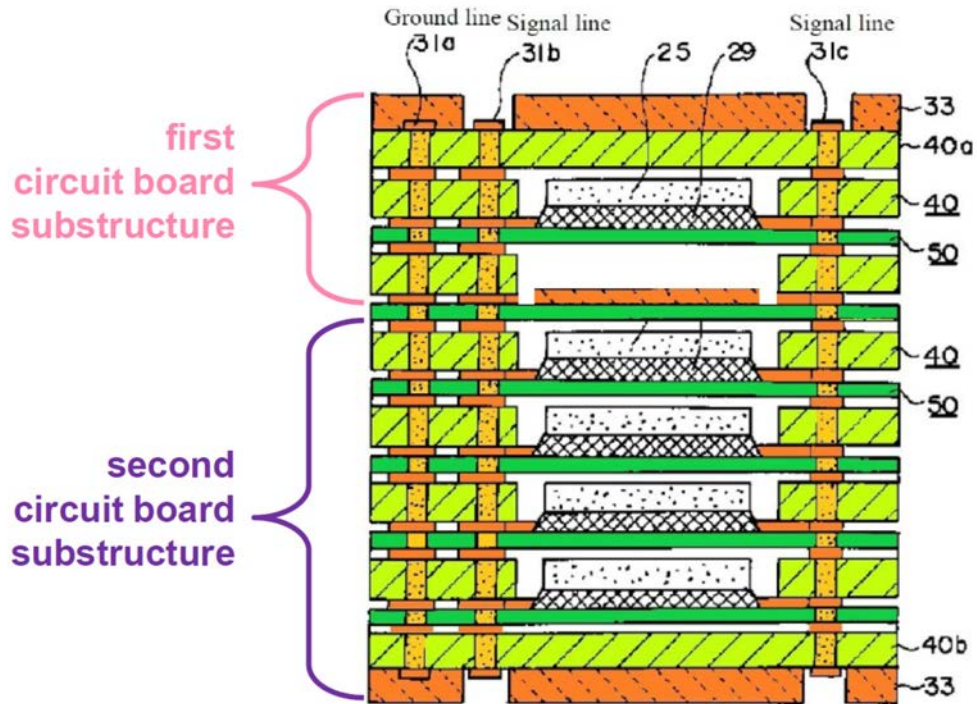


A POSITA would have been motivated to form metal film 33 in the middle of the stacked structure on laminated plate 50 (which would otherwise include semiconductor 25) because Imoto states that metal film 33 provides a “shielding effect.” Ex-1007, ¶0022; Ex-1002, ¶¶114-119. A POSITA would have understood that shielding is used to protect semiconductors 25 from EMI and that EMI can come from outside or internal sources (such as other semiconductors 25). Ex-1002, ¶114. Furthermore, the use of a shield between semiconductors 25 was well known in the art. Ex-1002, ¶¶116-118. For example, U.S. Patent No. 6,459,593 (“Kwong”) and

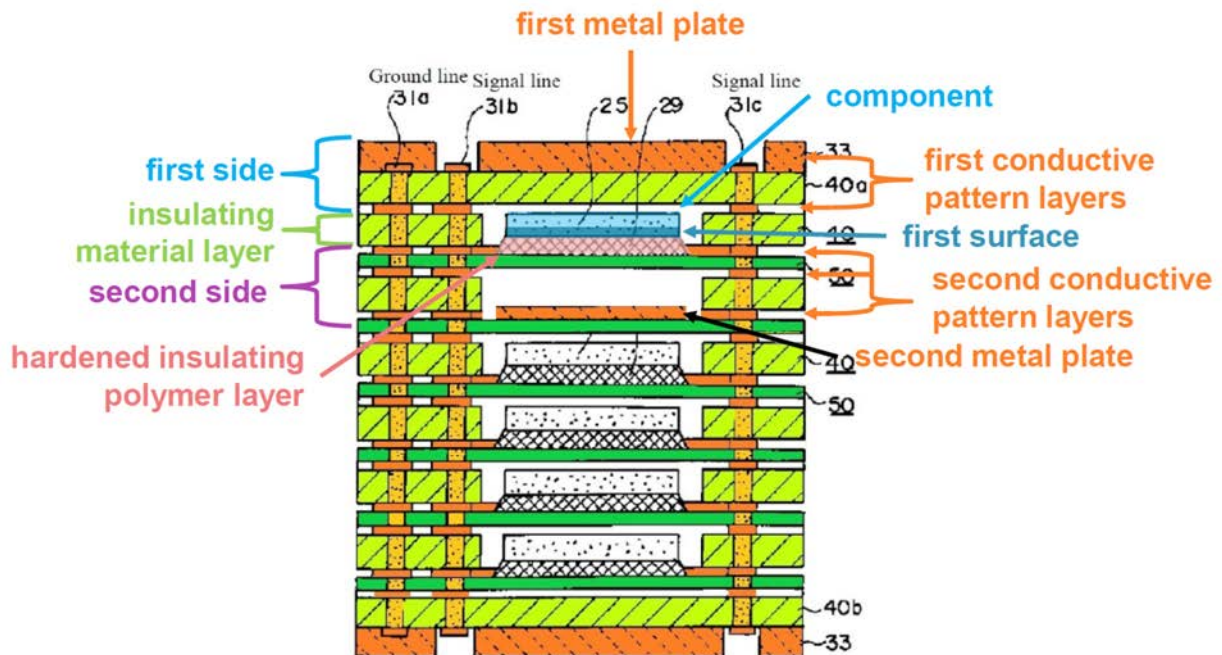
U.S. Patent Publication No. 2003/0090833 (“Asahi U.S. Publication”) teach a metal plate between semiconductors embedded in insulating layers. Ex-1020, 7:57-65; 8:35-41, 8:48-50 (describing shield plate 162 between components 156 and 158 in Figure 2); Ex 1025, ¶¶0089-92 (describing shield electrode 1010 in Figure 10 and electromagnetic shielding layer 1110 in Figure 11). Thus, a POSITA would have been motivated to include metal film 33 in the middle of the stacked structure to shield semiconductors 25 on either side of metal film 33 from interfering with one another. Ex-1002, ¶119.

A POSITA would have had a reasonable expectation of success in forming metal film 33 on laminated plate 30/50 in the middle of the structure. Ex-1002, ¶120. Metal film 33 is formed of “metal foil” (Ex-1007, ¶0022) like the wiring pattern 8 and land 17 on laminated plates 30/50 (*Id*, ¶¶0011, 0015). Furthermore, Imoto teaches to “adjust[] the material and thickness of the metal film...as need[ed].” *Id*, ¶0022.

The above stacked structure discloses Claim 15. Ex-1002, ¶121. The first circuit board substructure is above the second circuit board substructure, as shown below. *Id.*



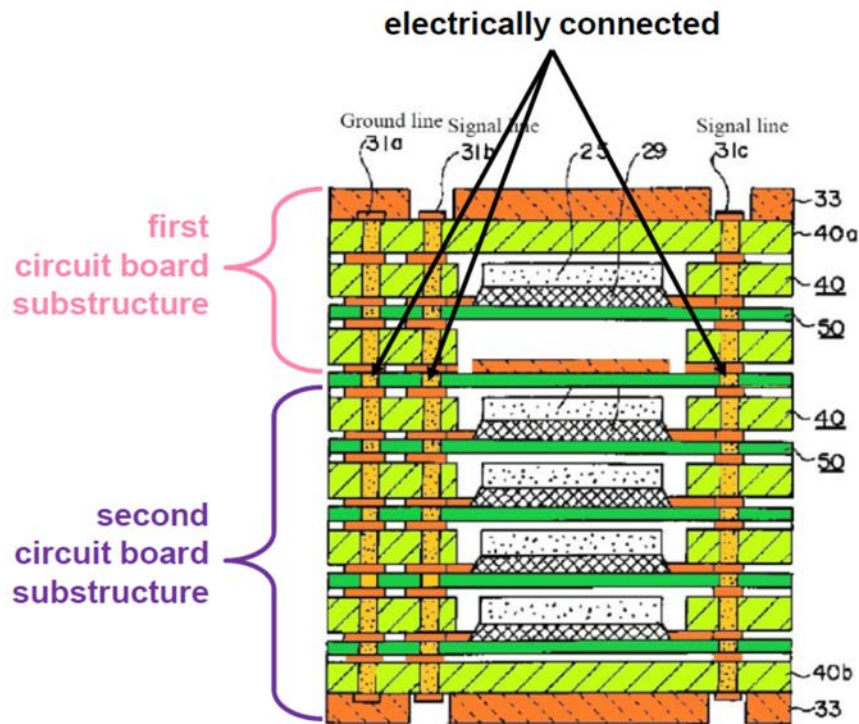
As shown below, the first circuit board substructure meets Elements 15[a]-15[f] as described for Elements 1[a]-1[f] (§VII.A.1). Ex-1002, ¶122.



- 9. Dependent Claim 16: The multi-layered circuit board of claim 15, wherein said first circuit board substructure and said second circuit board substructure are electrically connected to each other to form a multi-layered functioning totality.**

Imoto renders obvious Claim 16. Ex-1002, ¶¶123-124. As described for Claim 2 (§VII.A.2), metal films 33 are electrically connected to each other through electrode 31a and to ground. Ex-1007, ¶0022. Thus, the two circuit board substructures “are electrically connected to each other to form a multi-layered

functioning totality,” through at least connection electrodes 31a, 31b, and 31c as illustrated below. Ex-1002, ¶124.

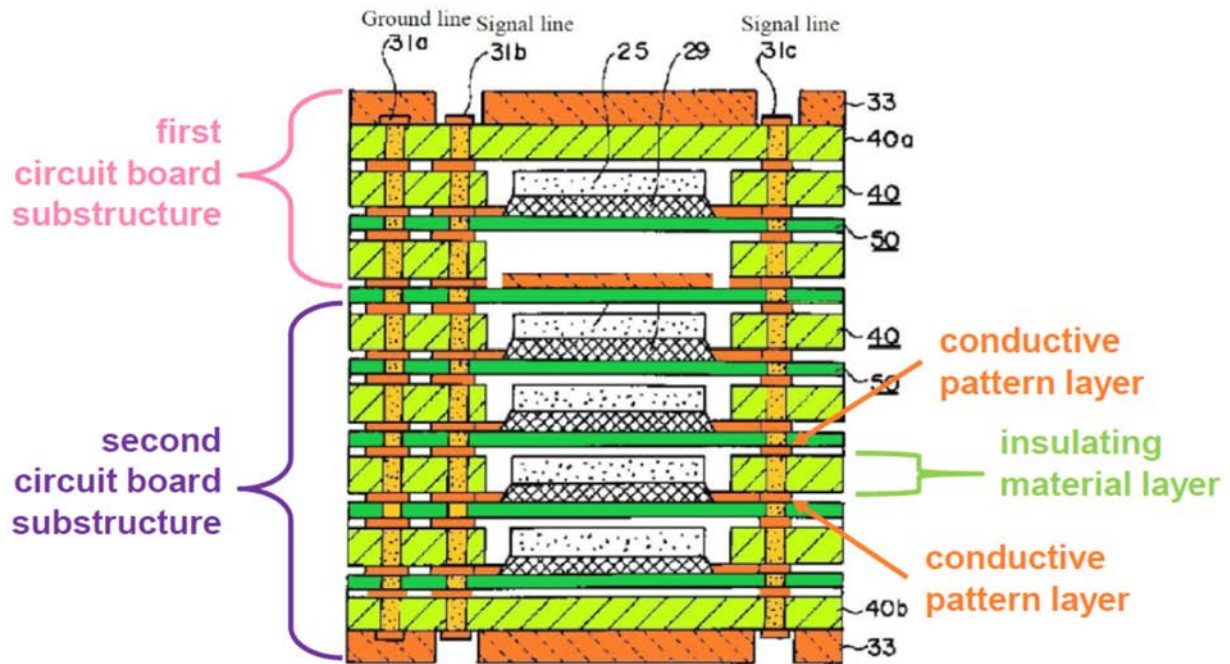


10. **Dependent Claim 17: The multi-layered circuit board of claim 16, wherein said second circuit board substructure comprises an insulating material layer and at least one conductive pattern layer in the insulating material layer.**

Imoto renders obvious Claim 17. Ex-1002, ¶¶125-126.

As shown below, the second circuit board substructure includes an insulating material layer and at least one conductive pattern layer in the insulating material

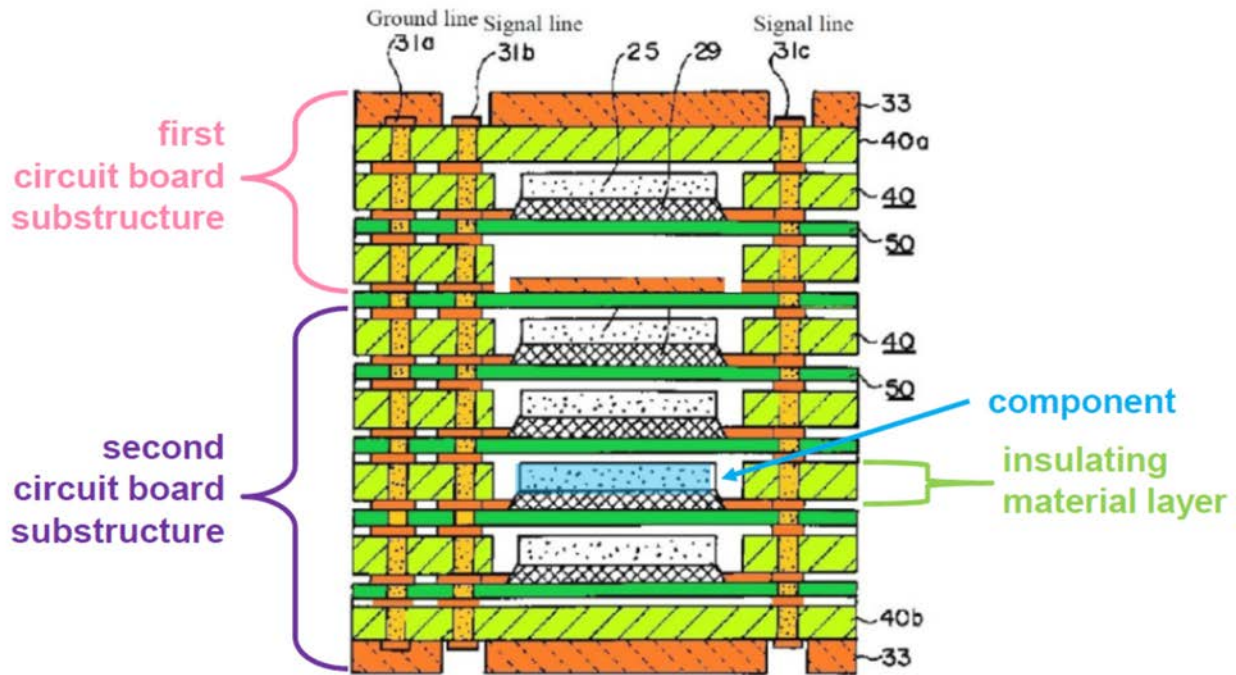
layer, for the reasons described for Element 1[a] (§VII.A.1.b) and Element 1[b] (§VII.A.1.c). Ex-1002, ¶126.



11. **Dependent Claim 18:** The multi-layered circuit board of claim 17, wherein said second circuit board substructure includes a component embedded in the insulating material layer.

Imoto renders obvious Claim 18. Ex-1002, ¶¶127-28

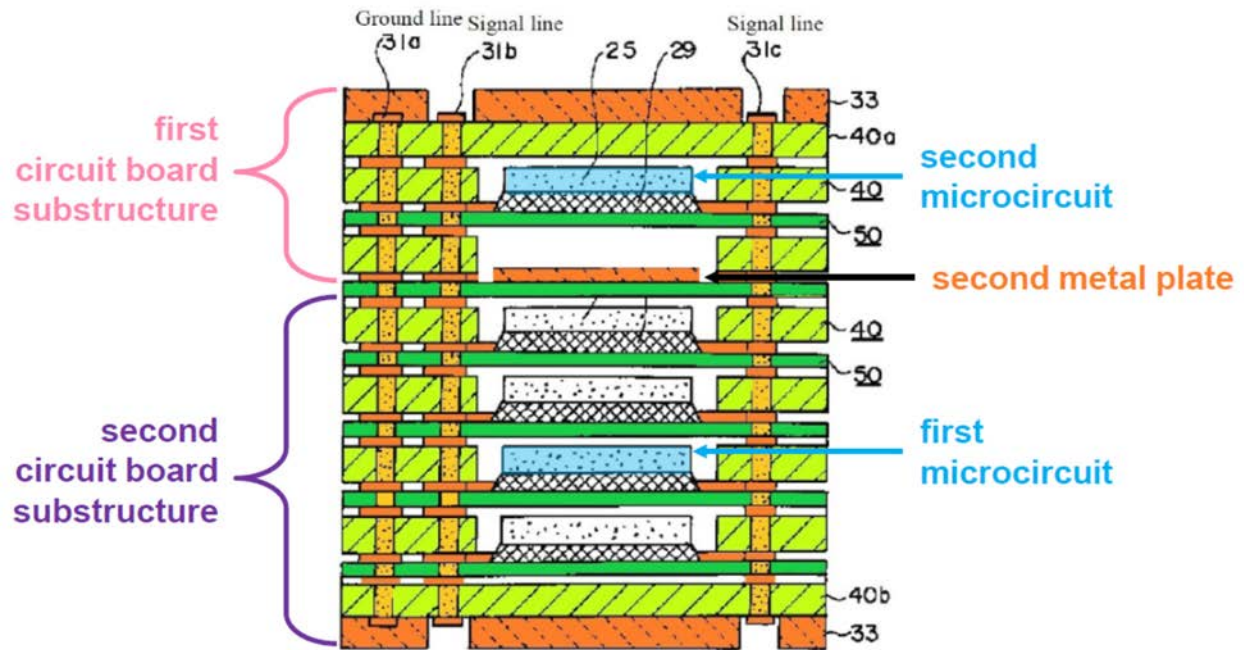
As shown below, the second circuit board substructure includes a component embedded in the insulating material layer, for the reasons described for Element 1[e] (§VII.A.1.f). Ex-1002, ¶128.



12. **Dependent Claim 19:** The multi-layered circuit board of claim 15, wherein said first circuit board substructure comprises a first microcircuit and said second circuit board substructure comprises a second microcircuit such that the first and second microcircuits are on top of each other and at least one of the first and second metal plates is located between said first and second microcircuits.

Imoto renders obvious Claim 19. Ex-1002, ¶¶129-31.

As shown below, the first circuit board substructure includes a first microcircuit, and the second circuit board substructure includes a second microcircuit on top of the first microcircuit. Ex-1002, ¶130. As described for Claim 15 (§VII.A.8), metal film 33 in the middle of the structure is the second plate, which is located between the two microcircuits. *Id.*

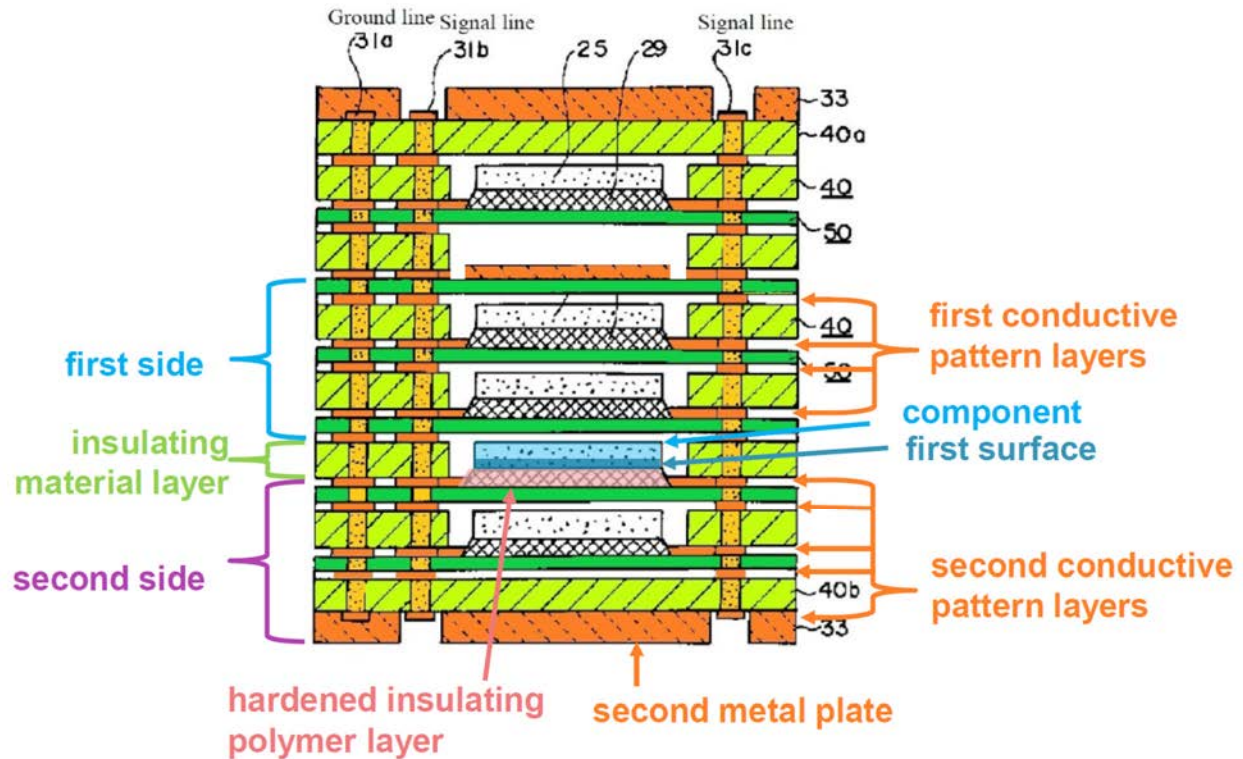


13. Dependent Claim 20

Imoto renders obvious Claim 20. Ex-1002, ¶¶132-34.

Claim 20 requires that the second circuit board substructure include Elements 1[a]-1[f] of Claim 1, except the **first** metal plate. Compare Elements 20[a]-[f] with Elements 1[a]-[f]; Ex-1002, ¶133.

As shown below, the second circuit board substructure meets Elements 20[a]-20[f] as described for Elements 1[a]-1[f] (§VII.A.1). Ex-1002, ¶134. .

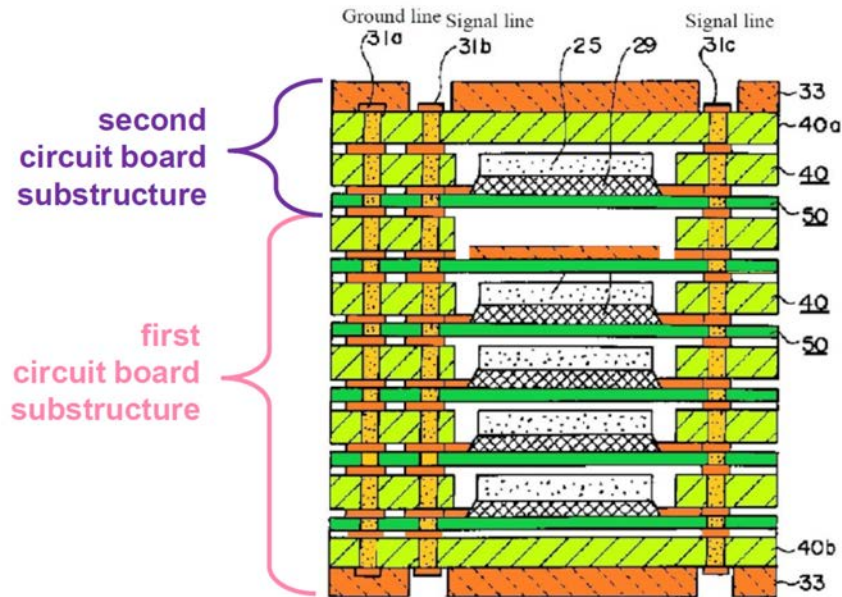


14. Dependent Claim 21

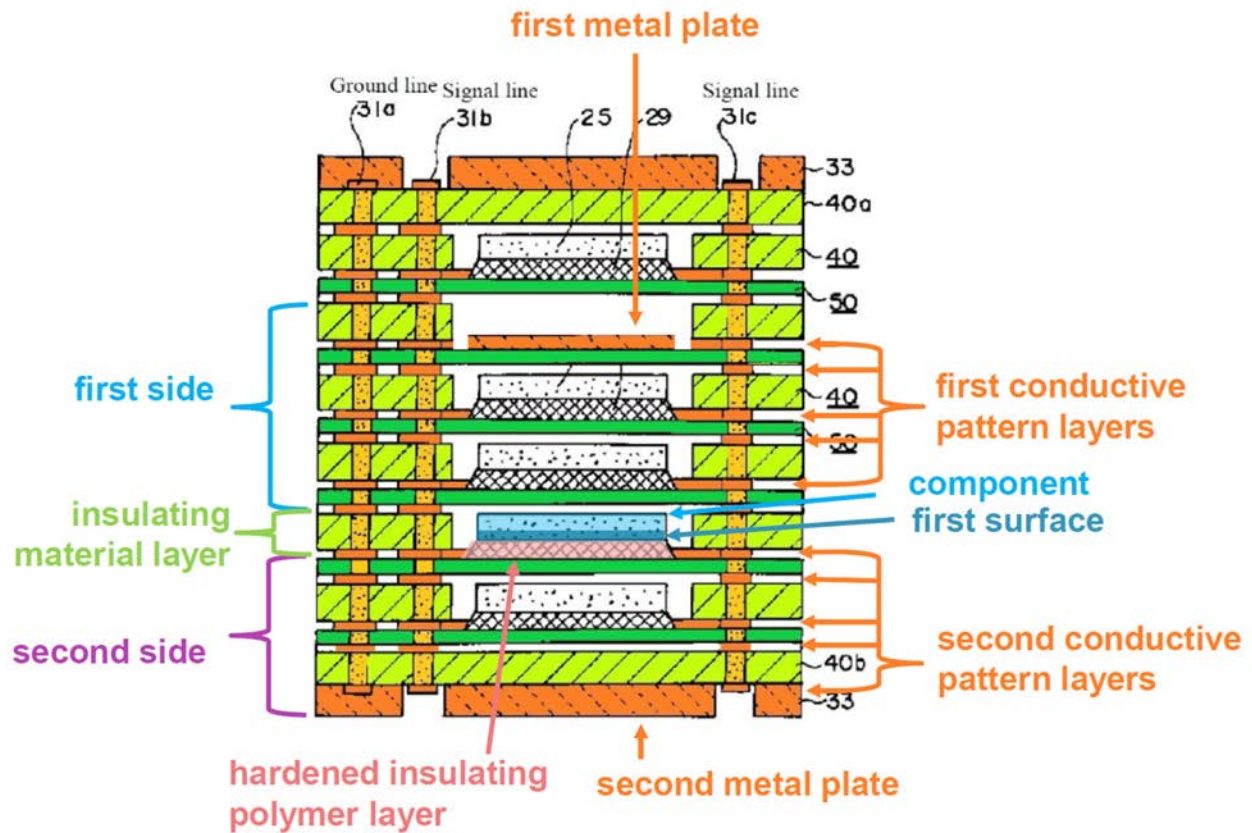
Imoto renders obvious Claim 21. Ex-1002, ¶¶135-139.

Claim 21 is like Claim 20, with one minor difference. Ex-1002, ¶136. Claim 21 requires that the second circuit board substructure include all elements of Claim 1, except the **second** metal plate. Compare Elements 21[a]-[f] with Elements 1[a]-[f]; *Id.*

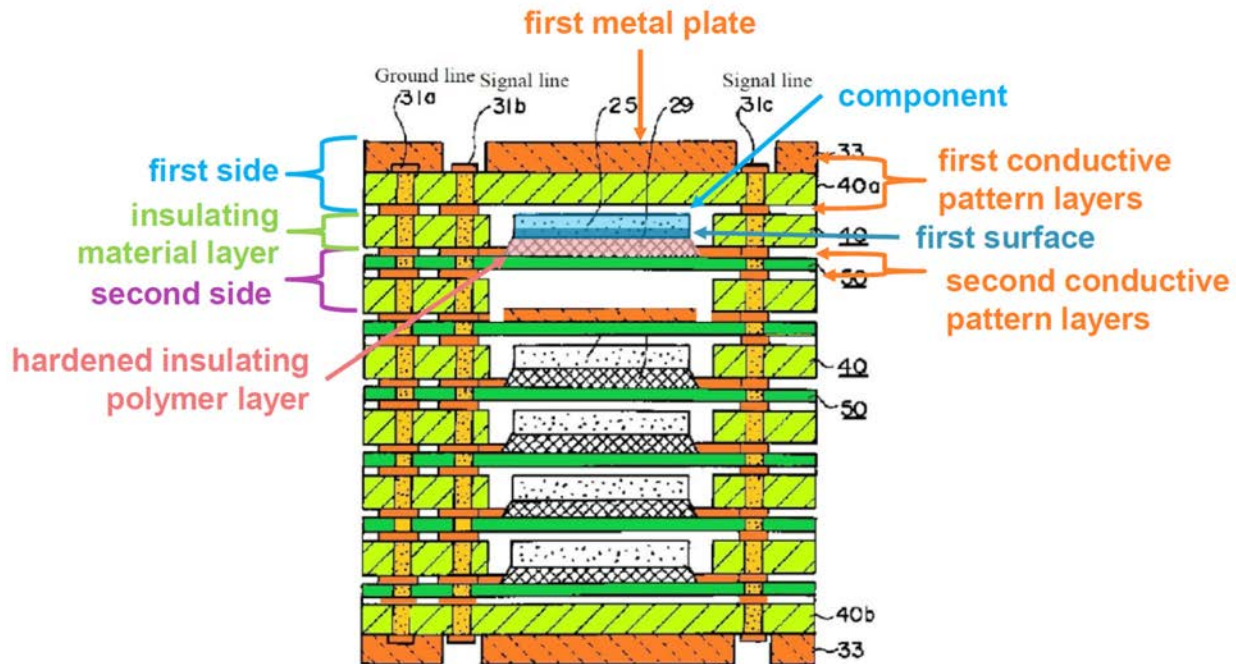
Imoto renders obvious Claim 21 under an alternative mapping where the first circuit board substructure is beneath the second circuit board substructure, as shown below. Ex-1002, ¶137.



As shown below, the first circuit board substructure meets Elements 15[a]-15[f] as described for Elements 1[a]-1[f] (§VII.A.1). Ex-1002, ¶138.



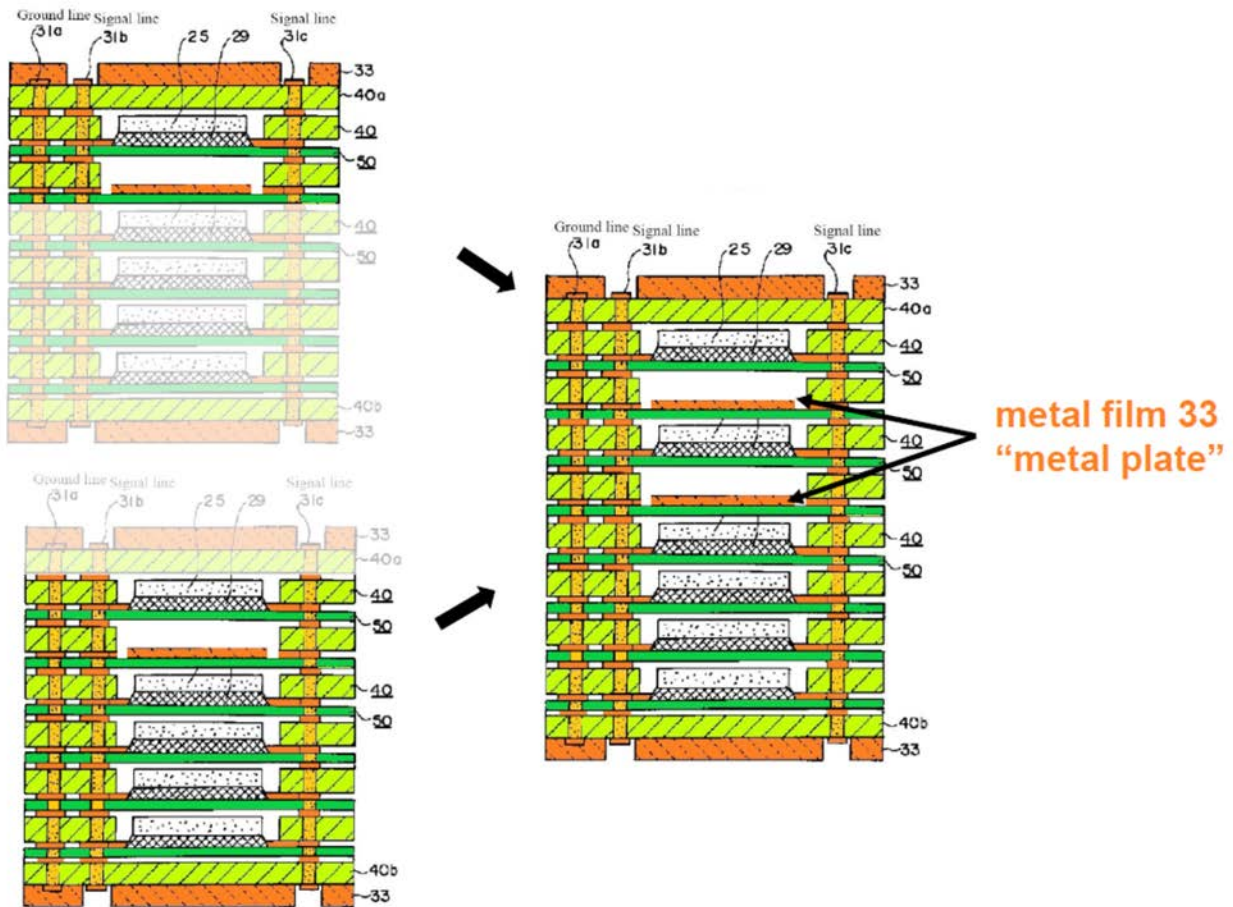
As shown below, the second circuit board substructure meets Elements 20[a]-20[f] as described for Elements 1[a]-1[f] (§VII.A.1). Ex-1002, ¶139.



15. **Dependent Claims 22: The multi-layered circuit board of claim 15, comprising a third circuit board substructure on top of the first and second circuit board substructures.**

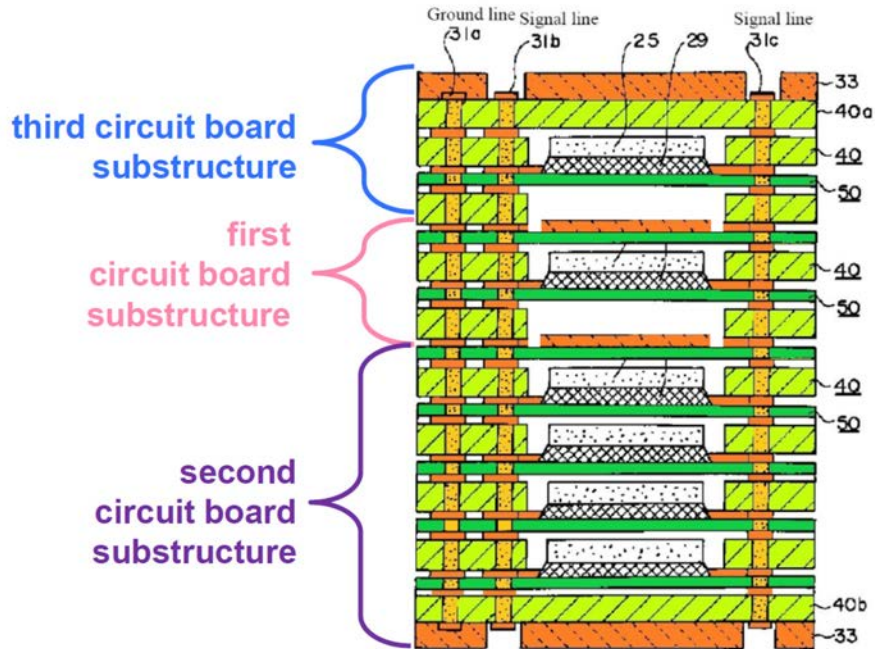
Imoto renders obvious Claim 22. Ex-1002, ¶¶140-45.

Claims 22 introduce a third circuit board substructure on top of the first and second circuit board substructures of Claim 15. Ex-1002, ¶141. The below figure shows the stacked structure of Claims 15-21, but adds layers for the same reasons described above for Claim 15 (§VII.A.8). *Id.*, ¶142.

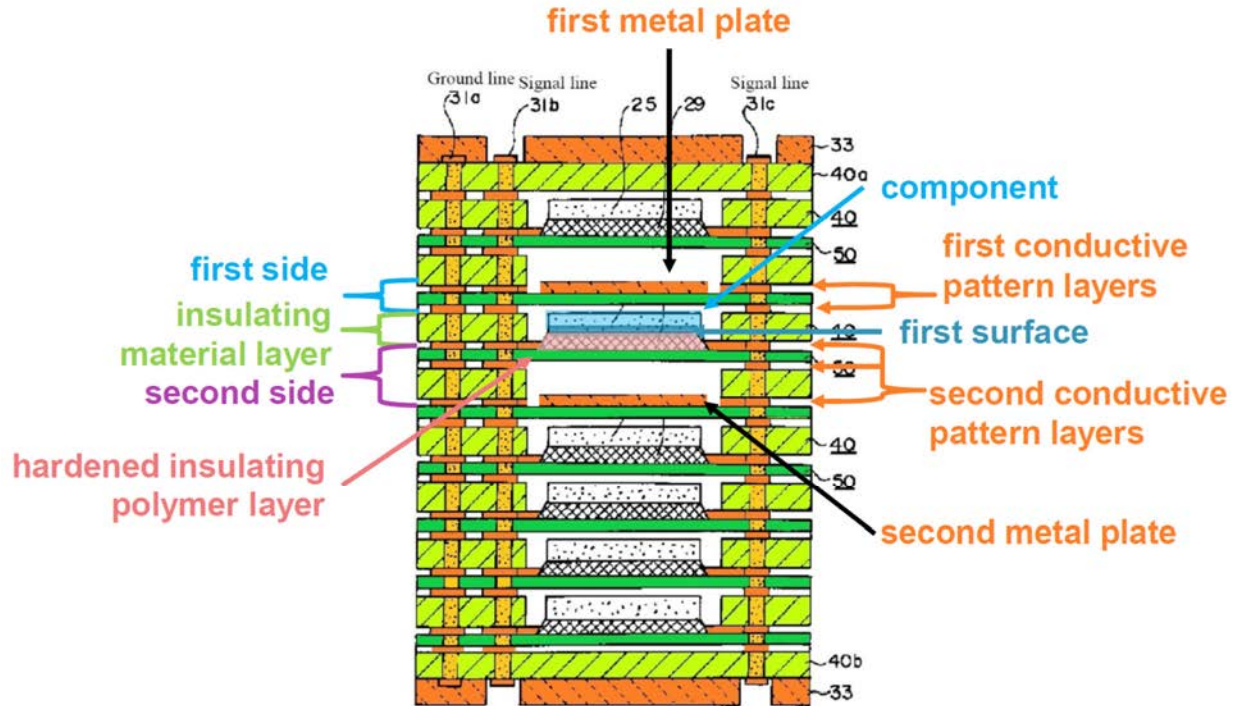


As described in Claim 15 (§VII.A.8), Imoto teaches that the structure can include additional layers, and thus, it would have been obvious to a POSITA to add layers to increase functions, reduce manufacturing costs, and save space. Ex-1002, ¶143.

As shown below, a third circuit board substructure is on top of the first and second circuit board substructures, as recited in Claim 22. Ex-1002, ¶144.



As shown below, the first circuit board substructure meets Elements 15[a]-15[f] as described for Elements 1[a]-1[f] (§VII.A.1). Ex-1002, ¶145.

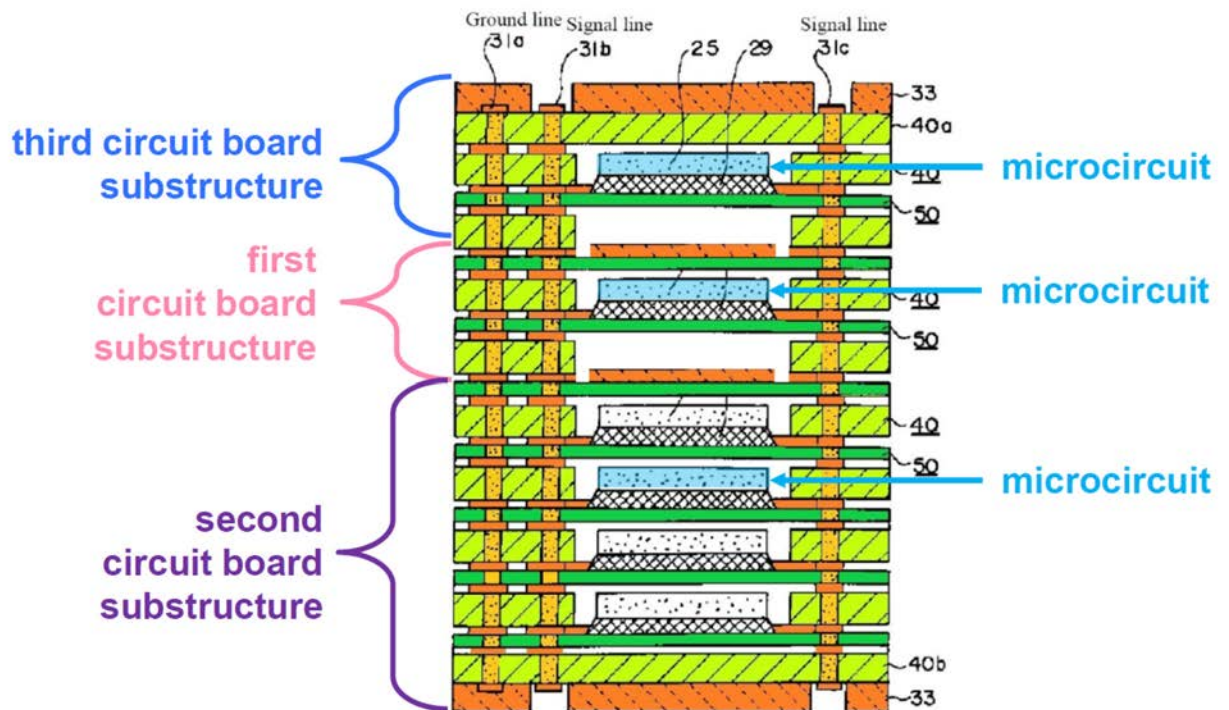


16. **Dependent Claim 23:** The multi-layered circuit board of claim 22, wherein the first circuit board substructure is between the second and third circuit board substructures.

As shown for Claim 22 (§VII.A.15), the first circuit board substructure is between the second and third circuit board substructures, and thus, Imoto renders obvious Claim 23. Ex-1002, ¶¶146-47.

17. Dependent Claim 24: The multi-layered circuit board of claim 22, wherein each of the first, second and third circuit board substructures includes an embedded microcircuit.

The first, second and third circuit board substructures identified for Claim 22 (§VII.A.15) include embedded microcircuits, and thus, Imoto renders obvious Claim 24, as shown below. Ex-1002, ¶¶148-50.



18. Dependent Claims 25: The multi-layered circuit board of claim 15, wherein the first and second metal plates are electronically connected to each other.

Claim 25 is the same as Claim 2 but depends from Claim 15. For the reasons described for Claim 2 (§VII.A.2) and Claim 15 (§VII.A.8), Imoto renders obvious Claim 25. Ex-1002, ¶151-.

- 19. Dependent Claim 26: The multi-layered circuit board of claim 15, wherein the first and second metal plates are electrically connected to each other.**

Claim 26 is the same as Claim 2 but depends from Claim 15. For the reasons described for Claim 2 (§VII.A.2) and Claim 15 (§VII.A.8), Imoto renders obvious Claims 26. Ex-1002, ¶¶152-53.

- 20. Dependent Claim 29: The multi-layered circuit board of claim 15, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.**

Claim 29 is the same as Claim 11 but depends from Claim 15. Thus, for the reasons described for Claim 11 (§VII.A.5) and Claim 15 (§VII.A.8), Imoto renders obvious Claim 29. Ex-1002, ¶¶154-55.

- 21. Dependent Claim 30: The multi-layered circuit board of claim 15, wherein the component is a microcircuit.**

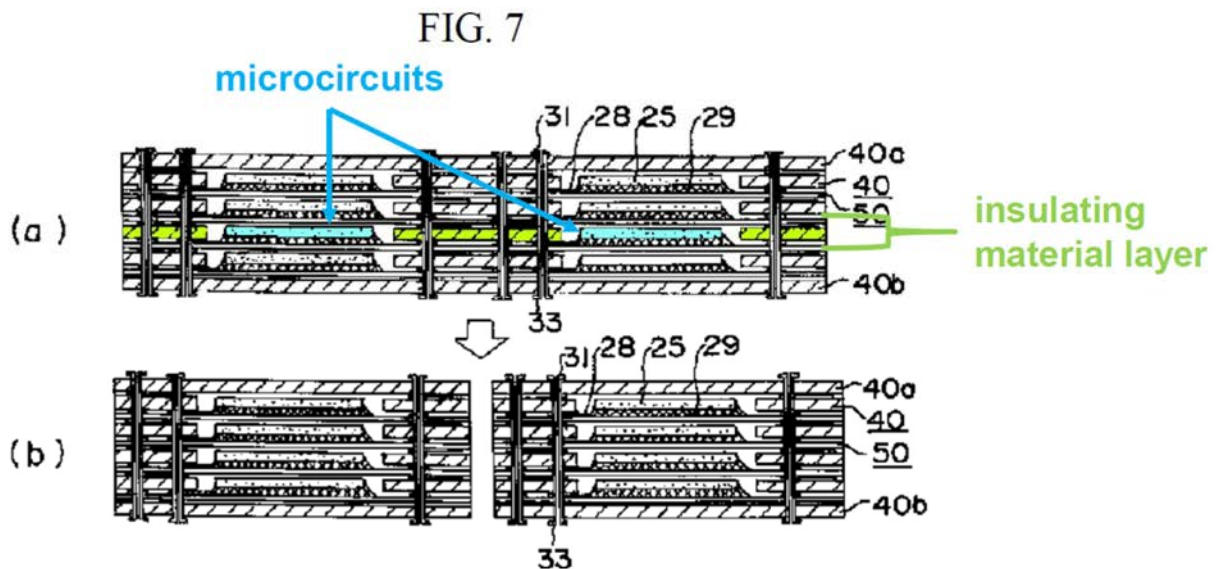
Claim 30 is the same as Claim 13 but depends from Claim 15. Thus, for the reasons described for Claim 13 (§VII.A.6) and Claim 15 (§VII.A.8), Imoto renders obvious Claim 30. Ex-1002, ¶¶156-58.

- 22. Dependent Claims 31: The multi-layered circuit board of claim 15, wherein the first circuit board substructure comprises at least two microcircuits inside the insulating material layer.**

Imoto renders obvious Claim 31. Ex-1002, ¶¶159-62.

As described for Claim 15 (§VII.A.8), the first circuit board substructure includes at least two microcircuits. Ex-1002, ¶160.

To the extent Claim 31 is argued to require the two microcircuits in a single insulating material layer, Imoto discloses that two microcircuits (semiconductor elements 25) can be embedded in each insulating material layer (laminated plate 40). Ex-1007, ¶0015 (“A region where the semiconductor elements **[plural]** are stored on the insulating plate 1 such as a printed laminated plate or the like is punched out and used as the chip cavity section 12 (FIG. 2).”); Ex-1002, ¶162. Moreover, Figure 7 of Imoto shows two microcircuits (semiconductors 25) in insulating material layer (laminated plate 40).¹⁰ Ex-1007, ¶0020 (“a plurality of chip cavity sections are formed in the conductive via laminated plate 40, a plurality of semiconductor elements are mounted on the wiring substrate 50”); Ex-1002, ¶162.



¹⁰ Although Imoto describes cutting Figure 7a into separate pieces for packaging (Ex-1007, ¶0019), it would have been obvious to a POSITA to skip the cutting step and to use Figure 7a as the final product to add functionality, to reduce manufacturing costs, and to save space. Ex-1002, ¶162 n.9.

B. Ground 2: Claims 4-7, 10, 27, 28, and 32-36 are obvious over Imoto in view of Dudderar.

1. A POSITA would be motivated to combine Imoto and Dudderar's teachings and would have a reasonable expectation of success.

A POSITA would have been motivated to combine the teachings of Imoto and Dudderar and would have had a reasonable expectation of success in doing so because each relates to the same well-known technologies. Ex-1002, ¶¶163-165. Both relate to embedding semiconductor devices within the cavity of a printed circuit board. Ex-1007, ¶¶0011-12; Ex-1009, 2:53-54. Both also describe using ground metallization above and below semiconductor devices to act as an EMI shield. Ex-1007, ¶0022; Ex-1009, 2:63-3:3. Dudderar further describes extending that metallization to the inside walls of the cavity housing the semiconductor devices. Ex-1009, 4:45-50.

A POSITA would have been motivated to apply this teaching of Dudderar to Imoto by using metallization on the sidewalls of the cavity. Ex-1002, ¶164. Imoto recognized the benefits of using grounded metallization as an EMI shield, and based on Dudderar, a POSITA would have recognized that grounded metallization on the sidewalls of Imoto would enhance those benefits, resulting in more reliable chips less likely to malfunction due to EMI. *Id.* Thus, design incentives and market forces would have motivated a POSITA to apply the teachings of Dudderar to Imoto. *Id.*

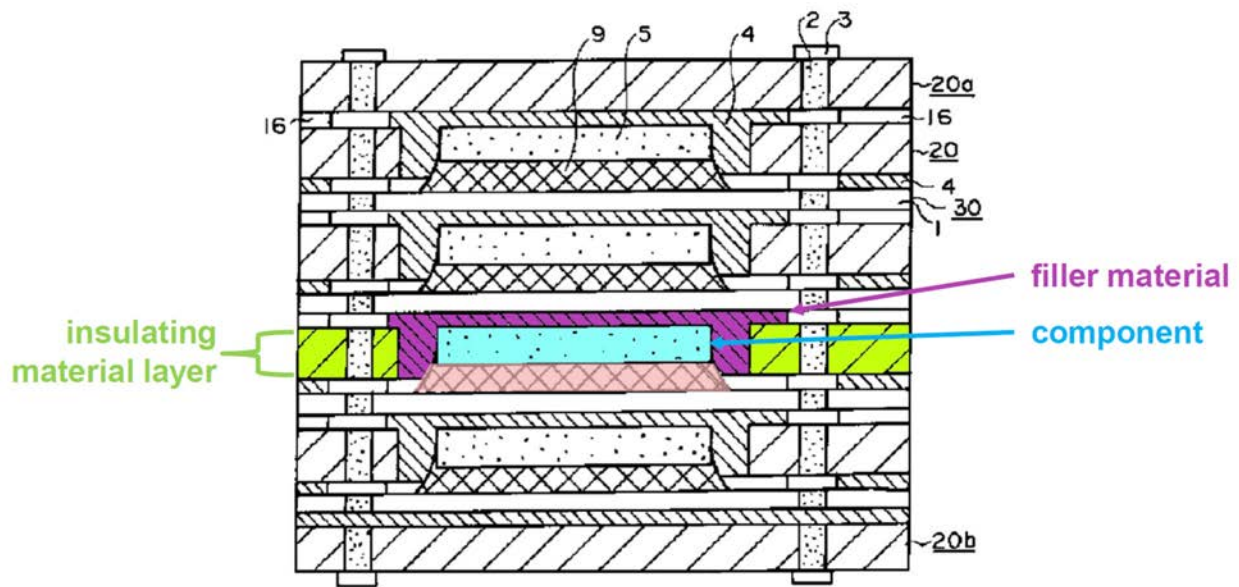
A POSITA would have had a reasonable expectation of success in combining Imoto and Dudderar. Ex-1002, ¶165. A POSITA would have understood that these references disclose interrelated teachings based on routine technologies that would have been amendable to various well-understood and predictable combinations. *Id.*

2. **Dependent Claim 4: The circuit board of claim 1, wherein the component is located in a hole in the insulating material layer, and the circuit board comprises metal foil covering the sidewalls of the hole and a filler material in the hole between the metal foil and the component.**

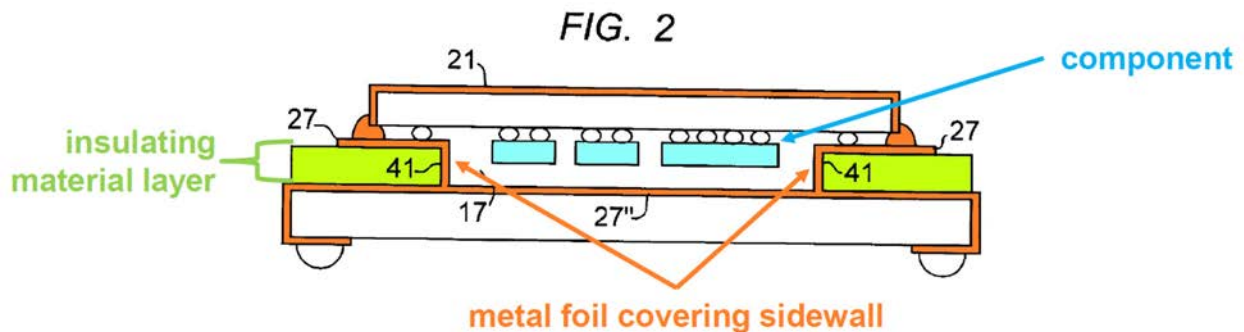
Imoto-Dudderar in combination teach Claim 4. Ex-1002, ¶¶166-169.

Imoto disclose that the component is located in a hole in the insulating material layer and that the hole includes filler material, as shown below. Ex-1002, ¶167. As described for Element 1[d] (§VII.A.1.e), Imoto’s semiconductor element 25 is located in a hole in the insulating material layer. Imoto further describes that “adhesive material 4 fills the chip cavity section 12,” as illustrated in Figure 5. Ex-1007, ¶0012; *see also* Ex-1007, ¶0013 (stating the space between the semiconductor element and the chip cavity section is “filled with a flexible adhesive material such as an elastomer”).

FIG. 5



Dudderar discloses metal foil covering sidewalls 41 of chip cavity 17, as shown below. Ex-1009, 4:45-50.

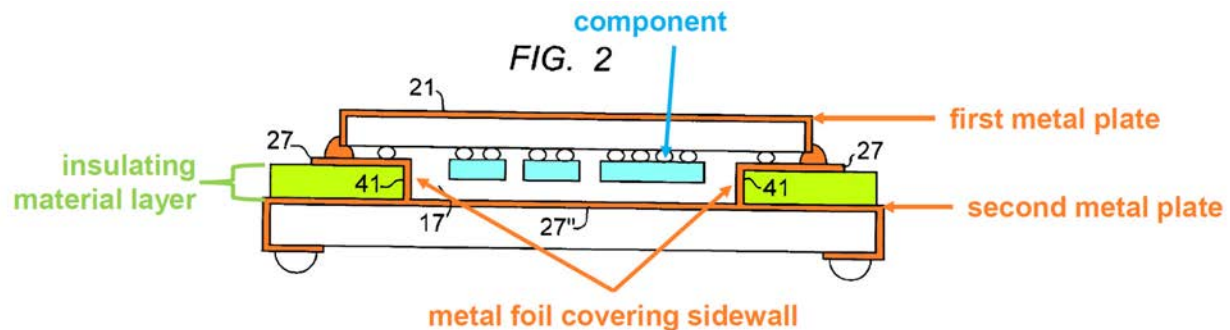


It would have been obvious to a POSITA to apply this teaching to the sidewalls of the chip cavity in Imoto. Ex-1002, ¶169. Imoto recognized the benefit of using grounded metallization to shield the semiconductor element from EMI, and a POSITA would have been motivated to implement grounded metallization on the sidewalls of Imoto to enhance those shielding benefits, as taught in Dudderar. *Id.*

3. Dependent Claim 5: The circuit board of claim 4, wherein the metal foil is electrically connected to at least one of the first and second metal plates.

Imoto-Dudderar in combination teaches Claim 5. Ex-1002, ¶¶170-72.

As described for Claim 4 (§VII.B.2), it would have been obvious to include metal foil on the sidewalls of Imoto as taught in Dudderar. Ex-1002, ¶171. Dudderar also teaches that the metal foil on the sidewalls is connected to the first and second metal plates and to ground, as shown below. Ex-1009, 3:28-37, 4:45-50.



Because Imoto also teaches that the metal plates (metal film 33) are connected together and connected to ground (*see supra* §VII.A.2; Ex-1007, ¶0022), a POSITA would have been similarly motivated to electrically connect metal foil on the sidewalls of Imoto to the first and second metal plates and to ground. Ex-1002, ¶172.

4. Dependent Claim 6: The circuit board of claim 4, wherein the metal foil is electronically connected to an earth connection of the circuit board.

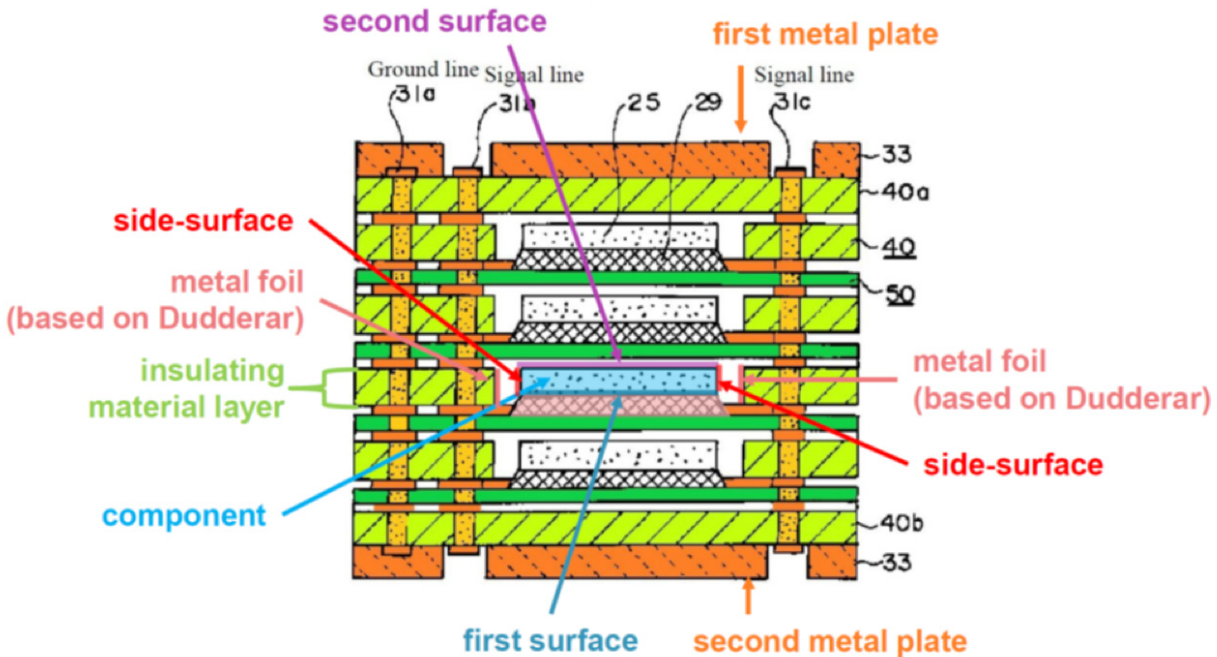
Imoto-Dudderar in combination renders obvious Claim 6. Ex-1002, ¶¶173-75.

As explained for Claim 5 (§VII.B.3), Imoto and Dudderar teach connecting metallization to ground to act as an EMI shield, and thus it would have been obvious to electronically connect metal foil on the sidewalls of Imoto to an earth connection of the circuit board. Ex-1002, ¶174.

5. **Dependent Claim 7: The circuit board of claim 4, wherein the component has a second surface opposite to the first surface and side-surfaces between the first and second surfaces, and wherein the first and second metal plates and the metal foil form an electromagnetic interference shield around the component such that the side-surfaces of the component face towards the metal foil, the first surface of the component face towards the second metal plate, and the second surface of the component face towards the first metal plate.**

Imoto-Dudderar in combination renders obvious Claim 7. Ex-1002, ¶¶176-177.

As explained for Claim 4 (§VII.B.2), it would have been obvious to include metal foil that forms an EMI shield on the sidewalls of Imoto as taught in Dudderar. Ex-1002, ¶¶177. As shown below, the side surfaces (red) of the component face the metal foil (pink), the first surface (dark blue) of the component faces the second metal plate, and the second surface (purple) of the component faces the first metal place. *Id.*



6. **Dependent Claim 10:** The circuit board of claim 8, wherein the component is located in a hole in the baseboard; and the circuit board comprises conductive material on the sidewalls of the hole and a filler material in the hole between the metal foil and the component, wherein the metal foil creates an interference protection structure around the component.

Claim 10 combines the elements of Claims 4 and 8. Thus, as described for Claim 4 (§VII.B.2) and Claim 8 (§VII.A.4), Imoto-Dudderar in combination renders obvious Claim 10. Ex-1002, ¶¶178-79. As taught in Dudderar, the metallization “surrounds” the component to provide EMI protection. Ex-1009, 3:48-51, 4:45-50.

7. **Dependent Claim 27: The multi-layered circuit board of claim 15, wherein the component is located in a hole in the insulating material layer, and the circuit board comprises metal foil covering the sidewalls of the hole and a filler material in the hole between the metal foil and the component.**

Claim 27 is the same as Claim 4 but depends from Claim 15. Thus, as described for Claim 4 (§VII.B.2) and Claim 15 (§VII.A.8), Imoto-Dudderar in combination renders obvious Claim 27. Ex-1002, ¶¶180-81.

8. **Dependent Claim 28: The multi-layered circuit board of claim 15, wherein the metal foil is electronically connected to at least one of the first and second metal plates.**

Claim 28 is the same as Claim 5 but depends from Claim 15. Thus, as described above for Claim 5 (§VII.B.3) and Claim 15 (§VII.A.8), Imoto-Dudderar in combination renders obvious Claim 28. Ex-1002, ¶¶182-83.

9. **Independent Claim 32**

- a. **Element 32[preamble]: An electronic module comprising**

Imoto's Figure 8 shows a multilayer substrate including semiconductor elements and thus teaches the preamble of Claim 1, to the extent it is limiting. Ex-1007, ¶¶00021-22; Ex-1002, ¶184.

- b. **Element 32[a]: an insulating material layer having a first side and a second side**

Element 32[a] is the same as Element 1[a], and thus Imoto discloses this element as described for Element 1[a] (§VII.A.1.b). Ex-1002, ¶185.

- c. **Element 32[b]: at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate**

Element 32[b] is the same as Element 1[b], and thus Imoto discloses this element as described for Element 1[b] (§VII.A.1.c). Ex-1002, ¶186.

- d. **Element 32[c]: at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate**

Element 32[c] is the same as Element 1[c], and thus Imoto discloses this element as described for Element 1[c] (§VII.A.1.d). Ex-1002, ¶187.

- e. **Elements 32[d], [e], [f], and [g]: a hole having sidewalls defined in the insulating material layer and located between the first and second metal plates, a metal foil covering the sidewalls of the hole, a microcircuit inside the hole and having a first surface facing towards the second metal plate, and contact areas on the first surface, a filler material in the hole between the metal foil and the microcircuit**

Elements 32[d], [e], [f], and [g] are the same as Elements 1[d], Element 1[e], Claims 4, and Claim 13, and thus, Imoto-Dudderar in combination renders obvious these elements as described for Element 1[d] (§VII.A.1.e), Element 1[e] (§VII.A.1.f), Claim 4 (§VII.B.2) and Claim 13 (VII.A.6). Ex-1002, ¶188.

- f. Element 32[h]: a hardened insulating polymer layer between the first surface of the microcircuit and at least one conductive pattern of said at least one second conductive pattern layer**

Element 32[h] is the same as Element 1[e], and thus Imoto discloses this element as described for Element 1[e] (§VII.A.1.f). Ex-1002, ¶189.

- g. Element 32[i]: contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the microcircuit and the at least one second conductive pattern layer or layers.**

Element 32[i] is the same as Element 1[f], and thus Imoto discloses this element as described for Element 1[f] (§VII.A.1.g). Ex-1002, ¶190.

- 10. Dependent Claim 33: The electronic module of claim 32, wherein the first and second metal plates are electronically connected to each other.**

Claim 33 is the same as Claim 2, but depends from Claim 32. Thus, as described for Claim 2 (§VII.A.2) and Claim 32 (§VII.B.9), Imoto-Dudderar in combination renders obvious Claim 33. Ex-1002, ¶¶191-92.

- 11. Dependent Claim 34: The electronic module of claim 32, wherein the first and second metal plates are electrically connected to an earth connection of the electronic module.**

Claim 34 is the same as Claim 3, but depends from Claim 32. Thus, as described for Claim 3 (§VII.A.3) and Claim 32 (§VII.B.9), Imoto-Dudderar in combination renders obvious Claim 33. Ex-1002, ¶¶193-95.

- 12. Dependent Claim 35: The electronic module of claim 32, wherein the metal foil is electronically connected to at least one of the first and second metal plates.**

Claim 35 is the same as Claim 5, but depends from Claim 32. Thus, as described for Claim 5 (§VII.B.3) and Claim 32 (§VII.B.9), Imoto-Dudderar in combination renders obvious Claim 33. Ex-1002, ¶¶196-97.

- 13. Dependent Claim 36: The electronic module of claim 32, wherein the metal foil and the first and second metal plates are electronically connected to an earth connection of the electronic module.**

Claim 36 is the same as Claims 3 and 6, but depends from Claim 32. Thus, for the reasons described for Claim 3 (§VII.A.3), Claim 6 (§VII.B.4), and Claim 32 (§VII.B.9), Imoto-Dudderar in combination renders obvious Claim 36. Ex-1002, ¶¶198-99.

C. Ground 3: Claims 9 and 31 are obvious over Imoto in view of Mowatt.

- 1. A POSITA would be motivated to combine Imoto and Mowatt's teachings and would have a reasonable expectation of success.**

A POSITA would have been motivated to combine the teachings of Imoto and Mowatt and would have had a reasonable expectation of success in doing so, because each relates to the same well-known technologies. Ex-1002, ¶200. Both relate to embedding semiconductor devices within a printed circuit board. Ex-1007, ¶¶0011-12; Ex-1010, 9:40-43. A POSITA would have understood that these references

disclose interrelated teachings based on routine technologies and would have been amendable to various well-understood and predictable combinations. Ex-1002, ¶200.

2. Dependent Claims 9: The circuit board of claim 8, wherein the baseboard is a glass-fibre reinforced epoxy board.

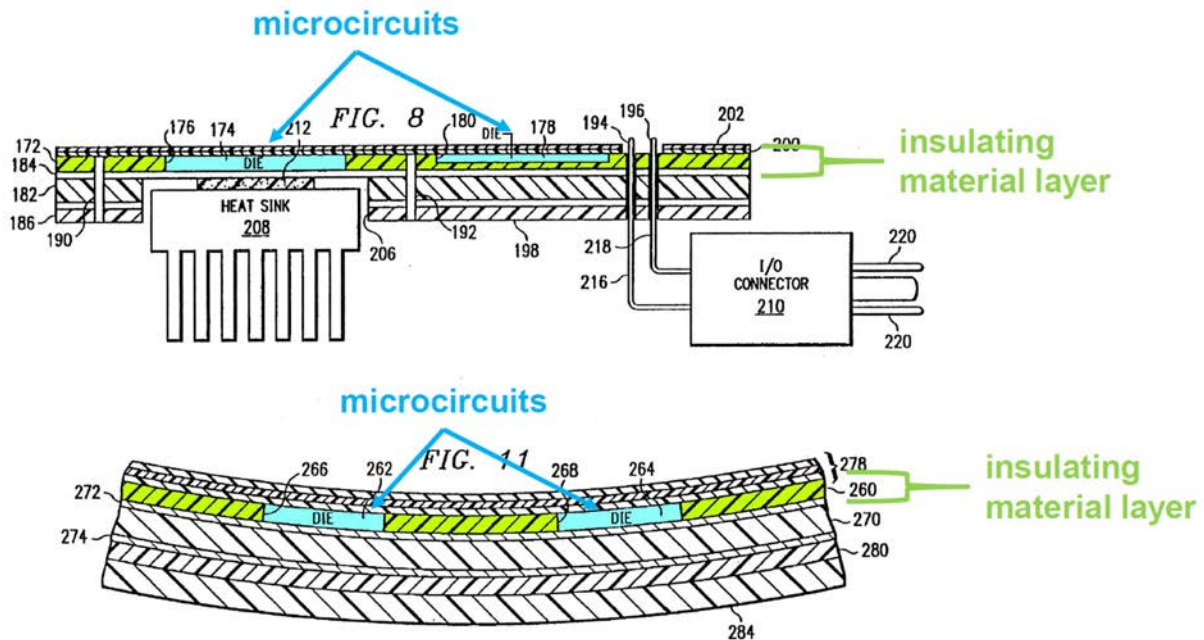
Imoto-Mowatt in combination renders obvious Claim 9. Ex-1002, ¶¶201-202.

As described for Claim 8 (§I.A.4), the insulating material layer in Imoto includes baseboard (plate 40), such as a “polyimide substrate.” Ex-1007, ¶¶0011, ¶0015. Like Imoto, Mowatt describes embedding semiconductor devices within a laminated plate. Ex-1010, 9:40-43. Mowatt teaches that the laminated plate could include “an *epoxy glass material*, or polyimide glass material, teflon or other materials commonly used in PWB fabrication.” *Id.*, 4:40-43 (emphasis added). Based on Mowatt, it would have been obvious to a POSITA that the baseboard in Imoto (laminated plate 40) could be a glass-fibre reinforced epoxy board. Ex-1002, ¶202. A POSITA would have been motivated to use glass-fibre reinforced epoxy boards to increase the baseboard’s rigidity and stability. *Id.*

3. Dependent Claims 31: The multi-layered circuit board of claim 15, wherein the first circuit board substructure comprises at least two microcircuits inside the insulating material layer

Imoto alone renders obvious Claim 31. *See supra* §VII.A.22

Alternatively, Imoto-Mowatt in combination renders obvious Claim 31. Ex-1002, ¶¶204-206. As shown below, Figures 8 and 11 of Mowatt disclose two microcircuits inside the same insulating material layer. Ex-1010, 9:40-43, 11:58-59; Ex-1002, ¶¶204-205.



In view of Figure 8 and 11 of Mowatt and the additional teachings of Imoto (§VII.A.21), it would have been obvious to a POSITA that at least two microcircuits can be embedded in an insulating material layer (laminated plate 40) in Imoto. Ex-1002, ¶206. A POSITA would have been motivated to add a microcircuit to increase functionality, to reduce manufacturing costs, and to save space. *Id.*

D. Ground 4: Claims 11 and 29 are obvious over Imoto in view of Lau.

- 1. A POSITA would be motivated to combine Imoto and Lau’s teachings and would have a reasonable expectation of success.**

A POSITA would have been motivated to combine the teachings of Imoto and Lau and would have had a reasonable expectation of success in doing so, because each relates to the same well-known technologies. Ex-1002, ¶207. Imoto discloses that semiconductor element 5 is “die bonded and mounted on the wiring substrate 30 using flip chip method or the like.” Ex-1007, ¶0016. It describes the use of “solder balls and the like.” *Id.* Lau describes implementation details for flip-chip and die bonding technologies, including solder balls and underfill resins. Ex-1011, 44, 47-48, 159-61, 186-87. A POSITA would have understood that these references disclose interrelated teachings based on routine technologies and would have been amenable to various well-understood and predictable combinations. Ex-1002, ¶207.

- 2. Dependent Claim 11: The circuit board of claim 1, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.**

Imoto alone renders obvious Claim 11. *See supra* §VII.A.5.

Alternatively, Imoto-Lau in combination renders obvious Claim 11. Ex-1002, ¶¶209-213. As described for Element 1[f] (§VII.A.1.g), the conductors in the

contact openings of Imoto are connection terminals 11 surrounded by underfill resin 9/29. *Id.*, ¶209.

Semiconductor element 5/25 in Imoto is “die bonded and mounted on the wiring substrate 30 using flip chip method or the like,” and “connection terminals 11 such as solder balls or the like are connected to the wiring pattern 8.” Ex-1007, ¶0016. A POSITA would have been motivated to implement the solder balls in Imoto using under-bump metallurgy (UBM) as taught in Lau. Ex-1011, 43-44; Ex-1002, ¶210. UBM is necessary to form an effective physical, metallurgical, and electrical connection between the solder and the chip. Ex-1011, 43-44; Ex-1002, ¶210. As shown in Table 2.4 of Lau (Ex-1011, 44), UBM for solder typically involves copper, which can be applied by electroplating. Ex-1002, ¶210. Lau describes electroplating to apply Ti-Cu or TiW-Cu and 6-25 μm of Cu (copper), as shown below. Ex-1011, 47-48, 186-87.

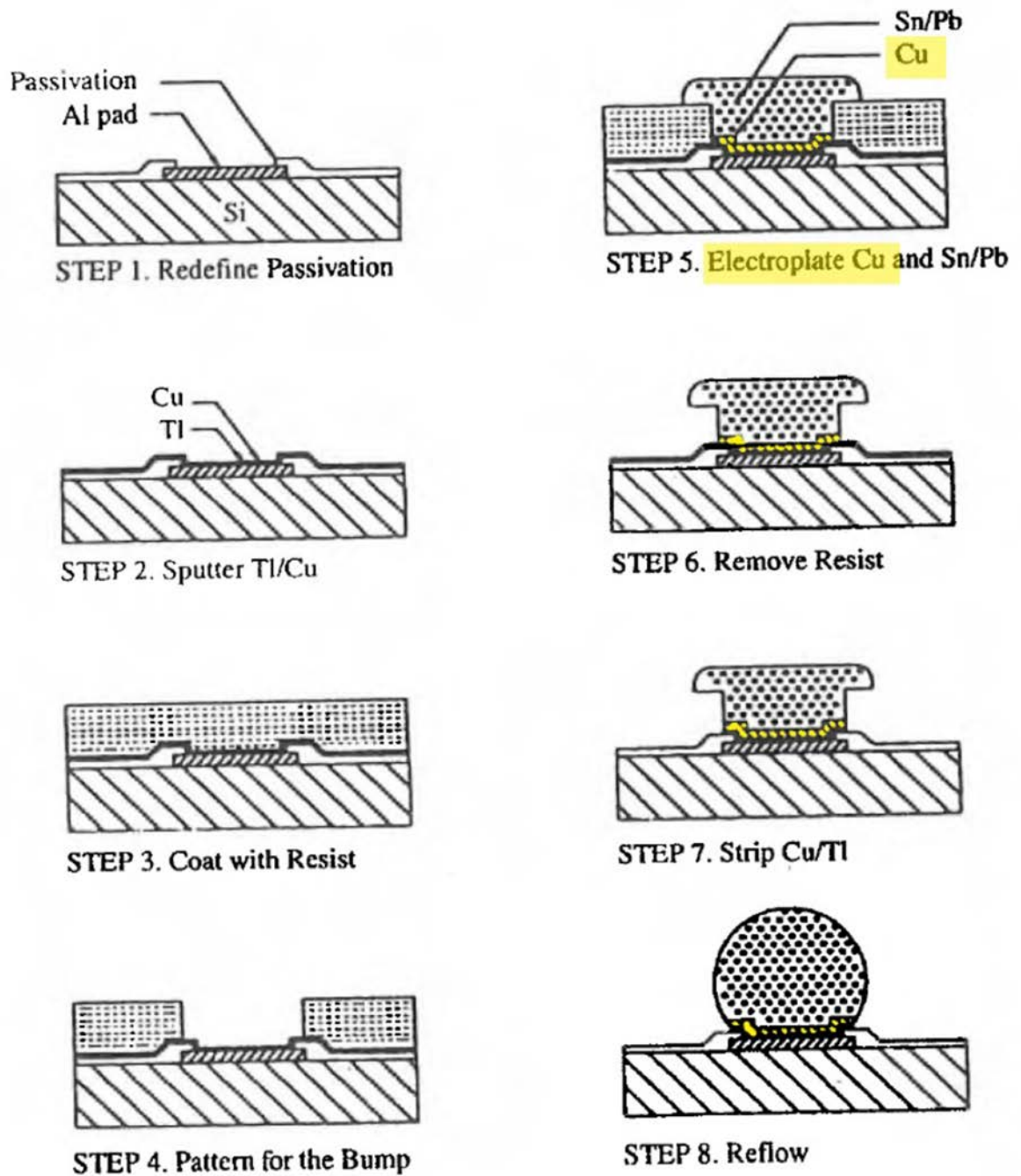


Figure 2.19 Electroplated solder wafer-bumping process.

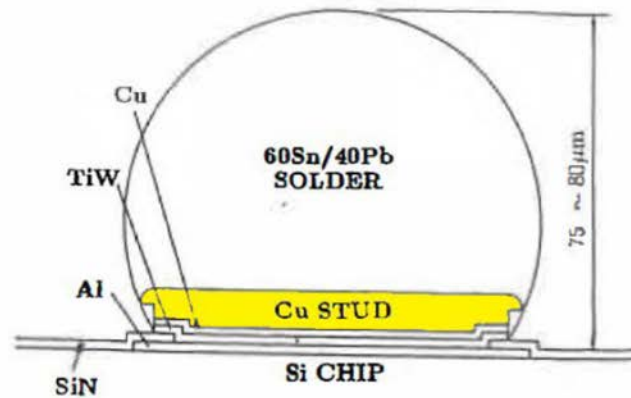


Figure 6.7 Sharp's eutectic solder bump.

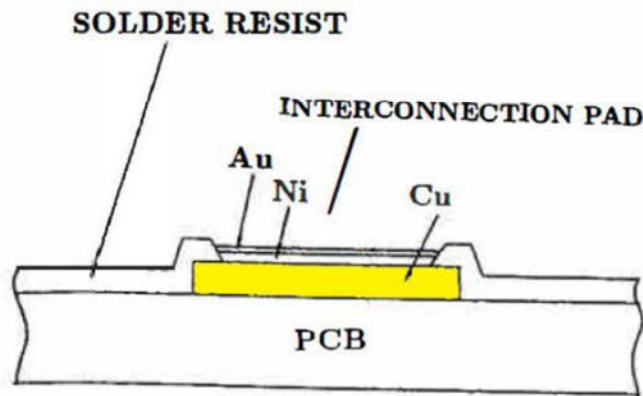


Figure 6.8 Sharp's low-cost PCB.

Electroplating is an electrochemical deposition process and, thus, the result is electrochemically deposited copper. Ex-1002, ¶211. In view of Lau, it would have been obvious to a POSITA that, in Imoto, the conductors in underfill resin 9/29 (hardened insulating polymer layer) include electrochemically deposited copper (in addition to solder), as recited in Claim 11. *Id.*

Alternatively, instead of solder, connection terminals 11 in Imoto could be copper bumps as taught in Lau. Ex-1002, ¶212. Imoto teaches that connection terminals 11 could be solder balls “or the like.” Ex-1007, ¶0016. Lau describes

that, instead of solder, semiconductor chips are also mounted using copper bumps.

Ex-1011, 159-61.

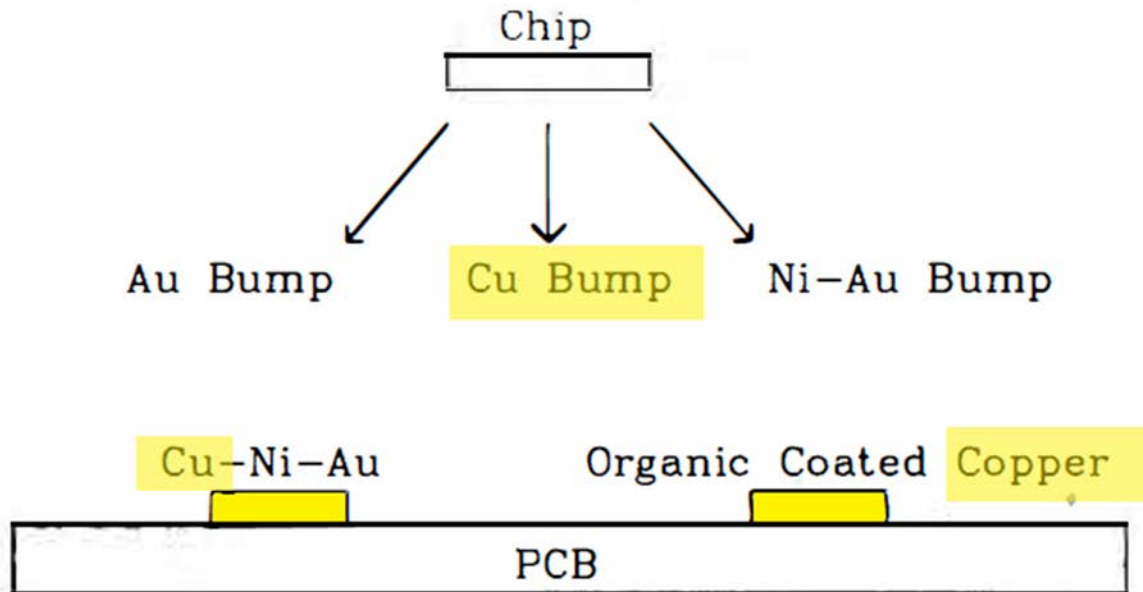


Figure 5.2 Flip chip with three different kinds of bumps on two different kinds of PCBs.

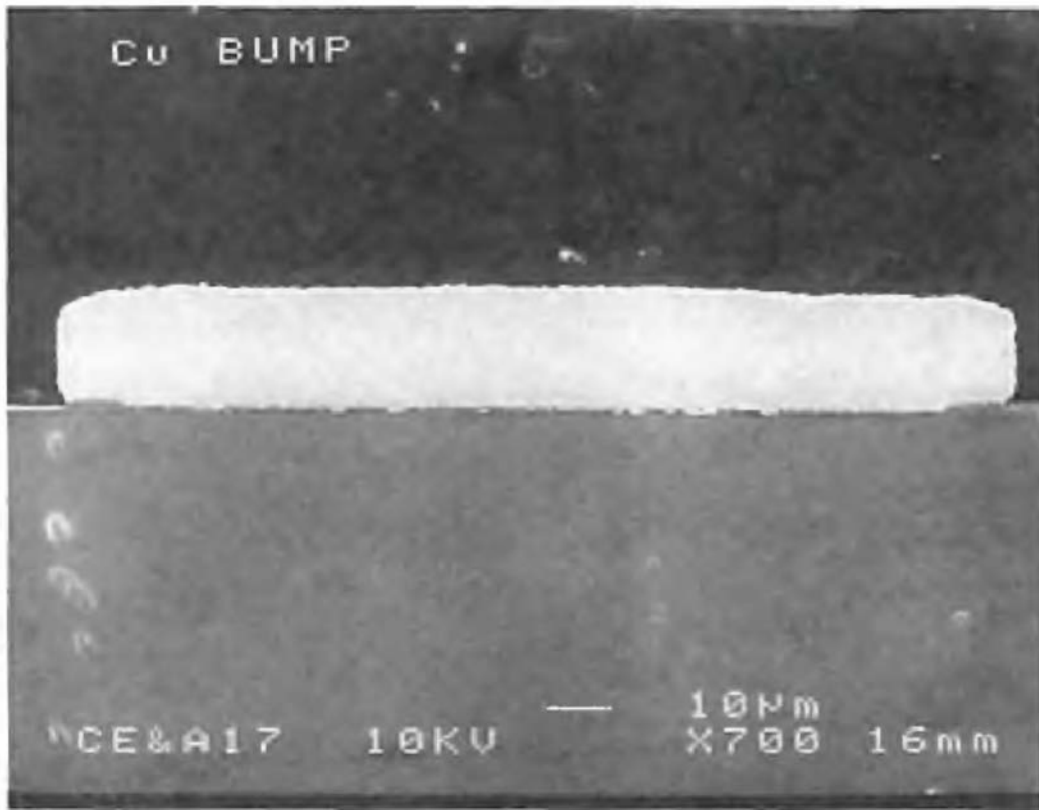


Figure 5.5 A typical Si chip with Cu bump.

Lau describes that copper bumps are formed by electroplating. Ex-1011, 159 (Au bumps formed by “electroplating”), 160 (copper bump formed same way and identified as “plated Cu”). As Lau explains, a POSITA would have been motivated to use a solderless material “for the sake of a green environment.” Ex-1011, 157. In addition, a POSITA would have understood that copper is highly conductive and is widely used to form reliable interconnections in integrated circuits. Ex-1002, ¶213. Thus, in view of Lau, it would have been obvious to a POSITA that connection terminals 11 in Imoto could be copper bumps as opposed to solder and, thus, that

connection terminals 22 in underfill resin 9/29 (hardened insulating polymer layer) would include electrochemically deposited copper, as recited in Claim 11. *Id.*

3. **Dependent Claim 29: The multi-layered circuit board of claim 15, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.**

Claim 29 is the same as Claim 11 but depends from Claim 15. Thus, for the reasons described for Claim 11 (§VII.D.2) and Claim 15 (§VII.A.8), Imoto-Lau in combination renders obvious Claim 29. Ex-1002, ¶¶214-215.

E. Ground 5: Claim 12 is obvious over Imoto in view of Lehmann.

1. **Dependent Claim 12: The circuit board of claim 1, wherein the hardened insulating polymer layer contains epoxy.**

Imoto-Lehman in combination renders obvious Claim 12. Ex-1002, ¶¶216-218.

As described above for Element 1[e] (VII.A.1.f), the hardened insulating polymer layer in Imoto is underfill resin 9/29. Like Imoto, Lehmann describes the use of solder balls and underfill resin to attach a chip to a substrate. Ex-1012, 266. Lehman teaches that the underfill resin can be “epoxy resin.” Ex-1012, 266. Based on this teaching in Lehmann, it would have been obvious to POSITA to implement underfill resin 9/29 (hardened insulating polymer layer) in Imoto contains epoxy. Ex-1002, ¶217.

A POSITA would have been motivated to combine the teachings of Imoto and Lehmann and would have had a reasonable expectation of success in doing so, because each relates to the same well-known technologies. Both relate to the use of solder ball and underfill resin to attach chips to substrates. Ex-1007, ¶0016; Ex-1012, 266. A POSITA would have been motivated to use epoxy resin to “protect[] both the chip and the solder joints” as taught in Lehman. Ex-1012, 266. A POSITA would also have had a reasonable expectation of success in combining Imoto and Lehmann. Ex-1002, ¶218. A POSITA would have understood that these references disclose interrelated teachings based on routine technologies and would have been amenable to various well-understood and predictable combinations. *Id.*

F. Ground 6: Claims 1-3, 8, 11, 13-26, and 29-31 are rendered obvious by Kurita.

1. Independent Claims 1

a. Element 1[preamble]: A circuit board comprising

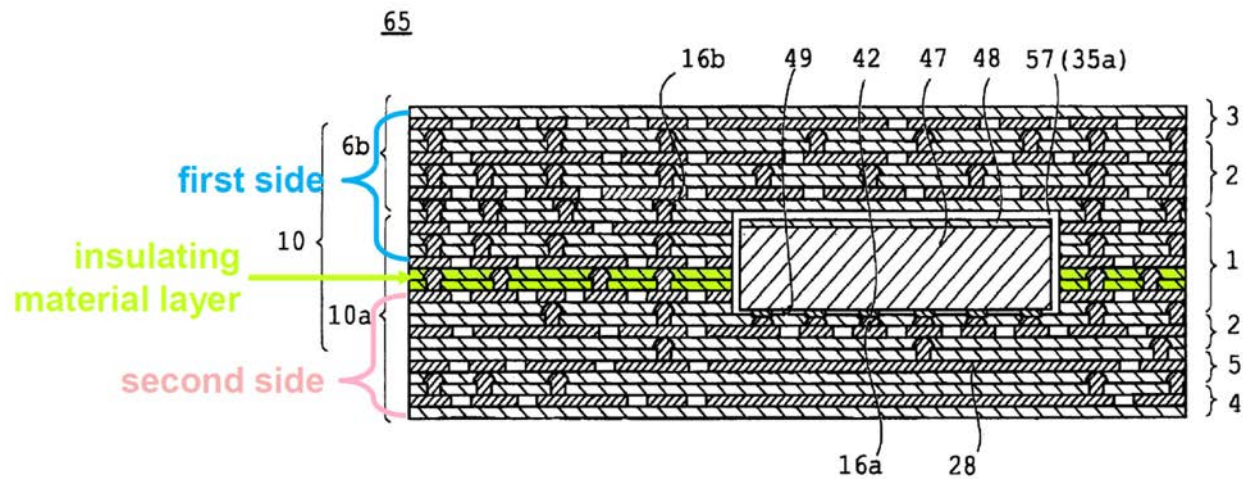
Kurita teaches the preamble of Claim 1, to the extent it is limiting. Ex-1002, ¶¶219-20. As indicated by its title “Multi-Layer Flexible Printed Wiring Board,” Kurita teaches a circuit board. Ex-0013, 1:6-8, 5:57-58; Ex-1002, ¶220. The circuit board in Kurita is multilayer substrate 65 in Figure 7. Ex-0013, 11:50-56.

b. Element 1[a]: an insulating material layer having a first side and a second side

Kurita discloses Element 1[a]. Ex-1002, ¶¶221-26.

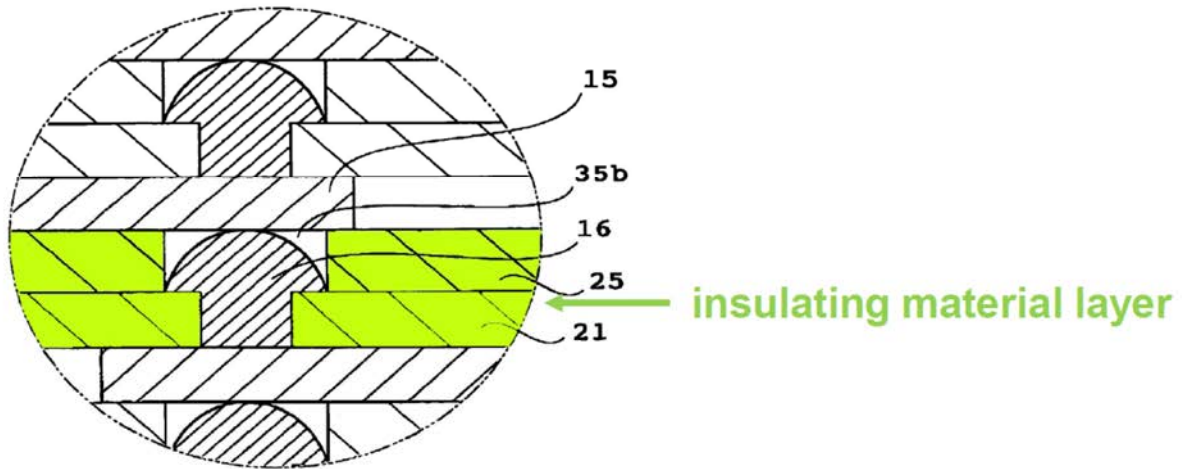
Kurita discloses an insulating material layer with first and second sides, as shown below. Ex-1002, ¶222.

FIG. 7



The insulating material layer is adhesive films 21 and resin film 25, as shown in Figure 3A. Ex-1002, ¶223.

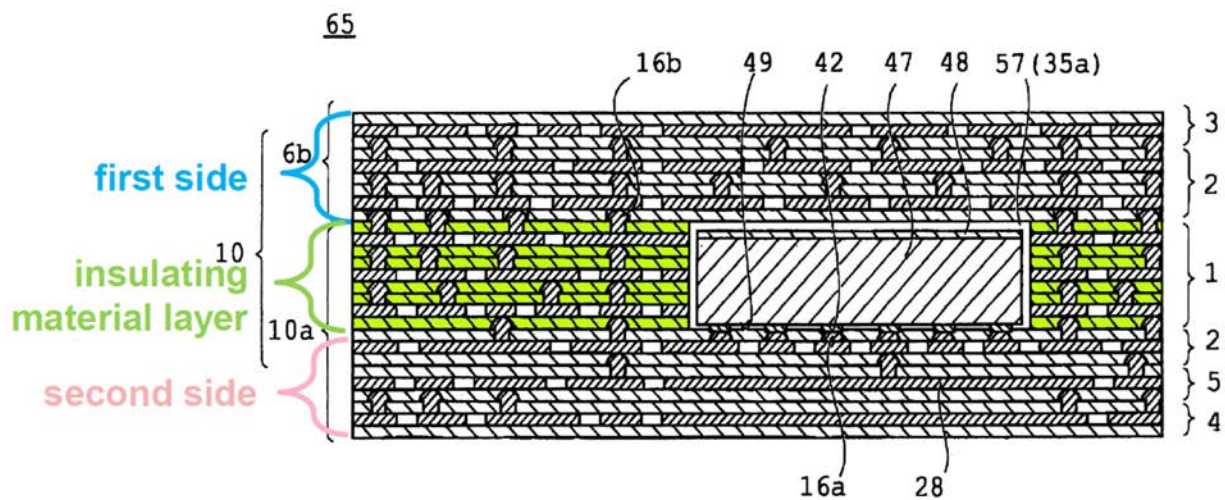
FIG. 3A



Adhesive layer 21 is a thermoplastic formed from heating polyimide. Ex-1013, 6:42-50, 7:62-8:6. Resin film 25 is “formed of polyimide film by hardening of the precursor coat 23.” Ex-1013, 7:25-27. Thus, resin film 25 and adhesive film 21 is an insulating material layer. Ex-1002, ¶224.

Under an alternative mapping of the claims, the insulating material layer is the combination of resin films 25 and adhesive films 21¹¹ making up the side of housing section 57 in Figure 7. Ex-1002, ¶225.

FIG. 7



Although the below analysis of other claim elements focuses on the first mapping, the below analysis applies equally to this alternative mapping.

- c. **Element 1[b]: at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate**

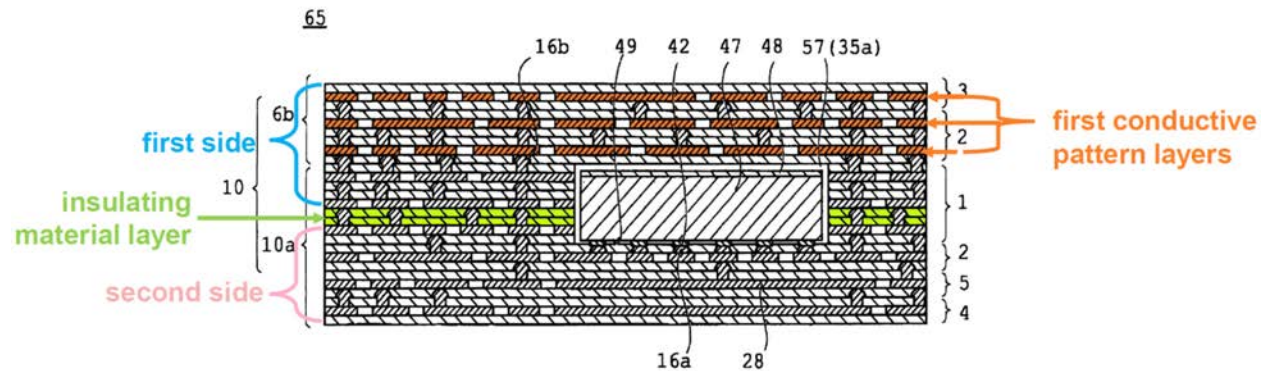
Kurita discloses Element 1[b]. Ex-1002, ¶¶227-33.

¹¹ The presence of intervening wiring films 15 is consistent with the '944 Patent, which contemplates there may be “at least one conductive pattern layer *in the insulating material layer*.” Ex-1001, 11:13-14 (emphasis added).

As shown below, the first conductive pattern layers in Figure 7 are the layers of wiring film 15 (shaded orange) above the insulating material layer (shaded green).

Ex-1002, ¶228.

FIG. 7



The first conductive pattern layers identified above correspond to wiring films 15 in Figures 1-3. Ex-1002, ¶229. Kurita states wiring film 15 is made by “patterning” metallic foil 11, as shown in Figure 1J and 1K. Ex-1013, 6:51-64.

FIG. 1J

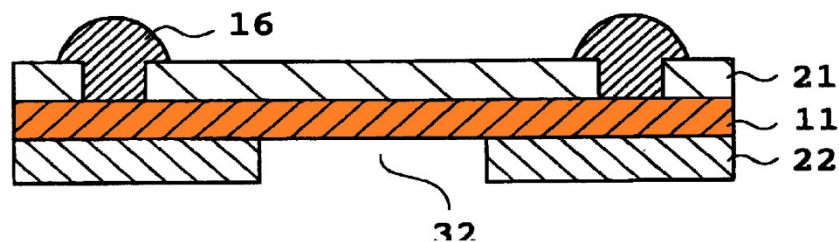
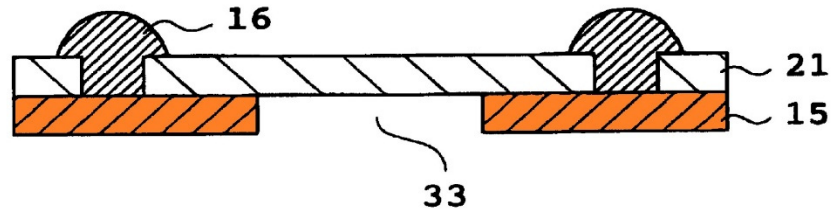


FIG. 1K



Kurita also discloses that wiring film 15 can be patterned to form shield section 28, which provides a larger surface area that may be grounded to shield semiconductor device 47 from EMI. Ex-1013, 4:1-9, 5:24-30, 6:62-64, 11:56-63, 12:8-15, 12:40-46. Figure 8 illustrates an example of shield section 28.

FIG. 8

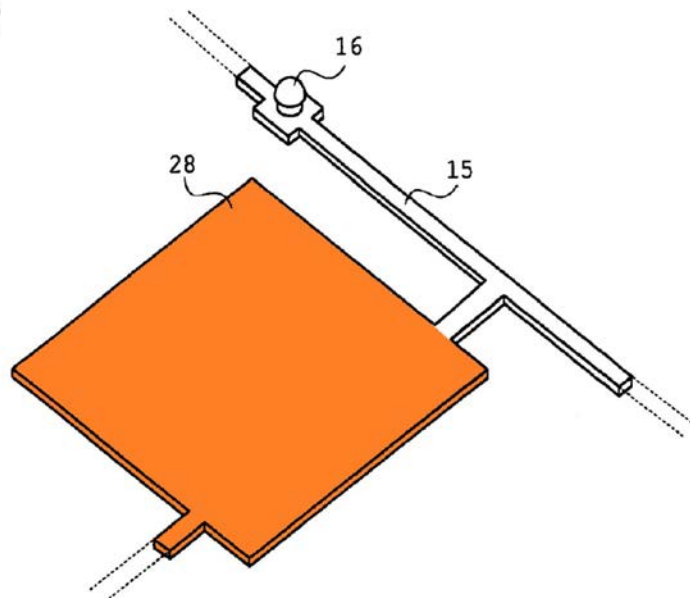
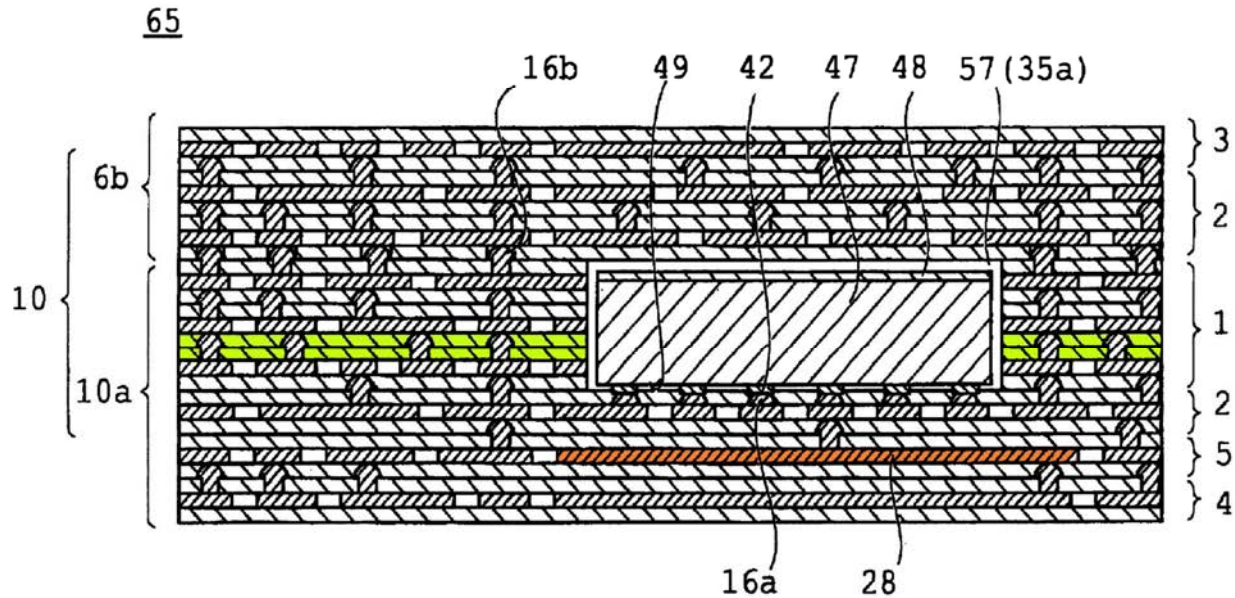


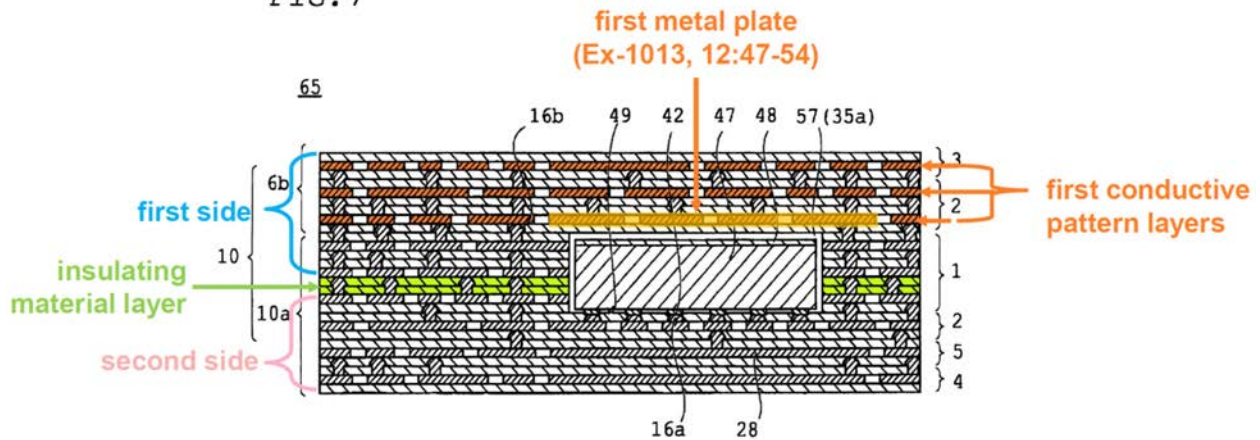
Figure 7 shows shield section 28 below semiconductor device 47.

FIG. 7



But Kurita explains that “it is more effective to arrange the shield sections 28 on both side [sic] of the semiconductor device 47.” Ex-1013, 12:47-54. When placed above semiconductor device 47 as Kurita teaches, shield section 28 corresponds to the claimed first metal plate. Ex-1002, ¶233. Based on Kurita’s description, this Petition uses orange shading to identify where a first metal plate is located above device 47, as shown below.

FIG. 7

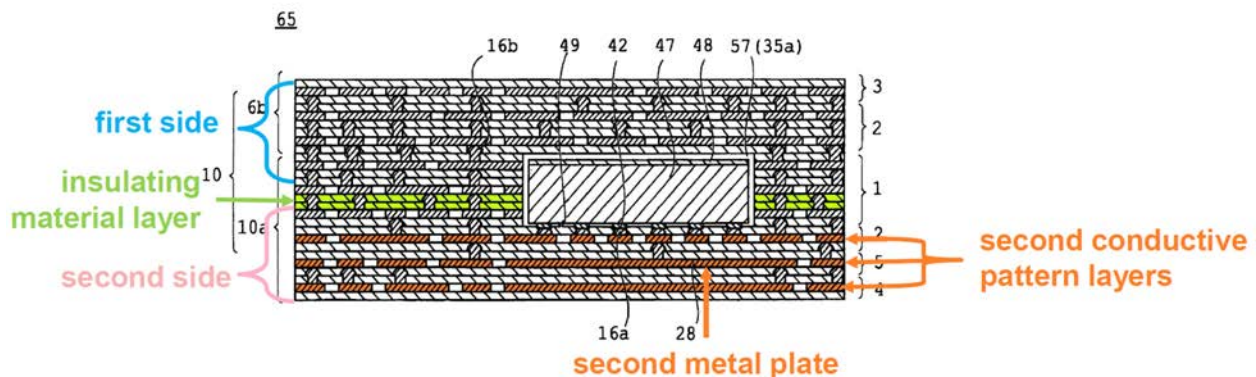


- d. **Element 1[c]: at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate**

Kurita discloses Element 1[c]. Ex-1002, ¶¶234-35.

The second conductive pattern layers in Figure 8 are the same wiring films 15 described for first conductive pattern layers of Element 1[b] (§VII.F1.c), but *below* the insulating material layer. Ex-1002, ¶235. Shield section 28 is the claimed second metal plate. *See supra* §VII.F1.c; Ex-1002, ¶235.

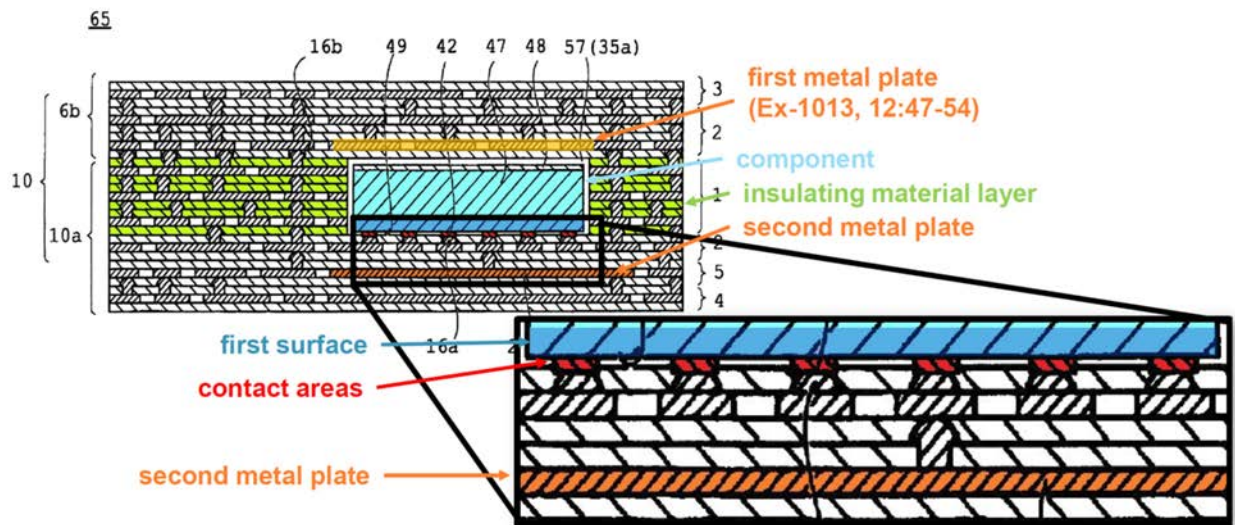
FIG. 7



- e. Element 1[d]: a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface**

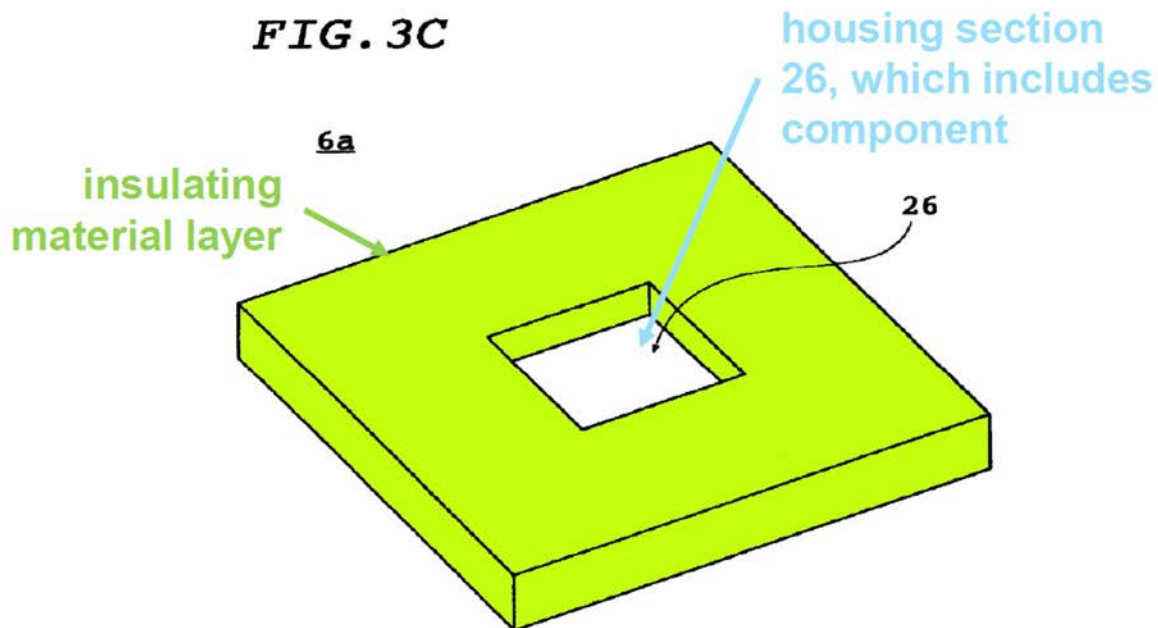
Kurita discloses Element 1[d]. Ex-1002, ¶¶236-39.

As shown below in Figure 7, the component is semiconductor device 47 (light blue), which is inside insulating material layer (light green) and between first and second metal plates (orange). Ex-1002, ¶¶237.



As shown above, the first surface (dark blue) of semiconductor 47 faces the second metal plate and includes contact areas (red). Ex-1002, ¶238. The contact areas are bonding pads 42, which face the bottom of housing 57. Ex-1013, 9:18-25.

The insulating material layer forms a housing section 26 as shown in Figure 3C and, semiconductor device 47 (which resides in housing section 26) is located “inside the insulating material layer” as required by Element 1[d]. Ex-1013, 9:6-11, 12:16-17; Ex-1002, ¶239.



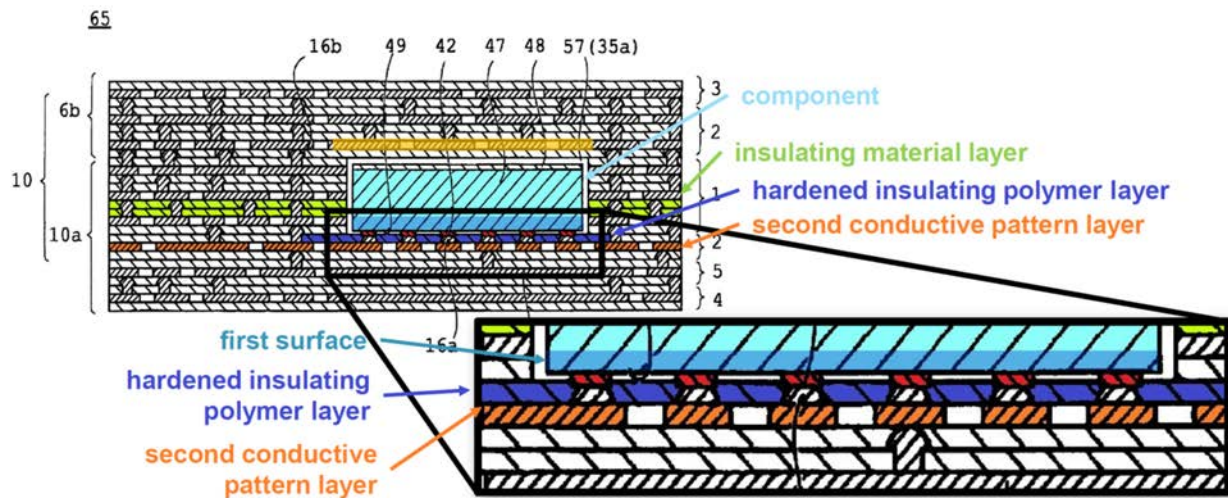
- f. **Element 1[e]: a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and**

Kurita discloses Element 1[e]. Ex-1002, ¶¶240-42.

The hardened insulating polymer film is adhesive film 21 at the bottom of housing section 57. Ex-1013, 9:29-36, 12:16-30; Ex-1002, ¶241. As shown below,

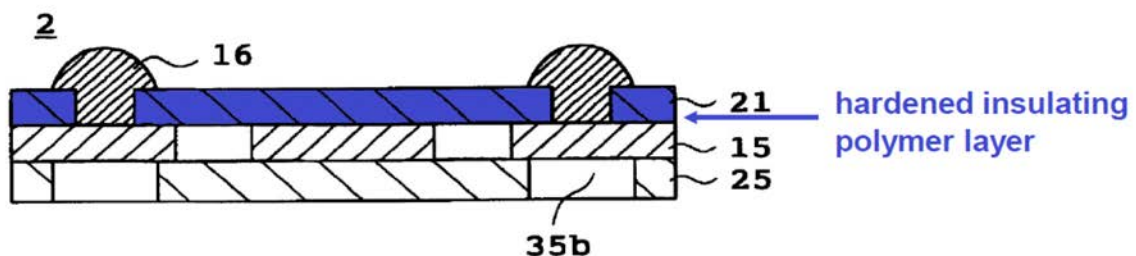
the hardened insulating polymer layer (dark blue) is located between the first surface of the component (semiconductor 47) and at least one second conductive pattern layer (wiring film 15). Ex-1013, 12:24-28; Ex-1002, ¶241.

FIG. 7



The hardened insulating polymer layer in Figure 7 corresponds to adhesive layer 21 in Figure 2A, which is a thermoplastic formed from heating polyimide resin to become adhesive. Ex-1013, 6:42-50, 7:62-8:6. Thus, adhesive layer 21 is a hardened insulating polymer film. Ex-1002, ¶242.

FIG. 2A

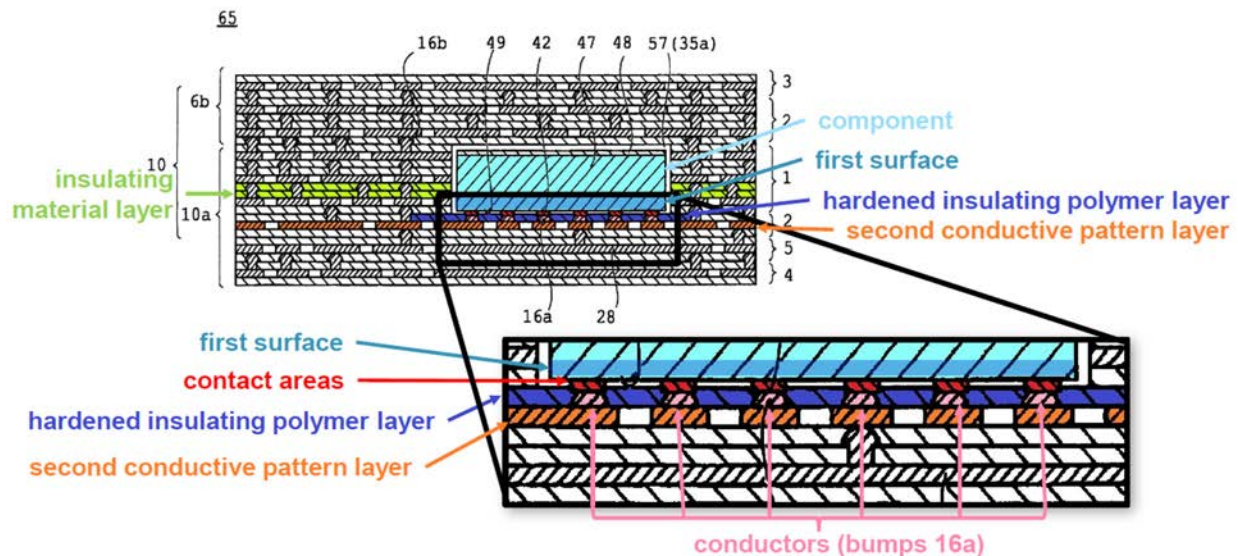


- g. **Element 1[f]: contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one second conductive pattern layer or layers**

Kurita discloses Element 1[f]. Ex-1002, ¶¶243-244.

The “conductors in the contact opening” are bumps 16a in openings of adhesive layer 21 (the hardened insulating polymer layer) at the bottom of housing 57. Ex-1013, 9:21-36; Ex-1002, ¶244. Bumps 16a form electrical contacts between the contact areas (bonding pads 42) and at least one second conductive pattern layer (wiring film 15). Ex-1013, 12:24-28.

FIG. 7

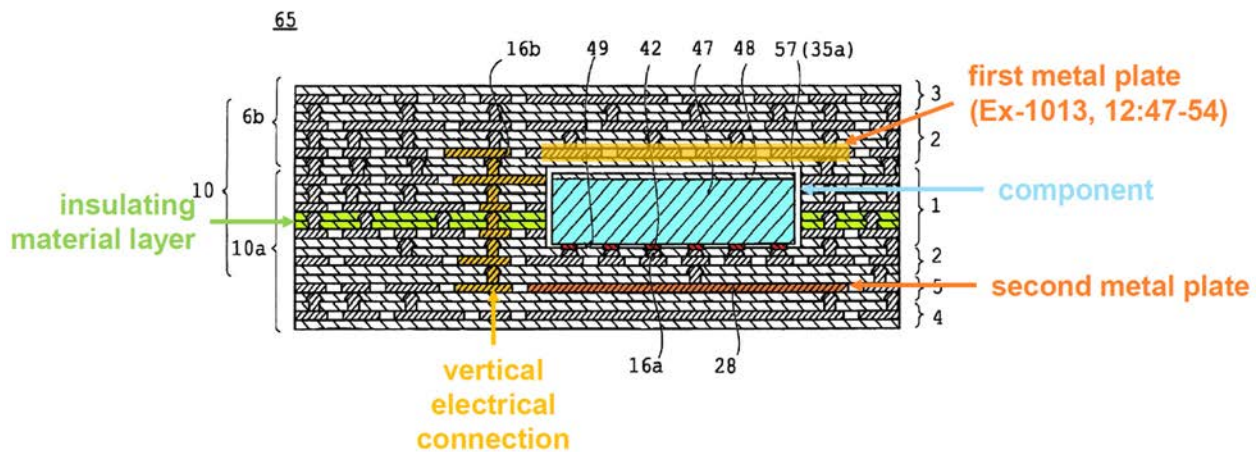


2. **Dependent Claim 2: The circuit board of claim 1, wherein the first and second metal plates are electrically connected to each other.**

Kurita renders obvious Claim 2. Ex-1002, ¶¶245-46.

Kurita teaches that shield sections 28 should be connected to ground to shield EMI. Ex-1013, Abstract, 4:1-9, 5:24-30, 12:40-50. A POSITA would have understood that the grounded elements in Kurita's circuit board are connected to the same ground (*e.g.*, a ground plane); thus, connecting shield sections 28 on both sides of semiconductor device 47 to ground (as taught in Kurita) would connect them to each other. Ex-1002, ¶246. A POSITA would have understood that wiring patterns in Figure 7 could be modified to connect shield sections 28 to the vertical electrical connection identified below and thus connecting them to each other. *Id.*

FIG. 7



3. Dependent Claim 3: The circuit board of claim 1, wherein the first and second metal plates are electrically connected to an earth connection of the circuit board.

Kurita discloses Claim 3. Ex-1002, ¶¶247-49. Kurita teaches that shield sections 28 should be connected to ground to shield EMI. Ex-1013, Abstract, 4:1-9, 5:24-30, 12:40-50.

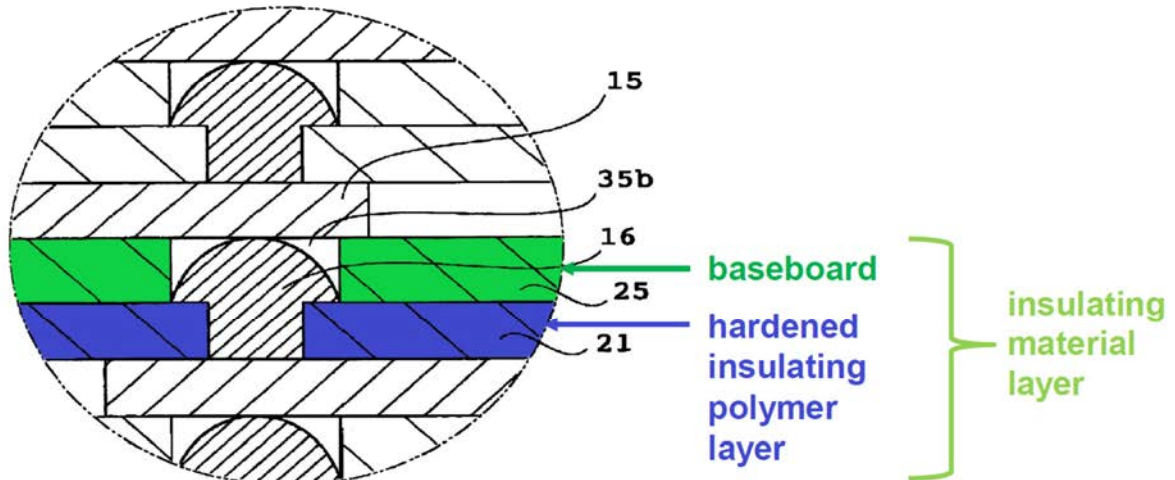
4. Dependent Claim 8: The circuit board of claim 1, wherein the insulating material layer includes a baseboard and the hardened insulating polymer layer.

Kurita discloses Claim 8. Ex-1002, ¶¶250-51.

Claim 8 redefines insulating material layer to include a baseboard and the hardened insulating polymer layer. In Kurita, the baseboard is resin film 25, and the hardened insulating polymer layer is adhesive layer 21.¹² Ex-1002, ¶251. These layers are stacked and adjacent to one another, as shown in Figure 3. *Id.*

¹² Adhesive layer 21 and resin film 25 are described above for Element 1[a] (§VII.F.1.b).

FIG. 3A



5. **Dependent Claim 11: The circuit board of claim 1, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.**

Kurita discloses Claim 11. Ex-1002, ¶¶252-53. As described for Element 1[f] (§VII.F.1.g), the “conductors in the contact opening” are bumps 16a in openings of adhesive layer 21 at the bottom of housing section 57. Bumps 16a are electrochemically deposited copper. Ex-1013, 6:14-24.

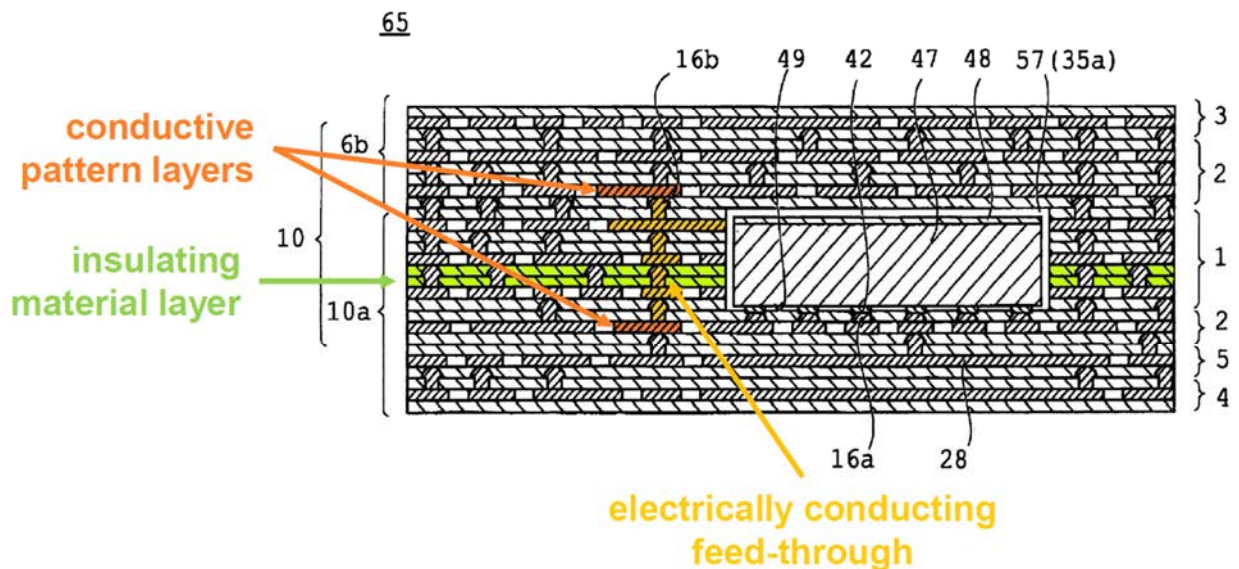
6. **Dependent Claim 13: The circuit board of claim 1, wherein the component is a microcircuit.**

Kurita discloses Claim 13. Ex-1002, ¶¶254-56. As described for Element 1[d] (§VII.F.1.e), the claimed component is semiconductor device 47, which is a microcircuit. Ex-1013, 12:6-7; Ex-1002, ¶255.

- 7. Dependent Claim 14: The circuit board of claim 1, comprising an electrically conducting feed-through between the conductive pattern layers on the both sides of the insulating material layer.**

Kurita discloses Claim 14. Ex-1002, ¶¶259-61. As shown below, Figure 7 includes electrically conducting feed-throughs between the conductive pattern layers on the both sides of the insulating material layer. Ex-1002, ¶¶260.

FIG. 7



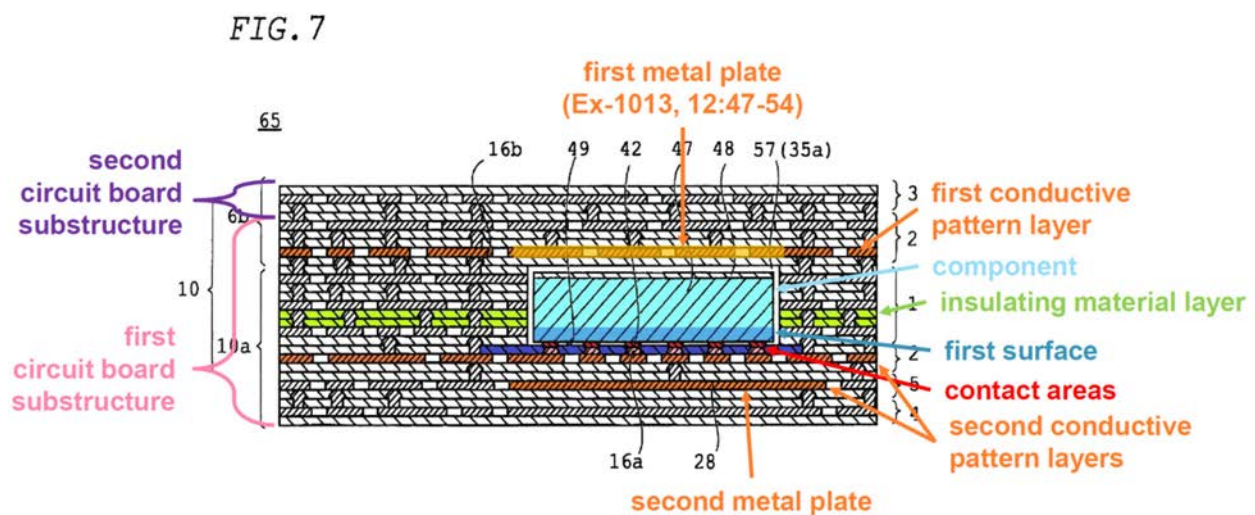
The electrically conducting feed-through corresponds to either bumps 16a in the insulating material layer or a combination of bumps 16a and wiring film 15 between the two conductive pattern layers. Ex-1002, ¶261.

8. Independent Claim 15

Kurita discloses Claim 15. Ex-1002, ¶¶262-65.

As explained for Claim 15 in Ground 1 (§VII.A.1.8), Claim 15 is the same as Claim 1, except for the preamble. Claim 15 requires “a first circuit board substructure and second circuit board substructure on top of each other, wherein at least the first circuit board substructure comprises” the same Elements [a]-[f] as recited in Claim 1. Ex-1002, ¶263.

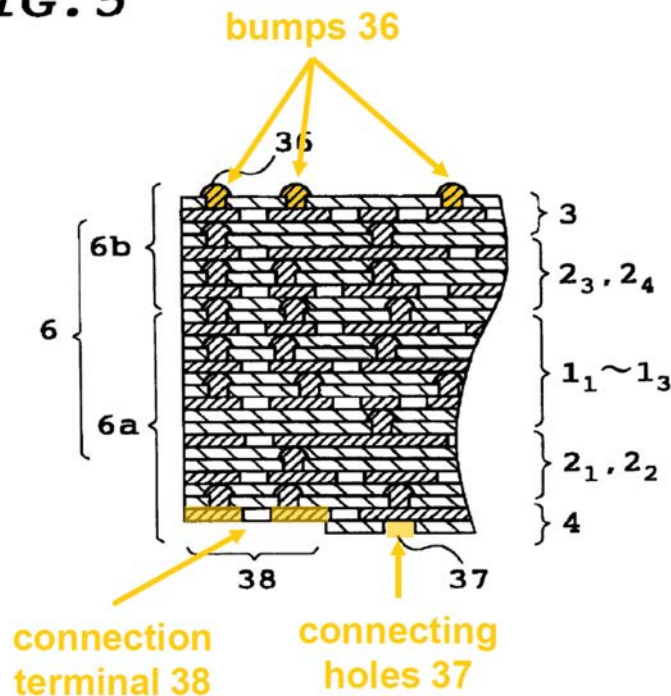
Even if the preamble of Claim 15 is limiting, Kurita discloses Claim 15. Because multi-layer substrate 65 of Figure 7 include multiple layers, the top layer is the second circuit board substructure, and the remaining layers are the first circuit board substructure that meets Elements 15[a]-15[f] as described for Elements 1[a]-1[f] (§VII.F.1). Ex-1002, ¶264.



Alternatively, the multi-layer substrate 65 of Figure 7 is the first circuit board substructure that meets Elements 15[a]-15[f] as described for Elements 1[a]-1[f] (§VII.F.1). Ex-1002, ¶265. Kurita discloses this multi-layer substrate may be connected to “other circuit substrates,” which correspond to the claimed the second circuit board substructure. Ex-1013, 10:13-27; Ex-1002, ¶265. As shown in Figure 5, a multi-layer substrate includes bumps 36 on the top surface and connecting holes 37 or connection terminals 38 on the bottom surface to connect to these other circuit substrates.¹³ Ex-1013, 10:13-27. A POSITA would have been motivated to add a second circuit board substructure to add functionality, reduce manufacturing cost, and save space. Ex-1002, ¶265.

¹³ Kurita discloses or it would have been obvious to POSITA that this teaching for the multilayer substrate in Figure 5 also applies to the multilayer substrate of Figure 7. Ex-1002, ¶265 n.12.

FIG. 5

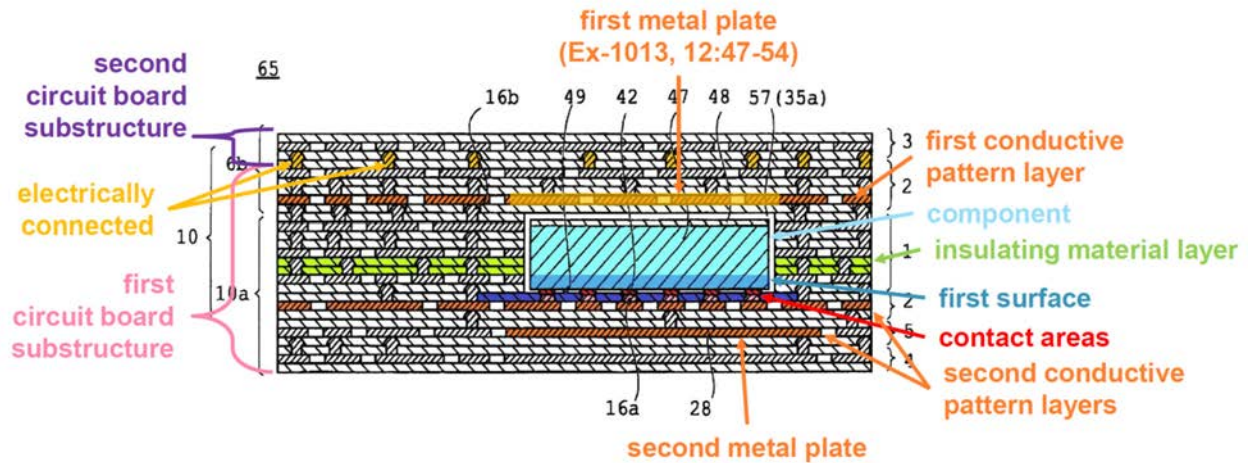


9. **Dependent Claim 16: The multi-layered circuit board of claim 15, wherein said first circuit board substructure and said second circuit board substructure are electrically connected to each other to form a multi-layered functioning totality.**

Kurita discloses Claim 16. Ex-1002, ¶¶266-68.

The first and second circuit board substructures identified for Claim 15 (§VII.F.8) are electrically connected to each other to form a multi-layered functioning totality, as shown below. Ex-1002, ¶267.

FIG. 7

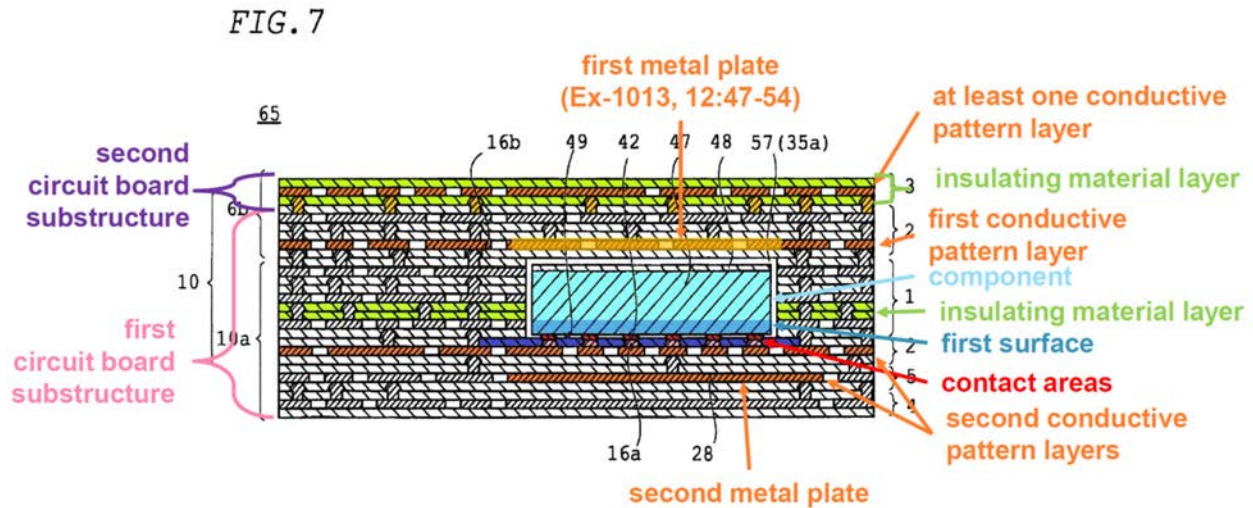


Alternatively, as described for Claim 15 (§VII.F.8), Kurita discloses that a multilayer substrate may be connected on top or bottom to “other circuit substrates.” Kurita states that semiconductor devices and wiring films 15 inside a multilayer substrate can be “electrically connected” to these other circuit substrates. Ex-1013, 10:13-22. Thus, Kurita discloses that the first circuit board substructure (multilayer substrate) and second circuit board substructure (“other circuit substrate”) are electrically connected to each other to form a multi-layered functioning totality. Ex-1002, ¶268.

- 10. Dependent Claim 17: The multi-layered circuit board of claim 16, wherein said second circuit board substructure comprises an insulating material layer and at least one conductive pattern layer in the insulating material layer.**

Kurita discloses and renders obvious Claim 17. Ex-1002, ¶¶269-76.

The second circuit board substructure identified for Claim 15 (§VII.F.8) includes an insulating material layer and at least one conductive pattern layer in the insulating material layer, as shown below. Ex-1002, ¶270.



Alternatively, as described for Claim 15 (§VII.F.8), Kurita discloses that a multilayer substrate may be connected to “other circuit substrates.” Because a multilayer substrate is a “circuit substrate,” Kurita discloses that one multilayer substrate can be connected to another multilevel substrate. Ex-1002, ¶271. At the very least, it would have been obvious to a POSITA that the “other circuit substrates” could be another multilevel substrate. *Id.*

The below diagram depicts connecting one multilayer substrate of Figure 7 to another. Ex-1002, ¶272.

FIG. 7

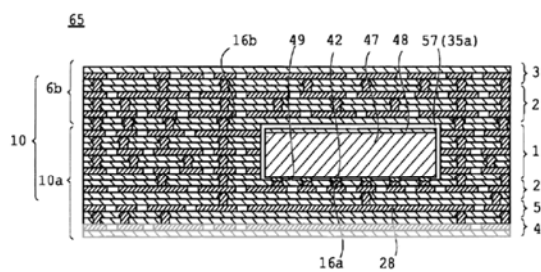
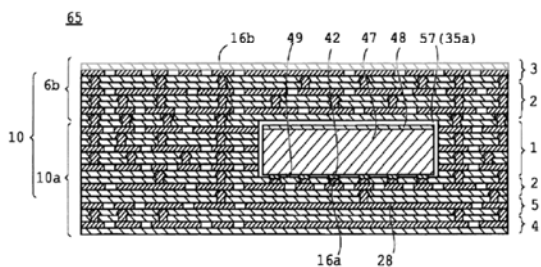
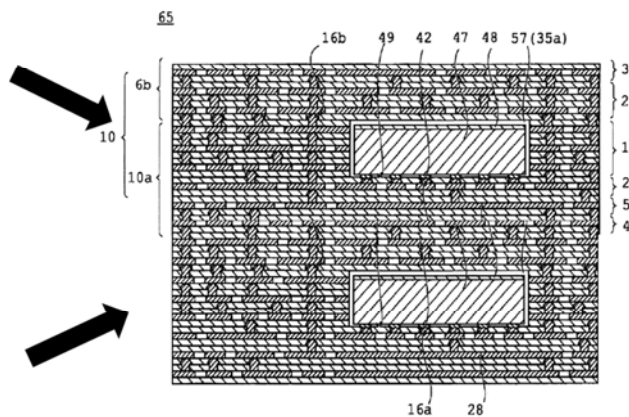
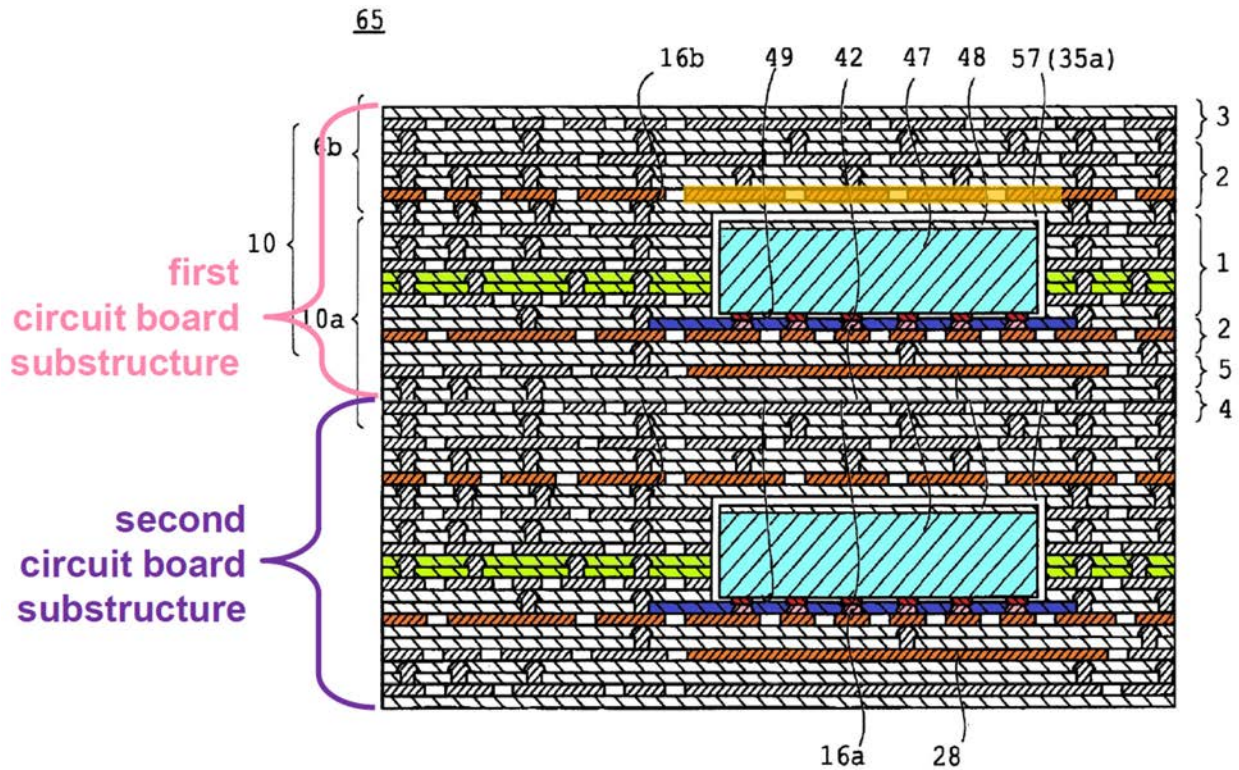


FIG. 7



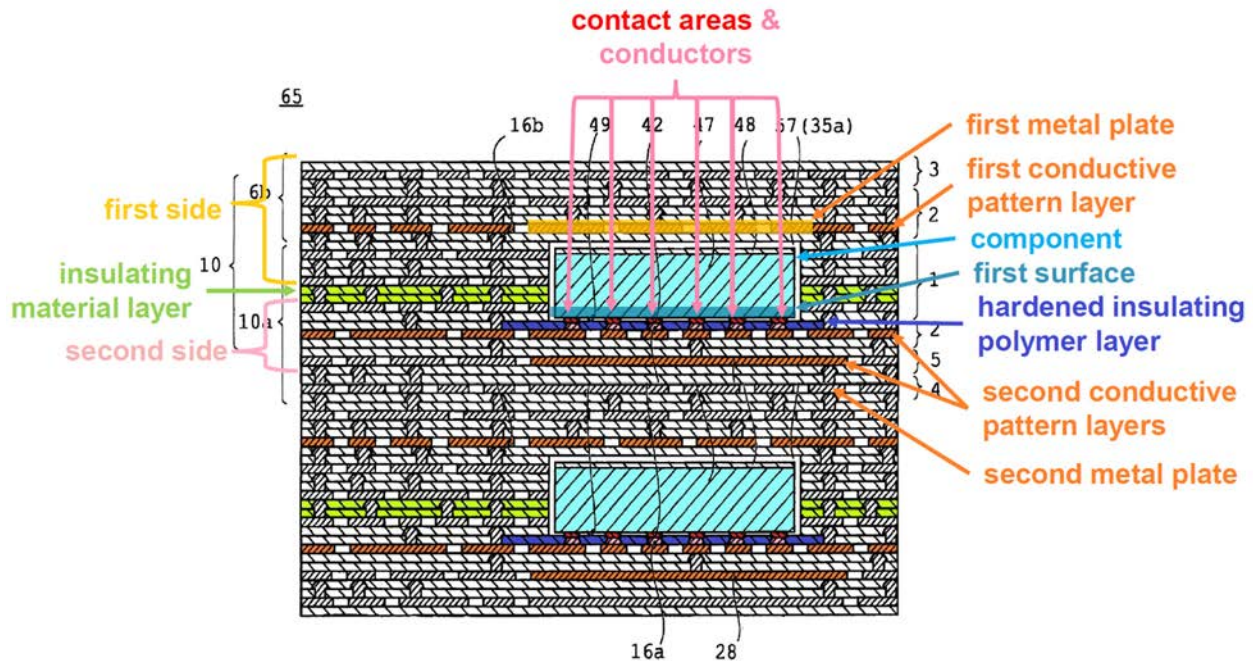
This stacked structure discloses Claim 17.

The following figure identifies the claimed first and second circuit board substructures in this stacked structure. Ex-1002, ¶273.



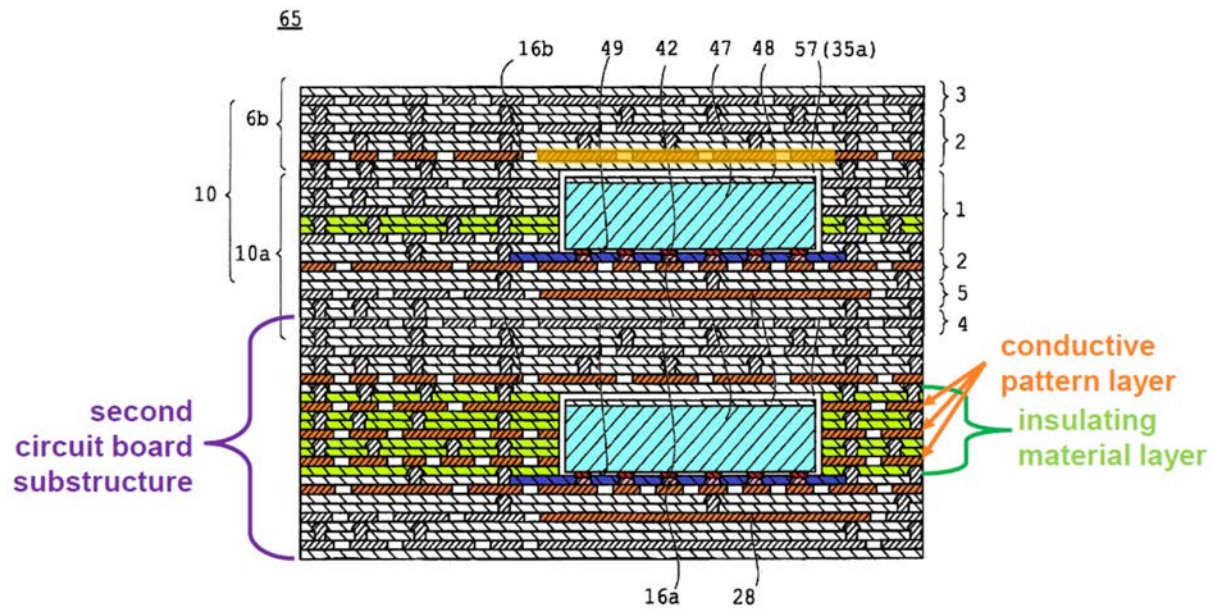
As discussed above in Section VII.A.8, a POSITA would have been motivated to including a metal plate between components 47.

The first circuit board substructure meets Elements 15[a]-15[f] for the reasons described for Elements 1[a]-1[f] (§VII.F.1.a-f), as shown below. Ex-1002, ¶274.



The stacked structure also meets Claim 16. *See supra* VII.F.9.

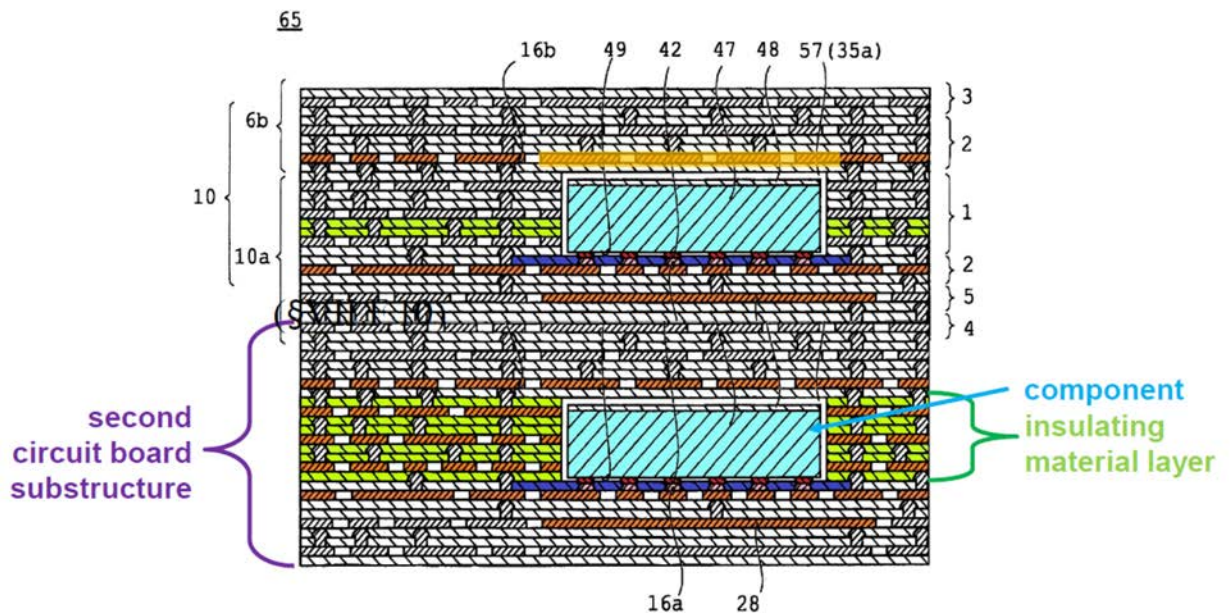
For the reasons described for Elements 1[a]-[c] (Sections VII.F.1.b-d), Kurita discloses and renders obvious that the second circuit board substructure comprises an insulating material layer (resin film 25) and at least one conductive pattern layer (wiring film 15) in the insulating layer, as shown below and recited in Claim 17. Ex-1002, ¶276.



11. **Dependent Claim 18: The multi-layered circuit board of claim 17, wherein said second circuit board substructure includes a component embedded in the insulating material layer.**

Kurita discloses and renders obvious Claim 18. Ex-1002, ¶¶277-78.

For the reasons described for Element 1[d] (§VII.F.1.e), the second circuit board substructure in Claim 17 (§VII.F.10) includes a component (semiconductor device 47) embedded in the insulating material, as shown below. Ex-1002, ¶278.



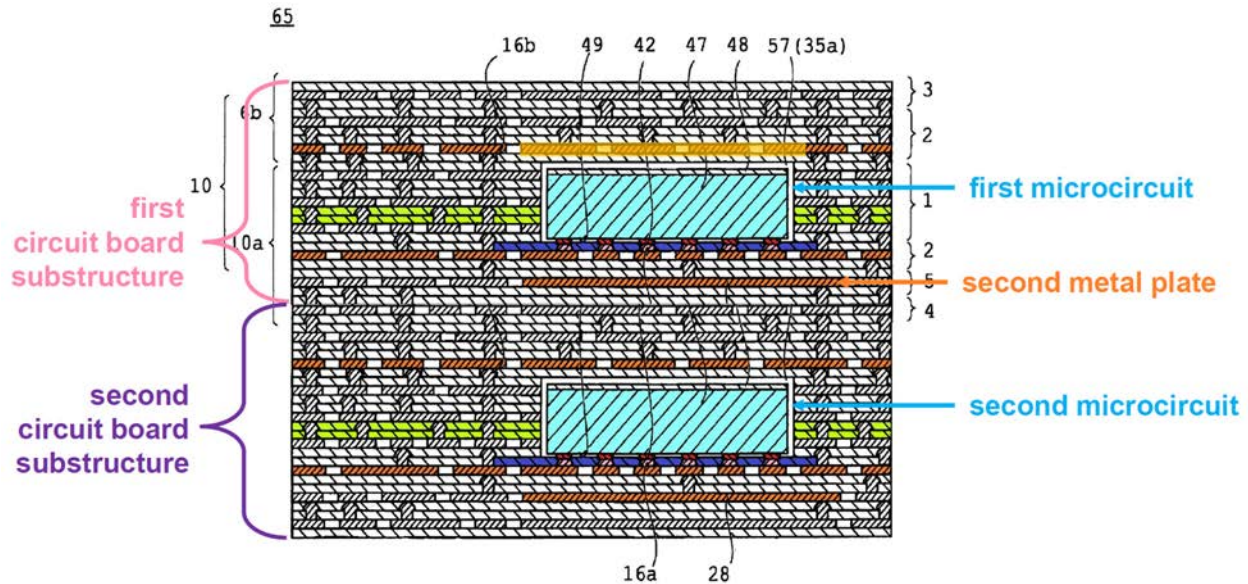
12. **Dependent Claim 19: The multi-layered circuit board of claim 15, wherein said first circuit board substructure comprises a first microcircuit and said second circuit board substructure comprises a second microcircuit such that the first and second microcircuits are on top of each other and at least one of the first and second metal plates is located between said first and second microcircuits.**

Kurita discloses and renders obvious Claim 19. Ex-1002, ¶¶279-82.

As described for Claim 17 (§VII.F.10), Kurita discloses or renders obvious connecting one multilayer substrate of Figure 7 to another, and the resulting stacked structure satisfies Claim 15. Ex-1002, ¶280.

Additionally, the first circuit board substructure comprises a first microcircuit (semiconductor device 47) and the second circuit board substructure comprises a second microcircuit (semiconductor device 47) such that the microcircuits are on top

of each other and at least one of the first and second metal plates is located between the microcircuits, as recited in Claim 19. Ex-1002, ¶281.



13. Dependent Claim 20

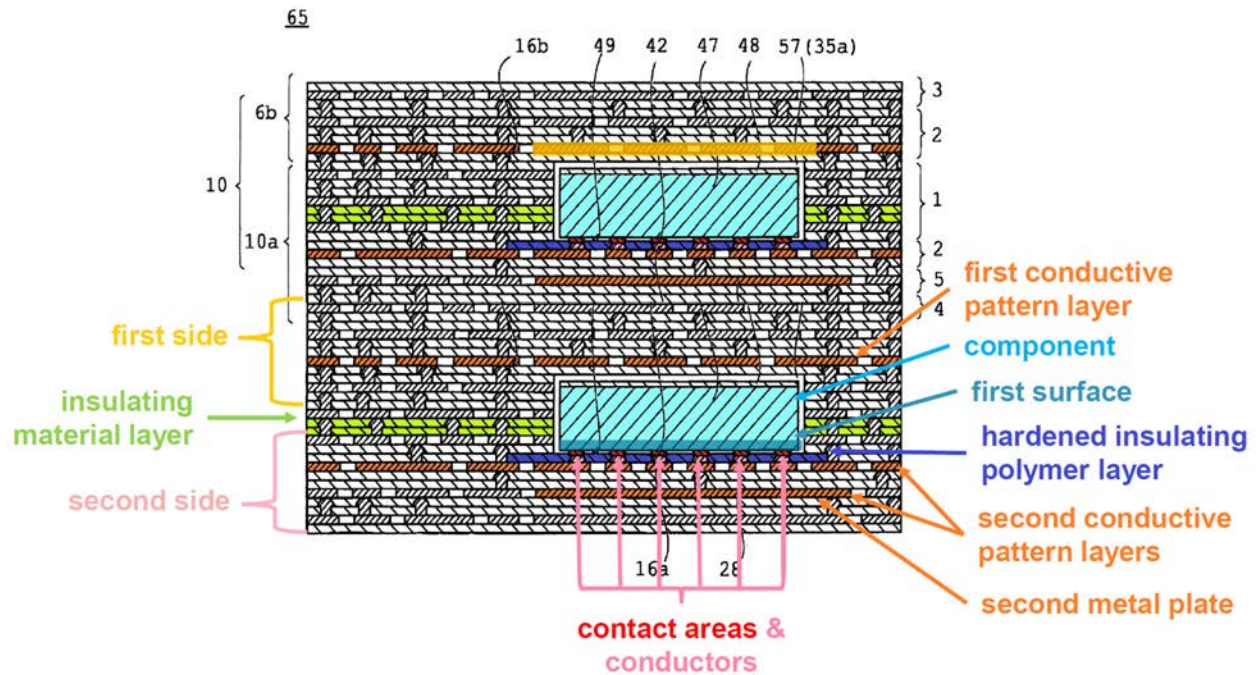
Kurita discloses and renders obvious Claim 20. Ex-1002, ¶¶283-86.

Claim 20 requires that the second circuit board substructure include all elements of Claim 1, except the **first** metal plate. *Compare* Elements 20[a]-[f] with Elements 1[a]-[f]; Ex-1002, ¶284.

As described for Claim 17 (§VII.F.10), Kurita discloses or renders obvious connecting one multilayer substrate of Figure 7 to another, and the resulting stacked structure satisfies Claim 15. Ex-1002, ¶285.

Also for the reasons described for Elements 1[a]-1[f] (§VII.F.1.a-f), the second circuit board substructure meets Elements 20[a]-20[f], as shown below.

Ex-1002, ¶286.



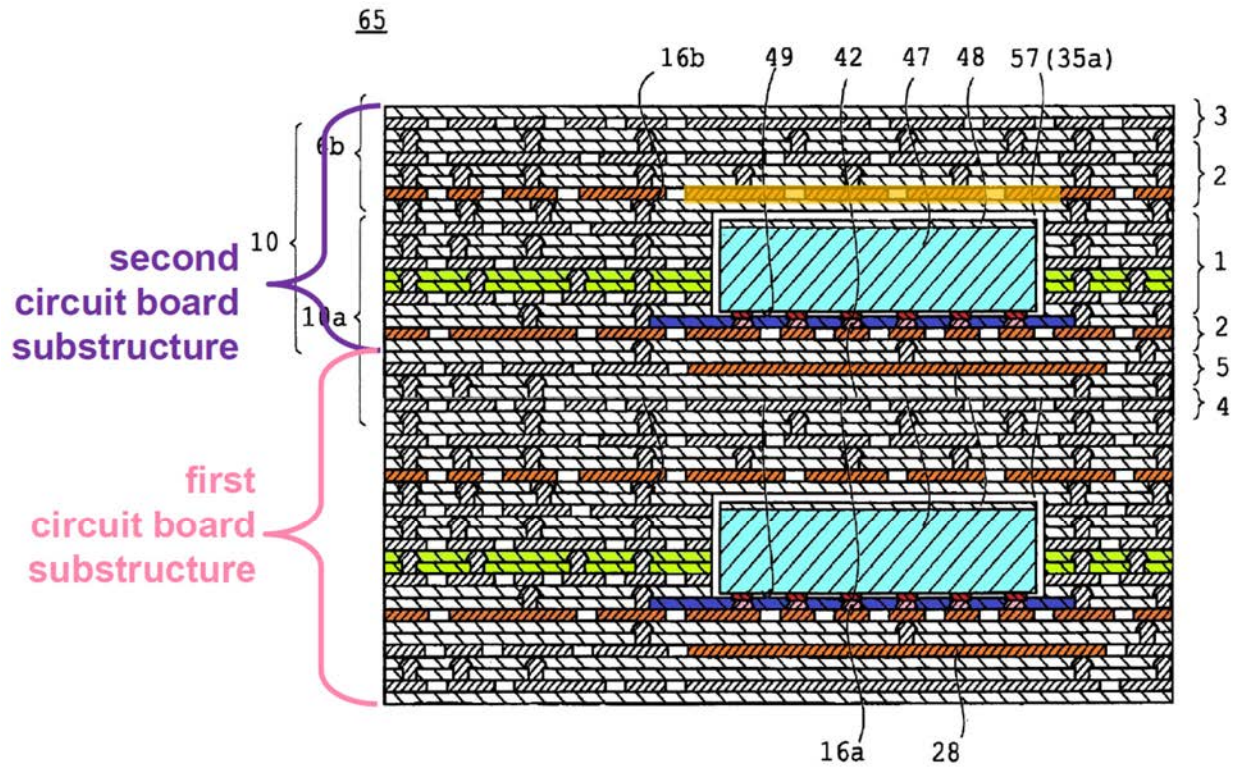
14. Dependent Claim 21

Kurita discloses and renders obvious Claim 21. Ex-1002, ¶¶287-93.

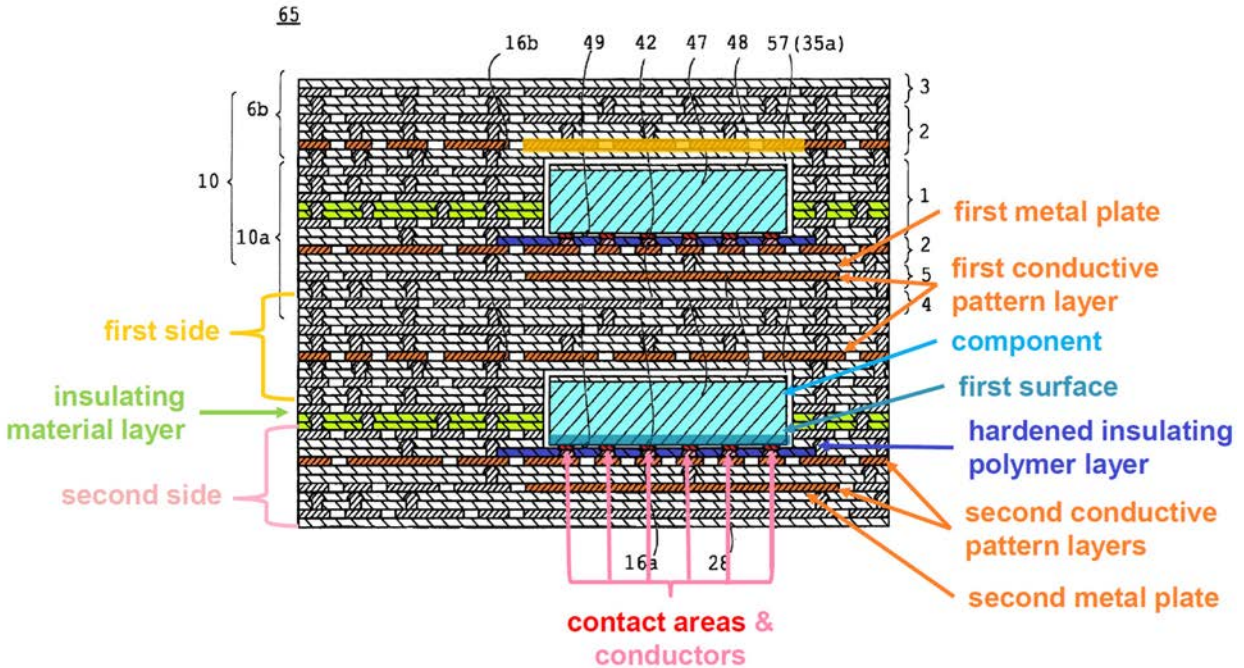
Claim 21 is like Claim 20, with one small difference. Ex-1002, ¶288. Claim 21 requires that the second circuit board substructure include all elements of Claim 1, except the **second** metal plate. Compare Element 21[a]-[f] with Elements 1[a]-[f]; Ex-1002, ¶288.

As described for Claim 17 (§VII.F.10), Kurita discloses or renders obvious connecting one multilayer substrate of Figure 7 to another. Ex-1002, ¶289.

The following figure identifies the claimed first and second circuit board substructures. Ex-1002, ¶290.

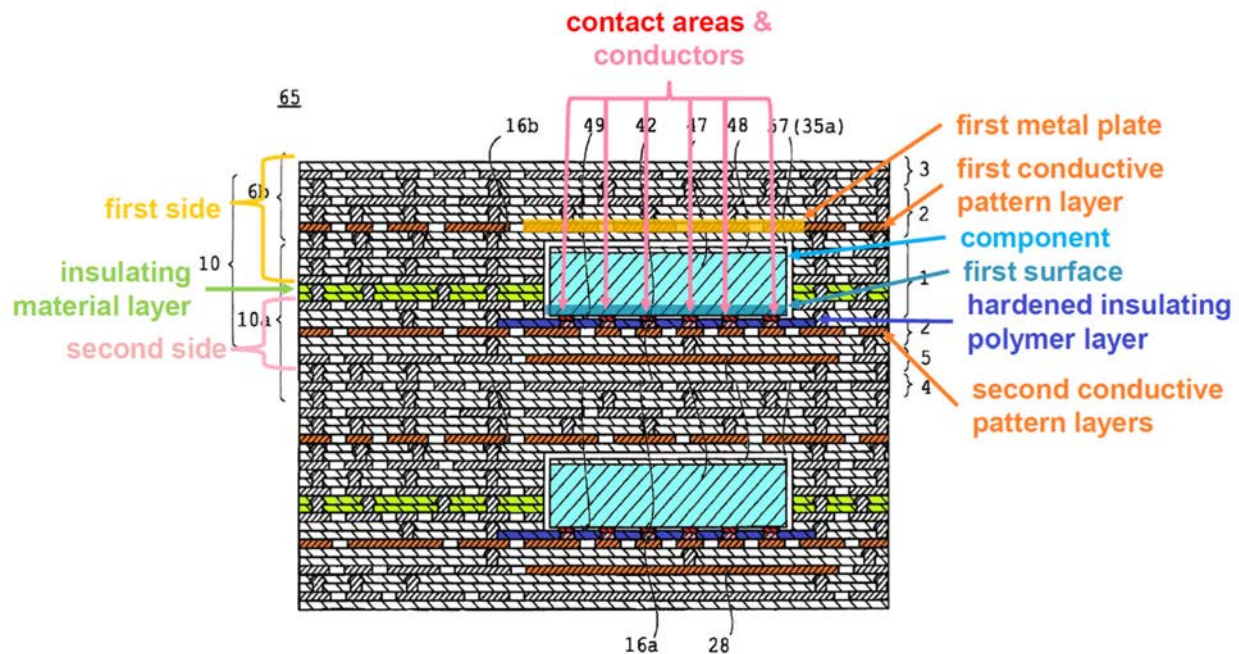


The first circuit board substructure meets Elements 15[a]-15[f] for the reasons described for Elements 1[a]-1[f] (§VII.F.1.a-f), as shown below. Ex-1002, ¶291.



Also for the reasons described for Elements 1[a]-1[f] (§VII.F.1.a-f), the second circuit board substructure meets Elements 20[a]-20[f], as shown below.

Ex-1002, ¶292.



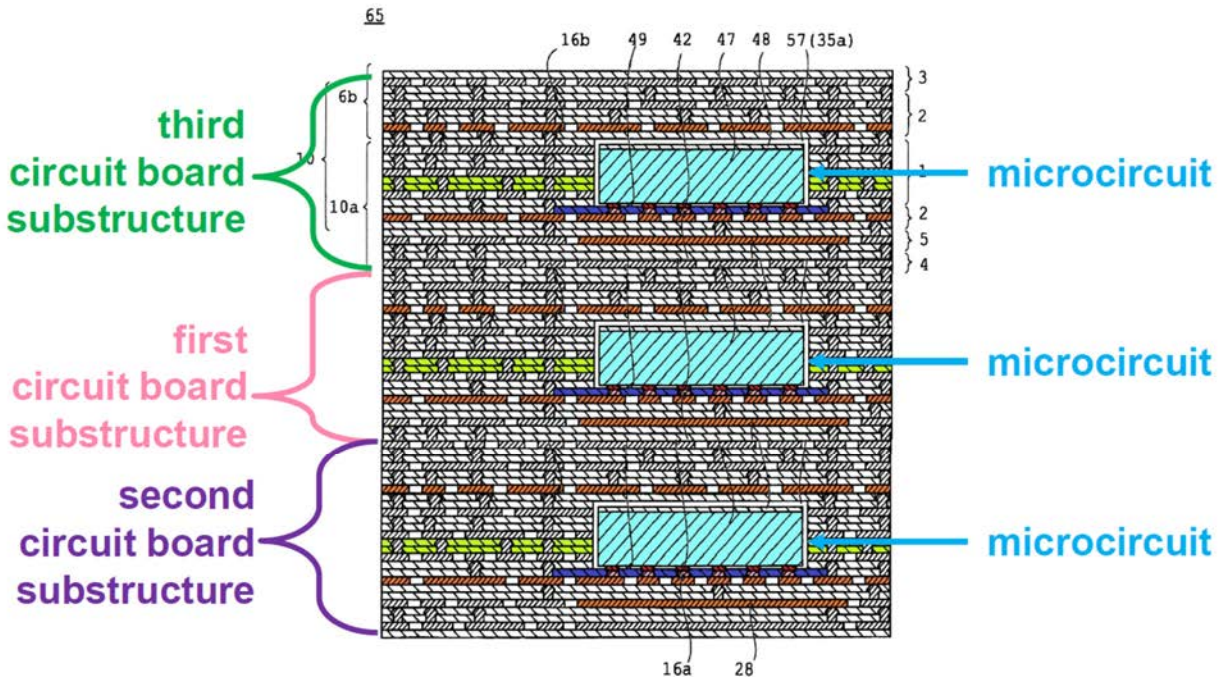
15. Dependent Claims 22: The multi-layered circuit board of claim 15, comprising a third circuit board substructure on top of the first and second circuit board substructures.

Kurita discloses and renders obvious Claim 22. Ex-1002, ¶¶294-97.

As described for Claim 17 (§VII.F.10), Kurita discloses and renders obvious that one multilayer substrate can be connected to another multilevel substrate. Based on the same disclosures and the same motivations, Kurita discloses and renders obvious to POSITA that three multilayer substrates of Figure 7 could be stacked on top of one another. Ex-1002, ¶295.

The below figure shows a stack of three multilayer substrates of Figure 7.

Ex-1002, ¶296.



As shown above, the third circuit board substructure is on top of the first and second circuit board substructures, and thus Kurita discloses or renders obvious Claim 22.

Ex-1002, ¶297.

- 16. Dependent Claim 23: The multi-layered circuit board of claim 22, wherein the first circuit board substructure is between the second and third circuit board substructures.**

Kurita discloses and renders obvious Claim 23 because, as shown above for Claim 22 (§VII.F.15), the first circuit board substructure is between the second and third circuit board substructures. Ex-1002, ¶298.

- 17. Dependent Claim 24: The multi-layered circuit board of claim 22, wherein each of the first, second and third circuit board substructures includes an embedded microcircuit.**

Kurita discloses and renders obvious Claim 24 because, as shown above for Claim 22 (§VII.F.15), the first, second and third circuit board substructures include an embedded microcircuit. Ex-1002, ¶299-300.

- 18. Dependent Claims 25: The multi-layered circuit board of claim 15, wherein the first and second metal plates are electronically connected to each other.**

Claim 25 is the same as Claim 2 but depends from Claim 15. For the reasons described for Claim 2 (§VII.F.2) and Claim 15 (§VII.F.8), Imoto renders obvious Claim 25. Ex-1002, ¶301.

- 19. Dependent Claim 26: The multi-layered circuit board of claim 15, wherein the first and second metal plates are electrically connected to each other.**

Claim 26 is the same as Claim 2 but depends from Claim 15. For the reasons described for Claim 2 (§VII.F.2) and Claim 15 (§VII.F.8), Imoto renders obvious Claims 26. Ex-1002, ¶302.

- 20. Dependent Claim 29: The multi-layered circuit board of claim 15, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.**

Claim 29 is the same as Claim 11 but depends from Claim 15. As described for Claim 11 (§VII.F.5) and Claim 15 (§VII.F.8), Kurita discloses and renders obvious Claim 29. Ex-1002, ¶303.

21. Dependent Claim 30: The multi-layered circuit board of claim 15, wherein the component is a microcircuit.

Claim 30 is the same as Claim 13 but depends from Claim 15. As described for Claim 13 (§VII.F.6) and Claim 15 (VII.F.8), Kurita discloses and renders obvious Claim 30. Ex-1002, ¶304.

22. Dependent Claims 31: The multi-layered circuit board of claim 15, wherein the first circuit board substructure comprises at least two microcircuits inside the insulating material layer.

Kurita discloses and renders obvious Claim 22. Ex-1002, ¶¶305-307. Kurita discloses or renders obvious the first circuit board substructure including at least two microcircuits inside the insulating material layer. Ex-1013, 10:36-44 (describing embedding “a plurality of semiconductor devices” in a multilayer substrate); Ex-1002, ¶¶305-307.

G. Ground 7: Claims 4-7, 10, 27, 28, and 32-36 are obvious over Kurita in view of Dudderar.

1. A POSITA would be motivated to combine Kurita and Dudderar’s teachings and would have a reasonable expectation of success.

A POSITA would have been motivated to combine the teachings of Kurita and Dudderar and would have had a reasonable expectation of success in doing so, because each relates to the same well-known technologies. Both relate to embedding semiconductor devices within a printed circuit board. Ex-1009, 2:53-54; Ex-1013, 9:6-11, 12:16-17. Both also describe using grounded metallization above and below

semiconductor devices to shield EMI. Ex-1009, 2:63-3:3; Ex-1013, 4:1-9, 5:24-30, 6:62-64, 11:56-63, 12:8-15, 12:40-46. Dudderar further describes extending that metallization to the inner walls of the cavity housing the semiconductor devices. Ex-1009, 4:45-50.

A POSITA would have been motivated to apply this teaching of Dudderar to Kurita by using metallization on the sidewalls of the cavity. Ex-1002, ¶309. Kurita recognized the benefits of using grounded metallization to shield EMI, and based on Dudderar, a POSITA would have recognized that grounded metallization on the sidewalls of Kurita enhances those benefits, producing more reliable chips less likely to malfunction due to EMI. *Id.* Thus, design incentives and market forces would have motivated a POSITA to apply the teachings of Dudderar to Kurita. *Id.*

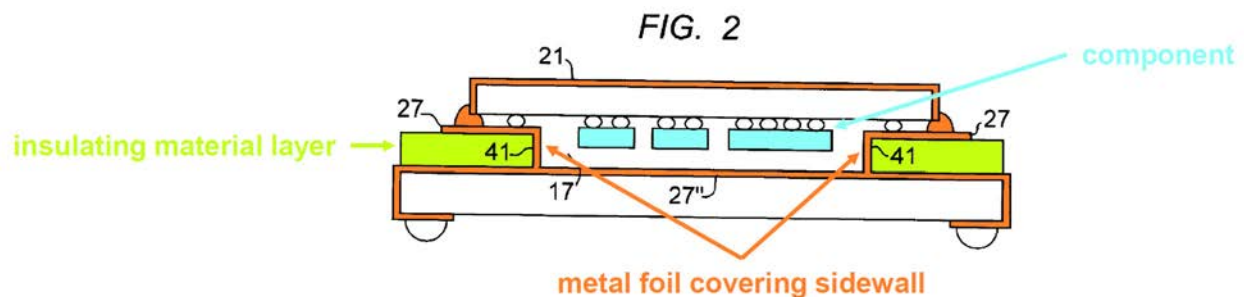
A POSITA would also have had a reasonable expectation of success in combining Kurita and Dudderar. Ex-1002, ¶310. A POSITA would have understood that these references disclose interrelated teachings based on routine technologies and would have been amendable to various well-understood and predictable combinations. *Id.*

2. **Dependent Claim 4: The circuit board of claim 1, wherein the component is located in a hole in the insulating material layer, and the circuit board comprises metal foil covering the sidewalls of the hole and a filler material in the hole between the metal foil and the component.**

Kurita-Dudderar in combination renders obvious Claim 4. Ex-1002, ¶¶311-15.

As described for Element 1[d] (§VII.F.1.e), Kurita discloses a component (semiconductor device 47) in a hole (housing section 57) in the insulating material layer.

It would have been obvious to modify Kurita to include metal foil on sidewalls as Dudderar describes. Ex-1002, ¶313. In Dudderar, sidewalls 41 of chip cavity 17 are covered with grounded metallization for shielding EMI, as shown below. Ex-1009, 4:45-50.



It would have been obvious to a POSITA to apply this teaching to the sidewalls of housing section 57 in Kurita. Ex-1002, ¶314. Kurita recognized the benefit of using grounded metallization to shield EMI, and it would have been obvious to a POSITA

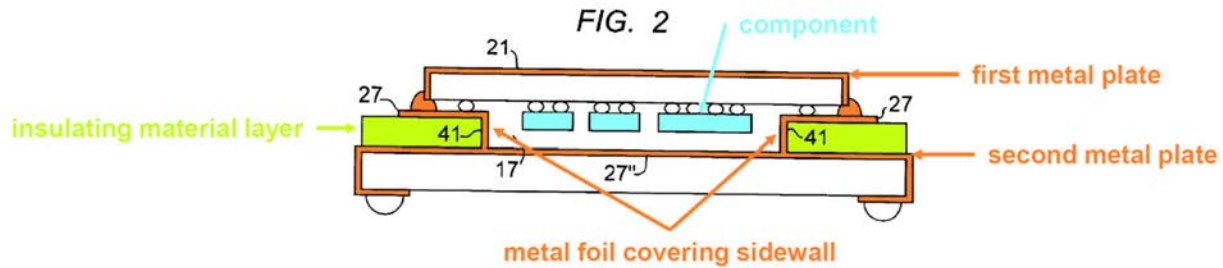
that grounded metallization on the sidewalls of Kurita enhances those benefits, as taught in Dudderar. *Id.*

It also would have been obvious to modify Kurita to include filler material in housing section 57 as Dudderar describes. Dudderar incorporates by reference Degani. *See supra* §V.C.2. Degani discloses the use of an encapsulating material 22/27 in the cavity of a substrate to protect an embedded chip and its interconnections. Degani, 5:63-6:3, 5:25-27. It would have been obvious to a POSITA to apply such encapsulation material to housing section 57 in Kurita to protect semiconductor device 47 and its interconnections. Ex-1002, ¶315.

3. Dependent Claim 5: The circuit board of claim 4, wherein the metal foil is electrically connected to at least one of the first and second metal plates.

Kurita-Dudderar in combination renders obvious Claim 5. Ex-1002, ¶¶316-18.

As explained for Claim 4 (§VII.G.2), it would have been obvious to apply Dudderar to Kurita by covering the sidewalls of housing section 57 with metal foil for shielding EMI. Dudderar also teaches that the metal foil is connected to the first and second metal plates and to ground, as shown below. Ex-1009, 3:28-37, 4:45-50.



Because Kurita also teaches that the metal plates (shield section 28) are connected together to ground (*see supra* §VII.F.2), it would have been obvious to electrically connect metal foil on the sidewalls of housing section 57 to the first and second metal plates and to ground. Ex-1002, ¶318.

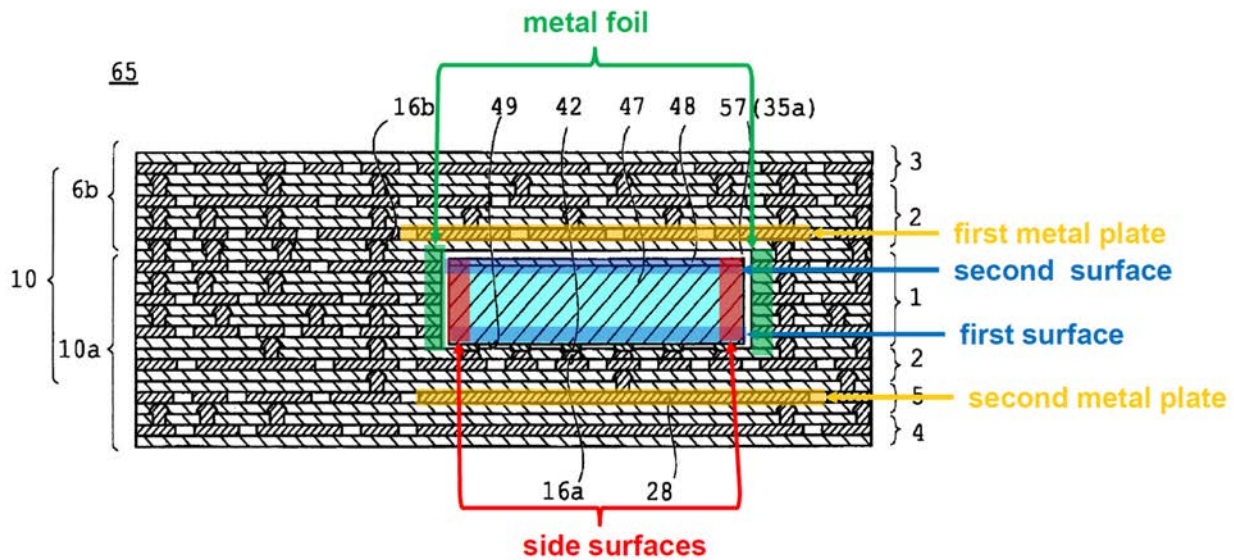
4. Dependent Claim 6: The circuit board of claim 4, wherein the metal foil is electronically connected to an earth connection of the circuit board.

As explained for Claim 5 (§VII.G.3), both Kurita and Dudderar teach connecting metallization to ground to shield EMI. Thus, it would have been obvious to electronically connect metal foil on the sidewalls of Kurita to an earth connection of the circuit board. Ex-1002, ¶319.

5. **Dependent Claim 7: The circuit board of claim 4, wherein the component has a second surface opposite to the first surface and side-surfaces between the first and second surfaces, and wherein the first and second metal plates and the metal foil form an electromagnetic interference shield around the component such that the side-surfaces of the component face towards the metal foil, the first surface of the component face towards the second metal plate, and the second surface of the component face towards the first metal plate.**

As explained for Claim 4 (§VII.G.2), it would have been obvious to apply Dudderar to Kurita by covering the sidewalls of housing section 57 with metal foil to shield EMI. As shown below, Kurita-Dudderar in combination renders obvious Claim 7. Ex-1002, ¶¶320-22.

FIG. 7



6. **Dependent Claim 10: The circuit board of claim 8, wherein the component is located in a hole in the baseboard; and the circuit board comprises conductive material on the sidewalls of the hole and a filler material in the hole between the metal foil and the component, wherein the metal foil creates an interference protection structure around the component.**

Claim 10 combines the elements of Claims 4 and 8. As described for Claims 4 (§VII.G.2) and Claim 8 (§VII.F.4), Kurita-Dudderar in combination renders obvious Claim 10. Ex-1002, ¶¶323-24.

7. **Dependent Claim 27: The multi-layered circuit board of claim 15, wherein the component is located in a hole in the insulating material layer, and the circuit board comprises metal foil covering the sidewalls of the hole and a filler material in the hole between the metal foil and the component.**

Claim 27 is the same as Claim 4 but depends from Claim 15. As described for Claim 4 (§VII.G.2) and Claim 15 (§VII.F.8), Kurita-Dudderar in combination renders obvious Claim 27. Ex-1002, ¶¶325-26.

8. **Dependent Claim 28: The multi-layered circuit board of claim 15, wherein the metal foil is electronically connected to at least one of the first and second metal plates.**

Claim 28 is the same as Claim 5 but depends from Claim 15. As described for Claim 5 (§VII.G.3) and Claim 15 (§VII.F.8), Kurita-Dudderar in combination renders obvious Claim 27. Ex-1002, ¶¶327-28.

9. Independent Claim 32

a. Element 32[preamble]: An electronic module comprising

Kurita discloses a multi-layer substrates including semiconductor devices and thus teaches the preamble of Claim 1, to the extent it is limiting. Ex-0013, 1:6-8, 5:57-58; Ex-1002, ¶329.

b. Element 32[a]: an insulating material layer having a first side and a second side,

Element 32[a] is the same as Element 1[a], and thus Kurita discloses this element as described for Element 1[a] (§VII.F.1.b). Ex-1002, ¶330.

c. Element 32[b]: at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate,

Element 32[b] is the same as Element 1[b], and thus Kurita discloses this element as described for Element 1[b] (§VII.F.1.c). Ex-1002, ¶331.

d. Element 32[c]: at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate,

Element 32[c] is the same as Element 1[c], and thus Kurita discloses this element as described for Element 1[c] (§VII.F.1.d). Ex-1002, ¶332.

- e. **Elements 32[d], [e], [f], and [g]: a hole having sidewalls defined in the insulating material layer and located between the first and second metal plates, a metal foil covering the sidewalls of the hole, a microcircuit inside the hole and having a first surface facing towards the second metal plate, and contact areas on the first surface, a filler material in the hole between the metal foil and the microcircuit,**

Element 32[d], [e], [f], and [g] are the same as Element 1[d], Element 1[e], Claim 4, and Claim 13, and thus, Kurita-Dudderar in combination renders obvious these elements as described for Element 1[d] (§VII.F.1.e), Element 1[e] (§VII.F.1.f), Claim 4 (§VII.G.2) and Claim 13 (VII.F.6). Ex-1002, ¶333.

- f. **Element 32[h]: a hardened insulating polymer layer between the first surface of the microcircuit and at least one conductive pattern of said at least one second conductive pattern layer, and**

Element 32[h] is the same as Element 1[e], and thus Kurita discloses this element as described for Element 1[e] (§VII.F.1.f). Ex-1002, ¶334.

- g. **Element 32[i]: contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the microcircuit and the at least one second conductive pattern layer or layers.**

Element 32[i] is the same as Element 1[f], and thus Kurita discloses this element as described for Element 1[f] (§VII.F.1.g). Ex-1002, ¶335.

- 10. Dependent Claim 33: The electronic module of claim 32, wherein the first and second metal plates are electronically connected to each other.**

Claim 33 is the same of Claim 2 but depends from Claim 32. Thus, as described for Claim 2 (§VII.F.2) and Claim 32 (§VII.G.9), Kurita-Dudderar in combination renders obvious Claim 33. Ex-1002, ¶336.

- 11. Dependent Claim 34: The electronic module of claim 32, wherein the first and second metal plates are electrically connected to an earth connection of the electronic module.**

Claim 34 is the same of Claim 3 but depends from Claim 32. Thus, as described for Claim 3 (§VII.F.3) and Claim 32 (§VII.G.9), Kurita-Dudderar in combination renders obvious Claim 33. Ex-1002, ¶337.

- 12. Dependent Claim 35: The electronic module of claim 32, wherein the metal foil is electronically connected to at least one of the first and second metal plates.**

Claim 35 is the same of Claim 5 but depends from Claim 32. Thus, as described for Claim 5 (§VII.G.3) and Claim 32 (§VII.G.9), Kurita-Dudderar in combination renders obvious Claim 33. Ex-1002, ¶338.

- 13. Dependent Claim 36: The electronic module of claim 32, wherein the metal foil and the first and second metal plates are electronically connected to an earth connection of the electronic module.**

Claim 36 is the same of Claim 3 and 6 but depends from Claim 32. Thus, as described for Claim 3 (§VII.F.3), Claim 6 (§VII.G.4), and Claim 32 (§VII.G.9), Kurita-Dudderar in combination renders obvious Claim 36. Ex-1002, ¶339.

H. Ground 8: Claims 9, 12, and 31 are obvious over Kurita in view of Mowatt.

1. A POSITA would be motivated to combine Kurita and Mowatt's teachings and would have a reasonable expectation of success.

A POSITA would have been motivated to combine the teachings of Kurita and Mowatt and would have had a reasonable expectation of success in doing so, because each relates to the same well-known technologies. Ex-1002, ¶340. Both relate to embedding semiconductor devices within a printed circuit board. Ex-1010, 9:40-43; Ex-1013, 9:6-11, 12:16-17. A POSITA would have understood that these references disclose interrelated teachings based on routine technologies and would have been amendable to various well-understood and predictable combinations. Ex-1002, ¶340.

2. Dependent Claims 9: The circuit board of claim 8, wherein the baseboard is a glass-fibre reinforced epoxy board.

Kurita-Mowatt in combination renders obvious Claim 9. Ex-1002, ¶¶341-42.

As described for Claim 8 (§VII.F.4), the baseboard in Kurita is resin film 25, which is “formed of polyimide film by hardening of the precursor coat 23.” Ex-1013, 7:25-27. Like Kurita, Mowatt describes embedding semiconductor devices within a baseboard. Ex-1010, 9:40-43. Mowatt teaches that the baseboard could include “an *epoxy glass material*, or polyimide glass material, teflon or other materials commonly used in PWB fabrication.” Ex-1010, 4:40-43 (emphasis added).

It would have been obvious to POSITA to apply this teaching to Kurita so that the baseboard is a glass-fibre reinforced epoxy board. Ex-1002, ¶342. A POSITA would have been motivated to use glass-fibre reinforced epoxy boards to increase the rigidity and stability of the substrates. *Id.*

3. Dependent Claim 12: The circuit board of claim 1, wherein the hardened insulating polymer layer contains epoxy.”

Kurita-Mowatt in combination renders obvious Claim 12. Ex-1002, ¶¶343-46.

As described for Element 1[e] (§VII.F.1.f), the hardened insulating polymer layer in Kurita is adhesive layer 21, which is a thermoplastic formed from heating polyimide resin to become adhesive. Ex-1013, 6:42-50, 7:62-8:6.

Like Kurita, Mowatt teaches the use of a polyimide resin between layers in a multilayer circuit board. Ex-1010, 7:18-30. In particular, Mowatt teaches the use of a “thermoset adhesive such as Siloxide Polyimide epoxy.” Ex-1010, 7:24-25.

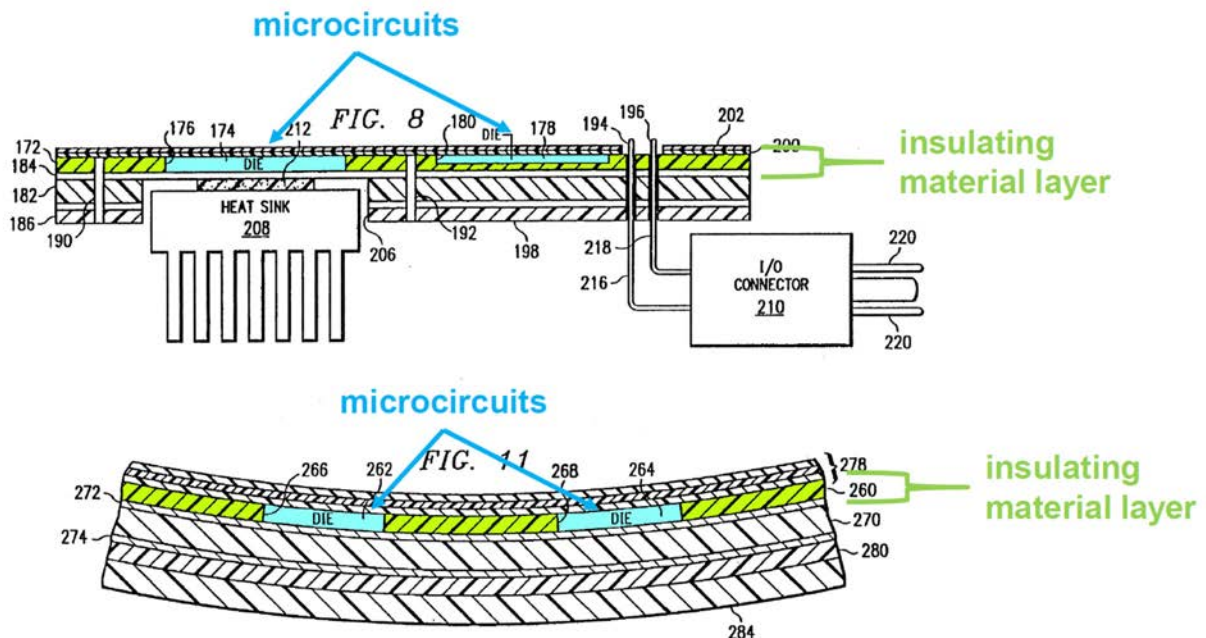
It would have been obvious to a POSITA to apply this teaching to Kurita so that adhesive layer 2 is a polyimide resin containing epoxy. Ex-1002, ¶346. Thus, Kurita-Mowatt in combination renders obvious that the hardened insulating polymer layer (adhesive layer 21) contains epoxy. *Id.*

4. Dependent Claims 31: The multi-layered circuit board of claim 15, wherein the first circuit board substructure comprises at least two microcircuits inside the insulating material layer

Kurita alone discloses and renders obvious Claim 31. *See supra* §VII.F.22.

Alternatively, Kurita-Mowatt in combination renders obvious Claim 31.

Ex-1002, ¶¶348-50. Mowatt discloses two microcircuits inside the same insulating material layer, as shown below in Figures 8 and 11. *See supra* §VII.C.3



In view of Figure 8 and 11 of Mowatt and the additional teachings of Kurita (§VII.F.21), it would have been obvious to a POSITA that at least two microcircuits (semiconductor devices 47) can be embedded in an insulating material layer. Ex-1002, ¶350. A POSITA would have been motivated to add a microcircuit to increase functionality, to reduce manufacturing costs, and to save space.

VIII. THE BOARD SHOULD NOT USE ITS DISCRETION TO DENY INSTITUTION UNDER *FINTIV*.

The Board should decline to exercise its discretion to deny institution under 35 U.S.C. § 314(a). While Director Vidal’s June 21, 2022 Guidance made clear that “*Fintiv* is limited to facts of that case,” for completeness, Petitioner addresses the factors set forth in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential). As explained below, the six factors set out in *Fintiv* do not justify denying institution.

The **first *Fintiv* factor** is neutral here because Samsung has not yet moved to stay the district court proceedings pending IPR, and the PTAB will not infer how the district court would rule should a stay be requested. *See, e.g., Hulu LLC v. SITO Mobile R&D IP, LLC et al.*, IPR2021-00298, Paper 11 at 10-11 (PTAB May 19, 2021).

For the **second *Fintiv* factor**, the district court has not set a trial date in the *Samsung* matter. Speculating based on prior practice in Judge Gilstrap’s Court, the earliest estimated trial date is approximately June 2024. Even if trial proceeds in April 2024, the above timing does not tip in favor of denying the petition in this case. *See, e.g., Apple Inc. v. Koss Corp.*, IPR2021-00305, Paper 14 at 13 (PTAB June 3, 2021). This Petition is filed in December 2022. An institution decision should be issued within six months of docketing, around June 2023. And a final written

decision (FWD) should be issued in June 2024. Thus, the ***earliest*** estimated trial date is around the same time as the FWD. Recent PTAB cases analyzing similar schedules have weighed the second factor as neutral or, at most, slightly in favor of denial. *See, e.g., Google LLC et al. v. Parus Holdings, Inc.*, IPR2020-00847, Paper 9 at 12 (PTAB Oct. 21, 2020) (trial scheduled for three months before FWD weighs “at best, neutral”); *Apple Inc. v. Koss Corp.*, IPR2021-00305, Paper 14 at 13-14 (PTAB June 3, 2021) (trial scheduled for two months before FWD weighs “at most, minimally in favor” of denial).

On the other hand, if the median time to trial for civil actions in the Eastern District of Texas is used to estimate the trial date, as advised by Director Vidal’s June 2022 Guidance, trial should not be expected to occur until August 2024, at least a month *after* a FWD will issue, Ex-1021, 35 (indicating a most-recent median time to trial for civil actions in the Eastern District of Texas of 24.5 months).

The **third *Fintiv* factor** weighs strongly against denial. Samsung has not yet answered ImberaTek’s Complaint, and has instead moved to dismiss the complaint for lack of standing and pre-suit notice. No hearing has been set and no substantive activity has occurred in the case. The Case Management Conference is scheduled for January 2024. Because the investment in the trial has been minimal and Petitioner acted diligently, this factor weighs strongly against discretionary denial. *See, e.g., Hulu*, Paper 11 at 13.

The **fourth *Fintiv* factor** also weighs against denial. As explained above, the median time to trial for civil actions in the Eastern District of Texas suggests that trial will not occur until at least a month after a FWD. Thus, “there is a reasonable likelihood that the Board will address the overlapping validity issues prior to the district court reaching them at trial..., thereby providing the possibility of simplifying issues for trial.” *Juniper Networks, Inc. v. Packet Intelligence LLC*, IPR2020-0039, Paper 21 at 18 (PTAB Sept. 10, 2020); *see also MED-EL Elektromedizinische Geraete GmbH v. Sonova AG*, IPR2020-00176, Paper 13 at 15 (PTAB June 3, 2020) (“[O]verlap exists between the invalidity issues in this case and in the district court. This overlap may inure to the district court’s benefit, however, by simplifying issues for trial should we reach our determination on the challenges raised in the Petition before trial.”).

On the **fifth *Fintiv* factor**, the Board should give little weight to the fact that Petitioner and PO are the same parties as in district court. *See Weatherford U.S., L.P., v. Enventure Global Tech., Inc.*, Paper 16 at 11-13 (PTAB April 14, 2021). Although Samsung is both petitioner and litigation defendant, this factor does not outweigh the other factors that strongly weigh against discretionary denial.

“Other circumstances” under the **sixth *Fintiv* factor** further weigh against discretionary denial. The merits of the Petition are especially strong. *See Align*

Technology, Inc. v. 3Shape A/S, IPR2020-01087, Paper 15 at 42-43 (PTAB Jan. 20, 2021). *See supra* §VII.

Taken together holistically, the *Fintiv* factors strongly weigh against denial.

IX. CONCLUSION

Petitioner requests institution of IPR for Claims 1-36 of the '944 Patent based on each of the grounds in this Petition.

Respectfully Submitted,

/s/ John Kappos

John Kappos (Reg. No. 37,861)

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Petitioner certifies that this petition includes 13,999 words, as measured by Microsoft Word, exclusive of the table of contents, mandatory notices under § 42.8, certificates of service, word count, and exhibits.

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned certifies pursuant to 37 C.F.R. §§42.6(e) and 42.105 that on December 9, 2022, a true and correct copy of the Petition For *Inter Partes* Review Of U.S. Patent No. 7,989,944 and Exhibits 1001 through 1025 were served via express mail on the Patent Owner at the below correspondence address of record:

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