AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas, Waco Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:22-cv-00105	1/27/2022	Western District of Texas, Waco Division

PLAINTIFF	DEFENDANT
GREENTHREAD, LLC	INTEL CORPORATION, DELL INC., AND DELL TECHNOLOGIES INC.,

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	8,421,195	4/16/2013	GREENTHREAD, LLC
2	9,190,502	11/17/2015	GREENTHREAD, LLC
3	10,510,842	12/17/2019	GREENTHREAD, LLC
4	10,734,481	8/4/2020	GREENTHREAD, LLC
5	11,121,222	9/14/2021	GREENTHREAD, LLC

In the above---entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☑ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading		
	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	11,316,014	4/26/2022	GREENTHREAD, LLC
2			
3			
4			
5			

In the above---entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1---Upon initiation of action, mail this copy to Director Copy 3---Upon termination of action, mail this copy to Director
Copy 2---Upon filing document adding patent(s), mail this copy to Director Copy 4---Case file copy

SONY 1007

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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GREENTHREAD, LLC	INTEL CORPORATION, DELL INC., AND DELL TECHNOLOGIES INC.,

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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2	9,190,502	11/17/2015	GREENTHREAD, LLC
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In the above---entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above---entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1---Upon initiation of action, mail this copy to Director Copy 3---Upon termination of action, mail this copy to Director
Copy 2---Upon filing document adding patent(s), mail this copy to Director Copy 4---Case file copy

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/947,294	09/14/2021	11121222	GRTD60-35294	6907

25883 7590 08/25/2021

MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

GREENTHREAD, LLC, Dallas, TX;
G.R. Mohan Rao, Allen, TX;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25883 7590 08/11/2021
MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD60-35294	6907

TITLE OF INVENTION: SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	11/12/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
ARORA, AJAY	2892	257-025000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Gregory M. Howison
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: GREENTHREAD, LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY): DALLAS, TEXAS

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 50-0208

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Gregory M. Howison, Reg. #30646/ Date August 11, 2021

Typed or printed name GREGORY M. HOWISON Registration No. 30,646

Electronic Patent Application Fee Transmittal

Application Number:	16947294
Filing Date:	27-Jul-2020
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Filer:	Gregory Michael Howison/Anna Nguyen
Attorney Docket Number:	GRTD60-35294

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
UTILITY APPL ISSUE FEE	1501	1	1200	1200
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1200**

Electronic Acknowledgement Receipt

EFS ID:	43481763
Application Number:	16947294
International Application Number:	
Confirmation Number:	6907
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	25883
Filer:	Gregory Michael Howison
Filer Authorized By:	
Attorney Docket Number:	GRTD60-35294
Receipt Date:	11-AUG-2021
Filing Date:	27-JUL-2020
Time Stamp:	15:54:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1200
RAM confirmation Number	E20218AF55164564
Deposit Account	500208
Authorized User	Gregory Howison

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	GRT35294IssueFeeTransmittal.pdf	1235057 bcc7d713d5093b3da2caf0714325c11158a3f3e9	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	40279 89ee78f80675f92f2bff9aca0fbabba28b7b353f	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1275336		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

25883 7590 08/11/2021

MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

EXAMINER	
ARORA, AJAY	
ART UNIT	PAPER NUMBER
2892	

DATE MAILED: 08/11/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD60-35294	6907

TITLE OF INVENTION: SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	11/12/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25883 7590 08/11/2021
MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD60-35294	6907

TITLE OF INVENTION: SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	11/12/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
ARORA, AJAY	2892	257-025000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD60-35294	6907

25883 7590 08/11/2021

MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

EXAMINER	
ARORA, AJAY	
ART UNIT	**PAPER NUMBER**
2892	

DATE MAILED: 08/11/2021

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/947,294	Applicant(s) Rao, G.R. Mohan	
	Examiner AJAY ARORA	Art Unit 2892	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 7/27/2020.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-44 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☑ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 9/29/2020 & 6/30/2021.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/AJAY ARORA/
Primary Examiner, Art Unit 2892

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Reasons for Allowance

2. Claims 1-44 are allowed. The following is an examiner's statement of reasons for allowance:

Claims 1-20 are allowed because the prior art of record does not teach or suggest, singularly or in combination, at least the limitations of the base claim 1 that requires "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions" (see last 5 lines).

The closest reference is Hong (US 2007/0045682), hereinafter Hong. More specifically, regarding claim 17, Hong (refer to Figures 4A-4D and 5A-5C) teaches a semiconductor device, comprising:

a substrate (312 – see para 29) of a first doping type (i.e. parts 312 and 21 of the substrate have n-type doping, see para 29) at a first doping level having a surface;

a first region (311, which includes wells such as 21, 22, 5, 2) disposed adjacent the first surface,

a second active region (such as source/drain region 2, see para 40; or 2 or 5 or 22 of pixel cell formed in an adjacent region separated by shallow trench isolation 37 – see para 30) separate from the first region disposed adjacent to the first active region and within which transistors (406, 407) may be formed;

at least a portion of at least one of the first and second regions having at least one graded dopant concentration (350 – see para 24, last 3 sentences; also see Figure 5C and para 29) to aid carrier movement (para 26).

However, the first region is not an "active" region and the structure does not show that the graded dopant region is to "aid carrier movement from the surface to the area of the substrate where there are no active regions". Further, it is not obvious to modify Hong as changing first region and second region as above would change the intended function of the device.

Similarly, claims 21-38 are allowed because the prior art of record does not teach or suggest, singularly or in combination, at least the limitations of base claim 21 that requires "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions" (see last 5 lines). Again, the closest reference is Hong.

Similarly, claims 39-40 are allowed because the prior art of record does not teach or suggest, singularly or in combination, at least the limitations of base claim 30 that requires "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region" (see last 3 lines). Again, the closest reference is Hong.

Similarly, claim 41 is allowed because the prior art of record does not teach or suggest, singularly or in combination, at least the limitations of "at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region" (see last 3 lines). Again, the closest reference is Hong.

Similarly, claim 42 is allowed because the prior art of record does not teach or suggest, singularly or in combination, at least the limitations of "at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region" (see last 3 lines). Again, the closest reference is Hong.

Similarly, claim 43 is allowed because the prior art of record does not teach or suggest, singularly or in combination, at least the limitations of "at least one graded acceptor dopant concentration and one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region" (see last 3 lines). Again, the closest reference is Hong.

Similarly, claim 44 is allowed because the prior art of record does not teach or suggest, singularly or in combination, at least the limitations of "a second static

unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions" (see last 3 lines). Again, the closest reference is Hong.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AJAY ARORA whose telephone number is (571)272-8347. The examiner can normally be reached on 9 AM - 5 PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on 5712721708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-

my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/AJAY ARORA/
Primary Examiner, Art Unit 2892

Notice of References Cited	Application/Control No. 16/947,294	Applicant(s)/Patent Under Reexamination Rao, G.R. Mohan	
	Examiner AJAY ARORA	Art Unit 2892	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20070045682-A1	03-2007	Hong; Sungkwon C.	H01L27/14689	257/292
*	B	US-20140034997-A1	02-2014	RAHIMO; Munaf	H01L29/861	257/139
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/947,294	Rao, G.R. Mohan
	Examiner	Art Unit
	AJAY ARORA	2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☑ Claims renumbered in the same order as presented by applicant			☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE								
Final	Original	07/31/2021								
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	3	=								
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	41	=								
	42	=								

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/947,294	Rao, G.R. Mohan
	Examiner	**Art Unit**
	AJAY ARORA	2892

CLAIM		DATE								
Final	Original	07/31/2021								
	43	=								
	44	=								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/947,294	Rao, G.R. Mohan
	Examiner	Art Unit
	AJAY ARORA	2892

CPC - Searched*		
Symbol	Date	Examiner
H01L 29/1095	07/31/2021	AKA

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
257	25	07/31/2021	AKA

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Inventor search	07/31/2021	AKA
Assignee search	07/31/2021	AKA
All references for parent applications considered	07/31/2021	AKA
.clm. interference search	07/31/2021	AKA
EAST search history report	07/31/2021	AKA

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
H01L	29/1095	07/31/2021	AKA
257	25	07/31/2021	AKA

/AJAY ARORA/ Primary Examiner, Art Unit 2892	

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/947,294	Rao, G.R. Mohan
	Examiner	**Art Unit**
	AJAY ARORA	2892

CPC						
Symbol					**Type**	**Version**
H01L	/	29	/	1095	F	2013-01-01
H01L	/	27	/	11524	I	2013-01-01
H01L	/	27	/	14643	I	2013-01-01
H01L	/	27	/	11521	I	2013-01-01
H01L	/	29	/	7395	I	2013-01-01
H01L	/	29	/	36	I	2013-01-01
H01L	/	27	/	0214	A	2013-01-01
H01L	/	27	/	10844	A	2013-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	44	
/AJAY ARORA/ Primary Examiner, Art Unit 2892	31 July 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5B

U.S. Patent and Trademark Office — Part of Paper No.: 20210731

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/947,294	Rao, G.R. Mohan
	Examiner	Art Unit
	AJAY ARORA	2892

INTERNATIONAL CLASSIFICATION					
CLAIMED					
H01L29/10	/	29	/	10	

NON-CLAIMED					
	/		/		

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
257	25

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	44	
/AJAY ARORA/ Primary Examiner, Art Unit 2892	31 July 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5B

U.S. Patent and Trademark Office — Part of Paper No.: 20210731

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/947,294	Rao, G.R. Mohan
	Examiner	**Art Unit**
	AJAY ARORA	2892

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	44	
/AJAY ARORA/ Primary Examiner, Art Unit 2892	31 July 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5B

U.S. Patent and Trademark Office — Part of Paper No.: 20210731

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	16/947,294	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/07/31 19:23
L2	3	16/717,950	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/07/31 19:23
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L16	10	l13 and drift	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/07/31 19:28
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L22	12,797	H01L29/7395.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/07/31 19:31
L23	1	((source drain "source/drain") and drift and ((gradient graded) near2 concentration near2 dop$3) and well and ((no near2 active) (inactive))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/07/31 19:32
L24	1	((source drain "source/drain") and drift and ((gradient graded) near2 concentration near2 dop$3) and ((no near2 active) (inactive))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/07/31 19:32
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L38	267	L3 L5 L7 L9 L11 L26 L28 L30 L32 L34 L36	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/07/31 19:38
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L41	1	((source drain "source/drain" active) and drift and ((gradient graded) near2 concentration near2 dop$3) and well and ((no near2 active) (inactive))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/07/31 19:47
L43	31	((source drain "source/drain" active) and drift and ((gradient graded) near2 concentration near2 dop$3) and well and ((no near2 active) (inactive)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/07/31 19:51
L44	0	l43 and L38	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/07/31 19:52
L45	1	l43 and L13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/07/31 19:52
L46	17	L14 and L18 and L19 and L20 and L21 and L22	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2021/07/31 19:53

			DERWENT; IBM_TDB			
L47	17	L14 and L18 and L19 and L21 and L22	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/07/31 19:53
L48	17	L14 and L19 and L21 and L22	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/07/31 19:53
L49	267	L14 and L19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/07/31 19:53
L50	1	("20070045682").PN.	US-PGPUB; USPAT	OR	OFF	2021/07/31 20:42

7/31/2021 9:53:28 PM
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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16947294
Filing Date	2020-07-27
First Named Inventor	G.R. Mohan Rao
Art Unit	2892
Examiner Name	NA
Attorney Docket Number	GRTD.01.01.DV7

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	2	4160985	A	1979-07-10	Kamins et al.	
	3	4347654	A	1982-09-07	Allen et al.	
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	8	5213988	A	1993-05-25	Yamauchi et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.A/

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	9	5262345	A	1993-11-16	Nasser et al.	
	10	5329144	A	1994-07-12	Luryi	
	11	5448087	A	1995-09-05	Streit et al.	
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	16	5575862	A	1996-11-19	Nishida	
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	18	5797999	A	1998-08-25	Sannomiya et al.	
	19	5888857	A	1999-03-30	Zhang et al.	

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	20	5973575	A	1999-10-26	Kamogawa et al.	
	21	6211028	B1	2001-04-03	Tsai et al.	
	22	6310366	B1	2001-10-30	Rhodes et al.	
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Attorney Docket Number	GRTD.01.01.DV7

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	38	6756616	B2	2004-06-29	Rhodes	
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	42	6921946	B2	2005-07-26	Kenney et al.	
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	Examiner Name	NA
	Attorney Docket Number	GRTD.01.01.DV7

	53	10510842	B2	2019-12-17	Rao	
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	3	20020074585	A1	2002-06-20	Tsang et al.	
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	6	20020102783	A1	2002-08-01	Fujimoto et al.	

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	Examiner Name	NA
	Attorney Docket Number	GRTD.01.01.DV7

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	8	20030026126	A1	2003-02-06	Uemura	
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	Examiner Name	NA
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EXAMINER SIGNATURE

Examiner Signature	/AJAY ARORA/	Date Considered	07/31/2021

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Art Unit	2892
Examiner Name	NA
Attorney Docket Number	GRTD.01.01.DV7

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Bill R. Naifeh, Reg. No. 44962/	Date (YYYY-MM-DD)	2020-09-29
Name/Print	Bill R. Naifeh	Registration Number	44962

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16947294
Filing Date	2020-07-27
First Named Inventor	G.R. Mohan Rao
Art Unit	2892
Examiner Name	ARORA, AJAY
Attorney Docket Number	GRTD60-35294

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4160985	A	1979-07-10	Kamins et al.	
	2	4684971	A	1987-08-04	Payne	
	3	4688063	A	1987-08-18	Lu et al.	
	4	4907058	A	1990-03-06	Sakai	
	5	4994887	A	1991-02-19	Hutter et al.	
	6	5835402	A	1998-11-10	Rao et al.	
	7	6025237	A	2000-02-15	Choi	
	8	6384431	B1	2002-05-07	Takahashi et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.A/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16947294
	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	ARORA, AJAY
	Attorney Docket Number	GRTD60-35294

	9	6465862	B1	2002-10-15	Harris	

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U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20010028097	A1	2001-10-11	Matsuoka et al.	
	2	20020195656	A1	2002-12-26	Hattori	
	3	20030183856	A1	2003-10-02	Wieczorek et al.	
	4	20080142899	A1	2008-06-19	Morris et al.	
	5	20170243876	A1	2017-08-24	Rao	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2003051551	JP	A	2003-02-21	Miyamoto et al.		X

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16947294
	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
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	Examiner Name	ARORA, AJAY
	Attorney Docket Number	GRTD60-35294

	2	2003218356	JP	A	2003-07-31	Matsumoto et al.		☒
	3	s6482563	JP	A	1989-03-28	Kondo		☒
	4	2004049453	WO	A1	2004-06-10	Zheng et al.		☐

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	IPR2020-00288-Exhibit 1029-Claim Construction District Court 4 20-2020	
	2	IPR2020-00288-Exhibit 2007-Minutes for Markman Hearing Held Via Video Conference Before U.S. District Judge Rodney Gilstrap, Greenthread, LLC v. Samsung Electronics Co., Ltd., et al., Case No. 2:19-CV-147-JRG, Dkt. 61	
	3	IPR2020-00288-Petitioner Reply	
	4	IPR2020-00289-00289 Petitioner Reply	
	5	IPR2020-00292 - Petition for IPR	
	6	IPR2020-00292-Exhibit 2002-Excerpt from Exhibit 4 to Appendix B of Samsung Electronics Co., Ltd.'s Invalidity Contentions (Invalidity Contention based on U.S. Patent No. 6,384,431 to Takahashi	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	ARORA, AJAY
	Attorney Docket Number	GRTD60-35294

	7	IPR2020-00288 - Ex. 1020 - Michael Nastasi and James W. Mayer, Ion Implantation and Synthesis of Materials (2006). 4 pages	
	8	IPR2020-00288-Exhibit 2001 - IPR2020-00288 - Excerpt from Exhibit 1 to Appendix A of Samsung Electronics Co., Ltd.'s Invalidity Contentions regarding Morris	
	9	IPR2020-00288-Exhibit 2002-xcerpt from Exhibit 2 to Appendix A of Samsung Electronics Co., Ltd.'s Invalidity Contentions regarding Miyamoto	
	10	IPR2020-00288-Exhibit 2009-Complaint for Patent Infringement, Greenthread, LLC v. Samsung Electronics Co., Ltd., et al., Case No. 2:19-CV-147-JRG, Dkt. 1	
	11	IPR2020-00288-Exhibit 2011- Exhibit A to Revised Joint Claim Construction Chart Pursuant to Patent Rule 4-5, Greenthread, LLC v. Samsung Electronics Co., Ltd., et al., Case No. 2:19-CV-147-JRG, Dkt. 60-1	
	12	IPR2020-00288-Exhibit 2012-Samsungs Responsive Claim Construction Brief - District Court	
	13	IPR2020-00288-Exhibit 2013- Glew Dec	
	14	IPR2020-00288-Exhibit 2014- Excerpt from Exhibit 10 to Appendix A of Samsung Electronics Co., Ltd.'s Invalidity Contentions	
	15	IPR2020-00288-Patent Owner Preliminary Response	
	16	IPR2020-00288-Patent Owner Sur Reply	
	17	IPR2020-00288-Petition	

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	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	ARORA, AJAY
	Attorney Docket Number	GRTD60-35294

	18	IPR2020-00289-Exhibit 1 to Appendix C of Samsung Electronics Co., Ltd.'s Invalidity Contentions regarding Payne	
	19	IPR2020-00289-Exhibit 1003-Smith Dec	
	20	IPR2020-00289-Exhibit 1010- S. M. Sze et al., Semiconductor Devices: Physics and Technology,John Wiley & Sons, 2nd Ed., 2002 ("Sze '02")	
	21	IPR2020-00289-Exhibit 1012-Ben G. Streetman, Solid State Electronic Devices, 2nd Ed., Prentice-Hall, 1980 ("Streetman")	
	22	IPR2020-00289-Exhibit 2001-Exhibit 1 to Appendix C of Samsung Electronics Co., Ltd.'s Invalidity Contentions regarding Payne	
	23	IPR2020-00289-Exhibit 2002- Exhibit 3 to Appendix C of Samsung Electronics Co., Ltd.'s Invalidity Contentions regarding Wieczorek	
	24	IPR2020-00289-Exhibit 2011-Behzad Razavi, Design of Analog CMOS Integrated Circuits, 2001 ("Razavi")	
	25	IPR2020-00289-Exhibit 2012-Excerpts from Wolf, S., Silicon Processing for the VLSI Era, Vol.4 - Deep-Submicron Process Technology (2002) ("Wolf Vol. 4")	
	26	IPR2020-00289-Exhibit 2013-Glew Dec	
	27	IPR2020-00289-Patent Owner Pre Resp	
	28	IPR2020-00289-Patent Owner Sur reply	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	16947294
Filing Date	2020-07-27
First Named Inventor	G.R. Mohan Rao
Art Unit	2892
Examiner Name	ARORA, AJAY
Attorney Docket Number	GRTD60-35294

	29	IPR2020-00289-Petition	
	30	IPR2020-00290-Exhibit 1003-Declaration of Dr. Bruce Smith	
	31	IPR2020-00290-Exhibit 1013-Tango, Mega bit Memory Technology	
	32	IPR2020-00290-Patent Owner Preliminary Resp	
	33	IPR2020-00290-Patent Owner Sur Reply	
	34	IPR2020-00290-Petition	
	35	IPR2020-00290-Petitioners Reply to Patent Owner Preliminary Response	
	36	IPR2020-00291-Exhibit 1003-Declaration of Dr. Bruce Smith	
	37	IPR2020-00291-Exhibit 1011- The Insulated Gate Bipolar Transistor: IGBT Theory and Design, Vinod Kumar Khanna, IEEE Press and Wiley-Interscience, 2003	
	38	IPR2020-00291-Exhibit 1020-S. M. Sze, Physics of Semiconductor Devices, Wiley-Interscience, 2nd Ed., 1981 ("Sze '81")	
	39	IPR2020-00291-Exhibit 1021-S. M. Sze, Semiconductor Devices: Physics and Technology, John Wiley & Sons, 2nd Ed., 2002 ("Sze '02")	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.A/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	16947294
Filing Date	2020-07-27
First Named Inventor	G.R. Mohan Rao
Art Unit	2892
Examiner Name	ARORA, AJAY
Attorney Docket Number	GRTD60-35294

	40	IPR2020-00291-Exhibit 2001-Exhibit 2 to Appendix B of Samsung Electronics Co., LTD's Invalidity Contentions (Invalidity Contention based on U.S. Patent Application Publication No. 2002/0195656 ("Hattori"))	
	41	IPR2020-00291-Exhibit 2013- Declaration of Dr. Alexander D. Glew	
	42	IPR2020-00291-Patent Owner Preliminary Resp	
	43	IPR2020-00291-Patent Owner Sur Reply	
	44	IPR2020-00291-Petition	
	45	IPR2020-00291-Petitioners Reply	
	46	IPR2020-00292-Exhibit 1003-Declaration of Dr. Bruce Smith	
	47	IPR2020-00292-Exhibit 2001-Excerpt from Exhibit 1 to Appendix B of Samsung Electronics Co., Ltd.'s Invalidity Contentions (Invalidity Contention based on "Insulated Gate Bipolar Transistor IGBT Theory and Design" by Vinod Kumar Khanna	
	48	IPR2020-00292-Exhibit 2012-Excerpt from Exhibit A to Joint Claim Construction Chart Pursuant to Patent Rule 4-5, Greenthread, LLC v. Samsung Electronics Co., Ltd., et al., Case No. 2:19-CV-147-JRG, Dkt. 53-1 (Mar. 18, 2020)	
	49	IPR2020-00292-Patent Owner Preliminary Response	

If you wish to add additional non-patent literature document citation information please click the Add button Add

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16947294
	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	ARORA, AJAY
	Attorney Docket Number	GRTD60-35294

EXAMINER SIGNATURE			
Examiner Signature	/AJAY ARORA/	Date Considered	07/31/2021

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16947294
Filing Date	2020-07-27
First Named Inventor	G.R. Mohan Rao
Art Unit	2892
Examiner Name	ARORA, AJAY
Attorney Docket Number	GRTD60-35294

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Gregory M. Howison, Reg. #30646/	Date (YYYY-MM-DD)	2021-06-24
Name/Print	Gregory M. Howison	Registration Number	30646

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Bibliographic Data

Application No: 16/947,294

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /AJAY ARORA/ Examiner's Signature | Initials

Title: SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
07/27/2020	257	2892	GRTD60-35294
RULE			

APPLICANTS

GREENTHREAD, LLC, Dallas, TX, UNITED STATES

INVENTORS

G.R. Mohan Rao, Allen, TX, UNITED STATES

CONTINUING DATA

This application is a CON of 16717950 12/17/2019 PAT 10734481

16717950 is a CON of 15590282 05/09/2017 PAT 10510842

15590282 is a CON of 14931636 11/03/2015 PAT 9647070

14931636 is a CON of 14515584 10/16/2014 PAT 9190502

14515584 is a CON of 13854319 04/01/2013ABN

13854319 is a CON of 11622496 01/12/2007 PAT 8421195

11622496 is a DIV of 10934915 09/03/2004ABN

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

08/03/2020

STATE OR COUNTRY

UNITED STATES

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MUNCK WILSON MANDALA L.L.P

P.O. Drawer 800889

DALLAS, TX 75380

UNITED STATES

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD60-35294

CONFIRMATION NO. 6907

25883
MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

POA ACCEPTANCE LETTER

OC000000127152029

Date Mailed: 07/23/2021

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/20/2021.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/sibrahim/

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD.01.01.DV7

CONFIRMATION NO. 6907

POWER OF ATTORNEY NOTICE

40672
BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380

OC000000127152011

Date Mailed: 07/23/2021

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/20/2021.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/sibrahim/

Doc Code: PA..
Document Description: Power of Attorney

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Application Number	16/947,294
Filing Date	2020-07-27
First Named Inventor	R Mohan Rao G
Title	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
Art Unit	
Examiner Name	
Attorney Docket Number	GRTD60-35294

SIGNATURE of Applicant or Patent Practitioner

Signature	/GregoryMHowison#30646/	Date (Optional)	2021-07-15
Name	Gregory M. Howison	Registration Number	30646
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date
16/947,294	2020-07-27

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 25883

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☒ The address associated with the above-mentioned Customer Number

OR

☑ The address associated with Customer Number: 25883

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Greenthread, LLC

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Phil John Phillip W John Jr.	Date (Optional)	2021-07-15
Name	Phil John Phillip W John Jr.		
Title	President		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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No more than ten (10) patent practitioners total may be appointed as set forth below by name and registration number. This page need not be submitted if appointing the Patent Practitioner(s) associated with a Customer Number (see form PTO/AIA/82B):

Name	Registration Number

Electronic Acknowledgement Receipt

EFS ID:	43300849
Application Number:	16947294
International Application Number:	
Confirmation Number:	6907
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	40672
Filer:	Gregory Michael Howison
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Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	GRTDREVPOA.pdf	2993357 a0530366f1da6b2c29b1cbd912dbdaae5d0555a9	no	3

Warnings:

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Total Files Size (in bytes):	2993357

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	G.R. Mohan RAO
Serial No.:	16/947,294
Confirmation No.:	6907
Filed:	July 27, 2020
Group:	2892
Examiner:	Ajay ARORA
For:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

Mail Stop Amendments/DD
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. 1.97

In accordance with the requirements of 37 C.F.R. §§ 1.56, 1.97, and 1.98, attached please find a Form PTO SB/08 listing information for consideration by the Office in connection with its examination of the above-captioned patent application. A copy of each listed document is enclosed herewith.

Information related to IPRs 2020-00288, 00289, 00290, 00291 has been submitted in the attached Form SB/08a. Additionally, the related patent family to these IPRS was the subject matter of District Court Action styled *Greenthread, LLC v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-CV-147-JRG, Dkt. 1 (Apr. 30, 2019). All relevant information related to this District Court case is included in the IPR submitted document.

Applicant request that this information disclosure statement be considered and that a copy of the Form PTO SB/08 be returned to the undersigned indicating the consideration of each document listed.

Respectfully submitted,
MUNCK WILSON MANDALA, LLP
Attorneys for Applicant(s)

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Application Number:	16947294
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1	Non Patent Literature	NPL_IPR202000288SurReply.pdf	188110 016c23a9a828470659760723 91f03ad987a03037	no	13

Warnings:

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2	Non Patent Literature	NPL_IPR202000292POPR.pdf	2474863 10024da7c840175f6763f2b5999ed90b65def9e9	no	75
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3	Non Patent Literature	NPL292Exhibit2002Exhibit4toInvalidityContentions.pdf	8383853 44bb846f131c1ef304f556f69b4dc7e9d480bb5f	no	27
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4	Foreign Reference	WO2004049453A1.pdf	1000408 2f402b8dfe42d2643aaf402eb7926ad15cd74abd	no	14
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5	Non Patent Literature	NPL_IPR2020002884 81POPR.pdf	2292379 68c78c9e814ba319e9ae0453f6fbef9741f02fd8	no	84
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6	Non Patent Literature	NPL_00291Exhibit1020Sze.pdf	12801935 1a640fa8a83a471f3cd044c7a7b5d69cf5b1ea5a	no	206
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7	Non Patent Literature	NPL_Ex_2013GlewDec.pdf	3369738 c56d25401a6672d5e7cdeef473a93450f8c98d77	no	79
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8	Non Patent Literature	NPL_Ex_201300291_GlewDeclaration.pdf	1826545 74aaaf3ef8c8145a069d46ec927d945236942f89	no	47
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9	Non Patent Literature	NPL_Ex2012_WolfVol4.pdf	3779059 4d892466d6a253759cf9df1f2fb4fc7374f240e3	no	52
Warnings:					
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10	Non Patent Literature	NPL_Ex2013_195GlewDec.pdf	2797823 dd947a40481a2b4fbd087064aefb6a8edd8ef0b4	no	69
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11	Non Patent Literature	NPL_IonImplantation.pdf	342865 5121aa94aecab3a738636c0e60dded96ac2873d5	no	4
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12	Non Patent Literature	NPL_Exhibit1011KhannaPart2.pdf	9657165 492d544396816ed498881ebdcdb77a3fc4f88ba6	no	165
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13	Transmittal Letter	GRTD60-35294IDSTransmittal.pdf	96496 15ef1d14309a48eb913b3b06f0f00c74849e9a6a	no	2
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New Applications Under 35 U.S.C. 111

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New International Application Filed with the USPTO as a Receiving Office

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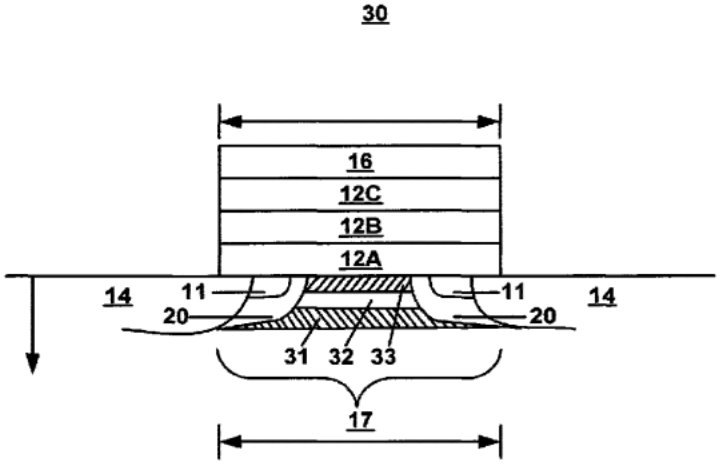
(54) Title: RETROGRADE CHANNEL DOPING TO IMPROVE SHORT CHANNEL EFFECT



(57) Abstract: A memory semiconductor cell (30) comprises a gate region (16), a source region (14) and a drain region (14). A channel region (17) is formed between the source region (14) and the drain region (14). The channel region (17) comprises a first channel portion (33) with a first concentration of doping material, the first channel portion (33) disposed adjacent to an edge of the channel region (17) closest to and substantially parallel to the gate region (16). The channel region (17) further comprises a second channel portion (31) with a second concentration of doping material, the second channel portion (31) disposed substantially parallel to the first channel portion (33) and a third channel portion (32), disposed between the first channel portion (33) and the second channel portion (31), with a third concentration of doping material. The third concentration is lower than the first concentration and lower than the second concentration. The memory cell may be one of two general types of non-volatile memory, a floating gate cell or a nitride read only memory (NROM), whereby layer (12B) in a floating gate or a nitride layer respectively.

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RETROGRADE CHANNEL DOPING TO IMPROVE SHORT CHANNEL EFFECT

TECHNICAL FIELD

Embodiments of the present invention relate to design of sub-micron metal oxide semiconductors. More particularly, embodiments of the present invention provide retrograde channel doping to improve the short channel effect.

BACKGROUND ART

Figure 1 shows a memory cell 10 as has been well known in the conventional art. Regions 14 are the drain and/or source regions for memory cell 10. They may be used as source and/or drain interchangeably. Control gate 16 is used to control the operation of memory cell 10. A channel region 17 is formed between source/drain regions 14. Feature size 18 is the nominal size of the smallest feature that can be created by a particular semiconductor process. In memory cells of this type, the gate 16 width and channel 17 length typically correspond approximately to feature size 18. Memory cell 10 may also have a source/drain extension 11 structure. Source/drain extension 11 is a shallow diffusion that connects the channel 17 with the deeper source/drain 14, typically intended to prevent degradation of drive current.

Memory cell 10 may be one of two general types of non-volatile memory, a "floating gate" cell or a nitride read only memory (NROM) cell. In a floating gate cell, layer 12B of the gate stack is typically conductive polysilicon. Layers 12A and 12C are insulating materials which isolate or "float" gate layer 12B, which is usually referred to as a floating gate. Floating gate 12B is the storage element of memory cell 10.

Silicon nitride based flash memory has many advantages as compared to its floating gate and tunneling oxide based counterparts. Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) is potentially very dense in terms of number of cells per unit area that can be used and it requires fewer process steps as compared to floating gate memory. Moreover, it can be easily integrated with standard SRAM process technology. A further advantage of using SONOS devices is their suitability for applications requiring large temperature variations and radiation hardening. The SONOS stack is a gate dielectric stack and consists of a single layer of polysilicon, a triple stack ONO (Oxide-Nitride-Oxide) gate dielectric layer and a MOS channel 17. The ONO structure may consist of a tunnel oxide 12A, a nitride memory storage layer 12B and a blocking oxide layer 12C.

Memory device manufacturers are continually challenged to provide ever greater amounts of memory at ever lower costs. Recently, Advanced Micro Devices, Incorporated of California has introduced MIRROR BIT ™ nitride-based flash ROM that stores multiple bits per memory cell 10 physically separated in nitride layer 12B. Such storage of multiple bits per cell increases the storage density of the memory device, thereby reducing the cost per bit of storage.

Another primary approach employed to achieve lower memory costs is the industry-wide on-going reduction in semiconductor feature size. By making features, such as signal lines and transistors smaller, more memory devices may be placed in a given die area, resulting in lower production costs.

However, as feature size decreases to, for example, about 0.3 microns and smaller, the channel length also decreases. As channel length grows shorter, threshold voltage begins to decrease and leakage current increases. These effects are commonly referred to in the semiconductor arts as the "short channel effect." An increase in leakage current is particularly onerous in flash memory devices as flash has found wide acceptance in very low power applications, for example mobile phones, due to the ability of flash to retain information without applied power. Increases in leakage current may have a significant deleterious effect on total power consumption

of the flash device and the product using the flash device. Consequently, much research and development effort has gone into mitigating the short channel effect.

Prior art approaches to improve leakage current and reduce the short channel effect include, for example, "halo" doping and retrograde wells. Halo doping 20 creates a steep dopant profile at the edges of the source/drain regions, as shown in Figure 1. A conventional retrograde well has a non-uniform doping concentration that increases, for example, linearly with depth 22 in the channel region 17. The doping of a conventional retrograde well generally follows a continuous, monotonically increasing profile with no abrupt changes. Conventional retrograde wells are typically created by using a slow diffusing dopant species such as arsenic or antimony for PMOS devices and indium for NMOS devices. Both halo doping and retrograde well profiles serve to inhibit the flow of charge carriers, raising the threshold voltage and reducing leakage current for the device.

However, both halo doping and conventional retrograde wells, alone and in combination, are found to be lacking. Such prior art approaches simply do not reduce leakage current to commercially acceptable levels for flash memory at modern process feature sizes, for example, 0.17 microns and smaller.

Semiconductor processing equipment is extremely expensive. Fundamental semiconductor processing steps, e.g., doping, typically require long periods of development and extensive qualification testing. Any solution to the short channel effect should be compatible with existing semiconductor processes and equipment without the need for revamping well established tools and techniques.

Thus a need exists to prevent short channel effects in memory cells. A further need exists for preventing short channel effects in a manner that is compatible and complimentary with conventional approaches to minimize short channel effects. A still further need exists for the above mentioned needs to be achieved with existing semiconductor processes and equipment without revamping well established tools and techniques.

DISCLOSURE OF THE INVENTION

Embodiments of the present invention provide a means to prevent short channel effects in memory cells. Further embodiments of the present invention prevent short channel effects in a manner that is compatible and complimentary with existing approaches to minimize short channel effects. Still further embodiments of the present invention provide for the above mentioned solutions to be achieved with existing semiconductor processes and equipment without revamping well established tools and techniques.

A memory semiconductor cell comprises a gate region, a source region and a drain region. A channel region is formed between the source region and the drain region. The channel region comprises a first channel portion with a first concentration of doping material, the first channel portion disposed adjacent to an edge of the channel region closest to and substantially parallel to the gate region. The channel region further comprises a second channel portion with a second concentration of doping material, the second portion disposed substantially parallel to the first channel portion and a third channel portion, disposed between the first channel portion and the second channel portion, with a third concentration of doping material. The third concentration is lower than the first concentration and lower than the second concentration.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a memory cell as has been well known in the conventional art.

Figure 2 illustrates a memory cell with a retrograde channel, according to an embodiment of the present invention.

Figure 3 illustrates an exemplary profile of doping concentration in a channel region versus channel depth, according to an embodiment of the present invention.

Figures 4A, 4B and 4C illustrate a charge carrier flow through a channel region of a memory cell, according to an embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

In the following detailed description of the present invention, retrograde channel doping to improve short channel effect, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one skilled in the art that the present invention may be practiced without these specific details or with equivalents thereof. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

RETROGRADE CHANNEL DOPING TO IMPROVE SHORT CHANNEL EFFECT

Embodiments of the present invention are described in the context of design and operation of flash memory devices. However, it is appreciated that embodiments of the present invention may be utilized in other areas of electronic design and operation.

Figure 2 illustrates a memory cell 30 with a novel retrograde channel, according to an embodiment of the present invention. The channel region comprises three portions, 31, 32 and 33. Channel portion 33 is closest to gate 16 and substantially parallel to the long axis of gate 16. Channel portion 32 is substantially parallel to channel portion 33 and at a greater depth into the substrate material than channel portion 32. Channel portion 31 is substantially parallel to channel portion 32 and at a still greater depth into the substrate material. Channel portion 32 is disposed between channel portions 31 and 33. It is appreciated that memory cell 30 is shown with source/drain extensions 11 and halo implant regions 20. Embodiments of the present invention are well suited to memory cells with or without these features. If one or both were absent, channel portions 31, 32 and 33 would extend horizontally to the halo implant or the source drain extension or the source/drain.

By well known semiconductor processing techniques, for example implantation and diffusion, channel portion 33 may be constructed and given a particular concentration of doping material. Likewise, channel portion 31 may be constructed and given a particular concentration of doping material. In general, no specific operations are performed to construct channel portion 32, rather channel portion 32 is a result of constructing portions 31 and 33 with no overlap. The bottom of channel portion 31 may be, for example, 0.1 μm from the top edge of the substrate.

According to an embodiment of the present invention, the doping concentration in both channel portion 31 and channel portion 33 is higher than the doping concentration of channel portion 32. Graph 40 of Figure 3 illustrates an exemplary profile 41 of doping concentration in a channel region versus channel depth. Channel portion 33 may have a doping concentration as depicted by profile 41 in region 33A. Channel portion 32 may have a doping concentration as depicted by profile 41 in region 32A. Channel portion 31 may have a doping concentration as depicted by profile 41 in region 31A.

It is to be appreciated that, in contrast to conventional retrograde wells, the doping profile of this novel well is neither monotonic nor necessarily continuous, according to an embodiment of the present invention. There may be relatively abrupt (as allowed by semiconductor physics) changes in doping profile at the boundaries between channel portions, for example between channel portions 31 and 32, and between channel portions 32 and 33.

In channel portions 31 and 33 charge carrier migration is hindered due to the to relatively high concentration of doping material(s). Consequently, the effective channel region is reduced to approximately

channel portion 32. For example, channel portion 32 may form a "tunnel" (not to be confused with quantum effect tunneling) between channel portions 31 and 33. As a beneficial result of the reduced effective channel, threshold voltage is increased and leakage current is decreased, reducing or eliminating the short channel effect. It is to be appreciated that the depths, thickness and doping concentrations of the respective channel portions will vary according to a wide range of variables including, for example, source/drain thickness, channel length, operating voltage, doping materials and whether the device operates as a P channel or an N channel.

Channel portion 31 may be initially formed by using a slow diffusing dopant species, for example, arsenic or antimony for PMOS devices. Such a diffusion process may enable high concentrations of doping material to reach the channel depths required. Channel portion 33 may be formed by using faster diffusing dopants, e.g., boron. A shorter diffusion may produce a high concentration of doping material at relatively shallow depths in the channel region.

Figures 4A, 4B and 4C further illustrate a charge carrier flow through a channel region of memory cell 30, according to an embodiment of the present invention. In Figure 4A, charge carriers, for example, electrons 403 attempt to flow from source/drain region 401 to source/drain region 402. Electrons are impeded from flowing into channel portion 33 due to a high concentration of doping material. Likewise, electrons 405 are impeded from flowing into channel portion 31 due to a high concentration of doping material. In contrast, electrons 404 are able to overcome a relatively small energy barrier and flow into channel portion 32.

As shown in Figure 4B, electrons 403, otherwise disposed to travel horizontally (as depicted) into channel region 33, must change direction to travel around the "corner" of channel region 33 in order to enter channel region 32, wherein electrons are more able to flow. Such changes of direction require energy, resulting in a higher energy budget for electrons traversing a complex path, in contrast to electrons which may be able to travel in substantially a straight line. In addition, because region 401 is fully populated with charge carriers, e.g., electrons 404 and 405, additional energy is required to overcome the electrostatic repulsion of like charges in order to move the charge carriers closer together. As a beneficial result of the increased path length, the indirect nature of the path, as well as electrostatic repulsion, electrons 403 require more energy to travel from region 401 to 402 and consequently have a beneficially higher threshold voltage for embodiments of the present invention when compared to the prior art.

In a similar manner, electrons 405 must change direction and overcome electrostatic repulsion in order to travel into channel portion 32 from their original positions adjacent to channel portion 31. Consequently, electrons 405 have a higher threshold voltage than would otherwise be required.

Electrons 404, while disposed adjacent to channel portion 32, are also beneficially affected by embodiments of the present invention. Although electrons 404 are not obviously redirected to avoid channel portions of higher doping concentration, electrons 404 are affected by the localized increased concentration of charge carriers resulting in electrostatic forces acting upon electrons 404 in a similar manner to the electrostatic forces acting upon electrons 403 and 405.

Figure 4C shows a cumulative effect of the present retrograde channel on charge carrier flow, according to an embodiment of the present invention. Electrons in region 401 are inhibited from flowing in channel portions 33 and 31, favoring channel portion 32. However, due to the physically constrictive nature of channel portion 32 combined with electrostatic forces acting upon the like charge carriers, the electrons tend to "bunch up" at the interface between region 401 and channel portion 32. The net effect of "bunching up" is seen externally as a desirable increase in threshold voltage, and a corresponding decrease in leakage current.

It is to be appreciated that although a PMOS device has been illustrated herein, embodiments of the present invention are well suited to NMOS devices as well. The choices of materials, e.g., for dopants, for use with NMOS devices are well understood in the semiconductor arts.

This novel design and method to implement this design reduce and/or eliminate the short channel effect, allowing for decreased feature size and increased density of memory cells. These beneficial results allow for less expensive memory devices with lower power consumption, rendering a competitive advantage to the users practicing embodiments of the present invention.

Embodiments of the present invention provide a means to prevent short channel effects in memory cells. Further embodiments of the present invention prevent short channel effects in a manner that is compatible and complimentary with existing approaches to minimize short channel effects. Still further embodiments of the present invention provide for the above mentioned solutions to be achieved with existing semiconductor processes and equipment without revamping well established tools and techniques.

The preferred embodiment of the present invention retrograde channel doping to improve short channel effect is thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.

CLAIMS

What is claimed is:

1. A method of manufacturing a memory semiconductor cell (30) comprising:

forming a first channel portion (33) to produce a first concentration of doping material, said first channel portion (33) disposed adjacent to an edge of a channel region closest to and substantially parallel to a gate region (16) of said memory semiconductor cell;

forming a second channel portion (31) to produce a second concentration of doping material, said second portion (31) disposed substantially parallel to said first channel portion (33); and

forming a third channel portion (32), disposed between said first channel portion (33) and said second channel portion (31), comprising a third concentration of doping material, wherein said third concentration is lower than said first concentration and lower than said second concentration.

2. The method as described in Claim 1 further comprising implanting a halo implant (20) disposed adjacent to a source region or a drain region of said memory semiconductor cell (30).

3. The memory semiconductor cell (30) described in Claim 1 wherein a source region of said memory semiconductor cell comprises a source extension region (11).

4. The method as described in Claim 1 further comprising forming said second channel portion (31) prior to the formation of said first channel portion (33).

5. The method as described in Claim 1 wherein said memory semiconductor cell (30) is non-volatile.

6. The method as described in Claim 5 wherein said memory semiconductor cell (30) comprises a nitride layer as a storage element (12B).

7. The method as described in Claim 5 wherein said memory semiconductor cell comprises a floating gate (12B) as a storage element.

8. A memory semiconductor cell (30) comprising:

a gate region (16), a source region (14) and a drain region (14);

a channel region (17) between said source region (14) and said drain region (14);

wherein said channel region (17) comprises:

a first channel portion (33) comprising a first concentration of doping material, said first channel portion (33) disposed adjacent to an edge of said channel region (17) closest to and substantially parallel to said gate region (16);

a second channel portion (31) comprising a second concentration of doping material, said second portion (31) disposed substantially parallel to said first channel portion (33); and

a third channel portion (32), disposed between said first channel portion (33) and said second channel portion (31), comprising a third concentration of doping material, wherein said third concentration is lower than said first concentration and lower than said second concentration.

9. The memory semiconductor cell described in Claim 8 wherein said channel region (17) further comprises a halo implant (20) disposed adjacent to said source region (14) or said drain region (14).

10. The memory semiconductor cell described in Claim 8 wherein said source region (17) comprises a source extension region (11).

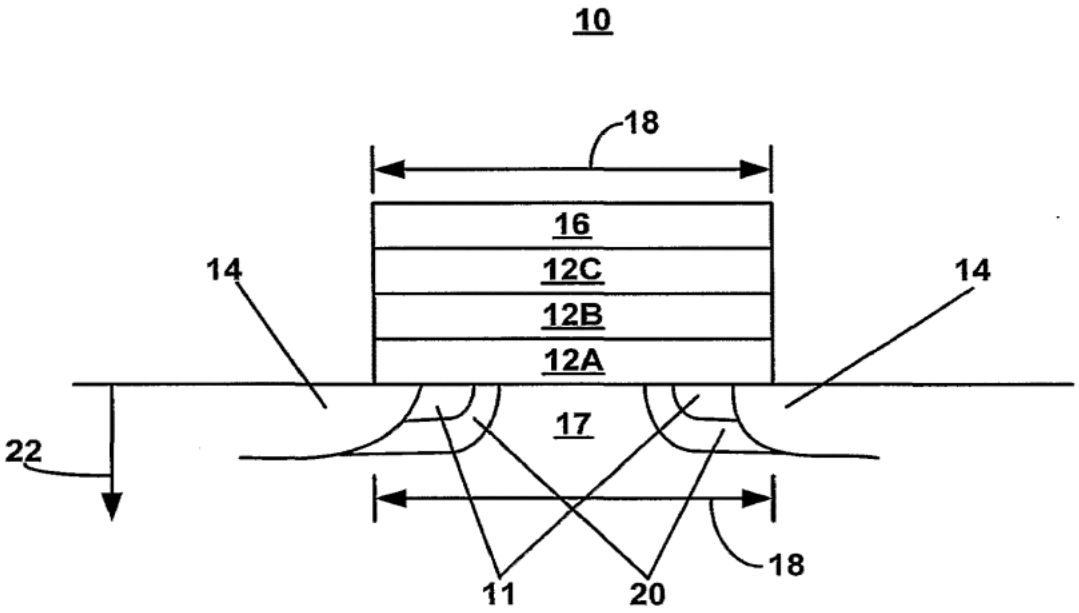

FIG. 1
(CONVENTIONAL ART)

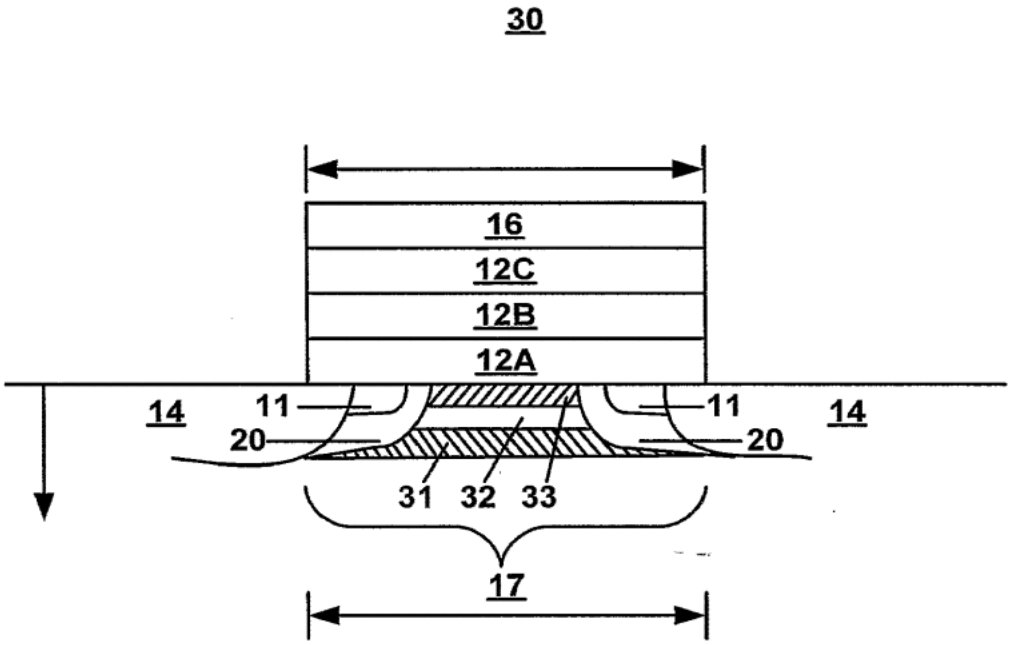

FIG. 2

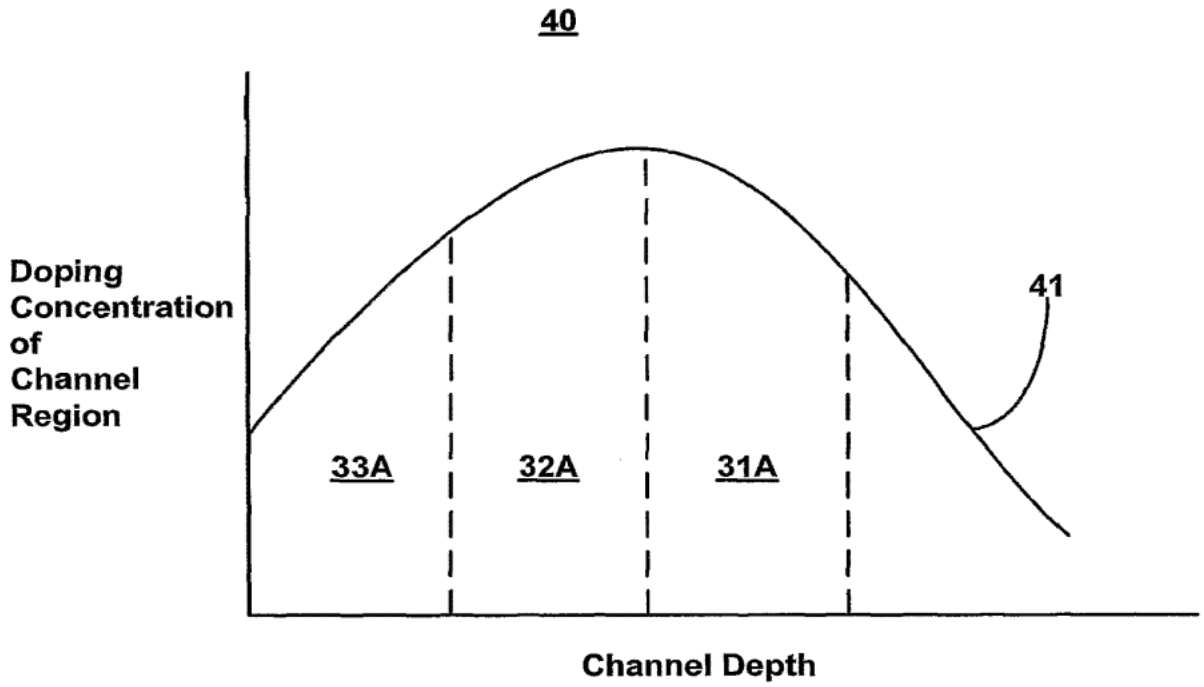
40
Doping Concentration of Channel Region
41
33A
32A
31A
Channel Depth

FIG. 3

4/4

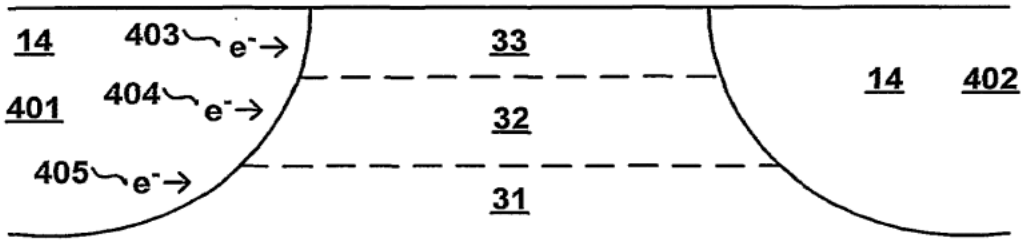

FIG. 4A

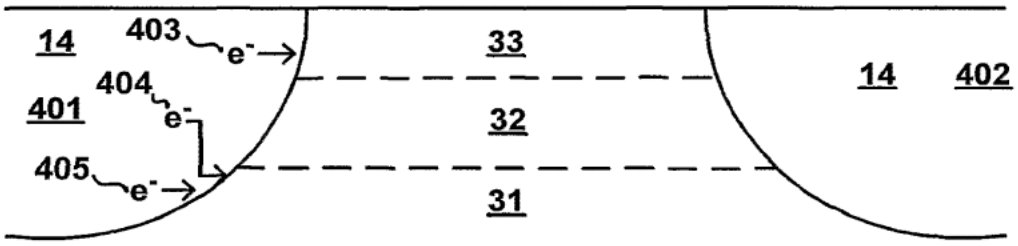

FIG. 4B

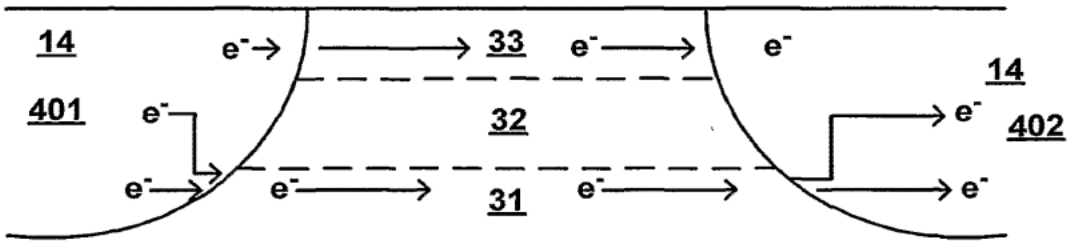

FIG. 4C

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/21682

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/788 H01L29/792 H01L21/8234 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2002/106852 A1 (CHANG CHI ET AL) 8 August 2002 (2002-08-08) paragraphs '0047!-'0055!; figures 5-8 ---	1-10
Y	US 5 923 985 A (AOKI KENJI ET AL) 13 July 1999 (1999-07-13) column 3, line 60 -column 4, line 28; figures 8A-8D,9 ---	1-10
Y	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 03, 30 March 2000 (2000-03-30) -& JP 11 354778 A (MITSUBISHI ELECTRIC CORP), 24 December 1999 (1999-12-24) abstract; figures --- -/--	1-10

[X] Further documents are listed in the continuation of box C.

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Date of the actual completion of the international search	Date of mailing of the international search report
11 February 2004	18/02/2004

Name and mailing address of the ISA	Authorized officer
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Y	PATENT ABSTRACTS OF JAPAN vol. 008, no. 161 (E-257), 26 July 1984 (1984-07-26) -& JP 59 061070 A (FUJITSU KK), 7 April 1984 (1984-04-07) abstract; figures	1-10

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 03/21682

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EFS ID:	43082725
Application Number:	16947294
International Application Number:	
Confirmation Number:	6907
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	40672
Filer:	Gregory Michael Howison/Joselyn Rodriguez
Filer Authorized By:	Gregory Michael Howison
Attorney Docket Number:	GRTD.01.01.DV7
Receipt Date:	30-JUN-2021
Filing Date:	27-JUL-2020
Time Stamp:	18:56:55
Application Type:	Utility under 35 USC 111(a)

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	NPL_Ex2014_AppendixA_10.pdf	8399723 9cb02bf0cc734fcdfd537d8536bc22752b7012f6	no	38

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12	Non Patent Literature	NPL_Ex2007_NPL_00288202002402Dkt61_MinutesforMarkmanHearing.pdf	115841 2efca8b9513c7638f5f83e6246b963d4b2362ba6	no	1
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14	Non Patent Literature	NPL_Ex2011_Dkt60_1_ExAtoRevisedJointClaimConstructionChart.pdf	235800 b10bb3ba6c806c49a91fe048e29873554066ee59	no	20
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17	Non Patent Literature	NPL_Exhibit_1003_292SmithDec.pdf	3253090 f5888c31c06f0d0ea10d74b7e15171a76649e132	no	82
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19	Non Patent Literature	NPL_IPR2020_00289_PetitionforInterPartesReview.pdf	2174024 321305047be749105f6cec4cd60edd3f8d300b77	no	91
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20	Non Patent Literature	NPL_IPR2020_00290_502Sur_Reply.pdf	188385 0faaf8f9b35326d29bc7b7f04723ee6a39873228	no	13
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Application Number	16947294
Filing Date	2020-07-27
First Named Inventor	G.R. Mohan Rao
Art Unit	2892
Examiner Name	ARORA, AJAY
Attorney Docket Number	GRTD60-35294

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	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
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	Examiner Name	ARORA, AJAY
	Attorney Docket Number	GRTD60-35294

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	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	ARORA, AJAY
	Attorney Docket Number	GRTD60-35294

	2	2003218356	JP	A	2003-07-31	Matsumoto et al.		☒
	3	s6482563	JP	A	1989-03-28	Kondo		☒
	4	2004049453	WO	A1	2004-06-10	Zheng et al.		☐

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	1	IPR2020-00288-Exhibit 1029-Claim Construction District Court 4 20-2020	
	2	IPR2020-00288-Exhibit 2007-Minutes for Markman Hearing Held Via Video Conference Before U.S. District Judge Rodney Gilstrap, Greenthread, LLC v. Samsung Electronics Co., Ltd., et al., Case No. 2:19-CV-147-JRG, Dkt. 61	
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	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	ARORA, AJAY
	Attorney Docket Number	GRTD60-35294

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	15	IPR2020-00288-Patent Owner Preliminary Response	
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	17	IPR2020-00288-Petition	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16947294
	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	ARORA, AJAY
	Attorney Docket Number	GRTD60-35294

	18	IPR2020-00289-Exhibit 1 to Appendix C of Samsung Electronics Co., Ltd.'s Invalidity Contentions regarding Payne	
	19	IPR2020-00289-Exhibit 1003-Smith Dec	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	ARORA, AJAY
	Attorney Docket Number	GRTD60-35294

	29	IPR2020-00289-Petition
	30	IPR2020-00290-Exhibit 1003-Declaration of Dr. Bruce Smith
	31	IPR2020-00290-Exhibit 1013-Tango, Mega bit Memory Technology
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	33	IPR2020-00290-Patent Owner Sur Reply
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	ARORA, AJAY
	Attorney Docket Number	GRTD60-35294

	40	IPR2020-00291-Exhibit 2001-Exhibit 2 to Appendix B of Samsung Electronics Co., LTD's Invalidity Contentions (Invalidity Contention based on U.S. Patent Application Publication No. 2002/0195656 ("Hattori"))	
	41	IPR2020-00291-Exhibit 2013- Declaration of Dr. Alexander D. Glew	
	42	IPR2020-00291-Patent Owner Preliminary Resp	
	43	IPR2020-00291-Patent Owner Sur Reply	
	44	IPR2020-00291-Petition	
	45	IPR2020-00291-Petitioners Reply	
	46	IPR2020-00292-Exhibit 1003-Declaration of Dr. Bruce Smith	
	47	IPR2020-00292-Exhibit 2001-Excerpt from Exhibit 1 to Appendix B of Samsung Electronics Co., Ltd.'s Invalidity Contentions (Invalidity Contention based on "Insulated Gate Bipolar Transistor IGBT Theory and Design" by Vinod Kumar Khanna	
	48	IPR2020-00292-Exhibit 2012-Excerpt from Exhibit A to Joint Claim Construction Chart Pursuant to Patent Rule 4-5, Greenthread, LLC v. Samsung Electronics Co., Ltd., et al., Case No. 2:19-CV-147-JRG, Dkt. 53-1 (Mar. 18, 2020)	
	49	IPR2020-00292-Patent Owner Preliminary Response	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16947294
	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	ARORA, AJAY
	Attorney Docket Number	GRTD60-35294

EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	Application Number	16947294
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CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Gregory M. Howison, Reg. #30646/	Date (YYYY-MM-DD)	2021-06-24
Name/Print	Gregory M. Howison	Registration Number	30646

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I, Michael Fletcher, declare:

1. I am well versed in both the Japanese and English languages and have over 15 years of experience translating Japanese technical documents into English.

2. The following translation of the patent document JPS64-482563 to English is accurate and complete to the best of my knowledge.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and accurate.

Executed this 18th day of September 2019, at Parowan, UT

Michael Fletcher

(19) JAPANESE PATENT OFFICE (JP)

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(54) Title of The Invention Semiconductor Device

(21) Application No. S62-241827

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(74) Agent Patent Attorney OIWA, Masuo and two others

Specification

(57) [Abstract] This publication is application data prior to electronic applications and so there is no abstract data recorded.

1. Title of The Invention

Semiconductor Device

2. What is Claimed Is

(1) A semiconductor device comprising a first conduction type first area; a second conduction type second area formed on the primary surface of one side of the first area; a first conductive type third area formed at least partially on the upper layer of the second area; a second conductive type fourth area formed partially on the upper layer of the third area; an insulator formed so as to cover at least from the primary surface of the second area to the primary surface of the third area reaching the primary surface of the fourth area; a first electrode formed on the primary surface of the other side of the first area; a second electrode formed on the primary surface of the insulator; and a third electrode formed at least in contact with the primary surface of the fourth area, wherein the impurity distribution of the second area comprises a gradient in the vertical direction relative to the primary surface.

(2) The semiconductor device according to claim 1, wherein the second area is prepared as a two layer structure of a medium concentration impurity area in contact with the first area and a low concentration impurity area in contact with the third area and there is an impurity distribution established in the medium concentration impurity area such that the impurity concentration decreases moving from the low concentration impurity area towards the first area.

(3) The semiconductor device according to claim 1, wherein an impurity distribution of the impurity concentration is established in the medium concentration impurity area with an increase moving from the low concentration impurity area toward the first area.

(4) The semiconductor device according to claim 1, wherein an impurity distribution of the impurity concentration is established in the low concentration impurity area with an increase moving from the third area toward the medium concentration impurity area.

(5) The semiconductor device according to claim 1, wherein an impurity distribution of the impurity concentration is established in the low concentration impurity area with an increase moving from the medium concentration impurity area towards the third area.

DETAILED DESCRIPTION OF THE INVENTION

FIELD OF INDUSTRIAL USE

The present invention is related to a semiconductor device and in particular to the improving of turn-off time for an insulated gate bipolar transistor (hereafter "IGBT").

BACKGROUND TECHNOLOGY

FIG. 5 (a) is a cross-section view of a conventional IGBT and FIG. 5 (b) is a schematic drawing showing the impurity distribution of each of the areas along the E-E line. In FIG. 5, 1 is a first P-type area with a P type impurity uniformly distributed at high concentration. A first N-type area 2 is formed on the primary surface of one side of this first P-type area 1 with N type impurities uniformly distributed at a medium concentration. In addition, a second N-type area 3 is formed on this first N-type area 2 with N type impurities uniformly distributed at low concentration. Furthermore, a plurality of mutually isolated second P-type areas 4 are formed on the upper layer of this second N-type area 3 with P type impurities uniformly distributed at a medium concentration. Also, a third N-type area 5 is formed over a part of the upper layers of the respective second P-type areas 4 with N type impurities uniformly distributed at high concentration. Furthermore, a gate electrode 7 is formed with an insulating film 6 interposed on the main surface of the second N-type area 3 and on a part of the main surface of the second P-type area 4. In addition, an emitter electrode 8 is formed on the remaining part of the main surface of the second P-type area 4 and the main surface of the third N-type area 5. On the other hand, a collector electrode 9 is formed overlain on the other primary surface of the first P-type area 1.

Next, the operating mechanism of the IGBT above will be described. First, under normal operating conditions, relative to the emitter electrode 8, positive high DC voltage is applied to the collector electrode 9 and further, positive stepped constant voltage is applied to the gate electrode 7. With stepped positive voltage applied between the gate and emitter in this manner, an N channel is formed at the boundary layer of the second P-type area 4 and insulating film 6, and electrons are injected through this N channel from the third N-type area 5 to the second N-type area 3 and first N-type area 2. Therefore, the potential of the second N-type area 3 and first N-type area 2 is reduced and the P-N junction at the boundary layer of the first P-type area 1 and first N-type area 2 is biased in the forward direction causing electron holes to be injected from the first P-type area 1 to the first N-type area 2. The injected electrons and electron holes neutralize electrically so large numbers of electrons and electron holes are supplemented and injected respectively from the third N-type area 5 and first P-type area 1 causing accumulation of a lot of electron holes and electrons on the first N-type area 2 and second N-type area 3. As a result, the specific resistance of the first N-type area 2 and second N-type area 3 is lowered setting the IGBT in conduction state with high current from the collector electrode 9 to the emitter electrode 8.

Next, when positive voltage is no longer applied to the gate electrode 7, the N channel at the boundary layer of the second P-type area 4 and insulating film 6 vanishes and electrons are no longer injected from the third N-type area 5 to the second N-type area 3 and first N-type area 2. The current based on this type of electron injection is equivalent to a PNP transistor with the first P-type area 1 as the emitter, the second N-type area 3 and first N-type area 2 as base, and the second P-type area 4 as the collector. Therefore, IGBT current in the case that electron injection is terminated is anticipated to be approximately the equivalent of PNP transistor current for the case that base current has been terminated for the PNP transistor. In other words, when electron injection is terminated, current flowing through the IGBT is reduced and FIG. 6 shows a schematic of this waveform.

In FIG. 6, the vertical axis is current flowing through the IGBT and horizontal axis is time. As shown in FIG. 6, at time t = t_0, when gate electrode positive voltage is terminated, current instantaneously drops from I_0 to I_1 and then gradually reduces to zero.

THE PROBLEM(S) THAT THIS INVENTION INTENDS TO RESOLVE

One of the elements that exhibits the current characteristics of this IGBT is the turn-off time t_{off}. This turn-off time is defined as

$$t_{off} = t_1 - t_0 \qquad (1)$$

Here, t_0 is the time that positive voltage is terminated on the gate electrode and t_1 is the time that current reaches $0.1I_0$.

As can be seen in FIG. 6, the turn-off time t_{off} is dependent on the current attenuation characteristics of the attenuation region from time t_0 to time t_1. Here, as described above, this IGBT approximates a PNP transistor so the current waveform in the attenuation region can be approximated using

$$I(t) = I_1 \exp\left(-\frac{t - t_0}{\beta \tau_b}\right) \qquad \cdots (2)$$

Here, β is the grounded emitter current gain and τ_b is the base travel time for a PNP transistor. In formula (2), if the value of $\beta\tau_b$ is reduced, attenuation in the attenuation region becomes remarkable enabling shortening the turn-off time t_{off} of the IGBT. Furthermore, approximation of βτb,

$$y = \beta \tau_b = \frac{\gamma \alpha_T}{1 - \gamma \alpha_T} \tau_b \qquad \cdots (3)$$

However,

$$\alpha_T = \mathrm{sech}\left(\sqrt{\frac{2\tau_b}{\tau_{eff}}}\right) \qquad \cdots (4)$$

Here, γ is the emitter injection efficiency of the PNP transistor. α_T is the base transport efficiency of the PNP transistor and τ_{eff} is the effective carrier lifespan inside the PNP transistor base area.

In the past, the effective carrier lifespan τ_{eff} inside the PNP transistor base area was reduced using electron beam irradiation to shorten the IGBT turn off time t_{off}. In other words, reducing the effective carrier lifetime τ_{eff} in the PNP transistor base area reduces the $\beta\tau_b$ value and as a result, current attenuation in the attenuation region becomes remarkable and the IGBT turn-off time t_{off} is shortened.

However, when the effective carrier lifespan τ_{eff} in the PNP transistor base area is reduce in this manner, there was the problem that the number of electron holes and electrons accumulated on the first N-type area 2 and second N-type area 3 was reduced while in conduction status and thus increased effective resistance.

An objective of the present invention is to resolve the problems as described above and obtain a semiconductor device with a short turn-off time while also having a small effective resistance while in conduction state.

MEANS FOR SOLVING THE VARIOUS PROBLEMS

The semiconductor device according to the present invention comprises a first conduction type first area; a second conduction type second area formed on the primary surface of one side of the first area; a first conductive type third area formed at least partially on the upper layer of the second area; a second conductive type fourth area formed partially on the upper layer of the third area; an insulator formed so as to cover at least from the primary surface of the second area to the primary surface of the third area reaching the primary surface of the fourth area; a first electrode formed on the primary surface of the other side of the first area; a second electrode formed on the primary surface of the insulator; and a third electrode formed at least in contact with the primary surface of the fourth area, wherein the impurity distribution of the second area is established so as to comprise a gradient in the vertical direction relative to the primary surface.

FUNCTION

Regarding the semiconductor device according to the present invention, the impurity distribution comprises a gradient in the vertical direction relative to the primary surface generating an internal electric field in the second area and the effective diffusion constant of carriers in the second area are controlled by this internal electric field, shortening the turn-off time.

EMBODIMENTS

FIG. 1 (a) is a cross-section view of the IGBT that is an embodiment of this invention, and FIG. 1 (b) is a schematic drawing showing the impurity distribution of each of the areas along the A-A line. In FIG. (1), the only point of difference from conventional is the N-type impurity distribution of a first N-type area 2. As shown in FIG. 1 (b), the N-type impurity concentration of the first N-type area 2 is the lowest at the boundary surface of a first P-type area 1. The value thereof increases when approaching a second N-type area 3, and reaches a medium concentration on the boundary surface of the second N-type area 3 in a similar manner to conventional.
In this manner, an internal electric field is generated within the first N-type area 2 by providing a slope to the N-type impurity concentration of the first N-type area 2. The type of internal electric field that is generated based on the slope of the N-type impurity concentration is described as follows. The relationship between this internal electric field and the N type impurities is given by

$$E(x) = -\frac{kT}{q} \cdot \frac{1}{N(x)} \cdot \frac{dN(x)}{dx} \quad \cdots (5)$$

Here, E(x) is the internal electric field, k is the Boltzmann's constant, T is absolute temperature, q is the amount of electron charge, and N(x) is the N-type impurity concentration distribution. As understood from formula (5), the internal electric field direction and the N-type impurity concentration distribution gradient are in opposite directions. Therefore, when indicating an N-Type impurity concentration distribution such as the one shown in FIG. 1, the internal electric field directionality is from the second N-type area 3 towards the first P-type area 1. This type of internal electric field will act to obstruct the diffusion of electron holes that are injected through the first P-type area 1 and attempting to diffuse to the second N-type area 3, reducing the effective electron hole diffusion constant.

FIG. 2 (a) is a cross-section view of the IGBT that is another embodiment of this invention, and FIG. 2 (b) is a schematic drawing showing the impurity distribution of each of the areas along the B-B line. Regarding points of difference from conventional in this drawing, as shown in FIG. 2 (b), the N-type impurity concentration of the first N-type area 2 at the boundary surface with the second N-type area 3 has a low concentration in a similar manner to the N-type impurity concentration of the second N-type area 3. With approaching the first P-type

area 1, the value thereof increases, reaching a medium concentration at the boundary surface similar to conventional.

By providing a slope opposite to what is shown in FIG. 1 for the N-type impurity concentration of the first N-type area 2 in this manner, an internal electric field opposite of the one shown in the first drawing is generated in the first N-type area 2. Therefore, as this internal electric field acts in a direction accelerating electron hole diffusion, the effective electron hole diffusion constant is increased.

FIG. 3 (a) is a cross-section view of the IGBT that is another embodiment of this invention, and (b) of the same FIG. is a schematic drawing showing the impurity distribution of each of the areas along the C-C line. Regarding points of difference from conventional in this drawing, as shown in FIG. 3 (b), the N-type impurity concentration of the second N-type area 3 has a low concentration at the boundary surface with the second p-type area 4 in a similar manner to that of conventional. With approaching the first N-type area 2, the value thereof increases, reaching a medium concentration of N type impurity concentration in the first N-type area 2 at the boundary surface with the first N-type area 2.

By providing a slope opposite to that shown in FIG. 1 for the N-type impurity concentration of the second N-type area 3 in this manner, an internal electric field opposite of the one shown in FIG. 1 is generated in the second N-type area 3. Therefore, as this internal electric field acts in a direction accelerating electron hole diffusion, the effective electron hole diffusion constant is increased.

FIG. 4 (a) is a cross-section view of the IGBT that is another embodiment of this invention, and FIG. 4 (b) is a schematic drawing showing the impurity distribution of each of the areas along the D-D line. For points of difference from convention in this drawing as shown in FIG. 4 (b), the N-type impurity concentration of the second N-type area 3 has a low concentration at the boundary surface with the first N-type area 2 in a similar manner to that of conventional. With approaching the second P-type area 4, the value thereof increases, reaching a high concentration at the boundary surface with the second P-type area 4.

By providing a slope the same as that shown in FIG. 1 for the N-type impurity concentration of the second N-type area 3 in this manner, an internal electric field the same as the one shown in FIG. 1 is generated in the second N-type area 3. Therefore, as this internal electric field acts in the direction of obstructing electron hole diffusion, the effective electron hole diffusion constant is decreased.

As stated above, a suitable internal electric field is generated in either the first N-type area 2 or the second N-type area 3 by applying a gradient to the impurity distribution of either the first N-type area 2 or the second N-type area 3 in the direction vertical relative to the main surface, and the effective diffusion constant of the electron holes of the first N-type area 2 or the second N-type area 3 can be controlled.

Next is a description of the theory behind shortening of the IGBT turn-off time by controlling the electron hole effective diffusion constant.

Here, for the base area, or in other words when assuming that the thickness of the first N-type area 2 and the second N-type area 3 do not change, the base travel time is reduced as the electron hole diffusion constant becomes larger, and conversely, the base travel time increases as the electron hole diffusion constant becomes smaller. In other words, the base travel time can be controlled by controlling the electron hole diffusion constant. Furthermore, the IGBT turn-off time can be controlled by controlling the base travel time. Next is a description of the reasons why this is the case.

First, differentiating the approximation formula $\beta\tau_b$ (3) by the base travel time T_b is

$$\frac{dy}{d\tau_b} > 0 \quad \text{Gives} \quad \frac{2\tau_b}{\tau_{eff}} < \sqrt{2} \qquad \cdots (6)$$

$$\frac{dy}{d\tau_b} < 0 \quad \text{Gives} \quad \frac{2\tau_b}{\tau_{eff}} > \sqrt{2} \qquad \cdots (7)$$

If equation (6) is valid, the turn-off time t_{off} is shortened as the base travel time τ_b becomes smaller. On the other hand, if equation (7) is valid, the turn-off time t_{off} is shortened as the base travel time τ_b becomes larger.

By generating an internal electric field in the first N-type area 2 or the second N-type area 3 as a result of applying a slope to the impurity concentration distribution of either the first N-type area 2 or the second N-type area 3, the electron hole diffusion constant in addition to the base travel time can be controlled, which enables shortening the IGBT turn-off time. In addition, the actions described above enable shortening the turn-off time without reduction of the effective carrier lifespan of the first N-type area 2 or second N-type area 3 that was required previously and enables suppressing the effective resistance of the first N-type area 2 or second N-type area 3.

Next is a description based on the FIG. 1 regarding a manufacturing method of a semiconductor device according to the present invention. First, the first N-type area 2 is formed on the first P-type area 1 using the vapor-phase epitaxial growth method. When conducting vapor-phase epitaxial growth, the first N-type area 2 with an N-type impurity concentration distribution as shown in FIG. 1 (b) can be obtained by gradually increasing the N-type impurity concentration in proportion to the growth film thickness. Next, the second N-type area 3 is formed on the first N-type area 2 using the vapor-phase epitaxial growth principle. Furthermore, by applying the manufacturing process of a normal double-diffusion-type MOS transistor, the second P-type area 4, third N-type area 5, insulating film 6, gate electrode 7, and emitter electrode 8 are formed, and the IGBT as shown in the FIG. can be produced.

In addition, if a gradient is applied to the N-type impurity concentration to a first N-type area 3 [sic] as shown in FIG. 2, the N-type impurity concentration can be reduced gradually based on the growth film thickness when forming the first N-type area 2 on the first P-type area 1 in accordance with the vapor-phase epitaxial growth principle.

In addition, if a gradient is applied to the N-type impurity concentration of the second N-type area 3 as shown in FIG. 3 and FIG. 4, the N-type impurity concentration can be changed gradually based on the growth film thickness when forming the second N-type area 3 on the first N-type area 2 in accordance with the vapor-phase epitaxial growth principle.

EFFECT OF THE INVENTION

The turn-off time is shortened for the semiconductor device of the present invention by controlling the carrier effective diffusion constant in addition to the base travel time using the internal electric field generated by the

impurity concentration distribution. This results in enabling obtaining a high-performance semiconductor device without increasing the effective resistance while in a conductive state.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a drawing showing an embodiment of the present invention. FIG. 2 through FIG. 4 are drawings showing other embodiments of the present invention. FIG. 5 is a drawing showing a conventional example. FIG. 6 is a drawing showing the relationship between the electric current and the time where voltage applied to the IGBT gate electrode is stopped.

In the drawings, 1 is the first P-type area, 2 is the first N_type area, 3 is the second N-type area, 4 is the second P-type area, 5 is the third N-type area, 6 is the insulating film, 7 is the gate electrode, 8 is the emitter electrode, and 9 is the collector electrode

Furthermore, the same symbols in the drawings indicate the same or corresponding parts.

FIG. 6

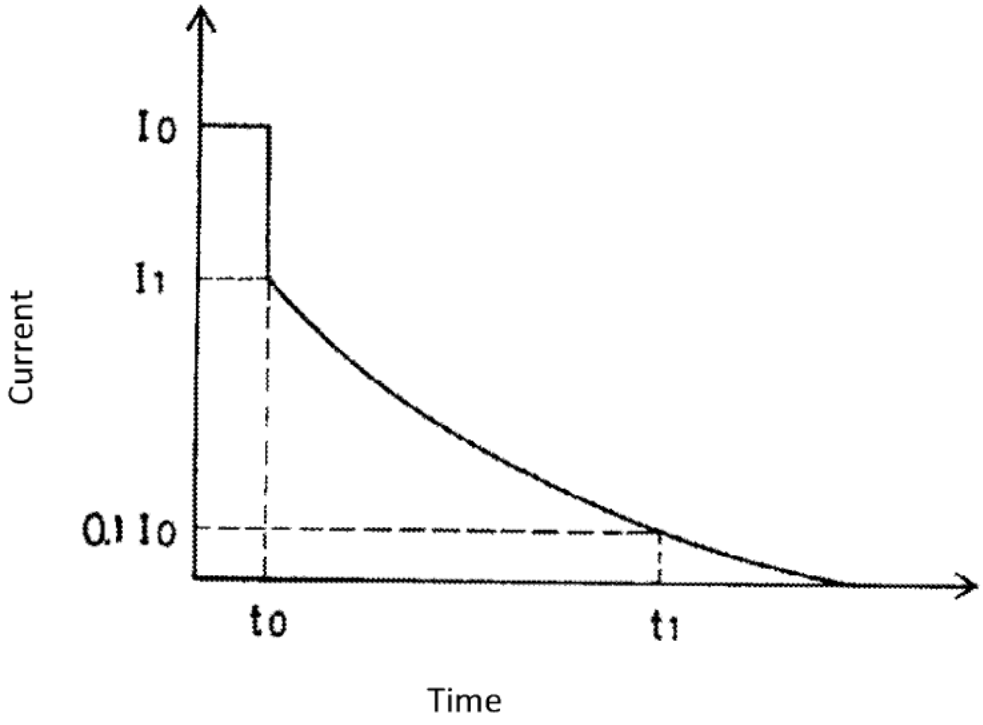
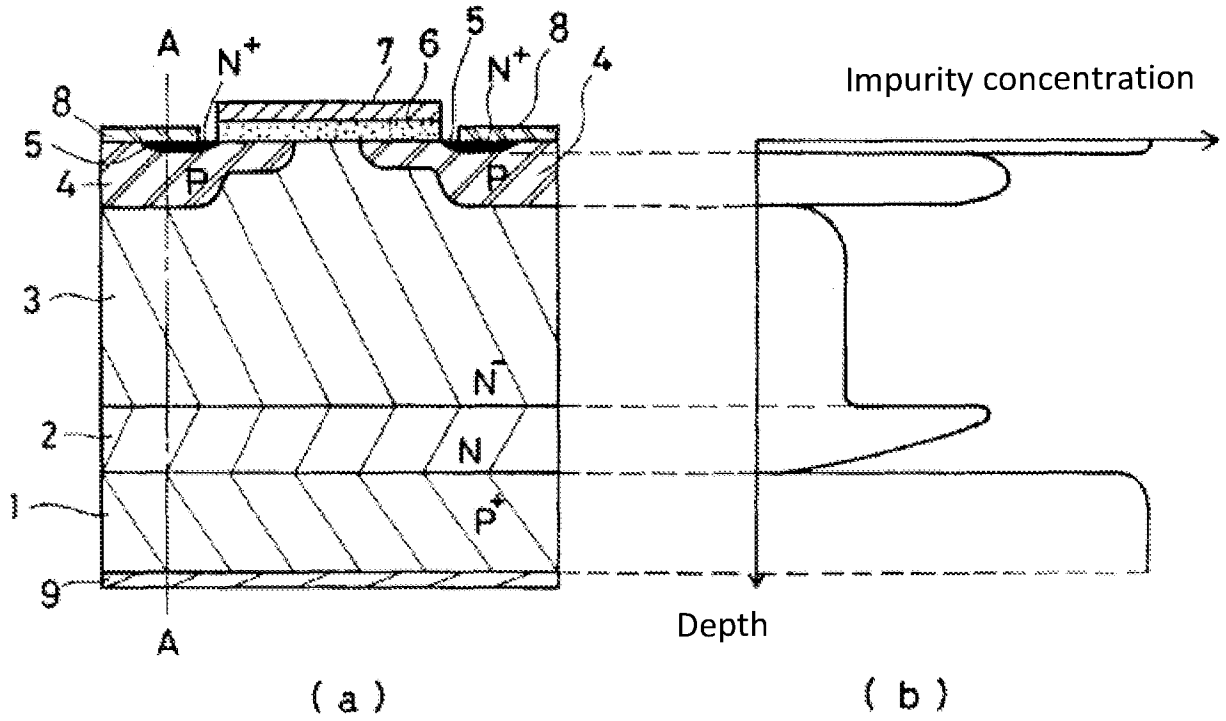


FIG. 1



1: First P type area
2: First N type area
3: Second N type area
4: Second P type area
5: Third N type area
6: Insulator film
7: Gate electrode
8: Emitter electrode
9: Collector electrode

FIG. 2

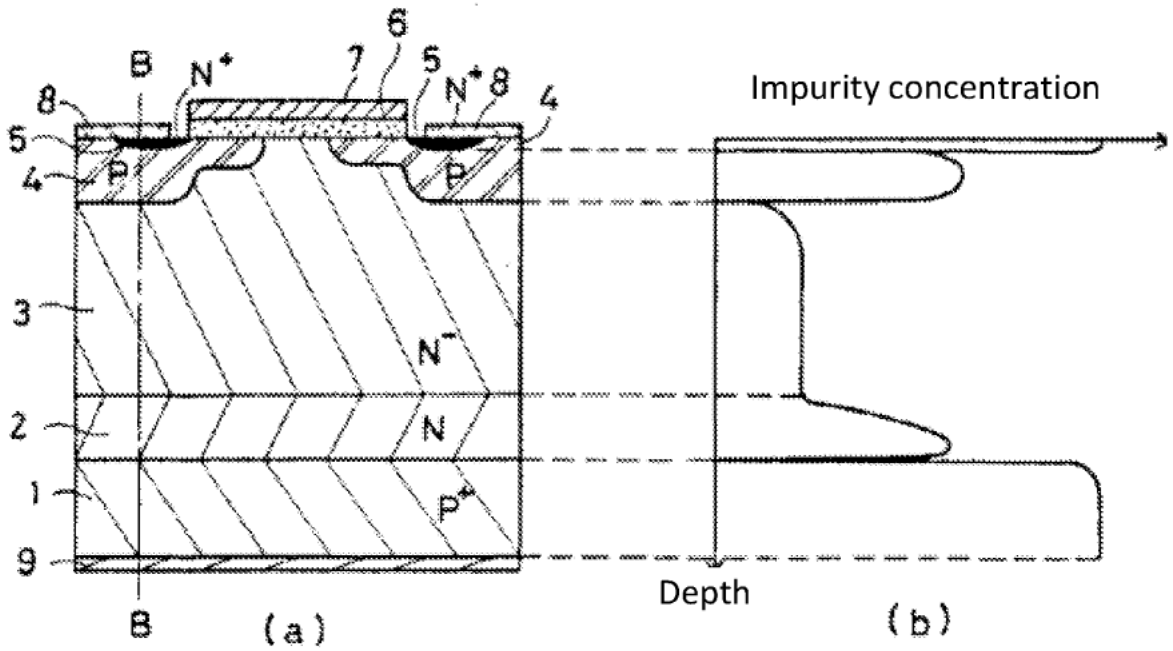

B
N+
7
6
5
N+
8
4
8
5
4
P
P
3
N−
2
N
1
P+
9
B
(a)
Impurity concentration
Depth
(b)

FIG. 3

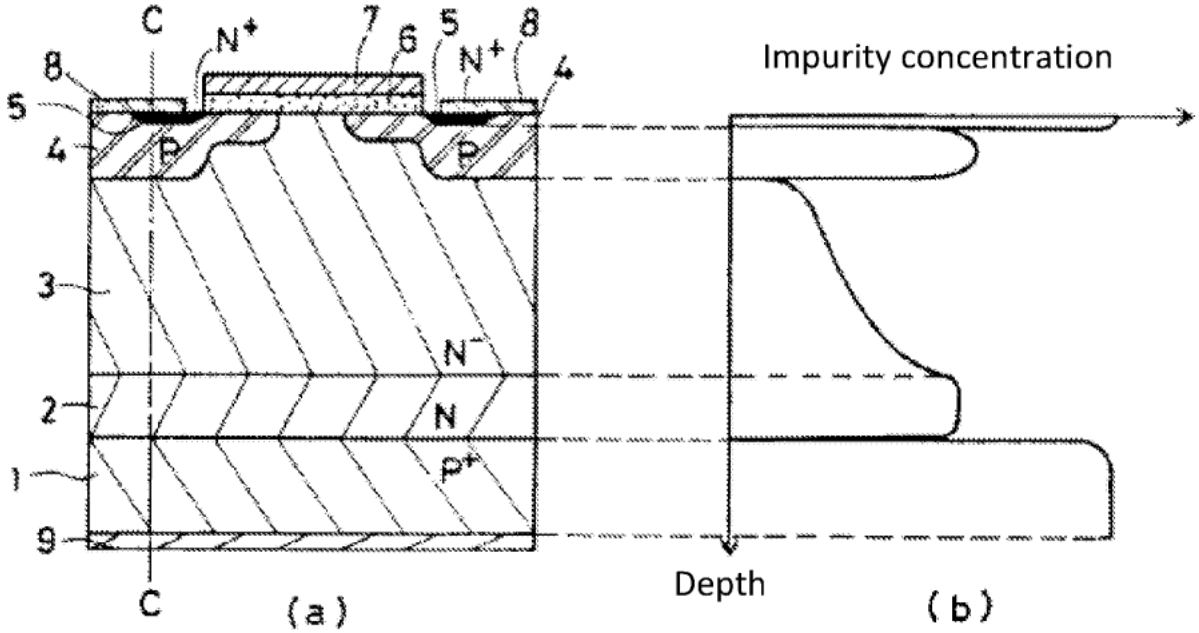

C
N+
7
6
5
N+
8
4
8
5
4
P
P
3
N−
2
N
1
P+
9
C
(a)
Impurity concentration
Depth
(b)

FIG. 4

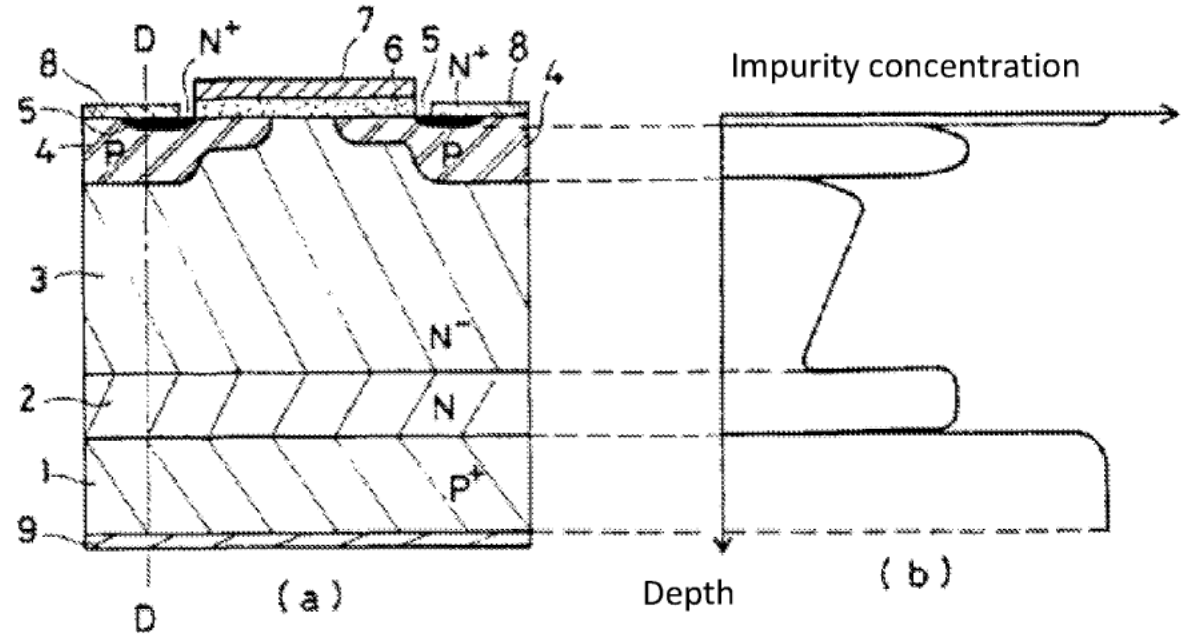
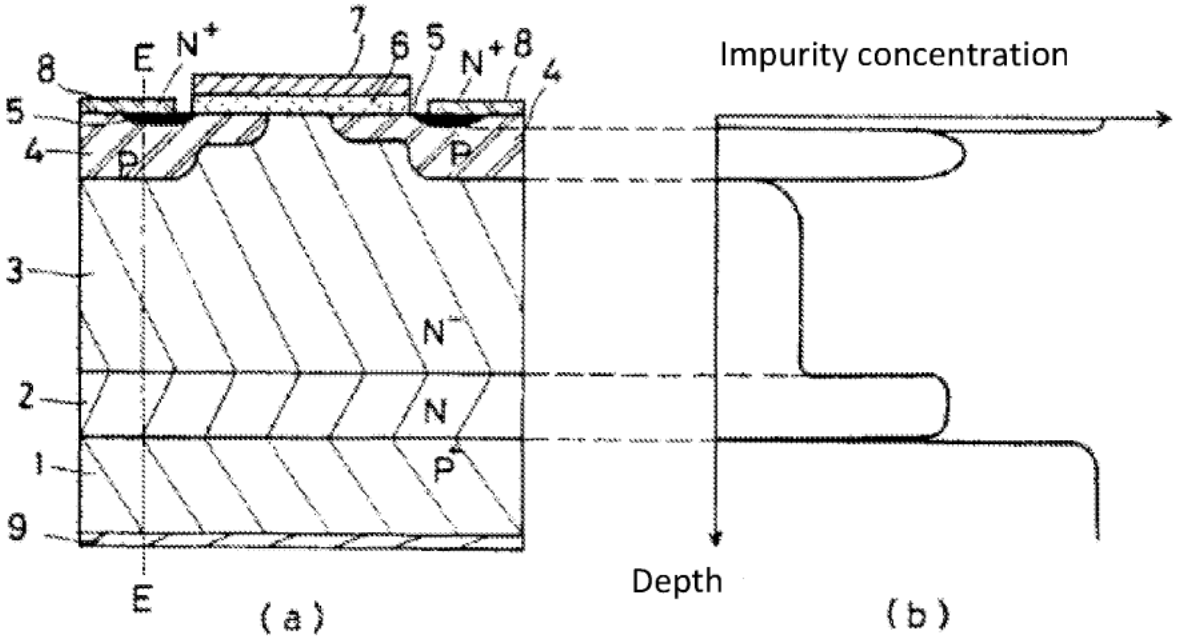

D
N+
7
6
5
N+
8
8
4
5
4
P
P
3
N−
2
N
1
P+
9
D
(a)
Impurity concentration
Depth
(b)

FIG. 5


E
N+
7
6
5
N+
8
8
4
5
4
P
P
3
N−
2
N
1
P+
9
E
(a)
Impurity concentration
Depth
(b)

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⑤4発明の名称　半導体装置

⑳特　願　昭62－241827

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明　細　書

1．発明の名称

半導体装置

2．特許請求の範囲

(1)　第1導電型の第1領域と、

前記第1領域の一方の主表面上に形成された第2導電型の第2領域と、

前記第2領域の上層部に少なくとも1箇所部分的に形成された第1導電型の第3領域と、

前記第3領域の上層部に部分的に形成された第2導電型の第4領域と、

前記第2領域の主表面から前記第4領域の主表面に至る前記第3領域の主表面を少なくとも覆うように形成された絶縁体と、

前記第1領域の他方の主表面に形成された第1電極と、

前記絶縁体の主表面上に形成された第2電極と、

少なくとも前記第4領域の主表面に接するように形成された第3電極とを有する半導体装置において、

前記第2領域内における不純物分布が主表面に対して垂直な方向に勾配を有することを特徴とする半導体装置。

(2)　前記第2領域は、前記第1領域に接する中濃度不純物領域と前記第3領域に接する低濃度不純物領域の2層構造に仕上げられ、前記中濃度不純物領域内の不純物濃度が前記低濃度不純物領域から前記第1領域に向かうにつれて減少するように不純物分布が定められている特許請求の範囲第1項記載の半導体装置。

(3)　前記中濃度不純物領域内の不純物濃度が前記低濃度不純物領域から前記第1領域に向かうにつれて増加するように不純物分布が定められている特許請求の範囲第1項記載の半導体装置。

(4)　前記低濃度不純物領域内の不純物濃度が前記第3領域から前記中濃度不純物領域に向かうにつれて増加するように不純物分布が定められている特許請求の範囲第1項記載の半導体装置。

(5)　前記低濃度不純物領域内の不純物濃度が前記中濃度不純物領域から前記第3領域に向かう

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につれて増加するように不純物分布が定められている特許請求の範囲第１項記載の半導体装置。

３．発明の詳細な説明

〔産業上の利用分野〕

この発明は半導体装置、特に絶縁ゲート型バイポーラトランジスタ（以下「ＩＧＢＴ」という）のターンオフ時間の改善に関するものである。

〔従来の技術〕

第５図(a)は従来のＩＧＢＴの断面図であり、同図(b)はＥ－Ｅ線に沿った各領域における不純物分布を模式的に示した図である。同図において、１は高濃度で均一にＰ型不純物が分布されている第１Ｐ型領域であり、この第１Ｐ型領域１の一方の主表面上に中濃度で均一にＮ型不純物が分布されている第１Ｎ型領域２が形成されている。また、この第１Ｎ型領域２上に低濃度で均一にＮ型不純物が分布されている第２Ｎ型領域３が形成されている。そして、この第２Ｎ型領域３の上層部に中濃度で均一にＰ型不純物が分布されている第２Ｐ型領域４が複数相互に隔離されて形成されており、さらに、この第２Ｐ型領域４のそれぞれの上層部に高濃度で均一にＮ型不純物が分布されている第３Ｎ型領域５が部分的に形成されている。そして、第２Ｎ型領域３の主表面および第２Ｐ型領域４の主表面の一部上に絶縁薄膜６を介してゲート電極７が形成されている。また、第２Ｐ型領域４の主表面の残りの部分および第３Ｎ型領域５の主表面上にエミッタ電極８が形成されている。一方、第１Ｐ型領域１の他方の主表面にはコレクタ電極９が積層して形成されている。

次に、上記ＩＧＢＴの動作機構について説明する。まず、通常の動作状態では、エミッタ電極８に対して負荷抵抗を通して正の直流高電圧をコレクタ電極９に印加し、さらに、正のステップ状定電圧をゲート電極７に印加する。このようにステップ状の正電圧がゲート・エミッタ間に印加されると、第２Ｐ型領域４と絶縁薄膜６との境界面にＮチャネルが形成され、そのＮチャネルを通して第３Ｎ型領域５から第２Ｎ型領域３および第１Ｎ型領域２に電子が注入される。そのため、第２Ｎ型領域３および第１Ｎ型領域２の電位が低下し、第１Ｐ型領域１と第１Ｎ型領域２との界面にあるＰ－Ｎ接合が順方向バイアスされることとなり、第１Ｐ型領域１から第１Ｎ型領域２および第２Ｎ型領域３に正孔が注入される。注入された電子と正孔は電気的に中和されるので、第３Ｎ型領域５および第１Ｐ型領域１からそれぞれ電子および正孔がさらに補充されて多数注入され、第１Ｎ型領域２および第２Ｎ型領域３に多数の正孔および電子が蓄積される。その結果、第１Ｎ型領域２および第２Ｎ型領域３の比抵抗が低下し、コレクタ電極９からエミッタ電極８へ大電流が流れＩＧＢＴは導通状態になる。

次に、ゲート電極７への正電圧の印加がなくなると、第２Ｐ型領域４と絶縁薄膜６との界面のＮチャネルが消滅し、第３Ｎ型領域５から第２Ｎ型領域３および第１Ｎ型領域２の電子への注入がなくなる。このような電子注入による電流は、第１Ｐ型領域１をエミッタ，第２Ｎ型領域３と第１Ｎ型領域２をベース，また第２Ｐ型領域４をコレクタとするＰＮＰトランジスタのベース電流に相当している。したがって、電子注入がなくなった場合のＩＧＢＴの電流は、近似的にＰＮＰトランジスタにおいてベース電流がなくなった場合のＰＮＰトランジスタの電流に等しいと考えられる。つまり、電子注入がなくなった場合、ＩＧＢＴを流れる電流は減少し、その波形は模式的に第６図に示すようになる。

第６図において、縦軸はＩＧＢＴ中を流れる電流であり、横軸は時間を示す。同図に示すように、時刻$t = t_0$においてゲート電極の正電圧がなくなると、電流は瞬間的にI_0からI_1に減少したのち、徐々に零まで減少する。

〔発明が解決しようとする問題点〕

このＩＧＢＴの電流特性を表す要素のひとつとして、ターンオフ時間t_{off}がある。このターンオフ時間t_{off}は、

$$t_{off} = t_1 - t_0 \quad \cdots (1)$$

と定義される。ここで、t_0はゲート電極の正電圧がなくなる時刻であり、t_1は電流が０．１

I_0 になる時刻である。

同図からわかるように、このターンオフ時間 t_{off} は時刻 t_0 から時刻 t_1 にかけての減衰領域における電流の減衰特性に依存する。そこで、上記のごとく、このＩＧＢＴがＰＮＰトランジスタに類似していることから減衰領域における電流波形を

$$I(t) = I_1 \exp\left(-\frac{t-t_0}{\beta\tau_b}\right) \quad \cdots(2)$$

のように近似的に表すことができる。ここで、β はＰＮＰトランジスタにおけるエミッタ接地電流利得であり、τ_b はＰＮＰトランジスタにおけるベース走行時間である。(2) 式において、$\beta\tau_b$ の値を小さくすれば減衰領域における減衰が顕著になり、ＩＧＢＴのターンオフ時間 t_{off} を短くすることができる。さらに、$\beta\tau_b$ の近似式は、

$$y = \beta\tau_b = \frac{\gamma\alpha_T}{1-\gamma\alpha_T}\tau_b \quad \cdots(3)$$

ただし、

$$\alpha_T = \mathrm{sech}\left(\sqrt{\frac{2\tau_b}{\tau_{eff}}}\right) \quad \cdots(4)$$

となる。ここで、γ はＰＮＰトランジスタのエミッタ注入効率であり、α_T はＰＮＰトランジスタのベース輸送効率であり、τ_{eff} はＰＮＰトランジスタのベース領域内での実効キャリア寿命である。

従来においては、ＩＧＢＴのターンオフ時間 t_{off} を短くするために電子ビーム照射等によりＰＮＰトランジスタのベース領域内での実行キャリア寿命 τ_{eff} を小さくなるようにしていた。すなわち、このＰＮＰトランジスタのベース領域内での実効キャリア寿命 τ_{eff} を小さくすることにより $\beta\tau_b$ の値が小さくなり、その結果、減衰領域における電流の減衰が顕著になりＩＧＢＴのターンオフ時間 t_{off} が短くなる。

しかしながら、このようにＰＮＰトランジスタのベース領域内での実効キャリア寿命 τ_{eff} を小さくすると、導通状態で第１Ｎ型領域２および第２Ｎ型領域３に蓄積される正孔および電子の数が減少するため、実効抵抗が大きくなるという問題点があった。

この発明は上記のような問題点を解消するためになされたものであり、ターンオフ時間が短く、かつ導通状態での実効抵抗が小さい半導体装置を得ることを目的とする。

（問題点を解決するための手段）

この発明に係る半導体装置は、第１導電型の第１領域と、前記第１領域の一方の主表面上に形成された第２導電型の第２領域と、前記第２領域の上層部に少なくとも１箇所部分的に形成された第１導電型の第３領域と、前記第３領域の上層部に部分的に形成された第２導電型の第４領域と、前記第２領域の主表面から前記第４領域の主表面に至る前記第３領域の主表面を少なくとも覆うように形成された絶縁体と、前記第１領域の他方の主表面に形成された第１電極と、前記絶縁体の主表面上に形成された第２電極と、少なくとも前記第４領域の主表面に接するように形成された第３電極とを有する半導体装置において、前記第２領域内における不純物分布が主表面に対して垂直な方向に勾配を有するように定めている。

（作用）

この発明における半導体装置は、第２領域内における不純物分布が主表面に対して垂直な方向に勾配を有するようにしたことにより、前記第２領域内に内蔵電界が発生し、この内蔵電界により前記第２領域内でのキャリアの実効的な拡散定数が制御されてターンオフ時間を短くする。

（実施例）

第１図(a) はこの発明に係る一実施例であるＩＧＢＴの断面図であり、同図(b) はＡ－Ａ線に沿った各領域における不純物分布を模式的に示した図である。同図において、従来との相違点は第１Ｎ型領域２におけるＮ型不純物の分布のみである。同図(b) に示すように、第１Ｎ型領域２におけるＮ型不純物の濃度は第１Ｐ型領域１との境界面で最低であり、第２Ｎ型領域３に近ずくにしたがってその値は高くなっていき、第２Ｎ型領域３との境界面で従来と同じく中濃度となる。

このように第１Ｎ型領域２におけるＮ型不純物の濃度に傾斜を設けたことにより第１Ｎ型領域２ないで内蔵電界が発生する。ここで、Ｎ型不純物濃度の傾斜によりどのような内蔵電界が発生するかについて詳説する。この内蔵電界とＮ型不純物の分布との関係は、

$$E(x) = -\frac{kT}{q} \cdot \frac{1}{N(x)} \cdot \frac{dN(x)}{dx} \quad \cdots (5)$$

である。ここで、Ｅ(x) は内蔵電界であり、ｋはボルツマン定数であり、Ｔは絶対温度であり、ｑは電子の電荷量であり、Ｎ(x) はＮ型不純物濃度分布である。(5) 式からわかるように、内蔵電界の方向とＮ型不純物濃度分布の勾配とが逆方向である。そのため、第１図に示すようなＮ型不純物濃度分布を示す場合には内蔵電界は第２Ｎ型領域３から第１Ｐ型領域１に向っている。このような内蔵電界は第１Ｐ型領域１から注入され第２Ｎ型領域３に拡散しようとしている正孔の拡散を阻止する方向に働くので、実効的な正孔の拡散定数は小さくなる。

第２図(a) はこの発明に係る他の実施例であるＩＧＢＴの断面図であり、同図(b) はＢ－Ｂ線に沿った各領域における不純物分布を模式的に示した図である。同図において、従来との相違点は、同図(b) に示すように、第１Ｎ型領域２におけるＮ型不純物の濃度が第２Ｎ型領域３との境界面で第２Ｎ型領域３におけるＮ型不純物の濃度と同じく低濃度であり、第１Ｐ型領域１に近ずくにしたがってその値は高くなっていき、第１Ｐ型領域１との境界面で従来と同じく中濃度となるようにしたことである。

このように第１Ｎ型領域２におけるＮ型不純物の濃度において第１図に示したものとは逆の傾斜を設けたことにより、第１Ｎ型領域２内で第１図に示したものとは逆の内蔵電界が発生する。したがって、この内蔵電界が正孔の拡散を加速する方向に働くので、実効的な正孔の拡散定数は大きくなる。

第３図(a) はこの発明に係る他の実施例であるＩＧＢＴの断面図であり、同図(b) はＣ－Ｃ線に沿った各領域における不純物分布を模式的に示した図である。同図において、従来との相違点は、同図(b) に示すように、第２Ｎ型領域３におけるＮ型不純物の濃度は第２Ｐ型領域４との境界面で従来と同じく低濃度であり、第１Ｎ型領域２に近ずくにしたがってその値は高くなっていき、第１Ｎ型領域２との境界面で第１Ｎ型領域２におけるＮ型不純物の濃度と同じく中濃度となるようにしたことである。

このように第２Ｎ型領域３におけるＮ型不純物の濃度に第１図に示したものとは逆の傾斜を設けたことにより第２Ｎ型領域３内で第１図に示したものとは逆の内蔵電界が発生する。したがって、この内蔵電界が正孔の拡散を加速する方向に働くので、実効的な正孔の拡散定数は大きくなる。

第４図(a) はこの発明に係る他の実施例であるＩＧＢＴの断面図であり、同図(b) はＤ－Ｄ線に沿った各領域における不純物分布を模式的に示した図である。同図において、従来との相違点は、同図(b) に示すように、第２Ｎ型領域３におけるＮ型不純物の濃度は第１Ｎ型領域２との境界面で従来と同じく低濃度であり、第２Ｐ型領域４に近ずくにしたがってその値は高くなっていき、第２Ｐ型領域４との境界面で従来よりもやや高い濃度となるようにしたことである。

このように第２Ｎ型領域３におけるＮ型不純物の濃度に第１図に示したものと同じ傾斜を設けたことにより第２Ｎ型領域３内で第１図に示したものと同じ内蔵電界が発生する。したがって、この内蔵電界が正孔の拡散を阻止する方向に働くので、実効的な正孔の拡散定数は小さくなる。

以上のように、第１Ｎ型領域２あるいは第２Ｎ型領域３における不純物分布を主表面に対して垂直な方向に勾配を有するようにすることにより第１Ｎ型領域２あるいは第２Ｎ型領域３に適当な内蔵電界が発生して、この第１Ｎ型領域２あるいは第２Ｎ型領域３での正孔の実効的な拡散定数を制御することができる。

次に、この正孔の実効的な拡散定数を制御することによりＩＧＢＴのターンオフ時間を短くする

ことができる原理について説明する。

ここでベース領域、言い換えれば第１Ｎ型領域２および第２Ｎ型領域３の厚みが変らないと仮定すると、正孔の拡散定数が大きくなるとベース走行時間が小さくなり、逆に正孔の拡散定数が小さくなると、ベース走行時間が大きくなる。すなわち、正孔の拡散定数を制御することによりベース走行時間を制御することができる。さらに、このベース走行時間を制御することにより、ＩＧＢＴのターンオフ時間を制御することができる。ここで、その理由について詳説する。

まず、$\beta\tau_b$の近似式である(3)式をベース走行時間τ_bで微分すると、

$$\frac{dy}{d\tau_b} > 0 \quad \text{但し} \quad \frac{2\tau_b}{\tau_{eff}} < \sqrt{2} \qquad \cdots(6)$$

$$\frac{dy}{d\tau_b} < 0 \quad \text{但し} \quad \frac{2\tau_b}{\tau_{eff}} > \sqrt{2} \qquad \cdots(7)$$

となる。(6)式が成立する場合には、ベース走行時間τ_bが小さくなるにしたがってターンオフ時間t_{off}は短くなり、一方、(7)式が成立する場合には、ベース走行時間τ_bが大きくなるにしたがってターンオフ時間t_{off}は短くなる。

以上のように第１Ｎ型領域２あるいは第２Ｎ型領域３の不純物濃度分布に傾斜をもたせ、その結果として、第１Ｎ型領域２あるいは第２Ｎ型領域３に発生する内蔵電界により正孔の拡散定数、ひいてはベース走行時間を制御し、これによりＩＧＢＴのターンオフ時間を短くすることができる。また、上記のようにしてターンオフ時間を短くすることができ、従来のように第１Ｎ型領域２あるいは第２Ｎ型領域３の実効キャリア寿命を小さくする必要がないので、第１Ｎ型領域２あるいは第２Ｎ型領域３の実効抵抗は低く抑えることができなる。

次に、この発明に係る半導体装置の製造方法について第１図を基に説明する。まず、気相エピタキシャル成長法により第１Ｐ型領域１上に第１Ｎ型領域２を形成する。この気相エピタキシャル成長を行なう際、成長の膜厚に応じて徐々にＮ型不純物の濃度を高くすることにより第１図(b)に示すようなＮ型不純物濃度の分布を持った第１Ｎ型領域２が得られる。次に、気相エピタキシャル成長法により第１Ｎ型領域２上に第２Ｎ型領域３を形成する。さらに、通常の二重拡散型ＭＯＳトランジスタの製造工程を適用することにより、第２Ｐ型領域４，第３Ｎ型領域５，絶縁薄膜６，ゲート電極７およびエミッタ電極８を形成して同図に示すＩＧＢＴを製造することができる。

また、第１Ｎ型領域３に第２図に示すようなＮ型不純物濃度の分布の勾配を持たせる場合には、気相エピタキシャル成長法により第１Ｐ型領域１上に第１Ｎ型領域２を形成する際に、成長の膜厚に応じて徐々にＮ型不純物の濃度を低くしてやればよい。

また、第２Ｎ型領域３に第３図や第４図に示すようなＮ型不純物濃度の分布の勾配を持たせる場合には、気相エピタキシャル成長法により第１Ｎ型領域２上に第２Ｎ型領域３を形成する際に、成長の膜厚に応じて徐々にＮ型不純物の濃度を変化させてやればよい。

〔発明の効果〕

以上のように、この発明の半導体装置によれば、不純物濃度の分布によって発生する内蔵電界を利用してキャリアの実効拡散定数を、ひいてはベース走行時間を制御することによりターンオフ時間を短くしているので、導通状態での実効抵抗が増加することなく、高性能の半導体装置が得られる効果がある。

４．図面の簡単な説明

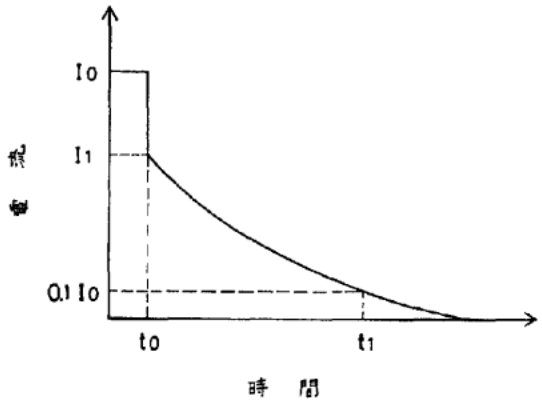
第１図はこの発明に係る一実施例を示す図、第２図ないし第４図はこの発明に係る他の実施例を示す図、第５図は従来例を示す図、第６図はＩＧＢＴのゲート電極への電圧印加を停止した際の時間と電流との関係を示す図である。

図において、１は第１Ｐ型領域、２は第１Ｎ型領域、３は第２Ｎ型領域、４は第２Ｐ型領域、５は第３Ｎ型領域、６は絶縁薄膜、７はゲート電極、８はエミッタ電極、９はコレクタ電極である。

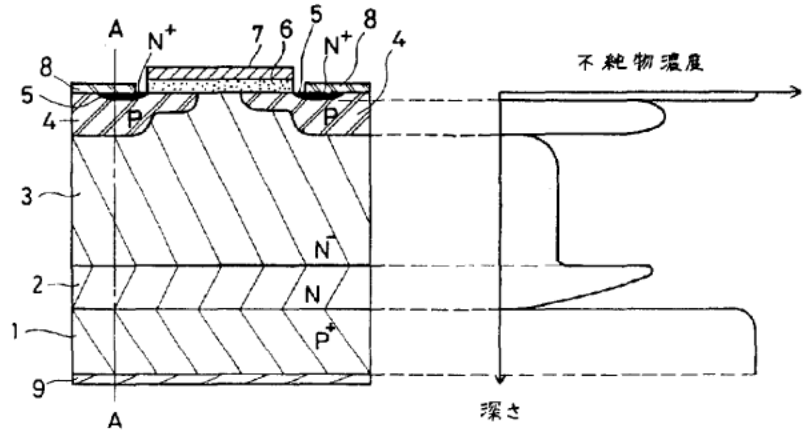
なお、各図中同一符号は同一または相当部分を示す。

代理人　大岩増雄

第 6 図

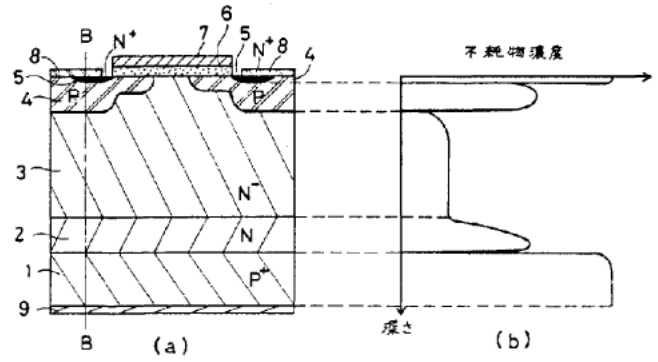


第 1 図

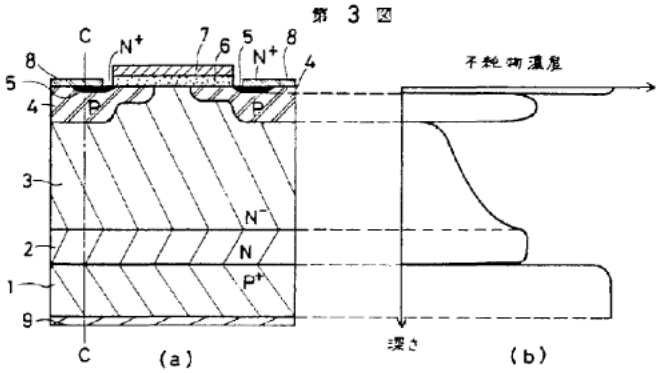


1：第1P型領域　2：第1N型領域
3：第2N型領域　4：第2P型領域
5：第3N型領域　6：絶縁薄膜
7：ゲート電極　8：エミッタ電極
9：コレクタ電極

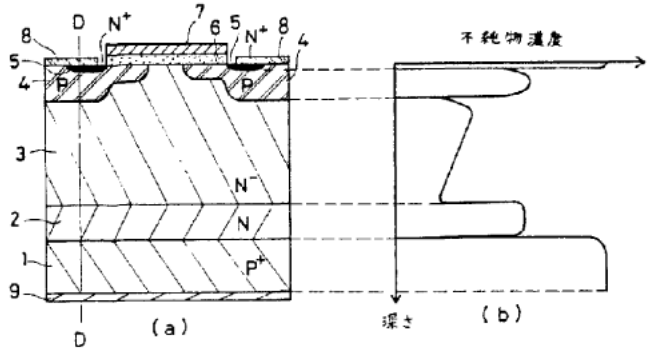
第 2 図



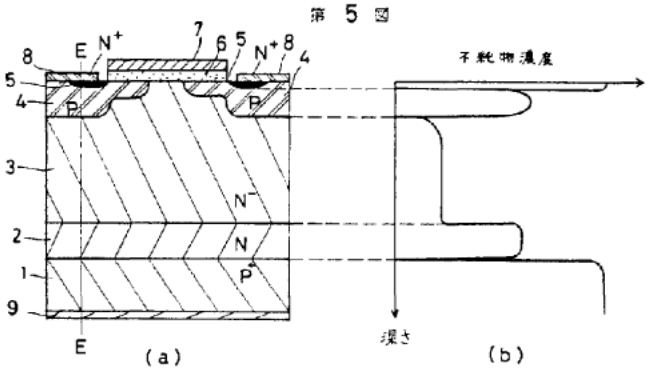
第 3 図



第 4 図



第 5 図



JP2003218356A METHOD FOR MANUFACTURING AND DESIGNING SOI TYPE SEMICONDUCTOR DEVICE, AND SOI TYPE SEMICONDUCTOR DEVICE

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[0001] BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to an SOI type semiconductor device manufacturing method, design method and SOI type semiconductor device having an SOI semiconductor layer formed on a semiconductor substrate with a buried insulating film interposed.

[0002] 2. Description of the Related Art SOI (Silicon On Insulator) structure facilitates complete isolation from the substrate or between elements, reducing various parasitic capacitances, and suppressing soft errors and latch-up characteristic of CMOS transistor circuits. become. For this reason, the role that SOI isolation technology plays in increasing the speed, lowering the voltage, and improving the reliability of so-called SOI-type CMOS LSIs has become increasingly important.

[0003] On the other hand, in many CMOS LSIs at present, P-type and N-type wells are formed in a semiconductor substrate (semiconductor bulk), N-type channel NMOS transistors are formed in the P-type well, and P-type wells are formed in the N-type well. This is a so-called bulk type semiconductor device in which a type-channel PMOS transistor is formed.

[0004] However, when designing an SOI type semiconductor device, since it has a substrate structure different from that of a bulk type semiconductor device having the same function, an already designed bulk type semiconductor device is provided. The layout pattern cannot be applied as it is. Therefore, in many cases, it has been necessary to re-design the pattern for SOI type semiconductor devices. This is because the bulk semiconductor device requires an electrode for fixing the well potential, while the SOI type semiconductor device uses the SOI semiconductor layer in a floating state, fixes the potential, or fixes the semiconductor substrate potential. One of the main reasons was the existence of various potential fixing methods.

[0005] The first object of the present invention is suitable, for example, when the SOI semiconductor layer is in a floating state and the substrate potential is fixed, and the layout pattern used in the bulk type semiconductor device is changed to the SOI type with a minimum change. An object of the present invention is to provide a design method for converting to a layout pattern of a semiconductor device and a method for manufacturing an SOI type semiconductor device including a step of forming a photomask using the method. A second object of the present invention is to provide an SOI type semiconductor device having a structure capable of making substrate contact even if the layout pattern of elements and wirings used in a bulk type semiconductor device is applied as it is.

[0006] According to a first aspect of the present invention, there is provided an SOI type semiconductor device manufacturing method for achieving the first object, wherein a buried insulating film is formed on a semiconductor substrate. A method for manufacturing an SOI type semiconductor device in which elements are integrated in an SOI semiconductor layer formed through the interposition, and corresponds to a well contact region of a bulk type semiconductor device in which elements are integrated in a well formed in a semiconductor substrate. A step of modifying the pattern of the element isolation insulating layer of the bulk type semiconductor device to form a photomask so that the element isolation insulating layer is also formed at the location, and the inside of the SOI semiconductor layer using the formed photomask Forming an element isolation insulating layer on the substrate, dividing the SOI semiconductor layer into a plurality of active layers in which elements are formed, and a portion corresponding to a well contact region of the bulk type semiconductor device Etching the element isolation insulating layer and the buried insulating film therebelow to form a substrate contact region, and utilizing a photomask for a well contact of the bulk type semiconductor device, the substrate in the substrate contact region Forming a contact plug.

[0007] Preferably, the method further includes a step of forming a source / drain impurity region to be a source or a drain of the insulated gate transistor in the active layer, and the same impurity is implanted from the substrate contact region simultaneously with the formation of the source / drain impurity region. Then, impurity regions for substrate contact connection are formed in the semiconductor substrate. Alternatively, preferably, a step of forming a source / drain impurity region to be a source or drain of an insulated gate transistor in the

active layer, and a step of forming a voltage supply plug connected on the source / drain impurity region; A step of forming a voltage supply wiring layer connected on the voltage supply plug, and in the step of forming the substrate contact plug, the well contact and source / drain impurity regions of the bulk type semiconductor device are formed. A contact opening using a photomask for simultaneously forming a voltage supply contact is formed, and the substrate contact plug is formed simultaneously with the voltage supply plug.

[0008] Preferably, the step of forming the element isolation insulating layer includes a step of forming a mask layer around a region where the element isolation insulating layer is to be formed, and an etching using the mask layer to form the buried insulating film on the SOI semiconductor layer. A step of forming a trench reaching, a step of depositing an element isolation insulating film filling the entire surface of the trench, and a step of partially removing the element insulating film around the trench, and forming the substrate contact region, Simultaneously with the step of removing the element isolation insulating film around the trench. In that case, the mask layer at the time of forming the trench includes a stopper film made of a material having a high etching selectivity with respect to the element isolation insulating film. In the step of forming the substrate contact region, the semiconductor surface of the active layer is formed by the stopper film. It is preferable to expose the surface portion of the semiconductor substrate to be contacted while protecting. Or after the said trench formation, you may further have the process of removing the said embedded insulating film part exposed in the trench by the etching using the said mask layer used for the said trench formation as it is.

[0009] An SOI type semiconductor device design method according to a second aspect of the present invention is for achieving the first object, and a bulk type semiconductor device in which elements are integrated in a well formed in a semiconductor substrate. The method for designing an SOI type semiconductor device includes a step of converting a pattern for use into an SOI type semiconductor device in which elements are integrated in an SOI semiconductor layer formed on a substrate with a buried insulating film interposed therebetween. When the bulk type semiconductor device has a well contact, the well contact pattern is used as it is as a substrate contact pattern reaching the semiconductor substrate of the SOI type semiconductor device in the conversion step.

[0010] Preferably, in the conversion step, the pattern of the element isolation insulating layer of the bulk type semiconductor device is partially modified so that the well contact region becomes the element isolation insulating layer, and the element isolation isolation of the SOI type semiconductor device is performed. Generating a pattern of layers. In that case, more preferably, the pattern for the bulk type semiconductor device is a pattern for partially removing the element isolation insulator deposited so as to be embedded in the trench when the element isolation insulating layer is formed by etching around the trench. And the conversion step adds a pattern of openings to the pattern for removing the element isolation insulator around the trench of the bulk semiconductor device so that the well contact region is also etched. And a step of generating a pattern for forming an impurity region for connecting a substrate contact of the SOI type semiconductor device on the semiconductor substrate.

[0011] In such an SOI type semiconductor device design method, a layout pattern for a bulk type semiconductor device can be easily converted into a layout pattern for an SOI type semiconductor device with only a slight modification of the pattern of the element isolation insulating layer. . If there is no step of removing the element isolation insulating film around the trench, a layout pattern dedicated to the substrate contact is required separately from this.

[0012] In addition, in the manufacturing method of the SOI type semiconductor device described above, it is necessary to correct the photomask in one step (element isolation step), and if necessary, a new photomask is added in one step (substrate contact region forming step). Is required. Thus, the change from the well contact to the substrate contact is very easy.

[0013] An SOI type semiconductor device according to a third aspect of the present invention is for achieving the second object described above, and an element is formed on an SOI semiconductor layer formed on a semiconductor substrate with a buried insulating film interposed therebetween. An SOI type semiconductor device in which a chip integrated with a semiconductor chip is fixed on a die pad of a lead frame in a state where the semiconductor substrate is electrically connected to the die pad, and an element formed in the SOI semiconductor layer and its wiring have the same function. By forming the pattern for the bulk type semiconductor device having the island-shaped SOI semiconductor layer portion surrounded by the element isolation insulating layer at a location corresponding to the well contact region of the bulk type semiconductor device. Then, the island-shaped SOI semiconductor layer portion is connected to a wiring for supplying a ground potential or a power supply voltage to the element, so that the wiring, bonding pad, It is electrically

connected to the die pad via the Ya.

[0014] In this SOI type semiconductor device, the layout pattern at the time of forming the elements and wirings is the same as that of the bulk type semiconductor device. Therefore, in the bulk type, an isolated SOI semiconductor layer portion is necessarily formed at a position corresponding to the well contact region. However, this part is not used for the substrate contact. The substrate contact is achieved by electrically connecting the semiconductor substrate to a wiring for supplying a ground potential or a power supply voltage to the transistor via a bonding pad, a wire, and a die pad of a lead frame.

[0015] DESCRIPTION OF THE PREFERRED EMBODIMENTS [First Embodiment] A first embodiment of the present invention will be described below with reference to the drawings, taking as an example a CMOS logic LSI having an SOI type substrate separation structure. FIG. 1 and FIG. 2 are an inverter and a NAND gate showing examples of gate circuits in a CMOS logic LSI. In each figure, (A) shows each gate circuit symbol, and (B) is a pattern plan view of each gate circuit in this embodiment adopting an SOI type substrate separation structure.

[0016] The pattern of the inverter 1 shown in FIG. 1B includes a region (PMOS region) 2 where a P-type MOS transistor and a region (NMOS region) 3 where an N-type MOS transistor is formed. It is divided roughly into. An N-type active layer 21 made of a semiconductor doped with an N-type impurity is formed in the PMOS region 2, and a P-type active layer 31 made of a semiconductor doped with a P-type impurity is formed in the NMOS region 3. Has been. The periphery of these active layers 21 and 31 is surrounded by the element isolation insulating layer 4 to achieve isolation between elements.

[0017] A gate electrode 5 to which an input signal of the inverter is applied is overlaid on these active layers 21 and 31. The gate electrode 5 is made of doped polycrystalline silicon to which an impurity is added, for example, and impurities of different conductivity types are arranged as necessary. In general, in order to make each MOS transistor a buried channel type and to be strong against a fine shape effect such as a short channel effect, a P-type impurity is present in the gate electrode portion on the PMOS side, and an N-type impurity is present in the gate electrode portion on the NMOS side. Is added. P-type impurities are implanted into the surface of the N-type active layer 21 using the gate electrode 5 as a mask, thereby forming a source impurity region S2 and a drain impurity region D2. Similarly, N-type impurities are implanted into the surface of the P-type active layer 31 using the gate electrode 5 as a mask, thereby forming a source impurity region S3 and a drain impurity region D3. A gate contact GC that constitutes an input terminal of the inverter is provided at the center of the gate electrode 5.

[0018] The source impurity region S2 of the PMOS transistor is electrically connected to the supply line (VDD line) 6 of the power supply voltage Vdd made of the upper metal layer via the source contact SCp on the PMOS transistor. The drain impurity region D2 of the PMOS transistor is electrically connected to the drain impurity region D3 of the NMOS transistor via the drain contact DCp, the internal connection line 7 made of an upper metal layer, and the drain contact DCn. Further, the source impurity region S3 of the NMOS transistor is connected to a power supply voltage GND supply line (GND line) 8 made of an upper metal layer through a source contact SCn thereon.

[0019] In the pattern of the NAND gate 10 according to this embodiment shown in FIG. 2B, two PMOS transistors are arranged in parallel in the N-type active layer 21. The source impurity regions S2a and S2b of the two PMOS transistors are electrically connected to the upper VDD line 6 via source contacts SCa and SCb, respectively. The common drain-in impurity region D2 between the two PMOS transistors is electrically connected to the output line 9 made of the upper metal layer via the drain contact DCp.

[0020] On the other hand, two NMOS transistors are arranged in parallel in the P-type active layer 31. The two NMOS transistors are electrically connected in series, and are inserted between the output line 9 and the GND line. That is, the drain impurity region D3 of one NMOS transistor is connected to the output line 9 via the drain contact DCn, and the source impurity region S3 of the other NMOS transistor is connected to the GND line 8 via the source contact SCn. Since the common source / drain region SD between the two NMOS transistors is not connected to the other, it is in a floating state when both transistors are off.

[0021] The gate electrode 4a to which the first input signal is applied from the gate contact GCa is disposed on the left side of the figure, and the gate electrode 4b to which the second input signal is applied from the gate contact GCb is disposed on the left side of the figure. The gate electrode intersects the N-type active layer 21 and the P-type active layer 31.

[0022] The gate circuit configured in this way has an SOI type configuration. FIG. 3 shows a cross-sectional structure of an inverter as a representative. This figure is a schematic cross-sectional view along the line BB in FIG. In this embodiment, a buried insulating film 11 made of silicon dioxide or the like is formed on a semiconductor substrate 10 made of an N-type silicon wafer or the like, and a silicon layer (hereinafter referred to as an SOI semiconductor layer) having an SOI type substrate isolation structure formed thereon. The N-type active layer 21, the P-type active layer 31, and the element isolation insulating layer 4 described above are formed in 12. Further, source impurity regions S2 and S3 (and drain impurity regions D2 and D3) are formed on the surface portion in the N-type active layer 21.

[0023] An interlayer insulating film 13 made of, for example, silicon dioxide is deposited on the entire surface of the SOI semiconductor layer 12. Plugs made of metal, doped polycrystalline silicon, or the like are embedded in the interlayer insulating film 13, thereby forming the source contacts SCp and SCn. The source contact SCp is connected to the source impurity region S2 on the PMOS side, and the source contact SCn is connected to the source impurity region S3 on the NMOS side. On the interlayer insulating film 13, the VCC line 6 connected to the source contact SCp and the GND line 8 connected to the source contact SCn are formed. These wirings 6 and 8 are made of a metal layer such as aluminum.

[0024] By the way, in an SOI type semiconductor device, there may be a case where a substrate contact for fixing a semiconductor substrate in potential with a constant voltage is required. An SOI-type MOS transistor may be used when an SOI semiconductor layer is used with a potential fixed, or may be used while a potential is floating. If the thickness of the so-called SOI semiconductor layer is reduced to about 50 nm, the SOI semiconductor layer is completely depleted in the thickness direction during operation, resulting in a fully depleted device. In this case, in order to suppress fluctuations in threshold value, substrate bias and It is often performed to fix the semiconductor substrate in potential with the same idea. Even when the SOI semiconductor layer is relatively thick and partially depleted, it is possible to fix the potential of the SOI semiconductor layer only in a circuit portion critical to threshold fluctuations and use the other SOI semiconductor layers in a floating state. Many. This is because the number of contacts to the SOI semiconductor layer is reduced as much as possible to suppress an increase in area. Even in this case, a substrate bias is often applied with the intention of suppressing threshold fluctuation as much as possible or reducing leakage at the interface between the SOI semiconductor layer and the buried insulating film.

[0025] This embodiment corresponds to the case where the substrate bias is applied without fixing the potential of the SOI semiconductor layer, and the ground potential VGND is applied to the semiconductor substrate 10. Therefore, it is necessary to short-circuit the semiconductor substrate 10 with the GND line 8. Specifically, as shown in FIG. 3, the element isolation insulating layer 4 and a portion of the buried insulating film 11 therebelow are opened, and the upper GND is placed in the interlayer insulating film 13 buried therein. A substrate contact VSC made of a plug reaching the line 8 is formed. An N-type contact impurity region 14 having a higher concentration than the substrate bulk is formed on the surface portion in the semiconductor substrate 10 provided with the substrate contact VSC. The reason why the element isolation insulating layer 4 and a part of the buried insulating film 11 therebelow are opened is to form the contact impurity region 14. This formation is desirably performed simultaneously with the source impurity region S3 (and the drain impurity region D3) of the NMOS transistor. In this sense, the semiconductor substrate 10 of this embodiment is an N type.

[0026] When this part is seen in the plan view of FIG. 1 (A), at the branch branch point extending from the backbone of the GND line 8 arranged in the lateral direction so as to be shared with the adjacent gate circuit (not shown) to the NMOS side. A substrate contact VSC is provided, and a large contact impurity region 14 is formed around the substrate contact VSC.

[0027] On the other hand, also in the VDD line 6, a contact VDC is formed at a branch branch point extending from the trunk to the PMOS side. However, as shown in FIG. 3, the contact VDC is connected via a contact impurity region 16 to an active layer 15 surrounded by the element isolation insulating layer 4 and in a potential floating state. These contact VDC, active layer 15 and contact impurity region 16 are unnecessary in terms of circuit function, and are inevitably formed by sharing a pattern with the bulk type semiconductor device of the comparative example, as will be described later. It is a part that ends up.

[0028] In the case where it is desired to shift the circuit configuration and the threshold as a whole, the substrate bias can be performed by applying the power supply voltage Vdd. In that case, the pattern is changed so that the element isolation insulating layer 4 is formed also in this portion so that the contact VDC reaches the

semiconductor substrate 10. The contact impurity region 16 is preferably formed simultaneously with the P-type impurity region (source impurity region S2 and drain impurity region D2) of the PMOS transistor.

[0029] Next, a comparative example of a bulk structure inverter will be described in comparison with such an SOI structure inverter.

[0030] FIG. 1C is a pattern plan view of a bulk type inverter in which the same function is formed in a semiconductor bulk or well as a comparative example. FIG. 4 is a schematic sectional view taken along the line CC of FIG. The plane pattern of the bulk type inverter 100 is almost the same as the plane pattern of the SOI type inverter described above. A slightly different point is that an active layer (well) is exposed at a position where the SOI type substrate contact VSC is provided, and a well contact impurity region 101 is formed on the surface portion thereof. In the illustrated example, the pattern of the well contact impurity region 101 is the same as the pattern of the substrate contact VSC in the SOI type. The other patterns are the same as those of the bulk type, and unless otherwise specified, in FIG. 1C, the same reference numerals as those in FIG.

[0031] In the cross section of FIG. 4, the substrate structure is different from the SOI type. An N-type well 103 serving as an active layer of a PMOS transistor and a P-type well 104 serving as an active layer of an NMOS transistor are formed on a semiconductor substrate 102 made of a silicon wafer of any conductivity type. The surface portions in and around the wells are separated by the element isolation insulating layer 4.

[0032] Source impurity regions S2, S3 (and drain impurity regions D2, D3) are formed in the same pattern as the SOI type on the surface portion in the N-type well 103 and the surface portion in the P-well 104. A well contact portion is provided in each of the N well 103 and the P well 104 in a state separated from the impurity regions of these transistors by the element isolation insulating layer 4. The well contact portion of the N well 103 is an N-type contact impurity region 16 provided on the inner surface of the well, and a plug connecting the upper surface of the contact impurity region 16 and the upper VDD line 6. It consists of a well contact NWC. The N well contact NWC corresponds to the SOI type contact VDC, and is embedded in the interlayer insulating film 13.

[0033] Similarly, the well contact portion of the P well 4 is a plug provided on the inner surface of the well for connecting the higher concentration N-type contact impurity region 101, the upper surface of the contact impurity region 101, and the upper GND line 8. And a P-well contact NWC. The P well contact PWC is provided in place of the SOI type substrate contact VSC, and is buried in the interlayer insulating film 13.

[0034] Other configurations, that is, the gate electrode 4, the gate contact GC, the source contacts SCp and SCn, the drain contacts DCp and DCn, the interlayer insulating film 13, the VDD line 6 and the GND line 8 are made of the same pattern and material as the SOI type described above. .

[0035] Such a difference in pattern and structure is the same in the NAND gate circuit. The description is abbreviate | omitted with the same code | symbol.

[0036] When a new SOI type semiconductor device having the same function is newly designed using the existing pattern and layout data of the bulk type semiconductor device having such a configuration, a part of the pattern of the element isolation insulating film 4 is first modified. Specifically, in the case of the illustrated inverter, for example, the opening of the pattern of the element isolation insulating film 4 is eliminated for the P-well contact on the NMOS side.

[0037] In addition, a pattern for partially opening the element isolation insulating layer 4 and the buried insulating film 11 thereunder is required for the substrate contact. As will be described later, if a process for selectively etching the insulating film deposited on the entire surface when the element isolation insulating layer 4 is formed on the active layer is necessary, the pattern at the time of the selective etching is changed. It can be dealt with by correcting. In that case, no photomask is added. On the other hand, when such a selective etching process is not originally performed, a new photomask is added for the substrate contact.

[0038] In this way, conversion from bulk type to SOI type can be performed by performing pattern correction twice or by adding one pattern layer for making a new additional photomask. In addition, these pattern corrections and creation of new patterns are simple and simple by adding at least one simple rectangular pattern. Therefore, there is an advantage that the cost associated with the change of the substrate separation structure can be suppressed as much as possible. In addition, since there is no change in the effective element pattern, it is possible to easily estimate the effect of improving characteristics due to the change from the bulk type to the

SOI type. This is because there is no change in the element characteristic parameter depending on the planar pattern shape, and the improvement of the characteristic due to the change of the substrate separation structure is reflected in the electric characteristic of the element as it is.

[0039] Finally, an embodiment of the method for manufacturing the SOI type semiconductor device will be described by taking an inverter as an example. 5 to 11 are cross-sectional views in the middle of manufacturing this inverter. First, a substrate having an SOI type substrate separation structure (SOI substrate) is formed by a known method. For example, in the method of laminating the substrates, a buried insulating film 11 is formed on the surface of a first silicon wafer (substrate to be polished) to be the SOI semiconductor layer 12, and further, for example, polycrystalline silicon or the like is formed on the surface as necessary. An adhesive layer is formed, and the surface of the adhesive layer is polished and planarized. The substrate to be polished is bonded to the second silicon wafer (support substrate) 10 from the flattened surface and annealed to improve the adhesive strength. When the surface of the substrate to be polished is ground and thinned to a certain extent, it is thinned to a predetermined thickness, for example, about 100 nm by chemical mechanical polishing (CMP). Thereby, the SOI semiconductor layer 12 is formed. A stopper 17 made of a material having a high etching selectivity with respect to the element isolation insulating material is formed on the surface of the SOI semiconductor layer 12. As the film material of the stopper, when the element isolation insulating material is silicon dioxide, for example, silicon nitride can be selected. FIG. 5 is a cross-sectional view after the stopper is formed. Note that the SOI substrate may be formed by a so-called SIMOX method.

[0040] A resist pattern is formed on the stopper film 17 using a photomask of an element isolation pattern whose design has been partially changed, and the stopper 17 and the SOI semiconductor layer 12 therebelow are etched by RIE or the like using this as a mask. As a result, as shown in FIG. 6, the SOI semiconductor layer 12 is divided by the trench, and an active layer having a predetermined pattern is formed.

[0041] As shown in FIG. 7, a film 4a of element isolation insulating material is deposited so as to cover the active layer and completely fill the trench.

[0042] Next, the insulating film 4a is polished and flattened. Before that, a resist R1 having a pattern opening above each active layer is formed on the insulating film 4a as shown in FIG. The resist R1 is partially opened at portions other than the active layer in order to form a substrate contact region. The photomask used for the pattern formation of the resist R1 is prepared in advance using pattern data obtained by partially correcting an existing bulk type pattern. Etching is performed using the resist R1 as a mask to pattern the insulating film 4a. In the etching at this time, the surface of the active layer is protected by the presence of the stopper 17. This etching is performed until the buried insulating film portion under the substrate contact region is further etched and the semiconductor substrate 10 is exposed.

[0043] After removing the resist R1, the surface of the insulating film 4a is planarized by CMP or the like. If the stopper 17 is formed of a material having high hardness, the surface of the active layer is protected by the stopper 17 even in this CMP, and the end point of the CMP can be easily detected. As a result, the insulating film 4a is separated at a necessary portion, and as a result, the element isolation insulating layer 4 is formed.

[0044] The stopper 17 is removed by chemical treatment. Before or after removing the stopper, N-type impurity ions and P-type impurity ions are divided into the active layer to form the N-type active layers 21 and 15 on the PMOS side, and the P-type active layer 31 is formed on the NMOS side. To do. Further, if necessary, the threshold value is adjusted by introducing a P-type or N-type impurity into the surface of the active layer. Thereafter, a gate insulating film (not shown) made of silicon dioxide or the like and a polycrystalline silicon film are sequentially formed and patterned to form the gate electrode 5. Since the polycrystalline silicon film at this time has not yet been doped with impurities, its conductivity is low. Further, since the gate oxide film is formed by thermally oxidizing the surface of the active layer, it is hardly formed between the gate electrode 5 on the element isolation insulating layer 4 as shown in FIG.

[0045] As shown in FIG. 11, resist R2 opening in the NMOS formation region 3 is formed, and using this as a mask, low concentration ion implantation for LDD or ions for Extentio S / D having a higher concentration than LDD in order to reduce parasitic resistance. Implantation is performed, and N-type impurities are introduced into the exposed surface portion of the active layer. Thereby, pocket ion implantation is performed as necessary. In this ion implantation, for example, the total dose is 1 × 10 14 / cm 2, the energy is 1 keV, and phosphorus ions P or BF 2 ions are implanted at an implantation angle of 15 °. Further, ion implantation is performed by dividing the wafer into eight directions from eight directions. Although not particularly illustrated, a 10 nm TEOS film, a silicon nitride film, etc. are CVD-etched and etched back to form sidewall spacers. Using this

sidewall spacer as a mask, an N-type impurity (for example, arsenic As) is ion-implanted at a relatively high dose of about 3 × 10 15 / cm 2. As a result, the source impurity region S3 (and the drain impurity region D3) is formed on the surface portion in the P-type active layer 31, and at the same time, the substrate contact impurity region 14 is formed in the opening of the semiconductor substrate 10. Further, this NMOS gate electrode portion is made N-type conductive.

[0046] Although not particularly shown, a resist opening on the PMOS side is formed in the same manner, and ion implantation of P-type impurities for LDD or Extension S / D, formation of sidewall spacers, and ion implantation for S / D are performed. In this S / D ion implantation, for example, boron BF2 is ion-implanted at a high dose of about 3 × 10 15 / cm 2. Thereby, a source impurity region S2 (and a drain impurity region D2) is formed on the surface portion in the N-type active layer 21. In addition, the PMOS gate electrode portion is made P-type conductive.

[0047] Thereafter, an interlayer insulating film 13 is deposited on the entire surface, and this is opened, and a metal material such as tungsten W or doped polycrystalline silicon or the like is buried in the opening to flatten the surface, thereby various contacts SCn, SCp. , VSC, VDC, etc. Further, various wirings 6 and 8 made of a metal material or the like are formed.

[0048] As a modification of this embodiment, the portion of the buried insulating film 11 opened in the trench may be removed by etching following the formation of the element isolation trench (FIG. 6). In this case, it is not necessary to etch the buried insulating film 11 when forming a substrate contact region (to be described later) (FIG. 8), so that the etching amount above the active layer can be made substantially the same, which is desirable. In this case, the etching stopper 17 can be omitted on condition that low damage etching is performed.

[0049] [Second Embodiment] In this embodiment, the substrate contact is taken from the back surface of the chip. FIG. 12 is a view when the SOI type semiconductor chip described in the first embodiment is fixed to a lead frame. An SOI type semiconductor chip is fixed to a die pad of a lead frame 40 made of a metal material having a high conductivity via a conductive adhesive layer 41 such as an Ag paste, and the back surface of the semiconductor substrate 10 is connected to the lead frame 40 with a low resistance. Conducted at. A lead frame 40 and a bonding pad 43 formed on the surface of the semiconductor chip and electrically connected to the GND line 8 are bonded by a wire 41. Such a die-bonded lead frame is accommodated in a mold resin or other package. At this time, the lead is pulled out of the package, but the lead to which the ground potential VGND is applied is usually a part of the illustrated lead frame 40 having a die pad, so that the ground potential VGND is the lead frame 40, the wire 41, and the bonding. It is supplied to the element through the pad 43, the GND line 8, the source contact SCn, and the like. At the same time, the ground potential VGND is supplied to the semiconductor substrate 10 via the lead frame 40 and the conductive adhesive layer 41.

[0050] In the above embodiment, the substrate contact inside the chip is unnecessary, and as shown in the figure, the contact VCS is connected only to the active layer surrounded by the element isolation insulating layer 4 and reaches the semiconductor substrate 10. Absent. Therefore, in the manufacture of such a chip, there is no need to change the pattern, and there is an advantage that the photomask used for the bulk type manufacturing can be used as it is.

[0051] The manufacturing method and design method of an SOI type semiconductor device according to the present invention are used in a bulk type semiconductor device when the SOI semiconductor layer is floating and the substrate potential is fixed. It is possible to easily manufacture the SOI type semiconductor device by converting the layout pattern to the layout pattern of the SOI type semiconductor device with a minimum change and forming a photomask with the converted pattern. According to the SOI semiconductor device of the present invention, it is possible to make substrate contact by directly applying the element and wiring layout pattern used in the bulk type semiconductor device.

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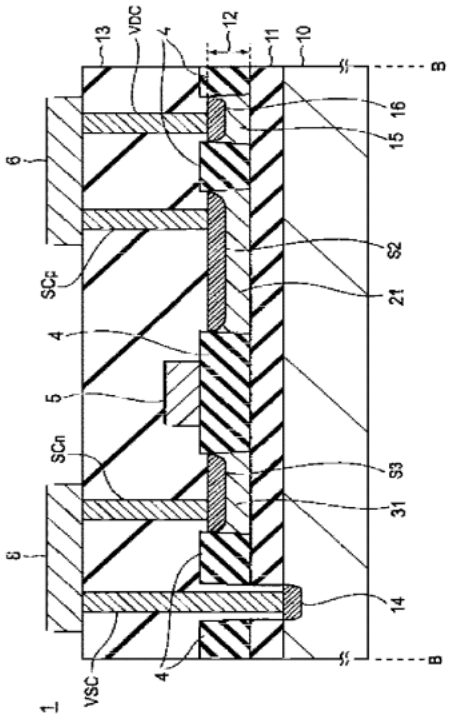
(54)【発明の名称】　ＳＯＩ型半導体装置の製造方法、設計方法およびＳＯＩ型半導体装置

(57)【要約】
【課題】　バルク型半導体装置に用いられていたレイアウトパターンを必要最小限の変更でＳＯＩ型半導体装置のレイアウトパターンに変換して用いる。
【解決手段】　ＳＯＩ型半導体装置の製造方法であって、バルク型半導体装置のウェルコンタクト領域に相当する箇所にも素子分離絶縁層４が形成されるように、バルク型半導体装置パターンを修正してフォトマスクを形成する工程と、このフォトマスクを用いてＳＯＩ半導体層１２内に素子分離絶縁層４、活性層１５，３１，３２を形成する工程と、バルク型半導体装置のウェルコンタクト領域に相当する箇所の素子分離絶縁層４およびその下の埋込絶縁膜１１をエッチングして基板コンタクト領域を形成する工程と、バルク型半導体装置のウェルコンタクトのフォトマスクを流用して、基板コンタクト領域内に基板コンタクト用のプラグＶＳＣを形成する工程とを含む。



【特許請求の範囲】
【請求項１】半導体基板上に埋込絶縁膜を介在させて形成されたＳＯＩ半導体層に素子が集積されたＳＯＩ型半導体装置の製造方法であって、
半導体基板に形成されたウェルに素子が集積されたバルク型半導体装置のウェルコンタクト領域に相当する箇所にも素子分離絶縁層が形成されるように、バルク型半導体装置の素子分離絶縁層のパターンを修正してフォトマスクを形成する工程と、
形成したフォトマスクを利用して上記ＳＯＩ半導体層内に素子分離絶縁層を形成し、当該ＳＯＩ半導体層を素子が形成される複数の活性層に分割する工程と、
上記バルク型半導体装置のウェルコンタクト領域に相当する箇所の上記素子分離絶縁層およびその下の上記埋込絶縁膜をエッチングして基板コンタクト領域を形成する工程と、
上記バルク型半導体装置のウェルコンタクトのフォトマスクを流用して、上記基板コンタクト領域内に基板コンタクト用のプラグを形成する工程とを含むＳＯＩ型半導体装置の製造方法。
【請求項２】上記活性層に絶縁ゲートトランジスタのソースまたはドレインとなるソース・ドレイン不純物領域を形成する工程を更に有し、
当該ソース・ドレイン不純物領域の形成と同時に、同じ不純物を上記基板コンタクト領域から注入し、基板コンタクト接続用の不純物領域を上記半導体基板に形成する請求項１に記載のＳＯＩ型半導体装置の製造方法。
【請求項３】上記活性層に絶縁ゲートトランジスタのソースまたはドレインとなるソース・ドレイン不純物領域を形成する工程と、
当該ソース・ドレイン不純物領域上に接続した電圧供給用のプラグを形成する工程と、
当該電圧供給用のプラグ上に接続した電圧供給配線層を形成する工程とを更に有し、
上記基板コンタクト用のプラグを形成する工程では、上記バルク型半導体装置のウェルコンタクトとソース・ドレイン不純物領域への電圧供給用のコンタクトとを同時に形成するためのフォトマスクを流用したコンタクト開口を行い、上記基板コンタクト用のプラグを上記電圧供給用のプラグと同時に形成する請求項１記載のＳＯＩ型半導体装置の製造方法。
【請求項４】上記素子分離絶縁層の形成工程が、
素子分離絶縁層を形成する領域の周囲にマスク層を形成する工程と、
マスク層を用いたエッチングにより上記ＳＯＩ半導体層に上記埋込絶縁膜に達するトレンチを形成する工程と、
トレンチ内を埋め込む素子分離絶縁膜を全面に堆積する工程と、
トレンチ周囲の素子絶縁膜を一部除去する工程とを有し、
上記基板コンタクト領域の形成工程を、トレンチ周囲の素子分離絶縁膜の除去工程と同時に行う請求項１記載のＳＯＩ型半導体装置の製造方法。
【請求項５】上記トレンチ形成時のマスク層に、上記素子分離絶縁膜に対しエッチング選択比が高い材料からなるストッパ膜を含み、
上記基板コンタクト領域の形成工程では、ストッパ膜により活性層の半導体表面を保護しながら、基板コンタクトを行う半導体基板の表面部分を露出させる請求項４記載のＳＯＩ型半導体装置の製造方法。
【請求項６】上記トレンチ形成後に、当該トレンチ形成に用いた上記マスク層をそのまま利用したエッチングにより、トレンチ内に表出した上記埋込絶縁膜部分を除去する工程を更に有した請求項４記載のＳＯＩ型半導体装置の製造方法。
【請求項７】半導体基板に形成されたウェルに素子が集積されたバルク型半導体装置用のパターンを、基板上に埋込絶縁膜を介在させて形成されたＳＯＩ半導体層に素子が集積されたＳＯＩ型半導体装置用のパターンに変換する工程を含むＳＯＩ型半導体装置の設計方法であって、
上記バルク型半導体装置がウェルコンタクトを有する場合に、上記変換工程では、当該ウェルコンタクトのパターンを、そのまま上記ＳＯＩ型半導体装置の半導体基板に達する基板コンタクトのパターンに流用するＳＯＩ型半導体装置の設計方法。
【請求項８】上記バルク型およびＳＯＩ型の半導体装置は、導電型が異なる２種類のウェルまたはＳＯＩ半導体層からなる活性層のそれぞれに活性層導電型とは逆のチャネル導電型を有した絶縁ゲートトランジスタが形成された相補型絶縁ゲートトランジスタ回路を有し、
上記バルク型半導体装置のＰ型ウェルがウェルコンタクトを有する場合に、上記変換工程では、当該Ｐ型ウェルのウェルコンタクトのパターンを、そのまま上記ＳＯＩ型半導体装置の半導体基板に達し接地電圧を供給するための基板コンタクトのパターンに流用する請求項７記載のＳＯＩ型半導体装置の設計方法。
【請求項９】上記バルク型およびＳＯＩ型の半導体装置は、導電型が異なる２種類のウェルまたはＳＯＩ半導体層からなる活性層のそれぞれに活性層導電型とは逆のチャネル導電型を有した絶縁ゲートトランジスタが形成された相補型絶縁ゲートトランジスタ回路を有し、
上記バルク型半導体装置のＮ型ウェルがウェルコンタクトを有する場合に、上記変換工程では、当該Ｎ型ウェルのウェルコンタクトのパターンを、そのまま上記ＳＯＩ型半導体装置の半導体基板に達し電源電圧を供給するための基板コンタクトのパターンに流用する請求項７記載のＳＯＩ型半導体装置の設計方法。
【請求項１０】上記変換工程が、
上記バルク型半導体装置の素子分離絶縁層のパターン

を、そのウェルコンタクト領域が素子分離絶縁層となるように一部修正して、上記ＳＯＩ型半導体装置の素子分離絶縁層のパターンを生成する工程を含む請求項７記載のＳＯＩ型半導体装置の設計方法。

【請求項１１】上記バルク型半導体装置用のパターンが、

素子分離絶縁層の形成時にトレンチ内に埋め込むように堆積された素子分離絶縁物をトレンチ周囲でエッチングにより一部除去するためのパターンを有し、

上記変換工程が、

上記バルク型半導体装置のトレンチ周囲の素子分離絶縁物を除去するためのパターンに、そのウェルコンタクト領域でもエッチングがされるように開口部のパターンを付加することにより、上記ＳＯＩ型半導体装置の基板コンタクト接続用の不純物領域を上記半導体基板に形成するためのパターンを生成する工程を更に含む請求項１０記載のＳＯＩ型半導体装置の設計方法。

【請求項１２】半導体基板上に埋込絶縁膜を介在させて形成されたＳＯＩ半導体層に素子が集積されたチップがリードフレームのダイパッド上に、その半導体基板がダイパッドと導通した状態で固着されたＳＯＩ型半導体装置であって、

ＳＯＩ半導体層に形成する素子とその配線とを、同じ機能を有するバルク型半導体装置用のパターンを流用して形成することにより、バルク型半導体装置のウェルコンタクト領域に相当した箇所に、周囲を素子分離絶縁層に囲まれた島状のＳＯＩ半導体層部分を有し、

当該島状のＳＯＩ半導層部分が、上記素子に接地電圧V_{GND}または電源電圧を供給する配線に対し接続されることにより、当該配線、ボンディングパッド、ワイヤを介して上記ダイパッドと電気的に接続されたＳＯＩ型半導体装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体基板に対し埋込絶縁膜を介在させて形成されたＳＯＩ半導体層を有したＳＯＩ型半導体装置の製造方法、設計方法およびＳＯＩ型半導体装置に関する。

【０００２】

【従来の技術】ＳＯＩ(Silicon On Insulator)構造によって基板との、あるいは素子間同士の完全分離が容易となり各種寄生容量が低下するほか、ソフトエラーやＣＭＯＳトランジスタ回路に特有なラッチアップの抑制が可能になる。このため、いわゆるＳＯＩ型のＣＭＯＳ・ＬＳＩの高速化、低電圧化および信頼性の向上に、ＳＯＩ分離技術が果たす役割がますます重要になってきている。

【０００３】これに対し、現在でも多くのＣＭＯＳ・ＬＳＩでは、半導体基板（半導体バルク）にＰ型およびＮ型のウェルを形成し、Ｐ型ウェルにＮ型チャネルのＮＭＯＳトランジスタを形成し、Ｎ型ウェルにＰ型チャネルのＰＭＯＳトランジスタを形成した、いわゆるバルク型半導体装置となっている。

【０００４】

【発明が解決しようとする課題】ところが、ＳＯＩ型半導体装置を設計する場合、同じ機能を有したバルク型半導体装置とは異なった基板構造を有しているため、既に設計済みのバルク型半導体装置のレイアウトパターンをそのまま適用することができない。したがって、多くの場合、ＳＯＩ型半導体装置用として新たにパターン設計をやり直す必要があった。これは、バルク半導体装置ではウェル電位を固定する電極が必要であり、その一方、ＳＯＩ型半導体装置ではＳＯＩ半導体層をフローティングにして用いる場合、電位を固定する場合、あるいは半導体基板電位を固定する場合など、様々な電位固定方法が存在することが主な理由の一つであった。

【０００５】本発明の第１の目的は、たとえばＳＯＩ半導体層をフローティングとし基板電位を固定して使用するような場合に好適で、バルク型半導体装置に用いられていたレイアウトパターンを最小限の変更でＳＯＩ型半導体装置のレイアウトパターンに変換する設計方法と、その方法を用いてフォトマスクを形成する工程を含むＳＯＩ型半導体装置の製造方法とを提供することにある。本発明の第２の目的は、バルク形半導体装置に用いられていた素子および配線のレイアウトパターンをそのまま適用しても基板コンタクトが可能な構造のＳＯＩ型半導体装置を提供することにある。

【０００６】

【課題を解決するための手段】本発明の第１の観点にかかるＳＯＩ型半導体装置の製造方法は、上記第１の目的を達成するためのものであり、半導体基板上に埋込絶縁膜を介在させて形成されたＳＯＩ半導体層に素子が集積されたＳＯＩ型半導体装置の製造方法であって、半導体基板に形成されたウェルに素子が集積されたバルク型半導体装置のウェルコンタクト領域に相当する箇所にも素子分離絶縁層が形成されるように、バルク型半導体装置の素子分離絶縁層のパターンを修正してフォトマスクを形成する工程と、形成したフォトマスクを利用して上記ＳＯＩ半導体層内に素子分離絶縁層を形成し、当該ＳＯＩ半導体層を素子が形成される複数の活性層に分割する工程と、上記バルク型半導体装置のウェルコンタクト領域に相当する箇所の上記素子分離絶縁層およびその下の上記埋込絶縁膜をエッチングして基板コンタクト領域を形成する工程と、上記バルク型半導体装置のウェルコンタクトのフォトマスクを流用して、上記基板コンタクト領域内に基板コンタクト用のプラグを形成する工程とを含む。

【０００７】好適に、上記活性層に絶縁ゲートトランジスタのソースまたはドレインとなるソース・ドレイン不純物領域を形成する工程を更に有し、当該ソース・ドレ

イン不純物領域の形成と同時に、同じ不純物を上記基板コンタクト領域から注入し、基板コンタクト接続用の不純物領域を上記半導体基板に形成する。あるいは、好適に、上記活性層に絶縁ゲートトランジスタのソースまたはドレインとなるソース・ドレイン不純物領域を形成する工程と、当該ソース・ドレイン不純物領域上に接続した電圧供給用のプラグを形成する工程と、当該電圧供給用のプラグ上に接続した電圧供給配線層を形成する工程とを更に有し、上記基板コンタクト用のプラグを形成する工程では、上記バルク型半導体装置のウェルコンタクトとソース・ドレイン不純物領域への電圧供給用のコンタクトとを同時に形成するためのフォトマスクを流用したコンタクト開口を行い、上記基板コンタクト用のプラグを上記電圧供給用のプラグと同時に形成する。

【０００８】好適に、上記素子分離絶縁層の形成工程が、素子分離絶縁層を形成する領域の周囲にマスク層を形成する工程と、マスク層を用いたエッチングにより上記ＳＯＩ半導体層に上記埋込絶縁膜に達するトレンチを形成する工程と、トレンチ内を埋め込む素子分離絶縁膜を全面に堆積する工程と、トレンチ周囲の素子絶縁膜を一部除去する工程とを有し、上記基板コンタクト領域の形成工程を、トレンチ周囲の素子分離絶縁膜の除去工程と同時に行う。その場合、上記トレンチ形成時のマスク層に、上記素子分離絶縁膜に対しエッチング選択比が高い材料からなるストッパ膜を含み、上記基板コンタクト領域の形成工程では、ストッパ膜により活性層の半導体表面を保護しながら、基板コンタクトを行う半導体基板の表面部分を露出させるとよい。あるいは、上記トレンチ形成後に、当該トレンチ形成に用いた上記マスク層をそのまま利用したエッチングにより、トレンチ内に表出した上記埋込絶縁膜部分を除去する工程を更に有していてもよい。

【０００９】本発明の第２の観点にかかるＳＯＩ型半導体装置の設計方法は、前記した第１の目的を達成するためのものであり、半導体基板に形成されたウェルに素子が集積されたバルク型半導体装置用のパターンを、基板上に埋込絶縁膜を介在させて形成されたＳＯＩ半導体層に素子が集積されたＳＯＩ型半導体装置用のパターンに変換する工程を含むＳＯＩ型半導体装置の設計方法であって、上記バルク型半導体装置がウェルコンタクトを有する場合に、上記変換工程では、当該ウェルコンタクトのパターンを、そのまま上記ＳＯＩ型半導体装置の半導体基板に達する基板コンタクトのパターンに流用する。

【００１０】好適に、上記変換工程が、上記バルク型半導体装置の素子分離絶縁層のパターンを、そのウェルコンタクト領域が素子分離絶縁層となるように一部修正して、上記ＳＯＩ型半導体装置の素子分離絶縁層のパターンを生成する工程を含む。その場合、更に好適に、上記バルク型半導体装置用のパターンが、素子分離絶縁層の形成時にトレンチ内に埋め込むように堆積された素子分離絶縁物をトレンチ周囲でエッチングにより一部除去するためのパターンを有し、上記変換工程が、上記バルク型半導体装置のトレンチ周囲の素子分離絶縁物を除去するためのパターンに、そのウェルコンタクト領域でもエッチングがされるように開口部のパターンを付加することにより、上記ＳＯＩ型半導体装置の基板コンタクト接続用の不純物領域を上記半導体基板に形成するためのパターンを生成する工程を更に含む。

【００１１】このようなＳＯＩ形半導体装置の設計方法では、最低でも素子分離絶縁層のパターンを少しだけ修正するだけで、バルク型半導体装置用のレイアウトパターンをＳＯＩ型半導体装置用のレイアウトパターンに容易に変換できる。なお、素子分離絶縁膜をトレンチの周囲で除去する工程がない場合は、これとは別に、基板コンタクト専用のレイアウトパターンが必要となる。

【００１２】また、前記したＳＯＩ型半導体装置の製造方法では、１工程（素子分離工程）でフォトマスクの修正が必要となり、必要に応じて、更に１工程（基板コンタクト領域の形成工程）で新たなフォトマスクが必要となる。このようにウェルコンタクトから基板コンタクトへの変更が極めて容易である。

【００１３】本発明の第３の観点に係るＳＯＩ型半導体装置は、前記した第２の目的を達成するためのものであり、半導体基板上に埋込絶縁膜を介在させて形成されたＳＯＩ半導体層に素子が集積されたチップがリードフレームのダイパッド上に、その半導体基板がダイパッドと導通した状態で固着されたＳＯＩ型半導体装置であって、ＳＯＩ半導体層に形成する素子とその配線とを、同じ機能を有するバルク型半導体装置用のパターンを流用して形成することにより、バルク型半導体装置のウェルコンタクト領域に相当した箇所に、周囲を素子分離絶縁層に囲まれた島状のＳＯＩ半導体層部分を有し、当該島状のＳＯＩ半導層部分が、上記素子に接地電位または電源電圧を供給する配線に対し接続されることにより、当該配線、ボンディングパッド、ワイヤを介して上記ダイパッドと電気的に接続されている。

【００１４】このＳＯＩ型半導体装置では、その素子および配線の形成時のレイアウトパターンをバルク型半導体装置と同じとしているため、バルク型ではウェルコンタクト領域に相当する箇所に孤立したＳＯＩ半導体層部分が必然的に形成されるが、この部分は基板コンタクトに使用されていない。基板コンタクトは、ボンディングパッド、ワイヤ、リードフレームのダイパッドを介して、半導体基板が、接地電位または電源電圧等をトランジスタに供給する配線に電気的に接続されていることにより達成されている。

【００１５】

【発明の実施の形態】［第１実施形態］以下、本発明の第１の実施形態を、ＳＯＩ形基板分離構造を有したＣＭＯＳ・ロジックＬＳＩを例に図面を参照しながら説明す

る。図１と図２は、ＣＭＯＳ・ロジックＬＳＩ内のゲート回路例を示すインバータとＮＡＮＤゲートである。各図において、（Ａ）は各ゲート回路記号を示し、（Ｂ）はＳＯＩ形基板分離構造を採用した本実施形態における各ゲート回路のパターン平面図である。

【００１６】図１（Ｂ）に示すインバータ１のパターンは、それを構成するＰ型のＭＯＳトランジスタが形成される領域（ＰＭＯＳ領域）２と、Ｎ型のＭＯＳトランジスタが形成される領域（ＮＭＯＳ領域）３とに大別される。ＰＭＯＳ領域２には、Ｎ型の不純物が導入された半導体からなるＮ型活性層２１が形成され、ＮＭＯＳ領域３には、Ｐ型の不純物が導入された半導体からなるＰ型活性層３１が形成されている。これらの活性層２１，３１の周囲は素子分離絶縁層４に囲まれ、素子間の分離が達成されている。

【００１７】これらの活性層２１，３１に対して、インバータの入力信号が印加されるゲート電極５が重ねられている。ゲート電極５は、たとえば不純物が添加されたドープド多結晶珪素からなり、必要に応じて異なる導電型の不純物が打ち分けられている。一般的には、各ＭＯＳトランジスタを埋め込みチャネル型として短チャネル効果等の微細形状効果に対し強くするために、ＰＭＯＳ側のゲート電極部分にＰ型不純物が、ＮＭＯＳ側のゲート電極部分にＮ型不純物が添加されている。ゲート電極５をマスクにしてＮ型活性層２１の表面にＰ型不純物が注入され、これによりソース不純物領域Ｓ２とドレイン不純物領域Ｄ２が形成されている。同様に、ゲート電極５をマスクにしてＰ型活性層３１の表面にＮ型不純物が注入され、これによりソース不純物領域Ｓ３とドレイン不純物領域Ｄ３が形成されている。ゲート電極５の中央部にはインバータの入力端子を構成するゲートコンタクトＧＣが設けられている。

【００１８】ＰＭＯＳトランジスタのソース不純物領域Ｓ２は、その上のソースコンタクトＳＣｐを介して、上層のメタル層からなる電源電圧Ｖｄｄの供給線（ＶＤＤ線）６に電気的に接続されている。ＰＭＯＳトランジスタのドレイン不純物領域Ｄ２は、ドレインコンタクトＤＣｐ、上層のメタル層からなる内部接続線７、およびドレインコンタクトＤＣｎを介して、ＮＭＯＳトランジスタのドレイン不純物領域Ｄ３に電気的に接続されている。さらに、ＮＭＯＳトランジスタのソース不純物領域Ｓ３は、その上のソースコンタクトＳＣｎを介して、上層のメタル層からなる電源電圧ＧＮＤの供給線（ＧＮＤ線）８に接続されている。

【００１９】図２（Ｂ）に示す本実施形態に係るＮＡＮＤゲート１０のパターンでは、Ｎ型活性層２１に２つのＰＭＯＳトランジスタが並列に配置されている。２つのＰＭＯＳトランジスタの各ソース不純物領域Ｓ２ａ，Ｓ２ｂは、それぞれソースコンタクトＳＣａ，ＳＣｂを介して上層のＶＤＤ線６に電気的に接続されている。２つのＰＭＯＳトランジスタの間の共通なドレンイン不純物領域Ｄ２は、ドレインコンタクトＤＣｐを介して上層のメタル層からなる出力線９に電気的に接続されている。

【００２０】一方、Ｐ型活性層３１に２つのＮＭＯＳトランジスタが並列に配置されている。この２つのＮＭＯＳトランジスタは電気的には直列接続され、前記した出力線９とＧＮＤ線との間に挿入されている。つまり、一方のＮＭＯＳトランジスタのドレイン不純物領域Ｄ３がドレインコンタクトＤＣｎを介して出力線９に接続され、他方のＮＭＯＳトランジスタのソース不純物領域Ｓ３がソースコンタクトＳＣｎを介してＧＮＤ線８に接続されている。２つのＮＭＯＳトランジスタ間の共通なソース・ドレイン領域ＳＤは、他に接続されていないので、両トランジスタがオフのときはフローティング状態となる。

【００２１】ゲートコンタクトＧＣａから第１の入力信号が印加されるゲート電極４ａが図の左側に配置され、ゲートコンタクトＧＣｂから第２の入力信号が印加されるゲート電極４ｂが図の左側に配置され、それぞれのゲート電極がＮ型活性層２１とＰ型活性層３１に交差している。

【００２２】このように構成されたゲート回路は、ＳＯＩ型の構成を有している。図３に、代表してインバータの断面構造を示す。この図は、図２（Ｂ）のＢ－Ｂ線に沿った概略断面図である。本実施形態ではＮ型シリコンウェーハなどからなる半導体基板１０に、二酸化珪素などからなる埋込絶縁膜１１が形成され、その上に形成されたＳＯＩ形基板分離構造のシリコン層（以下、ＳＯＩ半導体層という）１２に、前述したＮ型活性層２１、Ｐ型活性層３１および素子分離絶縁層４が形成されている。また、Ｎ型活性層２１内の表面部分にソース不純物領域Ｓ２，Ｓ３（及びドレイン不純物領域Ｄ２，Ｄ３）が形成されている。

【００２３】ＳＯＩ半導体層１２の表面全域には、たとえば二酸化珪素などからなる層間絶縁膜１３が堆積されている。金属またはドープド多結晶珪素などからなるプラグが層間絶縁膜１３内に埋め込まれ、これにより前記したソースコンタクトＳＣｐ，ＳＣｎが形成されている。ソースコンタクトＳＣｐはＰＭＯＳ側のソース不純物領域Ｓ２上に接続し、ソースコンタクトＳＣｎはＮＭＯＳ側のソース不純物領域Ｓ３上に接続している。層間絶縁膜１３上に、ソースコンタクトＳＣｐに接続した前記ＶＣＣ線６と、ソースコンタクトＳＣｎに接続したＧＮＤ線８が形成されている。これらの配線６，８は、アルミニウムなどのメタル層などからなる。

【００２４】ところで、ＳＯＩ型半導体装置では、半導体基板を一定の電圧で電位的に固定する基板コンタクトが必要となる場合がある。ＳＯＩ型ＭＯＳトランジスタは、ＳＯＩ半導体層を電位的に固定して使用する場合と、電位的にフローティング状態にして使用する場合が

ある。いわゆるＳＯＩ半導体層の厚さを５０ｎｍ程度まで薄くするとＳＯＩ半導体層が動作時に厚さ方向に完全に空乏化して完全空乏型の素子となるが、この場合、閾値の変動を抑えるには基板バイアスと同じ考えで半導体基板を電位的に固定しておくことが良く行われる。また、ＳＯＩ半導体層が比較的厚く部分空乏型となる場合でも、閾値変動に対しクリティカルな回路部分のみＳＯＩ半導体層を電位固定して、その他のＳＯＩ半導体層を電位的にフローティングにして用いることが多い。ＳＯＩ半導体層へのコンタクト数をできるだけ少なくして面積増大を抑制するためである。この場合でも閾値変動を極力抑制し、あるいはＳＯＩ半導体層と埋め込み絶縁膜との界面でのリークを低減する意図で、基板バイアスを印加することが良く行われる。

【００２５】本実施形態はＳＯＩ半導体層の電位固定は行わないで基板バイアスを印加する場合に対応し、半導体基板１０に接地電位V_{GND}を付与することとしている。そこで、半導体基板１０をＧＮＤ線８と短絡する必要がある。具体的には、図３に示すように、素子分離絶縁層４とその下の埋込絶縁膜１１の一部を開口して、その中に埋め込まれた層間絶縁膜１３内に、上方のＧＮＤ線８に達するプラグからなる基板コンタクトＶＳＣを形成している。基板コンタクトＶＳＣが設けられた半導体基板１０内の表面部分に、基板バルクより高濃度なＮ型のコンタクト不純物領域１４が形成されている。素子分離絶縁層４とその下の埋込絶縁膜１１の一部を開口させているのは、コンタクト不純物領域１４を形成するためである。この形成は、ＮＭＯＳトランジスタのソース不純物領域Ｓ３（およびドレイン不純物領域Ｄ３）と同時に行うことが望ましく、その意味で、本実施形態の半導体基板１０はＮ型となっている。

【００２６】この部分を図１（Ａ）の平面図で見ると、隣接する不図示のゲート回路と共有できるように横方向に配置されたＧＮＤ線８の基幹からＮＭＯＳ側に延びた枝の分岐の箇所に基板コンタクトＶＳＣを設け、その周囲に一回り大きなコンタクト不純物領域１４が形成されている。

【００２７】一方、ＶＤＤ線６においても、その基幹からＰＭＯＳ側に延びた枝の分岐の箇所にコンタクトＶＤＣが形成されている。ただし、このコンタクトＶＤＣは、図３に示すように、周囲を素子分離絶縁層４に囲まれて電位的にフローティング状態となった活性層１５にコンタクト不純物領域１６を介して接続されている。これらのコンタクトＶＤＣ，活性層１５およびコンタクト不純物領域１６は、回路機能的には不要なものであり、後述するように、比較例のバルク型半導体装置とパターンを共用したことにより必然的にできてしまう部分である。

【００２８】なお、回路の構成や閾値を全体的にシフトさせたい場合においては、基板バイアスを電源電圧Ｖｄｄの印加により行うこともできる。その場合、この部分にも素子分離絶縁層４が形成されるようにパターンを変更して、コンタクトＶＤＣが半導体基板１０に達するようにする。そして、コンタクト不純物領域１６は、ＰＭＯＳトランジスタのＰ型不純物領域（ソース不純物領域Ｓ２およびドレイン不純物領域Ｄ２）と同時に形成することが望ましい。

【００２９】つぎに、このようなＳＯＩ構造のインバータとの比較において、比較例のバルク構造のインバータを説明する。

【００３０】図１（Ｃ）は、比較例として同じ機能を半導体バルクまたはウェルに形成したバルク型インバータのパターン平面図である。図４は、図１（Ｃ）のＣ－Ｃ線に沿った概略断面図である。このバルク型インバータ１００の平面パターンは、上記したＳＯＩ型インバータの平面パターンと殆ど同じである。わずかに異なる点は、ＳＯＩ型で基板コンタクトＶＳＣが設けられた箇所に活性層（ウェル）が表出し、その表面部分にウェルコンタクト不純物領域１０１が形成されていることである。この図示例では、ウェルコンタクト不純物領域１０１のパターンは、ＳＯＩ型における基板コンタクトＶＳＣのパターンと同じとなっている。それ以外のパターンはバルク型と同じであり、以下、特に言及しない限り、図１（Ｃ）において図１（Ｂ）と同じ符号を付して、それらの説明を省略する。

【００３１】図４の断面では、その基板構造がＳＯＩ型と異なる。任意の導電型のシリコンウェーハからなる半導体基板１０２に、ＰＭＯＳトランジスタの活性層となるＮ型ウェル１０３と、ＮＭＯＳトランジスタの活性層となるＰ型ウェル１０４とが形成されている。そして、これらのウェル内およびウェル周囲の表面部分が素子分離絶縁層４により分離されている。

【００３２】Ｎ型ウェル１０３内の表面部分、Ｐウェル１０４内の表面部分に、ＳＯＩ型と同じパターンにてソース不純物領域Ｓ２，Ｓ３（およびドレイン不純物領域Ｄ２，Ｄ３）が形成されている。これらトランジスタの不純物領域とは素子分離絶縁層４により分離された状態で、Ｎウェル１０３とＰウェル１０４のそれぞれにウェルコンタクト部が設けられている。Ｎウェル１０３のウェルコンタクト部は、ウェル内表面部に設けられた、より高濃度なＮ型のコンタクト不純物領域１６と、コンタクト不純物領域１６上面と上層のＶＤＤ線６とを接続するプラグからなるＮウェルコンタクトＮＷＣとからなる。ＮウェルコンタクトＮＷＣは、ＳＯＩ型におけるコンタクトＶＤＣに該当し、層間絶縁膜１３中に埋め込んで形成されている。

【００３３】同様に、Ｐウェル４のウェルコンタクト部は、ウェル内表面部に設けられた、より高濃度なＮ型のコンタクト不純物領域１０１と、コンタクト不純物領域１０１上面と上層のＧＮＤ線８とを接続するプラグから

なるＰウェルコンタクトＮＷＣとからなる。Ｐウェルコンタクト ＰＷＣは、ＳＯＩ型における基板コンタクトＶＳＣの代わりに設けられ、層間絶縁膜１３中に埋め込んで形成されている。

【００３４】その他の構成、すなわちゲート電極４、ゲートコンタクトＧＣ、ソースコンタクトＳＣｐ，ＳＣｎ、ドレインコンタクトＤＣｐ，ＤＣｎ、層間絶縁膜１３、ＶＤＤ線６およびＧＮＤ線８は、前記したＳＯＩ型と同じパターン、材料からなる。

【００３５】このようなパターンおよび構造の相違は、ＮＡＮＤゲート回路でも同じである。同一符号をもって、その説明を省略する。

【００３６】このような構成のバルク型半導体装置の既存のパターンおよびレイアウトデータを用いて、同じ機能のＳＯＩ型半導体装置を新たに設計する場合、まず、素子分離絶縁膜４のパターンを一部修正する。具体的には、図示例のインバータの場合、たとえばＮＭＯＳ側のＰウェルコンタクトのために素子分離絶縁膜４のパターンの開口部をなくす。

【００３７】また、基板コンタクト用に素子分離絶縁層４およびその下の埋込絶縁膜１１を一部開口させるパターンが必要となる。このパターンは、後述するように素子分離絶縁層４の形成時に全面に堆積した絶縁膜を活性層上で選択的にエッチングするための工程が必要であるならば、その選択的エッチング時のパターンを修正することで対応できる。その場合、フォトマスクの追加はない。これに対し、そのような選択的エッチング工程がもともとない場合は、基板コンタクト用に新たなフォトマスクが１枚追加となる。

【００３８】このように、パターン修正を２回行うか、１回のパターン修正と、新たな追加フォトマスク作製のための１枚のパターンレイヤの追加によって、バルク型からＳＯＩ型の変換が可能となる。しかも、これらのパターン修正や新規パターンの作成は、単純な矩形パターンを最低１個付加するだけよく簡単である。したがって、基板分離構造の変更にともなう経費を極力抑制できる利点が得られる。また、実効的な素子パターンに変更がないので、バルク型からＳＯＩ型に変更したことによる特性改善の効果を容易に見積もることができる。平面パターン形状に依存した素子特性パラメータに変化がないため、純粋に基板分離構造の変更による特性の向上がそのまま素子の電気的特性に反映されるためである。

【００３９】最後に、このＳＯＩ型半導体装置の製造方法の実施形態を、インバータを例として説明する。図５～図１１は、このインバータの製造途中の断面図である。まず、ＳＯＩ型基板分離構造の基板（ＳＯＩ基板）を既知の方法によって形成する。たとえば基板張り合わせ方では、ＳＯＩ半導体層１２となる第１のシリコンウェーハ（被研磨基板）の表面に埋込絶縁膜１１を形成し、さらにその表面に必要に応じて、たとえば多結晶珪素などからなる接着層を形成し、接着層の表面を研磨して平坦化する。被研磨基板を、その平坦化した面から第２のシリコンウェーハ（支持基板）１０と張り合わせ、アニールして接着強度を向上させる。被研磨基板の裏面から研削して、ある程度まで薄くなったら化学的機械研磨（ＣＭＰ）により所定の厚さ、たとえば１００ｎｍ程度まで薄くする。これによりＳＯＩ半導体層１２が形成される。ＳＯＩ半導体層１２の表面に、素子分離絶縁材料とのエッチング選択比が高い材料のストッパ１７を形成する。ストッパの膜材料は、素子分離絶縁材料が二酸化珪素の場合、たとえば窒化珪素が選択できる。図５は、このストッパ形成後の断面図である。なお、ＳＯＩ基板を、いわゆるＳＩＭＯＸ法により形成してもよい。

【００４０】ストッパ膜１７上に、一部設計変更した素子分離パターンのフォトマスクを用いてレジストパターンを形成し、これをマスクとしてストッパ１７およびその下のＳＯＩ半導体層１２をＲＩＥ等でエッチングする。これにより、図６に示すように、ＳＯＩ半導体層１２がトレンチにより分割され、所定パターンの活性層が形成される。

【００４１】図７に示すように、活性層を覆って、かつトレンチ内を完全に埋め込むように素子分離絶縁材料の膜４ａを堆積する。

【００４２】つぎに、この絶縁膜４ａを研磨して平坦化するのであるが、その前に、図８に示すように、各活性層の上方で開口するパターンのレジストＲ１を絶縁膜４ａ上に形成する。このレジストＲ１は、さらに基板コンタクト領域を形成するために一部、活性層以外の箇所でも開口している。このレジストＲ１のパターン形成に用いるフォトマスクは、既存のバルク型のパターンを一部修正したパターンデータを用いて予め作製される。レジストＲ１をマスクとしたエッチングを行って、絶縁膜４ａをパターンニングする。このときのエッチングでは、ストッパ１７の存在により活性層表面が保護される。また、このエッチングは、基板コンタクト領域ではさらにその下の埋込絶縁膜部分がエッチングされて半導体基板１０が露出するまで行う。

【００４３】レジストＲ１を除去後、絶縁膜４ａの表面をＣＭＰなどで平坦化する。ストッパ１７を硬度が高い材料から形成しておくと、このＣＭＰにおいてもストッパ１７により活性層表面が保護され、またＣＭＰの終点検出も容易である。これにより絶縁膜４ａが必要箇所で分離され、その結果、素子分離絶縁層４が形成される。

【００４４】ストッパ１７を薬液処理で除去する。このストッパの除去前または後で、活性層にＮ型不純物イオンとＰ型不純物イオンを打ち分けて、ＰＭＯＳ側でＮ型活性層２１，１５を形成し、ＮＭＯＳ側でＰ型活性層３１を形成する。また、必要に応じて、Ｐ型またはＮ型の不純物を活性層表面部に導入して閾値の調整を行う。その後、二酸化珪素などからなるゲート絶縁膜（不図示）

および多結晶珪素膜を順次形成して、これをパターンニングしてゲート電極５を形成する。このときの多結晶珪素膜にはまだ不純物は添加されていないので導電率は低い。また、ゲート酸化膜は活性層表面を熱酸化して形成するので、図１０のように素子分離絶縁層４上のゲート電極５との間には殆ど形成されない。

【００４５】図１１に示すように、ＮＭＯＳ形成領域３で開口するレジストＲ２を形成し、これをマスクとして、ＬＤＤ用の低濃度イオン注入、あるいは寄生抵抗下げるためＬＤＤより高濃度なＥｘｔｅｎｔｉｏ　Ｓ／Ｄ用のイオン注入を行い、Ｎ型不純物を表出した活性層表面部分に導入する。これにより、また、必要に応じて、ポケットイオン注入を行う。このイオン注入は、たとえばトータルのドーズを１×１０^{14}／ｃｍ^{2}、エネルギーを１ｋｅＶで、燐イオンＰまたはBF_2イオンを注入角度１５°で注入する。また、ウェーハの８方向から８分割りにてイオン注入する。特に図示しないが、１０ｎｍのＴＥＯＳ膜、窒化珪素膜などをＣＶＤし、これをエッチバックしてサイドウォールスペーサを形成する。このサイドウォールスペーサをマスクにして、３×１０^{15}／ｃｍ^{2}程度の比較的高いドーズでＮ型不純物（たとえば、砒素Ａｓ）をイオン注入する。これにより、Ｐ型活性層３１内の表面部にソース不純物領域Ｓ３（およびドレイン不純物領域Ｄ３）が形成され、これと同時に半導体基板１０の開口部分に基板コンタクト不純物領域１４が形成される。また、このＮＭＯＳゲート電極部分がＮ型に導電化される。

【００４６】特に図示しないが、同様にしてＰＭＯＳ側で開口するレジストを形成してＬＤＤまたはＥｘｔｅｎｔｉｏｎ　Ｓ／Ｄ用のＰ型不純物のイオン注入、サイドウォールスペーサの形成、Ｓ／Ｄ用のイオン注入を行う。このＳ／Ｄ用のイオン注入では、たとえば、ホウ素BF_2を３×１０^{15}／ｃｍ^{2}程度の高ドーズでイオン注入する。これにより、Ｎ型活性層２１内の表面部にソース不純物領域Ｓ２（およびドレイン不純物領域Ｄ２）が形成される。また、このＰＭＯＳゲート電極部分がＰ型に導電化される。

【００４７】その後は、層間絶縁膜１３を全面に堆積し、これを開口して、開口部にタングステンＷ等の金属材料またはドープド多結晶珪素などを埋め込んで表面を平坦化することにより、各種コンタクトＳＣｎ，ＳＣｐ，ＶＳＣ，ＶＤＣ等を形成する。また、金属材料などからなる各種配線６，８等を形成する。

【００４８】本実施形態の変形例として、素子分離用のトレンチ形成時（図６）に続けて、トレンチ内に開口した埋込絶縁膜１１の部分をエッチングにより除去してもよい。こうすると、後述する基板コンタクト領域の形成時（図８）に埋込絶縁膜１１をエッチングしないですむので、活性層上方とのエッチング量をほぼ同じとすることができ、望ましい。この場合、低ダメージエッチングを行うことを条件にエッチングストッパ１７の省略も可能である。

【００４９】［第２実施形態］この実施形態では、基板コンタクトをチップ裏面からとる。図１２は、第１実施形態で説明したＳＯＩ型半導体チップをリードフレームに固着させたときの図である。導電率が高い金属材料からなるリードフレーム４０のダイパッドに、ＳＯＩ型半導体チップが、たとえばＡｇペーストなどの導電性接着層４１を介して固着され、半導体基板１０の裏面が、リードフレーム４０と低抵抗で導通している。また、リードフレーム４０と、半導体チップ表面に形成されＧＮＤ線８と電気的に導通したボンディングパッド４３とがワイヤ４１によりボンディングされている。このようなダイボンド後のリードフレームはモールド樹脂、その他のパッケージ内に収容される。このときパッケージ外部にリードが引き出されるが、接地電位V_{GND}が印加されるリードは、通常、ダイパッドを有する図示のリードフレーム４０の一部であるので、接地電位V_{GND}がリードフレーム４０、ワイヤ４１、ボンディングパッド４３、ＧＮＤ線８、ソースコンタクトＳＣｎ等を介して素子に供給される。それと同時に、接地電位V_{GND}がリードフレーム４０、導電性接着層４１を介して半導体基板１０に供給される。

【００５０】上記形態では、チップ内部の基板コンタクトは不要であり、図示のように、コンタクトＶＣＳは周囲を素子分離絶縁層４に囲まれた活性層に接続されるのみで、半導体基板１０にまでは達していない。したがって、このようなチップの製造ではパターンの変更は一切不要となり、バルク型の製造に用いていたフォトマスクをそのまま流用できるという利点がある。

【００５１】

【発明の効果】本発明に係るＳＯＩ型半導体装置の製造方法および設計方法によれば、ＳＯＩ半導体層をフローティングとし基板電位を固定して使用するような場合に、バルク型半導体装置に用いられていたレイアウトパターンを最小限の変更でＳＯＩ型半導体装置のレイアウトパターンに変換し、この変換後のパターンによりフォトマスクを形成してＳＯＩ型半導体装置を容易に製造することができる。本発明に係るＳＯＩ半導体装置によれば、バルク形半導体装置に用いられていた素子および配線のレイアウトパターンをそのまま適用して基板コンタクトが可能となる。

【図面の簡単な説明】

【図１】（Ａ）は、本発明の第１実施形態に係るＣＭＯＳ・ロジックＬＳＩ内のＳＯＩ型インバータの回路記号、（Ｂ）はそのパターン平面図である。（Ｃ）は、比較例としてのバルク型インバータのパターン平面図である。

【図２】（Ａ）は、本発明の第１実施形態に係るＣＭＯＳ・ロジックＬＳＩ内のＳＯＩ型ＮＡＮＤゲートの回路

記号、（Ｂ）はそのパターン平面図である。（Ｃ）は、比較例としてのバルク型ＮＡＮＤゲートのパターン平面図である。

【図３】本発明の第１の実施形態に係るＳＯＩ型インバータにおいて、図１（Ｂ）のＢ－Ｂ線に沿った概略断面図である。

【図４】比較例のＳＯＩ型インバータにおいて、図１（Ｃ）のＣ－Ｃ線に沿った概略断面図である。

【図５】本発明の第１の実施形態に係るＳＯＩ型インバータの製造において、エッチングストッパとなる膜の形成後の断面図である。

【図６】本発明の第１の実施形態に係るＳＯＩ型インバータの製造において、トレンチ形成後の断面図である。

【図７】本発明の第１の実施形態に係るＳＯＩ型インバータの製造において、素子分離絶縁膜の堆積後の断面図である。

【図８】本発明の第１の実施形態に係るＳＯＩ型インバータの製造において、基板コンタクト領域の開口後の断面図である。

【図９】本発明の第１の実施形態に係るＳＯＩ型インバータの製造において、素子分離絶縁層の形成後の断面図である。

【図１０】本発明の第１の実施形態に係るＳＯＩ型インバータの製造において、エッチングストッパとなる膜の形成後の断面図である。

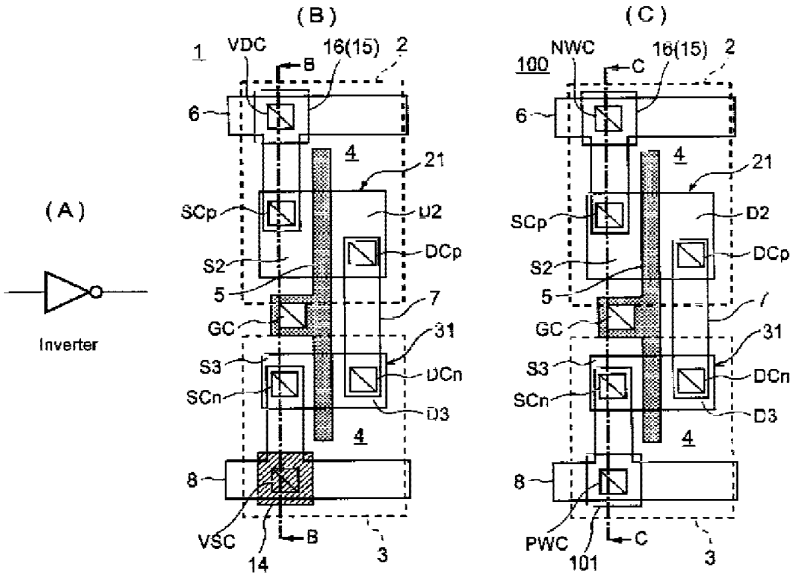
【図１１】本発明の第１の実施形態に係るＳＯＩ型インバータの製造において、基板コンタクト不純物領域形成のためのイオン注入時の断面図である。

【図１２】本発明の第２の実施形態に係るＳＯＩ型半導体装置の要部構成を示す図である。

【符号の説明】

１…ＳＯＩ型インバータ、２…ＰＭＯＳ形成領域、３…ＮＭＯＳ形成領域、４…素子分離絶縁層、４ａ…素子分離絶縁膜、５，５ａ，５ｂ…ゲート電極、６…ＶＤＤ線、７…内部接続線、８…ＧＮＤ線、９…出力線、１０，１０２…半導体基板、１１…埋込絶縁膜、１２…ＳＯＩ半導体層、１３…層間絶縁膜、１４…基板コンタクト不純物領域、１５…活性層、１６，１０１…コンタクト不純物領域、１７…エッチングストッパ、２１…Ｎ型活性層、３１…Ｐ型活性層、４０…リードフレーム、４１…導電性接着層、４２…ワイヤ、４３…ボンディングパッド、１０３…Ｎ型ウェル、１０４…Ｐ型ウェル、ＳＣｎ，ＳＣｐ…ソースコンタクト、ＤＣｎ，ＤＣｐ…ドレインコンタクト、ＧＣ，ＧＣａ，ＧＣｂ…ゲートコンタクト、ＶＳＣ，ＶＤＣ…コンタクト、Ｓ２，Ｓ２ａ，Ｓ２ｂ，Ｓ３…ソース不純物領域、Ｄ２，Ｄ３…ドレイン不純物領域、ＳＤ…ソース・ドレイン不純物領域、ＰＷＣ，ＮＷＣ…ウェルコンタクト

【図１】



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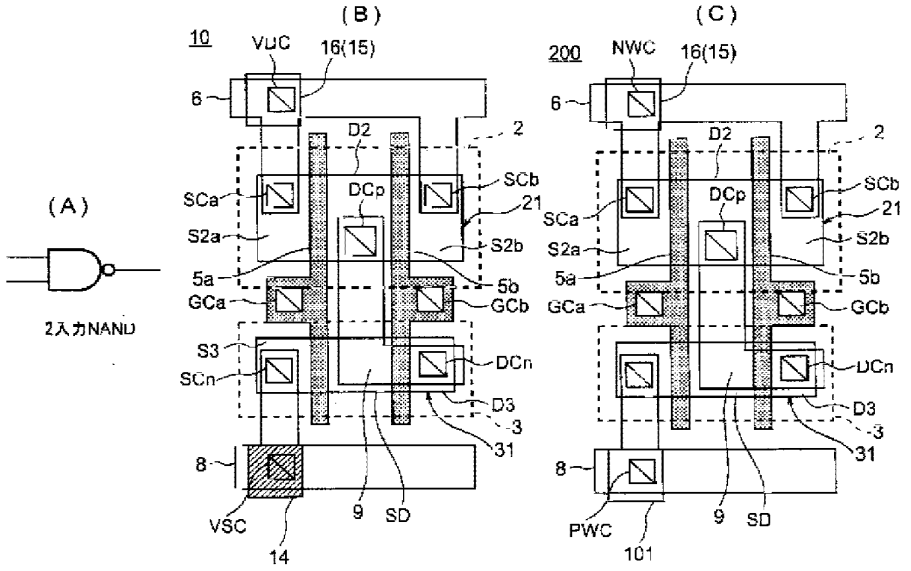
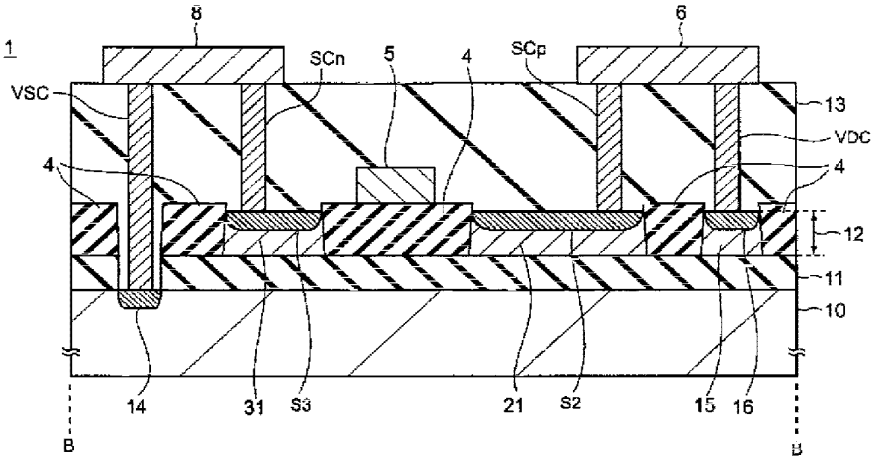
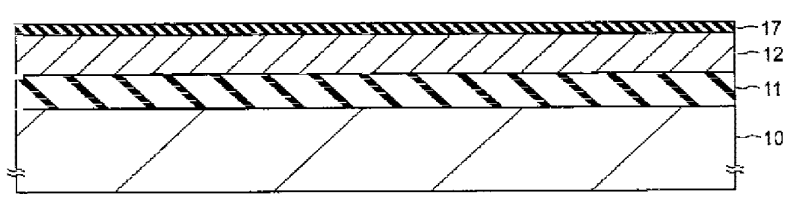

(A)
2入力NAND
(B)
10
VDC
16(15)
6
D2
2
SCa
DCp
SCb
21
S2a
S2b
5a
5b
GCa
GCb
S3
SCn
DCn
D3
3
31
8
VSC
14
9
SD
(C)
200
NWC
16(15)
6
D2
2
SCa
DCp
SCb
21
S2a
S2b
5a
5b
GCa
GCb
DCn
D3
3
31
8
PWC
101
9
SD

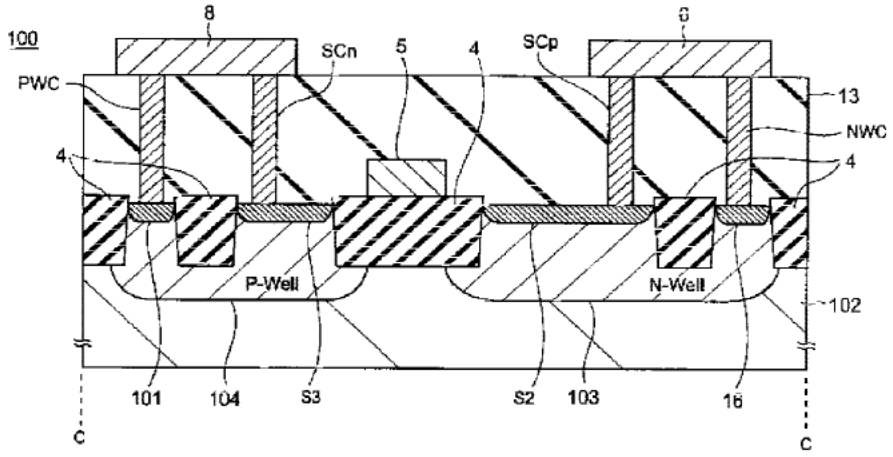
【図3】


1
8
6
VSC
SCn
5
4
SCp
13
VDC
4
4
12
11
10
14
31
S3
21
S2
15
16
B
B

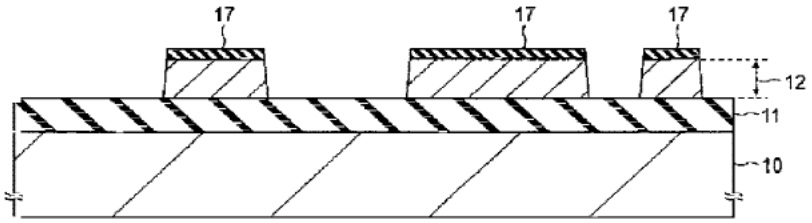
【図5】


17
12
11
10

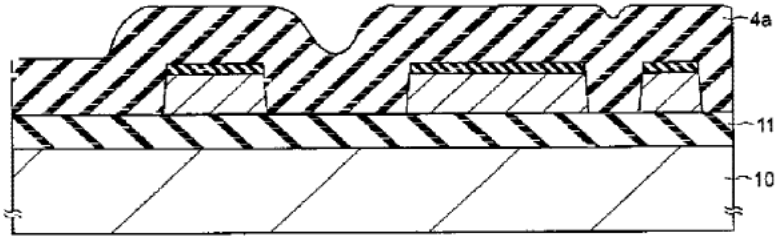
【図4】


100
8
SCn
5
4
SCp
6
PWC
13
NWC
4
4
P-Well
N-Well
102
101
104
S3
S2
103
16
C
C

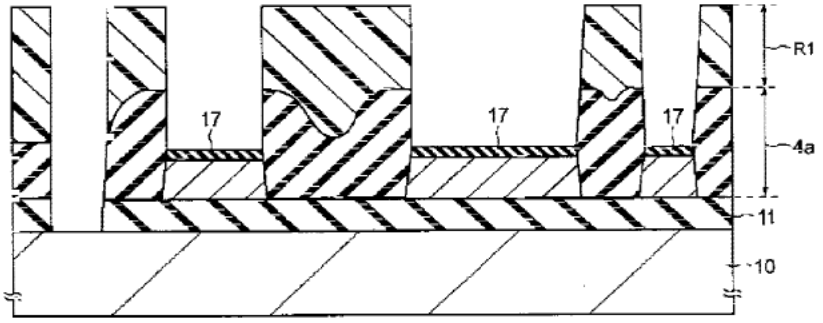
【図6】


17
17
17
12
11
10

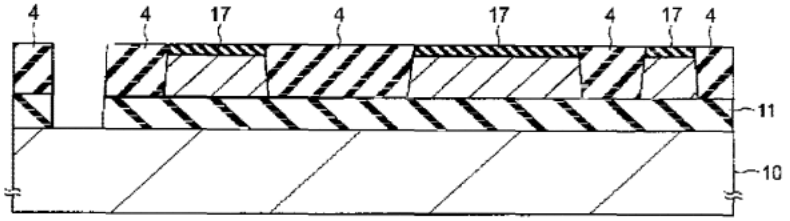
【図7】


4a
11
10

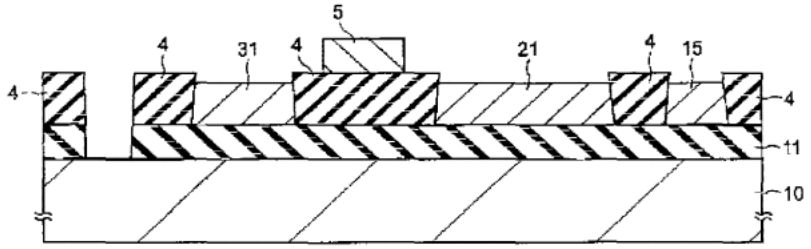
【図8】


R1
17
17
17
4a
11
10

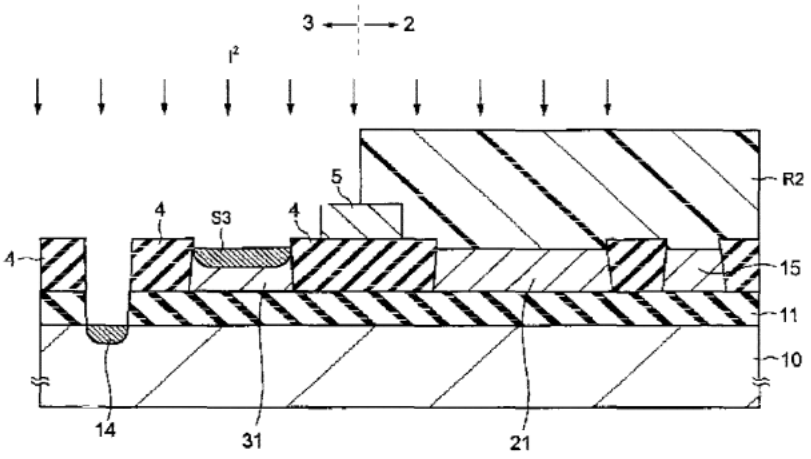
【図9】


4
4
17
4
17
4
17
4
11
10

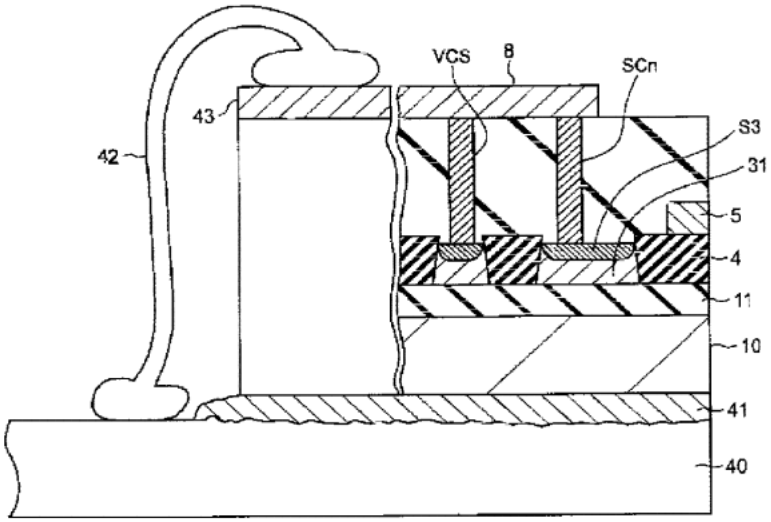
【図10】


5
4
31
4
21
4
15
4
4
11
10

【図11】


3
2
I²
5
R2
4
S3
4
4
15
11
10
14
31
21

【図12】



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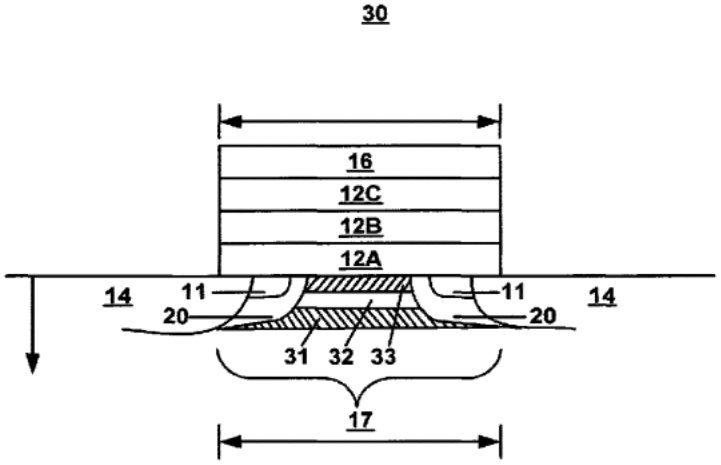

(57) Abstract: A memory semiconductor cell (30) comprises a gate region (16), a source region (14) and a drain region (14). A channel region (17) is formed between the source region (14) and the drain region (14). The channel region (17) comprises a first channel portion (33) with a first concentration of doping material, the first channel portion (33) disposed adjacent to an edge of the channel region (17) closest to and substantially parallel to the gate region (16). The channel region (17) further comprises a second channel portion (31) with a second concentration of doping material, the second channel portion (31) disposed substantially parallel to the first channel portion (33) and a third channel portion (32), disposed between the first channel portion (33) and the second channel portion (31), with a third concentration of doping material. The third concentration is lower than the first concentration and lower than the second concentration. The memory cell may be one of two general types of non-volatile memory, a floating gate cell or a nitride read only memory (NROM), whereby layer (12B) in a floating gate or a nitride layer respectively.

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RETROGRADE CHANNEL DOPING TO IMPROVE SHORT CHANNEL EFFECT

TECHNICAL FIELD

Embodiments of the present invention relate to design of sub-micron metal oxide semiconductors. More particularly, embodiments of the present invention provide retrograde channel doping to improve the short channel effect.

BACKGROUND ART

Figure 1 shows a memory cell 10 as has been well known in the conventional art. Regions 14 are the drain and/or source regions for memory cell 10. They may be used as source and/or drain interchangeably. Control gate 16 is used to control the operation of memory cell 10. A channel region 17 is formed between source/drain regions 14. Feature size 18 is the nominal size of the smallest feature that can be created by a particular semiconductor process. In memory cells of this type, the gate 16 width and channel 17 length typically correspond approximately to feature size 18. Memory cell 10 may also have a source/drain extension 11 structure. Source/drain extension 11 is a shallow diffusion that connects the channel 17 with the deeper source/drain 14, typically intended to prevent degradation of drive current.

Memory cell 10 may be one of two general types of non-volatile memory, a "floating gate" cell or a nitride read only memory (NROM) cell. In a floating gate cell, layer 12B of the gate stack is typically conductive polysilicon. Layers 12A and 12C are insulating materials which isolate or "float" gate layer 12B, which is usually referred to as a floating gate. Floating gate 12B is the storage element of memory cell 10.

Silicon nitride based flash memory has many advantages as compared to its floating gate and tunneling oxide based counterparts. Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) is potentially very dense in terms of number of cells per unit area that can be used and it requires fewer process steps as compared to floating gate memory. Moreover, it can be easily integrated with standard SRAM process technology. A further advantage of using SONOS devices is their suitability for applications requiring large temperature variations and radiation hardening. The SONOS stack is a gate dielectric stack and consists of a single layer of polysilicon, a triple stack ONO (Oxide-Nitride-Oxide) gate dielectric layer and a MOS channel 17. The ONO structure may consist of a tunnel oxide 12A, a nitride memory storage layer 12B and a blocking oxide layer 12C.

Memory device manufacturers are continually challenged to provide ever greater amounts of memory at ever lower costs. Recently, Advanced Micro Devices, Incorporated of California has introduced MIRROR BIT ™ nitride-based flash ROM that stores multiple bits per memory cell 10 physically separated in nitride layer 12B. Such storage of multiple bits per cell increases the storage density of the memory device, thereby reducing the cost per bit of storage.

Another primary approach employed to achieve lower memory costs is the industry-wide on-going reduction in semiconductor feature size. By making features, such as signal lines and transistors smaller, more memory devices may be placed in a given die area, resulting in lower production costs.

However, as feature size decreases to, for example, about 0.3 microns and smaller, the channel length also decreases. As channel length grows shorter, threshold voltage begins to decrease and leakage current increases. These effects are commonly referred to in the semiconductor arts as the "short channel effect." An increase in leakage current is particularly onerous in flash memory devices as flash has found wide acceptance in very low power applications, for example mobile phones, due to the ability of flash to retain information without applied power. Increases in leakage current may have a significant deleterious effect on total power consumption

of the flash device and the product using the flash device. Consequently, much research and development effort has gone into mitigating the short channel effect.

Prior art approaches to improve leakage current and reduce the short channel effect include, for example, "halo" doping and retrograde wells. Halo doping 20 creates a steep dopant profile at the edges of the source/drain regions, as shown in Figure 1. A conventional retrograde well has a non-uniform doping concentration that increases, for example, linearly with depth 22 in the channel region 17. The doping of a conventional retrograde well generally follows a continuous, monotonically increasing profile with no abrupt changes. Conventional retrograde wells are typically created by using a slow diffusing dopant species such as arsenic or antimony for PMOS devices and indium for NMOS devices. Both halo doping and retrograde well profiles serve to inhibit the flow of charge carriers, raising the threshold voltage and reducing leakage current for the device.

However, both halo doping and conventional retrograde wells, alone and in combination, are found to be lacking. Such prior art approaches simply do not reduce leakage current to commercially acceptable levels for flash memory at modern process feature sizes, for example, 0.17 microns and smaller.

Semiconductor processing equipment is extremely expensive. Fundamental semiconductor processing steps, e.g., doping, typically require long periods of development and extensive qualification testing. Any solution to the short channel effect should be compatible with existing semiconductor processes and equipment without the need for revamping well established tools and techniques.

Thus a need exists to prevent short channel effects in memory cells. A further need exists for preventing short channel effects in a manner that is compatible and complimentary with conventional approaches to minimize short channel effects. A still further need exists for the above mentioned needs to be achieved with existing semiconductor processes and equipment without revamping well established tools and techniques.

DISCLOSURE OF THE INVENTION

Embodiments of the present invention provide a means to prevent short channel effects in memory cells. Further embodiments of the present invention prevent short channel effects in a manner that is compatible and complimentary with existing approaches to minimize short channel effects. Still further embodiments of the present invention provide for the above mentioned solutions to be achieved with existing semiconductor processes and equipment without revamping well established tools and techniques.

A memory semiconductor cell comprises a gate region, a source region and a drain region. A channel region is formed between the source region and the drain region. The channel region comprises a first channel portion with a first concentration of doping material, the first channel portion disposed adjacent to an edge of the channel region closest to and substantially parallel to the gate region. The channel region further comprises a second channel portion with a second concentration of doping material, the second portion disposed substantially parallel to the first channel portion and a third channel portion, disposed between the first channel portion and the second channel portion, with a third concentration of doping material. The third concentration is lower than the first concentration and lower than the second concentration.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a memory cell as has been well known in the conventional art.

Figure 2 illustrates a memory cell with a retrograde channel, according to an embodiment of the present invention.

Figure 3 illustrates an exemplary profile of doping concentration in a channel region versus channel depth, according to an embodiment of the present invention.

Figures 4A, 4B and 4C illustrate a charge carrier flow through a channel region of a memory cell, according to an embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

In the following detailed description of the present invention, retrograde channel doping to improve short channel effect, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one skilled in the art that the present invention may be practiced without these specific details or with equivalents thereof. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

RETROGRADE CHANNEL DOPING TO IMPROVE SHORT CHANNEL EFFECT

Embodiments of the present invention are described in the context of design and operation of flash memory devices. However, it is appreciated that embodiments of the present invention may be utilized in other areas of electronic design and operation.

Figure 2 illustrates a memory cell 30 with a novel retrograde channel, according to an embodiment of the present invention. The channel region comprises three portions, 31, 32 and 33. Channel portion 33 is closest to gate 16 and substantially parallel to the long axis of gate 16. Channel portion 32 is substantially parallel to channel portion 33 and at a greater depth into the substrate material than channel portion 32. Channel portion 31 is substantially parallel to channel portion 32 and at a still greater depth into the substrate material. Channel portion 32 is disposed between channel portions 31 and 33. It is appreciated that memory cell 30 is shown with source/drain extensions 11 and halo implant regions 20. Embodiments of the present invention are well suited to memory cells with or without these features. If one or both were absent, channel portions 31, 32 and 33 would extend horizontally to the halo implant or the source drain extension or the source/drain.

By well known semiconductor processing techniques, for example implantation and diffusion, channel portion 33 may be constructed and given a particular concentration of doping material. Likewise, channel portion 31 may be constructed and given a particular concentration of doping material. In general, no specific operations are performed to construct channel portion 32, rather channel portion 32 is a result of constructing portions 31 and 33 with no overlap. The bottom of channel portion 31 may be, for example, 0.1 μm from the top edge of the substrate.

According to an embodiment of the present invention, the doping concentration in both channel portion 31 and channel portion 33 is higher than the doping concentration of channel portion 32. Graph 40 of Figure 3 illustrates an exemplary profile 41 of doping concentration in a channel region versus channel depth. Channel portion 33 may have a doping concentration as depicted by profile 41 in region 33A. Channel portion 32 may have a doping concentration as depicted by profile 41 in region 32A. Channel portion 31 may have a doping concentration as depicted by profile 41 in region 31A.

It is to be appreciated that, in contrast to conventional retrograde wells, the doping profile of this novel well is neither monotonic nor necessarily continuous, according to an embodiment of the present invention. There may be relatively abrupt (as allowed by semiconductor physics) changes in doping profile at the boundaries between channel portions, for example between channel portions 31 and 32, and between channel portions 32 and 33.

In channel portions 31 and 33 charge carrier migration is hindered due to the to relatively high concentration of doping material(s). Consequently, the effective channel region is reduced to approximately

channel portion 32. For example, channel portion 32 may form a "tunnel" (not to be confused with quantum effect tunneling) between channel portions 31 and 33. As a beneficial result of the reduced effective channel, threshold voltage is increased and leakage current is decreased, reducing or eliminating the short channel effect. It is to be appreciated that the depths, thickness and doping concentrations of the respective channel portions will vary according to a wide range of variables including, for example, source/drain thickness, channel length, operating voltage, doping materials and whether the device operates as a P channel or an N channel.

Channel portion 31 may be initially formed by using a slow diffusing dopant species, for example, arsenic or antimony for PMOS devices. Such a diffusion process may enable high concentrations of doping material to reach the channel depths required. Channel portion 33 may be formed by using faster diffusing dopants, e.g., boron. A shorter diffusion may produce a high concentration of doping material at relatively shallow depths in the channel region.

Figures 4A, 4B and 4C further illustrate a charge carrier flow through a channel region of memory cell 30, according to an embodiment of the present invention. In Figure 4A, charge carriers, for example, electrons 403 attempt to flow from source/drain region 401 to source/drain region 402. Electrons are impeded from flowing into channel portion 33 due to a high concentration of doping material. Likewise, electrons 405 are impeded from flowing into channel portion 31 due to a high concentration of doping material. In contrast, electrons 404 are able to overcome a relatively small energy barrier and flow into channel portion 32.

As shown in Figure 4B, electrons 403, otherwise disposed to travel horizontally (as depicted) into channel region 33, must change direction to travel around the "corner" of channel region 33 in order to enter channel region 32, wherein electrons are more able to flow. Such changes of direction require energy, resulting in a higher energy budget for electrons traversing a complex path, in contrast to electrons which may be able to travel in substantially a straight line. In addition, because region 401 is fully populated with charge carriers, e.g., electrons 404 and 405, additional energy is required to overcome the electrostatic repulsion of like charges in order to move the charge carriers closer together. As a beneficial result of the increased path length, the indirect nature of the path, as well as electrostatic repulsion, electrons 403 require more energy to travel from region 401 to 402 and consequently have a beneficially higher threshold voltage for embodiments of the present invention when compared to the prior art.

In a similar manner, electrons 405 must change direction and overcome electrostatic repulsion in order to travel into channel portion 32 from their original positions adjacent to channel portion 31. Consequently, electrons 405 have a higher threshold voltage than would otherwise be required.

Electrons 404, while disposed adjacent to channel portion 32, are also beneficially affected by embodiments of the present invention. Although electrons 404 are not obviously redirected to avoid channel portions of higher doping concentration, electrons 404 are affected by the localized increased concentration of charge carriers resulting in electrostatic forces acting upon electrons 404 in a similar manner to the electrostatic forces acting upon electrons 403 and 405.

Figure 4C shows a cumulative effect of the present retrograde channel on charge carrier flow, according to an embodiment of the present invention. Electrons in region 401 are inhibited from flowing in channel portions 33 and 31, favoring channel portion 32. However, due to the physically constrictive nature of channel portion 32 combined with electrostatic forces acting upon the like charge carriers, the electrons tend to "bunch up" at the interface between region 401 and channel portion 32. The net effect of "bunching up" is seen externally as a desirable increase in threshold voltage, and a corresponding decrease in leakage current.

It is to be appreciated that although a PMOS device has been illustrated herein, embodiments of the present invention are well suited to NMOS devices as well. The choices of materials, e.g., for dopants, for use with NMOS devices are well understood in the semiconductor arts.

This novel design and method to implement this design reduce and/or eliminate the short channel effect, allowing for decreased feature size and increased density of memory cells. These beneficial results allow for less expensive memory devices with lower power consumption, rendering a competitive advantage to the users practicing embodiments of the present invention.

Embodiments of the present invention provide a means to prevent short channel effects in memory cells. Further embodiments of the present invention prevent short channel effects in a manner that is compatible and complimentary with existing approaches to minimize short channel effects. Still further embodiments of the present invention provide for the above mentioned solutions to be achieved with existing semiconductor processes and equipment without revamping well established tools and techniques.

The preferred embodiment of the present invention retrograde channel doping to improve short channel effect is thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.

CLAIMS

What is claimed is:

1. A method of manufacturing a memory semiconductor cell (30) comprising:

forming a first channel portion (33) to produce a first concentration of doping material, said first channel portion (33) disposed adjacent to an edge of a channel region closest to and substantially parallel to a gate region (16) of said memory semiconductor cell;

forming a second channel portion (31) to produce a second concentration of doping material, said second portion (31) disposed substantially parallel to said first channel portion (33); and

forming a third channel portion (32), disposed between said first channel portion (33) and said second channel portion (31), comprising a third concentration of doping material, wherein said third concentration is lower than said first concentration and lower than said second concentration.

2. The method as described in Claim 1 further comprising implanting a halo implant (20) disposed adjacent to a source region or a drain region of said memory semiconductor cell (30).

3. The memory semiconductor cell (30) described in Claim 1 wherein a source region of said memory semiconductor cell comprises a source extension region (11).

4. The method as described in Claim 1 further comprising forming said second channel portion (31) prior to the formation of said first channel portion (33).

5. The method as described in Claim 1 wherein said memory semiconductor cell (30) is non-volatile.

6. The method as described in Claim 5 wherein said memory semiconductor cell (30) comprises a nitride layer as a storage element (12B).

7. The method as described in Claim 5 wherein said memory semiconductor cell comprises a floating gate (12B) as a storage element.

8. A memory semiconductor cell (30) comprising:

a gate region (16), a source region (14) and a drain region (14);

a channel region (17) between said source region (14) and said drain region (14);

wherein said channel region (17) comprises:

a first channel portion (33) comprising a first concentration of doping material, said first channel portion (33) disposed adjacent to an edge of said channel region (17) closest to and substantially parallel to said gate region (16);

a second channel portion (31) comprising a second concentration of doping material, said second portion (31) disposed substantially parallel to said first channel portion (33); and

a third channel portion (32), disposed between said first channel portion (33) and said second channel portion (31), comprising a third concentration of doping material, wherein said third concentration is lower than said first concentration and lower than said second concentration.

9. The memory semiconductor cell described in Claim 8 wherein said channel region (17) further comprises a halo implant (20) disposed adjacent to said source region (14) or said drain region (14).

10. The memory semiconductor cell described in Claim 8 wherein said source region (17) comprises a source extension region (11).

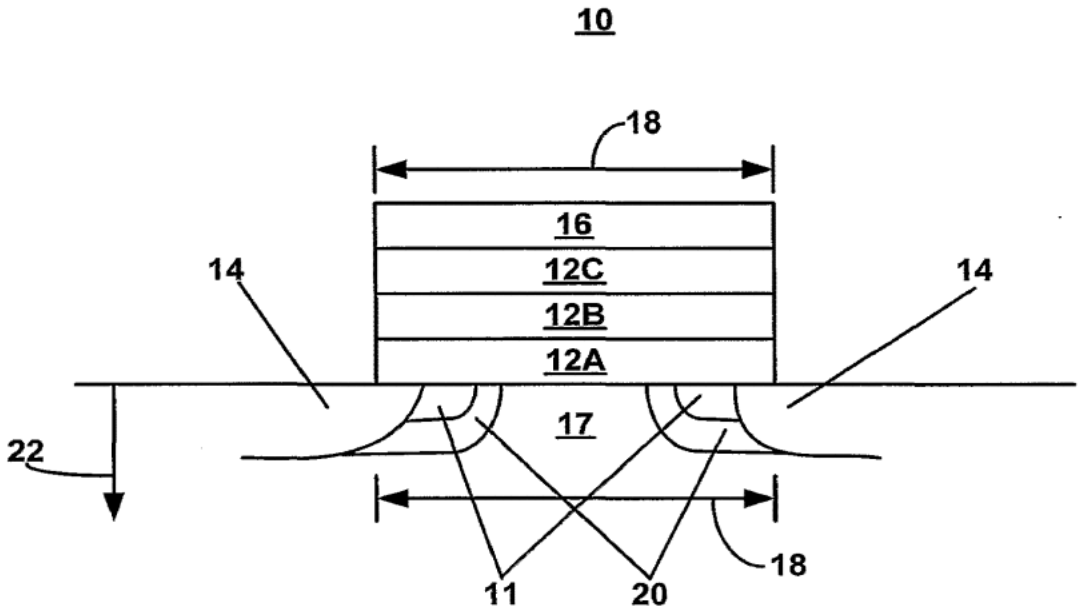

FIG. 1
(CONVENTIONAL ART)

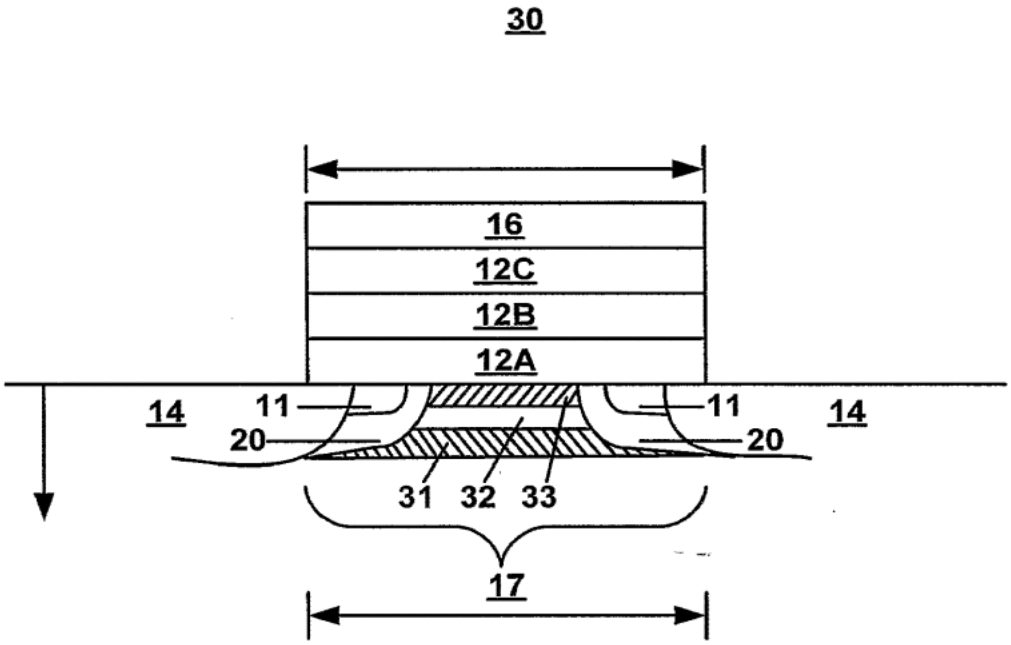

FIG. 2

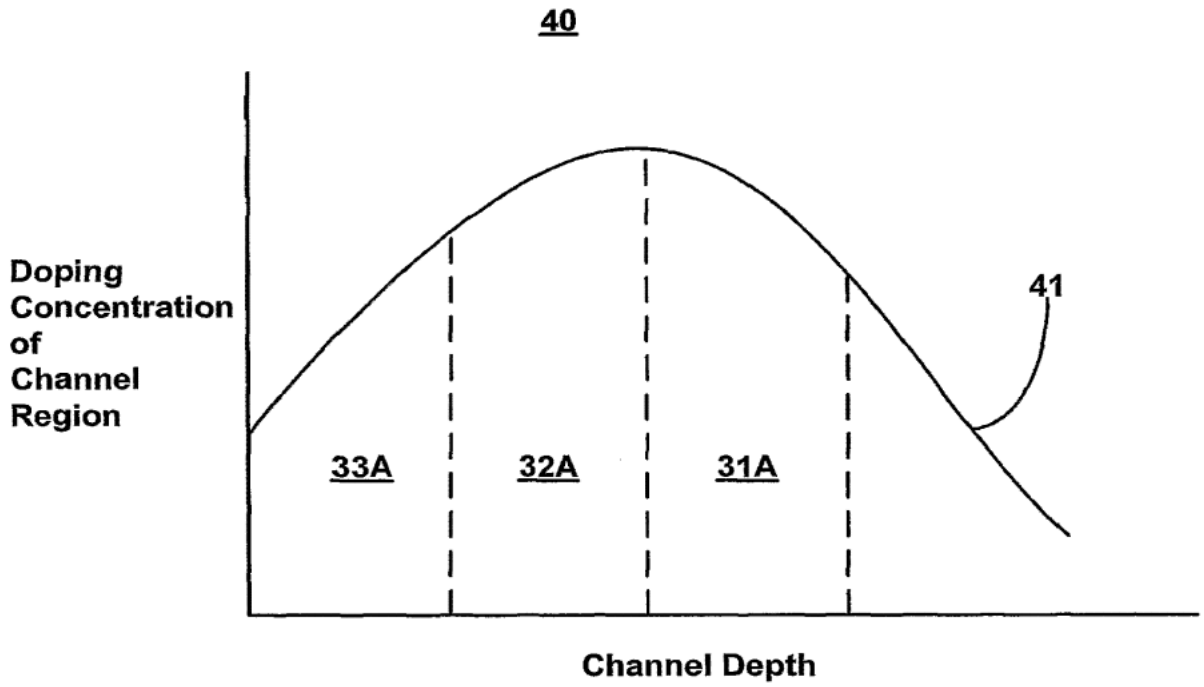
40
Doping Concentration of Channel Region
41
33A
32A
31A
Channel Depth

FIG. 3

4/4

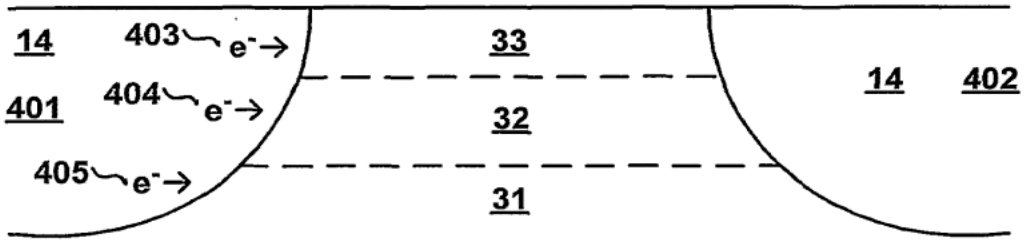

FIG. 4A

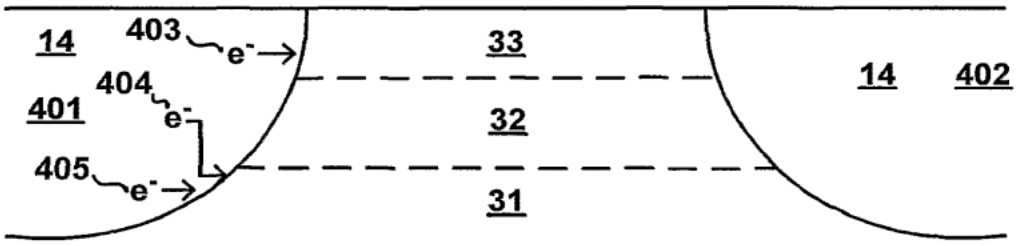

FIG. 4B

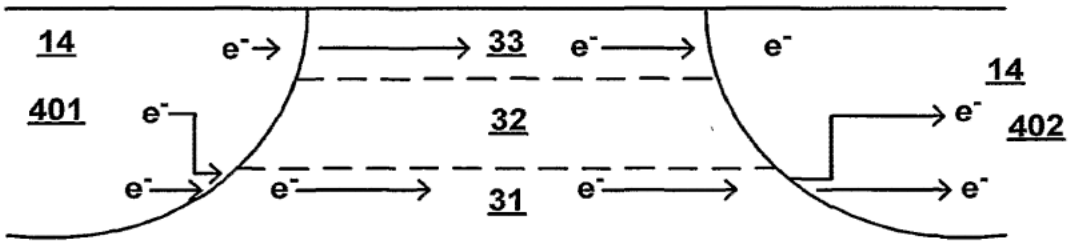

FIG. 4C

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/21682

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/788 H01L29/792 H01L21/8234 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2002/106852 A1 (CHANG CHI ET AL) 8 August 2002 (2002-08-08) paragraphs '0047!-'0055!; figures 5-8 ---	1-10
Y	US 5 923 985 A (AOKI KENJI ET AL) 13 July 1999 (1999-07-13) column 3, line 60 -column 4, line 28; figures 8A-8D,9 ---	1-10
Y	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 03, 30 March 2000 (2000-03-30) -& JP 11 354778 A (MITSUBISHI ELECTRIC CORP), 24 December 1999 (1999-12-24) abstract; figures --- -/--	1-10

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 February 2004	18/02/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Blackley, W

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/21682

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 929 486 A (KITAKADO HIDEHITO) 27 July 1999 (1999-07-27) column 5, line 55 -column 9, line 22; figures 3,5A,5B	1-10
Y	US 6 258 645 B1 (KANG WOO TAG) 10 July 2001 (2001-07-10) the whole document	1-10
Y	PATENT ABSTRACTS OF JAPAN vol. 008, no. 161 (E-257), 26 July 1984 (1984-07-26) -& JP 59 061070 A (FUJITSU KK), 7 April 1984 (1984-04-07) abstract; figures	1-10

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 03/21682

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		US 2001042889 A1	22-11-2001
JP 59061070 A	07-04-1984	NONE	

I, Michael Fletcher, declare:

1. I am well versed in both the Japanese and English languages and have over 15 years of experience translating Japanese technical documents into English.

2. The following translation of the patent document JP07-306752 to English is accurate and complete to the best of my knowledge.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and accurate.

Executed this 4th day of September 2019, at Parowan, UT

Michael Fletcher

(19) Japanese Patent Office (JP)

(12) Laid-Open Patent Application Bulletin (A)

(11) Laid-Open Patent Application No. 2003-51551

(43) Laid-Open Disclosure Date: February 21, 2003

(51) Int. Cl.[7]	ID Number	JPO File Number	FI	Theme code (ref.)		
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21/761					321B	5F048
27/08	331			21/76	J	5F140
27/092				29/78	301R	
29/78						

Request for Examination: No Number of Claims: 5 OL Total pages: 10

(21) Application No.: 2001-235765

(22) Application Date: August 3, 2001

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Continued on last page

(54) TITLE OF THE INVENTION:

Semiconductor Device Manufacturing Method and Semiconductor Device

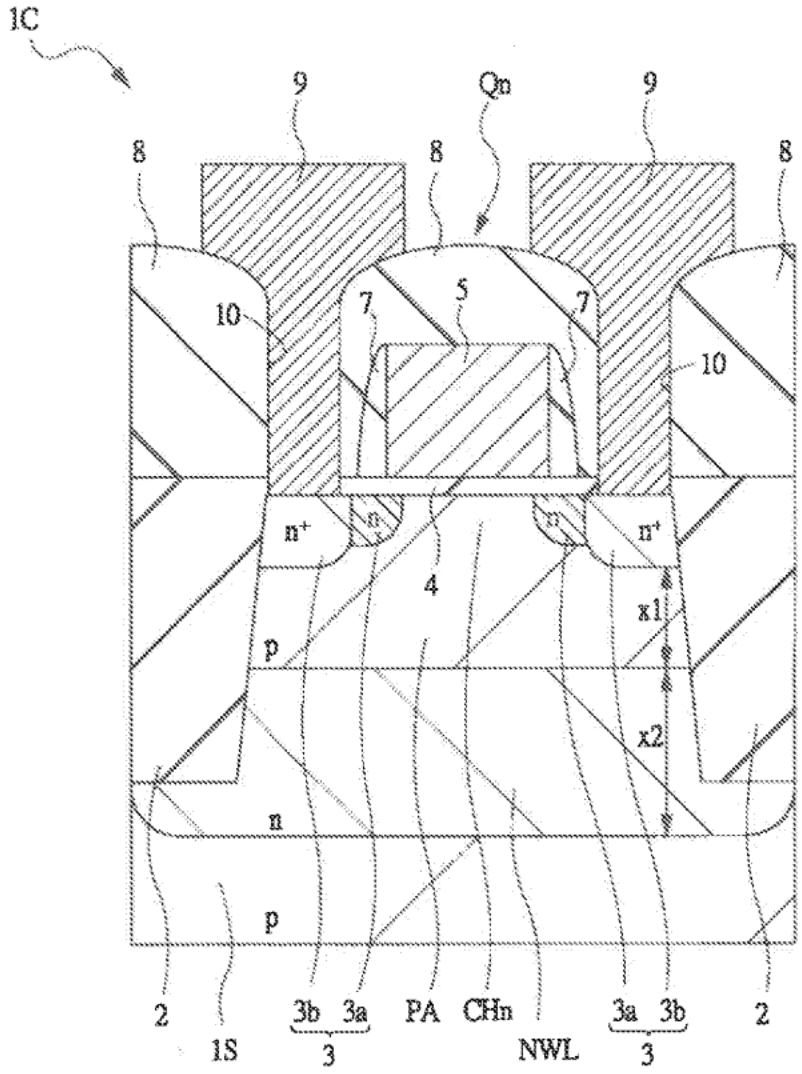
(57) ABSTRACT (Revised)

[Issue]Achieve increase in drive current through substrate floating, achieve reduction in junction capacitance, and resolve thermal insulation and crystal defects that are shortcomings of SOI substrates.

MEANS FOR SOLVING THE PROBLEM

Providing of an n (p) well NWL (PML) between the p (n) type semiconductor area PA (PN) and semiconductor substrate 1S arranged using n (p) chancel type MISFETQn (Qp) to electrically isolate the p (n) type semiconductor area PA (PN) and the semiconductor substrate 1S.

図 1



1S: Semiconductor substrate
NWL: n-Well
Qn: n-channel type MISFET
PA: p type semiconductor area

CLAIMS
[Claim 1]
A semiconductor device manufacturing method comprising the following steps:
(a) a step of through introduction of a first impurity onto a first conductivity type semiconductor substrate, forming a second conductivity type semiconductor area with the opposite conductivity type than the first conductivity type, (b) a step of through introduction of a second impurity onto said semiconductor substrate, forming a first conductivity semiconductor area formed with an impurity peak position arranged on the main surface of said semiconductor substrate at a position more shallow than the impurity peak position of the

second conductivity type semiconductor area, and (c) a step of forming a field effect transistor with a second conductivity type channel area within the first conductivity type semiconductor area.

[Claim 2]
A semiconductor device with a field effect transistor provided within a first conductivity type semiconductor area provided on a semiconductor substrate having a second conductivity type channel area with the opposite conductivity type than the first conductivity type, wherein a second conductivity type semiconductor area is provided between said semiconductor substrate and said first conductivity type semiconductor area to isolate said first conductivity type semiconductor area on which the second conductivity type channel area of said field effect transistor is formed from said semiconductor substrate.

[Claim 3]
A semiconductor device with a field effect transistor provided within a first conductivity type semiconductor area provided on a semiconductor substrate having a second conductivity type channel area with the opposite conductivity type than the first conductivity type, and a configuration where a second conductivity type semiconductor area is provided between said semiconductor substrate and said first conductivity type semiconductor area to isolate said first conductivity type semiconductor area on which the second conductivity type channel area of said field effect transistor is formed from said semiconductor substrate, wherein the thickness of said first conductivity type semiconductor area under the semiconductor area for said field effect transistor source and drain is greater than the sum of the width of the depletion layer of the junction between the semiconductor areas for source and drain for when supply voltage is applied and said first conductivity type semiconductor area and the width of the depletion layer of the junction between the first conductivity type semiconductor area and the second conductivity type semiconductor area.

[Claim 4]
A semiconductor device with a field effect transistor provided within a first conductivity type semiconductor area provided on a semiconductor substrate having a second conductivity type channel area with the opposite conductivity type than the first conductivity type and a configuration where a second conductivity type semiconductor area is provided between said semiconductor substrate and said first conductivity type semiconductor area to isolate said first conductivity type semiconductor area on which the second conductivity type channel area of said field effect transistor is formed from said semiconductor substrate, wherein the thickness of the second conductivity type semiconductor area is greater than the sum of the width of the depletion layer of the junction between the first conductivity type semiconductor area and the second conductivity type semiconductor area and the width of the depletion layer of the junction between the second conductivity type semiconductor area and the semiconductor substrate.

[Claim 5]
A semiconductor device with a first field effect transistor and a second field effect transistor on the main surface of a semiconductor substrate, wherein said first field effect transistor is provided with a first conductivity type semiconductor area provided on said semiconductor substrate, this first conductivity type semiconductor area is electrically isolated from said semiconductor substrate by a second conductivity type semiconductor area with opposite conductivity type than the first conductivity type provided between the first conductivity type semiconductor area and said semiconductor substrate and the second field effect transistor is provided within said second conductivity type semiconductor area.

DETAILED DESCRIPTION OF THE INVENTION
[0001]
TECHNOLOGICAL FIELD INVENTION BELONGS TO

The present invention is related to a semiconductor device manufacturing method and a semiconductor device and in particular related to effective technology applied to a manufacturing method for a semiconductor device with a field effect transistor as well as to semiconductor device technology.

[0002]
BACKGROUND TECHNOLOGY
The technology investigated by the inventors is a semiconductor device structure providing a field effect transistor on a, for example, partially depleted SOI (Silicon On Insulator) substrate. An SOI substrate has a structure of a thin semiconductor layer provided on a substrate insulator layer with an element such as a field effect transistor or the like formed on the primary surface of the semiconductor layer. When voltage is applied to the gate electrode of the field effect transistor of this structure, the depletion layer expands from the gate insulation film but does not reach the substrate insulator layer even at maximum depletion layer width leaving substrate area that is not depleted. This is the structure most widely used and the substrate (in other words, semiconductor layer) is electrically insulated so when conducting, the substrate potential rises and threshold voltage lowers and this results in achieving high drive current. In addition, semiconductor area for source and drain and depletion layer for joining with a channel layer extends as far as the substrate insulator layer dramatically reducing junction capacitance.

[0003]
A partially depleted SOI substrate is described in Scalability of SOI Technology into 0.13 μm 1.2V CMOS Generation, E. Leobandung, et. al, Tech Digest of IEDM98, PP403-406,1998 IBM.

[0004]
THE ISSUE(S) THAT THIS INVENTION INTENDS TO RESOLVE
However, with the semiconductor device technology that uses an SOI substrate described above, the substrate price is high price, 5 times that of a normal substrate. The structure is an element area covered with an insulator body so thermal resistance is high and this readily leads to increase in bonding temperature. Currently, crystal defects are high compared to normal substrate structures. In addition, the element area is completely isolated by the insulator leading to the problem that substrate floating control is difficult. Here, achieving the advantages of a SOI structure on a normal substrate structure in some manner is an important issue.

[0005]
An objective of the present invention is to provide technology that improves the performance of semiconductor devices.

[0006]
Furthermore, an objective of the present invention is to provide technology reducing the cost of semiconductor devices.

[0007]
This and other objects of the present invention will become clear through the description in this specification as well as the attached drawings.

[0008]
MEANS FOR SOLVING THE VARIOUS ISSUES
A simple description of a summary representing the invention disclosed in this application is provided below.

[0009]

In other words, the present invention is separation of a semiconductor substrate and a semiconductor area formed by a channel of a field effect transistor formed on the primary surface thereof using a pn junction.

[0010]
In addition, the present invention is, with a semiconductor substrate and semiconductor area having a field effect transistor formed on the main surface thereof, a semiconductor area with a conductivity type opposite that of the semiconductor area is provided therebetween to isolate the semiconductor substrate and semiconductor area.

[0011]
EMBODIMENTS OF THE INVENTION
In the following embodiments, the description is separated into a plurality of sections or embodiments as needed for convenience. However, except for when stated explicitly, these are not mutually unrelated where one is a partial or full modified example of another and are related in terms of detail and supplemental description and the like.

[0012]
In addition, in the embodiments below, when number of elements are referred to (including pieces, number amount, range and the like), it is not limited to the indicated number and can be more or less than the indicated number except where stated explicitly and when clearly limited to a specific number based on principle.

[0013]
Furthermore, in the following embodiments, it goes without saying that the structural elements (including element steps and the like) are not necessarily essential unless stated explicitly or can be considered to be clearly essential based on principle.

[0014]
In a similar manner, when structural element shape and positional relationships are referenced in the embodiments below, this includes items that are approximate or similar or the like essentially that shape or the like except when stated explicitly or can be considered that this is clearly not the case based on principle. The same goes for numerical values and range described above.

[0015]
In addition, items with the same function are given the same code in all drawings for describing the embodiments and repeated description is omitted.

[0016]
In addition, in the present embodiments, MISFET (Metal Insulator Semiconductor Field Effect Transistor) that is representative of field effect transistors is abbreviated as MIS, p channel type MISFIT is abbreviated as pMIS, and n channel type MISFET is abbreviated as nMIS.

[0017]
An embodiment of the present invention will be described in detail below based on the drawings.

[0018]
(Embodiment 1) FIG. 1 shows a cross section of the main part of the logic circuit on the semiconductor chip 1C that makes up the semiconductor device that is embodiment 1 of the present invention. In addition, FIG. 2

shows the impurity concentration distribution of the semiconductor substrate (hereafter, simply substrate) 1S that makes up the semiconductor chip 1C.

[0019]
The substrate 1S is made up of a single crystal of, for example, p type silicon (Si). A groove type partitioning part (SGI; Shallow Groove Isolation) 2 is formed on the main surface (device forming surface). The groove type partitioning part 2 is formed, for example after forming a groove for partitioning on the main surface of the substrate 1S, by depositing an insulating membrane such as a silicon oxide membrane (SiO_2) and the like on the main surface of the substrate 1S embedded within the groove, and further by polishing using CMP (Chemical Mechanical Polishing) and the like such that the insulating membrane is left only within the groove. The depth of the groove type partitioning part 2 (distance from main surface of substrate 1S to bottom surface of partition part 2) is, for example, roughly 0.2 to 0.3 μm. The area surrounded by this groove type partitioning part 2 is an active area (device forming area). With regards to this substrate 1S, a p type semiconductor area PA (first conductivity type semiconductor area) is formed in this active area. Boron (B) or Boron difluoride (BF_2), for example, is included in this p type semiconductor area PA. Here, nMISQn for a logic circuit formed inside this p type semiconductor area PA is shown as an example.

[0020]
The nMISQn comprises semiconductor areas 3, 3 for source and drain, a channel area CHn, a gate insulating film 4, and a gate electrode 5. The semiconductor areas 3, 3 for source and drain are arranged in a pair on both sides with the channel areas CHn formed in the p type semiconductor area PA interposed, each comprising an n type semiconductor area 3a arranged in the vicinity of each of the channel areas CHn and an n^+ type semiconductor area 3b arranged in a position at a distance from the channel area CHn with the n type semiconductor 3a interposed. The n type semiconductor 3a and n^+ type semiconductor area 3b both contain, for example, phosphorus (P) or arsenic (As). However, the n type semiconductor 3a is also called an extension area, of which impurity concentration is set to be lower than that of the n^+ type semiconductor area 3b. In other words, it is a LDD (Lightly Doped Drain) structure.

[0021]
In addition, with the structure of the present embodiment 1 as described below, as the p type semiconductor area PA is in a state of floating electrically, reducing the threshold voltage, the threshold voltage is set such that it is 50 mV to 100 mV higher than normal by having a comparatively high impurity concentration of the channel area CHn to prevent the threshold voltage from falling too much. Here, ions are implanted on the main surface of the substrate 1S, for example, with boron at an ion implantation energy of around 10 keV into the channel area CHn, as a way to adjust the threshold voltage.

[0022]
The gate insulating film 4 is made up of, for example, silicon oxide (SiO_2). The thickness thereof is the silicon dioxide exchange film thickness, for example, 2.5 nm or less, or roughly 1.5 nm as an example. However, materials for the gate insulating film are not limited to this, and can be changed, for example, the gate insulating film 4 can be a silicon oxynitride film (SiON). In other words, there can be a structure segregating nitrogen at the interface layer between the gate insulating film 4 and the substrate 1S. A silicon oxynitride film can suppress interface level generation in the film and has high effectiveness in decreasing electron trap compared to a silicon oxide film, such that it can improve hot carrier tolerance in the gate insulating film 4 and improve dielectric strength. In addition, it is more difficult for impurities to penetrate a silicon oxynitride membrane compared to a silicon oxide membrane; therefore, use of a silicon oxynitride membrane enables control of fluctuations in threshold voltage that can cause scattering of impurities in the gate electrode material on the substrate 1S side. In order to form a silicon oxynitride membrane, for example, the substrate 1S is subjected to heat treatment in a

nitrogen-containing gas atmosphere such as NO, NO_2, or NH_3. In addition, the effects as stated above can also be obtained by heat treating the substrate 1S in the nitrogen-containing gas atmosphere after forming a gate insulating film 4 made up of silicon oxide on the surface of the substrate 1S, and segregating the nitrogen in the interface layer between the gate insulating film 4 and the substrate 1S. In addition, the gate insulating film 4 can have a structure where a silicon nitride film is laminated on the silicon oxide film. Furthermore, the gate insulating film 4 can be formed from an insulating film made up of high dielectric films, for example, HfO_2 (dielectric constant ⍺r = 20.6), ZrO_2 (⍺r = 24.7), Al_2O_3 (⍺r = 8.4), Y_2O_3 (⍺r = 14), $HfSiO_4$, $ZrSiO_4$ (⍺r = 19.4), and the like.

[0023]
The gate electrode 5, for example, is made up of a low-resistance polycrystalline silicon. However, it is not limited to this, and various modifications are feasible, for example, it can be a so-called polymetal gate electrode structure providing a metal membrane such as tungsten and the like on a so-called polycide gate electrode structure or low-resistance polycrystalline silicon membrane through a barrier metal layer such as a tungsten nitride (WN) and the like, which provides a silicide layer such as a cobalt silicide ($CoSi_x$) on the low-resistance polycrystalline silicon membrane. A sidewall 7 made up of a silicon oxide membrane is formed to form a LDD structure on the side surface of the gate electrode 5. In addition, the gate lengths are around 0.14 μm for a gate insulating film 4 thickness of 2.5 nm, and around 0.08 μm for a gate insulating film 4 thickness of 1.5 nm. In addition, the source voltage on the high-voltage side of the logic circuit area formed on the nMISQn is, for example, around 1.5 V to 0.7 V, and is comparatively lower than the source voltage on the high-voltage side of the surrounding circuit areas. Furthermore, regarding the semiconductor chip 1C, the source voltage on the high-voltage side of the surrounding circuit areas (for example, the input circuit, output circuit, and input/output bidirectional circuit) is around 3.0 V or 3.3 V.

[0024]
This type of nMISQn is covered by an interlayer insulating membrane 8 deposited on the main surface of the substrate 1S. The interlayer insulating membrane 8 is made up of, for example, a silicon oxide membrane, and a first layer wiring 9 is formed on the surface thereof. The first layer wiring 9, is made up of, for example, aluminum or aluminum alloy, and is electrically connected to a semiconductor area 3 for source and drain through contact holes 10 that are bored in the interlayer insulating membrane 8.

[0025]
Incidentally, the present inventors found while developing a semiconductor device using a partially depleted SOI substrate, that many of the merits of using a partially depleted SOI substrate compared to use of a normal substrate were an increase in drive current due to floating of the substrate and a decrease in junction capacitance. Here, a structure such as the one that follows was used in order to achieve a structure that has these kinds of merits with a normal substrate.

[0026]
In other words, regarding the present embodiment 1, an n-well NWL (second conductive type semiconductor area) is provided between the p type semiconductor area PA where the nMISQn is formed and the lower layer substrate 1S. Regarding the depth from the main surface of the substrate 1S so that the substrate 1S and p type semiconductor area PA as well as the channel area CHn and substrate 1S are not electrically connected, the impurity distribution of the n-well NWL is formed at a position slightly more shallow than the bottom of the groove type partitioning part 2, and distributed from a position deeper than the peak position of the p type semiconductor area PA to a position slightly more shallow than the bottom of the groove type partitioning part 2. In other words, regarding the present embodiment 1, the channel areas CHn of the nMISQn, and the p type semiconductor area PA and the substrate 1S, are electrically isolated by a pn junction between the n-well NWL

and the substrate 1S. Here, with a power supply voltage applied to the semiconductor area 3 for the nMISQn source and drain, connecting of the n^+ type semiconductor area 3b and n-well NWL needs to be prevented by a depleted layer with the junction of the channel area CHn (p type semiconductor area PA) and depleted layer spreading between the channel area CHn (p type semiconductor area PA) and n-well NWL. In other words, the distance x 1 in FIG.1 needs to be larger than the sum of the widths of the depletion layers described above. In addition, the width x2 of the n-well NWL itself can not be allowed to be reduced by the depletion layer with the channel area CHn (p type semiconductor area PA) or the depletion layer with the substrate 1S. In other words, the width x2 needs to be larger than the sum of the depletion layer widths. This type of n-well NWL can be formed using ion implantation of phosphorus, for example, onto the main surface of the substrate 1S with an ion implantation energy of around 450 keV of phosphorus, for example, after the groove type partitioning part 2 is formed. Furthermore, the impurity concentration of the n-well NWL at its peak position is, for example, around $10^{18}/cm^3$ or somewhat lower, as shown in FIG. 2.

[0027]
By providing this type of n-well NWL, similar effects to those of using an SOI substrate can be obtained depending on the performance of the semiconductor device. In other words, while conducting, the threshold voltage of the nMISQn decreases and current increases, due to an increase in potential of the channel area CHn (p type semiconductor area PA) from a capacitive coupling of the gate electrode 5 and the channel area CHn (p type semiconductor area PA), and an increase in potential of the channel area CHn (p type semiconductor area PA) due to the generation of impact ionization holes from drain current flow. FIG. 3 shows the gate voltage dependence of the drain current between the nMISQn of the present embodiment 1 and the nMIS formed on a normal substrate that does not contain an n-well isolation structure. In the present embodiment 1, as the channel area CHn (p type semiconductor area PA) is electrically insulated, threshold voltage is lowered and drain current can be increased when gate voltage is applied. In addition, the junction capacitance between the semiconductor area 3 for source and drain and the substrate 1S can be decreased to 1/3 of a case where the n-well NWL is not provided, as the junction capacitance of the n^+ type semiconductor area 3b and the channel area CHn (p type semiconductor area PA), the junction capacitance of the channel area CHn (p type semiconductor area PA) and the n-well NWL, and the junction capacitance of the n-well NWL and the substrate 1S are put in a state of serial connection. Therefore, operation speeds of a circuit comprising this transistor can be increased.

[0028]
In addition, as the channel area CHn (p type semiconductor area PA) and the substrate 1S are not completely isolated by an insulator, and have a structure such that they are isolated by the n-well NWL that more readily releases heat in comparison to an SOI substrate, increase in heat resistance can be substantially reduced, suppressing an increase in junction temperature. Therefore, operation reliability of the semiconductor device can be improved. In addition, a cooling structure of the package itself, or a cooling device or cooling mechanism for cooling the semiconductor device can be simplified.

[0029]
In addition, crystal defects can be reduced in comparison to an SOI substrate. Therefore, the yield and reliability of the semiconductor device can be improved.

[0030]
In addition, an increase in substrate potential can be controlled with comparative ease by controlling the leakage current of the pn junction under the channel area CHn. In other words, the controllability of substrate floating can be improved. Therefore, this can simplify circuit design.

[0031]
In addition, providing of an n-well NWL is basically a normal substrate structure and so this enables reducing costs of the semiconductor device compared to the case of using a high cost SOI substrate.

[0032]
(Embodiment 2) Embodiment 2 is a description of applying the present invention to a semiconductor device that has a CMIS (Complementary MIS).

[0033]
FIG. 4 shows a cross section of the main part of a CMIS circuit that makes up a logic circuit on the semiconductor chip 1C that forms the semiconductor device of another embodiment of the present invention.

[0034]
As the vertical structure of the area the nMISQn is formed on is the same as that in embodiment 1, the explanation thereof is omitted. Here, a description of the vertical structure of the area pMISQp is formed on is provided. Regarding the area the pMISQp is formed on, an n type semiconductor area NA (second conductive type semiconductor area) is formed on the active area of the substrate 1S, and the pMISQp is formed within this n type semiconductor area NA. The n type semiconductor area NA, for example, contains phosphorus (P) or arsenic (As).

[0035]
The pMISQp comprises semiconductor areas 11, 11 for a source and drain, a channel area CHp, a gate insulating film 4, and a gate electrode 5. The semiconductor areas 11, 11 for source and drain are arranged as a pair with a channel area CHp interposed can comprise p type semiconductor areas 11a arranged respectively close to the channel area CHp and p^+ type semiconductor area 11b arranged at a distance from the channel area CHp with the p type semiconductor areas 11a interposed. The p type semiconductor area 11a and p^+ type semiconductor area 11b both contain, for example, boron (B) or boron difluoride (BF_2). However, the p type semiconductor area 11a can be called an extension area, of which impurity concentration is set to be lower than that of the p^+ type semiconductor area 11b. In other words, it is a LDD structure.

[0036]
In addition, regarding the present embodiment 2, a p-well PWL (first conductivity type semiconductor area) is provided between the n type semiconductor area NA where the pMISQp is formed and the substrate 1S. In other words, regarding the present embodiment 2, the channel areas CHp (n type semiconductor area NA) of the pMISQp and the substrate 1S are electrically isolated by the pn junction between the p-well PWL and the n type semiconductor area NA. As the impurity distribution forming conditions for the p-well PWL are the same as the n-well NWL, the explanation thereof is omitted. This type of p-well PWL can be formed by ion implantation on the main surface of the substrate 1S with an ion implantation energy of around 160 keV of boron, for example, after the groove type partitioning part 2 is formed. Furthermore, the impurity concentration at the peak position of the p-well PWL is around the same as the n-well NWL. The channel area CHp of the pMISQp is formed by ion implantation of phosphorus onto the main surface of the substrate 1S surface with using roughly 20 keV, for example, to reach the prescribed desired threshold (enhancement of roughly 50 mV to 100 mV compared to a conventional structure). Other items are the same as embodiment 1, and the description is omitted.

[0037]
In this manner, with embodiment 2, the following effects, other than the effects obtained in embodiment 1, can be obtained. In other words, the pMISQp achieves the same effects as the nMISQn. Therefore, the operating

speed (performance) of a semiconductor device that has a logic circuit configured with a CMIS circuit can be improved.

[0038]
(Embodiment 3) Regarding the vertical structure of the MIS in embodiments 1 and 2, operation speed can be improved as stated above, however, MIS threshold voltage fluctuates within the active area and becomes unstable. Here, regarding the present embodiment 3, MIS that use a vertical structure and those that do not, even for MIS that are formed on the same substrate 1S, were produced separately. In other words, there are different purposes, a MIS vertical structure as explained in embodiments 1 and 2 according to the electrical characteristics required by the circuit, and a normal MIS vertical structure. More specifically, the MIS vertical structure above is used for a MIS configured with a circuit in which the operations thereof are not obstructed by threshold voltage to a certain extent, and a general MIS vertical structure is used ant not the MIS vertical structure above for a MIS configured with a circuit in which operations thereof are obstructed by a fluctuating threshold voltage. For example, for a MIS that makes up a digital circuit, the MIS vertical structure as explained in embodiments 1 and 2 is used. In addition, for example, the MIS vertical structure described above were not used for MIS that make up analog circuits where, for example, high operation precision is required, input/output circuits, or memory cells or sense amp circuits of memory circuits (hereafter simply called analog circuits and the like). Here, normal MIS vertical structures were used. While a memory cell is a digital circuit, they read and write microscopic signals (charges), so threshold voltage fluctuations of the MISFET that makes up the memory cell can hinder data processing, such that use of a common MIS vertical structure is preferable. In addition, based on analysis by the present inventors, when considering from the perspective of the MIS operating voltage (source voltage on the high-voltage side), if the operating voltage is 1.5 V or less, for example, use of the MIS vertical structure as explained in embodiments 1 and 2 is preferable. On the other hand, if the operating voltage of the MIS is higher than 1.5 V, use of the common MIS vertical structure is preferable.

[0039]
FIG. 5 shows an example of a cross-section view of the main part of the semiconductor device of the present embodiment 3. An area A1 shows an arrangement area of the nMISQn that makes up a logic circuit (digital circuit) and the pMISQp (first field effect transistor). In the area A1, the MIS vertical structure as described in embodiments 1 and 2 is used.

[0040]
On the other hand, an area A2 shows an arrangement area of a nMISQn1, Qp1 (2nd field effect transistor) that makes up a circuit generating an obstruction when threshold voltage such as the analog circuit, input/output circuit, memory cells or sense circuit of a memory circuit, or the like fluctuates. In the area A2, a common MIS vertical structure is used. In other words, the nMISQn1 is formed inside of the p-well PWL, and a pMISQp1 is formed inside the n-well NWL. The structures of the p-well PWL and the n-well NWL of the area A2 are the same structures of the p-well PWL and the n-well NWL of the area A1. Channel ion implantation is performed for channel areas CHn1, CHp1 of the nMISQn1 and the pMISQp1 in area A2 as well; performing adjustments to threshold voltage.

[0041]
In this manner, regarding the present embodiment 3, effects as follows other than those that were obtained in the embodiments 1 and 2 can be obtained.

[0042]
In other words, by using a MIS vertical structure as described in embodiments 1 and 2 for a logic circuit MIS, and using a normal MIS vertical structure for an analog circuit and the like, an improvement in operating speed of

the logic circuit and an improvement in operating reliability of the analog circuit and the like can both be achieved.

[0043]
(Embodiment 4) In the CMIS circuit structure of embodiment 2, there are cases where the increase in substrate potential when voltage is applied to the gate is too large. In this case, as shown in FIG. 6, a crystal defect 12 is formed in the vicinity of the junction of the p type semiconductor area PA and the n-well NWL by ion implantation of impurity ions such as argon (Ar), germanium (Ge), and the like. As this causes a moderate re-combination in the depletion layer of the pn junction of the p type semiconductor area PA and the n-well NWL, allowing a leakage current to flow, ability to control this enables suppressing rise in potential of the p type semiconductor area PA. Therefore, as this improves controllability of nMISQn threshold voltage settings, operating reliability of the semiconductor device can be improved. Furthermore, electrons that were generated by the impact ionization of the pMISQp n type semiconductor area flow to the source p^+ type semiconductor area 11b (power supply wiring on the high-potential side). On the pMISQp side, a floating suppression effect for substrate potential is not produced even if a re-combination nucleus is formed so a crystal defect is not provided on the pMISQp side.

[0044]
(Embodiment 5) The present embodiment 5 is an explanation of a modified example to achieve the same objective as explained in embodiment 4. In other words, with an objective of suppressing an increase in substrate potential, a p^+ type semiconductor area 13P with a high impurity concentration is provided on the lower part of the p type semiconductor area PA (between the p type semiconductor area PA and the n-well NWL), as shown in FIG. 7. The p^+ type semiconductor area 13P comes in contact with both the p type semiconductor area PA and the n-well NWL. By providing this type of p^+ type semiconductor area 13P, the impurity concentrations in the area corresponding to the parasitic bipolar transistor base area formed by the source and drain semiconductor area 3 of the nMISQn and the p type semiconductor area PA can be increased, such that the current amplification factor of the parasitic bipolar transistor can be reduced. As a result, increase in substrate potential can be controlled. Therefore, as this improves controllability of nMISQn threshold voltage settings, operating reliability of the semiconductor device can be improved.

[0045]
In addition, regarding the present embodiment 5, with an objective of suppressing rise in substrate potential, an n^+ type semiconductor area 13N with a high impurity concentration is provided on the lower part of the n type semiconductor area NA (between the n type semiconductor area NA and the p-well PWL). The n^+ type semiconductor area 13N comes in contact with both the n type semiconductor area NA and the p-well PWL. Providing this type of n^+ type semiconductor area 13N, improves setting controllability of the pMISQp threshold value for the same reasons as with the nMISQn, enabling improving operating reliability of the semiconductor device.

[0046]
(Embodiment 6) The present embodiment 6 is a description of a modified example to achieve the same objective as explained in embodiments 4 and 5. In other words, with an objective of suppressing rise in substrate potential, regarding the forming area of the nMISQn, a p^+ type semiconductor area 13 is provided in a state of contact with the lower part of the p type semiconductor area PA, and an n^+ type semiconductor area 14 is provided in a state of contact with the lower part thereof, and the n-well NWL is provided in a state of contact with the lower part thereof, as shown in FIG. 8. This enables forming p^+ and n^+ high impurity concentration junctions, increasing the diode tunnel current, and causing a re-combination, such that the increase in substrate potential of the p type semiconductor area PA can be further suppressed. Therefore, as this improves

controllability of nMISQn threshold voltage settings, operating reliability of the semiconductor device can be improved. Furthermore, on the pMISQp side, an n^+ semiconductor area and a p^+ semiconductor area are not provided on the lower part of the n type semiconductor area NA for the same reasons as explained in embodiments 4 and 5.

[0047]
The present invention discovered by inventors has been specifically described using an embodiment; however, the present invention is not restricted to the embodiment described above and it goes without saying that various changes that do not deviate from the essentials of the invention can be made.

[0048]
In these explanations the invention made by the present inventors were mainly explained by application to semiconductor devices that have CMIS circuits, a use field of their background. However, use is not limited as such, and for example, can also be applied to semiconductor devices that have memory circuits such as DRAM (Dynamic Random Access Memory), SRAM (Static Random Access Memory), or flash memory (EEPROM; Electric Erasable Programmable Read Only Memory), and the like, semiconductor devices that have logic circuits such as a microprocessor, or consolidated type semiconductor devices that provide a memory circuit and a logic circuit on the same semiconductor substrate.

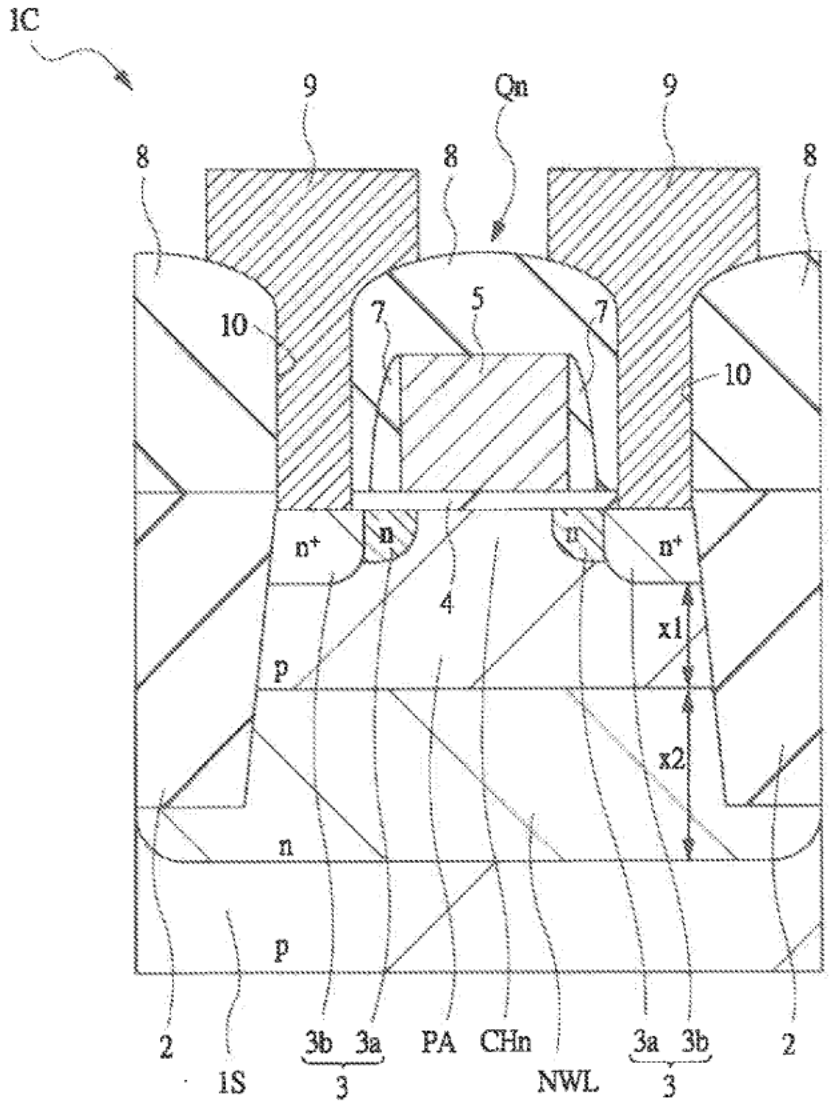
[0049]
EFFECT OF THE INVENTION
A simple description of the effects that can be obtained representing the invention disclosed in this application is provided below.
(1) The performance of a semiconductor device can be improved by using a pn junction to isolate a semiconductor substrate and a semiconductor area formed by a field effect transistor channel formed on the main surface thereof.
(2) A semiconductor device can be configured using a normal substrate structure without using an SOI structure that has a relatively high number of defects and is highly priced, by isolating a semiconductor substrate and a semiconductor area formed by a field effect transistor channel formed on the main surface thereof using a pn junction, enabling cost reduction.

BRIEF DESCRIPTION OF THE DRAWINGS
FIG. 1 is a cross-section view of the main part of the semiconductor chip that makes up the semiconductor device of the first embodiment of the present invention.
FIG. 2 is a graph diagram showing the impurity concentration distribution of the semiconductor substrate of the semiconductor device in FIG. 1.
FIG. 3 is a graph diagram showing the drain current gate voltage dependence of the field effect transistor of the semiconductor device in FIG. 1 and the field effect transistor formed on a normal semiconductor substrate.
FIG. 4 is a cross-section view of the main part of the semiconductor chip that makes up the semiconductor device of another embodiment of the present invention.
FIG. 5 is a cross-section view of the main part of the semiconductor chip that makes up the semiconductor device of another embodiment of the present invention.
FIG. 6 is a cross-section view of the main part of the semiconductor chip that makes up the semiconductor device of another embodiment of the present invention.
FIG. 7 is a cross-section view of the main part of the semiconductor chip that makes up the semiconductor device of another embodiment of the present invention.
FIG. 8 is a cross-section view of the main part of the semiconductor chip that makes up the semiconductor device of a further additional embodiment of the present invention.

EXPLANATION OF CODES
1C. semiconductor chip
1S. semiconductor substrate
2. Partitioning part
3. Semiconductor area
3a. n type semiconductor area
3b. n^+ semiconductor area
4. Gate insulating film
5. Gate electrode
7. Sidewall
8. Interlayer insulating membrane
9. First layer wiring
10. Contact hole
11. Semiconductor area
11a. p type semiconductor area
11b. p^+ type semiconductor area
12. Crystal defect
13P. p^+ type semiconductor area
13N. n^+ semiconductor area
14. n^+ semiconductor area
PA. p type semiconductor area (first conductivity type semiconductor area)
NWL. n-well (second conductivity type semiconductor area)
NA. n type semiconductor area (second conductivity type semiconductor)
PWL. p-well (first conductivity type semiconductor area)
Qp. p-channel type MISFET (first field effect transistor)
Qn. n-channel type MISFET (first field effect transistor)
Qp1. p-channel type MISFET (second field effect transistor)
Qn1. n-channel type MISFET (second field effect transistor)
CHn, CHn1 channel areas
CHp, CHp1 channel areas

[FIG. 1]

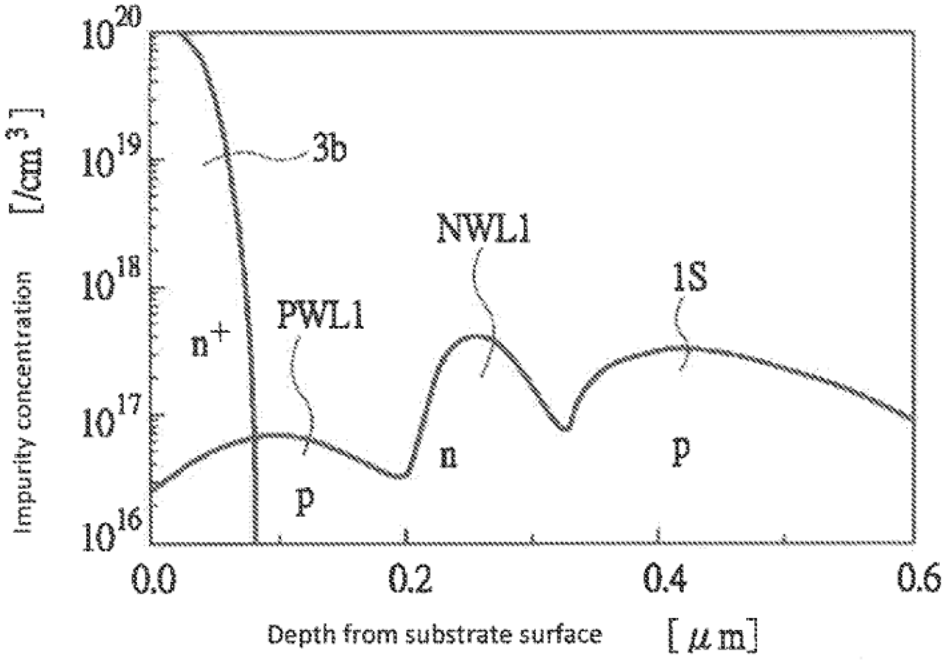
FIG. 1



1S: Semiconductor substrate
NWL: n-Well
Qn: n-channel type MISFET
PA: p type semiconductor area

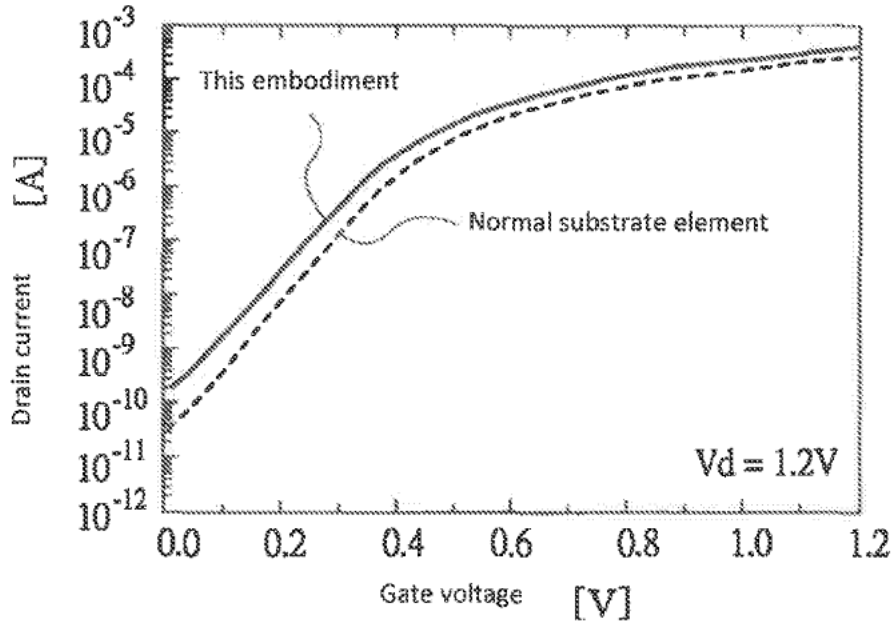
[FIG. 2]

FIG. 2


10^{20}
10^{19}
10^{18}
10^{17}
10^{16}
Impurity concentration [/cm^3]
3b
NWL1
1S
PWL1
n^+
n
p
p
0.0
0.2
0.4
0.6
Depth from substrate surface [μm]

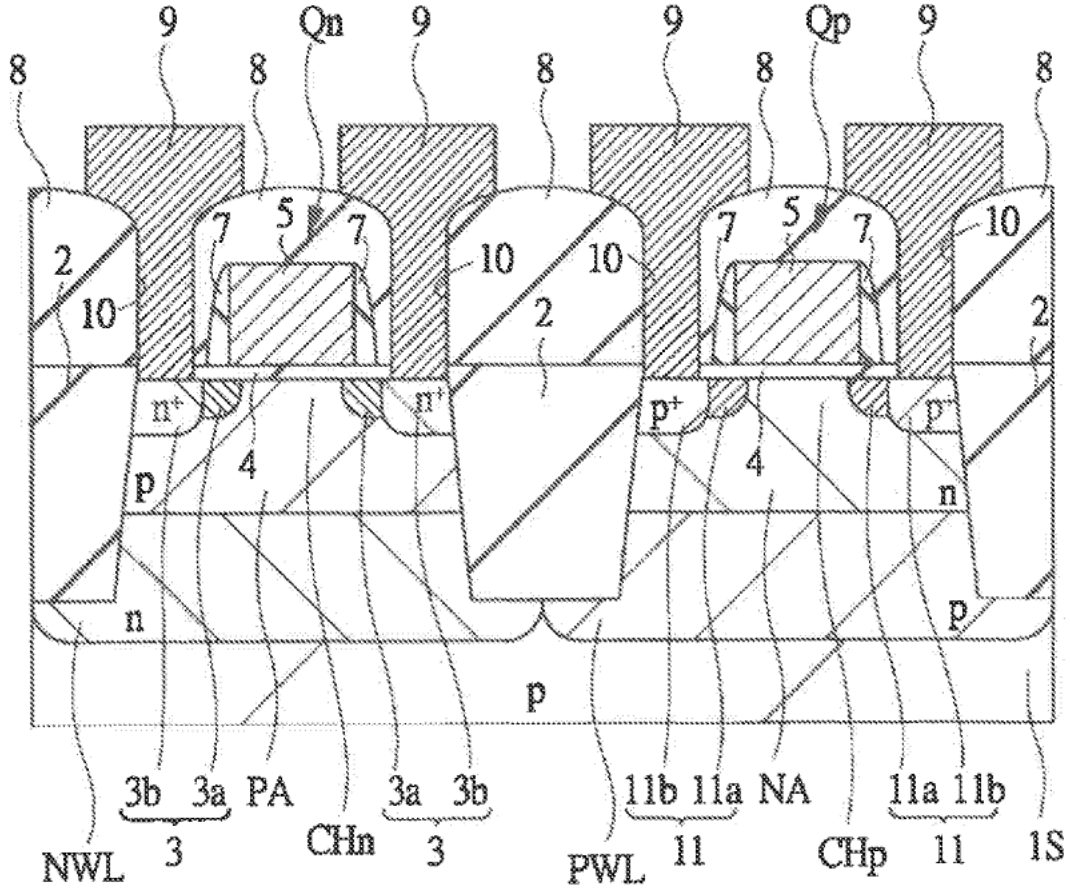
[FIG. 3]

FIG. 3


Drain current [A]
10-3
10-4
10-5
10-6
10-7
10-8
10-9
10-10
10-11
10-12
This embodiment
Normal substrate element
Vd = 1.2V
0.0
0.2
0.4
0.6
0.8
1.0
1.2
Gate voltage [V]

[FIG. 4]

FIG. 4


9
Qn
9
9
Qp
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8
7
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7
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10
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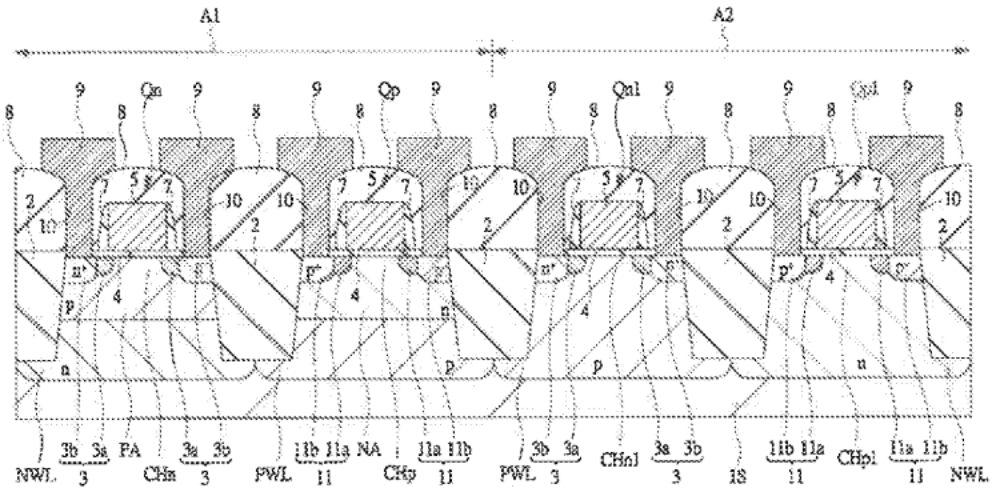
2
2
2
n+
n+
p+
p+
p
4
4
n
n
p
p
NWL
3b
3a
3
PA
CHn
3a
3b
3
PWL
11b
11a
11
NA
CHp
11a
11b
11
1S

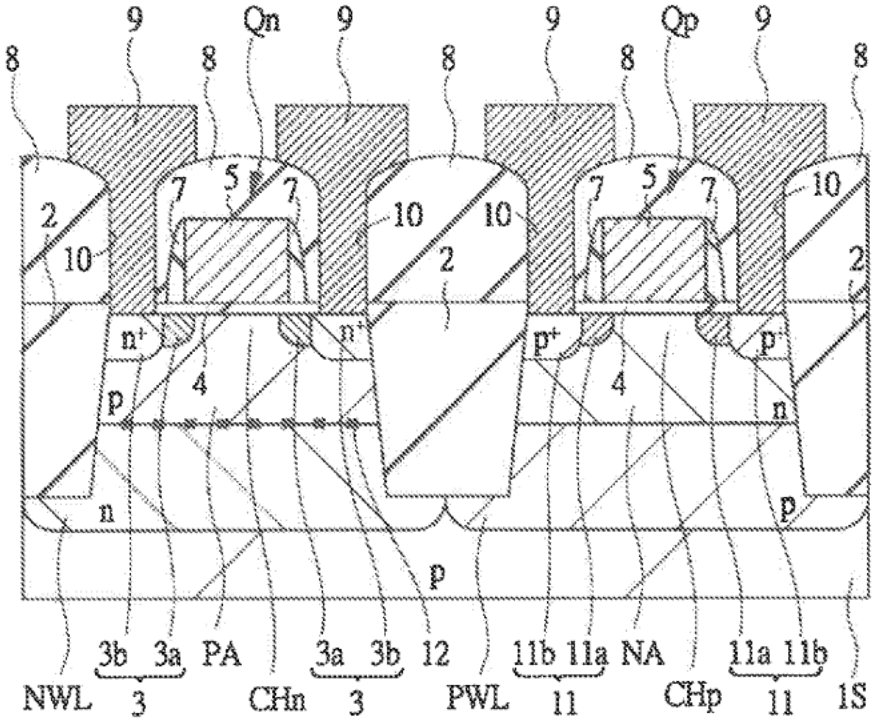
[FIG. 5]

FIG. 5



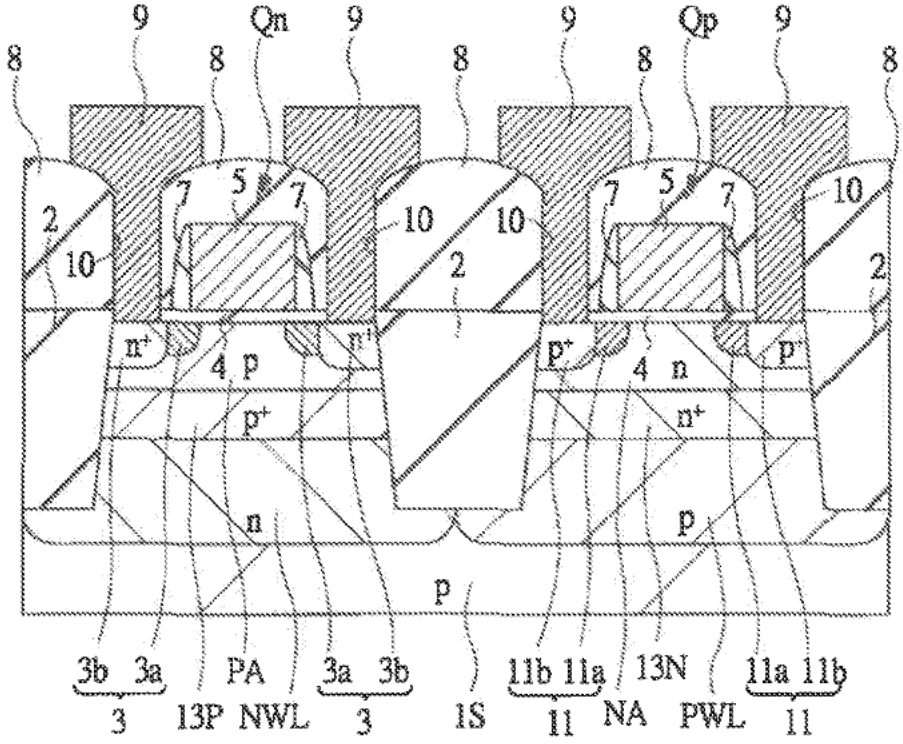
[FIG. 6]

FIG. 6



[FIG. 7]

FIG. 7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Qn
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Qp
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7
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7
5
7
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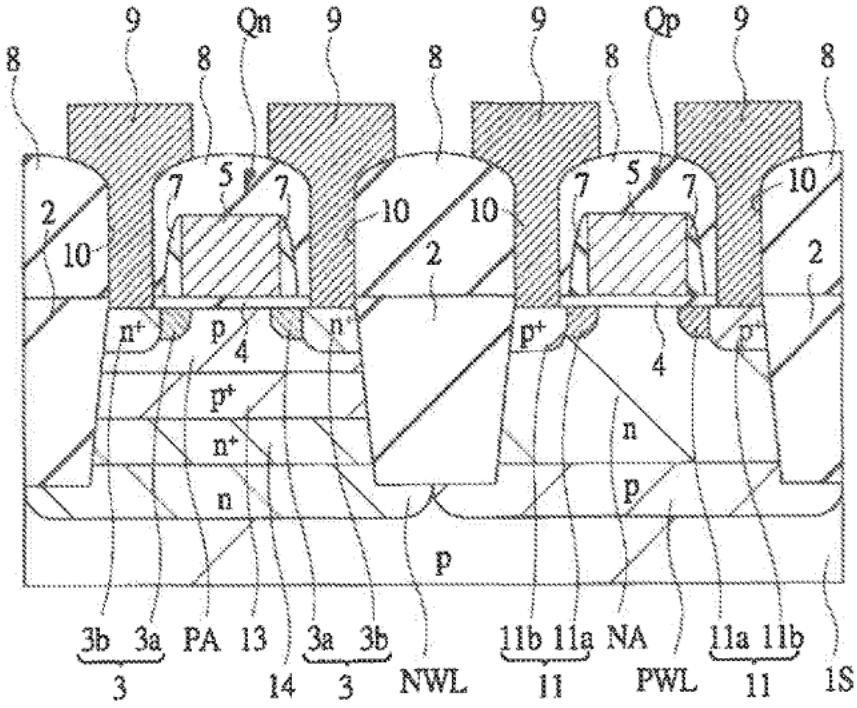
10
10
10
10
2
2
n+
n+
p+
p+
4 p
4 n
p+
n+
n
p
p
3b 3a
PA
3a 3b
11b 11a
13N
11a 11b
3
13P NWL
3
1S
11
NA PWL
11

[FIG. 8]

FIG. 8



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F-Terms (reference)

5F032 AA35 AA44 AB01 AB03 CA01
CA03 CA17 CA20 DA60 DA63

5F048 AA01 AA03 AA04 AA07 AB01
AB03 BA01 BA13 BB05 BB08
BB09 BB11 BB12 BB13 BB14
BC06 BE02 BE03 BG14 BH01
BH03 DA25

5F140 AA00 AB03 BA01 BD09 BD11
BD13 BF01 BF04 BF11 BF18
BF20 BF21 BF25 BF27 BG08
BG12 BH15 BH50 BJ01 BJ05
BK13 CB04 CB08 CB10 CD02

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27/08	３３１	21/76	Ｊ　５Ｆ１４０
27/092		29/78	３０１Ｒ
29/78			

審査請求　未請求　請求項の数５　ＯＬ　（全 10 頁）

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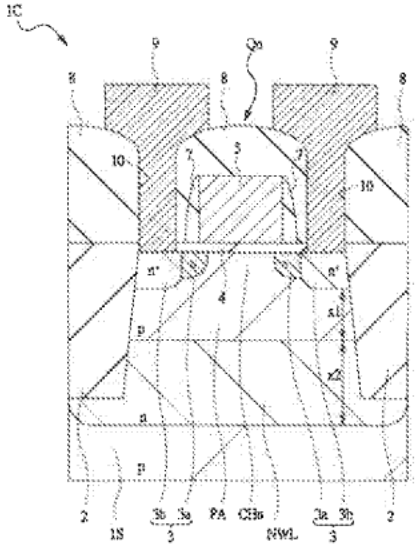
最終頁に続く

(54)【発明の名称】　半導体装置の製造方法および半導体装置

(57)【要約】　（修正有）
【課題】　高価なＳＯＩ基板を用いることなく、基板フローティングによる駆動電流の増加と、接合容量の低減を実現するとともに、ＳＯＩ基板の欠点である熱抵抗と結晶欠陥の課題を解決する。
【解決手段】　ｎ（ｐ）チャネル型のＭＩＳ・ＦＥＴＱｎ（Ｑｐ）が配置されたｐ（ｎ）型の半導体領域ＰＡ（ＰＮ）と、半導体基板１Ｓとの間にｎ（ｐ）ウエルＮＷＬ（ＰＭＬ）を設けることにより、そのｐ（ｎ）型の半導体領域ＰＡ（ＰＮ）と半導体基板１Ｓとを電気的に分離する。

図１



【特許請求の範囲】
【請求項１】　以下の工程を有することを特徴とする半導体装置の製造方法；
（ａ）第１導電型の半導体基板に第１不純物を導入することにより、前記第１導電型とは反対の導電型の第２導電型の半導体領域を形成する工程、（ｂ）前記半導体基板に第２不純物を導入することにより、前記第２導電型の半導体領域の不純物ピーク位置よりも、前記半導体基板の主面から浅い位置に不純物ピーク位置が配置するように形成された第１導電型の半導体領域を形成する工程、（ｃ）前記第１導電型の半導体領域内に、第２導電型のチャネル領域を有する電界効果トランジスタを形成する工程。
【請求項２】　半導体基板に設けられた第１導電型の半導体領域内に、その第１導電型とは反対導電型の第２導電型のチャネル領域を有する電界効果トランジスタを設け、前記半導体基板と、前記第１導電型の半導体領域との間に、第２導電型の半導体領域を設けることで、前記電界効果トランジスタの第２導電型のチャネル領域が形成される前記第１導電型の半導体領域と、前記半導体基板とを電気的に分離したことを特徴とする半導体装置。
【請求項３】　半導体基板に設けられた第１導電型の半導体領域内に、その第１導電型とは反対導電型の第２導電型のチャネル領域を有する電界効果トランジスタを設け、前記半導体基板と、前記第１導電型の半導体領域との間に、第２導電型の半導体領域を設けることで、前記電界効果トランジスタの第２導電型のチャネル領域が形成される前記第１導電型の半導体領域と、前記半導体基板とを電気的に分離した構造を有し、
前記電界効果トランジスタのソースおよびドレイン用の半導体領域下における前記第１導電型の半導体領域の厚さは、電源電圧の印加時に前記ソースおよびドレイン用の半導体領域および前記第１導電型の半導体領域の間における接合の空乏層幅と、前記第１導電型の半導体領域および前記第２導電型の半導体領域の間における接合の空乏層幅との和よりも大きいことを特徴とする半導体装置。
【請求項４】　半導体基板に設けられた第１導電型の半導体領域内に、その第１導電型とは反対導電型の第２導電型のチャネル領域を有する電界効果トランジスタを設け、前記半導体基板と、前記第１導電型の半導体領域との間に、第２導電型の半導体領域を設けることで、前記電界効果トランジスタの第２導電型のチャネル領域が形成される前記第１導電型の半導体領域と、前記半導体基板とを電気的に分離した構造を有し、
前記第２導電型の半導体領域の厚さは、前記第１導電型の半導体領域および第２導電型の半導体領域の間における接合の空乏層幅と、前記第２導電型の半導体領域および前記半導体基板の間における接合の空乏層幅との和よりも大きいことを特徴とする半導体装置。
【請求項５】　半導体基板の主面に第１の電界効果トランジスタと、第２の電界効果トランジスタとを有し、
前記第１の電界効果トランジスタは、前記半導体基板に設けられた第１導電型の半導体領域内に設けられ、その第１導電型の半導体領域は、その第１導電型の半導体領域と前記半導体基板との間に設けられた第１導電型とは反対導電型の第２導電型の半導体領域によって前記半導体基板と電気的に分離され、
前記第２の電界効果トランジスタは、前記半導体基板に設けられた前記第２導電型の半導体領域内に設けられていることを特徴とする半導体装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、半導体装置の製造方法および半導体装置技術に関し、特に、電界効果トランジスタを有する半導体装置の製造方法および半導体装置技術に適用して有効な技術に関するものである。
【０００２】
【従来の技術】本発明者らが検討した技術は、例えば部分空乏型のＳＯＩ（Silicon On Insulator）基板に電界効果トランジスタを設けた半導体装置構造である。ＳＯＩ基板は、下地絶縁層上に薄い半導体層を設け、その半導体層の主面上に電界効果トランジスタ等のような素子を形成する構造を有している。この構造の電界効果トランジスタのゲート電極に電圧が印加されると、ゲート絶縁膜側から空乏層が広がるが、反転層が形成される最大の空乏層幅となっても下地絶縁層には到達せず、空乏化しない基板領域が残される。この構造は最も良く用いられているが、基板（すなわち、半導体層）が電気的に絶縁されていることにより、導通時に基板電位が上昇し、しきい値電圧が下がる結果、駆動電流を多くとれる効果がある。また、ソースおよびドレイン用の半導体領域とチャネル層との接合の空乏層が下地絶縁層の上まで広がり、接合容量を大幅に低減できる。
【０００３】なお、部分空乏化型のＳＯＩ基板については、例えばScalability of SOI Technology into 0.13 μm 1.2V CMOS Generation, E.Leobandung,et.al,Tech.Digest of IEDM98,pp403-406,1998.IBMに記載がある。
【０００４】
【発明が解決しようとする課題】ところが、上記ＳＯＩ基板を用いた半導体装置技術においては、基板価格が通常基板の５倍以上と高価である、素子領域が絶縁体で覆われる構造のため熱抵抗が大きく接合温度が上昇し易い、現状では結晶欠陥が通常の基板構造に比べて多い、また、素子領域が絶縁体で完全に分離されるため基板電位のフローティングの制御が難しい等のような問題がある。そこで、ＳＯＩ構造が有している長所を如何にして通常の基板構造で実現するかが重要な課題となっている。

【０００５】本発明の目的は、半導体装置の性能を向上させることのできる技術を提供することにある。

【０００６】また、本発明の目的は、半導体装置のコストを低減することのできる技術を提供することにある。

【０００７】本発明の前記ならびにその他の目的と新規な特徴は、本明細書の記述および添付図面から明らかになるであろう。

【０００８】

【課題を解決するための手段】本願において開示される発明のうち、代表的なものの概要を簡単に説明すれば、次のとおりである。

【０００９】すなわち、本発明は、半導体基板と、その主面に形成された電界効果トランジスタのチャネルが形成される半導体領域とをｐｎ接合によって分離するものである。

【００１０】また、本発明は、半導体基板と、その主面に形成された電界効果トランジスタが形成された半導体領域との間に、前記半導体基板と半導体領域とを分離するように、その半導体領域とは反対導電型の半導体領域を設けるものである。

【００１１】

【発明の実施の形態】以下の実施の形態においては便宜上その必要があるときは、複数のセクションまたは実施の形態に分割して説明するが、特に明示した場合を除き、それらはお互いに無関係なものではなく、一方は他方の一部または全部の変形例、詳細、補足説明等の関係にある。

【００１２】また、以下の実施の形態において、要素の数等（個数、数値、量、範囲等を含む）に言及する場合、特に明示した場合および原理的に明らかに特定の数に限定される場合等を除き、その特定の数に限定されるものではなく、特定の数以上でも以下でも良い。

【００１３】さらに、以下の実施の形態において、その構成要素（要素ステップ等も含む）は、特に明示した場合および原理的に明らかに必須であると考えられる場合等を除き、必ずしも必須のものではないことは言うまでもない。

【００１４】同様に、以下の実施の形態において、構成要素等の形状、位置関係等に言及するときは、特に明示した場合および原理的に明らかにそうでないと考えられる場合等を除き、実質的にその形状等に近似または類似するもの等を含むものとする。このことは、上記数値および範囲についても同様である。

【００１５】また、本実施の形態を説明するための全図において同一機能を有するものは同一の符号を付し、その繰り返しの説明は省略する。

【００１６】また、本実施の形態においては、電界効果トランジスタを代表するＭＩＳ・ＦＥＴ（Metal Insulator Semiconductor Field Effect Transistor）をＭＩＳと略し、ｐチャネル型のＭＩＳ・ＦＥＴをｐＭＩＳと略し、ｎチャネル型のＭＩＳ・ＦＥＴをｎＭＩＳと略す。

【００１７】以下、本発明の実施の形態を図面に基づいて詳細に説明する。

【００１８】（実施の形態１）図１は、本発明の一実施の形態である半導体装置を構成する半導体チップ１Ｃのロジック回路部における要部断面図を示している。また、図２は、半導体チップ１Ｃを構成する半導体基板（以下、単に基板という）１Ｓの不純物濃度分布を示している。

【００１９】基板１Ｓは、例えばｐ型のシリコン（Ｓｉ）単結晶からなり、その主面（デバイス形成面）には、溝型の分離部（ＳＧＩ；Shallow Groove Isolation）２が形成されている。溝型の分離部２は、例えば基板１Ｓの主面に分離用の溝を形成した後、その溝内を埋め込むように基板１Ｓの主面上に酸化シリコン膜（SiO_2）等のような絶縁膜を堆積し、さらにその絶縁膜を溝内にのみに残されるようにＣＭＰ（Chemical Mechanical Polishing）等によって研磨することにより形成されている。溝型の分離部２の深さ（基板１Ｓの主面から分離部２の底面までの距離）は、例えば０．２～０．３μｍ程度である。この溝型の分離部２に囲まれた領域は活性領域（デバイス形成領域）となっている。この基板１Ｓにおいて活性領域にはｐ型の半導体領域ＰＡ（第１導電型の半導体領域）が形成されている。ｐ型の半導体領域ＰＡには、例えばホウ素（Ｂ）または二フッ化ホウ素（BF_2）が含有されている。ここでは、そのｐ型の半導体領域ＰＡ内に形成されたロジック回路用のｎＭＩＳＱｎが例示されている。

【００２０】ｎＭＩＳＱｎは、ソースおよびドレイン用の半導体領域３，３と、チャネル領域ＣＨｎと、ゲート絶縁膜４と、ゲート電極５とを有している。ソースおよびドレイン用の半導体領域３，３は、ｐ型の半導体領域ＰＡ内に形成されるチャネル領域ＣＨｎを挟んでその両側に一対となるように配置されており、それぞれチャネル領域ＣＨｎの近傍に配置されたｎ型の半導体領域３ａと、そのｎ型の半導体領域３ａ分を挟んでチャネル領域ＣＨｎから離間した位置に配置されたｎ⁺型の半導体領域３ｂとを有している。ｎ型の半導体領域３ａおよびｎ⁺型の半導体領域３ｂには、共に、例えばリン（Ｐ）またはヒ素（Ａｓ）が含有されているが、ｎ型の半導体領域３ａは、いわゆるエクステンション領域とも呼ばれ、その不純物濃度の方が、ｎ⁺型の半導体領域３ｂのそれよりも低くなるように設定されている。すなわち、ＬＤＤ（Lightly Doped Drain）構造とされている。

【００２１】また、後述する本実施の形態１の構造では、ｐ型の半導体領域ＰＡが電気的にフローティング状態となり、しきい値電圧が低下するので、そのしきい値電圧の低下し過ぎを防ぐべく、チャネル領域ＣＨｎの不純物濃度を高めにすることで、しきい値電圧が通常より

も５０ｍＶ～１００ｍＶほど高めになるように設定されている。ここでは、しきい値電圧を調整するために、チャネル領域ＣＨｎに、例えばホウ素が１０ｋｅＶ程度のイオン打ち込みエネルギーで基板１Ｓの主面からイオン注入されている。

【００２２】ゲート絶縁膜４は、例えば酸化シリコン（SiO_2）からなり、その厚さは、二酸化シリコン換算膜厚で、例えば２．５ｎｍ以下、一例としては１．５ｎｍ程度である。ただし、ゲート絶縁膜の材料は、これに限定されるものではなく種々変更可能であり、例えばゲート絶縁膜４を酸窒化シリコン膜（ＳｉＯＮ）としても良い。すなわち、ゲート絶縁膜４と基板１Ｓとの界面に窒素を偏析させる構造としても良い。酸窒化シリコン膜は、酸化シリコン膜に比べて膜中における界面準位の発生を抑制したり、電子トラップを低減したりする効果が高いので、ゲート絶縁膜４のホットキャリア耐性を向上でき、絶縁耐性を向上させることができる。また、酸窒化シリコン膜は、酸化シリコン膜に比べて不純物が貫通し難いので、酸窒化シリコン膜を用いることにより、ゲート電極材料中の不純物が基板１Ｓ側に拡散することに起因するしきい値電圧の変動を抑制することができる。酸窒化シリコン膜を形成するには、例えば基板１ＳをＮＯ、N_2OまたはNH_3といった含窒素ガス雰囲気中で熱処理すれば良い。また、基板１Ｓの表面に酸化シリコンからなるゲート絶縁膜４を形成した後、基板１Ｓを上記した含窒素ガス雰囲気中で熱処理し、ゲート絶縁膜４と基板１Ｓとの界面に窒素を偏析させることによっても、上記と同様の効果を得ることができる。また、ゲート絶縁膜４を、酸化シリコン膜上に窒化シリコン膜を積層した構造としても良い。さらに、ゲート絶縁膜４を、例えばHfO_2（誘電率ε＝２０．６）、ZrO_2（ε＝２４．７）、Al_2O_3（ε＝８．４）、Y_2O_3（ε＝１４）や$HfSiO_4$、$ZrSiO_4$（ε＝１９．４）等のような高誘電体膜からなる絶縁膜で形成しても良い。

【００２３】上記ゲート電極５は、例えば低抵抗多結晶シリコンからなる。ただし、これに限定されるものではなく種々変更可能であり、例えば低抵抗多結晶シリコン膜上にコバルトシリサイド（$CoSi_2$）等のようなシリサイド層を設けた、いわゆるポリサイドゲート電極構造や低抵抗多結晶シリコン膜上に窒化タングステン（ＷＮ）等のようなバリアメタル層を介してタングステン等のようなメタル膜を設けた、いわゆるポリメタルゲート電極構造としても良い。ゲート電極５の側面には、ＬＤＤ構造を形成すべく、例えば酸化シリコン膜からなるサイドウォール７が形成されている。また、ゲート長は、ゲート絶縁膜４の厚さが２．５ｎｍ程度であれば０．１４μｍ程度、ゲート絶縁膜４の厚さが１．５ｎｍ程度であれば０．０８μｍ程度である。また、ｎＭＩＳＱｎが形成されたロジック回路領域の高電位側の電源電圧は、例えば１．５Ｖ～０．７Ｖ程度であり、周辺回路領域の高電位側の電源電圧よりも相対的に低い。なお、半導体チップＩＣにおいて、周辺回路領域（例えば入力回路、出力回路および入出力双方向回路）の高電位側の電源電圧は、例えば３．０Ｖまたは３．３Ｖ程度である。

【００２４】このようなｎＭＩＳＱｎは、基板１Ｓの主面上に堆積された層間絶縁膜８によって覆われている。層間絶縁膜８は、例えば酸化シリコン膜からなり、その上面には、第１層配線９が形成されている。第１層配線９は、例えばアルミニウムまたはアルミニウム合金からなり、層間絶縁膜８に穿孔されたコンタクトホール１０を通じてソースおよびドレイン用の半導体領域３と電気的に接続されている。

【００２５】ところで、本発明者らは、部分空乏型のＳＯＩ基板を用いた半導体装置の開発中に、部分空乏型のＳＯＩ基板を用いた場合において、通常の基板を用いた場合に対するメリットの多くが、基板フローティングによる駆動電流の増加と、接合容量の低減とにあることを見出した。そこで、そのようなメリットを生じさせるような構造を通常の基板で実現するために、次のような構成を採用した。

【００２６】すなわち、本実施の形態１においては、ｎＭＩＳＱｎが形成されたｐ型の半導体領域ＰＡとその下層の基板１Ｓとの間にｎウエルＮＷＬ（第２導電型の半導体領域）が設けられている。このｎウエルＮＷＬの不純物分布は、基板１Ｓとｐ型の半導体領域ＰＡおよびチャネル領域ＣＨｎと基板１Ｓとが電気的に接続されないように、基板１Ｓの主面からの深さにおいて、溝型の分離部２の底部よりは若干浅い位置であって、ｐ型の半導体領域ＰＡのピーク位置よりは深い位置から溝型の分離部２の底部よりは若干深い位置に広がって分布されるように形成されている。すなわち、本実施の形態１においては、ｎＭＩＳＱｎのチャネル領域ＣＨｎおよびｐ型の半導体領域ＰＡと基板１Ｓとが、ｎウエルＮＷＬと基板１Ｓとのｐｎ接合によって電気的に分離されている。ここでは、ｎＭＩＳＱｎのソースおよびドレイン用の半導体領域３に対して電源電圧を印加した状態で、チャネル領域ＣＨｎ（ｐ型の半導体領域ＰＡ）の接合間の空乏層幅と、チャネル領域ＣＨｎ（ｐ型の半導体領域ＰＡ）とｎウエルＮＷＬとの間に広がる空乏層によって、ｎ型の半導体領域３ｂと、ｎウエルＮＷＬとが接続されないようにする必要がある。すなわち、図１中の距離ｘ１は、上記の空乏層幅の和よりも大きい必要がある。また、ｎウエルＮＷＬ自体の幅ｘ２もチャネル領域ＣＨｎ（ｐ型の半導体領域ＰＡ）との間の空乏層、基板１Ｓとの間の空乏層によって消滅しないようにする必要がある。すなわち、幅ｘ２は、上記空乏層の幅の和よりも大きい必要がある。このようなｎウエルＮＷＬは、上記溝型の分離部２を形成した後、例えばリンを４５０ｋｅＶ程度のイオン打ち込みエネルギーで基板１Ｓの主面からイオン注入することにより形成されている。なお、ｎウ

エルＮＷＬのピーク位置での不純物濃度は，図２に示すように，例えば１０^{9}／ｃｍ^{3}か若干それより低い程度である。

【００２７】このようなｎウエルＮＷＬを設けたことにより、半導体装置の性能上においてＳＯＩ基板を用いた場合と同様の効果を得ることができる。すなわち、導通時には、ゲート電極５と、チャネル領域ＣＨｎ（ｐ型の半導体領域ＰＡ）との容量結合によるチャネル領域ＣＨｎ（ｐ型の半導体領域ＰＡ）の電位の上昇と、Ｄレイン電流が流れインパクトイオゼイションによるホールが発生することによるチャネル領域ＣＨｎ（ｐ型の半導体領域ＰＡ）の電位の上昇とによって，ｎＭＩＳＱｎのしきい値電圧が下がり電流が増加する。図３は、本実施の形態１のｎＭＩＳＱｎと，ｎウエル分離構造を有しない通常の基板に形成されたｎＭＩＳとのドレイン電流のゲート電圧依存性を示している。本実施の形態１では，チャネル領域ＣＨｎ（ｐ型の半導体領域ＰＡ）が電気的に絶縁されているためにゲート電圧印加時には，しきい値電圧が低下し、ドレイン電流を増加させることができる。また、ソースおよびドレイン用の半導体領域３と基板１Ｓとの間の接合容量は、ｎ$^{-}$型の半導体領域３ｂとチャネル領域ＣＨｎ（ｐ型の半導体領域ＰＡ）との接合容量と、チャネル領域ＣＨｎ（ｐ型の半導体領域ＰＡ）とｎウエルＮＷＬとの接合容量と、ｎウエルＮＷＬと基板１Ｓとの接合容量とが直列接続された状態となるため、ｎウエルＮＷＬを設けない場合の約１／３に低減することができる。これらにより、このトランジスタを含む回路の動作速度を向上させることが可能となる。

【００２８】また、チャネル領域ＣＨｎ（ｐ型の半導体領域ＰＡ）と基板１Ｓとが絶縁体で完全に分離されるわけではなく、ｎウエルＮＷＬで分離される構造とされており、ＳＯＩ基板に比べて熱を逃がし易い構造となっているので、熱抵抗の増大を大幅に低減することができ，接合温度の上昇を抑えることができる。このため、半導体装置の動作信頼性を向上させることができる。また、パッケージ自体の冷却構造または半導体装置を冷却するための冷却装置や冷却機器を簡略化できる。

【００２９】また、ＳＯＩ基板に比べて結晶欠陥を低減できる。このため、半導体装置の歩留まりおよび信頼性を向上させることができる。

【００３０】また、基板電位の上昇の制御に関しても、チャネル領域ＣＨｎの下のｐｎ接合のリーク電流を制御することにより，比較的容易に制御することができる。すなわち、基板フローティングの制御性を向上させることができる。このため、回路設計を容易にすることができる。

【００３１】また、ｎウエルＮＷＬを設けているだけで基本的に通常の基板構造なので、高価なＳＯＩ基板を用いた場合に比べて半導体装置のコストを低減することができる。

【００３２】（実施の形態２）本実施の形態２においては、ＣＭＩＳ（Complementary MIS）回路を有する半導体装置に本発明を適用した場合について説明する。

【００３３】図４は、本発明の他の実施の形態である半導体装置を構成する半導体チップ１Ｃのロジック回路部を構成するＣＭＩＳ回路部の要部断面図を示している。

【００３４】ｎＭＩＳＱｎの形成領域の縦構造は、前記実施の形態１と同じなので説明を省略し、ここでは、ｐＭＩＳＱｐの形成領域の縦構造について説明する。ｐＭＩＳＱｐの形成領域において基板１Ｓの活性領域には、ｎ型の半導体領域ＮＡ（第２導電型の半導体領域）が形成されており，このｎ型の半導体領域ＮＡ内にｐＭＩＳＱｐが形成されている。このｎ型の半導体領域ＮＡには、例えばリン（Ｐ）またはヒ素（Ａｓ）が含有されている。

【００３５】ｐＭＩＳＱｐは、ソースおよびドレイン用の半導体領域１１，１１と、チャネル領域ＣＨｐと、ゲート絶縁膜４と、ゲート電極５とを有している。ソースおよびドレイン用の半導体領域１１，１１は，チャネル領域ＣＨｐを挟んで一対となるように配置されており、それぞれチャネル領域ＣＨｐの近傍に配置されたｐ型の半導体領域１１ａと，そのｐ型の半導体領域１１ａ分を挟んでチャネル領域ＣＨｐから離間した位置に配置されたｐ$^{+}$型の半導体領域１１ｂとを有している。ｐ型の半導体領域１１ａおよびｐ$^{+}$型の半導体領域１１ｂには、共に，例えばホウ素（Ｂ）またはフッ化ホウ素（ＢＦ$_{2}$）が含有されているが、ｐ型の半導体領域１１ａは，いわゆるエクステンション領域とも呼ばれ、その不純物濃度の方が，ｐ$^{+}$型の半導体領域１１ｂのそれよりも低くなるように設定されている。すなわち，ＬＤＤ構造とされている。

【００３６】そして、本実施の形態２においては、ｐＭＩＳＱｐが形成されたｎ型の半導体領域ＮＡとその下層の基板１Ｓとの間にｐウエルＰＷＬ（第１導電型の半導体領域）が設けられている。すなわち、本実施の形態２においては、ｐＭＩＳＱｐのチャネル領域ＣＨｐ（ｎ型の半導体領域ＮＡ）と基板１Ｓとが、ｐウエルＰＷＬとｎ型の半導体領域ＮＡとのｐｎ接合によって電気的に分離されている。このｐウエルＰＷＬの不純物分布や形成状態は，前記ｎウエルＮＷＬと同じなので説明を省略する。このようなｐウエルＰＷＬは、上記導型の分離部２を形成した後、例えばホウ素を１６０ｋｅＶ程度のイオン打ち込みエネルギーで基板１Ｓの主面からイオン注入することにより形成されている。なお、ｐウエルＰＷＬのピーク位置での不純物濃度は、ｎウエルＮＷＬと同じ程度である。ｐＭＩＳＱｐのチャネル領域ＣＨｐは、所望のしきい値（従来構造の場合よりも５０ｍＶ～１００ｍＶ程度エンハンス側）となるように、例えばリンを２０ｋｅＶ程度基板１Ｓの主面側からイオン注入することで形成されている。これ以外は、前記実施の形態１と同

じなので説明を省略する。

【００３７】このように本実施の形態２によれば、前記実施の形態１で得られた効果の他に、以下の効果を得ることができる。すなわち、ｐＭＩＳＱｐでも、上記ｎＭＩＳＱｎと同様の効果を得ることができる。したがって、ＣＭＩＳ回路で構成されるロジック回路を有する半導体装置の動作速度（性能）を向上させることができる。

【００３８】（実施の形態３）前記実施の形態１，２のＭＩＳの縦構造においては、上記のように動作速度を向上させることはできるが、ＭＩＳのしきい値電圧が動作領域内で変動し不安定になる。そこで、本実施の形態３においては、同一の基板１Ｓに形成されるＭＩＳであっても、前記ＭＩＳの縦構造を採用するものと、採用しないものとの作り分けを行った。すなわち、回路に必要とされる電気的特性に応じて前記実施の形態１，２で説明したＭＩＳの縦構造と、通常のＭＩＳの縦構造とを使い分けた。具体的には、しきい値電圧がある程度変動しても動作に支障をきたさない回路を構成するＭＩＳには前記ＭＩＳの縦構造を採用し、しきい値電圧が変動すると動作に支障をきたす回路を構成するＭＩＳには前記ＭＩＳの縦構造を採用せず一般的なＭＩＳの縦構造とした。例えばデジタル回路を構成するＭＩＳには、前記実施の形態１，２で説明したＭＩＳの縦構造を採用した。また、例えば高い動作精度を必要とするアナログ回路、入出力回路またはメモリ回路のメモリセルやセンスアンプ回路等（以下、単にアナログ回路等という）を構成するＭＩＳは、前記ＭＩＳの縦構造を採用せず、通常のＭＩＳの縦構造を採用した。メモリセルは、デジタル回路ではあるが、微小な信号（電荷）を読み出したり、書き込んだりするので、メモリセルを構成するＭＩＳ・ＦＥＴのしきい値電圧が変動するとデータ処理に支障をきたすことから、通常のＭＩＳの縦構造を採用することが好ましい。また、本発明者らの検討によれば、ＭＩＳの動作電圧（高電位側の電源電圧）の観点で考慮した場合、その動作電圧が、例えば１．５Ｖ以下ならば、前記実施の形態１，２で説明したＭＩＳの縦構造を採用することが好ましい。一方、ＭＩＳの動作電圧が、例えば１．５Ｖよりも高いならば、上記通常のＭＩＳの縦構造を採用することが好ましい。

【００３９】図５は、本実施の形態３の半導体装置の要部断面図の一例を示している。領域Ａ１は、ロジック回路（デジタル回路）を構成するｎＭＩＳＱｎおよびｐＭＩＳＱｐ（第１の電界効果トランジスタ）の配置領域を示している。この領域Ａ１では、前記実施の形態１，２で説明したＭＩＳの縦構造が採用されている。

【００４０】一方、領域Ａ２は、上記アナログ回路、入出力回路、メモリ回路のメモリセルやセンスアンプ回路等のようなしきい値電圧が変動すると支障を来す回路を構成するｎＭＩＳＱｎ１、Ｑｐ１（第２の電界効果トランジスタ）の配置領域を示している。この領域Ａ２では、上記通常のＭＩＳの縦構造が採用されている。すなわち、ｎＭＩＳＱｎ１は、ｐウエルＰＷＬ内に形成され、ｐＭＩＳＱｐ１は、ｎウエルＮＷＬ内に形成されている。領域Ａ２のｐウエルＰＷＬおよびｎウエルＮＷＬの構造は、領域Ａ１のｐウエルＰＷＬおよびｎウエルＮＷＬの構造と同じである。この領域Ａ２のｎＭＩＳＱｎ１およびｐＭＩＳＱｐ１においても、チャネル領域ＣＨｎ１、ＣＨｐ１へのチャネルイオン注入が行われ、しきい値電圧の調整が行われている。

【００４１】このように、本実施の形態３においては、前記実施の形態１，２で得られた効果の他に以下の効果を得ることが可能となる。

【００４２】すなわち、ロジック回路のＭＩＳには、前記実施の形態１，２で説明したＭＩＳの縦構造を採用し、アナログ回路等のＭＩＳには、通常のＭＩＳの縦構造を採用したことにより、ロジック回路における動作速度の向上と、アナログ回路等における動作信頼性の向上とを両立することが可能となる。

【００４３】（実施の形態４）前記実施の形態２のＣＭＩＳ回路の構造では、ゲート電圧印加時の基板電位の上昇が大きすぎる場合がある。この場合には、図６に示すように、ｐ型の半導体領域ＰＡとｎウエルＮＷＬとの接合周辺に、例えばアルゴン（Ａｒ）またはゲルマニウム（Ｇｅ）等のような不純物イオンをイオン注入することにより、結晶欠陥１２を形成する。これにより、ｐ型の半導体領域ＰＡとｎウエルＮＷＬとのｐｎ接合の空乏層内に濃度な再結合を生じさせ、リーク電流を流し、これを制御することができるので、ｐ型の半導体領域ＰＡの電位の上昇を抑えることができる。したがって、ｎＭＩＳＱｎのしきい値電圧の設定制御性を向上させることができるので、半導体装置の動作信頼性を向上させることが可能となる。なお、ｐＭＩＳＱｐのｎ型の半導体領域のインパクトイオン化で発生した電子は、ソース用のｐ＋型の半導体領域１１ｂ（高電位側の電源配線）に流れ、ｐＭＩＳＱｐ側では再結合中心を形成しても基板電位のフローティング抑制に効果が生じないので、ｐＭＩＳＱｐ側には結晶欠陥を設けていない。

【００４４】（実施の形態５）本実施の形態５は、前記実施の形態４で説明したのと同じ目的を達成するための変形例を説明するものである。すなわち、基板電位の上昇を抑制することを目的として、図７に示すように、ｐ型の半導体領域ＰＡの下部（ｐ型の半導体領域ＰＡとｎウエルＮＷＬとの間）に高不純物濃度のｐ型の半導体領域１３Ｐを設ける。ｐ＋型の半導体領域１３Ｐは、ｐ型の半導体領域ＰＡおよびｎウエルＮＷＬの両方に接している。このようなｐ＋型の半導体領域１３Ｐを設けることにより、ｎＭＩＳＱｎのソースおよびドレイン用のｎ＋型半導体領域３と、ｐ型の半導体領域ＰＡとで形成される寄生バイポーラトランジスタのベース領域に相当する領

域の不純物濃度を高くすることができるので、その寄生バイポーラトランジスタの電流増幅率を低減することができる。その結果、基板電位の上昇を抑制することができる。したがって、ｎＭＩＳＱｎのしきい値電圧の設定制御性を向上させることができるので、半導体装置の動作信頼性を向上させることが可能となる。

【００４５】また、本実施の形態５においては、基板電位の上昇を抑制することを目的として、ｎ型の半導体領域ＮＡの下部（ｎ型の半導体領域ＮＡとｐウエルＰＷＬとの間）に高不純物濃度のｎ'型の半導体領域１３Ｎを設ける。ｎ'型の半導体領域１３Ｎは、ｎ型の半導体領域ＮＡおよびｐウエルＰＷＬの両方に接している。このようなｎ'型の半導体領域１３Ｎを設けることにより、上記のｎＭＩＳＱｎと同様の理由からｐＭＩＳＱｐのしきい値電圧の設定制御性を向上させることができるので、半導体装置の動作信頼性を向上させることが可能となる。

【００４６】（実施の形態６）本実施の形態６は、前記実施の形態４、５で説明したのと同じ目的を達成するための変形例を説明するものである。すなわち、基板電位の上昇を抑制することを目的として、図８に示すように、ｎＭＩＳＱｎの形成領域において、ｐ型の半導体領域ＰＡの下部に、これに接した状態でｐ'型の半導体領域１３を設け、さらにその下部に、これに接した状態でｎ'型の半導体領域１４を設け、その下部に、これに接した状態で上記ｎウエルＮＷＬが設けている。これにより、ｐ'ｎ'の高不純物濃度の接合を形成することができ、ダイオードのトンネル電流を増大させ、再結合を生じさせることができるので、ｐ型の半導体領域ＰＡの基板電位の上昇をさらに抑制することができる。したがって、ｎＭＩＳＱｎのしきい値電圧の設定制御性を向上させることができるので、半導体装置の動作信頼性を向上させることが可能となる。なお、ｐＭＩＳＱｐ側には、前記実施の形態４、５で説明したのと同じ理由から、ｎ型の半導体領域ＮＡの下部にｎ'型の半導体領域およびｐ'型の半導体領域を設けていない。

【００４７】以上、本発明者によってなされた発明を実施の形態に基づき具体的に説明したが、本発明は前記実施の形態に限定されるものではなく、その要旨を逸脱しない範囲で種々変更可能であることはいうまでもない。

【００４８】以上の説明では主として本発明者によってなされた発明をその背景となった利用分野であるＣＭＩＳ回路を有する半導体装置に適用した場合について主に説明したが、それに限定されるものではなく、例えばＤＲＡＭ（Dynamic Random Access Memory）、ＳＲＡＭ（Static Random Access Memory）またはフラッシュメモリ（ＥＥＰＲＯＭ；Electric Erasable Programmable Read Only Memory）等のようなメモリ回路を有する半導体装置、マイクロプロセッサ等のような論理回路を有する半導体装置あるいは上記メモリ回路と論理回路とを同一半導体基板に設けている混載型の半導体装置にも適用できる。

【００４９】

【発明の効果】本願によって開示される発明のうち、代表的なものによって得られる効果を簡単に説明すれば、以下の通りである。

(1).半導体基板と、その主面に形成された電界効果トランジスタのチャネルが形成される半導体領域とをｐｎ接合によって分離することにより、半導体装置の性能を向上させることが可能となる。

(2).半導体基板と、その主面に形成された電界効果トランジスタのチャネルが形成される半導体領域とをｐｎ接合によって分離することにより、比較的欠陥が多く高価なＳＯＩ構造を用いず、通常の基板構造を用いて半導体装置を構成することができるので、半導体装置のコストを低減することが可能となる。

【図面の簡単な説明】

【図１】本発明の一実施の形態である半導体装置を構成する半導体チップの要部断面図である。

【図２】図１の半導体装置の半導体基板における不純物濃度分布を示すグラフ図である。

【図３】図１の半導体装置の電界効果トランジスタと通常の半導体基板に形成された電界効果トランジスタとのドレイン電流のゲート電圧依存性を示すグラフ図である。

【図４】本発明の他の実施の形態である半導体装置を構成する半導体チップの要部断面図である。

【図５】本発明の他の実施の形態である半導体装置を構成する半導体チップの要部断面図である。

【図６】本発明の他の実施の形態である半導体装置を構成する半導体チップの要部断面図である。

【図７】本発明の他の実施の形態である半導体装置を構成する半導体チップの要部断面図である。

【図８】本発明のさらに他の実施の形態である半導体装置を構成する半導体チップの要部断面図である。

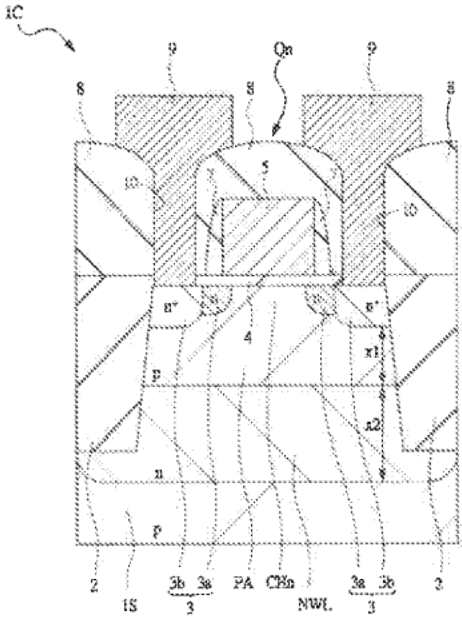
【符号の説明】

１Ｃ　半導体チップ
１Ｓ　半導体基板
２　分離部
３　半導体領域
３ａ　ｎ型の半導体領域
３ｂ　ｎ'型の半導体領域
４　ゲート絶縁膜
５　ゲート電極
７　サイドウォール
８　層間絶縁膜
９　第１層配線
１０　コンタクトホール
１１　半導体領域
１１ａ　ｐ型の半導体領域

１１ｂ　ｐ型の半導体領域
１２　結晶欠陥
１３Ｐ　ｐ型の半導体領域
１３Ｎ　ｎ型の半導体領域
１４　ｎ型の半導体領域
ＰＡ　ｐ型の半導体領域（第１導電型の半導体領域）
ＮＷＬ　ｎウエル（第２導電型の半導体領域）
ＮＡ　ｎ型の半導体領域（第２導電型の半導体領域）
ＰＷＬ　ｐウエル（第１導電型の半導体領域）
Ｑｐ　ｐチャネル型のＭＩＳ・ＦＥＴ（第１の電界効果＊トランジスタ）
Ｑｎ　ｎチャネル型のＭＩＳ・ＦＥＴ（第１の電界効果トランジスタ）
Ｑｐｌ　ｐチャネル型のＭＩＳ・ＦＥＴ（第２の電界効果トランジスタ）
Ｑｎｌ　ｎチャネル型のＭＩＳ・ＦＥＴ（第２の電界効果トランジスタ）
ＣＨｎ，ＣＨｎｌ　チャネル領域
ＣＨｐ，ＣＨｐｌ　チャネル領域

【図１】

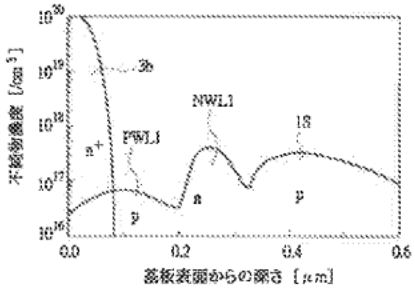
図 1



1S：半導体基板
NWL：nウエル
Qn：nチャネル型のMIS・FET
PA：p型の半導体領域

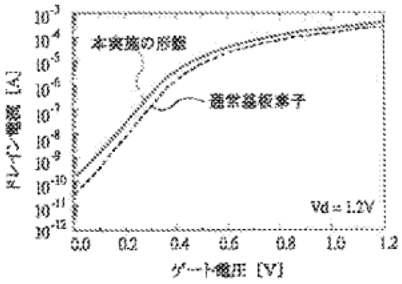
【図２】

図 2



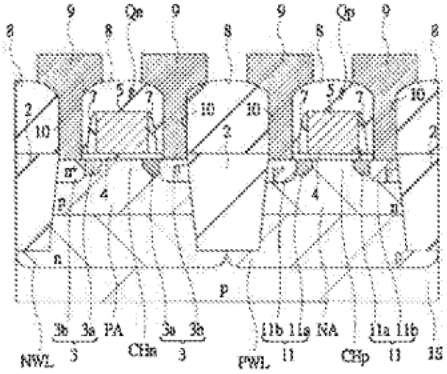
【図３】

図 3



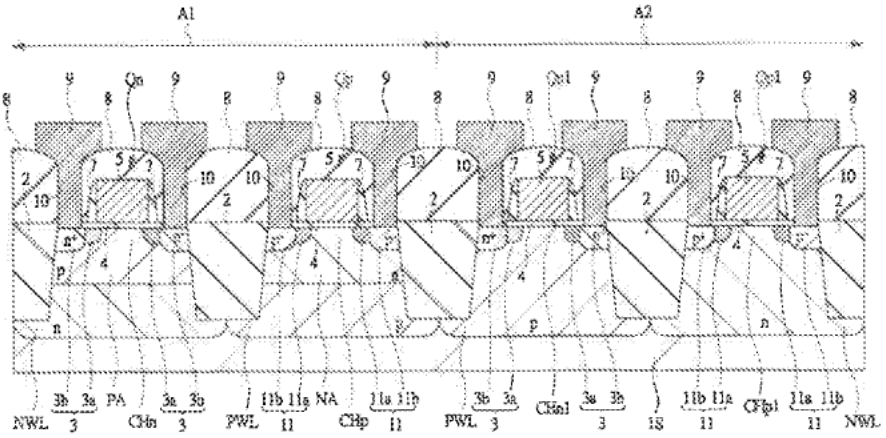
【図４】

図 4



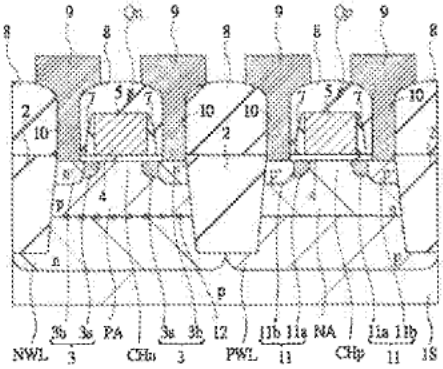
【図５】

図 5



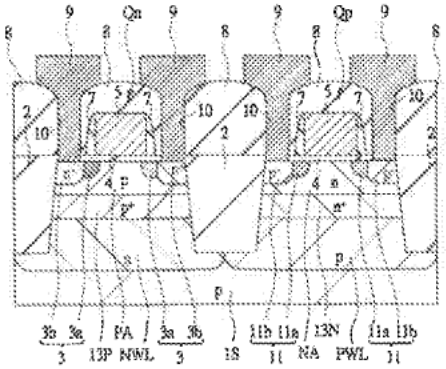
【図６】

図 6



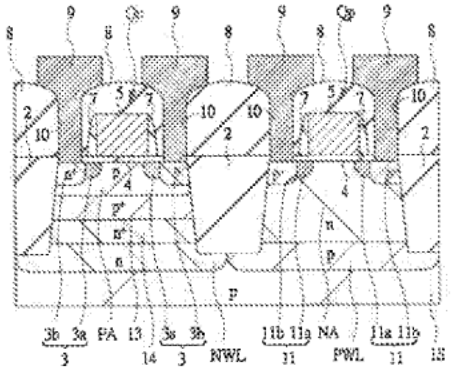
【図７】

図 7



【図８】

図８



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Ｆターム(参考) 5F032 AA35 AA44 AB01 AB03 CA01
CA03 CA17 CA20 DA60 DA63
5F048 AA01 AA03 AA04 AA07 AB01
AB03 BA01 BA13 BB05 BB08
BB09 BB11 BB12 BB13 BB14
BC06 BE02 BE03 BG14 BH01
BH03 DA25
5F140 AA00 AB03 BA01 BD09 BD11
BD13 BF01 BF04 BF11 BF18
BF20 BF21 BF25 BF27 BG08
BG12 BH15 BH50 BJ01 BJ05
BK13 CB04 CB08 CB10 CD02

Electronic Acknowledgement Receipt

EFS ID:	43081214
Application Number:	16947294
International Application Number:	
Confirmation Number:	6907
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	40672
Filer:	Gregory Michael Howison/Joselyn Rodriguez
Filer Authorized By:	Gregory Michael Howison
Attorney Docket Number:	GRTD.01.01.DV7
Receipt Date:	30-JUN-2021
Filing Date:	27-JUL-2020
Time Stamp:	18:55:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	GRT35294IDS.pdf	1055732 cc674ed0f5a92e99f49716a1e1cb55e262dca969	no	10

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2	Foreign Reference	JP6482563.pdf	1365088 bb0ae772df1736c1a8ff315d1fa06cbb81c6cd1f	no	18
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5	Non Patent Literature	Exhibit1003SmithDec.pdf	2514721 171acfb9b7b76961c2f73f9a242bab8f7124a115	no	94
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6	Non Patent Literature	NPL_00288PetitionforInterPartesReview.pdf	2788021 d4d8ea2381ecd7089fb35bd8dd501fa7453ea0b9	no	86
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7	Non Patent Literature	NPL_00289PetitionerReply.pdf	159371 ec6ad1e0b2999e5748b315d332451f9c3875c676	no	13
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8	Non Patent Literature	NPL_00290Exhibit1003SmithDec.pdf	2514695 89b46b651ebf1b91116ba5cf711578c0c57dba20	no	94
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14	Non Patent Literature	NPL_195SurReply.pdf	186970 475b0cf6146a0ed8831deca31e0ac2d13e3d16b5	no	13
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Information:					
		Total Files Size (in bytes):	76755121		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD.01.01.DV7	6907

40672 7590 02/12/2021

BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380

EXAMINER	

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
02/12/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@naifeh.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

In re Application of	:	
Rao, G.R. Mohan	:	
Application No. 16/947,294	:	DECISION ON PETITION
Filed: 27 Jul 2020	:	
For: SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS	:	

This is a notice regarding your renewed request filed January 22, 2021, for acceptance of a fee deficiency submission under 37 CFR 1.28(c).

The Office no longer investigates or rejects original or reissue applications under 37 CFR 1.56. **1098 Off. Gaz. Pat. Office 502 (January 3, 1989)**. Therefore, nothing in this Notice is intended to imply that an investigation was done.

Your fee deficiency submission under 37 CFR 1.28(c) is hereby **ACCEPTED**.

Accordingly, status as a small entity has been removed and any future fee(s) submitted must be paid at the undiscounted rate.

Inquiries related to this communication should be directed to the undersigned at (571) 272-1058.

/Angela Walker/
Angela Walker
Paralegal Specialist
Office of Petitions

United States Patent and Trademark Office

Office of the Chief Financial Officer

Document Code:WFEE

User :C41722

Sale Accounting Date:02/09/2021

Sale Item Reference Number	Effective Date
16947294	09/28/2020

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I202129F04190768	1461	1.28(C) SUBMISSIONS - APPLIC FILE FEE	$3,135.00	Salea

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:	G.R. Mohan Rao	§	Confirmation No.	6907
Serial No:	16/947,294	§	Group Art Unit:	2812
Filed:	July 27, 2020	§	Examiner:	N/A

For: **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS**

Via EFS-Web
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

RESPONSE TO DECISION ON PETITION AND
RENEWED NOTIFICATION OF LOSS OF ENTITLEMENT TO SMALL ENTITY STATUS

Dear Sir:

In response to the Decision on Petition mailed January 15, 2021, Applicant hereby submits the following itemization:

Type of Fee Paid	Amount of Fee Paid	Date Paid	Deficiency Owed
Basic filing fee	$75.00	9/25/2020	$225.00
Surcharge	$80.00	9/25/2020	$80.00
Search fee	$330.00	9/25/2020	$330.00
Exam Fee	$380.00	9/25/2020	$380.00
Additional claims fees	$2,120.00	9/25/2020	$2,120.00
Total Deficiency Payment Owed and Paid			**$3,135.00**

Applicant hereby notifies the Office of its loss of entitlement to small entity status.

On September 25, 2020, Applicant submitted payment of fees in the amount of $2,985.00 in response to the Notice to File Missing Parts.

On September 28, 2020, Applicant filed a Notification of Loss of Entitlement to Small Entity Statement and submitted payment of $3,135.00 via Credit Card. On October 5, 2020, the Patent Office charged the Credit Card in the amount of $3,135.00 for the deficiency fee payment owed. Therefore, no further fees are due.

Applicant hereby requests acceptance of this Response and Renewed Notification of Loss Entitlement to Small Entity Status.

Respectfully submitted,

/Bill R. Naifeh, Reg. No. 44,962/

Bill R. Naifeh
Registration No. 44,962

Law Office of Bill Naifeh
P.O. Box 803423
Dallas, TX 75380
972-726-9500
214-550-2542 (fax)

Electronic Acknowledgement Receipt

EFS ID:	41719937
Application Number:	16947294
International Application Number:	
Confirmation Number:	6907
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	40672
Filer:	Bill Naifeh/April Reasoner
Filer Authorized By:	Bill Naifeh
Attorney Docket Number:	GRTD.01.01.DV7
Receipt Date:	22-JAN-2021
Filing Date:	27-JUL-2020
Time Stamp:	14:57:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Notification of loss of entitlement to small entity status	ResponsetoDecision.pdf	19938 78cd0f143b8a8a8f55848a65adc2cd020b2db564	no	2

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Information:	
Total Files Size (in bytes):	19938

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD.01.01.DV7	6907

40672 7590 01/15/2021

BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380

EXAMINER	
ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
01/15/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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In re Application of	:	
Rao, G.R. Mohan	:	
Application No. 16/947,294	:	DECISION ON PETITION
Filed: July 27, 2020	:	
For: SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS	:	

This is a notice in response to the request filed on September 28, 2020, a request for acceptance of a fee deficiency submission under 37 CFR 1.28(c).

The Office no longer investigates or rejects original or reissue applications under 37 CFR 1.56. **1098 Off. Gaz. Pat. Office 502 (January 3, 1989)**. Therefore, nothing in this Notice is intended to imply that an investigation was done.

The fee deficiency submission under 37 CFR 1.28(c) is **NOT ACCEPTED**.

Applicant should note that 37 CFR 1.28(c) states in part: If status as a small entity is established in good faith, and fees as a small entity are paid in good faith, in any application or patent, and it is later discovered that such status as a small entity was established in error, or that through error the Office was not notified of a loss of entitlement to small entity status as required by § 1.27(g)(2), the error will be excused upon compliance with the separate submission and itemization. See 37 CFR 1.28(c)(2)(ii).

The itemization must include the following information:

(A) Each particular type of fee that was erroneously paid as a small entity, (e.g., basic statutory filing fee, two-month extension of time fee) along with the current fee amount for a non-small entity;

(B) The small entity fee actually paid, and when. This will permit the Office to differentiate, for example, between two one-month extension of time fees erroneously paid as a small entity but on different dates;

(C) The deficiency owed amount (for each fee erroneously paid); and

(D) The total deficiency payment owed, which is the sum or total of the individual deficiency owed amounts set forth in paragraph (c)(2)(ii)(C) of this section.

An itemization chart was not included with the request. Any renewed request must include the information in item(s) A-D above.

Applicant is given **ONE MONTH** to submit a complete listing of all the fees erroneously paid as a small entity and the total fee deficiency to avoid non acceptance of the present fee deficiency paper. This time period is not extendable under 37 CFR 1.136(a).

Further correspondence with respect to this matter should be addressed as follows:

By Mail:	Mail Stop PETITION Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450
By FAX:	(571) 273-8300 ATTN: Office of Petitions
By Hand:	U. S. Patent and Trademark Office Customer Service Window, Mail Stop Petitions Randolph Building 401 Dulany Street Alexandria, VA 22314
By Internet:	EFS-Web[1]

Telephone inquiries regarding this matter should be directed to undersigned at (571) 272-1058.

/Angela Walker/
Angela Walker
Paralegal Specialist
Office of Petitions

[1] www.uspto.gov/ebc/efs_help.html (for help using EFS-Web call the Patent Electronic Business Center at (866) 217-9197)

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD.01.01.DV7

CONFIRMATION NO. 6907

40672
BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380

PUBLICATION NOTICE

OC000000122504813

Title:SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

Publication No.US-2021-0005716-A1
Publication Date:01/07/2021

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

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Sale Item Reference Number	Effective Date
16947294	09/28/2020

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I202005B53483009	1599	MAINTENANCE/PETITION INTERNAL FEE CODE	$3,135.00	Credit Card

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16947294
Filing Date	2020-07-27
First Named Inventor	G.R. Mohan Rao
Art Unit	2892
Examiner Name	NA
Attorney Docket Number	GRTD.01.01.DV7

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4001864	A	1997-01-04	Gibbons	
	2	4160985	A	1979-07-10	Kamins et al.	
	3	4347654	A	1982-09-07	Allen et al.	
	4	4481522	A	1984-11-06	Jastrzebski et al.	
	5	4866000	A	1989-09-12	Okita	
	6	5029277	A	1991-07-02	Kane	
	7	5130262	A	1992-07-14	Masquelier et al.	
	8	5213988	A	1993-05-25	Yamauchi et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	NA
	Attorney Docket Number	GRTD.01.01.DV7

	9	5262345	A	1993-11-16	Nasser et al.	
	10	5329144	A	1994-07-12	Luryi	
	11	5448087	A	1995-09-05	Streit et al.	
	12	5480816	A	1996-01-02	Uga et al.	
	13	5496746	A	1996-03-05	Matthews	
	14	5517052	A	1996-05-14	Ishaque	
	15	5569612	A	1996-10-29	Frisina et al.	
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	17	5637898	A	1997-06-10	Baliga	
	18	5797999	A	1998-08-25	Sannomiya et al.	
	19	5888857	A	1999-03-30	Zhang et al.	

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	Examiner Name	NA
	Attorney Docket Number	GRTD.01.01.DV7

	20	5973575	A	1999-10-26	Kamogawa et al.	
	21	6211028	B1	2001-04-03	Tsai et al.	
	22	6310366	B1	2001-10-30	Rhodes et al.	
	23	RE37441	E	2001-11-13	Yamazaki	
	24	6452086	B1	2002-09-17	Muller	
	25	6465862	B1	2002-10-15	Harris	
	26	6472715	B1	2002-10-29	Liu et al.	
	27	6670544	B2	2003-12-30	Kibbel et al	
	28	6683343	B2	2004-01-27	Matsudai et al.	
	29	6696314	B2	2004-02-24	Rhodes	
	30	6706550	B2	2004-03-16	Lee et al.	

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	Examiner Name	NA
	Attorney Docket Number	GRTD.01.01.DV7

	31	6713813	B2	2004-03-30	Marchant	
	32	6720622	B1	2004-04-13	Yu	
	33	6737722	B2	2004-05-18	Yamamoto et al.	
	34	6744117	B2	2004-06-01	Dragon et al.	
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	36	6753202	B2	2004-06-22	Chen et al.	
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	38	6756616	B2	2004-06-29	Rhodes	
	39	6780713	B2	2004-08-24	Bromberger et al.	
	40	6831292	B2	2004-12-14	Currie et al.	
	41	6878603	B2	2005-04-12	Bromberger et al.	

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	Examiner Name	NA
	Attorney Docket Number	GRTD.01.01.DV7

	42	6921946	B2	2005-07-26	Kenney et al.	
	43	6933215	B2	2005-08-23	Bromberger et al.	
	44	7064385	B2	2006-06-20	Dudek et al.	
	45	7115925	B2	2006-10-03	Rhodes	
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	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	NA
	Attorney Docket Number	GRTD.01.01.DV7

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	55	4684971	A	1987-08-04	Payne	

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	1	20010040622	A1	2001-11-15	Maruyama	
	2	20020056883	A1	2002-05-16	Baliga	
	3	20020074585	A1	2002-06-20	Tsang et al.	
	4	20020084430	A1	2002-07-04	Bamji et al.	
	5	20020093281	A1	2002-07-18	Cathey	
	6	20020102783	A1	2002-08-01	Fujimoto et al.	

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	Application Number	16947294
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	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	NA
	Attorney Docket Number	GRTD.01.01.DV7

	7	20020134419	A1	2002-09-26	Macris	
	8	20030026126	A1	2003-02-06	Uemura	
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	15	20120048462	A1	2013-02-28	Lee	
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	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	NA
	Attorney Docket Number	GRTD.01.01.DV7

	18	20030183856	A1	2003-10-02	Wieczorek	
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	1	P.D. Moor, Advanced CMOS-based pixel sensors, https://indico.cern.ch/event/122027/contributions/88236/attachments/69340/99377/FEEimecPdM.pdf, 2011, 41 pages	
	2	E. Parton, CMOS Sensors, Laser Focus World, http://www.laserfocusworld.com/articles/print/volume-49/issue-10/features/cmos-sensors-cmos-based-specialty-imagers-reach-new-performance-levels.html, Oct. 14, 2013, 5 pages	
	3	Z. Cao, Design of Pixel for High Speed CMOS Image Sensors, http://www.imagesensors.org/Past%20Workshops/2013%20Workshop/2013%20Papers/07-11_072-Cao_papers.pdf, 4 pages	
	4	M. Tanenbaum, BSTJ: Diffused Emitter and Base Silicon Transisters, The Bell System Technical Journal, Jan. 1956, 22 pages, vol. XXXV, https://archive.org/details/bstj35-1-1	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16947294
	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	NA
	Attorney Docket Number	GRTD.01.01.DV7

	5	IMEC Image Sensors and Vision Systems, http:www2.imec.be/content/user/File/Brochures/cmos%20imagers%20brochure-april26.pdf, Apr. 2014, 2 pages	
	6	A.S. Grove, Physics and Technology of Semiconductor Devices, John Wiley Sons, Inc., New York, Nov. 1967.	
	7	W. Murray Bullis and W. R. Runyan, Influence of Mobility and Lifetime Variations on Drift-Field Effects in Silicon-Junction Devices, IEEE Transactions on Electron Devices, vol. Ed-14, No. 2, Feb. 1967	
	8	Berinder Brar et al., Herb's Bipolar Transistors, IEEE Transactions on Electron Devices, vol. 48, No. 11, Nov. 2001	

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16947294
	Filing Date	2020-07-27
	First Named Inventor	G.R. Mohan Rao
	Art Unit	2892
	Examiner Name	NA
	Attorney Docket Number	GRTD.01.01.DV7

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Bill R. Naifeh, Reg. No. 44962/	Date (YYYY-MM-DD)	2020-09-29
Name/Print	Bill R. Naifeh	Registration Number	44962

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

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EFS ID:	40710276
Application Number:	16947294
International Application Number:	
Confirmation Number:	6907
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	40672
Filer:	Bill Naifeh/April Reasoner
Filer Authorized By:	Bill Naifeh
Attorney Docket Number:	GRTD.01.01.DV7
Receipt Date:	29-SEP-2020
Filing Date:	27-JUL-2020
Time Stamp:	19:14:47
Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	GRTD-DV7_IDSTransmittal.pdf	27181 1f312cbb6f77ba05029806fa02232cdc5fdf8156	no	2

Warnings:

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2	Information Disclosure Statement (IDS) Form (SB08)	GRTD-DV7_IDS.pdf	1037133 1ab985a09accd3003de06dfb996d83bf703c0a2b	no	11
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	G.R. Mohan Rao	§	Conf. No.	6907
Serial No:	16/947,294	§	Group Art Unit:	2892
Filed:	July 27, 2020	§	Examiner:	NA

For: **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS**

Via EFS

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313.1450

INFORMATION DISCLOSURE STATEMENT (IDS)

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, the attention of the United States Patent and Trademark Office is hereby directed to the references listed on the attached Form PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of the above-identified application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

In accordance with 37 C.F.R. § 1.97(g), the filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made. In accordance with 37 C.F.R. § 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in this Information Disclosure Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

Applicant has not submitted copies of each cited U.S. patent and U.S. patent application in accordance with 37 C.F.R. § 1.98(a)(2).

Applicant has not submitted copies of each cited non-patent literature document listed in the attached Information Disclosure Statement in accordance with 37 C.F.R. 1.98(d). Copies of the non-patent literature documents were submitted to the Office in earlier Application No. 16/717,950, which is relied on for an earlier effective filing date.

This Information Disclosure Statement is made pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office Action on the merits.

It is submitted that the Information Disclosure Statement is in compliance with 37 C.F.R. § 1.98, and the Examiner is respectfully requested to consider the listed references.

Respectfully submitted,

/Bill R. Naifeh, Reg. No. 44,962/

Bill R. Naifeh
Registration No. 44,962

Bill R. Naifeh
Law Office of Bill Naifeh
P.O. Box 803423
Dallas, TX 75380
972-726-9500
214-550-2542 (fax)

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/947,294

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	75		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	330		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	380		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	44 minus 20 =	* 24	x 50 =	1200	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	7 minus 3 =	* 4	x 230 =	920			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	2905		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/947,294	07/27/2020	2812	2985	GRTD.01.01.DV7	44	7

CONFIRMATION NO. 6907

UPDATED FILING RECEIPT

40672
BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380

OC000000120229081

Date Mailed: 09/29/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

G.R. Mohan Rao, Allen, TX;

Applicant(s)

GREENTHREAD, LLC, Dallas, TX;

Power of Attorney: The patent practitioners associated with Customer Number 40672

Domestic Priority data as claimed by applicant

This application is a CON of 16/717,950 12/17/2019 PAT 10734481
which is a CON of 15/590,282 05/09/2017 PAT 10510842
which is a CON of 14/931,636 11/03/2015 PAT 9647070
which is a CON of 14/515,584 10/16/2014 PAT 9190502
which is a CON of 13/854,319 04/01/2013 ABN
which is a CON of 11/622,496 01/12/2007 PAT 8421195
which is a DIV of 10/934,915 09/03/2004 ABN

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 08/03/2020
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/947,294**
Projected Publication Date: 01/07/2021
Non-Publication Request: No
Early Publication Request: No
**** SMALL ENTITY ****
Title

SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative,

this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

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SEP 28 2020

Customer No. 000040672
Attorney Docket No. GRTD.01.01.DV7

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:	G.R. Mohan Rao	§	Confirmation No.	6907
Serial No:	16/947,294	§	Group Art Unit:	2812
Filed:	July 27, 2020	§	Examiner:	N/A

For: **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS**

2020 OCT -1 PM 12:3

USPTO
RECEIPTS ACCOUNTING
DIVISION

Via Facsimile
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Certificate of Facsimile Transmission
I hereby certify that this correspondence is being submitted to the U.S. Patent Office via facsimile transmission to (571) 273-8300 on September 28, 2020.

/April Reasoner/
April Reasoner, Paralegal

NOTIFICATION OF LOSS OF ENTITILEMENT TO SMALL ENTITY STATUS

Dear Sir:

Applicant hereby notifies the Office of its loss of entitlement to small entity status.

On September 25, 2020, Applicant submitted payment of fees in the amount of $2985 in response to the Notice to File Missing Parts.

Applicant hereby submits payment of the additional fees due in the amount of $3135 as follows:

Basic filing fee	$ 300
Surcharge	$ 160
Search Fee	$ 660
Exam Fee	$ 760
Additional claim fees	$4240
Total Fees	$6120
Amount Paid	- $2985
Total Amount Due	**$3135**

Customer No. 000040672
Attorney Docket No. GRTD.01.01.DV7

Attached is Form PTO-2038 Credit Card Payment Form for payment of the additional fees.

Respectfully submitted,

/Bill R. Naifeh, Reg. No. 44,962/

Registration No. 44,962

Law Office of Bill Naifeh
P.O. Box 803423
Dallas, TX 75380
972-726-9500
214-550-2542 (fax)

1,28

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SEP 28 2020

161

FAX COVER SHEET

TO	USPTO
COMPANY	
FAX NUMBER	15712738300
FROM	Bill Naifeh
DATE	2020-09-29 01:12:06 GMT
RE	Entity Status and Payment of Fees

COVER MESSAGE

Dear Sir:
Attached is a Notification of Loss of Entitlement to Small Entity Status, along with a cc authorization form for payment of the additional fees due.
Regards,
April Reasoner

PAGE 1/4 * RCVD AT 9/28/2020 9:12:23 PM [Eastern Daylight Time] * SVR:W-PTOFAX-001/27 * DNIS:2738300 * CSID:12145502542 * ANI:4803836933 * DURATION (mm-ss):02-35

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:	G.R. Mohan Rao	§	Confirmation No.	6907
Serial No:	16/947,294	§	Group Art Unit:	2812
Filed:	July 27, 2020	§	Examiner:	N/A

For: **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS**

Via EFS
Mail Stop Missing Parts
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

RESPONSE TO NOTICE TO FILE MISSING PARTS

Dear Sir:

In Response to the Notice to File Missing Parts, mailed October 5, 2020, in the above application, Applicant hereby submits payment of the following fees:

Basic filing fee	$ 75
Surcharge	$ 80
Search fee	$ 330
Examination fee	$ 380
Additional claim fees	$2120
Total Filing Fees	$2985

Respectfully submitted,

/Bill R. Naifeh, Reg. No. 44,962/

Bill R. Naifeh
Registration No. 44,962

Law Office of Bill Naifeh
P.O. Box 803423
Dallas, TX 75380
972-726-9500
214-550-2542 (fax)

Electronic Patent Application Fee Transmittal

Application Number:	16947294
Filing Date:	27-Jul-2020
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Filer:	Bill Naifeh/April Reasoner
Attorney Docket Number:	GRTD.01.01.DV7

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY FILING FEE (ELECTRONIC FILING)	4011	1	75	75
UTILITY SEARCH FEE	2111	1	330	330
UTILITY EXAMINATION FEE	2311	1	380	380
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	2202	24	50	1200
INDEPENDENT CLAIMS IN EXCESS OF 3	2201	4	230	920
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
LATE FILING FEE FOR OATH OR DECLARATION	2051	1	80	80
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**2985**

Electronic Acknowledgement Receipt

EFS ID:	40672359
Application Number:	16947294
International Application Number:	
Confirmation Number:	6907
Title of Invention:	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS
First Named Inventor/Applicant Name:	G.R. Mohan Rao
Customer Number:	40672
Filer:	Bill Naifeh/April Reasoner
Filer Authorized By:	Bill Naifeh
Attorney Docket Number:	GRTD.01.01.DV7
Receipt Date:	25-SEP-2020
Filing Date:	27-JUL-2020
Time Stamp:	14:43:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$2985
RAM confirmation Number	E20209OE43553297
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	GRTD-DV7_PayFees.pdf	239654 6d5cb8bebaf15c7f385591146570e3692a0698df	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	40542 d2a29a44d26086dd0df61801748cf9e5e4dcd744	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	280196		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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COMMISSIONER FOR PATENTS
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ALEXANDRIA VA 22313-1451

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BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380

Courtesy Reminder for
Application Serial No: 16/947,294

Attorney Docket No: GRTD.01.01.DV7
Customer Number: 40672
Date of Electronic Notification: 08/05/2020

This is a courtesy reminder that new correspondence is available for this application. If you have not done so already, please review the correspondence. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:
patents@naifeh.com

To view your correspondence online or update your email addresses, please visit us anytime at **https://ppair-my.uspto.gov/pair/PrivatePair.**
If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov or call 1-866-217-9197.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/947,294

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
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MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
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						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
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	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/947,294	07/27/2020	2812	0.00	GRTD.01.01.DV7	44	7

CONFIRMATION NO. 6907

40672
BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380

FILING RECEIPT

OC000000118944484

Date Mailed: 08/05/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

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Inventor(s)

G.R. Mohan Rao, Allen, TX;

Applicant(s)

GREENTHREAD, LLC, Dallas, TX;

Power of Attorney: The patent practitioners associated with Customer Number 40672

Domestic Priority data as claimed by applicant

This application is a CON of 16/717,950 12/17/2019 PAT 10734481
which is a CON of 15/590,282 05/09/2017 PAT 10510842
which is a CON of 14/931,636 11/03/2015 PAT 9647070
which is a CON of 14/515,584 10/16/2014 PAT 9190502
which is a CON of 13/854,319 04/01/2013 ABN
which is a CON of 11/622,496 01/12/2007 PAT 8421195
which is a DIV of 10/934,915 09/03/2004 ABN

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/947,294**
Projected Publication Date: To Be Determined - pending completion of Missing Parts
Non-Publication Request: No
Early Publication Request: No
**** SMALL ENTITY ****
Title

SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/947,294	07/27/2020	G.R. Mohan Rao	GRTD.01.01.DV7

CONFIRMATION NO. 6907

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FORMALITIES LETTER

OC000000118944485

Date Mailed: 08/05/2020

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Additional claim fees of $ **2120** as a small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. Small entity discount is in effect. If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **75** basic filing fee.
- $ **80** surcharge.
- $ **330** search fee.
- $ **380** examination fee.
- $ **920** for **4** independent claims over 3.
- $ **1200** for **24** total claims over 20.

- $(**0**) previous unapplied payment amount.
- $ **2985** TOTAL FEE BALANCE DUE.

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/ltan/

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Respectfully submitted,

/Bill R. Naifeh, Reg. No. 44,962/

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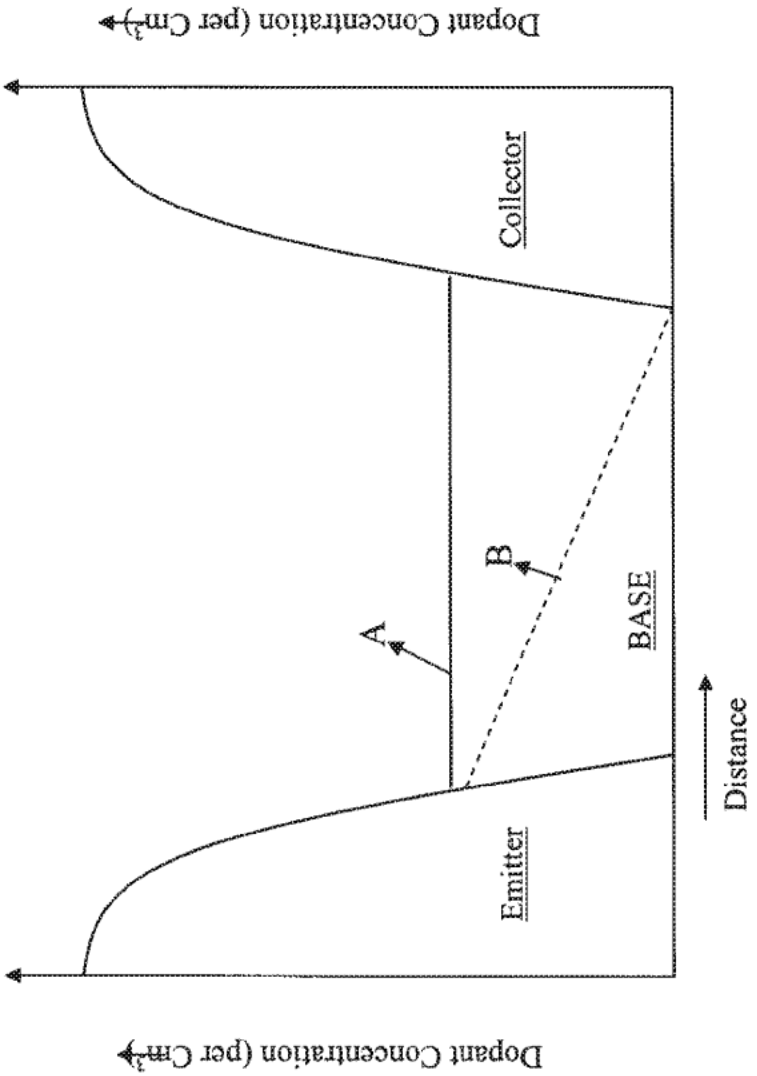

Figure 1 Prior Art

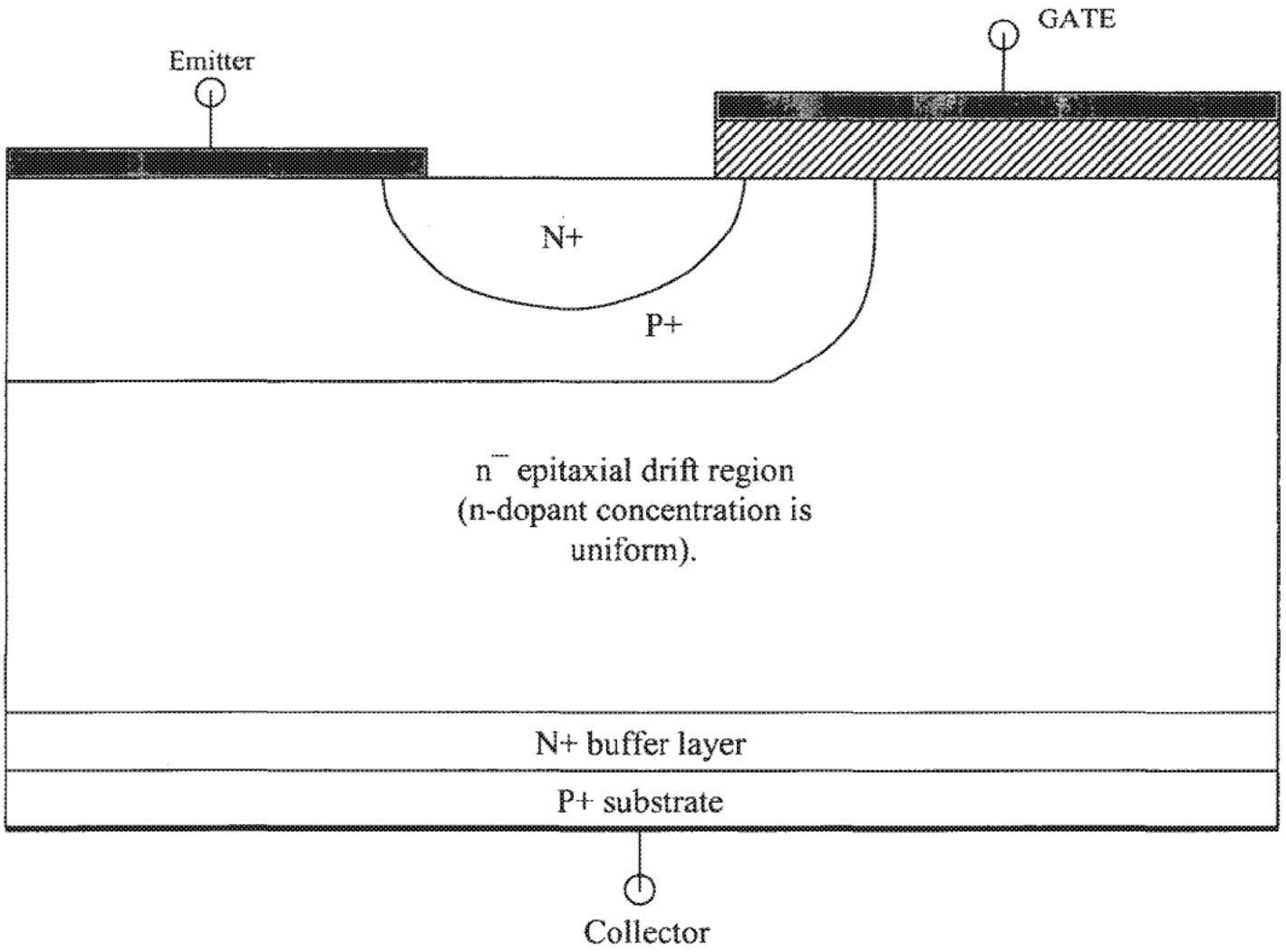

FIGURE 2 Prior art

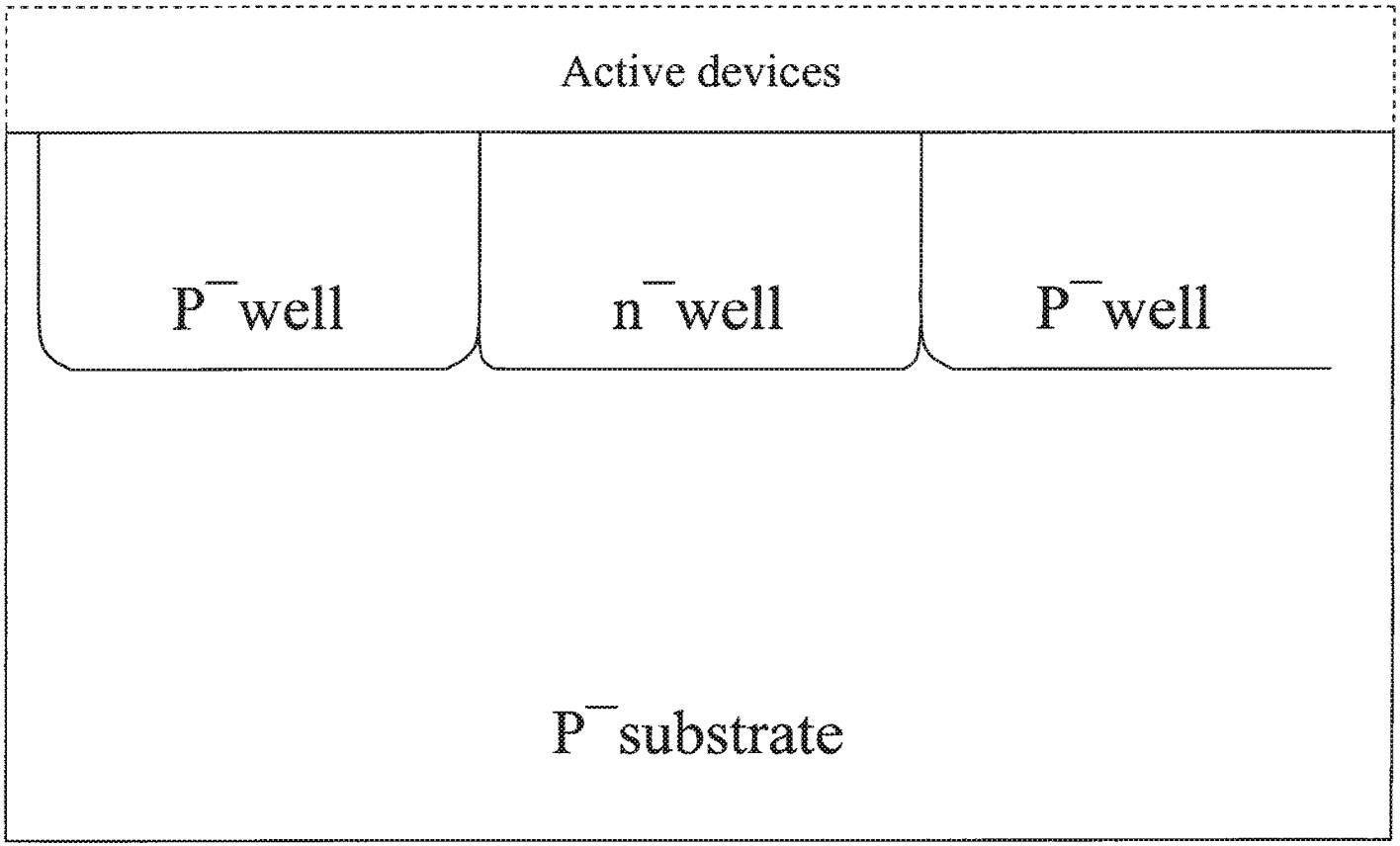

FIGURE 3A Prior art (Twin well CMOS) for a CMOS integrated circuit

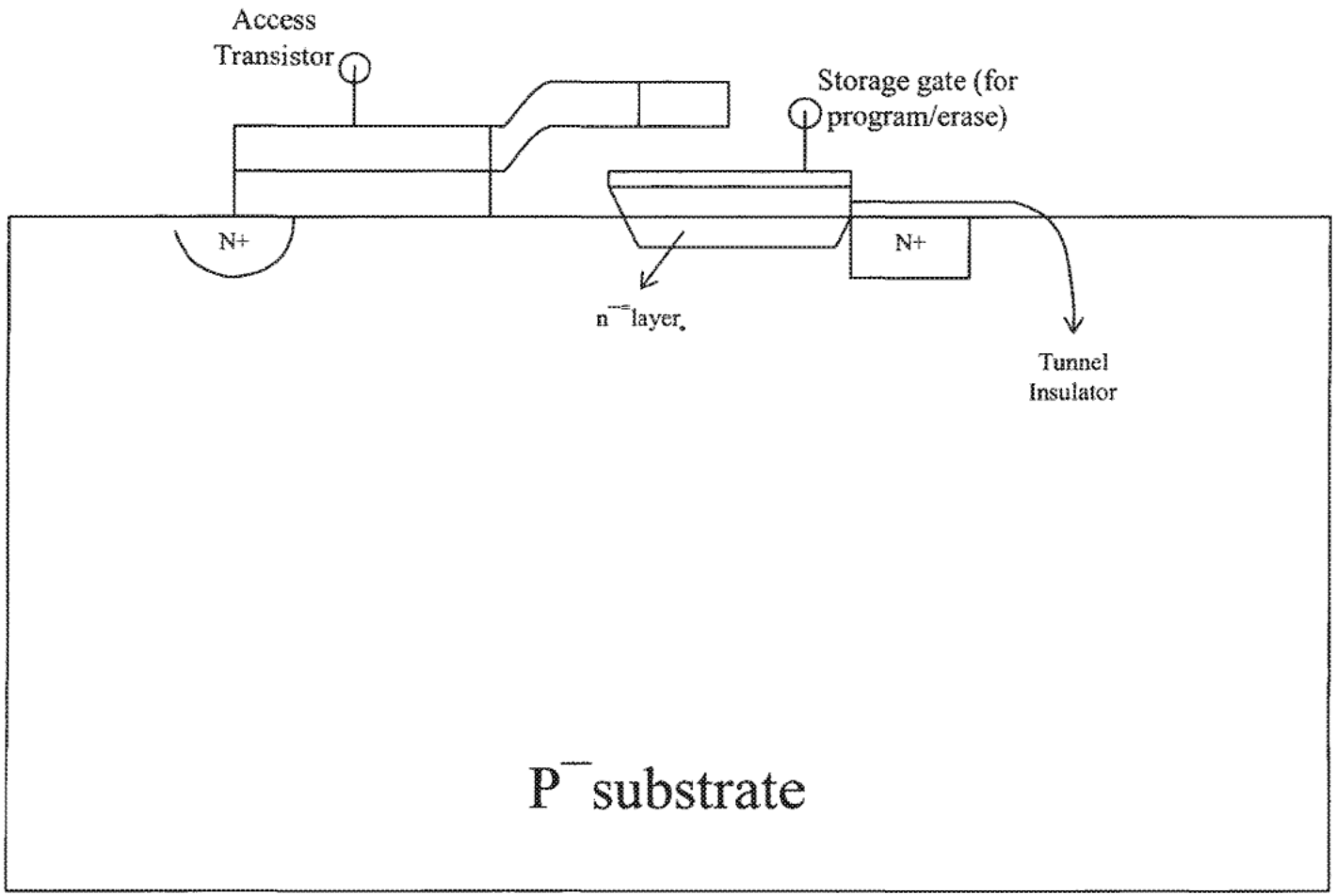

FIGURE 3B Prior art for a two-device EEPROM memory cell

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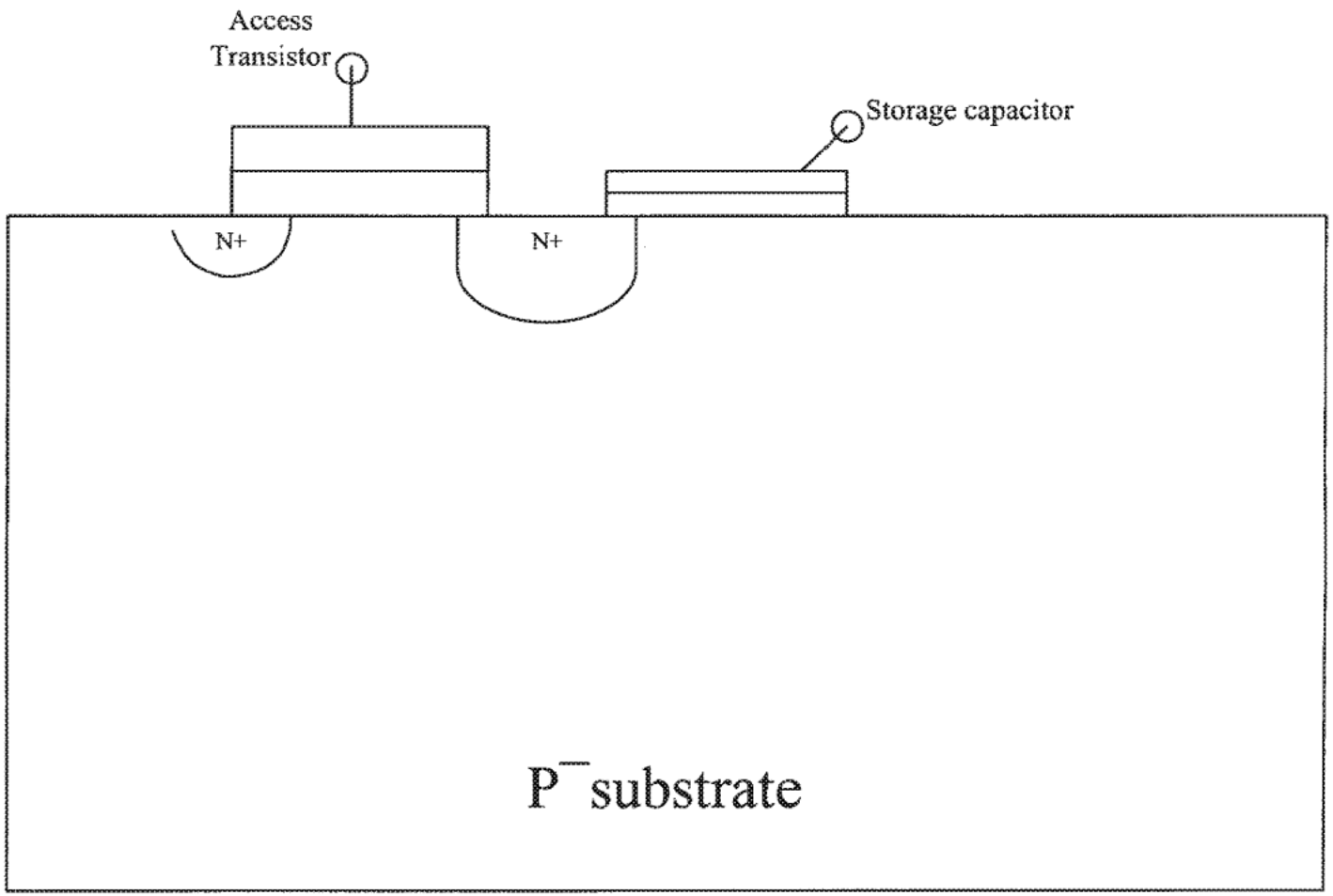

FIGURE 3C Prior art for a 1T-1C DRAM memory cell

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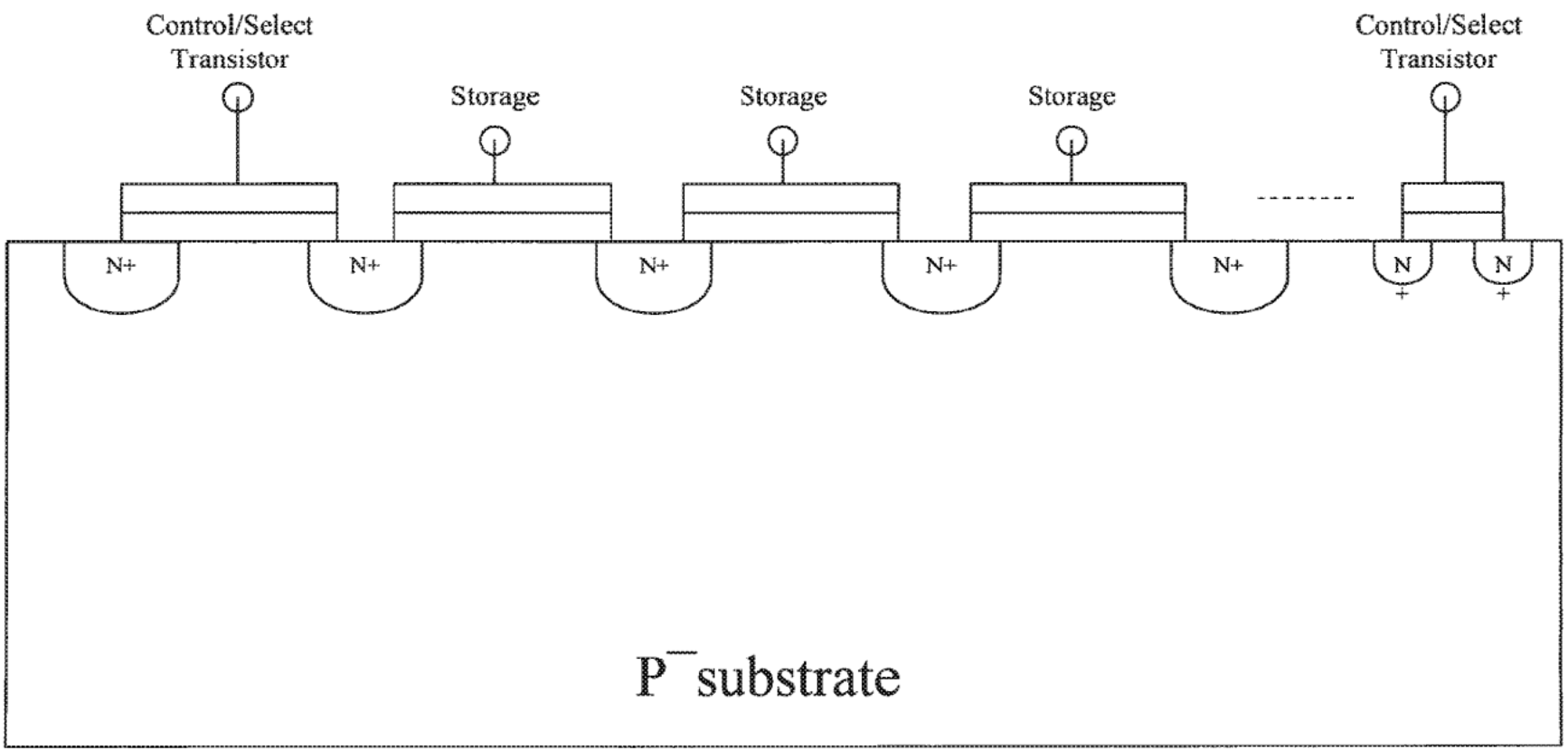

FIGURE 3D Prior art for a NAND flash memory cell

Note: Control/ Sect transistors have a single insulator - traditional MOS transistor.
Storage nodes have a stacked gate structure, typically with a floating gate and control gate comprising the stack.

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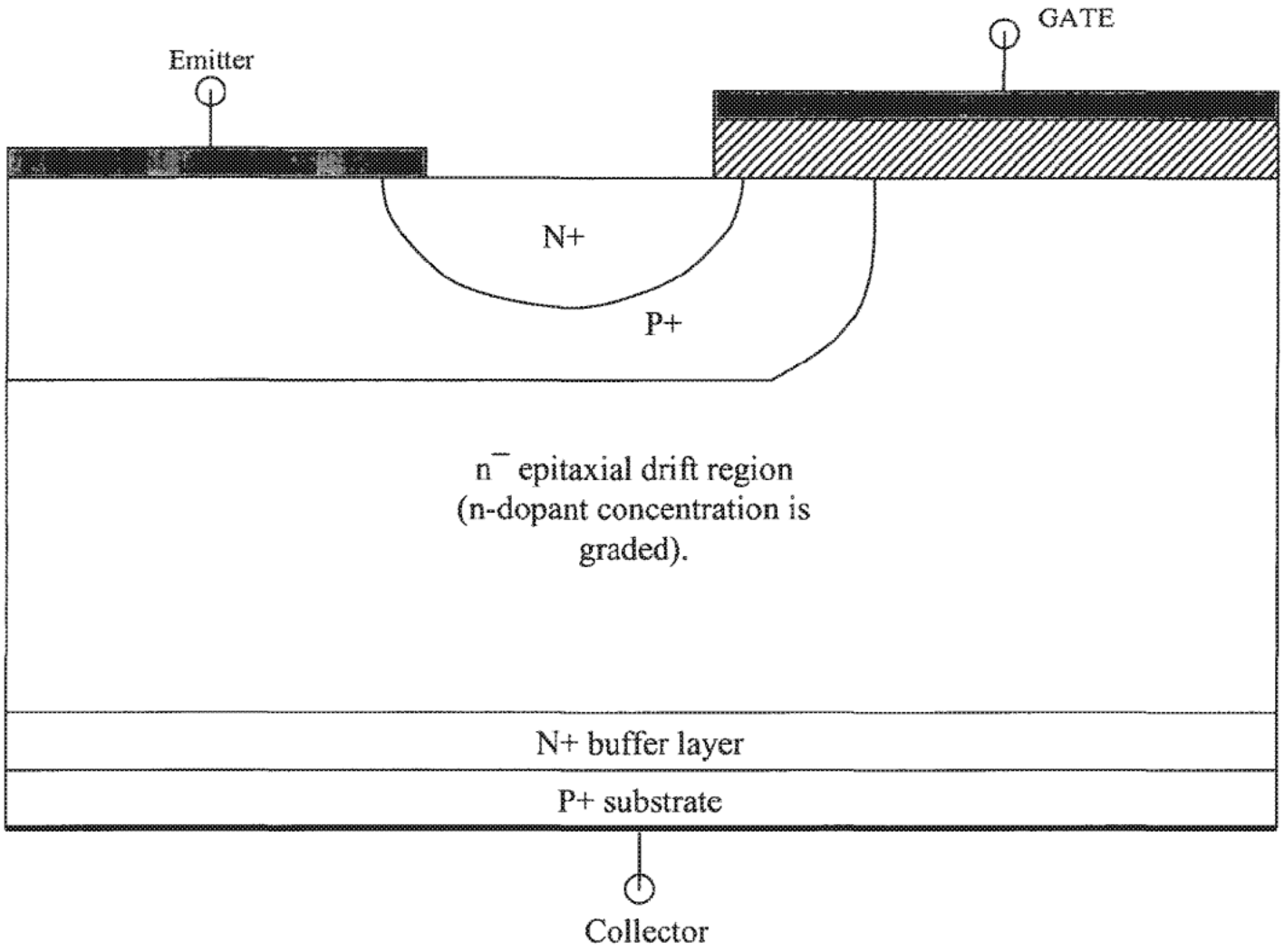

FIGURE 4 A dopant - concentration grinded drift region in a IGBT

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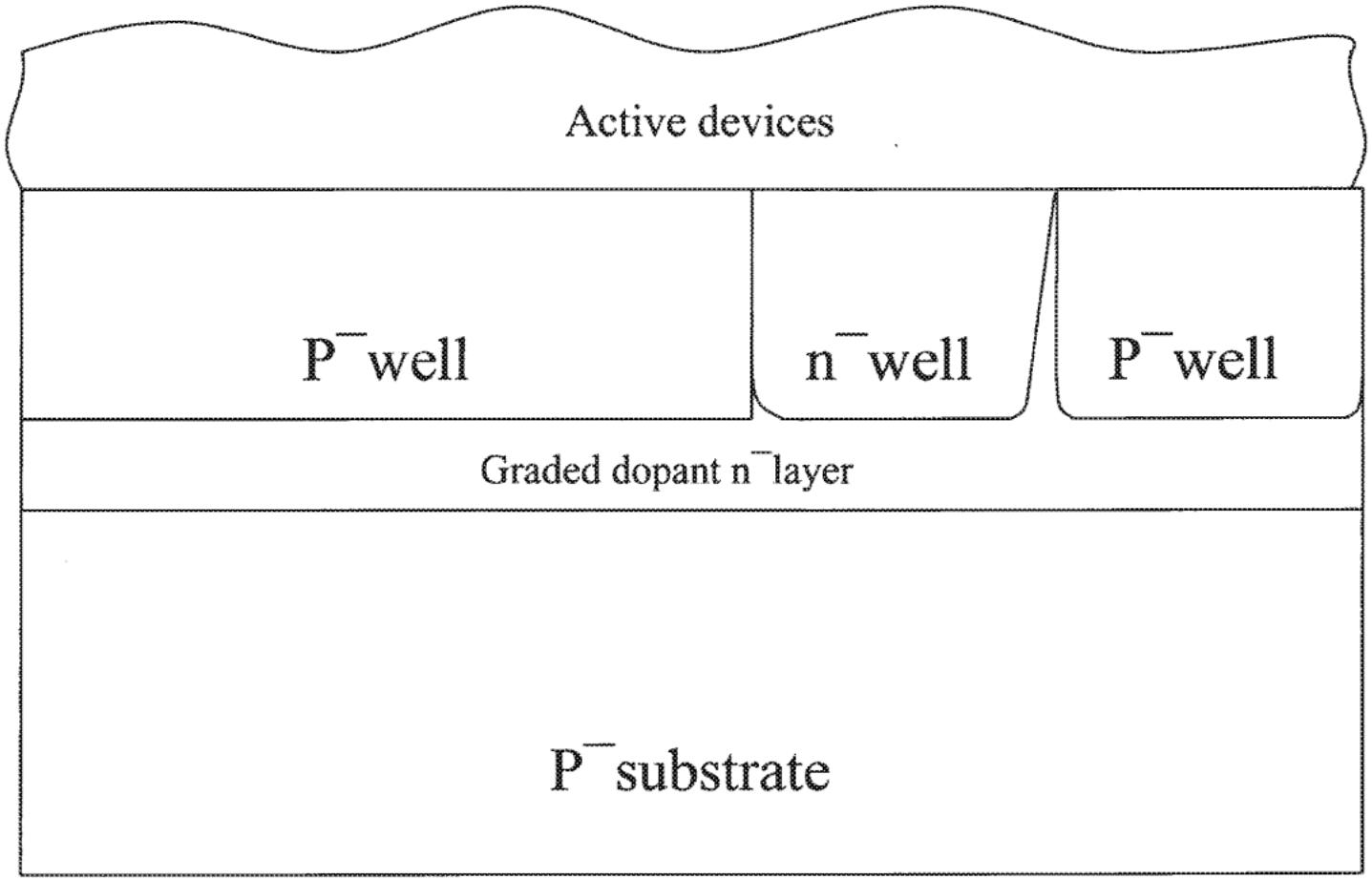

FIGURE 5A A CMOS Substrate for digital, mixed, signal, and senors IC's

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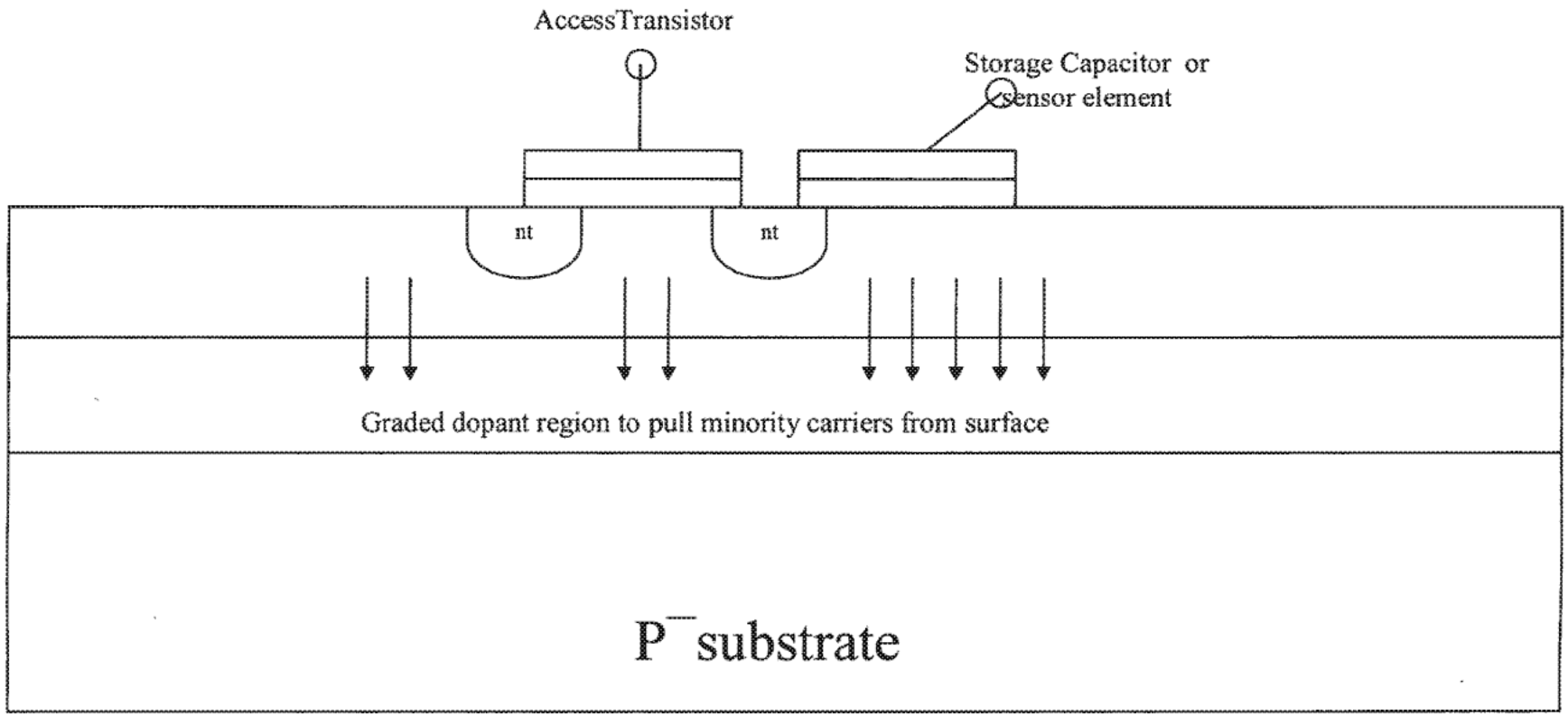

FIGURE 5B CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

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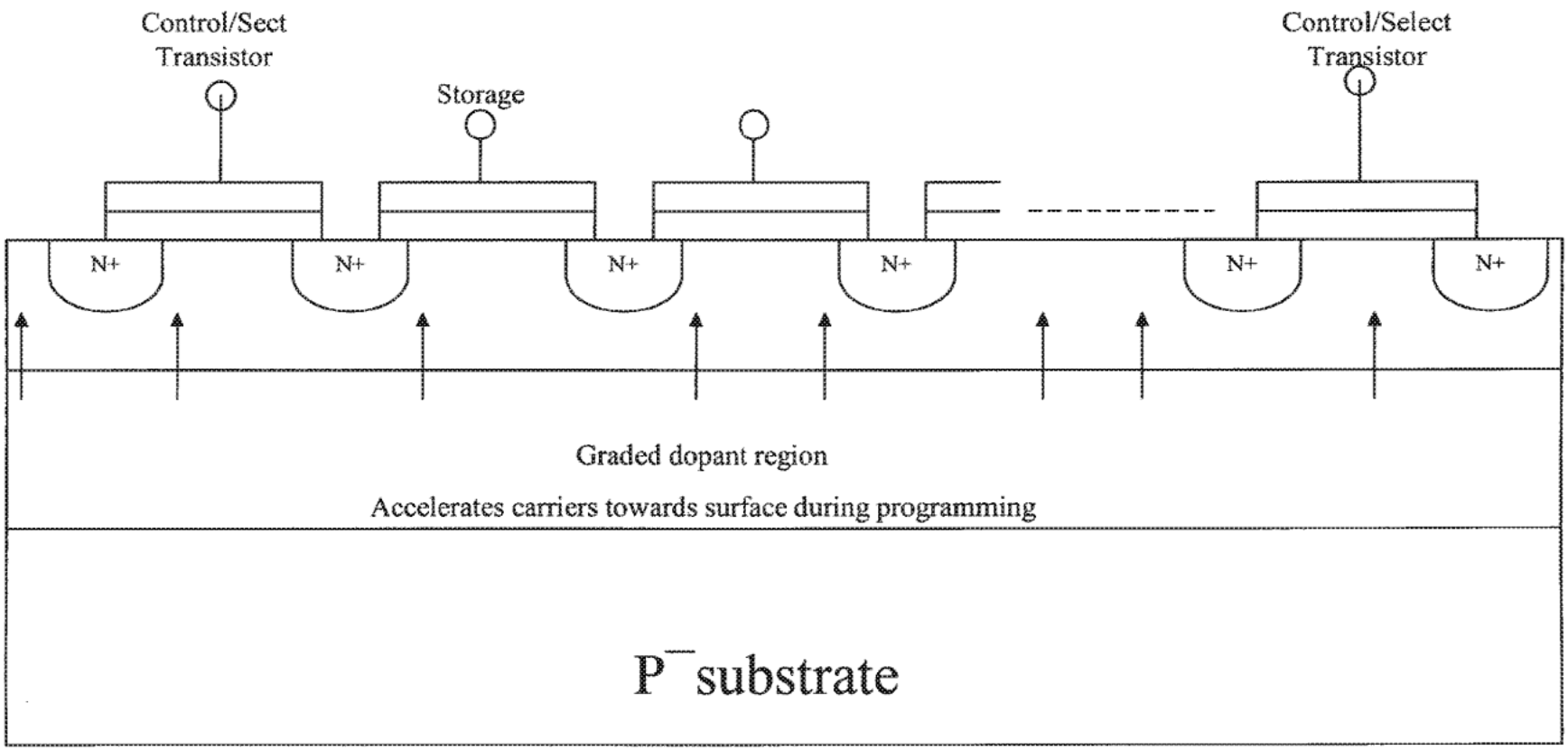

FIGURE 5C CMOS Substrate for a NAND flash device to improve programming times

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SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation of U.S. Patent Application No. 16/717,950, filed December 17, 2019, which this a Continuation of U.S. Patent Application No. 15/590,282, filed May 9, 2017, which is a Continuation of U.S. Patent Application No. 14/931,636, filed November 3, 2015, which is Continuation of U.S. Patent Application No. 14/515,584, filed October 16, 2014, which is a Continuation of U.S. Patent Application No. 13/854,319 filed April 1, 2013, which is a Continuation of 11/622,496, filed January 12, 2007, which is a Divisional of U.S. Patent Application No. 10/934,915, filed September 3, 2004. The disclosures of which are incorporated herein by reference in their entirety.

TECHNICAL FIELD

[0002] This present invention relates to all semiconductor devices and systems. Particularly it applies to diffused diodes, avalanche diodes, Schottky devices, power MOS transistors, JFET's, RF bipolar transistors, IGBTs (Insulated Gate Bipolar Transistors), varactors, digital VLSI, mixed signal circuits and sensor devices including camera ICs employing CCD (Charge Coupled Device) as well as CMOS technologies.

BACKGROUND

[0003] Bipolar Junction Transistors (BJT) are classified as minority carrier devices because minority carriers are the principle device conduction mechanism. However, majority carriers also play a small but finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. The carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT's (Insulated Gated Base Transistors), still use a uniformly doped 'drift epitaxial' region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the uniformly doped epi region in an IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the sidewalls in a vertical device. Other device architectures to combine planar and vertical conductions are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and hole recombination as fast as possible in n-channel IGBT) necessitate different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

[0004] Retrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits. FIG. 3A shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are

subsequently fabricated. FIGS. 3B, 3C, and 3D illustrate device cross sections, as practiced today. Retrograde and halo wells have also been attempted to improve refresh time in DRAMs (dynamic random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0006] FIG. 1 illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base ("A") and graded base ("B");

[0007] FIG. 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base);

[0008] FIGS. 3A, 3B, 3C, and 3D illustrate cross sections of commonly used prior art CMOS silicon substrates; FIG. 3A showing a typical prior art IC with two wells (one n^- well in which p-channel transistors are subsequently fabricated and one p^-well in which n-channel transistors are subsequently fabricated); FIG 3B showing a prior art EEPROM (Electronically Erasable Programmable Read-Only Memory) memory cell having a tunnel insulator; FIG. 3C showing a prior art DRAM memory cell; and FIG. 3D showing a prior art NAND flash memory cell;

[0009] FIG. 4 illustrates the cross section of an IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

[0010] FIGS. 5A, 5B, and 5C illustrate the cross sections of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention to improve performance in each application—VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION

[0011] The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/cm^3$, whereas the base region is 10^{14} to $10^{16}/cm^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100× at the emitter-base junction, relative to the base-collector junction (1×). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift electric field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped (base) BJT. The improvement in cut-off frequency (or, frequency at unity gain, f_T) can be as large as 2×-5×. Similar performance improvements are also applicable to n-p-n transistors.

[0012] As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region—n^+ buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The "average" base resistance is optimized so that conductivity modulation and lifetime (for minority carriers) in the base region are not compromised. By sweeping the carriers towards the n^+ buffer region a number of advantages are obtained. First, the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. Second, and maybe more importantly, during t_{off}, holes can be recombined much quicker at the n^+ buffer layer, compared to the uniformly doped n^-epitaxial drift region by establishing a different dopant gradient near the n^+ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Although epitaxy enhances lifetime, it is not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The "reverse recovery time" for an IGBT is significantly improved due to the optimized graded dopant in the so called "drift region" as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n^+ buffer

layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n^+ buffer layer. This can improve t_{on} and t_{off} in the same device.

[0013] As illustrated in FIGS. 5A, 5B, and 5C, donor gradient is also of benefit to very large scale integrated circuits (VLSI)—VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory ICs. These unwanted carriers can discharge dynamically-held "actively held high" nodes. In most cases, statically-held nodes (with V_{cc}) cannot be affected. Degradation of refresh time in DRAMs is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images in digital imaging ICs is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging ICs with the embodiments described herein. Creating "subterranean" recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique is described herein which creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible. In a preferred embodiment, the subterranean n^- layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar "transfer" mechanisms. This n^-layer can be a deeply-implanted layer. It can also be an epitaxial layer. As desired, the n^-well and p^-wells can also be graded or retrograded in dopants to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. To decrease programming time in nonvolatile memory devices, carriers should be accelerated towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction Field-Effect transistors where the "channel pinch-off" is controlled by a graded channel instead of a uniformly doped channel (as practiced in the prior art).

[0014] One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single-well, and triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below.

[0015] Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

[0016] It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

WHAT IS CLAIMED IS:

1. A VLSI semiconductor device, comprising:

a substrate of a first doping type at a first doping level having a surface;

a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region;

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and

at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

2. The VLSI semiconductor device of Claim 1, wherein the substrate is a p-type substrate.

3. The VLSI semiconductor device of Claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

4. The VLSI semiconductor device of Claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices.

5. The VLSI semiconductor device of Claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

6. The VLSI semiconductor device of Claim 1, wherein the first active region and second active region are each separated by at least one isolation region.

7. The VLSI semiconductor device of Claim 1, wherein the graded dopant is fabricated with an ion implantation process.

8. The VLSI semiconductor device of Claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.

9. The VLSI semiconductor device of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.

10. The VLSI semiconductor device of Claim 1, wherein dopants of the graded dopant concentration in the first active region are both p-type and n-type.

11. The VLSI semiconductor device of Claim 1, wherein dopants of the graded dopant concentration in the second active region are both p-type and n-type.

12. The VLSI semiconductor device of Claim 1, wherein dopants of the graded dopant region in the well region are both p-type and n-type.

13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.

14. The VLSI semiconductor device of Claim 1, wherein the device is a dynamic random access memory (DRAM).

15. The VLSI semiconductor device of Claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.

16. The VLSI semiconductor device of Claim 1, wherein the device is a flash memory.

17. The VLSI semiconductor device of Claim 1, wherein the device comprises digital logic and capacitors.

18. The VLSI semiconductor device of Claim 1, wherein the device is central processing unit.

19. The VLSI semiconductor device of Claim 1, wherein the device is an image sensor.

20. The VLSI semiconductor device of Claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.

21. A VLSI semiconductor device, comprising:

a substrate of a first doping type at a first doping level having a surface;

a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;

transistors formed in at least one of the first active region or second active region;

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and

at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no

active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.

22. The VLSI semiconductor device of Claim 21, wherein the substrate is an n-type substrate.

23. The VLSI semiconductor device of Claim 21, wherein the substrate is a p-type substrate.

24. The VLSI semiconductor device of Claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

25. The VLSI semiconductor device of Claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.

26. The VLSI semiconductor device of Claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

27. The VLSI semiconductor device of Claim 21, wherein the first active region and second active region are each separated by at least one isolation region.

28. The VLSI semiconductor device of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.

29. The VLSI semiconductor device of Claim 21, wherein dopants of the graded dopant concentration in the first active region are both p-type and n-type.

30. The VLSI semiconductor device of Claim 21, wherein dopants of the graded dopant concentration in the second active region are both p-type and n-type.

31. The VLSI semiconductor device of Claim 21, wherein dopants of the graded dopant region in the well region are both p-type and n-type.

32. The VLSI semiconductor device of Claim 21, wherein the graded dopant is fabricated with an ion implantation process.

33. The VLSI semiconductor device of Claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.

34. The VLSI semiconductor device of Claim 21, wherein the device is a flash memory.

35. The VLSI semiconductor device of Claim 21, wherein the device is a logic device with capacitors in at least some of the first or second active regions.

36. The VLSI semiconductor device of Claim 21, wherein the device is central processing unit.

37. The VLSI semiconductor device of Claim 21, wherein the device is an image sensor.

38. The VLSI semiconductor device of Claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.

39. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level;

a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.

41. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level;

a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

42. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level;

a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

43. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level;

a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded acceptor dopant concentration and one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

44. A CMOS Semiconductor device comprising:

a surface layer;

a substrate;

an active region including a source and a drain, disposed on one surface of the surface layer;

a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from

the surface layer to an area of the substrate where there are no active regions; and

at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.

ABSTRACT

Most semiconductor devices manufactured today, have uniform dopant concentration, either in the lateral or vertical device active (and isolation) regions. By grading the dopant concentration, the performance in various semiconductor devices can be significantly improved. Performance improvements can be obtained in application specific areas like increase in frequency of operation for digital logic, various power MOSFET and IGBT ICs, improvement in refresh time for DRAMs, decrease in programming time for nonvolatile memory, better visual quality including pixel resolution and color sensitivity for imaging ICs, better sensitivity for varactors in tunable filters, higher drive capabilities for JFETs, and a host of other applications.

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [x] The attached application, or
- [ ] United States application or PCT international application number _____

filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: G.R. Mohan Rao Date (Optional): Sept 30, 2015

Signature: G R Mohan Rao

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Doc Code: PA..
Document Description: Power of Attorney

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

[X] I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: **40672**

OR

[ ] I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

[X] The address associated with the above-mentioned Customer Number

OR

[ ] The address associated with Customer Number:

OR

[ ] Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

GREENTHREAD, LLC

[ ] Inventor or Joint Inventor (title not required below)
[ ] Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)
[X] Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)
[ ] Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Philip W. John Jr.	Date (Optional)	3/20/2020
Name	Philip W. John, Jr.		
Title	PRESIDENT		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

[ ] Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

AFFIRMATIVE RECESSION OF PREVIOUS DISCLAIMER

This Application is a continuation or continuation-in-part of previous applications and patents.

Except as explicitly set forth in the prosecution of this application, to the extent any amendments, characterizations, or other assertions made (in this or in any related patent applications or patents, including any parent, sibling, or child) with respect to any art, prior or otherwise, could be construed as a disclaimer of any subject matter supported by the present disclosure of this application, Applicant hereby rescinds and retracts such disclaimer. Applicant also respectfully submits that any prior art considered in any related patent applications or patents, including any parent, sibling, or child, may need to be re-visited.

New claims in this Application may be broader than the claims previously allowed in parent or related applications.

Respectfully submitted,

/Bill R. Naifeh, Reg. No. 44,962/

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	GRTD.01.01.DV7
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	G.R. Mohan		Rao	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Allen	State/Province	TX	Country of Residence	US

Mailing Address of Inventor:

Address 1	1611 Willingham Drive
Address 2	

City	Allen	State/Province	TX
Postal Code	72013	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	40672		
Email Address	patents@naifeh.com	Add Email	Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS		
Attorney Docket Number	GRTD.01.01.DV7	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	10	Suggested Figure for Publication (if any)	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	GRTD.01.01.DV7
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	40672		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	16717950	2019-12-17

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	GRTD.01.01.DV7
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS	

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16717950	Continuation of	15590282	2017-05-09	10510842	2019-11-26

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15590282	Continuation of	14931636	2015-11-03	9647070	2017-05-09

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14931636	Continuation of	14515584	2014-10-16	9190502	2015-11-17

Prior Application Status	Abandoned	Remove

Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14515584	Continuation of	13854319	2013-04-01

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13854319	Continuation of	11622496	2007-01-12	8421195	2013-04-16

Prior Application Status	Abandoned	Remove

Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
11622496	Division of	10934915	2004-09-03

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	GRTD.01.01.DV7
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS	

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	GRTD.01.01.DV7
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	GRTD.01.01.DV7
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	GREENTHREAD, LLC		
Mailing Address Information For Applicant:			
Address 1	4544 Harrys Lane		
Address 2			
City	Dallas	**State/Province**	TX
Country	US	Postal Code	75229
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	GRTD.01.01.DV7
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Bill R. Naifeh, Reg No. 44962/			Date (YYYY-MM-DD)	2020-07-27
First Name	Bill R.	Last Name	Naifeh	Registration Number	44962

Additional Signature may be generated within this form by selecting the Add button. Add

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	GRTD.01.01.DV7
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/947,294	07/27/2020 08:36:19 PM ET	GRTD.01.01.DV7

Title of Invention

SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	6907	FILED BY	April Reasoner
PATENT CENTER #	60059993	FILING DATE	-
CUSTOMER #	40672	FIRST NAMED INVENTOR	G.R. Mohan Rao
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Bill Naifeh

Documents

TOTAL DOCUMENTS: 9

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
03_Drawings.pdf	10	Drawings-only black and white line drawings	480 KB
04_Declaration.pdf	1	Oath or Declaration filed	100 KB
05_POA-Greenthread.pdf	1	Power of Attorney	2920 KB
07_RecessionDisclaimer.pdf	1	Miscellaneous Incoming Letter	97 KB
01_ADS.pdf	9	Application Data Sheet	1227 KB
02_ContinuationAppDV7.pdf	16	-	1931 KB
02_ContinuationAppDV7- (1-7)	7	Specification	905 KB

SPEC.pdf				
02_ContinuationAppDV7-CLM.pdf	(8-15)	8	Claims	811 KB
02_ContinuationAppDV7-ABST.pdf	(16-16)	1	Abstract	58 KB
06_EmailAuthorization.pdf		1	Internet Communications Authorized	62 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
03_Drawings.pdf	9FD58A577F2B804E7ABDF350855AEE2845B9635BBEB3A3238800A120DC4CD3E25E19259D7C224B7170C0DF3157ABFCBAA3C687569E21013DF63B2903CBB00495
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06_EmailAuthorization.pdf	C087053DDA153A6AD99D8DD2C066D62F9D002C8A9F2CE2D3 683B00A585EC5B450A6B18805E854F877CA7DF35FEE8CFE0E 8FA1C2F3FF0179EF8D649D1798359CE

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.