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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BMW OF NORTH AMERICA, LLC,
Petitioner,

v.

STRAGENT, LLC,
Patent Owner.

Case No. IPR2023-00333
U.S. Patent No. 11,188,400

**PETITION FOR INTER PARTES REVIEW
OF U.S. PATENT NO. 11,188,400**

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Ex-1001	U.S. Patent No. 11,188,400 to Axel Fuchs, et al. (“the ’400 patent”).
Ex-1002	Prosecution History of the ’400 patent.
Ex-1003	Declaration of Dr. Vijay Madiseti, Ph.D.
Ex-1004	U.S. Provisional Patent Application No. 60/434,018.
Ex-1005	U.S. Patent Application Publication No. 2003/0223436 A1 to Lohrmann et al. (“ <i>Lohrmann</i> ”).
Ex-1006	U.S. Patent No. 6,625,169 to Tofano (“ <i>Tofano</i> ”).
Ex-1007	U.S. Patent No. 5,202,887 to Ueno et al. (“ <i>Ueno</i> ”).
Ex-1008	U.S. Patent Application Publication No. 2002/0073243 A1 to Staiger (“ <i>Staiger</i> ”).
Ex-1009	U.S. Patent No. 6,141,710 to Miesterfeld (“ <i>Miesterfeld</i> ”).
Ex-1010	Stewart et. Al., “ <i>Integration of Real-Time Software Modules for Reconfigurable Sensor-Based Control Systems</i> ,” IEEE/RSJ International Conference on Intelligent Robots and Systems, Raleigh, North Carolina (July 1992) (“ <i>Stewart</i> ”).
Ex-1011	H-C. von der <i>Wense</i> et al., “Building Automotive LIN Applications,” <i>Advanced Microsystems for Automotive Applications</i> , 280-292 (2001) (“ <i>Wense</i> ”).
Ex-1012	U.S. Patent No. 6,434,459 to Wong et al. (“ <i>Wong</i> ”).
Ex-1013	U.S. Patent No. 6,954,463 to Ma (“ <i>Ma</i> ”).
Ex-1014	Nick Grattan and Marshall Brian, “ <i>Windows CE 3.0 Application Programming</i> ,” (Prentice Hall PTR) (First Ed., 2000).

Exhibit	Description
Ex-1015	The Ohio State University Libraries MARC Record for H-C. von der Wense et al., “ <i>Building Automotive LIN Applications</i> ,” Advanced Microsystems for Automotive Applications, 280-292 (2001).
Ex-1016	IPR2017-00457, Paper 34 (Final Written Decision) (P.T.A.B. June 13, 2018).
Ex-1017	IPR2017-00458 Paper 31 (Final Written Decision) (P.T.A.B. June 13, 2018).
Ex-1018	IPR2017-01502, Paper 24 (Final Written Decision) (P.T.A.B. Dec. 6, 2018).
Ex-1019	International Organization for Standardization 11898-1, First Edition (Dec. 1, 2003).
Ex-1020	U.S. Patent Application Publication No. 2003/0043739 A1 to Reinold et al.
Ex-1021	U.S. Patent No. 6,934,612 to Remboski et al.
Ex-1022	U.S. Patent No. 7,480,312 to Ossman.
Ex-1023	IPR2021-00417, Paper 29 (Final Written Decision) (P.T.A.B. July 12, 2022).
Ex-1024	MARC Record for Stewart et. al., “Integration of Real-Time Software Modules for Reconfigurable Sensor-Based Control Systems,” IEEE/RSJ International Conference on Intelligent Robots and Systems, Raleigh, North Carolina (July 1992)
Ex-1025	IPR2021-00417, Paper 13 (Patent Owner’s Response) (P.T.A.B. October 12, 2021).
Ex-1026	IPR2021-00417, Paper 19 (Patent Owner’s Sur-Reply) (P.T.A.B. February 28, 2022).

Exhibit	Description
Ex-1027	IPR2017-00676, Paper 11 (Patent Owner’s Response) (P.T.A.B. September 21, 2017).
Ex-1028	IPR2017-01502, Paper 10 (Patent Owner’s Response) (P.T.A.B. March 12, 2018).
Ex-1029	The Foundation Fieldbus Primer, Fieldbus, Inc. (Rev. 1.1, Jun. 24, 2001).
Ex-1030	Ralf Hadelers and Hans-Jörg Mathony, “ <i>Design of Intelligent Body Networks</i> ,” (SAE International) (2000).
Ex-1031	Chuck Powers and Randy Frank, “ <i>The Consumerization of the Automotive Environment: The ITS Data Bus</i> ,” (SAE International) (1997).
Ex-1032	Bruce D. Emaus, “ <i>Current Vehicle Network Architecture Trends – 2000</i> ,” (SAE International) (2000).

I. Introduction

BMW of North America, LLC (“Petitioner”) requests *inter partes* review and cancellation of claims 1-33 of U.S. Patent No. 11,188,400 (the “’400 Patent”) based on the following grounds:

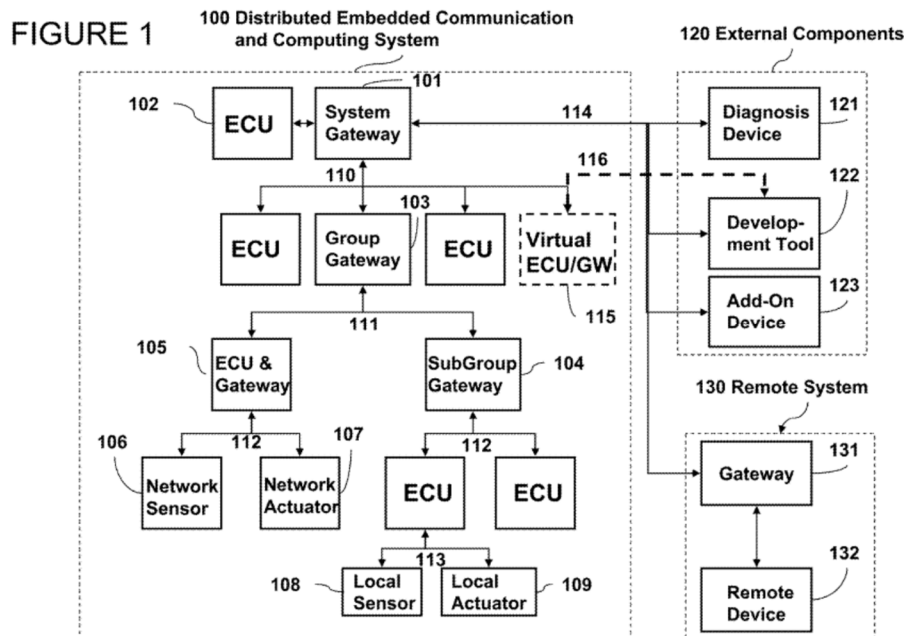
Ground	Claim(s) Challenged	35 USC §	References
1	1-33	103	<i>Lohrmann, Tofano, Ueno, and Staiger</i>
2	1-7 and 27-33	103	<i>Miesterfeld, Wong, Stewart, and Wense</i>
3	8-26	103	<i>Miesterfeld, Wong, Stewart, Wense, and Ma</i>

II. The ’400 Patent

A. Overview

The ’400 patent describes systems and methods “for sharing information in a distributed framework.” Ex-1001, title, 1:37-38. In automobiles, electronic control units (“ECUs”) control applications such as the engine, brakes, or diagnostics through connections to sensors and actuators organized into separate subnetworks. *Id.*, 3:22-25. FIG. 1 shows gateways 101, 103, 104, 105, which relay messages

through system layers. *Id.*, 3:34-36. Each layer may contain multiple ECUs connected through wired serial multiplexing bus systems. *Id.*

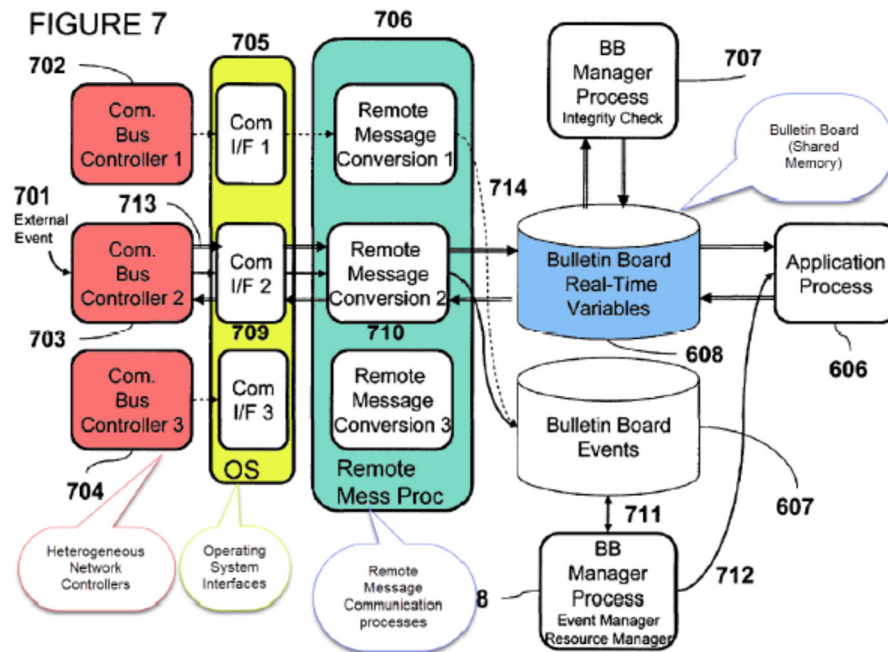


'400 Patent, FIG. 1

At the highest level, “the system level,” system gateway 101 connects buses to other system-level ECUs, subsequent gateways 103, and external components 120. *Id.*, 4:4-8. ECU 102 receives real-time input variables from networked sensors 106 via multiplexing bus system 112, processes the input and generates output variables that may be shared with other ECUs. *Id.*, 3:50-56.

Annotated FIG. 7 shows a bulletin board 608 (blue), which acts as a shared memory for sharing variables. *Id.*, 2:54-57. The bulletin board interacts with multiple communication buses 701-703 (red) and associated operating system interfaces 705 (yellow). *Id.*, 6:46-50. Data received from one communication bus is

stored on the bulletin board and shared as a new message with other network types via remote message communication processes 706 (green) that add/extract network-specific information. *Id.*; Ex-1003, 35-37.



Miesterfeld, FIG. 7 (annotated)

B. Prosecution History

Claims 1-33 were allowed following an Examiner's Amendment reflecting claims submitted in an applicant-initiated interview. *Id.*, 63-80, 111-151. None of the Notices of Allowance¹ include an Examiner's reason for allowance, and the Examiner never rejected the claims over the prior art. *See generally id.* The only

¹ The Examiner issued five Notices of Allowance, including two Corrected Notices of Allowance.

rejection of record, which is not directed to the claims at issue, relates to double patenting. *Id.*, 354-418.

III. Level of Ordinary Skill

A skilled artisan would have had at least a bachelor's degree in electrical, computer, or a related engineering discipline; two years of industry experience in the field of distributed computing or automotive engineering, or equivalent experience; and knowledge or familiarity with in-vehicle computing. Ex-1003, 38-39.

IV. Claim Construction

The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). For purposes of this IPR, the plain meaning of each claim term can be applied. Ex-1003, 40-41. Petitioner reserves the right to contend that any of the Challenged Claims is indefinite.

V. *Lohrmann* Ground

*Lohrmann*² discloses the heart of the '400 patent claims, but arguably lacks express disclosure of a memory, instructions, and processor (1[b]-1[c]) (taught by *Tofano*), accessing a storage resource (1[e]-1[j]) (taught by *Ueno*), and sharing

² *Lohrmann*, filed March 11, 2003, is prior art under at least pre-AIA 35 U.S.C. §102(e).

sensor information in less than a second (1[k]) (taught by *Staiger*). Additional references render each of these trivial additional limitations obvious. Ex-1003, 54.

Lohrmann discloses a system for managing communications networks in automobiles, and particularly a network with a plurality of network segments that are physically connected via gateways. *Lohrmann*, 2, 19. Control units or control unit applications, such as actuators or sensors, are physically connected to one another by respective data buses (CAN, FlexRay, or LIN) and communicate data over the network. *Id.*, 18, 20,21; Ex-1003, 43.

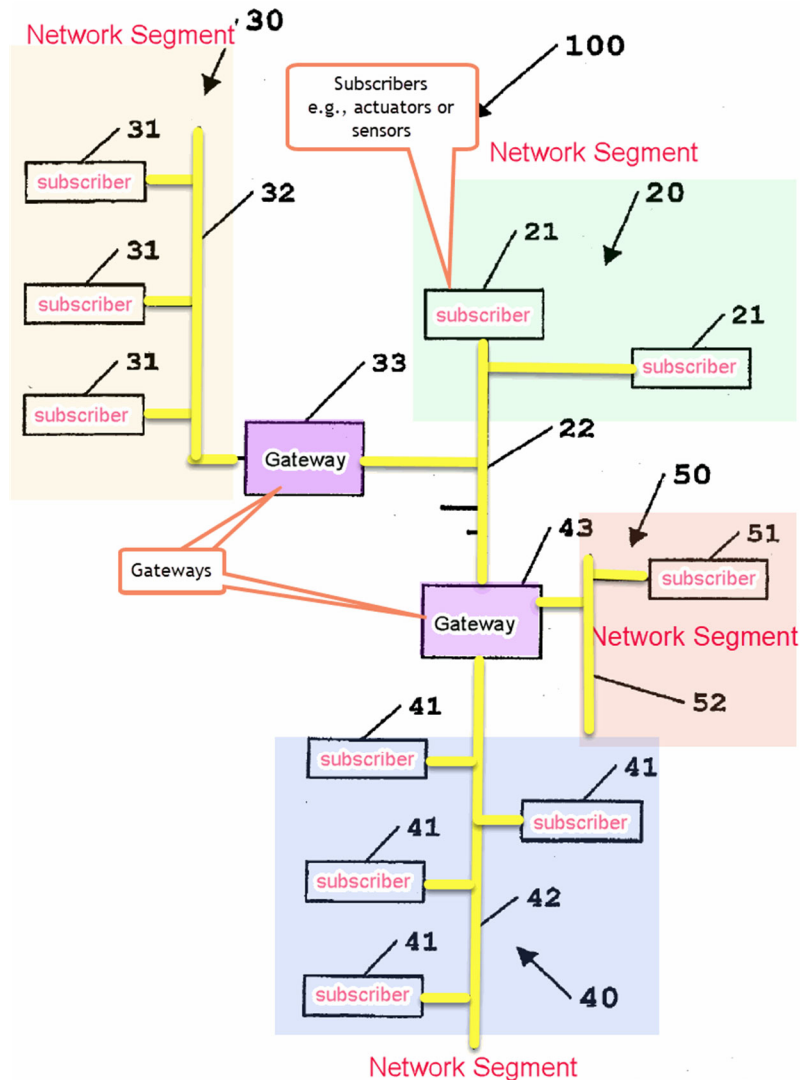


Fig. 1

Lohrmann, FIG. 1 (annotated)

**A. MEMORY, INSTRUCTIONS, AND PROCESSOR (1[b]-1[c]):
A POSITA Would Have Understood That *Lohrmann*'s Gateway
Either Includes Memory Storage, Instructions, and a Processor
or Would have Required the Same for Executing its Disclosed
Process**

A POSITA would have understood that memory and instructions are necessary for *Lohrmann*'s gateway to function and would have understood

Lohrmann's disclosure of a gateway to at least suggest a memory and instructions. Ex-1003, 55.

To the extent *Lohrmann* does not expressly disclose memory, instructions, and a processor, *Tofano*³ does and it would have been obvious to add these conventional computing components to *Lohrmann*'s gateway. *Tofano* teaches a communication system for exchanging data between networks, the system including first and second network interfaces, a shared non-switched system bus, and a processor. *Tofano*, 3:18-31. The processor "can be provided with a suitable software program to execute, thereby enabling the processor to accomplish any required functions for the communication system" and "each processor ... may have the necessary memory, disk, non-volatile storage, I/O, networking and communications peripherals, and other support necessary for it to accomplish the required functions." *Id.*, 15:56-65; Ex-1003, 56.

Tofano, like *Lohrmann*, relates to the same technical field: communication networks. A POSITA would have had a reasonable expectation of success in modifying *Lohrmann*'s gateway to include a hardware processor for executing

³*Tofano*, filed June 14, 2001, is prior art under at least pre-AIA 35 U.S.C. §102(e).

instructions stored in memory to perform the disclosed process, and the modification would have required only ordinary skill to implement. Ex-1003, 57.

B. ACCESSING A STORAGE RESOURCE (1[e]-1[j]): A POSITA Would Have Been Motivated to Incorporate a Storage Resource and Corresponding Processes for Ensuring Storage Availability into *Lohrmann*

Lohrmann at least suggests a storage resource because *Lohrmann* discloses that the “network management system stores information on the state of the network 100 or of the network segments 20, 30, 40, 50 of the network 100 and of the subscribers 21, 31, 33, 41, 43, 51.” *Lohrmann*, 2; Ex-1003, 58.

*Ueno*⁴ renders this feature and the corresponding processes obvious. *Ueno* teaches a shared storage device and a method of accessing that storage. *Ueno*, Abstract, 1:8-10 (“the present invention relates to a direct access storage device ... shared by a plurality of central processing units.”). *Ueno* teaches well-known memory management techniques relating to explicit resource management, including determining storage accessibility (*id.*, 11:27-41, FIG. 5), threshold implementation (*id.*), and error notification. *Id.*, 10:19-23; 11:1-6; Ex-1003, 59.

Ueno, like *Lohrmann* and *Tofano*, relates to the same technical field: communication networks. A POSITA would have had a reasonable expectation of success in modifying the combined system of *Lohrmann* and *Tofano* to include a

⁴ *Ueno* issued on April 13, 1993 and is prior art under pre-AIA 35 U.S.C. §102(b).

storage resource and corresponding processes, and the modification would have required only ordinary skill to implement. Ex-1003, 60.

C. SHARING SENSOR INFORMATION IN LESS THAN ONE SECOND (1[K]): A POSITA Would Have Understood That Lohrmann’s Gateway Shares Sensor Information in Less than One Second or Would Have Been Motivated to Accommodate this Time Restriction.

Lohrmann discloses that sensor information is exchanged using a control area network (CAN). *Lohrmann*, 20,21. A POSITA would have understood that the information is *capable* being of shared in less than one second because CANs are known to facilitate information transmission at speeds of less than one millisecond. Ex-1003, 61.

*Staiger*⁵ describes systems and methods for vehicle network communication and renders this feature obvious. *Staiger*, 2, 22, 43. *Staiger* explains that CAN, FireWire, and MOST busses are “real-time” buses, capable of “respond[ing] to stimuli within some small upper limit of response time, typically [in] milliseconds or microseconds,” such that, upon receiving a message, an intercommunication preprocessor “processes the message and initiates immediate distribution” of an “output[] message.” *Id.*, 7, 35, 51, claim 1, Abstract; Ex-1003, 62.

⁵ *Staiger*, filed December 4, 2001, is prior art under at least pre-AIA 35 U.S.C. §102(e).

Both *Lohrmann* and *Staiger* relate to automotive network communication, with *Staiger* clarifying how fast *Lohrmann*'s CAN bus can share information. Thus, A POSITA would have had a reasonable expectation of success in configuring *Lohrmann*'s gateway such that sensor information is capable of being shared in less than one second, and the modification would have required only ordinary skill to implement. Ex-1003, 63.

D. A POSITA Would Have Been Motivated to Combine *Lohrmann*, *Tofano*, *Ueno*, and *Staiger*

All *Lohrmann* Ground references relate to communication networks, and are combinable individually and as a whole. Ex-1003, 64. A POSITA would have been motivated to modify *Lohrmann* to incorporate a processor (taught by *Tofano*), a storage resources and corresponding processes (taught and suggested by *Ueno*) and the capability to send sensor information in less than one second (taught by *Staiger*). None of these components alter the overall functionality of *Lohrmann* and each modification would have been obvious to a POSITA and required only routine skill to implement. *Id.*

E. Ground 1: Claims 1-33 are obvious over *Lohrmann* in view of *Tofano*, *Ueno*, and *Staiger*

1. Claim 1[preamble]: “A system, comprising:”

Lohrmann discloses “a system for managing networks in a transportation unit.” *Lohrmann*, Abstract; Ex-1003, 65.

2. 1[a]: “an automotive electronic control unit including a memory storage comprising instructions, and”

Lohrmann discloses “control units” (called “subscribers”) for controlling automotive sensors or actuators, and therefore discloses an automotive electronic control unit (ECU). *Lohrmann*, 21. *Lohrmann* also discloses that a gateway is a type of subscriber (and therefore also an automotive ECU) that exchanges data over a network. *Id.*, 3, 18. A POSITA would have understood *Lohrmann*’s disclosure of a “gateway” to at least suggest a memory and instructions because memory and instructions are necessary gateway components that facilitate gateway functionality. Ex-1003, 66.

To the extent Patent Owner disagrees, *Tofano* renders this limitation obvious. *Tofano* discloses an integrated communication system that “enable[s] data and information exchanges between various networks and various network formats” and “transparently interconnects different networks,” which includes a processor for translating or converting incoming data from a first network format to another network format. *Tofano*, 2:56-62, 15:47-51. *Tofano*’s processor is operably connected to components of the system, and “can be provided with a suitable software program to execute, thereby enabling the processor to accomplish any required functions for the communication system.” *Id.*, 15:56-61. “[E]ach processor ... may have the necessary memory, disk, non-volatile storage, I/O, networking and

communications peripherals, and other support necessary for it to accomplish the required functions.” *Id.*, 3:18-20, 29-32. Thus, *Tofano* also teaches a gateway, having memory storage comprising instructions. Ex-1003, 44, 67.

It would have been obvious to a POSITA to incorporate a memory storage including instructions and the corresponding processor into *Lohrmann* to facilitate the gateway’s required functions. Ex-1030, 5 (explaining that a gateway ECU has a microprocessor); Ex-1003, 68.

**3. 1[b] and 1[c]: “at least one hardware processor in
hardwired communication with the memory storage,
wherein the at least one hardware processor executes the
instructions for:”**

As explained for 1[a], *Tofano*’s communication system includes processor 228 and corresponding software. *Id.*, 15:56-65. “[T]he processor 228 executes a suitable software program therein for translating between at least one network format, such as between at least one of the first network format and the second network format,” and therefore executes instructions related to message handling. *Tofano*, 13:23-32; Ex-1003, 69.

**4. 1[d]: “receiving sensor information associated with a
message;”**

Lohrmann’s gateway controls data exchange between “control unit[s] or control unit applications, such as sensors and actuators,” by “passing on messages

from one network segment to a further network segment.” *Lohrmann*, 4:19, 21; Ex-1003, 70.

5. **1[e] and 1[f]: “in response to receiving the sensor information, issuing, by the at least one hardware processor and to a storage resource included in the automotive electronic control unit, a storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information and, in response to issuing the storage resource request, determining whether the storage resource is available to store the sensor information;”**

Lohrmann and *Tofano* in combination with *Ueno* teaches this limitation. *Ueno* “relates to a direct access storage device (hereinafter referred to as DASD) shared by a plurality of central processing units.” *Ueno*, 1:8-10, 2:57-63. *Ueno*’s central processing units (CPUs) correspond to *Tofano*’s processor, and *Ueno*’s DASD corresponds to the claimed storage resource. *Ueno*, 1:8-10, 4:50-53, FIG. 1; Ex-1003, 45, 71.

Ueno’s CPU reads and writes datasets (information) to and from the DASD using a program. *Id.*, 4:65-5:2. Before *Ueno*’s CPU writes data to the DASD (stores information in the storage resource), it searches the DASD for “control information” to determine whether it may access the DASD. *Id.*, 3:47-51, 4:57-64, 5:27-31. A POSITA would have understood that searching the DASD for control information prior to writing the data to the DASD is a “storage resource request to access the

storage resource” because it determines whether the storage resource is available for writing data. Ex-1003, 72.

Ueno also discloses that “reserve flags, the reserve CPU numbers and the blockage flags of the two searched control information sets are checked” after the CPU searches for the control information. *Ueno*, 5:33-35. *Ueno*’s flags and reserve CPU numbers indicate whether the DASD is capable of receiving/storing the data to be written (*id.*, 4:57-64, 5:33-43); thus, a POSITA would have understood that “checking” for flags and a CPU number constitutes determining whether the storage resource (the DASD) is available to store the information (data) in response to issuing the storage resource request (the search). Ex-1003, 73.

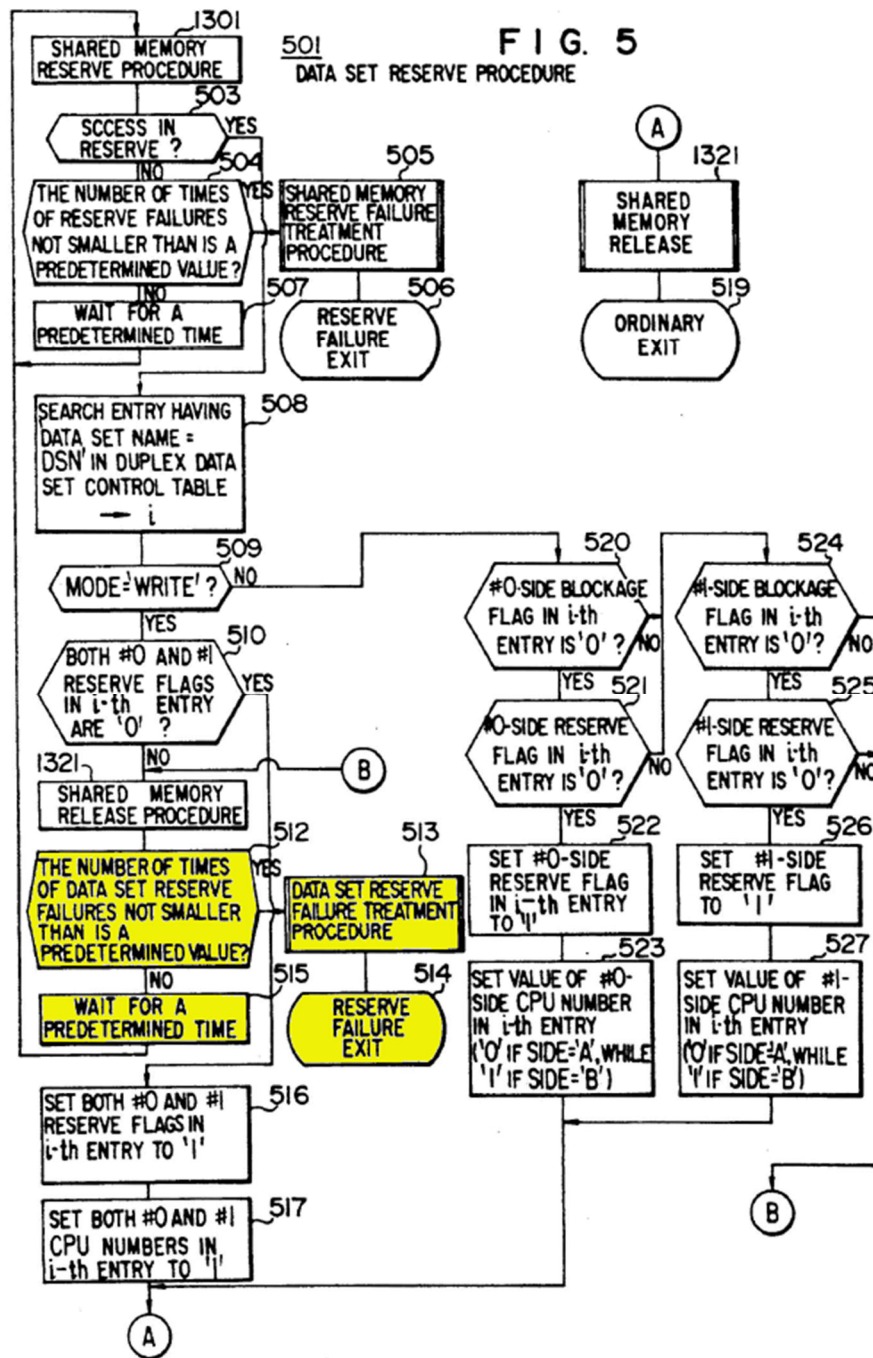
Ueno’s search and check method minimizes computer system overhead (*Ueno*, 2:61-64) and ensures accessibility to shared database storage systems. *Id.*, 2:51-56, 6:56-61; Ex-1003, 74.

A POSITA would have been motivated to implement *Ueno*’s search and check method for accessing a storage resource into the *Lohrmann-Tofano* system for these reasons. As combined, the automotive ECU gateway processor (taught by *Lohrmann* and *Tofano*) determines whether the storage resource is available to store the sensor information in response to issuing the storage resource request (taught by *Ueno*). This modification would have been within the purview of a POSITA because it would have required using routine components like processors and memories to

assess storage resource is availability. The combination would have yielded the predictable results of minimizing system overhead and ensuring accessibility. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 415-421 (2007) (“[a] person of ordinary skill is also a person of ordinary creativity, not an automaton”); Ex-1003, 60, 74-75.

6. **1[g]: “determining whether a threshold tracked since the issuance of the storage resource request has been reached indicating that the storage resource has not been available in association with the threshold tracked since the issuance of the storage resource request;”**

As explained for 1[e] and 1[f], the combination teaches issuing a storage request and determining whether the storage resource is available (searching and checking). Ex-1003, 76. *Ueno*’s searching and checking includes an iterative process whereby the processor checks for flags (storage resource accessibility) after a predetermined number of attempts or time (a threshold) elapses. *Ueno*, 11:27-41, FIG. 5.



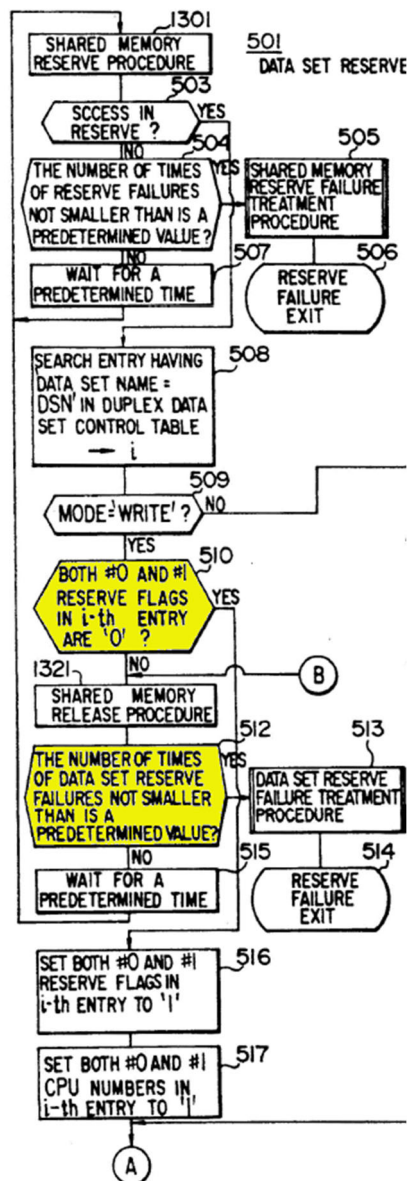
Ueno, FIG. 5 (annotated)

If the number of attempts exceeds the predetermined threshold, an “abnormality” is detected, and the DASD is determined to be unavailable.

Id., 11:37-42, FIG. 5. A POSITA would have understood that *Ueno* discloses a “threshold” because *Ueno* uses the quantity of access attempts or time elapsed to trigger an abnormality finding and determination of DASD availability. Ex-1003, 77.

7. **1[h]: “when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has not been reached indicating that the storage resource has not been available in association with the threshold tracked since the issuance of the storage resource request, issuing, by the at least one hardware processor to the storage resource included in the automotive electronic control unit, another storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information;”**

As explained for 1[g], the *combination* teaches an iterative process whereby the processor checks for flags (storage resource accessibility) after a predetermined number of attempts or time (a threshold) elapses. *Ueno*, 11:27-41, FIG. 5. *Ueno*’s iterative process includes repeating the search and check cycle (issuing another storage resource request) “if the number of times in a data set reserving failure is within a predetermined value.” *Id.*, 11: 33-37; FIG. 5, Ex-1003, 78.



Ueno, FIG. 5 (annotated)

A POSITA would have understood that *Ueno* teaches repeating the check and search process (issuing another storage request) when the DASD is determined to be unavailable, and the predetermined value of access attempts or time (threshold) has not been exceeded. As combined with *Ueno*'s check and search process, the

processor in *Lohrmann*'s gateway (1) checks the reserve flags associated with a DASD to determine its availability to receive data, and (2) if the reserve flags are not both zero, and the number of attempts is within "a predetermined value," researching and rechecking until either the number of retries exceeds a predetermined value or the DASD is determined to be available. *Ueno*, 11:12–42; Ex-1003, 79.

8. **1[i]: "when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request or the another storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has been reached, sending an error notification; and"**

As explained for 1[g], the combination teaches determining whether the DASD (storage resource) is unavailable. *Ueno*, 11:37-42, FIG. 5. The resource is unavailable "[i]f at least one of the reserve flags 202-1 and 202-2 is '1' (Step 510)." *Id.*, 11:25-33; Ex-1003. *Ueno* further discloses reporting "a failure" if the DASD is determined to be unavailable and the number of reattempts (as explained for 1[h]) exceeds the predetermined threshold. *Id.*, 10:19-23; 11:1-6 (reporting other failures); Ex-1003, 80.

9. **1[j]: “when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request or the another storage resource request, to be available, storing the sensor information utilizing the storage resource;”**

As explained for 1[e] and 1[f], the combination teaches determining whether the DASD (storage resource) is available. *Ueno* further teaches that if both reserve flags are 0, “[t]he CPU executes writing the same contents into the data sets on the two DASDs.” *Id.*, 5:42-43. A POSITA would have understood that *Ueno* discloses storing data to the storage resource and that the combination teaches storing sensor information (as disclosed by *Lohrmann*) to a DASD in response to performing (and repeating) the search and check process (issuing the/another storage resource request). Ex-1003, 81.

10. **1[k]: “wherein the automotive electronic control unit is operable such that the sensor information is capable of being shared in less than one second, and”**

Lohrmann exchanges information using a control area network (CAN). *Lohrmann*, 20. A POSITA would have understood that the information is *capable* of being shared in less than one second because CANs are known to facilitate transmission at speeds of less than one millisecond. Ex-1003, 82.

To the extent Patent Owner disputes this, *Staiger* renders this limitation obvious. *Staiger* discloses an ECU connected to a plurality of real-time networks, including “several individual CAN [] busses or other multiple purpose networks.”

Id., 3. *Staiger*'s ECU executes an application for controlling remote automobile systems while concurrently performing gateway functions between the different networks. *Id.*, 4-5. *Staiger* explains that the CAN, FireWire, and MOST buses are "real-time" buses, capable of "respond[ing] to stimuli within some small upper limit of response time, typically [in] milliseconds or microseconds," such that, upon receiving a message, an intercommunication preprocessor "processes the message and initiates immediate distribution" of an "output[] message," to, *e.g.*, a "destination unit." *Id.*, 7, 35, 51, claim 1, Abstract (emphasis added); Ex-1003, 46, 83.

It would have also been obvious to a POSITA to configure the modified system of *Lohrmann* such that message information sent from a sensor origin on a CAN, LIN, or FlexRay Network reaches its destination in milliseconds or microseconds ("less than one second") to facilitate immediate receipt of an incoming message from a sensor origin and distribution of an output message to a destination, such as an actuator. *Staiger*, 7, 35, 51, claim 1, Abstract; Ex-1003, 84.

11. 1[l]: "the automotive electronic control unit includes a plurality of interfaces including: a first interface; and a second interface for interfacing with a network, where the network is at least one of a Controller Area Network, a Flexray network, or a Local Interconnect Network."

Lohrmann's network includes "a plurality of network segments 20, 30, 40, 50, which are physically connected via gateways 33, 43." *Lohrmann*, 19. *Lohrmann*

discloses that “[t]he interface between the network segments is generally implemented in ... a gateway.” *Id.*, 3. Thus, *Lohrmann* discloses a plurality of interfaces (a first interface between a first set of network segments and a second interface between a second set of network segments) implemented in the gateway (automatic ECU). Ex-1003, 85. *Lohrmann* further discloses that various data bus systems may be used within each network segment, including CAN, FlexRay and LIN (*Lohrmann*, 20) and that the system is “suitable for operating network segments which are based on different bus systems, since the actual data bus system in the network segment is not significant for managing network segments.” *Id.*, 10. Thus, *Lohrmann* discloses that the network is at least one of a Controller Area, Flexray, or Local Interconnect Network. Ex-1003, 85.

12. Independent Claim 8

Independent claim 8 largely mirrors independent claim 1, except that it is directed to an “apparatus” (Ex-1001, 13:48), and further recites a “first network” associated with a “first protocol” and corresponding “first interface,” wherein “the first network is at least one of a Controller Area Network type, a Flexray network type, or a Local Interconnect Network type;” and a “second network” associated with a “second protocol” and corresponding “second interface,” wherein “the second network is at least one of the Controller Area Network type, the Flexray network type, or the Local Interconnect Network type.” *Id.*, 14:39-57. These limitations are

obvious for the reasons discussed in claim 1. For example, *Lohrmann* discloses a plurality of interfaces (a first interface between a first set of network segments and a second interface between a second set of network segments) implemented in the gateway (the automatic ECU). Ex-1003, 86-87. *Lohrmann* also discloses that data bus systems may be used within each network segment, including CAN, FlexRay and LIN (*Lohrmann*, 20) and that the system is “suitable for operating network segments which are based on different bus systems.” *Id.*, 10. Each network is associated with a network protocol, for example, CAN uses CAN protocol. Thus, *Lohrmann* discloses first and second networks, associated protocols, and corresponding to first and second interfaces, wherein the network(s) are at least one of a Controller Area, FlexRay, or Local Interconnect Network. Ex-1003, 87.

Claim 8 also recites additional features of the first and second interfaces which are obvious for the additional reasons discussed below.

- a. **the first interface including a first interface-related data link layer component for using first network-related data link layer header bits and a first interface-related network layer component for using first network-related network layer header bits,**

A POSITA would have found it obvious to provide, or understood that *Lohrmann*’s first interface (between a first set of network segments) includes, a data link layer component for using first network-related data link layer header bits and a first interface-related network layer component for using first network-related

network layer header bits because the industry standard⁶ for network communication at the time of the invention required as much to facilitate communication using CAN, LIN, and FlexRay networks. Ex-1019 (establishing a CAN “serial communication protocol” that supports distributed real-time control and multiplexing for use within road vehicles and explaining that the “layered” CAN architecture established by the OSI reference model includes a data link layer and a physical layer (PL) for bit encoding/decoding); Ex-1003, 88-89.

To the extent Patent Owner disputes this, *Tofano* teaches examples of network layer models (including OSI) which “support the transfer of data and information through one or more networks having a network format corresponding to a network layer model.” *Tofano*, 11:6-10. Regarding the OSI model, *Tofano* states:

Layer **2**, the Data Link layer **152**, also known as the Protocol layer, controls transmissions made through the physical layer, while detecting and correcting transmission errors to ensure error free, end-to-end transmissions 50 between networked devices. Network layer **153**, the third network layer, controls the operation of the data link and physical layers while providing higher level services such as routing and congestion control for transmissions.

Id., 11:47-54.

⁶ Set forth by the International Standards Organization (ISO).

It would have been obvious to a POSITA to configure *Lohrmann's* first interface to transmit sensor information using the OSI Reference model, as taught by *Tofano*, whereby a data link layer controls transmission through the physical layer, and the network layer controls the operation of the data link and physical layers, to support data transfer through *Lohrmann's* network. *Tofano*, 11:6-10; Ex-1003, 90-91. A POSITA would have understood that such a configuration requires a data link layer component for using data link layer header bits associated with the first network (*e.g.*, CAN, LIN or FlexRay) and a network layer component for using the CAN, LIN or FlexRay network layer header bits, because the interface needs to have the requisite “mechanisms” (“components”) to enable the transfer. Ex-1003, 91.

- b. a second interface for interfacing with the second network, the second interface including a second interface-related data link layer component for using second network-related data link layer header bits and a second interface-related network layer component for using second network-related network layer header bits, where the second network is at least one of the Controller Area Network type, the Flexray network type, or the Local Interconnect Network type.**

A POSITA would have also found it obvious or understood that *Lohrmann's* second interface (between a second set of network segments) includes, a second interface-related data link layer component for using second network-related data

link layer header bits and a second interface-related network layer component for using second network-related network layer header bits for the same reasons as the first interface. Ex-1003, 92.

13. Independent Claim 27

Independent claim 27 largely mirrors claim 1, except that claim 27 is directed to a “non-transitory computer-readable medium” (Ex-1001, 21:33-38) and further recites a “first network,” a “second network,” and corresponding first and second interfaces. *Id.*, 22:16-29. These limitations are also rendered obvious by the combination for the reasons explained for claim 1. Ex-1003, 93.

Claim 27 also specifies that the “threshold” is “time-related” and that the second network “is another one of “the Controller Area, the Flexray or the Local Interconnect Networks. These limitations are also rendered obvious by the combination for the reasons explained for claim 1. For example, as discussed in 1[g], *Ueno*’s threshold is “time-related” because *Ueno* uses the quantity of access attempts or time elapsed to trigger an abnormality finding and determination of DASD availability. Regarding the networks and as discussed in 1[l], *Lohrmann* discloses that the system “is preferably suitable for operating network segments which are based on different bus systems, since the actual data bus system in the network segment is not significant for managing network segments.” *Lohrmann.*, 10, 20. Thus, *Lohrmann* discloses that the first network is one of a Controller area,

Flexray, or Local Interconnect Network and the second network is “based on different bus systems,” i.e., “another one of” the networks. Ex-1003, 94.

Lastly, claim 27 recites “ceasing repeating issuance of another storage resource request” instead of “sending an error notification.” But because the combination, as discussed in 1[i] teaches sending the error notification instead of another storage resource request, the combination also renders obvious “ceasing” repeating the storage request. Ex-1003, 95.

14. Claims 2-7, 10, 11, and 28-33: sharing “in less than one [millisecond/second].”

Dependent claims 2-7, 10, 11, and 28-33 each require some sharing event to occur “in less than one second,” “in less than one millisecond,”⁷ or “with sufficient speed for use in connection with an automotive device.” *Staiger* teaches that CAN buses are “real-time” busses, capable of “respond[ing] to stimuli within some small upper limit of response time, typically [in] milliseconds or microseconds,” such that, upon receiving a message, an intercommunication preprocessor “processes the message and initiates immediate distribution” of an “output[] message,” to *e.g.*, a “destination unit.” *Id.*, 7, 35, 51, claim 1. Thus, *Lohrmann*, in combination with

⁷ Claim 33 requires the computer program product to be configured for sharing “in less than the one millisecond second [*sic*].”

Tofano, *Ueno*, and *Staiger* renders claims 2-6, 10, 11, and 28-33 obvious. Ex-1003, 96-97.

Claim 7 requires the system to be configured for sharing “with sufficient speed for use in connection with an automotive device.” Ex-1001, 13:44-47. The combination renders this limitation obvious because, as explained above in element 1[k], data is written and read (shared), in milliseconds or microseconds. *Staiger*, 7, 35, 51, claim 1. A POSITA would have understood that this speed is “sufficient” “for use in connection with an automotive device,” as evidenced by the specification of the ’400 patent, which explains that “[i]n the context of the present description, real-time may include any response time that may be measured in milli- or microseconds, and/or is less than 1 second.” Ex-1001, 3:45-49. Ex-1003, 98.

15. Claim 9: “The apparatus as recited in claim 8, wherein the apparatus is operable such that network layer translation is capable of being avoided.”

Tofano further teaches that “[s]ometimes, differences in network layer models may not be important or significant. For example, a preset number of network layers from different networks may be encapsulated as payload and transmitted between different networks without requiring any comparisons or translations.” *Tofano*, 14:47-52. Thus, *Lohrmann* as modified by *Tofano* further teaches that “network layer translation is capable of being avoided.” Ex-1003, 99.

16. **Claim 12: “The apparatus as recited in claim 11, wherein the apparatus is operable such that the sensor information is shared by the second interface-related network layer component using the second network-related network layer header bits by adding the second network-related network layer header bits to a data unit including the sensor information, and then the second interface-related data link layer component using the second network-related data link layer header bits by adding the second network-related data link layer header bits to the data unit, before communicating the data unit on a physical link of the second network.”**

Tofano further teaches an encoding process for transmitting (sharing) data between networks using the OSI model. The process “requires adding a suitable layer 2 and layer 1 ... representing the data link layer and physical media layer respectively, to the payload data 302 as represented by layers L3 through L7.” *Tofano*, 28: 8-13. The process “can add one or more layers from a given network format to the payload data to prepare it for transmission to the outgoing network” so that ultimately, the payload data is embodied in a network layer model stack which can be transmitted through a network interface to an outgoing network in a compatible network format. *Id.*, 28:14-21.

That is, *Tofano* teaches adding the second network-related network layer header bits (“one or more layers from a given network format”) to a data unit and adding the second network-related data link layer header bits (“suitable layer 2”) to the data unit before communicating the data on a physical link of the network. Ex-

1003, 100; *see also* Ex 1022, 2:43-62 (explaining “a transport header, network header and data link header ... [are] attached to the data at each of those layers, with each step typically including data moving and copying, before sending the data as bit packets, over the network, to the second host”).

17. **Claim 13: “The apparatus as recited in claim 12, wherein the apparatus is operable such that the first interface-related data link layer component uses the first network-related data link layer header bits by removing the first network-related data link layer header bits from another data unit, and the first interface-related network layer component uses the first network-related network layer header bits by removing the first network-related network layer header bits from the another data unit so that the sensor information is removed from the another data unit, before the sharing.”**

Tofano further teaches that “data received in a network format may be decoded or extracted from its incoming physical layer and data link layer, so that decoded data can be represented by the contents of network layers 3 through 7 inclusive.” *Tofano*, 23:36-49. In Figure 7a “layers 3 through 7 are removed by decoding, and the decoded data 302 is represented as extracted from physical layer L1 and data link layer L2. L1 and L2 are collectively denoted as 303, and are removed by the network interface, processor, or both.” *Id.*, 24:51-58 (emphasis added).

Thus, *Tofano* teaches removing the first network-related data link layer header bits (Layer 2) from another data unit, and removing the first network-related network

layer header bits (layer 3) from the “another” data unit so that the information is removed from the another data unit. Ex 1022, 2:63-3:7 (explaining that “headers are removed and data processed in order from the lowest (Physical) layer to the highest (Application) layer” when data packets are received); Ex-1003, 101-102.

As explained for claim 12, a POSITA would have understood that sending payload data over a network involves adding header bits to form a message, sending the message, and removing the header bits to extract the payload data. Ex-1022, 2:43-62; Ex-1003, 103.

18. Claims 14 and 15: “The apparatus as recited in claim 8, wherein the apparatus is operable such that the storage resource request and the another storage resource request are [identical/the same].”

As explained for 1[h], *Ueno* teaches repeating the write request (search and check) if a reserve flag is “1” and a retry value has not been exceeded. *Ueno*, 11:12-42. This is the exact procedure described in the ’400 patent’s specification. Ex-1001, 8:36-37 (“If the resource is not available, it may try it again after a waiting period (1011) until the resource is available.”); Ex-1003, 104. Thus, a POSITA would have understood that *Ueno* teaches that “the another storage resource request” is identical to or the same as “the storage resource request.” *Id.*

19. Claims 16 and 17: “The apparatus as recited in claim 8, wherein the apparatus is operable such that the sensor information excludes all [a portion of any] header bits of the message.”

As explained for claim 13, layers are decoded and header bits removed prior to transmission. Because the payload (the actual information being transmitted), in the instant combination is the sensor information, a POSITA would have understood that the portion of a message that is sensor information excludes all header bits of the message. Ex-1003, 105. If “all header bits of the message” are excluded, then “a least a portion of any header bits” are necessarily excluded. Thus, claim 17 is obvious for the same reasons as claim 16. *Id.*

20. Claim 18: “The apparatus as recited in claim 8, wherein the apparatus is operable such that the storage resource includes a bulletin board.”

As explained in 1[e], *Lohrmann* as modified by *Tofano* and *Ueno* teaches a DASD. *Ueno*, 1:8-10, 5:21-22, 41-42. The DASD is a database from which electronic data may be read and written. *Id.* Thus, a POSITA would have understood that the DASD is a “bulletin board” within the meaning of the ’400 patent. Ex-1001, 5:20-24 (“the bulletin board may refer to any database that enables users to send and/or read electronic messages, files, and/or other data that are of general interest and/or addressed to no particular person/process.”). Ex-1003, 106.

- 21. Claims 19-21: “The apparatus as recited in claim 8, wherein the apparatus is operable such that the error notification is sent, when the storage resource included in the automotive electronic control unit is determined, in response to issuing the [another] storage resource request [and the another storage resource request], to not be available and the threshold tracked since the issuance of the storage resource request has been reached.”**

Claims 19-21 are similar except claim 19 recites “the storage resource request,” claim 20 recites “the another storage resource request,” and claim 21 recites both “the storage resource request and the another storage resource request.”

Because, as explained for 1[i], the combination teaches sending an error notification when the storage resource is determined to be unavailable “in response to issuing the storage resource request or the another storage resource request” and reaching the threshold, claims 19 and 20 are for the same reason as 1[i]. *Ueno*, 11:27-41, FIG. 5. Ex-1003, 107-108.

As discussed in 1[h] and 1[i], *Lohrmann*’s modified process is iterative such that the DASD may be determined to be unavailable after issuing another request and reaching the threshold. *Ueno*, 11:27-41, FIG. 5. This occurs, for example, when the number of attempts (which includes “the request” and the “another request”) exceeds the threshold. Thus, claim 21 is also obvious. Ex-1003, 109.

22. Claims 22 and 26: “The apparatus as recited in claim 8, wherein at least one of: the memory storage includes the storage resource; the memory storage does not include the storage resource....”

Claims 22 and 26 require “at least one of” numerous features listed in the alternative describing the apparatus of claim 8. Ex-1001, 15:62-16:62, 17:12-21:32. Because “at least one” of these features, *e.g.*, “the memory storage includes the storage resource” is taught by the combination, claims 22 and 26 are obvious for same reasons as claim 8. Ex-1003, 110.

23. Claim 23: “The apparatus as recited in claim 8, wherein the apparatus is operable such that the information associated with the message is identified in another storage resource that stores the information after the message is received.”

As discussed in 1[e], 1[f] and 1[j], *Ueno* teaches that the DASD (storage resource) is one of a “pair” of DASDs. *Ueno*, 4:49-53. The second DASD constitutes “another storage resource” that “stores the information” for the same reasons the first DASD constitutes “a storage resource” that stores the information. Ex-1003, 111. The second DASD, like the first DASD, also reads (identifies) the information. *Ueno*, 5:5-22. Accordingly, the modified system of *Lohrmann* teaches “another storage resource” that identifies and stores the sensor information. *Id.*; Ex-1003, 111.

24. **Claim 24: “The apparatus as recited in claim 8, wherein the apparatus is operable such that the information associated with the message is identified in another storage resource that stores the information after the message is received and before the information is stored utilizing the storage resource, the another storage resource capable of being used for information storage, regardless as to a particular network with which the information is shared.”**

As discussed above in claim 23 *Ueno* teaches that the second DASD is operable to read (identify) the data after the message is received (as discussed in claim element 1[d]). Ex-1003, 112. The data is read then written to (stored in) the first DASD. *Ueno*, 5:5-43. *Ueno* does not expressly teach that the DASD is capable of storing information “regardless” of the network used to share the information.

Tofano further teaches that its “communication system allows data or information in any form to be processed and conveyed transparently through the communication system to support ‘end to end’ exchanges of data and information between networks. As such, data and information in any form, and in various diverse network formats, can be processed and exchanged between networks in a common, efficient, and integrated manner by the communication systems of the present invention.” *Tofano*, 10:13-21 (emphasis added).

Accordingly, it would have been obvious to a POSITA to configure the storage resource of the proposed combination to be “capable” of storing information

regardless network format, to facilitate information processing and exchange in a “common, efficient, and integrated manner.” *Id.*; Ex-1003, 113-114.

25. Claim 25: “The apparatus as recited in claim 24, wherein the apparatus is operable such that the information is stored utilizing the another storage resource in response to a corresponding request that is separate from the storage resource request.”

As explained for 1[k], the combination teaches storing the information in each DASD. *Ueno*, 5:42-43. *Ueno* teaches that there is “one control information set for each data set for each DASD of the pair of DASDs forming the shared duplex DASD pair,” (*id.*, 1:54-57); thus, *Ueno* teaches that the request to store information in the first DASD (storage resource) is “separate” from a request to store information in the second DASD (another storage resource) because *each* DASD is searched and checked prior to saving the information. *Id.*, 5:28-43 (“The reserve flags, the reserve CPU numbers and the blockage flags of the two searched control information sets are checked, and when both the control information sets satisfy the condition “reserve flag=0 and blockage flag=0 ... The CPU executes writing the same contents into the data sets on the two DASDs”) (emphasis added); Ex-1003, 115.

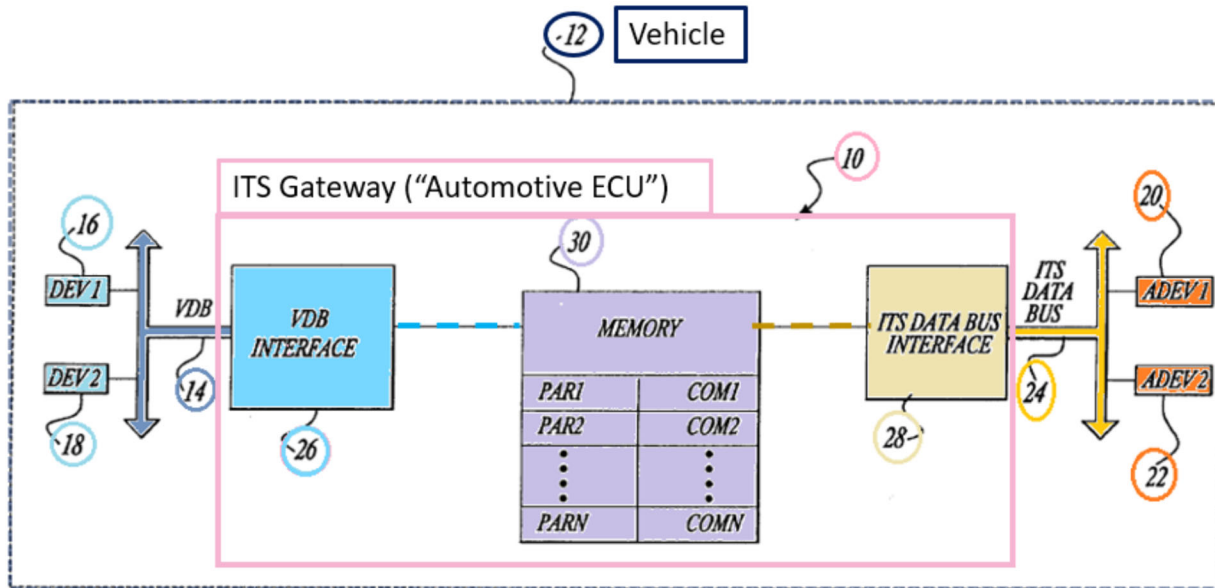
VI. *Miesterfeld* Grounds

*Miesterfeld*⁸ discloses the heart of the '400 patent claims, but arguably lacks express disclosure of a hardware processor (1[c]) (taught by *Wong*), a threshold (1[g]-1[i]) (taught by *Stewart*), sending an error notification (1[i]) (taught by *Stewart*), and CAN, FlexRay, and LIN networks (1[l]) (taught by *Wense*). Additional references *Wong*, *Stewart*, and *Wense* render each of these trivial additional limitations obvious. Ex-1003, 116.

Miesterfeld discloses a data exchange system including a controller for “process[ing] vehicle data to control at least one vehicle related function.” *Miesterfeld*, 2:23-27. The controller may be implemented on a vehicle 12 having a vehicle data bus (VDB) 14, an intelligent transportation system (ITS) data bus 28, and corresponding devices, 16, 18, 20, and 22, which “write data to or read data from” their respective data buses. *Id.*, 3:1-16. In operation, the controller (“gateway 10”) facilitates data exchange between the VDB and ITS data bus via shared memory 30. *Id.*, 2:36-39, 3:18-20. To “effect such an exchange,” the system includes VDB and ITS data bus interfaces which “read[] and write data from” both the data buses

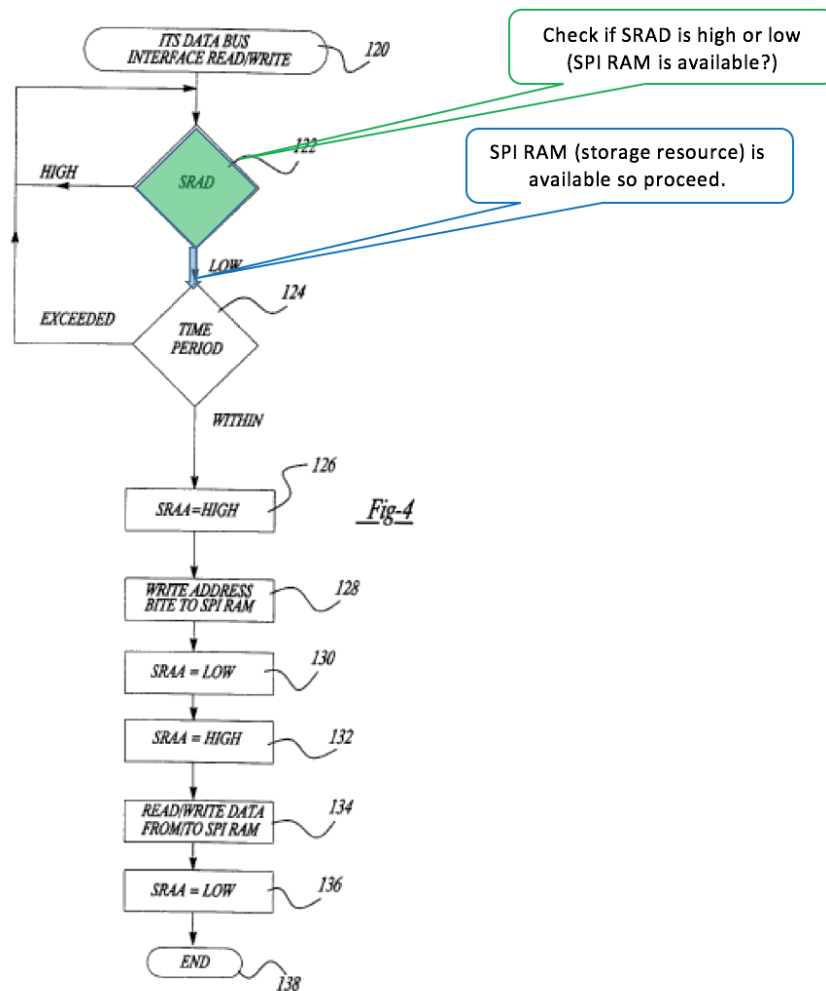
⁸ *Miesterfeld* issued on October 31, 2000 and is prior art under pre-AIA 35 U.S.C. §102(b). Patent Owner has not disputed that *Miesterfeld* pertains to the same technical field as other members of the '400 Patent family. Ex-1026, 1.

and shared memory 30. *Id.*, 20-25. Annotated FIG. 1. illustrates *Miesterfeld*'s data exchange system on vehicle 12; Ex-1003, 27, 117.



Miesterfeld, FIG. 1 (annotated)

Miesterfeld further discloses a process for reading and writing (storing) data received through the vehicle's devices. *Id.*, 4:22-26, 5:38-43, 6:33-40, FIG. 4. As illustrated in annotated FIG. 4, the process includes, *inter alia*, determining whether SPI RAM is available and storing data if so. *Id.* The process is iterative—the system repeatedly attempts to determine SPI RAM availability until it either becomes available or too much time has elapsed. *Id.*, 6:40-45 (explaining the handshake arbitrating access to the SPI RAM (SRAA) "must" be set to "high" within 5 μ s of determining that the SRAD signal line is low.); Ex-1003, 48, 118.



Miesterfeld, FIG. 4 (annotated)

A. HARDWARE PROCESSOR (1[c]): A POSITA Would Have Understood that *Miesterfeld*'s Controller Either Included or Would have Required a Processor for Executing its Disclosed Process

A POSITA would have understood that a processor and instructions are implicit to *Miesterfeld*'s gateway's functionality, *e.g.*, enabling data exchange between vehicle systems and third-party systems, and controlling information sharing between electronic control devices on the VDB and the ITS data bus for the

purpose of monitoring and controlling vehicle functions. *Miesterfeld*, 1:13–40, 2:66–3:49; Ex-1003, 119.

To the extent *Miesterfeld* does not expressly disclose a processor, *Wong*⁹ does, and it would have been obvious to add a processor to *Miesterfeld*’s controller. *Wong* teaches vehicle information system 20 including master control unit (MCU) 24 and one or more secondary control units (SCU) 26(1) and 26(2) connected to automobile components and systems 32, 34, 36. *Wong*, (54), 1:52-60, 2:32-373:25-4:2, FIG. 1. The MCU and SCUs include “processor 100” running a “real-time, multitasking operating system that is capable of supporting “plug-and-play system configuration and providing high stability, security, and efficiency.” *Id.*, 1:52-60, 2:32-37, 5:64-6:29. Like *Miesterfeld*’s controller, *Wong*’s controller can execute instructions for controlling data flow management (*Id.*, 6:40-42) and permits communication among automobile devices, including sensors. *Id.*, 7:51-58. A POSITA would have had a reasonable expectation of success in modifying *Miesterfeld*’s controller (gateway) to include a hardware processor for executing instructions to perform the disclosed

⁹*Wong*, filed June 21, 1999, is prior art under at least pre-AIA 35 U.S.C. §102(e). Patent Owner has not disputed that *Wong* belongs to the same technical field as other members of the ’400 patent family. Ex-1026, 1.

process, and the modification would have required only ordinary skill to implement.
Ex-1003, 49,120.

B. THRESHOLD AND ERROR MESSAGE (1[g]-1[i]): A POSITA Would Have Understood *Miesterfeld*'s Countdown to 5 μ s Is a "Threshold" and Would Have Found it Obvious to Provide an Error Notification if the Threshold Is Exceeded

Miesterfeld discloses tracking whether SRAA is "high" within 5 μ s of determining that the SRAD signal line is low (*Miesterfeld*, 6:40-45); and thus discloses a "threshold." Ex-1003, 121.

To the extent *Miesterfeld*'s countdown is not an express disclosure of a threshold, *Stewart*¹⁰ renders it obvious. *Stewart* teaches a framework for integrating real-time software control modules for real-time sensor-based systems. *Stewart*, 1, 6, 7. To "guarantee that tasks will get the data they require on time, every time," *Stewart* teaches implementing a "bounding wait time" (threshold) in a multiprocessor synchronization method. *Id.*, 11. *Stewart* also teaches implementing a "time-out mechanism" (threshold) for preventing data transfer when a "pre-

¹⁰ *Stewart*, a publication of the 1992 proceedings of the IEEE conference on Intelligent Robots and Systems, is prior art under pre-AIA 35 U.S.C. §102(b). Patent Owner did not dispute that *Stewart* is prior art to other members of the '400 patent family. See generally Ex-1025; Ex-1027; Ex-1028, 10-11; Ex-1024.

specified time or number of retries” elapses and that “error handlers should be installed to detect tasks that suffer successive time-out errors.” *Id*; Ex-1003, 50, 122.

A POSITA would have been motivated to add the thresholds and error notification of *Stewart* to “guarantee that tasks will get the data they require on time, every time,” as taught by *Stewart*. *Stewart*, 11. A POSITA would have understood that implementing the thresholds and error notification of *Stewart* within *Miesterfeld* would have improved *Miesterfeld*’s system by identifying errors and preventing a continuous loop of retries. Ex-1003, 123.

Both *Miesterfeld* and *Stewart* relate to real-time distributed computer control systems and use similar techniques to solve the same problem (a shared memory architecture for facilitating data exchange between control modules in a real-time distributed system) (*Stewart*, 1, 6, 7; *Miesterfeld*, 6:60-63, FIG. 4). A POSITA would have had a reasonable expectation of success in modifying *Miesterfeld*’s instructions to include the step of determining whether a threshold is reached (and other threshold-based steps) and providing an error notification, and the modification would have required only ordinary skill to implement. Ex-1003, 124.

C. CAN, FLEXRAY, AND LIN NETWORKS (1|1|1): A POSITA Would Have Found It Obvious for *Miesterfeld*'s Data Buses to Comprise at Least One of a Controller Area, FlexRay, or Local Interconnect Network

Miesterfeld discloses that the ITS data bus 24 (first network) may be “any of a number of ITS data buses” (*Miesterfeld*, 4:5-10, 9:55-57) and that the VDB 14 (second network) may be “configured to implement the J1850 configuration as prescribed by the Society of Automotive Engineers (SAE) or any other industry standard as may be required.” *Id.*, 4:7-10. Thus, *Miesterfeld* suggests using CAN, LIN, or Flex Ray Networks because a POSITA would have understood these to be the industry standards *Miesterfeld* expressly contemplates. Ex-1003, 125.

To the extent *Miesterfeld* does not expressly disclose that its ITS data bus 24 is one of CAN, LIN, or Flex Ray Networks, *Wense*¹¹ expressly discloses that cars utilize “[s]everal multiplex protocols,” including CAN (for engine and body control networks), FlexRay (for safety, braking, and steering systems), and LIN (for cost-critical distributed body electronics). *Wense*, 11; Ex-1003, 126. *Wense* simply clarifies the types of industry-standard networks that would have been implemented in *Miesterfeld*'s vehicle system. Thus, a POSITA would have had a reasonable

¹¹ *Wense* is a book published in 2001 and is prior art under pre-AIA 35 U.S.C. §102(b). Patent Owner did not dispute that *Wense* is prior art to other members of the '400 patent family. *See generally* Ex-1025; Ex-1027; Ex-1028, 10-11; Ex-1015.

expectation of success in configuring *Miesterfeld*'s networks to be one of CAN, LIN or FlexRay, and the modification would have required only ordinary skill to implement. *Id.*

**D. A POSITA Would Have Been Motivated to Combine
*Miesterfeld, Wong, Stewart, and Wense***

Each of the references of the *Miesterfeld* Grounds relate to communication networks, and are combinable individually and as a whole. A POSITA would have been motivated to modify *Miesterfeld* to incorporate a processor (taught by *Wong*), a threshold and error notification (taught by *Stewart*) and at least one of a CAN, LIN, or Flexray network (taught by *Wense*) because each of the secondary references improves *Miesterfeld*'s system by adding conventional, necessary components (a processor), providing routine timing mechanisms to identify and prevent errors (a threshold and error notification), and facilitating compliance with automotive industry standards (CAN, FlexRay, and LIN Networks). None of these modifications alters the overall functionality of *Miesterfeld* and each would have been obvious to a POSITA and required only routine skill to implement. Ex-1003, 127.

E. Ground 2: Claims 1-7 and 27-33 are obvious over *Miesterfeld* in view of *Wong, Stewart, and Wense*

1. Claim 1[preamble]: “A system, comprising:”

To the extent the preamble is limiting, *Miesterfeld* discloses a system. *Miesterfeld*, 2:23-24 (“[t]his invention is directed to a data sharing system in a vehicle.”), 1:6-10; Ex-1003, 128.

2. 1[a]: “an automotive electronic control unit including a memory storage comprising instructions, and”

Miesterfeld’s system includes a “vehicle system controller” (“gateway”) for “process[ing] vehicle data to control at least one vehicle related function.” *Miesterfeld*, 2:24-28. The gateway “has at least intermittent and direct access to and exchanges data on a vehicle data bus” and as illustrated in annotated FIG. 1 below, includes a memory through which a vehicle data bus (VDB) and intelligent transportation system (ITS) data bus exchange data and commands. *Id.*, 1:5-11, 2:24-49, claim 1. The gateway facilitates communication between computerized devices (automotive ECUs) through a combination of hardware and software (instructions) read from or written to the memory. *Id.*, 1:13-3:19 (explaining that “a further object of the present invention to provide a data exchange gateway to enable a third party device to implement selected commands on a vehicle system” and that the common memory between the VDB and ITS “may be used to store specific commands which a third party device may request of a specific vehicle controller”). Accordingly, the

gateway corresponds to the claimed “automotive electronic control unit.” Ex-1003, 129; *see also* Ex-1030, 5 (explaining that “a gateway node is an ECU”).

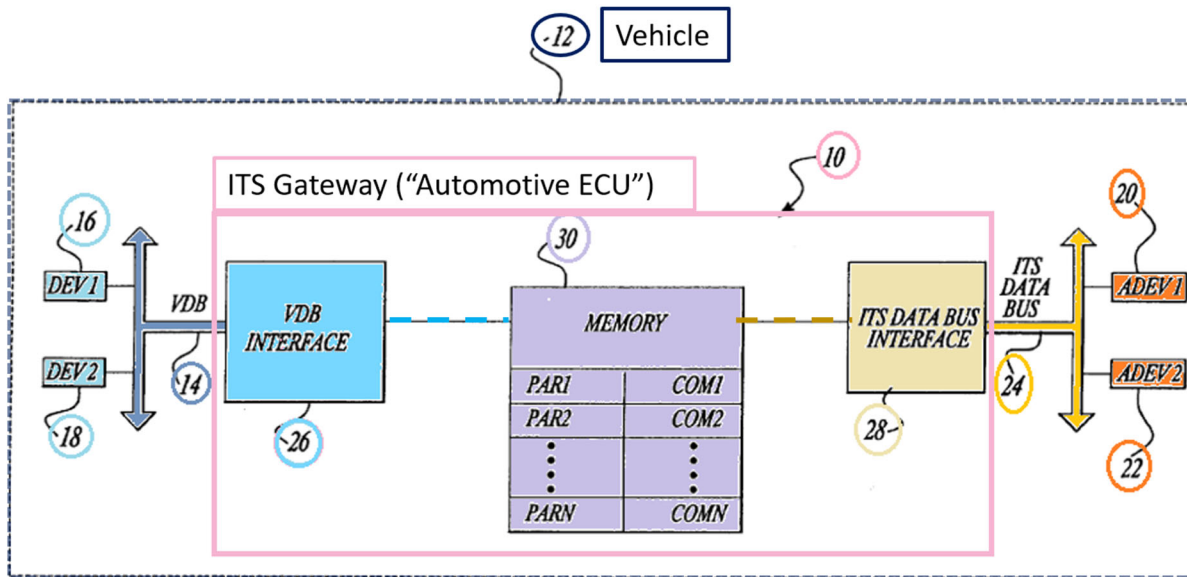


Fig-1

Miesterfeld, FIG. 1 (annotated)

3. **1[b] and 1[c]: “at least one hardware processor in hardwired communication with the memory storage, wherein the at least one hardware processor executes the instructions for:”**

Miesterfeld at least suggests a hardware processor executing instruction and in hardwired communication with the memory storage because a POSITA would have understood that a processor and instructions are implicit to *Miesterfeld*’s gateway’s functionality, *e.g.*, enabling data exchange between vehicle systems and third party systems, and controlling information sharing between electronic control devices on the VDB and the ITS data bus for the purpose of monitoring and

controlling vehicle functions. *Miesterfeld*, 1:13–40, 2:66–3:49; Ex-1030, 5 (explaining that a gateway ECU has a microprocessor); Ex-1003, 130.

To the extent Patent Owner disputes this, *Wong* expressly teaches an automobile control unit (also called “cluster controller”) including a processor, volatile memory, non-volatile memory, and a processor in hardwired communication with each memory. *Wong*, FIG. 4, 3:27-30, 6:4-6; Ex-1003, 131.

A POSITA would have been motivated to incorporate *Wong*’s processor in *Miesterfeld*’s ITS gateway, whereby the processor is hardwired to the memory and executes instructions, to facilitate data processing for the purpose of monitoring and controlling vehicle functions. *Wong*¹², 6 10-21, 36-43; 7:51-60; Ex-1003, 132.

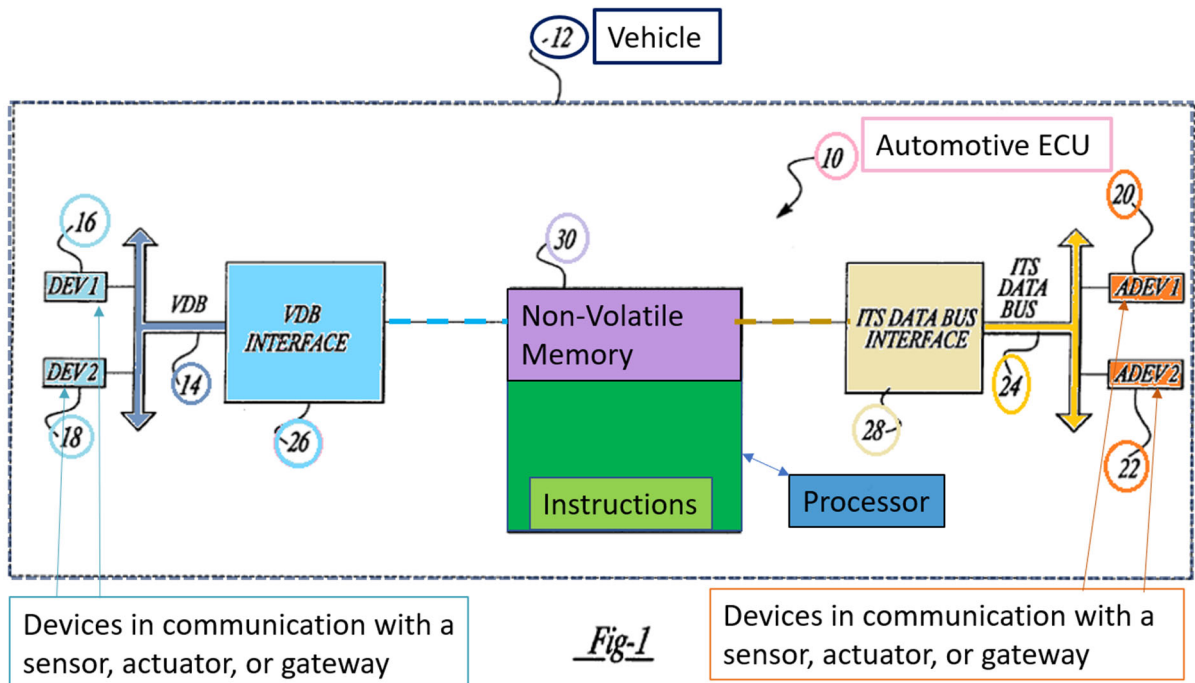
4. Claim 1[d]: “receiving sensor information associated with a message;”

Miesterfeld’s gateway receives information obtained from devices 16, 18, 20 and 22 data over the VDB and ITS data bus. *Miesterfeld*, FIG. 1, abstract, 2:66-3:25. The information obtained from devices 16, 18, 20 and 22 pertains to sensor information because it relates to measured vehicle data. *Id.*, 3:2-25, 1:13-25 (explaining that devices 16 and 18 “control vehicle operations such as engine

¹² The Board previously confirmed that POSITA reviewing *Miesterfeld* would have been motivated to look to a general-purpose microprocessor as taught in *Wong*. Ex-1023, 18-19.

operation, transmission operation, instrumentation operation, and the like”), 1:31-40, 3:14-17 (explaining that devices 20 and 22 “require vehicle data as input in order to operate the device or implement some additional feature on the vehicle” and “may also seek to control vehicle functions where appropriate and safe”).¹³ *Miesterfeld*’s sensor information is associated with a message because it is stored and accessible through memory read/write operations. *Miesterfeld*, 2:66-3:1, 3:18-25, 3:40-43, 3:59-64, *see also id.*, 1:62-2:15 (describing gateway functions for exchanging data between networks). Thus, *Miesterfeld*’s process includes receiving sensor information associated with a message from either VDB 14 or ITS data bus 24. Ex-1003, 133.

¹³ The Board previously agreed that *Miesterfeld*’s system “receive[s] input from various devices and sensors.” Ex-1023, 63.



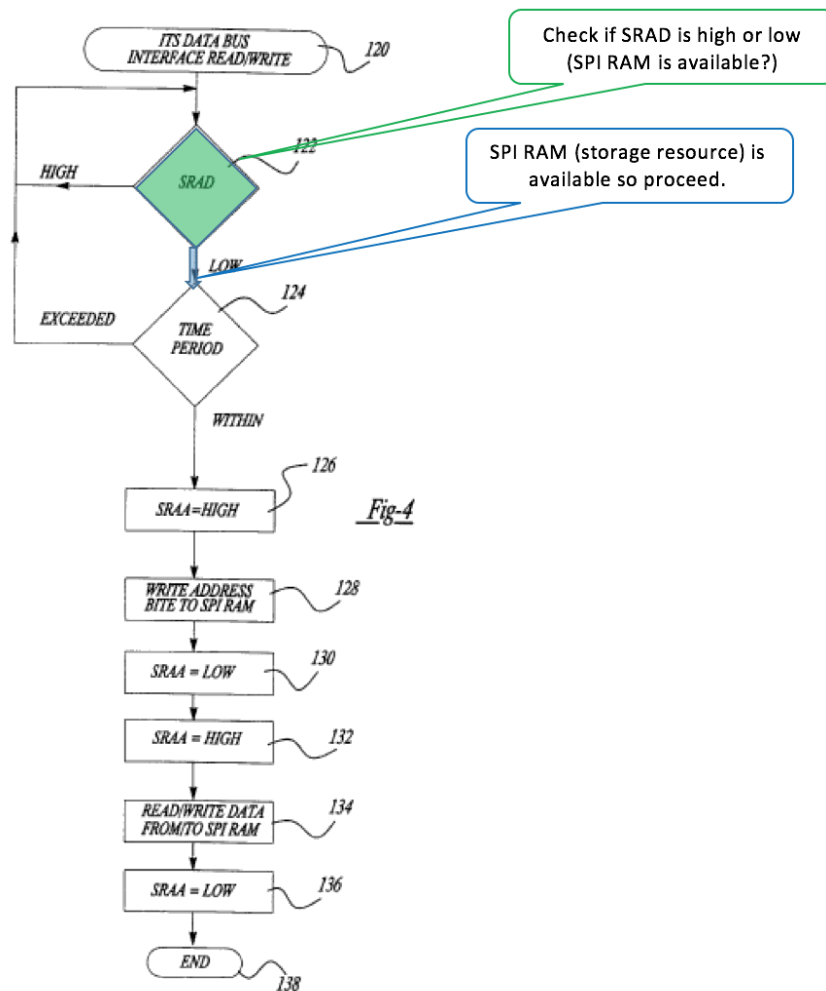
Miesterfeld, FIG. 1 (annotated)

5. **Claim 1[e]: “in response to receiving the sensor information, issuing, by the at least one hardware processor and to a storage resource included in the automotive electronic control unit, a storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information and,”**

Miesterfeld as modified by *Wong* teaches issuing a request to access a storage resource to store information in response to receiving the information. *Miesterfeld* explains, for example, that when ITS data bus interface 58 (another example of the ITS data bus interface 28 shown in FIG. 1) “attempts to access SPI RAM 64” (a specific implementation of memory 30) such as for reading or writing, “the ITS data bus interface 58 must first test the SRAD signal line as shown at block 122.” *Miesterfeld*, 6:34-36. *Miesterfeld*’s “attempts to access SPI RAM 64” is a request to

access a storage resource (memory). *Miesterfeld*, 3:26-39, 3:64-66.¹⁴ *Miesterfeld* discloses that before reading or writing to the shared memory, the ITS data bus interface first determines whether the shared memory is available by checking whether the SPI RAM Access Denied (SRAD) signal line is high—if SRAD is high, the SPI RAM is unavailable. *Miesterfeld*, 6:33-40; *see also id.*, 4:11-26, 5:32-43. Checking whether the SRAD signal line is available corresponds to “issuing” a storage resource request to access the shared memory. Ex-1003, 134.

¹⁴ The Board previously found that *Miesterfeld* discloses issuing a storage resource request to access a storage resource. Ex-1017, 41; Ex-1018, 60; Ex-1016, 33; Ex-1023, 38-39.



Miesterfeld, FIG. 4 (annotated)

6. **Claim 1[f]: “in response to issuing the storage resource request, determining whether the storage resource is available to store the sensor information;”**

Miesterfeld discloses determining whether the storage resource is available for storing the information. As shown above in annotated FIG. 4., *Miesterfeld* discloses that “[i]f SRAD is high, the VDB interface 62 is accessing SPI RAM 64, and ITS data bus interface 58 must wait until SPI RAM 64 is available, and control

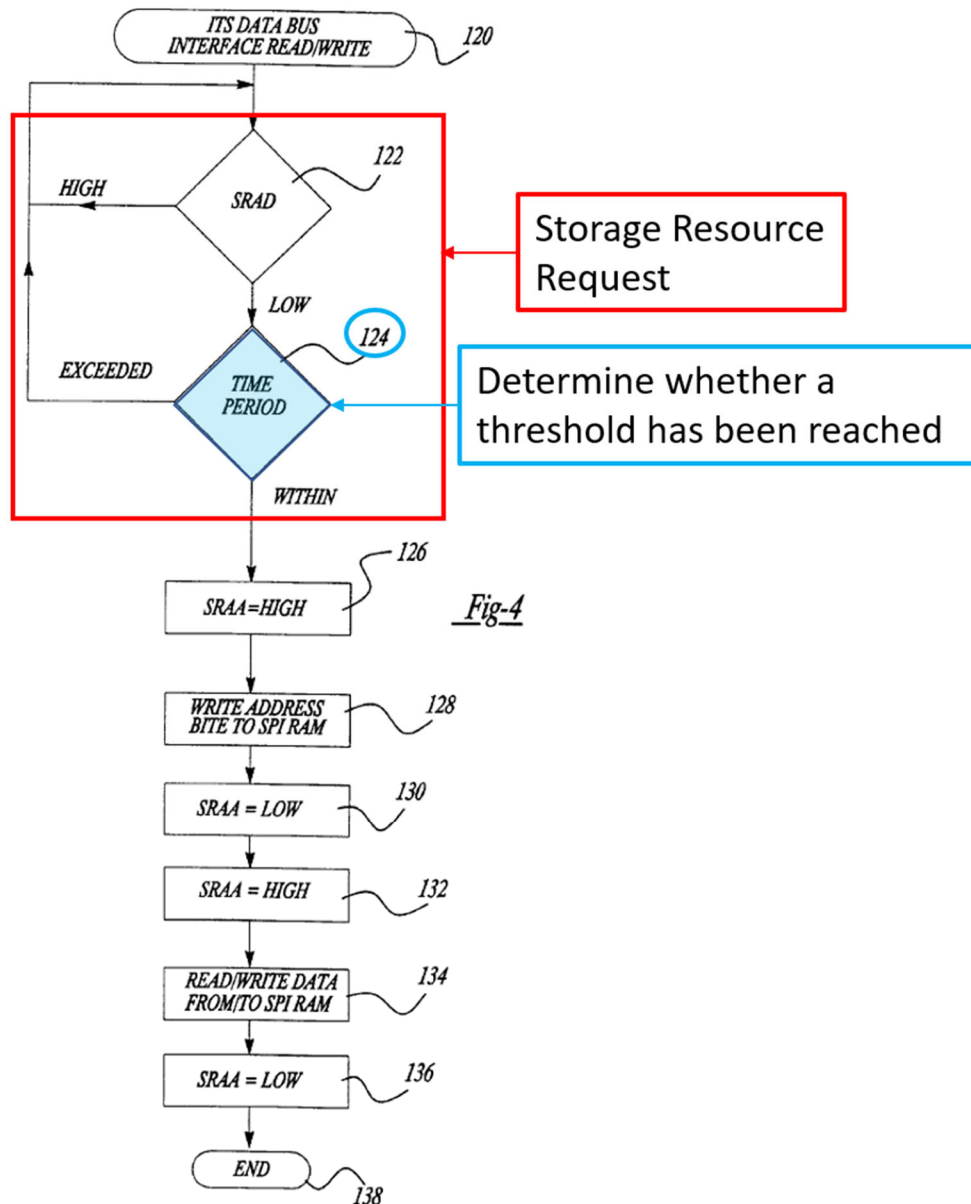
returns to block 122,” but “[i]f SRAD is low, SPIRAM 64 is available.” *Miesterfeld*, 4:22-26, 5:38-43, 6:33-40. Checking the state of SRAD to determine if another bus interface is accessing the storage resource corresponds to “determining whether the storage resource is available to store the sensor information.” Ex-1003, 135.¹⁵

7. Claim 1[g]: “determining whether a threshold tracked since the issuance of the storage resource request has been reached indicating that the storage resource has not been available in association with the threshold tracked since the issuance of the storage resource request;”

Miesterfeld discloses determining whether a threshold tracked since issuance of the storage resource request has been reached. *Miesterfeld*, 6:46-50. As shown in annotated FIG. 4, *Miesterfeld* discloses that “[w]hen ITS data bus interface 58 determines that SPI RAM 64 is available, ITS data bus interface 58 sets the SRAA signal line high, as shown at block 126” and that “in a preferred embodiment, setting SRAA high must occur within 5 micro-seconds after determining that the SRAD signal line is low.” *Miesterfeld*, 6:40-45. By checking in step 124 whether the 5-microsecond threshold has been reached in connection with the storage resource request (**red**), *Miesterfeld*’s process determines whether a threshold has been reached

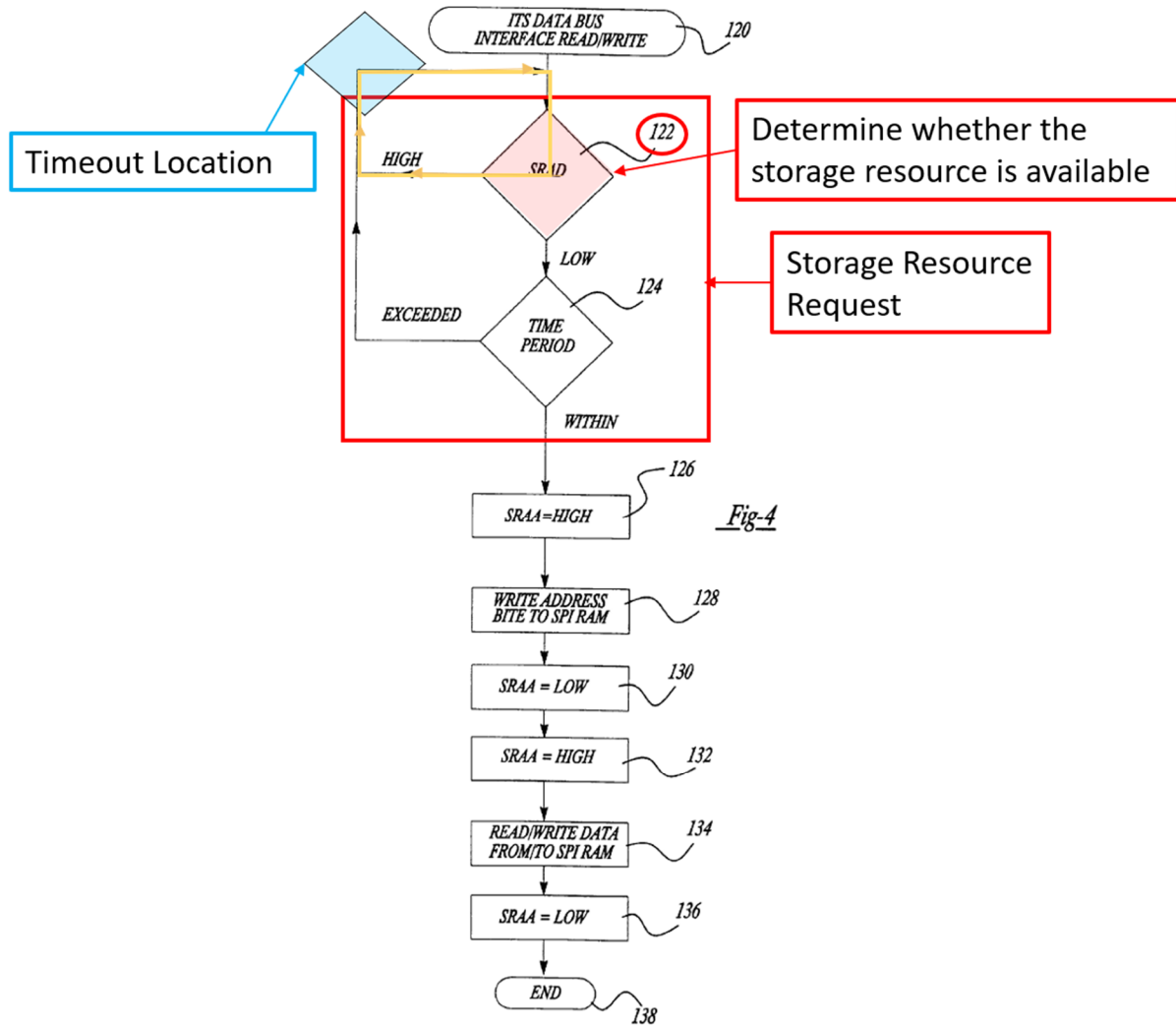
¹⁵ The Board previously found that *Miesterfeld* discloses determining whether a storage resource is available based on the storage resource request. Ex-1017, 41; Ex-1018, 60; Ex-1016, 33; Ex-1023, 38.

in association with the storage resource request. Ex-1003, 136. Because the countdown to 5 microseconds begins as soon as the SRAD signal line is determined to be low, the threshold (a timeout) is “tracked since the issuance of the storage request.” *Id.*



Miesterfeld, FIG. 4 (annotated)

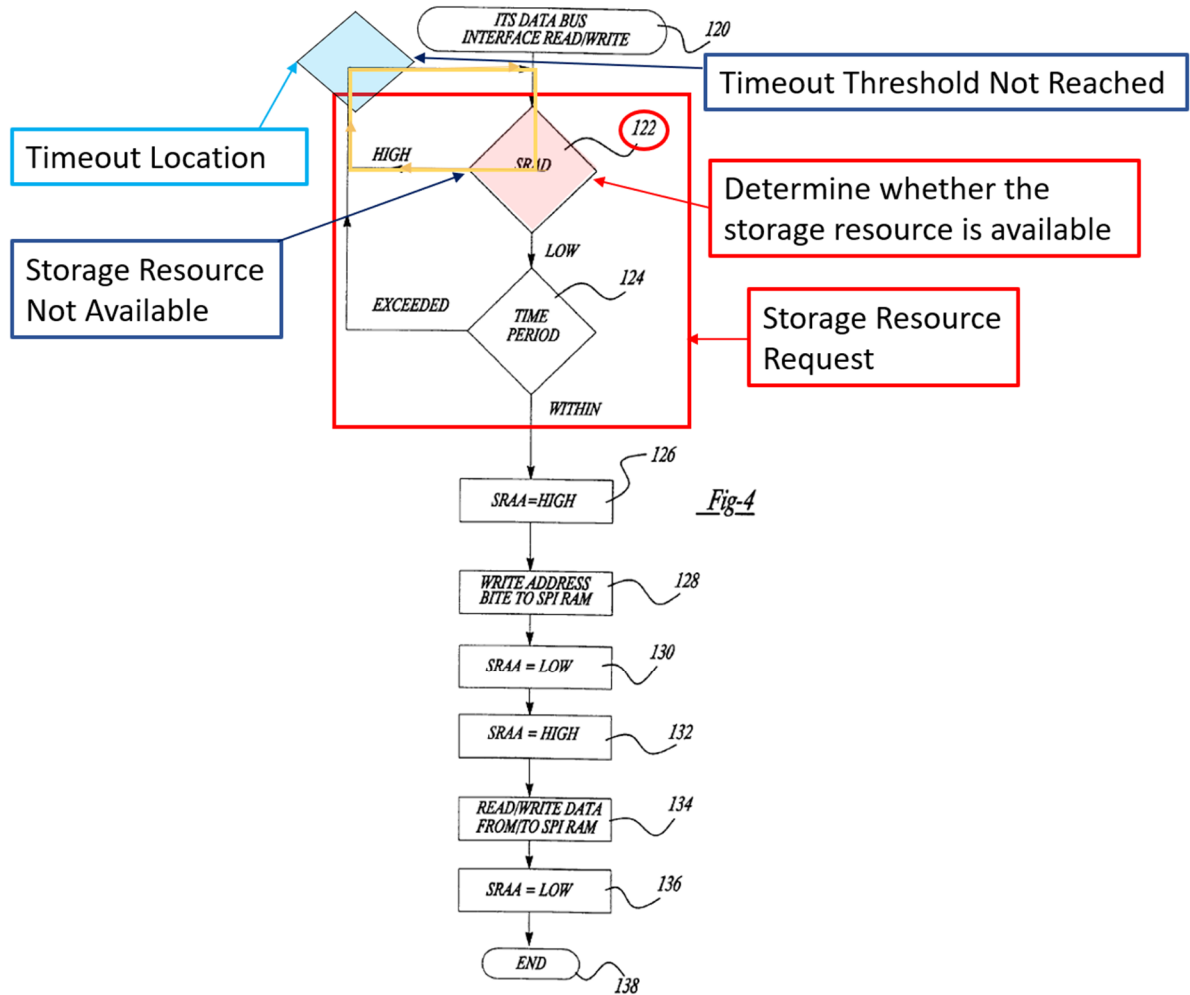
To the extent Patent Owner disputes this, *Stewart* teaches a multiprocessor synchronization method in which a “bounding wait time” (threshold) is implemented to “guarantee that tasks will get the data they require on time, every time.” *Stewart*, 11. *Stewart* also teaches implementing a “time-out mechanism” (threshold) for preventing data transfer when a “pre-specified time or number of retries” elapses. *Id.* (emphasis added); Ex-1003, 137. It would have been obvious to a POSITA to modify *Miesterfeld*’s process to implement a timeout threshold (blue) in the logical loop (yellow) as illustrated in annotated FIG. 4 below to ensure timely and consistent data exchange. Ex-1003, 138.



Miesterfeld, FIG. 4 (annotated)

8. **Claim 1[h]: “when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has not been reached indicating that the storage resource has not been available in association with the threshold tracked since the issuance of the storage resource request, issuing, by the at least one hardware processor to the storage resource included in the automotive electronic control unit, another storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information;”**

Miesterfeld discloses repeating the storage resource request if SRAD is high (issuing another storage resource request “when the storage resource is not available”). *Miesterfeld*, FIG. 4. As discussed above in element 1[g], *Stewart*'s timeout operates by preventing data transfer if the number of retries has not been exceeded; thus, the combination is such that *Miesterfeld*'s request repeats if a “pre-specified” number of retries have not elapsed. *Stewart*, 11; Ex-1003, 139.



Miesterfeld, FIG. 4 (annotated)

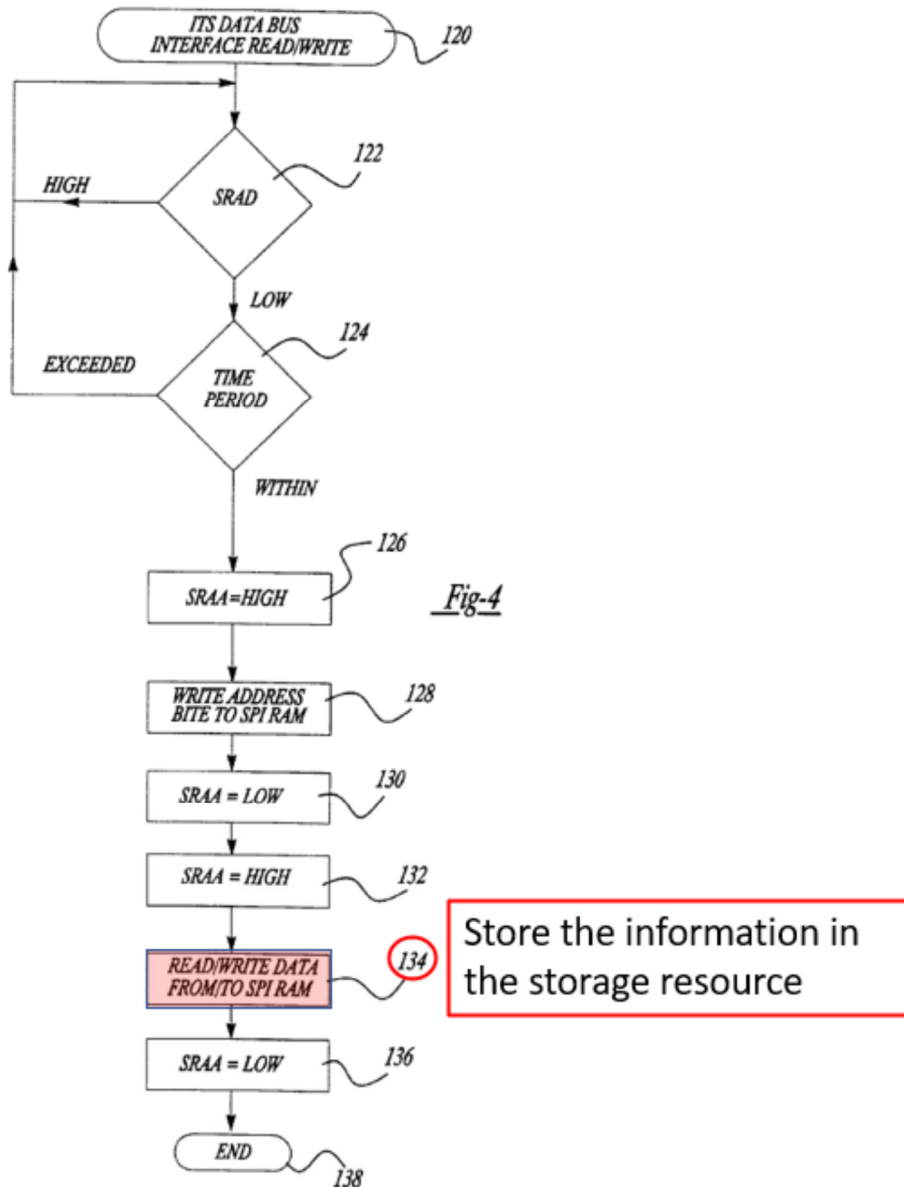
- 9. Claim 1[i]: “when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request or the another storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has been reached, sending an error notification; and”**

Miesterfeld in combination with *Stewart* teaches sending an error notification when the threshold is reached. *Stewart* discloses that “error handlers should be installed to detect tasks that suffer successive time-out errors.” *Stewart*, 11.

A POSITA would have understood that *Stewart*'s error handlers detect the error and provide error notification. Indeed, a POSITA would have understood that error detection without notification is useless. Such notification may have been embodied as an exit code or error message. Thus, it would have been further obvious to a POSITA to modify *Miesterfeld*'s system to incorporate error handlers, such handlers providing an error notification in the form of e.g., an exit code or an error message, as at least suggested by *Stewart*. Ex-1014, 42-45, 54-56, 59-60 (explaining that using a timeout to prevent deadlock, which could lead to program failure, was well-known in the art); Ex-1003, 140-141.

10. Claim 1[j]: “when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request or the another storage resource request, to be available, storing the sensor information utilizing the storage resource;”

Miesterfeld discloses storing the information using the shared memory if the memory is available because *Miesterfeld* discloses that the ITS data bus stores data in the SPI RAM (shared memory/storage resource) after the “ITS data bus interface 58 determines that the SPI RAM 64 is available,” and sets the SPI RAM Access Required (SRAA) signal line to high. *Miesterfeld*, 6:40-54; Ex-1003, 142.



Miesterfeld, FIG. 4 (annotated)

11. Claim 1[k]: “wherein the automotive electronic control unit is operable such that the sensor information is capable of being shared in less than one second, and”

Miesterfeld discloses that “the time period between selecting the desired memory page and reading/writing data to SPI RAM 64 (between steps 130 and 132) is less than 5 microseconds.” *Miesterfeld*, 6:60-63, FIG. 4. *Miesterfeld* also explains

that the VDB interface may transmit any data received from the ITS data bus within **40 milliseconds**. *Id.*, 8:51-56. Thus, *Miesterfeld* discloses that the data is capable of being shared in less than one second. Ex-1003, 143.

12. Claim 1[|]: “the automotive electronic control unit includes a plurality of interfaces including: a first interface; and a second interface for interfacing with a network, where the network is at least one of a Controller Area Network, a Flexray network, or a Local Interconnect Network.”

Miesterfeld’s gateway includes an ITS data bus interface for interfacing with an ITS data bus (a first network) and interconnected devices 20 and 22, and a VDB interface for interfacing with a VDB (a second network) and interconnected devices 16 and 18. *Miesterfeld*, FIG. 1, 3:20-25. Thus, *Miesterfeld* discloses a first interface and a second interface for interfacing with a network of interconnected devices. Ex-1003, 144.

Miesterfeld at least suggests that the network is at least one of a Controller Area Network (CAN), a Flexray network, or a Local Interconnect Network (LIN) because the ITS data bus 24 (first network) may be “any of a number of ITS data buses, such as D2B, USB, IDB, Firewall, and the like” (*Miesterfeld*, 4:5-10, 9:55-57) and the VDB 14 (second network) may be “configured to implement the J1850 configuration as prescribed by the Society of Automotive Engineers (SAE) or any other industry standard as may be required.” *Id.*, 4:7-10; Ex-1003, 145.

To the extent Patent Owner disputes this, *Wense* teaches that cars utilize “[s]everal multiplex protocols,” including CAN (*e.g.*, for engine and body control networks), FlexRay (*e.g.*, for safety, braking, and steering systems), and LIN (*e.g.*, for cost-critical distributed body electronics). *Wense*, 11; Ex-1003, 51, 146.

A POSITA would have found it obvious to implement *Miesterfeld*’s VDB and ITS using known bus architectures like CAN, FlexRay, or LIN, as taught by *Wense*, because each was a commonly-used and well-known vehicle data bus for controlling the various vehicle systems of *Miesterfeld*. *Wense*, 11; *Miesterfeld*, 4:7-10; Ex-1020, 31, 40, 48 (explaining concurrent use of legacy bus architectures such as CAN, LIN, FLEXRAY “provides for the total integration of vehicle systems and functions, and permits plug-and-play device integration, scalability and upgradeability.”); Ex-1021, 1:21-32; Ex-1004, 2 (“[t]he automotive industry has developed the [CAN] [] in the 1980s and subsequently added new communication bus systems such as MOST, IDB, LIN, and FlexRay.”); Ex-1003, 147.

13. Independent Claim 27

As discussed above in Ground 1, independent claim 27 largely mirrors independent claim 1. The differences are accounted for and rendered obvious by the combination for the same reasons set forth for independent claim 1. Ex-1003, 148.

For example, as discussed for 1[1], *Miesterfeld* discloses an ITS data bus interface for interfacing with an ITS data bus (first network) and interconnected

devices 20 and 22, and a VDB interface for interfacing with a VDB (second network) and interconnected devices 16 and 18. *Miesterfeld*, FIG. 1, 3:20-25. *Wense* renders obvious the first network being one of a Controller Area Network, a FlexRay network, or a Local Interconnect Network; and the second network being another one of the Controller Area Network, the FlexRay network, or the Local Interconnect Network. *Wense*, 11; *see also* Ex-1020, 31, 40, 48; Ex-1021, 1:21-32; Ex-1032, 6 (identifying “advantages of multiple vehicle network architecture”); and Ex-1003, 149.

14. Claims 2-7 and 28-33: sharing “in less than one [millisecond/second].”

Claims 2-7 and 28-33 are obvious over *Miesterfeld*, in combination with *Wong*, *Stewart*, and *Wense*. Dependent claims 2-7 and 28-33 each require some sharing event to occur “in less than one second,” “in less than one millisecond,”¹⁶ or “with sufficient speed for use in connection with an automotive device.” As explained for 1[k], *Miesterfeld* discloses sharing and storing of information across networks occurs within microseconds. *Miesterfeld*, 6:43-62, 8:51-56; Ex-1003, 150.

Claim 7 requires the system to be configured for sharing “with sufficient speed for use in connection with an automotive device.” Ex-1001, 13:44-47. *Miesterfeld*

¹⁶ Claim 33 requires the computer program product to be configured for sharing “in less than the one millisecond second [*sic*].”

discloses this limitation because, as explained for 1[k], data is written and read (shared) in under 5 microseconds. *Miesterfeld*, 6:60-62. A POSITA would have understood that this speed is “sufficient” “for use in connection with an automotive device,” as evidenced by the specification of the ’400 patent. Ex-1001,3:45-48; Ex-1003, 151.

F. Ground 3: Claims 8-26 are obvious over *Miesterfeld* in view of *Wong, Stewart, Wense, and Ma*

*Ma*¹⁷ teaches apparatuses and methods for processing data packets in the data communications field. *Ma*, 1:7-10. *Ma* teaches that data packets include a data field and one or more header fields whereby the packet headers and their functions are “typically” arranged in an orderly fashion according to the open-systems interconnection (OSI) reference model (*id.*, 1:26-31) and explains that the OSI model partitions packet communications functions into layers, each layer having a header stripped or prepended during data processing. *Id.*, 5:48-63. *Ma* simply clarifies what the standard components for data transmission are. Thus, a POSITA would have had a reasonable expectation of success in configuring *Miesterfeld*’s interfaces to transmit sensor information using the OSI Reference model, whereby the information is packaged into a packet of layers, as taught by *Ma*, and the

¹⁷ *Ma*, filed December 11, 2000, is prior art under at least pre-AIA 35 U.S.C.

§102(e).

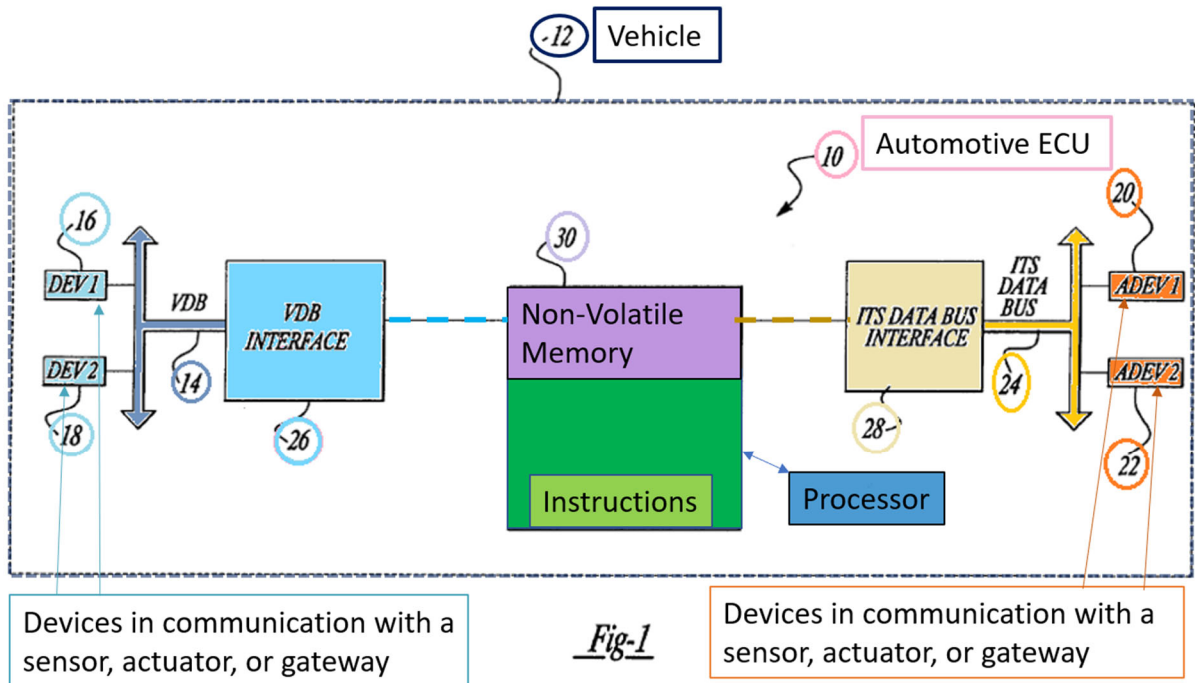
modification would have required only ordinary skill. Ex-1003, 52, 152. Implementing a datalink layer component for using data link layer header bits associated with the first network (CAN, LIN or FlexRay) and a network layer component for using the CAN, LIN or FlexRay network layer header bits, would have been routine for the same reasons. *Id.*

1. Independent Claim 8

Independent claim 8 largely mirrors claim 1, as explained in Ground 1. The differences are obvious for the same reasons. As discussed for 1[1], *Miesterfeld* further discloses that the gateway includes a plurality of interfaces—an ITS data bus interface for interfacing with an ITS data bus (first network) and interconnected devices 20 and 22 and a VDB interface for interfacing with a VDB (second network) and interconnected devices 16 and 18. *Miesterfeld*, FIG. 1, 3:20-25. Thus, *Miesterfeld* discloses a “first network” (VDB) and corresponding “first interface” (VDB Interface), a “second network” (ITS data bus) and corresponding “second interface” (ITS data bus interface). Ex-1003, 153-154.

A POSITA would have found it obvious to implement *Miesterfeld*’s VDB and ITS using known bus architectures like CAN, FlexRay, or LIN, as taught by *Wense*, because each was a commonly-used and well-known for controlling the various vehicle systems of *Miesterfeld*. *Wense*, 11. The proposed modification also teaches that the first and second network are “at least one of the Controller Area Network

type, the Flexray network type, or the Local Interconnect Network type.” *Id.*
Annotated figure 1 below illustrates the combination. Ex-1003, 154.



Miesterfeld, FIG. 1 (annotated)

Claim 8 also recites additional obvious features of the first and second interfaces.

- a. the first interface including a first interface-related data link layer component for using first network-related data link layer header bits and a first interface-related network layer component for using first network-related network layer header bits,

A POSITA would have found it obvious to provide, or understood that *Miesterfeld*'s VDB interface includes, a datalink layer component for using first network-related data link layer header bits and a first interface-related network layer

component for using first network-related network layer header bits because, as discussed in Ground 1, the industry standard for network communication at the time of the invention, required as much to facilitate communication using CAN, LIN, and FlexRay networks. A POSITA would have found it necessary and obvious in view of the industry standards to provide *Miesterfeld*'s VDB interface with a "network layer component for using first network-related header bits" to facilitate communication between either dissimilar network protocols or of messages that are too large for the data link layer. Ex-1003, 156.

To the extent Patent Owner disputes this, *Ma* discloses transmitting data, as was well known in the communications field, in a "packet," including a data field and header field. *Ma*, 1:14-17. The data field contains "virtually any kind of digital data" and the header field conveys information identifying, *e.g.*, the packet's source or destination, the protocol to be used to interpret the packet, or the packet's place in a sequence of packets. *Id.*, 1:18-25. *Ma* further discloses that the packet headers and their functions are "typically" arranged according to the open-systems interconnection (OSI) reference model in a plurality of hierarchical layers. *Id.*, 1: 28-34. Regarding the first three layers of the hierarchy, *Ma* states:

Layer 1, the physical layer, is concerned with transmission of a bit stream over a physical link. Layer 2, the data link layer, provides mechanisms for the transfer of frames of data across a single physical link, typically using a link-layer header on each frame. Layer 3, the

network layer, provides network-wide packet delivery and switching functionality—the well-known Internet Protocol (IP) is a layer 3 protocol.

Id., 1:34-41; *see also* Ex-1029, 6, 33 (explaining that the network layer facilitates data transmission across the data link layer. Thus, *Ma* teaches data link layer and network layer header bits, and corresponding mechanisms (components) for using the bits. Ex-1003, 157.

It would have been obvious to a POSITA to configure *Miesterfeld*'s VDB interface to transmit sensor information using the OSI Reference model, whereby the information is packaged into a packet of layers, as taught by *Ma*, to facilitate data transfer (sensor information transfer) and provide network-wide packet delivery. Ex-1003, 158. This configuration would have ensured compliance with the ISO and OSI reference model. *Id.*

A POSITA would have further understood that the modification is such that the VDB interface includes a datalink layer component for using data link layer header bits associated with the first network (CAN, LIN or FlexRay) and a network layer component for using the CAN, LIN or FlexRay network layer header bits, because the interface needs to have the requisite “mechanisms” (components) to enable the transfer. *Ma*, 1:35-38; Ex-1003, 159.

- b. the second interface including a second interface-related data link layer component for using second network-related data link layer header bits and a second interface-related network layer component for using second network-related network layer header bits, where the second network is at least one of the Controller Area Network type, the Flexray network type, or the Local Interconnect Network type.**

A POSITA would have found it obvious to, or understood that *Miesterfeld's* ITS data bus interface (second interface) includes, a second interface-related data link layer component for using second network-related data link layer header bits and a second interface-related network layer component for using second network-related network layer header bits for the same reasons explained in for the VDB interface (first interface). *See also* Ex-1031, 5-6, Figure 5 (explaining that ITS data bus protocol is based on the ISO and OSI reference model). Ex-1003, 160.

2. Claim 9: “The apparatus as recited in claim 8, wherein the apparatus is operable such that network layer translation is capable of being avoided.”

Miesterfeld discloses that network layer translation is avoidable because *Miesterfeld* uses data lines to read and output data. *Miesterfeld*, 5:20-31. *Miesterfeld* discloses that VDB interface 62 communicates with SPI RAM 64 through a pair of data lines 66a, 66b, and a serial clock line 66c to define SPI bus 66. *Id.*, 5:20-22. Line 66a is a master-in-slave-out (MISO) data line that enables a master device to read data from the slaved SPI RAM 64, data line 66b is a master-out-slave-in (MOSI) data line that enables a master device to output data to the slaved SPI RAM 64, and

the VDB and ITS data bus interfaces each function as master devices with respect to slaved device SPI RAM 64. *Id.*, 5:22-31. A POSITA would have understood that *Miesterfeld*'s system translates between VDB and ITS buses without network layer translation because it uses bus lines which do not need to use network level addresses. Ex-1003, 161.

3. Claims 10 and 11: sharing “in less than one [millisecond/second].”

Dependent claims 10 and 11 recite identical limitations to dependent claims 2 and 3 are obvious for the same reasons. Ex-1003, 162.

4. Claim 12: “The apparatus as recited in claim 11, wherein the apparatus is operable such that the sensor information is shared by the second interface-related network layer component using the second network-related network layer header bits by adding the second network-related network layer header bits to a data unit including the sensor information, and then the second interface-related data link layer component using the second network-related data link layer header bits by adding the second network-related data link layer header bits to the data unit, before communicating the data unit on a physical link of the second network.”

Ma discloses that data packet transmission includes adding an L2 (data link layer) header to the packet (*i.e.*, stripping and rewriting the packet header), and “prepend[ing]” a network layer header to the packet prior to transmission. *Ma*, 5:40-47, 11:23-33. This packet processing ensures “delivery and interpretation of the packet contents.” *Id.*, 1: 17-21.

Thus, the combination teaches adding the second network-related network layer header bits and adding the second network-related data link layer header bits to the packet, which includes the sensor information, before communicating the data on a physical link of the network. Ex-1003, 163-164; Ex 1022, 2:43-62 (“a transport header, network header and data link header ... [are] attached to the data at each of those layers, with each step typically including data moving and copying, before sending the data as bit packets, over the network, to the second host”).

5. **Claim 13: “The apparatus as recited in claim 12, wherein the apparatus is operable such that the first interface-related data link layer component uses the first network-related data link layer header bits by removing the first network-related data link layer header bits from another data unit, and the first interface-related network layer component uses the first network-related network layer header bits by removing the first network-related network layer header bits from the another data unit so that the sensor information is removed from the another data unit, before the sharing.”**

Ma discloses that when a network interface receives the data packet, the packet’s headers are “modified”—that is, the L2 headers are “stripped” and the backplane header (*i.e.*, the network layer header) is removed. *Ma*, 5:48-61; 11:41-47. Thus, the combination teaches removing the first network-related data link layer header bits (layer 2) from “another data unit” and removing the first network-related network layer header bits (layer 3) from the “another data unit” so that the information is removed from the “another data unit.” Ex-1003, 165-166; Ex 1022,

2:63-3:7 (“headers are removed and data processed in order from the lowest (Physical) layer to the highest (Application) layer” when data packets are received).

6. Claims 14 and 15: “The apparatus as recited in claim 8, wherein the apparatus is operable such that the storage resource request and the another storage resource request are identical [the same].”

As explained for 1[h], *Miesterfeld* discloses repeating the storage resource request process (“issuing ... another storage resource request to access the storage resource”) if SRAD is high (“when the storage resource is not available”). *Miesterfeld*, FIG. 4, 6:33-43. This is the exact procedure described in the ’400 patent’s specification. Ex-1001, 8:36-37. Thus, a POSITA would have understood that *Miesterfeld*’s “the another storage resource request” is identical to, or the same as, “the storage resource request.” Ex-1003, 167.

7. Claims 16 and 17: “The apparatus as recited in claim 8, wherein the apparatus is operable such that the sensor information excludes all [a portion of any] header bits of the message.”

As explained for claim 13, header bits are removed from the data packet upon receipt. Because the data being received in the instant combination is sensor information, a POSITA would have understood that the portion of a message that is “sensor information” excludes all header bits of the message. Ex-1003, 168. If “all header bits of the message” are excluded, then “a least a portion of any header bits”

are necessarily excluded. Thus, claim 17 is obvious for the same reasons as claim 16. *Id.*

8. Claim 18: “The apparatus as recited in claim 8, wherein the apparatus is operable such that the storage resource includes a bulletin board.”

Miesterfeld discloses that the “[m]emory 30 is accessible to both VDB interface 26 and ITS data bus interface 28 so that each interface will be able [to] read from and/or write to memory 30.” *Miesterfeld*, 3:40-43. That is, any network connected to ITS gateway 10 has access to memory 30 and can store data in or retrieve data from the database stored there. A POSITA would have understood that *Miesterfeld*’s database is a “bulletin board” because it enables devices on different networks to read and write data to the database in the memory. Ex-1003, 169; Ex-1023, 50-51 (finding that *Miesterfeld* discloses a bulletin).

9. Claims 19-21: “The apparatus as recited in claim 8, wherein the apparatus is operable such that the error notification is sent, when the storage resource included in the automotive electronic control unit is determined, in response to issuing the [another] storage resource request [and the another storage resource request], to not be available and the threshold tracked since the issuance of the storage resource request has been reached.”

Claims 19-21 are similar as explained in Ground 1. Because, as explained for 1[i], *Miesterfeld* in combination with *Stewart* teaches sending an error notification when the storage resource is determined to be unavailable “in response to issuing the storage resource request or the another storage resource request” and reaching

the threshold, claims 19-20 are obvious for the same reason as 1[i]. Ex-1003, 170-171.

As discussed above in 1[h] and 1[i], *Miesterfeld*'s modified process is iterative such that storage resource may be determined to be unavailable after issuing another request and reaching the threshold. *Miesterfeld*, FIG. 4; *Stewart*, 11. This occurs, for example, when the number of attempts (which includes "the request" and the "another request") exceeds the threshold. *Stewart*, 11. Thus, claim 21 is also obvious over the combination. Ex-1003, 172.

10. Claims 22 and 26: "The apparatus as recited in claim 8, wherein at least one of: the memory storage includes the storage resource; the memory storage does not include the storage resource...."

Claims 22 and 26 require "at least one of" numerous features describing the apparatus of claim 8. Ex-1001, 15:62-16:62, 17:13-2132. These features are listed in the alternative. Because "at least one" of these features, *e.g.*, "the memory storage includes the storage resource," is taught by the combination, claims 22 and 26 are obvious for same reasons explained for claim 8. Ex-1003, 173.

11. Claim 23: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the information associated with the message is identified in another storage resource that stores the information after the message is received."

A POSITA would have understood that *Miesterfeld* at least suggests that one option for facilitating the exchange of sensor information would involve at least

temporarily storing the data in another storage resource because *Miesterfeld* discloses “desirable” data exchange between VDB 14 and ITS data bus 24. *Miesterfeld*, 3:18-24. Ex-1003, 174.

Wong also renders this limitation obvious. As explained for 1[b], *Wong*, discloses systems for facilitating communication between automobile components. *Wong*, abstract, 2:41-45. *Wong*’s components are grouped into logical clusters (each cluster having its own controller for managing information flow among the cluster’s components) and the cluster controllers are interconnected via another data communications bus (bus 28) to enable information flow between clusters. *Id.*, abstract, 2:54-61, 5:34-42. Each cluster has its own local memory, so that information shared between clusters is stored in the cluster controller’s local memory (*id.*, 6:4-9), and “any component in one cluster can share information with any component in another cluster without need for dedicated wiring or specially written code.” *Id.*, abstract; Ex-1003, 175-176.

It would have been obvious to a POSITA to configure *Miesterfeld* to include two storage resources (the storage resource and “another” storage resource”), whereby the other storage resource identifies and stores the information associated with the message, as disclosed by *Wong*, to facilitate data exchange between data buses. Ex-1003, 177; *Wong*, 4:62-67. In this *Miesterfeld-Wong* combination, *Wong*’s storage resource (SPI RAM) is accessed in accordance with *Miesterfeld* (as

explained for 1[e]), and “the another” storage resource is utilized to (at least temporarily) store information shared between the devices (automobile components) and their corresponding VDB or ITS, as taught by *Wong*. Ex-1003, 177.

12. **Claim 24: “The apparatus as recited in claim 8, wherein the apparatus is operable such that the information associated with the message is identified in another storage resource that stores the information after the message is received and before the information is stored utilizing the storage resource, the another storage resource capable of being used for information storage, regardless as to a particular network with which the information is shared.”**

As explained for claim 23, *Wong* teaches identifying the information after receiving, and prior to storing it in local memory. *Wong*’s local memory is capable of storing the information, regardless of the network with which the information is shared. *Wong*, 6:4-9; Ex-1003, 178.

13. **Claim 25: “The apparatus as recited in claim 24, wherein the apparatus is operable such that the information is stored utilizing the another storage resource in response to a corresponding request that is separate from the storage resource request.”**

As explained for claim 23, the combination’s storage resource (SPI RAM) is accessed according to *Miesterfeld* and “the another” storage resource of *Wong* is utilized to (at least temporarily) store information shared between the devices (automobile components) and their corresponding data buses. In this configuration, the request to store information in the local memory (another storage) is separate from the storage resource request, *i.e.*, the request to access shared memory/SPI

RAM 30. Ex-1003, 179; *Wong*, 5:17-42 (explaining that the process of sharing data between controllers (akin to reading/writing data from IDS/VDB to *Miesterfeld*'s shared memory) is distinct from the process of sharing/storing data from the automobile components and the local memory of each controller (akin to reading/writing data from devices 16, 18, 20, 22 to a local memory associated with the VDN and ITS)).

VII. The Board Should Not Exercise Discretion to Deny Institution Under §325(d)

The Board should not exercise its discretion to deny institution under §325(d) because none of the references or arguments relied upon in this Petition were substantively considered by the Examiner. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8-9 (2020) (precedential) (citing *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17-18 (2017) (precedential)). This Petition also relies on new references—*Lohrmann* and *Ma*, which were never before the Examiner.

Advanced Bionics: part 1

Petitioner acknowledges that certain references relied upon herein are cited on the face of the '400 Patent. Ex-1001. This point is trivial, however, because the Examiner neither applied these references in any rejection, nor evaluated the particular combination of references set forth in Grounds 1-3. *See generally* Ex-

1008. The arguments presented herein do not overlap with arguments presented during prosecution. Accordingly, Petitioner submits that the first part of the *Advanced Bionics* framework is not satisfied because the Petition includes grounds based on combinations of prior art not previously presented to the Office.

Advanced Bionics: part 2

To the extent the Board determines an analysis under part 2 of *Advanced Bionics* is warranted, Petitioner submits that the asserted grounds demonstrate that the Examiner erred in its evaluation of the cited prior art. Accordingly, Petitioner submits that the evidence and facts presented in the Petition warrant reconsideration of the prior art, and respectfully requests the Board decline to exercise its discretion to deny institution under 325(d).

VIII. Mandatory Notices

A. Real Party-in-Interest Under 37 C.F.R. §42.8(b)(1)

The real parties-in-interest are BMW of North America, LLC and Bayerische Motoren Werke, AG.

B. Related Matters Under 37 C.F.R. §42.8(b)(2)

To the best of Petitioner's knowledge, the '400 patent is not involved in any related matters.

C. Lead and Back-Up Counsel Under 37 C.F.R. §42.8(b)(3)

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D. Service Information Under 37 C.F.R. §42.8(b)(4)

Please address all correspondence to lead counsel and back-up counsel at the addresses shown above. Petitioner also consents to electronic service by email at BMW-Stragent-IPRs@finnegan.com.

IX. Grounds for Standing

Petitioner certifies that it is not barred or estopped from requesting *inter partes* review.

X. Conclusion

Petitioner has established that it is more likely than not that at least one challenged claim is unpatentable and respectfully requests institution.

Dated: December 30, 2022

Respectfully submitted,

/Lionel M. Lavenue/
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Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. §42.24(a)(1)(ii), the undersigned hereby certifies that the foregoing PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 11,188,400 contains 13,788 words, excluding parts of this Petition exempted under §42.24(a), as measured by the word-processing system used to prepare this paper.

Dated: December 30, 2022

/Lionel M. Lavenue/
Lionel M. Lavenue (Reg. No. 46,859)
Counsel for Petitioner

CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the above Petition for *Inter Partes* Review of U.S. Patent No. 11,188,400, the associated Power of Attorney, and Exhibits 1001 through 1032, were served on December 30, 2022 via Priority Mail Express on the correspondence address of record with the USPTO as follows:

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A courtesy copy has also been mailed to the following:

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Dated: December 30, 2022

By: Lisa C. Hines/
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