UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BMW OF NORTH AMERICA, LLC,
Petitioner,

v.

STRAGENT, LLC,
Patent Owner.

Case No. IPR2023-00333
U.S. Patent No. 11,188,400

DECLARATION OF DR. VIJAY K. MADISETTI

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1[b] and 1[c]: "at least one hardware processor in hardwired communication with the memory storage,.....39

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1[d]: "receiving sensor information associated with a message;" 39

1[e] and 1[f]: "in response to receiving the sensor information, issuing, by the at least one hardware processor and to a storage resource included in the automotive electronic control unit, a storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information and, in response to issuing the storage resource request, determining whether the storage resource is available to store the sensor information;".....39

1[g]: "determining whether a threshold tracked since the issuance of the storage resource request has been reached indicating that the storage resource has not been available in association with the threshold tracked since the issuance of the storage resource request;" 41

1[h]: "when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has not been reached indicating that the storage resource has not been available in association with the threshold tracked since the issuance of the storage resource request, issuing, by the at least one hardware processor to the storage resource included in the automotive electronic control unit, another storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information;".....44

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Claims 2-7, 10, 11, and 28-33: sharing "in less than one [millisecond/second]." 60

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Claims 16 and 17: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the sensor information excludes all [at least a portion of any] header bits of the message." 65

Claim 18: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the storage resource includes a bulletin board." 66

Claims 19-21: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the error notification is sent, when the storage resource included in the automotive electronic control unit is determined, in response to issuing the [another] storage resource request [and the another storage resource request], to not be available and the threshold tracked since the issuance of the storage resource request has been reached."....66

Claims 22 and 26: "The apparatus as recited in claim 8, wherein at least one of: the memory storage includes the storage resource; the memory storage does not include the storage resource…."....68

Claim 23: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the information associated with the message is identified in another storage resource that stores the information after the message is received." 68

Claim 24: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the information associated with the message is identified in another storage resource that stores the information after the message is received and before the information is stored utilizing the storage resource, the another storage resource capable of being used for information storage, regardless as to a particular network with which the information is shared."....69

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A POSITA Would Have Been Motivated to Combine *Miesterfeld*, *Wong*, *Stewart*, and *Wense*....77

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Claim 1[preamble]: "A system, comprising:"....78

1[a]: "an automotive electronic control unit including a memory storage comprising instructions, and"....78

1[b] and 1[c]: "at least one hardware processor in hardwired communication with the memory storage, wherein the at least one hardware processor executes the instructions for:"....80

1[d]: "receiving sensor information associated with a message;"....81

1[e]: "in response to receiving the sensor information, issuing, by the at least one hardware processor and to a storage resource included in the automotive electronic control unit, a storage resource request to access the storage

resource included in the automotive electronic control unit to store the sensor information and,”.....82

1[f]: “in response to issuing the storage resource request, determining whether the storage resource is available to store the sensor information;”.....84

1[g]: “determining whether a threshold tracked since the issuance of the storage resource request has been reached indicating that the storage resource has not been available in association with the threshold tracked since the issuance of the storage resource request;”.....85

1[h]: “when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has not been reached indicating that the storage resource has not been available in association with the threshold tracked since the issuance of the storage resource request, issuing, by the at least one hardware processor to the storage resource included in the automotive electronic control unit, another storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information;”.....89

1[i]: “when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request or the another storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has been reached, sending an error notification; and”.....90

1[j]: “when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request or the another storage resource request, to be available, storing the sensor information utilizing the storage resource;”.....91

1[k]: "wherein the automotive electronic control unit is operable such that the sensor information is capable of being shared in less than one second, and"....93

1[l]: "the automotive electronic control unit includes a plurality of interfaces including: a first interface; and a second interface for interfacing with a network, where the network is at least one of a Controller Area Network, a Flexray network, or a Local Interconnect Network."....93

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Claim 13: "The apparatus as recited in claim 12, wherein the apparatus is operable such that the first interface-related

data link layer component uses the first network-related data link layer header bits by removing the first network-related data link layer header bits from another data unit, and the first interface-related network layer component uses the first network-related network layer header bits by removing the first network-related network layer header bits from the another data unit so that the sensor information is removed from the another data unit, before the sharing." 105

Claims 14 and 15: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the storage resource request and the another storage resource request are identical [the same]." 106

Claims 16 and 17: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the sensor information excludes all [a portion of any] header bits of the message." 106

Claim 18: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the storage resource includes a bulletin board." 107

Claims 19-21: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the error notification is sent, when the storage resource included in the automotive electronic control unit is determined, in response to issuing the [another] storage resource request [and the another storage resource request], to not be available and the threshold tracked since the issuance of the storage resource request has been reached."....107

Claims 22 and 26: "The apparatus as recited in claim 8, wherein at least one of: the memory storage includes the storage resource; the memory storage does not include the storage resource…."....108

Claim 23: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the information associated with the message is identified in another storage resource that stores the information after the message is received." 109

Claim 24: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the information associated with the message is identified in another storage resource that stores the information after the message is received and before the information is stored utilizing the storage resource, the another storage resource capable of being used for information storage, regardless as to a particular network with which the information is shared."....110

Claim 25: "The apparatus as recited in claim 24, wherein the apparatus is operable such that the information is stored utilizing the another storage resource in response to a corresponding request that is separate from the storage resource request."....111

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I, Dr. Vijay K. Madisetti, declare as follows:

I. INTRODUCTION

1. I have been asked to submit this declaration on behalf of BMW of North America, LLC (Petitioner) in connection with a petition for *inter partes* review (IPR) of U.S. Patent No. 11,188,400 (the ’400 patent), which I have been told is being submitted to the Patent Trial and Appeal Board of the United States Patent and Trademark Office by Petitioner. I understand that the ’400 patent is Exhibit 1001 to the petition for IPR of the ’400 patent.

2. Specifically, I have been retained as a technical expert by Petitioner to study and provide my opinions on the technology claimed in, and the patentability or unpatentability of, claims 1-33 of the ’400 patent (“the challenged claims”). For purposes of this declaration, I was not asked to provide any opinions that are not expressed herein.

II. SUMMARY OF OPINIONS

3. This declaration is directed to the challenged claims of the ’400 patent, and sets forth the opinions I have formed, the conclusions I have reached, and the bases for each. Based on my experience, knowledge of the art as of the priority date of the ’400 patent, analysis of prior art references, and the understanding a person of ordinary skill in the art would have had of the claim terms in light of the specification as of the earliest possible priority date, it is my

opinion that the challenged claims of the ’400 patent are unpatentable over the prior-art references[1] discussed below.

III. BACKGROUND AND QUALIFICATIONS

4. I am a tenured Professor in the Colleges of Computing and Engineering at the Georgia Institute of Technology (Georgia Tech). I have worked within the area of embedded computing systems, wireless communications, and digital signal processing for over twenty-five years, and have authored, co-authored, or edited several books and numerous peer-reviewed technical papers in these areas.

5. I received my B. Tech (Hons) in ECE from the Indian Institute of Technology (IIT), Kharagpur, India in 1984. I obtained my Ph.D. in Electrical Engineering and Computer Science at the University of California, Berkeley, in 1989. I received the Demetri Angelakos Outstanding Graduate Student Award from the University of California, Berkeley and the IEEE/ACM Ira M. Kay Memorial Paper Prize in 1989.

6. I joined Georgia Tech in Fall of 1989 and am now a tenured Professor in Electrical and Computer Engineering. I have been active in the areas of computer systems, embedded systems, multimedia (audio, video, speech, wireless,

[1] Each of the references cited predate the earliest possible priority date of the ’400 patent.

etc.), wireless communications, digital signal processing, integrated circuit design (analog & digital), software engineering, system-level design methodologies and tools, and software systems. I have been the principal investigator (PI) or co-PI in several active research programs in these areas, including DARPA's Rapid Prototyping of Application Specific Signal Processors, the State of Georgia's Yamacraw Initiative, the United States Army's Federated Sensors Laboratory Program, and the United States Air Force Electronics Parts Obsolescence Initiative. I have received an IBM Faculty Award and NSF's Research Initiation Award. I have been awarded the 2006 Frederick Emmons Terman Medal by the American Society of Engineering Education for contributions to Electrical Engineering, including authoring a widely used textbook in the design of VLSI digital signal processors.

7. I have created and taught undergraduate and graduate courses in hardware and software design for computer systems, control systems, signal processing and wireless communication circuits at Georgia Tech for the past twenty years.

8. I have been an active consultant to the electronics and automation industries and various research laboratories (including Massachusetts Institute of Technology Lincoln Labs and Johns Hopkins University Applied Physics Laboratory (APL)). I have founded three companies in the areas of embedded

avionics and wireless software, military chipsets involving imaging technology and guidance technologies, and wireless communications. I have supervised the Ph.D. dissertations of over twenty engineers in the areas of computer engineering, signal processing, communications, rapid prototyping, and system-level design methodology, of which five have resulted in thesis prizes or paper awards.

9. My consulting work for MIT Lincoln Labs involved high resolution imaging for defense avionics applications, where I worked in the area of prototyping complex and specialized computing systems. My consulting work for the APL mainly involved localization of objects in image fields, where I worked on identifying targets in video and other sensor fields and identifying avionics computer architectures and circuits for power and space-efficient designs.

10. I have developed wireless baseband and protocol stack software and assembly code for a leading telecommunications handset vendor that focused on efficient realization of speech codecs and echo-cancellation. My work in this regard included creation of software code, and analysis and revision of existing software code. This work spanned approximately three years of industry work between 2000 and 2004.

11. The first of the companies I founded, VP Technologies, offers products in the area of semiconductor integrated circuits, including building computing systems for imaging systems in United States Air Force helicopters. I

remain a director of VP Technologies. The second of these companies, Soft Networks, LLC, offers software for multimedia and wireless computing platforms, including the development of a set-top box for Intel that decodes MPEG-2 video streams and imaging codes for multimedia phones. The technology involved with the design, development, and implementation of the Intel set-top box included parsing the bit streams, decoding communications protocols, extracting image and video data, and then processing for subsequent display or storage. The third of these companies, Elastic Video, uses region of interest based video encoding or decoding for capturing high quality video at very low bit rates, with primary application for wireless video systems.

12. I have been elected a Fellow of the IEEE, for contributions to embedded computing systems. The Fellow is the highest grade of membership of the IEEE, a world professional body consisting of over 300,000 electrical and electronics engineers, with only one-tenth of one percent (0.1%) of the IEEE membership being elected to the Fellow grade each year. Election to Fellow is based upon votes cast by existing Fellows in IEEE.

13. I have authored or co-authored several books, including VLSI Digital Signal Processors (IEEE Press 1995) and the Digital Signal Processing Handbook (CRC Press, 1998). I am also Editor of the three-volume DSP Handbook set: Volume 1: Digital Signal Processing Fundamentals, Volume 2: Video, Speech, and

Audio Signal Processing and Associated Standards, and Volume 3: Wireless, Networking, Radar, Sensory Array Processing, and Nonlinear Signal Processing, published in 2010 by CRC Press, Boca Raton, Florida. I have also authored papers on control circuits related to control of electrical motors and generators.

14. I have designed several specialized computer and communication systems over the past two decades at Georgia Tech for tasks such as wireless audio and video processing and protocol processing for portable platforms, such as cell phones and PDAs. I have worked on designing systems that are efficient from performance, size, weight, area, and thermal considerations. I have developed courses and classes for the industry on these topics, and many of my lectures in advanced computer system design, developed under the sponsorship of the United States Department of Defense in the late 1990s, are available for educational use at "http://www.eda.org/rassp" and have been used by several U.S. and international universities as part of their course work. Some of my recent publications in the area of design of wireless communications systems and associated protocols are listed in Appendix A, my CV.

15. I am knowledgeable and familiar with standards related to the automotive, avionics, wireless and telecommunications systems industries, and as shown in Appendix A, some of my papers describe the application of these standards in optimizing the design and testing of these systems. I am also

knowledgeable and familiar with microprocessor architecture and associated software and firmware design for embedded, wireless and telecommunications terminals and base stations.

16. I have authored, co-authored, or edited several books in the area of computer systems and distributed systems in the past twenty years, including:

- *VLSI Digital Signal Processors*, Madisetti, V.K.
- *Quick-Turnaround ASIC Design in VHDL*, Romdhane, M., Madisetti, V.K., Hines, J.
- *The Digital Signal Processing Handbook (First Edition)*, Madisetti, V. K., Williams, D. (Editors).
- *VHDL: Electronics Systems Design Methodologies*, Madisetti, V. K. (Editor).
- *Platform-Centric Approach to System-on-Chip (SoC) Design*, Madisetti, V. K., Arpnikanondt, A.
- *The Digital Signal Processing Handbook – Second Edition,* Madisetti, V. K. (2009/2010).
- *Cloud Computing: A Hands-On Approach*, A Bahga, V. Madisetti (2013).

- *Internet of Things: A Hands-On Approach*, A Bahga, V. Madisetti (2014).

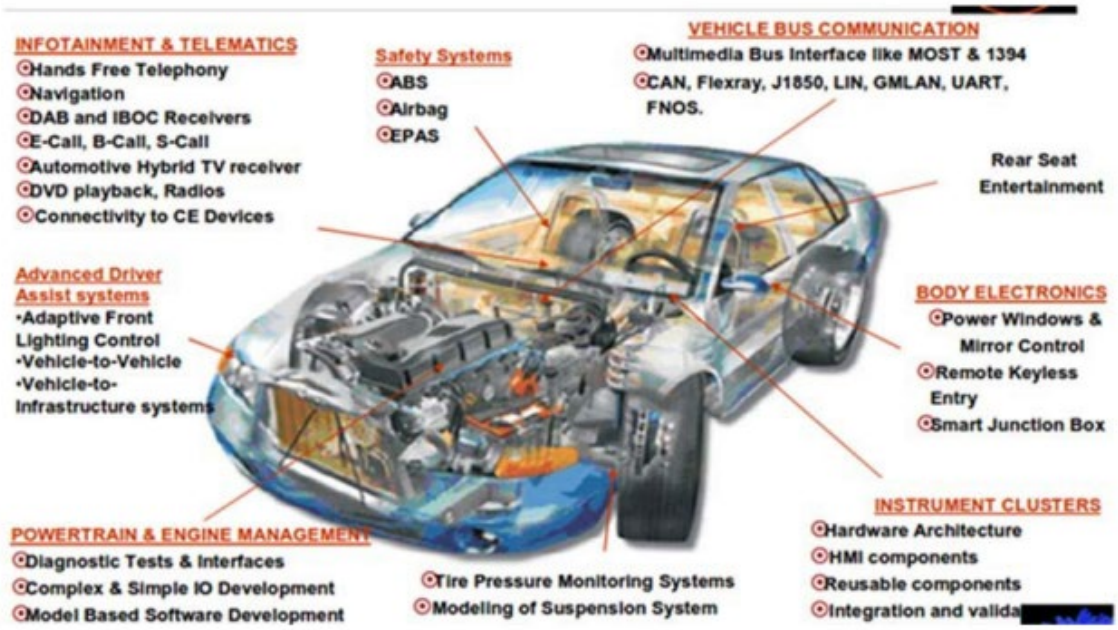
17. In the past decade I have also authored several peer-reviewed papers in the area of computers, computer software applications, and software design, and these include:

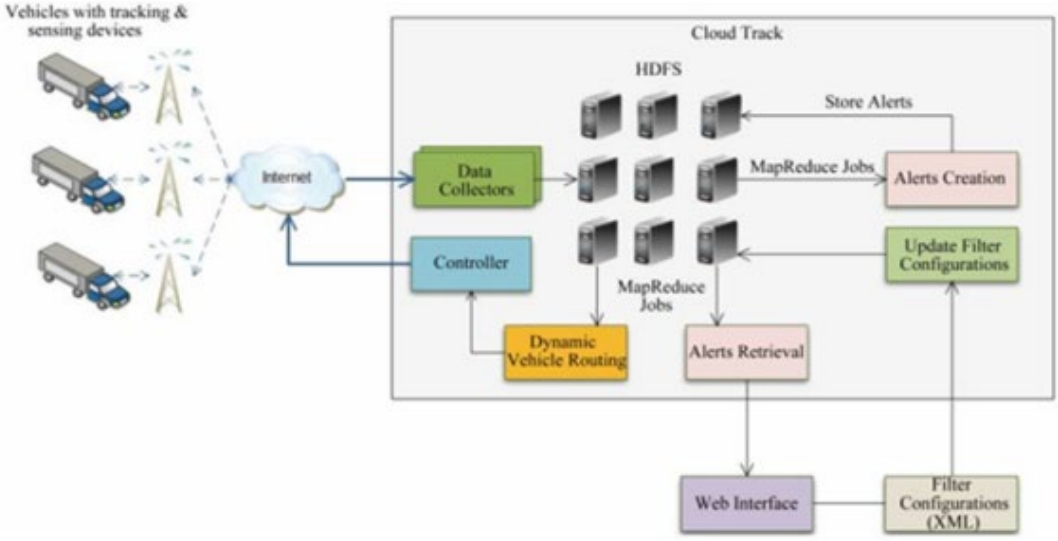
- Madisetti, *et al.*: "*The Georgia tech Digital Signal Multiprocessor, IEEE Transactions on Signal Processing*," Vol. 41, No. 7, July 1993.
- Madisetti, *et al.*, "*Rapid Prototyping on the Georgia Tech Digital Signal Multiprocessor*," IEEE Transactions on Signal Processing, Vol. 42, March 1994.
- Madisetti, "*Reengineering legacy embedded systems*," IEEE Design & Test of Computers, Vol. 16, Vol. 2, 1999.
- V. Madisetti, *et al.*, "*Virtual Prototyping of Embedded Microcontroller based DSP Systems*," IEEE Micro, Vol. 15, Issue 5, 1995.
- V. Madisetti, *et al.*, "*Incorporating Cost Modeling in Embedded-System Design*," IEEE Design & Test of Computers, Vol. 14, Issue 3, 1997.

- V. Madisetti, *et al.*, "*Conceptual Prototyping of Scalable Embedded DSP Systems*," IEEE Design & Test of Computers, Vol. 13, Issue 3, 1996.
- V. Madisetti, "*Electronic System, Platform & Package Codesign*," IEEE Design & Test of Computers, Vol. 23, Issue 3, June 2006.
- V. Madisetti, *et al.*, "*A Dynamic Resource Management and Scheduling Environment for Embedded Multimedia and Communications Platfor*ms," IEEE Embedded Systems Letters, Vol. 3, Issue 1, 2011.

18. Some of my recent work in the automotive area includes predicting travel times of cars on freeways for use in mass transportation, and analysis of travel and logistical data in real-time intelligent transportation networks. Representative publications include "Configuration for Predicting Travel-Time Using Wavelet Packets and Support Vector Regression," Journal of Transportation Technologies, Vol. 3, Issue 3, 2013, and "Cloud-Based Information Technology Framework for Data-Driven Intelligent Transportation Systems," Journal of Transportation Technologies, Vol. 3, No 2, April 2013. I am also a member of SAE (Society of Automotive Engineers).

19. In the late 2000s, I collaborated with a leading automotive supplier to design and development embedded software and electronic control unit (ECU) controller modules in the area of energy profiling for hybrid/gas cars (described in U.S. Provisional Patent App. No. 61/209,403). The system we developed is described in more detail in the figures below:





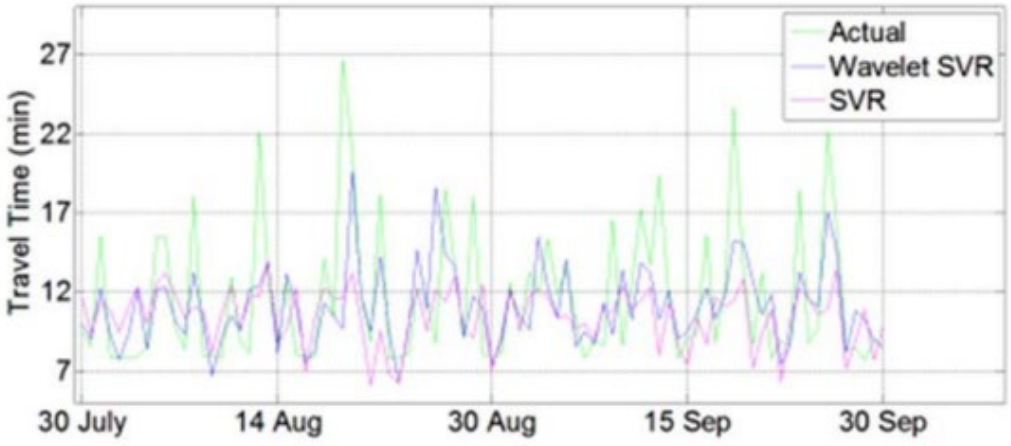


Figure 9. Comparison of actual travel time, and predicted travel-time by Support Vector Regression and Wavelet decomposed Support Vector Regression methods.

20. I have designed and implemented multiple processor computing systems that perform multimedia tasks (*e.g.*, speech and audio recognition) and also avionics/embedded guidance systems since the mid-1990s, and I have also implemented real-time operating systems in the same time frame. Representative

publications of my work in these areas include, "*The Georgia Tech Digital Signal Multiprocessor (DSMP)*," IEEE Transactions on Signal Processing, Vol. 41, Issue 7, 1993, and "*Task Scheduling on the Georgia Tech Digital Signal Multiprocessor*", Proc. IEEE ICASSP 1992. More recent work that is related to multimedia processing on multiprocessor systems can be found in "*A Dynamic Resource Management and Scheduling Environment for Embedded Multimedia and Communications Platforms*," IEEE Embedded Systems Letters, Vol. 3, Issue 1, 2011. Three generations of Digital Signal Multiprocessors (DSMP's) (listed in the table below) were designed at Georgia Tech as part of my research and education efforts.

TABLE II
FEATURES OF THREE GENERATIONS OF DSMP'S

Generation	Name	Processor/Word-length/MFLOPS	Number of Processors	Topology
DSMP-I	OSCAR I	Am29325/32/4	16	2-D grid/torus
DSMP-II	OSCAR-32	WE-DSP32/32/8	2-16	chorded ring
DSMP-III	DSMP-III	TMS320C40/32/40	16-128	3-D grid/torus

Fig. 10. Six-processor DSMP-II.

21. In collaboration with the US Air Force, Lockheed Martin, and Hughes Corporation, I designed and implemented a 192-processor multiprocessor system for processing real-time avionics data (infrared search and track applications – IRST), and this represented one of the largest multiprocessor systems used in the mid-1990s timeframe on aircraft. See my publications, "*Virtual Prototyping of Embedded Microcontroller-Based DSP Systems*," IEEE Micro, 1995, and also "*VHDL TokenBased Performance Modeling for 2D and 3D Infrared Search and Track*," Proc. SPIE VIUF, 1998.

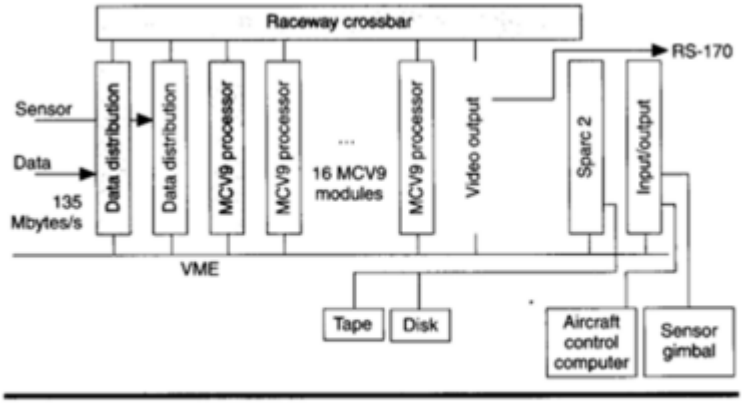


Figure 8. Block diagram of IRST signal processor representing MCV9 boards, data/video distribution, and Sparc cards.[9,11] Shaded components indicate the virtual prototype.

22. I have been active in the area of wireless OFDM-MIMO communications systems for several years, and some of my publications in this area include "*Frequency Dependent Space-Interleaving of MIMO OFDM Systems*," Proc. IEEE Radio and Wireless Conference (RAWCON '03), 2003, "*Embedded Alamouti Space Time Codes for High Rate and Low Decoding*

Complexity," Proc. of IEEE Asilomar Conf. on Signals, Systems and Computers, 2008; and "*Asymmetric Golden Codes for Fast Decoding in Time Varying Channels*," Wireless Personal Communications (2011).

23. Additional representative peer-reviewed publications in this area of wireless embedded systems are the following: (i) Turkboylari, M. and Madisetti, V.K., "*Effect of Handoff Delay on System Performance of TDMA Cellular Systems*," 4th International Workshop, Mobile & Wireless Communication Network, pp. 411- 415, 2002; (ii) Jatunov, L. and Madisetti, V.K., "*Computationally-Efficient SNR Estimation for Bandlimited Wideband CDMA Systems*," IEEE Transactions on Wireless Communications, Issue 12, pp. 3480-3491, December 2006, and (iii) N. Radia, Y. Zhang, M. Tatipamula, V. Madisetti, "*Next Generation Applications on Cellular Networks: Trends, Challenges, and Solutions*," Proceedings on IEEE, vol. 100, Issue 4, pp. 841-854, April 2012. I have significant experience analyzing, designing, and testing systems based on 3GPP Technical Specifications, including specifications describing WCDMA and HSDPA technologies.

24. A copy of my curriculum vitae is attached hereto as Appendix A.

25. Overall, I have used my education, industry, teaching, writing, and membership and service experiences in the computer vision field, and my understanding of the knowledge, creativity, and experience of a person having at

least ordinary skill in the art in forming the opinions expressed in this report, as well as any other materials discussed herein. My extensive experience with embedded computing systems, wireless communications, and digital signal processing is applicable to analyzing the ’400 patent.

26. I am being compensated for services provided in this matter at my usual and customary rate of $500.00 per hour plus travel expenses. My compensation is not conditioned on the conclusions I reach as a result of my analysis or on the outcome of this matter, and in no way affects the substance of my statements in this declaration. I have no financial interest in Petitioners, or any of their subsidiaries. I also have no financial interest in Patent Owner, Stragent, LLC. I do not have any financial interest in the ’400 patent and have not had any contact with the named inventors of the ’400 patent

27. Except as otherwise stated, I have personal knowledge of the facts stated in this declaration, and I have formed the opinions expressed in this declaration based on my expertise, experience, and information that I have reviewed.

IV. MATERIALS REVIEWED

28. In forming my opinions, I read and considered the ’400 patent and its prosecution history, as well as the other materials, exhibits, papers, and previous Board decisions regarding the previous ’477 IPR (in which I also submitted

declarations) referenced and discussed herein and shown in the below table. I have also used my education, industry, teaching, mentoring, writing, and membership and service experiences in the Electrical and Computer Science Engineering fields, and my understanding of the knowledge, creativity, and experience of a person having ordinary skill in the art in forming the opinions expressed in this report, as well as any other materials discussed herein. I have been asked to assume that each of prior art references identified in the analysis section of my declaration qualifies as prior art to the challenged claims of the '400 patent.

Exhibit	Description
Ex-1001	U.S. Patent No. 11,188,400 to Axel Fuchs, et al. ("the '400 patent")
Ex-1002	Prosecution History of the '400 patent
Ex-1004	U.S. Provisional Patent Application No. 60/434,018.
Ex-1005	U.S. Patent Application Publication No. 2003/0223436 A1 to Lohrmann et al ("*Lohrmann*").
Ex-1006	U.S. Patent No. 6,625,169 to Tofano ("*Tofano*").
Ex-1007	U.S. Patent No. 5,202,887 to Ueno et al ("*Ueno*").
Ex-1008	U.S. Patent Application Publication No. 2002/0073243 A1 to Dieter E. Staiger ("*Staiger*").
Ex-1009	U.S. Patent No. 6,141,710 to Frederick O. Miesterfeld ("*Miesterfeld*").
Ex-1010	Stewart et. Al., "*Integration of Real-Time Software Modules for Reconfigurable Sensor-Based Control Systems*," IEEE/RSJ

Exhibit	Description
	International Conference on Intelligent Robots and Systems, Raleigh, North Carolina (July 1992) ("*Stewart*")
Ex-1011	H-C. von der *Wense* et al., "Building Automotive LIN Applications," *Advanced Microsystems for Automotive Applications*, 280-292 (2001) ("*Wense*").
Ex-1012	U.S. Patent No. 6,434,459 to William S. Wong et al ("*Wong*").
Ex-1013	U.S. Patent No. 6,954,463 to Ma ("*Ma*").
Ex-1014	Nick Grattan and Marshall Brian, "*Windows CE 3.0 Application Programming*," (Prentice Hall PTR) (First Ed., 2000).
Ex-1015	The Ohio State University Libraries MARC Record for H-C. von der *Wense* et al., "*Building Automotive LIN Applications*," Advanced Microsystems for Automotive Applications, 280-292 (2001) ("*Wense*").
Ex-1016	IPR2017-00457, Paper 34 (Final Written Decision) (P.T.A.B. June 13, 2018).
Ex-1017	IPR2017-00458 Paper 31 (Final Written Decision) (P.T.A.B. June 13, 2018).
Ex-1018	IPR2017-01502, Paper 24 (Final Written Decision) (P.T.A.B. Dec. 6, 2018).
Ex-1019	International Organization for Standardization 11898-1, First Edition (Dec. 1, 2003).
Ex-1020	U.S. Patent Application Publication No. 2003/0043739 A1 to Juergen Reinold et al.
Ex-1021	U.S. Patent No. 6,934,612 to Remboski et al.
Ex-1022	U.S. Patent No. 7,480,312 to Ossman.
Ex-1023	IPR2021-00417, Paper 29 (Final Written Decision) (P.T.A.B. July 12, 2022).

Exhibit	Description
Ex-1024	MARC Record for Stewart et. al., "Integration of Real-Time Software Modules for Reconfigurable Sensor-Based Control Systems," IEEE/RSJ International Conference on Intelligent Robots and Systems, Raleigh, North Carolina (July 1992)
Ex-1025	IPR2021-00417, Paper 13 (Patent Owner's Response) (P.T.A.B. October 12, 2021).
Ex-1026	IPR2021-00417, Paper 19 (Patent Owner's Sur-Reply) (P.T.A.B. February 28, 2022).
Ex-1027	IPR2017-00676, Paper 11 (Patent Owner's Response) (P.T.A.B. September 21, 2017).
Ex-1028	IPR2017-01502, Paper 10 (Patent Owner's Response) (P.T.A.B. March 12, 2018).
Ex-1029	The Foundation Fieldbus Primer, Fieldbus, Inc. (Rev. 1.1, Jun. 24, 2001)
Ex-1030	Ralf Hadeler and Hans-Jörg Mathony, "*Design of Intelligent Body Networks*," (SAE International) (2000).
Ex-1031	Chuck Powers and Randy Frank, "The *Consumerization of the Automotive Environment: The ITS Data Bus*," (SAE International) (1997).
Ex-1032	Bruce D. Emaus, "*Current Vehicle Network Architecture Trends – 2000*," (SAE International) (2000).

V. LEGAL STANDARDS

29. It is my understanding that there are two ways that prior art references can render a patent claim unpatentable: anticipation and obviousness, based on 35

U.S.C. §§ 102 and 103, respectively. I understand that the petitioner has the burden in an IPR to show unpatentability by a preponderance of the evidence.

A. Obviousness

30. I understand that the claims define the invention. I also understand that an unpatentability analysis is a two-step process. First, the claims of the patent are construed to determine their meaning and scope. Second, after the claims are construed, the content of the prior art is compared to the construed claims. I understand that a claimed invention may be patentable when it is new or nonobvious in light of the "prior art."

31. It is my understanding that a claimed invention is patentable if the differences between the invention and the prior art are such that the subject matter as a whole would not have been obvious to a person having ordinary skill in the art to which the subject matter pertains at the time the invention was made.

32. I have also been advised that several factual inquiries underlie a determination of obviousness. These inquiries include (1) the scope and content of the prior art, (2) the level of ordinary skill in the field of the invention, and (3) the differences between the claimed invention and the prior art.

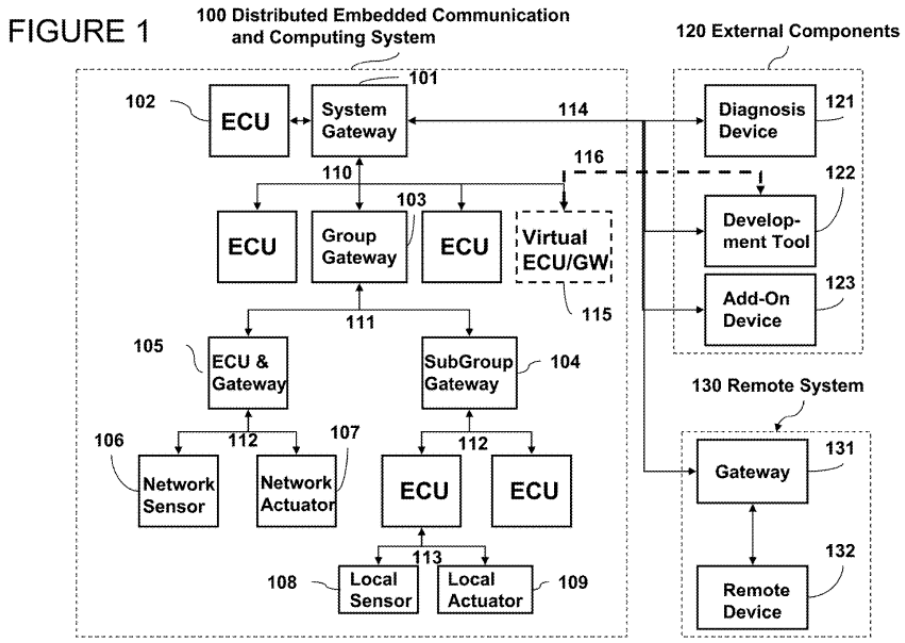
33. I understand that where the prior art fails to disclose a claim element or fails to provide an apparent reason to modify existing prior art in a manner to meet a missing claim limitation, the claimed invention likely is not obvious. In

other words, even if one of ordinary skill in the art would be motivated to combine two references, a claim is likely not obvious if the combination does not produce the claimed invention.

34. I also understand that the existence of each and every element of the claimed invention in the prior art does not necessarily prove obviousness and that most, if not all, inventions rely on building blocks of prior art.

VI. NATURE OF THE INVENTION CLAIMED IN THE '400 PATENT

35. The '400 patent describes systems and methods "for sharing information in a distributed framework." Ex-1001, title, 1:37-38. In automobiles, electronic control units (ECUs) control applications such as the engine, brakes, or diagnostics through connections to sensors and actuators organized into separate subnetworks. *Id.*, 3:22-25. FIG. 1 shows gateways 101, 103, 104, 105, which relay messages through system layers. *Id.*, 3:34-36. Each layer may contain multiple ECUs connected through wired serial multiplexing bus systems. *Id.*

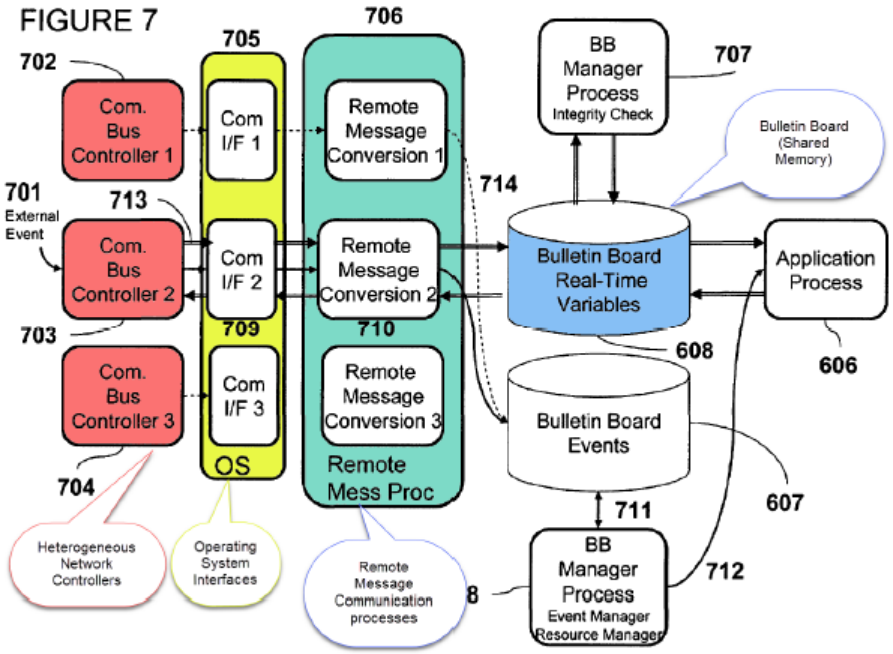


'400 Patent, FIG. 1

36. At the highest level, "the system level," system gateway 101 connects buses to other system-level ECUs, subsequent gateways 103, and external components 120. *Id.*, 4:4-8. ECU 102 receives real-time input variables from networked sensors 106 via multiplexing bus system 112, processes the input and generates output variables that may be shared with other ECUs. *Id.*, 3:50-56.

37. Annotated FIG. 7 shows a bulletin board 608 (blue), which acts as a shared memory for sharing variables. *Id.*, 2:54-57. The bulletin board interacts with multiple communication buses 701-703 (red) and associated operating system interfaces 705 (yellow). *Id.*, 6:46-50. Data received from one communication bus is stored on the bulletin board and shared as a new message with other network types

via remote message communication processes 706 (green) that add/remove network-specific information. *Id*.



Id., FIG. 7 (annotated)

VII. LEVEL OF ORDINARY SKILL IN THE ART

38. I understand a person of ordinary skill in the art (POSITA) is determined by looking at (A) type of problems encountered in the art, (B) prior art solutions to those problems, (C) rapidity with which innovations are made, (D) sophistication of the technology, and (E) educational level of active workers in the field. Based on my experience in this art and accounting for these factors, I believe a person of ordinary skill in the art would have had, as of the relevant date of the '400 patent, at least a bachelor's degree in electrical, computer, or a related

engineering discipline; two years of industry experience in the field of distributed computing or automotive engineering, or equivalent experience; and knowledge or familiarity with in-vehicle computing.

39. Based on my education, training, and professional experience in the field of the claimed invention, I am familiar with the level and abilities of a person of ordinary skill in the art at the time of the claimed invention. I have technically supervised or worked with such individuals at the relevant time and I, myself, also met at least these minimum qualifications at the relevant time. I meet these qualifications today, as well.

VIII. CLAIM CONSTRUCTION

40. I have been informed that the first step in an invalidity analysis involves construing the claims, as necessary, to determine their scope. And, second, the construed claim language is then compared to the disclosure of the prior art. In proceedings before the USPTO, I have been told by counsel that a claim in a patent subject to *inter partes* review should be given their ordinary and customary meaning to a person of ordinary skill in the art at the time of the invention.

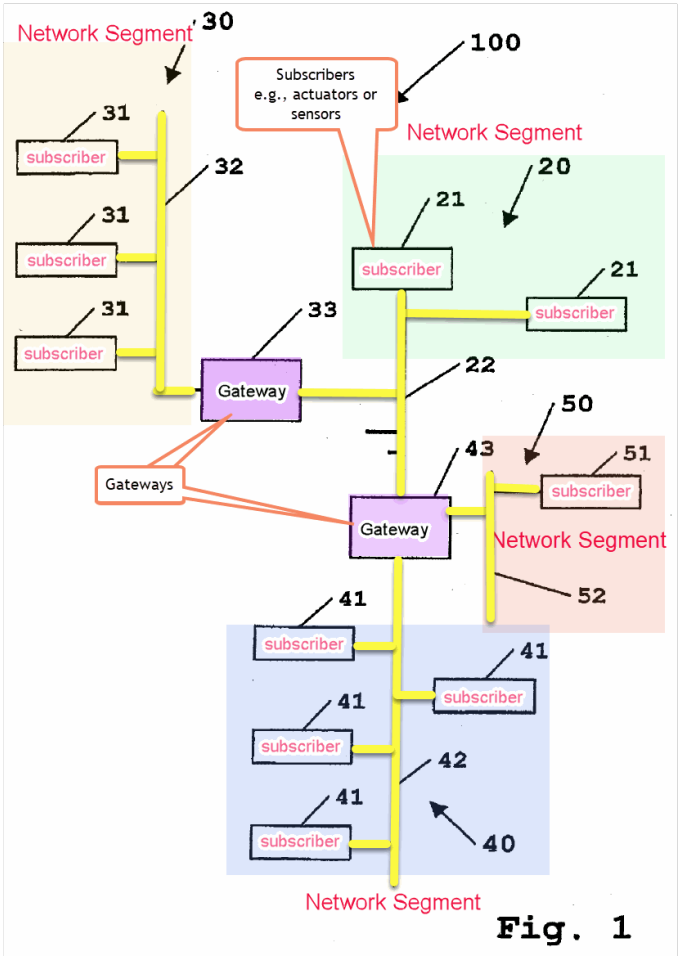
41. In my opinion, the plain and ordinary meaning of the claims applies to each claim term of the ’400 patent.

IX. SUMMARY OF THE PRIOR ART

42. My opinions below relate to the patentability or unpatentability of claims 1-33 of the ’400 patent based on a combination of prior art.

A. Lohrmann

43. *Lohrmann* discloses a system for managing communications networks in automobiles, and particularly a network with a plurality of network segments that are physically connected via gateways. *Lohrmann*, 2, 19. Control units or control unit applications, such as actuators or sensors, are physically connected to one another by respective data buses (CAN, FlexRay, or LIN) and communicate data over the network. *Id.*, 18, 20,21.



Lohrmann, FIG. 1 (annotated)

B. Tofano

44. *Tofano* discloses an integrated communication system that "enable[s] data and information exchanges between various networks and various network formats" and "transparently interconnects different networks," which includes a processor for translating or converting incoming data from a first network format to another network format. *Tofano*, 2:56-62, 15:47-51. *Tofano*'s processor is operably connected to components of the system, and "can be provided with a

suitable software program to execute, thereby enabling the processor to accomplish any required functions for the communication system.*" Id*., 15:56-61. "[E]ach processor … may have the necessary memory, disk, non-volatile storage, I/O, networking and communications peripherals, and other support necessary for it to accomplish the required functions." *Id.*, 3:18-20, 29-32. Thus, *Tofano* also teaches a gateway, having memory storage comprising instructions.

C. Ueno

45. *Ueno* "relates to a direct access storage device (DASD) shared by a plurality of central processing units." *Ueno*, 1:8-10, 2:57-63. Ueno discloses methods for accessing the DASD.

D. Staiger

46. *Staiger* discloses an ECU connected to a plurality of real-time networks, including "several individual CAN [] busses or other multiple purpose networks." *Id.*, ¶ 3. *Staiger*'s ECU executes an application for controlling remote automobile systems while concurrently performing gateway functions between the different networks. *Id.*, ¶¶ 4-5. *Staiger* explains that the CAN, FireWire, and MOST buses are "real-time" buses, capable of "respond[ing] to stimuli within some small upper limit of response time, typically [in] milliseconds or microseconds," such that, upon receiving a message, an intercommunication preprocessor "processes the message and initiates immediate distribution" of an

"output[] message," to, *e.g.*, a "destination unit." *Id.*, ¶¶ 7, 35, 51, claim 1, Abstract.

E. Miesterfeld

47. *Miesterfeld* discloses a data exchange system including a controller for "process[ing] vehicle data to control at least one vehicle related function." *Miesterfeld*, 2:23-27. The controller may be implemented on a vehicle 12 having a vehicle data bus (VDB) 14, an intelligent transportation system (ITS) data bus 28, and corresponding devices, 16, 18, 20, and 22, which "write data to or read data from" their respective data buses. *Id.*, 3:1-16. In operation, the controller ("gateway 10") facilitates data exchange between the VDB and ITS data bus via shared memory 30. *Id.*, 2:36-39, 3:18-20. To "effect such an exchange," the system includes VDB and ITS data bus interfaces which "read [] and write data from" both the data buses and shared memory 30. *Id.*, 20-25. Annotated FIG. 1. illustrates *Miesterfeld*'s data exchange system on vehicle 12.

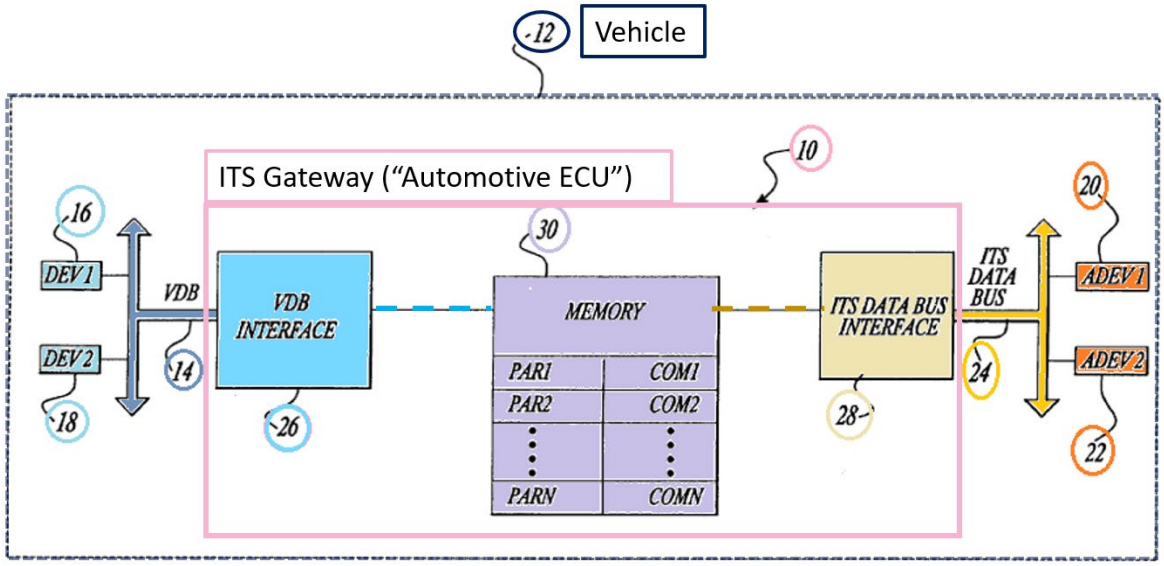
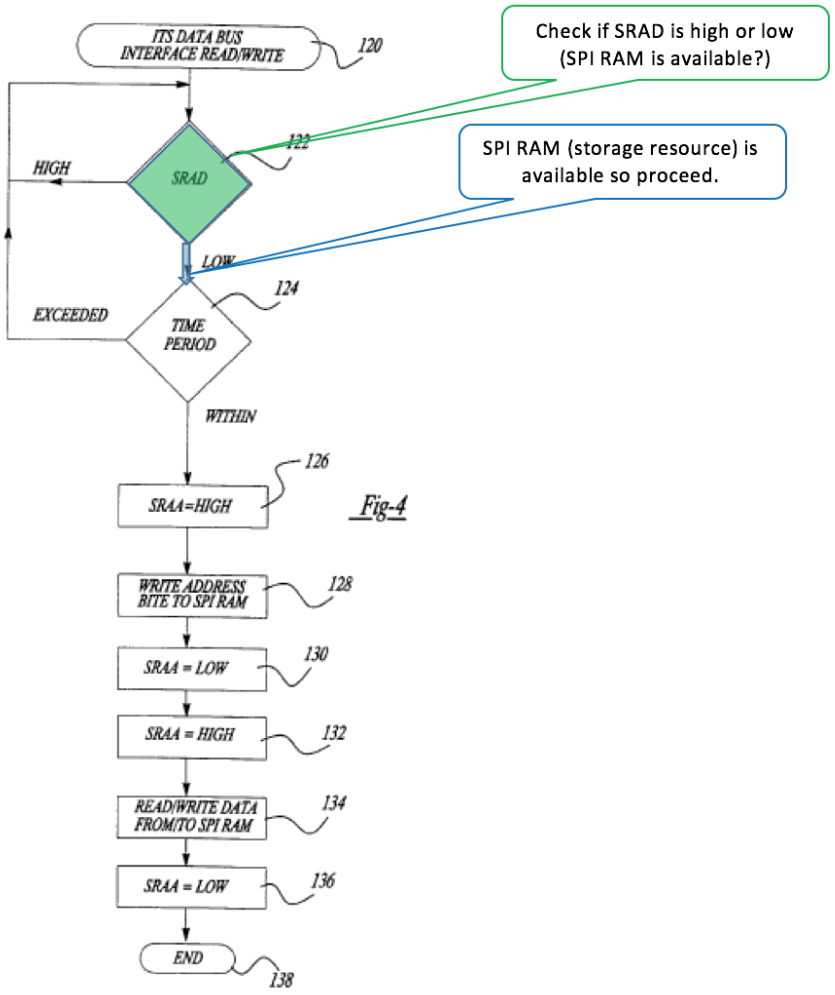


Fig-1

Miesterfeld, FIG. 1 (annotated)

48. *Miesterfeld* further discloses a process for reading and writing (storing) data received through the vehicle's devices. *Id.* 4:22-26, 5:38-43, 6:33-40, Fig. 4. As illustrated in annotated FIG. 4, the process includes, *inter alia,* determining whether SPI RAM is available and storing data if so. *Id.* The process is iterative—the system repeatedly attempts to determine SPI RAM availability until it either becomes available or too much time has elapsed. *Id.*, 6:40-45 (explaining the handshake arbitrating access to the SPI RAM (SRAA) "must" be set to "high" within 5 µs of determining that the SRAD signal line is low.).



Miesterfeld, FIG. 4 (annotated)

F. Wong

49. *Wong* teaches vehicle information system 20 including master control unit (MCU) 24 and one or more secondary control units (SCU) 26(1) and 26(2) connected to automobile components and systems 32, 34, 36. *Wong*, (54), 1:52-60, 2:32-373:25-4:2, Fig. 1. The MCU and SCUs include "processor 100" running a "real-time, multitasking operating system that is capable of supporting "plug-and-

play system configuration and providing high stability, security, and efficiency." *Id*., 1:52-60, 2:32-37, 5:64-6:29. *Wong*'s controller can execute instructions for controlling data flow management (*id.*, 6:40-42) and permits communication among automobile devices, including sensors. *Id.*, 7:51-58.

G. Stewart

50. *Stewart* teaches a framework for integrating real-time software control modules for real-time sensor-based systems. *Stewart*, 1, 6, 7. To "guarantee that tasks will get the data they require on time, every time," *Stewart* teaches implementing a "bounding wait time" (threshold) in a multiprocessor synchronization method. *Id.*, 11. *Stewart* also teaches implementing a "time-out mechanism" (threshold) for preventing data transfer when a "pre-specified time or number of retries" elapses and that "error handlers should be installed to detect tasks that suffer successive time-out errors." *Id.*

H. Wense

51. *Wense* teaches that cars utilize "[s]everal multiplex protocols," including CAN (*e.g.*, for engine and body control networks), FlexRay (*e.g.*, for safety, braking, and steering systems), and LIN (*e.g.*, for cost-critical distributed body electronics). *Wense*, 11.

I. Ma

52. *Ma* teaches apparatuses and methods for processing data packets in the data communications field. *Ma*, 1:7-10. *Ma* teaches that data packets include a data field and one or more header fields whereby the packet headers and their functions are "typically" arranged in an orderly fashion according to the open-systems interconnection (OSI) reference model (*id.*, 1:26-31) and explains that the OSI model partitions packet communications functions into layers, each layer having a header stripped or prepended during data processing. *Id.*, 5:48-63.

X. OPINIONS

53. My opinions below relate to the obviousness of claims 1-33 of the '400 patent based on the following grounds:

Ground	Claim(s) Challenged	35 USC §	References
1	1-33	103	*Lohrmann, Tofano*, *Ueno*, and *Staiger*
2	1-7 and 27-33	103	*Miesterfeld, Wong*, *Stewart*, and *Wense*
3	8-26	103	*Miesterfeld, Wong*, *Stewart*, *Wense,* and *Ma*

A. LOHRMANN GROUND

54. Ground 1 establishes that Lohrmann discloses or suggests each of the claimed features but arguably lacks express disclosure of (1) a memory, instructions, and processor, (2) accessing a storage resource and related steps, and (3) sharing sensor information in less than a second. *Tofano*, *Ueno*, and *Staiger* are relied upon to teach each of these respective features. Ground 1 also relies on *Tofano* to explain the hierarchal layers (*e.g.*, data link and network layers) of the data packets being transmitted and corresponding data processing steps (*e.g.*, adding and removing header bits).

A POSITA Would Have Understood That *Lohrmann*'s Gateway Either Includes Memory Storage, Instructions, and a Processor, or Would have Required the Same for Executing its Disclosed Process

55. It is my opinion that *Lohrmann*'s gateway would have utilized a memory and instructions to operate, which a POSITA would have readily understood, and thus *Lohrmann*'s disclosure at least suggests these implicit components.

56. To the extent *Lohrmann* does not expressly disclose memory, instructions, and a processor, *Tofano* does, and it is my opinion that a POSITA would have been motivated to add these conventional computing components to *Lohrmann*'s gateway. *Tofano* teaches a communication system for exchanging data between networks, the system including first and second network interfaces, a

shared non-switched system bus, and a processor. *Tofano*, 3:18-31. The processor "can be provided with a suitable software program to execute, thereby enabling the processor to accomplish any required functions for the communication system" and "each processor … may have the necessary memory, disk, non-volatile storage, I/O, networking and communications peripherals, and other support necessary for it to accomplish the required functions." *Id.*, 15:56-65.

57. *Tofano* and *Lohrmann* relate to the same technical field: communication networks. In my opinion, a POSITA would have had a reasonable expectation of success in modifying *Lohrmann*'s gateway to include a hardware processor for executing instructions stored in memory to perform the disclosed process. The modification would have required only ordinary skill. For example, *Lohrmann* explains that the interface between network segments is implemented in control units which also contain application functions referred to as "gateway," (*Lohrmann*, ¶ 3) and describes gateway functions including controlling system wide operations of the network including routing messages (*id.* ¶4), as well as management functions such as network interfacing and configuration, monitoring, detection, and diagnostics. *Id.* ¶*5.* A POSITA would have understood that an efficient, flexible, and configurable way of implementing these functionalities would have been through software executing on a processor, as taught by *Tofano*. This combination would have been predictable and without risk or undue

experimentation, and had a high chance of success. Accordingly, there would have been a high expectation of success utilizing this approach. A POSITA would have also understood that *Tofan*o, as illustrated in Fig. 5 and described in 4:13-51, teaches a processor having multiple network interfaces and is capable of information exchange with various networks and network management. *Tofano,* 2:53-68.

A POSITA Would Have Been Motivated to Incorporate a Storage Resource and Corresponding Processes for Ensuring Storage Availability into *Lohrmann*

58. *Lohrmann* at least suggests a storage resource because *Lohrmann* discloses that the "network management system stores information on the state of the network 100 or of the network segments 20, 30, 40, 50 of the network 100 and of the subscribers 21, 31, 33, 41, 43, 51." *Lohrmann*, ¶ 2. Storing such information necessarily requires a "storage resource." A POSITA would have readily understood this.

59. In my opinion, *Ueno* also renders this feature and the corresponding processes, *e.g.*, determining storage resource availability and utilizing the storage, obvious. *Ueno* teaches a shared storage device and a method of accessing that storage. *Ueno*, Abstract, 1:8-10 ("the present invention relates to a direct access storage device … shared by a plurality of central processing units"). *Ueno* teaches well-known memory management techniques relating to explicit resource management, including determining storage accessibility (*id.*, 11:27-41, Fig. 5),

threshold implementation (*id.*), and error notification. *Id.*, 10:19-23; 11:1-6.

60. *Ueno*, like *Lohrmann* and *Tofano*, relates to the same technical field: communication networks. It is my opinion that a POSITA would have reasonably expected that modifying the combined system of *Lohrmann* and *Tofano* to include a storage resource and corresponding processes would succeed, and that the modification would have required only ordinary skill. For example, *Lohrman*n discloses in ¶¶ 23-33, as part of the gateway's network system management functionality, that the gateway must store information about the state of the network, including operating modes, bus states, network segment states, and configuration states to ensure stable operation of the network. Further, *Lohrmann* explains that network segments can be selectively and synchronously turned off and on. *Id*, 11-14. A POSITA would have understood storage the storage and associated processes of Ueno would have improved upon Lohrmann by ensuring real time and reliable operation.

A POSITA Would Have Understood That *Lohrmann*'s Gateway Shares Sensor Information in Less than One Second or Would Have Been Motivated to Configure the Gateway To Do So

61. *Lohrmann* discloses that sensor information is exchanged using a control area network (CAN). *Lohrmann*, ¶¶ 20,21. It is my opinion that this information is capable being of shared in less than one second because CANs facilitate information transmission at speeds of less than one millisecond.

62. To the extent further clarification is required, *Staiger* also describes systems and methods for vehicle network communication and renders this feature obvious. *Staiger*, ¶¶ 2, 22, 43. *Staiger* explains that CAN, FireWire, and MOST busses are "real-time" buses, capable of "respond[ing] to stimuli within some small upper limit of response time, typically [in] milliseconds or microseconds," such that, upon receiving a message, an intercommunication preprocessor "processes the message and initiates immediate distribution" of an "output[] message." *Id.*, ¶¶ 7, 35, 51, claim 1, Abstract.

63. Both *Lohrmann* and *Staiger* relate to automotive network communication, and *Staiger* clarifies how fast *Lohrmann*'s CAN bus can share information. Accordingly, it is my opinion that a POSITA would have had a reasonable expectation of success in configuring *Lohrmann*'s gateway such that sensor information is capable of being shared in less than one second. The modification would have required only ordinary skill.

A POSITA Would Have Been Motivated to Combine *Lohrmann*, *Tofano*, *Ueno*, and *Staiger*

64. All of the *Lohrmann* Ground references relate to communication networks and are combinable individually and as a whole. *Lohrmann's* modified system incorporates a processor (taught by *Tofano*), a storage resource and corresponding processes (taught by *Ueno*), and the capability to send sensor

information in less than one second (taught by *Staiger*). None of these components alter the overall functionality of *Lohrmann* and each modification would have been obvious and required only routine skill to implement.

1. Ground 1: Claims 1-33 are obvious over *Lohrmann* in view of *Tofano*, *Ueno*, and *Staiger*

Claim 1[preamble]: "A system, comprising:"

65. *Lohrmann* discloses "a system for managing networks in a transportation unit." *Lohrmann*, Abstract.

1[a]: "an automotive electronic control unit including a memory storage comprising instructions, and"

66. *Lohrmann* discloses "control units" (called "subscribers") for controlling automotive sensors or actuators, and therefore discloses an automotive electronic control unit (ECU). *Lohrmann*, ¶ 21. *Lohrmann* also discloses that a gateway is a type of subscriber (and therefore also an automotive ECU) that exchanges data over a network. *Id.*, ¶¶ 3, 18. In my opinion, a POSITA would have understood *Lohrmann*'s disclosure of a "gateway" to at least suggest a memory and instructions because memory and instructions are necessary gateway components that facilitate gateway functionality, *e.g.*, network management, data exchange and communication between buses. *Lohrmann* also discloses the use of control unit applications, which would have also suggested to a POSITA that memory and instructions are present.

67. It is also my opinion that *Tofano* renders this limitation obvious. *Tofano* discloses an integrated communication system that "enable[s] data and information exchanges between various networks and various network formats" and "transparently interconnects different networks," which includes a processor for translating or converting incoming data from a first network format to another network format. *Tofano*, 2:56-62, 15:47-51. *Tofano*'s processor is operably connected to components of the system, and "can be provided with a suitable software program to execute, thereby enabling the processor to accomplish any required functions for the communication system*." Id*., 15:56-61. "[E]ach processor … may have the necessary memory, disk, non-volatile storage, I/O, networking and communications peripherals, and other support necessary for it to accomplish the required functions." *Id.*, 3:18-20, 29-32. Thus, *Tofano* also teaches a gateway, having memory storage comprising instructions.

68. In my opinion, it would have been obvious to a POSITA to incorporate a memory storage including instructions and the corresponding processor into *Lohrmann* to facilitate the gateway's required functions which "include, inter alia, the provision of services for controlling the system-wide operation of the network. For example, a gateway is responsible for "routing" messages from and to various network segments." *Lohrmann*, ¶ 4

1[b] and 1[c]: "at least one hardware processor in hardwired communication with the memory storage,

wherein the at least one hardware processor executes the instructions for:"

69. As explained for 1[a], *Tofano*'s communication system includes processor 228 and corresponding software. *Tofano*, 15:56-65. "[T]he processor 228 executes a suitable software program therein for translating between at least one network format, such as between at least one of the first network format and the second network format," and therefore executes instructions related to message handling. *Id.*, 13:23-3.

1[d]: "receiving sensor information associated with a message;"

70. *Lohrmann*'s gateway controls data exchange between "control unit[s] or control unit applications, such as sensors and actuators," by "passing on messages from one network segment to a further network segment." *Lohrmann*, ¶ 4,19, 21.

1[e] and 1[f]: "in response to receiving the sensor information, issuing, by the at least one hardware processor and to a storage resource included in the automotive electronic control unit, a storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information and,

in response to issuing the storage resource request, determining whether the storage resource is available to store the sensor information;"

71. *Lohrmann* and *Tofano* in combination with *Ueno* teaches this

limitation. *Ueno* "relates to a direct access storage device (hereinafter referred to as DASD) shared by a plurality of central processing units." *Ueno*, 1:8-10, 2:57-63. *Ueno's* central processing units (CPUs) correspond to *Tofano's* processor, and *Ueno's* DASD corresponds to the claimed storage resource because it stores data. *Ueno*, 1:8-9, 4:50-53, Fig. 1.

72. *Ueno*'s CPU reads and writes datasets (information) to and from the DASD using a program. *Id.*, 4:65-5:2. Before *Ueno*'s CPU writes data to the DASD (stores information in the storage resource), it searches the DASD for "control information" to determine whether it may access the DASD. *Id.*, 3:47-51, 4:57-64, 5:27-31. In my opinion, a POSITA would have understood that searching the DASD for control information prior to writing the data to the DASD is a "storage resource request to access the storage resource" because it determines whether the storage resource is available for writing data.

73. *Ueno* also discloses that "reserve flags, the reserve CPU numbers and the blockage flags of the two searched control information sets are checked" after the CPU searches for the control information. *Ueno*, 5:33-35. *Ueno*'s flags and reserve CPU numbers indicate whether the DASD is capable of receiving/storing the data to be written. *Id.*, 4:57-64, 5:33-43. In my opinion, a POSITA would have understood that "checking" for flags and a CPU number constitutes determining whether the storage resource (the DASD) is available to store the information

(data) in response to issuing the storage resource request (the search) because the presence of flags indicates that the DASD cannot receive data, and the absence of flags indicates that the DASD can receive data. *Id.* 5:33-43 (explaining that certain flag conditions must be satisfied before data may be written to the DASD).

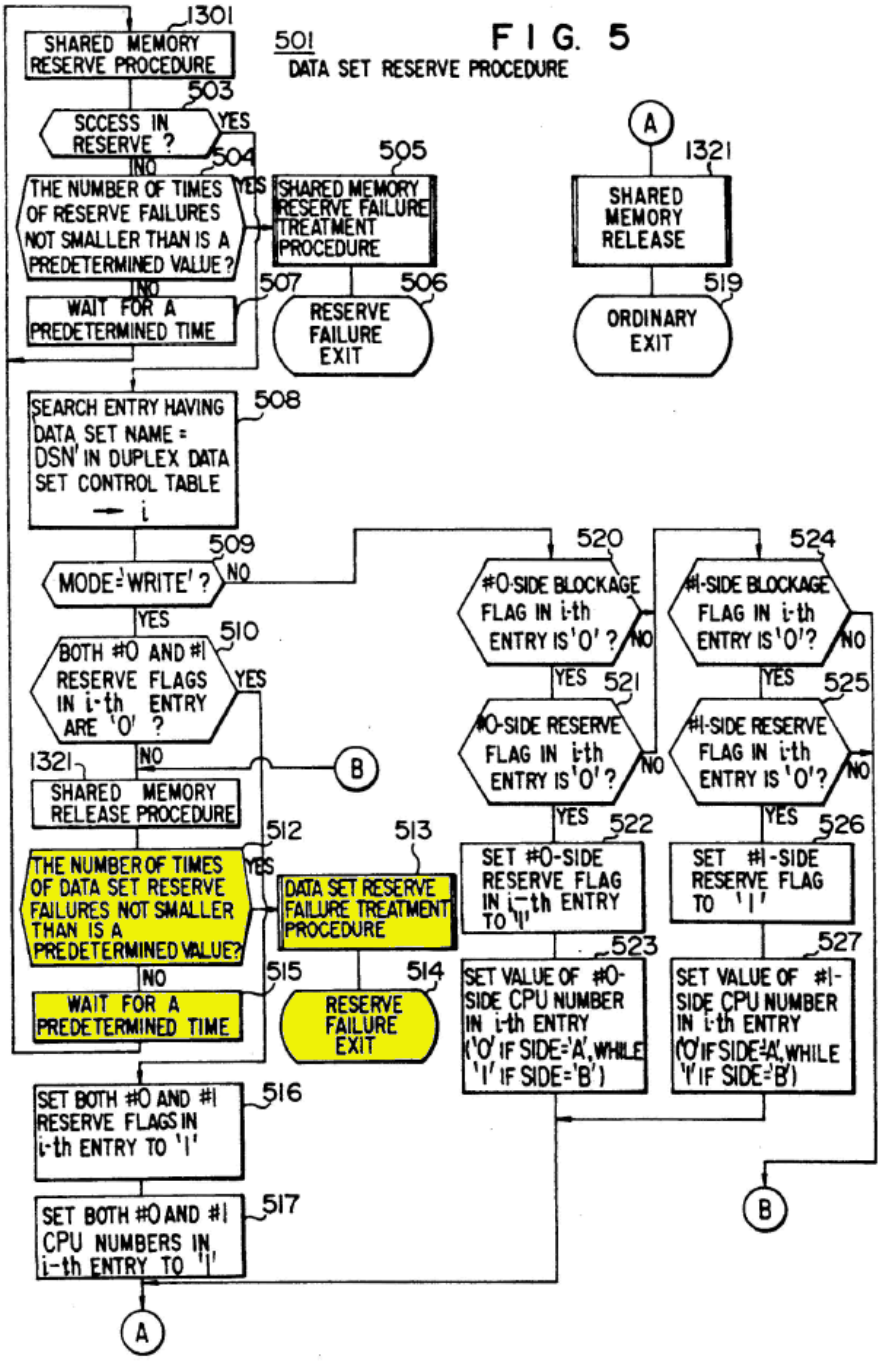
74. *Ueno*'s search and check method minimizes computer system overhead (*Ueno*, 2:61-64) and ensures accessibility to shared database storage systems. *Id.* 2:51-56, 6:56-61. In my opinion, a POSITA would have been motivated to implement *Ueno*'s search and check method for accessing a storage resource into the *Lohrmann-Tofano* system for these reasons.

75. As combined, the automotive ECU gateway processor (taught by *Lohrmann* and *Tofano*) determines whether the storage resource is available to store the sensor information in response to issuing the storage resource request (taught by *Ueno*). It is my opinion that this modification would have been within the purview of a POSITA because it would have required using routine components like processors and memories to assess storage resource is availability. The combination would have yielded the predictable results of minimizing system overhead and ensuring storage accessibility—results recognized expressly in *Ueno*.

1[g]: "determining whether a threshold tracked since the issuance of the storage resource request has been reached indicating that the storage resource has not been available in association with the

threshold tracked since the issuance of the storage resource request;"

76. As explained for 1[e] and 1[f], *Lohrmann* as modified by *Tofano* and *Ueno* teaches issuing a storage request and determining whether the storage resource is available using the search and check method of *Ueno*. *Ueno*'s searching and checking involves an iterative process whereby the processor checks for flags (storage resource accessibility) after a predetermined number of attempts or time (a threshold) elapses. *Ueno*, 11:27-41, Fig. 5.



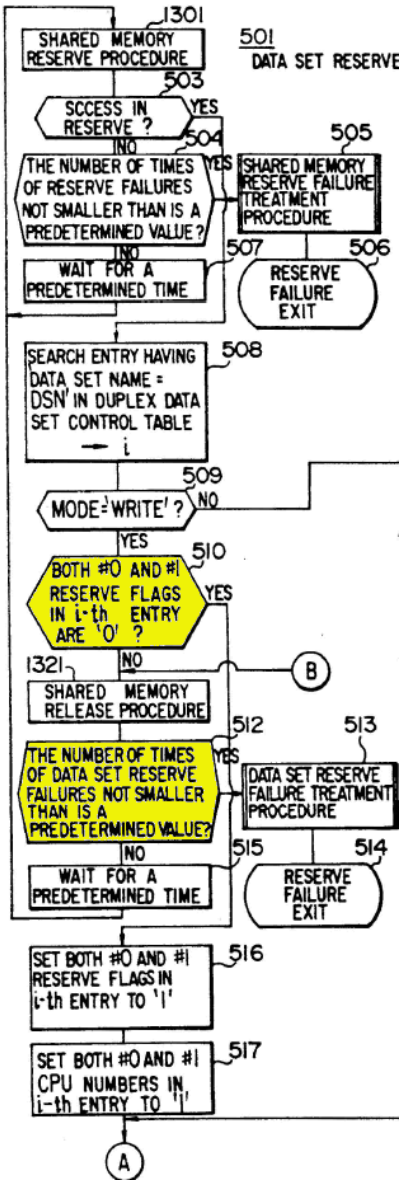
Ueno, FIG. 5 (annotated)

77. If the number of attempts exceeds the predetermined threshold, an "abnormality" is detected, and the DASD is determined to be unavailable. *Id.*,

11:37-42, FIG. 5. In my opinion, a POSITA would have understood that *Ueno* discloses a "threshold" because *Ueno* uses the quantity of access attempts or time elapsed to trigger an abnormality finding and determination of DASD availability.

> **1[h]: "when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has not been reached indicating that the storage resource has not been available in association with the threshold tracked since the issuance of the storage resource request, issuing, by the at least one hardware processor to the storage resource included in the automotive electronic control unit, another storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information;"**

78. As explained for 1[g], *Lohrmann* as modified by *Tofano* and *Ueno* teaches an iterative process whereby the processor checks for flags (storage resource accessibility) after a predetermined number of attempts or time (a threshold) elapses. *Ueno*, 11:27-41, FIG. 5. *Ueno*'s iterative process includes repeating the search and check cycle (and thus issuing another storage resource request) "if the number of times in a data set reserving failure is within a predetermined value." *Id.*, 11: 33-37; Fig. 5.



Ueno, FIG. 5 (annotated)

79. In my opinion, A POSITA would have understood that *Ueno* teaches repeating the check and search process (issuing another storage request) when the DASD is determined to be unavailable, and the predetermined value of access attempts or time (threshold) has not been exceeded. As combined with *Ueno*'s

check and search process, the processor in *Lohrmann*'s gateway (1) checks the reserve flags associated with a DASD to determine its availability to receive data, and (2) if the reserve flags are not both zero, and the number of attempts is within "a predetermined value," researching and rechecking until either the number of retries exceeds a predetermined value or the DASD is determined to be available. *Ueno*, 11:12–42.

1[i]: "when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request or the another storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has been reached, sending an error notification; and"

80. As explained for 1[g], *Lohrmann* as modified by *Tofano* and *Ueno* teaches determining whether the DASD (storage resource) is unavailable. *Ueno*, 11:37-42, FIG. 5. The resource is unavailable "[i]f at least one of the reserve flags 202-1 and 202-2 is '1' (Step 510)." *Id.*, 11:25-33. *Ueno* further discloses reporting "a failure" if the DASD is determined to be unavailable and the number of reattempts (as explained for 1[h]) exceeds the predetermined threshold. *Id.*, 10:19-23; 11:1-6 (reporting other failures). In my opinion, reporting "a failure" corresponds to the claimed "sending an error notification."

1[j]: "when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request or the another storage resource request, to be available, storing the sensor information utilizing the storage resource;"

81. As explained for 1[e] and 1[f], *Lohrmann* as modified by *Tofano* and *Ueno* teaches determining whether the DASD (storage resource) is available. *Ueno* further teaches that if both reserve flags are 0, "[t]he CPU executes writing the same contents into the data sets on the two DASDs." *Id.*, 5:42-43. In my opinion, a POSITA would have understood that *Ueno* discloses storing data to the storage resource and that the combination teaches storing sensor information (as disclosed by *Lohrmann*) to a DASD in response to performing (and repeating) the search and check process (issuing the/another storage resource request).

1[k]: "wherein the automotive electronic control unit is operable such that the sensor information is capable of being shared in less than one second, and"

82. *Lohrmann*'s information is exchanged using a control area network (CAN). *Lohrmann*, ¶ 20. It is my opinion that a POSITA would have understood that the information is capable of being shared in less than one second because CANs are known to facilitate transmission at speeds of less than one millisecond. Indeed, rapid, real-time transmission is essential to the data sharing in vehicular systems because it ensures that the vehicle components respond to sensor input in a

timely fashion. This is especially important where, for example, the input relates to vehicle safety mechanisms such as brake control.

83. To the extent Patent Owner disputes this, *Staiger* renders this limitation obvious. *Staiger* discloses an ECU connected to a plurality of real-time networks, including "several individual CAN [] busses or other multiple purpose networks." *Id.*, ¶ 3. *Staiger*'s ECU executes an application for controlling remote automobile systems while concurrently performing gateway functions between the different networks. *Id.*, ¶¶ 4-5. *Staiger* explains that the CAN, FireWire, and MOST buses are "real-time" buses, capable of "respond[ing] to stimuli within some small upper limit of response time, typically [in] milliseconds or microseconds," such that, upon receiving a message, an intercommunication preprocessor "processes the message and initiates immediate distribution" of an "output[] message," to, *e.g.*, a "destination unit." *Id.*, ¶¶ 7, 35, 51, claim 1, Abstract (emphasis added).

84. In my opinion, it would have also been obvious to a POSITA to configure the modified system of *Lohrmann* such that message information sent from a sensor origin on a CAN, LIN, or FlexRay Network reaches its destination in milliseconds or microseconds ("less than one second") to facilitate immediate receipt of an incoming message from a sensor origin and distribution of an output message to a destination, such as an actuator. *Staiger*, 7, 35, 51, claim 1, Abstract.

Such a modification would have ensured real-time responses crucial to vehicle safety and operation.

1[l]: "the automotive electronic control unit includes a plurality of interfaces including: a first interface; and a second interface for interfacing with a network, where the network is at least one of a Controller Area Network, a Flexray network, or a Local Interconnect Network."

85. *Lohrmann*'s network includes "a plurality of network segments 20, 30, 40, 50, which are physically connected via gateways 33, 43." *Lohrmann*, ¶ 19. *Lohrmann* discloses that "[t]he interface between the network segments is generally implemented in … a gateway." *Id.*, ¶ 3. Thus, in my opinion, *Lohrmann* discloses a plurality of interfaces (a first interface between a first set of network segments and a second interface between a second set of network segments) implemented in the gateway (automatic ECU). *Lohrmann* further discloses that various data bus systems may be used within each network segment, including CAN, FlexRay and LIN (*id.*, ¶ 20) and that the system is "suitable for operating network segments which are based on different bus systems, since the actual data bus system in the network segment is not significant for managing network segments." *Id.*, ¶ 10. Thus, *Lohrmann* discloses that the network is at least one of a Controller Area, Flexray, or Local Interconnect Network.

Independent Claim 8

86. As illustrated in the chart below, independent claim 8 largely mirrors independent claim 1, except that it is directed to an "apparatus" (Ex-1001, 13:48), and further recites a "first network" associated with a "first protocol" and corresponding "first interface," wherein "the first network is at least one of a Controller Area Network type, a Flexray network type, or a Local Interconnect Network type;" and a "second network" associated with a "second protocol" and corresponding "second interface," wherein "the second network is at least one of the Controller Area Network type, the Flexray network type, or the Local Interconnect Network type." *Id.*, 14:39-57.

87. These limitations are obvious for the reasons discussed in claim 1. For example, *Lohrmann* discloses a plurality of interfaces (a first interface between a first set of network segments and a second interface between a second set of network segments) implemented in the gateway (the automatic ECU). *Lohrmann* also discloses that data bus systems may be used within each network segment, including CAN, FlexRay and LIN (*Lohrmann*, ¶20) and that the system is "suitable for operating network segments which are based on different bus systems, since the actual data bus system in the network segment is not significant for managing network segments." *Id.*, ¶10. Each network or network segment is associated with a network protocol, for example, CAN uses CAN protocol. Thus, *Lohrmann*

discloses first and second networks having associated network protocols and corresponding to first and second interfaces, wherein the network(s) are at least one of a Controller Area, FlexRay, or Local Interconnect Network.

1[preamble]: "A system, comprising:"	8[preamble]: "An apparatus, comprising:"
1[a]: "an automotive electronic control unit including a memory storage comprising instructions, and"	8[a]: "an automotive electronic control unit including a memory storage comprising instructions, and"
1[b]: "at least one hardware processor in hardwired communication with the memory storage,"	8[b]: "at least one hardware processor in hardwired communication with the memory storage,"
1[c]: "wherein the at least one hardware processor executes the instructions for:"	8[c]: "wherein the at least one hardware processor executes the instructions for:"
1[d]: "receiving sensor information associated with a message;"	8[d]: "identifying sensor information associated with a message received **utilizing a first network protocol associated with a first network**;"
1[e]: "in response to receiving the sensor information, issuing, by the at least one hardware processor and to a storage resource included in the automotive electronic control unit, a storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information and,"	8[e]: "in response to identifying the sensor information, issuing, by the at least one hardware processor and to a storage resource included in the automotive electronic control unit, a storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information and,"
1[f]: "in response to issuing the storage resource request, determining whether the storage resource is available to store the sensor information;"	8[f]: "in response to issuing the storage resource request, determining whether the storage resource is available to store the sensor information;"
1[g]: "determining whether a threshold tracked since the issuance of the	8[g]: "determining whether a threshold tracked since the issuance of the

storage resource request has been reached indicating that the storage resource has not been available in association with the threshold tracked since the issuance of the storage resource request;"	storage resource request has been reached indicating that the storage resource has not been available in association with the threshold tracked since the issuance of the storage resource request;"
1[h]: "when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has not been reached indicating that the storage resource has not been available in association with the threshold tracked since the issuance of the storage resource request, issuing, by the at least one hardware processor to the storage resource included in the automotive electronic control unit, another storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information;"	8[h]: "in the event the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has not been reached indicating that the storage resource has not been available in association with the threshold tracked since the issuance of the storage resource request, issuing, by the at least one hardware processor to the storage resource included in the automotive electronic control unit, another storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information;"
1[i]: "when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request or the another storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has been reached, sending an error notification; and"	8[i]: "in the event the storage resource included in the automotive electronic control unit is determined, in response to issuing the another storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has been reached, sending an error notification; and"
1[j]: "when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request	8[j]: "in the event the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request

or the another storage resource request, to be available, storing the sensor information utilizing the storage resource;"	or the another storage resource request, to be available, storing the sensor information utilizing the storage resource;"
1[k]: "wherein the automotive electronic control unit is operable such that the sensor information is capable of being shared in less than one second, and"	8[k]: "wherein the apparatus is operable such that the sensor information is capable of being shared in less than one second **utilizing a second network protocol associated with a second network,** and the automotive electronic control unit remains in hardwired communication with the first network and the second network and includes:"
1[l]: "the automotive electronic control unit includes a plurality of interfaces including: a first interface; and a second interface for interfacing with a network, where the network is at least one of a Controller Area Network, a Flexray network, or a Local Interconnect Network."	8[l] "a first interface for interfacing with the first network, **the first interface including a first interface-related data link layer component for using first network-related data link layer header bits and a first interface-related network layer component for using first network-related network layer header bits,** where the first network is at least one of a Controller Area Network type, a Flexray network type, or a Local Interconnect Network type; and
	8[m]: "a second interface for interfacing with the second network**, the second interface including a second interface-related data link layer component for using second network-related data link layer header bits and a second interface-related network layer component for using second network-related network layer header bits,** where the second network is at least one of the Controller Area Network type, the

	Flexray network type, or the Local Interconnect Network type."

88. Claim 8 also recites additional features of the first and second interfaces (recited in 8[l] and 8[m] above) which, in my opinion, are obvious for the additional reasons discussed below.

8[l] "the first interface including a first interface-related data link layer component for using first network-related data link layer header bits and a first interface-related network layer component for using first network-related network layer header bits"

89. In my opinion, A POSITA would have found it obvious to provide, or understood that *Lohrmann*'s first interface (between a first set of network segments) includes, a datalink layer component for using first network-related data link layer header bits and a first interface-related network layer component for using first network-related network layer header bits because the International Standards Organization (ISO), which established the industry standard for automobile network communication at the time of the invention, required as much to facilitate communication using CAN, LIN, and FlexRay networks. Ex. 1046, 7 (establishing a CAN "serial communication protocol that supports distributed real-time control and multiplexing for use within road vehicles" and explaining that the "layered" CAN architecture established by the OSI reference model includes a data link layer and a physical layer (PL) for bit encoding/decoding).

90. To the extent this requires further clarification, *Tofano* teaches examples of network layer models (including OSI) which "support the transfer of data and information through one or more networks having a network format corresponding to a network layer model." *Tofano*, 11:6-10. Regarding the OSI model, *Tofano* states:

> Layer **2,** the Data Link layer **152,** also known as the Protocol layer, controls transmissions made through the physical layer, while detecting and correcting transmission errors to ensure error free, end-to-end transmissions 50 between networked devices. Network layer **153,** the third network layer, controls the operation of the data link and physical layers while providing higher level services such as routing and congestion control for transmissions.

Id., 11:47-54.

91. In my opinion, it would have been obvious to a POSITA to configure the first interface of *Lohrmann* to transmit sensor information using the OSI Reference model, as taught by *Tofano*, whereby a data link layer controls transmission through the physical layer, and the network layer controls the operation of the data link and physical layers, to support data transfer through *Lohrmann*'s network. *Tofano*, 11:6-10. It is also my opinion that A POSITA would have understood that such a configuration requires a data link layer component for

using data link layer header bits associated with the first network (*e.g.*, CAN, LIN or FlexRay) and a network layer component for using the CAN, LIN or FlexRay network layer header bits, because the interface needs to have the requisite "mechanisms" ("components") to enable the transfer.

> **8[m] "a second interface for interfacing with the second network, the second interface including a second interface-related data link layer component for using second network-related data link layer header bits and a second interface-related network layer component for using second network-related network layer header bits, where the second network is at least one of the Controller Area Network type, the Flexray network type, or the Local Interconnect Network type."**

92. It is my opinion that A POSITA would have also understood that *Lohrmann*'s second interface (between a second set of network segments) includes (or found it obvious to include) a second interface-related data link layer component for using second network-related data link layer header bits and a second interface-related network layer component for using second network-related network layer header bits for the same reasons set forth above regarding the first interface.

Independent Claim 27

93. As illustrated in the chart below, independent claim 27 largely mirrors claim 1, except that claim 27 is directed to a "non-transitory computer-readable medium" (Ex-1001, 21:33-38) and further recites a "first network" associated with

a "first protocol" a "second network," and corresponding first and second interfaces. *Id.*, 22:16-29. These limitations are also rendered obvious by *Lohrmann*, *Tofano*, *Ueno*, and *Staiger* for the reasons explained for claim 1.

94. Claim 27 also specifies that the "threshold" is "time-related" and that the second network "is another one of the Controller Area Network, the Flexray network, or the Local Interconnect Network." These limitations are also rendered obvious by *Lohrmann*, *Tofano*, *Ueno*, and *Staiger* for the reasons explained for claim 1. For example, as discussed in 1[g], *Ueno* discloses a "threshold" because *Ueno* uses the quantity of access attempts or time elapsed to trigger an abnormality finding and determination of DASD availability. Regarding the networks, as discussed in 1[l], *Lohrmann* discloses that CAN, FlexRay and LIN may be used within each network segment and that the system "is preferably suitable for operating network segments which are based on different bus systems, since the actual data bus system in the network segment is not significant for managing network segments." *Lohrmann.*, ¶¶ 10, 20. Thus, *Lohrmann* discloses that the first network is one of a Controller area, Flexray, or Local Interconnect Network and the second network is "based on different bus systems," *i.e.*, another one of the Controller Area Network, the Flexray network, or the Local Interconnect Network.

95. Lastly, claim 27 recites "ceasing repeating issuance of another storage resource request" instead of "sending an error notification." But because the

combination, as discussed in 1[i] teaches sending the error notification instead of another storage resource request, the combination also renders obvious "ceasing" repeating the storage request.

1[preamble]: "A system, comprising:"	27[preamble]: "A non-transitory computer-readable medium of an automotive electronic control unit for storing a computer program product including code that, when executed by at least one hardware processor included in the automotive electronic control unit in communication with the non-transitory computer-readable medium, is for:"
1[a]: "an automotive electronic control unit including a memory storage comprising instructions, and"	
1[b]: "at least one hardware processor in hardwired communication with the memory storage,"	
1[c]: "wherein the at least one hardware processor executes the instructions for:"	
1[d]: "receiving sensor information associated with a message;"	27[d]: "receiving sensor information associated with a message received **utilizing a first network protocol associated with a first network**;"
1[e]: "in response to receiving the sensor information, issuing, by the at least one hardware processor and to a storage resource included in the automotive electronic control unit, a storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information and,"	27[e]: "in response to receiving the sensor information, issuing, by the at least one hardware processor and to a storage resource included in the automotive electronic control unit, a storage resource request to access the storage resource included in the automotive electronic control unit,"
1[f]: "in response to issuing the storage resource request, determining whether the storage resource is available to store the sensor information;"	27[f]: "for determining whether the storage resource included in the automotive electronic control unit is available to store the sensor information;
1[g]: "determining whether a threshold tracked since the issuance of the storage resource request has been reached indicating that the storage resource has not been available in	27[g]: "determining whether a **time-related** threshold tracked after the issuance of the storage resource request has been reached in association with

association with the threshold tracked since the issuance of the storage resource request;"	the determination whether the storage resource is available;"
1[h]: "when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has not been reached indicating that the storage resource has not been available in association with the threshold tracked since the issuance of the storage resource request, issuing, by the at least one hardware processor to the storage resource included in the automotive electronic control unit, another storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information;"	27[h]: "when the storage resource included in the automotive electronic control unit is determined to not be available and the threshold associated with the determination whether the storage resource is available has not been reached, issuing, by the at least one hardware processor to the storage resource included in the automotive electronic control unit, another storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information;"
1[i]: "when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request or the another storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has been reached, sending an error notification; and"	27[i]: "when the storage resource included in the automotive electronic control unit is determined to not be available and the threshold associated with determination whether the storage resource is available has been reached, **ceasing repeating issuance of another storage resource request**; and"
1[j]: "when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request or the another storage resource request, to be available, storing the sensor	27[j]: "when the storage resource included in the automotive electronic control unit is determined to be available, storing the sensor information utilizing the storage resource;"

information utilizing the storage resource;"	
1[k]: "wherein the automotive electronic control unit is operable such that the sensor information is capable of being shared in less than one second, and"	27[k]: "wherein the computer program product is operable such that the sensor information is capable of being shared in less than one second utilizing the automotive electronic control unit that remains in hardwired communication with the first network and a second network,"
1[l]: "the automotive electronic control unit includes a plurality of interfaces including: a first interface; and a second interface for interfacing with a network, where the network is at least one of a Controller Area Network, a Flexray network, or a Local Interconnect Network."	27[l] "and that includes a plurality of interfaces including: a first interface for interfacing with the first network where the first network is one of a Controller Area Network, a Flexray network, or a Local Interconnect Network;"
	27[m]: "and a second interface for interfacing with the second network, where the second network **is another one of the Controller Area Network**, the Flexray network, or the Local Interconnect Network."

Claims 2-7, 10, 11, and 28-33: sharing "in less than one [millisecond/second]."

96. Dependent claims 2-7, 10, 11, and 28-33 each require some sharing event to occur "in less than one second," "in less than one millisecond," or "with sufficient speed for use in connection with an automotive device." Claim 33 requires the computer program product to be configured for sharing "in less than the one millisecond second [*sic*]."

97. *Staiger* teaches that CAN busses are "real-time" busses, capable of

"respond[ing] to stimuli within some small upper limit of response time, typically [in] milliseconds or microseconds," such that, upon receiving a message, an intercommunication preprocessor "processes the message and initiates immediate distribution" of an "output[] message," to *e.g.*, a "destination unit." *Id.*, ¶¶ 7, 35, 51, claim 1. Thus, it is my opinion that *Lohrmann*, in combination with *Tofano*, *Ueno*, and *Staiger* renders claims 2-6, 10, 11, and 28-33 obvious.

98. Claim 7 requires the system to be configured for sharing "with sufficient speed for use in connection with an automotive device." Ex-1001, 13:44-47. *Lohrmann*, in combination with *Tofano*, *Ueno*, and *Staiger* render this limitation obvious because, as explained above in element 1[k], data is written and read (shared), in milliseconds or microseconds. *Staiger*, ¶¶ 7, 35, 51, claim 1. In my opinion A POSITA would have understood that this speed is "sufficient" "for use in connection with an automotive device," as recited in claim 7 and as evidenced by the specification of the '400 patent, which explains that "[i]n the context of the present description, real-time may include any response time that may be measured in milli- or microseconds, and/or is less than 1 second.." Ex-1001, 3:45-49.

Claim 9: "The apparatus as recited in claim 8, wherein the apparatus is operable such that network layer translation is capable of being avoided."

99. *Tofano* further teaches that "[s]ometimes, differences in network layer

models may not be important or significant. For example, a preset number of network layers from different networks may be encapsulated as payload and transmitted between different networks without requiring any comparisons or translations." *Tofano*, 14:47-52. Thus, *Lohrmann* as modified by *Tofano* further teaches that "network layer translation is capable of being avoided.

> **Claim 12: "The apparatus as recited in claim 11, wherein the apparatus is operable such that the sensor information is shared by the second interface-related network layer component using the second network-related network layer header bits by adding the second network-related network layer header bits to a data unit including the sensor information, and then the second interface-related data link layer component using the second network-related data link layer header bits by adding the second network-related data link layer header bits to the data unit, before communicating the data unit on a physical link of the second network."**

100. *Tofano* further teaches an encoding process for transmitting (sharing) data between networks using the OSI model. The process "requires adding a suitable layer **2** and layer **1** … representing the data link layer and physical media layer respectively, to the payload data **302** as represented by layers L**3** through L**7**." *Tofano*, 28: 8-13. The process "can add one or more layers from a given network format to the payload data to prepare it for transmission to the outgoing network" so that ultimately, the payload data is embodied in a network layer model stack which can be transmitted through a network interface to an outgoing network in a compatible network format. *Tofano*, 28:14-21.

That is, *Tofano* teaches adding the second network-related network layer header bits ("one or more layers from a given network format") to a data unit and adding the second network-related data link layer header bits ("suitable layer 2") to the data unit before communicating the data on a physical link of the network. It is well known in the networking art that network packets comprise headers, which are comprised of header bits, and that the headers are added to payload bits, i.e., the actual information of interest, prior to transmission. This is because the packet header includes important information relating to the data's origin and intended destination, and therefore facilitates transmission between networks. *See also* Ex 1054, 2:43-62 (explaining "a transport header, network header and data link header ... [are] attached to the data at each of those layers, with each step typically including data moving and copying, before sending the data as bit packets, over the network, to the second host").

Claim 13: "The apparatus as recited in claim 12, wherein the apparatus is operable such that the first interface-related data link layer component uses the first network-related data link layer header bits by removing the first network-related data link layer header bits from another data unit, and the first interface-related network layer component uses the first network-related network layer header bits by removing the first network-related network layer header bits from the another data unit so that the

sensor information is removed from the another data unit, before the sharing."

101. *Tofano* further teaches that "data received in a network format may be decoded or extracted from its incoming physical layer and data link layer, so that decoded data can be represented by the contents of network layers 3 through 7 inclusive." *Tofano*, 23:36-49. In Figure 7a "layers 3 through 7 are removed by decoding, and the decoded data 302 is represented as extracted from physical layer L1 and data link layer L2. L1 and L2 are collectively denoted as 303, and are removed by the network interface, processor, or both." *Id.*, 24:51-58 (emphasis added).

102. Thus, *Tofano* teaches removing the first network-related data link layer header bits (Layer 2) from another data unit, and removing the first network-related network layer header bits (layer 3) from the "another" data unit so that the information is removed from the another data unit.

103. As explained for claim 12, it is my opinion that a POSITA would have understood that sending payload data over a network involves adding header bits to form a message, sending the message, and removing the header bits to extract the payload data. *See also* Ex 1054, 2:63-3:7 (explaining that "headers are removed and data processed in order from the lowest (Physical) layer to the highest (Application) layer" when data packets are received).

Claims 14 and 15: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the storage resource request and the another storage resource request are [identical/the same]."

104. As explained for 1[h], *Ueno* teaches repeating the write request (search and check) if a reserve flag is "1" and a retry value has not been exceeded. *Ueno*, 11:12-42. This is the exact procedure described in the '400 patent's specification, which only requires repeating the storage resource request. Ex-1001, 8:36-37 ("If the resource is not available, it may try it again after a waiting period (1011) until the resource is available."), Thus, it is my opinion that a POSITA would have understood that *Ueno* teaches that "the another storage resource request" is identical to or the same as "the storage resource request" because this is consistent with the '400 patent's disclosure.

Claims 16 and 17: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the sensor information excludes all [at least a portion of any] header bits of the message."

105. As explained for claim 13, layers are decoded and header bits removed prior to transmission. Because the payload (the actual information being transmitted), in the instant combination is the sensor information, it is my opinion that a POSITA would have understood that the portion of a message that is "sensor information" would not include, i.e., excludes all header bits. If "all header bits of the message" are excluded, then "a least a portion of any header bits" are

necessarily excluded. Thus, in my opinion, claim 17 is obvious for the same reasons as claim 16.

Claim 18: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the storage resource includes a bulletin board."

106. As explained in 1[e], *Lohrmann* as modified by *Tofano* and *Ueno* teaches a DASD. *Ueno*, 1:8-9, 5:21-22, 41-42. The DASD is a database from which electronic data may be read and written. *Id.* In my opinion, a POSITA would have understood that the DASD is a "bulletin" within the meaning of the '400 patent, which states: "the bulletin board may refer to any database that enables users to send and/or read electronic messages, files, and/or other data that are of general interest and/or addressed to no particular person/process." Ex-1001, 5:20-24.

Claims 19-21: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the error notification is sent, when the storage resource included in the automotive electronic control unit is determined, in response to issuing the [another] storage resource request [and the another storage resource request], to not be available and the threshold tracked since the issuance of the storage resource request has been reached."

107. Claims 19-21 are similar except that claim 19 recites "the storage resource request," claim 20 recites "the another storage resource request," and claim 21 recites both "the storage resource request and the another storage resource request."

108. As discussed above with respect to claim element 1[i], *Ueno* teaches reporting (i.e., sending) "a failure," *e.g.*, to an operator, if the DASD is determined to be unavailable and the number of reattempts (as discussed above in claim element 1[h]) exceeds the predetermined threshold. *Ueno,* 10: 19-24, 11:1-6 (reporting other failures to an operator). Thus, it is my opinion that the modified system teaches sending an error notification when the storage resource is determined to be unavailable in "response to issuing the storage request" and reaching the threshold, as recited in claim 19.

109. *Ueno's* process is iterative such that the DASD may be determined to be unavailable after issuing another request and reaching the threshold. This occurs, for example, when the number of attempts (which includes "the request" and the "another request") exceeds the predetermined maximum (*Ueno*, 11:27-41, Fig. 5) and causes a failure to be reported. Thus, it is my opinion that the modified system teaches sending an error notification when the storage resource is determined to be unavailable in "response to issuing the another storage request" and reaching the threshold, as recited in claim 20. Claim 21 is obvious for the same reason.

Claims 22 and 26: "The apparatus as recited in claim 8, wherein at least one of: the memory storage includes the storage resource; the memory storage does not include the storage resource…."

110. Claims 22 and 26 require "at least one of" numerous features listed in the alternative describing the apparatus of claim 8. Ex. 1001, 15:62-16:62, 17:12-21:32. Because "at least one" of these features, *e.g.*, "the memory storage includes the storage resource" is taught by the combination of *Lohrmann*, *Tofano*, *Ueno* and *Staiger*, it is my opinion that claims 22 and 26 are obvious for same reasons as claim 8.

Claim 23: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the information associated with the message is identified in another storage resource that stores the information after the message is received."

111. As discussed above in claim elements 1[e], 1[f] and 1[j], *Ueno* teaches that the DASD (storage resource) is one of a "pair" of DASDs. *Ueno*, 4:49-53. The second DASD constitutes "another storge resource" that "stores the information" for the same reasons the first DASD constitutes "a storage resource" that stores the information. The second DASD, like the first DASD, also reads (identifies) the information. *Ueno*, 5:5-22. Accordingly, it is my opinion that the modified system of *Lohrmann* teaches "another storage resource" that identifies and stores the sensor information. *Id.*

Claim 24: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the information associated with the message is identified in another storage resource that stores the information after the message is received and before the information is stored utilizing the storage resource, the another storage resource capable of being used for information storage, regardless as to a particular network with which the information is shared."

112. As discussed above in regard to claim 23, *Ueno* teaches that the second DASD is operable to read (identify) the data after the message is received (as discussed in claim element 1[d]). The data is read then written to (stored in) the first DASD. *Ueno*, 5:5-43. *Ueno* does not expressly teach that the DASD is capable of storing information "regardless" of the network used to share the information.

113. *Tofano* further teaches that its "communication system allows data or information in any form to be processed and conveyed transparently through the communication system to support 'end to end' exchanges of data and information between networks. As such, data and information in any form, and in various diverse network formats, can be processed and exchanged between networks in a common, efficient, and integrated manner by the communication systems of the present invention." *Tofano*, 10:13-21 (emphasis added).

114. In my opinion, a POSITA reading Tofano would have understood that the disclosed benefits apply equally to storage applications. That is, configuring a

storage resource to enable data and information to be stored "in any form, and in various diverse network formats" would have also facilitated common and efficient data exchange across networks. Thus, it is my opinion that it would have been obvious to a POSITA to configure the storage resource of the proposed combination to be "capable" of storing information regardless network format, to facilitate information processing and exchange in a "common, efficient, and integrated manner." *Tofano,* 10:13-21.

Claim 25: "The apparatus as recited in claim 24, wherein the apparatus is operable such that the information is stored utilizing the another storage resource in response to a corresponding request that is separate from the storage resource request."

115. As explained for 1[k], the combination teaches storing the information in each DASD. *Ueno*, 5:42-43. *Ueno* teaches that there is "one control information set for each data set for each DASD of the pair of DASDs forming the shared duplex DASD pair," (*id.*, 1:54-57); thus, *Ueno* teaches that the request to store information in the first DASD (storage resource) is "separate" from a request to store information in the second DASD (another storage resource) because *each* DASD is searched and checked prior to saving the information. *Id.*, 5:28-43 ("The reserve flags, the reserve CPU numbers and the blockage flags of the two searched control information sets are checked, and when both the control information sets

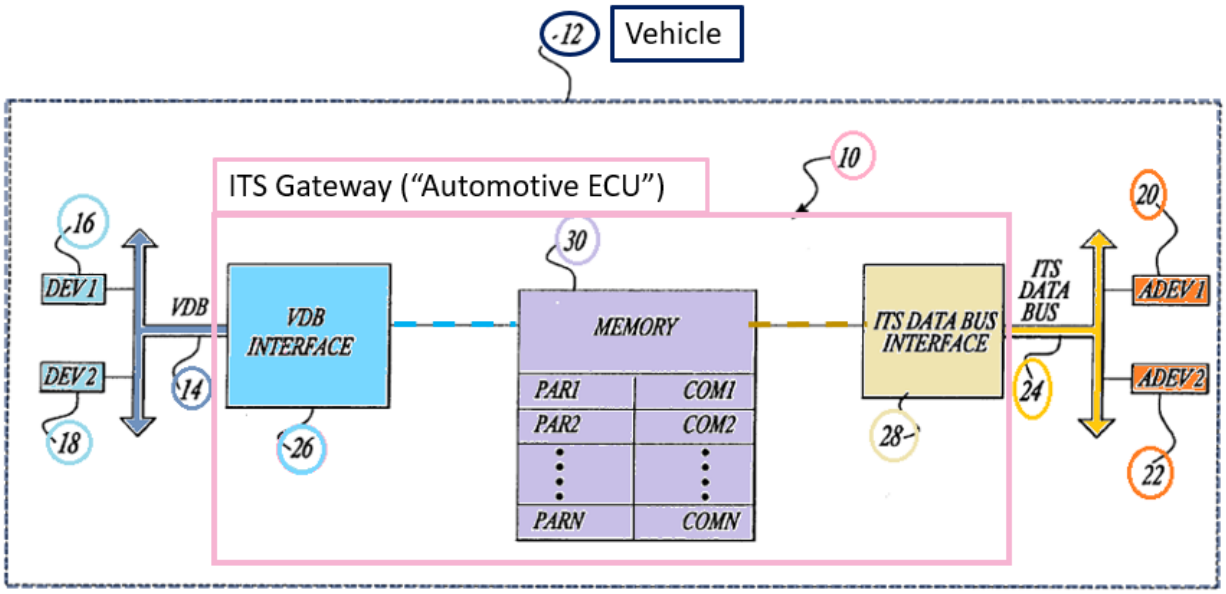
satisfy the condition 'reserve flag=0 and blockage flag=0' …. The CPU executes writing the same contents into the data sets on the two DASDs") (emphasis added).

B. Miesterfeld Grounds

116. Ground 2 establishes that *Miesterfeld* discloses or suggests each of the claimed features but arguably lacks express disclosure of (1) a hardware processor, (2) implementing a threshold and corresponding error notification, and (3) CAN, FlexRay, and LIN networks. *Wong*, *Stewart*, and *Wense* are relied upon to teach each of these respective features. Ground 3 adds *Ma* to explain the hierarchal layers (*e.g.*, data link and network layers) of the data packets being transmitted and corresponding data processing steps (*e.g.*, adding and removing header bits) required in independent claim 8 and certain dependent claims.

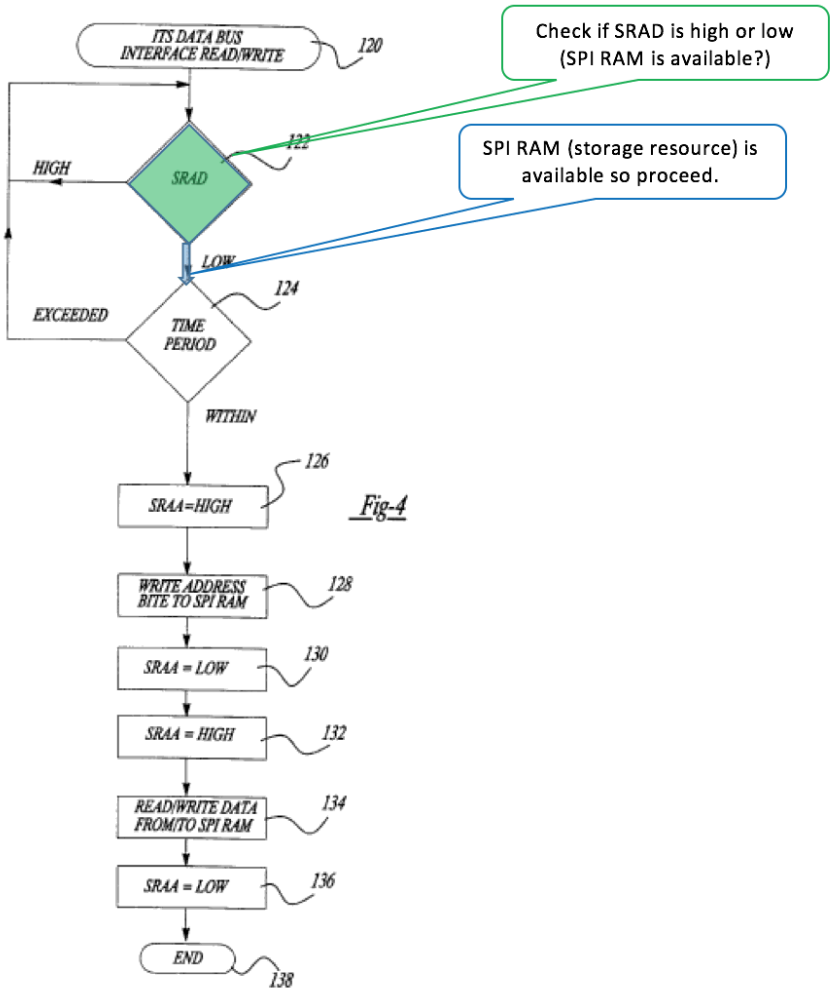
117. *Miesterfeld* discloses a data exchange system including a controller for "process[ing] vehicle data to control at least one vehicle related function." *Miesterfeld*, 2:23-27. The controller may be implemented on a vehicle 12 having a vehicle data bus (VDB) 14, an intelligent transportation system (ITS) data bus 28, and corresponding devices, 16, 18, 20, and 22, which "write data to or read data from" their respective data buses. *Id.*, 3:1-16. In operation, the controller ("gateway 10") facilitates data exchange between the VDB and ITS data bus via shared memory 30. *Id.*, 2:36-39, 3:18-20. To "effect such an exchange," the system includes VDB and ITS data bus interfaces which "read[] and write data from" both

the data buses and shared memory 30. *Id.*, 20-25. Annotated FIG. 1. illustrates *Miesterfeld*'s data exchange system on vehicle 12.



Miesterfeld, FIG. 1 (annotated)

118. *Miesterfeld* further discloses a process for reading and writing (storing) data received through the vehicle's devices. *Id.* 4:22-26, 5:38-43, 6:33-40, Fig. 4. As illustrated in annotated FIG. 4, the process includes, *inter alia,* determining whether SPI RAM is available and storing data if so. *Id.* The process is iterative—the system repeatedly attempts to determine SPI RAM availability until it either becomes available or too much time has elapsed. *Id.*, 6:40-45 (explaining the handshake arbitrating access to the SPI RAM (SRAA) "must" be set to "high" within 5 µs of determining that the SRAD signal line is low.).



Miesterfeld, FIG. 4 (annotated)

A POSITA Would Have Understood that *Miesterfeld*'s Controller Either Included or Would have Required a Processor for Executing its Disclosed Process

119. In my opinion, a POSITA would have understood that a processor and instructions are implicit to *Miesterfeld*'s gateway's functionality, *e.g.*, enabling data exchange between vehicle systems and third-party systems, and controlling information sharing between electronic control devices on the VDB and the ITS

data bus for the purpose of monitoring and controlling vehicle functions. *Miesterfeld*, 1:13–40, 2:66–3:49.

120. To the extent *Miesterfeld* does not expressly disclose a processor, *Wong* does, and it would have been obvious to add a processor to *Miesterfeld*'s controller. *Wong* teaches vehicle information system 20 including master control unit (MCU) 24 and one or more secondary control units (SCU) 26(1) and 26(2) connected to automobile components and systems 32, 34, 36. *Wong*, (54), 1:52-60, 2:32-373:25-4:2, Fig. 1. The MCU and SCUs include "processor 100" running a "real-time, multitasking operating system that is capable of supporting "plug-and-play system configuration and providing high stability, security, and efficiency." *Id*., 1:52-60, 2:32-37, 5:64-6:29. Like *Miesterfeld*'s controller, *Wong*'s controller can execute instructions for controlling data flow management (*Id.*, 6:40-42) and permits communication among automobile devices, including sensors. *Id.*, 7:51-58. Thus, it is my opinion that a POSITA would have had a reasonable expectation of success in modifying *Miesterfeld*'s controller (gateway) to include a hardware processor for executing instructions to perform the disclosed process, and that the modification would have required only ordinary skill.

A POSITA Would Have Understood *Miesterfeld*'s Countdown to 5 µs Is a "Threshold" and Would Have Found It Obvious to Provide an Error Notification if the Threshold Is Exceeded

121. *Miesterfeld* discloses tracking whether SRAA is "high" within 5µs of determining that the SRAD signal line is low (*Miesterfeld*, 6:40-45); and thus discloses a "threshold."

122. To the extent *Miesterfeld*'s countdown is not an express disclosure of a threshold, *Stewart* renders this feature obvious. *Stewart* teaches a framework for integrating real-time software control modules for real-time sensor-based systems. *Stewart*, 1, 6, 7. To "guarantee that tasks will get the data they require on time, every time," *Stewart* teaches implementing a "bounding wait time" (threshold) in a multiprocessor synchronization method. *Id.*, 11. *Stewart* also teaches implementing a "time-out mechanism" (threshold) for preventing data transfer when a "pre-specified time or number of retries" elapses and that "error handlers should be installed to detect tasks that suffer successive time-out errors." *Id.*

123. In my opinion, a POSITA would have been motivated to add the thresholds and error notification of *Stewart* to "guarantee that tasks will get the data they require on time, every time." *Stewart*, 11. It is also my opinion that a POSITA would have understood that implementing the thresholds and error notification of *Stewart* within *Miesterfeld* would have improved *Miesterfeld*'s

system by identifying errors and preventing the system from being locked into a futile cycle of storage access attempts.

124. Both *Miesterfeld* and *Stewart* relate to real-time distributed computer control systems and use similar techniques to solve the same problem (a shared memory architecture for facilitating data exchange between control modules in a real-time distributed system). *Stewart*, 1, 6, 7; *Miesterfeld*, 6:60-63, FIG. 4. In my opinion, a POSITA would have a reasonable expectation of success in modifying *Miesterfeld*'s instructions to include the step of determining whether a threshold is reached (and other threshold-based steps) and providing an error notification. Such a modification would have required only ordinary skill.

A POSITA Would Have Found It Obvious for *Miesterfeld*'s Data Buses to Comprise at Least One of a Controller Area, FlexRay, or Local Interconnect Network

125. *Miesterfeld* discloses that the ITS data bus 24 (first network) may be "any of a number of ITS data buses" (*Miesterfeld*, 4:5-10, 9:55-57) and that the VDB 14 (second network) may be "configured to implement the J1850 configuration as prescribed by the Society of Automotive Engineers (SAE) or any other industry standard as may be required." *Id.*, 4:7-10. Thus, it is my opinion that *Miesterfeld* suggests using CAN, LIN, or Flex Ray Networks because a POSITA would have understood these to be the industry standards *Miesterfeld* expressly contemplates.

126. To the extent *Miesterfeld* does not expressly disclose that its ITS data bus 24 is one of CAN, LIN, or Flex Ray Networks, *Wense*[2] expressly discloses that cars utilize "[s]everal multiplex protocols," including CAN (for engine and body control networks), FlexRay (for safety, braking, and steering systems), and LIN (for cost-critical distributed body electronics). *Wense*, 11. *Wense* simply clarifies the types of industry-standard networks that would have been implemented in *Miesterfeld*'s vehicle system; thus, it is my opinion that a POSITA would have had a reasonable expectation of success in configuring *Miesterfeld*'s networks to be one of CAN, LIN or FlexRay, and would have required only ordinary skill.

A POSITA Would Have Been Motivated to Combine *Miesterfeld*, *Wong*, *Stewart*, and *Wense*

127. Each of the references of the *Miesterfeld* Grounds relate to communication networks and are combinable individually and as a whole. A POSITA would have been motivated to modify *Miesterfeld* to incorporate a processor (taught by *Wong*), a threshold and error notification (taught by *Stewart*)

[2] *Wense* is a book published in 2001 and is prior art under pre-AIA 35 U.S.C. § 102(b). Patent Owner did not dispute that *Wense* is prior art to other members of the '400 patent family. *See generally* Ex-1064; Ex-1066; Ex-1067, 10-11.

and at least one of a CAN, LIN, or Flexray network (taught by *Wense*) because each of the secondary references improves *Miesterfeld*'s system by adding conventional, necessary components (a processor), providing routine timing mechanisms to identify and prevent errors (a threshold and error notification), and facilitating compliance with automotive industry standards (CAN, FlexRay, and LIN Networks). Each of the components are routine and none of them alters the overall functionality of *Miesterfeld.* Thus, in my opinion, each modification would have been obvious to a POSITA and required only routine skill to implement.

1. Ground 2: Claims 1-7 and 27-33 are obvious over *Miesterfeld* in view of *Wong*, *Stewart*, and *Wense*

Claim 1[preamble]: "A system, comprising:"

128. To the extent the preamble is limiting, *Miesterfeld* discloses a system. *Miesterfeld*, 2:23-24 ("[t]his invention is directed to a data sharing system in a vehicle."), 1:6-10.

1[a]: "an automotive electronic control unit including a memory storage comprising instructions, and"

129. *Miesterfeld*'s system includes a "vehicle system controller" ("gateway") for "process[ing] vehicle data to control at least one vehicle related function." *Miesterfeld*, 2:24-28. The gateway "has at least intermittent and direct access to and exchanges data on a vehicle data bus" and as illustrated in annotated FIG. 1 below, includes a memory through which a vehicle data bus (VDB) and

intelligent transportation system (ITS) data bus exchange data and commands. *Id.*, 1:5-11, 2:24-49, claim 1. The gateway facilitates communication between computerized devices (automotive ECUs) through a combination of hardware and software (instructions) read from or written to the memory. *Id.*, 1:13-3:19 (explaining that "a further object of the present invention to provide a data exchange gateway to enable a third party device to implement selected commands on a vehicle system" and that the common memory between the VDB and ITS "may be used to store specific commands which a third party device may request of a specific vehicle controller"). Accordingly, it is my opinion that the gateway corresponds to the claimed "automotive electronic control unit."

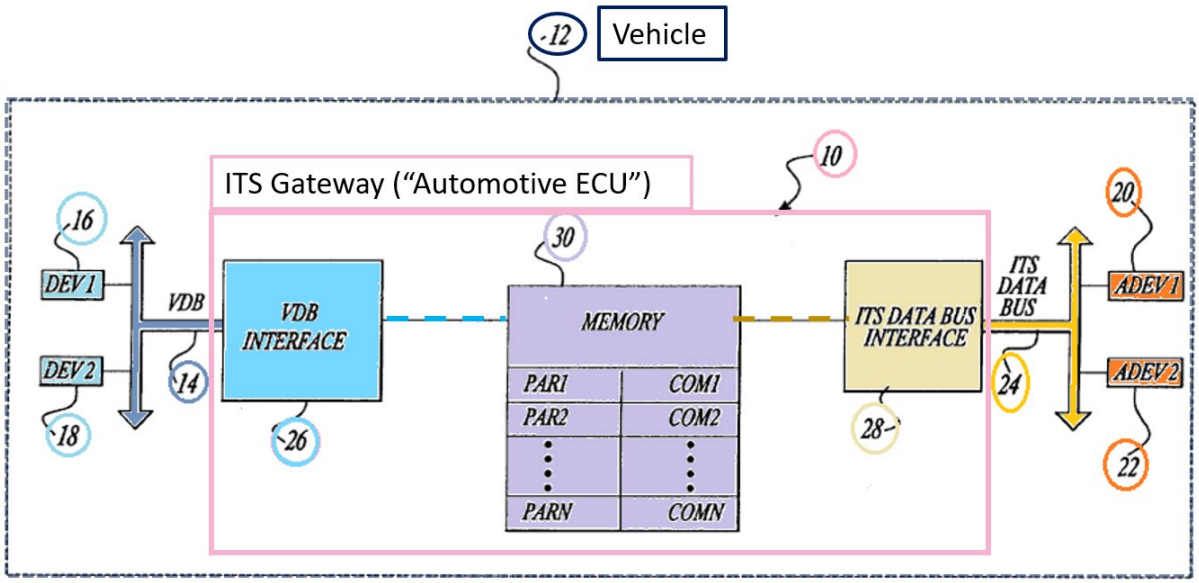


Fig-1

Miesterfeld, FIG. 1 (annotated)

1[b] and 1[c]: "at least one hardware processor in hardwired communication with the memory storage, wherein the at least one hardware processor executes the instructions for:"

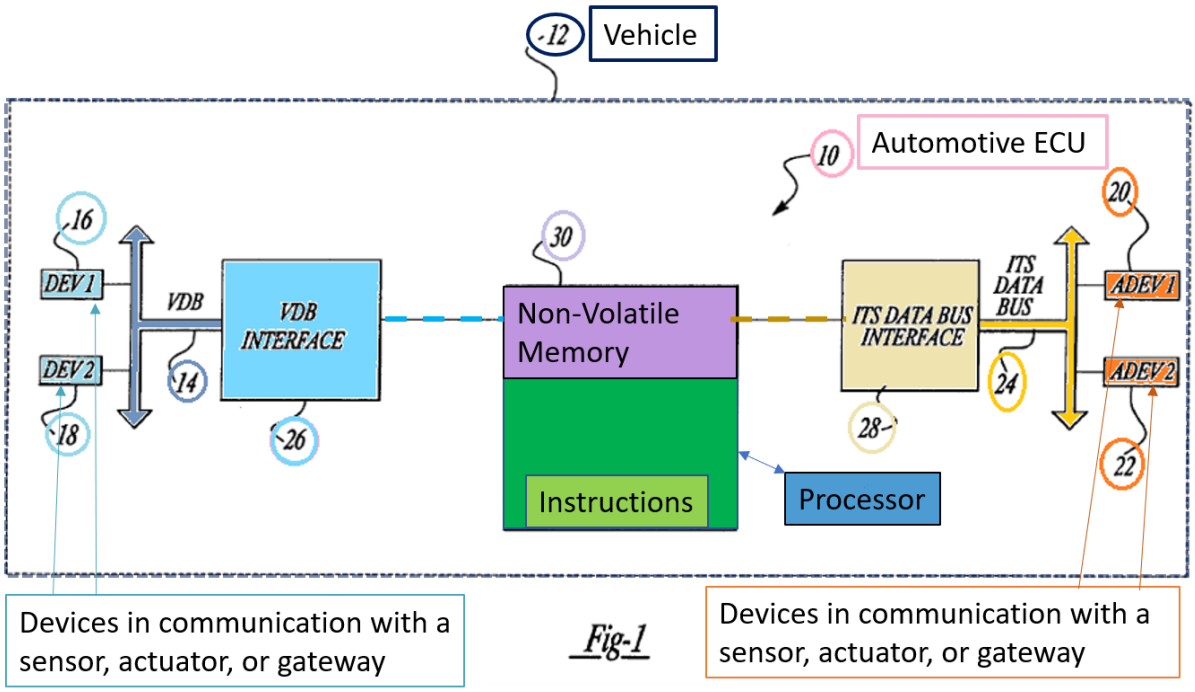
130. In my opinion, *Miesterfeld* at least suggests a hardware processor executing instruction and in hardwired communication with the memory storage because a POSITA would have understood that a processor and instructions are implicit to *Miesterfeld*'s gateway's functionality, *e.g.*, enabling data exchange between vehicle systems and third party systems, and controlling information sharing between electronic control devices on the VDB and the ITS data bus for the purpose of monitoring and controlling vehicle functions. *Miesterfeld*, 1:13–40, 2:66–3:49.

131. It is also my opinion that *Wong* renders this feature obvious because *Wong* expressly teaches an automobile control unit (also called "cluster controller") including a processor, volatile memory, non-volatile memory, and a processor in hardwired communication with each memory. *Wong*, Fig. 4, 3:27-30, 6:4-6.

132. In my opinion, a POSITA would have been motivated to incorporate *Wong*'s processor in *Miesterfeld*'s ITS gateway, whereby the processor is hardwired to the memory and executes instructions, to facilitate data processing for the purpose of monitoring and controlling vehicle functions. *Wong*, 6 10-21, 36-43; 7:51-60.

1[d]: "receiving sensor information associated with a message;"

133. *Miesterfeld*'s gateway receives information obtained from devices 16, 18, 20 and 22 data over the VDB and ITS data bus. *Miesterfeld*, Fig. 1, abstract, 2:66-3:25. The information obtained from devices 16, 18, 20 and 22 pertains to sensor information because it relates to measured vehicle data. *Id.*, 3:2-25, 1:13-25 (explaining that devices 16 and 18 "control vehicle operations such as engine operation, transmission operation, instrumentation operation, and the like"), 1:31-40, 3:14-17 (explaining that devices 20 and 22 "require vehicle data as input in order to operate the device or implement some additional feature on the vehicle" and "may also seek to control vehicle functions where appropriate and safe"). *Miesterfeld*'s sensor information is associated with a message because it is stored and accessible through memory read/write operations. *Miesterfeld*, 2:66-3:1, 3:18-25, 3:40-43, 3:59-64, *see also id.*, 1:62-2:15 (describing gateway functions for exchanging data between networks). Thus, it is my opinion that *Miesterfeld*'s process includes receiving sensor information associated with a message from either VDB 14 or ITS data bus 24.

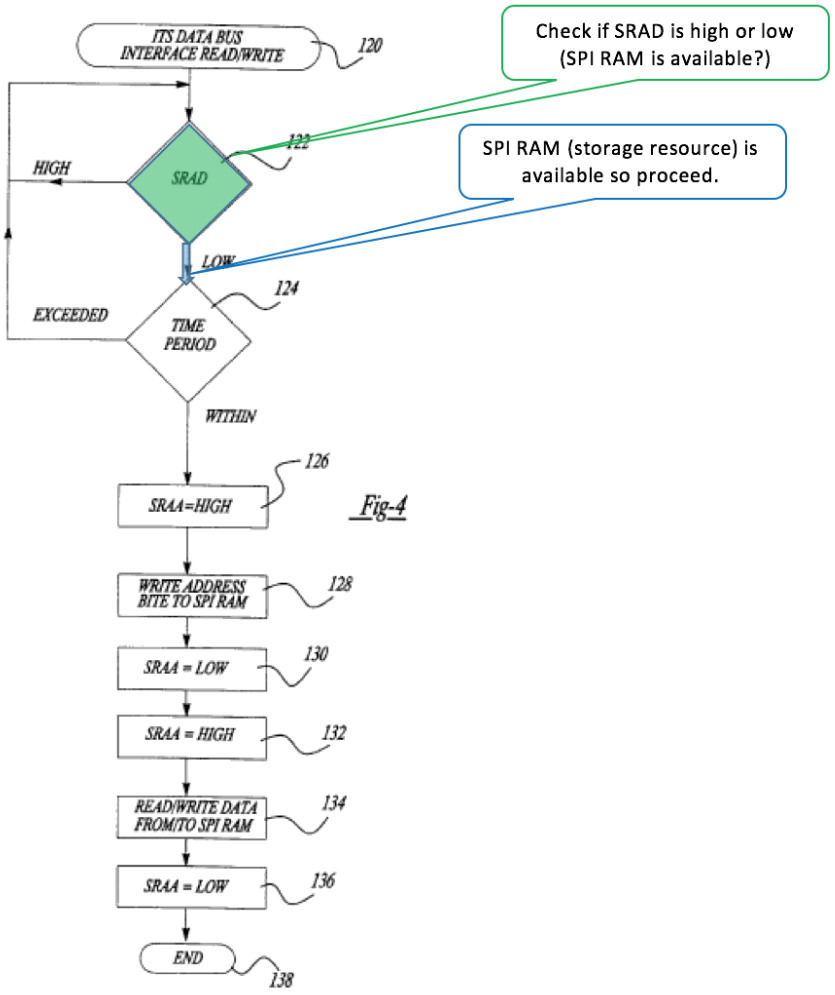


Miesterfeld, FIG. 1 (annotated)

1[e]: "in response to receiving the sensor information, issuing, by the at least one hardware processor and to a storage resource included in the automotive electronic control unit, a storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information and,"

134. *Miesterfeld* as modified by *Wong* teaches issuing a request to access a storage resource to store information in response to receiving the information. *Miesterfeld* explains, for example, that when ITS data bus interface 58 (another example of the ITS data bus interface 28 shown in FIG. 1) "attempts to access SPI RAM 64" (a specific implementation of memory 30) such as for reading or

writing, "the ITS data bus interface 58 must first test the SRAD signal line as shown at block 122." *Miesterfeld*, 6:34-36. *Miesterfeld*'s "attempts to access SPI RAM 64" is a request to access a storage resource (memory). *Miesterfeld*, 3:26-39, 3:64-66. *Miesterfeld* discloses that before reading or writing to the shared memory, the ITS data bus interface first determines whether the shared memory is available by checking whether the SPI RAM Access Denied (SRAD) signal line is high—if SRAD is high, the SPI RAM is unavailable. *Miesterfeld*, 6:33-40; *see also id.*, 4:11-26, 5:32-43. Checking whether the SRAD signal line is available corresponds to "issuing" a storage resource request to access the shared memory.



Miesterfeld, FIG. 4 (annotated)

1[f]: "in response to issuing the storage resource request, determining whether the storage resource is available to store the sensor information;"

135. *Miesterfeld* discloses determining whether the storage resource is available for storing the information. As shown above in annotated FIG. 4., *Miesterfeld* discloses that "[i]f SRAD is high, the VDB interface 62 is accessing SPI RAM 64, and ITS data bus interface 58 must wait until SPI RAM 64 is

available, and control returns to block 122," but "[i]f SRAD is low, SPIRAM 64 is available." *Miesterfeld*, 4:22-26, 5:38-43, 6:33-40; Checking the state of SRAD to determine if another bus interface is accessing the storage resource corresponds to "determining whether the storage resource is available to store the sensor information."

1[g]: "determining whether a threshold tracked since the issuance of the storage resource request has been reached indicating that the storage resource has not been available in association with the threshold tracked since the issuance of the storage resource request;"

136. *Miesterfeld* discloses determining whether a threshold tracked since issuance of the storage resource request has been reached. *Miesterfeld*, 6:46-50. As shown in annotated FIG. 4, *Miesterfeld* discloses that "[w]hen ITS data bus interface 58 determines that SPI RAM 64 is available, ITS data bus interface 58 sets the SRAA signal line high, as shown at block 126" and that "in a preferred embodiment, setting SRAA high must occur within 5 micro-seconds after determining that the SRAD signal line is low." *Miesterfeld*, 6:40-45. By checking in step 124 whether the 5-microsecond threshold has been reached in connection with the storage resource request (red), *Miesterfeld*'s process determines whether a threshold has been reached in association with the storage resource request. Because the countdown to 5 microseconds begins as soon as the SRAD signal line

is determined to be low, the threshold (a timeout) is "tracked since the issuance of the storage request."

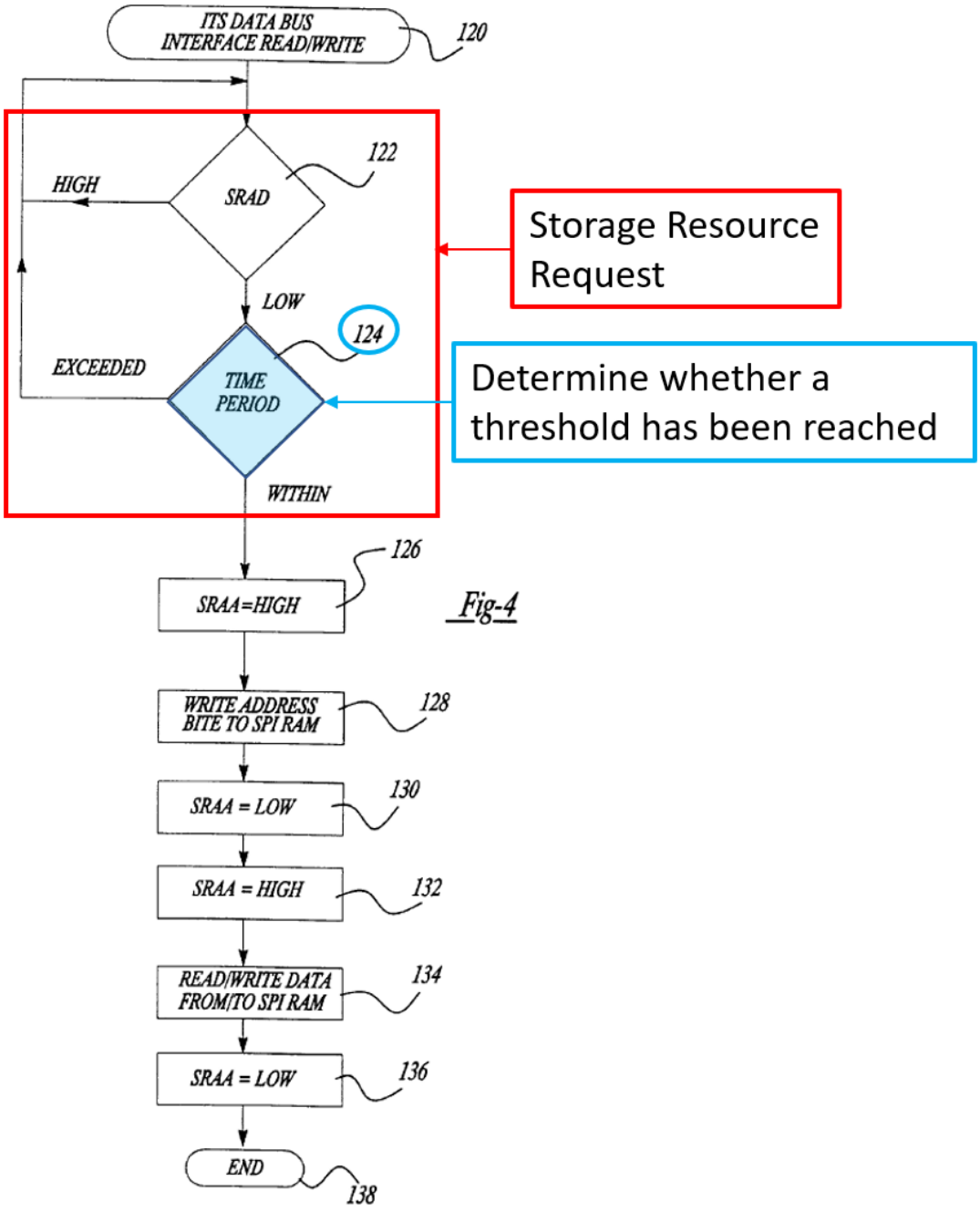
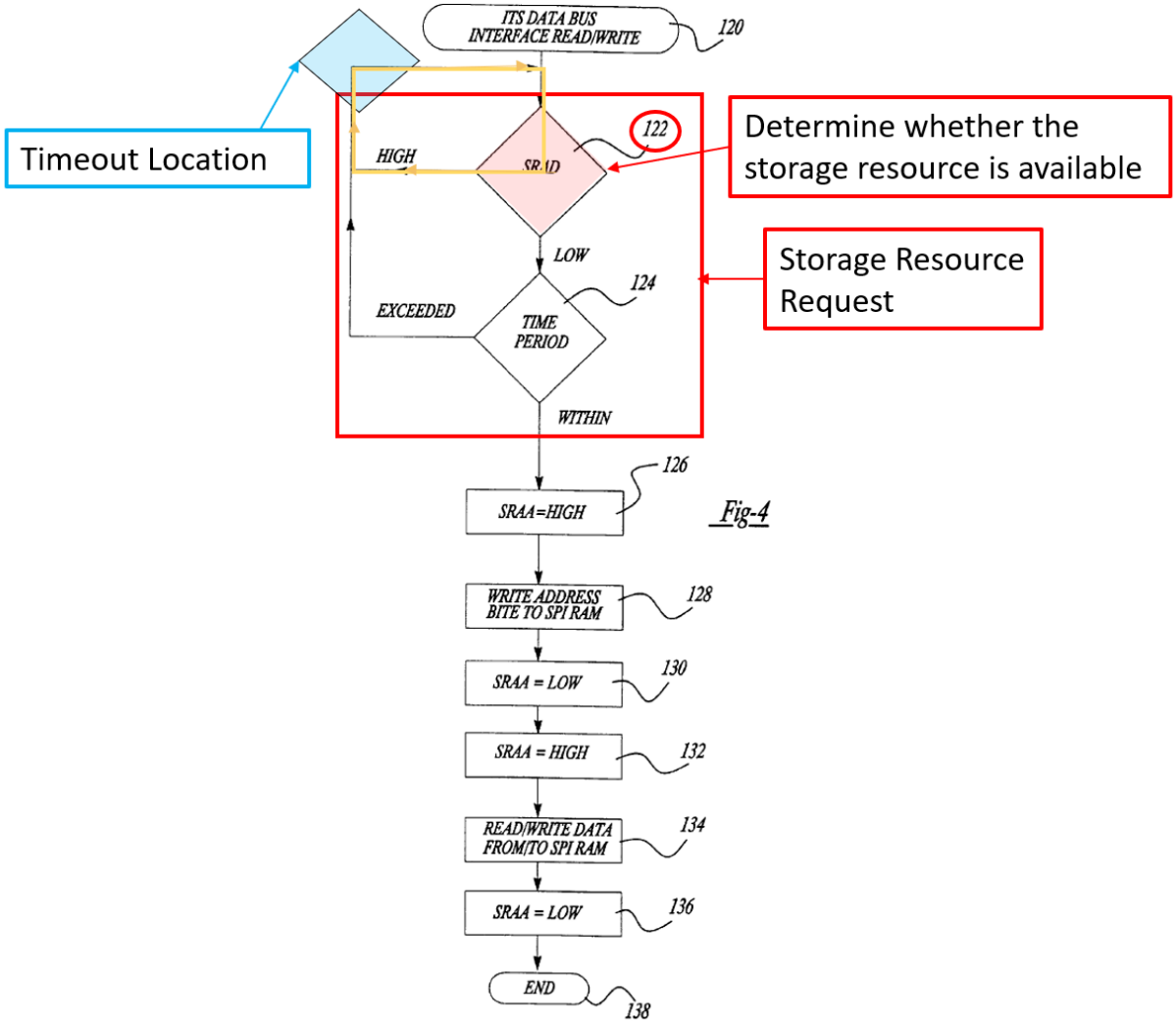


Fig-4

Miesterfeld, FIG. 4 (annotated)

137. It is my opinion that *Stewart* also renders this feature obvious because *Stewart* teaches a multiprocessor synchronization method in which a "bounding wait time" (threshold) is implemented to "guarantee that tasks will get the data they require on time, every time." *Stewart*, 330. *Stewart* also teaches implementing a "time-out mechanism" (threshold) for preventing data transfer when a "pre-specified time or number of retries" elapses. *Stewart*, 330 (emphasis added).

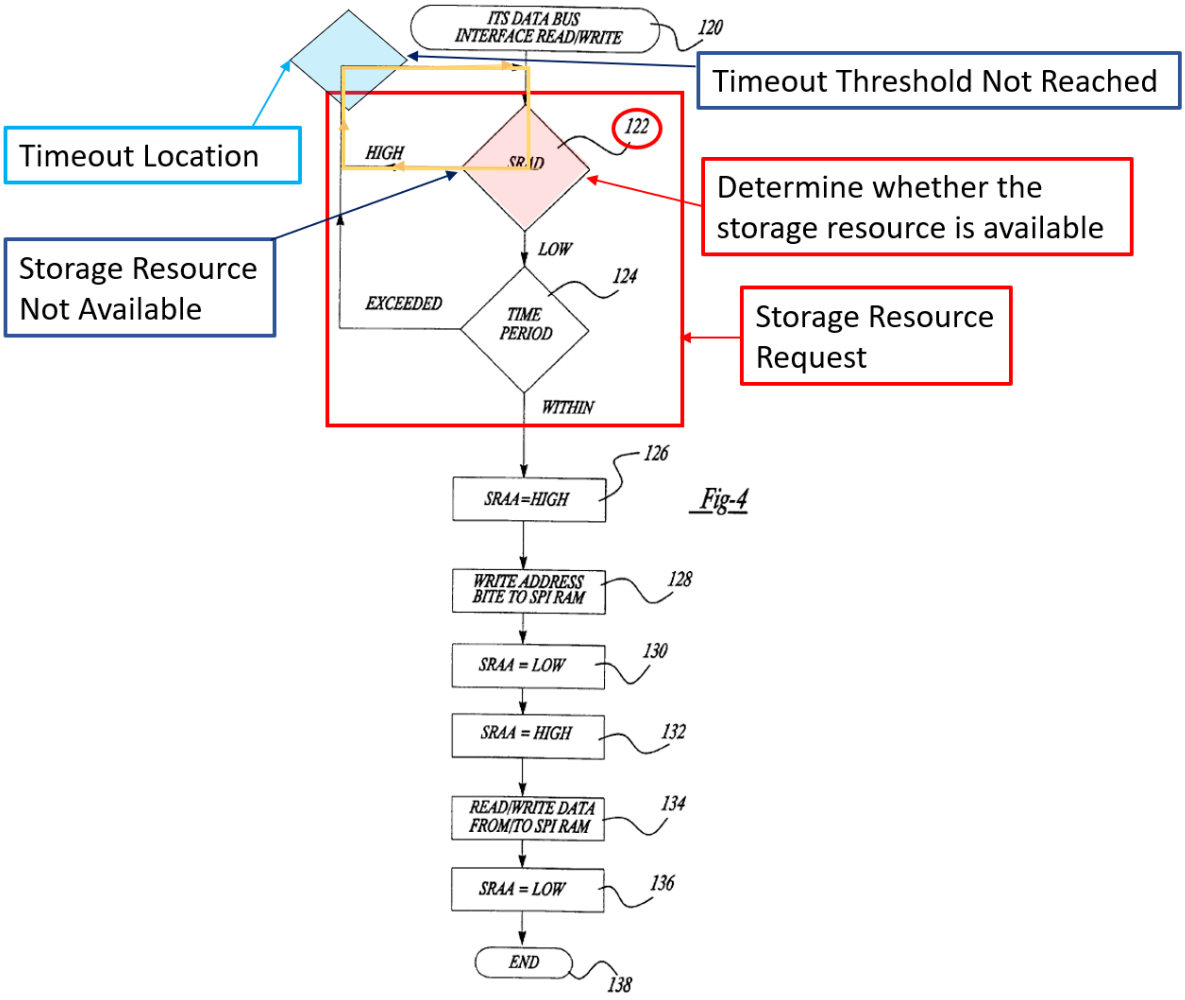
138. In my opinion, it would have been obvious to a POSITA to modify *Miesterfeld*'s process to implement a timeout threshold (blue) in the logical loop (yellow) as illustrated in annotated Fig. 4 below to ensure timely and consistent data exchange.



Miesterfeld, FIG. 4 (annotated)

1[h]: "when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has not been reached indicating that the storage resource has not been available in association with the threshold tracked since the issuance of the storage resource request, issuing, by the at least one hardware processor to the storage resource included in the automotive electronic control unit, another storage resource request to access the storage resource included in the automotive electronic control unit to store the sensor information;"

139. *Miesterfeld* discloses repeating the storage resource request if SRAD is high (issuing another storage resource request "when the storage resource is not available"). *Miesterfeld*, Fig. 4. As discussed above in element 1[g], *Stewart's* timeout operates by preventing data transfer if the number of retries has not been exceeded; thus, the combination is such that *Miesterfeld*'s request repeats if a "pre-specified" number of retries have not elapsed. *Stewart*, 330.



Miesterfeld, FIG. 4 (annotated)

1[i]: "when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request or the another storage resource request, to not be available and the threshold tracked since the issuance of the storage resource request has been reached, sending an error notification; and"

140. *Miesterfeld* in combination with *Stewart* teaches sending an error notification when the threshold is reached. *Stewart* discloses that "error handlers should be installed to detect tasks that suffer successive time-out errors." *Stewart*,

330. It is my opinion that a POSITA would have understood that *Stewart*'s error handlers not only detect the error but that the use of "error handlers" discloses or render obvious error notification as is well known in the art. Indeed, a POSITA would have understood that error detection without notification is useless and would have found it obvious for the error handlers to do so. Such notification may have been embodied as an exit code or error message.

141. Thus, in my opinion, it would have been further obvious to a POSITA to modify *Miesterfeld*'s system to incorporate error handlers, such handlers providing an error notification in the form of e.g., an exit code or an error message, as at least suggested by *Stewart*. *See also* Ex-1012, 137-38, 149-51, 154-56 (explaining that using a timeout to prevent deadlock, which could lead to program failure, was well-known in the art).

1[j]: "when the storage resource included in the automotive electronic control unit is determined, in response to issuing the storage resource request or the another storage resource request, to be available, storing the sensor information utilizing the storage resource;"

142. *Miesterfeld* discloses that the ITS data bus stores data in the SPI RAM (shared memory/storage resource) after the "ITS data bus interface 58 determines that the SPI RAM 64 is available," and sets the SPI RAM Access Required (SRAA) signal line to high. *Miesterfeld*, 6:40-54. Thus, as illustrated in annotated

Fig. 4 below, *Miesterfeld* discloses storing the data (sensor information) using the shared memory (storage resource) if the shared memory is available.

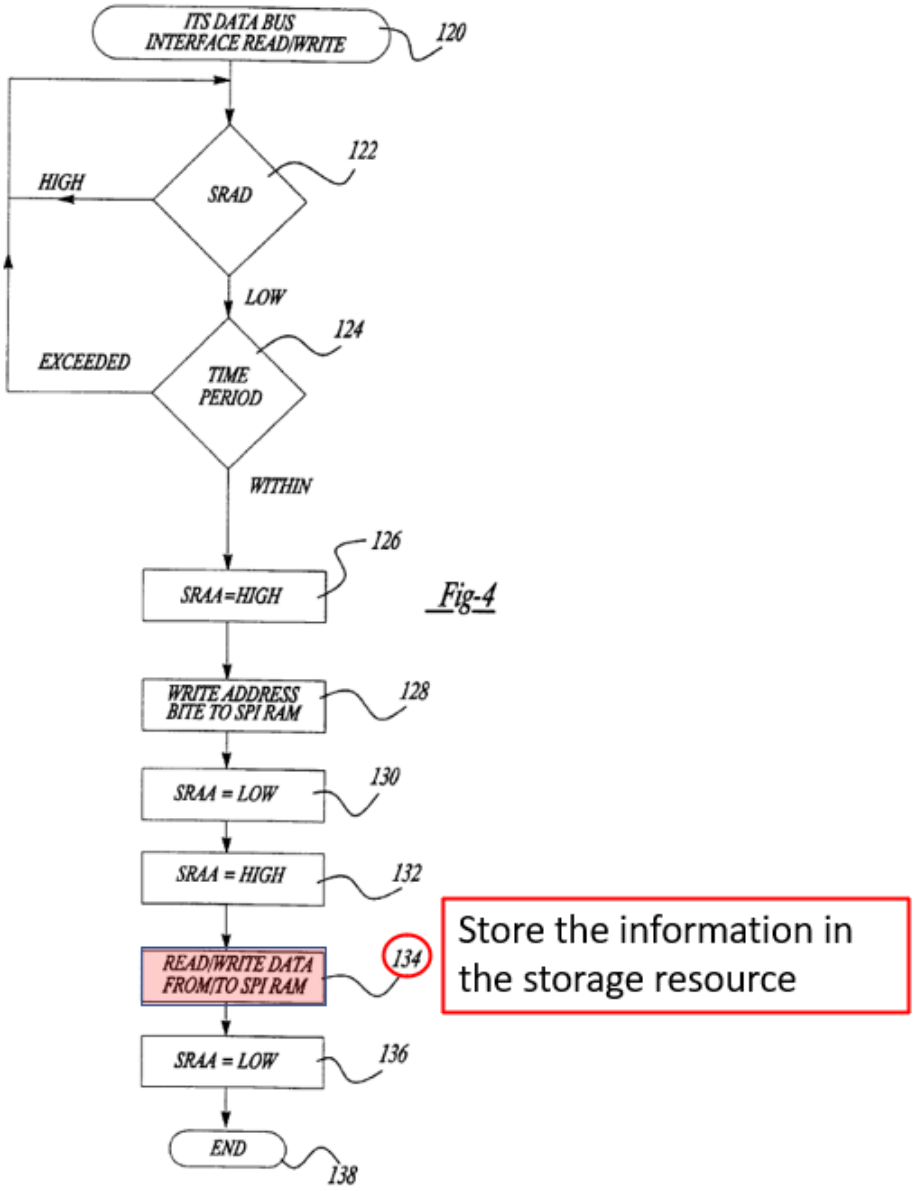


Fig-4

Miesterfeld, FIG. 4 (annotated)

1[k]: "wherein the automotive electronic control unit is operable such that the sensor information is capable of being shared in less than one second, and"

143. *Miesterfeld* discloses that "the time period between selecting the desired memory page and reading/writing data to SPI RAM 64 (between steps 130 and 132) is less than 5 microseconds." *Miesterfeld*, 6:60-63, Fig. 4. *Miesterfeld* also explains that the VDB interface may transmit any data received from the ITS data bus within ***40 milliseconds***. *Id.*, 8:51-56 (emphasis added). Thus, *Miesterfeld* discloses that the data is capable of being shared in less than one second.

1[l]: "the automotive electronic control unit includes a plurality of interfaces including: a first interface; and a second interface for interfacing with a network, where the network is at least one of a Controller Area Network, a Flexray network, or a Local Interconnect Network."

144. *Miesterfeld*'s gateway includes an ITS data bus interface for interfacing with an ITS data bus (a first network) and interconnected devices 20 and 22, and a VDB interface for interfacing with a VDB (a second network) and interconnected devices 16 and 18. *Miesterfeld*, Fig. 1, 3:20-25. Thus, *Miesterfeld* discloses a first interface and a second interface for interfacing with a network of interconnected devices.

145. It is my opinion that *Miesterfeld* at least suggests that the network is at least one of a Controller Area Network *(*CAN), a Flexray network, or a Local Interconnect Network (LIN) because the ITS data bus 24 (first network) may be

"any of a number of ITS data buses, such as D_2B, USB, IDB, Firewall, and the like" (*Miesterfeld*, 4:5-10, 9:55-57) and the VDB 14 (second network) may be "configured to implement the J1850 configuration as prescribed by the Society of Automotive Engineers (SAE) or any other industry standard as may be required." *Id.*, 4:7-10.

146. To the extent this requires further clarification, *Wense* teaches that cars utilize "[s]everal multiplex protocols," including CAN (*e.g.*, for engine and body control networks), FlexRay (*e.g.*, for safety, braking, and steering systems), and LIN (*e.g.*, for cost-critical distributed body electronics). *Wense*, 11.

147. In my opinion, a POSITA would have found it obvious to implement *Miesterfeld*'s VDB and ITS using known bus architectures like CAN, FlexRay, or LIN, as taught by *Wense*, because each was a commonly-used and well-known vehicle data bus for controlling the various vehicle systems of *Miesterfeld*. *Wense*, 11; *Miesterfeld*, 4:7-10; Ex-1047, ¶¶31, 40, 48 (explaining concurrent use of legacy bus architectures such as CAN, LIN, FLEXRAY "provides for the total integration of vehicle systems and functions, and permits plug-and-play device integration, scalability and upgradeability."); Ex-1052, 1:21-32; Ex-1004, 2 ("[t]he automotive industry has developed the [CAN] [] in the 1980s and subsequently added new communication bus systems such as MOST, IDB, LIN, and FlexRay.").

Independent Claim 27

148. As discussed above in Ground 1, independent claim 27 largely mirrors independent claim 1. The differences are accounted for and rendered obvious by *Miesterfeld*, *Wong*, *Stewart*, and *Wense* for the same reasons set forth for independent claim 1.

149. For example, as explained for 1[l], *Miesterfeld* discloses an ITS data bus interface for interfacing with an ITS data bus (first network) and interconnected devices 20 and 22, and a VDB interface for interfacing with a VDB (second network) and interconnected devices 16 and 18. *Miesterfeld*, Fig. 1, 3:20-25. *Wense* renders obvious the first network being one of a Controller Area Network, a FlexRay network, or a Local Interconnect Network; and the second network being another one of the Controller Area Network, the FlexRay network, or the Local Interconnect Network. *Wense*, 11; *See also* Ex-1047, ¶¶31, 40, 48; Ex-1052, 1:21-32.

Claims 2-7 and 28-33: sharing "in less than one [millisecond/second]."

150. Claims 2-7 and 28-33 are obvious over *Miesterfeld*, in combination with *Wong*, *Stewart*, and *Wense*. Dependent claims 2-7 and 28-33 each require some sharing event to occur "in less than one second," "in less than one millisecond," or "with sufficient speed for use in connection with an automotive device." Claim 33 requires the computer program product to be configured for

sharing "in less than the one millisecond second [*sic*]." As explained for 1[k], *Miesterfeld* discloses sharing and storing of information across networks occurs within microseconds; thus, it is my opinion that each of these claims are disclosed by. *Miesterfeld*, 6:43-62, 8:51-56.

151. Claim 7 requires the system to be configured for sharing "with sufficient speed for use in connection with an automotive device." Ex. 1001, 13:44-47. *Miesterfeld* discloses this limitation because, as explained for 1[k], data is written and read (shared) in under 5 microseconds. *Miesterfeld*, 6:60-62. In my opinion A POSITA would have understood that this speed is "sufficient" "for use in connection with an automotive device," as recited in claim 7 and as evidenced by the specification of the '400 patent, which explains that "[i]n the context of the present description, real-time may include any response time that may be measured in milli- or microseconds, and/or is less than 1 second." Ex-1001, 3:45-49.

2. <u>Ground 3:</u> Claims 8-26 are obvious over *Miesterfeld* in view of *Wong*, *Stewart*, *Wense,* and *Ma*

152. *Ma* teaches apparatuses and methods for processing data packets in the data communications field. *Ma*, 1:7-10. *Ma* teaches that data packets include a data field and one or more header fields whereby the packet headers and their functions are "typically" arranged in an orderly fashion according to the open-systems interconnection (OSI) reference model (*id.*, 1:26-31) and explains that the

OSI model partitions packet communications functions into layers, each layer having a header stripped or prepended during data processing. *Id.*, 5:48-63. *Ma* simply clarifies what the standard components for data transmission are. It is my opinion that a POSITA would have had a reasonable expectation of success in configuring *Miesterfeld*'s interfaces to transmit sensor information using the OSI Reference model, whereby the information is packaged into a packet of layers, as taught by *Ma*. The modification would have required only ordinary skill. Implementing a datalink layer component for using data link layer header bits associated with the first network (CAN, LIN or FlexRay) and a network layer component for using the CAN, LIN or FlexRay network layer header bits, would have been routine for the same reasons.

Independent Claim 8

153. As discussed above in the *Lohrmann* Grounds, independent claim 8 largely mirrors claim 1, except that it is directed to an "apparatus" (Ex-1001, 13:48), and further recites a "first network" and corresponding "first interface," wherein "the first network is at least one of a Controller Area Network type, a Flexray network type, or a Local Interconnect Network type;" and a "second network" and corresponding "second interface," wherein "the second network is at least one of the Controller Area Network type, the Flexray network type, or the

Local Interconnect Network type." *Id.*, 14:39-57. Each of these limitations are obvious for the reasons discussed in claim 1.

154. For example, as explained in 1[l], *Miesterfeld* further discloses that the gateway includes a plurality of interfaces—an ITS data bus interface for interfacing with an ITS data bus (first network) and interconnected devices 20 and 22 and a VDB interface for interfacing with a VDB (second network) and interconnected devices 16 and 18. *Miesterfeld*, Fig. 1, 3:20-25. Thus, *Miesterfeld* discloses a "first network" (VDB) and corresponding "first interface" (VDB Interface), a "second network" (ITS data bus) and corresponding "second interface" (ITS data bus interface). In my opinion, a POSITA would have found it obvious to implement *Miesterfeld*'s VDB and ITS using known bus architectures like CAN, FlexRay, or LIN, as taught by *Wense*, because each was a commonly-used and well-known for controlling the various vehicle systems of *Miesterfeld*. *Wense*, 11. The proposed modification also teaches that the first and second network are "at least one of the Controller Area Network type, the Flexray network type, or the Local Interconnect Network type." *Id.* Annotated figure 1 below illustrates the combination.

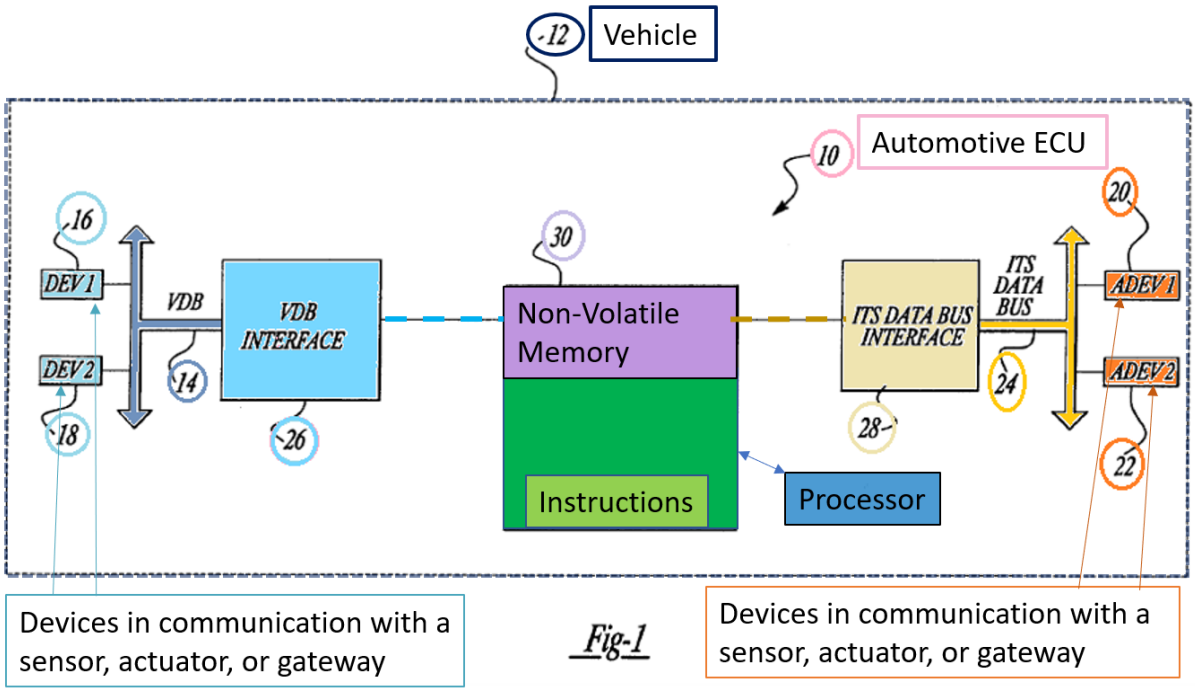


Fig-1

Miesterfeld, Fig. 1 (annotated)

155. Claim 8 also recites additional obvious features of the first and second interfaces.

> **the first interface including a first interface-related data link layer component for using first network-related data link layer header bits and a first interface-related network layer component for using first network-related network layer header bits,**

156. It is my opinion that A POSITA would have found it obvious to provide, or understood that *Miesterfeld*'s VDB interface includes, a data link layer component for using first network-related data link layer header bits and a first interface-related network layer component for using first network-related network layer header bits because the International Standards Organization (ISO), which

established the industry standard for automobile network communication at the time of the invention, required as much to facilitate communication using CAN, LIN, and FlexRay networks. Ex. 1046, 7 (establishing a CAN "serial communication protocol that supports distributed real-time control and multiplexing for use within road vehicles" and .explaining that the "layered" CAN architecture established by the OSI reference model includes a data link layer and a physical layer (PL) for bit encoding/decoding); *see also* Ex-1046 (explaining the "layered" CAN architecture established by the OSI reference model includes a data link layer and a physical layer (PL) for bit encoding/decoding. It is also my opinion that a POSITA would have found it obvious, if not necessary, to provide *Miesterfeld*'s VDB interface with a "network layer component for using first network-related header bits" to facilitate communication between either dissimilar network protocols or of messages that are too large for the data link layer, based on this standard.

157. To the extent this requires further clarification, *Ma* discloses transmitting data, as was well known in the communications field, in a "packet," including a data field and header field. *Ma*, 1:14-17. The data field contains "virtually any kind of digital data" and the header field conveys information identifying, *e.g.*, the packet's source or destination, the protocol to be used to interpret the packet, or the packet's place in a sequence of packets. *Id.*, 1:18-25.

Ma further discloses that the packet headers and their functions are "typically" arranged according to the open-systems inter connection (OSI) reference model in a plurality of hierarchical layers. *Id.*, 1: 28-34. Regarding the first three layers of the hierarchy, *Ma* states:

> Layer 1, the physical layer, is concerned with transmission of a bit stream over a physical link. Layer 2, the data link layer, provides mechanisms for the transfer of frames of data across a single physical link, typically using a link-layer header on each frame. Layer 3, the network layer, provides network-wide packet delivery and switching functionality—the well-known Internet Protocol (IP) is a layer 3 protocol.

Id. 1:34-41; *see also* Ex-1069, 3, 30 (explaining that the network layer facilitates data transmission across the data link layer. Thus, *Ma* teaches data link layer and network layer header bits, and corresponding mechanisms (components) for using the bits.

158. In my opinion, it would have been obvious to a POSITA to configure *Miesterfeld*'s VDB interface to transmit sensor information using the OSI Reference model, whereby the information is packaged into a packet of layers, as taught by *Ma*, to facilitate data transfer (sensor information transfer) and provide network-wide packet delivery. This configuration would have ensured compliance with the ISO and OSI reference model.

159. In my opinion, a POSITA would have further understood that the modification is such that the VDB interface includes a datalink layer component for using data link layer header bits associated with the first network (CAN, LIN or FlexRay) and a network layer component for using the CAN, LIN or FlexRay network layer header bits, because the interface needs to have the requisite "mechanisms" (components) to enable the transfer. *Ma*, 1:35-38.

the second interface including a second interface-related data link layer component for using second network-related data link layer header bits and a second interface-related network layer component for using second network-related network layer header bits, where the second network is at least one of the Controller Area Network type, the Flexray network type, or the Local Interconnect Network type.

160. In my opinion, a POSITA would have found it obvious to include, or understood that *Miesterfeld*'s ITS data bus interface (second interface) includes, a second interface-related data link layer component for using second network-related data link layer header bits and a second interface-related network layer component for using second network-related network layer header bits for the same reasons explained in for the VDB interface (first interface).

Claim 9: "The apparatus as recited in claim 8, wherein the apparatus is operable such that network layer translation is capable of being avoided."

161. *Miesterfeld* discloses that network layer translation is avoidable because *Miesterfeld* uses data lines and bus interfaces to read and write data.

Miesterfeld, 5:20-31. *Miesterfeld* discloses that VDB interface 62 communicates with SPI RAM 64 through a pair of data lines 66a, 66b, and a serial clock line 66c to define SPI bus 66. *Id.*, 5:20-22. Line 66a is a master-in-slave-out (MISO) data line that enables a master device to read data from the slaved SPI RAM 64, data line 66b is a master-out-slave-in (MOSI) data line that enables a master device to output data to the slaved SPI RAM 64, and the VDB and ITS data bus interfaces each function as master devices with respect to slaved device SPI RAM 64. *Id.*, 5:22-31. Therefore, in my opinion, a POSITA would have understood that *Miesterfeld*'s system translates between VDB and ITS buses without network layer translation because it uses bus lines which do not need to use network level addresses.

Claims 10 and 11: sharing "in less than one second [a millisecond]."

162. Dependent claims 10 and 11 recite identical limitations to dependent claims 2 and 3. In my opinion, claims 10 and 11 are therefore obvious for the same reasons as claims 2 and 3.

Claim 12: "The apparatus as recited in claim 11, wherein the apparatus is operable such that the sensor information is shared by the second interface-related network layer component using the second network-related network layer header bits by adding the second network-related network layer header bits to a data unit including the sensor information, and then the second interface-related data link layer component using the second network-related data link layer header bits by adding the second network-related data link layer header bits to the data unit, before communicating the data unit on a physical link of the second network."

163. *Ma* discloses that data packet transmission includes adding an L2 (data link layer) header to the packet (*i.e.*, stripping and rewriting the packet header), and "prepend[ing]" a network layer header to the packet prior to transmission. *Ma*, 5:40-47, 11:23-33. This packet processing ensures "delivery and interpretation of the packet contents." *Id.* 1: 17-21.

164. Thus, the combination teaches adding the second network-related network layer header bits and adding the second network-related data link layer header bits to the packet, which includes the sensor information, before communicating the data on a physical link of the network, as is well known in the art. *See also* Ex 1054, 2:43-62 (explaining that "a transport header, network header and data link header … [are] attached to the data at each of those layers, with each step typically including data moving and copying, before sending the data as bit packets, over the network, to the second host").

Claim 13: "The apparatus as recited in claim 12, wherein the apparatus is operable such that the first interface-related data link layer component uses the first network-related data link layer header bits by removing the first network-related data link layer header bits from another data unit, and the first interface-related network layer component uses the first network-related network layer header bits by removing the first network-related network layer header bits from the another data unit so that the sensor information is removed from the another data unit, before the sharing."

165. *Ma* discloses that when a network interface receives the data packet, the packet's headers are "modified"—that is, the L2 headers are "stripped" and the backplane header (*i.e.*, the network layer header) is removed. *Ma*, 5:48-61; 11:41-47.

166. Thus, the combination teaches removing the first network-related data link layer header bits (layer 2) from "another data unit" and removing the first network-related network layer header bits (layer 3) from the "another data unit" so that the information is removed from the "another data unit" as is well known in the art, *See also* Ex 1054, 2:63-3:7 (explaining "headers are removed and data processed in order from the lowest (Physical) layer to the highest (Application) layer" when data packets are received).

Claims 14 and 15: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the storage resource request and the another storage resource request are identical [the same]."

167. As explained for 1[h], *Miesterfeld* discloses repeating the storage resource request process ("issuing … another storage resource request to access the storage resource") if SRAD is high ("when the storage resource is not available"). *Miesterfeld*, Fig. 4, 6:33-43. This is the exact procedure described in the '400 patent's specification, which discloses repeating the storage resource request. Ex-1001, 8:36-37 ("If the resource is not available, it may try it again after a waiting period (1011) until the resource is available."). In my opinion, a POSITA would have understood that *Miesterfeld* discloses that "the another storage resource request" is identical to, or the same as, "the storage resource request" to the extent the '400 patent discloses the same.

Claims 16 and 17: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the sensor information excludes all [a portion of any] header bits of the message."

168. As explained for claim 13, header bits are removed from the data packet upon receipt. Because the data being received in the instant combination is sensor information, it is my opinion that a POSITA would have understood that the portion of a message that is "sensor information" excludes all header bits of the message. Because "at least a portion of any header bits of the message" is excluded

if "all header bits of the message" are excluded, claim 17, in my opinion, is obvious for the same reasons as claim 16.

Claim 18: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the storage resource includes a bulletin board."

169. *Miesterfeld* discloses that the "[m]emory 30 is accessible to both VDB interface 26 and ITS data bus interface 28 so that each interface will be able [to] read from and/or write to memory 30." *Miesterfeld*, 3:40-43. That is, any network connected to ITS gateway 10 has access to memory 30 and can store data in or retrieve data from the database stored there. In my opinion, a POSITA would have understood that *Miesterfeld*'s database is a "bulletin board" because it enables devices on different networks to read and write data to the database in the memory. *Miesterfeld*, 3:18-4:31.

Claims 19-21: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the error notification is sent, when the storage resource included in the automotive electronic control unit is determined, in response to issuing the [another] storage resource request [and the another storage resource request], to not be available and the threshold tracked since the issuance of the storage resource request has been reached."

170. Claims 19-21 are similar as explained in Ground 1.

171. As discussed above with respect to claim element 1[i], *Miesterfeld* in combination with *Stewart* teaches sending an error notification when the storage resource is determined to be unavailable "in response to issuing the storage

resource request or the another storage resource request" and reaching the threshold. Thus, it is my opinion that claims 19 and 20 are rendered obvious by the combination for the same reason as 1[i].

172. As discussed above in 1[h] and 1[i], *Miesterfeld*'s modified process is iterative such that storage resource may be determined to be unavailable after issuing another request and reaching the threshold. *Miesterfeld,* Fig. 4; *Stewar*t, 330. This occurs, for example, when the number of attempts (which includes "the request" and the "another request") exceeds the threshold. *Stewart*, 330. Thus, it is my opinion that the modified system teaches sending an error notification when the storage resource is determined to be unavailable in "response to issuing the storage request and the another storage request" and reaching the threshold, as recited in claim 21.

Claims 22 and 26: "The apparatus as recited in claim 8, wherein at least one of: the memory storage includes the storage resource; the memory storage does not include the storage resource…."

173. Claims 22 and 26 require "at least one of" numerous features describing the apparatus of claim 8. Ex-1001, 15:62-16:62, 17:13-2132. These features are listed in the alternative. Because "at least one" of these features, *e.g.*, "the memory storage includes the storage resource," is taught by the combination of *Miesterfeld*, *Wong*, *Wense*, and *Stewart*, it is my opinion that claims 22 and 26 are obvious for same reasons explained for claim 8.

Claim 23: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the information associated with the message is identified in another storage resource that stores the information after the message is received."

174. A POSITA would have understood that *Miesterfeld* at least suggests that one option for facilitating the exchange of sensor information involves at least temporarily storing the data in another storage resource because *Miesterfeld* discloses "desirable" data exchange between VDB 14 and ITS data bus 24. *Miesterfeld,* 3:18-24. A POSITA would have understood that it is desirable to temporarily store the sensor data to prevent it from being lost, for example during periods of contention for access to limited bus, network, or permanent storage resources.

175. Even if *Miesterfeld* does not expressly disclose using "another storage resource" to identify and store the information associated with the message read/written from memory 30, it is my opinion that *Wong* renders this limitation obvious.

176. As explained for 1[b], *Wong*, discloses systems for facilitating communication between automobile components. *Wong*, abstract, 2:41-45. *Wong*'s components are grouped into logical clusters (each cluster having its own controller for managing information flow among the cluster's components) and the cluster controllers are interconnected via another data communications bus (bus

28) to enable information flow between clusters. *Id.*, abstract, 2:54-61, 5:34-42. Each cluster has its own local memory, so that information shared between clusters is stored in the cluster controller's local memory (*id.*, 6:4-9), and "any component in one cluster can share information with any component in another cluster without need for dedicated wiring or specially written code." *Id.*, abstract

177. In my opinion, it would have been obvious to a POSITA to configure *Miesterfeld* to include two storage resources (the storage resource and "another" storage resource"), whereby the other storage resource identifies and stores the information associated with the message, as disclosed by *Wong*, to facilitate data exchange between data buses. *Wong*, 4:62-67. In this *Miesterfeld-Wong* combination, *Wong*'s storage resource (SPI RAM) is accessed in accordance with *Miesterfeld* (as explained for 1[e]), and "the another" storage resource is utilized to (at least temporarily) store information shared between the devices (automobile components) and their corresponding VDB or ITS, as taught by *Wong*.

Claim 24: "The apparatus as recited in claim 8, wherein the apparatus is operable such that the information associated with the message is identified in another storage resource that stores the information after the message is received and before the information is stored utilizing the storage resource, the another storage resource capable of being used for information storage,

regardless as to a particular network with which the information is shared."

178. As explained for claim 23, *Wong* teaches identifying the information after receiving, and prior to storing it in local memory. *Wong*'s local memory is capable of storing the information, regardless of the network with which the information is shared. *Wong*, 6:4-9.

Claim 25: "The apparatus as recited in claim 24, wherein the apparatus is operable such that the information is stored utilizing the another storage resource in response to a corresponding request that is separate from the storage resource request."

179. As explained for claim 23, the combination's storage resource (SPI RAM) is accessed according to *Miesterfeld* and "the another" storage resource of *Wong* is utilized to (at least temporarily) store information shared between the devices (automobile components) and their corresponding data buses. In this configuration, the request to store information in the local memory (another storage) is separate from the storage resource request, *i.e.*, the request to access shared memory/SPI RAM 30. *Wong*, 5:17-42 (explaining that the process of sharing data between controllers (akin to reading/writing data from IDS/VDB to *Miesterfeld*'s shared memory) is distinct from the process of sharing/storing data from the automobile components and the local memory of each controller (akin to reading/writing data from devices 16, 18, 20, 22 to a local memory associated with the VDN and ITS)).

XI. CONCLUSION

180. As discussed above, it is my opinion that the Challenged Claims are obvious over the above-cited references.

181. I reserve the right to supplement my opinions in the future to account for new information as it becomes available to me.

182. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on this Dec 30, 2022, in Johns Creek, GA.

By: _____
Dr. Vijay K. Madisetti