

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BMW OF NORTH AMERICA, LLC,
Petitioner,

v.

STRAGENT, LLC,
Patent Owner.

Case No. IPR2023-00334
U.S. Patent No. 11,354,179

DECLARATION OF DR. VIJAY K. MADISETTI

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I, Dr. Vijay K. Madiseti, declare as follows:

I. INTRODUCTION

1. I have been asked to submit this declaration on behalf of BMW of North America, LLC (Petitioner) in connection with a petition for inter partes review (IPR) of U.S. Patent No. 11,354,179 (the '179 patent), which I have been told is being submitted to the Patent Trial and Appeal Board of the United States Patent and Trademark Office by Petitioner. I understand that the '179 patent is Exhibit 1001 to the petition for IPR of the '179 patent.

2. Specifically, I have been retained as a technical expert by Petitioner to study and provide my opinions on the technology claimed in, and the patentability or unpatentability of, claims 1-27 of the '179 patent ("the challenged claims"). For purposes of this declaration, I was not asked to provide any opinions that are not expressed herein

II. SUMMARY OF OPINIONS

3. This declaration is directed to the challenged claims of the '179 patent, and sets forth the opinions I have formed, the conclusions I have reached, and the bases for each. Based on my experience, knowledge of the art as of the effective filing date of the '179 patent, analysis of prior art references, and the understanding a person of ordinary skill in the art would have had of the claim terms in light of the specification as of the effective filing date, it is my opinion

that the challenged claims of the '179 patent are unpatentable over the prior-art references discussed below.

III. BACKGROUND AND QUALIFICATIONS

4. I am a tenured Professor in the Colleges of Computing and Engineering at the Georgia Institute of Technology ("Georgia Tech"). I have worked within the area of embedded computing systems, wireless communications, and digital signal processing for over twenty-five years, and have authored, co-authored, or edited several books and numerous peer-reviewed technical papers in these areas.

5. I received my B. Tech (Hons) in ECE from the Indian Institute of Technology (IIT), Kharagpur, India in 1984. I obtained my Ph.D. in Electrical Engineering and Computer Science at the University of California, Berkeley, in 1989. I received the Demetri Angelakos Outstanding Graduate Student Award from the University of California, Berkeley and the IEEE/ACM Ira M. Kay Memorial Paper Prize in 1989.

6. I joined Georgia Tech in Fall of 1989 and am now a tenured Professor in Electrical and Computer Engineering. I have been active in the areas of computer systems, embedded systems, multimedia (audio, video, speech, wireless, etc.), wireless communications, digital signal processing, integrated circuit design (analog & digital), software engineering, system-level design

methodologies and tools, and software systems. I have been the principal investigator ("PI") or co-PI in several active research programs in these areas, including DARPA's Rapid Prototyping of Application Specific Signal Processors, the State of Georgia's Yamacraw Initiative, the United States Army's Federated Sensors Laboratory Program, and the United States Air Force Electronics Parts Obsolescence Initiative. I have received an IBM Faculty Award and NSF's Research Initiation Award. I have been awarded the 2006 Frederick Emmons Terman Medal by the American Society of Engineering Education for contributions to Electrical Engineering, including authoring a widely used textbook in the design of VLSI digital signal processors.

7. I have created and taught undergraduate and graduate courses in hardware and software design for computer systems, control systems, signal processing and wireless communication circuits at Georgia Tech for the past twenty years.

8. I have been an active consultant to the electronics and automation industries and various research laboratories (including Massachusetts Institute of Technology Lincoln Labs and Johns Hopkins University Applied Physics Laboratory ("APL")). I have founded three companies in the areas of embedded avionics and wireless software, military chipsets involving imaging technology and guidance technologies, and wireless communications. I have supervised the Ph.D.

dissertations of over twenty engineers in the areas of computer engineering, signal processing, communications, rapid prototyping, and system-level design methodology, of which five have resulted in thesis prizes or paper awards.

9. My consulting work for MIT Lincoln Labs involved high resolution imaging for defense avionics applications, where I worked in the area of prototyping complex and specialized computing systems. My consulting work for the APL mainly involved localization of objects in image fields, where I worked on identifying targets in video and other sensor fields and identifying avionics computer architectures and circuits for power and space-efficient designs.

10. I have developed wireless baseband and protocol stack software and assembly code for a leading telecommunications handset vendor that focused on efficient realization of speech codecs and echo-cancellation. My work in this regard included creation of software code, and analysis and revision of existing software code. This work spanned approximately three years of industry work between 2000 and 2004.

11. The first of the companies I founded, VP Technologies, offers products in the area of semiconductor integrated circuits, including building computing systems for imaging systems in United States Air Force helicopters. I remain a director of VP Technologies. The second of these companies, Soft Networks, LLC, offers software for multimedia and wireless computing platforms,

including the development of a set-top box for Intel that decodes MPEG-2 video streams and imaging codes for multimedia phones. The technology involved with the design, development, and implementation of the Intel set-top box included parsing the bit streams, decoding communications protocols, extracting image and video data, and then processing for subsequent display or storage. The third of these companies, Elastic Video, uses region of interest based video encoding or decoding for capturing high quality video at very low bit rates, with primary application for wireless video systems.

12. I have been elected a Fellow of the IEEE, for contributions to embedded computing systems. The Fellow is the highest grade of membership of the IEEE, a world professional body consisting of over 300,000 electrical and electronics engineers, with only one-tenth of one percent (0.1%) of the IEEE membership being elected to the Fellow grade each year. Election to Fellow is based upon votes cast by existing Fellows in IEEE.

13. I have authored or co-authored several books, including VLSI Digital Signal Processors (IEEE Press 1995) and the Digital Signal Processing Handbook (CRC Press, 1998). I am also Editor of the three-volume DSP Handbook set: Volume 1: Digital Signal Processing Fundamentals, Volume 2: Video, Speech, and Audio Signal Processing and Associated Standards, and Volume 3: Wireless, Networking, Radar, Sensory Array Processing, and Nonlinear Signal Processing,

published in 2010 by CRC Press, Boca Raton, Florida. I have also authored papers on control circuits related to control of electrical motors and generators.

14. I have designed several specialized computer and communication systems over the past two decades at Georgia Tech for tasks such as wireless audio and video processing and protocol processing for portable platforms, such as cell phones and PDAs. I have worked on designing systems that are efficient from performance, size, weight, area, and thermal considerations. I have developed courses and classes for the industry on these topics, and many of my lectures in advanced computer system design, developed under the sponsorship of the United States Department of Defense in the late 1990s, are available for educational use at "<http://www.eda.org/rassp>" and have been used by several U.S. and international universities as part of their course work. Some of my recent publications in the area of design of wireless communications systems and associated protocols are listed in Appendix A, my CV.

15. I am knowledgeable and familiar with standards related to the automotive, avionics, wireless and telecommunications systems industries, and as shown in Appendix A, some of my papers describe the application of these standards in optimizing the design and testing of these systems. I am also knowledgeable and familiar with microprocessor architecture and associated

software and firmware design for embedded, wireless and telecommunications terminals and base stations.

16. I have authored, co-authored, or edited several books in the area of computer systems and distributed systems in the past twenty years, including:

- *VLSI Digital Signal Processors*, Madisetti, V.K.
- *Quick-Turnaround ASIC Design in VHDL*, Romdhane, M., Madisetti, V.K., Hines, J.
- *The Digital Signal Processing Handbook (First Edition)*, Madisetti, V. K., Williams, D. (Editors).
- *VHDL: Electronics Systems Design Methodologies*, Madisetti, V. K. (Editor).
- *Platform-Centric Approach to System-on-Chip (SoC) Design*, Madisetti, V. K., Arpnikanondt, A.
- *The Digital Signal Processing Handbook – Second Edition*, Madisetti, V. K. (2009/2010).
- *Cloud Computing: A Hands-On Approach*, A Bahga, V. Madisetti (2013).
- *Internet of Things: A Hands-On Approach*, A Bahga, V. Madisetti (2014).

17. In the past decade I have also authored several peer-reviewed papers in the area of computers, computer software applications, and software design, and these include:

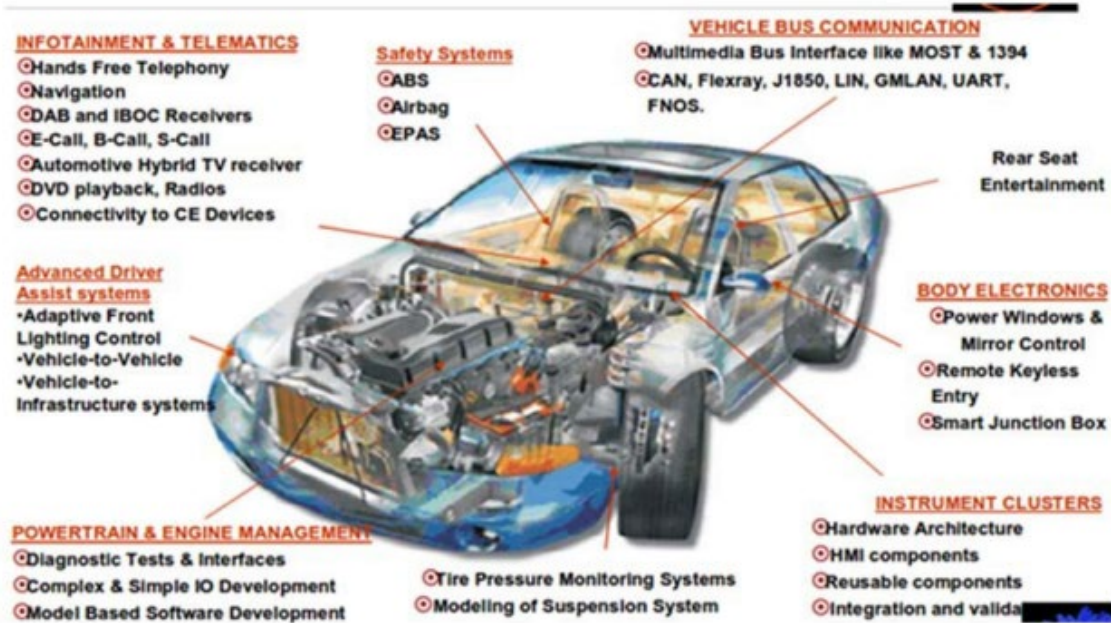
- Madiseti, et al: “*The Georgia tech Digital Signal Multiprocessor, IEEE Transactions on Signal Processing,*” Vol. 41, No. 7, July 1993.
- Madiseti et al, “*Rapid Prototyping on the Georgia Tech Digital Signal Multiprocessor,*” IEEE Transactions on Signal Processing, Vol. 42, March 1994.
- Madiseti, “*Reengineering legacy embedded systems,*” IEEE Design & Test of Computers,” Vol. 16, Vol. 2, 1999.
- V. Madiseti et al, “*Virtual Prototyping of Embedded Microcontroller based DSP Systems,*” IEEE Micro, Vol. 15, Issue 5, 1995.
- V. Madiseti, et al, “*Incorporating Cost Modeling in Embedded-System Design,*” IEEE Design & Test of Computers, Vol. 14, Issue 3, 1997.
- V. Madiseti, et al, “*Conceptual Prototyping of Scalable Embedded DSP Systems,*” IEEE Design & Test of Computers, Vol. 13, Issue 3, 1996.

- V. Madiseti, “*Electronic System, Platform & Package Codesign,*” IEEE Design & Test of Computers, Vol. 23, Issue 3, June 2006.
- V. Madiseti, et al, “*A Dynamic Resource Management and Scheduling Environment for Embedded Multimedia and Communications Platforms,*” IEEE Embedded Systems Letters, Vol. 3, Issue 1, 2011.

18. Some of my recent work in the automotive area includes predicting travel times of cars on freeways for use in mass transportation, and analysis of travel and logistical data in real-time intelligent transportation networks. Representative publications include “Configuration for Predicting Travel-Time Using Wavelet Packets and Support Vector Regression,” Journal of Transportation Technologies, Vol. 3, Issue 3, 2013, and “Cloud-Based Information Technology Framework for Data-Driven Intelligent Transportation Systems,” Journal of Transportation Page 10 of 133 Inter Partes Review of U.S. Patent No. 10,248,477 11 Technologies, Vol. 3, No 2, April 2013. I am also a member of SAE (Society of Automotive Engineers).

19. In the late 2000s, I collaborated with a leading automotive supplier to design and development embedded software and electronic control unit (“ECU”) controller modules in the area of energy profiling for hybrid/gas cars (described in

U.S. Provisional Patent App. No. 61/209,403). The system we developed is described in more detail in the figures below:



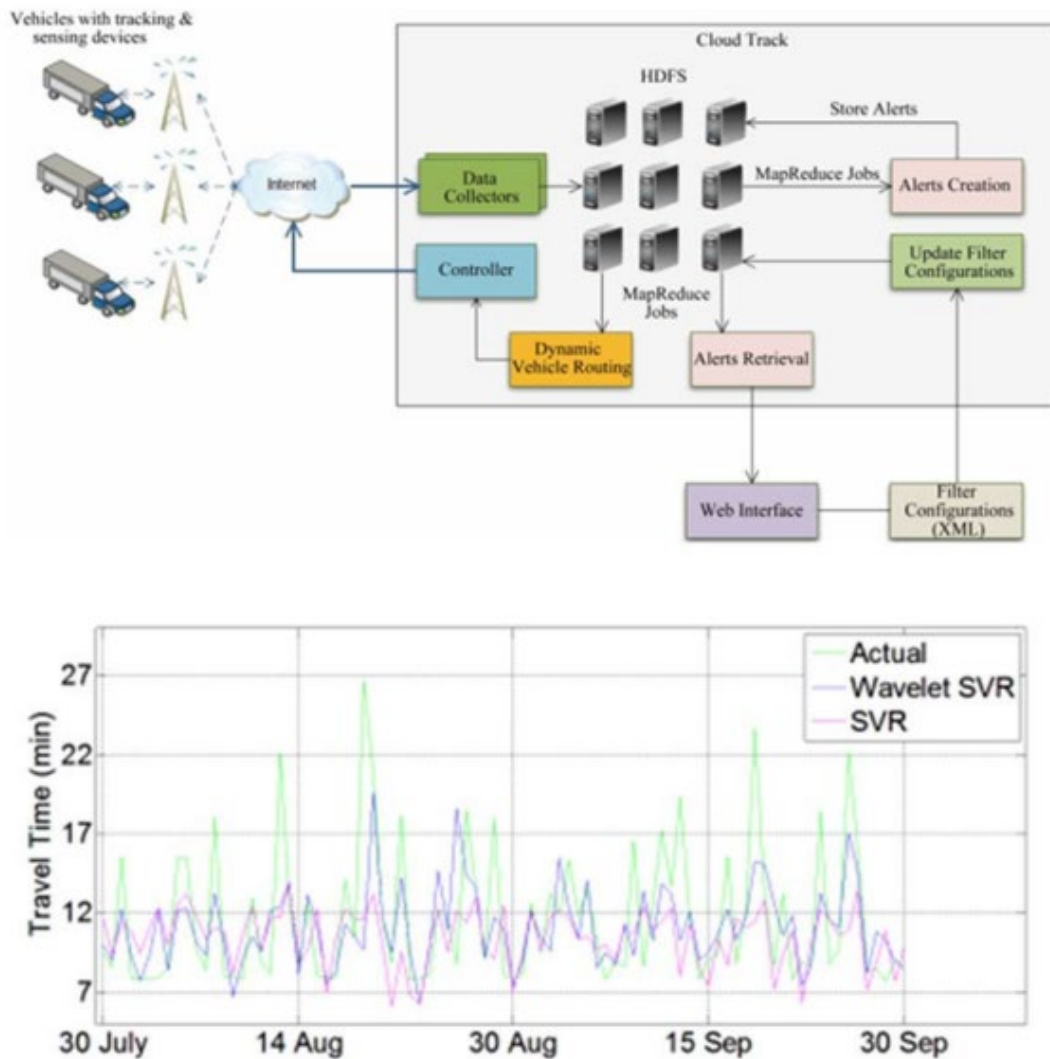


Figure 9. Comparison of actual travel time, and predicted travel-time by Support Vector Regression and Wavelet decomposed Support Vector Regression methods.

20. I have designed and implemented multiple processor computing systems that perform multimedia tasks (e.g., speech and audio recognition) and also avionics/embedded guidance systems since the mid-1990s, and I have also implemented real-time operating systems in the same time frame. Representative

publications of my work in these areas include, The Georgia Tech Digital Signal Multiprocessor (DSMP), IEEE Transactions on Signal Processing, Vol. 41, Issue 7, 1993, and “Task Scheduling on the Georgia Tech Digital Signal Multiprocessor”, Proc. IEEE ICASSP 1992. More recent work that is related to multimedia processing on multiprocessor systems can be found in “A Dynamic Resource Management and Scheduling Environment for Embedded Multimedia and Communications Platforms,” IEEE Embedded Systems Letters, Vol. 3, Issue 1, 2011. Three generations of Digital Signal Multiprocessors (DSMP’s) (listed in the table below) were designed at Georgia Tech as part of my research and education efforts.

IEEE TRANSACTIONS ON SIGNAL PROCESSING, VOL. 41, NO. 7, JULY 1993

TABLE II
FEATURES OF THREE GENERATIONS OF DSMP’S

Generation	Name	Processor/Word-length /MFLOPS	Number of Processors	Topology
DSMP-I	OSCAR I	Am29325/32/4	16	2-D grid/torus
DSMP-II	OSCAR-32	WE-DSP32/32/8	2-16	chorded ring
DSMP-III	DSMP-III	TMS320C40/32/40	16-128	3-D grid/torus



Fig. 10. Six-processor DSMP-II.

21. In collaboration with the US Air Force, Lockheed Martin, and Hughes Corporation, I designed and implemented a 192-processor multiprocessor system for processing real-time avionics data (infrared search and track applications –IRST), and this represented one of the largest multiprocessor systems used in the mid-1990s timeframe on aircraft. See my publications, “Virtual Prototyping of Embedded Microcontroller-Based DSP Systems,” IEEE Micro, 1995, and also “*VHDL TokenBased Performance Modeling for 2D and 3D Infrared Search and Track*”, *Proc. SPIE VIUF*, 1998.

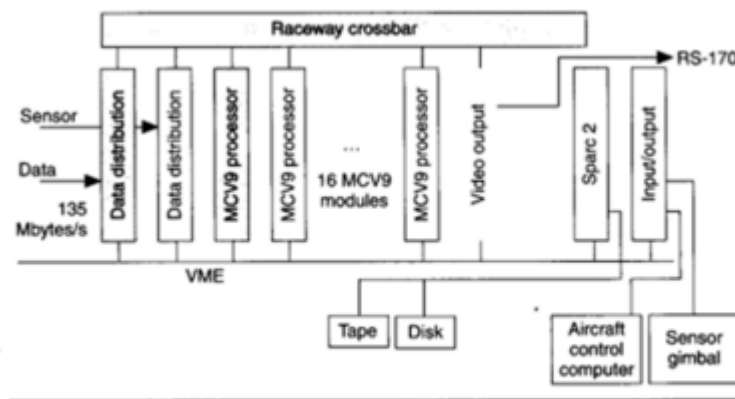


Figure 8. Block diagram of IRST signal processor representing MCV9 boards, data/video distribution, and Sparc cards.^{3,11} Shaded components indicate the virtual prototype.

22. I have been active in the area of wireless OFDM-MIMO communications systems for several years, and some of my publications in this area include “Frequency Dependent Space-Interleaving of MIMO OFDM Systems” Proc. IEEE Radio and Wireless Conference (RAWCON '03), 2003,

“Embedded Alamouti Page 14 of 133 Inter Partes Review of U.S. Patent No. 10,248,477 15 Space Time Codes for High Rate and Low Decoding Complexity”, Proc. Of IEEE Asilomar Conf. on Signals, Systems and Computers, 2008; and “Asymmetric Golden Codes for Fast Decoding in Time Varying Channels”, Wireless Personal Communications (2011).

23. Additional representative peer-reviewed publications in this area of wireless embedded systems are the following: (i) Turkboylari, M. and Madisetti, V.K., “*Effect of Handoff Delay on System Performance of TDMA Cellular Systems*,” 4th International Workshop, Mobile & Wireless Communication Network, pp. 411- 415, 2002; (ii) Jatunov, L. and Madisetti, V.K., “*Computationally-Efficient SNR Estimation for Bandlimited Wideband CDMA Systems*,” IEEE Transactions on Wireless Communications, Issue 12, pp. 3480-3491, December 2006, and (iii) N. Radia, Y. Zhang, M. Tatipamula, V. Madisetti, “*Next Generation Applications on Cellular Networks: Trends, Challenges, and Solutions*,” Proceedings on IEEE, vol. 100, Issue 4, pp. 841-854, April 2012. I have significant experience analyzing, designing, and testing systems based on 3GPP Technical Specifications, including specifications describing WCDMA and HSDPA technologies.

24. A copy of my curriculum vitae is attached hereto as Appendix A.

25. Overall, I have used my education, industry, teaching, writing, and membership and service experiences in the computer vision field, and my understanding of the knowledge, creativity, and experience of a person having ordinary skill in the art in forming the opinions expressed in this report, as well as any other materials discussed herein. My extensive experience with embedded computing systems, wireless communications, and digital signal processing is applicable to analyzing the '179 patent.

26. I am being compensated for services provided in this matter at my usual and customary rate of \$500.00 per hour plus travel expenses. My compensation is not conditioned on the conclusions I reach as a result of my analysis or on the outcome of this matter, and in no way affects the substance of my statements in this declaration. I have no financial interest in Petitioners, or any of their subsidiaries. I also have no financial interest in Patent Owner, Stragent, LLC. I do not have any financial interest in the '179 patent and have not had any contact with the named inventors of the '179 patent.

27. Except as otherwise stated, I have personal knowledge of the facts stated in this declaration, and I have formed the opinions expressed in this declaration based on my expertise, experience, and information that I have reviewed.

IV. MATERIALS REVIEWED

28. In forming my opinions, I read and considered the '179 patent and its prosecution history, as well as the other materials, exhibits, papers, and previous Board decisions regarding the previous '477 IPR (in which I also submitted declarations) referenced and discussed herein and shown in the below table. I have also used my education, industry, teaching, mentoring, writing, and membership and service experiences in the Electrical and Computer Science Engineering fields, and my understanding of the knowledge, creativity, and experience of a person having ordinary skill in the art in forming the opinions expressed in this report, as well as any other materials discussed herein. I have been asked to assume that each of prior art references identified in the analysis section of my declaration qualifies as prior art to the challenged claims of the '179 patent.

Exhibit	Description
Ex-1001	U.S. Patent No. 11,354,179 to Axel Fuchs, <i>et al.</i> (“the '179 patent”).
Ex-1002	Prosecution History of the '179 patent.
Ex-1004	U.S. Provisional Patent Application No. 60/434,018.
Ex-1005	U.S. Patent Application Publication No. 2003/0223436 A1 to Lohrmann, <i>et al.</i> (“Lohrmann”).
Ex-1006	U.S. Patent No. 6,625,169 to Tofano (“Tofano”).
Ex-1007	U.S. Patent No. 5,202,887 to Ueno, <i>et al.</i> (“Ueno”).

Ex-1008	U.S. Patent Application Publication No. 2002/0073243 A1 to Dieter E. Staiger (“ <i>Staiger</i> ”).
Ex-1009	U.S. Patent No. 6,141,710 to Frederick O. Miesterfeld (“ <i>Miesterfeld</i> ”).
Ex-1010	Stewart, <i>et al.</i> , “ <i>Integration of Real-Time Software Modules for Reconfigurable Sensor-Based Control Systems</i> ,” IEEE/RSJ International Conference on Intelligent Robots and Systems, Raleigh, North Carolina (July 1992) (“ <i>Stewart</i> ”).
Ex-1011	H-C. von der Wense, <i>et al.</i> , “Building Automotive LIN Applications,” <i>Advanced Microsystems for Automotive Applications</i> , 280-292 (2001) (“ <i>Wense</i> ”).
Ex-1012	U.S. Patent No. 6,434,459 to William S. Wong, <i>et al.</i> (“ <i>Wong</i> ”).
Ex-1013	U.S. Patent No. 6,954,463 to Ma (“ <i>Ma</i> ”).
Ex-1014	Nick Grattan and Marshall Brian, “ <i>Windows CE 3.0 Application Programming</i> ,” (Prentice Hall PTR) (First Ed., 2000).
Ex-1015	The Ohio State University Libraries MARC Record for H-C. von der Wense, <i>et al.</i> , “ <i>Building Automotive LIN Applications</i> ,” <i>Advanced Microsystems for Automotive Applications</i> , 280-292 (2001).
Ex-1016	IPR2017-00457, Paper 34 (Final Written Decision) (P.T.A.B. June 13, 2018).
Ex-1017	IPR2017-00458 Paper 31 (Final Written Decision) (P.T.A.B. June 13, 2018).
Ex-1018	IPR2017-01502, Paper 24 (Final Written Decision) (P.T.A.B. Dec. 6, 2018).
Ex-1019	International Organization for Standardization 11898-1 (1st. Ed., Dec. 1, 2003).
Ex-1020	U.S. Patent Application Publication No. 2003/0043739 A1 to Juergen Reinold, <i>et al.</i>

Ex-1021	U.S. Patent No. 6,934,612 to Remboski, <i>et al.</i>
Ex-1022	U.S. Patent No. 7,480,312 to Ossman.
Ex-1023	IPR2021-00417, Paper 29 (Final Written Decision) (P.T.A.B. July 12, 2022).
Ex-1024	MARC Record for Stewart, <i>et al.</i> , “Integration of Real-Time Software Modules for Reconfigurable Sensor-Based Control Systems,” IEEE/RSJ International Conference on Intelligent Robots and Systems, Raleigh, North Carolina (July 1992).
Ex-1025	IPR2021-00417, Paper 13 (Patent Owner’s Response) (P.T.A.B. October 12, 2021).
Ex-1026	IPR2021-00417, Paper 19 (Patent Owner’s Sur-Reply) (P.T.A.B. February 28, 2022).
Ex-1027	IPR2017-00676, Paper 11 (Patent Owner’s Response) (P.T.A.B. September 21, 2017).
Ex-1028	IPR2017-01502, Paper 10 (Patent Owner’s Response) (P.T.A.B. March 12, 2018).
Ex-1029	The Foundation Fieldbus Primer, Fieldbus, Inc. (Rev. 1.1, Jun. 24, 2001).
Ex-1030	Ralf Hadelar and Hans-Jörg Mathony, “ <i>Design of Intelligent Body Networks</i> ,” (SAE International) (2000).
Ex-1031	Chuck Powers and Randy Frank, “ <i>The Consumerization of the Automotive Environment: The ITS Data Bus</i> ,” (SAE International) (1997).
Ex-1032	Bruce D. Emaus, “ <i>Current Vehicle Network Architecture Trends – 2000</i> ,” (SAE International) (2000).

V. LEGAL STANDARDS

29. It is my understanding that there are two ways that prior art references can render a patent claim unpatentable: anticipation and obviousness based on 35 U.S.C. §§ 102 and 103, respectively. I understand that the petitioner has the burden in an IPR to show unpatentability by a preponderance of the evidence.

A. Obviousness

30. I understand that the claims define the invention. I also understand that an unpatentability analysis is a two-step process. First, the claims of the patent are construed to determine their meaning and scope. Second, after the claims are construed, the content of the prior art is compared to the construed claims. I understand that a claimed invention may be patentable when it is new or nonobvious in light of the “prior art.”

31. It is my understanding that a claimed invention is patentable if the differences between the invention and the prior art are such that the subject matter as a whole would not have been obvious to a person having ordinary skill in the art to which the subject matter pertains at the time the invention was made.

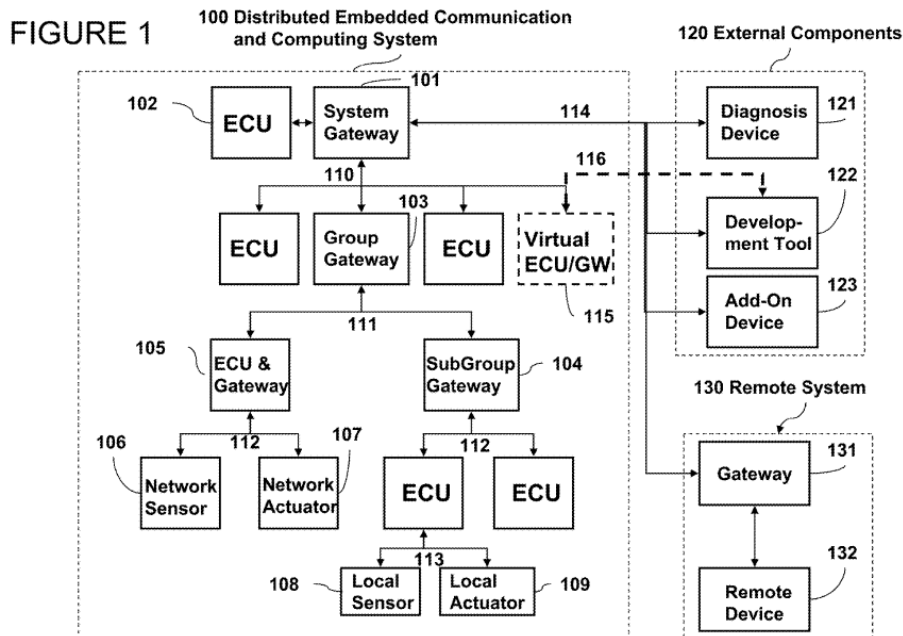
32. I have also been advised that several factual inquiries underlie a determination of obviousness. These inquiries include (1) the scope and content of the prior art, (2) the level of ordinary skill in the field of the invention, and (3) the differences between the claimed invention and the prior art.

33. I understand that where the prior art fails to disclose a claim element or fails to provide an apparent reason to modify existing prior art in a manner to meet a missing claim limitation, the claimed invention likely is not obvious. In other words, even if one of ordinary skill in the art would be motivated to combine two references, a claim is likely not obvious if the combination does not produce the claimed invention.

34. I also understand that the existence of each and every element of the claimed invention in the prior art does not necessarily prove obviousness and that most, if not all, inventions rely on building blocks of prior art.

VI. NATURE OF THE INVENTION CLAIMED IN THE '179 PATENT

35. The '179 patent describes systems and methods “for sharing information in a distributed framework.” Ex-1001, (54), 1:40-42. In automobiles, electronic control units (“ECUs”) control applications such as engine, the, brakes, or diagnostics through connections to sensors and actuators organized into separate subnetworks. *Id.*, 4:65-5:3. FIG. 1 shows gateways 101, 103, 104, 105, which relay messages through system layers. *Id.*, 5:12-14. Each layer may contain multiple ECUs connected through wired serial multiplexing bus systems. *Id.*

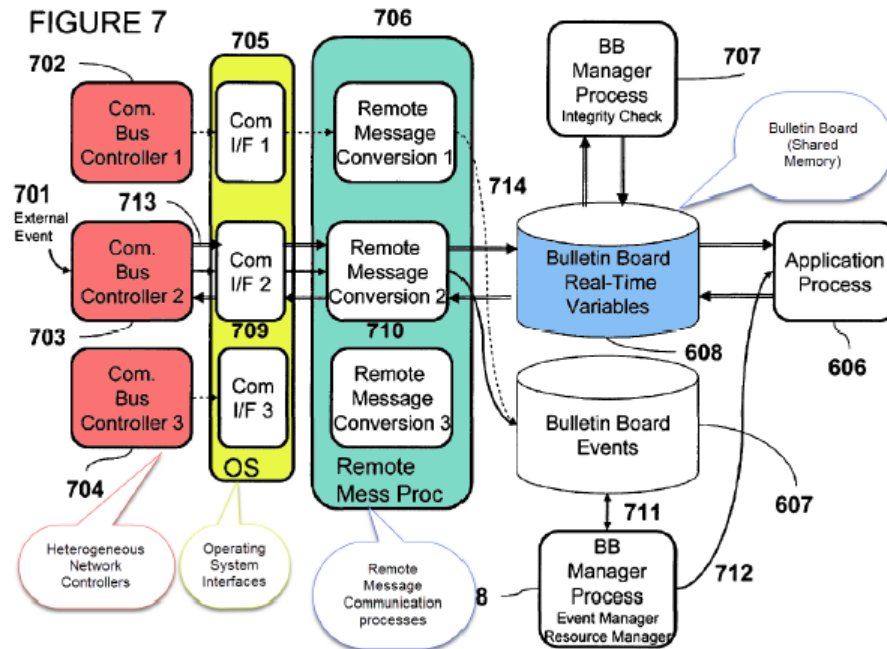


Ex-1001, FIG. 1

36. At the highest level, “the system level,” system gateway 101 connects buses to other system-level ECUs, subsequent gateways 103, and external components 120. *Id.*, 5:47-56. ECU 102 receives real-time input variables from networked sensors 106 via multiplexing bus system 112, processes the input and generates output variables that may be shared with other ECUs. *Id.*, 5:27-33.

37. Annotated FIG. 7 shows a bulletin board 608 (blue), which acts as a shared memory for sharing variables. *Id.*, 8:18-23. The bulletin board interacts with multiple communication buses 701-703 (red) and associated operating system interfaces 705 (yellow). *Id.*, 4:33-36. Data received from one communication bus is stored on the bulletin board and shared as a new message with other network types

via remote message communication processes 706 (green) that add/extract network-specific information. *Id.*



Id., FIG. 7 (annotated)

VII. LEVEL OF ORDINARY SKILL IN THE ART

38. I understand a person of ordinary skill in the art (“POSITA”) is determined by looking at (A) type of problems encountered in the art, (B) prior art solutions to those problems, (C) rapidity with which innovations are made, (D) sophistication of the technology, and (E) educational level of active workers in the field. Based on my experience in this art and accounting for these factors, I believe a person of ordinary skill in the art would have had, as of the relevant date of the ’179 patent, at least a bachelor’s degree in electrical, computer, or a related

engineering discipline; two years of industry experience in the field of distributed computing or automotive engineering, or equivalent experience; and knowledge or familiarity with in-vehicle computing.

39. Based on my education, training, and professional experience in the field of the claimed invention, I am familiar with the level and abilities of a person of ordinary skill in the art at the time of the claimed invention. I have technically supervised or worked with such individuals at the relevant time and I, myself, also met at least these minimum qualifications at the relevant time. I meet these qualifications today, as well.

VIII. CLAIM CONSTRUCTION

40. I have been informed that the first step in an invalidity analysis involves construing the claims, as necessary, to determine their scope. And, second, the construed claim language is then compared to the disclosure of the prior art. In proceedings before the USPTO, I have been told by counsel that a claim in a patent subject to inter partes review should be given their ordinary and customary meaning to a person of ordinary skill in the art at the time of the invention.

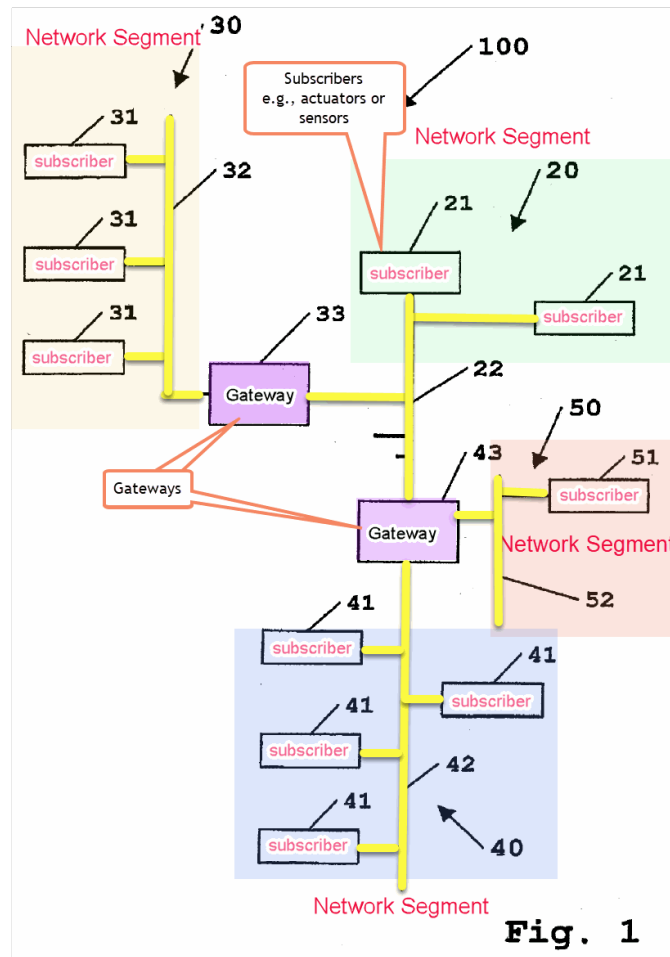
41. In my opinion, the plain and ordinary meaning of the claims applies to each claim term of the '179 patent.

IX. SUMMARY OF THE PRIOR ART

42. My opinions below relate to the patentability or unpatentability of claims 1-27 of the '179 patent based on a combination of prior art.

A. Lohrmann

43. *Lohrmann* discloses a system for managing communications networks in automobiles, and particularly a network with a plurality of network segments that are physically connected via gateways. *Lohrmann*, 2, 19. Control units or control unit applications, such as actuators or sensors, are physically connected to one another by respective data buses (CAN, FlexRay, or LIN) and communicate data over the network. *Id.*, 18, 20,21.



Lohrmann, FIG. 1 (annotated)

B. Tofano

44. *Tofano* discloses an integrated communication system that “enable[s] data and information exchanges between various networks and various network formats” and “transparently interconnects different networks,” which includes a processor for translating or converting incoming data from a first network format to another network format. *Tofano*, 2:56-62, 15:47-51. *Tofano*’s processor is

operably connected to components of the system, and “can be provided with a suitable software program to execute, thereby enabling the processor to accomplish any required functions for the communication system.” *Id.*, 15:56-61. “[E]ach processor ... may have the necessary memory, disk, non-volatile storage, I/O, networking and communications peripherals, and other support necessary for it to accomplish the required functions.” *Id.*, 3:18-20, 29-32. Thus, *Tofano* also teaches a gateway, having memory storage comprising instructions.

C. Ueno

45. *Ueno* “relates to a direct access storage device (DASD) shared by a plurality of central processing units.” *Ueno*, 1:8-10, 2:57-63. *Ueno* discloses methods for accessing the DASD.

D. Staiger

46. *Staiger* discloses an ECU connected to a plurality of real-time networks, including “several individual CAN [] busses or other multiple purpose networks.” *Id.*, ¶ 3. *Staiger*’s ECU executes an application for controlling remote automobile systems while concurrently performing gateway functions between the different networks. *Id.*, ¶¶ 4-5. *Staiger* explains that the CAN, FireWire, and MOST buses are “real-time” buses, capable of “respond[ing] to stimuli within some small upper limit of response time, typically [in] milliseconds or microseconds,” such that, upon receiving a message, an intercommunication

preprocessor “processes the message and initiates immediate distribution” of an “output[] message,” to, *e.g.*, a “destination unit.” *Id.*, ¶¶ 7, 35, 51, claim 1, Abstract.

E. Miesterfeld

47. *Miesterfeld* discloses a data exchange system including a controller for “process[ing] vehicle data to control at least one vehicle related function.” *Miesterfeld*, 2:23-27. The controller may be implemented on a vehicle 12 having a vehicle data bus (VDB) 14, an intelligent transportation system (ITS) data bus 28, and corresponding devices, 16, 18, 20, and 22, which “write data to or read data from” their respective data buses. *Id.*, 3:1-16. In operation, the controller (“gateway 10”) facilitates data exchange between the VDB and ITS data bus via shared memory 30. *Id.*, 2:36-39, 3:18-20. To “effect such an exchange,” the system includes VDB and ITS data bus interfaces which “read[] and write data from” both the data buses and shared memory 30. *Id.*, 20-25. Annotated FIG. 1. illustrates *Miesterfeld*’s data exchange system on vehicle 12.

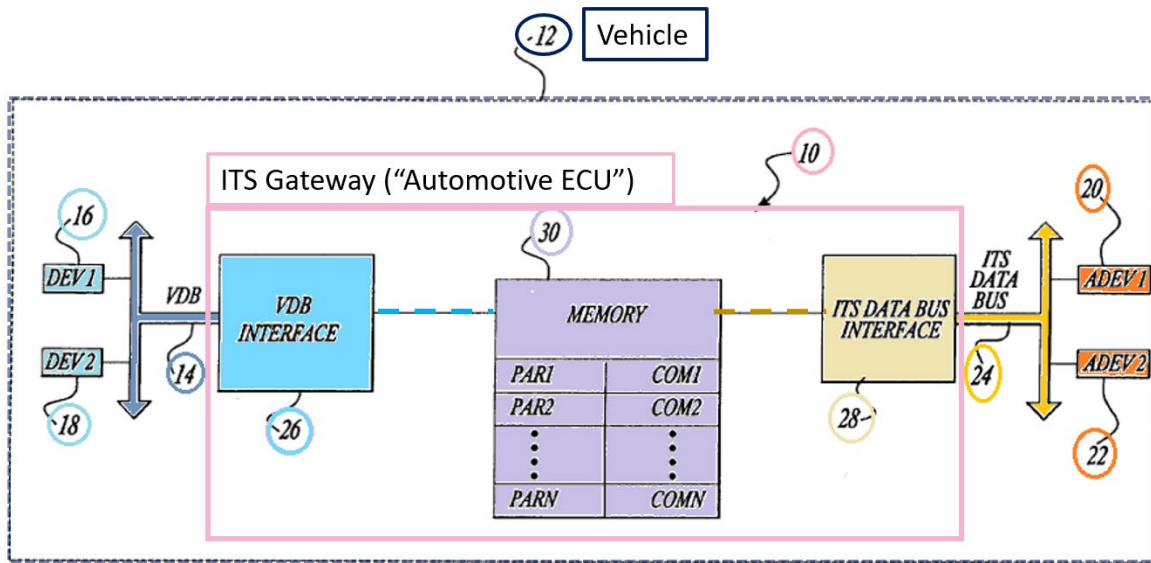
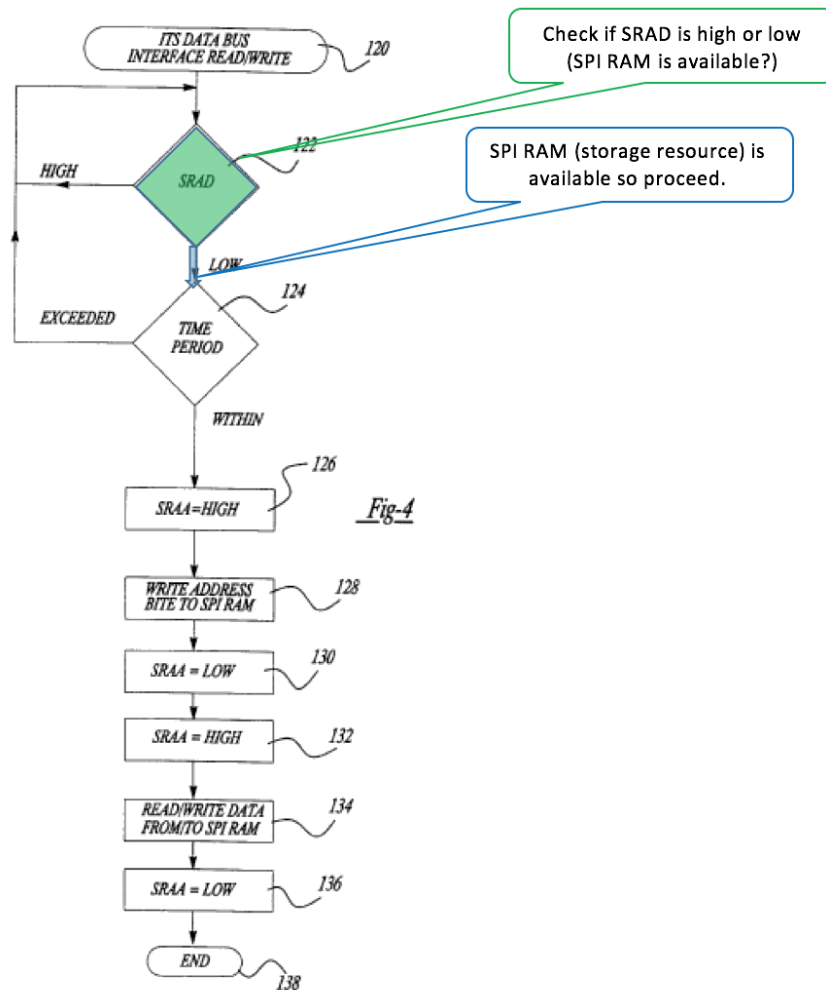


Fig-1

Miesterfeld, FIG. 1 (annotated)

Miesterfeld further discloses a process for reading and writing (storing) data received through the vehicle's devices. *Id.* 4:22-26, 5:38-43, 6:33-40, Fig. 4. As illustrated in annotated FIG. 4, the process includes, *inter alia*, determining whether SPI RAM is available and storing data if so. *Id.* The process is iterative—the system repeatedly attempts to determine SPI RAM availability until it either becomes available or too much time has elapsed. *Id.*, 6:40-45 (explaining the handshake arbitrating access to the SPI RAM (SRAA) “must” be set to “high” within 5 μ s of determining that the SRAD signal line is low.).



Miesterfeld, FIG. 4 (annotated)

F. Wong

48. *Wong* teaches vehicle information system 20 including master control unit (MCU) 24 and one or more secondary control units (SCU) 26(1) and 26(2) connected to automobile components and systems 32, 34, 36. *Wong*, (54), 1:52-60, 2:32-373:25-4:2, Fig. 1. The MCU and SCUs include “processor 100” running a “real-time, multitasking operating system that is capable of supporting “plug-and-

play system configuration and providing high stability, security, and efficiency.”

Id., 1:52-60, 2:32-37, 5:64-6:29. *Wong*’s controller can execute instructions for controlling data flow management (*id.*, 6:40-42) and permits communication among automobile devices, including sensors. *Id.*, 7:51-58.

G. Stewart

49. *Stewart* teaches a framework for integrating real-time software control modules for real-time sensor-based systems. *Stewart*, 1, 6, 7. To “guarantee that tasks will get the data they require on time, every time,” *Stewart* teaches implementing a “bounding wait time” (threshold) in a multiprocessor synchronization method. *Id.*, 11. *Stewart* also teaches implementing a “time-out mechanism” (threshold) for preventing data transfer when a “pre-specified time or number of retries” elapses and that “error handlers should be installed to detect tasks that suffer successive time-out errors.” *Id.*

H. Wense

50. *Wense* teaches that cars utilize “[s]everal multiplex protocols,” including CAN (*e.g.*, for engine and body control networks), FlexRay (*e.g.*, for safety, braking, and steering systems), and LIN (*e.g.*, for cost-critical distributed body electronics). *Wense*, 11.

I. Ma

51. *Ma* teaches apparatuses and methods for processing data packets in the data communications field. *Ma*, 1:7-10. *Ma* teaches that data packets include a data field and one or more header fields whereby the packet headers and their functions are “typically” arranged in an orderly fashion according to the open-systems interconnection (OSI) reference model (*id.*, 1:26-31) and explains that the OSI model partitions packet communications functions into layers, each layer having a header stripped or prepended during data processing. *Id.*, 5:48-63.

X. OPINIONS

52. My opinions below relate to the obviousness of claims 1-27 of the '179 patent based on the following grounds:

Ground	Claim(s) Challenged	35 USC §	References
1	1 and 8	103	<i>Lohrmann</i> , and <i>Ueno</i>
2	2-7	103	<i>Lohrmann</i> , <i>Ueno</i> , and <i>Staiger</i>
3	9-27	103	<i>Lohrmann</i> , <i>Tofano</i> , <i>Ueno</i> and <i>Staiger</i>

4	1-7	103	<i>Miesterfeld and Stewart</i>
5	8	103	<i>Miesterfeld, Stewart, and Wense</i>
6	9-14, 17-20	103	<i>Miesterfeld, Wong, Stewart, and Wense</i>
7	15, 16	103	<i>Miesterfeld, Wong, Stewart, Wense, and Ma</i>
8	21-24, and 27	103	<i>Miesterfeld, Wong, and Stewart</i>
9	25 and 26	103	<i>Miesterfeld, Wong, Stewart, and Wense</i>

A. LOHRMANN GROUNDS

53. The *Lohrmann* grounds establish that *Lohrmann* discloses or suggests each of the claimed features but arguably lacks express disclosure of, (1) accessing a storage and related steps (all Grounds), (2) sharing sensor information in less than a second (Grounds 2-3), and (3) a memory, instructions, and processor (Ground 3). *Ueno*, *Staiger*, and *Tofano* are relied upon to teach each of these

respective features. Ground 3 also relies on *Tofano* to explain the hierarchal layers (e.g., data link and network layers) of the data packets being transmitted and corresponding data processing steps (e.g., removing header bits).

1. Ground 1: Claims 1 and 8 are obvious over *Lohrmann* in view of *Ueno*.

Claim 1[preamble]: “A method, comprising:”

54. *Lohrmann* discloses “a system for managing networks in a transportation unit” and corresponding method *Lohrmann*, Abstract, 2.

1[a]: “at an automotive electronic control unit: receiving sensor information associated with a message;”

55. *Lohrmann*’s system includes “control units” (also called “subscribers”) for controlling automotive sensors or actuators. *Lohrmann*, ¶ 21. *Lohrmann* discloses that a “gateway” is a type of control unit, and that the gateway controls data exchange between other “control unit or control unit applications, such as sensors and actuators,” by “passing on messages from one network segment to a further network segment.” *Lohrmann*, ¶ 4,19, 21. Thus, *Lohrmann* discloses an automotive ECU (gateway) receiving sensor information, associated with a message.

1[b] “based on receiving the sensor information, issuing, to a storage included in the automotive electronic control unit, a request to access the storage included in the automotive electronic control unit to store the sensor information and, based on issuing

the request, determining whether the storage is available to store the sensor information”

56. *Lohrmann* in combination with *Ueno* teaches this limitation.

57. *Ueno* teaches a system and method for accessing a storage device.

Ueno, 1:8-10, 2:57-63 (“The present invention relates to a direct access storage device (hereinafter referred to as DASD) shared by a plurality of central processing units.”). The central processing units (CPUs) correspond to the claimed processor and the DASD corresponds to the claimed “storage.” *Ueno*, 1:8-9, 4:50-53, Fig. 1. The CPU reads and writes data sets (i.e., information) to and from the DASD using a program. *Id.*, 4:65-5:2.

58. *Ueno* further teaches that before the CPU writes data to the DASD (i.e., stores information in the storage), it searches the DASD for “control information.” *Id.*, 5:27-31. The control information determines whether the CPU may access the DASD (*id.*, 3:47-51, 4:57-64); thus, it is my opinion that a POSITA would have understood that searching the DASD for control information before writing the data to the DASD is a “storage request to access the storage,” for the purposes of storing information (i.e., writing data) to the storage.

59. *Ueno* also teaches that “reserve flags, the reserve CPU numbers and the blockage flags of the two searched control information sets are checked” after the CPU searches for the control information *Ueno*, 5:33-35. The flags and reserve

CPU numbers each indicate whether the DASD is capable of receiving/storing the data to be written (*id.*, 4:57-64, 5:33-43); thus, in my opinion a POSITA would have also understood that “checking” for flags and a CPU number constitutes determining whether the storage (i.e., the DASD) is available to store the information (i.e., data) based on issuing the storage request (i.e., the search).

60. *Ueno*, like *Lohrmann*, relates to the same technical field: communication networks. It is my opinion that a POSITA would have reasonably expected that modifying the combined system of *Lohrmann* and *Tofano* to include a storage resource and corresponding processes would succeed, and that the modification would have required only ordinary skill. For example, *Lohrmann* discloses in ¶¶ 23-33, as part of the gateway’s network system management functionality, that the gateway must store information about the state of the network, including operating modes, bus states, network segment states, and configuration states to ensure stable operation of the network. Further, *Lohrmann* explains that network segments can be selectively and synchronously turned off and on. *Id.*, ¶¶ 11-14. A POSITA would have understood storage the storage and associated processes of *Ueno* would have improved upon *Lohrmann* by ensuring real time and reliable operation.

61. *Ueno*’s search and check method helps to minimize computer system overhead (*Ueno*, 2:61-64) and helps to ensure accessibility to shared database

storage systems. *Id.* 2:51-56, 6:56-61. Thus, it is my opinion that a POSITA would have been motivated to implement *Ueno*'s search and check method for accessing a storage into *Lohrmann*'s system, to minimize computer system overhead and help ensure data accessibility to in the shared database storage system. As combined, the automotive ECU (as taught by *Lohrmann*) determines whether the storage is available to store the sensor information based on issuing the storage request (as taught by *Ueno*).

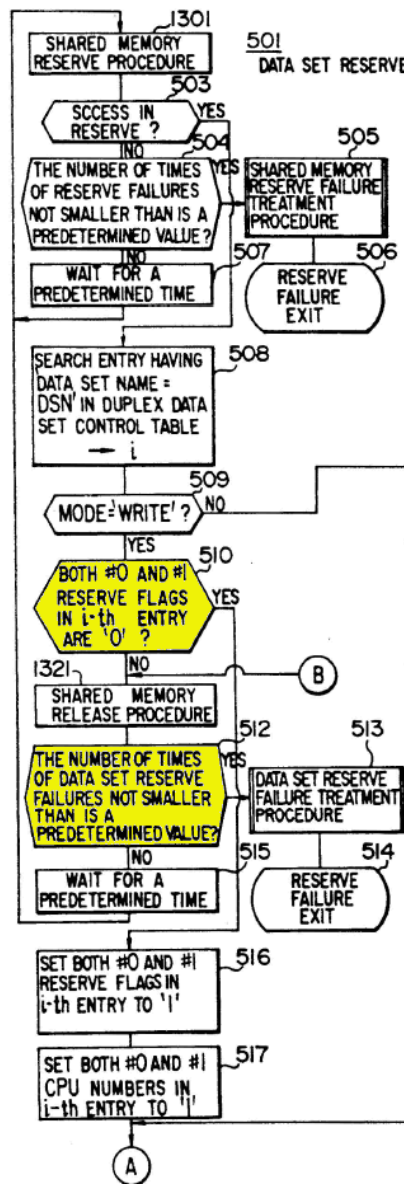
1[c]: “determining whether a value tracked since the issuance of the request has been reached indicating that the storage has not been available in association with the value tracked since the issuance of the request;”

62. As explained for element 1[b] *Lohrmann* as modified by *Ueno* teaches issuing a storage request and determining whether the storage is available (i.e., searching and checking). *Ueno* teaches that the searching and checking includes an iterative process whereby the processor checks for flags (i.e., storage accessibility) after a predetermined number of attempts or time (i.e., a value) elapses. *Ueno*, 11:27-41, Fig. 5.

11:37-42, FIG. 5. Accordingly, it is my opinion that a POSITA would have understood that *Ueno* teaches using a “value” (access attempts or time) to determine whether the storage (DASD) is available to receive/store the data to be written.

1[d]: “based on the storage included in the automotive electronic control unit being determined, based on issuing the request, to not be available and the value tracked since the issuance of the request having not been reached indicating that the storage has not been available in association with the value tracked since the issuance of the request, issuing, to the storage included in the automotive electronic control unit, another request to access the storage included in the automotive electronic control unit to store the sensor information; and”

64. As explained for element 1[c], *Lohrmann* as modified by *Ueno* teaches an iterative process whereby the automotive ECU checks for flags (i.e., storage availability) after a predetermined number of attempts or time (i.e., a value) elapses. *Ueno*, 11:27-41, Fig. 5. *Ueno* further teaches, as part of the iterative process, repeating the search and check cycle (i.e., issuing another request to access storage) “if the number of times in a data set reserving failure is within a predetermined value.” *Id.*, 11: 33-37; Fig. 5.



Ueno, FIG. 5 (annotated)

65. Accordingly, it is my opinion that a POSITA would have understood that *Ueno* teaches repeating the check and search process (issuing another request) when the DASD is determined to be unavailable, and the predetermined value of access attempts or time has not been exceeded. As combined with

Ueno, Lohrmann's gateway (1) checks the reserve flags associated with a DASD to determine its availability to receive data, and (2) if the reserve flags are not both zero, and the number of attempts is within "a predetermined value," researching and rechecking until either the number of retries exceeds a predetermined value or the DASD is determined to be available. *Ueno*, 11:12–42.

1[e]: "based on the storage included in the automotive electronic control unit being determined, based on issuing the request or the another request, to not be available and the value tracked since the issuance of the request having been reached, sending an error notification; and"

66. As explained for 1[c], *Lohrmann* as modified by *Ueno* teaches determining whether the DASD (storage) is unavailable. *Ueno*, 11:37-42, FIG. 5. The resource is unavailable "[i]f at least one of the reserve flags 202-1 and 202-2 is '1' (Step 510)." *Id.*, 11:25-33. *Ueno* further teaches reporting "a failure," e.g., to an operator, if the DASD is determined to be unavailable and the number of reattempts (as explained for claim element 1[d]) exceeds the predetermined value. *Id.*, 10: 19-23; see *also id.* 11:1-6 (reporting other failures to an operator).

1[f]: "based on the storage included in the automotive electronic control unit being determined, based on issuing the request or the another request, to be available, storing the sensor information utilizing the storage."

67. As explained for element 1[b], *Lohrmann* as modified by *Ueno* teaches determining whether the DASD (storage) is available. *Ueno* further teaches

that if both reserve flags are set to 0, “[t]he CPU executes writing the same contents into the data sets on the two DASDs.” *Id.*, 5:42-43.

68. In my opinion, a POSITA would have understood that *Ueno* teaches storing the data to the storage and that the combination of *Lohrmann* and *Ueno* teaches storing sensor information (as disclosed by *Lohrmann*) to a DASD (as taught by *Ueno*) in response to performing (and repeating) the search and check process of *Ueno* (issuing the/another request).

Claim 8: “The method as recited in claim 1, wherein automotive sensor data is transmitted between heterogeneous networks including at least one of a Controller Area Network, a Flexray network, or a Local Interconnect Network.”

69. *Lohrmann* discloses that the data is transmitted using various data bus systems, including CAN, FlexRay and LIN, and that the system “is preferably suitable for operating network segments which are based on different bus systems, since the actual data bus system in the network segment is not significant for managing network segments. *Lohrmann*, ¶¶ 10,20. Thus, *Lohrmann* discloses transmitting between heterogeneous networks. *Id.*

2. Ground 2: Claims 2-7 are obvious over *Lohrmann* in view of *Ueno* and *Staiger*

Claims 2 and 3 “The method as recited in claim 1, wherein the sensor information reaches a destination in less than one second [a millisecond].”

70. *Lohrmann* discloses that the information is exchanged using a control area network (CAN). *Lohrmann*, ¶ 20. In my opinion, a POSITA would have understood that the information is shared (i.e., reaches its destination) in less than one second because CANs are known to facilitate information transmission at speeds of less than one millisecond.

71. To the extent this requires further clarification, *Staiger* teaches an ECU connected to a plurality of real-time networks, e.g., “several individual CAN [] busses or other multiple purpose networks.” *Id.* ¶ 3. The ECU executes an application program for controlling remote systems of automobiles while concurrently performing gateway functions between the different networks. *Id.* ¶¶ 4–5. *Staiger* explains that the CAN, FireWire, and MOST busses are “real-time” busses, capable of “respond[ing] to stimuli within some small upper limit of response time, typically [in] milliseconds or microseconds,” such that, upon receiving a message, an intercommunication preprocessor “processes the message and initiates immediate distribution” of an “output[] message,” to e.g., a “destination unit.” *Id.* ¶¶ 7, 35, 51, claim 1, Abstract (emphasis added).

72. *Staiger*, like *Lohrmann* and *Ueno* relates to network communication, and *Staiger* simply clarifies how fast *Lohrmann*'s gateway can facilitate information sharing. Accordingly, it is my opinion that configuring *Lohrmann*'s gateway such that the sensor information is capable of being shared in less than one second, would have required only ordinary skill and a reasonable expectation of success. In my opinion, it would have been obvious to a POSITA to configure the modified system of *Lohrmann* such that message information sent from a sensor origin on a CAN, LIN, or FlexRay Network reaches its destination in milliseconds or microseconds (i.e., "less than one second" or "less than a millisecond") to facilitate immediate receipt of an incoming message from a sensor origin and distribution of an output message to a destination, such as an actuator. *Staiger*, 7, 35, 51, claim 1, Abstract.

Claims 4 and 5 "The method as recited in claim 1, wherein a duration between the sensor information being received and being transmitted is less than one second [a millisecond]."

73. As explained in claim 2, it is my opinion that a POSITA would have understood that *Lohrmann*'s CAN bus shares the sensor information, such that it is transmitted and received, in less than 1 second (e.g., milliseconds or microseconds).

74. It is also my opinion that it would have been obvious to a POSITA to configure the modified system of *Lohrmann* such that message information sent

from a sensor origin on a CAN, LIN, or FlexRay Network and reaches its destination in milliseconds or microseconds (i.e., “less than one second” or “less than a millisecond”) to facilitate immediate receipt of an incoming message from a sensor origin and distribution of an output message to a destination, such as an actuator. *Staiger*, 7, 35, 51, claim 1, Abstract. Thus, claims 4 and 5 are obvious for the same reason as claims 2 and 3.

Claim 6 “The method as recited in claim 1, wherein the sensor information is transmitted from the automotive electronic control unit in less than a millisecond from a time when the message is received at the automotive electronic control unit.”

75. As discussed above in claim 4, it is my opinion that a POSITA would have understood that the *Lohrmann*’s CAN bus shares the sensor information such that it is transmitted and received, in less than a millisecond (e.g., microseconds).

76. It is also my opinion that it would have been obvious to a POSITA to configure the modified system of *Lohrmann* such that message information sent from a sensor origin on a CAN, LIN, or FlexRay Network and reaches its destination in milliseconds or microseconds (i.e., “less than one second”) to facilitate immediate receipt of an incoming message from a sensor origin and distribution of an output message to a destination, such as an actuator. *Staiger*, 7, 35, 51, claim 1, Abstract. Thus, claim 5 is obvious for the same reason as claim 4.

Claim 7: “The method as recited in claim 6, wherein at least one of: ...the value is time related ...”

77. Claim 7 requires “at least one of” numerous features describing the method of claim 6. Ex. 1001, 14:65-15:42. These features are listed in the alternative. Because “at least one” of these features, e.g., a “time related” value is taught, claim 7 is also obvious over the prior art. For example, as discussed above in claim element 1[c] *Ueno* teaches that the value is time related. *Ueno*, 11:27-41 (“If the number of times in a data set reserving failure is within a predetermined value (Step 512), the data set reserving procedure (Step 1301) is carried out after waiting for about tens of msec (Step 515). If the number of times in data set reserving is over the predetermined value (Step 512), occurrence of abnormality pertaining to the data set reserving is supposed so that the procedure is terminated at a reserving failure exit (Step 514) after a data set reserving failure procedure (513)”) (emphasis added).

3. Ground 3: Claims 9-27 are obvious over *Lohrmann* in view of *Tofano*, *Ueno*, and *Staiger*

Claim 9[pre]: “An apparatus, comprising:”

78. *Lohrmann* discloses “a system for managing communications networks in motor vehicles.” *Lohrmann*, ¶ 2.

Claim 9[a]: “an automotive electronic control unit including a memory storage comprising instructions, and”

79. *Lohrmann* discloses that the system includes “control units” (also called “subscribers”) for controlling automotive sensors or actuators, and therefore discloses an automotive electronic control unit (ECU). *Lohrmann*, ¶ 21. *Lohrmann* also discloses that a gateway, is a type of subscriber (and therefore also an automotive ECU) that exchanges data over a network (*Lohrmann*, ¶¶ 3, 18), but does not expressly disclose that it includes a memory storage comprising instructions. In my opinion, a POSITA would have understood *Lohrmann*’s disclosure of a “gateway” to at least suggest a memory and instructions because memory and instructions are necessary gateway components that facilitate gateway functionality, *e.g.*, network management, data exchange and communication between buses. *Lohrmann* also discloses the use of control unit applications, which would have also suggested to a POSITA that memory and instructions are present.

80. *Tofano* also renders this limitation obvious. *Tofano* teaches an integrated communication system that “enable[s] data and information exchanges between various networks and various network formats” and “transparently interconnects different networks” the system including a processor for translating or converting incoming data from a first network format to another network

format. *Tofano*, 2:56-62, 15:47-51. Thus, *Tofano*, like *Lohrmann*, teaches a gateway.

81. *Tofano* further teaches a processor operably connected to components of the system, wherein the “the processor ... can be provided with a suitable software program to execute, thereby enabling the processor to accomplish any required functions for the communication system” and that “each processor ... may have the necessary memory, disk, non-volatile storage, I/O, networking and communications peripherals, and other support necessary for it to accomplish the required functions.” *Tofano*, 3:18-20, 29-32, 15:56-65. Thus, *Tofano* also teaches a gateway, having memory storage comprising instructions.

82. *Tofano*, like *Lohrmann*, *Ueno*, and *Staiger* relate to the same technical field: communication networks. In my opinion, a POSITA would have had a reasonable expectation of success in modifying *Lohrmann*’s gateway to include a hardware processor for executing instructions to perform the disclosed process, and that the modification would have required only ordinary skill. For example, *Lohrmann* explains that the interface between network segments is implemented in control units which also contain application functions referred to as “gateway,” (*Lohrmann*, ¶ 3) and describes gateway functions including controlling system wide operations of the network including routing messages (*id.* ¶4), as well as management functions such as network interfacing and configuration, monitoring,

detection, and diagnostics. *Id.* ¶5. A POSITA would have understood that an efficient, flexible, and configurable way of implementing these functionalities would have been through software executing on a processor, as taught by *Tofano*. This combination would have been predictable and without risk or undue experimentation, and had a high chance of success. Accordingly, there would have been a high expectation of success utilizing this approach. A POSITA would have also understood that *Tofano*, as illustrated in Fig. 5 and described in 4:13-51, teaches a processor having multiple network interfaces and is capable of information exchange with various networks and network management. *Tofano*, 2:53-68. It is also my opinion that it would have been obvious to a POSITA to incorporate a memory storage including instructions (and the corresponding processor) into the system of *Lohrmann* to facilitate the gateway's required functions.

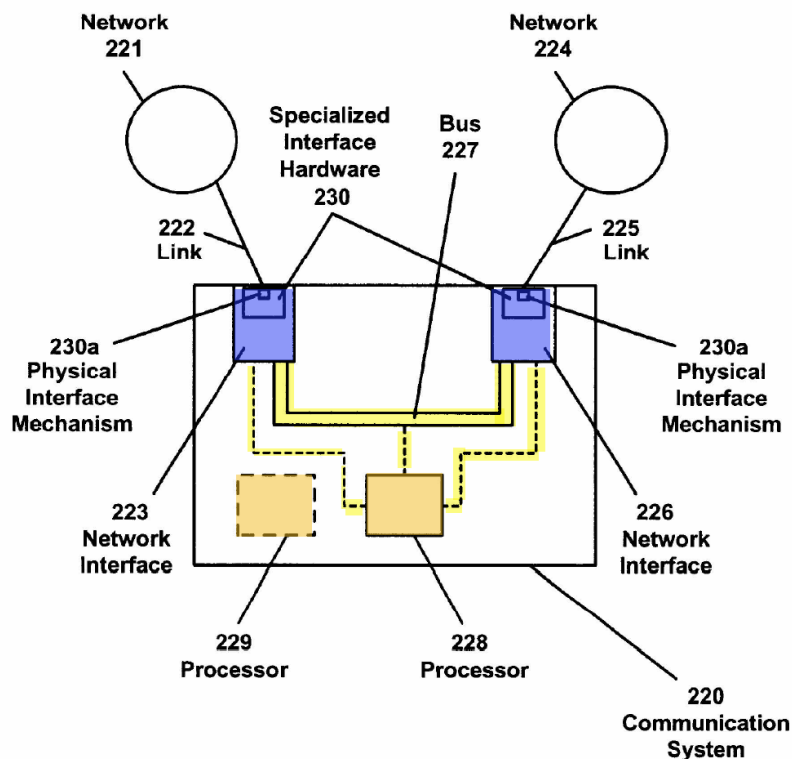
Claim 9[b]: “at least one hardware processor in hardwired communication with the memory storage,”

83. As explained for element 9[a], *Tofano*'s communication system includes a processor 228 and corresponding software for executing and “thereby enabling the processor to accomplish any required functions for the communication system” and that “each processor ... may have the necessary memory, disk, non-volatile storage, I/O, networking and communications peripherals, and other support necessary for it to accomplish the required

functions.” *Id.*, 15:56-65. Thus, *Tofano* teaches a processor in hardwired communication with the memory storage.

Claim 9[c]: “wherein the at least one hardware processor executes the instructions for:”

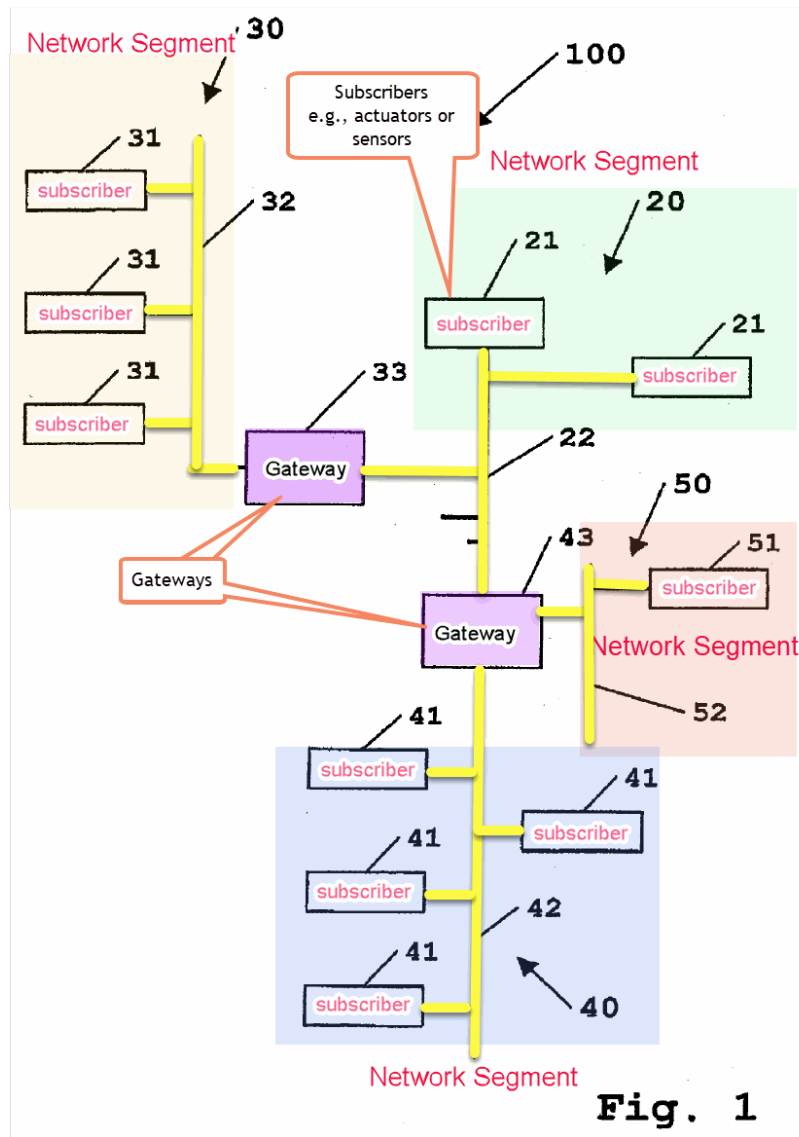
84. As discussed above for element 9[a], *Tofano*’s processor executes the instructions related to message handling. “[T]he processor 228 executes a suitable software program therein for translating between at least one network format, such as between at least one of the first network format and the second network format.” *Tofano*, 13:23-32.



Tofano, FIG. 5 (annotated)

Claim 9[d]: “identifying sensor information associated with a message received utilizing a first network protocol associated with a first network;”

85. *Lohrmann*’s gateway controls data exchange between “control unit or control unit applications, such as sensors and actuators” by “passing on messages” between network segments. *Lohrmann*, ¶ 4, 19, 21. Each network segment includes a corresponding data bus, such as a CAN bus that receives the incoming data and message. *Id.*, 19 (explaining that subscribers (sensors/actuators) are connected to one another within one of the network segments by a corresponding data bus), Fig. 1. Thus, in my opinion, *Lohrmann* as modified by *Tofano* teaches executing instructions for identifying sensor information, associated with a message, received utilizing a first network protocol (CAN protocol) associated with a first network (CAN data bus).



Lohrmann, FIG. 1 (annotated)

Claim 9[e]: “in response to identifying the sensor information, issuing, by the at least one hardware processor and to a storage included in the automotive electronic control unit, a request to access the storage included in the automotive electronic control unit to store the sensor information and, in response to issuing the

request, determining whether the storage is available to store the sensor information;”

86. *Lohrmann* and *Tofano* in combination with *Ueno* teaches this limitation.

87. *Ueno* teaches a system and method for accessing a storage device. *Ueno*, 1:8-10, 2:57-63 (“The present invention relates to a direct access storage device (hereinafter referred to as DASD) shared by a plurality of central processing units.”). The central processing units (CPUs) correspond to the claimed processor and the DASD corresponds to the claimed “storage e.” *Ueno*, 1:8-9, 4:50-53, Fig. 1. The CPU reads and writes data sets (i.e., information) to and from the DASD using a program. *Id.*, 4:65-5:2.

88. *Ueno* further teaches that before the CPU writes data to the DASD (i.e., stores information in the storage), it searches the DASD for “control information.” *Id.*, 5:27-31. The control information determines whether the CPU may access the DASD (*id.*, 3:47-51, 4:57-64); thus, it is my opinion that a POSITA would have understood that searching the DASD for control information prior to writing the data to the DASD is a “storage request to access the storage,” for the purposes of storing information (i.e., writing data) to the storage.

89. *Ueno* also teaches that “reserve flags, the reserve CPU numbers and the blockage flags of the two searched control information sets are checked” after

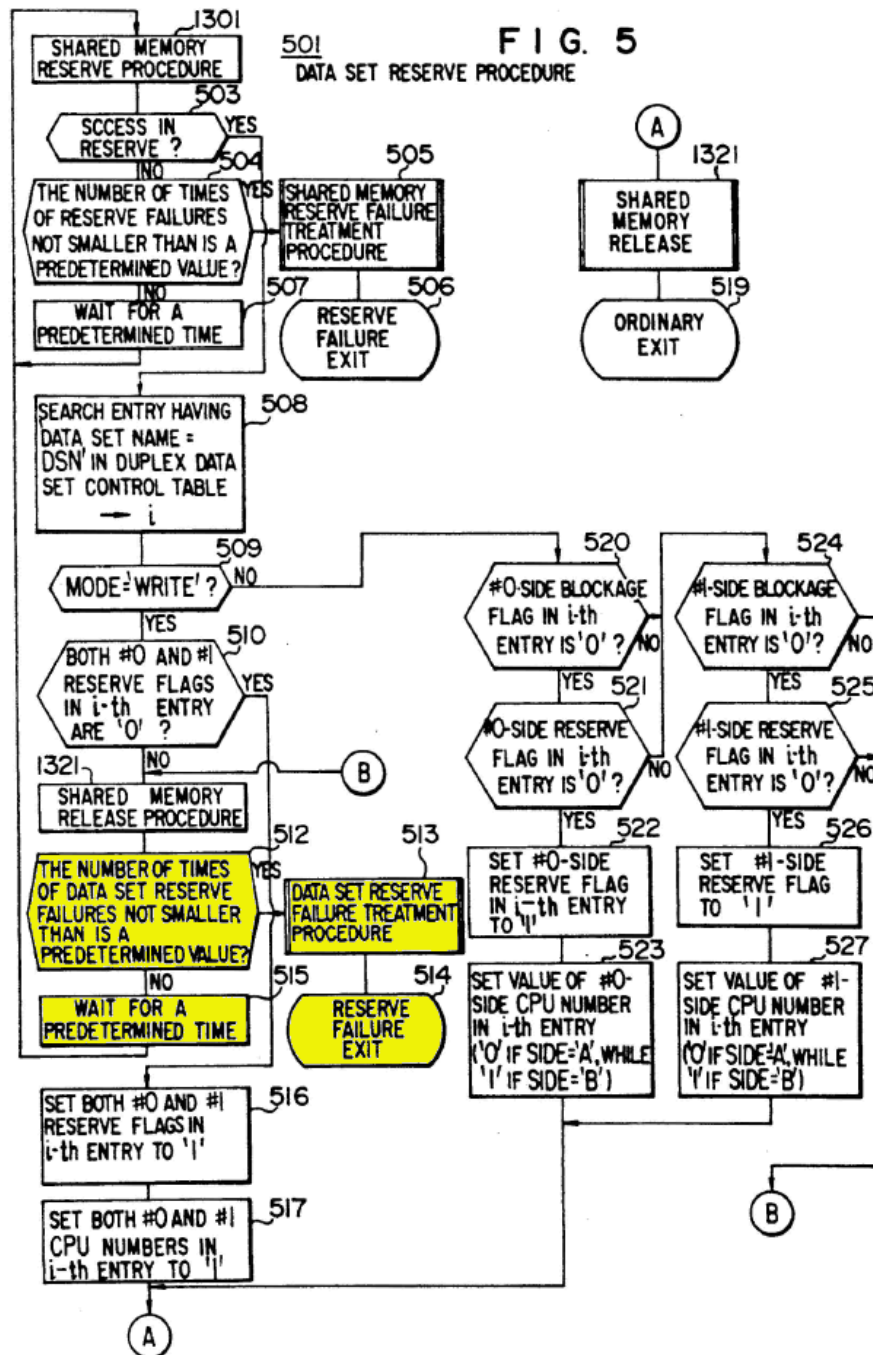
the CPU searches for the control information *Ueno*, 5:33-35. The flags and reserve CPU numbers each indicate whether the DASD is capable of receiving/storing the data to be written (*id.*, 4:57-64, 5:33-43); thus, in my opinion, a POSITA would have also understood that “checking” for flags and a CPU number constitutes determining whether the storage (i.e., the DASD) is available to store the information (i.e., data) based on issuing the storage request (i.e., the search).

90. *Ueno*’s search and check method helps to minimize computer system overhead (*Ueno*, 2:61-64) and helps to ensure accessibility to shared database storage systems. *Id.* 2:51-56, 6:56-61. Thus, in my opinion a POSITA would have been motivated to implement *Ueno*’s search and check method for accessing a storage into *Lohrmann*’s system, to minimize computer system overhead and help ensure data accessibility to in the shared database storage system. The modification is such that the automotive ECU (as taught by *Lohrmann*) determines whether the storage is available to store the sensor information based on issuing the storage request (as taught by *Ueno*). As explained above in Ground 1, such a modification would have been within the purview of a POSITA.

Claim 9[f]: “determining whether a value tracked since the issuance of the request has been reached;”

91. As discussed above for element 9[e] *Lohrmann* as modified by *Tofano* and *Ueno* teaches issuing a storage request and determining whether the storage is

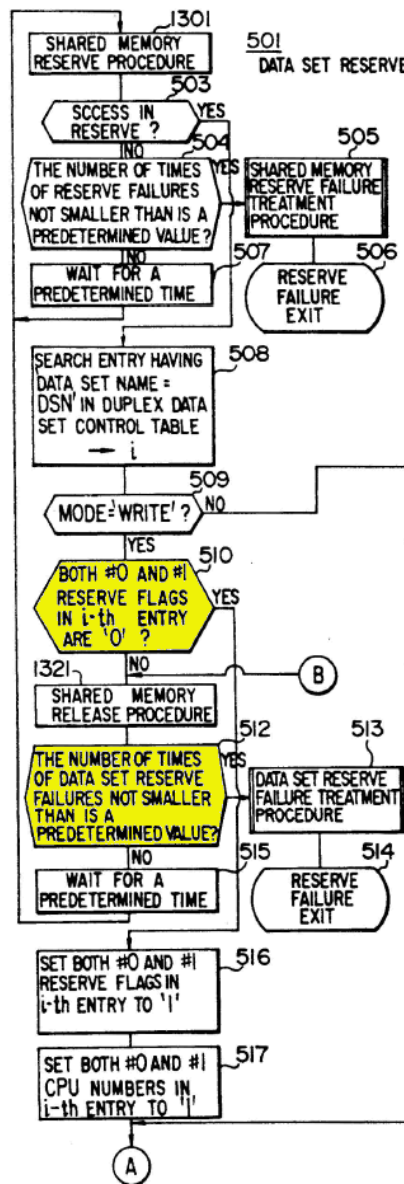
available (i.e., searching and checking). *Ueno* further teaches that the searching and checking includes an iterative process whereby the processor checks for flags (i.e., storage accessibility) after a predetermined number of attempts or time (i.e., a value) elapses. *Ueno*, 11:27-41, Fig. 5.



Ueno, FIG. 5 (annotated)

Claim 9[g]: “in the event the storage included in the automotive electronic control unit is determined, in response to issuing the request, to not be available and the value tracked since the issuance of the request has not been reached, issuing, by the at least one hardware processor to the storage included in the automotive electronic control unit, another request to access the storage included in the automotive electronic control unit to store the sensor information”

92. As discussed above for 9[f], *Lohrmann* as modified by *Tofano* and *Ueno* teaches an iterative process whereby the automotive ECU checks for flags (i.e., storage availability) after a predetermined number of attempts or time (i.e., a value) elapses. *Ueno*, 11:27-41, Fig. 5. *Ueno* further teaches, as part of the iterative process, repeating the search and check cycle (i.e., issuing another request to access storage) “if the number of times in a data set reserving failure is within a predetermined value.” *Id.*, 11: 33-37; Fig. 5.



Ueno, FIG. 5 (annotated)

93. Accordingly, in my opinion, a POSITA would have understood that *Ueno* teaches repeating the check and search process (issuing another request) when the DASD is determined to be unavailable, and the predetermined value of access attempts or time has not been exceeded. The modified system of *Lohrmann*

operates such that the processor *Lohrmann*'s gateway (1) checks the reserve flags associated with a DASD to determine its availability to receive data, and (2) if the reserve flags are not both zero, and the number of attempts is within "a predetermined value," researching and rechecking until either the number of retries exceeds a predetermined value or the DASD is determined to be available. *Ueno*, 11:12–42.

Claim 9[h]: "in the event the storage included in the automotive electronic control unit is determined, in response to issuing the another request, to not be available and the value tracked since the issuance of the request has been reached, sending an error notification; and"

94. *Lohrmann* as modified by *Tofano* and *Ueno* teaches determining whether the DASD (storage) is unavailable. *Ueno*, 11:37-42, FIG. 5. The resource is unavailable "[i]f at least one of the reserve flags 202-1 and 202-2 is '1' (Step 510)." *Id.*, 11:25-33. *Ueno* further teaches reporting "a failure," e.g., to an operator, if the DASD is determined to be unavailable and the number of reattempts (as discussed above in claim element 1[h]) exceeds the predetermined value. *Id.*, 10:19-23; see *also id.* 11:1-6 (reporting other failures to an operator).

Claim 9[i]: "in the event the storage included in the automotive electronic control unit is determined, in response to issuing the

request or the another request, to be available, storing the sensor information utilizing the storage;”

95. As discussed above for element 9[f], *Lohrmann* as modified by *Tofano* and *Ueno* teaches determining whether the DASD (storage) is available. *Ueno* further teaches that if both reserve flags are set to 0, “[t]he CPU executes writing the same contents into the data sets on the two DASDs.” *Id.*, 5:42-43. Thus, it is my opinion that a POSITA would have understood that *Ueno* teaches storing the data to the storage and that the combination of *Lohrmann Tofano* and *Ueno* teaches storing sensor information (as disclosed by *Lohrmann*) to a DASD (as taught by *Ueno*) in response to performing (and repeating) the search and check process (issuing the/another request).

Claim 9[j]: “wherein the automotive electronic control unit is operable such that the sensor information is capable of being transmitted in less than one second using a second network protocol associated with a second network, and”

96. *Lohrmann* further discloses that the information is *capable* of being transmitted using a second network protocol associated with a second network (e.g., CAN, Lin, FlexRay). *Lohrmann*, ¶ 20. In my opinion, a POSITA would have understood that the information is *capable* of shared in less than one second because networks such as CAN are known to facilitate information transmission at speeds of less than one millisecond.

97. For example, *Staiger* teaches an ECU connected to a plurality of real-time networks, e.g., “several individual CAN [] busses or other multiple purpose networks.” *Id.* ¶ 3. The ECU executes an application program for controlling remote systems of automobiles while concurrently performing gateway functions between the different networks. *Id.* ¶¶ 4–5. *Staiger* explains that the CAN, FireWire, and MOST busses are “real-time” busses, capable of “respond[ing] to stimuli within some small upper limit of response time, typically [in] milliseconds or microseconds,” such that, upon receiving a message, an intercommunication preprocessor “processes the message and initiates immediate distribution” of an “output[] message,” to e.g., a “destination unit.” *Id.* ¶¶ 7, 35, 51, claim 1, Abstract (emphasis added).

98. Thus, in my opinion, a POSITA would have understood that the network protocol associated with *Lohrmann*’s network is “capable” of sharing the sensor information in less than 1 second (e.g., milliseconds or microseconds). It is also my opinion that it would have also been obvious to a POSITA to configure the modified system of *Lohrmann* such that message information sent from a sensor origin on a CAN, LIN, or FlexRay Network reaches its destination in milliseconds or microseconds (i.e., “less than one second”) to facilitate immediate receipt of an incoming message from a sensor origin and distribution of an output message to a destination, such as an actuator. *Staiger*, 7, 35, 51, claim 1, Abstract.

Claim 9[k]: “where the first network is one of a Controller Area Network, a Flexray network, or a Local Interconnect Network, and the second network is another one of the Controller Area Network, the Flexray network, or the Local Interconnect Network.”

99. *Lohrmann* discloses that various data bus systems may be used within each network segment, including CAN, FlexRay and LIN (*Lohrmann*, ¶ 20) and that the system “is preferably suitable for operating network segments which are based on different bus systems, since the actual data bus system in the network segment is not significant for managing network segments.” *Id.*, ¶ 10. Thus, *Lohrmann* discloses that the first network is one of a Controller area, Flexray, or Local Interconnect Network and the second network is “based on different bus systems,” i.e., another one of the Controller Area Network, the Flexray network, or the Local Interconnect Network.

Claim 10: “The apparatus as recited in claim 9, wherein the apparatus is operable such that network layer translation is capable of being avoided.”

100. *Tofano* further teaches that “[s]ometimes, differences in network layer models may not be important or significant. For example, a preset number of network layers from different networks may be encapsulated as payload and transmitted between different networks without requiring any comparisons or translations.” *Tofano*, 14:47-52. Thus, *Lohrmann* as modified by *Tofano* further teaches that “network layer translation is capable of being avoided.”

Claims 11 and 12: “The apparatus as recited in claim 9, wherein the apparatus is configured for sharing automotive sensor data received via the first network for use in connection with an automotive device on the second network, in less than the one second [a millisecond].”

101. *Lohrmann* further discloses sharing sensor data received via a first network segment (and corresponding data bus) for use “in connection with” an automotive device on an another network segment (and corresponding data bus). *Lohrmann*, ¶¶ 3, 4, 21 (explaining that a control unit (e.g., sensor or actuator) in a first network communicates with another control unit on another network, and that the control units correspond to automotive devices e.g., the “engine” or “interior”).

102. As discussed above for element 9[j], a POSITA would have understood that *Lohrmann*’s CAN bus can transmit the sensor information between networks in less than 1 second (e.g., milliseconds or microseconds). In my opinion, it would have also been obvious to a POSITA to configure the modified system of *Lohrmann* such that the information is shared between networks in milliseconds or microseconds (i.e., “less than one second” or “less than a millisecond”) to facilitate immediate receipt of an incoming message from a sensor origin and distribution of an output message to a destination, such as an actuator. *Staiger*, 7, 35, 51, claim 1, Abstract.

Claims 13 and 14: “The apparatus as recited in claim 9, wherein the apparatus is operable such that the request and the another request are identical [the same].”

103. As explained with respect to element 9[g], *Ueno* teaches repeating the write request (search and check) if a reserve flag is “1” and a retry value has not been exceeded. *Ueno*, 11:12-42. This is the exact procedure described in the ’179 patent’s specification. Ex-1001, 10:12-14 (“If the resource is not available, it may try it again after a waiting period (1011) until the resource is available.”) Thus, it is my opinion that a POSITA would have understood that *Ueno* teaches that “the another request” is identical to or the same as “the request” to the extent that the ’179 patent discloses the same.

Claims 15 and 16: “The apparatus as recited in claim 9, wherein the apparatus is operable such that the sensor information excludes all [at least a portion of any] header bits of the message.”

104. It is my opinion that a POSITA would have understood or found it obvious that *Lohrmann*’s sensor information does not include, and therefore excludes, all or at least a portion of any header bits of the message because the industry standard¹ for network communication at the time of the invention, required as much to facilitate communication between CAN, LIN, and Flexray

¹ Set forth by the International Standards Organization (ISO and establishing a CAN “serial communication protocol that supports distributed real-time control and multiplexing for use within road vehicles.” Ex. 1019, 7.

networks. Ex. 1019 (explaining that the “layered” CAN architecture established by the OSI reference model includes a data link layer and a physical layer (PL) for bit encoding/decoding); Ex 1022, 2:63-3:7 (explaining that “headers are data processed in order from the lowest (Physical) layer to the highest (Application) layer” when data packets are received).

105. To the extent this requires clarification, *Tofano* teaches examples of network layer models (including OSI) which “support the transfer of data and information through one or more networks having a network format corresponding to a network layer model.” *Tofano*, 11:6-10. Regarding the OSI model, *Tofano* states:

Layer **2**, the Data Link layer **152**, also known as the Protocol layer, controls transmissions made through the physical layer, while detecting and correcting transmission errors to ensure error free, end-to-end transmissions 50 between networked devices. Network layer **153**, the third network layer, controls the operation of the data link and physical layers while providing higher level services such as routing and congestion control for transmissions.

Id., 11:47-54.

106. *Tofano* further teaches a decoding process for receiving data between networks using the OSI model, whereby “data received in a network format may be decoded or extracted from its incoming physical layer and data link layer, so

that decoded data can be represented by the contents of network layers 3 through 7 inclusive.” *Tofano*, 23:36-49. In Figure 7a, for example, “layers 3 through 7 are removed by decoding, and the decoded data 302 is represented as extracted from physical layer L1 and data link layer L2. L1 and L2 are collectively denoted as 303, and are removed by the network interface, processor, or both. *Id.*, 24:51-58 (emphasis added).

107. In my opinion, it would have been obvious to a POSITA to configure *Lohrmann*’s apparatus to transmit sensor information using the OSI Reference model, whereby the information is packaged into a packet of layers including header bits, and the packet is decoded such that the header bits are removed from the packet (message) upon receipt, as taught by *Tofano*, to facilitate data transfer (sensor information transfer) and provide network-wide packet delivery. This configuration would have ensured compliance with the ISO and OSI reference model. *Id.*; Ex 1022, 2:63-3:7 (explaining that “headers are removed and data processed in order from the lowest (Physical) layer to the highest (Application) layer” when data packets are received).

108. Because the payload (the actual information being transmitted), in the instant combination is the sensor information, it is my opinion that a POSITA would have understood that the portion of a message that is “sensor information” would not include, *i.e.*, excludes all header bits. If “all header bits of the message”

are excluded, “at least a portion of any header bits of the message” are necessarily excluded; thus, claim 16 is obvious for the same reasons as claim 15.

Claim 17: “The apparatus as recited in claim 9, wherein the apparatus is operable such that the storage includes a bulletin board.”

109. As discussed above with respect to claim element 9[e], *Lohrmann* as modified by *Tofano* and *Ueno* teaches a DASD. *Ueno*, 1:8-9, 5:21-22, 41-42. The DASD is a database from which electronic data may be read and written. *Id.* In my opinion, A POSITA would have understood that the DASD is a “bulletin” within the meaning of the ‘179 patent, which provides that “the bulletin board may refer to any database that enables users to send and/or read electronic messages, files, and/or other data that are of general interest and/or addressed to no particular person/process.” Ex-1001, 6:64-7:3.

Claims 18-20: “The apparatus as recited in claim 9, wherein the apparatus is operable such that the error notification is sent, when the storage included in the automotive electronic control unit is determined, in response to issuing the [another] request, to not be available and the value tracked since the issuance of the request has been reached.”

110. As discussed above with respect to claim element 9[f], *Ueno* teaches reporting (i.e., sending) “a failure,” e.g., to an operator, if the DASD is determined to be unavailable and the number of reattempts (as discussed above in claim

element 9[e]) exceeds the predetermined value. *Id.*, 10: 19-23; see *also id.* 11:1-6 (reporting other failures to an operator).

4. Independent Claim 21

111. As illustrated in the chart below, Independent claim 21 largely mirrors independent claim 9, except that claim 21 is directed to a “non-volatile or volatile computer-readable medium of an automotive electronic control unit” (Ex. 1001, 17:7-12) and does not require that “the first network is one of a Controller Area Network, a Flexray network, or a Local Interconnect Network, and the second network is another one of the Controller Area Network, the Flexray network, or the Local Interconnect Network.”

112. Claim 21 also recites “ceasing repeating issuance of another storage resource request” instead of “sending an error notification.” But because the combination, as discussed in 9[h] teaches sending the error notification instead of another storage resource request, the combination also renders obvious “ceasing” repeating the storage request. Thus, in my opinion claim 21 is obvious over Lohrmann, *Tofano*, *Ueno*, and *Staiger* for the reasons explained for independent claim 9.

9 [pre]. An apparatus, comprising:	21[pre]: A non-volatile or volatile computer-readable medium of an automotive electronic control unit for storing a computer program product including code that, when executed by
9[a]an automotive electronic control unit including a memory storage comprising instructions, and	

9b at least one hardware processor in hardwired communication with the memory storage,	at least one hardware processor included in the automotive electronic control unit in communication with the computer-readable medium, is for:
9c wherein the at least one hardware processor executes the instructions for:	
9[d]identifying sensor information associated with a message received utilizing a first network protocol associated with a first network;	receiving sensor information associated with a message received utilizing a first network protocol associated with a first network;
9[e]in response to identifying the sensor information, issuing, by the at least one hardware processor and to a storage included in the automotive electronic control unit, a request to access the storage included in the automotive electronic control unit to store the sensor information and, in response to issuing the request, determining whether the storage is available to store the sensor information;	in response to receiving the sensor information, issuing, by the at least one hardware processor and to a storage included in the automotive electronic control unit, a request to access the storage included in the automotive electronic control unit, for determining whether the storage included in the automotive electronic control unit is available to store the sensor information;
9[f]determining whether a value tracked since the issuance of the request has been reached;	determining whether a time-related value tracked after the issuance of the request has been reached in association with the determination whether the storage is available;
9[g]in the event the storage included in the automotive electronic control unit is determined, in response to issuing the request, to not be available and the value tracked since the issuance of the request has not been reached, issuing, by the at least one hardware processor to the storage included in the automotive electronic control unit, another request to access the storage	when the storage included in the automotive electronic control unit is determined to not be available and the value associated with the determination whether the storage is available has not been reached, issuing, by the at least one hardware processor to the storage included in the automotive electronic control unit, another request to access the storage included in the automotive

included in the automotive electronic control unit to store the sensor information;	electronic control unit to store the sensor information;
9[h]in the event the storage included in the automotive electronic control unit is determined, in response to issuing the another request, to not be available and the value tracked since the issuance of the request has been reached, sending an error notification; and	when the storage included in the automotive electronic control unit is determined to not be available and the value associated with determination whether the storage is available has been reached, ceasing repeating issuance of another request ; and
9[i]in the event the storage included in the automotive electronic control unit is determined, in response to issuing the request or the another request, to be available, storing the sensor information utilizing the storage;	when the storage included in the automotive electronic control unit is determined to be available, storing the sensor information utilizing the storage;
9[j]wherein the apparatus is operable such that the sensor information is capable of being transmitted in less than one second utilizing a second network protocol associated with a second network,	wherein the computer program product is operable such that the sensor information is capable of being transmitted in less than one second utilizing the automotive electronic control unit that remains in hardwired communication with the first network and a second network.
9[k]where the first network is one of a Controller Area Network, a Flexray network, or a Local Interconnect Network, and the second network is another one of the Controller Area Network, the Flexray network, or the Local Interconnect Network.	

Dependent Claims 22-24 and 27

113. Dependent claims 22-24 mirror dependent claims 2, 3, and 5, respectively. Therefore, it is my opinion that claims 22-24 are obvious over *Staiger* for the same reasons discussed above in Ground 2. Dependent claim 27 mirrors dependent claim 12 and is likewise obvious for the same reasons.

Dependent Claims 25 and 26

114. Dependent claim 25 mirrors dependent claims 5 and 24 but further requires the first Network to be one of a Controller Area Network, a Flexray network, or a Local Interconnect Network, and the second network is another one of the Controller Area Network, the Flexray network, or the Local Interconnect Network (Ex-1001, 18:19-27), which *Lohrmann* already discloses as discussed for element 9[k]. Thus, in my opinion, claim 25 is obvious for the same reason as claim 24 and 9[k].

115. Dependent claim 26 requires “the transmitting” to be “completed in less than a millisecond” and therefore encompasses the same scope as claim 25 and is obvious for the same reasons.

B. MIESTERFELD GROUNDS

116. Ground 2 establishes that *Miesterfeld* discloses or suggests each of the claimed features but arguably lacks express disclosure of (1) tracking a “value” and corresponding error notification (all Grounds), (2) CAN, FlexRay, and LIN

networks (Grounds 5-7), (3) a hardware processor (Grounds 6-8) and (4) header bit removal (Ground 7). *Stewart, Wense, Wong, and Ma* are relied upon to teach each of these respective features.

1. Ground 4 Claims 1-7 and are obvious over *Miesterfeld* in view of *Stewart*.

Claim 1[pre]: “A method, comprising:”

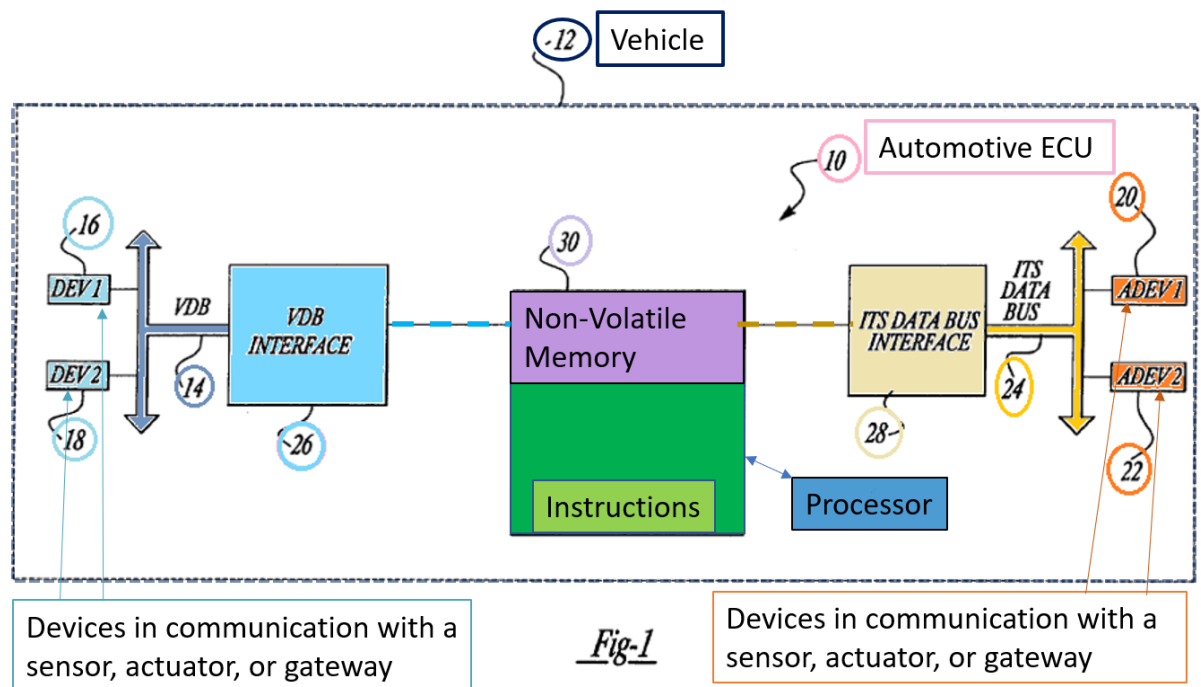
117. To the extent the preamble is limiting, *Miesterfeld* discloses a system and corresponding method. *Miesterfeld*, 2:23-24 (“[t]his invention is directed to a data sharing system in a vehicle.”); *id.*, 1:6-10.

Claim 1[a]: “at an automotive electronic control unit: receiving sensor information associated with a message;”

118. *Miesterfeld* discloses an automotive electronic control unit (ECU) because *Miesterfeld*’s system includes a “vehicle system controller,” i.e., a “gateway” for “process[ing] vehicle data to control at least one vehicle related function.” *Miesterfeld*, 2:24-28. Using a vehicle data bus (VDB) and an intelligent transportation system (ITS) data bus, the gateway receives sensor information from automotive devices 16, 18, 20 and 22. *Miesterfeld*, Fig. 1, 1:13-25, 2:66-3:25 (explaining that devices 16 and 18 “control vehicle operations such as engine operation, transmission operation, instrumentation operation, and the like”), 1:31-40, 3:14-17 (explaining that devices 20 and 22 “require vehicle data as input in

order to operate the device or implement some additional feature on the vehicle”
and “may also seek to control vehicle functions where appropriate and safe”);.

119. *Miesterfeld*’s sensor information is associated with a message because it is stored and accessible through memory read/write operations. *Miesterfeld*, 2:66-3:1, 3:18-25, 3:40-43, 3:59-64, *see also id.*, 1:62-2:15 (describing gateway functions for exchanging data between networks). Thus, in my opinion, *Miesterfeld*’s process includes a gateway (ECU) receiving sensor information associated with a message from either VDB 14 or ITS data bus 24.



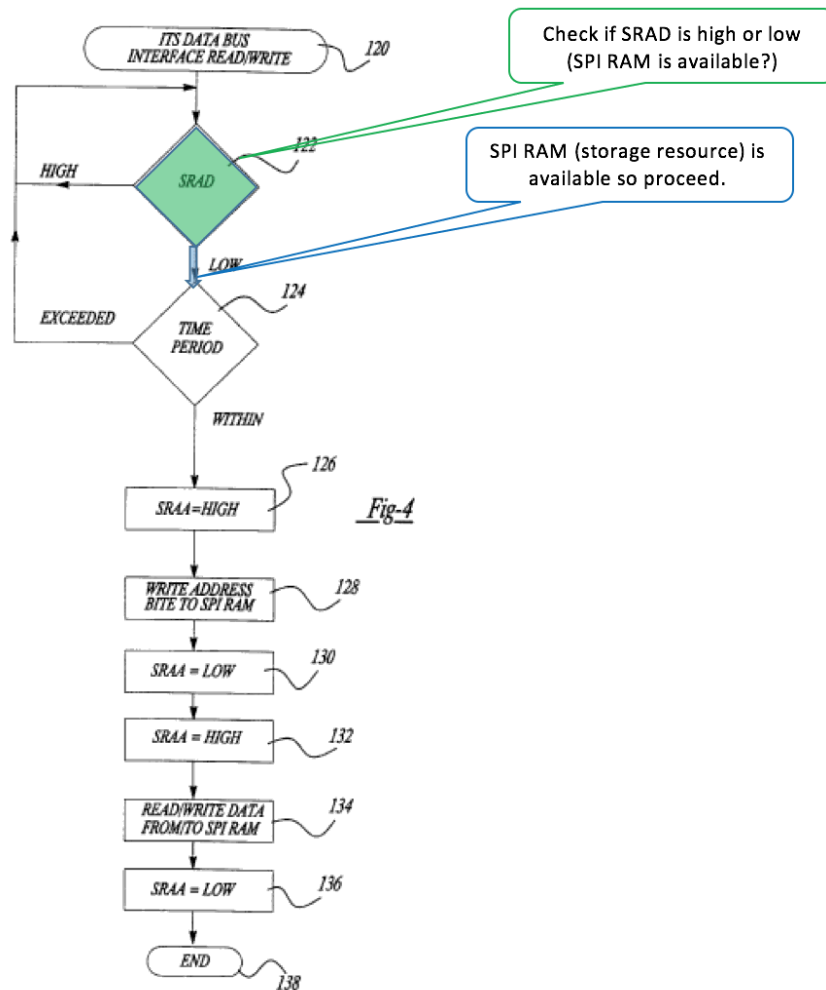
Miesterfeld, FIG. 1 (annotated)

Claim 1[b]: “based on receiving the sensor information, issuing, to a storage included in the automotive electronic control unit, a request to access the storage included in the automotive electronic

control unit to store the sensor information and, based on issuing the request, determining whether the storage is available to store the sensor information”

120. *Miesterfeld* issues a request to access the storage in response to the receiving the information. *Miesterfeld* explains, for example, that when ITS data bus interface 58 (another example of the ITS data bus interface 28 shown in FIG. 1) “attempts to access SPI RAM 64” (a specific implementation of memory 30) such as for reading or writing, “the ITS data bus interface 58 must first test the SRAD signal line as shown at block 122.” *Miesterfeld*, 6:34-36. *Miesterfeld*’s “attempts to access SPI RAM 64” is a “request to access the storage” (i.e., request to access memory, which is a storage). *Miesterfeld*, 3:64-66; 3:26-39.

121. *Miesterfeld* also discloses determining whether the storage is available for storing the information. As shown above in annotated FIG. 4., *Miesterfeld* discloses that “[i]f SRAD is high, the VDB interface 62 is accessing SPI RAM 64, and ITS data bus interface 58 must wait until SPI RAM 64 is available, and control returns to block 122,” but “[i]f SRAD is low, SPIRAM 64 is available.” *Miesterfeld*, 4:22-26, 5:38-43, 6:33-40. In my opinion, checking the state of SRAD to determine if another bus interface is accessing the storage corresponds to “determining whether the storage is available to store the sensor information.”

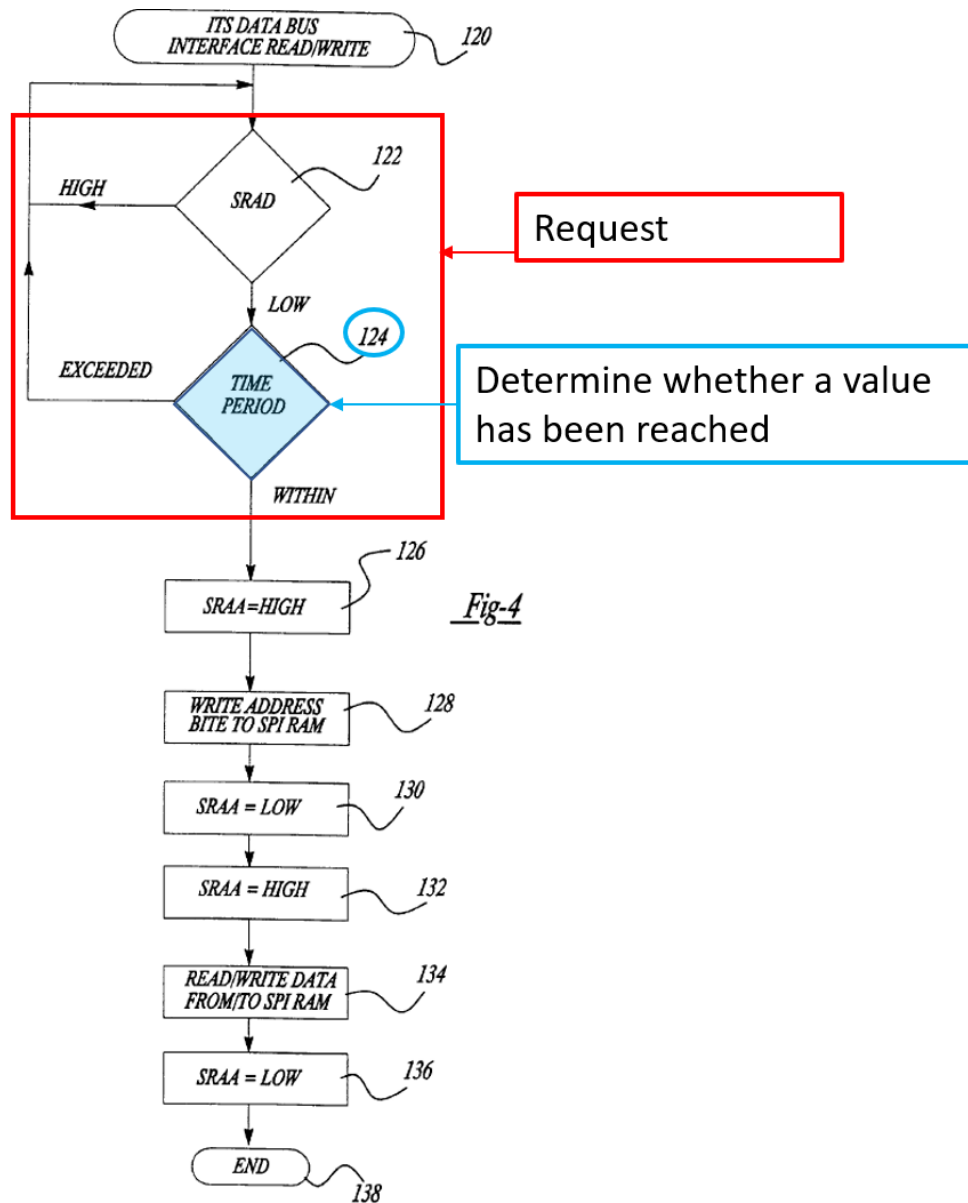


Miesterfeld, FIG. 4 (annotated)

Claim 1[c]: “determining whether a value tracked since the issuance of the request has been reached indicating that the storage has not been available in association with the value tracked since the issuance of the request;”

122. *Miesterfeld* discloses tracking a value upon issuing the storage request and determining whether the value has been reached. *Miesterfeld*, 6:46-50. As

shown in annotated FIG. 4, *Miesterfeld* discloses that “[w]hen ITS data bus interface 58 determines that SPI RAM 64 is available, ITS data bus interface 58 sets the SRAA signal line high, as shown at block 126” and that “in a preferred embodiment, setting SRAA high must occur within 5 micro-seconds after determining that the SRAD signal line is low.” *Miesterfeld*, 6:40-45. Thus, it is my opinion that *Miesterfeld*’s process tracks how much time (a value) has elapsed since issuing the storage request. By determining in step 124 whether 5 μ s have elapsed (red), *Miesterfeld* also discloses whether the value indicating storage unavailability has been reached.



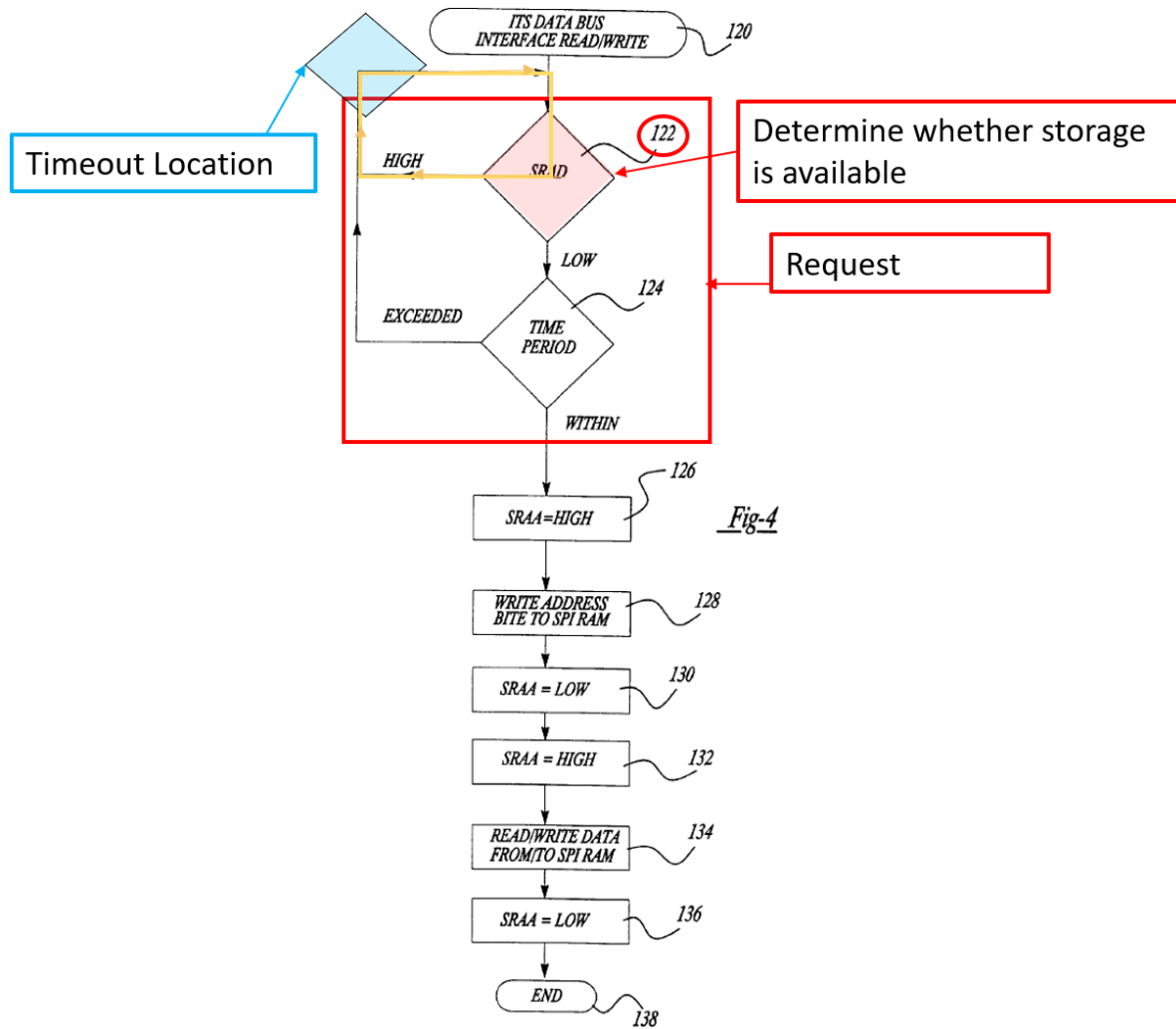
Miesterfeld, FIG. 4 (annotated)

123. In my opinion, *Stewart* also teaches this feature. *Stewart* teaches a multiprocessor synchronization method in which a “bounding wait time” (value) is implemented to “guarantee that tasks will get the data they require on time, every time.” *Stewart*, 330. *Stewart* also teaches implementing a “time-out mechanism”

for preventing data transfer when a “pre-specified time or number of retries” elapses. *Stewart*, 330 (emphasis added).

124. Both *Miesterfeld* and *Stewart* relate to real-time distributed computer control systems and use similar techniques to solve the same problem (a shared memory architecture for facilitating data exchange between control modules in a real-time distributed system. *Stewart*, 1, 6, 7; *Miesterfeld*, 6:60-63, Fig. 4). It is my opinion that a POSITA would have had a reasonable expectation of success in modifying *Miesterfeld*’s process to include the step of determining whether a value is reached (and other value-based steps) and providing an error notification (as discussed below), and that the modification would have required only ordinary skill.

125. In my opinion, it would have been obvious to a POSITA to modify *Miesterfeld*’s process to implement a timeout mechanism (blue) in the logical loop (yellow) as illustrated in annotated Fig. 4 below to ensure timely and consistent data exchange.

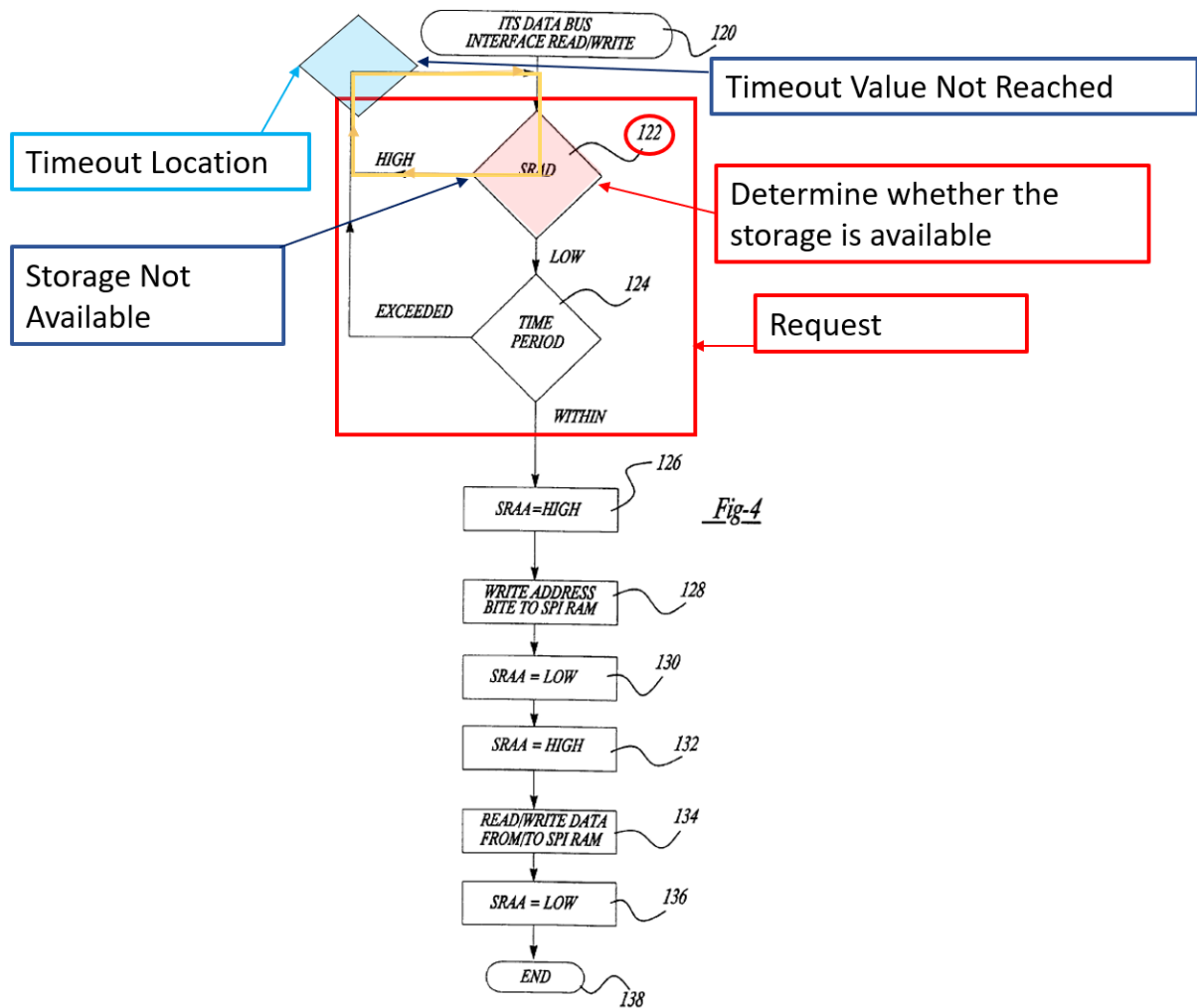


Miesterfeld, FIG. 4 (annotated)

Claim 1[d]: “based on the storage included in the automotive electronic control unit being determined, based on issuing the request, to not be available and the value tracked since the issuance of the request having not been reached indicating that the storage has not been available in association with the value tracked since the issuance of the request, issuing, to the storage included in the automotive electronic control unit, another

request to access the storage included in the automotive electronic control unit to store the sensor information; and”

126. *Miesterfeld* discloses repeating the storage request if SRAD is high and therefore discloses issuing “another” request to access the storage “when the storage is not available.” *Miesterfeld*, Fig. 4. As discussed above for 1[c], *Stewart's* timeout operates by preventing data transfer if the number of retries has not been exceeded; thus, the combination is such that *Miesterfeld's* request repeats if a “pre-specified” number of retries have not elapsed, i.e., “if the value tracked” has not “been reached.” *Stewart*, 330.



Miesterfeld, FIG. 4 (annotated)

Claim 1[e]: “based on the storage included in the automotive electronic control unit being determined, based on issuing the request or the another request, to not be available and the value tracked since the issuance of the request having been reached, sending an error notification; and”

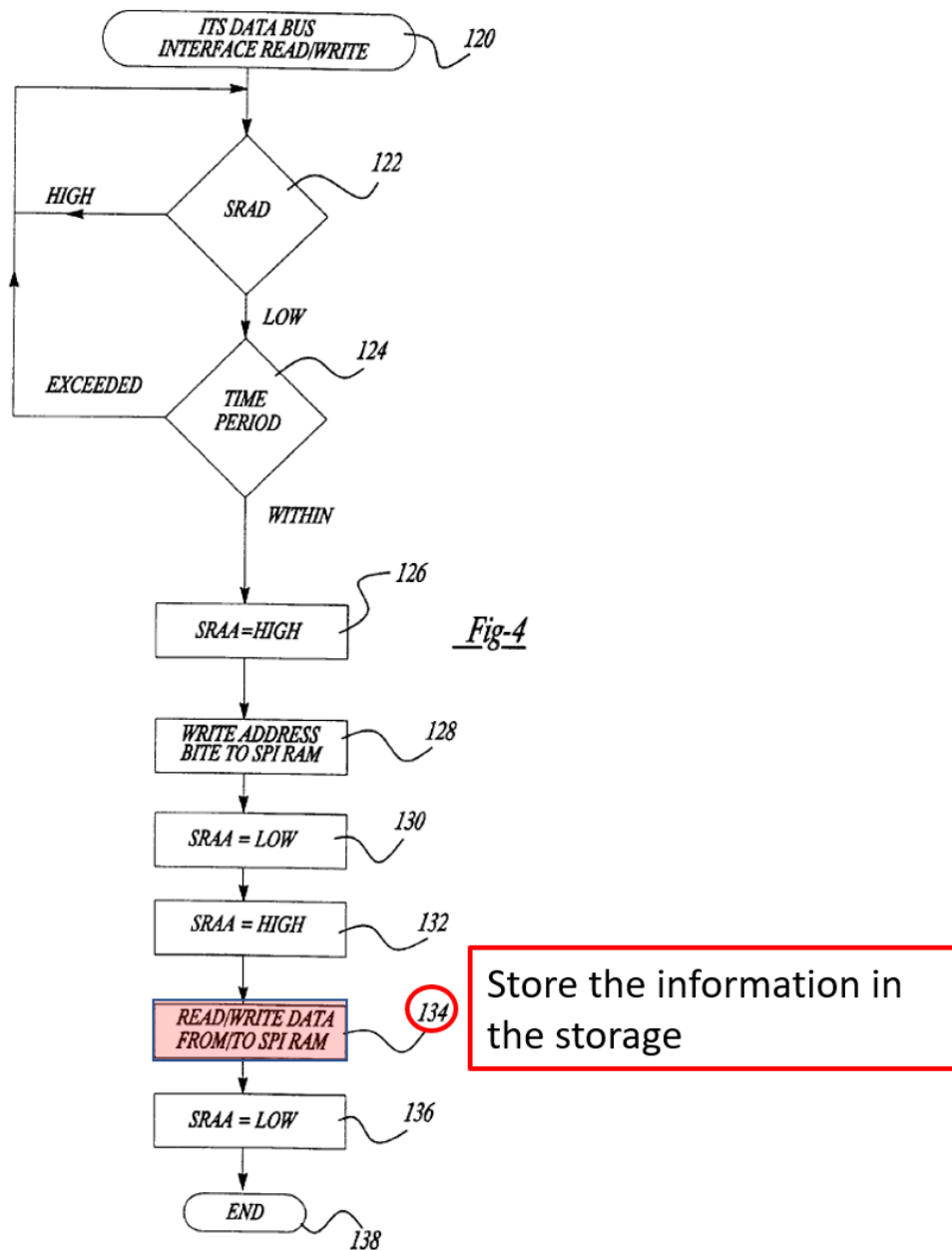
127. *Miesterfeld* in combination with *Stewart* teaches sending an error notification when the value is reached. *Stewart* discloses that “error handlers should be installed to detect tasks that suffer successive time-out errors.” *Stewart*, 330. It is my opinion that a POSITA would have understood that *Stewart*’s error

handlers not only detect the error but that the use of “error handlers” discloses or render obvious error notification as is well known in the art. Indeed, a POSITA would have understood that error detection without notification is useless and would have found it obvious for the error handlers to do so. Such notification may have been embodied as an exit code or error message.

128. In my opinion, it would have been further obvious to a POSITA to modify *Miesterfeld*’s process to incorporate sending error notification by providing an exit code or an error message, as at least suggested by *Stewart*, when a timeout occurs and if the storage is not available. Ex-1014, 137-38, 149-51, 154-56 (explaining that using a timeout to prevent deadlock (which could lead to program failure) was well-known in the art).

Claim 1[f]: “based on the storage included in the automotive electronic control unit being determined, based on issuing the request or the another request, to be available, storing the sensor information utilizing the storage”

129. *Miesterfeld* discloses storing the information using the shared memory if the memory is available. *Miesterfeld* discloses that the ITS data bus stores data in the SPI RAM (shared memory/storage) after the “ITS data bus interface 58 determines that the SPI RAM 64 is available,” and sets the SPI RAM Access Required (SRAA) signal line to high. *Miesterfeld*, 6:40-54.



Miesterfeld, FIG. 4 (annotated)

Claims 2 and 3 “The method as recited in claim 1, wherein the sensor information reaches a destination in less than one second [millisecond].”

130. *Miesterfeld* discloses that “the time period between selecting the desired memory page and reading/writing data to SPI RAM 64 (between steps 130

and 132) is less than 5 microseconds.” *Miesterfeld*, 6:60-63, Fig. 4. *Miesterfeld* also explains that the VDB interface may transmit any data received from the ITS data bus within 40 milliseconds. *Id.*, 8:51-56. Thus, in my opinion, *Miesterfeld* discloses that the data (and corresponding information) reaches “a destination” in less than one second.

Claims 4 and 5 “The method as recited in claim 1, wherein a duration between the sensor information being received and being transmitted is less than one second [millisecond].”

131. As discussed above in claim 2, *Miesterfeld* discloses that “the time period between selecting the desired memory page and reading/writing data to SPI RAM 64 (between steps 130 and 132) is less than 5 microseconds.” *Miesterfeld*, 6:60-63, Fig. 4a. Thus, *Miesterfeld* discloses that the duration between the sensor information being received and being transmitted is less than one second or millisecond.

Claim 6 “The method as recited in claim 1, wherein the sensor information is transmitted from the automotive electronic control unit in less than a millisecond from a time when the message is received at the automotive electronic control unit.”

132. As discussed above in claim 2, *Miesterfeld* discloses that “the time period between selecting the desired memory page and reading/writing data to SPI RAM 64 (between steps 130 and 132) is less than 5 microseconds.” *Miesterfeld*, 6:60-63, Fig. 4a. Thus, in my opinion, *Miesterfeld* discloses that the sensor

information is transmitted (written) in less than a millisecond (within 5 μ s) from when the data and corresponding message are received (read).

Claim 7: “The method as recited in claim 6, wherein at least one of: ...the value is time related ...”

133. Claim 7 requires “at least one of” numerous features describing the method of claim 6. Ex. 1001, 14:65-15:42. These features are listed in the alternative. Because *Miesterfeld* discloses “at least one” of these features, e.g., that “the request includes a storage resource request,” it is my opinion that claim 7 is also obvious over the prior art.

2. Ground 5: Claim 8 is obvious over *Miesterfeld* in view of *Stewart and Wense*

Claim 8: “The method as recited in claim 1, wherein automotive sensor data is transmitted between heterogeneous networks including at least one of a Controller Area Network, a Flexray network, or a Local Interconnect Network.”

134. *Miesterfeld*’s gateway receives information obtained from devices 16, 18, 20 and 22 data over the VDB and ITS data bus. *Miesterfeld*, Fig. 1, abstract, 2:66-3:25. The information obtained from devices 16, 18, 20 and 22 pertains to sensor information because it relates to measured vehicle data. *Id.*, 3:2-25, 1:13-25 (explaining that devices 16 and 18 “control vehicle operations such as engine operation, transmission operation, instrumentation operation, and the like”), 1:31-40, 3:14-17 (explaining that devices 20 and 22 “require vehicle data as input in

order to operate the device or implement some additional feature on the vehicle” and “may also seek to control vehicle functions where appropriate and safe”). Thus, *Miesterfeld* discloses transmitting automotive sensor data between heterogeneous networks.

135. In my opinion, *Miesterfeld* at least suggests that the heterogenous networks include at least one of a Controller Area Network (CAN), a Flexray network, or a Local Interconnect Network (LIN) because the ITS data bus 24 (first network) may be “any of a number of ITS data buses, such as D2B, USB, IDB, Firewall, and the like” (*Miesterfeld*, 4:5-10, 9:55-57) and the VDB 14 (second network) may be “configured to implement the J1850 configuration as prescribed by the Society of Automotive Engineers (SAE) or any other industry standard as may be required.” *Id.*, 4:7-10.

136. To the extent further clarification is required, *Wense* teaches that cars utilize “[s]everal multiplex protocols,” including CAN (e.g., for engine control and body control networks), FlexRay (e.g., for safety control, braking, and steering systems), and LIN (e.g., for cost critical distributed body electronics). *Wense*, 11.

137. *Wense*, like *Miesterfeld* and *Stewart* relates to network communication, and *Wense* simply clarifies the types of industry-standard networks that would have been implemented in *Miesterfeld*’s vehicle system. Thus, it is my opinion that a POSITA would have had a reasonable expectation of

success in configuring *Miesterfeld*'s networks to be one of CAN, LIN or FlexRay, and that the modification would have required only ordinary skill.

138. In my opinion, a POSITA would have found it obvious to implement *Miesterfeld*'s VDB and ITS using known bus architectures like CAN, FlexRay, or LIN, as taught by *Wense*, because each was a commonly-used and well-known vehicle data bus for controlling the various vehicle systems of *Miesterfeld*. *Wense*, 11; *Miesterfeld*, 4:7-10; Ex-1020, ¶¶31, 40, 48 (explaining that concurrent use of legacy bus architectures such as CAN, LIN, FLEXRAY “provides for the total integration of vehicle systems and functions, and permits plug-and-play device integration, scalability and upgradeability.”); Ex-1021, 1:21-32; Ex-1004, 2 (“[t]he automotive industry has developed the [CAN] [] in the 1980s and subsequently added new communication bus systems such as MOST, IDB, LIN, and FlexRay.”).

**3. Ground 6: Claims 9-14 and 17-20 are obvious over
Miesterfeld in view of *Wong*, *Stewart* and *Wense***

Claim 9[pre]: “An apparatus, comprising:”

139. To the extent the preamble is limiting, *Miesterfeld* discloses a system. *Miesterfeld*, 2:23-24 (“[t]his invention is directed to a data sharing system in a vehicle.”); *id.*, 1:6-10.

Claim 9[a]: “an automotive electronic control unit including a memory storage comprising instructions, and”

140. *Miesterfeld*'s system includes a “vehicle system controller,” i.e., a “gateway” for “process[ing] vehicle data to control at least one vehicle related function.” *Miesterfeld*, 2:24-28. The gateway “has at least intermittent and direct access to and exchanges data on a vehicle data bus” and as illustrated in annotated FIG. 1 below, includes a memory through which a vehicle data bus (VDB) and intelligent transportation system (ITS) data bus exchange data and commands. *Id.*, 1:5-11, 2:24-49, claim 1. The gateway facilitates communication between computerized devices (automotive ECUs) through a combination of hardware and software (instructions) being read from or written to the memory. *Miesterfeld*, 1:13-3:19 (explaining that “a further object of the present invention to provide a data exchange gateway to enable a third party device to implement selected commands on a vehicle system” and that the common memory between the VDB and ITS “may be used to store specific commands which a third party device may request of a specific vehicle controller”). Accordingly, it is my opinion that *Miesterfeld*'s gateway corresponds to the claimed “automotive electronic control unit.”

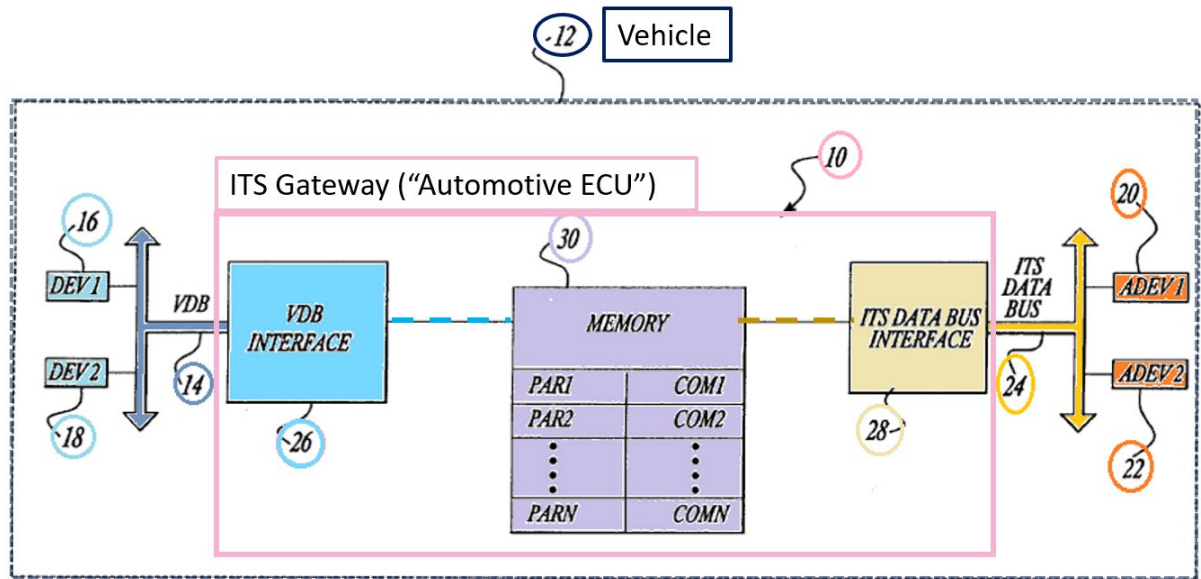


Fig-1

Miesterfeld, FIG. 1 (annotated)

Claim 9[b] and 9[c]: “at least one hardware processor in hardwired communication with the memory storage, wherein the at least one hardware processor executes the instructions for:”

141. In my opinion, *Miesterfeld* at least suggests a hardware processor executing instruction and in hardwired communication with the memory storage because a POSITA would have understood that a processor and instructions are required for *Miesterfeld*’s gateway’s functionality, e.g., enabling data exchange between vehicle systems and third party systems, and controlling information sharing between electronic control devices on the VDB and the ITS data bus for the purpose of monitoring and controlling vehicle functions. *Miesterfeld*, 1:13–40, 2:66–3:49.

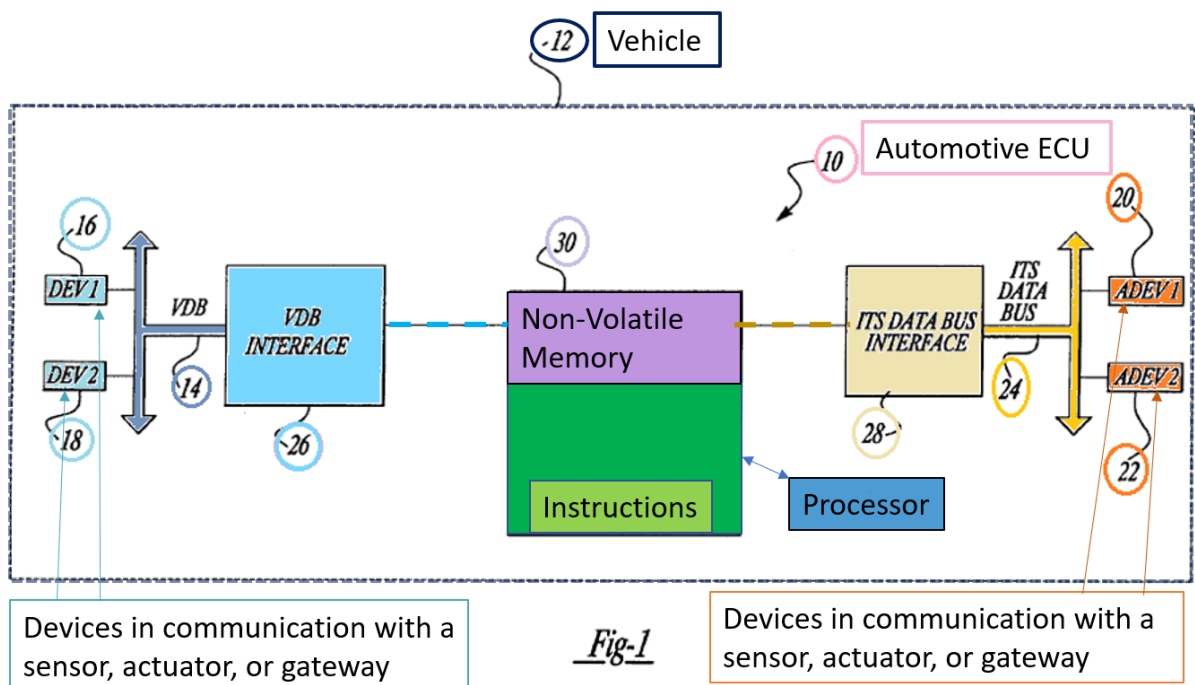
142. In my opinion, *Wong* also renders this feature obvious because *Wong* expressly teaches an automobile control unit (also called “cluster controller”) including a processor, volatile memory, non-volatile memory, and a processor in hardwired communication with each memory. *Wong*, Fig. 4, 3:27-30, 6:4-6.

143. Like *Miesterfeld*’s controller, *Wong*’s controller can execute instructions for controlling data flow management (*Id.*, 6:40-42) and permits communication among automobile devices, including sensors. *Id.*, 7:51-58. Thus, it is my opinion that a POSITA would have had a reasonable expectation of success in modifying *Miesterfeld*’s controller (gateway) to include a hardware processor for executing instructions to perform the disclosed process, and that the modification would have required only ordinary skill. In my opinion, a POSITA would have been motivated to incorporate *Wong*’s processor in *Miesterfeld*’s ITS gateway, whereby the processor is hardwired to the memory and executes instructions, to facilitate data processing for the purpose of monitoring and controlling vehicle functions. *Wong*, 6 10-21, 36-43; 7:51-60.

Claim 9[d]: “identifying sensor information associated with a message received utilizing a first network protocol associated with a first network;”

144. *Miesterfeld*’s gateway receives information obtained from devices 16, 18, 20 and 22 data over the VDB and ITS data bus (i.e., networks and their associated network protocols). *Miesterfeld*, Fig. 1, abstract, 2:66-3:25. The

information obtained from devices 16, 18, 20 and 22 pertains to sensor information because it relates to measured vehicle data. *Id.*, 3:2-25, 1:13-25 (explaining that devices 16 and 18 “control vehicle operations such as engine operation, transmission operation, instrumentation operation, and the like”), 1:31-40, 3:14-17 (explaining that devices 20 and 22 “require vehicle data as input in order to operate the device or implement some additional feature on the vehicle” and “may also seek to control vehicle functions where appropriate and safe”). *Miesterfeld*’s sensor information is associated with a message because it is stored and accessible through memory read/write operations. *Miesterfeld*, 2:66-3:1, 3:18-25, 3:40-43, 3:59-64, *see also id.*, 1:62-2:15 (describing gateway functions for exchanging data between networks).



Miesterfeld, FIG. 1 (annotated)

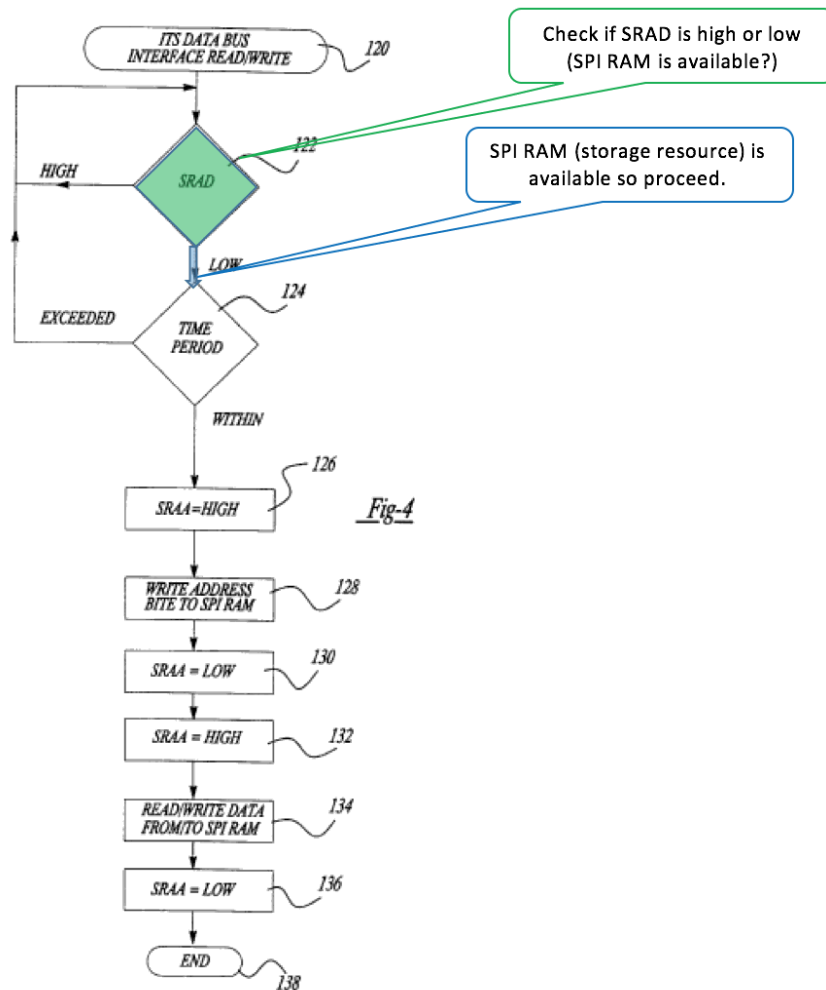
145. Thus, it is my opinion that *Miesterfeld*'s process includes receiving sensor information associated with a message utilizing a first network protocol (VDB or ITS data bus protocol) associated with a first network (VDB 14 or ITS data bus 24). *Miesterfeld* as modified by *Tofano* therefore render obvious a processor executing instructions for identifying sensor information, associated with a message, received utilizing a first network protocol associated with a first network.

Claim 9[e]: “in response to identifying the sensor information, issuing, by the at least one hardware processor and to a storage included in the automotive electronic control unit, a request to access the storage included in the automotive electronic control unit to store the sensor information and, in response to issuing the request, determining whether the storage is available to store the sensor information;”

146. *Miesterfeld* as modified by *Wong* issues a request to access the storage in response to the receiving the information. *Miesterfeld* explains, for example, that when ITS data bus interface 58 (another example of the ITS data bus interface 28 shown in FIG. 1) “attempts to access SPI RAM 64” (a specific implementation of memory 30) such as for reading or writing, “the ITS data bus interface 58 must first test the SRAD signal line as shown at block 122.” *Miesterfeld*, 6:34-36.

Miesterfeld's "attempts to access SPI RAM 64" is a "request to access the storage" (i.e., request to access memory, which is a storage). *Miesterfeld*, 3:64-66; 3:26-39.

147. *Miesterfeld* also discloses determining whether the storage is available for storing the information. As shown above in annotated FIG. 4., *Miesterfeld* discloses that "[i]f SRAD is high, the VDB interface 62 is accessing SPI RAM 64, and ITS data bus interface 58 must wait until SPI RAM 64 is available, and control returns to block 122," but "[i]f SRAD is low, SPIRAM 64 is available." *Miesterfeld*, 4:22-26, 5:38-43, 6:33-40. In my opinion, checking the state of SRAD to determine if another bus interface is accessing the storage corresponds to "determining whether the storage is available to store the sensor information."

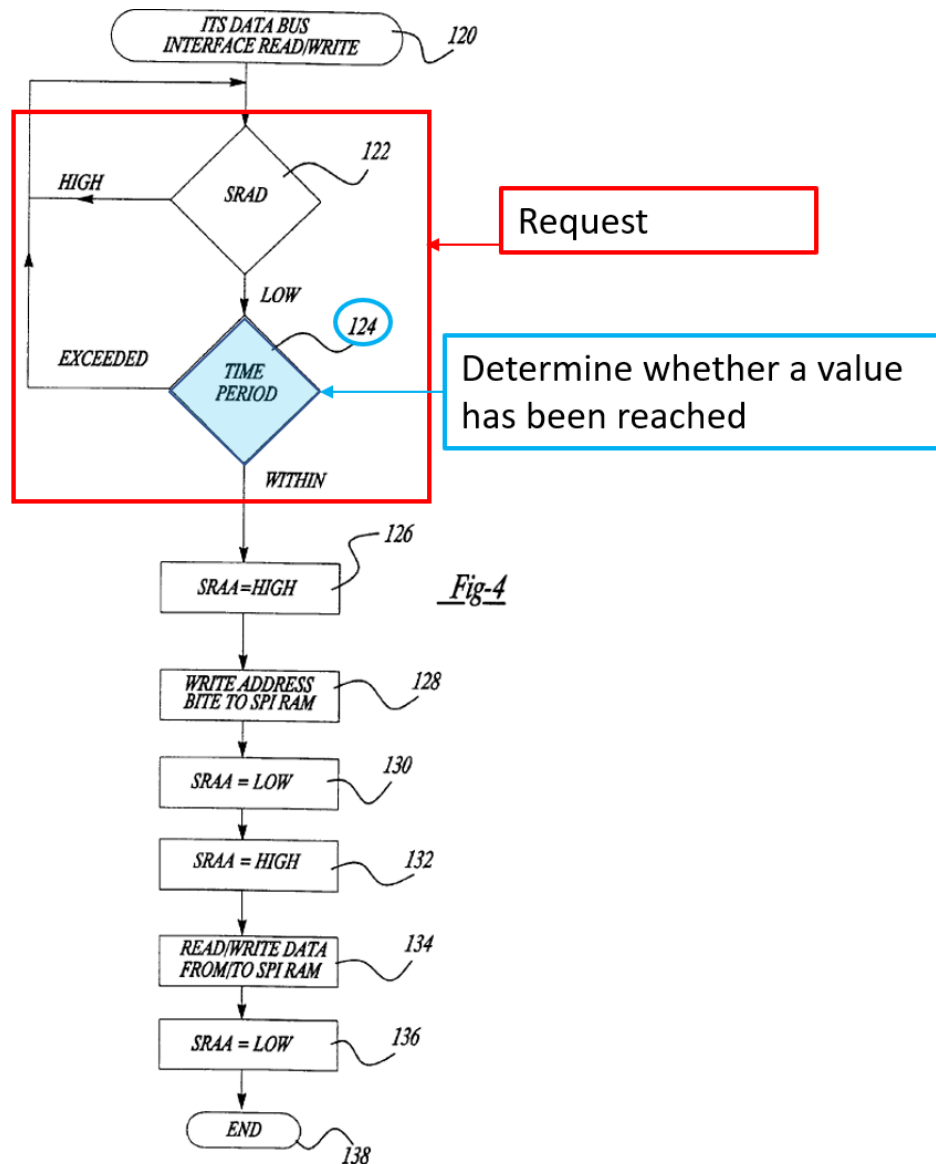


Miesterfeld, FIG. 4 (annotated)

Claim 9[f]: “determining whether a value tracked since the issuance of the request has been reached;”

148. In my opinion, *Miesterfeld* discloses determining whether a value tracked since issuance of the storage request has been reached. *Miesterfeld*, 6:46-50. As shown in annotated FIG. 4, *Miesterfeld* discloses that “[w]hen ITS data bus interface 58 determines that SPI RAM 64 is available, ITS data bus interface 58 sets the SRAA signal line high, as shown at block 126” and that “in a preferred

embodiment, setting SRAA high must occur within 5 micro-seconds after determining that the SRAD signal line is low.” *Miesterfeld*, 6:40-45. By checking in step 124 whether “5-microseconds” have elapsed in connection with the storage request (red), *Miesterfeld*’s process determines whether a value has been reached in association with the storage request. Because the countdown to 5 microseconds begins as soon as the SRAD signal line is determined to be low, the value (a timeout) is “tracked since the issuance of the request.” *Id.*

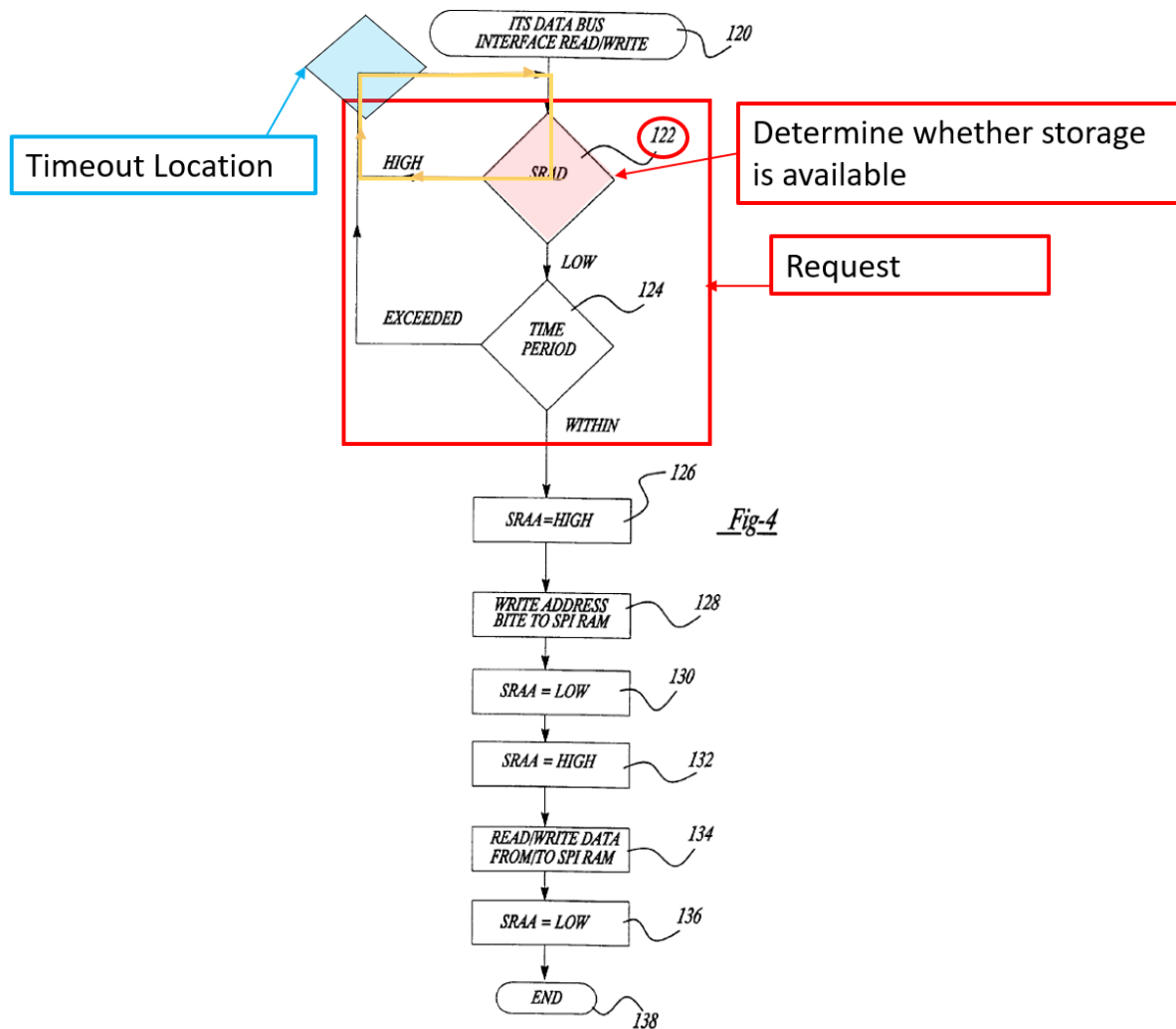


Miesterfeld, FIG. 4 (annotated)

149. It is also my opinion that *Stewart* teaches this feature because *Stewart* teaches a multiprocessor synchronization method in which a “bounding wait time” (threshold value) is implemented to “guarantee that tasks will get the data they require on time, every time.” *Stewart*, 330. *Stewart* also teaches implementing a

“time-out mechanism” (another type of value) for preventing data transfer when a “pre-specified time or number of retries” elapses. *Stewart*, 330 (emphasis added).

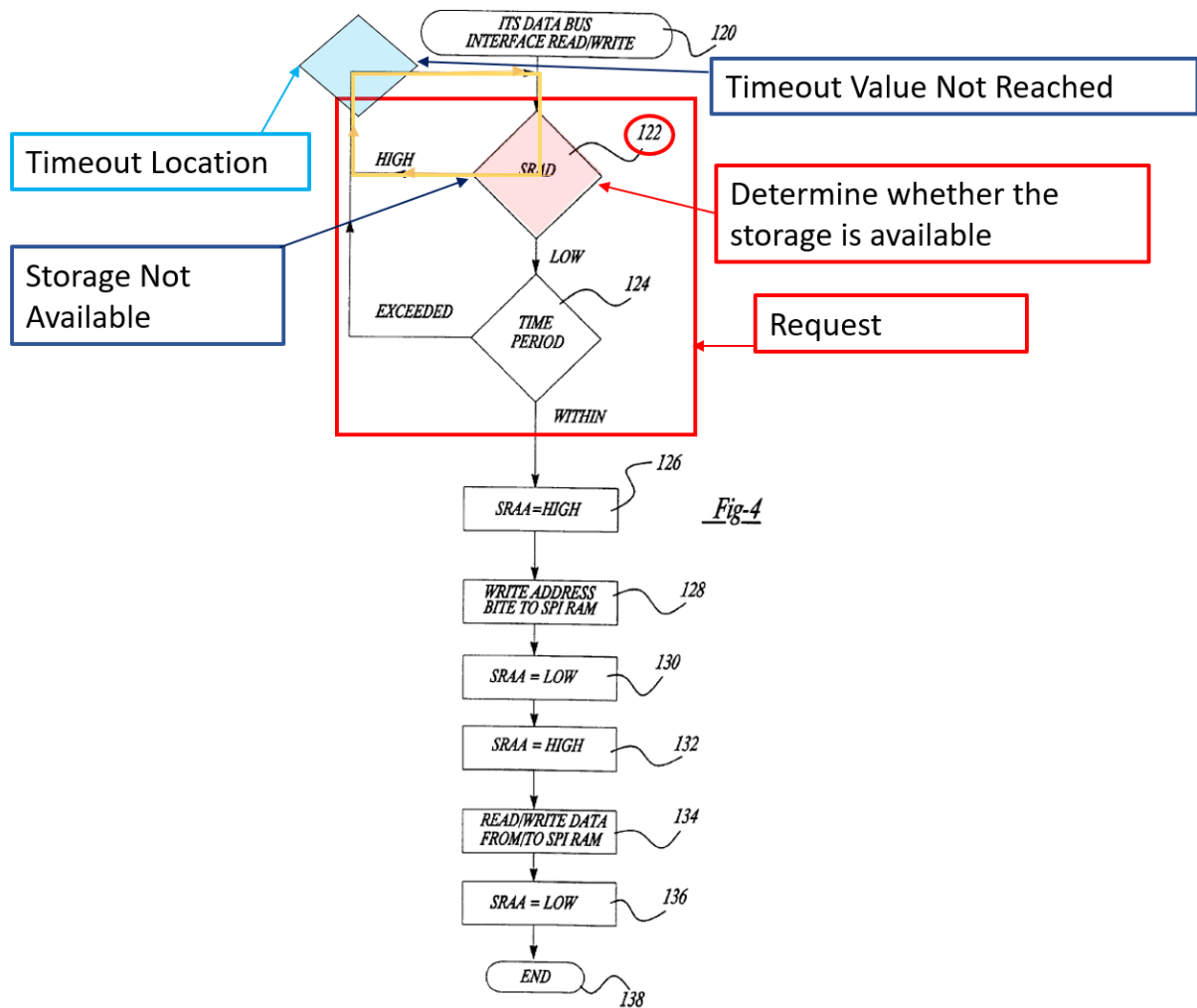
150. In my opinion, it would have been obvious to a POSITA to modify *Miesterfeld*’s process to implement a timeout value (blue) in the logical loop (yellow) as illustrated in annotated Fig. 4 below to ensure timely and consistent data exchange.



Miesterfeld, FIG. 4 (annotated)

Claim 9[g]: “in the event the storage included in the automotive electronic control unit is determined, in response to issuing the request, to not be available and the value tracked since the issuance of the request has not been reached, issuing, by the at least one hardware processor to the storage included in the automotive electronic control unit, another request to access the storage included in the automotive electronic control unit to store the sensor information”

151. In my opinion, *Miesterfeld* discloses repeating the storage request if SRAD is high (issuing another storage request when the storage is “not available.” *Miesterfeld*, Fig. 4. As discussed above in element 9[f], Stewart's timeout operates by preventing data transfer if the number of retries has not been exceeded; thus, the combination is such that *Miesterfeld*'s request repeats if a “pre-specified” number of retries have not elapsed. *Stewart*, 330.



Miesterfeld, FIG. 4 (annotated)

Claim 9[h]: “in the event the storage included in the automotive electronic control unit is determined, in response to issuing the another request, to not be available and the value tracked since the issuance of the request has been reached, sending an error notification; and”

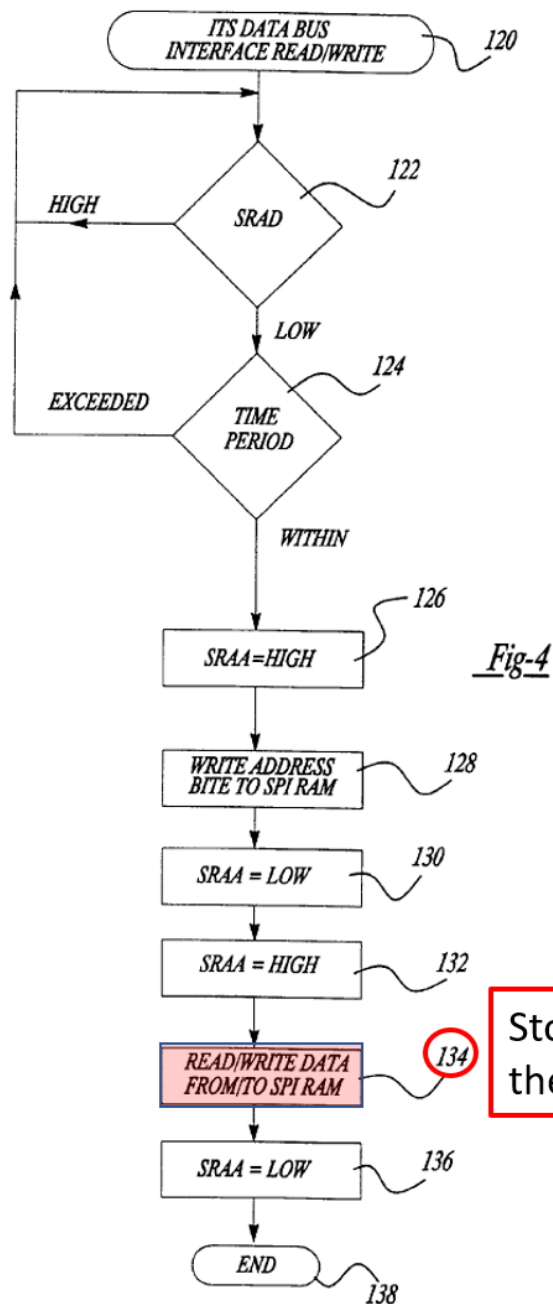
152. *Miesterfeld* in combination with *Stewart* teaches sending an error notification when the threshold is reached. *Stewart* discloses that “error handlers should be installed to detect tasks that suffer successive time-out errors.” *Stewart*, 330.

153. In my opinion, a POSITA would have understood that *Stewart*'s error handlers not only detect the error but that the use of "error handlers" discloses or render obvious error notification as is well known in the art. Indeed, a POSITA would have understood that error detection without notification is useless and would have found it obvious for the error handlers to do so. Such notification may have been embodied as an exit code or error message.

154. It would have been further obvious to a POSITA to modify *Miesterfeld*'s system to incorporate an error notification by providing an exit code or an error message, as at least suggested by *Stewart*, when a timeout occurs and if the storage is not available. Ex-1012, 137-38, 149-51, 154-56 (explaining that using a timeout to prevent deadlock (which could lead to program failure) was well-known in the art).

Claim 9[i]: "in the event the storage included in the automotive electronic control unit is determined, in response to issuing the request or the another request, to be available, storing the sensor information utilizing the storage;"

155. *Miesterfeld* discloses storing the information using the shared memory if the memory is available. *Miesterfeld* discloses that the ITS data bus stores data in the SPI RAM (shared memory/storage) after the "ITS data bus interface 58 determines that the SPI RAM 64 is available," and sets the SPI RAM Access Required (SRAA) signal line to high. *Miesterfeld*, 6:40-54.



Store the information in
the storage

Miesterfeld, FIG. 4 (annotated)

Claim 9[j]: “wherein the automotive electronic control unit is operable such that the sensor information is capable of being

transmitted in less than one second using a second network protocol associated with a second network, and”

156. *Miesterfeld* further discloses that the information is *capable* of being transmitted using a second network protocol associated with the VDB (second network) *Miesterfeld*, 3:59-4:10 (explaining that the VDB transmits data using the J1850 configuration “or any other industry standard as may be required.”). *Miesterfeld* discloses that “the time period between selecting the desired memory page and reading/writing data to SPI RAM 64 (between steps 130 and 132) is less than 5 microseconds” (*id.*, 6:60-63, Fig. 4) and VDB interface may transmit any data received from the ITS data bus within 40 milliseconds. *Id.*, 8:51-56. Thus, in my opinion, *Miesterfeld* discloses that the data is capable of being transmitted in less than one second.

Claim 9[k]: “where the first network is one of a Controller Area Network, a Flexray network, or a Local Interconnect Network, and the second network is another one of the Controller Area Network, the Flexray network, or the Local Interconnect Network.”

157. *Miesterfeld* further discloses that the buses are heterogeneous. *Miesterfeld*, 4:5-10, 9:55-57(explaining that the VDB can be one type of network and the ITS data bus may be another type of network). In my opinion, *Miesterfeld* at least suggests that the first network is at least one of a Controller Area Network (CAN), a Flexray network, or a Local Interconnect Network (LIN) because the ITS

data bus 24 may be “any of a number of ITS data buses, such as D₂B, USB, IDB, Firewall, and the like” *Id.* 9:55-57 (emphasis added). *Miesterfeld* also suggests that the second network is another one of the CAN, LIN or Flexray network because the VDB 14 may be “configured to implement the J1850 configuration as prescribed by the Society of Automotive Engineers (SAE) or any other industry standard as may be required.” *Id.*, 4:7-10 (emphasis added).

158. To the extent further clarification is required, *Wense* teaches that cars utilize “[s]everal multiplex protocols,” including CAN (e.g., for engine control and body control networks), FlexRay (e.g., for safety control, braking, and steering systems), and LIN (e.g., for cost critical distributed body electronics). *Wense*, 11.

159. In my opinion, a POSITA would have found it obvious to implement *Miesterfeld*’s VDB and ITS using known bus architectures like CAN, FlexRay, or LIN, as taught by *Wense*, because each was a commonly-used and well-known vehicle data bus for controlling the various vehicle systems of *Miesterfeld*. *Wense*, 11; *Miesterfeld*, 4:7-10. Ex-1020, ¶¶31, 40, 48 (explaining that concurrent use of legacy bus architectures such as CAN, LIN, FLEXRAY “provides for the total integration of vehicle systems and functions, and permits plug-and-play device integration, scalability and upgradeability.”); Ex-1021, 1:21-32; Ex-1004, 2 (“[t]he automotive industry has developed the [CAN] [] in the 1980s and subsequently

added new communication bus systems such as MOST, IDB, LIN, and FlexRay.”).

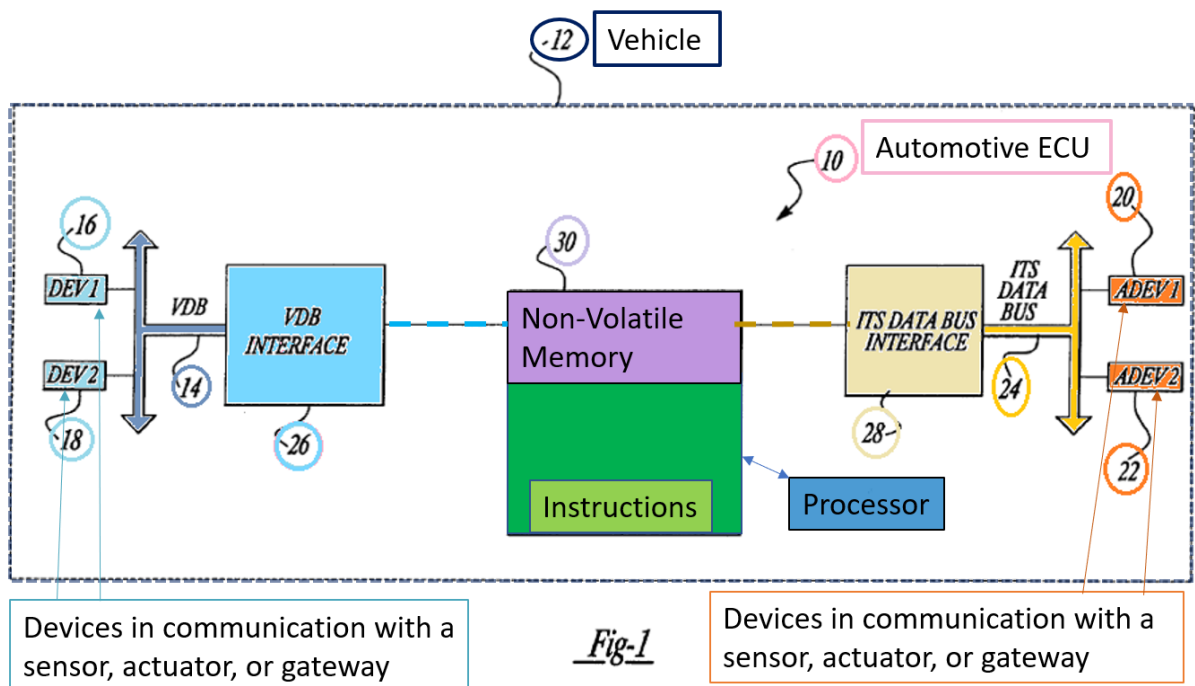
Claim 10: “The apparatus as recited in claim 9, wherein the apparatus is operable such that network layer translation is capable of being avoided.”

160. *Miesterfeld* discloses that network layer translation is avoidable because *Miesterfeld* uses data lines to read and output data. *Miesterfeld*, 5:20-31. *Miesterfeld* discloses that VDB interface 62 communicates with SPI RAM 64 through a pair of data lines 66a, 66b, and a serial clock line 66c to define SPI bus 66. *Id.*, 5:20-22. Line 66a is a master-in-slave-out (MISO) data line that enables a master device to read data from the slaved SPI RAM 64, data line 66b is a master-out-slave-in (MOSI) data line that enables a master device to output data to the slaved SPI RAM 64, and the VDB and ITS data bus interfaces each function as master devices with respect to slaved device SPI RAM 64. *Id.*, 5:22-31. In my opinion, a POSITA would have understood that *Miesterfeld*’s system translates between VDB and ITS buses without network layer translation because it uses bus lines which do not need to use network level addresses.

Claims 11 and 12: “The apparatus as recited in claim 9, wherein the apparatus is configured for sharing automotive sensor data received via the first network for use in connection with an

automotive device on the second network, in less than the one second [a millisecond].”

161. *Miesterfeld* further discloses that the ITS data bus (first network) shares data for use “in connection with” automotive devices (16, 18) on the VDB (second network). *Miesterfeld*, Fig. 1; 3: 19-24 (“To effect such an exchange, a vehicle data bus (VDB) interface 26 reads and writes data from VDB 14. VDB interface 26 enables the exchange of data between memory 30 and VDB 14. Similarly, ITS data bus interface 28 enables data exchange between memory 30 and ITS data bus 24.”). The data corresponds to “sensor data” for reasons set forth in element 1[a].



Miesterfeld, FIG. 1 (annotated)

162. The information is shared in less than one second or millisecond because, as discussed in element 9[j], *Miesterfeld* discloses that “the time period between selecting the desired memory page and reading/writing data to SPI RAM 64 (between steps 130 and 132) is less than 5 microseconds.” *Id.*, 6:60-63, Fig. 4.

Claims 13 and 14: “The apparatus as recited in claim 9, wherein the apparatus is operable such that the request and the another request are identical [the same].”

163. As explained for 9[g], *Miesterfeld* discloses repeating the storage request process (issuing “another request”) if SRAD is high (“when the storage is not available”). *Miesterfeld*, Fig. 4, 6:33-43. This is the exact procedure described in the ’179 patent’s specification. Ex-1001, 10:12-14 (“If the resource is not available, it may try it again after a waiting period (1011) until the resource is available.”). Thus, in my opinion, a POSITA would have understood that *Miesterfeld* discloses that “the another request” is identical to, or the same as, “the request” for the same reasons as the ’179 patent.

Claim 17: “The apparatus as recited in claim 9, wherein the apparatus is operable such that the storage includes a bulletin board.”

164. *Miesterfeld* discloses that “[m]emory 30 is accessible to both VDB interface 26 and ITS data bus interface 28 so that each interface will be able [to] read from and/or write to memory 30.” *Miesterfeld*, 3:40-43. That is, any network connected to ITS gateway 10 has access to memory 30 and can store data in or

retrieve data from the database stored there. In my opinion, a POSITA would have understood that *Miesterfeld*'s database is a "bulletin board" because it enables devices on different networks to read and write data to the database in the memory. *Miesterfeld*, 3:18-4:31.

Claims 18-20: "The apparatus as recited in claim 9, wherein the apparatus is operable such that the error notification is sent, when the storage included in the automotive electronic control unit is determined, in response to issuing the [another] request, to not be available and the value tracked since the issuance of the request has been reached."

165. As explained for 9[g] and 9[h], *Stewart* discloses that "error handlers should be installed to detect tasks that suffer successive time-out errors." *Stewart*, 330. Such successive timeouts occur after sending repeated requests ("another request"). *Id.* In my opinion, a POSITA would have understood that error detection (via error handlers) is useless without a notification, and therefore, would have understood *Stewart*'s error handlers to both detect and provide notice of the error.

166. In my opinion, it would have been obvious to a POSITA to modify *Miesterfeld* to send an error notification by providing an exit code or an error message if the storage is not available and when a timeout occurs (i.e., when another request is submitted that exceeds the predetermined value/timeout). Ex-1012, 137-38, 149-51, 154-56 (explaining that using a timeout to prevent deadlock (which could lead to program failure) was well-known in the art).

4. Ground 7: Claims 15 and 16 obvious are over *Miesterfeld* in view of *Wong, Stewart, Wense and Ma*

Claims 15 and 16: “The apparatus as recited in claim 9, wherein the apparatus is operable such that the sensor information excludes all [at least a portion of any] header bits of the message.”

167. In my opinion, a POSITA would have understood or found it obvious that *Miesterfeld*’s sensor information excludes all or at least a portion of any header bits of the message because the International Standards Organization (ISO) which set forth the industry standard for network communication at the time of the invention, required as much to facilitate communication using CAN, LIN, and Flexray networks. Ex. 1019 (establishing a CAN “serial communication protocol that supports distributed real-time control and multiplexing for use within road vehicles” and explaining that the “layered” CAN architecture established by the OSI reference model includes a data link layer and a physical layer (PL) for bit encoding/decoding).

168. To the extent clarification is required, *Ma* discloses that data, as is well known in the communications field, is transmitted in a “packet,” including a data field and header field. *Ma*, 1:14-17. The data field contains “virtually any kind of digital data” and the header field conveys information identifying, e.g., the packet’s source or destination, the protocol to be used to interpret the packet, or the packet’s place in a sequence of packets. *Id.*, 1:18-25. *Ma* further discloses that the

packet headers and their functions are “typically” arranged according to the open-systems inter connection (OSI) reference model in a plurality of hierarchical layers. *Id.*, 1: 28-34. Regarding the first three layers of the hierarchy, *Ma* states:

Layer 1, the physical layer, is concerned with transmission of a bit stream over a physical link. Layer 2, the data link layer, provides mechanisms for the transfer of frames of data across a single physical link, typically using a link-layer header on each frame. Layer 3, the network layer, provides network-wide packet delivery and switching functionality—the well-known Internet Protocol (IP) is a layer 3 protocol.

Id. 1:34-41; see also Ex. 1029, 3, 30 (explaining that the network layer facilitates data transmission across the data link layer.

169. *Ma* further discloses that the packet’s headers are “modified” such that the L2 headers are “stripped” and the backplane header (i.e., the network layer header) is removed when the data packet is received at a network interface. *Ma*, 5:48-61; 11:41-47. *Ma* simply clarifies what a standard data packet configuration includes; thus, it is my opinion that a POSITA would have had a reasonable expectation of success in implementing the OSI Reference model, whereby the information is packaged into a packet of layers, as taught by *Ma*, and that the modification would have required only ordinary skill. Processing the packets in

accordance with the standard, e.g., by removing header bits, would have been routine for the same reasons.

170. In my opinion, it would have been obvious to a POSITA to configure *Miesterfeld*'s apparatus to transmit sensor information using the OSI Reference model, whereby the information is packaged into a packet of layers including header bits and the header bits are stripped from the packet (message) upon receipt, as taught by *Ma*, to facilitate data transfer (sensor information transfer) and provide network-wide packet delivery. This configuration would have ensured compliance with the ISO and OSI reference model. *Id*; Ex 1022, 2:63-3:7 (explaining that "headers are removed and data processed in order from the lowest (Physical) layer to the highest (Application) layer" when data packets are received). Because the data being transmitted in the instant combination is sensor information, it is my opinion that a POSITA would have understood that the portion of a message that is sensor information excludes all header bits of the message.

171. Because "at least a portion of any header bits of the message" is excluded if "all header bits of the message" are excluded, claim 16 is obvious for the same reasons as claim 15.

5. Ground 8: Claims 21-24 and 27 are obvious over *Miesterfeld* in view of *Wong* and *Stewart*.

Independent Claim 21

172. As explained in Ground 3, Independent claim 21 largely mirrors independent claim 9. Thus, it is my opinion that claim 21 is obvious over *Miesterfeld* in view of *Wong* and *Stewart* for the reasons explained for independent claim 9 in Ground 6.

Dependent Claims 22-24 and 27

173. Dependent claims 22-24 mirror dependent claims 2, 3, and 5, respectively. *Miesterfeld* discloses the claimed features for the same reasons discussed above in Ground 5. Dependent claim 27 mirrors dependent claim 12. *Miesterfeld* discloses the claimed features for the same reasons discussed above in Ground 6.

6. Ground 9: Claims 25 and 26 are obvious over *Miesterfeld* in view of *Wong*, *Stewart*, and *Wense*.

174. Dependent claim 25 mirrors dependent claims 5 and 24 but further requires the first Network to be one of a Controller Area Network, a Flexray network, or a Local Interconnect Network, and the second network is another one of the Controller Area Network, the Flexray network, or the Local Interconnect Network, which *Wense* already discloses as discussed in claim element 9[k]. Thus, in my opinion, claim 25 is obvious for the same reason as claim 24 and 9[k].

175. Dependent claim 26 requires “the transmitting” to be “completed in less than a millisecond” and therefore encompasses the same scope as claim 25 and is obvious for the same reasons.

XI. CONCLUSION

176. As discussed above, it is my opinion that the Challenged Claims are obvious over the above cited references.

177. I reserve the right to supplement my opinions in the future to account for new information as it becomes available to me.

178. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on this Dec 30, 2022, in Johns Creek, GA

By: 
Dr. Vijay K. Madiseti