

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED,

Petitioner,

v.

ALIDDOUBLE, INC.

Patent Owner.

U.S. Patent No. 9,356,169

PETITION FOR *INTER PARTES* REVIEW

OF U.S. PATENT NO. 9,356,169

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EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 9,356,169 (“the ’169 Patent”)
1002	Prosecution File History for the ’169 Patent
1003	Declaration of Dr. Konstantinos P. Giapis
1004	U.S. Patent No. 7,498,650 (“Lauxtermann”)
1005	S. Zucca et al, <i>Monolithic Pixel Sensors for Fast Particle Trackers in a Quadruple Well CMOS Technology</i> , 2012 IEEE Nuclear Science Symposium and Medical Imaging Conference Record (“Zucca”)
1006	U.S. Patent No. 8,076,172 (“Akiyama”)
1007	J. Ballin et al, <i>Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixels</i> , Sensors 2008 (“Ballin”)
1008	U.S. Patent No. 8,723,284 (“Hynecek”)
1009	U.S. Patent App. Pub. No. 2010/0159632 (“Rhodes”)
1010	U.S. Patent No. 8,531,565 (“Wang”)
1011	U.S. Patent No. 7,944,012 (“Turchetta”)
1012	Coath et al, <i>Advanced Pixel Architectures for Scientific Image Sensors</i> , Proceedings of the 2009 Topical Workshop on Electronics for Particle Physics (“Coath I”)
1013	Coath et al, <i>A Low Noise Pixel Architecture for Scientific CMOS Monolithic Active Pixel Sensors</i> , 2009 IEEE Nuclear Science Symposium Conference Record (“Coath II”)
1014	U.S. Patent No. 7,710,477 (“Nam”)

Exhibit No.	Description
1015	Battiato et al, <i>Image Processing for Embedded Devices</i> , 2010 (“Battiato”)
1016	Heddle, <i>Electrostatic Lens Systems</i> , 2nd ed, 2000 (“Heddle”)
1017	U.S. Patent No. 8,921,803 (“Welkie”)
1018	U.S. Patent No. 6,770,889 (“Iwasawa”)
1019	U.S. Patent Appl. Pub. No. 2011/0101201 (“Venezia”)
1020	U.S. Patent No. 7,505,206 (“Deng”)
1021	U.S. Patent App. Pub. No. 2013/0270663 (“Lin”)
1022	International Patent App. Pub. No. WO 2007/025102 (“Li”)
1023	U.S. Patent App. Pub. No. 2012/0038014 (“Tai”)
1024	Sze & Lee, <i>Semiconductor Devices: Physics and Technology</i> , 3rd ed, 2012 (“Sze&Lee”)
1025	Sze & Ng, <i>Physics of Semiconductor Devices</i> , 3rd ed, 2006 (“Sze&Ng”)
1026	U.S. Patent No. 8,736,006 (“Tsai”)
1027	U.S. Patent Appl. Pub. No. 2013/0203208 (“Shinohara”)
1028	E. R. Fossum and D. B. Hondongwa, “A review of the pinned photodiode for CCD and CMOS image sensors,” <i>IEEE J. Electron Devices Soc.</i> , vol. 2, no. 3, pp. 33-43, May 2014 (“Fossum I”)
1029	U.S. Patent No. 5,903,021 (“Lee”)
1030	https://en.wikipedia.org/wiki/Back-illuminated_sensor
1031	U.S. Patent No. 6,168,965 (“Malinovich”)

Exhibit No.	Description
1032	E.R. Fossum, “Active Pixel Sensors: Are CCD's Dinosaurs?,” Proc. SPIE 1900, Charge-Coupled Devices and Solid State Optical Sensors III, (July, 1993) (“Fossum II”)
1033	Y. Kohyama et al., “A 1.4 μm Pixel Backside Illuminated CMOS Image Sensor with 300 mm Wafer Based on 65 nm Logic Technology,” International Image Sensor Workshop (IISW), 2009.
1034	S. Iwabuchi, et al., “A back-illuminated high-sensitivity small-pixel color CMOS image sensor with flexible layout of metal wiring”, Proc. IEEE Int. Solid State Circuits Conf.-Dig. Tech. Papers, pp. 1171-1178, Feb. 2006.
1035	N. Teranishi et al., “Evolution of optical structure in image sensors”, IEDM Tech. Dig., pp. 24, Dec. 2012.
1036	Y. Kitamura et al., “Suppression of crosstalk by using back-side deep trench isolation for 1.12 μm back-side illuminated CMOS image sensor”, 2012 International Electron Devices Meeting, pp. 24.2.1-24.2.4, 2012.
1037	“Digital camera,” <i>Encyclopedia Britannica</i> (https://www.britannica.com/technology/digital-camera)
1038	https://www.tel.com/museum/exhibition/principle/cmos.html
1039	Boyd Fowler, X. Liu, P. Vu, “CMOS image sensors – past, present and future”, Proceedings ICIS 2006 – International Congress of Imaging Science (2006) (“Folwer”).
1040	L. J. Kozlowski, et al, “Comparison of passive and active pixel schemes for CMOS visible imagers,” Proc. SPIE 3360, Infrared Readout Electronics IV (September, 1998) (“Kozlowski”)
1041	U.S. Patent No. 8,063,963 (“Dierickx”)

Exhibit No.	Description
1042	E. R. Fossum “CMOS Image Sensors: Electronic Camera-On-A-Chip,” <i>IEEE Transactions on Electron Devices</i> , no. 10, pp. 1689-98, Oct. 1997
1043	U.S. Patent No. 9,257,479 (“Koizumi”)
1044	Barbe, F., “A Tradeoff Analysis for CCD Area Imagers: Frontside Illuminated Interline Transfer vs. Backside Illuminated Frame Transfer,” in <i>Procs., CCD Applications Conf.</i> , pp. 13-20 (1973) (“Barbe”)
1045	L. Brissot et al., “High-definition CCDs for enhanced definition television,” in <i>High-Resolution Sensors and Hybrid Systems</i> , SPIE, vol. 1656, pp. 427-436 (Aug. 12, 1992) (“Brissot”)
1046	https://www.photometrics.com/learn/imaging-topics/quantum-efficiency
1047	U.S. Patent No. 5,244,817 (“Hawkins”)
1048	U.S. Patent No. 5,270,221 (“Garcia”)
1049	U.S. Patent No. 5,494,833 (“Martin”)
1050	U.S. Patent No. 8,709,852 (“Hynecek852”)
1051	U.S. Patent No. 8,409,909 (“Nagaraja”)
1052	U.S. Patent No. 8,963,066 (“Sato”)
1053	Declaration of Dr. Sylvia Hall-Ellis
1054	S. Mendis et al., “CMOS Active Pixel Image Sensor”, <i>IEEE Transactions on Electron Devices</i> , vol. 41, No, 3, March 1994.
1055	Stanley Wolf, <i>Silicon Processing for The VLSI Era, Volume 2: Process Integration</i> , 1990.
1056	https://www.dpreview.com/articles/4281372431/sonycmos

Exhibit No.	Description
1057	U.S. Patent No. 8,198,602
1058	R. Aihara, M. Obata, and H. Sawaragi, “Stabilization of An Electrostatic Lens for A Focused Ion Beam System,” <i>Journal of Vacuum Science & Technology B: Microelectronics Processing and Phenomena</i> 6, 958 (1988).
1059	T. Joy, et al., “Development of a Production-Ready, Back-Illuminated CMOS Image Sensor with Small Pixels,” <i>IEDM</i> , pp.1008-1010, 2007
1101	Intentionally omitted
1102	J. Ballin <i>et al.</i> , “Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixels.” <i>Sensors</i> , vol. 8, no. 9, 2008: 5336-5351
1103	Intentionally omitted
1104	S. Zucca <i>et al.</i> , “Monolithic Pixel Sensors for Fast Particle Trackers in a Quadruple Well CMOS Technology.” <i>2012 IEEE Nuclear Science Symposium and Medical Imaging Conference Record (NSS/MIC)</i> , pp. 1742-1749, 2012.

LIST OF CHALLENGED CLAIMS

Claim	Limitation
1pre	A back-side illumination (BSI) complementary metal-oxide-semiconductor (CMOS) pixel array comprising:
1a	a plurality of pixels, a pixel of said plurality of pixels comprising:
1b	one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-well (NW) region or a P-well (PW) region;
1c	a photodiode;
1d	an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and
1e	a barrier layer separating said absorption area from said one or more well regions.
2	The BSI CMOS pixel array of claim 1, wherein said photodiode comprises a low fill factor (FF) diode.
3	The BSI CMOS pixel array of claim 1, wherein said collection area extends from said absorption area to said photodiode through said barrier layer.
4	The BSI CMOS pixel array of claim 1, wherein said collection area is configured to perform the functionality of an electrostatic lens to collect said electrons from said absorption area.
5	The BSI CMOS pixel array of claim 1, wherein said barrier layer is configured to prevent diffusion of said electrons from said absorption area to said well regions.

Claim	Limitation
6	The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 4 micron (um).
7	The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 10 micron (um).
8	The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 15 micron (um).
9	The BSI CMOS pixel array of claim 1, wherein a resistivity of said epi layer is greater than 100 ohm to centimeter (ohm-cm).
10	The BSI CMOS pixel array of claim 1 comprising a micro lens, said absorption area is between said micro lens and said barrier layer.
11	The BSI CMOS pixel array of claim 10 comprising an anti-reflective coating (ARC) layer, said ARC layer is between said micro lens and said absorption area.
12	The BSI CMOS pixel array of claim 1, wherein said one or more MOS transistors comprise one or more transistors selected from a group consisting of one or more P-type MOS (PMOS) transistors and one or more N-type MOS (NMOS) transistors.
13	The BSI CMOS pixel array of claim 1, wherein said barrier layer comprises a deep PW implant.
14	The BSI CMOS pixel array of claim 1, wherein said barrier layer comprises a boron implant.
15	The BSI CMOS pixel array of claim 1, wherein said photodiode comprises a fully pinned diode.
16pre	A complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) comprising:
16a	a circuitry; and
16b	a back-side illumination (BSI) pixel array comprising:

Claim	Limitation
16c	a plurality of pixels, a pixel of said plurality of pixels comprising:
16d	one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-well (NW) region or a P-well (PW) region;
16e	a photodiode;
16f	an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to said absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and
16g	a barrier layer separating said absorption area from said well regions.
17	The CMOS IC of claim 16 comprising a guard ring separating said circuitry from said BSI pixel array.
18	The CMOS IC of claim 17, wherein said guard ring is configured to prevent diffusion of photoelectrons from said circuitry to said BSI pixel array.
19pre	An imaging device comprising:
19a	a memory; an input; an output; a processor; and
19b	a complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) comprising:
19c	a circuitry; and
19d	a back-side illumination (BSI) pixel array comprising:
19e	a plurality of pixels, a pixel of said plurality of pixel sensors comprising:

Claim	Limitation
19f	one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-well (NW) region or a P-well (PW) region;
19g	a photodiode;
19h	an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to said absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and
19i	a barrier layer separating said absorption area from said well regions.
20	The imaging device of claim 19 comprising a digital camera or a Smartphone.

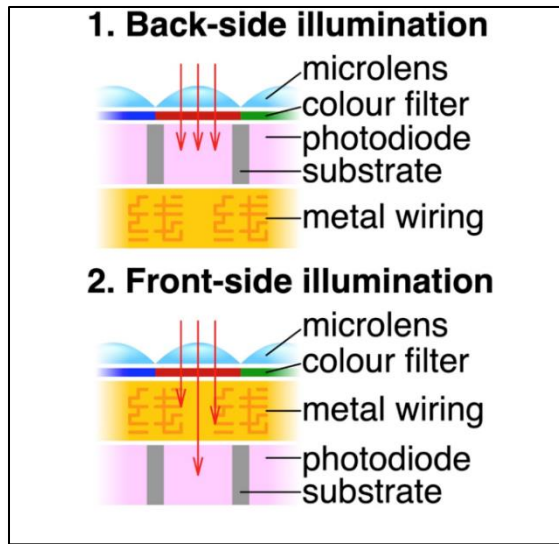
I. INTRODUCTION

Taiwan Semiconductor Manufacturing Company Limited (“TSMC” or “Petitioner”) respectfully requests *inter partes review* of claims 1-20 (“the Challenged Claims”) of U.S. Patent No. 9,356,169 (“the ’169 patent”) pursuant to 35 U.S.C. § 311 and 37 C.F.R. § 42.100.

II. BACKGROUND OF THE TECHNOLOGY

Complementary metal-oxide semiconductor (“CMOS”) image sensors (“CIS”) are ubiquitous in today’s electronic devices, such as digital cameras. *See* Ex. 1031; Ex. 1032 at 1. These devices use CMOS sensors to measure light intensity and color. Ex. 1037; Ex. 1003, ¶¶33-35. A CIS includes a pixel array, where each pixel has a photodetector, antireflective coating, and microlens. Ex. 1038; Ex. 1003, ¶¶34-35.

A CIS may either be frontside illuminated (FSI) or backside illuminated (BSI). Ex. 1044, 1. The difference between a BSI image sensor and an FSI image sensor is the arrangement of imaging elements in the sensor with respect to incident light to the pixel. Ex. 1003, ¶¶41-42.



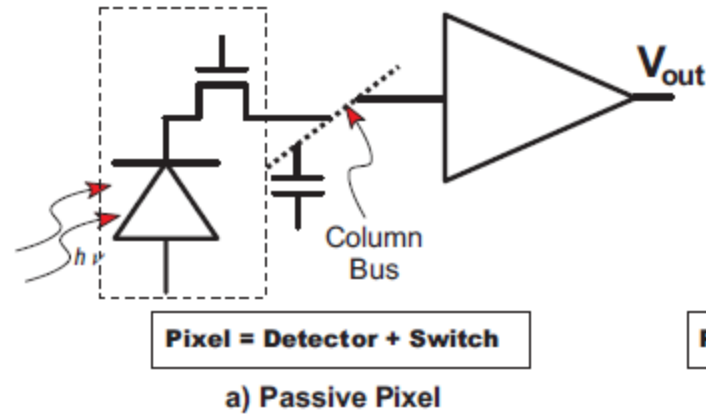
Ex. 1030.

BSI has better imaging performance than FSI because BSI allows the image sensors to achieve higher quantum efficiency. Ex. 1046; Ex. 1047, 1:10-11; Ex. 1048, 4:7-11; Ex. 1049, 2:26-30; Ex. 1003, ¶43.

A. Pixels

1. Passive Pixel Sensors

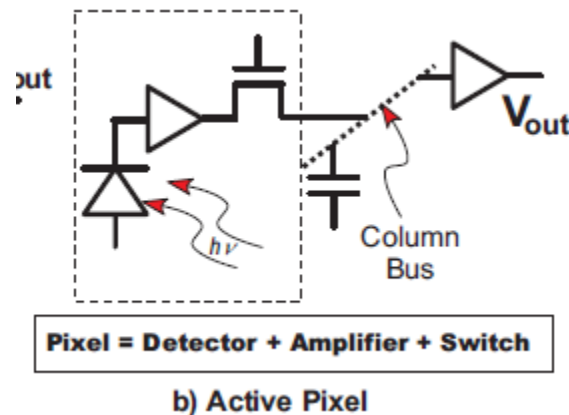
The first MOS integrating solid stage image sensor was developed in 1967 with a MOS passive pixel architecture. Ex. 1039, 135. This architecture uses a reverse biased photodiode connected to a single p-channel MOS transistor to individually access each pixel in a linear array. *Id.* Passive pixels are read out without pixel-based amplification. Ex. 1003, ¶36.



Ex. 1040, FIG. 2(a).

2. Active Pixel Sensors (APS)

After the development of MOS passive pixel architectures, MOS *active* pixel architecture was proposed. A MOS active pixel architecture incorporates transistors in each pixel to amplify the signal voltage. Ex. 1039, 135; Ex. 1003, ¶37.



Ex. 1040, FIG. 2(b).

APS sensors are less sensitive to noise fluctuations due to their pixel-based amplification. Ex. 1041, 1:45-51. APS technology allows for a higher fill factor while maintaining sensitivity, noise, and dynamic range. *Id.*; Ex. 1003, ¶¶38-39.

3. In-Pixel Processing

In-pixel processing embeds processing capabilities within the individual APS pixels, which often requires the use of fully complementary MOS transistors (i.e., both PMOS and NMOS). Ex. 1012, 57. However, adding PMOS transistors to APS pixels creates parasitic effects as a result of the formation of parasitic p-n junctions, which reduce the overall amount of charge collected by the photodiode. Ex. 1012 at 57, FIG. 1. To avoid this parasitic p-n junction issue, one solution is to add an additional deep p-well layer underneath the n-wells of the PMOS transistor as a barrier layer to prevent the parasitic n-wells from collecting electric charges. Ex. 1012, 57-58, FIG. 2; Ex. 1013, 1311, FIG. 2; Ex. 1011, [0032], Fig. 6; Ex. 1003, ¶¶40.

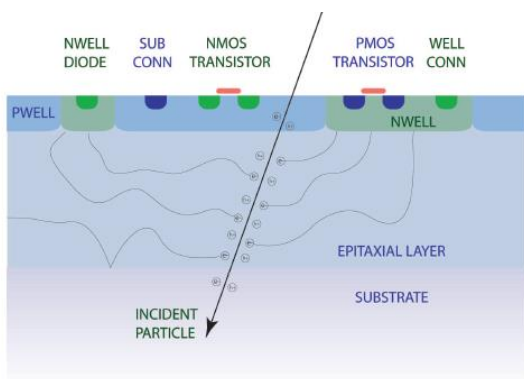


Figure 1: Cross-Section of a Typical CMOS Pixel

Ex. 1012, FIG. 1

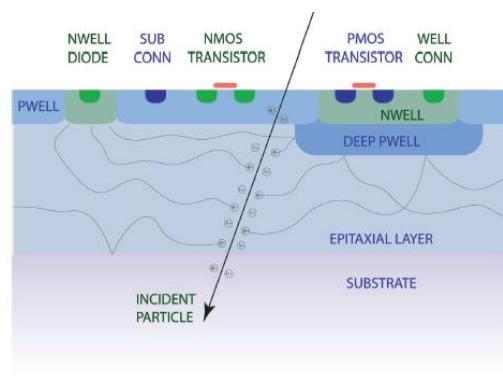


Figure 2: Cross-Section of a Typical CMOS Pixel Showing Addition of INMAPS Deep P-Well Layer

Ex. 1012, FIG. 2

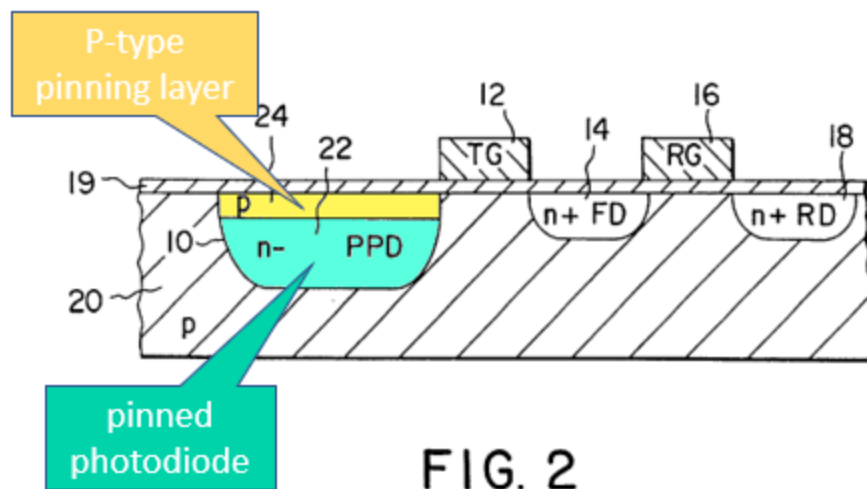
B. Photodiodes

A standard CMOS APS pixel contains a photodetector called a pinned photodiode (“PPD”). Ex. 1028, 35. PPDs were first used in BSI CMOS image

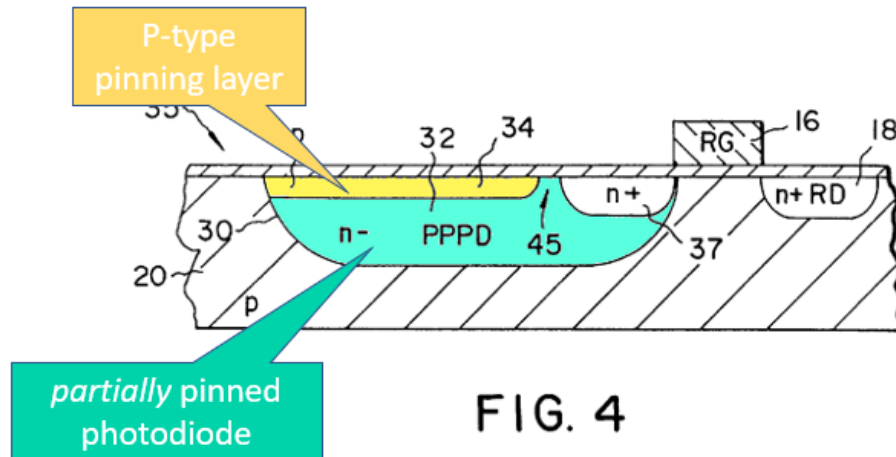
sensors in the late 1990s, and “[m]ass-production of BSI PPD CMOS image sensors [was] routine” by 2014. *Id.*, 35-36; Ex. 1003, ¶¶59-63.

1. Pinned photodiode

A photodiode may be pinned, partially pinned, or unpinned. A pinned photodiode has a p⁺ pinning layer that covers the photodiode while a partially pinned photodiode has an n⁺ region in an area of the photodiode not covered by the p⁺ pinning layer, as shown below. Ex. 1029, 3:61-4:5, 4:32-67; Ex. 1003, ¶¶59-63.



Ex. 1029, FIG. 2.



Ex. 1029, FIG. 4.

2. 4T Pixel

The integration of the pinned photodiode (“PPD”) with CMOS APS is often referred to as the “4T” pixel because the pixel has four (4) transistor gates. Ex. 1028, 35. A CMOS APS 4T pixel architecture typically consists of a pinned photodiode (PPD), a floating diffusion (FD) node, and four transistors: a transfer gate (TG) transistor, a reset (RST) transistor, a source follower (SF) transistor, and a row select (SEL) transistor. *Id.* 35, FIG. 3.

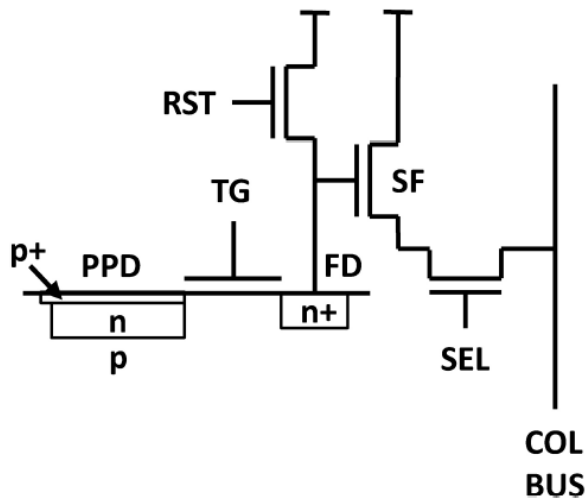


Fig. 3. Schematic of CMOS APS pixel with PPD.

Ex. 1028, FIG. 3; Ex. 1003, ¶¶64-65.

In contrast, a “3T” pixel refers to a CMOS APS pixel where the photodiode is directly connected to the SF transistor and the photodiode may be a partially pinned photodiode. Ex. 1028, 35; Ex. 1003, ¶64.

C. ARC and Microlens

ARC: Another well-known component of BSI CMOS image sensors is anti-reflective coatings (ARCs). The use of an ARC “allows light to pass through from a lens to the photodiode while minimizing reflection that would decrease the efficiency of the device.” Ex. 1021, [0013]. BSI CMOS sensors “typically” include one or more ARCs behind the microlenses. Ex. 1023, [0042]; Ex. 1021, [0025]-[0026]; Ex. 1003, ¶¶54-55.

Microlens: It was well-known that microlenses can be used to focus lights on the photodiode of a pixel, thereby “boost[ing the] effective fill factor (i.e., the ratio

of the active refracting area to the total area occupied by the lens array)” of the photodiode, and improving sensitivity of the pixel. Ex. 1015, 11. Therefore, microlens arrays are widely employed in image sensor technology, such as CMOS image sensors. Ex. 1020, 1:6-11; Ex. 1003, ¶¶52-53.

III. BACKGROUND OF THE ’169 PATENT

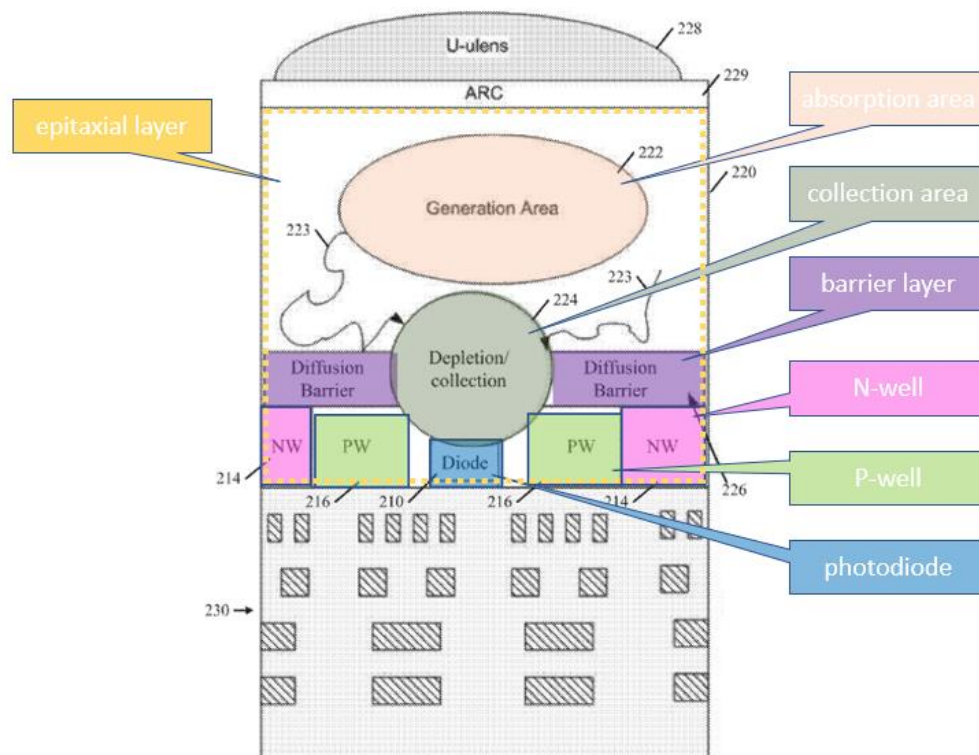
A. The ’169 Patent

The ’169 patent is directed to “Back-Side Illumination (BSI)” complementary metal-oxide-semiconductor (CMOS) pixel array. Ex. 1001, 1:16-19. The ’169 patent discloses a CMOS pixel that includes a photodiode and in-pixel processing transistors. *Id.*, 3:30-33, 4:9-40. As the specification states, a pixel would have poor collection efficiency if photogenerated electrons are absorbed not by the photodiode but by well regions (specifically, the n-well regions) of the transistors, which act as parasitic photodiodes. *Id.*, 4:41-61. The ’169 patent purports to address this issue by placing a barrier layer below the transistor well regions to prevent the photogenerated electrons from diffusing to the transistor well regions. *Id.*, 5:57-60, 6:57-60; Ex. 1003, ¶24.

The ’169 patent discloses a BSI CMOS image sensor pixel, as shown in FIG. 2 below¹, that includes: (1) one or more MOS transistors with one or more well

¹ Coloration and annotations added to figures unless otherwise noted.

regions (N-well 214 and/or P-well 216), (2) a photodiode 210, (3) an epitaxial layer 220 with an absorption area 222 and a collection area 224, the latter of which connects absorption area 222 to photodiode 210, and (4) a barrier layer 226 separating absorption area 222 from the one or more well regions to prevent diffusion of electrons to the one or more well regions. Ex. 1001, Abstract, FIGs. 1 and 2; Ex. 1003, ¶25.



Ex. 1001, Fig. 2.

The '169 patent explains that in some embodiments the photodiode (PD) may be a low fill factor PD. *Id.*, 3:64-4:8; 8:15-18. The photodiode can be fully pinned (see, e.g., *id.*, 3:37-38, 9:7-8), non-pinned (see, e.g., *id.*, 3:39-40, 9:11-13), or any other diode such as a partially pinned diode (*id.*, 3:41-42); Ex. 1003, ¶26.

B. Prosecution History

The '169 patent was filed on July 6, 2015, claiming priority to Provisional Application No. 62/021,152 filed on July 6, 2014. Ex. 1001.

In a Notice of Allowability issued on January 20, 2016, the Examiner allowed all original claims without discussion of any prior art. Ex. 1002, 46-49.

IV. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) at the time of the alleged invention would have been a person having a Master’s degree in electrical engineering, material science, physics, or other related disciplines with at least three years of industry experience in integrated circuit design, layout, packaging or fabrication. A greater level of experience may compensate for less education and vice versa. Ex. 1003 ¶¶66-68.

V. CLAIM CONSTRUCTION

For purposes of this proceeding only, Petitioner does not believe the claim terms need to be construed to resolve the prior art issues presented in this Petition. The challenged claims are invalid under their plain and ordinary meaning. Ex. 1003 ¶70.

VI. STATUTORY GROUNDS OF CHALLENGE

Petitioner requests *inter partes* review and cancelation of the challenged claims on the following grounds:

Grounds	Claims	Statutory Basis	Prior Art
1	1-6, 10-15	§103	Lauxtermann
2	2, 6-7, 9	§103	Lauxtermann in view of Zucca
3	10, 11	§103	Lauxtermann in view of Akiyama
4	16-20	§103	Lauxtermann in view of Wang
5	1, 3-8, 12-15	§103	Ballin
6	10, 11	§103	Ballin in view of Akiyama

None of the above references relied upon were before or considered by the Examiner during prosecution of the '169 patent. Further, none of the grounds in this Petition rely on prior art combinations that were evaluated during prosecution.

The grounds are not duplicative of each other. Grounds 1-4 rely on Lauxtermann as the primary reference. To the extent Patent Owner argues that Lauxtermann does not render obvious an epitaxial layer with a thickness of 10 or 15 microns, that aspect of the claims is expressly disclosed by Ballin, the primary reference for grounds 5-6.

VII. OVERVIEW OF CITED PRIOR ART

A. Lauxtermann

Lauxtermann is directed to BSI CMOS image sensors with pinned photodiodes. Ex. 1004, 1:6-9. Lauxtermann identifies that one of the drawbacks of BSI CMOS image sensors is that the pinned photodiode collects only a small fraction of the photogenerated charges. This is because some of the charges diffuse not only towards the pinned photodiode but also towards active pixel circuitry within the pixel. *Id.*, 4:56-62.

Ex. 1004, FIG. 4.

B. Ballin

Ballin is a printed publication. As set forth in the accompanying declaration of Dr. Hall-Ellis, Ballin qualifies as a printed publication because it was published in a September 2008 edition of the journal *Sensors* available to the public in the National Library of Medicine in Bethesda Maryland. Ex. 1053, ¶¶57-64. Further supporting the public availability of these proceedings is that a copy of Ballin is available from the publisher's website, the National Library of Medicine, and the digital repositories *ResearchGate* and *Semantic Scholar*. *Id.*, ¶58.

The well-known nature of this and other similar publications by the *Sensors* journal is confirmed by Dr. Giapis. Dr. Giapis states in his declaration that he was aware of the *Sensors* journal and that Ballin, along with the other papers published in the journal would have been readily available as of the publication. Ex. 1003, ¶74.

Ballin is inherently reliable and trustworthy given the well-known publication source, *Sensors*. Ex. 1102. Indeed, the Board has taken “Official Notice that members in the scientific and technical communities who both publish and engage in research rely on information published” in similarly well-known publications. *Ericsson Inc. v. Intellectual Ventures I LLC*, IPR 2014-00527, Paper 41 at 11 (PTAB May 18, 2015). The Board has further found that “[a]llowing IPR petitioners to rely on” publication dates from these well-known sources “serves the interests of

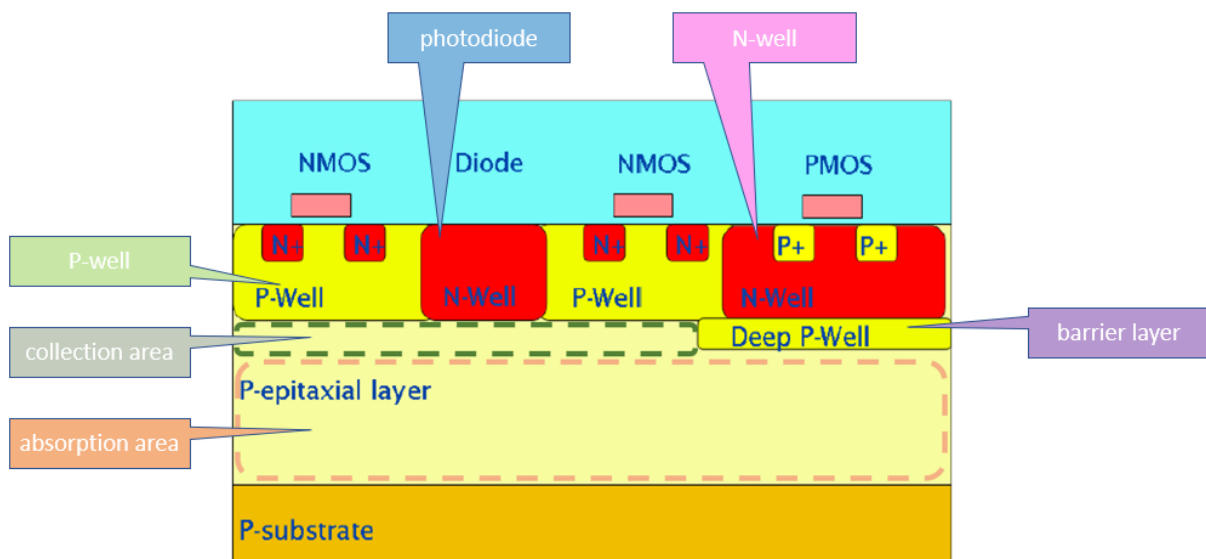
justice.” *Id.* at 12. And last, the Board has found that the copyright line on such a publication to be admissible under the residual hearsay exception. *Id.* at 11.

Based on this and other library records, Dr. Hall-Ellis concludes that Ballin “was published and accessible to the public on September 2, 2008.” *Id.*, ¶64.

Ballin is also authentic. As set forth in Dr. Ellis’s declaration, she obtained a copy from the National Library of Medicine. *Id.*, ¶60. The copy of Ballin obtained by Dr. Hall-Ellis is the same as the copy relied on in this Petition. *Compare* Ex. 1102 with Ex. 1007.

Ballin is directed to Isolated N-wells MAPS (INMAPS) image sensors, which may be front-illuminated or back-illuminated CMOS image sensors. Ex. 1007, 5336, 5339. Ballin discloses that conventional CMOS sensors includes NMOS transistors implanted in P-wells, PMOS transistors implanted in N-wells, and an N-well photodiode. It further discloses that charges are collected by the N-well photodiode as well as the N-wells of the PMOS transistors, which act as parasitic photodiodes. *Id.*, 5339, 5341, FIG. 1. Thus, maximum effective fill factor (i.e., high quantum efficiency) “is only obtained if the collection [N-well photodiode] junction is only such junction in the pixel.” *Id.*, 5339, FIG. 1. To achieve a high effective factor in the pixel while incorporating PMOS transistors implanted in N-wells in the pixel, Ballin proposes a “novel approach for isolating the N-wells of PMOS transistors ... by adding a deep P implant” underneath the N-wells.

As shown in FIG. 2 below, each pixel of Ballin's CMOS image sensor includes: (1) at least two NMOS transistors formed in **P-wells** and one PMOS transistor formed in an **N-well**, (2) an **N-well photodiode**, (3) a P- epitaxial layer with an **absorption area** and a **collection area**, where the collection area connects the absorption area to the photodiode, and (4) a **deep P-well implant** under the PMOS **N-well** acting as a **barrier layer** to isolate the **N-well** of the PMOS transistor from the **absorption area** of the epitaxial layer. Ex. 1007, FIG. 2, 5339-40; Ex. 1003, ¶¶75-76.



Ex. 1007, FIG. 2 (annotated, colors in original)

C. Zucca

Zucca is a printed publication. As set forth in the accompanying declaration of Dr. Hall-Ellis, Zucca was published in the *2012 IEEE Nuclear Science Symposium and Medical Imaging Conference Record* available to the public in the Kurt F.

Wendt Engineering Library at the University of Wisconsin – Madison. *Id.*, ¶¶74-81. This volume was first indexed at a library at Cornell University on April 12, 2012. *Id.*, ¶78.

Further supporting the public availability of these proceedings is that a copy of the Zucca conference paper is also available in the *IEEE Xplore* database and the digital repositories *ResearchGate*. *Id.*, ¶75.

The well-known nature of this and other similar IEEE publications is confirmed by Dr. Giapis. Dr. Giapis states in his declaration that he was aware of the *IEEE Nuclear Science Symposium and Medical Imaging Conference* and that Zucca, along with the other papers presented at that conference (and published in its proceedings) would have been readily available as of the publication of those proceedings. Ex. 1003, ¶79.

Moreover, Zucca was published by the IEEE as it relates to an IEEE conference. The Zucca conference proceedings bears a copyright notice of 2012, which is inherently reliable and trustworthy, given the publication source, the IEEE. Indeed, the Board has stated that the “IEEE is a well-known, reputable compiler and publisher of scientific and technical publications, and we take Official Notice that members in the scientific and technical communities who both publish and engage in research rely on information published on the copyright line of IEEE publications.” *Ericsson*, IPR 2014-00527, Paper 41 at 11. The board has further

found that “[a]llowing IPR petitioners to rely on the IEEE publication date in an IPR proceeding ... serves the interests of justice.” *Id.* at 12. And last, the Board has found that the copyright line on such a publication to be admissible under the residual hearsay exception. *Id.* at 11.

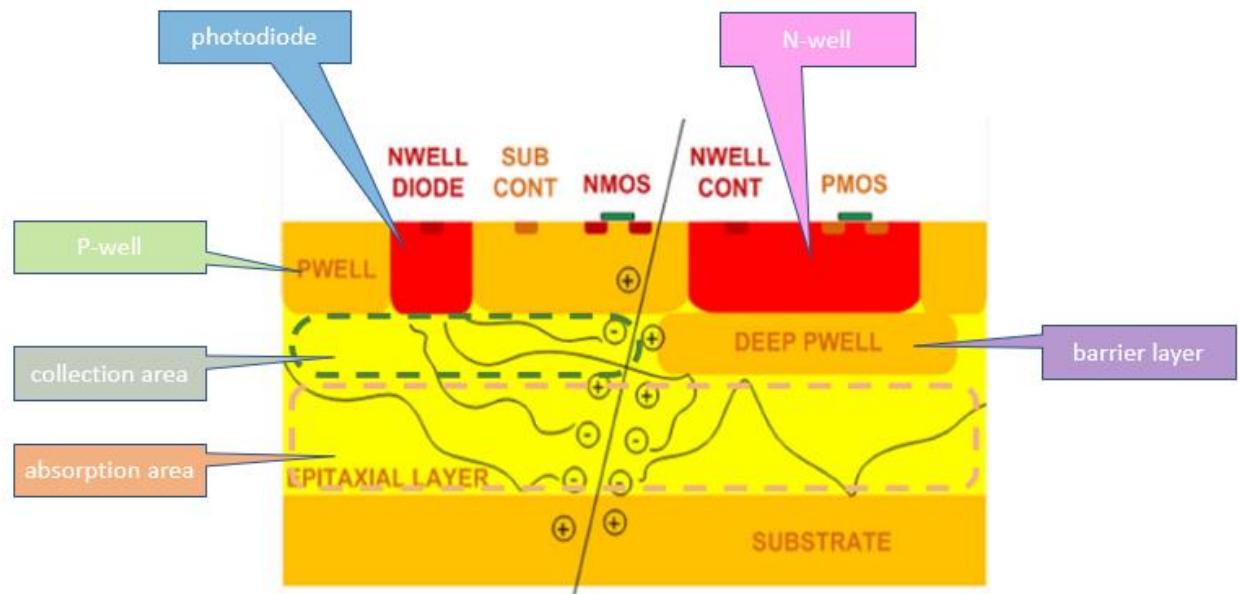
Based on this and other library records, Dr. Hall-Ellis concludes that Zucca “was published and publicly accessible on or shortly after April 12, 2012.” *Id.*, ¶81.

Zucca is also authentic. As set forth in Dr. Ellis’s declaration, she obtained a copy from the National Library of Medicine. *Id.*, ¶60. The copy of Zucca obtained by Dr. Hall-Ellis is the same as the copy relied on in this Petition. *Compare* Ex. 1102 with Ex. 1005.

Zucca is directed to monolithic active pixel sensor (MAPS), which “are also referred to as CMOS APS (active pixel sensor) or as CIS (CMOS image sensors).” Ex. 1005, 1742. Zucca discloses its MAPS image sensor is also a BSI CMOS sensor. *Id.*, 744-45 (“The samples were **illuminated from the back side....**”).

Zucca discloses that conventional MAPS image sensor architecture includes a PMOS transistor formed in an Nwell. *Id.*, 1742. However, the Nwell may degrade the pixel charge collection efficiency because it acts as a parasitic charge collector. *Id.* To overcome this problem, Zucca discloses “a high energy deep Pwell implant is deposited beneath the PMOS competitive Nwells.” *Id.* The deep Pwell implant “represents a barrier for the charge diffusing in the epitaxial layer, preventing the

carriers from being collected by the positively biased Nwells hosting the PMOS transistors.” *Id.*



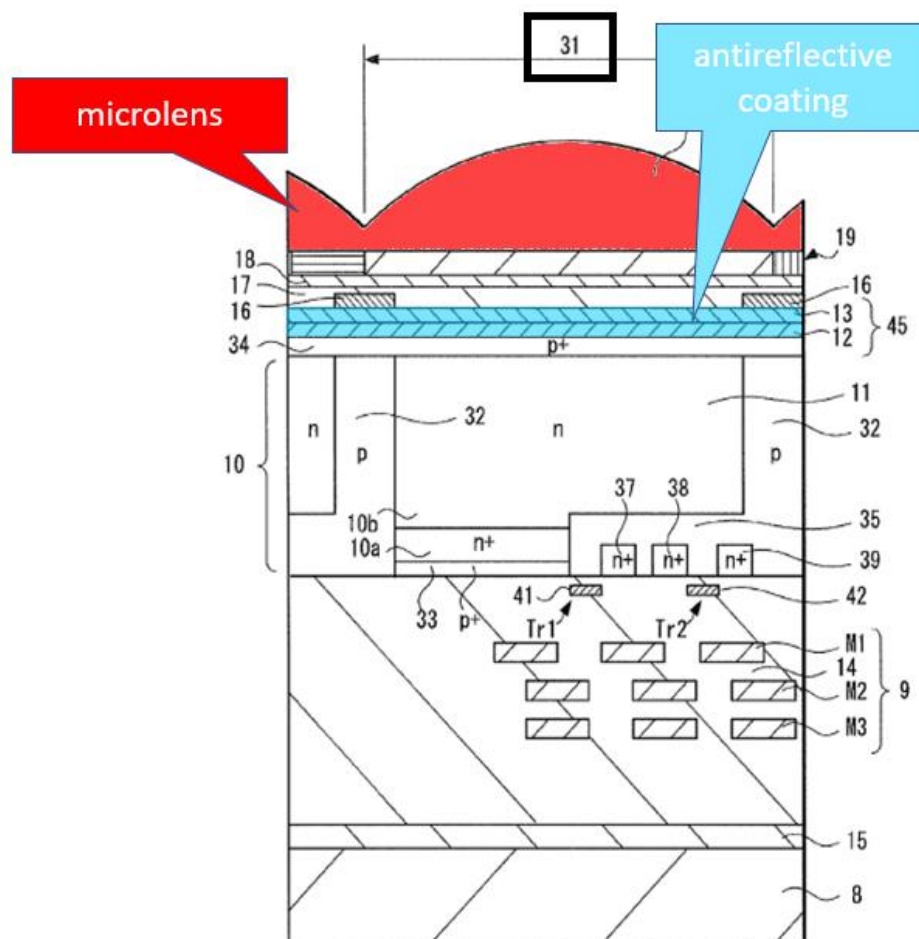
Zucca further discloses that its epitaxial layer can have different thicknesses and resistivities. *Id.*, 1743. Zucca provides three additional exemplary topologies for

its epitaxial layer: (1) 5 μm thick with standard resistivity, (2) 12 μm thick with standard resistivity, and (3) 12 μm with high resistivity. Ex. 1003, ¶83.

D. Akiyama

Akiyama is directed to solid-state imaging devices, and more specifically, to BSI CMOS solid-state imaging devices. Ex. 1006, 1:9-19.

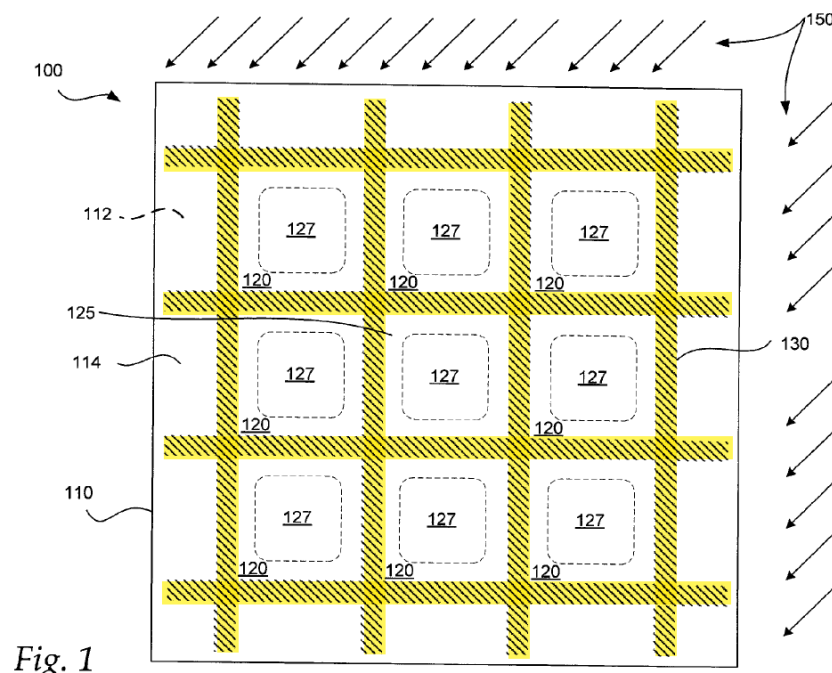
As shown in FIG. 4 below, Akiyama discloses one **pixel 31** of a BSI CMOS image sensor, which includes among other things an **antireflective coating (ARC)** 45 and a **microlens 21**. Ex. 1006, FIG. 4; 5:6-30; 5:55-6:3; Ex. 1003, ¶¶84-85.



Ex. 1006, FIG. 4.

E. Wang

Wang is directed to frontside implanted guard ring structures for BSI sensors for use in “suitable applications” such as digital cameras. Ex. 1010, Cover, 1:38-41. Wang teaches that while BSI sensors detect light projected toward the backside surface of a substrate, the sensors themselves are formed on the frontside of the substrate and, therefore, light must pass through the substrate to reach the sensors. *Id.*, 1:45-49. When passing through the substrate, some light is scattered and reaches neighboring pixels and their corresponding sensors. *Id.*, 1:49-54. Furthermore, photogenerated charges from one pixel may drift into other pixels and associated peripheral circuitry. *Id.*, 2:12-18; 3:23-26; 7:15-18; 8:10-13. Wang solves such crosstalk problems using a guard ring structure. *Id.*, 2:16-18, 4:3-5. The guard ring structure is shown in Wang’s figures, highlighted in yellow:



Wang also teaches that the guard ring structure isolates the peripheral circuitry from the pixel array. *Id.*, 8:10-13; Ex. 1003, ¶¶86-87.

VIII. GROUND 1: CLAIMS 1-6 AND 10-15 ARE OBVIOUS IN VIEW OF LAUXTERMANN

Lauxtermann renders obvious claims 1-6 and 10-15 of the '169 patent. Ex. 1003 ¶91.

1. Claim 1

[1pre] A back-side illumination (BSI) complementary metal-oxide-semiconductor (CMOS) pixel array comprising:

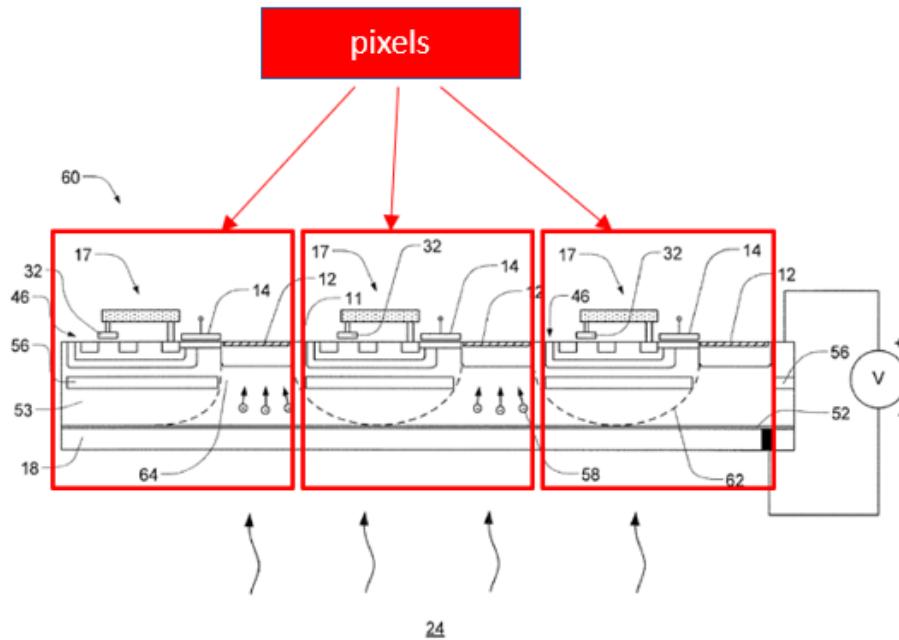
To the extent the preamble is considered to be a limitation, Lauxtermann discloses a BSI CMOS pixel array. Ex. 1003 ¶¶92-93. Lauxtermann's FIG. 5 illustrates three **BSI CMOS image sensors 60** (i.e., a **pixel array**), and Lauxtermann's FIG. 4 further illustrates that each of these CMOS image sensors 54 (i.e., a pixel) include at least a photodiode 12 and a transistor 17. Ex. 1004, Abstract, 1:6-10, FIGs. 4, 5, 5:1-3, 5:50-53. Thus, Lauxtermann discloses the claimed BSI CMOS pixel array. Ex. 1003, ¶¶92-93.

The '169 patent also states that BSI CMOS image sensors were known in prior art. Ex. 1001, 1:31-40.

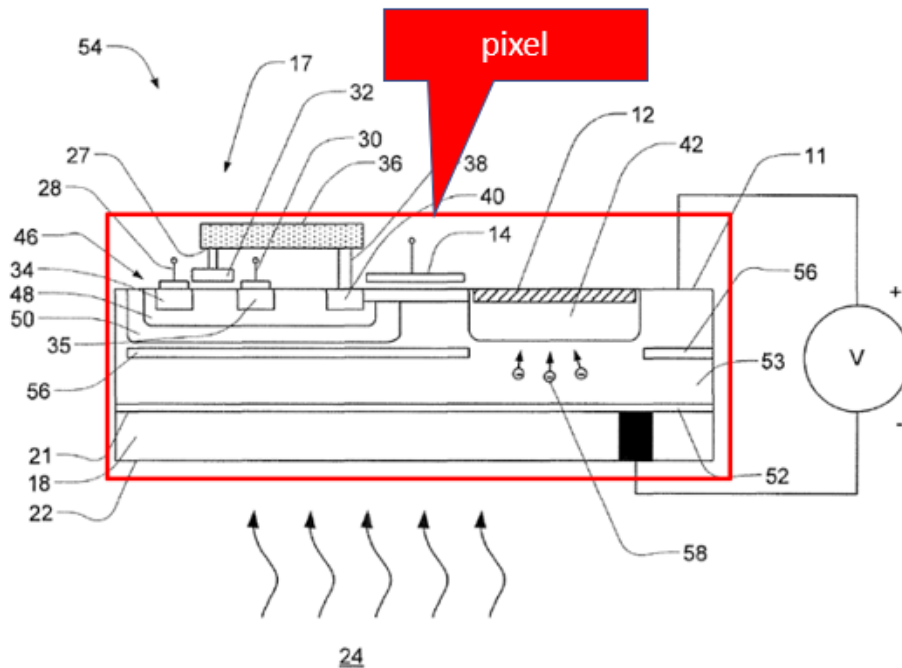
[1a] a plurality of pixels, a pixel of said plurality of pixels comprising:
--

Lauxtermann discloses a plurality of pixels. Ex. 1003 ¶95. Lauxtermann's FIG. 5 illustrates three **BSI CMOS image sensors 60** (i.e., **plurality of pixels**).

Lauxtermann's FIG. 4 further details that each of these CMOS image sensors 54 (i.e., **pixel**) of FIG. 5 includes at least a photodiode 12 and a transistor 17. This is shown below in annotated FIGs. 4 and 5. Ex. 1003, ¶96.



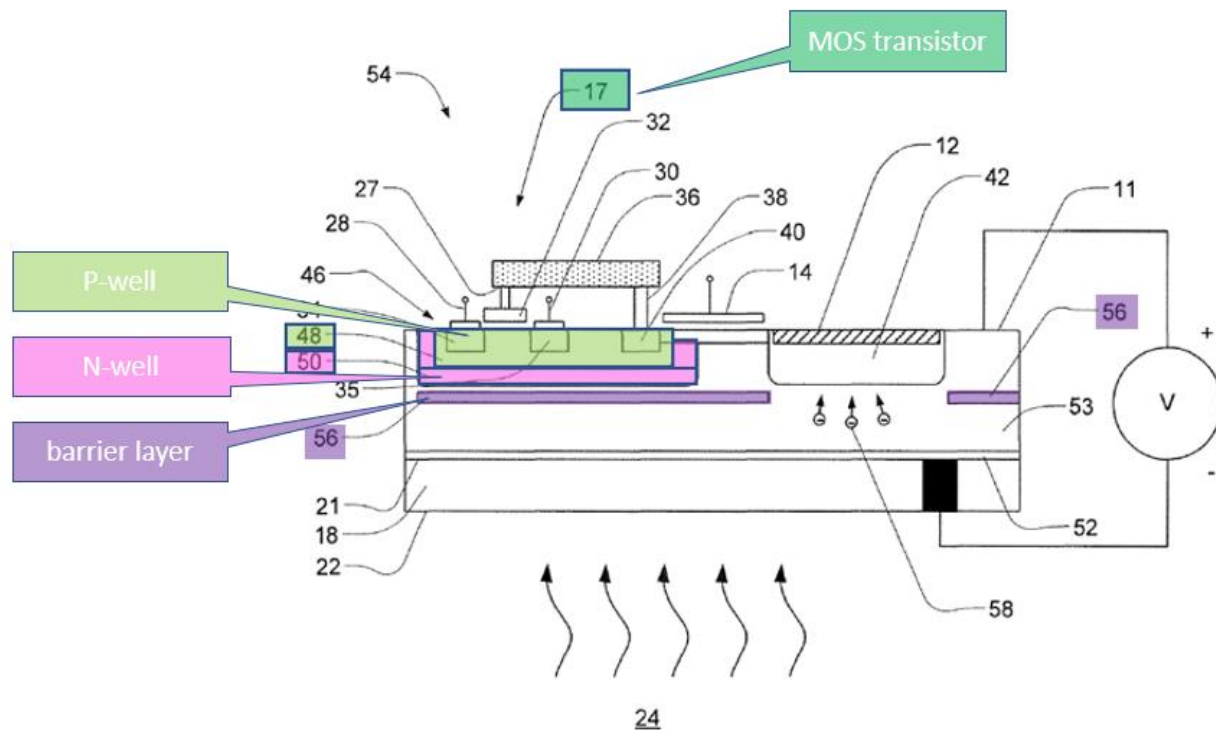
Ex. 1004, FIG. 5.



Ex. 1004, FIG. 4.

[1b] one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-well (NW) region or a P-well (PW) region;

Lauxtermann discloses one or more MOS transistors with N-well or P-well regions. Ex. 1003 ¶97. In particular, Lauxtermann discloses its BSI CMOS image sensor 54 (i.e., **pixel**) includes a **transistor 17**, which is expressly disclosed to be a **MOS transistor**, more specifically a **NMOS transistor**. See, e.g., Ex. 1004, FIG. 4, 3:47-50, 5:11-13 (“Source follower transistor 17 may be an NMOS device . . .”). As shown in FIG. 4 below, Lauxtermann discloses that its transistor 17 includes a **P-well region 48** and an **N-well region 50**. Ex. 1004, Fig. 4, 5:16-19.



Ex. 1004, FIG. 4.

Lauxtermann further discloses that its CMOS image sensor implements “a four transistor (4T) architecture,” which includes at least a transfer gate 14, a reset transistor 15, a transistor 17 (expressly disclosed to be a **MOS transistor**), and a row select transistor 19. *Id.*, 2:51-58. A POSITA would understand that these four transistors in Lauxtermann’s 4T structure are all **MOS transistors** because they are part of a CMOS image sensor made using a CMOS fabrication process. Ex. 1003 ¶¶98-99.

[1c] a photodiode;

Lauxtermann discloses a photodiode. Ex. 1003, ¶100. In particular, Lauxtermann discloses its BSI CMOS image sensor 54 (i.e., pixel) includes a

[1d] an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and
--

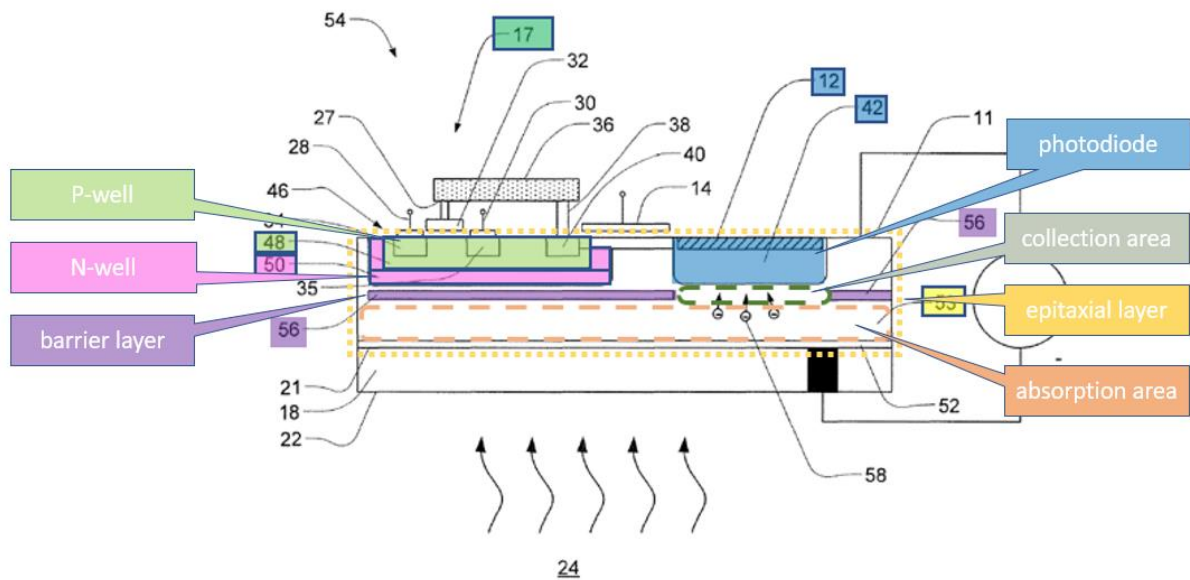
Lauxtermann renders obvious claim 1d. Ex. 1003 ¶102.

An epitaxial layer: Lauxtermann discloses that its BSI CMOS image sensor 54 (i.e., pixel) includes a **semiconductor layer 53**, and the **photodiode** is fabricated on semiconductor layer 53. Ex. 1004, FIG. 4.

Lauxtermann's semiconductor layer 53 is an **epitaxial layer** because it is formed by deposition on a single-crystalline Silicon substrate. Ex. 1003 ¶104. While other solid phases of Silicon can be grown by deposition, the CMOS devices of the image sensor perform best on epitaxial Silicon. Lauxtermann teaches semiconductor layer 53 is deposited just like semiconductor layer 16. Ex. 1004, 5:29-31 ("prior to the deposition of semiconductor layer 53"). A POSITA would have understood that semiconductor layer 53 must be Silicon deposited epitaxially on the substrate, and thus an epitaxial layer. Ex. 1003 ¶¶103-104. Moreover, in describing another embodiment, Lauxtermann expressly teaches that the "semiconductor layer" is "an **epitaxial layer**." Ex. 1004, FIG. 1, 3:4-8 (semiconductor layer 16 is "an **epitaxial layer** with a p-doped region"). A POSITA would therefore understand that Lauxtermann's semiconductor layer 53 is an epitaxial layer.

Comprising an absorption area and a collection area: Within that **epitaxial layer**, layer 53 includes a **collection area** and an **absorption area**,² the former of which connects the absorption area to the **photodiode**. The absorption area is configured **to absorb incoming photons** (from light 24) and **generate charges** 58 (i.e., electrons) **by means of the photoelectric effect**. Ex. 1003 ¶105; Ex. 1004, 2:59-6; 5:45-49. Just like the absorption area 222 in Figure 2 of the '169 patent, the identified **absorption area** in Lauxtermann is a part of **epitaxial layer 53** generally located below **p-layers (barriers) 56**. The **collection area** connects the **absorption area** to the **photodiode** to provide the charges 58 to the **photodiode**. Ex. 1003 ¶105. A POSITA would understand that the **collection area** collects the charges 58 from the **absorption area** and funnels them towards the **photodiode** in conjunction with the **p-layers 56** (since p layers repel the charges). *Id.* And just like the **collection area 224** in Figure 2 of the '169 patent, the identified **collection area** in Lauxtermann is a part of **epitaxial layer 53** generally located adjacent to **p-layers (barriers) 56** (e.g., between them) and under **photodiode 12**.

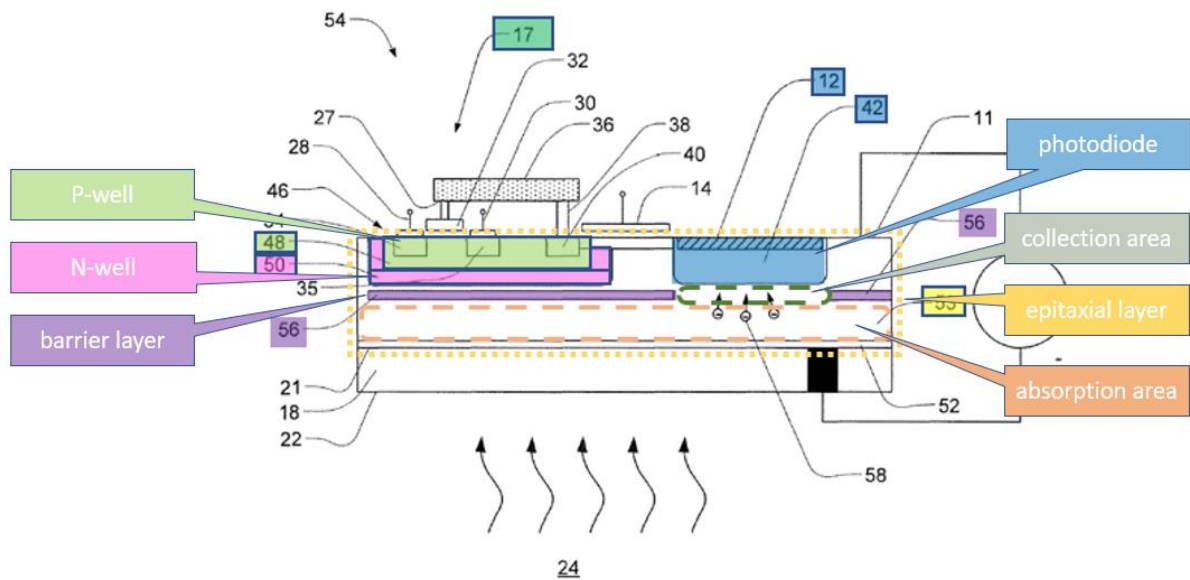
² According to the plain language of the claims and Figure 2, absorption **area** and collection **area** are portions of the epitaxial **layer**. They need not be separate layers.



Ex. 1004, FIG. 4.

[1e] a barrier layer separating said absorption area from said one or more well regions.

Lauxtermann discloses a barrier layer separating the absorption area from the well regions. Ex. 1003 ¶106. In particular, FIG. 4 shows that BSI CMOS image sensor 54 (i.e., pixel) includes a **p-layer (barrier) 56** that **separates the absorption area from the P-well 48 and N-well 50**. Ex. 1004, FIG. 4; 5:16-19; 5:41-45. Specifically, Lauxtermann discloses that its barrier layer 56 “may be a deep p⁺ implant” located underneath transistor 17 and that barrier layer 56 “allows charge 58 to drift, rather than diffuse, to the light receiving element of the pinned photodiode 12.” *Id.*, 5:41-45; Ex. 1003, ¶107.



Ex. 1004, FIG. 4.

2. Claim 2

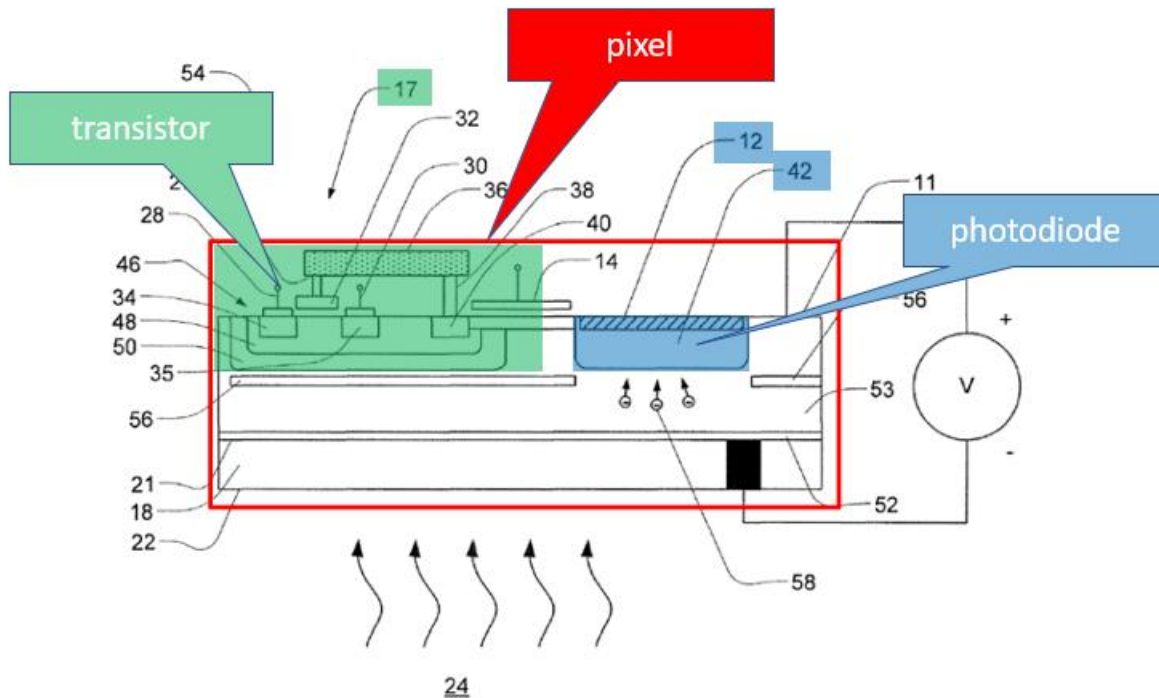
2. The BSI CMOS pixel array of claim 1, wherein said photodiode comprises a low fill factor (FF) diode.

Lauxtermann renders obvious claim 2. Ex. 1003 ¶¶108-111. The fill factor of a photodiode in an image sensor pixel is the ratio of the photodiode area to the total area of the pixel, and that a low fill factor photodiode allows transistors and other image processing components to be integrated in the pixel. Ex. 1003 ¶¶108-109.

As shown in Lauxtermann’s FIG. 4, its **photodiode 12** occupies a small area of the pixel and enables electronic components, such as **transistor 17** and transfer gate 14, to be included inside the pixel. In fact, Lauxtermann discloses that BSI CMOS image sensors provide the advantage of having photodiodes that allows “additional space in the pixel for integration of in-pixel signal processing circuits.”

Ex. 1004, 1:38-43, FIG. 4 (below). Lauxtermann discloses that its CMOS image sensor (i.e., pixel) implements “a four transistor (4T) architecture,” where at least “a floating diffusion 13, a transfer gate 14, a reset transistor 15, a source follower transistor 17 and a row select transistor 19” are integrated into one pixel, in addition to the **photodiode 12**. *Id.*, 2:51-58. Therefore, Lauxtermann’s **photodiode 12** is a **low fill factor diode**. Ex. 1003 ¶110.

Moreover, a POSITA would have understood that integration of the transistors and other imaging processing components with the photodiode in the pixel improves the efficiency and at the same time reduces the size of the image sensor. *Id.*, ¶111; Ex. 1004, 1:42-43. Accordingly, it would have been obvious to use a **low fill factor diode** for Lauxtermann’s photodiode so that other image processing components can be integrated into the pixel to improve performance of the image sensor. Ex. 1003, ¶111.



Ex. 1004, FIG. 4.

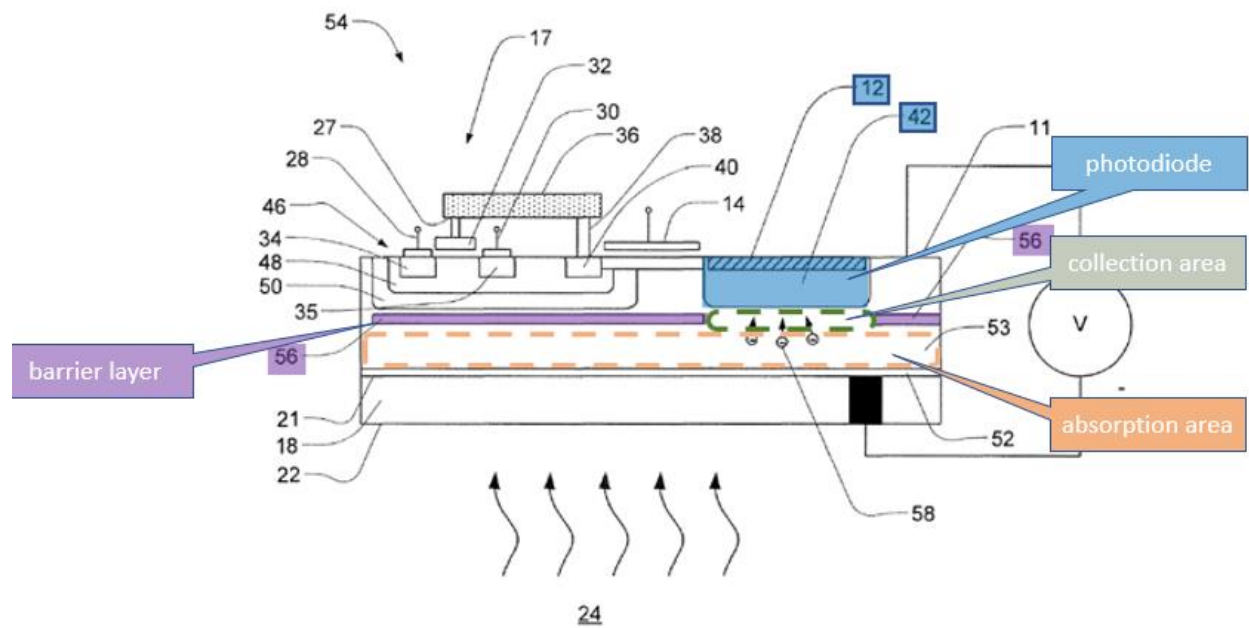
3. Claim 3

3. The BSI CMOS pixel array of claim 1, wherein said collection area extends from said absorption area to said photodiode through said barrier layer.

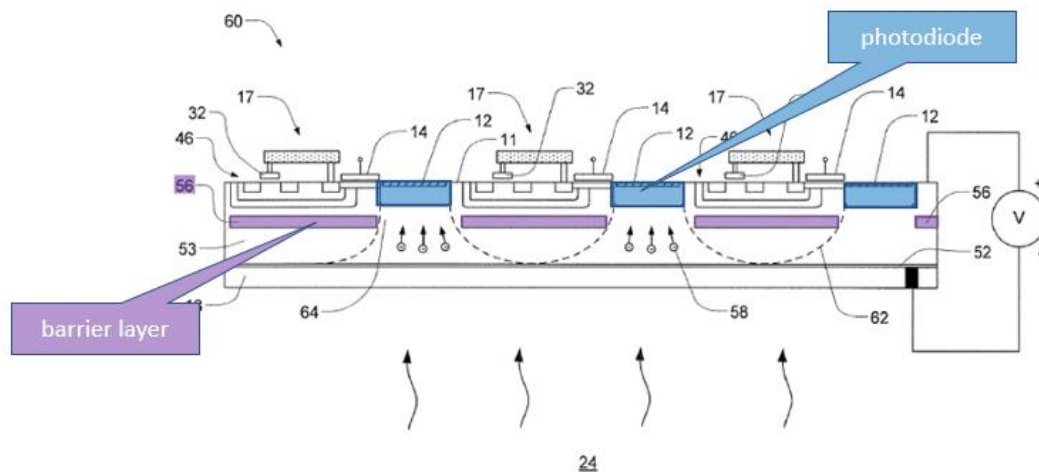
Lauxtermann renders obvious claim 3. Ex. 1003 ¶112. In particular, as shown in Lauxtermann's FIG. 4, the collection area extends from the absorption area to photodiode 12 through barrier layer 56. Ex. 1004, FIG. 4; Ex. 1003 ¶113.

Lauxtermann's **collection area** collects electric charges 58 (i.e., electrons) from the **absorption area** and guides and/or directs the collected electrons to the **photodiode 12**. Ex. 1004, Fig. 4, 5:41-45 (“[T]he p-layer 56 allows charge 58 to drift, rather than diffuse, to the light receiving element of the pinned photodiode 12.”); Ex. 1003 ¶115. Lauxtermann's **collection area** is configured to perform the functionality of an electrostatic lens because electric fields 62 around p-layers 56 create an electron funnel 64 at the **collection area**, which collects and guides electrons to **photodiode 12**. Ex. 1004, 5:50-65, FIG. 5. Specifically, Lauxtermann's heavily doped p⁺ barrier layers 56 repel electrons (i.e., electric charges 58) in the **absorption area** and facilitate lateral movement of the electrons towards the **collection area**. Electrons that reach the collection area are driven across the junction into the n-type layer 42 of the **photodiode 12**. *Id.* ¶115. This is the functionality of the electrostatic lens according to the '169 patent. Ex. 1001, 7:23-32. Therefore, Lauxtermann's **collection area** is **configured to perform the functionality of an electrostatic lens**.

structural character of the limitation-in-question or otherwise impart structure to the claim term.”).



Ex. 1004, FIG. 4.

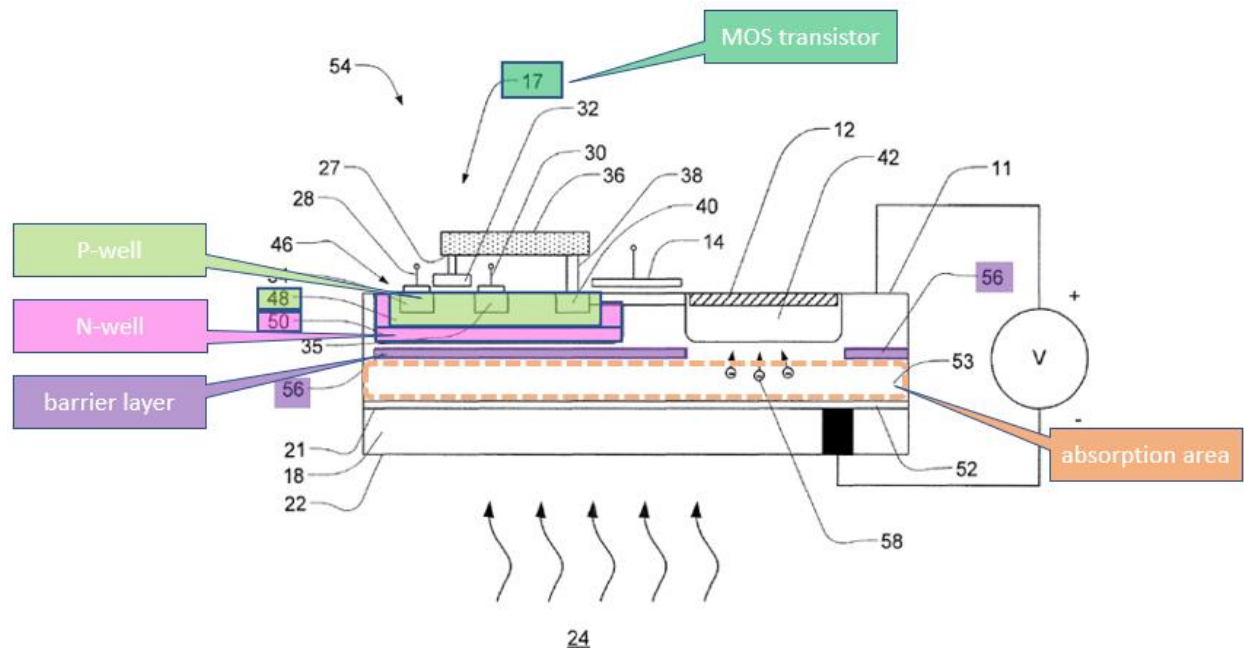


Id. FIG. 5.

5. Claim 5

5. **The BSI CMOS pixel array of claim 1, wherein said barrier layer is configured to prevent diffusion of said electrons from said absorption area to said well regions.**

Lauxtermann discloses that its **barrier layer 56** is configured to prevent diffusion of electron from the **absorption area** to the **N-well 50**. Ex. 1003 ¶116; Ex. 1004, FIG. 4; 5:41-45. Lauxtermann discloses that its barrier layer 56 “may be a deep p+ implant” located underneath transistor 17 and its P-well region 48 and N-well region 50, and that the barrier layer 56 “allows charge 58 to drift, rather than diffuse, to the light receiving element of the pinned photodiode 12.” Ex. 1004, FIG. 4; 5:41-45. Without barrier layer 56, charges would diffuse towards both pinned **photodiode 12** and the active pixel circuitry (i.e., **transistor 17** with **N-well 50**). *Id.*, 4:57-65. Barrier layer 56 is therefore **configured to prevent diffusion of electrons from the absorption area to the well regions**. Ex. 1003 ¶117.



Ex. 1004, FIG. 4.

6. Claim 6

6. The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 4 micron (μm).

Lauxtermann renders obvious claim 6. Ex. 1003 ¶118. As discussed in Section VIII.1, in connection with claim elements 1d and 1e, semiconductor layers 53 (FIG. 4) and 16 (FIG. 1) are both epitaxial layers. Ex. 1004, *compare* FIG. 1 *with* FIG. 4; Ex. 1003 ¶119. Lauxtermann explains that the Figure 1 embodiment “is a backside illuminated CMOS image sensor 10, according to an embodiment of the invention” (Ex. 1004, 2:50-51), while the Figure 4 embodiment is “a backside illuminated CMOS image sensor 54 with a p-layer 56” (*id.*, 5:1-3). Both embodiments teach use of a “pinned photodiode 12” which is fabricated on a semiconductor layer. *Id.*, 3:4-

5. Lauxtermann expressly discloses the pinned photodiode is fabricated on **epitaxial** layer 16, which includes a p-doped region 20 that is **5 μm** thick. Ex. 1004, 3:4-8

Lauxtermann, however, does not expressly disclose the thickness of semiconductor layer 53 (the epitaxial layer identified in Ground 1). Ex. 1003 ¶120. However, given Lauxtermann's teachings that the pinned photodiodes are fabricated on a 5 μm thick epitaxial layer (as claimed), it would have been obvious to a POSITA to fabricate Lauxtermann's semiconductor layer 53 with a thickness similar to the thickness of its semiconductor layer 16. *Id.* Layers 16 and 53 are from similar embodiments of the same invention and both layers perform the same function of converting lights 24 into electric charges and serving as the underlying substrate for **photodiode 12** and the active pixel circuitry, including floating diffusion 13 (n-doped region 40 in Fig. 4), transfer gate 14, and source follower transistor 17. *Id.*

Further, it would have been obvious to a POSITA to use a at least 4 micron thick epitaxial layer in a BSI CMOS image sensor to improve the light sensitivity of the image sensor. Ex. 1003 ¶121. A POSITA would have understood that the amount of electric charges generated by an epitaxial layer from absorbed light incident on the image sensor is approximately proportional to the thickness of the epitaxial layer. *Id.*; Ex. 1005, 1745. Therefore, a POSITA would use a at least 4 micron thick epitaxial layer, like the 5 micron epitaxial layer in Lauxtermann's FIG. 1 in every embodiment of Lauxtermann's BSI CMOS image sensors. Ex. 1003 ¶121.

7. Claim 10

10. The BSI CMOS pixel array of claim 1 comprising a micro lens, said absorption area is between said micro lens and said barrier layer.

Lauxtermann renders obvious claim 10. Ex. 1003 ¶122. It was well-known that a microlens arrays are used in BSI CMOS image sensors. *Id.* Microlens arrays focus light incident on each microlens towards the absorption area of a corresponding photodiode. *Id.* The use of microlenses with BSI CMOS image sensors like Lauxtermann's was very well-known and highly conventional. *Id.*; Exs. 1033-1036, 1059. Indeed, one well-known advantage of BSI image sensors is the "small distance between microlens and silicon photodiode." Ex. 1035, 24.1.1 (Introduction). Lauxtermann, which teaches a BSI CMOS image sensor, therefore expressly teaches a microlens. Ex. 1003 ¶122. It would have been obvious to include a microlens, in Lauxtermann's BSI CMOS sensor, specifically on the backside of the sensor so that the absorption layer is between the microlens and the barrier layer, to improve light collection efficiency of its image sensor for use in electronic devices. *Id.*

8. Claim 11

11. The BSI CMOS pixel array of claim 10 comprising an anti-reflective coating (ARC) layer, said ARC layer is between said micro lens and said absorption area.
--

Lauxtermann renders obvious claim 11. Ex. 1003 ¶123. It was well-known that ARC layers are used in BSI CMOS image sensors. *Id.* ARC layers allow more light to reach a photodiode by minimizing light reflection at the interface between a component on the backside surface of the image sensor die and the silicon material of the backside surface itself, which would otherwise decrease the efficiency of the image sensor. *Id.* The use of ARC layers with BSI CMOS image sensors like Lauxtermann's was very well-known and highly conventional. *Id.*; Exs. 1033-1036, 1059. Lauxtermann, which teaches a BSI CMOS image sensor, therefore expressly teaches an ARC layer. Ex. 1003 ¶123. To the extent Alidouble argues Lauxtermann doesn't expressly teach a BSI CMOS image sensor with a microlens, it would have been obvious to include an ARC layer in between the microlens and the absorption area to improve light collection efficiency of its image sensor for use in electronic devices. Ex. 1003 ¶123.

9. Claim 12

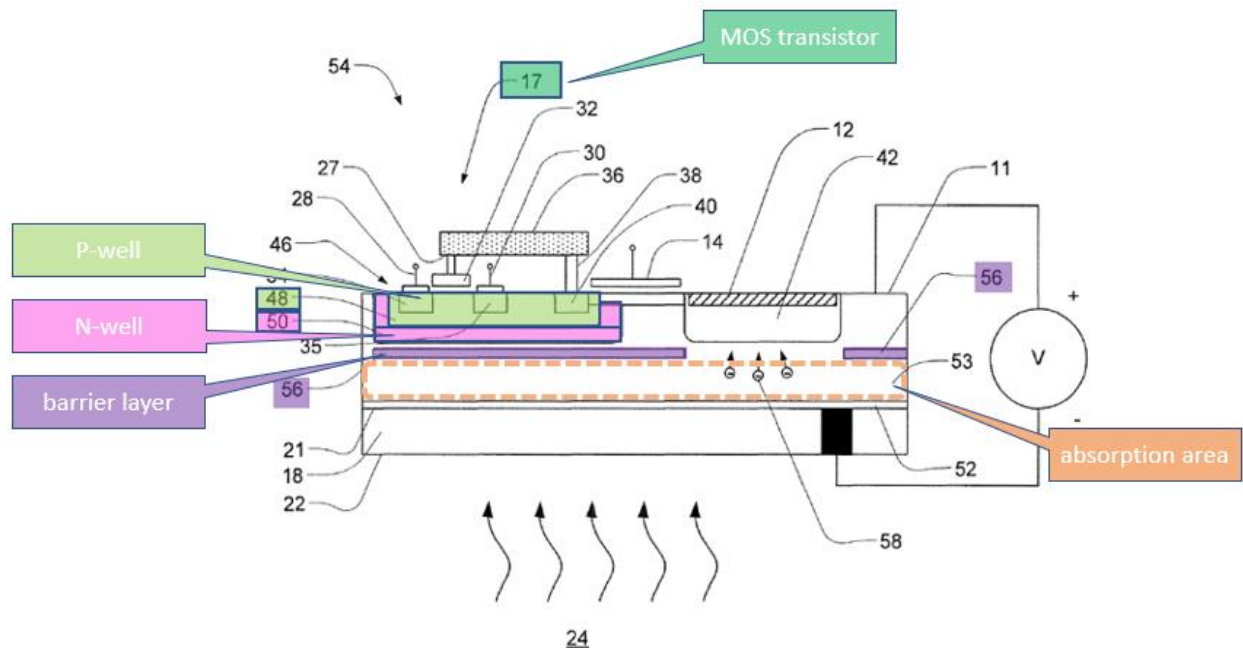
12. The BSI CMOS pixel array of claim 1, wherein said one or more MOS transistors comprise one or more transistors selected from a group consisting of one or more P-type MOS (PMOS) transistors and one or more N-type MOS (NMOS) transistors.
--

Lauxtermann discloses that its transistors are MOS transistors and that transistor 17 may be an NMOS transistor. Ex. 1003 ¶¶124-125; Ex. 1004, 3:45-50, 5:11-12. Lauxtermann further discloses “CMOS image sensor may [also] include active pixel circuitry, such as a p-type metal-oxide-semiconductor (PMOS) device.” *Id.*, 6:17-19. Lauxtermann therefore discloses that its **one or more MOS transistors are selected from a group consisting of PMOS and NMOS transistors**. Ex. 1003 ¶125.

10. Claim 13

13. The BSI CMOS pixel array of claim 1, wherein said barrier layer comprises a deep PW implant.

Lauxtermann discloses that its barrier layer 56, which is a p-layer, “may be a **deep p+ implant**” located underneath the transistor 17. Ex. 1004, 5:40-42, 6:19-22. A “PW” implant is a “p-well” implant according to the ’169 patent. Ex. 1003 ¶¶126-128; Ex. 1001, 4:30-32, 9:20-21, 9:52-56, FIGs. 3C-3D. Lauxtermann’s deep p+ implant of barrier layer 56 is therefore **a deep PW (P-well) implant** because barrier layer 56 is deeper than P-well 48. Ex. 1003 ¶¶126-127.



Ex. 1004, FIG. 4.

Moreover, the use of deep p-well implants in image sensors was well-known by the priority date of the '169 patent. See Ex. 1012, 57-58, FIG. 2; Ex. 1013, 1311, FIG. 2; Ex. 1050, 3:45-64; Ex. 1051, 1:33-39, 4:47-48, 6:37-67, Figs. 15A-15C. At a minimum, therefore, the use of a deep p-well implant in Lauxtermann's BSI CMOS image sensor would have been obvious. Ex. 1003 ¶128.

11. Claim 14

14. The BSI CMOS pixel array of claim 1, wherein said barrier layer comprises a boron implant.

Lauxtermann renders obvious claim 14. Ex. 1003 ¶129. In particular, Lauxtermann discloses that its p-layer 56 (i.e., barrier layer) may be a deep p⁺ implant. Ex. 1004, 5:41-42. Boron is the most common p-type dopant. Ex. 1003,

¶1030; Ex. 1024, 467; Ex. 1025, 31; Ex. 1026, 4:24-30; Ex. 1027, [0059], [0106], [0107]. Therefore, it would have been obvious to a POSITA to use a **boron implant** for Lauxtermann’s deep p-layer 56 (i.e., barrier layer). Ex. 1003, ¶130. Indeed, when describing other p-layers, Lauxtermann teaches the use of boron, confirming the obviousness of using boron—the most common p-type dopant—in Lauxtermann’s p-layer 56. Ex. 1004, 3:4-8.

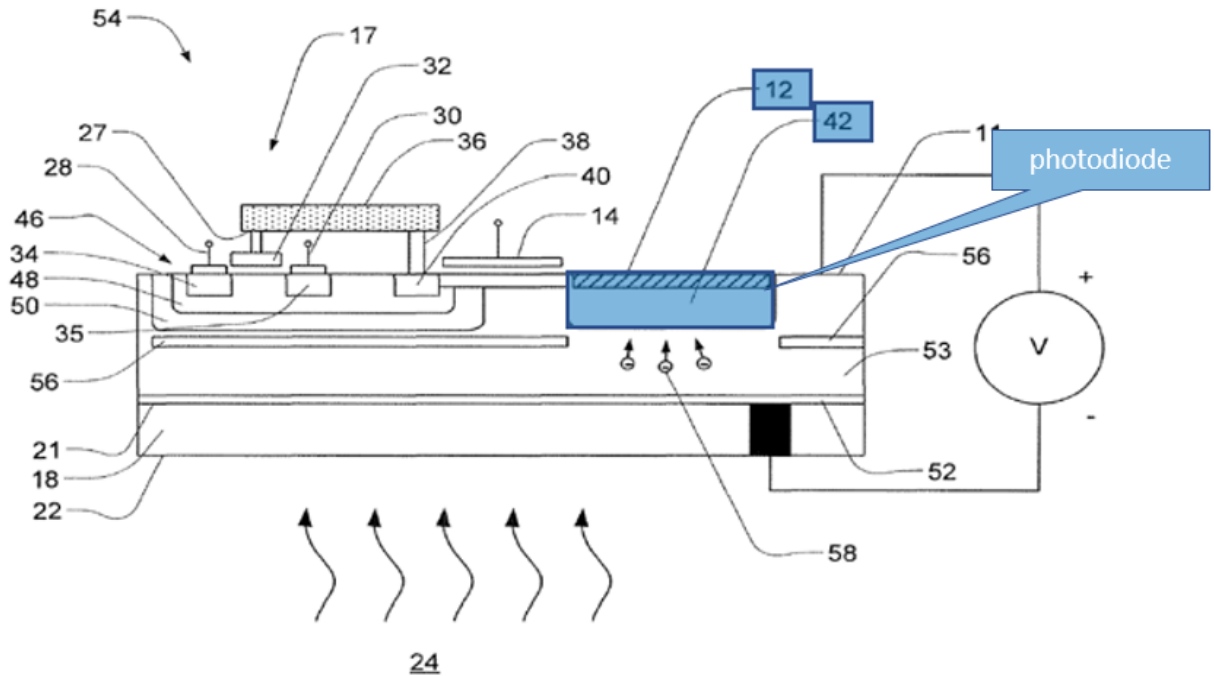
12. Claim 15

15. **The BSI CMOS pixel array of claim 1, wherein said photodiode comprises a fully pinned diode.**

Lauxtermann renders obvious claim 15. Ex. 1003 ¶131. The “fully pinned” terminology used in the ‘169 patent is what is commonly referred to as “pinned,” i.e., not partially pinned. *Id.* As discussed in Section II.B.2, a pinned photodiode has a p⁺ pinning layer that covers the photodiode while a partially pinned photodiode has an n⁺ region in an area of the photodiode not covered by the p⁺ pinning layer. Ex. 1029, 3:61-4:5, 4:32-67, Fig. 2, Fig. 4. Moreover, pinned photodiodes are often used with 4T CMOS APS pixels, while partially pinned photodiodes are often used with 3T CMOS APS pixels. Ex. 1028, 35; Ex. 1003 ¶132. Lauxtermann teaches the use of a 4T CMOS APS pixel. Ex. 1004, 2:51-56, Fig. 4; Ex. 1003 ¶132.

Lauxtermann specifically discloses a **pinned photodiode 12** which has a p⁺ pinning layer that covers the photodiode and does not include an n⁺ layer in an area of the photodiode not covered by the pinning layer. Ex. 1003, ¶133. “The pinned

photodiode 12 collects charge due to light 24” and “[t]ransfer gate 14 transfers the signal from the pinned photodiode 12 to the NMOS source follower device 17” without using any n+ region in the photodiode. *Id.*, 5:5-10. Therefore Lauxtermann’s photodiode is a **fully pinned photodiode**, as claimed. Ex. 1003, ¶¶132-133.



Ex. 1004, FIG. 4.

Moreover, Lauxtermann discloses “a need in the art for backside illuminated CMOS image sensors with reduced noise, dark current and sense node capacitance.” Ex. 1004, 1:50-52. It was well-known that fully pinned photodiodes have low noise, high quantum efficiency and low dark current. Ex. 1028, 33. Thus, a POSITA would readily understand that Lauxtermann’s “pinned photodiode” is a **fully pinned diode**, as opposed to a partially or non-pinned photodiode. Ex. 1003 ¶134.

IX. GROUND 2: CLAIMS 2, 6, 7 AND 9 ARE OBVIOUS OVER LAUXTERMANN IN VIEW OF ZUCCA

Lauxtermann in view of Zucca render obvious claims 2, 6, 7, and 9 of the '169 patent. Ex. 1003 ¶135.

1. Reasons to Combine Lauxtermann with Zucca

Claim 2 requires that the photodiode comprise a “low fill factor” (“FF”) diode. Claims 6 and 7 require that the epitaxial layer be of various minimum thicknesses. Claim 9 require that the epitaxial layer be of certain minimum resistivity. Zucca teaches (1) a low FF diode, which meets the requirement of claim 2, (2) an epitaxial layer of 12 μm thickness, which meets the “minimum” requirements of claims 6 and 7, and (3) an epitaxial layer with a high resistivity of about 1000 ohm-cm, which meets the requirement of claim 9. A POSITA would have been motivated to modify Lauxtermann to include these teachings and would have had a reasonable expectation of success, for the following reasons. Ex. 1003, ¶136.

An epi layer of at least 4 [claim 6] / 10 [claim 9] μm : A POSITA would have been motivated to include an epitaxial layer at least 4 μm thick in Lauxtermann's BSI CMOS image sensor according to Zucca's teachings because doing so would improve the light sensitivity and thus efficiency of its image sensor. Ex. 1003 ¶137. As disclosed in both Lauxtermann and Zucca, light incident on the back side of their respective BSI image sensors is absorbed by the epitaxial layer, which generates electric charges that are then collected by the photodiodes implanted in the epitaxial

layer. Ex. 1003 ¶137; Ex. 1004, 5:11-13, 5:36-39; Ex. 1005, FIG. 1. As further discussed in Zucca, the electric charges collected by the photodiodes of its monolithic pixel sensors (MAPS), which are BSI CMOS image sensors, are “almost proportional to the epitaxial layer thickness.” Ex. 1005, 1745. Specifically, Zucca discloses two image sensor designs, one with a 12 μm thick epitaxial layer and the other with a 5 μm thick epitaxial layer, and shows that the amount of electric charges collected by the sensor with the 12 μm epitaxial layer is about two times higher than the sensor with the 5 μm epitaxial layer. *Id.* Similarly, Lauxtermann discloses that one embodiment of its BSI image sensor includes an epitaxial layer 16 that is at least 5 μm thick. Ex. 1001, 3:4-8. Thus, a greater than 4 micron thick epitaxial layer is already contemplated by Lauxtermann. Therefore, including an at least 4 μm thick epitaxial layer in Lauxtermann’s BSI CMOS image sensor according to Zucca’s teachings would have the obvious added benefit of better electric charge collection performance and therefore improved efficiency of the image sensor, especially in low light conditions. And because Lauxtermann expressly teaches using a thick epitaxial layer, a POSITA would have had a reasonable expectation of success in doing so. Ex. 1003 ¶137.

An epitaxial layer of at least 100 ohm-cm [claim 9]: A POSITA would also have been motivated to use a high resistivity epitaxial layer (e.g., greater than 100 ohm to centimeter (ohm-cm)) in Lauxtermann’s BSI CMOS image sensor according

to Zucca's teachings to improve the efficiency of its image sensor. Ex. 1003 ¶138. As disclosed in Zucca, a higher resistivity in the epitaxial layer corresponds to more electric charges (generated from incident light) collected by the image sensor. Ex. 1005 at 1745 (reporting that "the charge collected by [a CMOS image sensor], featuring a high resistivity epitaxial layer, is about 35% higher than [another CMOS image sensor] featuring a standard resistivity epitaxial layer," while other parameters are equal). Zucca teaches its "high resistivity epitaxial layer option" improves "charge collection properties." *Id.*, 1748. Specifically, Zucca teaches a "sensor fabricated on a 12 μm thick high resistivity epitaxial layer" is "the best solution among different available options in terms both of the amount of collected charge and of charge collection uniformity." *Id.*

Lauxtermann similarly discloses that its semiconductor layer 53 (an epitaxial layer) is "a high resistivity semiconductor layer" and that the use of the high resistivity semiconductor layer 53 in combination with other measures (e.g., p-layer 56 as a barrier layer) "enhances the performance of the CMOS sensor 60, improves quantum efficiency and reduces noise, dark current and sense node capacitance." Ex. 1004 at 5:7-9, 5:61-65; Ex. 1003, ¶138.

A photodiode comprising a low fill factor diode [claim 2]: Finally, A POSITA would have also been motivated to include a low fill factor photodiode in Lauxtermann's BSI CMOS image sensor according to Zucca's teachings to improve

the image processing performance of its image sensor. Ex. 1003 ¶139. As a POSITA would have understood, a low fill factor photodiode occupies a small area of a pixel, and therefore allows image processing components such as transistors to be integrated into the pixel with the photodiode, which improves the image processing performance of the image sensor. *Id.* In fact, Lauxtermann already discloses that one advantage of BSI CMOS image sensors is the “availability of additional space in the pixel for integration of in-pixel signal processing circuits” and that its sensor implements “a four transistor (4T) architecture” where transistors and other components are integrated together with a photodiode into one pixel. Ex. 1004 at 1:40-43, 2:51-58. Thus, a POSITA would have used a low fill factor photodiode in Lauxtermann’s BSI CMOS image sensor according to Zucca’s teachings to improve the image processing performance of its image sensor. *Id.*

Similar techniques to solve the same problems: Like the ’169 patent, both Lauxtermann and Zucca address the same problem with similar techniques: to improve the efficiency of a BSI CMOS image sensor by using a barrier layer to prevent electric charges from diffusing to transistors integrated in the pixel, thereby allowing the photodiode to collect more electric charges. Ex. 1003, ¶141. Lauxtermann recognizes that its photodiode “collects only a fraction of the [electric] charges” because the charges “diffuse towards [both] the pinned photodiode 12 and the active pixel circuitry” and the pixel circuitry absorbs some of the electric charges.

Ex. 1004, 4:57-65, 4:13-37, Fig. 3. Lauxtermann solves the problem by implanting a p-layer (barrier layer) underneath the N-well of the pixel circuitry (transistor) to prevent diffusion of the electric charges to the transistor. *Id.*, FIG. 4, 5:40-49.

Similar to Lauxtermann, Zucca discloses that its each pixel of its image sensor integrates a photodiode (Nwell diode) and a PMOS transistor hosted in an Nwell, which “by acting as parasitic charge collectors, may degrade the pixel charge collection efficiency.” Ex. 1005, 1742. Zucca proposes depositing a “deep Pwell implant . . . beneath the PMOS competitive NWells” to prevent the charges been collected by the transistors. *Id.*; Ex. 1003, ¶142.

Same field of endeavor: Like the ’169 patent, both Lauxtermann and Zucca are directed to BSI CMOS image sensors and methods for improving the efficiency of the image sensors. Ex. 1003, ¶143.

Reasonable expectation of success/predictable results: A POSITA would have been motivated to include an at least 4 μm thick epitaxial layer with a high resistivity (e.g., greater than 100 ohm-cm) in Lauxtermann’s BSI CMOS image sensor with at least a reasonable expectation of success because the thickness and resistivity of the epitaxial layer in an image sensor is easily controllable in the fabrication process. Ex. 1003, ¶144. Indeed, Lauxtermann already discloses that one embodiment of its image sensor includes an epitaxial layer that has a thickness of at least 5 μm (Ex. 1005, 3:5-8) and a “high resistivity semiconductor layer [i.e.,

epitaxial layer] 53” (Ex. 1005, 5:7-8, 61-65). Thus, a POSITA with knowledge of Lauxtermann would have naturally looked to the disclosures of Zucca when finding a method to improve the efficiency of a BSI CMOS image sensor. Ex. 1003 ¶144.

Further, designing Lauxtermann’s BSI CMOS image sensor to include a low fill factor photodiode as disclosed in Zucca would also have been readily accomplished. As a POSITA would have understood, a low fill factor photodiode occupies a small area of a pixel and thus allows other image processing components such as transistors to be integrated in the pixel. Ex. 1003 ¶145. In fact, Lauxtermann already discloses one advantage of CMOS BSI image sensors is providing “availability of additional space in the pixel for integration of in-pixel signal processing circuits” and that its sensor implements “a four transistor (4T) architecture” where transistors and other components are integrated together with a photodiode into one pixel. Ex. 1004 at 1:40-43, 2:51-58; Ex. 1003, ¶145.

2. Claim 2

2. The BSI CMOS pixel array of claim 1, wherein said photodiode comprises a low fill factor (FF) diode.

Lauxtermann combined with the low fill factor diode of Zucca renders obvious claim 2. Ex. 1003 ¶¶146-147. Zucca discloses that one pixel of its image sensor has “a 50 μm pitch” (i.e. a width of 50 μm) and “4 interconnected Nwell square diodes, each with a 1.5 μm side.” Ex. 1004, 1743. This means that the photodiodes occupy **only about 0.36%** of the total area of a pixel. Further, the

relatively small photodiodes allow Zucca to integrate multiple NMOS transistors and PMOS transistors into one pixel. *Id.*, 1742, FIG. 1. Thus, a POSITA would understand that Zucca’s photodiodes are **low fill factor photodiodes**. Ex. 1003 ¶148.

In fact, Lauxtermann already discloses that one advantage of BSI CMOS image sensors is providing “availability of additional space in the pixel for integration of in-pixel signal processing circuits” and that its sensor implements “a four transistor (4T) architecture” where transistors and other components are integrated together with a photodiode into one pixel. Ex. 1004 at 1:40-43, 2:51-58. Thus, it would have been obvious to include Zucca’s low fill factor photodiodes in Lauxtermann’s BSI CMOS image sensors. Ex. 1003 ¶149.

3. Claim 6

6. The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 4 micron (μm).

Lauxtermann combined with Zucca’s disclosure render obvious claim 6. Ex. 1003 ¶¶150-151. As discussed in Section IX.3, Lauxtermann alone renders claim 6 obvious. Additionally, Zucca discloses that its BSI CMOS image sensor includes “a lightly P-doped epitaxial layer **about 10 μm thick**.” Ex. 1005, 1743. Zucca further provides three additional exemplary topologies for its epitaxial layer with different thicknesses and resistivities to achieve different performances: (1) **5 μm thick** with standard resistivity, (2) **12 μm thick** with standard resistivity, and (3) **12 μm thick** with high resistivity. *Id.* Thus, Zucca discloses that **a thickness of its epitaxial layer**

is at least 4 micron (μm). Ex. 1003 ¶152. It would have been obvious to include Zucca's at least 4 μm thick epitaxial layer in Lauxtermann's BSI CMOS image sensor. *Id.*

4. Claim 7

7. **The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 10 micron (μm).**

Lauxtermann combined with Zucca's disclosure render obvious claim 7. Ex. 1003 ¶¶153-154. Zucca discloses that its BSI CMOS image sensor includes "a lightly P-doped epitaxial layer **about 10 μm thick.**" Ex. 1005, 1743. Zucca further provides three additional exemplary topologies for its epitaxial layer with different thicknesses and resistivities to achieve different performances: (1) 5 μm thick with standard resistivity, (2) **12 μm thick** with standard resistivity, and (3) **12 μm thick** with high resistivity. *Id.* Thus, Zucca discloses **a thickness of its epitaxial layer is at least 10 micron (μm).** Ex. 1003 ¶155. It would have been obvious to include Zucca's at least 10 μm thick epitaxial layer in Lauxtermann's BSI CMOS image sensor. *Id.*

5. Claim 9

9. **The BSI CMOS pixel array of claim 1, wherein a resistivity of said epi layer is greater than 100 ohm to centimeter (ohm-cm).**

Lauxtermann combined with Zucca's disclosure render obvious claim 9. Ex. 1003 ¶¶156-157. Both Lauxtermann and Zucca disclose the benefits of using highly

resistive epitaxial layers. Ex. 1004, 5:59-65 (stating high resistivity semiconductor layer 53 may help improving “quantum efficiency and reduces noise, dark current and sense node capacitance”); Ex. 1005, 1745. Zucca further expressly discloses that one of its epitaxial layer designs has a high resistivity of about **1000 ohm-cm** with improved collection properties. Ex. 1005 at 1743. Thus, Zucca discloses that **a resistivity of its epitaxial layer is at least 100 ohm-cm**. Ex. 1003 ¶158. It would have been obvious to include Zucca’s 1000 ohm-cm epitaxial layer in Lauxtermann’s BSI CMOS image sensor. *Id.*

X. GROUND 3: CLAIMS 10 AND 11 ARE OBVIOUS OVER LAUXTERMANN IN VIEW OF AKIYAMA

Lauxtermann in view of Akiyama render obvious claims 10 and 11 of the ’169 patent. Ex. 1003 ¶159.

1. Reasons to Combine Lauxtermann with Akiyama

Claim 10 further requires a microlens and claim 11 further requires antireflective coating (ARC) layer. Akiyama teaches both a microlens and an ARC layer. A POSITA would have been motivated to include a microlens and an antireflective coating (ARC) layer in Lauxtermann’s BSI CMOS image sensor according to Akiyama’s teachings to improve the efficiency of its image sensor for use in electronic devices. Ex. 1003 ¶160.

Microlens [claim 10] and ARC layer [claim 11]: A POSITA would have understood that microlens arrays are widely used in CCD and CMOS image sensors

so that light incident on each microlens is focused towards a corresponding photodiode. *Id.* ¶161. A POSITA would also have understood that ARC allows more light to reach a photodiode by minimizing light reflection at the interface between a component on the backside surface of the image sensor die and the silicon material of the backside surface itself, which would otherwise decrease the efficiency of the image sensor. *Id.* Thus, a POSITA would have been motivated to incorporate a microlens and an ARC into Lauxtermann's image sensor according to Akiyama's teachings to improve light collection efficiency of its image sensor for use in electronic devices. *Id.*

Same field of endeavor: Like the '169 patent, both Lauxtermann and Akiyama are directed to BSI CMOS image sensors and methods for improving the performances of the image sensors. Ex. 1003, ¶163. Lauxtermann and Akiyama disclose BSI CMOS image sensors that have very similar structures. *Id.*

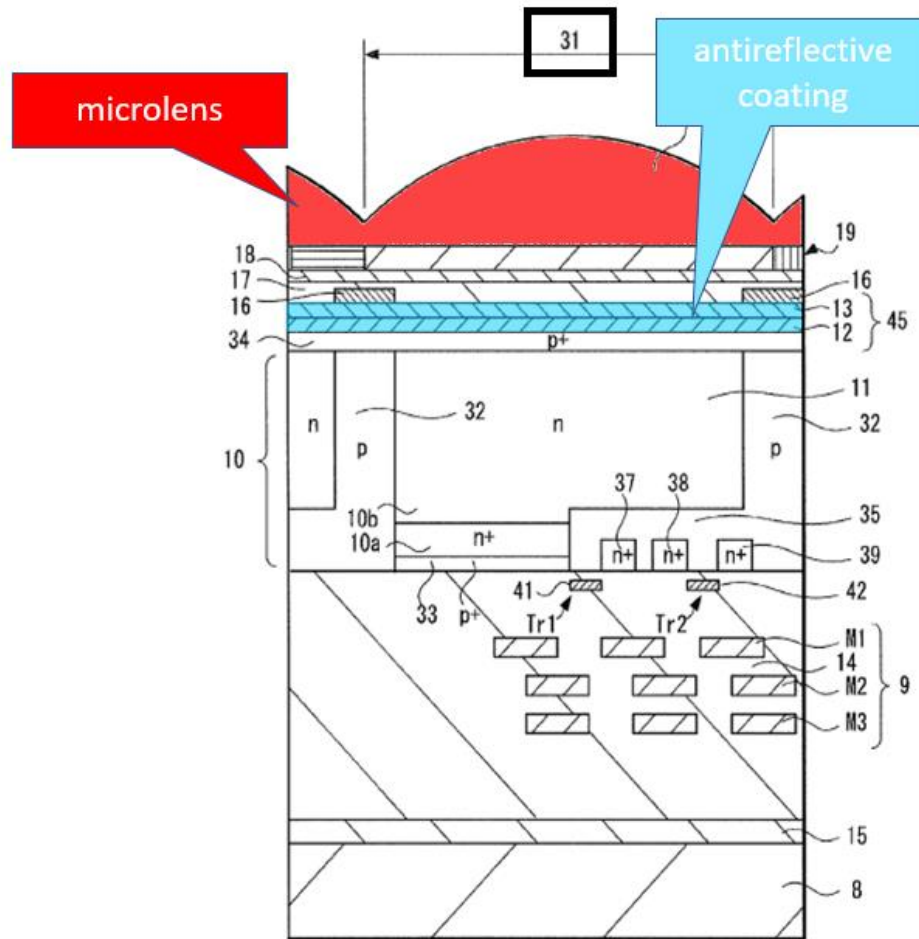
Reasonable expectation of success/predictable results: Designing Lauxtermann's BSI CMOS image sensor to include a microlens and an ARC according to Akiyama's teachings would have been readily accomplished. A POSITA with knowledge of Lauxtermann would have naturally looked to the disclosures of Akiyama when finding ways to improve the efficiency of a BSI CMOS image sensor. Ex. 1003 ¶164. A POSITA would have been motivated to include a microlens and an ARC in Lauxtermann's BSI CMOS image sensor with at

least a reasonable expectation of success because microlenses and ARCs are routinely used in BSI CMOS image sensors and it would have been routine to add these features during the fabrication process. *Id.*

2. Claim 10

10. The BSI CMOS pixel array of claim 1 comprising a micro lens, said absorption area is between said micro lens and said barrier layer.

Lauxtermann combined with Akiyama's disclosure render obvious claim 10. Ex. 1003 ¶¶165-166. It was highly conventional and very well-known that any BSI image sensor with a pixel array would include a microlens. *See, e.g.*, Ex. 1028, 1033-1036, 1059. Further, as shown in FIG. 4 below, Akiyama discloses a BSI CMOS image sensor with a **microlens 21** formed on the backside of a **pixel 31** and over a **photodiode 11**. Ex. 1006, FIG. 4; 5:6-30; 5:55-6:3; Ex. 1003 ¶167.

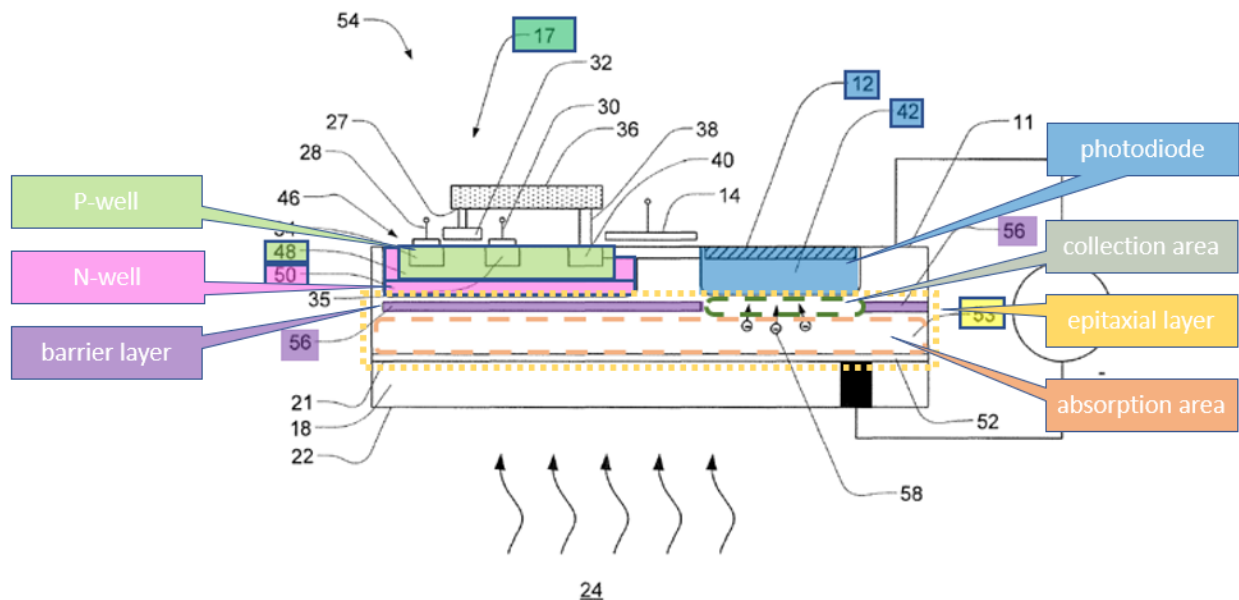


Ex. 1006, FIG. 4.

A POSITA would be motivated to modify Lauxtermann's BSI CMOS image sensor (as shown in FIG. 4 below) in view of Akiyama to include a **microlens** to focus incident light on **photodiode 12** to improve the light collection efficiency of its image sensor. Ex. 1003 ¶168. As discussed in Section III.C., microlenses have been widely employed in CMOS image sensors. Ex. 1020, 1:6-11, 1:17-20.

Further, a POSITA would have placed the microlens before the outermost layer of Lauxtermann's image sensor die in the path of incident light 24 (i.e., below layer 18) because the function of the microlens is to focus incident light before the

light enters the image sensor die. Ex. 1003, ¶169. This is consistent with Akiyama's teachings, where its microlens 21 is located before the outmost layer of its image sensor in the light's path. Ex. 1006, FIG. 4. With this arrangement of the microlens in Lauxtermann's image sensor, **the absorption area in the combination of Lauxtermann and Akiyama is between the micro lens and the barrier layer 56.** Ex. 1003, ¶169.



Ex. 1004, FIG. 4.

3. Claim 11

11. The BSI CMOS pixel array of claim 10 comprising an anti-reflective coating (ARC) layer, said ARC layer is between said micro lens and said absorption area.

Lauxtermann combined with Akiyama's disclosure render obvious claim 11.

Ex. 1003 ¶¶170-171. It was highly conventional and very well-known that any BSI

image sensor with a pixel array would include an ARC layer. *See, e.g.*, Ex. 1028, 1033-1036, 1059. Further, as shown in FIG. 4 below, Akiyama discloses an **antireflective coating (ARC) 45** formed on the backside of a **pixel 31**. Ex. 1006, FIG. 4; 5:6-30; 5:55-6:3; Ex. 1003 ¶172.

As discussed above, a POSITA would be motivated to modify Lauxtermann's BSI CMOS image sensor (as shown in FIG. 4 above) in view of Akiyama to include an **ARC layer** between the microlens and photodiode to improve the light collection efficiency of its **photodiode 12**. Ex. 1003 ¶173. An ARC layer allows more light to pass through from a microlens to a photodiode by minimizing reflection from a component on the backside surface of the image sensor die and the silicon material of the backside surface itself, which would otherwise decrease the efficiency of the device. *Id.*; Ex. 1021, [0013].

Further, a POSITA would have placed the ARC layer between the microlens and absorption area of Lauxtermann's image sensor because the ARC would allow more light to reach the photodiode by minimizing light reflection at the interface between a component on the backside surface of the image sensor die and the silicon material of the backside surface itself. Ex. 1003 ¶174. This is consistent with Akiyama's teachings, where the ARC layer is placed after the **microlens 21** and before the backside of the image sensor die. Ex. 1006, FIG. 4. With this arrangement

of the ARC layer and microlens in Lauxtermann's image sensor, **the ARC layer is between the microlens and the absorption area**. Ex. 1003 ¶174.

XI. GROUND 4: CLAIMS 16-20 ARE OBVIOUS OVER LAUXTERMANN IN VIEW OF WANG

Lauxtermann in view of Wang render obvious claims 16-20 of the '169 patent. Ex. 1003 ¶175.

1. Reasons to Combine Lauxtermann with Wang

Claims 16 and 19 further requires certain peripheral circuitry, claims 17 and 18 further requires a guard ring, and claim 20 further requires that the image sensor be used in a digital camera or smartphone. Wang teaches peripheral circuitry, guard ring, and digital camera that meet the requirements of these claims. A POSITA would have been motivated to modify Lauxtermann to include these teachings and would have had a reasonable expectation of success, for the following reasons. Ex. 1003, ¶176.

Guard ring [claims 17, 18]: A POSITA would have been motivated to include a guard ring in Lauxtermann's BSI CMOS image sensor according to Wang's teaching to reduce crosstalk between neighboring pixels and between the pixel array and any peripheral circuitry. Ex. 1003 ¶177. Without a guard ring 130, Wang discloses that scattered light would reach neighboring pixels 120, "causing crosstalk between various sensor signals." *Id.*; Ex. 1010, 1:51-54. Furthermore, without guard ring 130, Wang discloses light-generated charges from one pixel 120 may drift into

other pixels 120 and peripheral circuitry, such as ASIC control circuit 184. Ex. 1010, 2:12-18; 3:23-26; 7:15-18; 8:10-13. In view of Wang, a POSITA would include a guard ring in Lauxtermann's BSI CMOS image sensor to reduce crosstalk between pixels and between the pixel array and any peripheral circuitry. Ex. 1003, ¶177.

Peripheral circuitry [claim 16, 19]: Moreover, a POSITA would have been motivated to include peripheral circuitry in Lauxtermann's BSI CMOS image sensor according to Wang's teaching to access the pixels in the image sensor. Ex. 1003 ¶178. A POSITA would have understood that charge accumulation in a pixel must be measured by a sensor, and that the measurements from a given pixel's sensor is then used by other circuits to provide color and brightness information. *Id.*; Ex. 1030 at 1:38-41. There is nothing unique about BSI sensors in this regard. Indeed, Wang discloses "an image sensor 300, wherein an[] area 180 ... adjacent to a pixel forming area 182, includes a control circuit, e.g., an ASIC 184, that provides circuitry supporting pixels 120 and external communications to other devices." Ex. 1010, 6:64-7:2. In view of Wang, a POSITA would include a control circuit ASIC in Lauxtermann's BSI CMOS image sensor to access and otherwise support pixels. Ex. 1003, ¶178.

Same field of endeavor: Like the '169 patent, both Lauxtermann and Wang are directed to BSI CMOS image sensors and methods for improving the performances of the image sensors. Ex. 1003, ¶180.

Reasonable expectation of success/predictable results: Designing Lauxtermann's BSI CMOS image sensor to include a guard ring and peripheral circuitry according to Wang's teachings would have been readily accomplished. A POSITA with knowledge of Lauxtermann would have naturally looked to the disclosures of Wang when finding ways to improve the efficiency of a BSI CMOS image sensor and to reduce crosstalk. Ex. 1003 ¶181. A POSITA would have been motivated to include a guard ring and peripheral circuitry in Lauxtermann's BSI CMOS image sensor with at least a reasonable expectation of success because guard rings and peripheral circuitry are routinely used in BSI CMOS image sensors and it would have been routine to add these additional elements during the fabrication process. *Id.*

2. Claim 16

[16pre] A complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) comprising:

To the extent the preamble is limiting, the combination of Lauxtermann and Wang renders it obvious. Lauxtermann teaches a **CMOS** pixel array for the reasons discussed in connection with Ground 1. *See* Section VIII.1 (1pre). Lauxtermann teaches a CMOS image sensor with active pixel circuitry. Ex. 1004, 3:45-47, 4:16-17, 5:19-26. A POSITA would understand the active pixel circuitry is an integrated circuit with transistors formed on a semiconductor substrate in a CMOS fabrication process. . Therefore, Lauxtermann teaches a **CMOS IC**. Ex. 1003 ¶¶182-183.

[16a] a circuitry; and

The combination of Lauxtermann and Wang renders this limitation obvious. It is well-known that an integrated circuit with a CMOS image sensor must comprise circuitry to access and readout the pixel array in the image sensor. Therefore Lauxtermann's disclosed CMOS image sensor would necessarily include circuitry. Ex. 1003, ¶¶184-185.

Further, Wang teaches that its ASIC forming area 180 includes an ASIC control circuit 184 (i.e., **circuitry**) "that provides circuitry supporting pixels 120 and external communications to other devices." Ex. 1010, 6:64-7:2; Ex. 1003 ¶186.

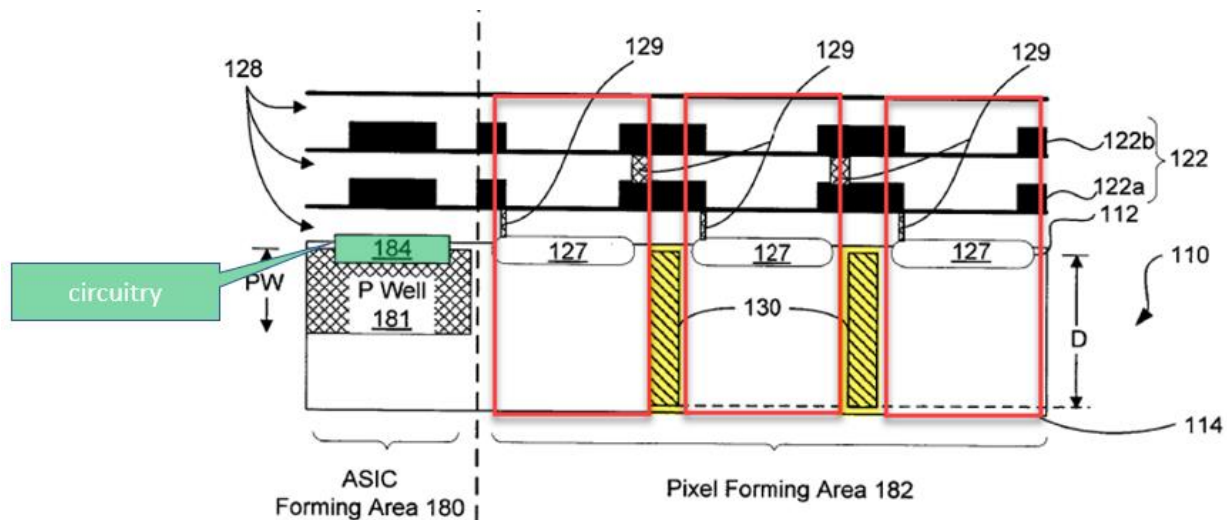


Fig. 4

[16b] a back-side illumination (BSI) pixel array comprising:

Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. See Section VII.1 (1pre).

[16c] a plurality of pixels, a pixel of said plurality of pixels comprising:

Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section VII.1 (1a).

[16d] one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-well (NW) region or a P-well (PW) region;

Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section VII.1 (1b).

[16e] a photodiode;

Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section VII.1 (1c).

[16f] an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to said absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and

Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section VII.1 (1d).

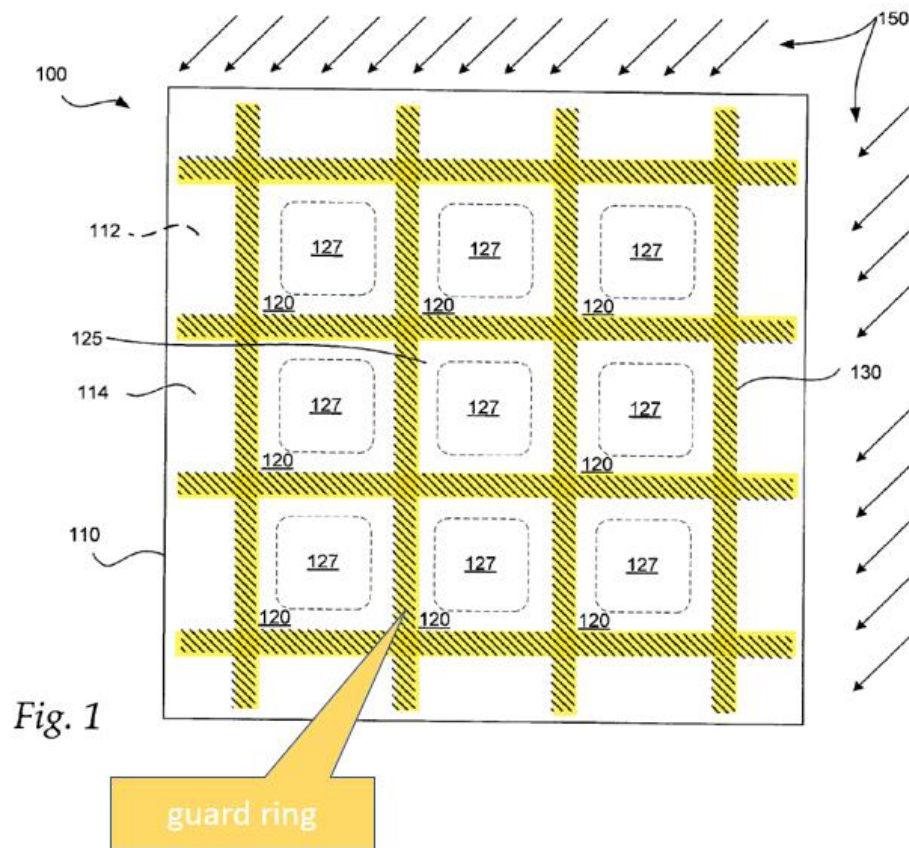
[16g] a barrier layer separating said absorption area from said well regions.

Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section VII.1 (1e).

3. Claim 17

17. The CMOS IC of claim 16 comprising a guard ring separating said circuitry from said BSI pixel array.

The combination of Lauxtermann and Wang renders this limitation obvious. Wang teaches employing a **guard ring** 130 both to separate neighboring pixels 120 (as shown in its figures) and to isolate ASIC 184 (peripheral circuitry) from adjacent pixels 120 (as described). Ex. 1010, 2:16-18, 3:16-26; 4:3-5, 7:15-18; 8:10-13. The guard ring structure is shown in Wang's figures, highlighted in yellow. Ex. 1003, ¶¶193-194.



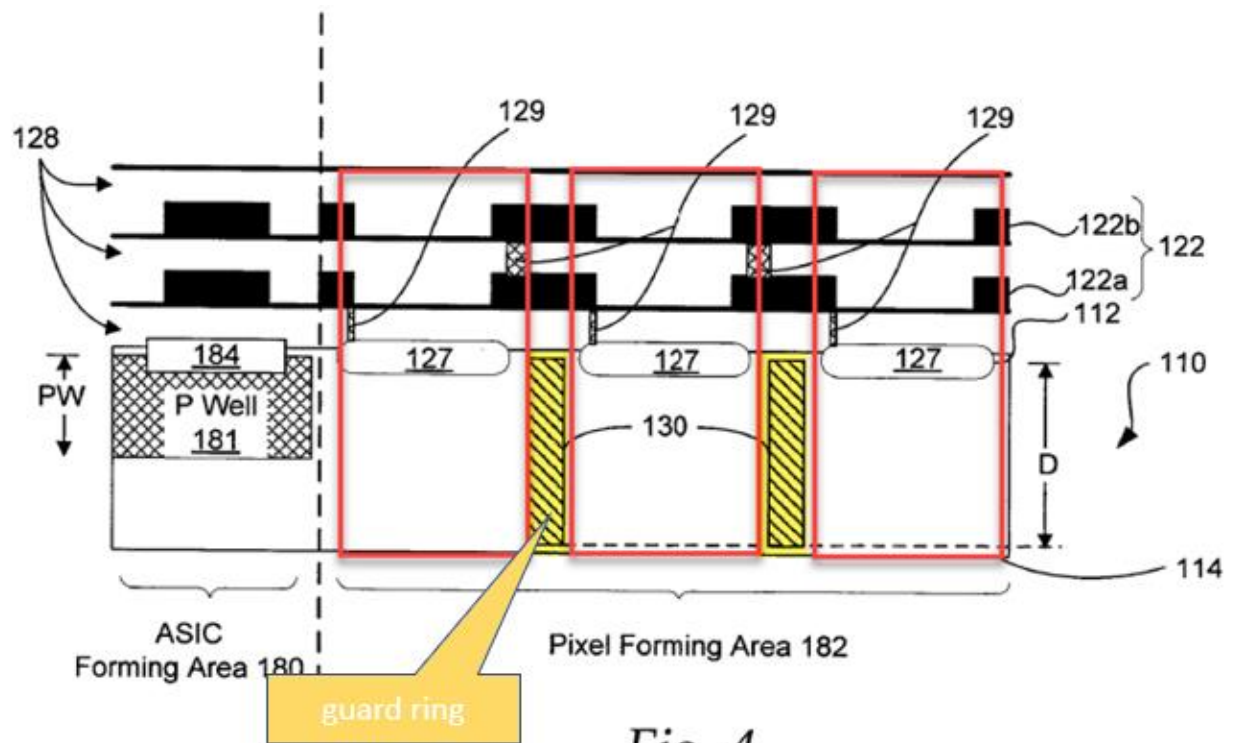


Fig. 4

Wang therefore teaches that the guard ring **separates said circuitry from said BSI pixel array**. It would have been obvious to include Wang's guard ring in Lauxtermann's BSI CMOS image sensor. Ex. 1003 ¶195.

4. Claim 18

18. The CMOS IC of claim 17, wherein said guard ring is configured to prevent diffusion of photoelectrons from said circuitry to said BSI pixel array.

The combination of Lauxtermann and Wang renders this limitation obvious. Wang discloses that the purpose guard ring 130 is to prevent light-generated charge carriers (i.e., **photoelectrons**) from reaching neighboring pixels 120 (i.e., pixels in the **BSI pixel array**). Ex. 10301010, 1:48-54; Ex. 1003 ¶¶196-197. The guard ring

130 also isolates ASIC 184 (circuitry) from adjacent pixels 120 (BSI pixel array) (i.e., it is **configured to prevent diffusion of photoelectrons from said circuitry to said BSI pixel array**). Ex. 1010, 7:15-18; 8:10-13; Ex. 1003 ¶197.

5. Claim 19

[19pre] An imaging device comprising:

To the extent the preamble is limiting, the combination of Lauxtermann and Wang renders it obvious. Wang teaches that BSI sensors are useful in various applications, including “digital cameras.” Ex. 1010, 1:38-41; Ex. 1003 ¶199. A digital camera is an **imaging device**. Ex. 1003 ¶¶198-199; Ex. 1052, 20:13-15 (referring to “an imaging device (camera)”).

[19a] a memory; an input; an output; a processor; and

The combination of Lauxtermann and Wang renders this limitation obvious. Wang teaches the use of CMOS sensors in digital cameras. Ex. 1010, 1:38-41; Ex. 1003 ¶¶200-201. A POSITA would understand that **a memory, an input, an output, and a processor** are necessarily components of a digital camera. At a minimum, it would have been obvious to a POSITA that a digital camera utilizing CMOS sensors would include these four components. Ex. 1003 ¶201.

[19b] a complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) comprising:

The combination of Lauxtermann and Wang renders obvious this limitation for the reasons discussed in connection with claim 16. *See* Section XII.2 (16pre).

[19c] a circuitry; and

The combination of Lauxtermann and Wang renders obvious this limitation for the reasons discussed in connection with claim 16. *See* Section XII.2 (16a).

[19d] a back-side illumination (BSI) pixel array comprising:

Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section VII.1 (1pre).

[19e] a plurality of pixels, a pixel of said plurality of pixel sensors comprising:

Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section VII.1 (1a).

[19f] one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-well (NW) region or a P-well (PW) region;

Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section VII.1 (1b).

[19g] a photodiode;

Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section VII.1 (1c).

[19h] an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to said absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and

Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section VII.1 (1d).

[19i] a barrier layer separating said absorption area from said well regions.

Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section VII.1 (1e).

6. Claim 20

20. The imaging device of claim 19 comprising a digital camera or a Smartphone.

The combination of Lauxtermann and Wang renders this limitation obvious. Wang teaches the use of BSI sensors in **digital cameras**. Ex. 1010, 1:38-41; Ex. 1003 ¶210.

XII. GROUND 5: CLAIMS 1, 3-8, AND 12-15 ARE OBVIOUS IN VIEW OF BALLIN

Ballin renders obvious claims 1, 3-8, 12-13, and 15 of the '169 patent. Ex. 1003 ¶211.

1. Claim 1

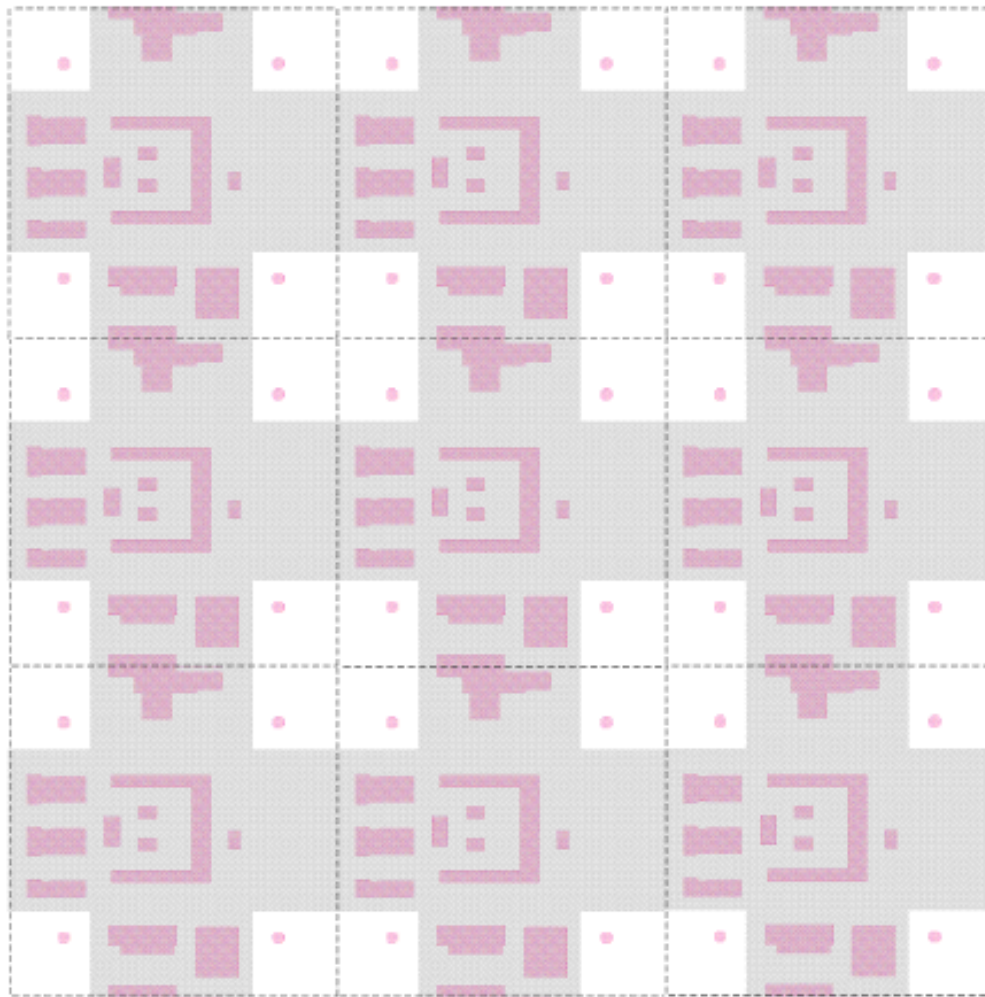
(a) [1pre]

To the extent the preamble is considered to be a limitation, Ballin discloses a BSI CMOS pixel array. Ex. 1003 ¶212. Ballin discloses its monolithic active pixel sensors (MAPS) include **CMOS pixels**, and the image sensor can be “**back-illuminated sensors**.” Ex. 1007, Title, 5339, FIG. 2. Ballin’s FIG. 2 illustrates one pixel of a **BSI CMOS image sensor**, where each pixel includes at least a photodiode and an NMOS transistor, a PMOS transistor, and a deep P-well implant in an epitaxial layer. Ex. 1007, 5338-39, FIG. 2; Ex. 1003, ¶213.

(b) [1a]

Ballin discloses a plurality of pixels. Ballin’s FIG. 5 (below) illustrates that that its BSI CMOS pixel array comprises **a plurality of pixels**, particularly a 3x3 pixel array. Ex. 1003 ¶¶214-215.

Figure 5. Layout of a 3x3 array of *preShape* pixel from the TPAC1.0 sensor. Only the N-well (purple) and deep P-well (grey) layers are shown. Every N- well but the detecting diodes have got deep P-well underneath. The non-physical boudary between pixels is shown as a dotted line.



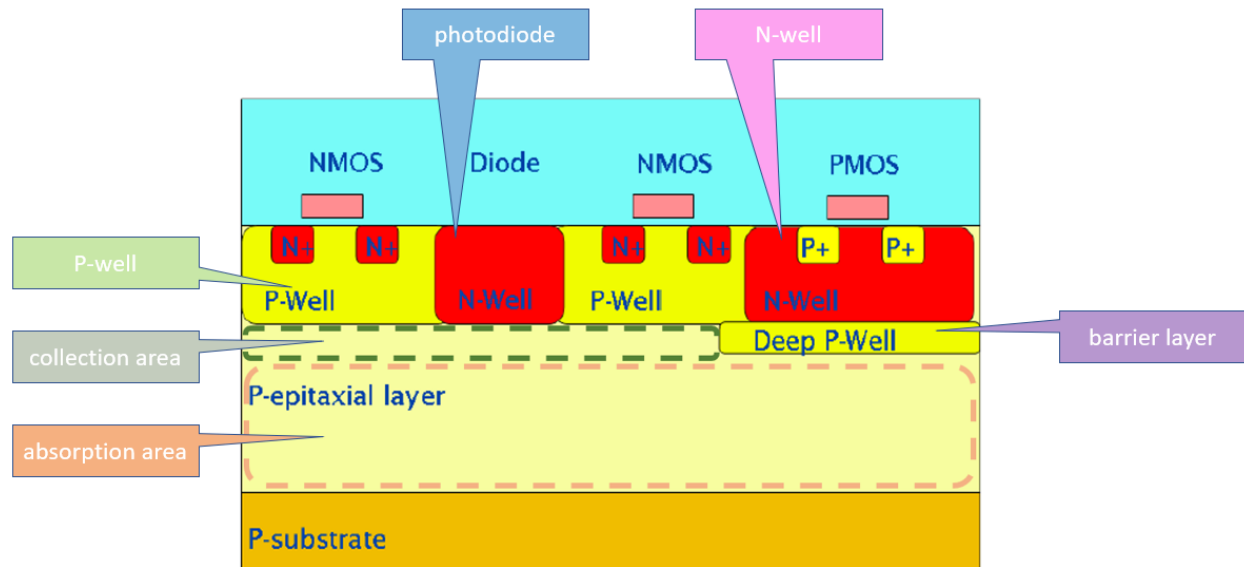
Ex. 1007, FIG. 5.

(c) [1b]

Ballin discloses one or more MOS transistors with N-well or P-well regions.

Ballin discloses that a pixel of its BSI CMOS image sensor includes at least two

NMOS transistors and a **PMOS transistor**. Ex. 1003 ¶¶216-217; Ex. 1007, FIG. 2, 5338, 5340.



Ex. 1007, FIG. 2.

As shown in FIG. 2 above, Ballin discloses that its two NMOS transistors are formed with two **P-well regions** and a PMOS transistor is formed with an **N-well region**. *Id.*, 5338; Ex. 1003 ¶218.

(d) [1c]

Ballin discloses a photodiode. Ballin discloses that a pixel of its BSI CMOS image sensor includes a least one N-well diode (i.e., **photodiode**) and teaches that pinned **photodiodes** have been used in CMOS sensors. Ex. 1003 ¶¶219-220; Ex. 1007, Fig. 2, 5337-38.

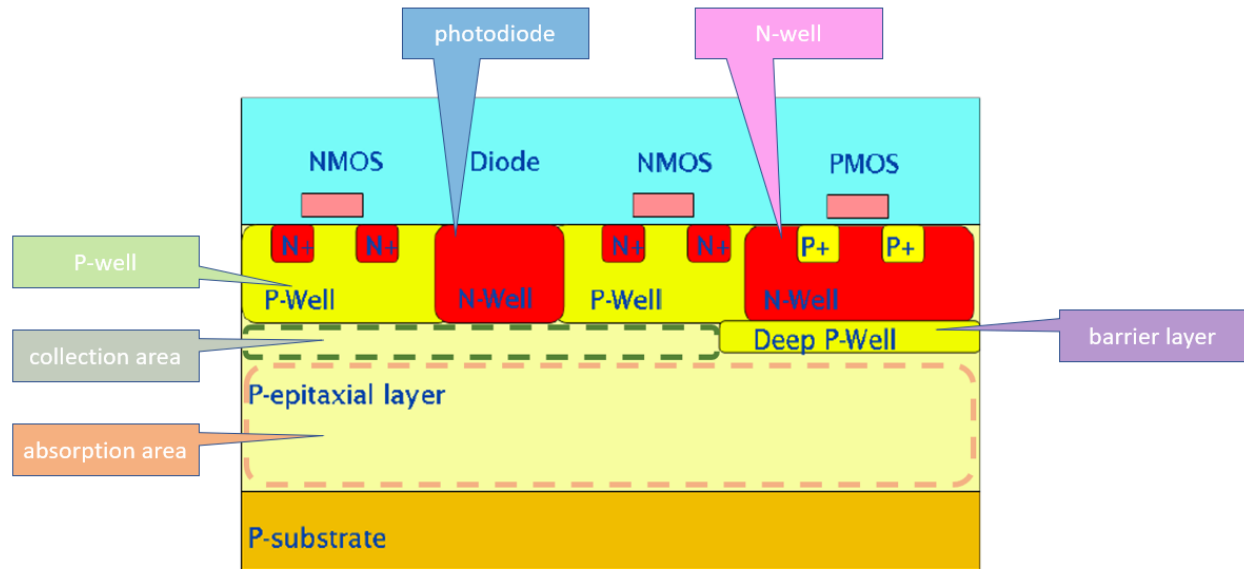
(e) [1d]

Ballin renders obvious claim 1d. Ex. 1003 ¶221.

An epitaxial layer: Ballin discloses that a pixel of its image sensor includes “a P-doped **epitaxial layer** . . . whose thickness is typically up to 20 μm.” Ex. 1007, FIG. 2, 5338; Ex. 1003, ¶222.

Comprising an absorption area and a collection area: The annotated FIG. 2 below discloses an epitaxial layer that includes an **absorption area** and a **collection area**,⁴ the latter of which connects the absorption area to a photodiode. Just like the absorption area 222 in Figure 2 of the ’169 patent, the identified **absorption area** in Ballin is a part of the epitaxial layer generally located below **the deep p-wells (barrier)** of the pixels. Just like the collection area 224 in Figure 2 of the ’169 patent, the identified **collection area** in Lauxtermann is a part of the epitaxial layer generally located adjacent to the **deep p-wells (barriers)** and under the **photodiode**. Ex. 1003, ¶223.

⁴ According to the plain language of the claims, absorption **area** and collection **area** are parts of the epitaxial **layer**. They need not be separate layers.

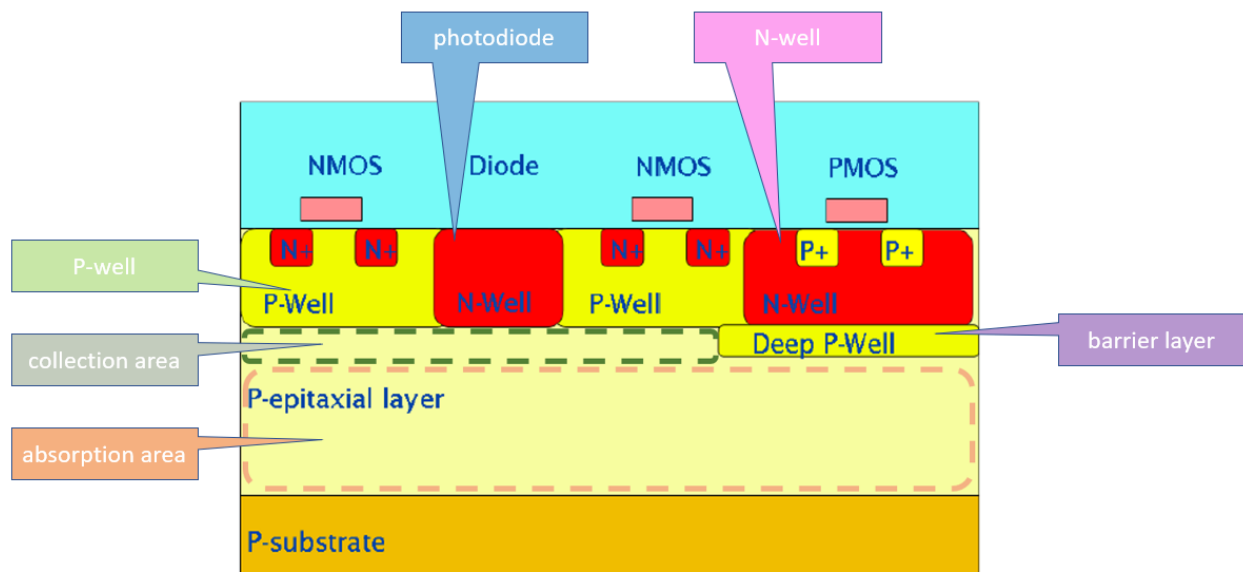


Ex. 1007, FIG. 2.

The absorption area is configured **to absorb incoming photons** (from light incident on the P-substrate) and **generate charges** (i.e., electrons) **by means of the photoelectric effect**. Ex. 1003 ¶224. Just like the absorption area 222 in Figure 2 of the '169 patent, the identified **absorption area** in Ballin is a part of **P-epitaxial layer** generally located below **deep P-wells (barriers)**. The **collection area** connects the **absorption area** to the **photodiode** to provide the collected charges to the **photodiode**. *Id.* A POSITA would understand that the collection area collects the charges from the absorption area and funnels them towards the photodiode in conjunction with the deep P-wells (since the deep P-wells repel the charges). *Id.* And just like the collection area 224 in Figure 2 of the '169 patent, the identified **collection area** in Ballin is a part of **P-epitaxial layer** generally located adjacent to **deep P-wells (barriers)** (e.g., between them) and under the **photodiode**. *Id.*

(f) [1e]

Ballin renders obvious claim 1e. Ballin discloses that a “novel approach for isolating the N-wells of PMOS transistors from the epitaxial layer ... by adding a **deep P implant**,” and that “[b]y adding the **deep P-well layer underneath all the N-wells used as substrate for PMOS transistors**, it is then possible to keep the collecting PN diode junction [i.e., **photodiode**] as the only one in the pixel that is exposed to the epitaxial layer.” Ex. 1007, 5339-40, FIG. 2 (annotated below). Ex. 1003 ¶¶225-226.



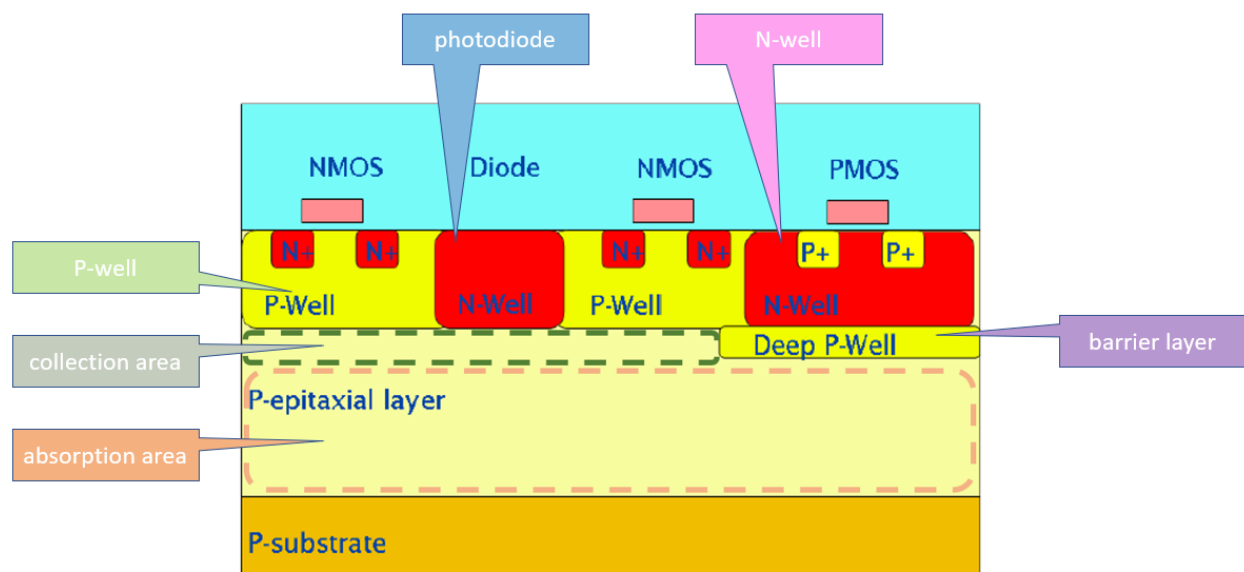
Ex. 1007, FIG. 2.

As shown in FIG. 2, Ballin’s deep P-well separates the **N-wells** of the PMOS transistors from the P-epitaxial layer, which comprises the **collection** and **absorption** areas. A POSITA would understand that Ballin’s deep P-well implant is

a **barrier layer** separating the **absorption area** from the one or more well regions. Ex. 1003 ¶227.

2. Claim 3

Ballin renders obvious claim 3. Ballin's **collection area** extends from the **absorption area** to the photodiode (N-well diode) through the **barrier layer** (deep P-well implant). Ex. 1007, FIG. 2; Ex. 1003 ¶¶228-229.



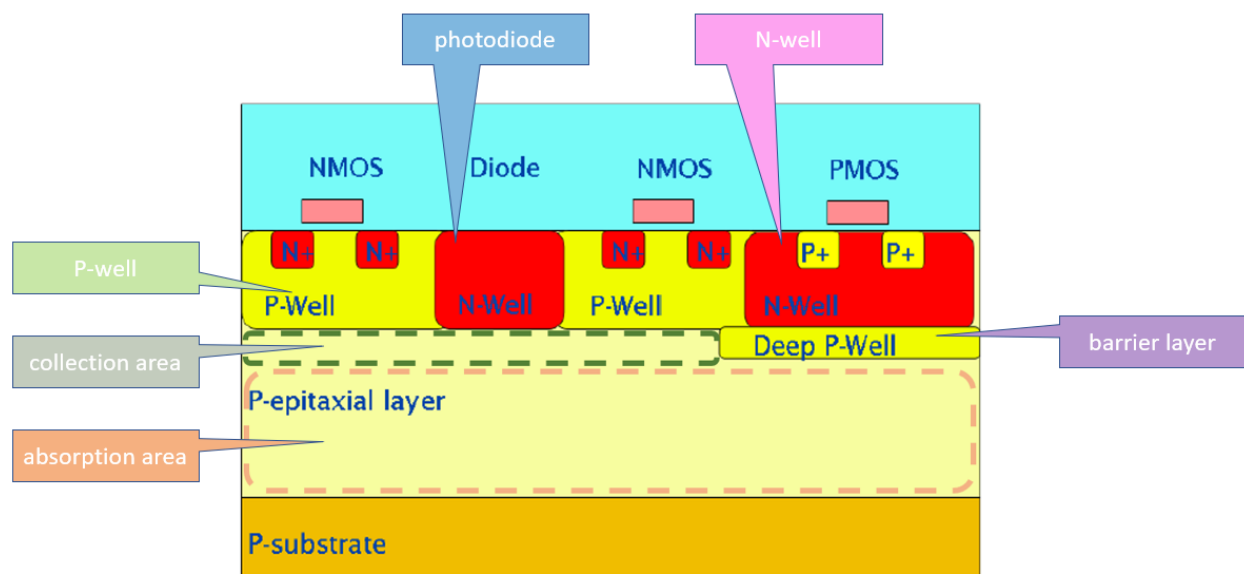
Ex. 1007, FIG. 2.

3. Claim 4

Ballin renders obvious claim 4. Ex. 1003, ¶¶230-231. As known in the art, an electrostatic lens creates an electric field to guide electrons towards a detector. Exs. 1016; 1057, 6:11-12, 6:65-7:5; 1058.

In Ballin, the area below the N-well diode and below the P-wells (the area in between the deep P-wells, which functions as a **barrier layer**) serves as a **collection**

area collecting electrons from the absorption area and then guides/directs the collected electrons to the photodiode (N-well diode). Ex. 1003, ¶231. Ballin's collection area is configured to perform as an electrostatic lens because the deep P-wells create electric fields that cause the collection area to become an electron funnel that collects and guides electrons to the photodiode. *Id.* This is the functionality of the electrostatic lens according to the '169 patent. Ex. 1001, 7:23-32. Therefore, Ballin's collection area is configured to perform the functionality of an electrostatic lens. Ex. 1003 ¶¶230-231.

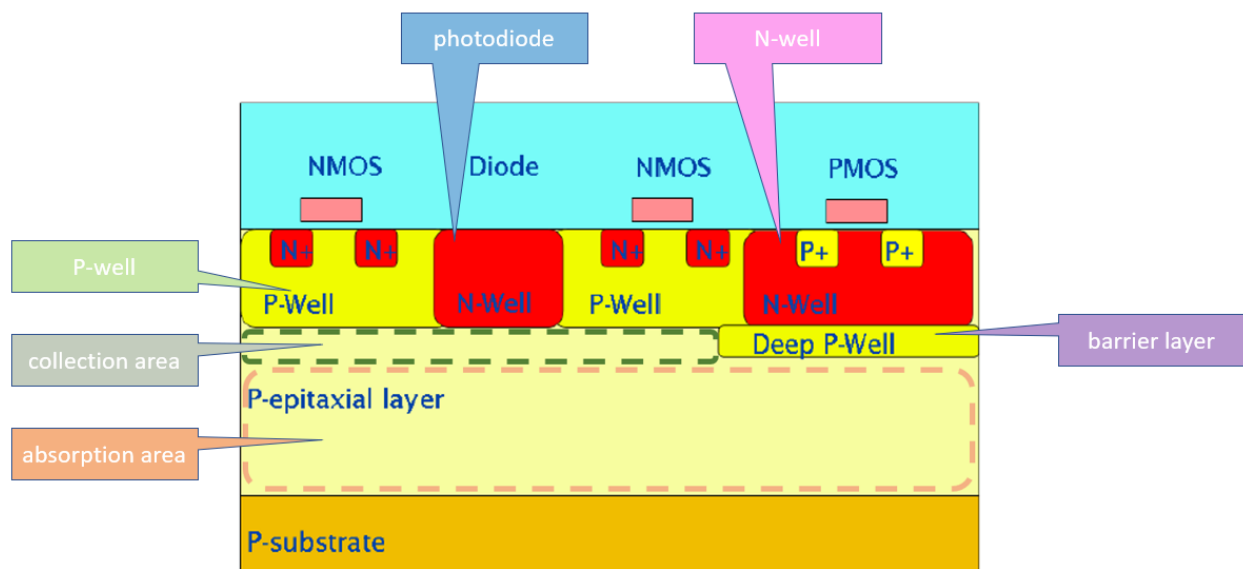


Ex. 1007, FIG. 2.

4. Claim 5

Ballin proposes a “novel approach for isolating the N-wells of PMOS transistors from the epitaxial layer ... by adding a **deep P implant**,” and that “[b]y adding the **deep P-well layer underneath all the N-wells** used as substrate for

PMOS transistors, it is then possible to keep the collecting PN diode junction [i.e., photodiode] as the only one in the pixel that is exposed to the epitaxial layer.” . 1007, 5339-40, FIG. 2. This deep P-well is **configured to prevent diffusion of electrons from the absorption area to the well regions** because without it, charges would diffuse towards the N-well region of the PMOS above. Ex. 103 ¶¶232-233. A POSITA would understand that Ballin’s deep P-well implant is the claimed **barrier layer**. *Id.*



Ex. 1007, FIG. 2.

5. Claim 6

Ballin discloses that its P-doped epitaxial layer has a thickness “typically **up to 20 μm .**” Ex. 1007, 5338. Ballin therefore discloses that **a thickness of its epi layer is at least 4 micron (μm).** Ex. 1003 ¶¶234-235.

6. Claim 7

Ballin discloses that its P-doped epitaxial layer has a thickness “typically **up to 20 μm .**” Ex. 1007, 5338. Ballin therefore discloses that **a thickness of its epi layer is at least 10 micron (μm).** Ex. 1003 ¶¶236-237.

7. Claim 8

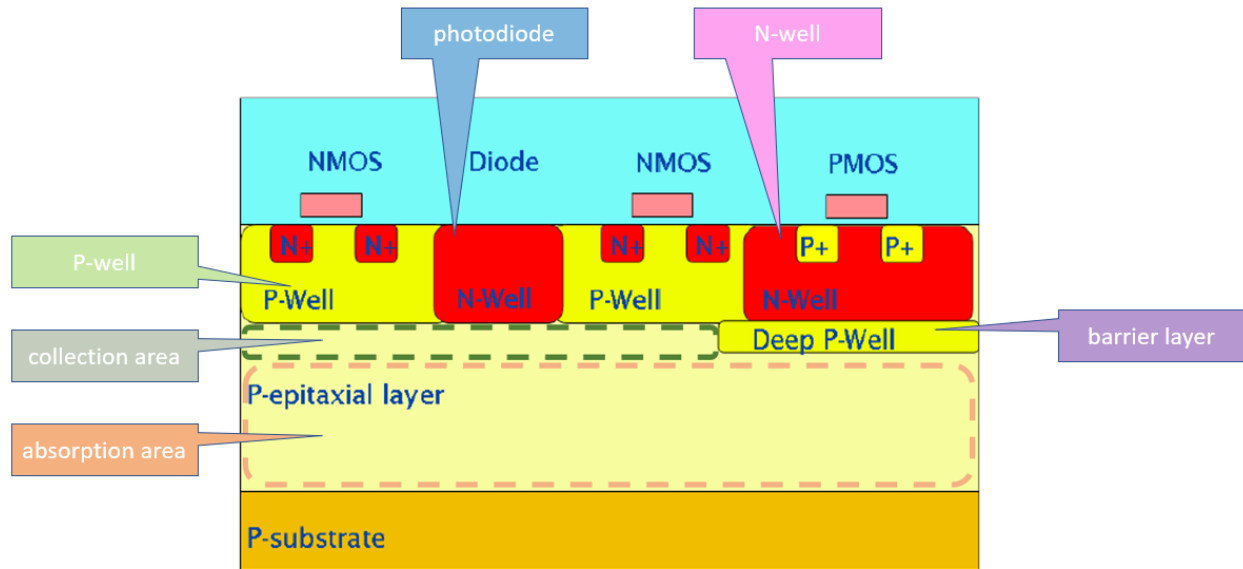
Ballin discloses that its P-doped epitaxial layer has a thickness “typically **up to 20 μm .**” Ex. 1007, 5338. Ballin therefore discloses that **a thickness of its epi layer is at least 15 micron (μm).** Ex. 1003 ¶¶238-239

8. Claim 12

Ballin discloses that each pixel of its image sensor may include at least two NMOS transistors and one PMOS transistor. Ex. 1007, FIG. 2, 5340. Ballin therefore discloses **one or more transistors selected from a group consisting of one or more P-type MOS (PMOS) transistors and one or more N-type MOS (NMOS) transistors.** Ex. 1003 ¶¶240-241.

9. Claim 13

Ballin renders obvious claim 13. Ex. 1003 ¶¶242-243. In particular, Ballin discloses that each pixel of its image sensor includes a “**deep P-well implant**” located underneath the N-well that acts as a barrier layer. Ex. 1007, FIG. 2, 5340. A “PW” implant is a “p-well” implant according to the ’169 patent. Ex. 1001, 4:30-32, 9:20-21, 9:52-56, FIGs. 3C-3D; Ex. 1003 ¶243.



Ex. 1007, FIG. 2.

10. Claim 14

Ballin renders obvious claim 14. Ex. 1003 ¶¶244-245. In particular, Ballin discloses that its pixel includes a **deep P-well implant** (i.e., **barrier layer**) underneath each PMOS N-well in the pixel. Ex. 1007, FIG. 2, 5339-40. A POSITA would understand boron is the most common p-type dopant. Ex. 1003, ¶245; Ex. 1024, 467; Ex. 1025, 31; Ex. 1026, 4:24-30; Ex. 1027, [0059], [0106], [0107]. Thus, it would have been obvious to a POSITA to use **boron implant** for Ballin's deep P-well implant. Ex. 1003 ¶245.

11. Claim 15

Ballin renders obvious claim 15. Ex. 1003 ¶¶246-247. A POSITA would have understood that when a photodiode is referred to as “pinned,” that photodiode is **fully pinned**. *Id.*; see Ex. 1028, Ex. 1029, Fig. 2. It was well-known that pinned

photodiodes were used in almost all CCD and CMOS image sensors. Ex. 1028, Abstract, 34.

Ballin discloses that each pixel includes an N-well diode (i.e., photodiode). Ex. 1007, FG. 2. Ballin further discloses that as pixels are fabricated in smaller and smaller sizes, “electronic noise and leakage current have had to be greatly improved, in particular through the introduction of **pinned photodiode** and transfer gates.” *Id.*, 5337. And it was well-known that fully pinned photodiodes have low noise, high quantum efficiency and low dark current. Ex. 1028, p. 33. Therefore, it would have been obvious for a POSITA to use a **fully pinned diode** for Ballin’s N-well diode, as opposed to a partially or non-pinned photodiode. Ex. 1003 ¶248.

XIII. GROUND 6: CLAIMS 10 AND 11 ARE OBVIOUS OVER BALLIN IN VIEW OF AKIYAMA

Ballin in view of Akiyama render obvious claims 10 and 11 of the ’169 patent. Ex. 1003 ¶249.

1. Reasons to Combine Ballin with Akiyama

Claim 10 further requires a microlens and claim 11 further requires antireflective coating (ARC) layer. Akiyama teaches both a microlens and an ARC layer. A POSITA would have been motivated to include a microlens and an ARC in Ballin’s BSI CMOS image sensor according to Akiyama’s teachings to improve the efficiency of its image sensor. Ex. 1003 ¶250.

Micro lens [claim 10] and ARC layer [claim 11]: A POSITA would have understood that microlens arrays are widely used in CCD and CMOS image sensors so that light incident on each microlens is focused towards a corresponding photodiode. *Id.*, ¶251. A POSITA would also have understood that ARC allows more light to pass through from a microlens to a photodiode by minimizing reflection caused by the difference in refractive indices of components on the light-receiving surface (i.e., backside) of the image sensor die, which would otherwise decrease the efficiency of the image sensor. *Id.* Thus, a POSITA would have been motivated to incorporate a microlens and an ARC into Ballin's image sensor according to Akiyama's teachings to improve light collection efficiency of its image sensor. *Id.*

Same field of endeavor: Like the '169 patent, both Ballin and Akiyama are directed to BSI CMOS image sensors and methods for improving the performances of the image sensors. Ballin and Akiyama disclose BSI CMOS image sensors that have very similar structures with each other. Ex. 1003, ¶253.

Reasonable expectation of success/predictable results: Designing Ballin's CMOS image sensor to include a microlens and an ARC according to Akiyama's teachings would have been readily accomplished. Ex. 1003 ¶254. A POSITA would have been motivated to include a microlens and an ARC in Ballin's CMOS image sensor with at least a reasonable expectation of success because microlenses and

ARCs are routinely used in image sensors and it would have been routine to add these features in the fabrication process. *Id.*

2. Claim 10

Akiyama discloses the microlens for the same reasons discussed in Ground 3. *See* Section X.2. A POSITA would have placed the microlens before Ballin's image sensor die in the light's path (i.e., below the P-substrate) because the function of a microlens is to focus incident light before the light enters the image sensor die. Ex. 1003, ¶¶255-257.

3. Claim 11

Akiyama discloses the ARC lens for the same reasons discussed in Ground 3. *See* Section X.3. A POSITA would have placed the ARC layer after the microlens but before the backside of Ballin's image sensor die in the light's path (i.e., above the microlens and below the p-substrate) because the ARC allows more light from the microlens to pass through and reach the photodiode by reducing reflections between a component on the backside and the silicon material of the backside surface itself. Ex. 1003 ¶¶258-261.

XIV. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies pursuant to Rule 42.104(a) that the '169 patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR of the Challenged Claims on the grounds identified in this Petition.⁵

XV. MANDATORY NOTICES AND FEES

A. Real Party-In-Interest

The real parties-in-interests here is Taiwan Semiconductor Manufacturing Company Limited. No other parties directed, controlled, or funded this *Inter Partes* Review proceeding (IPR).

B. Related Matters

The '169 patent is the subject of the following civil action: *Alidouble Inc. v. Taiwan Semiconductor Manufacturing Company Limited*, No. 2:22-cv-00298-JRG (E.D. Tex.).

⁵ Alidouble first sued TSMC on the '169 patent on December 14, 2021. *Alidouble Inc. v. Taiwan Semiconductor Manufacturing Company Limited*, No. 2:21-cv-00452-JRG (E.D. Tex.). TSMC was served with the Complaint in that action on December 16, 2021. *Id.*, ECF No. 6. The instant IPR petition is therefore being filed prior to the 1-year bar. 35 U.S.C. § 315(b).

C. Counsel and Service Information

Pursuant to 37 C.F.R. §42.8(b)(3) and 42.10(a), Petitioner provides the following counsel and service information. Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney accompanies this Petition.

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Petitioner consents to electronic service directed to the following email address: qe-tsmc-alidouble-ips@quinnemanuel.com.

D. Payment of Fees

The Office is authorized to charge fees for this Petition to Deposit Account No. 50-5708. Any additional fees that might be due are also authorized.

XVI. DISCRETIONARY ANALYSIS FOR REVIEW

The Board has discretion to deny institution under §314(a) and/or §325(d). However, in addition to the strong merits presented herein, Petitioner also hereby provides a *Sotera*-type stipulation and stipulates that if the PTAB institutes *inter partes* review in relation to any petition filed by TSMC with respect to the '169 patent, the Petitioner will not pursue in the district court litigation any ground raised or that could have been reasonably raised in the instituted IPR with respect to the patent claim subject to the instituted IPR. This stipulation precludes discretionary denial under §314(a). See Director Vidal Memorandum, Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, at 3-5, 7-8 (June 21, 2022).

Regarding §325(d), the '169 patent has not previously been challenged at the PTAB. Nor was any reference relied upon herein as part of any ground cited during prosecution or considered by the Examiner. Accordingly, discretionary denial under §325(d) and *General Plastic* is not warranted.

XVII. CONCLUSION

For at least the foregoing reasons, Petitioner requests institution of an IPR and cancellation of the Challenged Claims.

Date: December 16, 2022

Respectfully submitted,

By: /s/ James M. Glass
James M. Glass

Counsel for Petitioner

**CERTIFICATE OF COMPLIANCE WITH
TYPE-VOLUME LIMITATION, TYPEFACE REQUIREMENTS,
AND TYPE STYLE REQUIREMENTS**

1. This Petition complies with the type-volume limitation of 14,000 words, comprising 13,778 words, as counted using the Microsoft Word software that was used to prepare this paper, excluding the parts exempted by 37 C.F.R. § 42.24(a).

2. This Petition complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word in 14-point Times New Roman font.

Date: December 16, 2022

By: /s/ James M. Glass
James M. Glass

Counsel for Petitioner

CERTIFICATE OF SERVICE

The undersigned hereby certifies that on December 16, 2022, true and correct copies of the foregoing document and supporting materials were served in its entirety on the Patent Owner at the following address of record listed on the USPTO's Patent Center via FedEx Overnight:

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Date: December 16, 2022

By: /s/ James M. Glass

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