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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	TJZ1-P-00859-US
		Application Number	
Title of Invention	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
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	Assaf		Lahav		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Binyamina	Country of Residenceⁱ	IL		

Mailing Address of Inventor:

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Address 2					
City	Binyamina	State/Province			
Postal Code	30500	Countryⁱ	IL		

Inventor 2					Remove
Legal Name					
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	Amos		Fenigstein		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	TJZ1-P-00859-US
		Application Number	
Title of Invention	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY		

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Customer Number	86530		
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Application Information:

Title of the Invention	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY		
Attorney Docket Number	TJZ1-P-00859-US	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	6	Suggested Figure for Publication (if any)	

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

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Customer Number	86530		

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	TJZ1-P-00859-US
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Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the application number blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62021152	2014-07-06
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

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This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ^j (if applicable)
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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	TJZ1-P-00859-US
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☒ Authorization to Permit Access to the Instant Application by the Participating Offices
If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application. In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application. In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

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If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.		
Clear		
☒ Assignee	☐ Legal Representative under 35 U.S.C. 117	☐ Joint Inventor
☐ Person to whom the inventor is obligated to assign.	☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:		
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If the Applicant is an Organization check here. ☒		
Organization Name	Tower Semiconductor Ltd.	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	TJZ1-P-00859-US
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Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button. Add			

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	TJZ1-P-00859-US
		Application Number	
Title of Invention	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY		

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NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	/Naim Shichrur/		Date (YYYY-MM-DD)	2015-07-06	
First Name	Naim	Last Name	Shichrur	Registration Number	56248

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

**Title of
Invention**

APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI)
COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY

As the below named inventor, I hereby declare that:

This declaration ☒ The attached application, or
is directed to:

☐ United States application or PCT international application number _____
filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

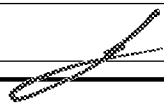
I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

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LEGAL NAME OF INVENTOR

Inventor: Amos Fenigstein Date (Optional) : _____

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

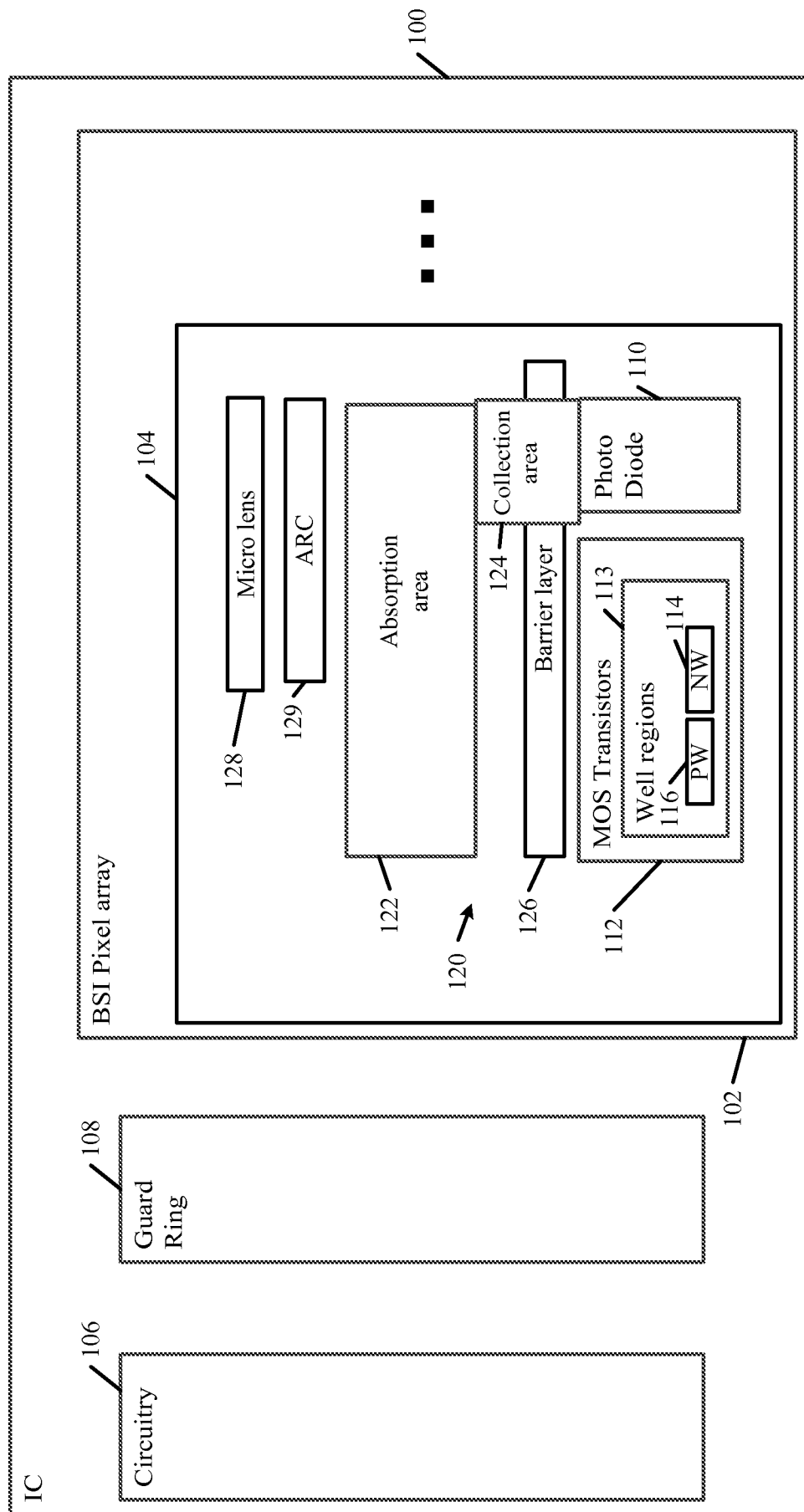


Fig. 1

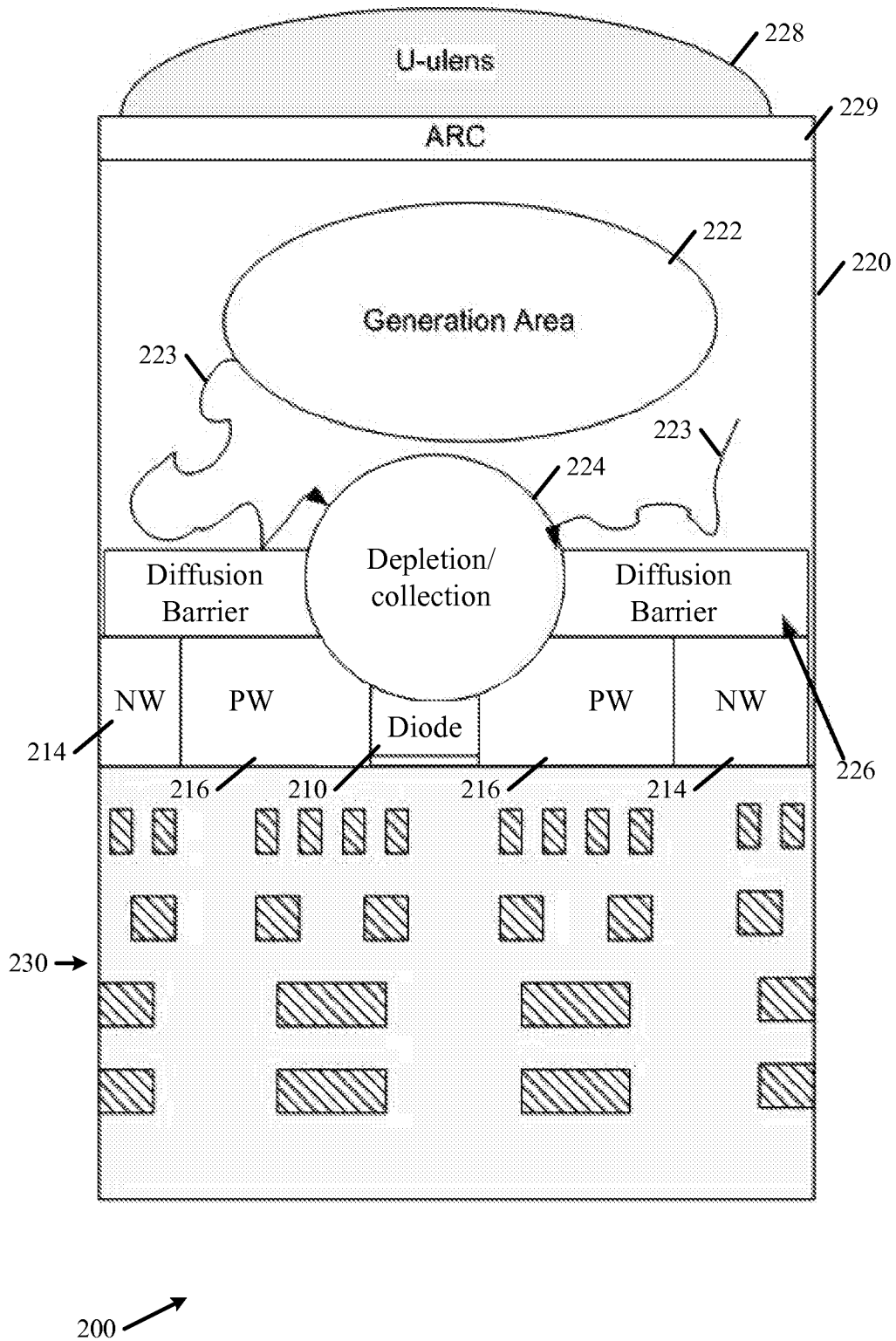
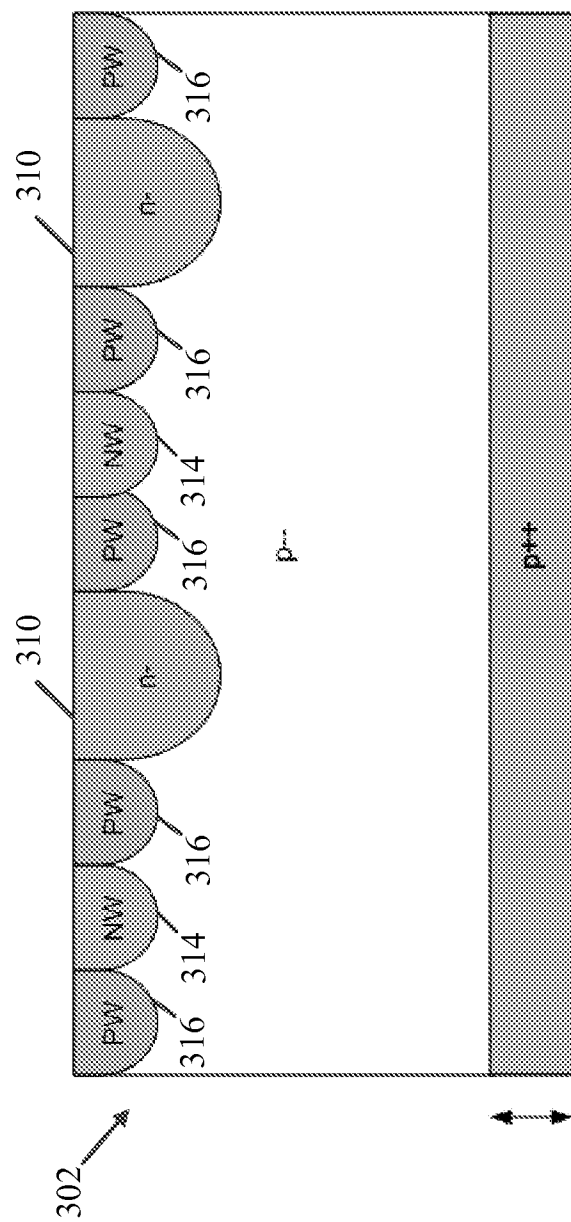
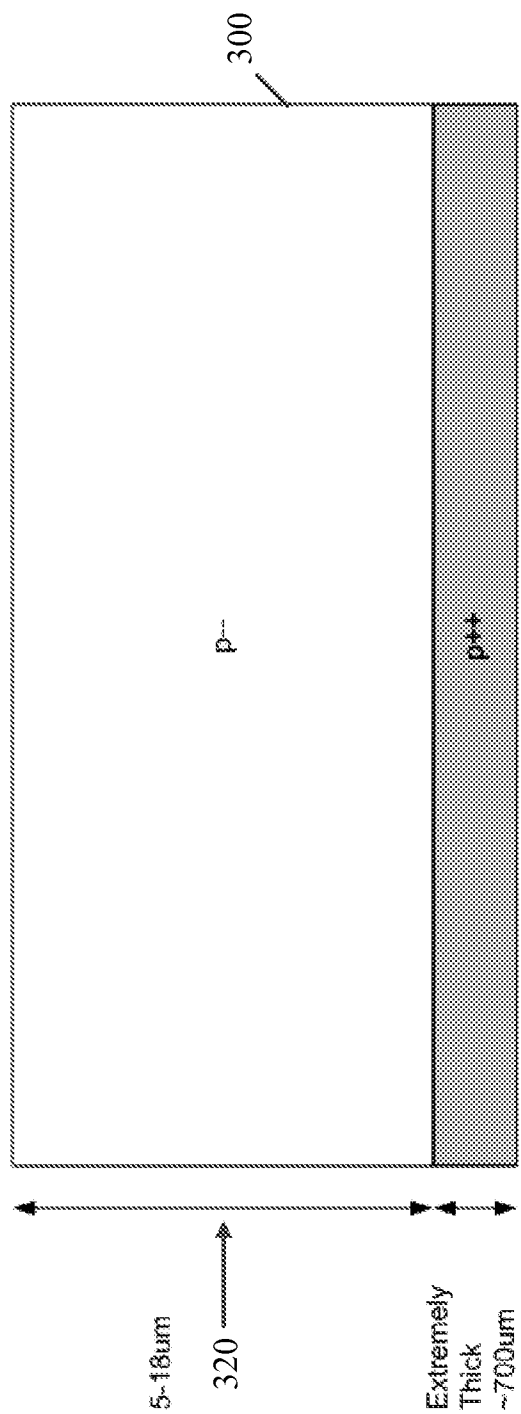


Fig. 2





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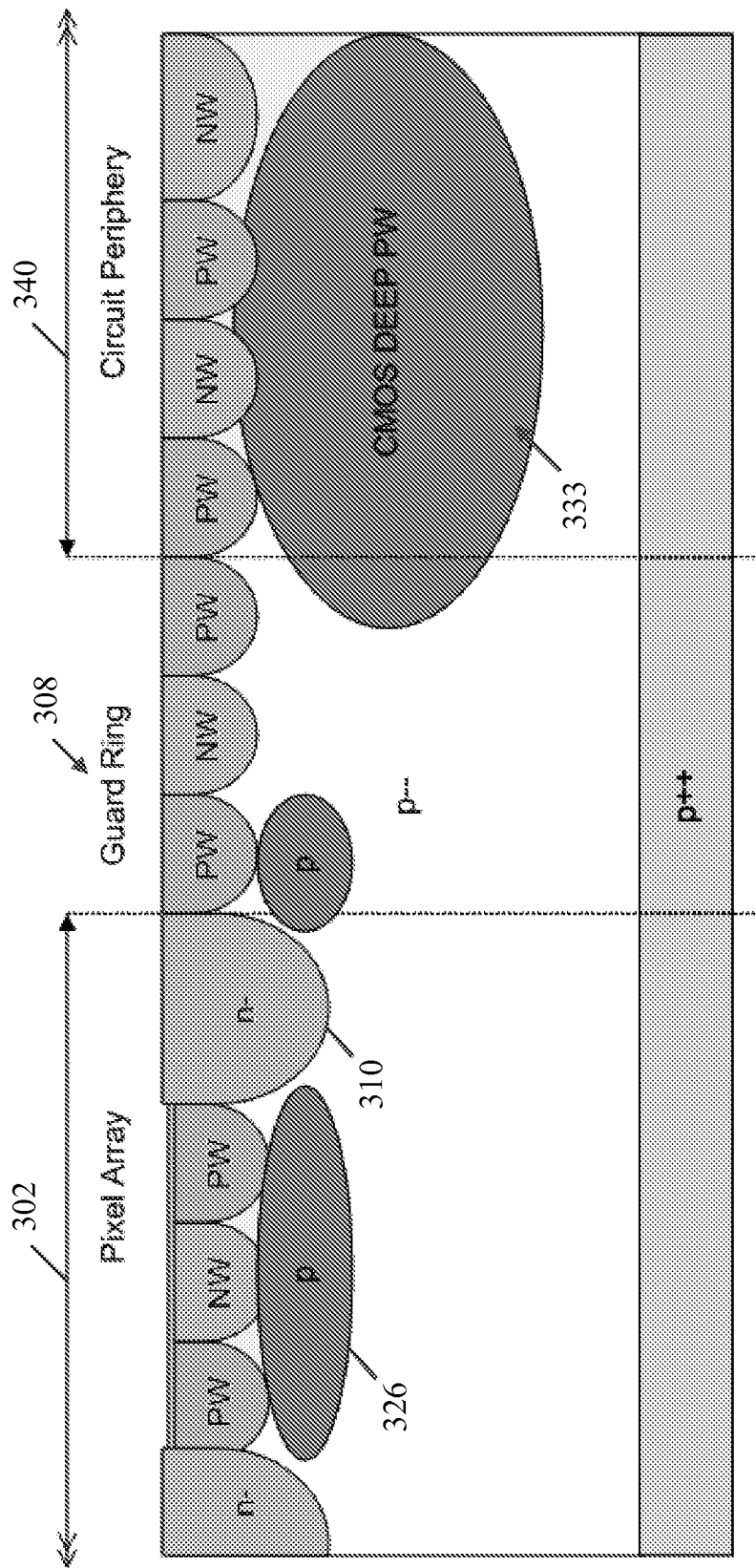


Fig. 3D

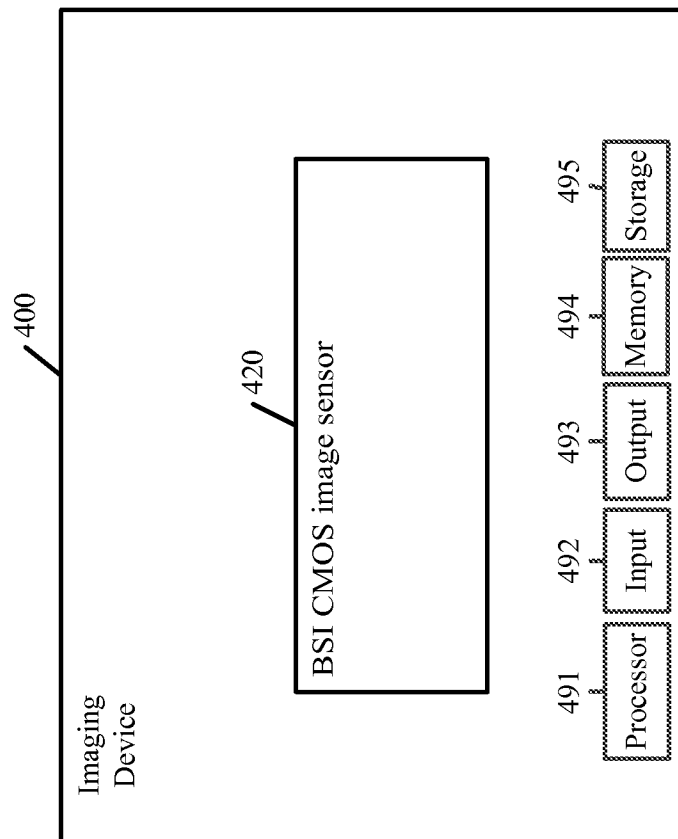


Fig. 4

UNITED STATES PATENT APPLICATION

FOR

**APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI)
COMPLEMENTARY METAL–OXIDE–SEMICONDUCTOR (CMOS) PIXEL
ARRAY**

INVENTOR(S):

**ASSAF LAHAV
AMOS FENIGSTEIN**

Prepared by Shichrur & Co.
ATTORNEY DOCKET TJZ1-P-00859-US
Client Reference TSL-211

**APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI)
COMPLEMENTARY METAL–OXIDE–SEMICONDUCTOR (CMOS) PIXEL
ARRAY**

CROSS REFERENCE

[001] This Application claims the benefit of and priority of US Provisional Patent Application No. 62/021,152 entitled “Apparatus, System and Method of Back Side Illumination Pixel Sensor”, filed July 06, 2014, the entire disclosure of which is incorporated herein by reference.

TECHNICAL FIELD

[002] Embodiments described herein generally relate to apparatus, system and method of Back Side Illumination (BSI) Complementary Metal–Oxide–Semiconductor (CMOS) pixel array.

BACKGROUND

[003] An imaging device, e.g., a camera, may include an image sensor to capture one or more images, photos, videos, and/or the like.

[004] The image sensor may include a pixel array including a plurality of pixels. A pixel of the plurality of pixels may include a photodiode configured to convert light from the image to an electronic signal, for example, to enable processing the image.

[005] The image sensor may be formed on a wafer, e.g., a substrate, using a Complementary Metal–Oxide–Semiconductor (CMOS) technology.

[006] A Back Side Illumination (BSI) Complementary Metal–Oxide–Semiconductor (CMOS) image sensor may be illuminated from the back-side of the wafer, for example, after thinning the back-side of the wafer.

[007] The BSI CMOS image sensor may have advantages over front-side illuminated image sensors. For example, metal interconnectors of the image sensor may not cast a shadow on light sensitive areas of the BSI CMOS image sensor.

BRIEF DESCRIPTION OF THE DRAWINGS

[008] For simplicity and clarity of illustration, elements shown in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity of presentation. Furthermore, reference numerals may be repeated among the figures to indicate corresponding or analogous elements. The figures are listed below.

[009] Fig. 1 is a schematic block diagram illustration of an integrated chip (IC), in accordance with some demonstrative embodiments.

[0010] Fig. 2 is a schematic illustration of a Back Side Illumination (BSI) Complementary Metal–Oxide–Semiconductor (CMOS) pixel, in accordance with some demonstrative embodiments.

[0011] Figs. 3A-3D are schematic illustrations of respective fabrication stages during fabrication of an integrated chip, in accordance with some demonstrative embodiments.

[0012] Fig. 4 is a schematic illustration of an imaging device, in accordance with some demonstrative embodiments.

DETAILED DESCRIPTION

[0013] In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of some embodiments. However, it will be understood by persons of ordinary skill in the art that some embodiments may be practiced without these specific details. In other instances, well-known methods, procedures, components, units and/or circuits have not been described in detail so as not to obscure the discussion.

[0014] Discussions herein utilizing terms such as, for example, “processing”, “computing”, “calculating”, “determining”, “establishing”, “analyzing”, “checking”, or the like, may refer to operation(s) and/or process(es) of a computer, a computing platform, a computing system, or other electronic computing device, that manipulate and/or transform data represented as physical (e.g., electronic) quantities within the computer’s registers and/or memories into other data similarly represented as physical quantities within the computer’s registers and/or memories or other information storage medium that may store instructions to perform operations and/or processes.

[0015] The terms “plurality” and “a plurality”, as used herein, include, for example, “multiple” or “two or more”. For example, “a plurality of items” includes two or more items.

[0016] References to “one embodiment”, “an embodiment”, “demonstrative embodiment”, “various embodiments” etc., indicate that the embodiment(s) so described may include a particular feature, structure, or characteristic, but not every embodiment necessarily includes the particular feature, structure, or characteristic. Further, repeated use of the phrase “in one embodiment” does not necessarily refer to the same embodiment, although it may.

[0017] As used herein, unless otherwise specified the use of the ordinal adjectives “first”, “second”, “third” etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner.

[0018] Some embodiments may be used in conjunction with various devices and systems, for example, an imaging device, a digital camera device, a video device, a camera module, a medical imaging device, a mobile computer, a laptop computer, a notebook computer, a tablet computer, a handheld computer, a handheld device, a Personal Digital Assistant (PDA) device, a handheld PDA device, a mobile or portable device, a consumer device, a Smartphone, and the like.

[0019] The terms “substrate” and/or “wafer”, as used herein, may relate to a thin slice of semiconductor material, for example, a silicon crystal, which may be used in fabrication of integrated circuits and/or any other microelectronic devices. For example, the wafer may serve as the substrate for the microelectronic devices, which may be built in and over the wafer.

[0020] The term “Integrated Circuit” (IC), as used herein, may relate to a set of one or more electronic circuits on a semiconductor material. For example, the electronic circuit may include electronic components and their interconnectors.

[0021] Reference is made to Fig. 1, which schematically illustrates a block diagram of an Integrated Circuit (IC) 100, in accordance with some demonstrative embodiments.

[0022] In some demonstrative embodiments, IC 100 may be configured to capture, record, process, handle and/or store one or more images, photos, videos, movies, clips and/or the like.

[0023] In some demonstrative embodiments, IC 100 may be implemented as part of an imaging device, e.g., as described below with reference to Fig. 4. For example, IC 100 may be included as part of an imaging device, a digital camera, a medical imaging device, and the like.

[0024] In some demonstrative embodiments, IC 100 may be formed on a substrate, e.g., a wafer, for example using a Complementary Metal–Oxide–Semiconductor (CMOS) technology.

[0025] In some demonstrative embodiments, IC 100 may include a pixel array 102 configured to sense and/or to capture an image.

[0026] In some demonstrative embodiments, IC 100 may include a circuitry 106 configured to process, to handle, to amplify, to manipulate, and/or to perform any other additional or alternative operations on a photo signal of an image, e.g., captured by pixel array 102.

[0027] In some demonstrative embodiments, pixel array 102 may be at an internal area of IC 100, e.g., at the center of IC 100, and/or circuitry 106 may be at the periphery of IC 100.

[0028] In some demonstrative embodiments, circuitry 102 may include one or more processors, memory components, electronic components, and/or the like.

[0029] In some demonstrative embodiments, pixel array 102 may be configured to capture photons corresponding to an image and to convert the photons into electronic signals, for

example, to enable circuitry 106 to process the image and/or to display the image on a display.

[0030] In some demonstrative embodiments, pixel array 102 may include a plurality of pixels 104.

[0031] In some demonstrative embodiments, a pixel 104 of the plurality of pixels 104 may be configured to capture incoming photons at an area of pixel 104, and to convert the photons into electronic signals.

[0032] In some demonstrative embodiments, pixel 104 may include a photodiode 110 configured to collect electrons, e.g., generated responsive to the incoming photons at the area of pixel 104.

[0033] In some demonstrative embodiments, photodiode 110 may be configured to generate the electronic signals, for example, based on the collected electrons.

[0034] In some demonstrative embodiments, photodiode 110 may include a fully pinned diode.

[0035] In some demonstrative embodiments, photodiode 110 may include a non-pinned diode.

[0036] In other embodiments, photodiode 110 may include any other diode, e.g., a partially pinned diode.

[0037] In some demonstrative embodiments, pixel array 102 may include a Back Side Illumination (BSI) pixel array.

[0038] In some demonstrative embodiments, the BSI pixel array may be configured to absorb light and/or to be illuminated from the backside of the wafer.

[0039] In some demonstrative embodiments, the BSI pixel array may include metal interconnectors and/or wiring, which may be located behind light sensitive elements of pixel array 102, e.g., photodiode 110, for example, compared to front side illuminated image sensors, in which the metal interconnectors and/or the wiring are located in front of the light sensitive elements.

[0040] In some demonstrative embodiments, the BSI pixel array may be able to capture an increased number of incoming photons from the image, for example, compared to the front side illuminated image sensors.

[0041] In one example, the BSI pixel array may be able to capture the increased number of incoming photons, for example, since the metal interconnectors of pixel array 102 may not cast a shadow on light sensitive areas of pixel array 102, e.g., photodiode 110.

[0042] In some demonstrative embodiments, photodiode 110 may include, and/or may perform the functionality of, a low fill factor diode, for example, a PD occupying a small part of pixel 104.

[0043] In some demonstrative embodiments, photodiode 110 may include a low fill factor diode, for example, to enable one or more electronic components and/or elements to be introduced inside pixel 104.

[0044] In other embodiments, photodiode 110 may include a low fill factor diode, for example, for any other reasons, e.g., physical reasons, design reasons, manufacturing reasons, and or any other reasons.

[0045] In some demonstrative embodiments, the one or more electronic components of pixel array 102 may be introduced inside pixel 104, for example, to perform one or more computational operations.

[0046] In one example, pixel 104 may be configured to perform the one or more computational operations, for example, in accordance with one or more requirements from one or more applications, e.g., imaging applications, video applications, photo applications, and/or any other applications.

[0047] In some demonstrative embodiments, pixel 104 may include one or more Metal-Oxide-Semiconductor (MOS) transistors 112, for example, to perform the computational operations.

[0048] In one example, pixel 104 may include a plurality of MOS transistors, e.g., many MOS transistors 112.

[0049] In some demonstrative embodiments, MOS transistors 112 may include one or more P-type MOS (PMOS) transistors and/or one or more N-type MOS (NMOS) transistors.

[0050] In some demonstrative embodiments, MOS transistors 112 may include one or more well regions 113.

[0051] In some demonstrative embodiments, a well region 113 may include an N-Well (NW) region 114 or a P-well (PW) region 116.

[0052] In one example, well region 113 may include an NW region 114, for example, of a PMOS transistor. For example, the PMOS transistor may be built over the NW region 114.

[0053] In another example, well region 113 may include PW region 116, for example, of an NMOS transistor. For example, the NMOS transistor may be built over the PW region 116.

[0054] In some demonstrative embodiments, well regions 113 may act as a parasitic photodiode.

[0055] In one example, NW region 114 may absorb electrons, e.g., generated responsive to the incoming photons at pixel array 102.

[0056] In one example, a photodiode in the BSI CMOS pixel sensor may be the biggest element of the pixel, e.g., compared to other elements of the BSI CMOS pixel. For example, the photodiode may occupy most of the area of the BSI CMOS pixel. Accordingly, most of the electrons generated by the incoming photons may be collected by the photodiode. If, for example, one or more MOS transistors are introduced into pixel 104, a size of photodiode 110 may be reduced and, as a result, well regions 113 may be able to collect a substantial amount of the electrons.

[0057] In some demonstrative embodiments, allowing a substantial amount of the electrons to be absorbed, for example, by the NW region 114, may reduce the number of electrons absorbed by photodiode 110, for example, if pixel 104 includes an electron-collecting pixel, e.g., as described below.

[0058] In some demonstrative embodiments, NW region 114 may be connected to a power supply, e.g., a VDD.

[0059] In some demonstrative embodiments, connecting the NW region 114 to the VDD may cause at least some of the electrons e.g., which may be generated responsive to the incoming photons at pixel array 102, to flow to the VDD.

[0060] In some demonstrative embodiments, NW region 114 may absorb a substantial amount of the electrons and, as a result, a reduced number of electrons may be collected by the photodiode 110.

[0061] In one example, the electrons may be generated in the well regions 113 of pixel 104. According to this example, a substantial amount of electrons, e.g., all electrons, which may be generated in NW region 114, may be lost and/or flow to the VDD and, as a result, may not contribute to a photo signal received by photodiode 110.

[0062] In some demonstrative embodiments, allowing a substantial amount of the electrons to be absorbed, for example, by the PW region 116, may affect the performance of pixel 104, for example, if pixel 104 includes an electron-collecting pixel.

[0063] In one example, absorption of the electrons in the PW region 116 may increase a probability of recombination of the electrons, and as a result, a reduced number of electrons may be collected by the photodiode 110.

[0064] In another example, absorption of the electrons in the PW region 116 may increase interference, e.g., “cross talk”, between adjacent pixels, which may cause the photo signal to appear in an adjacent pixel.

[0065] In some demonstrative embodiments, only a small part of the electrons generated in the PW region 116 may diffuse to an area of photodiode 110, and may contribute to the photo signal. As photodiode 110 may occupy a small part of pixel 104, the electrons that are actually contributing to the photo signal may include electrons that are generated in photodiode 110, and/or electrons managing to diffuse from PW region 116 to photodiode 110, e.g., as described above.

[0066] In some demonstrative embodiments, covering the MOS transistors 112 with a metal layer, e.g., according to a “metallization” scheme of a front side illumination process, for example, may prevent the electrons from being absorbed in the NW region. However, some of the incoming photons may be lost, for example, due to reflections.

[0067] In some demonstrative embodiments, other conventional methods may not be effective for pixels having a very small diode, and/or pixels including MOS transistors, e.g., pixel 104.

[0068] In one example, a standard BSI technology may use a very thin silicon, and implementing the conventional methods may be very complicated, and/or it may be very hard to implement the conventional methods on a pixel having CMOS circuits.

[0069] For example, according to a BSI integration scheme, an electrostatic lens may be based on a double epitaxial (epi) layer, e.g., a p layer on an n layer, and the n layer may be fully depleted to direct electrons into a photodiode. This scheme may be very complicated and very hard to implement on a pixel with CMOS circuits, e.g., pixel 104.

[0070] In another example, a fully depleted BSI sensor may include a high-end charge-coupled device (CCD) sensor, which may increase Infra Red quantum efficiency. This approach may be difficult to implement in CMOS image sensors.

[0071] In some demonstrative embodiments, pixel 104 may be configured to reduce, eliminate and/or to prevent the electrons to be absorbed by well regions 113, e.g., by NW region 114, of pixel 104.

[0072] In some demonstrative embodiments, photodiode 110 may be configured to collect the electrons from a large area of pixel 104, e.g., substantially an entire area of pixel 104.

[0073] Some demonstrative embodiments may enable to increase a collection efficiency of photodiode 110, and/or to significantly increase a quantum efficiency (QE) of the pixel 104, e.g., as described below.

[0074] In some demonstrative embodiments, IC 100 may be formed on a thick and/or high resistive silicon, e.g., as described below.

[0075] In some demonstrative embodiments, pixel 104 may include an epitaxial (epi) layer 120.

[0076] In some demonstrative embodiments, epi layer 120 may be relatively thick, e.g., compared to a thickness of an epi layer of common BSI CMOS pixel sensors.

[0077] In some demonstrative embodiments, using a thick epi layer 120 may reduce the amount of, or may even prevent, the electrons from being absorbed at NW region 114, e.g., as described below.

[0078] In some demonstrative embodiments, a thickness of epi layer 120 may be of at least 4 micron (um), e.g., compared to a thickness of between 2.6 and 3.5 um of an epi layer of the common BSI CMOS pixel sensors.

[0079] In some demonstrative embodiments, the thickness of epi layer 120 may be at least 10 um.

[0080] In some demonstrative embodiments, the thickness of epi layer 120 may be at least 15 um.

[0081] In another example, epi layer 120 may have any other thickens, for example, a thickness greater than 4 um, for example, between 4 and 18 um, or even greater than 18um.

[0082] In some demonstrative embodiments, epi layer 120 may have a high resistivity, e.g., compared to a resistivity of an epi layer of the common BSI CMOS pixel sensors.

[0083] In some demonstrative embodiments, using a high resistivity epi layer 120 may reduce the number of, or even may prevent, the electrons from being absorbed at NW region 114, e.g., as described below.

[0084] In some demonstrative embodiments, a resistivity of epi layer 120 may be greater than 30 ohm to centimeter (ohm-cm), e.g., compared to a resistivity of between 10 and 30 ohm-cm of an epi layer of the common BSI CMOS pixel sensors.

[0085] In some demonstrative embodiments, a resistivity of epi layer 120 may be greater than 100 ohm to centimeter (ohm-cm).

[0086] In some demonstrative embodiments, epi layer 120 may include an absorption area 122 configured to absorb incoming photons, which may be absorbed by pixel array 102.

[0087] In some demonstrative embodiments, absorption area 122 may be configured to generate electrons, e.g., responsive to the incoming photons.

[0088] In some demonstrative embodiments, epi layer 120 may include a collection area 124 configured to provide the electrons from absorption area 122 to photodiode 110.

[0089] In some demonstrative embodiments, collection area 124 may connect, e.g., directly connect, absorption area 122 to photodiode 110, for example, to provide the electrons from absorption area 122 to photodiode 110.

[0090] In some demonstrative embodiments, pixel 104 may include a barrier layer 126 configured to separate the absorption area 122 from P-well region 116 and/or N-well region 114.

[0091] In some demonstrative embodiments, barrier layer 126 may be configured to reduce or even prevent diffusion of the electrons from absorption area 122 to the N-well region 114 and/or to the P-well region 116.

[0092] In one example, barrier layer 126 may be configured to cover a large area of pixel 104, e.g., substantially the entire area of pixel 104, for example, except from an area of photodiode 110.

[0093] In some demonstrative embodiments, barrier layer 126 may include a deep PW implant. In other embodiments, barrier layer 126 may include any other suitable implant.

[0094] In some demonstrative embodiments, barrier layer 126 may include a boron implant.

[0095] In other embodiments, barrier layer 126 may include any other suitable material.

[0096] In some demonstrative embodiments, collection area 124 may extend from absorption area 122 to photodiode 110 through barrier layer 126.

[0097] In one example, collection area 124 may extend from absorption area 122 to photodiode 110 through barrier layer 126, for example, to provide the electrons from absorption area 122 to photodiode 110, e.g., through barrier layer 126.

[0098] In some demonstrative embodiments, collection area 124 may enhance a depletion region of photodiode 110, for example, by extending the depletion region of photodiode 110 beyond barrier layer 126.

[0099] In one example, the extension of collection area 124 from absorption area 122 to photodiode 110 through barrier layer 126 and within a thick epi layer 120, may reduce, or even prevent, diffusion of the electrons to NW region 114, and/or may enable to collect the electrons from a substantial area, e.g., the entire area, of absorption area 122, for example, from the entire area of pixel 104.

[00100] In some demonstrative embodiments, collection area 124 may perform the functionality of an electrostatic lens configured to collect the electrons from absorption area 122, e.g., as described below.

[00101] In one example, the electrostatic lens may enable to guide, direct, and/or focus the electrons towards photodiode 110. Accordingly, the electrostatic lens may enhance and/or magnify a collection efficiency of photo diode 110, and/or may reduce, or even prevent, the electrons from being absorbed by well regions 113.

[00102] In some demonstrative embodiments, pixel 104 may include a micro lens 128 configured to direct the incoming photons to absorption area 122.

[00103] In some demonstrative embodiments, absorption area 122 may be between micro lens 128 and barrier layer 126.

[00104] In some demonstrative embodiments, pixel 104 may include an anti-reflective coating (ARC) layer 129, e.g., configured to reduce reflections of micro lens 128.

[00105] In some demonstrative embodiments, ARC layer 129 may be between micro lens 128 and absorption area 122.

[00106] In some demonstrative embodiments, IC 100 may be configured to prevent interference between circuitry 106 and pixel array 102.

[00107] In some demonstrative embodiments, IC 100 may be configured to prevent diffusion of photoelectrons from circuitry 106 to pixel array 102.

[00108] In some demonstrative embodiments, IC 100 may include a guard ring 108 configured to separate circuitry 106 from BSI pixel array 102.

[00109] In some demonstrative embodiments, guard ring 108 may be between the internal area of IC 100, e.g., the location of BSI pixel array 102, and the periphery of IC 100, e.g., the location of circuitry 106.

[00110] In some demonstrative embodiments, guard ring 108 may be configured to prevent the diffusion of the photoelectrons from circuitry 106 to BSI pixel array 102, e.g., as described below with reference to Fig. 3D.

[00111] In some demonstrative embodiments, IC 100 may be configured to increase the quantum efficiency of the BSI CMOS pixel array, e.g., pixel array 102, including a plurality of MOS transistors, e.g., MOS transistors 112, and/or low fill factor diodes, for example, photodiode 110, e.g., as described above.

[00112] Reference is made to Fig. 2, which schematically illustrates a BSI CMOS pixel 200, in accordance with some demonstrative embodiments. For example, BSI CMOS pixel 200 may perform the functionality of pixel 104 (Fig. 1).

[00113] As shown in Fig. 2, BSI CMOS pixel 200 may include a micro lens 228 and an ARC layer 229. For example, micro lens 228 may perform the functionality of micro lens 128 (Fig. 1), and/or ARC layer 229 may perform the functionality of ARC layer 129 (Fig. 1).

[00114] As shown in Fig. 2, BSI CMOS pixel 200 may include wiring layers 230, for example, behind a photodiode 210. For example, photodiode 210 may perform the functionality of photodiode 110 (Fig. 1).

[00115] As shown in Fig. 2, photodiode 210 may include a low fill factor diode, e.g., a small diode.

[00116] As shown in Fig. 2, photodiode 210 may include the low fill factor diode, for example, to enable one or more NW regions 214 and one or more PW regions 216 of one or more MOS transistors to be introduced into BSI CMOS pixel 200.

[00117] As shown in Fig. 2, BSI CMOS pixel 200 may include an epi layer 220. For example, epi layer 220 may perform the functionality of epi layer 120 (fig. 1).

[00118] As shown in Fig. 2, epi layer 220 may be relatively thick, for example, having a thickness of between 4 and 18 um, or any other thickness, e.g., as described above.

[00119] As shown in figure 2, BSI CMOS pixel 200 may include a barrier layer 226 covering NW regions 214 and PW regions 216. For example, barrier layer 226 may perform the functionality of barrier layer 126 (Fig. 1).

[00120] As shown in Fig. 2, epi layer 220 may include an absorption area 222, for example, to absorb incoming photos and to generate electrons 223, e.g., from the incoming photos. For example, absorption area 222 may perform the functionality of absorption area 122 (Fig. 1).

[00121] As shown in Fig. 2, epi layer 220 may include a collection area 224 to provide the electrons 223 to photodiode 210. For example, collection area 224 may perform the functionality of collection area 124 (Fig. 1).

[00122] As shown in Fig. 2, collection area 224 may extend from absorption area 222 to photo diode 210 through barrier layer 226.

[00123] As shown in Fig. 2, collection area 224 may perform the functionality of electrostatic lens configured to guide and/or to direct electrons 223 to photodiode 210, and/or to prevent the electrons 223 from being absorbed at the one or more NW regions 214.

[00124] Reference is made to Figs. 3A-3D, which schematically illustrate respective stages of fabricating an integrated circuit, in accordance with some demonstrative embodiments.

[00125] In some demonstrative embodiments, IC 100 (Fig. 1) may be fabricated using the one or more operations describes below with respect to Figs 3A-3D.

[00126] In some demonstrative embodiments, fabrication of the IC may include a front-side processing operation, a pixel processing operation, and/or a backside processing operation, e.g., as described below.

[00127] As shown in Fig. 3A, the IC may be formed on a substrate 300, e.g., a starting material, or a wafer.

[00128] As shown in Fig. 3A, substrate 300 may include a thick substrate, e.g., an extremely thick substrate, for example, a substrate having a thickness of about 700 um.

[00129] As shown in Fig. 3A, substrate 300 may include a thick epi layer 320 formed on the substrate.

[00130] As shown in Fig. 3A, epi layer 320 may be thick, e.g., having a thickness of at least 5 μ m. For example, an epi layer having a thickness of between 5 and 18 μ m, or any other thickness.

[00131] As shown in Fig. 3A, epi layer 320 may have a high resistivity, e.g., a resistivity greater than 100 ohm-cm, or any other resistivity.

[00132] As shown in Fig. 3B, the front-side processing may include forming a pixel array 302. For example, pixel array 302 may perform the functionality of pixel array 102 (Fig. 1)

[00133] As shown in Fig. 3B, in one example, pixel array 302 may include a pinned photodiode 310, and one NW region 314.

[00134] As shown in Fig. 3B, in one example, pixel array 302 may include two PW regions 316.

[00135] In another example, pixel array 302 may include any other diode, e.g., a non-pinned diode, and/or any other number of NW regions 314 and/or PW regions 316.

[00136] As shown in Fig. 3C, one or more operations may be performed during the pixel processing of the IC, e.g., as described below.

[00137] As shown in Fig. 3C, a barrier layer 326 may be formed, e.g., using a high-energy boron implant 327.

[00138] As shown in Fig. 3C, barrier layer 326 may separate between NW regions 314 and/or PW regions 316, and an absorption area 322 of epi layer 320.

[00139] As shown in Fig. 3C, barrier layer 326 may be formed to cover substantially an entire area of pixel array 302, e.g., except from photodiode 310. For example, barrier layer 326 may be formed using one or more lithography barriers 329, e.g., on top of photodiode 310, when performing the boron implant.

[00140] In some demonstrative embodiments, a diode metrological junction, e.g., of photodiode 310, may include a deep implant. As a result, a depletion region of photodiode 310 may reach a depth beyond barrier layer 326.

[00141] As shown in Fig. 3C, photodiode 310 may be formed using a deep implant of n-, for example, to extend a depletion region of photo diode 310 through barrier layer 326, and/or to connect photodiode 310 to a connection area 324 of epi layer 320.

[00142] In some demonstrative embodiments, fabricating the pixel array 302 over the high resistive silicon may create one or more problems to predesigned circuits.

[00143] In one example, the high resistive silicon may create isolation problems, for example, between NW and NW regions, between Native transistors and/or between bipolar transistors.

[00144] In some demonstrative embodiments, an implant, e.g., a deep implant, may be configured to create conditions of a low resistivity substrate at the bottom of, e.g., each NW and PW, which are used in the periphery of the IC, for example, to overcome the isolation problems.

[00145] In some demonstrative embodiments, the front-side processing of the substrate may include forming an isolated PW, e.g., as described below.

[00146] As shown in Fig. 3D, the front-side processing may include forming a deep PW implant 333 configured to create a low resistivity substrate at the bottom of NW and PW regions at a periphery area 340 of the integrated circuit, e.g., an area of circuit 106 (Fig. 1).

[00147] As shown in Fig. 3D, a guard ring 308 may be formed to protect the pixel array 302, for example, from collecting photoelectrons diffusion from the periphery area 340 of the integrated circuit.

[00148] In one example, guard ring 308 may be configured to prevent injection from the periphery of pixel array 102 (Fig. 1) to the center of pixel array 102 (Fig. 1).

[00149] In some demonstrative embodiments, the backside processing of the substrate may include bonding, thinning, and/or passivation operations, e.g., using one or more backside processing CMOS techniques.

[00150] In some demonstrative embodiments, the backside processing of the substrate may include consideration of backside alignment for metal grid or color filter array (CFA), and/or PAD opening, e.g., for the thick and high resistive silicon.

[00151] Reference is made to Fig. 4, which schematically illustrates an imaging device 400, in accordance with some demonstrative embodiments.

[00152] In some demonstrative embodiments, image device 400 may be configured to capture one or more images.

[00153] In one example, image device 400 may capture, record, process, handle and/or store one or more photos, videos, movies, clips and/or the like.

[00154] In some demonstrative embodiments, image device 400 may include a camera, e.g., a digital camera, a digital video camera, a digital photo camera, a webcam, a mobile device, an imaging device, a medical imaging device, a mobile phone, e.g., including a camera, a Smartphone, and/or the like.

[00155] In some demonstrative embodiments, image device 400 may include a BSI image sensor 420. For example, BSI image sensor 420 may include IC 100 (Fig. 1).

[00156] In some demonstrative embodiments, BSI image sensor 420 may be configured to capture the one or more images, for example, by converting incoming photons into electronic signals.

[00157] In some demonstrative embodiments, image sensing device 400 may also include, for example, a processor 491, an input unit 492, an output unit 493, a memory unit 494, and/or a storage unit 495. Image sensing device 400 may optionally include other suitable hardware components and/or software components. In some demonstrative embodiments, some or all of the components of image sensing device 400 may be enclosed in a common housing or packaging, and may be interconnected or operably associated using one or more wired or wireless links. In other embodiments, components of image sensing device 400 may be distributed among multiple or separate devices.

[00158] In some demonstrative embodiments, processor 491 may include, for example, a Central Processing Unit (CPU), a Digital Signal Processor (DSP), one or more processor cores, a single-core processor, a dual-core processor, a multiple-core processor, a microprocessor, a host processor, a controller, a plurality of processors or controllers, a chip, a microchip, one or more circuits, circuitry, a logic unit, an Integrated Circuit (IC), an Application-Specific IC (ASIC), or any other suitable multi-purpose or specific processor or controller. For example, processor 491 executes instructions, for example, of an Operating System (OS) of image sensing device 400 and/or of one or more suitable applications.

[00159] In some demonstrative embodiments, memory unit 494 may include, for example, a Random Access Memory (RAM), a Read Only Memory (ROM), a Dynamic RAM (DRAM), a Synchronous DRAM (SD-RAM), a flash memory, a volatile memory, a non-volatile

memory, a cache memory, a buffer, a short term memory unit, a long term memory unit, or other suitable memory units. Storage unit 495 include, for example, a hard disk drive, a floppy disk drive, a Compact Disk (CD) drive, a CD-ROM drive, a DVD drive, or other suitable removable or non-removable storage units. For example, memory unit 494 and/or storage unit 495, for example, may store data processed by image sensing device 400.

[00160] In some demonstrative embodiments, input unit 492 may include, for example, a keyboard, a keypad, a mouse, a touch-screen, a touch-pad, a track-ball, a stylus, a microphone, or other suitable pointing device or input device. Output unit 493 includes, for example, a monitor, a screen, a touch-screen, a flat panel display, a Cathode Ray Tube (CRT) display unit, a Liquid Crystal Display (LCD) display unit, a plasma display unit, one or more audio speakers or earphones, or other suitable output devices.

EXAMPLES

[00161] The following examples pertain to further embodiments.

[00162] Example 1 includes a back-side illumination (BSI) complementary metal-oxide-semiconductor (CMOS) pixel array comprising a plurality of pixels, a pixel of the plurality of pixels comprising one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of the one or more well regions comprising an N-Well (NW) region or a P-well (PW) region; a photodiode; an epitaxial (epi) layer comprising an absorption area and a collection area, the absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, and the collection area connecting the absorption area to the photodiode to provide the electrons from the absorption area to the photodiode; and a barrier layer separating the absorption area from the one or more well regions.

[00163] Example 2 includes the subject matter of Example 1, and optionally, wherein the photodiode comprises a low fill factor (FF) diode.

[00164] Example 3 includes the subject matter of Example 1, and optionally, wherein the collection area extends from the absorption area to the photodiode through the barrier layer.

[00165] Example 4 includes the subject matter of Example 1, and optionally, wherein the collection area is configured to perform the functionality of an electrostatic lens to collect the electrons from the absorption area.

[00166] Example 5 includes the subject matter of Example 1, and optionally, wherein the barrier layer is configured to prevent diffusion of the electrons from the absorption area to the well regions.

[00167] Example 6 includes the subject matter of Example 1, and optionally, wherein a thickness of the epi layer is at least 4 micron (μm).

[00168] Example 7 includes the subject matter of Example 1, and optionally, wherein a thickness of the epi layer is at least 10 micron (μm).

[00169] Example 8 includes the subject matter of Example 1, and optionally, wherein a thickness of the epi layer is at least 15 micron (μm).

[00170] Example 9 includes the subject matter of Example 1, and optionally, wherein a resistivity of the epi layer is greater than 100 ohm to centimeter (ohm-cm).

[00171] Example 10 includes the subject matter of Example 1, and optionally, comprising a micro lens, the absorption area is between the micro lens and the barrier layer.

[00172] Example 11 includes the subject matter of Example 1, and optionally, comprising an anti-reflective coating (ARC) layer, the ARC layer is between the micro lens and the absorption area.

[00173] Example 12 includes the subject matter of Example 1, and optionally, wherein the one or more MOS transistors comprise one or more transistors selected from a group consisting of one or more P-type MOS (PMOS) transistors, and one or more N-type MOS (NMOS) transistors.

[00174] Example 13 includes the subject matter of Example 1, and optionally, wherein the barrier layer comprises a deep PW implant.

[00175] Example 14 includes the subject matter of Example 1, and optionally, wherein the barrier layer comprises a boron implant.

[00176] Example 15 includes the subject matter of Example 1, and optionally, wherein the photodiode comprises a fully pinned diode.

[00177] Example 16 includes the subject matter of Example 1, and optionally, wherein the photodiode comprises a non-pinned diode.

[00178] Example 17 includes a complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) comprising a circuitry; and a back-side illumination (BSI) pixel array

comprising a plurality of pixels, a pixel of the plurality of pixels comprising one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of the one or more well regions comprising an N-Well (NW) region or a P-well (PW) region; a photodiode; an epitaxial (epi) layer comprising an absorption area and a collection area, the absorption area to absorb incoming photons and to generate electrons responsive to the absorbed photons, and the collection area connecting the absorption area to the photodiode to provide the electrons from the absorption area to the photodiode; and a barrier layer separating the absorption area from the well regions.

[00179] Example 18 includes the subject matter of Example 17, and optionally, comprising a guard ring separating the circuitry from the BSI pixel array.

[00180] Example 19 includes the subject matter of Example 18, and optionally, wherein the guard ring is configured to prevent diffusion of photoelectrons from the circuitry to the BSI pixel array.

[00181] Example 20 includes the subject matter of Example 17, and optionally, wherein the photodiode comprises a low fill factor (FF) diode.

[00182] Example 21 includes the subject matter of Example 17, and optionally, wherein the collection area extends from the absorption area to the photodiode through the barrier layer.

[00183] Example 22 includes the subject matter of Example 17, and optionally, wherein the collection area is configured to perform the functionality of an electrostatic lens to collect the electrons from the absorption area.

[00184] Example 23 includes the subject matter of Example 17, and optionally, wherein the barrier layer is configured to prevent diffusion of the electrons from the absorption area to the well regions.

[00185] Example 24 includes the subject matter of Example 17, and optionally, wherein a thickness of the epi layer is at least 4 micron (μm).

[00186] Example 25 includes the subject matter of Example 17, and optionally, wherein a thickness of the epi layer is at least 10 micron (μm).

[00187] Example 26 includes the subject matter of Example 17, and optionally, wherein a thickness of the epi layer is at least 15 micron (μm).

[00188] Example 27 includes the subject matter of Example 17, and optionally, wherein a resistivity of the epi layer is greater than 100 ohm to centimeter (ohm-cm).

[00189] Example 28 includes the subject matter of Example 17, and optionally, comprising a micro lens, the absorption area is between the micro lens and the barrier layer.

[00190] Example 29 includes the subject matter of Example 29, and optionally, comprising an anti-reflective coating (ARC) layer, the ARC layer is between the micro lens and the absorption area.

[00191] Example 30 includes the subject matter of Example 17, and optionally, wherein the one or more MOS transistors comprise one or more transistors selected from a group consisting of one or more P-type MOS (PMOS) transistors and one or more N-type MOS (NMOS) transistors.

[00192] Example 31 includes the subject matter of Example 17, and optionally, wherein the barrier layer comprises a deep PW implant.

[00193] Example 32 includes the subject matter of Example 17, and optionally, wherein the barrier layer comprises a boron implant.

[00194] Example 33 includes the subject matter of Example 17, and optionally, wherein the photodiode comprises a fully pinned diode.

[00195] Example 34 includes the subject matter of Example 17, and optionally, wherein the photodiode comprises a non-pinned diode

[00196] Example 35 includes an imaging device comprising a memory; an input; an output; a processor; and a complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) comprising a circuitry; and a back-side illumination (BSI) pixel array comprising a plurality of pixels, a pixel of the plurality of pixel sensors comprising one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of the one or more well regions comprising an N-Well (NW) region or a P-well (PW) region; a photodiode; an epitaxial (epi) layer comprising an absorption area and a collection area, the absorption area to absorb incoming photons and to generate electrons responsive to the absorbed photons, and the collection area connecting the absorption area to the photodiode to provide the electrons from the absorption area to the photodiode; and a barrier layer separating the absorption area from the well regions.

[00197] Example 36 includes the subject matter of Example 35, and optionally, comprising a digital camera or a Smartphone.

[00198] Example 37 includes the subject matter of Example 35, and optionally, comprising a guard ring separating the circuitry from the BSI pixel array.

[00199] Example 38 includes the subject matter of Example 37, and optionally, wherein the guard ring is configured to prevent diffusion of photoelectrons from the circuitry to the BSI pixel array.

[00200] Example 39 includes the subject matter of Example 35, and optionally, wherein the photodiode comprises a low fill factor (FF) diode.

[00201] Example 40 includes the subject matter of Example 35, and optionally, wherein the collection area extends from the absorption area to the photodiode through the barrier layer.

[00202] Example 41 includes the subject matter of Example 35, and optionally, wherein the collection area is configured to perform the functionality of an electrostatic lens to collect the electrons from the absorption area.

[00203] Example 42 includes the subject matter of Example 35, and optionally, wherein the barrier layer is configured to prevent diffusion of the electrons from the absorption area to the well regions.

[00204] Example 43 includes the subject matter of Example 35, and optionally, wherein a thickness of the epi layer is at least 4 micron (um).

[00205] Example 44 includes the subject matter of Example 35, and optionally, wherein a thickness of the epi layer is at least 10 micron (um).

[00206] Example 45 includes the subject matter of Example 35, and optionally, wherein a thickness of the epi layer is at least 15 micron (um).

[00207] Example 46 includes the subject matter of Example 35, and optionally, wherein a resistivity of the epi layer is greater than 100 ohm to centimeter (ohm-cm).

[00208] Example 47 includes the subject matter of Example 35, and optionally, comprising a micro lens, the absorption area is between the micro lens and the barrier layer.

[00209] Example 48 includes the subject matter of Example 29, and optionally, comprising an anti-reflective coating (ARC) layer, the ARC layer is between the micro lens and the absorption area.

[00210] Example 49 includes the subject matter of Example 35, and optionally, wherein the one or more MOS transistors comprise one or more transistors selected from a group

consisting of one or more P-type MOS (PMOS) transistors and one or more N-type MOS (NMOS) transistors.

[00211] Example 50 includes the subject matter of Example 35, and optionally, wherein the barrier layer comprises a deep PW implant.

[00212] Example 51 includes the subject matter of Example 35, and optionally, wherein the barrier layer comprises a boron implant.

[00213] Example 52 includes the subject matter of Example 35, and optionally, wherein the photodiode comprises a fully pinned diode.

[00214] Example 53 includes the subject matter of Example 35, and optionally, wherein the photodiode comprises a non-pinned diode

[00215] Example 54 includes a method of fabricating a complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) comprising a pixel array, the method comprising forming on an epitaxial layer a photodiode and one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of the one or more well regions comprising an N-Well (NW) region or a P-well (PW) region, wherein the epitaxial layer comprising an absorption area and a collection area, the absorption area configured to absorb incoming photons and to generate electrons responsive to the absorbed photons, and the collection area configured to connect the absorption area to the photodiode to provide the electrons from the absorption area to the photodiode; and forming a barrier layer configured to separate the absorption area from the well regions.

[00216] Example 55 includes the subject matter of Example 54, and optionally, comprising forming a guard ring configured to separate a circuitry of the IC from the BSI pixel array.

[00217] Example 56 includes the subject matter of Example 55, and optionally, wherein the guard ring is configured to prevent diffusion of photoelectrons from the circuitry to the BSI pixel array.

[00218] Example 57 includes the subject matter of Example 54, and optionally, wherein the photodiode comprises a low fill factor (FF) diode.

[00219] Example 58 includes the subject matter of Example 54, and optionally, wherein the collection area extends from the absorption area to the photodiode through the barrier layer.

[00220] Example 59 includes the subject matter of Example 54, and optionally, wherein the collection area is configured to perform the functionality of an electrostatic lens to collect the electrons from the absorption area.

[00221] Example 60 includes the subject matter of Example 54, and optionally, wherein the barrier layer is configured to prevent diffusion of the electrons from the absorption area to the well regions.

[00222] Example 61 includes the subject matter of Example 54, and optionally, wherein a thickness of the epi layer is at least 4 micron (um).

[00223] Example 62 includes the subject matter of Example 54, and optionally, wherein a thickness of the epi layer is at least 10 micron (um).

[00224] Example 63 includes the subject matter of Example 54, and optionally, wherein a thickness of the epi layer is at least 15 micron (um).

[00225] Example 64 includes the subject matter of Example 54, and optionally, wherein a resistivity of the epi layer is greater than 100 ohm to centimeter (ohm-cm).

[00226] Example 65 includes the subject matter of Example 54, and optionally, comprising forming a micro lens, wherein the absorption area is between the micro lens and the barrier layer.

[00227] Example 66 includes the subject matter of Example 65, and optionally, comprising forming an anti-reflective coating (ARC) layer, the ARC layer is between the micro lens and the absorption area.

[00228] Example 67 includes the subject matter of Example 54, and optionally, wherein the one or more MOS transistors comprise one or more transistors selected from a group consisting of one or more P-type MOS (PMOS) transistors and one or more N-type MOS (NMOS) transistors.

[00229] Example 68 includes the subject matter of Example 54, and optionally, wherein the barrier layer comprises a deep PW implant.

[00230] Example 69 includes the subject matter of Example 54, and optionally, wherein the barrier layer comprises a boron implant.

[00231] Example 70 includes the subject matter of Example 54, and optionally, wherein the photodiode comprises a fully pinned diode.

[00232] Example 71 includes the subject matter of Example 54, and optionally, wherein the photodiode comprises a non-pinned diode

[00233] Functions, operations, components and/or features described herein with reference to one or more embodiments, may be combined with, or may be utilized in combination with, one or more other functions, operations, components and/or features described herein with reference to one or more other embodiments, or vice versa.

[00234] While certain features have been illustrated and described herein, many modifications, substitutions, changes, and equivalents may occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

CLAIMS

What is claimed is:

1. A back-side illumination (BSI) complementary metal–oxide–semiconductor (CMOS) pixel array comprising:
 - a plurality of pixels, a pixel of said plurality of pixels comprising:
 - one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-Well (NW) region or a P-well (PW) region;
 - a photodiode;
 - an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode;
 - and
 - a barrier layer separating said absorption area from said one or more well regions.
2. The BSI CMOS pixel array of claim 1, wherein said photodiode comprises a low fill factor (FF) diode.
3. The BSI CMOS pixel array of claim 1, wherein said collection area extends from said absorption area to said photodiode through said barrier layer.
4. The BSI CMOS pixel array of claim 1, wherein said collection area is configured to perform the functionality of an electrostatic lens to collect said electrons from said absorption area.
5. The BSI CMOS pixel array of claim 1, wherein said barrier layer is configured to prevent diffusion of said electrons from said absorption area to said well regions.
6. The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 4 micron (um).
7. The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 10 micron (um).

8. The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 15 micron (um).
9. The BSI CMOS pixel array of claim 1, wherein a resistivity of said epi layer is greater than 100 ohm to centimeter (ohm-cm).
10. The BSI CMOS pixel array of claim 1 comprising a micro lens, said absorption area is between said micro lens and said barrier layer.
11. The BSI CMOS pixel array of claim 1 comprising an anti-reflective coating (ARC) layer, said ARC layer is between said micro lens and said absorption area.
12. The BSI CMOS pixel array of claim 1, wherein said one or more MOS transistors comprise one or more transistors selected from a group consisting of one or more P-type MOS (PMOS) transistors and one or more N-type MOS (NMOS) transistors.
13. The BSI CMOS pixel array of claim 1, wherein said barrier layer comprises a deep PW implant.
14. The BSI CMOS pixel array of claim 1, wherein said barrier layer comprises a boron implant.
15. The BSI CMOS pixel array of claim 1, wherein said photodiode comprises a fully pinned diode.
16. A complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) comprising:
 - a circuitry; and
 - a back-side illumination (BSI) pixel array comprising:
 - a plurality of pixels, a pixel of said plurality of pixels comprising:
 - one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-Well (NW) region or a P-well (PW) region;
 - a photodiode;
 - an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to said absorbed photons, and said collection area connecting said absorption area to

said photodiode to provide said electrons from said absorption area to said photodiode; and

a barrier layer separating said absorption area from said well regions.

17. The CMOS IC of claim 16 comprising a guard ring separating said circuitry from said BSI pixel array.

18. The CMOS IC of claim 17, wherein said guard ring is configured to prevent diffusion of photoelectrons from said circuitry to said BSI pixel array.

19. An imaging device comprising:

a memory;

an input;

an output;

a processor; and

a complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) comprising:

a circuitry; and

a back-side illumination (BSI) pixel array comprising:

a plurality of pixels, a pixel of said plurality of pixel sensors comprising:

one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-Well (NW) region or a P-well (PW) region;

a photodiode;

an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to said absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and

a barrier layer separating said absorption area from said well regions.

20. The imaging device of claim 19 comprising a digital camera or a Smartphone.

ABSTRACT

Some demonstrative embodiments include devices and/or methods of Back Side Illumination (BSI) Complementary Metal–Oxide–Semiconductor (CMOS) pixel array. For example, a BSI CMOS pixel array may include a plurality of pixels, a pixel of the plurality of pixels may include one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of the one or more well regions comprising an N-Well (NW) region or a P-well (PW) region; a photodiode; an epitaxial (epi) layer comprising an absorption area and a collection area, the absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, and the collection area connecting the absorption area to the photodiode to provide the electrons from the absorption area to the photodiode; and a barrier layer separating the absorption area from the one or more well regions.

Electronic Patent Application Fee Transmittal

Application Number:				
Filing Date:				
Title of Invention:	Your fee transmittal sheet cannot be generated at this time. Please complete your submission. After completing your submission, please contact the Electronic Business Center (EBC) to request the fee transmittal sheet for this submission. We apologize for the inconvenience. Electronic Business Center (EBC) 1-866-217-9197 (toll-free) or 571-272-4100 6 a.m. to 12 Midnight Eastern Time Monday -Friday			
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Filer:				
Attorney Docket Number:				
Filing Fees				
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Pages:				
Claims:				
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Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
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Application Number: 14791657

Document Date: 07/06/2015

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
14/791,657	07/06/2015	2811	1600	TJZ1-P-00859-US	20	3

CONFIRMATION NO. 1756

FILING RECEIPT



0000000076342117

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ISRAEL

Date Mailed: 07/20/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

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Applicant(s)

Tower Semiconductor Ltd., Migdal Haemek, ISRAEL;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This appln claims benefit of 62/021,152 07/06/2014

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/791,657**

Projected Publication Date: 01/07/2016

Non-Publication Request: No

Early Publication Request: No

Title

APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/791,657	07/06/2015	Assaf Lahav	TJZ1-P-00859-US

CONFIRMATION NO. 1756

FORMALITIES LETTER



OC000000076342118

86530
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Azrieli Business Center
Triangle tower, 38th Floor
Tel Aviv, 6701101
ISRAEL

Date Mailed: 07/20/2015

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing.

Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.

The surcharge is due for any one of:

- late submission of the basic filing fee, search fee, or examination fee,
- late submission of inventor's oath or declaration,
- filing an application that does not contain at least one claim on filing, or
- submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- \$ **140** surcharge.
- \$(**0**) previous unapplied payment amount.
- \$ **140** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
Assaf Lahav

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

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/eggolla/

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/791,657				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720			
TOTAL CLAIMS (37 CFR 1.16(j))	20	minus 20 = *			OR	x 80 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 420 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	1600			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Assaf Lahav	Examiner:	Not yet assigned
Serial no.:	14/791,657	Group Art Unit:	2811
Filed:	July 6, 2015	Atty. Docket No.:	TJZ1-P-00859-US
For:	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY		

Mail Stop Missing Parts
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

**RESPONSE TO NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL
APPLICATION**

Sir:

This communication is in response to the Notice to File Missing Parts of Nonprovisional Application filed under 37 CFR 1.53(b), mailed July 20, 2015, pertaining to late submission of the inventor's declaration.

A Response is due September 21, 2015, since September 20, 2015 falls on a Weekend. Accordingly, this Response is being timely filed.

Applicant hereby submits a properly executed inventor's declaration for the inventor Assaf Lahav.

Applicant respectfully requests the acceptance of the Response.

The surcharge, in the amount of \$140.00, is being paid via EFS-Web.

If any additional fee is required, the undersigned hereby authorizes the Patent Office to charge such additional fee to Deposit Account 50-5839.

Respectfully submitted,

/Naim Shichrur/

Naim Shichrur

Agent for Applicant(s)

Registration No. 56,248

Dated: September 21, 2015

Customer No. 86530

Shichrur & Co.

132 Menahem Begin Blvd.

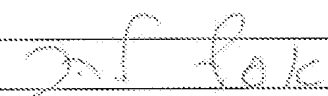
Triangle Tower, 38th Floor

Tel Aviv 67011, Israel

General Phone: (845) 335-4230

Facsimile: (212) 202-6436

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY
As the below named inventor, I hereby declare that: This declaration is directed to: ☐ The attached application, or ☒ United States application or PCT international application number <u>14/791,657</u> filed on <u>July 6, 2015</u> The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.	
LEGAL NAME OF INVENTOR Inventor: <u>Assaf Lahav</u> Date (Optional): _____ Signature: <u></u>	
Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.	

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	14791657			
Filing Date:	06-Jul-2015			
Title of Invention:	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY			
First Named Inventor/Applicant Name:	Assaf Lahav			
Filer:	Naim Avraham Shichrur/Yael Rapoport			
Attorney Docket Number:	TJZ1-P-00859-US			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Late Filing Fee for Oath or Declaration	1051	1	140	140
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				140

Electronic Acknowledgement Receipt

EFS ID:	23549977
Application Number:	14791657
International Application Number:	
Confirmation Number:	1756
Title of Invention:	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY
First Named Inventor/Applicant Name:	Assaf Lahav
Customer Number:	86530
Filer:	Naim Avraham Shichrur/Yael Rapoport
Filer Authorized By:	Naim Avraham Shichrur
Attorney Docket Number:	TJZ1-P-00859-US
Receipt Date:	21-SEP-2015
Filing Date:	06-JUL-2015
Time Stamp:	13:17:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 140
RAM confirmation Number	11424
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		TJZ1-P-00859-US- RESNOMP-21SEP15.PDF	293908 2acbc8cf54449d3a03893c1e7ed446636f3e e827	yes	3
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Applicant Response to Pre-Exam Formalities Notice		1	2	
	Oath or Declaration filed		3	3	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30887 d943300b254e7f35ff738ba45f1a0aeff304 30a	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			324795		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/791,657			
APPLICATION AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720		
TOTAL CLAIMS (37 CFR 1.16(j))	20	minus 20 = *			OR	x 80 =	0.00		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 420 =	0.00		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00		
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	1600		
APPLICATION AS AMENDED - PART II									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)		
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	OR	x =		
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	OR	x =		
	Application Size Fee (37 CFR 1.16(s))					OR			
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					OR			
				TOTAL ADD'L FEE		TOTAL ADD'L FEE			
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)		
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	OR	x =		
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	OR	x =		
	Application Size Fee (37 CFR 1.16(s))					OR			
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					OR			
				TOTAL ADD'L FEE		TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.									



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www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
14/791,657	07/06/2015	2811	1740	TJZ1-P-00859-US	20	3

CONFIRMATION NO. 1756

UPDATED FILING RECEIPT



86530
Shichrur & Co.
Azrieli Business Center
Triangle tower, 38th Floor
Tel Aviv, 6701101
ISRAEL

Date Mailed: 09/28/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Assaf Lahav, Binyamina, ISRAEL;
Amos Fenigstein, Haifa, ISRAEL;

Applicant(s)

Tower Semiconductor Ltd., Migdal Haemek, ISRAEL;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This appln claims benefit of 62/021,152 07/06/2014

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 07/16/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/791,657**

Projected Publication Date: 01/07/2016

Non-Publication Request: No

Early Publication Request: No

Title

APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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NOT GRANTED

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14791657	
	Filing Date		2015-07-06	
	First Named Inventor	Assaf Lahav		
	Art Unit	2811		
	Examiner Name	Not yet known		
	Attorney Docket Number	TJZ1-P-00859-US		

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5461425		1995-10-24	Fowler et al.	

If you wish to add additional U.S. Patent citation information please click the Add button.

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U.S.PATENT APPLICATION PUBLICATIONS						Remove
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² i	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14791657
	Filing Date		2015-07-06
	First Named Inventor	Assaf Lahav	
	Art Unit	2811	
	Examiner Name	Not yet known	
	Attorney Docket Number	TJZ1-P-00859-US	

1	ETOH, TAKEHARU G., ET AL, "Toward One Giga Frames per Second — Evolution of in Situ Storage Image Sensors", Sensors 13.4 (2013): 4640-4658, published April 08, 2013, 19 pages.	☐
2	Nae-In LEE et al., "Effect of the Silicidation Reaction Condition on the Gate Oxide Integrity in Ti-polycide Gate", Jpn. J. Appl. Vol. 33, January 1994, pp. 672-677, Part 1, No. 1B, 6 pages	☐
3	Naoya Watanabe et al., "Fabrication of Back-Side Illuminated Complementary Metal Oxide Semiconductor Image Sensor Using Compliant Bump", Japanese Journal of Applied Physics 49, 2010, 04DB01, 8 pages	☐

If you wish to add additional non-patent literature document citation information please click the Add button **Add**

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	14791657
Filing Date	2015-07-06
First Named Inventor	Assaf Lahav
Art Unit	2811
Examiner Name	Not yet known
Attorney Docket Number	TJZ1-P-00859-US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Naim Shichrur/	Date (YYYY-MM-DD)	2015-10-19
Name/Print	Naim Shichrur	Registration Number	56,248

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	23815973
Application Number:	14791657
International Application Number:	
Confirmation Number:	1756
Title of Invention:	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY
First Named Inventor/Applicant Name:	Assaf Lahav
Customer Number:	86530
Filer:	Naim Avraham Shichrur/Yael Rapoport
Filer Authorized By:	Naim Avraham Shichrur
Attorney Docket Number:	TJZ1-P-00859-US
Receipt Date:	19-OCT-2015
Filing Date:	06-JUL-2015
Time Stamp:	05:04:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	NPL2.pdf	1906648 04c0faea17adbadc653c360d3bf3df69dfcb2294	no	6

Warnings:

Information:

2	Non Patent Literature	NPL3.pdf	839744 f79c6c934372e2997b97de07e48f69fe4f5a9524	no	8
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	TJZ1-P-00859-US-IDS-19OCT15.PDF	612433 9fd115537a46fa1b6a40339ef2502055198bb8a6	no	4
Warnings:					
Information:					
4	Non Patent Literature	NPL1.pdf	3118417 5fb98c596d216c279d839946508e79a98ce54f5f	no	19
Warnings:					
Information:					
Total Files Size (in bytes):			6477242		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/791,657	07/06/2015	Assaf Lahav	TJZ1-P-00859-US

CONFIRMATION NO. 1756

PUBLICATION NOTICE



OC000000079763180

86530
Shichrur & Co.
Azrieli Business Center
Triangle tower, 38th Floor
Tel Aviv, 6701101
ISRAEL

Title: APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY

Publication No. US-2016-0005896-A1

Publication Date: 01/07/2016

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

86530 7590 01/20/2016
Shichrur & Co.
Azrieli Business Center
Triangle tower, 38th Floor
Tel Aviv, 6701101
ISRAEL

EXAMINER

VU, HUNG K

ART UNIT

PAPER NUMBER

2897

DATE MAILED: 01/20/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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14/791,657

07/06/2015

Assaf Lahav

TJZ1-P-00859-US

1756

TITLE OF INVENTION: APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	04/20/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

86530 7590 01/20/2016
Shichrur & Co.
Azrieli Business Center
Triangle tower, 38th Floor
Tel Aviv, 6701101
ISRAEL

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/791,657	07/06/2015	Assaf Lahav	TJZ1-P-00859-US	1756

TITLE OF INVENTION: APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	04/20/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
VU, HUNG K	2897	257-292000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.	2. For printing on the patent front page, list (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____ (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____ 3 _____
---	---

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.27
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____
 Typed or printed name _____ Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/791,657	07/06/2015	Assaf Lahav	TJZ1-P-00859-US	1756
86530	7590	01/20/2016	EXAMINER	
Shichrur & Co. Azrieli Business Center Triangle tower, 38th Floor Tel Aviv, 6701101 ISRAEL			VU, HUNG K	
			ART UNIT	PAPER NUMBER
			2897	

DATE MAILED: 01/20/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/791,657	Applicant(s) LAHAV ET AL.	
	Examiner HUNG VU	Art Unit 2897	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Application filed on 07/06/2015.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. ☒ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☒ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date <u>10/19/15</u> | 6. ☒ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other _____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

/HUNG VU/
Primary Examiner, Art Unit 2897

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Allowable Subject Matter

1. Claims 1-20 are allowed.

2. The following is an examiner's statement of reasons for allowance:

Applicant's claims 1-20 are allowable over the references of record because none of these references disclose or can be combined to yield the claimed back-side illumination complementary metal-oxide-semiconductor pixel array comprising a plurality of pixels, a pixel of the plurality of pixels comprising one or more Metal-Oxide Semiconductor transistors comprising one or more well regions, a well region of the one or more well regions comprising an N-well region or a P-well region, an epitaxial layer comprising an absorption area and a collection area, the absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, the collection area connecting the absorption area to the photodiode, a barrier layer separating the absorption area from the one or more well regions, in combination with the remaining claimed limitations of claim 1, the claimed complementary metal-oxide-semiconductor integrated circuit comprising a plurality of pixels, a pixel of the plurality of pixels comprising one or more Metal-Oxide Semiconductor transistors comprising one or more well regions, a well region of the one or more well regions comprising an N-well region or a P-well region, an epitaxial layer comprising an absorption area and a collection area, the absorption area to absorb incoming photons and to generate electrons responsive to absorbed

Art Unit: 2897

photons, the collection area connecting the absorption area to the photodiode, a barrier layer separating the absorption area from the one or more well regions, in combination with the remaining claimed limitations of claim 16; the claimed imaging device comprising a plurality of pixels, a pixel of the plurality of pixels comprising one or more Metal-Oxide Semiconductor transistors comprising one or more well regions, a well region of the one or more well regions comprising an N-well region or a P-well region, an epitaxial layer comprising an absorption area and a collection area, the absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, the collection area connecting the absorption area to the photodiode, a barrier layer separating the absorption area from the one or more well regions, in combination with the remaining claimed limitations of claim 19.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gidon et al. (PN 8,735,953), Augusto (PN 8,120,079), and Takeuchi (US 2009/0184387) disclose the formation of the plurality of pixels.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Monday to Friday 6:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fernando L. Toledo can be reached on (571) 272 - 1867. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hung Vu/

Primary Examiner

Notice of References Cited	Application/Control No. 14/791,657	Applicant(s)/Patent Under Reexamination LAHAV ET AL.	
	Examiner HUNG VU	Art Unit 2897	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-8,735,953 B2	05-2014	Gidon; Pierre	H01L27/14625	257/291
*	B	US-8,120,079 B2	02-2012	Augusto; Carlos J. R. P.	H01L27/14669	257/184
*	C	US-2009/0184387 A1	07-2009	Takeuchi; Kiyoshi	H01L27/1464	257/440
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
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	P					
	Q					
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	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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BIB DATA SHEET

CONFIRMATION NO. 1756

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
14/791,657	07/06/2015	257	2897	TJZ1-P-00859-US		
APPLICANTS Tower Semiconductor Ltd., Migdal Haemek, ISRAEL; INVENTORS Assaf Lahav, Binyamina, ISRAEL; Amos Fenigstein, Haifa, ISRAEL; ** CONTINUING DATA ***** This appln claims benefit of 62/021,152 07/06/2014 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 07/16/2015						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/HUNG K VU/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY ISRAEL	SHEETS DRAWINGS 6	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS Shichrur & Co. Azrieli Business Center Triangle tower, 38th Floor Tel Aviv, 6701101 ISRAEL						
TITLE APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY						
FILING FEE RECEIVED 1740	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14791657	
	Filing Date		2015-07-06	
	First Named Inventor	Assaf Lahav		
	Art Unit	2811		
	Examiner Name	Not yet known		
	Attorney Docket Number	TJZ1-P-00859-US		

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5461425		1995-10-24	Fowler et al.	

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	14791657
Filing Date	2015-07-06
First Named Inventor	Assaf Lahav
Art Unit	2811
Examiner Name	Not yet known
Attorney Docket Number	TJZ1-P-00859-US

1	ETOH, TAKEHARU G., ET AL, "Toward One Giga Frames per Second — Evolution of in Situ Storage Image Sensors", Sensors 13.4 (2013): 4640-4658, published April 08, 2013, 19 pages.	☐
2	Nae-In LEE et al., "Effect of the Silicidation Reaction Condition on the Gate Oxide Integrity in Ti-polycide Gate", Jpn. J. Appl. Vol. 33, January 1994, pp. 672-677, Part 1, No. 1B, 6 pages	☐
3	Naoya Watanabe et al., "Fabrication of Back-Side Illuminated Complementary Metal Oxide Semiconductor Image Sensor Using Compliant Bump", Japanese Journal of Applied Physics 49, 2010, 04DB01, 8 pages	☐

If you wish to add additional non-patent literature document citation information please click the Add button **Add**

EXAMINER SIGNATURE

Examiner Signature	/Hung Vu/	Date Considered	12/30/15
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

Index of Claims



Application/Control No.

14/791,657

Examiner

HUNG VU

Applicant(s)/Patent under
Reexamination

LAHAV ET AL.

Art Unit

2897

✓	Rejected
=	Allowed

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N	Non-Elected
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A	Appeal
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Claim		Date									
Final	Original	12/31/15									
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Issue Classification 	Application/Control No. 14791657	Applicant(s)/Patent Under Reexamination LAHAV ET AL.	
	Examiner HUNG VU	Art Unit 2897	

CPC						
Symbol					Type	Version
H01L		31	/	035272	F	2013-01-01
H01L		27	/	1464	I	2013-01-01
H01L		27	/	14643	I	2013-01-01
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NONE		Total Claims Allowed:	
		20	
(Assistant Examiner)	(Date)		
/HUNG VU/ Primary Examiner.Art Unit 2897	12/31/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Issue Classification 	Application/Control No. 14791657	Applicant(s)/Patent Under Reexamination LAHAV ET AL.
	Examiner HUNG VU	Art Unit 2897

☐ Claims renumbered in the same order as presented by applicant															
☐ CPA															
☐ T.D.															
☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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NONE	Total Claims Allowed: 20	
(Assistant Examiner)	(Date)	
/HUNG VU/ Primary Examiner.Art Unit 2897	12/31/2015	O.G. Print Claim(s) 1
(Primary Examiner)	(Date)	O.G. Print Figure 2

Search Notes 	Application/Control No. 14791657	Applicant(s)/Patent Under Reexamination LAHAV ET AL.
	Examiner HUNG VU	Art Unit 2897

CPC- SEARCHED		
Symbol	Date	Examiner
H01L27/1464, H01L27/14643, H01L27/3227, H01L31/035272	12/30/2015	/HV/

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	292, 294, 432, 447, 460	12/30/2015	/HV/

SEARCH NOTES		
Search Notes	Date	Examiner
EAST	12/30/2015	/HV/
Inventors Search	12/30/2015	/HV/

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
H01L	27/1464, 27/14643, 27/3227, 31/035272	12/30/2015	/HV/

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	Type	Hits	Search Text	DBs	Time Stamp
1	BRS	0	14/791657	US-PGPUB; USPAT	2015/12/30 07:31
2	BRS	43	((LAHAV near3 ASSAF)(FENIGSTEIN near3 AMOS)).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 07:32
3	BRS	0	S2 and (light near3 (emitting emitted) LED) and (back adj side backside)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 07:33
4	BRS	0	S2 and (light near3 (emitting emitted) LED)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 07:33
5	BRS	9	S2 and (pixel) and (back adj side backside)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 07:34
6	IS&R	11910	(257/292,294,432,447,460).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 07:49

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7	BRS	1395	S6 and (photodiode photo adj diode) and (backside back adj side back-side)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 07:50
8	BRS	375	S7 and (absor\$7) and (collect\$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 07:51
9	BRS	13144	H01L27/14643.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 10:45
10	BRS	634	H01L27/3227.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 10:45
11	BRS	6524	H01L27/1464.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 10:51
12	BRS	677	H01L31/035272.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 10:51

	Type	Hits	Search Text	DBs	Time Stamp
13	BRS	19257	S9 or S10 or S11 or S12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 10:51
14	BRS	2408	S13 and (photodiode photo adj diode) and (backside back adj side back-side)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 10:52
15	BRS	593	S14 and (absor\$7) and (collect\$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 10:52
16	BRS	363	S15 not S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 10:52
17	BRS	1759	(photodiode photo adj diode) and (backside back adj side back-side) and (absor\$7) and (collect\$5) and barrier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 14:57
18	BRS	1688	S17 and well	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 14:57

	Type	Hits	Search Text	DBs	Time Stamp
19	BRS	695	S18 and photon and electron	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2015/12/30 14:58
20	BRS	43	((LAHAV near3 ASSAF)(FENIGSTEIN near3 AMOS)).in.	US-PGPUB; USPAT	2015/12/31 09:15
21	BRS	9	S20 and (pixel) and (back adj side backside)	US-PGPUB; USPAT	2015/12/31 09:15
22	BRS	0	((photodiode photo adj diode) and (backside back adj side back-side) and (absor\$7) and (collect\$5) and barrier and photon and electron).clm.	US-PGPUB; USPAT	2015/12/31 09:16

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number

14/791,657

Filing Date

July 6, 2015

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)



I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

86530

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Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Tower Semiconductor Ltd.



Inventor or Joint Inventor (title not required below)



Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)



Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)



Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

Dina Back

Title

Associate Legal Counsel

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.



Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Electronic Acknowledgement Receipt

EFS ID:	25539485
Application Number:	14791657
International Application Number:	
Confirmation Number:	1756
Title of Invention:	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY
First Named Inventor/Applicant Name:	Assaf Lahav
Customer Number:	86530
Filer:	Naim Avraham Shichrur/Soshia Feldhamer
Filer Authorized By:	Naim Avraham Shichrur
Attorney Docket Number:	TJZ1-P-00859-US
Receipt Date:	20-APR-2016
Filing Date:	06-JUL-2015
Time Stamp:	03:25:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Assignee showing of ownership per 37 CFR 3.73	TJZ1-P-00859-US-0096-20APR16.pdf	1518529 bab9ba5ec625dda7c9df58578694d0b166a02d8a	no	5

Warnings:

Information:

2	Power of Attorney	TJZ1-P-00859-US- POA-20APR16.pdf	848592 523c31fd5f42e7fcb6b9ef8ff6515cc07b029 cb1	no	1
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Information:					
Total Files Size (in bytes):				2367121	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: Tower Semiconductor Ltd.Application No./Patent No.: 14/791,657 Filed/Issue Date: July 6, 2015Titled: APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAYTower Semiconductor Ltd., a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
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5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
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6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Naim Shichrur/

Signature

Naim Shichrur

Printed or Typed Name

April 20, 2016

Date

56248

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ASSIGNMENT

In consideration of One Dollar (\$1.00), and other good and valuable considerations, the Receipt of which is hereby acknowledged, I the undersigned, Assaf Lahav residing at 9 Ha Alon, Binyamina 30500, Israel; Amos Fenigstein residing at 63 Hatichon, Haifa 32293, Israel;

Hereby sell, assign and transfer to Tower Semiconductor Ltd., located at P.O. Box 619, Ramat Gavriel Industrial Park, Migdal Haemek 23105, Israel its successors, assigns and legal representatives (hereinafter, the "Assignee"), the entire right, title and interest for all countries, in and to any and all inventions which are disclosed and claimed, and as possessed by the undersigned, any and all inventions which are disclosed but not claimed in the application for United States Patent U.S. Serial No. (14/791,657) filed (July 6, 2015) and being entitled:

**APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI)
COMPLEMENTARY METAL–OXIDE–SEMICONDUCTOR (CMOS) PIXEL ARRAY**

and in and to said application and all divisional, continuing, substitute, renewal, reissue, and all other applications for U.S. Letters Patent or other related property rights in any and all foreign countries which have been or shall be filed on any of said inventions disclosed in said application; and in and to all original and reissued patents or related foreign documents which have been or shall be issued on said inventions. I hereby authorize and request our attorney(s), associated with **customer number 86530**, to insert in the parentheses above, the filing date and US Serial No. of said application when known;

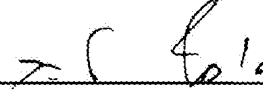
Authorize and request the Commissioner of Patents of the United States to issue to said Assignee, the corporation above named, its successors, assigns and legal representatives, in accordance with this assignment, any and all United States Letters Patent on said inventions or any of them disclosed in said application;

Agree that said Assignee may apply for and receive foreign Letters Patent or rights of any other kind for said inventions, or any of them; and may claim, in applications for said foreign Letters Patent or other rights, the priority of the aforesaid United States patent application under the provisions of the International Convention of 1883 and later modifications thereof, under the Patent

Cooperation Treaty, under the European Patent Convention or under any other available international agreement; and that, when requested, without charge to, but at the expense of, said Assignee, its successors, assigns and legal representatives, to carry out in good faith the intent and purpose of this assignment, the under-signed or the undersigned's executors or administrators will, for the United States and all foreign countries, execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications or other documents on any and all said inventions; execute all rightful oaths, assignments, powers of attorney and other papers; communicate to said Assignee, its successors, assigns and representatives, all facts known and documents available to the undersigned relating to said inventions and the history thereof; testify in all legal proceedings; and generally do everything possible which said Assignee, its successors, assigns or representatives shall consider desirable for aiding in securing, maintaining and enforcing proper patent protection for said inventions and for vesting title to said inventions and all applications for patents or related foreign rights and all patents on said inventions, in said Assignee, its successors, assigns and legal representatives; and

COVENANT with said Assignee, its successors, assigns and legal representatives that no assignment, grant, mortgage, license or other agreement affecting the rights and property herein conveyed has been made to others by the undersigned, and that full right to convey the same as herein expressed is possessed by the undersigned.

IN TESTIMONY WHEREOF, I have hereunto set my hand this 22 day of October, 2015.



Assaf Lahav

IN TESTIMONY WHEREOF, I have hereunto set my hand this 26 day of October, 2015.



Amos Fenigstein

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Assaf Lahav	Examiner:	VU, HUNG K
Serial No.:	14/791,657	Group Art Unit:	2897
Filed:	July 6, 2015		
Title:	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY		

AMENDMENT UNDER 37 CFR §1.312

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.312, kindly amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims, which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Filing Date: July 6, 2015

Title: APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY

Page 2

AMENDMENTS TO THE CLAIMS

Please add or amend the claims to read as follows, and cancel without prejudice or disclaimer to resubmission in a divisional or continuation application claims indicated as cancelled:

1. (Original) A back-side illumination (BSI) complementary metal-oxide-semiconductor (CMOS) pixel array comprising:
 - a plurality of pixels, a pixel of said plurality of pixels comprising:
 - one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-Well (NW) region or a P-well (PW) region;
 - a photodiode;
 - an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and
 - a barrier layer separating said absorption area from said one or more well regions.
2. (Original) The BSI CMOS pixel array of claim 1, wherein said photodiode comprises a low fill factor (FF) diode.
3. (Original) The BSI CMOS pixel array of claim 1, wherein said collection area extends from said absorption area to said photodiode through said barrier layer.
4. (Original) The BSI CMOS pixel array of claim 1, wherein said collection area is configured to perform the functionality of an electrostatic lens to collect said electrons from said absorption area.

Filing Date: July 6, 2015

Title: APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY

Page 3

-
5. (Original) The BSI CMOS pixel array of claim 1, wherein said barrier layer is configured to prevent diffusion of said electrons from said absorption area to said well regions.
 6. (Original) The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 4 micron (um).
 7. (Original) The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 10 micron (um).
 8. (Original) The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 15 micron (um).
 9. (Original) The BSI CMOS pixel array of claim 1, wherein a resistivity of said epi layer is greater than 100 ohm to centimeter (ohm-cm).
 10. (Original) The BSI CMOS pixel array of claim 1 comprising a micro lens, said absorption area is between said micro lens and said barrier layer.
 11. (Currently Amended) The BSI CMOS pixel array of claim ~~[[1]]~~ 10 comprising an anti-reflective coating (ARC) layer, said ARC layer is between said micro lens and said absorption area.
 12. (Original) The BSI CMOS pixel array of claim 1, wherein said one or more MOS transistors comprise one or more transistors selected from a group consisting of one or more P-type MOS (PMOS) transistors and one or more N-type MOS (NMOS) transistors.
 13. (Original) The BSI CMOS pixel array of claim 1, wherein said barrier layer comprises a deep PW implant.
 14. (Original) The BSI CMOS pixel array of claim 1, wherein said barrier layer comprises a boron implant.

Filing Date: July 6, 2015

Title: APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY

Page 4

15. (Original) The BSI CMOS pixel array of claim 1, wherein said photodiode comprises a fully pinned diode.

16. (Original) A complementary metal–oxide–semiconductor (CMOS) integrated circuit (IC) comprising:

a circuitry; and

a back-side illumination (BSI) pixel array comprising:

a plurality of pixels, a pixel of said plurality of pixels comprising:

one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-Well (NW) region or a P-well (PW) region;

a photodiode;

an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to said absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and

a barrier layer separating said absorption area from said well regions.

17. (Original) The CMOS IC of claim 16 comprising a guard ring separating said circuitry from said BSI pixel array.

18. (Original) The CMOS IC of claim 17, wherein said guard ring is configured to prevent diffusion of photoelectrons from said circuitry to said BSI pixel array.

19. (Original) An imaging device comprising:

a memory;

an input;

an output;

a processor; and

Filing Date: July 6, 2015

Title: APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY

Page 5

a complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) comprising:

a circuitry; and

a back-side illumination (BSI) pixel array comprising:

a plurality of pixels, a pixel of said plurality of pixel sensors comprising:

one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-Well (NW) region or a P-well (PW) region;

a photodiode;

an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to said absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and

a barrier layer separating said absorption area from said well regions.

20. (Original) The imaging device of claim 19 comprising a digital camera or a Smartphone.

Filing Date: July 6, 2015

Title: APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY

Page 6

REMARKS

The foregoing amendments and remarks are directed to formalities, in order to move the above-referenced patent application to issue. Entry of this paper is respectfully requested.

Remarks to the Claims

Claim 11 has been amended to amend a typographical error.

No new matter has been added.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Filing Date: July 6, 2015

Title: APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-
SEMICONDUCTOR (CMOS) PIXEL ARRAY

Page 7

No fees are believed to be necessary. However, if any fees are necessary please charge any additional fees or credit overpayment to Deposit Account No. 50-5839.

Respectfully submitted,

/Naim Shichrur/

Naim Shichrur
Agent for Applicant
Registration No. 56,248

Dated: April 20, 2016

Customer No. 86530
Shichrur & Co.

132 Menahem Begin Blvd.
Triangle Tower, 38th Floor
Tel Aviv 6701101, Israel
General Phone: (845) 335-4230
Facsimile: (212) 202-6436

Electronic Acknowledgement Receipt

EFS ID:	25543632
Application Number:	14791657
International Application Number:	
Confirmation Number:	1756
Title of Invention:	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY
First Named Inventor/Applicant Name:	Assaf Lahav
Customer Number:	86530
Filer:	Naim Avraham Shichrur/Yael Rapoport
Filer Authorized By:	Naim Avraham Shichrur
Attorney Docket Number:	TJZ1-P-00859-US
Receipt Date:	20-APR-2016
Filing Date:	06-JUL-2015
Time Stamp:	13:01:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		TJZ1-P-00859-US-312_Amendment-20APR16.pdf	43440 c4543444e6508adf88c468ae620a6d78336148e7	yes	7

Multipart Description/PDF files in .zip description			
Document Description	Start	End	
Amendment after Notice of Allowance (Rule 312)	1	1	
Claims	2	5	
Applicant Arguments/Remarks Made in an Amendment	6	7	

Warnings:

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

86530 7590 01/20/2016
Shichrur & Co.
Azrieli Business Center
Triangle tower, 38th Floor
Tel Aviv, 6701101
ISRAEL

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/791,657	07/06/2015	Assaf Lahav	TJZ1-P-00859-US	1756

TITLE OF INVENTION: APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	04/20/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
VU, HUNG K	2897	257-292000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Shichrur & Co.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Tower Semiconductor Ltd.

Migdal Haemek, Israel

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

- ☐ A check is enclosed.
- ☒ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Naim Shichrur/

Date April 19, 2016

Typed or printed name Naim Shichrur

Registration No. 56248

Electronic Patent Application Fee Transmittal				
Application Number:		14791657		
Filing Date:		06-Jul-2015		
Title of Invention:		APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY		
First Named Inventor/Applicant Name:		Assaf Lahav		
Filer:		Naim Avraham Shichrur/Yael Rapoport		
Attorney Docket Number:		TJZ1-P-00859-US		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Utility Appl Issue Fee	1501	1	960	960
Publ. Fee- Early, Voluntary, or Normal	1504	1	0	0
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt

EFS ID:	25543736
Application Number:	14791657
International Application Number:	
Confirmation Number:	1756
Title of Invention:	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY
First Named Inventor/Applicant Name:	Assaf Lahav
Customer Number:	86530
Filer:	Naim Avraham Shichrur/Yael Rapoport
Filer Authorized By:	Naim Avraham Shichrur
Attorney Docket Number:	TJZ1-P-00859-US
Receipt Date:	20-APR-2016
Filing Date:	06-JUL-2015
Time Stamp:	13:06:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$960
RAM confirmation Number	10530
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	TJZ1-P-00859-US- ISSFEE-20APR16.PDF	101467	no	1
			5b0fe0982d0e4fd5803569c5721872fc20b498f9		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32786	no	2
			769f3ec89d8720c3f2b1b337825d8e144d22fc1b		
Warnings:					
Information:					
Total Files Size (in bytes):			134253		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/791,657	07/06/2015	Assaf Lahav	TJZ1-P-00859-US

CONFIRMATION NO. 1756

POA ACCEPTANCE LETTER



OC000000082375694

86530
Shichrur & Co.
Azrieli Business Center
Triangle tower, 38th Floor
Tel Aviv, 6701101
ISRAEL

Date Mailed: 04/22/2016

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 04/20/2016.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/nhorne/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Assaf Lahav	Examiner:	VU, HUNG K
Serial No.:	14/791,657	Group Art Unit:	2897
Filed:	July 6, 2015		
Title:	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY		

AMENDMENT UNDER 37 CFR §1.312

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Please Enter.

Sir:

Thank you.

Pursuant to 37 CFR §1.312, kindly amend the above-identified application as follows:

/HV/

Amendments to the Claims are reflected in the listing of claims, which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/791,657	07/06/2015	Assaf Lahav	TJZ1-P-00859-US	1756
86530	7590	04/28/2016	EXAMINER	
Shichrur & Co. Azrieli Business Center Triangle tower, 38th Floor Tel Aviv, 6701101 ISRAEL			VU, HUNG K	
			ART UNIT	PAPER NUMBER
			2897	
			NOTIFICATION DATE	DELIVERY MODE
			04/28/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

DocketingUS@ShichrurLaw.com
Yael@ShichrurLaw.com

Response to Rule 312 Communication	Application No. 14/791,657	Applicant(s) LAHAV ET AL.
	Examiner HUNG VU	Art Unit 2897

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ The amendment filed on 20 April 2016 under 37 CFR 1.312 has been considered, and has been:

a) ☐ entered.

b) ☒ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.

Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

	/HUNG VU/ Primary Examiner, Art Unit 2897
--	--



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/791,657	05/31/2016	9356169	TJZ1-P-00859-US	1756

86530 7590 05/11/2016
Shichrur & Co.
Azrieli Business Center
Triangle tower, 38th Floor
Tel Aviv, 6701101
ISRAEL

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Assaf Lahav, Binyamina, ISRAEL;
Tower Semiconductor Ltd., Migdal Haemek, ISRAEL;
Amos Fenigstein, Haifa, ISRAEL;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

Patent 9,356,169

IN UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.: 9,356,169

Docket No: TJZ1-P-00859-US

Issue Date: May 31, 2016

Patentee: Tower Semiconductor Ltd.

Title APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION
(BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS)
PIXEL ARRAY

REQUEST FOR CERTIFICATE OF CORRECTION

Attn: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

It is requested that a Certificate of Correction be issued correcting printing errors appearing in the above-identified United States patent. A copy of the text of the Certificate in the suggested form is enclosed.

Issuance of the Certificate of Correction would neither expand nor contract the scope of the claims as properly allowed, and re-examination is not required.

Pursuant to 1.20(a), the charge of \$100.00 is being paid via EFS-Web.

The Examiner is authorized to charge any additional fees or credit overpayment to Deposit Account No. 50-5839.

Respectfully submitted,

By Representatives,

Customer Number: 86530

/Naim Shichrur/

Naim Shichrur

Registration No. 56,248

Dated: April 3, 2017

Customer No. 86530

Shichrur & Co.

Azrieli Business Center

Triangle Tower, 38th Floor

Tel Aviv 6701101, Israel

General Phone: (845) 335-4230

Facsimile: (212) 202-6436

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO : 9,356,169

Page 1 of 1

APPLICATION NO.: 14/791,657

ISSUE DATE : May 31, 2016

INVENTOR(S) : Assaf Lahav et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 16, line 62, in claim 19, delete "pixel sensors" and insert - - pixels - -, therefor.

MAILING ADDRESS OF SENDER:

PATENT NO. 9,356,169

CPA Global
P.O. Box 52050
Minneapolis, MN 55402

No. of additional copies



Atty Docket No: TJZ1-P-00859-US

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO : 9,356,169

Page 1 of 1

APPLICATION NO.: 14/791,657

ISSUE DATE : May 31, 2016

INVENTOR(S) : Assaf Lahav et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 16, line 62, in claim 19, delete "pixel sensors" and insert - - pixels - -, therefor.

MAILING ADDRESS OF SENDER:

PATENT NO. 9,356,169

CPA Global
P.O. Box 52050
Minneapolis, MN 55402

No. of additional copies



Atty Docket No: TJZ1-P-00859-US

Electronic Patent Application Fee Transmittal

Application Number:	14791657			
Filing Date:	06-Jul-2015			
Title of Invention:	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY			
First Named Inventor/Applicant Name:	Assaf Lahav			
Filer:	Naim Avraham Shichrur/Soshia Feldhamer			
Attorney Docket Number:	TJZ1-P-00859-US			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Certificate of correction	1811	1	100	100

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				100

Electronic Acknowledgement Receipt

EFS ID:	28846795
Application Number:	14791657
International Application Number:	
Confirmation Number:	1756
Title of Invention:	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY
First Named Inventor/Applicant Name:	Assaf Lahav
Customer Number:	86530
Filer:	Naim Avraham Shichrur/Soshia Feldhamer
Filer Authorized By:	Naim Avraham Shichrur
Attorney Docket Number:	TJZ1-P-00859-US
Receipt Date:	06-APR-2017
Filing Date:	06-JUL-2015
Time Stamp:	04:38:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 100
RAM confirmation Number	040617INTEFSW04401000
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	TJZ1-P-00859-US- RQST_COC-06APR17.pdf	140186	no	3
			61c7e8617c8f5ae9f65fcbd0914fa3000941 bef4		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30714	no	2
			8b83a0bec718eafa702e53daacf13ba88e3d b129		
Warnings:					
Information:					
Total Files Size (in bytes):			170900		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

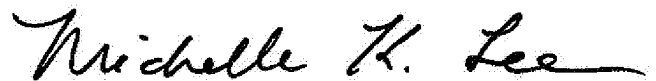
PATENT NO. : 9,356,169 B2
APPLICATION NO. : 14/791657
DATED : May 31, 2016
INVENTOR(S) : Assaf Lahav et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 16, Line 62, in Claim 19, delete “pixel sensors” and insert -- pixels --, therefor.

Signed and Sealed this
Second Day of May, 2017

A handwritten signature in black ink, reading "Michelle K. Lee". The signature is written in a cursive, flowing style with a long horizontal line extending from the end.

Michelle K. Lee
Director of the United States Patent and Trademark Office

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fax to:
571-273-6500

- OR -

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below:** If you have a Customer Number to represent the fee address. **When to check the second box below:** If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☒ Customer Number: 22888

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
9,356,169	14/791,657

Completed by (check one):

☐ Applicant/Inventor	/E. Eric Hoffman/ Signature
☒ Attorney or Agent of record 38186 (Reg. No.)	E. Eric Hoffman Typed or printed name
☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)	(925) 895-3545 Requester's telephone number
☐ Assignee recorded at Reel _____ Frame _____	June 28, 2019 Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☐ * Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETE D FORMS TO THIS ADDRESS.

SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	36444656
Application Number:	14791657
International Application Number:	
Confirmation Number:	1756
Title of Invention:	APPARATUS, SYSTEM AND METHOD OF BACK SIDE ILLUMINATION (BSI) COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) PIXEL ARRAY
First Named Inventor/Applicant Name:	Assaf Lahav
Customer Number:	86530
Filer:	Edward Eric Hoffman/Carrie Reddick
Filer Authorized By:	Edward Eric Hoffman
Attorney Docket Number:	TJZ1-P-00859-US
Receipt Date:	28-JUN-2019
Filing Date:	06-JUL-2015
Time Stamp:	12:53:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Maintenance Fee Address Change	TSL-211-PTO-Fee-Adrs-CHG- Filed.pdf	447520 9773e7301210fd0277fa0970d14842d4b7e2999d	no	1

Warnings:

Information:	
Total Files Size (in bytes):	447520
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
---	---

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
filed in the U.S. District Court Eastern District of Texas, Marshall Division on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 2:21-cv-452	DATE FILED 12/14/2021	U.S. DISTRICT COURT Eastern District of Texas, Marshall Division
PLAINTIFF ALIDDOUBLE INC		DEFENDANT TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,168,965	1/2/2001	Alidouble Inc.
2 6,169,319	1/2/2001	Alidouble Inc.
3 9,356,169	5/31/2016	Alidouble Inc.
4 9,431,455	8/30/2016	Alidouble Inc.
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
-------	-------------------	------

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
---	---

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas, Marshall Division on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 2:21-cv-452	DATE FILED 12/14/2021	U.S. DISTRICT COURT Eastern District of Texas, Marshall Division
PLAINTIFF ALIDouble INC		DEFENDANT TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,168,965	1/2/2001	Alidouble Inc.
2 6,169,319	1/2/2001	Alidouble Inc.
3 9,356,169	5/31/2016	Alidouble Inc.
4 9,431,455	8/30/2016	Alidouble Inc.
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
-------	-------------------	------

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy