

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED,

Petitioner,

v.

ALIDDOUBLE, INC.

Patent Owner.

U.S. Patent No. 9,356,169

DECLARATION OF DR. KONSTANTINOS P. GIAPIS

TABLE OF CONTENTS

TABLE OF CONTENTS.....	i
I. BACKGROUND AND QUALIFICATIONS.....	1
II. MATERIALS REVIEWED AND CONSIDERED	3
III. MY UNDERSTANDING OF PATENT LAW.....	8
A. Claim Construction	8
B. Obviousness.....	8
IV. OVERVIEW OF THE '169 PATENT	11
A. Background and Prosecution History	11
B. Alleged Invention.....	12
C. Claims	14
V. OVERVIEW OF THE TECHNOLOGY	15
A. Image Sensors	15
B. CCD and CMOS image sensors	16
1. CMOS Image Sensor (CIS)	17
2. Passive Pixel Sensors	18
3. Active Pixel Sensors (APS)	19
4. In-Pixel Processing	20
C. Frontside Illuminated (“FSI”) v. Backside Illuminated (“BSI”) Image Sensors	21
D. BSI CMOS Image Sensors.....	23
E. Conventional Components in a CMOS Image Sensor.....	25
1. Low Fill Factor Photodiodes.....	25

2.	Electrostatic Lens	27
3.	Microlens	28
4.	Anti-reflective Coating	28
5.	Boron Implant for p-type Doping	30
6.	Pinned Photodiodes.....	32
7.	4T Pixel	35
VI.	LEVEL OF ORDINARY SKILL IN THE ART	36
VII.	CLAIM CONSTRUCTION.....	38
VIII.	OVERVIEW OF THE PRIOR ART	38
A.	Lauxtermann	38
B.	Ballin.....	39
C.	Zucca.....	41
D.	Akiyama	44
E.	Wang.....	45
IX.	SPECIFIC GROUNDS FOR PETITION	46
A.	Overview of Grounds for Petition	46
B.	Ground 1: Claims 1-6 And 10-15 Are Obvious In View Of Lauxtermann	48
1.	Claim 1	48
2.	Claim 2	56
3.	Claim 3	58
4.	Claim 4	59
5.	Claim 5	61

6.	Claim 6	62
7.	Claim 10	64
8.	Claim 11	65
9.	Claim 12	66
10.	Claim 13	66
11.	Claim 14	68
12.	Claim 15	68
C.	Ground 2: Claims 2, 6, 7 And 9 Are Obvious Over Lauxtermann In View Of Zucca	72
1.	Reasons to Combine Lauxtermann with Zucca	72
2.	Claim 2	79
3.	Claim 6	80
4.	Claim 7	81
5.	Claim 9	82
D.	Ground 3: Claims 10 And 11 Are Obvious Over Lauxtermann In View Of Akiyama	83
1.	Reasons to Combine Lauxtermann with Akiyama	83
2.	Claim 10	85
3.	Claim 11	88
E.	Ground 4: Claims 16-20 Are Obvious Over Lauxtermann In View Of Wang	89
1.	Reasons to Combine Lauxtermann with Wang	89
2.	Claim 16	92
3.	Claim 17	95

4.	Claim 18	96
5.	Claim 19	97
6.	Claim 20	99
F.	Ground 5: Claims 1, 3-8, And 12-15 Are Obvious In View Of Ballin	99
1.	Claim 1	100
2.	Claim 3	106
3.	Claim 4	107
4.	Claim 5	108
5.	Claim 6	110
6.	Claim 7	110
7.	Claim 8	110
8.	Claim 12	111
9.	Claim 13	111
10.	Claim 14	112
11.	Claim 15	113
G.	Ground 6: Claims 10 And 11 Are Obvious Over Ballin In View Of Akiyama	114
1.	Reasons to Combine Ballin with Akiyama	114
2.	Claim 10	116
3.	Claim 11	117
X.	CONCLUSION	118

I, Dr. Konstantinos P. Giapis, declare as follows:

1. I have been retained as an expert witness on behalf of Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) for the above captioned Petition for *Inter Partes* Review (“IPR”) of U.S. Patent No. 9,356,169 (“the ’169 patent”) (Ex. 1001).

2. I am being compensated for my time in connection with this IPR at my standard consulting rate of \$700 per hour. My compensation is not affected by the outcome of this matter.

3. I have been asked to provide my opinions regarding whether claims 1-20 of the ’169 patent (the “Challenged Claims”) are invalid as being obvious over the prior art to a person having ordinary skill in the art at the time of the alleged invention.

4. I am not currently, and have not at any time in the past been, an employee of TSMC. I have no financial interest in TSMC.

I. BACKGROUND AND QUALIFICATIONS

5. I am a professor of chemical engineering at the California Institute of Technology (“Caltech”). I have held that position since 1992.

6. My research relates to processing of semiconductors, dielectrics, and metals, as performed in the fabrication of semiconductor devices, including microprocessors and digital memories. In particular, my work has focused upon

patterning layers of electronic materials to fabricate sub-micron features such as transistor gates, vias, and metal lines found in VLSI circuits. I have studied extensively plasma-surface interactions of relevance to depositing and etching semiconductor layers. I have also conducted modeling and simulations of the evolution of poly-silicon and metal gate profiles subjected to plasma etching and studied their charging interactions with plasmas. Since the start of my graduate career in 1985, I have accumulated over 35 years of experience on semiconductor materials, devices, and their processing.

7. In my professorial duties at Caltech, I have developed and taught new undergraduate and graduate level courses on semiconductor device physics and their processing. These innovative courses combined solid state physics and electronic materials processing technologies with the more traditional chemical engineering subjects of transport phenomena and chemical thermodynamics. The courses have prepared several generations of students for successful careers in the semiconductor industry.

8. During my research career, I have authored or co-authored 98 peer-reviewed papers, 12 refereed conferences proceedings, two book chapters. Most of my publications relate to semiconductor device processing. My papers on charging damage of high-density integrated devices such as microprocessors, and digital memories are highly cited. I have also been granted 13 patents.

9. My curriculum vitae is provided as Exhibit 1105.

II. MATERIALS REVIEWED AND CONSIDERED

10. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art, and have considered the viewpoint of a person having ordinary skill in the art (POSITA) at the time of the alleged invention.

11. In forming my opinions, I have reviewed and considered the following documents:

Exhibit No.	Description
1001	U.S. Patent No. 9,356,169 (“the ’169 Patent”)
1002	Prosecution File History for the ’169 Patent
1003	Intentionally omitted
1004	U.S. Patent No. 7,498,650 (“Lauxtermann”)
1005	S. Zucca et al, <i>Monolithic Pixel Sensors for Fast Particle Trackers in a Quadruple Well CMOS Technology</i> , 2012 IEEE Nuclear Science Symposium and Medical Imaging Conference Record (“Zucca”)
1006	U.S. Patent No. 8,076,172 (“Akiyama”)
1007	J. Ballin et al, <i>Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixels</i> , Sensors 2008 (“Ballin”)
1008	U.S. Patent No. 8,723,284 (“Hynecek”)
1009	U.S. Patent App. Pub. No. 2010/0159632 (“Rhodes”)

Exhibit No.	Description
1010	U.S. Patent No. 8,531,565 (“Wang”)
1011	U.S. Patent No. 7,944,012 (“Turchetta”)
1012	Coath et al, <i>Advanced Pixel Architectures for Scientific Image Sensors</i> , Proceedings of the 2009 Topical Workshop on Electronics for Particle Physics (“Coath I”)
1013	Coath et al, <i>A Low Noise Pixel Architecture for Scientific CMOS Monolithic Active Pixel Sensors</i> , 2009 IEEE Nuclear Science Symposium Conference Record (“Coath II”)
1014	U.S. Patent No. 7,710,477 (“Nam”)
1015	Battiato et al, <i>Image Processing for Embedded Devices</i> , 2010 (“Battiato”)
1016	Heddle, <i>Electrostatic Lens Systems</i> , 2nd ed, 2000 (“Heddle”)
1017	U.S. Patent No. 8,921,803 (“Welkie”)
1018	U.S. Patent No. 6,770,889 (“Iwasawa”)
1019	U.S. Patent Appl. Pub. No. 2011/0101201 (“Venezia”)
1020	U.S. Patent No. 7,505,206 (“Deng”)
1021	U.S. Patent App. Pub. No. 2013/0270663 (“Lin”)
1022	International Patent App. Pub. No. WO 2007/025102 (“Li”)
1023	U.S. Patent App. Pub. No. 2012/0038014 (“Tai”)
1024	Sze & Lee, <i>Semiconductor Devices: Physics and Technology</i> , 3rd ed, 2012 (“Sze&Lee”)
1025	Sze & Ng, <i>Physics of Semiconductor Devices</i> , 3rd ed, 2006 (“Sze&Ng”)
1026	U.S. Patent No. 8,736,006 (“Tsai”)

Exhibit No.	Description
1027	U.S. Patent Appl. Pub. No. 2013/0203208 (“Shinohara”)
1028	E. R. Fossum and D. B. Hondongwa, “A review of the pinned photodiode for CCD and CMOS image sensors,” <i>IEEE J. Electron Devices Soc.</i> , vol. 2, no. 3, pp. 33-43, May 2014; available at https://ieeexplore.ieee.org/document/6742594 (“Fossum I”)
1029	U.S. Patent No. 5,903,021 (“Lee”)
1030	https://en.wikipedia.org/wiki/Back-illuminated_sensor
1031	U.S. Patent No. 6,168,965 (“Malinovich”)
1032	E.R. Fossum, “Active Pixel Sensors: Are CCD's Dinosaurs?,” Proc. SPIE 1900, Charge-Coupled Devices and Solid State Optical Sensors III, (July, 1993) (“Fossum II”)
1033	Y. Kohyama et al., “A 1.4 μm Pixel Backside Illuminated CMOS Image Sensor with 300 mm Wafer Based on 65 nm Logic Technology,” International Image Sensor Workshop (IISW), 2009.
1034	S. Iwabuchi, et al., “A back-illuminated high-sensitivity small-pixel color CMOS image sensor with flexible layout of metal wiring”, Proc. IEEE Int. Solid State Circuits Conf.-Dig. Tech. Papers, pp. 1171-1178, Feb. 2006.
1035	N. Teranishi et al., “Evolution of optical structure in image sensors”, IEDM Tech. Dig., pp. 24, Dec. 2012.
1036	Y. Kitamura et al., “Suppression of crosstalk by using back-side deep trench isolation for 1.12 μm back-side illuminated CMOS image sensor”, 2012 International Electron Devices Meeting, pp. 24.2.1-24.2.4, 2012.
1037	“Digital camera,” <i>Encyclopedia Britannica</i> (https://www.britannica.com/technology/digital-camera)
1038	https://www.tel.com/museum/exhibition/principle/cmos.html

Exhibit No.	Description
1039	Boyd Fowler, X. Liu, P. Vu, “CMOS image sensors – past, present and future”, Proceedings ICIS 2006 – International Congress of Imaging Science (2006) (“Folwer”).
1040	L. J. Kozlowski, et al, “Comparison of passive and active pixel schemes for CMOS visible imagers,” Proc. SPIE 3360, Infrared Readout Electronics IV (September, 1998) (“Kozlowski”)
1041	U.S. Patent No. 8,063,963 (“Dierickx”)
1042	E. R. Fossum “CMOS Image Sensors: Electronic Camera-On-A-Chip,” 44 <i>IEEE Transactions on Electron Devices</i> , no. 10, pp. 1689-98, Oct. 1997
1043	U.S. Patent No. 9,257,479 (“Koizumi”)
1044	Barbe, F., “A Tradeoff Analysis for CCD Area Imagers: Frontside Illuminated Interline Transfer vs. Backside Illuminated Frame Transfer,” in Procs., CCD Applications Conf., pp. 13-20 (1973) (“Barbe”)
1045	L. Brissot et al., “High-definition CCDs for enhanced definition television,” in High-Resolution Sensors and Hybrid Systems, SPIE, vol. 1656, pp. 427-436 (Aug. 12, 1992) (“Brissot”)
1046	https://www.photometrics.com/learn/imaging-topics/quantum-efficiency
1047	U.S. Patent No. 5,244,817 (“Hawkins”)
1048	U.S. Patent No. 5,270,221 (“Garcia”)
1049	U.S. Patent No. 5,494,833 (“Martin”)
1050	U.S. Patent No. 8,709,852 (“Hynecek852”)
1051	U.S. Patent No. 8,409,909 (“Nagaraja”)
1052	U.S. Patent No. 8,963,066 (“Sato”)

Exhibit No.	Description
1053	Declaration of Dr. Sylvia Hall-Ellis
1054	S. Mendis et al., “CMOS Active Pixel Image Sensor”, IEEE Transactions on Electron Devices, vol. 41, No, 3, March 1994.
1055	Stanley Wolf, Silicon Processing for The VLSI Era, Volume 2: Process Integration, 1990.
1056	https://www.dpreview.com/articles/4281372431/sonycmos
1057	U.S. Patent No. 8,198,602
1058	R. Aihara, M. Obata, and H. Sawaragi, “Stabilization of An Electrostatic Lens for A Focused Ion Beam System,” Journal of Vacuum Science & Technology B: Microelectronics Processing and Phenomena 6, 958 (1988).
1059	T. Joy, et al., “Development of a Production-Ready, Back-Illuminated CMOS Image Sensor with Small Pixels,” IEDM, pp. 1008-1010, 2007.
1101	Intentionally omitted
1102	J. Ballin <i>et al.</i> , “Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixels.” <i>Sensors</i> , vol. 8, no. 9, 2008: 5336-5351
1103	Intentionally omitted
1104	S. Zucca <i>et al.</i> , “Monolithic Pixel Sensors for Fast Particle Trackers in a Quadruple Well CMOS Technology.” <i>2012 IEEE Nuclear Science Symposium and Medical Imaging Conference Record (NSS/MIC)</i> , pp. 1742-1749, 2012.

III. MY UNDERSTANDING OF PATENT LAW

12. I am not an attorney. For purposes of this declaration, I have been informed by counsel about certain aspects of the law that are relevant to my opinions. My understanding of the law is as listed below.

A. Claim Construction

13. I understand that in an IPR petition filed after November 13, 2018, a claim must be construed under the *Phillips* standard, which was set out by the Federal Circuit in the case named *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). Under that standard, words of a claim are given their plain and ordinary meaning as understood by a POSITA at the time of invention, in light of the specification and prosecution history, unless those sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent.

B. Obviousness

14. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed.

15. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

16. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- whether a POSITA could implement a predictable variation, and would see the benefit of doing so;

- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

17. I understand that a POSITA has ordinary creativity, and is not an automaton.

18. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

19. I understand that prior art to the '169 patent includes patents and printed publications in the relevant art that predate the Priority Date of the '169 patent.

20. I understand that certain factors—often called “secondary considerations”—may support or rebut an assertion of obviousness of a claim. I

understand that such secondary considerations include, among other things, commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I further understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

IV. OVERVIEW OF THE '169 PATENT

A. Background and Prosecution History

21. The '169 Patent is entitled “Apparatus, system and method of back side illumination (BSI) complementary metal-oxide-semiconductor (CMOS) pixel array.” The named inventors are Assaf Lahav and Amos Fenigstein. The named assignee of the '169 patent is Alidouble Inc (“Alidouble”).

22. The '169 patent was filed on July 6, 2015, claiming priority to Provisional Application No. 62/021,152 filed on July 6, 2014.

23. My opinion analyzes the invalidity of the '169 patent assuming that the Priority Date of the '169 patent is July 6, 2014.

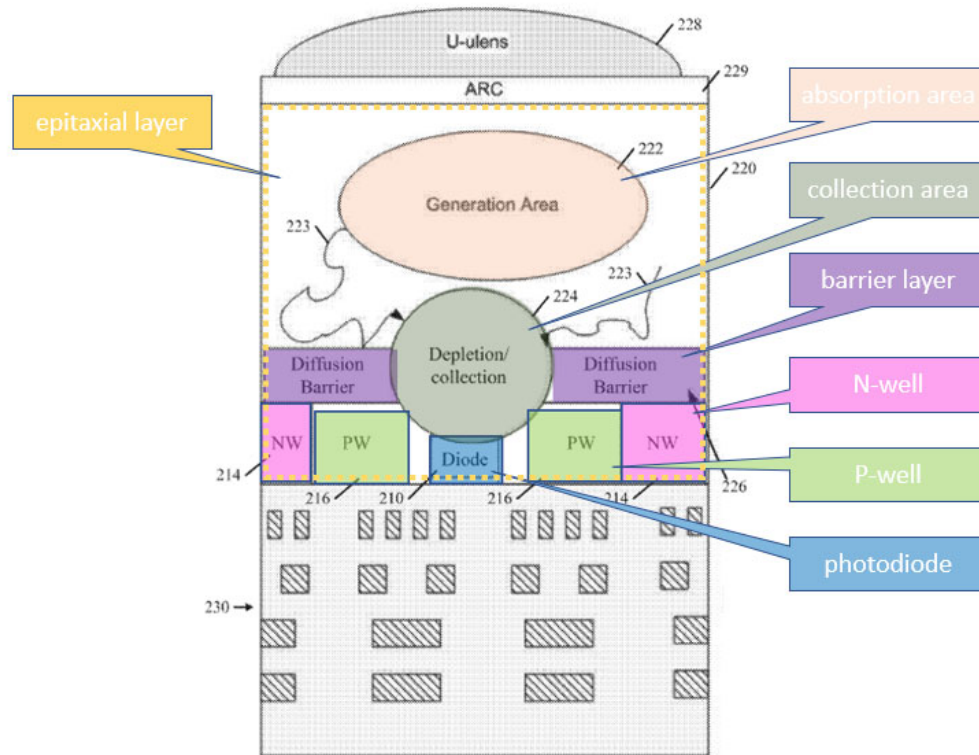
B. Alleged Invention

24. The '169 patent is directed to “Back-Side Illumination (BSI)” complementary metal-oxide-semiconductor (CMOS) pixel array. Ex. 1001, 1:16-19. The '169 patent discloses a CMOS pixel that includes a photodiode and in-pixel processing transistors. *Id.*, 3:30-33, 4:9-40. The pixel would have poor collection efficiency if some of the photogenerated electrons are absorbed not by the photodiode but by well regions (specifically, the n-well regions) of the transistors, which act as parasitic photodiodes. *Id.*, 4:41-61. Addressing this problem, the '169 patent places a barrier layer below the transistor well regions to prevent the photogenerated electrons from diffusing to the transistor well regions. *Id.*, 5:57-60, 6:57-60. However, as described in Section II.A.5, the use of a barrier layer below transistor well regions was already known by the priority date of the '169 patent.

25. The '169 patent discloses a BSI CMOS image sensor with a plurality of pixels (see FIG. 1) and, as shown in FIG. 2 below¹, each pixel includes: one or more MOS transistors with one or more well regions (N-well 214 and/or P-well 216), (2) a photodiode 210, (3) an epitaxial layer 220 with an absorption area 222 and a collection area 224, the latter of which connects absorption area 222 to photodiode 210, and (4) a barrier layer 226 separating absorption area 222 from the

¹ Coloration and annotations are added to figures unless otherwise noted.

one or more well regions to prevent diffusion of electrons to the one or more well regions. Ex. 1001, Abstract, FIGs. 1 and 2.



Ex. 1001, Fig. 2 (annotated).

26. The '169 patent explains that in some embodiments the photodiode (PD) “may include, and/or may perform the functionality of a low fill factor diode” because “a [low fill factor] PD occup[ies] a small part of pixel 104 ... to enable one or more electronic components and/or elements to be introduced inside pixel 104” or “for any other reasons, e.g., physical reasons, design reasons, manufacturing reasons, and or any other reasons.” *Id.*, 3:64-4:8; 8:15-18 (“to enable one or more NW regions 214 and one or more PW regions 216 of one or more MOS transistors to be introduced into BSI CMOS pixel 200”).

27. The photodiode can be fully pinned (*see, e.g., id.*, 3:37-38, 9:7-8), non-pinned (*see, e.g., id.*, 3:39-40, 9:11-13), or any other diode such as a partially pinned diode (*id.*, 3:41-42). FIG. 3B illustrates a pinned photodiode 310 (*id.*, 9:7-8):

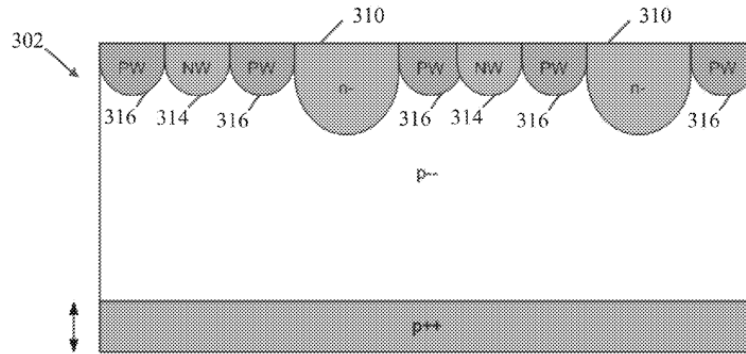


Fig. 3B

Ex. 1001, FIG. 3B.

28. As explained below, a BSI CMOS image sensor with the above structures and components was already known and used in the art.

C. Claims

29. The '169 patent has 20 claims. I understand that claims 1-15 are the Challenged Claims, with claim 1 the only independent claim.

30. For convenience, I have reproduced independent claim 1 below and have annotated it with the element numbering that is used in the claim mapping Section IX below.

- Preamble: “A back-side illumination (BSI) complementary metal-oxide-semiconductor (CMOS) pixel array comprising:”

- Element [1a]: “a plurality of pixels, a pixel of said plurality of pixels comprising:”
- Element [1b]: “one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-Well (NW) region or a P-well (PW) region;”
- Element [1c]: “a photodiode;”
- Element [1d]: “an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and”
- Element [1e]: “a barrier layer separating said absorption area from said one or more well regions.”

V. OVERVIEW OF THE TECHNOLOGY

A. Image Sensors

31. Semiconductor imaging sensors contain photosensitive elements called pixels, which are formed on a silicon substrate. Such sensors operate on the photoelectric effect, a phenomenon that describes the ability of materials to

generate free electrons when they absorb light of a suitable wavelength. When silicon is illuminated, electron-hole pairs are produced. If the electrons are separated from the holes and collected, a signal can be generated that reflects the amount of light absorbed. There are mainly two types of image sensors: charge-coupled devices (“CCD”) image sensors and complementary metal-oxide semiconductor (“CMOS”) image sensors.

32. The photosensitive part of each pixel is typically a photodiode, which permits the separation of carriers generated by the photoelectric effect. Electrons collected by the photodiode must be channeled out of the pixel to be read as signal reflecting the light received by the pixel. This is done by transistors, which are often CMOS based, a technology found extensively in microprocessors and digital memories.

B. CCD and CMOS image sensors

33. CCD and CMOS image sensors are ubiquitous and typically used in devices that output digital recordings of images. One category of such devices is digital cameras. These devices use CCD or CMOS sensors to measure light intensity and color. Ex. 1037 (“At the core of a digital camera is a semiconductor device (CCD) or ... CMOS[], which measures light intensity and colour (using different filters) transmitted through the camera’s lenses. When light strikes the individual light receptors, or pixels, on the semiconductor, an electric current is

induced and is translated into binary digits for storage within another digital medium, such as flash memory”).

1. CMOS Image Sensor (CIS)

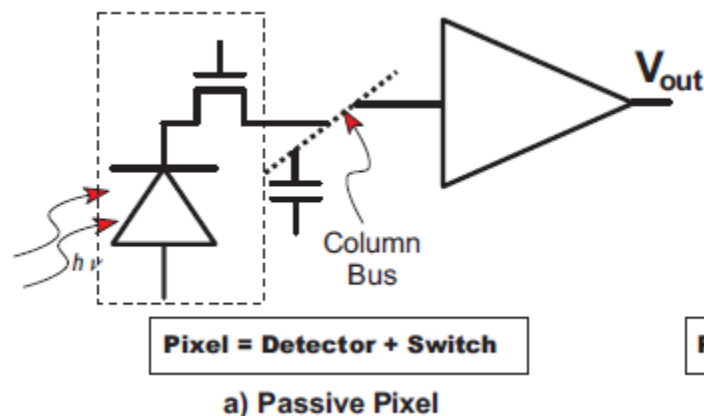
34. CIS was developed in the 1960s around the same time as CCDs but did not become dominant until the 1990s. *See* Ex. 1031 (“CMOS image sensors first appeared in 1967,” but that charge coupled devices (CCDs) “have prevailed since their invention in 1970” due to “their superior dynamic range, low fixed-pattern noise (FPN), and high sensitivity to light.”); *see also* Ex. 1032, 1 (“In the 23 years since their invention in 1970, [CCDs] have evolved to a sophisticated level of performance.”).

35. A CIS is comprised of “a photodiode and a CMOS transistor switch for each pixel, allowing the pixel signals to be amplified individually. By operating the matrix of switches, the pixel signals can be accessed directly and sequentially.” Ex. 1038. While CIS technology offered certain advantages over CCDs, such as “smaller size, faster frame rate, lower power consumption, and lower production cost,” they “required more uniformity and smaller features than silicon wafer foundries could deliver at the time.” Ex. 1035. Thus, CMOS was initially disfavored due to the additional manufacturing requirements not present with CCD sensors. As microlithography techniques advanced, CIS technology

became more mainstream starting in the 1990's . Ex. 1032. Today, CMOS is the standard image sensor in digital cameras included in consumer electronics. *Id.*

2. Passive Pixel Sensors

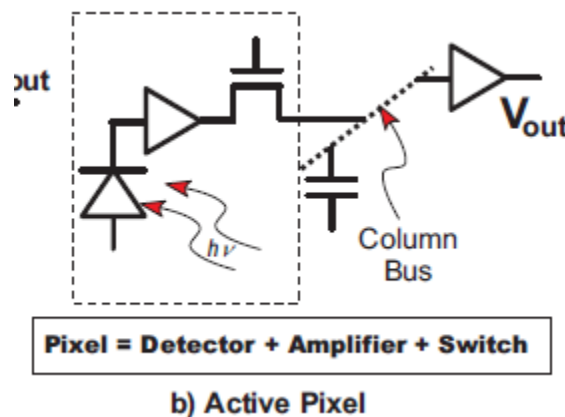
36. The first MOS integrating solid stage image sensor that had a MOS passive pixel architecture came out in 1967. Ex. 1039, 135. This architecture used a reverse biased photodiode to integrate photogenerated charge, connected to a single p-channel MOS transistor to individually access each pixel in a linear array. *Id.* The photodiode is read out by turning on the MOS access transistor and transferring charge from the photodiode to a column amplifier via the column bit line. During this process the photodiode is also reset to fixed voltage determined by the column level amplifier. *Id.* In other words, passive pixels are read out without pixel-based amplification as shown in Kozlowski's Figure 2(a) below. Ex. 1040, 2, FIG. 2(a).



Ex. 1040, FIG. 2(a).

3. Active Pixel Sensors (APS)

37. A year after a MOS passive pixel architecture was developed, a MOS active pixel architecture was proposed in 1968. Ex. 1039, 135. Active pixel sensors incorporate transistors in each pixel to convert the photo-generated charge to a voltage, amplify the signal voltage and reduce noise, as shown in Kozlowski's Figure 2(b) below. Ex. 1040, 3, FIG. 2(b).



Ex. 1040, FIG. 2(b).

38. APSs are less sensitive to noise fluctuations than passive pixels due to their pixel-based amplification Ex. 1041, 1:45-51. In fact, “APS technology preserves all the desirable features of CCDs, yet circumvents the major weaknesses of CCD technology.” Ex. 1032. Compared to CCDs, APS technology allows for a higher fill factor while maintaining the same sensitivity, noise, and dynamic range. *Id.* Further, because each pixel is mechanically collected with metal wires, there is no need to transport the signal through the semiconductor. *Id.*

39. CMOS-based active pixel sensors employ typically four transistors per pixel, which are placed in “wells” within the pixel area. Ex. 1054. The wells are doped regions of the substrate near the surface and come in two flavors: n-type and p-type wells, referred to as n-wells (NW) and p-wells (PW). Ex. 1055, 381-384. These wells occupy real estate within each pixel, thereby reducing the photosensitive part and resulting in a “low fill factor” photodiode. Ex. 1054.

4. In-Pixel Processing

40. In-pixel processing embeds processing capabilities within the individual APS pixels. “If in-pixel processing is required, complex readout circuitry often demands the use of fully complementary MOS transistors (i.e., both PMOS and NMOS).” Ex. 1012, 57. However, adding p-type MOS (PMOS) transistors to APS pixels creates parasitic effects as a result of the formation of parasitic p-n junctions, which reduce the overall amount of charge collected by the photodiode. Ex. 1012 at 57, FIG. 1. To avoid the parasitic p-n junction issue when both PMOS and NMOS transistors are included in the pixel, one solution is to add an additional deep p-well layer underneath the n-wells of the PMOS transistor as a barrier layer to prevent the parasitic n-wells from collecting electric charges. Ex. 1012, 57-58, FIG. 2; Ex. 1013, 1311, FIG. 2; *see also* Ex. 1011, [0032], Fig. 6.

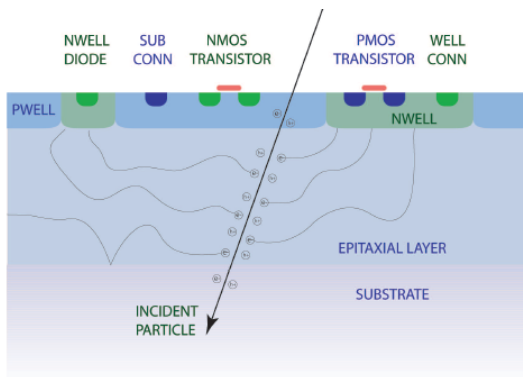


Figure 1: Cross-Section of a Typical CMOS Pixel

Ex. 1012, FIG. 1

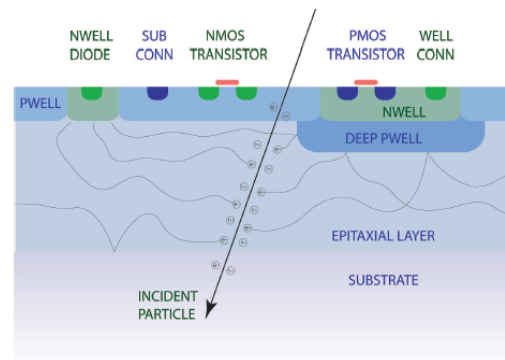
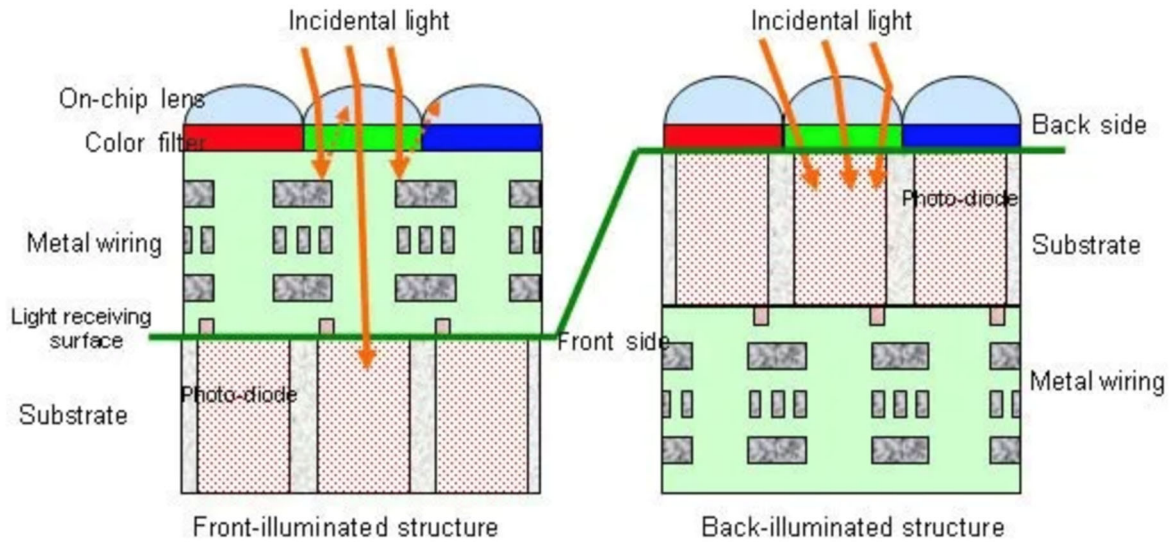


Figure 2: Cross-Section of a Typical CMOS Pixel Showing Addition of INMAPS Deep P-Well Layer

Ex. 1012, FIG. 2

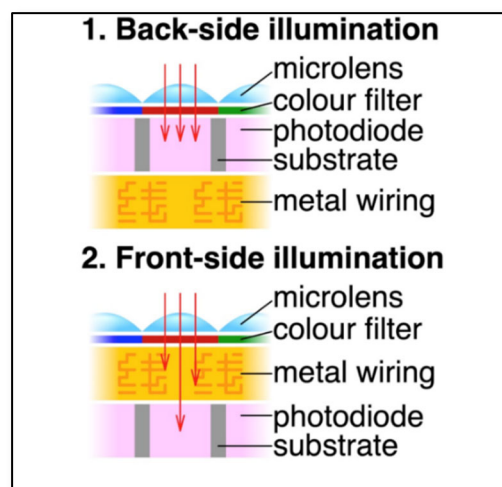
C. Frontside Illuminated (“FSI”) v. Backside Illuminated (“BSI”) Image Sensors

41. There are two fundamental design choices for image sensors: frontside illuminated (FSI) and backside illuminated (BSI). Ex. 1044. The figure below shows an FSI image sensor on the left and a BSI image sensor on the right. Ex. 1056. In an FSI image sensor, the incident light passes through metal wiring and transistors before reaching the photosensitive area, where the metal wiring and transistors reduce the amount of light arriving at the photosensitive areas and therefore reduces the light sensitivity of the image sensor. One way to solve this problem is to rearrange the sensor structure so that the light reaches the photosensitive area from the backside of the metal wiring and transistors so that the incident arrives at the photosensitive area unimpeded. This rearranged design results in a BSI image sensor as shown on the right figure below.



Ex. 1056.

42. As further shown in the image below, the main difference between a BSI image sensor and an FSI image sensor is the arrangement of imaging elements in the sensor with respect to incident light to the pixel. *See Ex. 1030.* BSI image sensors have advantages over FSI image sensors because “metal interconnectors of the image sensors may not cast a shadow on light sensitive areas of the BSI image sensor.” Ex. 1001, 1:38-41.



Ex. 1030.

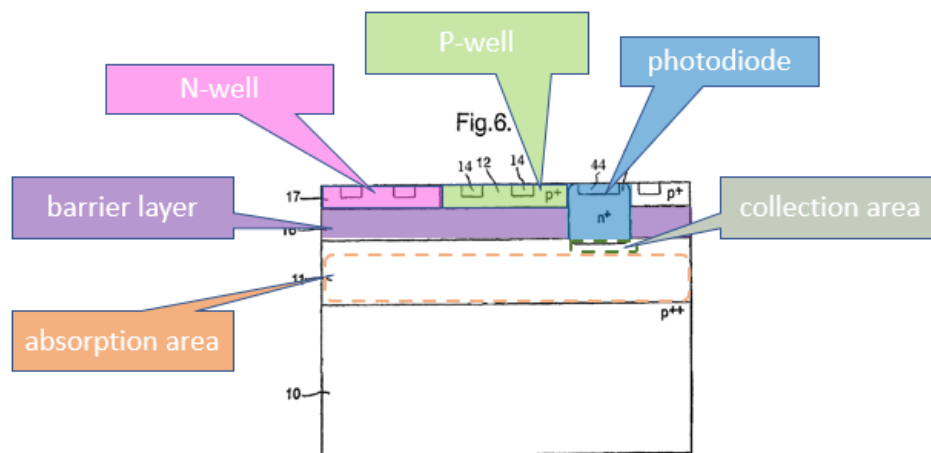
43. One important metric for image sensors is quantum efficiency, i.e., “the measure of the effectiveness of an imaging device to convert incident photons into electrons.” Ex. 1046. BSI, as opposed to FSI, allows the image sensors to achieve high quantum efficiency, which is a “desirable feature[.]” Ex. 1047, 1:10-11; Ex. 1048, 4:7-11 (“[O]ne objective of the present invention is to provide a method for fabricating thinned, back-illuminated, solid state image sensors that have an inherently high quantum efficiency over a broad spectral range.”); *see also* Ex. 1049, 2:26-30 (disclosing an “improved Metal Semiconductor Metal (MSM) photodiode device” where “frontside electrodes and backside illumination [is employed] to avoid active area shadowing in the device.”).

D. BSI CMOS Image Sensors

44. The '169 patent is directed to BSI CMOS pixel array. Ex. 1001, 1:16-19. The '169 patent concedes that BSI CMOS pixel arrays are commonly found in image sensors used in imaging devices such as a camera to capture images, photos, and/or videos. Ex. 1001, 1:23-25. In fact, the BSI CMOS image sensor structure disclosed in the '169 patent, as discussed in Section IV, was also well-known in the prior art before the priority date of the '169 patent.

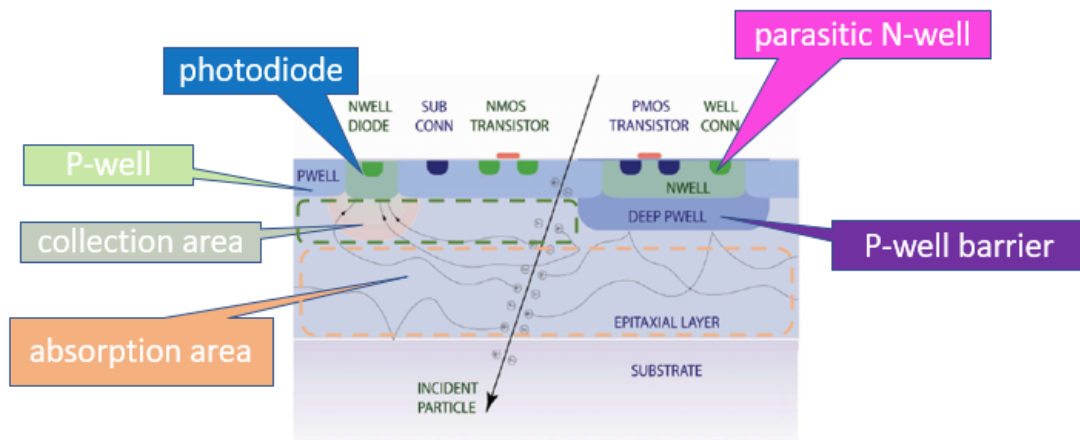
45. For example, like the '169 patent, Turchetta's FIG. 6 shows a BSI CMOS sensor where each pixel includes: (1) one or more MOS transistors with

one or more well regions (**n-well** and/or **p-well**), (2) a **photodiode**, (3) an epitaxial layer with an **absorption area** and a **collection area**, the latter of which connects the absorption area to the photodiode, and (4) a **barrier layer** separating the absorption area from the well regions to prevent diffusion of electrons to the well region. Ex. 1011, 4:28-43, FIG. 6.



Ex. 1011, FIG. 6 (annotated).

46. Similarly, like the '169 patent, Coath I and Coath II's FIG. 2 shows a BSI CMOS image sensor where each pixel includes: (1) one or more MOS transistors with one or more well regions (n-well and p-well), (2) a photodiode, (3) an epitaxial layer with an absorption area and a collection area, the latter of which connects the absorption area to the photodiode, and (4) a barrier layer separating the absorption area from the well regions to prevent diffusion of electrons to the well region. Ex. 1012, FIG. 2; Ex. 1013, FIG. 2.



Ex. 1013, FIG. 2 (annotated, colors in original).

E. Conventional Components in a CMOS Image Sensor

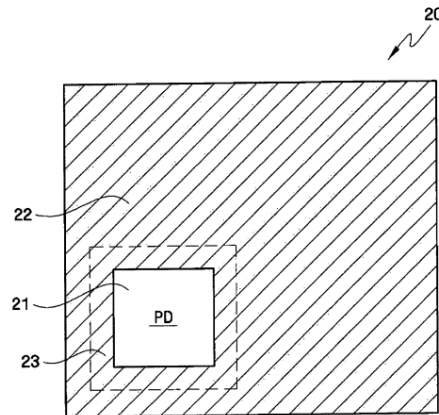
47. BSI CMOS image sensors generally include conventional components and features found in CIS image sensors, such as pinned photodiodes (e.g., with a low fill factor), p-doped regions with boron implant, anti-reflective coating (ARC), microlenses, and electrostatic lenses.

1. Low Fill Factor Photodiodes

48. The use of low fill factor photodiodes was well-known before the priority date of the '169 patent. For example, Nam discloses that “the pixel ‘fill factor’ ... refers to the ratio of the area of the light receiving region (or photosensitive region) of the pixel to the total area of the pixel.” Ex. 1014, 2:41-44. Further, “CMOS active pixel sensors have low ‘fill factors’ due to the incorporation of the active circuits and associated interconnects in the unit pixels surrounding the designed photosensitive regions,” as further illustrated in Nam’s

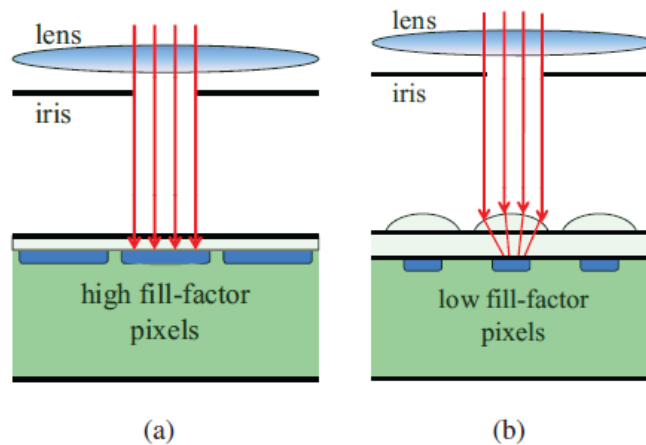
FIG. 2. *Id.*, 2:44-50. In other words, the use of a low fill factor photodiodes allows other circuit components (such as MOS transistors with one or more N well and P well regions) to be integrated within the pixel.

FIG. 2



Ex. 1014, FIG. 2.

49. Similarly, Battiatto provides a definition of “fill factor” consistent with that of Nam and discloses that the fill factor of a photodiode/pixel “may vary from 30% to 100%.” Ex. 1015, 11. Low and high fill-factor pixels/photodiodes are comparatively illustrated in Battiatto’s FIG. 2.3 below:



Ex. 1015, FIG. 2.3 (colors and annotations in original).

2. Electrostatic Lens

50. The functionality and use of electrostatic lens were well-known before the priority date of the '169 patent. *See, e.g.*, Ex. 1016 (Heddle, “Electrostatic Lens Systems”). As disclosed in Welkie, an electrostatic lens functions to assist the transport of electric charges, e.g., by “focus[ing] or otherwise re-direct[ing] the trajectories of ions with electrostatic fields.” Ex. 1017, 2:27-29; *see also* Ex. 1018 (Iwasawa), 2:11-18 (“controlling an electrostatic lens, . . . which converges/diverges a charged particle beam such as an ion beam, electron beam, etc.”).

51. Venizia similarly discloses an electron lens (i.e., electrostatic lens) operable to focus the electrons in the semiconductor material towards the photosensitive region. Ex. 1019, [0026]. Venizia further discloses that its electron lens may simply be “a more heavily doped region (e.g., a p⁺ doped region) of a less heavily doped (e.g., a p- type) semiconductor material 108” or “a thin metal layer formed over material 108 in which the metal layer is operable to create a hole accumulation region in an adjacent portion of the material 108 (e.g., a metal flash gate).” *Id.*, [0027].

3. Microlens

52. As Deng discloses, before the priority date of the '169 patent, “[m]icrolens arrays are widely employed in image sensor technology, such as charged coupling device (CCD) image sensors and complimentary metal-oxide-semiconductor (CMOS) image sensors.” Ex. 1020, 1:6-11. “Microlens arrays are often formed by patterning a polymer layer formed over a color filter or array, a dielectric layer, and/or other substrate features.” *Id.*, 1: 11-13. “Each microlens is aligned over a corresponding photo-sensor formed in the underlying substrate,” and “light that is incident on each microlens is focused towards a corresponding photo-sensor,” thereby improving the efficiency of the image sensor. *Id.*, 1:17-20.

53. Battiato, discussed above, also teaches that when the fill factor of a photodiode/pixel is low, microlenses can be used to focus lights on the photodiode, thereby “boost[ing the] effective fill factor (i.e., the ratio of the active refracting area to the total area occupied by the lens array)” of the photodiode, and improving sensitivity of the pixel. Ex. 1015, 11.

4. Anti-reflective Coating

54. The functionality and the use of anti-reflective coating (ARC) were well-known and widely used in image sensors, including BSI CMOS image sensors, before the priority date of the '169 patent. ARC “allows light to pass through from a lens to the photodiode while minimizing reflection that would

decrease the efficiency of the device.” Ex. 1021 (Lin), [0013]. “The anti-reflective film also can be light absorbing to provide further reductions in light reflection and consequent crosstalk.” Ex. 1022 (Li), Abstract.

55. Tai discloses that “[t]ypically, a BSI CMOS image sensor pixel includes one or several antireflective (‘AR’) coatings.” Ex. 1023, [0042]. Similarly, Lin discloses an anti-reflective layer for BSI CMOS sensors, where “[t]he anti-reflection film 270 includes one or more composite layers of thin metal oxides stacked over the photodiode over the back surface of the substrate.” Ex. 1021, [0026]. As shown in Lin’s FIG. 2 below, a color filter 290 and a lens 295 are also stacked on top of the anti-reflection film 270. *Id.*, [0025], FIG. 2.

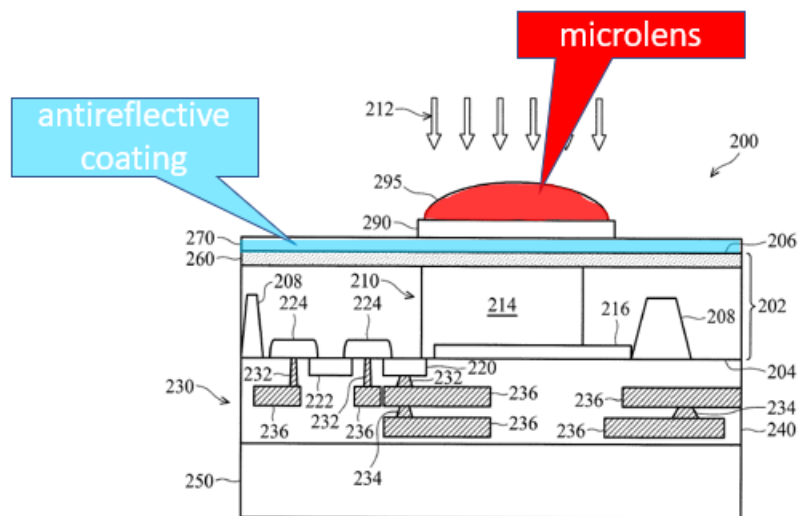


FIG. 2

Ex. 1021, FIG. 2 (annotated).

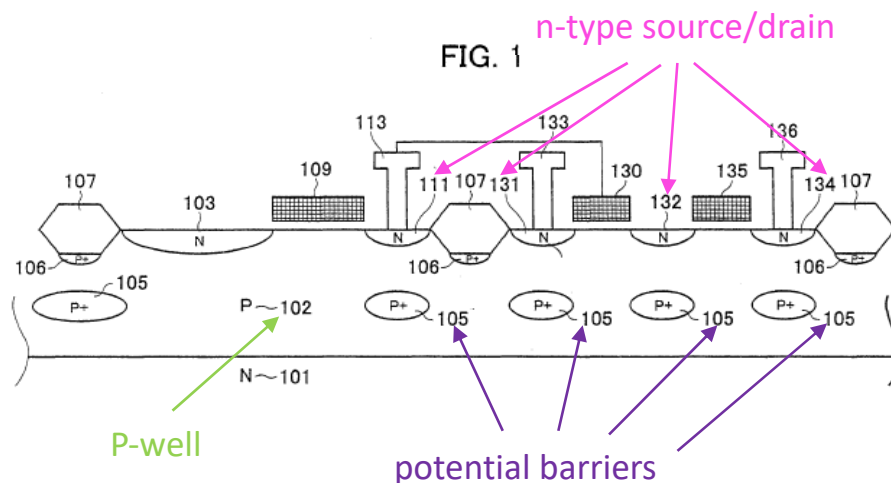
5. Boron Implant for p-type Doping

56. Using boron implant for p-type doping in silicon semiconductors was well-known in the art before the priority date of the '169 patent. For example, according to Sze&Lee, impurity doping was routinely used to change the electrical properties of the semiconductors. Ex. 1024, 466. "Diffusion and ion implantation are the two key methods of impurity doping." *Id.* There are two types of impurity doping: (1) n-type doping, where atoms with one or more valence band electron than Silicon (negative charge carriers) are added to the substrate, and (2) p-type doping, where atoms with one less valence band electron than Silicon (positive charge carriers) are added to the substrate. *See id.*, 34.

57. Sze&Lee further discloses that "boron is the most popular dopant for introducing a p-type impurity [dopant], whereas arsenic and phosphorus are used extensively as n-type dopants," partly because "[t]hese three elements are highly soluble in silicon." *Id.*, 467; *see also* Ex. 1025 (Sze&Ng), 31 (using "n-type phosphorus and p-type boron" as examples); Ex. 1026 (Tsai), 4:24-30 (Pixels of a BSI CMOS image sensor may be formed by a diffusion or implantation process, which "may include doping the device substrate [] with a p-type dopant such as boron or an n-type dopant such as phosphorous or arsenic.").

58. As an example, Shinohara discloses a solid-state image sensor (CCD or CMOS) with a potential barrier formed by boron implantation. Ex. 1027, FIG. 1.

Specifically, Shinohara's FIG. 1 shows an image sensor with an n-type substrate 101, a transfer transistor (which has a gate electrode 109, a source region 103, and a drain region 111), where the n-type source region 103 is formed in a p-well 102, and a p+ channel stopper 106 formed under insulating films 107. *Id.*, FIG. 1, [0054]. Further, p+ type potential barriers 105 are implanted underneath the n-type source/drain regions 111, 131, 132, 134 to prevent electric charges from being absorbed by these regions, thereby improving the sensitivity sensor because the charges are instead directed to the photodiode. *Id.*, [0061]-[0062]. Shinohara further discloses that its p+ type "potential barriers 105 are provided by **implanting . . . boron or gallium into the p-well 102** using ion implantation." *Id.*, [0059], [0106], [0107].



Ex. 1027, FIG. 1 (annotated).

6. Pinned Photodiodes

59. Using fully-pinned photodiodes in BSI CMOS image sensors was well-known in the art before the priority date of the '169 patent. A standard CMOS APS pixel contains a photodetector called a pinned photodiode ("PPD"). Ex. 1028, 35. PPDs were first used in BSI CMOS image sensors in the late 1990s, and "[m]ass-production of BSI PPD CMOS image sensors [was] routine" in 2014. *Id.*, 35-36. As Fossum recognizes, "[t]he 'pinned photodiode' is . . . used in almost all charge-coupled device (CCD) and CMOS image sensors (CIS) due to its low noise, high quantum efficiency and low dark current." Ex. 1028, Abstract.

60. A photodiode may be pinned, partially pinned, or unpinned. A fully-pinned photodiode is often simply referred as a "pinned photodiode" or a "PPD," which is compared to a partially-pinned photodiode often referred as a "PPPD" or an un-pinned photodiode. *See* Ex. 1028 (Fossum), Ex. 1029 (Lee). A photodiode is "pinned" when it incorporates a counter-doped pinning layer above the light sensitive structure within each pixel. *See* Ex. 1028; Ex. 1029. In Fossum, the pinning layer is a p⁺ layer above the n-type storage well (SW). Ex. 1028, FIGs. 4 and 5.

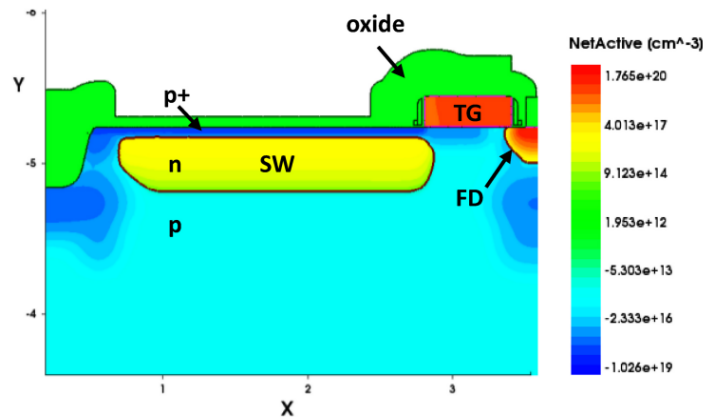


Fig. 4. Example of a pinned photodiode implemented in a CMOS image sensor showing doping concentrations. (Dimensional units are microns).

Ex. 1028, FIG. 4 (colors and annotations in original).

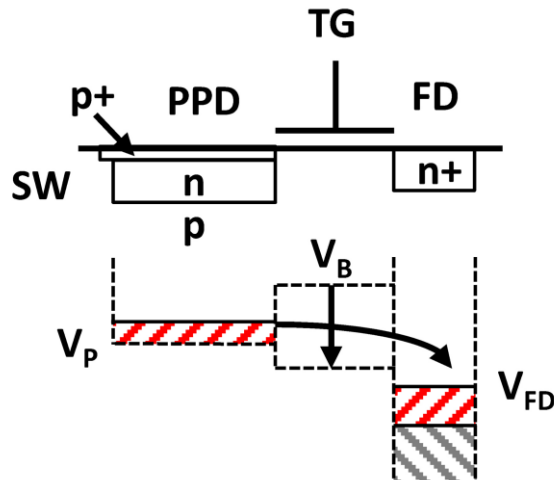


Fig. 5. Ideal potential well diagram for FSI PPD. Turning on transfer gate TG.

Ex. 1028, FIG. 5 (colors and annotations in original).

61. The difference between a pinned and a partially-pinned photodiode lies in whether the pinning layer covers the entire surface of the photodiode. This difference is illustrated in Lee, a prior art patent titled “Partially Pinned Photodiode for Solid State Image sensors.” Ex. 1029. In FIG. 2 (below), the prior art pinned

photodiode (PPD) has a p-type pinning layer 24 spanning the entire PPD 10. Ex. 1029, 3:61-4:5.

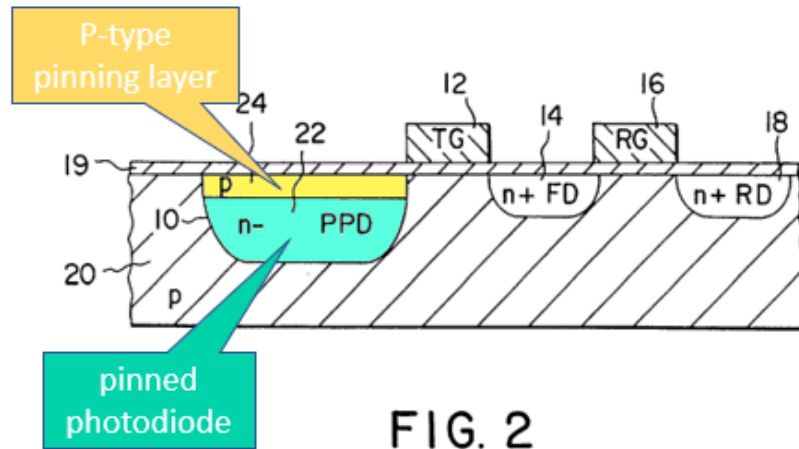


FIG. 2

Ex. 1029, FIG. 2 (annotated).

62. In contrast, in FIG. 4, a partially pinned photodiode (PPPD) has a p-type pinning layer 34 that only covers a portion of the photodiode. Ex. 1029, 4:32-67.

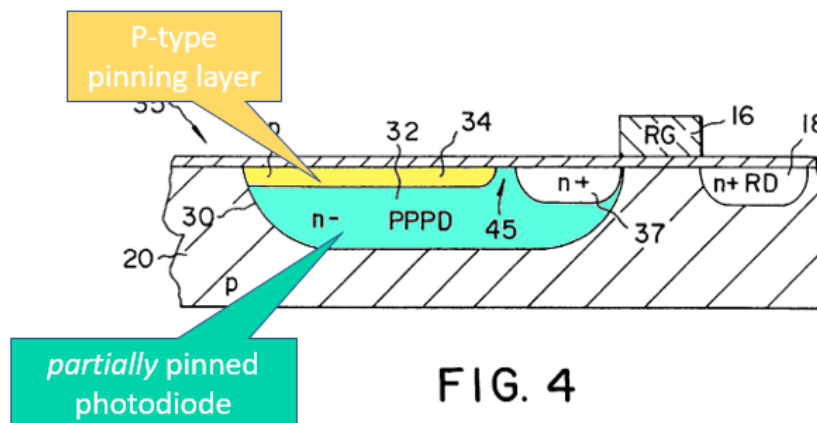


FIG. 4

Ex. 1029, FIG. 4 (annotated).

63. Lee explains that “[a] top view of this pixel 35 is shown in FIG. 4, where it is apparent that *an appreciable portion of the photo-sensitive region is encompassed by pinned region 34, with a relatively small area being allotted to unpinned region 45.*” Ex. 1029, 4:55-59 (emphasis added).

7. 4T Pixel

64. The integration of pinned photodiode with CMOS APS is often referred to as the “4T” pixel because “the PPD is often used in pixels with nominally four (4) transistor gates.” Ex. 1028, 35. In contrast, a “3T” pixel refers to a CMOS APS pixel where the photodiode is directly connected to the SF transistor and the photodiode may be a partially pinned photodiode. *Id.* An exemplary figure illustrating CMOS APS 4T pixel architecture is included below. A CMOS APS 4T pixel architecture typically consists of a pinned photodiode (PPD), a floating diffusion (FD) node, and four transistors: a transfer gate (TG) transistor, a reset (RST) transistor, a source follower (SF) transistor, and a row select (SEL) transistor. *Id.* 35, FIG. 3.

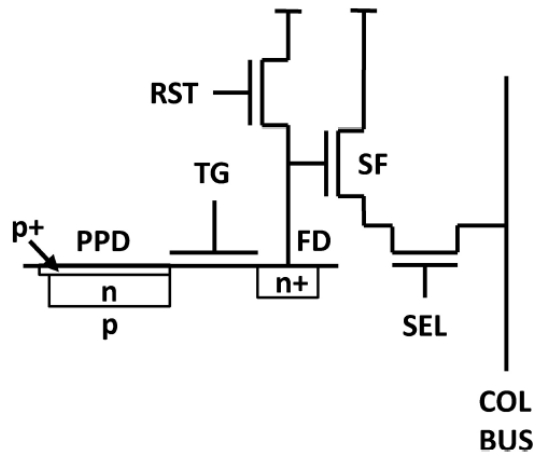


Fig. 3. Schematic of CMOS APS pixel with PPD.

Ex. 1028, FIG. 3.

65. In operation, while the TG transistor is off, charge is collected by the PPD, and when the TG transistor is turned on, the collected charge is transferred from the PPD to the FD node. The SF transistor amplifies the potential of the FD node, which is read out on the column bus (COL BUS) by turning on the SEL transistor. The potential of the FD transistor is reset to zero by turning on the RST transistor while the TG is off. The readout cycle is repeated for every pixel in the pixel array.

VI. LEVEL OF ORDINARY SKILL IN THE ART

66. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the technology, the type of problems encountered in the art, and the prior art solutions to those problems.

67. In determining the characteristics of a hypothetical person of ordinary skill in the art of the '035 Patent at the time of the alleged invention, I considered several things, including the type of problems encountered in this field, and the rapidity with which innovations were made. I also considered the sophistication of the technology involved, and the educational background and experience of those actively working in the field, and the level of education that would be necessary to understand the '169 patent. Finally, I placed myself back in the relevant periods of time, and considered the state of the art and the level of skill of the engineers working in this field in those times.

68. Based on the materials I have considered and my own experiences, it is my opinion that a person of ordinary skill in the art ("POSITA") at the time of the alleged invention would have been a person having a Master's degree in electrical engineering, material science, physics, or other related disciplines with at least three years of industry experience in integrated circuit design, layout, packaging or fabrication. A greater level of experience may compensate for less education and vice versa.

69. I also note that my opinions provided in this Declaration would not change in view of any minor modifications to this level of skill.

VII. CLAIM CONSTRUCTION

70. For purposes of this proceeding, the claim terms do not need to be construed to resolve the prior art issues presented in this Petition. This is because, as detailed in Section IX below, each of the prior art grounds teaches, in relevant part, the exact same combination of features found in the '169 patent.

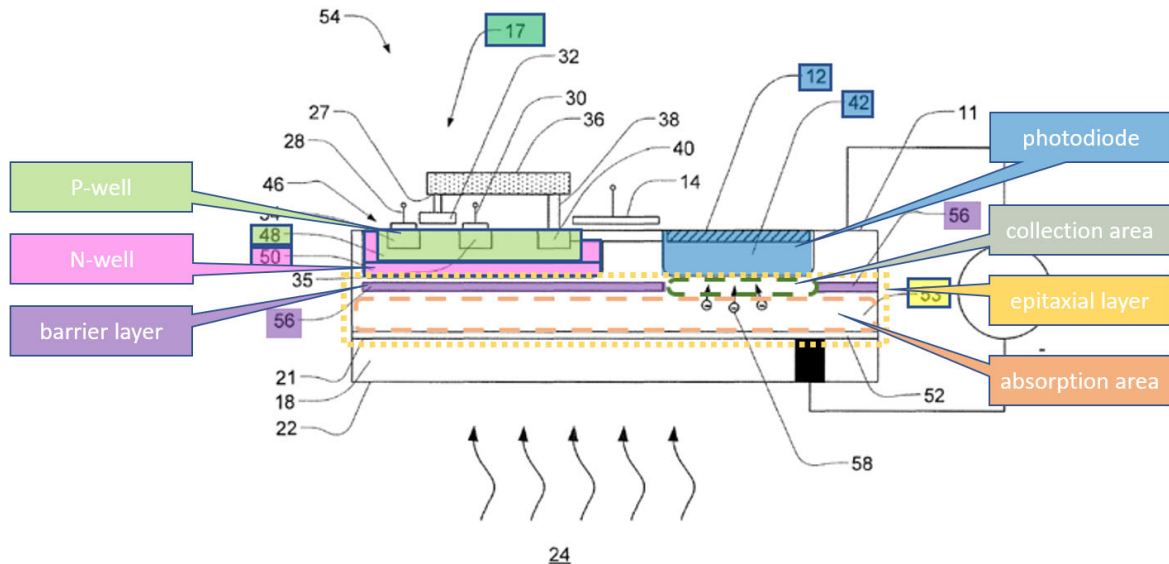
VIII. OVERVIEW OF THE PRIOR ART

A. Lauxtermann

71. Lauxtermann is directed to BSI CMOS image sensors with pinned photodiodes. Ex. 1004, 1:6-9. Lauxtermann discloses one drawback with BSI CMOS image sensor is that the pinned photodiode collects only a small fraction of the photogenerated charges because the charges diffuse not only towards the pinned photodiode but also towards active pixel circuitry within the pixel. *Id.*, 4:56-62.

72. To overcome the above drawbacks, Lauxtermann adds a **p-layer 56** (e.g., a deep p+ implant) under active pixel circuitry 17 (e.g., a source follower transistor) “to drift, rather than diffuse, [charges 58] to the light receiving element of the pinned photodiode 12.” *Id.*, 5: 40-45. Accordingly, Lauxtermann proposed an improved BSI CMOS image sensor that includes: (1) a source follower transistor 17 (MOS transistor) with a **P-well 48** and an **N-well 50**, (2) a **pinned photodiode 12**, (3) an epitaxial layer with an **absorption area** and a **collection area**, the latter of which connects the absorption area to the photodiode, and (4) a

p-layer 56 acting as a **barrier layer** to separate the **absorption area** from the well regions (e.g., **P-well 48** and **N-well 50**) to prevent diffusion of electrons to the well regions and to allow electrons to drift to the **pinned photodiode**. *Id.*, 1:56-2:12 and FIG. 2.



Ex. 1004, FIG. 4 (annotated).

B. Ballin

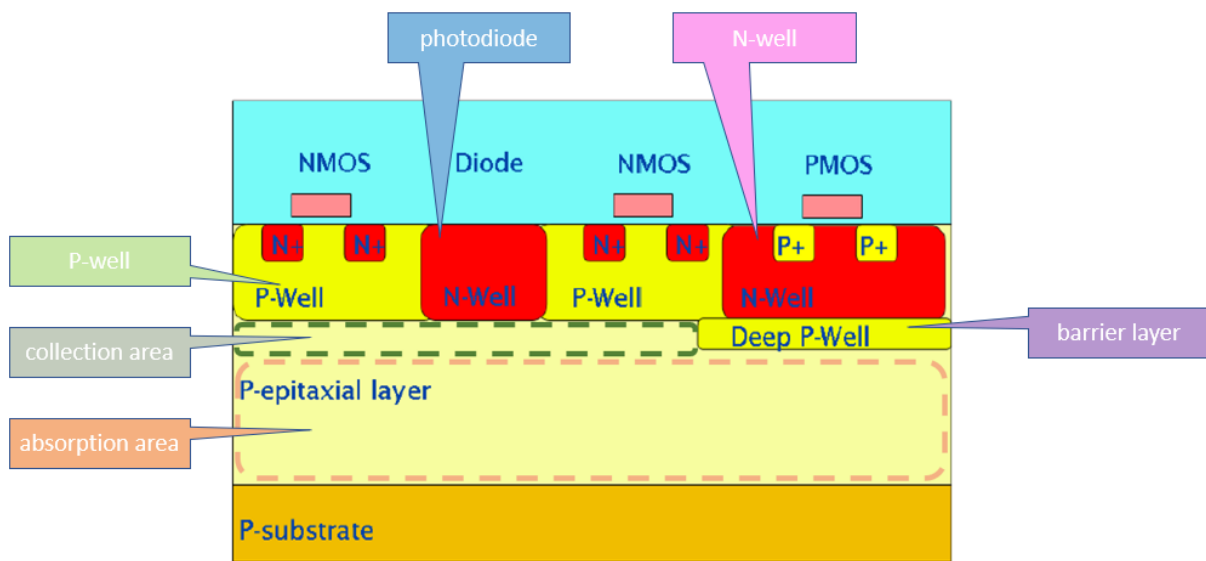
73. As confirmed in the Declaration of Dr. Sylvia Hall-Ellis, Ballin was published and publicly available no later than September 2008. Ex. 1053, ¶¶57-64. As set forth in the declaration of Dr. Hall-Ellis, Ballin was published in a September 2008 edition of the journal *Sensors* available to the public in the National Library of Medicine in Bethesda Maryland. Ex. 1053, ¶¶57. Further supporting the public availability of these proceedings is that a copy of Ballin is

available from the publisher's website, the National Library of Medicine, and the digital repositories *ResearchGate* and *Semantic Scholar*. *Id.*, ¶58.

74. Further, the *Sensors* journal is a well-known journal publication in the industry. I am aware of the *Sensors* journal and that Ballin, along with the other papers published in the journal would have been readily available as of the publication.

75. Ballin is directed to Isolated N-wells MAPS (INMAPS) image sensors, which may be front-illuminated or back-illuminated CMOS image sensors. Ex. 1007, 5336, 5339. Ballin discloses that conventional CMOS sensors includes NMOS transistors implanted in P-wells, PMOS transistor implanted in N-wells, and an N-well photodiode, and charges would be collected by the N-well photodiode as well as the N-wells of the PMOS transistors, which act as parasitic photodiodes. *Id.*, 5339, 5341, FIG. 1. Thus, maximum effective fill factor (which means high quantum efficiency) “is only obtained if the collection [N-well photodiode] junction is only such junction in the pixel.” *Id.*, 5339, FIG. 1. To achieve a high effective factor in the pixel while incorporating PMOS transistors implanted in N-wells in the pixel, Ballin proposes a “novel approach for isolating the N-wells of PMOS transistors ... by adding a deep P implant” underneath the N-wells.

76. As shown in FIG. 2 below, each pixel of Ballin's CMOS image sensor includes: (1) at least two NMOS transistors formed in **P-wells** and one PMOS transistor formed in an **N-well**, (2) an **N-well photodiode**, (3) a P- epitaxial layer with an **absorption area** and a **collection area**, where the collection area connects the absorption area to the photodiode, and (4) a **deep P-well implant** under the PMOS **N-well** acting as a **barrier layer** to isolate the **N-well** of the PMOS transistor from the **absorption area** of the epitaxial layer. Ex. 1007, FIG. 2, 5339-40.



Ex. 1007, FIG. 2 (annotated, colors in original)

C. Zucca

77. As confirmed in the Declaration of Dr. Sylvia Hall-Ellis, Zucca was published and publicly available no later than April 12, 2012. Ex. 1053, ¶¶74-81. As set forth in the declaration of Dr. Hall-Ellis, Zucca was published in the 2012

IEEE Nuclear Science Symposium and Medical Imaging Conference Record

available to the public in the Kurt F. Wendt Engineering Library at the University of Wisconsin – Madison. Ex. 1053, ¶74. This volume was first indexed at a library at Cornell University on April 12, 2012. *Id.*, ¶78.

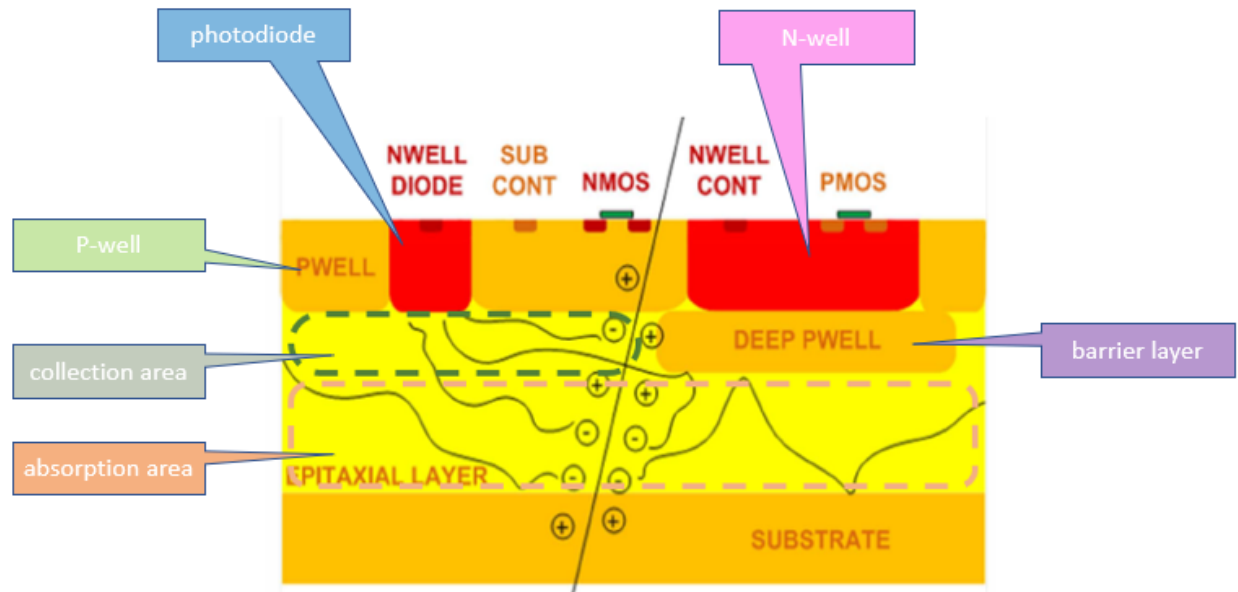
78. Further supporting the public availability of these proceedings is that a copy of the Zucca conference paper is also available in the *IEEE Xplore* database and the digital repositories *ResearchGate*. *Id.*, ¶75.

79. The *IEEE Nuclear Science Symposium and Medical Imaging Conference* and other IEEE publications are well-known in the industry. I was aware of the *IEEE Nuclear Science Symposium and Medical Imaging Conference* and that Zucca, along with the other papers presented at that conference (and published in its proceedings) would have been readily available as of the publication of those proceedings.

80. Zucca is directed to monolithic active pixel sensor (MAPS), which “are also referred to as CMOS APS (active pixel sensor) or as CIS (CMOS image sensors).” Ex. 1005, 1742. Zucca discloses its MAPS image sensor is also a BSI CMOS sensor. *Id.*, 744-45 (“The samples were **illuminated from the back side** in order to avoid reflections from the intricate net of metal interconnections laid out on the top of the chip.”).

81. Zucca discloses that conventional MAPS image sensor architecture includes a PMOS (p-type MOS) transistor formed in an Nwell. *Id.*, 1742. However, the Nwell may degrade the pixel charge collection efficiency because it acts as a parasitic charge collector. *Id.* To overcome this problem, Zucca discloses “a 180 nm CMOS planar technology with quadruple well called INMAPS in which ... a high energy deep Pwell implant is deposited beneath the PMOS competitive Nwells.” *Id.* The deep Pwell implant “represents a barrier for the charge diffusing in the epitaxial layer, preventing the carriers from being collected by the positively biased Nwells hosting the PMOS transistors.” *Id.*

82. As shown in FIG. 1 below, one pixel of Zucca’s image sensor includes “a lightly P-doped epitaxial layer about 10 μm thick” grown on a substrate, a **photodiode**, at least one NMOS transistor located in “heavily doped Pwells” over the epitaxial layer, a PMOS located in an **Nwell**, and a **deep Pwell implant** underneath the Nwell, where the deep Pwell implant acts as a **barrier layer**. *Id.*, 1742-43, FIG. 1. Also as annotated in FIG. 1, Zucca’s epitaxial layer includes a **collection area** by the photodiode and an **absorption area** connected to the collection area.



Ex. 1005, FIG. 1 (annotated, colors in original).

83. Zucca further discloses that its epitaxial layer can have different thicknesses and resistivities. *Id.*, 1743. Zucca provides three additional exemplary topologies for its epitaxial layer: (1) 5 μm thick with standard resistivity, (2) 12 μm thick with standard resistivity, and (3) 12 μm with high resistivity.

D. Akiyama

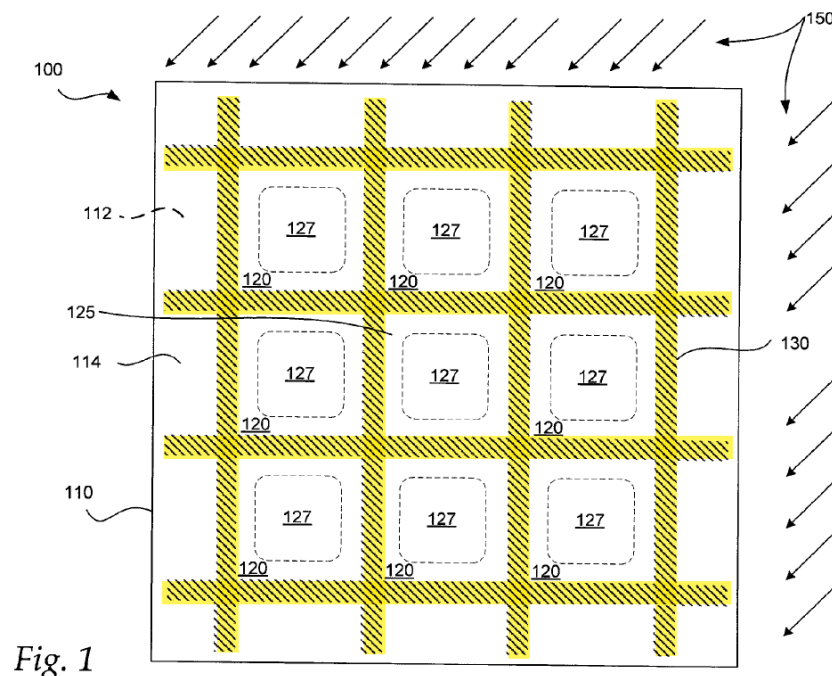
84. Akiyama is directed to solid-state imaging devices, and more specifically, to BSI CMOS solid-state imaging devices. Ex. 1006, 1:9-19.

85. As shown in FIG. 4 below, Akiyama discloses one **pixel 31** of a BSI CMOS image sensor, which includes among other things an **antireflective coating (ARC) 45** and a **microlens 21**. Ex. 1006, FIG. 4; 5:6-30; 5:55-6:3.

1:49-54. Furthermore, photogenerated charges from one pixel may drift into other pixels and associated peripheral circuitry. *Id.*, 2:12-18; 3:23-26; 7:15-18; 8:10-13.

Wang solves the cross-talk problems using a guard ring structure. *Id.*, 2:16-18,

4:3-5. The guard ring structure is shown in Wang's figures, highlighted in yellow:



87. Wang also teaches the guard ring structure isolates the peripheral circuitry from the pixel array. *Id.*, 8:10-13 (“forming a control circuit on the front-side surface of the semiconductor substrate, said control circuit being isolated from the at least one image sensing element by the guard ring structure.”).

IX. SPECIFIC GROUNDS FOR PETITION

A. Overview of Grounds for Petition

88. I am of the opinion that the Challenged Claims of the '169 patent are invalid on the following grounds:

Grounds	Claims	Statutory Basis	Prior Art
1	1-6, 10-15	§103	Lauxtermann
2	2, 6-7, 9	§103	Lauxtermann in view of Zucca
3	10, 11	§103	Lauxtermann in view of Akiyama
4	16-20	§103	Lauxtermann in view of Wang
5	1, 3-8, 12-15	§103	Ballin
6	10, 11	§103	Ballin in view of Akiyama

89. The prior art references relied on in the above Grounds include:

- Lauxtermann (Ex. 1004): U.S. Patent No. 7,498,650, which was filed March 8, 2007, published September 11, 2008, and issued March 3, 2009.
- Zucca (Ex. 1005): Zucca et al, “Monolithic Pixel Sensors for Fast Particle Trackers in a Quadruple Well CMOS Technology”, which was published in the *2012 IEEE Nuclear Science Symposium and Medical Imaging Conference Record*.
- Akiyama (Ex. 1006): U.S. Patent No. 8,076,172, which was filed May 11, 2009, published November 12, 2009, and issued December 13, 2011. Akiyama is prior art under §102(a).
- Ballin (Ex. 1007): Ballin et al, “Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixels”, which was published September 2, 2008 in *Sensors*.

- Wang (Ex. 1010): U.S. Patent No. 8,531,565, which was filed February 23, 2010, published September 2, 2010, and issued September 10, 2013, is prior art under §102(a).

90. None of these references relied upon were before or considered by the Examiner during prosecution of the '169 patent. Further, none of the Grounds above relies on prior art reference combinations that were evaluated during prosecution of the '169 patent.

B. Ground 1: Claims 1-6 And 10-15 Are Obvious In View Of Lauxtermann

91. I am of the opinion that Lauxtermann renders obvious claims 1-6 and 10-15 of the '169 patent.

1. Claim 1

[1pre] A back-side illumination (BSI) complementary metal-oxide-semiconductor (CMOS) pixel array comprising:

92. To the extent the preamble is considered to be a limitation, I am of the opinion that Lauxtermann discloses a BSI CMOS pixel array.

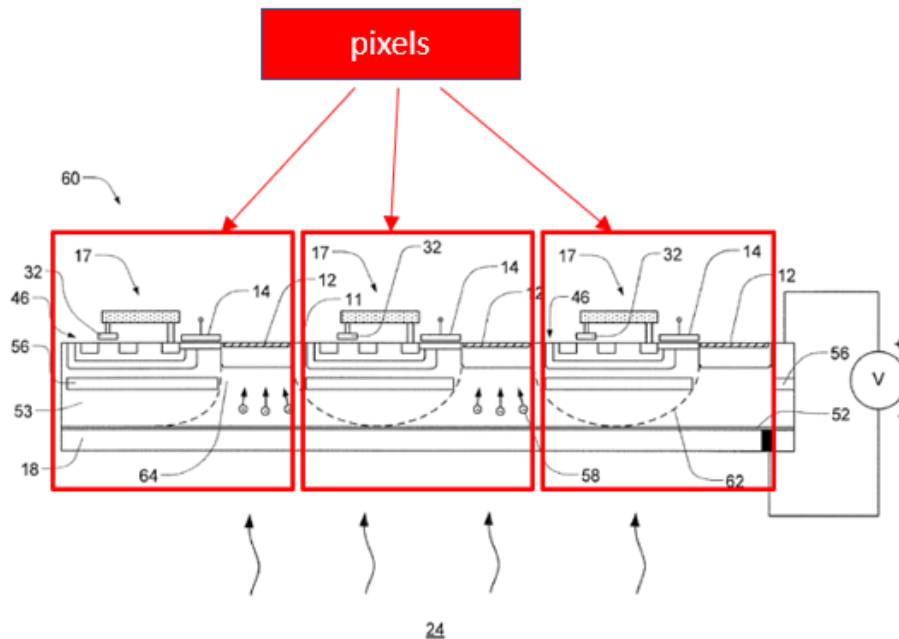
93. Lauxtermann's FIG. 5 illustrates three **BSI CMOS image sensors 60** (i.e., a **pixel array**), and Lauxtermann's FIG. 4 illustrates each CMOS image sensor 54 (i.e., a pixel) includes at least a photodiode 12 and a transistor 17. Ex. 1004, Abstract, 1:6-10; *see also* FIGs. 4 and 5; 5:1-3; 5:50-53. Thus, Lauxtermann discloses the claimed BSI CMOS pixel array.

94. The '169 patent also states that BSI CMOS image sensors was known in prior art. Ex. 1001, 1:31-40 (discussing BSI CMOS image sensors in the “Background” section).

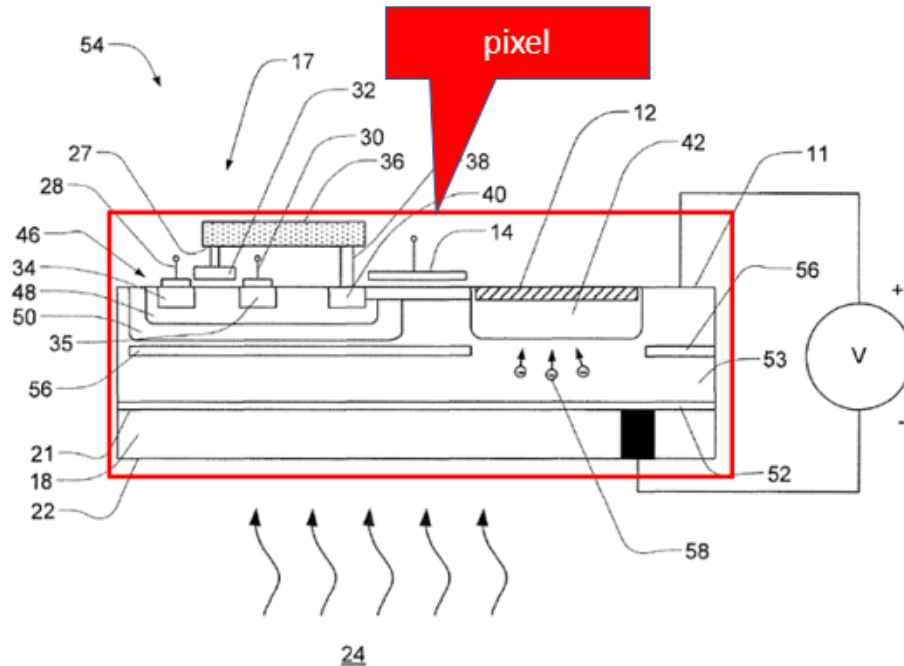
[1a] a plurality of pixels, a pixel of said plurality of pixels comprising:

95. I am of the opinion that Lauxtermann discloses a plurality of pixels.

96. As discussed above for 1[pre], Lauxtermann’s FIG. 5 illustrates three **BSI CMOS image sensors 60** (i.e., **plurality of pixels**), and Lauxtermann’s FIG. 4 illustrates each CMOS image sensor 54 (i.e., **pixel**) includes at least a photodiode 12 and a transistor 17.



Ex. 1004, FIG. 5 (annotated).

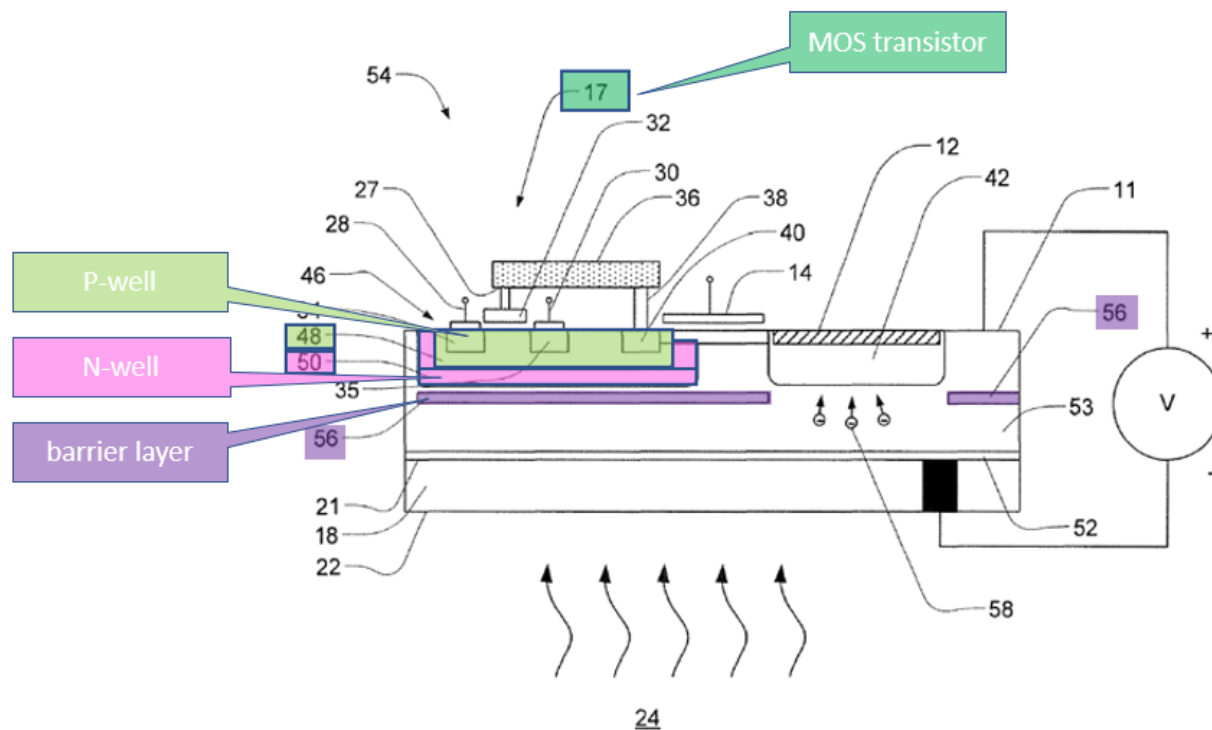


Ex. 1004, FIG. 4 (annotated).

[1b] one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-Well (NW) region or a P-well (PW) region;

97. I am of the opinion that Lauxtermann discloses one or more MOS transistors with N-well or P-well regions.

98. Lauxtermann discloses its BSI CMOS image sensor 54 (i.e., **pixel**) includes a **transistor 17**, which is expressly disclosed to be a **MOS transistor**, more specifically a **NMOS transistor**. See, e.g., Ex. 1004, FIG. 4, 3:47-50, 5:11-13 (“Source follower transistor 17 may be an NMOS device . . .”). As shown in FIG. 4 below, Lauxtermann discloses that its transistor 17 includes a **P-well region 48** and an **N-well region 50**. Ex. 1004, Fig. 4, 5:16-19.



Ex. 1004, FIG. 4.

99. Lauxtermann further discloses that its CMOS image sensor implements “a four transistor (4T) architecture,” which includes at least a transfer gate 14, a reset transistor 15, a transistor 17 (expressly disclosed to be a **MOS transistor**), and a row select transistor 19. *Id.*, 2:51-58. A POSITA would understand that these four transistors in Lauxtermann’s 4T structure are all **MOS transistors** because they are part of a CMOS image sensor made using a CMOS fabrication process.

[1c] a photodiode;

100. I am of the opinion that Lauxtermann discloses a photodiode.

[1d] an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and
--

102. I am of the opinion that Lauxtermann renders obvious claim 1d's requirement of "an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode."

103. *An epitaxial layer:* Lauxtermann discloses that its BSI CMOS image sensor 54 (i.e., pixel) includes a **semiconductor layer 53**, and the **photodiode** is fabricated on semiconductor layer 53. Ex. 1004, FIG. 4.

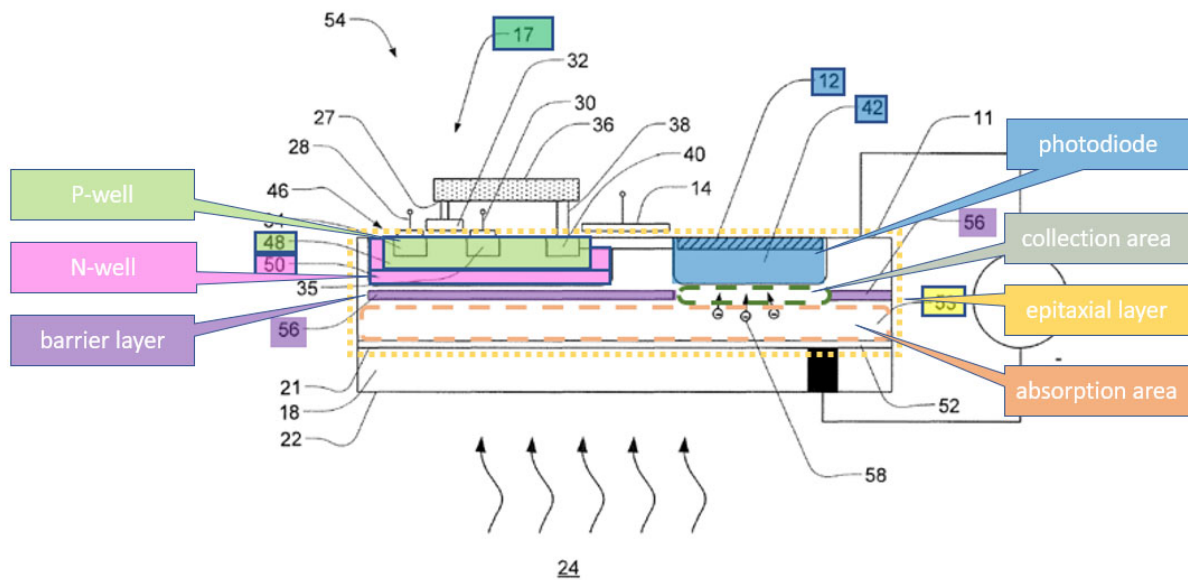
104. Lauxtermann's semiconductor layer 53 is an **epitaxial layer** because it is formed by deposition on a single-crystalline Silicon substrate. While other solid phases of Silicon can be grown by deposition, the CMOS devices of the image sensor perform best on epitaxial Silicon. Ex. 1055, 385-387. Lauxtermann teaches semiconductor layer 53 is deposited just like semiconductor layer 16. Ex. 1004, 5:29-31 ("prior to the deposition of semiconductor layer 53"). A POSITA would have understood that semiconductor layer 53 must be Silicon deposited epitaxially on the substrate, and thus an epitaxial layer. Moreover, in describing

another embodiment, Lauxtermann expressly teaches that the “semiconductor layer” is “an **epitaxial layer**.” Ex. 1004, FIG. 1, 3:4-8 (semiconductor layer 16 is “an **epitaxial layer** with a p-doped region”). A POSITA would therefore understand that Lauxtermann’s semiconductor layer 53 is an epitaxial layer.

105. *Comprising an absorption area and a collection area:* Within that **epitaxial layer**, layer 53 includes a **collection area** and an **absorption area**,² the former of which connects the absorption area to the **photodiode**. The absorption area is configured **to absorb incoming photons** (from light 24) and **generate charges 58** (i.e., electrons) **by means of the photoelectric effect**. Ex. 1004, 2:59-6; 5:45-49. Just like the absorption area 222 in Figure 2 of the ’169 patent, the identified **absorption area** in Lauxtermann is a part of **epitaxial layer 53** generally located below **p-layers (barriers) 56**. The **collection area** connects the **absorption area** to the **photodiode** to provide the charges 58 to the **photodiode**. Particularly, a POSITA would understand that the **collection area** collects the charges 58 from the **absorption area** and funnels them towards the **photodiode** in conjunction with the **p-layers 56** (since p-layers repel the charges). *Id.* And just like the **collection area 224** in Figure 2 of the ’169 patent, the identified **collection**

² According to the plain language of the claims, absorption *area* and collection *area* are part of the epitaxial *layer*. They need not be separate layers.

area in Lauxtermann is a part of **epitaxial layer 53** generally located adjacent to **p-layers (barriers) 56** (e.g., between them) and under **photodiode 12**.



Ex. 1004, FIG. 4.

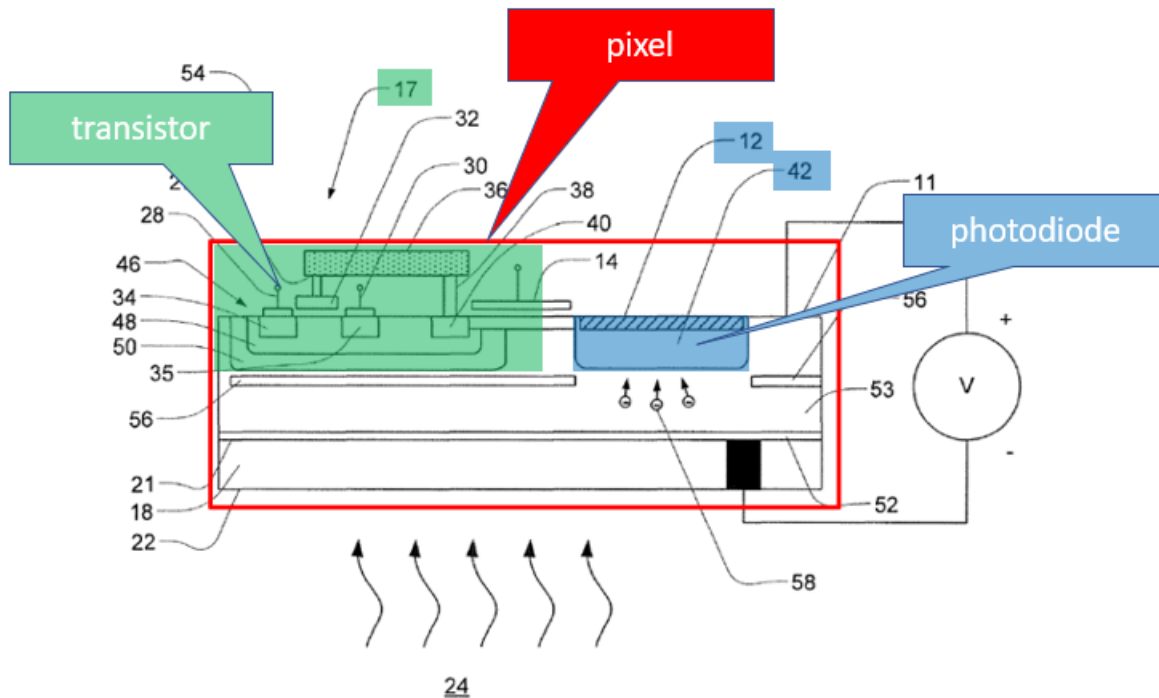
[1e] a barrier layer separating said absorption area from said one or more well regions.

106. I am of the opinion that Lauxtermann discloses a barrier layer separating the absorption area from the well regions.

107. Lauxtermann's FIG. 4 shows that BSI CMOS image sensor 54 (i.e., pixel) includes a **p-layer (barrier) 56** that **separates the absorption area from the P-well 48 and N-well 50**. Ex. 1004, FIG. 4; 5:16-19; 5:41-45. Specifically, Lauxtermann discloses that its barrier layer 56 "may be a deep p+ implant" located underneath transistor 17 and that barrier layer 56 "allows charge 58 to drift, rather

110. As shown in Lauxtermann's FIG. 4, its **photodiode 12** occupies a small area of the pixel and enables electronic components, such as **transistor 17** and transfer gate 14, to be included inside the pixel. In fact, Lauxtermann discloses that BSI CMOS image sensors provide the advantage of having photodiodes that allows "additional space in the pixel for integration of in-pixel signal processing circuits." Ex. 1004, 1:38-43, FIG. 4 (below). Particularly, Lauxtermann discloses that its CMOS image sensor (i.e., pixel) implements "a four transistor (4T) architecture," where at least "a floating diffusion 13, a transfer gate 14, a reset transistor 15, a source follower transistor 17 and a row select transistor 19" are integrated into one pixel, in addition to the **photodiode 12**. *Id.*, 2:51-58. Therefore, Lauxtermann's **photodiode 12** is a **low fill factor diode**.

111. Moreover, a POSITA would have understood that integration of the transistors and other imaging processing components with the photodiode in the pixel improves the efficiency and at the same time reduces the size of the image sensor. Ex. 1004, 1:42-43. Accordingly, it would have been obvious to use a **low fill factor diode** for Lauxtermann's photodiode so that other image processing components can be integrated into the pixel to improve performance of the image sensor.



Ex. 1004, FIG. 4 (annotated).

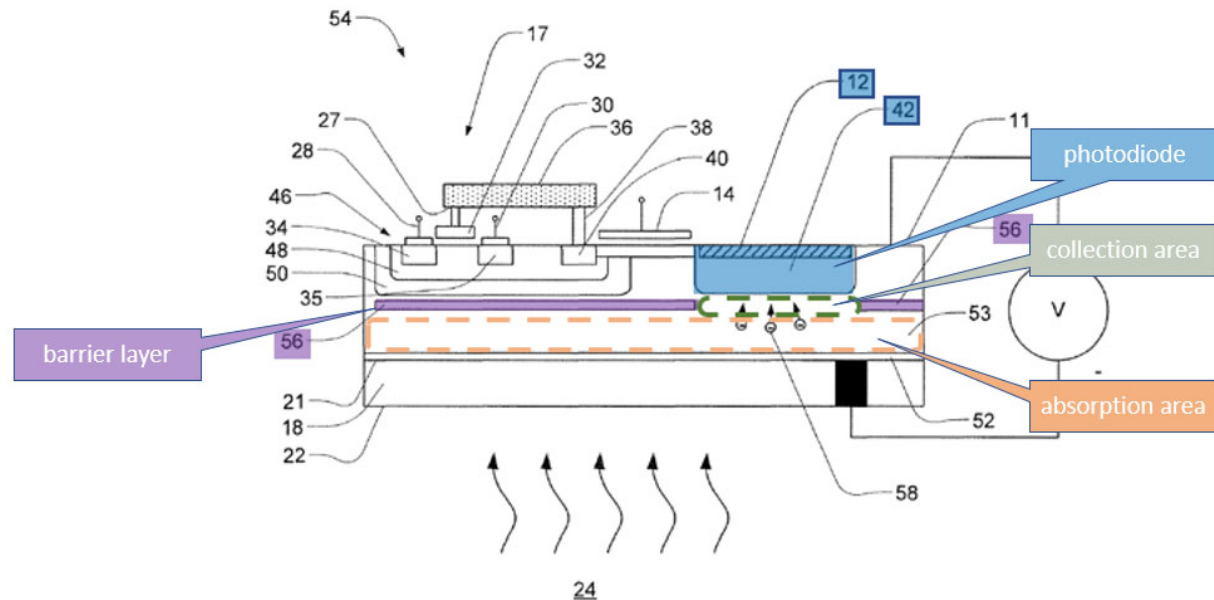
3. Claim 3

3. The BSI CMOS pixel array of claim 1, wherein said collection area extends from said absorption area to said photodiode through said barrier layer.

112. I am of the opinion that Lauxtermann renders obvious claim 3's requirement the "collection area extends from said absorption area to said photodiode through said barrier layer."

113. As shown in Lauxtermann's FIG. 4, the **collection area** extends from the **absorption area** to **photodiode 12** through **barrier layer 56**. Ex. 1004, FIG.

4.



Ex. 1004, Fig. 4 (annotated).

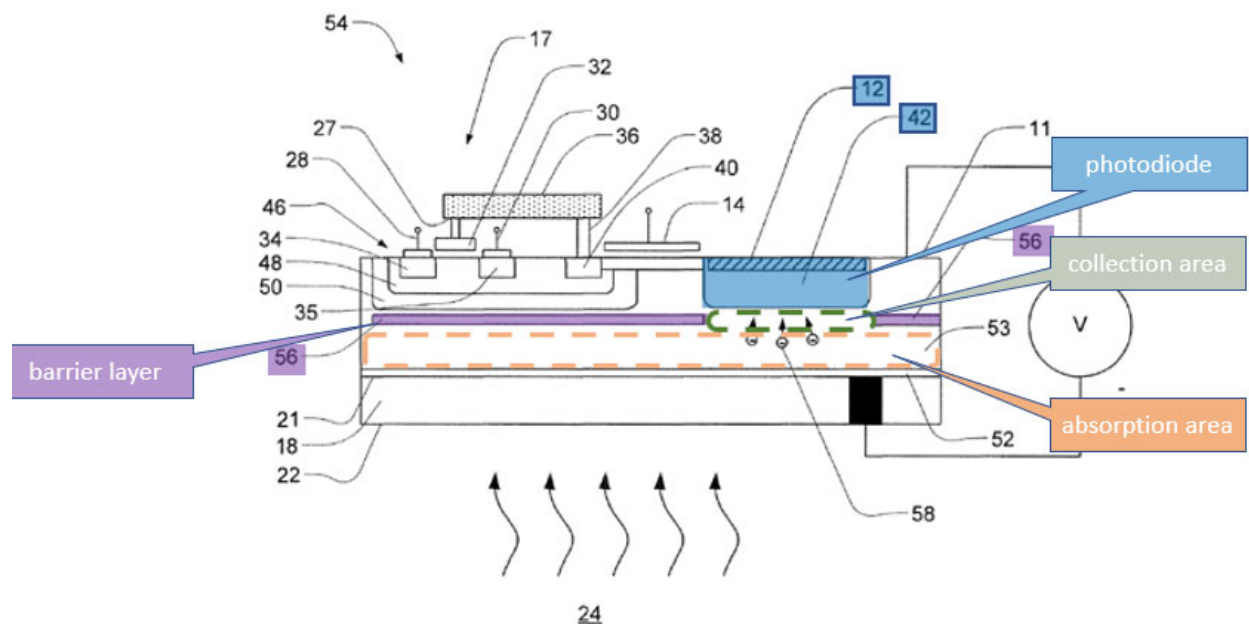
4. Claim 4

4. The BSI CMOS pixel array of claim 1, wherein said collection area is configured to perform the functionality of an electrostatic lens to collect said electrons from said absorption area.

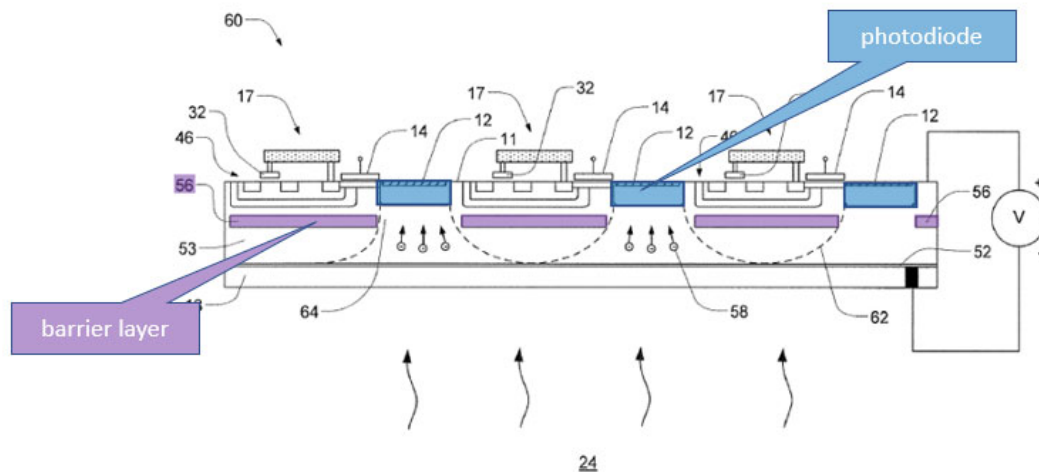
114. I am of the opinion that Lauxtermann renders obvious claim 4's requirement the "collection area is configured to perform the functionality of an electrostatic lens to collect said electrons from said absorption area." As known in the art, an electrostatic lens creates an electric field to guide electrons towards a detector. Exs. 1016; 1057, 6:11-12, 6:65-7:5.

115. A POSITA would understand that Lauxtermann's **collection area** collects electric charges 58 (i.e., electrons) from the **absorption area** and guides and/or directs the collected electrons to the **photodiode 12**. Ex. 1004, Fig. 4, 5:41-45 ("[T]he p-layer 56 allows charge 58 to drift, rather than diffuse, to the light

receiving element of the pinned photodiode 12.”). Lauxtermann’s **collection area** is configured to perform the functionality of an electrostatic lens because electric fields 62 around p-layers 56 create an electron funnel 64 at the **collection area**, which collects and guides electrons to **photodiode 12**. Ex. 1004, 5:50-65, FIG. 5. It would have been obvious to a POSITA that Lauxtermann’s heavily doped p-layers 56 repel electrons (i.e., electric charges 58) in the **absorption area** and facilitate lateral movement of the electrons towards the **collection area**. Electrons that reach the collection area are driven across the junction into the n-type layer 42 of the **photodiode 12**. This is the functionality of the electrostatic lens according to the ’169 patent. Ex. 1001, 7:23-32. Therefore, it would have been obvious that Lauxtermann’s **collection area** is **configured to perform the functionality of an electrostatic lens**.



Ex. 1004, FIG. 4 (annotated).



Ex. 1004, FIG. 5 (annotated).

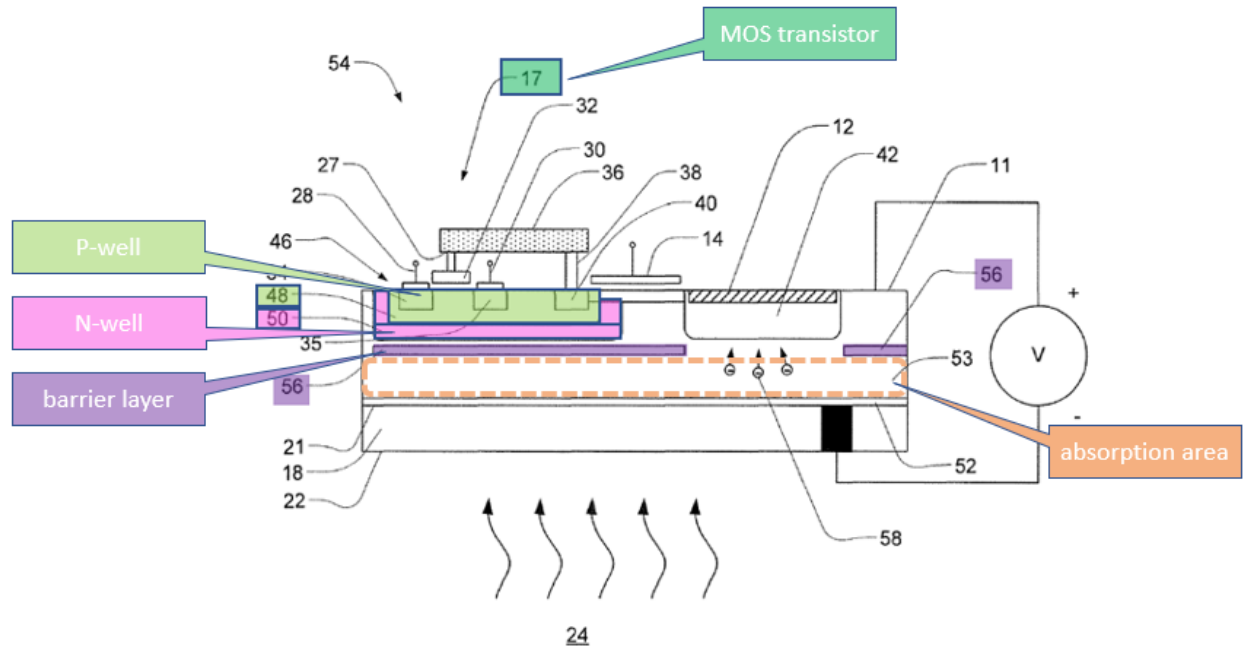
5. Claim 5

5. The BSI CMOS pixel array of claim 1, wherein said barrier layer is configured to prevent diffusion of said electrons from said absorption area to said well regions.

116. I am of the opinion that Lauxtermann discloses that its barrier layer 56 is configured to prevent diffusion of electron from the absorption area to the N-well 50.

117. Lauxtermann discloses that its barrier layer 56 “may be a deep p⁺ implant” located underneath transistor 17 and its P-well region 48 and N-well region 50, and that the barrier layer 56 “allows charge 58 to drift, rather than diffuse, to the light receiving element of the pinned photodiode 12.” Ex. 1004, FIG. 4; 5:41-45. Without barrier layer 56, charges would diffuse towards both pinned photodiode 12 and the active pixel circuitry (i.e. transistor 17 with N-well

50). *Id.*, 4:57-65. Barrier layer 56 is therefore **configured to prevent diffusion of electrons from the absorption area to the well regions.**



Ex. 1004, FIG. 4 (annotated).

6. Claim 6

- 6. The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 4 micron (μm).**

118. I am of the opinion that Lauxtermann renders obvious claim 6's requirement the "thickness of said epi layer is at least 4 micron (μm)."

119. As discussed in Section IX.B.1, in connection with claim elements 1d and 1e, a POSITA would understand that and that semiconductor layers 53 (FIG. 4) and 16 (FIG. 1) are both epitaxial layers. Ex. 1004, *compare* FIG. 1 *with* FIG. 4. Lauxtermann explains that the Figure 1 embodiment “is a backside illuminated

CMOS image sensor 10, according to an embodiment of the invention” (Ex. 1004, 2:50-51), while the Figure 4 embodiment is “a backside illuminated CMOS image sensor 54 with a p-layer 56” (*id.*, 5:1-3). Both embodiments teach use of a “pinned photodiode 12” which is fabricated on a semiconductor layer. *Id.*, 3:4-5.

Lauxtermann expressly discloses the pinned photodiode is fabricated on **epitaxial** layer 16, which includes a p-doped region 20 that is **5 μm** thick. Ex. 1004, 3:4-8.

120. Lauxtermann, however, does not expressly disclose the thickness of semiconductor layer 53 (the epitaxial layer identified in Ground 1). However, given Lauxtermann’s teachings that the pinned photodiodes are fabricated on a 5 μm thick epitaxial layer (as claimed), it would have been obvious to a POSITA to fabricate Lauxtermann’s semiconductor layer 53 with a thickness similar to the thickness of its semiconductor layer 16. Layers 16 and 53 are from similar embodiments of the same invention and both layers perform the same function of converting lights 24 into electric charges and serving as the underlying substrate for **photodiode 12** and the active pixel circuitry, including floating diffusion 13 (n-doped region 40 in Fig. 4), transfer gate 14, and source follower transistor 17.

121. Further, it would have been obvious to a POSITA to use a at least 4 micron thick epitaxial layer in a BSI CMOS image sensor to improve the light sensitivity of the image sensor. A POSITA would have understood that the amount of electric charges generated by an epitaxial layer from absorbed light incident on

the image sensor is approximately proportional to the thickness of the epitaxial layer. Ex. 1005 (Zucca), 1745. Therefore, a POSITA would use a at least 4 micron thick epitaxial layer, like the 5 micron epitaxial layer in Lauxtermann's FIG. 1 in every embodiment of Lauxtermann's BSI CMOS image sensors.

7. Claim 10

10. The BSI CMOS pixel array of claim 1 comprising a micro lens, said absorption area is between said micro lens and said barrier layer.

122. Lauxtermann renders obvious claim 10. A POSITA would have understood that microlens arrays are widely used in, and are extremely important to, BSI CMOS image sensors. Microlens arrays focus light incident on each microlens towards the absorption area of a corresponding photodiode. The use of microlenses with BSI CMOS image sensors like Lauxtermann's was very well-known and highly conventional. Exs. 1033-1036, 1059. Indeed, one well-known advantage of BSI image sensors is the "small distance between microlens and silicon photodiode." Ex. 1035, 24.1.1 (Introduction). Lauxtermann, which teaches a BSI CMOS image sensor, therefore expressly teaches a microlens. It would have also been obvious to a POSITA that Lauxtermann's BSI CMOS image sensor would include a microlens, specifically on the backside of the sensor so that the absorption layer is between the microlens and the barrier layer, to improve light collection efficiency of its image sensor for use in electronic devices.

8. Claim 11

11. The BSI CMOS pixel array of claim 10 comprising an anti-reflective coating (ARC) layer, said ARC layer is between said micro lens and said absorption area.

123. Lauxtermann renders obvious claim 11. It was well-known that ARC layers are widely used in, and extremely important to, BSI CMOS image sensors. A POSITA would have understood that ARC layers allow more light to reach a photodiode by minimizing light reflection at the interface between a component on the backside surface of the image sensor die and the silicon material of the backside surface itself, which would otherwise decrease the efficiency of the image sensor. The use of ARC layers with BSI CMOS image sensors like Lauxtermann's was very well-known and highly conventional. Exs. 1033-1036, 1059.

Lauxtermann, which teaches a BSI CMOS image sensor, therefore expressly teaches an ARC layer. It would have also been obvious to a POSITA to include an ARC layer, in between the microlens and the absorption area, to improve light collection efficiency of its image sensor for use in electronic devices.

9. Claim 12

12. The BSI CMOS pixel array of claim 1, wherein said one or more MOS transistors comprise one or more transistors selected from a group consisting of one or more P-type MOS (PMOS) transistors and one or more N-type MOS (NMOS) transistors.

124. I am of the opinion that Lauxtermann discloses claim 12's requirement the "MOS transistors comprise one or more transistors selected from a group consisting of one or more P-type MOS (PMOS) transistors and one or more N-type MOS (NMOS) transistors."

125. Lauxtermann discloses that its transistors are MOS transistors and that transistor 17 may be an NMOS transistor. Ex. 1004, 3:45-50, 5:11-12.

Lauxtermann further discloses "CMOS image sensor may [also] include active pixel circuitry, such as a p-type metal-oxide-semiconductor (PMOS) device." *Id.*, 6:17-19. Lauxtermann therefore discloses that its **one or more MOS transistors are selected from a group consisting of PMOS and NMOS transistors.**

10. Claim 13

13. The BSI CMOS pixel array of claim 1, wherein said barrier layer comprises a deep PW implant.

126. I am of the opinion that Lauxtermann discloses claim 13's requirement that "barrier layer comprises a deep PW implant."

127. Lauxtermann discloses that its barrier layer 56, which is a p-layer, "may be a **deep p+ implant**" located underneath the transistor 17. Ex. 1004, 5:40-

This diagram shows a cross-sectional view of a MOS transistor with an integrated photodiode. The MOS transistor is formed on a substrate (24) and includes a gate stack (12, 14, 17, 32, 36, 38, 40, 42) and source/drain regions (27, 28, 30, 34, 35). The photodiode is formed in a P-well (46) and N-well (50) region, with a barrier layer (56) and an absorption area (53). The photodiode is connected to a voltage source (V) and a current source (58). The diagram is labeled with various reference numerals (11, 12, 14, 17, 18, 21, 22, 27, 28, 30, 32, 34, 35, 36, 38, 40, 42, 46, 48, 50, 52, 53, 56, 58) and includes a legend for the P-well, N-well, and barrier layer.

128. Moreover, the use of deep p-well implants in image sensors was well-known by the priority date of the '169 patent. *See* Ex. 1012, 57-58, FIG. 2; Ex. 1013, 1311, FIG. 2; Ex. 1050, 3:45-64; Ex. 1051, 1:33-39, 4:47-48, 6:37-67, Figs. 15A-15C. At a minimum, therefore, the use of a deep p-well implant in Lauxtermann's BSI CMOS image sensor would have been obvious.

11. Claim 14

14. The BSI CMOS pixel array of claim 1, wherein said barrier layer comprises a boron implant.

129. I am of the opinion that Lauxtermann renders obvious claim 14's requirement the "barrier layer comprises a boron implant."

130. Lauxtermann discloses that its p-layer 56 (i.e., barrier layer) may be a deep p⁺ implant. Ex. 1004, 5:41-42. Boron is the most common p-type dopant. *See* Ex. 1024, 467; Ex. 1025, 31; Ex. 1026, 4:24-30; Ex. 1027, [0059], [0106], [0107]. Therefore, it would have been obvious to a POSITA to use a **boron implant** for Lauxtermann's deep p⁺ implant layer 56 (i.e., barrier layer). Indeed, when describing other p-layers, Lauxtermann teaches the use of boron, confirming the obviousness of using boron—the most common p-type dopant—in Lauxtermann's p⁺ implant layer 56. Ex. 1004, 3:4-8 ("The semiconductor layer 16 may be an epitaxial layer with a p-doped region 20.").

12. Claim 15

15. The BSI CMOS pixel array of claim 1, wherein said photodiode comprises a fully pinned diode.

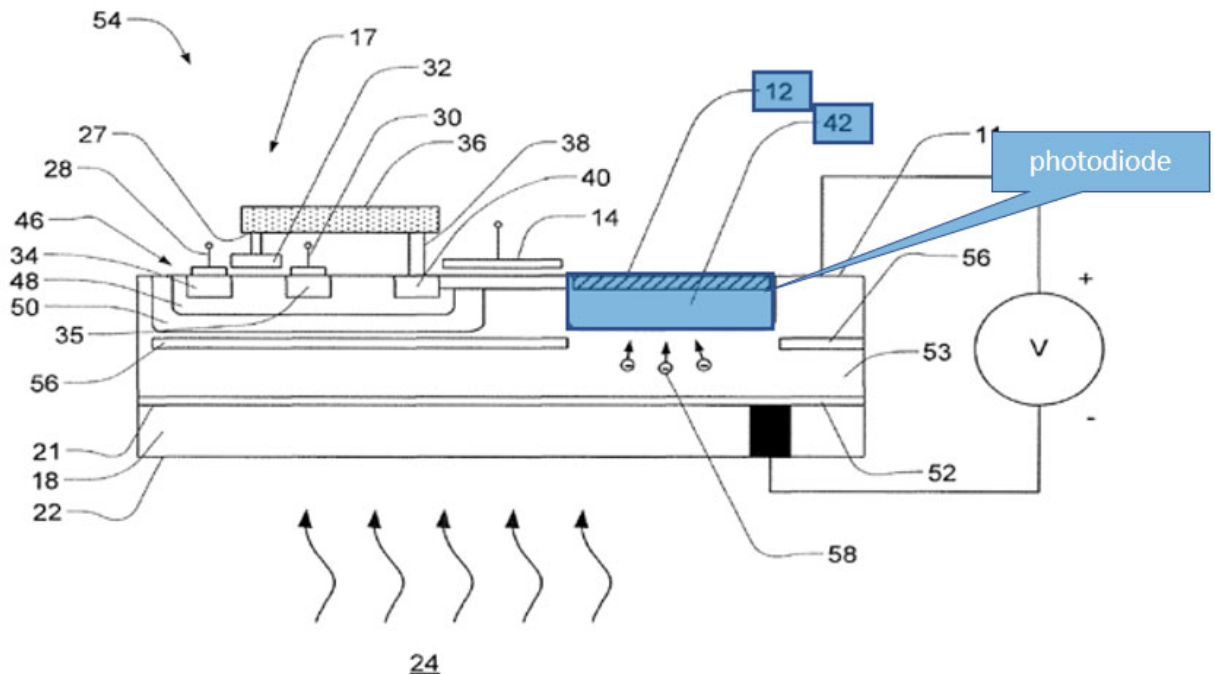
131. I am of the opinion that Lauxtermann renders obvious claim 15's requirement the "photodiode comprises a fully pinned diode." As stated above in Section V.E.6, a photodiode may be pinned, partially pinned, or unpinned. A pinned photodiode has a p⁺ pinning layer that covers the photodiode while a

partially pinned photodiode has an n⁺ region in an area of the photodiode not covered by the p⁺ pinning layer. Ex. 1029, 3:61-4:5, 4:32-67, Fig. 2, Fig. 4. The “fully pinned” terminology used in the ‘169 patent is what is commonly referred to as “pinned,” *i.e.*, not partially pinned. Lauxtermann discloses that its photodiode 12 is a **pinned photodiode**. *See*, e.g., Ex. 1004, 1:7-9 (“[T]he invention relates to backside illuminated CMOS image sensors with *pinned* photodiodes.”); 2:48-50, 59-61. A POSITA would have understood that when a photodiode is referred to as “pinned,” as in Lauxtermann, that photodiode is fully pinned (as that terminology is used in the ‘169 patent). *See* Ex. 1028, Ex. 1029, Fig. 2. Otherwise, a POSITA would have referred to it as “partially pinned” or “un-pinned” instead rather than simply “pinned.” *Compare* Ex. 1029, 3:61-4:5, Fig. 2 *with* 4:32-67, Fig. 4.

132. A pinned photodiode is often used with four (4) transistors in a 4T CMOS APS pixel while a partially pinned photodiode is used with three (3) transistors in a 3T CMOS APS pixel. “[T]he pinned photodiode is often used in pixels with nominally four (4) transistor gates, such a CMOS APS pixel is often referred to as a ‘4T’ pixel. (This is in contrast to a ‘3T’ pixel which refers to CMOS active pixel sensors where the photodiode is directly connected to the in-pixel source-follower, and complete intrapixel charge transfer from the photodiode is not performed. Sometimes ‘partially pinned photodiodes’ ... were used in 3T CMOS APS devices.)” Ex. 1028, 35. In a 4T CMOS APS pixel, a transfer gate

(TG) transfers the charges collected at the pinned photodiode (PDD) to a n⁺ floating diffusion (FD), whose potential is monitored by a source-follower (SF) transistor within the pixel. *Id.* In contrast, the partially pinned photodiode is used in pixels with three (3) transistors and such a CMOS APS pixel is referred to as a “3T” pixel. *Id.* Lauxtermann teaches the use of a 4T CMOS APS pixel (Ex. 1004, 2:51-56) and therefore a POSITA would readily understand that Lauxtermann’s pinned photodiode is fully pinned.

133. Further, as discussed in Section II.B.2, the difference between a pinned and a partially-pinned photodiode is whether the pinning layer covers the entire surface of the photodiode. Lauxtermann specifically discloses a **pinned photodiode 12**, which as shown in FIG. 4 below, has a p⁺ pinning layer that covers the photodiode and does not include an n⁺ layer in an area of the photodiode not covered by the pinning layer. Ex. 1004, FIG. 4; Ex. 1004, 1:7-9; 2:48-50, 59-61. And a POSITA would also understand that Lauxtermann’s p⁺ pinning layer 12 covers the entire surface of the n-doped region 42. “The pinned photodiode 12 collects charge due to light 24” and “[t]ransfer gate 14 transfers the signal from the pinned photodiode 12 to the NMOS source follower device 17” without using any n⁺ region in the photodiode. *Id.*, 5:5-10. Therefore Lauxtermann’s photodiode is a **fully pinned photodiode**, as claimed.



Ex. 1004, FIG. 4.

134. Moreover, Lauxtermann discloses “a need in the art for backside illuminated CMOS image sensors with reduced noise, dark current and sense node capacitance.” Ex. 1004, 1:50-52. It was well-known that fully pinned photodiodes have low noise, high quantum efficiency and low dark current. Ex. 1028, 33. Thus, a POSITA would readily understand that Lauxtermann’s “pinned photodiode” is a **fully pinned diode**, as opposed to a partially or non-pinned photodiode. It was well-known to a POSITA that pinned photodiodes are widely used in CCD and CMOS sensors due to its low noise, high quantum efficiency and low dark current. Ex. 1028, Abstract. In fact, pinned photodiodes were developed to overcome the problem of interline transfer (ILT) lag and kTC noise (thermal noise on a resistor-capacitor circuit) and suppress dark current. *Id.*, 34.

Lauxtermann discloses that a “backside illuminated CMOS image sensors with conventional photodiode” has disadvantages such as “high noise, high dark current and high sense node capacitance,” and therefor proposed “a backside illuminated CMOS image sensors with *pinned* photodiodes.” Ex. 1004, 1:7-9, 45-48. Thus, a POSITA would have understood that Lauxtermann’s reference to a “pinned” photodiode referred to a diode that was fully, as opposed to partially, pinned. Ex. 1004, 1:7-9, 2:48-50, 2:59-61, 5:3-10. Therefore, a POSITA would understand that Lauxtermann’s photodiode 12 is a **fully pinned diode** as claimed.

C. Ground 2: Claims 2, 6, 7 And 9 Are Obvious Over Lauxtermann In View Of Zucca

135. I am of the opinion that Lauxtermann in view of Zucca render obvious claims 2, 6, 7, and 9 of the ’169 patent.

1. Reasons to Combine Lauxtermann with Zucca

136. As discussed above, Lauxtermann discloses or renders obvious all the limitations of claim 1. Claim 2 requires that the photodiode comprise a “low fill factor” (“FF”) diode. Claims 6 and 7 require that the epitaxial layer be of various minimum thicknesses. Claim 9 require that the epitaxial layer be of certain minimum resistivity. Zucca teaches (1) a low FF diode, which meets the requirement of claim 2, (2) an epitaxial layer of 12 μm thickness, which meets the “minimum” requirements of claims 6 and 7, and (3) an epitaxial layer with a high resistivity of about 1000 ohm-cm, which meets the requirement of claim 9. A

POSITA would have been motivated to modify Lauxtermann to include these teachings and would have had a reasonable expectation of success, for the following reasons.

137. *An epi layer of at least 4 [claim 6] / 10 [claim 9] μm :* A POSITA would have been motivated to include an epitaxial layer at least 4 μm thick in Lauxtermann's BSI CMOS image sensor according to Zucca's teachings because doing so would improve the light sensitivity and thus efficiency of its image sensor. As disclosed in both Lauxtermann and Zucca, light incident on the back side of their respective BSI image sensors is absorbed by the epitaxial layer, which generates electric charges that are then collected by the photodiodes implanted in the epitaxial layer. Ex. 1004, 5:11-13, 5:36-39; Ex. 1005, FIG. 1. As further discussed in Zucca, the electric charges collected by the photodiodes of its monolithic pixel sensors (MAPS), which are BSI CMOS image sensors, are "almost proportional to the epitaxial layer thickness." Ex. 1005, 1745.

Specifically, Zucca discloses two image sensor designs, one with a 12 μm thick epitaxial layer and the other with a 5 μm thick epitaxial layer, and shows that the amount of electric charges collected by the sensor with the 12 μm epitaxial layer is about two times higher than the sensor with the 5 μm epitaxial layer. *Id.* Similarly, as discussed above, Lauxtermann discloses that one embodiment of its BSI image sensor includes an epitaxial layer 16 that is at least 5 μm thick. Ex. 1001, 3:4-8.

Thus, a greater than 4 micron thick epitaxial layer is already contemplated by Lauxtermann. Therefore, including an at least 4 μm thick epitaxial layer in Lauxtermann's BSI CMOS image sensor according to Zucca's teachings would have the obvious added benefit of better electric charge collection performance and therefore improved efficiency of the image sensor, especially in low light conditions. And because Lauxtermann expressly teaches using a thick epitaxial layer, a POSITA would have had a reasonable expectation of success in doing so.

138. *An epitaxial layer of at least 100 ohm-cm [claim 9]*: Further, a POSITA would also have been motivated to use a high resistivity epitaxial layer (e.g., greater than 100 ohm to centimeter (ohm-cm)) in Lauxtermann's BSI CMOS image sensor according to Zucca's teachings to improve the efficiency of its image sensor. As disclosed in Zucca, a higher resistivity in the epitaxial layer corresponds to more electric charges (generated from incident light) collected by the image sensor. Ex. 1005 at 1745 (reporting that "the charge collected by [a CMOS image sensor], featuring a high resistivity epitaxial layer, is about 35% higher than [another CMOS image sensor] featuring a standard resistivity epitaxial layer," while other parameters are equal). Zucca teaches its "high resistivity epitaxial layer option" improves "charge collection properties." *Id.*, 1748. Specifically, Zucca teaches a "sensor fabricated on a 12 μm thick high resistivity epitaxial layer" is "the best solution among different available options in terms both of the amount of

collected charge and of charge collection uniformity.” *Id.* Lauxtermann similarly discloses that its semiconductor layer 53 (an epitaxial layer) is “a high resistivity semiconductor layer” and that the use of the high resistivity semiconductor layer 53 in combination with other measures (e.g., p-layer 56 as a barrier layer) “enhances the performance of the CMOS sensor 60, improves quantum efficiency and reduces noise, dark current and sense node capacitance.” Ex. 1004 at 5:7-9, 5:61-65.

139. *A photodiode comprising a low fill factor diode [claim 2]:* Finally, A POSITA would have also been motivated to include a low fill factor photodiode in Lauxtermann’s BSI CMOS image sensor according to Zucca’s teachings to improve the image processing performance of its image sensor. As a POSITA would have understood, a low fill factor photodiode occupies a small area of a pixel, and therefore allows image processing components such as transistors to be integrated into the pixel with the photodiode, which improves the image processing performance of the image sensor. *Id.* In fact, Lauxtermann already discloses that one advantage of BSI CMOS image sensors is the “availability of additional space in the pixel for integration of in-pixel signal processing circuits” and that its sensor implements “a four transistor (4T) architecture” where transistors and other components are integrated together with a photodiode into one pixel. Ex. 1004 at 1:40-43, 2:51-58. Thus, a POSITA would have used a low fill factor photodiode in

Lauxtermann's BSI CMOS image sensor according to Zucca's teachings to improve the image processing performance of its image sensor.

140. A person of ordinary skill in the art would have been motivated to combine Lauxtermann and Zucca for the following additional reasons:

141. *Similar techniques to solve the same problems:* Like the '169 patent, both Lauxtermann and Zucca address the same problem with similar techniques: to improve the efficiency of a BSI CMOS image sensor by using a barrier layer to prevent electric charges from diffusing to transistors integrated in the pixel, thereby allowing the photodiode to collect more electric charges. Lauxtermann discloses that a photodiode and an "NMOS active pixel circuitry" (which includes a transistor hosted in a P-well, which is in turn hosted in an N-well) are integrated into each pixel of its image sensor. Ex. 1004, FIG. 3; 4:13-37. It recognizes that its photodiode "collects only a fraction of the [electric] charges" because the charges "diffuse towards [both] the pinned photodiode 12 and the active pixel circuitry" and the pixel circuitry absorbs some of the electric charges. *Id.*, 4:57-65. Thus, "[t]he efficiency of the CMOS image sensor 44 would greatly improve if more charge[s] traveled to the pinned photodiode 12 instead of the active pixel circuitry." *Id.* Lauxtermann solves the problem by implanting a p-layer (barrier layer) underneath the N-well of the pixel circuitry (transistor) to prevent diffusion of the electric

charges to the transistor, allowing the photodiode to collect more charges. *Id.*, FIG. 4, 5:40-49.

142. Similar to Lauxtermann, Zucca discloses that its each pixel of its image sensor integrates a photodiode (Nwell diode) and a PMOS transistor hosted in an Nwell, which “by acting as parasitic charge collectors, may degrade the pixel charge collection efficiency.” Ex. 1005, 1742. Similar to Lauxtermann’s solution, Zucca proposes depositing a “deep Pwell implant . . . beneath the PMOS competitive NWells” to prevent the charges been collected by the transistors and thereby improving the charge collection efficiency of the photodiode. *Id.*

143. ***Same field of endeavor:*** Like the ’169 patent, both Lauxtermann and Zucca are directed to BSI CMOS image sensors and methods for improving the efficiency of the image sensors. Both Lauxtermann and Zucca teach a BSI CMOS image sensor where each pixel integrates a photodiode and at least one transistor for image processing. Both use an epitaxial layer to absorb light incident on the image sensor and generate electric charges for collection at the photodiode. *Id.* Both Lauxtermann and Zucca recognize the performance degradation caused by parasitic charge collection of the transistor in the pixel, and both proposed implanting a barrier layer underneath the transistor to prevent diffusion and direct the electric charges to the photodiode instead.

144. *Reasonable expectation of success/predictable results:* A POSITA would have been motivated to include an at least 4 μm thick epitaxial layer with a high resistivity (e.g., greater than 100 ohm-cm) in Lauxtermann's BSI CMOS image sensor with at least a reasonable expectation of success because the thickness and resistivity of the epitaxial layer in an image sensor is easily controllable in the fabrication process. Indeed, Lauxtermann already discloses that one embodiment of its image sensor includes an epitaxial layer that has a thickness of at least 5 μm (Ex. 1005, 3:5-8) and a "high resistivity semiconductor layer [i.e., epitaxial layer] 53" (Ex. 1005, 5:7-8, 61-65). Thus, a POSITA with knowledge of Lauxtermann would have naturally looked to the disclosures of Zucca when finding a method to improve the efficiency of a BSI CMOS image sensor.

145. Further, designing Lauxtermann's BSI CMOS image sensor to include a low fill factor photodiode as disclosed in Zucca would also have been readily accomplished. As a POSITA would have understood, a low fill factor photodiode occupies a small area of a pixel and thus allows other image processing components such as transistors to be integrated in the pixel. In fact, Lauxtermann already discloses one advantage of CMOS BSI image sensors is providing "availability of additional space in the pixel for integration of in-pixel signal processing circuits" and that its sensor implements "a four transistor (4T) architecture" where transistors and other components are integrated together with a

photodiode into one pixel. Ex. 1004 at 1:40-43, 2:51-58. Therefore, a POSITA would have been motivated to include a low fill factor photodiode (i.e., a small photodiode) in Lauxtermann's BSI CMOS image with at least a reasonable expectation of success because Lauxtermann's image sensor already includes a small photodiode that allows the integration of at least one transistor in the same pixel.

2. Claim 2

2. The BSI CMOS pixel array of claim 1, wherein said photodiode comprises a low fill factor (FF) diode.

146. Claim 2 depends from claim 1. As discussed in Section IX.B.1 above, the Lauxtermann-Zucca combination discloses and/or renders obvious each element of claim 1 for the same reasons Lauxtermann alone discloses and/or renders obvious claim 1.

147. I am of the opinion that Lauxtermann combined with the low fill factor diode of Zucca renders obvious claim 2's further recitation of "said photodiode comprises a low fill factor (FF) diode."

148. Zucca discloses that one pixel of its image sensor has "a 50 μm pitch" (i.e. a width of 50 μm) and "4 interconnected Nwell square diodes, each with a 1.5 μm side." Ex. 1004, 1743. This means that the photodiodes occupy **only about 0.36%** of the total area of a pixel. Further, the relatively small photodiodes allow Zucca to integrate multiple NMOS transistors and PMOS transistors into one pixel.

Id., 1742, FIG. 1. Thus, a POSITA would understand that Zucca’s photodiodes are **low fill factor photodiodes**.

149. In fact, Lauxtermann already discloses that one advantage of BSI CMOS image sensors is providing “availability of additional space in the pixel for integration of in-pixel signal processing circuits” and that its sensor implements “a four transistor (4T) architecture” where transistors and other components are integrated together with a photodiode into one pixel. Ex. 1004 at 1:40-43, 2:51-58. Thus, it would have been obvious to include Zucca’s low fill factor photodiodes in Lauxtermann’s BSI CMOS image sensors.

3. Claim 6

6. The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 4 micron (μm).

150. Claim 6 depends from claim 1. As discussed in Section IX.B.1 above, the Lauxtermann-Zucca combination discloses and/or renders obvious each element of claim 1 for the same reasons Lauxtermann alone discloses and/or renders obvious claim 1.

151. I am of the opinion that Lauxtermann combined with Zucca’s disclosure render obvious claim 6’s further recitation of “a thickness of said epi layer is at least 4 micron (μm).”

152. As discussed in Section IX.B.6, Lauxtermann alone renders claim 6 obvious. Additionally, Zucca discloses that its BSI CMOS image sensor includes

“a lightly P-doped epitaxial layer **about 10 μm thick.**” Ex. 1005, 1743. Zucca further provides three additional exemplary topologies for its epitaxial layer with different thicknesses and resistivities to achieve different performances: (1) **5 μm thick** with standard resistivity, (2) **12 μm thick** with standard resistivity, and (3) **12 μm thick** with high resistivity. *Id.* Thus, Zucca discloses that **a thickness of its epitaxial layer is at least 4 micron (μm).** It would have been obvious to include Zucca’s at least 4 μm thick epitaxial layer in Lauxtermann’s BSI CMOS image sensor.

4. Claim 7

7. **The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 10 micron (μm).**

153. Claim 7 depends from claim 1. As discussed in Section IX.B.1 above, the Lauxtermann-Zucca combination discloses and/or renders obvious each element of claim 1 for the same reasons Lauxtermann alone discloses and/or renders obvious claim 1.

154. I am of the opinion that Lauxtermann combined with Zucca’s disclosure render obvious claim 7’s further recitation of “a thickness of said epi layer is at least 10 micron (μm).”

155. Zucca discloses that its BSI CMOS image sensor includes “a lightly P-doped epitaxial layer **about 10 μm thick.**” Ex. 1005, 1743. Zucca further provides three additional exemplary topologies for its epitaxial layer with different

thicknesses and resistivities to achieve different performances: (1) 5 μm thick with standard resistivity, (2) **12 μm thick** with standard resistivity, and (3) **12 μm thick** with high resistivity. *Id.* Thus, Zucca discloses **a thickness of its epitaxial layer is at least 10 micron (μm)**. It would have been obvious to include Zucca's at least 10 μm thick epitaxial layer in Lauxtermann's BSI CMOS image sensor.

5. Claim 9

9. The BSI CMOS pixel array of claim 1, wherein a resistivity of said epi layer is greater than 100 ohm to centimeter (ohm-cm).

156. Claim 9 depends from claim 1. As discussed in Section IX.B.1 above, the Lauxtermann-Zucca combination discloses and/or renders obvious each element of claim 1 for the same reasons Lauxtermann alone discloses and/or renders obvious claim 1.

157. I am of the opinion that Lauxtermann combined with Zucca's disclosure render obvious claim 9's further recitation of "a resistivity of said epi layer is greater than 100 ohm to centimeter (ohm-cm)."

158. Both Lauxtermann and Zucca disclose the benefits of using high resistive epitaxial layers. Ex. 1004, 5:59-65 (stating high resistivity semiconductor layer 53 may help improving "quantum efficiency and reduces noise, dark current and sense node capacitance"); Ex. 1005, 1745. Zucca further expressly discloses that one of its epitaxial layer designs has a high resistivity of about **1000 ohm-cm** with improved collection properties. Ex. 1005 at 1743. Thus, Zucca discloses that

a resistivity of its epitaxial layer is at least 100 ohm-cm. It would have been obvious to include Zucca's 1000 ohm-cm epitaxial layer in Lauxtermann's BSI CMOS image sensor.

D. Ground 3: Claims 10 And 11 Are Obvious Over Lauxtermann In View Of Akiyama

159. I am of the opinion that Lauxtermann in view of Akiyama render obvious claims 10 and 11 of the '169 patent.

1. Reasons to Combine Lauxtermann with Akiyama

160. As discussed above, Lauxtermann discloses or renders obvious all the limitations of claim 1. Claim 10 further requires a microlens and claim 11 further requires antireflective coating (ARC) layer. Akiyama teaches both a microlens and an ARC layer. A POSITA would have been motivated to include a microlens and an antireflective coating (ARC) layer in Lauxtermann's BSI CMOS image sensor according to Akiyama's teachings to improve the efficiency of its image sensor for use in electronic devices.

161. *Microlens [claim 10] and ARC layer [claim 11]:* A POSITA would have been motivated to include a microlens and an antireflective coating (ARC) layer in Lauxtermann's BSI CMOS image sensor according to Akiyama's teachings to improve the efficiency of its image sensor for use in electronic devices. A POSITA would have understood that microlens arrays are widely used in CCD and CMOS image sensors so that light incident on each microlens is

focused towards a corresponding photodiode. A POSITA would also have understood that ARC allows more light to reach a photodiode by minimizing light reflection at the interface between a component on the backside surface of the image sensor die and the silicon material of the backside surface itself, which would otherwise decrease the efficiency of the image sensor. Thus, a POSITA would have been motivated to incorporate a microlens and an ARC into Lauxtermann's image sensor according to Akiyama's teachings to improve light collection efficiency of its image sensor for use in electronic devices.

162. A person of ordinary skill in the art would have been motivated to combine Lauxtermann and Akiyama for the following additional reasons:

163. ***Same field of endeavor:*** Like the '169 patent, both Lauxtermann and Akiyama are directed to BSI CMOS image sensors and methods for improving the performances of the image sensors. Lauxtermann and Akiyama disclose BSI CMOS image sensors that have very similar structures. For example, both Lauxtermann and Akiyama disclose that each pixel of their image sensors integrates a photodiode and at least one transistor for image processing. Both include a photodiode implanted in a semiconductor layer, which generates electric charges from light and collects the charges to be transferred to the photodiode. Both include a least one transistor implanted in a well region adjacent to a photodiode.

164. *Reasonable expectation of success/predictable results*: Designing Lauxtermann’s BSI CMOS image sensor to include a microlens and an ARC according to Akiyama’s teachings would have been readily accomplished. A POSITA with knowledge of Lauxtermann would have naturally looked to the disclosures of Akiyama when finding ways to improve the efficiency of a BSI CMOS image sensor. A POSITA would have been motivated to include a microlens and an ARC in Lauxtermann’s BSI CMOS image sensor with at least a reasonable expectation of success because microlenses and ARCs are routinely used in BSI CMOS image sensors and it is very easy to add an ARC layer above Lauxtermann’s photodiode and then a microlens array above the ARC layer in the fabrication process.

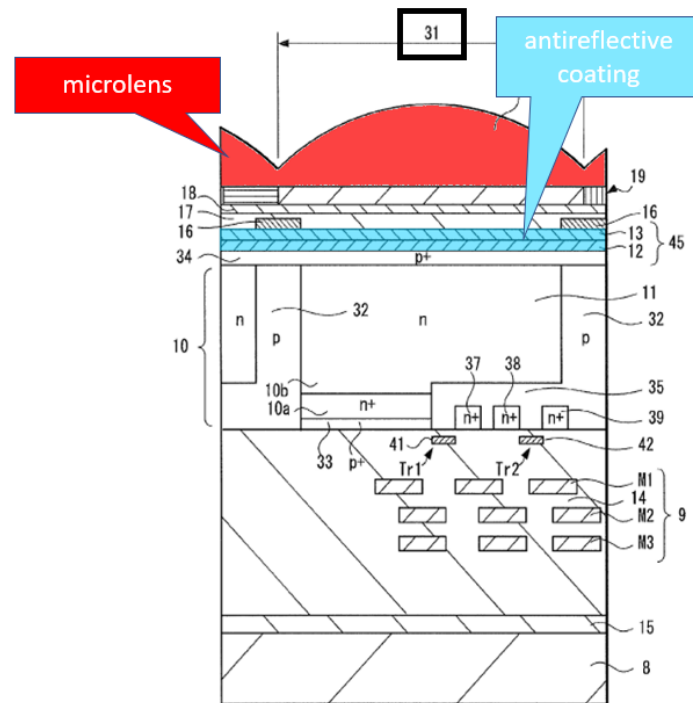
2. Claim 10

10. The BSI CMOS pixel array of claim 1 comprising a micro lens, said absorption area is between said micro lens and said barrier layer.

165. Claim 10 depends from claim 1. As discussed in Section IX.B.1 above, the Lauxtermann-Akiyamacombination discloses and/or renders obvious each element of claim 1 for the same reasons Lauxtermann alone discloses and/or renders obvious claim 1.

166. I am of the opinion that Lauxtermann combined with Akiyama’s disclosure render obvious claim 10’s further requirement of “a microlens” and that the “absorption area is between said micro lens and said barrier layer.”

167. It was highly conventional and very well-known that any BSI image sensor with a pixel array would include microlenses. *See, e.g.,* Ex. 1028, 1033-1036, 1059. Further, as shown in FIG. 4 below, Akiyama discloses a BSI CMOS image sensor with a **microlens 21** formed on the backside of a **pixel 31** and over a **photodiode 11**. Ex. 1006, FIG. 4; 5:6-30; 5:55-6:3.

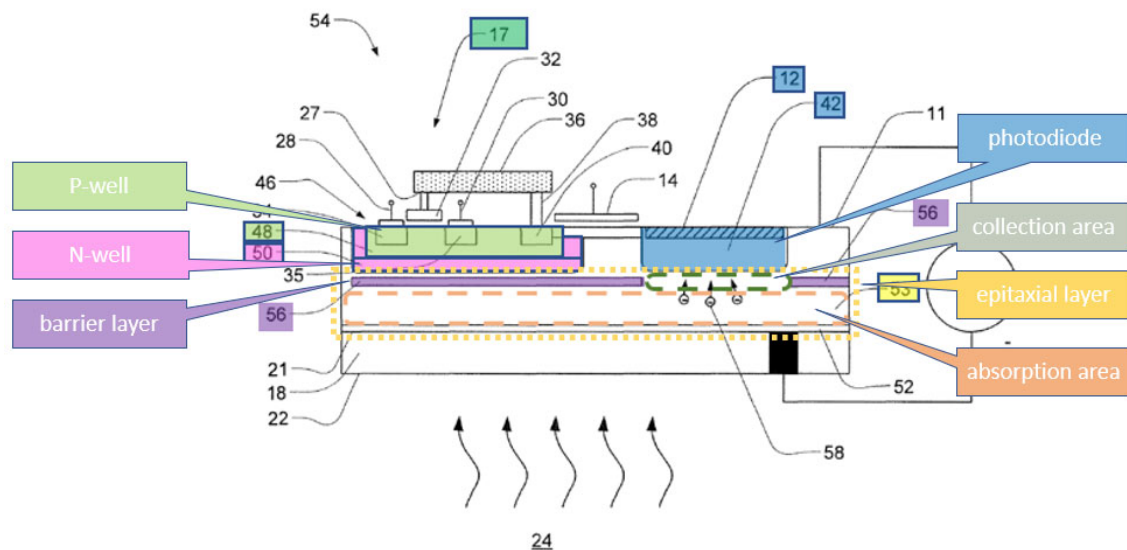


Ex. 1006, FIG. 4 (annotated).

168. As discussed above, a POSITA would be motivated to modify Lauxtermann's BSI CMOS image sensor (as shown in FIG. 4 below) in view of Akiyama to include a **microlens** to focus incident light on **photodiode 12** to improve the light collection efficiency of its image sensor. As discussed in Section III.C.3, microlenses have been widely employed in CMOS image sensors because

they focus light incident on the lens towards the corresponding photodiode, thereby improving the efficiency of the image sensor. *See* Ex. 1020, 1:6-11, 1:17-20.

169. Further, a POSITA would have placed the microlens before the outermost layer of Lauxtermann's image sensor die in the path of incident light 24 (i.e., below layer 18) because the function of the microlens is to focus incident light before the light enters the image sensor die. This is consistent with Akiyama's teachings, where its microlens 21 is located before the outmost layer of its image sensor in the light's path. Ex. 1006, FIG. 4. With this arrangement of the microlens in Lauxtermann's image sensor, the **absorption area in the combination of Lauxtermann and Akiyama is between the micro lens and the barrier layer** 56.



Ex. 1004, FIG. 4.

3. Claim 11

11. The BSI CMOS pixel array of claim 10 comprising an anti-reflective coating (ARC) layer, said ARC layer is between said micro lens and said absorption area.

170. Claim 11 depends from claim 1. As discussed in Section IX.B.1 above, the Lauxtermann-Akiyama combination discloses and/or renders obvious each element of claim 1 for the same reasons Lauxtermann alone discloses and/or renders obvious claim 1.

171. I am of the opinion that Lauxtermann combined with Akiyama's disclosure render obvious claim 11's further requirement of an ARC layer and that "ARC layer is between said micro lens and said absorption area."

172. It was highly conventional and very well-known that any BSI image sensor with a pixel array would include an ARC layer. *See, e.g.*, Ex. 1028, 1033-1036, 1059. Further, as shown in FIG. 4 below, Akiyama discloses an **antireflective coating (ARC) 45** formed on the backside of a **pixel 31**. Ex. 1006, FIG. 4; 5:6-30; 5:55-6:3.

173. As discussed above, a POSITA would be motivated to modify Lauxtermann's BSI CMOS image sensor (as shown in FIG. 4 above) in view of Akiyama to include an **ARC layer** between the microlens and photodiode to improve the light collection efficiency of its **photodiode 12**. An ARC layer allows more light to pass through from a microlens to a photodiode by minimizing

reflection from a component on the backside surface of the image sensor die and the silicon material of the backside surface itself, which would otherwise decrease the efficiency of the device. *See* Ex. 1021, [0013].

174. Further, a POSITA would have placed the ARC layer between the microlens and absorption area of Lauxtermann's image sensor because the ARC would allow more light to reach the photodiode by minimizing light reflection at the interface between a component on the backside surface of the image sensor die and the silicon material of the backside surface itself. This is consistent with Akiyama's teachings, where the ARC layer is placed after the **microlens 21** and before the backside of the image sensor die. Ex. 1006, FIG. 4. With this arrangement of the ARC layer and microlens in Lauxtermann's image sensor, **the ARC layer is between the microlens and the absorption area.**

E. Ground 4: Claims 16-20 Are Obvious Over Lauxtermann In View Of Wang

175. I am of the opinion that Lauxtermann in view of Wang render obvious claims 16-20 of the '169 patent.

1. Reasons to Combine Lauxtermann with Wang

176. As discussed above, Lauxtermann discloses or renders obvious all the limitations of claim 1. Claims 16 and 19 further requires certain peripheral circuitry, claims 17 and 18 further requires a guard ring, and claim 20 further requires that the image sensor be used in a digital camera or smartphone. Wang

teaches peripheral circuitry, guard ring, and digital camera that meet the requirements of these claims. A POSITA would have been motivated to modify Lauxtermann to include these teachings and would have had a reasonable expectation of success, for the following reasons.

177. ***Guard ring [claims 17, 18]:*** A POSITA would have been motivated to include a guard ring in Lauxtermann's BSI CMOS image sensor according to Wang's teaching to reduce crosstalk between neighboring pixels and between the pixel array and any peripheral circuitry. Without a guard ring 130, Wang discloses that scattered light would reach neighboring pixels 120, "causing crosstalk between various sensor signals." Ex. 1010, 1:51-54. Furthermore, without guard ring 130, Wang discloses light-generated charges from one pixel 120 may drift into other pixels 120 and peripheral circuitry, such as ASIC control circuit 184. Ex. 1010, 2:12-18; 3:23-26; 7:15-18; 8:10-13. In view of Wang, a POSITA would include a guard ring in Lauxtermann's BSI CMOS image sensor to reduce crosstalk between pixels and between the pixel array and any peripheral circuitry.

178. ***Peripheral circuitry [claim 16, 19]:*** Moreover, a POSITA would have been motivated to include peripheral circuitry in Lauxtermann's BSI CMOS image sensor according to Wang's teaching to access the pixels in the image sensor. A POSITA would have understood that charge accumulation in a pixel must be measured by a sensor, and that the measurements from a given pixel's sensor is

then used by other circuits to provide color and brightness information. Ex. 1030 at 1:38-41. There is nothing unique about BSI sensors in this regard. Indeed, Wang discloses “an image sensor 300, wherein an[] area 180 ... adjacent to a pixel forming area 182, includes a control circuit, e.g., an ASIC 184, that provides circuitry supporting pixels 120 and external communications to other devices.” Ex. 1010, 6:64-7:2. In view of Wang, a POSITA would include a control circuit ASIC in Lauxtermann’s BSI CMOS image sensor to access and otherwise support pixels.

179. A person of ordinary skill in the art would have been motivated to combine Lauxtermann and Wang for the following additional reasons:

180. ***Same field of endeavor:*** Like the ’169 patent, both Lauxtermann and Wang are directed to BSI CMOS image sensors and methods for improving the performances of the image sensors.

181. ***Reasonable expectation of success/predictable results:*** Designing Lauxtermann’s BSI CMOS image sensor to include a guard ring and peripheral circuitry according to Wang’s teachings would have been readily accomplished. A POSITA with knowledge of Lauxtermann would have naturally looked to the disclosures of Wang when finding ways to improve the efficiency of a BSI CMOS image sensor and to reduce crosstalk. A POSITA would have been motivated to include a guard ring and peripheral circuitry in Lauxtermann’s BSI CMOS image

sensor with at least a reasonable expectation of success because guard rings and peripheral circuitry are routinely used in BSI CMOS image sensors and it is very easy to add these additional elements during the fabrication process.

2. Claim 16

[16pre] A complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) comprising:

182. To the extent the preamble is limiting, I am of the opinion that the combination of Lauxtermann and Wang renders it obvious.

183. Lauxtermann teaches a **CMOS** pixel array for the reasons discussed in connection with Ground 1. *See* Section IX.B.1 (1pre). Lauxtermann teaches a CMOS image sensor with active pixel circuitry. Ex. 1004, 3:45-47, 4:16-17, 5:19-26. A POSITA would understand the active pixel circuitry is an integrated circuit with transistors formed on a semiconductor substrate in a CMOS fabrication process. Therefore, Lauxtermann teaches a **CMOS IC**.

[16a] a circuitry; and

184. The combination of Lauxtermann and Wang renders this limitation obvious.

185. It is well-known that an integrated circuit with a CMOS image sensor must comprise circuitry to access and readout the pixel array in the image sensor.

Therefore Lauxtermann's disclosed CMOS image sensor would necessarily include circuitry.

186. Further, Wang teaches that its ASIC forming area 180 includes an ASIC control circuit 184 (i.e., **circuitry**) "that provides circuitry supporting pixels 120 and external communications to other devices." Ex. 1010, 6:64-7:2.

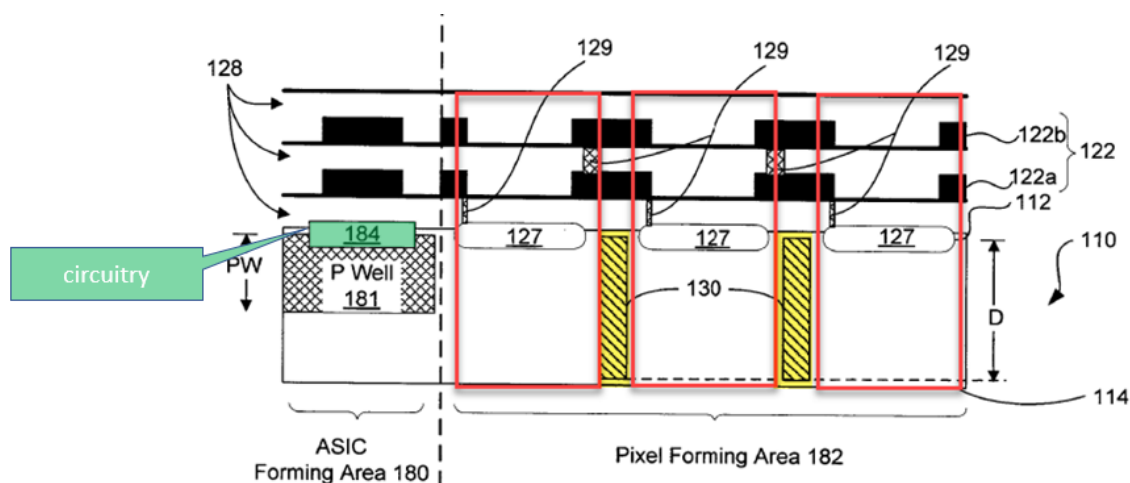


Fig. 4

[16b] a back-side illumination (BSI) pixel array comprising:

187. Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section IX.B.1 (1pre).

[16c] a plurality of pixels, a pixel of said plurality of pixels comprising:

188. Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section IX.B.1 (1a).

[16d] one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-Well (NW) region or a P-well (PW) region;

189. Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section IX.B.1 (1b).

[16e] a photodiode;

190. Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section IX.B.1 (1c).

[16f] an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to said absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and

191. Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section IX.B.1 (1d).

[16g] a barrier layer separating said absorption area from said well regions.

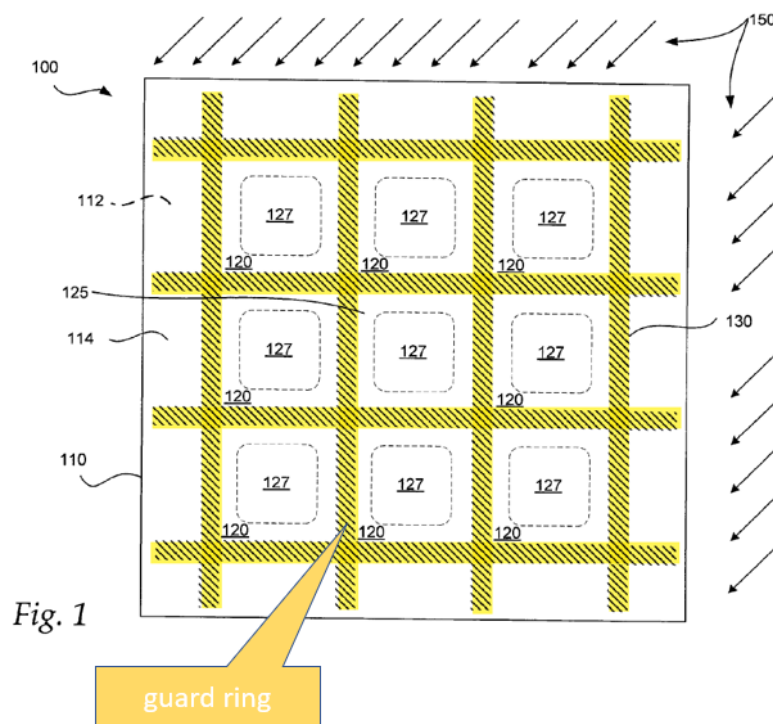
192. Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section IX.B.1 (1e).

3. Claim 17

17. The CMOS IC of claim 16 comprising a guard ring separating said circuitry from said BSI pixel array.

193. I am of the opinion that the combination of Lauxtermann and Wang renders this limitation obvious.

194. Wang teaches employing a **guard ring** 130 both to separate neighboring pixels 120 (as shown in its figures) and to isolate ASIC 184 (peripheral circuitry) from adjacent pixels 120 (as described). Ex. 1010, 2:16-18, 3:16-26; 4:3-5, 7:15-18; 8:10-13. The guard ring structure is shown in Wang's figures, highlighted in yellow:



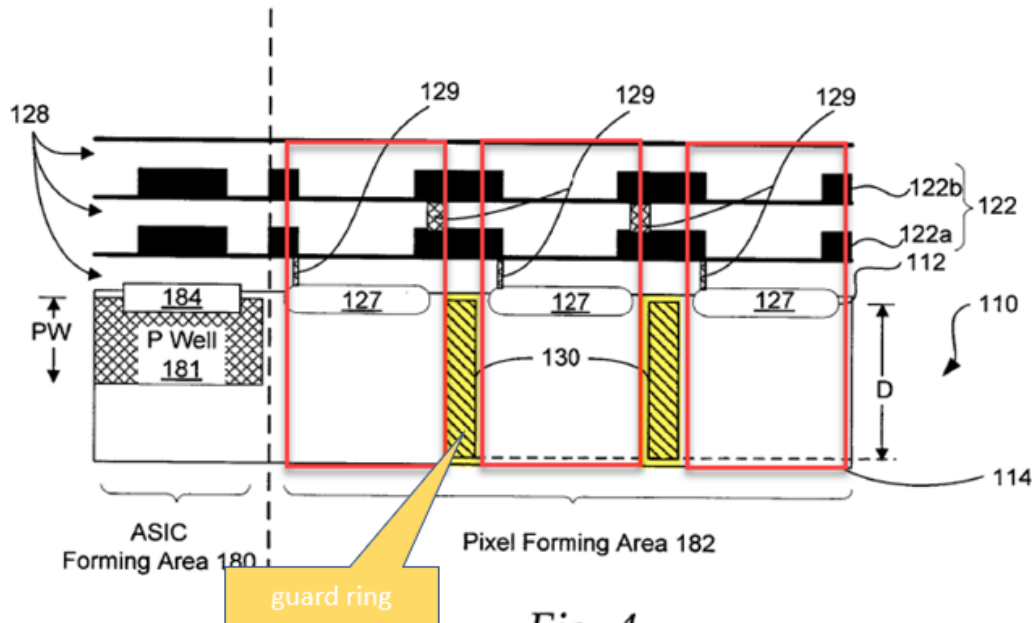


Fig. 4

195. Wang therefore teaches that the guard ring **separates said circuitry from said BSI pixel array**. It would have been obvious to include Wang's guard ring in Lauxtermann's BSI CMOS image sensor.

4. Claim 18

18. The CMOS IC of claim 17, wherein said guard ring is configured to prevent diffusion of photoelectrons from said circuitry to said BSI pixel array.

196. I am of the opinion that the combination of Lauxtermann and Wang renders this limitation obvious.

197. As discussed above in connection with claim 17, Wang discloses that the purpose guard ring 130 is to prevent light-generated charge carriers (i.e., **photoelectrons**) from reaching neighboring pixels 120 (i.e., pixels in the **BSI pixel array**). Ex. 10301010, 1:48-54. The guard ring 130 also isolates ASIC 184

(circuitry) from adjacent pixels 120 (BSI pixel array) (i.e., it is **configured to prevent diffusion of photoelectrons from said circuitry to said BSI pixel array**). Ex. 1010, 7:15-18; 8:10-13.

5. Claim 19

[19pre] An imaging device comprising:
--

198. To the extent the preamble is limiting, the combination of Lauxtermann and Wang renders it obvious.

199. Wang teaches that BSI sensors are useful in various applications, including “digital cameras.” Ex. 1010, 1:38-41. A digital camera is an **imaging device**. *See* Ex. 1052, 20:13-15 (referring to “an imaging device (camera)”).

[19a] a memory; an input; an output; a processor; and
--

200. The combination of Lauxtermann and Wang renders this limitation obvious.

201. Wang teaches the use of CMOS sensors in digital cameras. Ex. 1010, 1:38-41. A POSITA would understand that **a memory, an input, an output, and a processor** are necessarily components of a digital camera. At a minimum, it would have been obvious to a POSITA that a digital camera utilizing CMOS sensors would include these four components.

[19b] a complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) comprising:

202. The combination of Lauxtermann and Wang renders obvious this limitation for the reasons discussed in connection with claim 16. *See* Section IX.E.2 (16pre).

[19c] a circuitry; and

203. The combination of Lauxtermann and Wang renders obvious this limitation for the reasons discussed in connection with claim 16. *See* Section IX.E.2 (16a).

[19d] a back-side illumination (BSI) pixel array comprising:

204. Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section IX.B.1 (1pre).

[19e] a plurality of pixels, a pixel of said plurality of pixel sensors comprising:

205. Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section IX.B.1 (1a).

[19f] one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-Well (NW) region or a P-well (PW) region;

206. Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section IX.B.1 (1b).

[19g] a photodiode;

207. Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section IX.B.1 (1c).

[19h] an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to said absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and

208. Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section IX.B.1 (1d).

[19i] a barrier layer separating said absorption area from said well regions.

209. Lauxtermann teaches this limitation for the reasons discussed in connection with Ground 1. *See* Section IX.B.1 (1e).

6. Claim 20

20. The imaging device of claim 19 comprising a digital camera or a Smartphone.

210. The combination of Lauxtermann and Wang renders this limitation obvious. Wang teaches the use of BSI sensors in **digital cameras**. Ex. 1010, 1:38-41.

F. Ground 5: Claims 1, 3-8, And 12-15 Are Obvious In View Of Ballin

211. I am of the opinion that Ballin renders obvious claims 1, 3-8, and 12-15 of the '169 patent.

1. Claim 1

[1pre] A back-side illumination (BSI) complementary metal-oxide-semiconductor (CMOS) pixel array comprising:

212. To the extent the preamble is considered to be a limitation, I am of the opinion that Ballin discloses a BSI CMOS pixel array.

213. Ballin discloses its monolithic active pixel sensors (MAPS) include CMOS pixels, and the image sensor can be “back-illuminated sensors.” Ex.

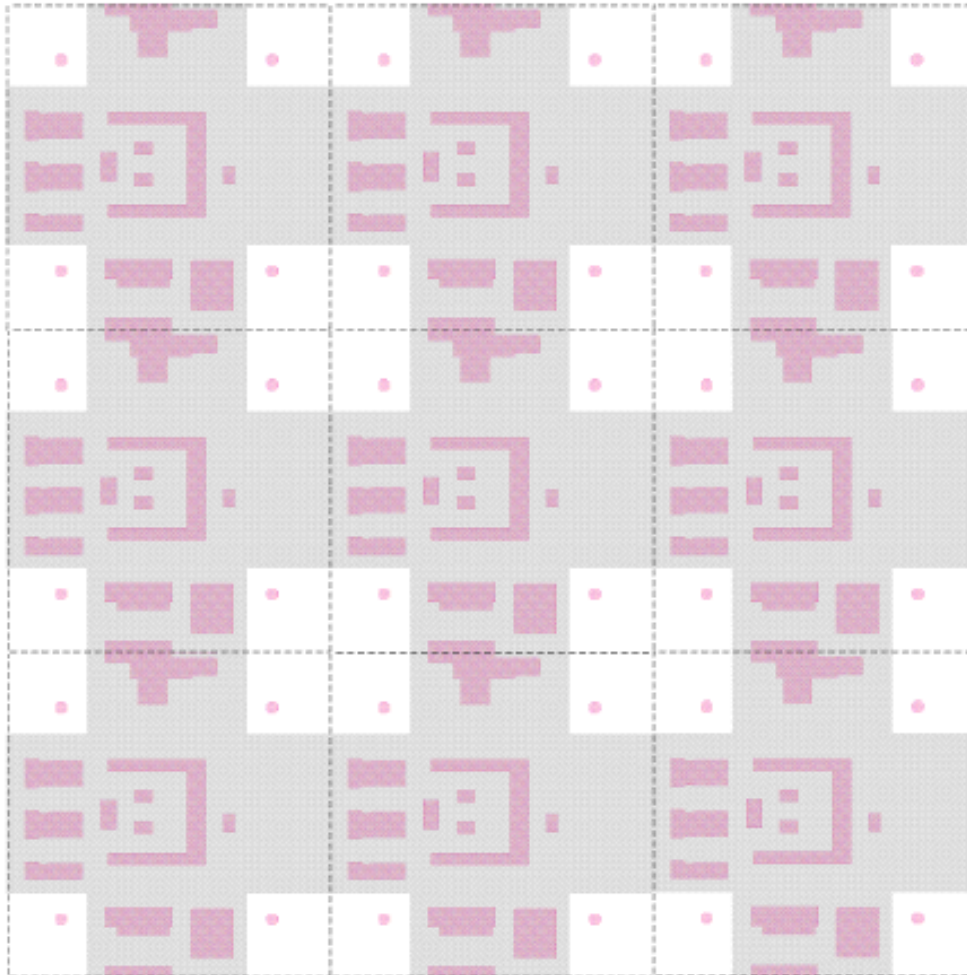
1007, Title, 5339, FIG. 2. Ballin’s FIG. 2 illustrates one pixel of a BSI CMOS image sensor, where each pixel includes at least a photodiode and an NMOS transistor, a PMOS transistor, and a deep P-well implant in an epitaxial layer. Ex. 1007, 5338-39, FIG. 2.

[1a] a plurality of pixels, a pixel of said plurality of pixels comprising:

214. I am of the opinion that Ballin discloses a plurality of pixels.

215. Ballin’s FIG. 5 (below) illustrates that that its BSI CMOS pixel array comprises a plurality of pixels, particularly a 3x3 pixel array:

Figure 5. Layout of a 3x3 array of *preShape* pixel from the TPAC1.0 sensor. Only the N-well (purple) and deep P-well (grey) layers are shown. Every N-well but the detecting diodes have got deep P-well underneath. The non-physical boundary between pixels is shown as a dotted line.

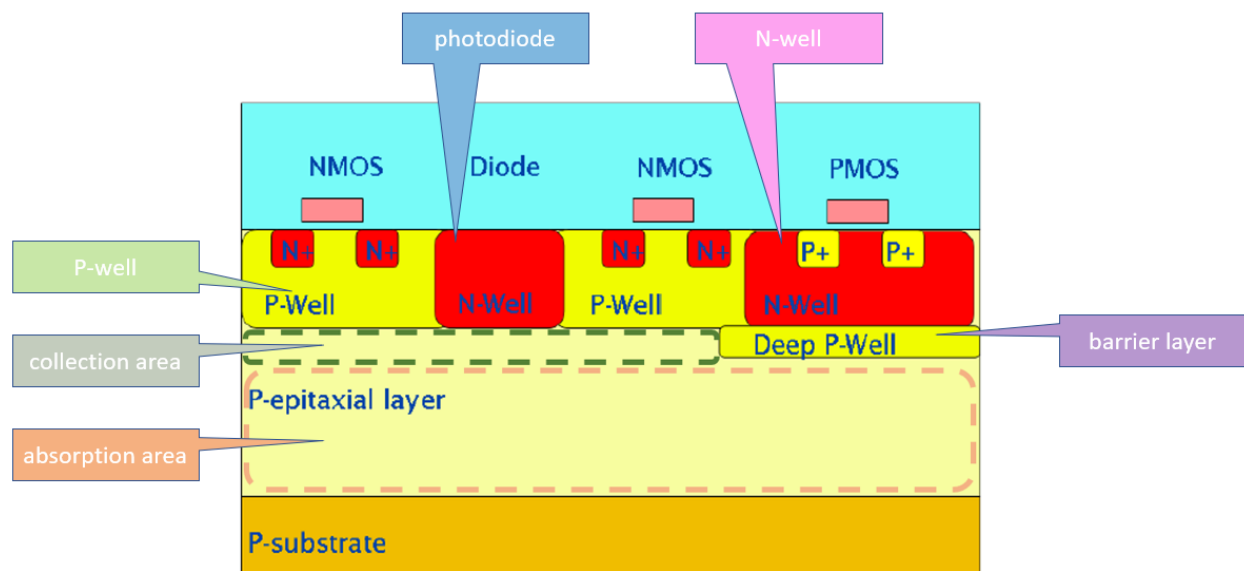


Ex. 1007, FIG. 5.

[1b] one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-Well (NW) region or a P-well (PW) region;

216. I am of the opinion that Ballin discloses one or more MOS transistors with N-well or P-well regions.

217. Ballin discloses that a pixel of its BSI CMOS image sensor includes at least two **NMOS transistors** and a **PMOS transistor**. Ex. 1007, FIG. 2, 5338, 5340.



Ex. 1007, FIG. 2 (annotated).

218. As shown in FIG. 2 above, Ballin discloses that its two NMOS transistors are formed with two **P-well regions** and a PMOS transistor is formed with an **N-well region**. *Id.*, 5338.

[1c] a photodiode;

219. I am of the opinion that Ballin discloses a photodiode.

220. Ballin discloses that a pixel of its BSI CMOS image sensor includes a least one N-well diode (i.e., **photodiode**) and teaches that pinned **photodiodes** have been used in CMOS sensors. Ex. 1007, Fig. 2, 5337-38.

[1d] an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and

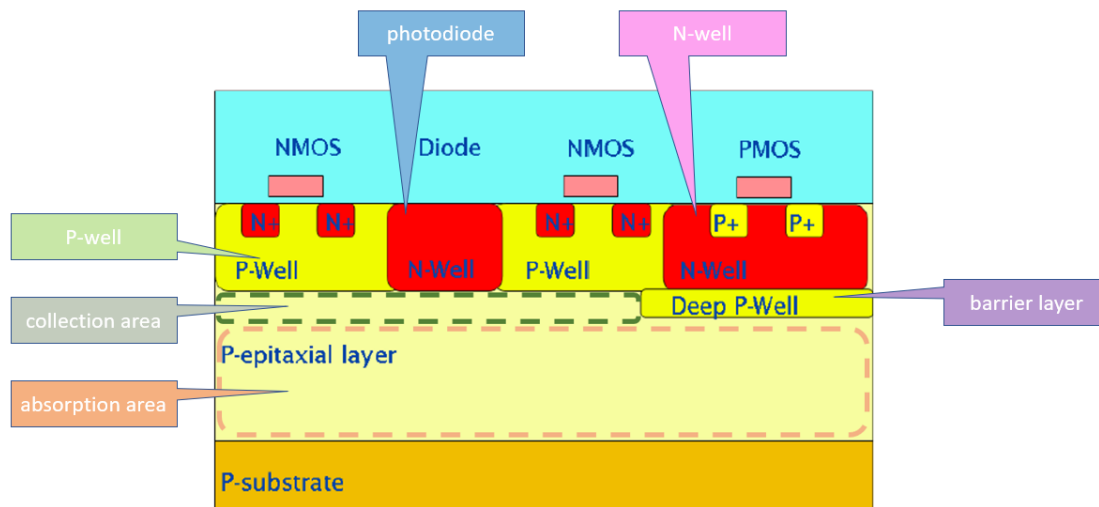
221. I am of the opinion that Ballin renders obvious claim 1d's requirement of "an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode."

222. *An epitaxial layer:* Ballin discloses that a pixel of its image sensor includes "a P-doped **epitaxial layer** . . . whose thickness is typically up to 20 μm ." Ex. 1007, FIG. 2, 5338.

223. *Comprising an absorption area and a collection area:* The annotated FIG. 2 below discloses an epitaxial layer that includes an **absorption area** and a **collection area**,³ the latter of which connects the absorption area to a photodiode. Just like absorption area 222 in Figure 2 of the '169 patent, the identified **absorption area** in Ballin is a part of the epitaxial layer generally located below

³ According to the plain language of the claims, absorption *area* and collection *area* are part of the epitaxial *layer*. They need not be separate layers.

the deep p-wells (barrier) of the pixels. Just like connection area 224 in Figure 2 of the '169 patent, the identified **collection area** in Lauxtermann is a part of the epitaxial layer generally located adjacent to the **deep p-wells (barriers)** and under the **photodiode**.



Ex. 1007, FIG. 2 (annotated).

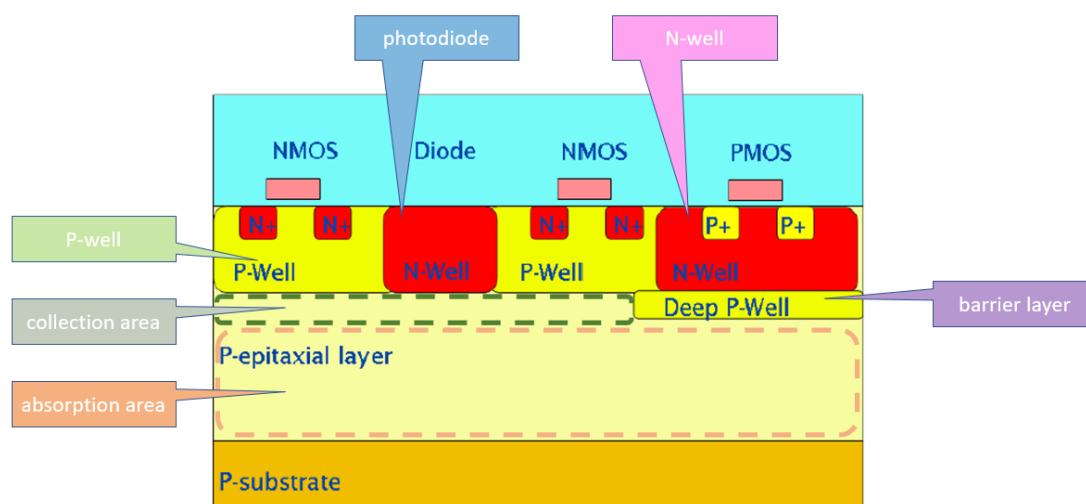
224. The absorption area is configured **to absorb incoming photons** (from light incident on the P-substrate) and **generate charges** (i.e., electrons) **by means of the photoelectric effect**. Just like the absorption area 222 in Figure 2 of the '169 patent, the identified **absorption area** in Ballin is a part of **P-epitaxial layer** generally located below **deep P-wells (barriers)**. The **collection area** connects the **absorption area** to the **photodiode** to provide the collected charges to the **photodiode**. A POSITA would understand that the collection area collects the charges from the absorption area and funnels them towards the photodiode in conjunction with the deep P-wells (since the deep P-wells repel the

charges). And just like the collection area 224 in Figure 2 of the '169 patent, the identified **collection area** in Ballin is a part of **P-epitaxial layer** generally located adjacent to **deep P-wells (barriers)** (e.g., between them) and under the **photodiode**.

[1e] a barrier layer separating said absorption area from said one or more well regions.

225. I am of the opinion that Ballin renders obvious claim 1e's requirement of "a barrier layer."

226. Particularly, Ballin discloses that a "novel approach for isolating the N-wells of PMOS transistors from the epitaxial layer ... by adding a **deep P implant**," and that "[b]y adding the **deep P-well layer underneath all the N-wells used as substrate for PMOS transistors**, it is then possible to keep the collecting PN diode junction [i.e., **photodiode**] as the only one in the pixel that is exposed to the epitaxial layer." Ex. 1007, 5339-40, FIG. 2 (annotated below).



Ex. 1007, FIG. 2 (annotated).

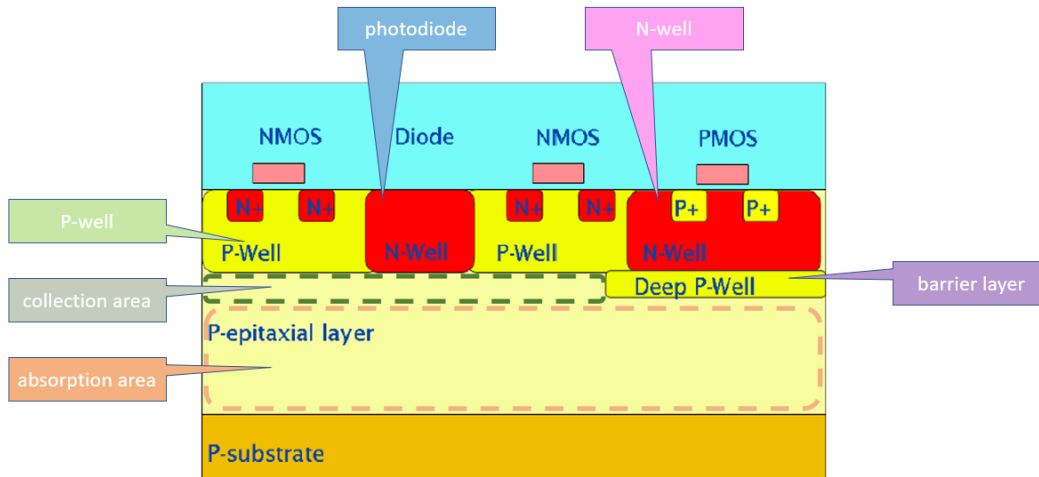
227. As shown in FIG. 2, Ballin's deep P-well separates the **N-wells** of the PMOS transistors from the P-epitaxial layer, which comprises the **collection** and **absorption** areas. A POSITA would understand that Ballin's deep P-well implant is a **barrier layer** separating the **absorption area** from the one or more well regions.

2. Claim 3

3. The BSI CMOS pixel array of claim 1, wherein said **collection area** extends from said **absorption area** to said photodiode through said **barrier layer**.

228. I am of the opinion that Ballin renders obvious claim 3's requirement the "collection area extends from said absorption area to said photodiode through said barrier layer."

229. As discussed above, Ballin's **collection area** extends from the **absorption area** to the photodiode (N-well diode) through the **barrier layer** (deep P-well implant). Ex. 1007, FIG. 2.



Ex. 1007, FIG. 2 (annotated).

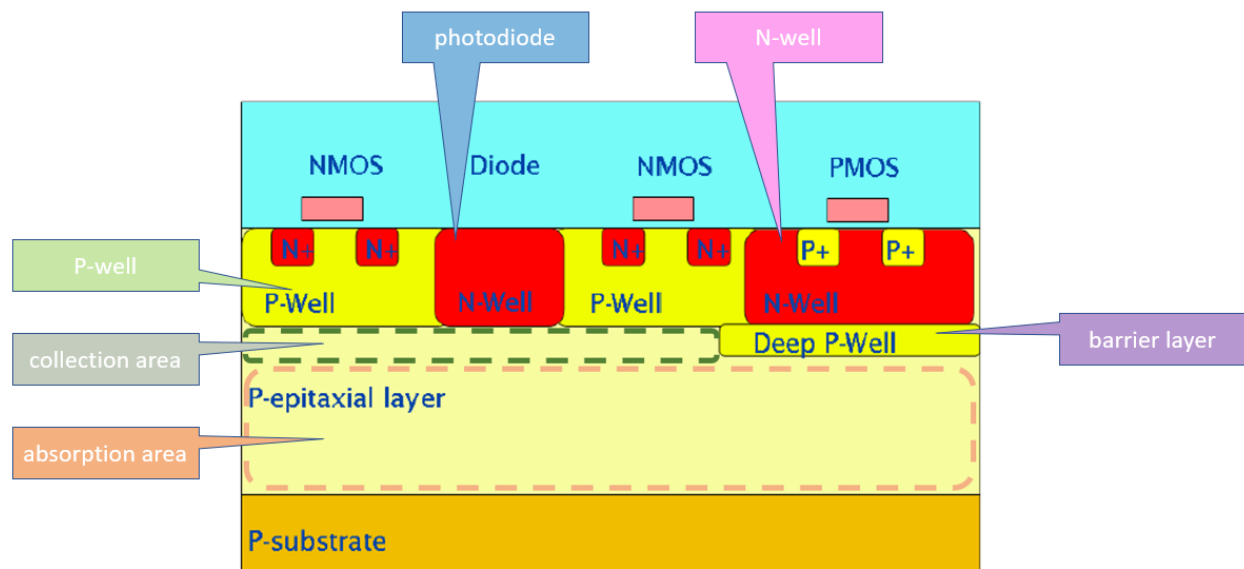
3. Claim 4

4. The BSI CMOS pixel array of claim 1, wherein said collection area is configured to perform the functionality of an electrostatic lens to collect said electrons from said absorption area.

230. I am of the opinion that Ballin renders obvious claim 4's requirement the "collection area is configured to perform the functionality of an electrostatic lens to collect said electrons from said absorption area." As known in the art, an electrostatic lens creates an electric field to guide electrons towards a detector. Exs. 1016; 1057, 6:11-12, 6:65-7:5.

231. It would have been obvious to a POSITA that the area below the N-well diode and below the P-wells (the area in between the deep P-wells, which functions as a **barrier layer**) serves as a **collection area** collecting electrons from the **absorption area** and then guides/directs the collected electrons to the **photodiode** (N-well diode). Ballin's **collection area** is configured to perform as an

electrostatic lens because the deep P-wells create electric fields that cause the **collection area** to become an electron funnel that collects and guides electrons to the **photodiode**. *Id.* This is the functionality of the electrostatic lens according to the '169 patent. Ex. 1001, 7:23-32. Therefore, Ballin's **collection area** is configured to perform the functionality of **an electrostatic lens**.



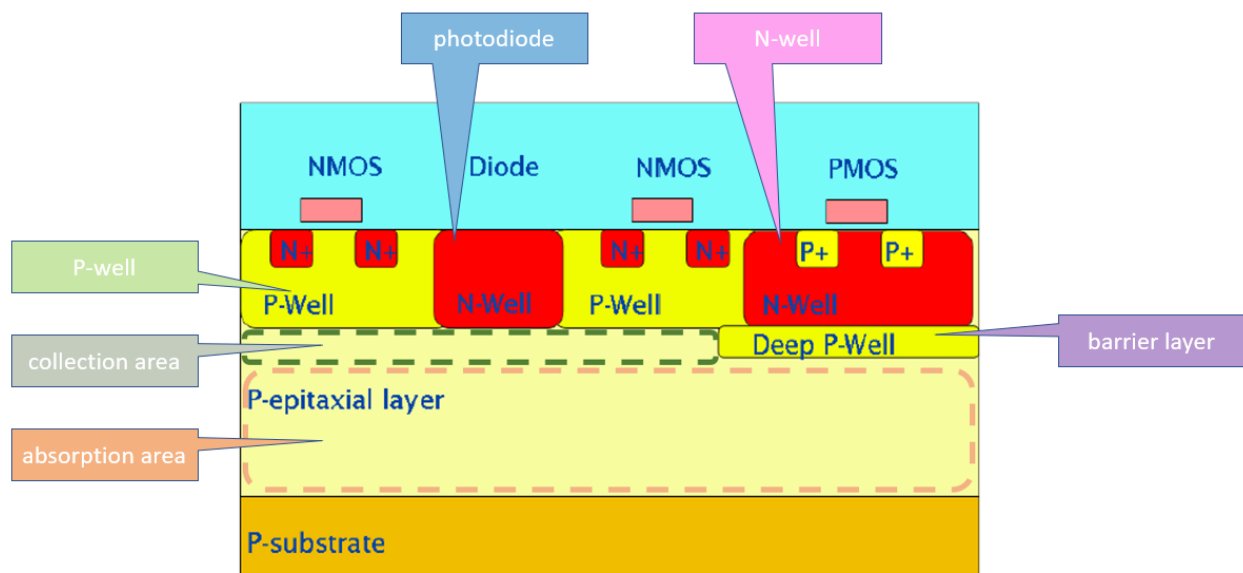
Ex. 1007, FIG. 2 (annotated).

4. Claim 5

5. The BSI CMOS pixel array of claim 1, wherein said barrier layer is configured to prevent diffusion of said electrons from said absorption area to said well regions.

232. I am of the opinion that Ballin discloses claim 5's requirement that the "barrier layer is configured to prevent diffusion of said electrons from said absorption area to said well regions."

233. Ballin proposes a “novel approach for isolating the N-wells of PMOS transistors from the epitaxial layer ... by adding a **deep P implant**,” and that “[b]y adding the **deep P-well layer underneath all the N-wells** used as substrate for PMOS transistors, it is then possible to keep the collecting PN diode junction [i.e., photodiode] as the only one in the pixel that is exposed to the epitaxial layer.” Ex. 1007, 5339-40, FIG. 2. This deep P-well is **configured to prevent diffusion of electrons from the absorption area to the well regions** because without it, charges would diffuse towards the N-well region of the PMOS above. A POSITA would understand that Ballin’s deep P-well implant is the claimed **barrier layer**.



Ex. 1007, FIG. 2 (annotated).

5. Claim 6

6. The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 4 micron (μm).

234. I am of the opinion that Ballin discloses claim 6's requirement that the "thickness of said epi layer is at least 4 micron (μm)."

235. Ballin discloses that its P-doped epitaxial layer has a thickness "typically **up to 20 μm .**" Ex. 1007, 5338. Ballin therefore discloses that **a thickness of its epi layer is at least 4 micron (μm).**

6. Claim 7

7. The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 10 micron (μm).

236. I am of the opinion that Ballin discloses claim 7's requirement that the "thickness of said epi layer is at least 10 micron (μm)."

237. Ballin discloses that its P-doped epitaxial layer has a thickness "typically **up to 20 μm .**" Ex. 1007, 5338. Ballin therefore discloses that **a thickness of its epi layer is at least 10 micron (μm).**

7. Claim 8

8. The BSI CMOS pixel array of claim 1, wherein a thickness of said epi layer is at least 15 micron (μm).

238. I am of the opinion that Ballin discloses claim 8's requirement that the "thickness of said epi layer is at least 15 micron (μm)."

239. Ballin discloses that its P-doped epitaxial layer has a thickness “typically **up to 20 μm .**” Ex. 1007, 5338. Ballin therefore discloses that **a thickness of its epi layer is at least 15 micron (μm).**

8. Claim 12

12. The BSI CMOS pixel array of claim 1, wherein said one or more MOS transistors comprise one or more transistors selected from a group consisting of one or more P-type MOS (PMOS) transistors and one or more N-type MOS (NMOS) transistors.

240. I am of the opinion that Ballin discloses claim 12’s requirement that the “MOS transistors comprise one or more transistors selected from a group consisting of one or more P-type MOS (PMOS) transistors and one or more N-type MOS (NMOS) transistors.”

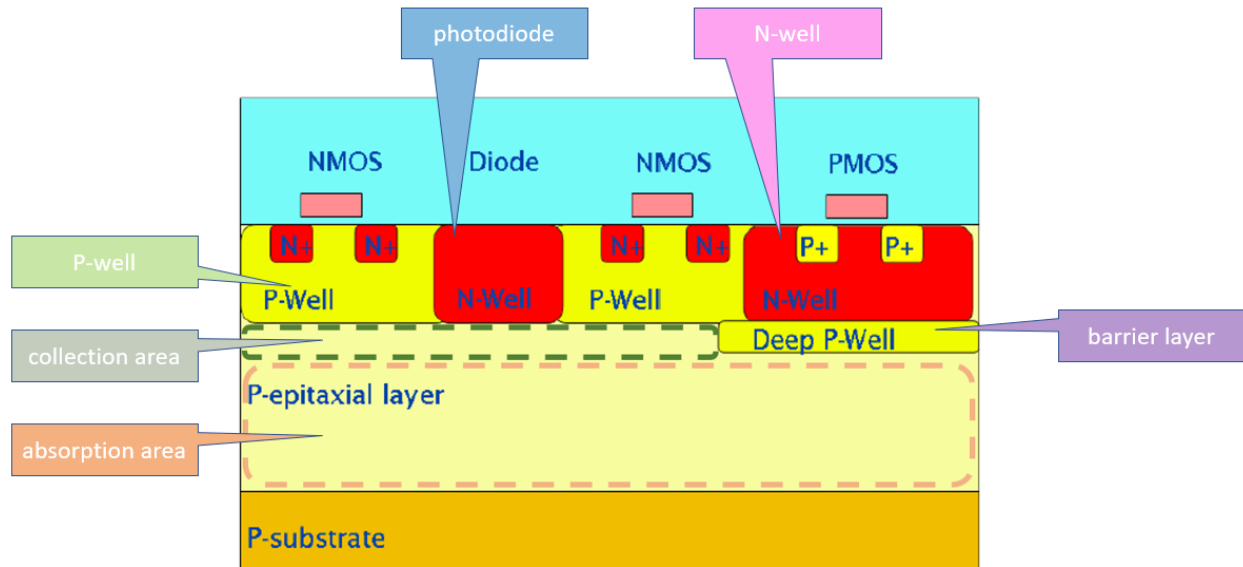
241. Ballin discloses that each pixel of its image sensor may include at least two NMOS transistors and one PMOS transistor. Ex. 1007, FIG. 2, 5340. Ballin therefore discloses **one or more transistors selected from a group consisting of one or more P-type MOS (PMOS) transistors and one or more N-type MOS (NMOS) transistors.**

9. Claim 13

13. The BSI CMOS pixel array of claim 1, wherein said barrier layer comprises a deep PW implant.

242. I am of the opinion that Ballin discloses claim 13’s requirement that the “barrier layer comprises a deep PW implant.”

243. Ballin discloses that each pixel of its image sensor includes a “**deep P-well implant**” located underneath the N-well that acts as a barrier layer. Ex. 1007, FIG. 2, 5340. A “PW” implant is a “p-well” implant according to the ’169 patent. Ex. 1001, 4:30-32, 9:20-21, 9:52-56, FIGs. 3C-3D.



Ex. 1007, FIG. 2 (annotated).

10. Claim 14

14. The BSI CMOS pixel array of claim 1, wherein said barrier layer comprises a boron implant.

244. Ballin renders obvious claim 14’s requirement the “barrier layer comprises a boron implant.”

245. Ballin discloses that its pixel includes a **deep P-well implant** (i.e., **barrier layer**) underneath each PMOS N-well in the pixel. Ex. 1007, FIG. 2, 5339-40. A POSITA would understand boron is the most common p-type dopant.

See Ex. 1024, 467; Ex. 1025, 31; Ex. 1026, 4:24-30; Ex. 1027, [0059], [0106], [0107]. Thus, it would have been obvious to a POSITA to use **boron implant** for Ballin's deep P-well implant.

11. Claim 15

15. The BSI CMOS pixel array of claim 1, wherein said photodiode comprises a fully pinned diode.

246. I am of the opinion that Ballin renders obvious claim 15's requirement the "photodiode comprises a fully pinned diode."

247. As discussed above, a POSITA would have understood that when a photodiode is referred to as "pinned," that photodiode is **fully pinned**. See Ex. 1028, Ex. 1029, Fig. 2. It was well-known at the time of the '169 patent that pinned photodiodes were used in almost all CCD and CMOS image sensors. Ex. 1028, Abstract, 34.

248. Ballin discloses that each pixel includes an N-well diode (i.e. photodiode). Ex. 1007, FG. 2. Ballin further discloses that as pixels are fabricated in smaller and smaller sizes, "electronic noise and leakage current have had to be greatly improved, in particular through the introduction of **pinned photodiode** and transfer gates." *Id.*, 5337. And it was well-known that fully pinned photodiodes have low noise, high quantum efficiency and low dark current. Ex. 1028, p. 33. Therefore, it would have been obvious for a POSITA to use a **fully pinned diode** for Ballin's N-well diode, as opposed to a partially or non-pinned photodiode, to

reduce electronic noises and dark currents and improve the quantum efficiency of its image sensors.

G. Ground 6: Claims 10 And 11 Are Obvious Over Ballin In View Of Akiyama

249. I am of the opinion that Ballin in view of Akiyama render obvious claims 10 and 11 of the '169 patent.

1. Reasons to Combine Ballin with Akiyama

250. As discussed above, Ballin discloses or renders obvious all the limitations of claim 1. Claim 10 further requires a microlens and claim 11 further requires antireflective coating (ARC) layer. Akiyama teaches both a microlens and an ARC layer. A POSITA would have been motivated to include a microlens and an ARC in Ballin's BSI CMOS image sensor according to Akiyama's teachings to improve the efficiency of its image sensor.

251. *Microlens [claim 10] and ARC layer [claim 11]*: A POSITA would have understood that microlens arrays are widely used in CCD and CMOS image sensors so that light incident on each microlens is focused towards a corresponding photodiode. A POSITA would also have understood that ARC allows more light to pass through from a microlens to a photodiode by minimizing reflection caused by the difference in refractive indices of components on the light-receiving surface (i.e., backside) of the image sensor die, which would otherwise decrease the efficiency of the image sensor. Thus, a POSITA would have been motivated to

incorporate a microlens and an ARC into Ballin's image sensor according to Akiyama's teachings to improve light collection efficiency of its image sensor.

252. A person of ordinary skill in the art would have been motivated to combine Ballin and Akiyama for the following additional reasons:

253. *Same field of endeavor*: Like the '169 patent, both Ballin and Akiyama are directed to BSI CMOS image sensors and methods for improving the performances of the image sensors. Ballin and Akiyama disclose BSI CMOS image sensors that have very similar structures with each other. For example, both Ballin and Akiyama disclose that each pixel of their image sensors integrates a photodiode and at least one transistor for image processing. Both include a photodiode implanted in a semiconductor/epitaxial layer, which generates electric charges from light and collects the charges to be transferred to the photodiode. Both include a least one transistor implanted in a well region adjacent to a photodiode. And both employ a p-type barrier layer/isolation region to prevent the electric charges from diffusing to components other than the photodiode.

254. *Reasonable expectation of success/predictable results*: Designing Ballin's CMOS image sensor to include a microlens and an ARC according to Akiyama's teachings would have been readily accomplished. A POSITA would have been motivated to include a microlens and an ARC in Ballin's CMOS image sensor with at least a reasonable expectation of success because microlenses and

ARCs are routinely used in image sensors and it is very easy to add an ARC layer above Ballin's photodiode and then a microlens array above the ARC layer in the fabrication process.

2. Claim 10

10. The BSI CMOS pixel array of claim 1 comprising a micro lens, said absorption area is between said micro lens and said barrier layer.

255. Claim 10 depends from claim 1. As discussed in Section IX.B.1 above, the Ballin-Akiyama combination discloses and/or renders obvious each element of claim 1 for the same reasons Lauxtermann alone discloses and/or renders obvious claim 1.

256. I am of the opinion that Ballin combined with Akiyama's disclosure render obvious claim 10's further requirement of "a microlens" and that the "absorption area is between said micro lens and said barrier layer."

257. Akiyama discloses the microlens for the same reasons discussed in Ground 3. *See* Section IX.D.2. A POSITA would have placed the microlens before Ballin's image sensor die in the light's path (i.e., below the P-substrate) because the function of a microlens is to focus incident light before the light enters the image sensor die.

3. Claim 11

11. The BSI CMOS pixel array of claim 10 comprising an anti-reflective coating (ARC) layer, said ARC layer is between said micro lens and said absorption area.

258. Claim 11 depends from claim 1. As discussed in Section IX.B.1 above, the Ballin-Akiyama combination discloses and/or renders obvious each element of claim 1 for the same reasons Lauxtermann alone discloses and/or renders obvious claim 1.

259. I am of the opinion that Lauxtermann combined with Akiyama's disclosure render obvious claim 11's further requirement of an ARC layer and that "ARC layer is between said micro lens and said absorption area."

260. Akiyama discloses the ARC lens for the same reasons discussed in Ground 3. *See* Section IX.D.3.

261. A POSITA would have placed the ARC layer after the microlens but before the backside of Ballin's image sensor die in the light's path (i.e., above the microlens and below the p-substrate) because the ARC allows more light from the microlens to pass through and reach the photodiode by reducing reflections between a component on the backside and the silicon material of the backside surface itself.

X. CONCLUSION

262. For the aforementioned reasons, in my opinion, to a person of ordinary skill in the art, the Challenged Claims of the '169 patent are invalid in view of the prior art.

263. I understand that the Patent Owner has not asserted secondary considerations of non-obviousness. I reserve the right to respond to any such assertions.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on the information and belief are believed to be true; I declare under penalty of perjury that the foregoing is true and correct, and understand that willful false statements and the like are punishable by fine or imprisonment, or both pursuant to 18 U.S.C. 1001.

Date: December 16, 2022

Respectfully Submitted

A handwritten signature in black ink, appearing to read 'Konstantinos P. Giapis', written in a cursive style.

Dr. Konstantinos P. Giapis