

A Low Noise Pixel Architecture for Scientific CMOS Monolithic Active Pixel Sensors

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Abstract—This paper presents the design and characterisation of FORTIS (4T Test Image Sensor), which is a low noise, CMOS monolithic active pixel sensor for scientific applications. The pixels present in FORTIS are based around the four transistor (4T) pixel architecture, which is already widely used in the commercial imaging community. The sensor design contains thirteen different variants of the 4T pixel architecture to investigate the effects of changing its core parameters. The variants include differences in the pixel pitch, the diode size, the in-pixel source follower, and the capacitance of the floating diffusion node (the input node of the in-pixel source follower). Processing variations have also been studied, which include varying the resistivity of the epitaxial layer and investigating the effects of a special deep p-well layer. By varying these parameters, the 4T pixel architecture can be optimised for scientific applications where detection of small amounts of charge is required.

I. INTRODUCTION

THE scientific community often requires advanced image sensors, where the requirements can include high sensitivity, low noise, high charge collection efficiency and a tolerance to radiation. CMOS Monolithic Active Pixel Sensors (MAPS) can achieve these requirements.

Low noise and high sensitivity are of concern in applications where detection of small amounts of charge is required. One example of this is in high energy physics, where charge from minimum ionising particles (MIPs) needs to be detected for determining the rate and/or the position of the particles. If the noise level is too high, the MIP (typically a few hundred electrons) will go undetected. The sensitivity is related to the conversion gain of the pixel (the number of volts generated per electron), which if low, a MIP will not produce enough signal to be successfully read by the rest of the circuitry.

Charge collection efficiency should also be considered when determining whether a technology is suitable for the desired application. If complex in-pixel circuitry is required, then it is desirable to use both PMOS and NMOS transistors. However, due to the fabrication of PMOS transistors inside n-wells, secondary charge collection areas form, reducing the amount of charge collected by the diode.

Charge collection efficiency is also degraded by crosstalk effects. Charge generated far away from the diode will diffuse within the epitaxial layer and may not be collected by the pixel

closest to where it was generated. This can lead to a reduced timing resolution and charge spreading across multiple pixels. In the field of particle physics, this problem can disguise the actual location of where a MIP hit, as well as decreasing the charge available to be detected by the pixel which it actually hit, which if teamed with high noise, can leave the MIP undetected. In the colour imaging world, crosstalk between pixels can lead to blurring of colours, which requires often complex correction techniques to be incorporated off-chip.

We have been developing a novel process called INMAPS [1]. INMAPS is a 0.18 μm CMOS Image Sensor process which addresses the issues of poor charge collection efficiency and crosstalk. We have also been investigating the four transistor (4T) pixel architecture for low noise and high conversion gain to give increased sensitivity to small amounts of charge. Both of these developments are demonstrated in FORTIS (4T Test Image Sensor). FORTIS is shown in Fig. 1, and explores several geometric variants of the 4T pixel under different processing conditions to optimise the architecture for low noise and high conversion gain. The pitch of the pixel was also investigated, as scientific applications generally require larger pixels to increase the total amount of charge collected at the cost of a reduced resolution.

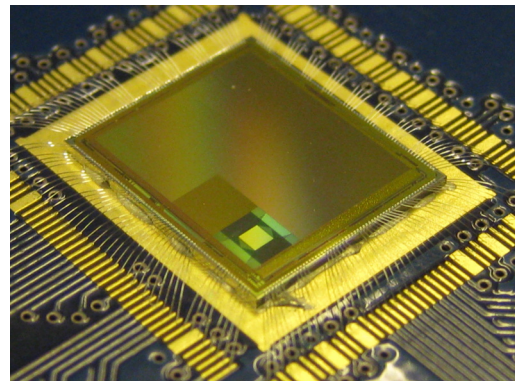


Fig. 1. The FORTIS 1.0 sensor

The contents of this paper is as follows. Section II will discuss the technologies involved in the INMAPS process and the 4T pixel architecture. Section III will discuss the FORTIS sensor developed using these technologies, and Section IV will present results from FORTIS, showing the benefits of these technologies. Results from radiation hardness tests will also be shown. Finally, the findings from FORTIS will be summarised in Section V.

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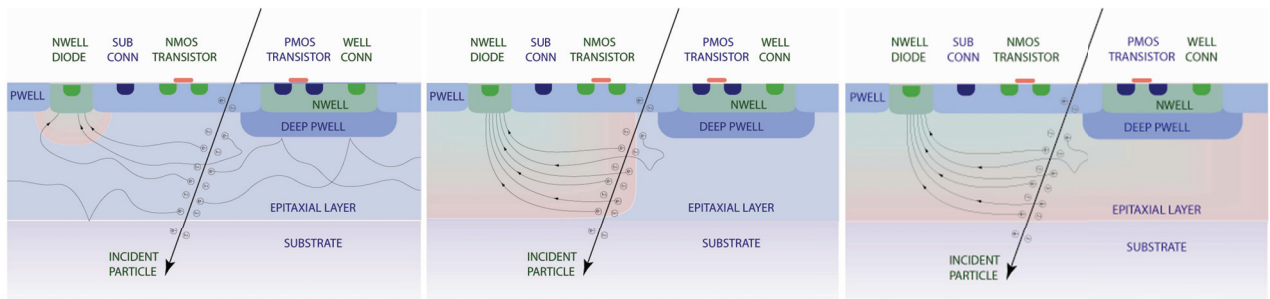


Fig. 2. Illustration of the depletion region width (pink) versus resistivity. From left to right: standard resistivity silicon, higher resistivity silicon, full depletion of epitaxial layer (ideal case). The deep p-well implant is also shown underneath the PMOS transistors, preventing charge from being collected by the n-wells in which they are situated.

II. TECHNOLOGIES

Improvements in the detection capabilities of MAPS devices can be implemented via careful tailoring of the resistivity of the epitaxial layer and the process used, or via the use of advanced pixel architectures. This section describes the technologies developed by us and implemented in FORTIS.

A. The INMAPS 0.18 μm Process

The INMAPS process is a 0.18 μm CMOS Image Sensor process developed in conjunction with a leading CMOS image sensor foundry. The process contains a special deep p-well layer for improved charge collection efficiency. This process has already been documented and will not be discussed in detail here [1]–[3].

A recent addition to the INMAPS process is the option to fabricate on a high resistivity epitaxial layer.

The resistivity of the epitaxial layer in which the CMOS pixel is manufactured defines, for a given bias voltage, the depth of the depletion region from the n-type implant which creates the diode. Standard epitaxial layer resistivity is between 10-100 Ωcm [4].

When electron-hole pairs are generated within silicon, the electrons will typically diffuse through the epitaxial layer. If they diffuse to a location sufficiently close to the depletion region of the diode, they will be collected. If an electron is generated far away from the diode, it will travel within the epitaxial layer for a longer distance compared to an electron generated close to the diode. This can lead to crosstalk between pixels, and degrade the magnitude of the signal collected, especially when only a small, finite amount of charge is present, for example, such as that generated by a MIP.

The depletion region width increases with increasing epitaxial layer resistivity. In the ideal case, the entire epitaxial layer would be depleted, changing the main charge transport mechanism from diffusion to drift and increasing the charge collection speed. This in turn increases the charge collection efficiency, reduces the crosstalk, reduces the image lag and increases the tolerance to radiation in situations where the minority carrier lifetime has been reduced, such as by bulk damage [5].

The resistivity of the silicon is inversely proportional to the doping concentration, so silicon with a doping concentration

close to the intrinsic level of silicon (10^{10} cm^{-3}) has the highest resistivity. Typical resistivities of high resistivity silicon are between 1-10 Ωcm [4], [6]. For a resistivity of this order, epitaxial layer thicknesses up to 20 μm may be fully depleted for the biasing voltages available in CMOS technology.

Fig. 2 shows the difference in depletion region depth for standard resistivity silicon versus higher resistivities, demonstrating the full depletion of the epitaxial layer in the ideal case.

B. The 4T Pixel Architecture

A common pixel architecture present in CMOS image sensors is that of the three transistor (3T) structure, as shown in Fig. 3. This architecture consists of a diode, a reset transistor, a source follower transistor and a row select transistor. To operate this pixel, first, the diode is reset via the reset transistor, and then charge generated in the epitaxial layer from photons or ionising particles is collected. After a set “integration” time, the SELECT transistor is enabled and the signal from the pixel is read out via external readout circuitry.

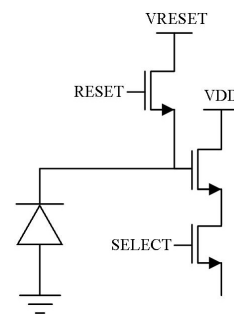


Fig. 3. 3T CMOS pixel architecture

The four transistor (4T) pixel architecture adds two additional elements to the 3T architecture. This architecture is shown in Fig. 4. These elements are the transfer gate (TX) and the floating diffusion node (FD). The architecture also exchanges the standard diode for a pinned photodiode [7]. Charge will be collected by the pinned photodiode as long as TX is disabled. Following the integration time, the charge is transferred to the floating diffusion node by enabling TX.

The pinned photodiode is manufactured with an additional shallow p-type implant above the standard n-type diffusion on a p-type epitaxial layer, producing a p-n-p structure. When the floating diffusion node is reset to a voltage above or equal to the pinning voltage and TX is enabled, the depletion regions from the two p-n junctions within the structure meet, fully depleting the diode and allowing for full noiseless charge transfer to occur. This process therefore simultaneously resets the diode and transfers the charge to the floating diffusion node ready to be read out from the pixel.

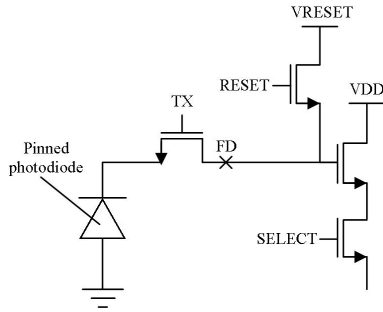


Fig. 4. 4T CMOS pixel architecture. The key elements are the transfer gate (TX) and the floating diffusion node (FD), and the pinned photodiode, which replaces the standard diode.

There are two key benefits to the 4T pixel architecture, both due to the fact that the charge collection area and the readout node within the pixel are separated. This is not the case within the 3T pixel. The separation of these two nodes allows low noise operation via the use of correlated double sampling.

The main noise source within a CMOS pixel is kTC noise (also known as “reset” noise). This originates from the resetting of the capacitive floating diffusion node through the resistive channel of the reset transistor, and is typically of the order of 500-1000 μV . If the floating diffusion node is sampled before and after TX is enabled, provided that the samples are temporally close enough together, the kTC noise is correlated. Taking the difference of the two samples eliminates the kTC noise, as well as some sources of fixed pattern noise. The remaining noise is due to readout noise, which can be thermal, 1/f or random telegraph signal (RTS) noise, and typically gives a noise value of the order of 200-300 μV , depending on the characteristics of the sensor [8]. The dominant of these noise sources is the RTS noise associated with single traps at the gate-oxide interface of the in-pixel source follower transistor, which can be reduced by careful geometric tailoring or via the use of special processing steps [9]. These ideas are both investigated in FORTIS, as will be discussed in the following sections.

The second benefit of the separated charge collection and readout nodes within the 4T pixel architecture is that a high conversion gain can be obtained. This parameter defines the sensitivity of the pixel to small amounts of charge, and is given by $V = q/C$, where q is the charge of an electron (1.6×10^{-19} C) and C is the capacitance where the charge is stored before readout. In the 3T case, C is the diode capacitance, but in the 4T case, C is the floating diffusion node capacitance. The floating diffusion capacitance can be

geometrically tailored to suit the application. If charge is transferred from a large capacitance (with a low conversion gain) to a smaller capacitance (with a higher conversion gain), then the sensitivity to small amounts of charge is increased.

III. FORTIS - 4T TEST IMAGE SENSOR

FORTIS (Fig. 1) is a prototype sensor containing up to thirteen different variants on a 4T pixel architecture. There have been two iterations of this sensor; FORTIS 1.0 and FORTIS 1.1. Both chips were fabricated using the 0.18 μm INMAPS process, and included circuitry to allow correlated double sampling for low noise operation. FORTIS 1.0 focused primarily on geometric variations of the source follower size, diode size, and floating diffusion node shape in order to find the optimum dimensions for low noise operation and high conversion gain. There were also four different pitches of pixels on the sensor; 6 μm , 15 μm , 30 μm and 45 μm . On FORTIS 1.0, three processing variations were implemented to investigate different processing steps to aid the charge transfer for the larger diodes by varying the pinning voltage.

FORTIS 1.1 took the best processing variation from FORTIS 1.0 and further explored the pixel variants via fabrication with and without the deep p-well layer previously mentioned, and on both a standard and a high resistivity epitaxial layer. FORTIS 1.1 also contained an optimised processing step to reduce the RTS noise associated with the in-pixel source follower and increase the gain of the source follower transistor, and an extra pixel variant to investigate the effects of binning charge from four diodes to one large floating diffusion node at the expense of reduced conversion gain.

IV. RESULTS FROM FORTIS

This section details the test results from both FORTIS 1.0 and FORTIS 1.1.

A. Basic Test Results

The basic characteristics of an image sensor can be easily obtained by taking a set of images for several exposures or light intensities, calculating the variance and mean for each exposure time/light intensity, and forming the photon transfer curve (PTC). This is a standard way of measuring image sensors and can provide a lot of information about the characteristics of an image sensor [10].

The pixel with the best performance (in terms of noise) from FORTIS 1.0 was one where the shape of the floating diffusion capacitance was varied. The PTC from this pixel is given in Fig. 5, and the corresponding input-referred noise histogram given in Fig. 6. The results from the three processing variations are given in Table I. The integration time was 23ms, and the number of pixels analysed to obtain these results was 64x64 (4096). The results were then calculated from 100 frames and then averaged over all pixels to obtain the mean and variance values to plot the PTC.

The results show that the conversion gain is high, relating to a floating diffusion capacitance of ~ 2.3 fF. The input-referred noise is 5.6 e-rms, which is taken directly from the standard deviation per pixel of 100 dark frames, averaged,

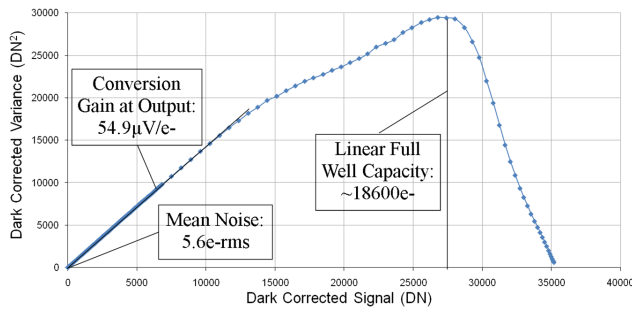


Fig. 5. Photon transfer curve from the best pixel of FORTIS 1.0. This was generated over 100 frames from the mean and variance of 64 x 64 (4096) pixels, and is the standard way of characterising image sensors.

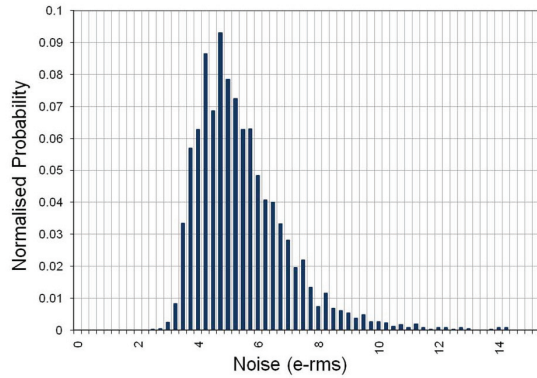


Fig. 6. Input-referred noise histogram from the best pixel of FORTIS 1.0 for 64 x 64 (4096) pixels. This was obtained from analysing the individual pixel data over 100 frames and calculating the mean and variance to form a photon transfer curve for each pixel, then multiplying the individual input-referred noise and gain values together and dividing by the average gain to form a noise histogram in e-rms.

Parameter	Processing Variation		
	A	B	C
Mean Noise (e-rms)	5.6	5.6	5.5
Most Probable Noise (e-rms)	4.75	5	4.75
Conversion Gain at Output ($\mu\text{V}/e^-$)	54.9	55.5	55.4
Conversion Gain at FD ($\mu\text{V}/e^-$)	68.7	69.3	69.3
FD Capacitance (fF)	2.3	2.3	2.3
Linear Full Well Capacity (e^-)	18600	18800	19200
Maximum Full Well Capacity (e^-)	24400	24500	24600
Linear Output Voltage Swing (V)	1.022	1.042	1.067
Maximum Output Voltage Swing (V)	1.679	1.699	1.703
Quantum Efficiency (%)	35.2	34.3	39.1
Dark Current (pA/cm^2)	4.86	5.17	6.29

TABLE I

RESULTS FROM THE BEST PIXEL OF FORTIS 1.0 AS OBTAINED FROM THE PHOTON TRANSFER CURVE (64 X 64 (4096) PIXELS)

then divided by the gain as measured from the PTC. The most probable input-referred noise value, which can be seen from the histogram in Fig. 6 is actually less than this value and is 4.75-5 e-rms. The reason for the difference in the two values is that RTS noise associated with the source follower is present, which increases the mean input-referred noise value from the most common (modal) input-referred noise value. The modal input-referred noise and mean input-referred noise would be very similar if RTS noise was not present.

The three processing variations (A, B and C) were designed

to vary the pinning voltage to aid the charge transfer for pixels with larger diodes. There appears at first glance to be very little difference between the three processing variations for the pixel of Table I. However, image lag effects were observed for processing variation C and not in the other two processing variations. Image lag effects could account for the higher quantum efficiency and linear full well capacity values obtained for variation C, where extra lag electrons are read as part of the actual signal in subsequent frames. Also, note that processing variation B was designed to have a higher pinning voltage than A, which would be expected to vary the output voltage swing. No difference is observed in these two processing variations, suggesting that the output voltage swing in the case of this pixel is limited by the maximum number of electrons stored by the floating diffusion node. For applications where high conversion gain is of importance and a small floating diffusion capacitance is used, processing variation B is therefore not beneficial.

Note that the dark current values are estimates, as there is no dedicated temperature sensor on-chip. All results were taken with the surroundings at room temperature, and it is estimated that the temperature on-chip varies by $\pm 1^\circ\text{C}$ when taking the results for the dark current calculation, which corresponds approximately to a $\pm 1 \text{ pA}/\text{cm}^2$ variation on the values stated in Table I.

B. Impact of Optimised Process on FORTIS 1.1

A pair of identical pixels was selected from FORTIS 1.0 and FORTIS 1.1. The only difference between the two pixels is that the one on FORTIS 1.1 has the addition of the optimised processing for reducing the RTS noise associated with the source follower transistor and increasing the conversion gain. Input-referred noise distributions were plotted for both pixels, and are given in Fig. 7.

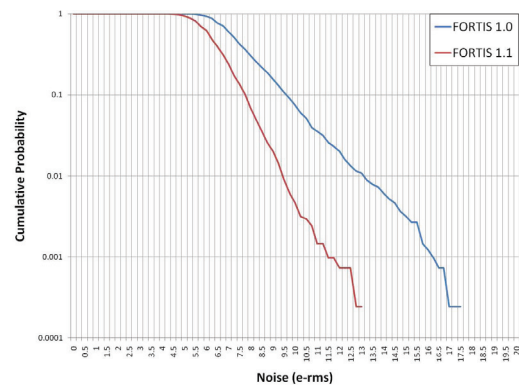


Fig. 7. Input-referred noise distributions from comparing the same pixel on FORTIS 1.0 and FORTIS 1.1 for 64 x 64 (4096) pixels. The cumulative probability gives the probability that a pixel has an input-referred noise higher than a certain value on the x-axis. FORTIS 1.1 has the addition of an optimised processing variation, providing a lower modal input-referred noise result due to an increased conversion gain, and a reduction in random telegraph signal noise.

The distributions show the input-referred noise value plotted against the cumulative probability. By displaying a graph in this way, the distributions give the probability that the pixel

has an input-referred noise higher than a particular value on the x-axis. For example, 100% of the pixels analysed have an input-referred noise level higher than 4 e-rms; 1% have an input-referred noise level high than 13 e-rms. From this data, it is immediately clear that the pixel's input-referred noise distribution has reduced in spread on FORTIS 1.1, and that the most probable input-referred noise value (taken from the steepest part of the curve around 5 e-rms) has also reduced on FORTIS 1.1. These reductions are due to the increased conversion gain as a result of the increased in-pixel source follower gain, combined with the reduction in RTS noise as shown by the reduction of the tail of the distribution.

C. Source Follower Size Variation

The geometric tailoring of the source follower size can lead to some reduction in RTS noise without the use of special processing steps. Fig. 8 shows the input-referred noise distributions from the four pixel variants intended to explore variations of the source follower size.

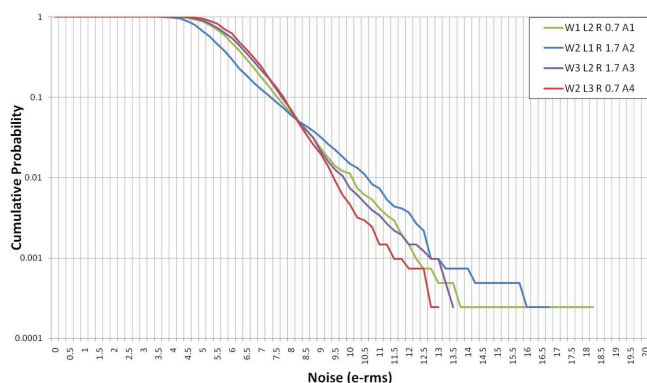


Fig. 8. Input-referred noise distributions from pixel variants exploring source follower size (W=width, L=length, R=ratio W/L, A=area, 1=smallest, 4=largest) for 64 x 64 (4096) pixels. The results show that shorter source follower transistors have a higher random telegraph signal noise distribution, which is visible as a long tail on the higher end of the distributions.

Two different width to length ratios were compared (0.7 and 1.7), obtained from combinations of three different source follower widths (W1-W3) and three different lengths (L1-L3), and producing four different areas of source follower (A1-A4). Note that “1” represents the smallest dimension and “4” represents the largest, therefore “W1 L2 R07 A1” had the smallest width, the second largest length, a width to length ratio of 0.7 and the smallest source follower area.

It has been suggested that the longer the source follower, the lower the RTS noise [9]. This is due to the decrease in probability of finding a single trap underneath the gate of the source follower with increasing length. The same trend is not seen as clearly for increasing width, as local geometric features within pixels can vary the threshold voltage across the width of the transistor and limit the actual channel width increase. The results show that the RTS noise, associated with the tail of the input-referred noise distribution, is less for the longer source followers than it is for source followers of the same width. It can also be seen that two source followers of

similar area (A1 and A2) but with different widths and lengths can give different input-referred noise distributions, and two source followers with the same width to length ratio (0.7 and 1.7) give similar RTS noise tails. The smallest and shortest source follower has one of the longest RTS tails (longer than that of the largest source follower), even though its modal input-referred noise was the lowest (due to having the highest conversion gain). The distributions clearly show a correlation between RTS noise and source follower length.

D. Use of a High Resistivity Epitaxial Layer

Interesting results from comparing fabrication of FORTIS 1.1 on a standard and a high resistivity epitaxial layer have been found via the use of charge collection efficiency scans. A white light source was focused down to a $2\ \mu\text{m} \times 2\ \mu\text{m}$ spot size and then horizontally scanned across the centre of the diodes of three adjacent pixels. The charge collection efficiency was then obtained by recording the location of the spot and the resulting signal obtained out of each pixel in turn. This was done for sensors that were manufactured on a standard and a high resistivity epitaxial layer.

Fig. 9 shows the results obtained from these scans. The standard resistivity case is shown on the left, and the high resistivity case is shown on the right. The geometric features of the pixels are immediately clear; the peaks represent the positions of the diodes (i.e. where the spot was focused directly on the pixel of interest) and the troughs mark where metal covers the pixel and light is prevented from illuminating the silicon. However, secondary peaks are also visible in the standard resistivity case. These represent the charge collected by one pixel when the spot is focused on the diode of its nearest neighbour, and is termed crosstalk. These peaks are not present on the high resistivity epitaxial layer scan, showing the benefits of its use for reducing crosstalk.

E. Radiation Hardness Results

Radiation hardness results were obtained for FORTIS 1.0 to estimate the radiation tolerance of the 4T pixel architecture to ionising radiation. The best pixel (as shown in Fig. 5) from five FORTIS 1.0 sensors was irradiated in steps up to 220 kRad using 50 kVp x-rays from an x-ray tube. In-between the irradiations, when not being tested, the chips were stored at $-25\ ^\circ\text{C}$. It was found that the input-referred noise and dark current increased logarithmically with respect to irradiation level up to 110 kRad, as shown in Fig. 10. Beyond this level, the noise increased to a level where obtaining an acceptable photon transfer curve for results analysis was no longer possible.

The dark current within a 4T pixel is believed to be dominated by the transfer gate [11], which would have been affected by ionising radiation by the formation of traps within the transfer gate oxide and at the corresponding silicon-silicon dioxide interface and could explain the increase in dark current observed with increasing irradiation level.

The input-referred noise distributions for one of the sensors before and after a dose of 110 kRad are given in Fig. 11. The input-referred noise distribution clearly spreads out, suggesting

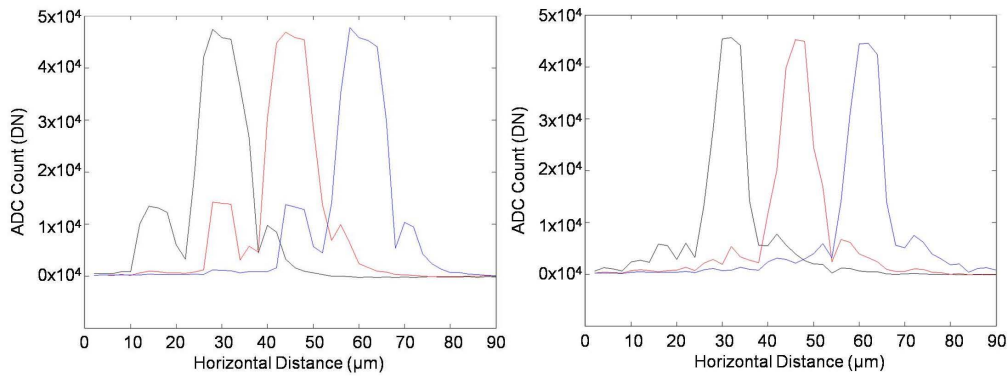


Fig. 9. FORTIS 1.1 charge collection scans from a 2 μm by 2 μm white light source. Standard resistivity is shown on the left; high resistivity on the right. The peaks and troughs represent the diode and metal within the pixel respectively, and the secondary peaks (more visible on the standard resistivity scan) represent crosstalk.

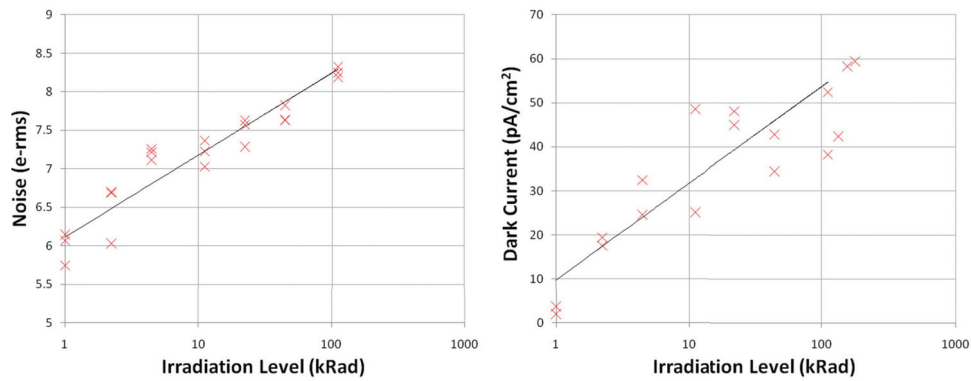


Fig. 10. Graphs of input-referred noise and dark current versus irradiation level for FORTIS 1.0 for 32 x 32 (1024) pixels. A logarithmic increase is observed for both, suggesting that the increase in input-referred noise is primarily due to the corresponding increase in dark current.

that RTS noise and $1/f$ noise have increased, which are both associated with charge trapping in the source follower transistor gate oxide and the corresponding silicon-silicon dioxide interface [12]. The increase in input-referred noise shown in Fig. 10 is also visible within these distributions.

V. CONCLUSIONS

FORTIS has proved 4T CMOS to be a very promising technology for applications where low noise and high sensitivity to small amounts of charge are of importance. The lowest input-referred noise was measured on FORTIS 1.0 to be 5.6 e-rms (most probable value 4.75-5 e-rms) and this pixel was also shown to be tolerant to ionising radiation up to 110 kRad.

It has been shown that tailoring of the geometric features and the process to form the 4T pixel architecture can influence its characteristics. The RTS noise associated with the source follower is dependent on the length of the source follower transistor, with longer transistors exhibiting less RTS noise. A specialised process used on FORTIS 1.1 was shown to reduce the RTS noise even further, and simultaneously increased the conversion gain by increasing the source follower gain.

The effects of using a high resistivity epitaxial layer has also been demonstrated via the use of charge collection efficiency scans. Crosstalk was shown to have decreased significantly with the use of a high resistivity epitaxial layer due to the change in the primary charge transport mechanism.

The results from FORTIS are currently being used to assess whether the sensor can be scaled up to a 5 cm x 5 cm active area, and 4T CMOS is also being pursued for a 4T-style digital electromagnetic calorimeter (DECAL) design [13]. This sensor

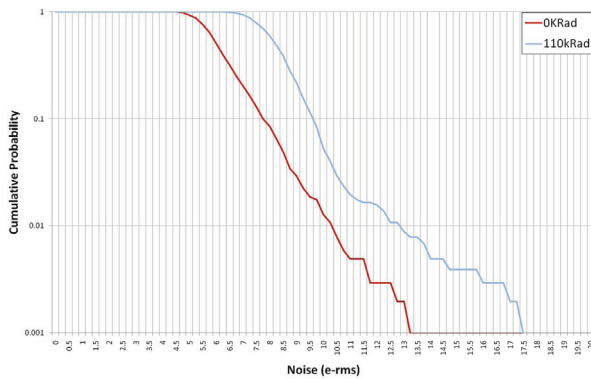


Fig. 11. Radiation hardness input-referred noise distributions from FORTIS 1.0 for an unirradiated sensor and the same sensor after a dose of 110 kRad for 32 x 32 (1024) pixels. The distributions show that the random telegraph signal noise has increased, and the mean input-referred noise has also increased.

has clearly showed the benefits of the 4T pixel architecture and the INMAPS process, which will be of great use to us in many other future developments.

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