Comparison of Passive and Active Pixel Schemes for CMOS Visible Imagers

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ABSTRACT

An active pixel sensor (APS) integrated in standard CMOS process technology is shown to be superior to an alternative passive pixel sensor (PPS). Further, the CMOS APS provides video sensitivity and SNR comparable to CCDs. Though the CMOS PPS has lower performance, it offers >50% optical fill factor without microlenses and can be produced at lower cost for applications not requiring broadcast quality SNR (>35 dB) under low light conditions (<20 lx). APS and PPS SNRs of 50 dB and 44 dB are reported at 200 lx using green filtering with ~80 nm bandpass.

Keywords: CMOS, APS, passive pixel, CCD

1. INTRODUCTION

Developments in CMOS image sensor technology are paving the way for a new generation of digital imaging products. Though most currently available electronic visible-light cameras use charge-coupled device technology for low-noise image capture, CMOS technology offers practical advantages with respect to on-chip integration of many camera-related functions and fundamental technological advantages with respect to temporal noise. The read noise of a CCD is effectively set by external circuits to a relatively wide bandwidth compatible with the video rate assuming that supporting chips are used to eliminate reset noise. CMOS APS read noise can be much lower because the noise bandwidth is much smaller – it is set by the on-chip electronics in the on-chip circuits servicing each column of pixel elements to service relatively low line rates. A second advantage is the relative ease at which higher sensitivity can be achieved in the CMOS imager paradigm. The key technical impediment to CMOS APS proliferation is the need to suppress the pixel-to-pixel fixed pattern noise generated by the same amplifiers that produce the clear-cut advantage in temporal noise.

Hybrid infrared imagers have used CMOS readouts since about 1985 for low-noise readout of photo-generated signals. Shrinking circuit geometries and advances in imager design have since enabled rapid improvements in the performance of the CMOS readouts used to interface various infrared detectors. Monolithic visible imagers have become available only recently because of the necessity for submicron photolithography to exploit the same low-noise signal extraction perfected for infrared sensors. The "sudden" emergence of CMOS imagers is, hence, only one more consequence of Moore's Law, which predicts the ability to double transistor integration on each integrated circuit about every 18 months. Shown in Figure 1 are the associated process and imager development trends, including the current general availability of CMOS processes having ~1 µm minimum feature and the imminent ability for much higher levels of transistor integration. CMOS imager development is consequently behaving as a delta function, where the amplitude depends on each developer's capability and imager complexity is driven by the application rather than process technology. The ongoing migration to even finer lithographies will thus enable the rapid development of CMOS imagers having even higher resolution, better image quality, higher levels of integration and lower overall imaging system cost than CCD-based solutions. The silicon wafer production infrastructure which has put personal computers into many homes is now enabling CMOS-based imaging in consumer products such as video and digital still cameras.

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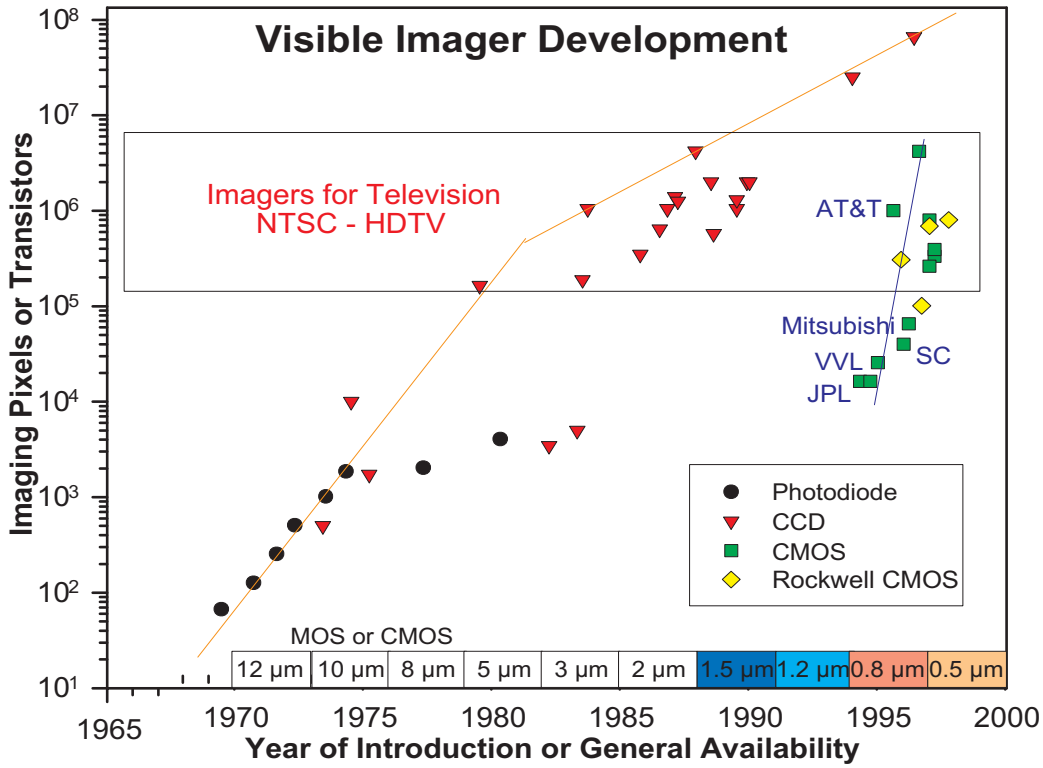

Figure 1.Chronology of Imager Pixel Count and CMOS Process Availability.

CMOS imagers use either active or passive pixels as shown in simplified form in Figure 2. Active-pixel sensors (APS) include some form of amplification in each pixel. Passive pixels are instead read out without pixel-based amplification. Since passive pixel sensors (PPS) have simple pixels consisting often of only a photodiode and a MOSFET switch, the circuit overhead cost is low and they have a high optical collection efficiency (fill factor) of 50 to 80 percent. The large optical fill factor maximizes signal collection and hence, minimizes fabrication cost by obviating the need for microlenses. Microlenses are a standard feature of CCD and CMOS APS imagers. When accurately deposited over each pixel, microlenses concentrate the incoming light into the photo-sensitive region. When the fill factor is low and microlenses are not used, the light falling elsewhere is either lost or, in some cases, creates artifacts in the imagery by generating electrical currents in the active circuitry.

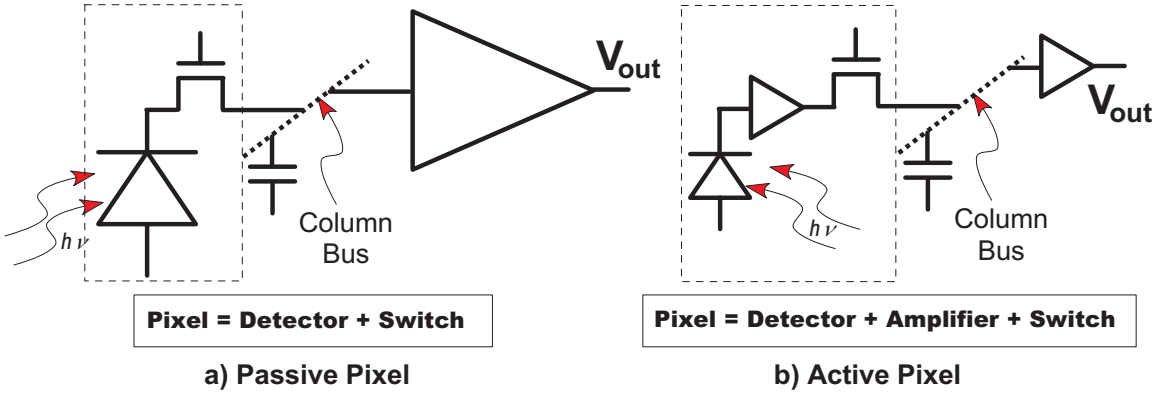

Figure 2. Passive and Active Pixel Sensors.

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Active pixel sensors incorporate transistors in each pixel to convert the photo-generated charge to a voltage, amplify the signal voltage and reduce noise. Adding these components reduces APS fill factor in 0.6 µm processes to about 20 to 30 percent. To maximize the effective fill factor, APSs often use microlenses (Figure 2) to capture light that would otherwise strike the pixel's insensitive area. Microlenses double or triple the effective fill factor. Figure 3 shows the cross-sectional view of a CMOS PPS imager with color filters and optional microlens.

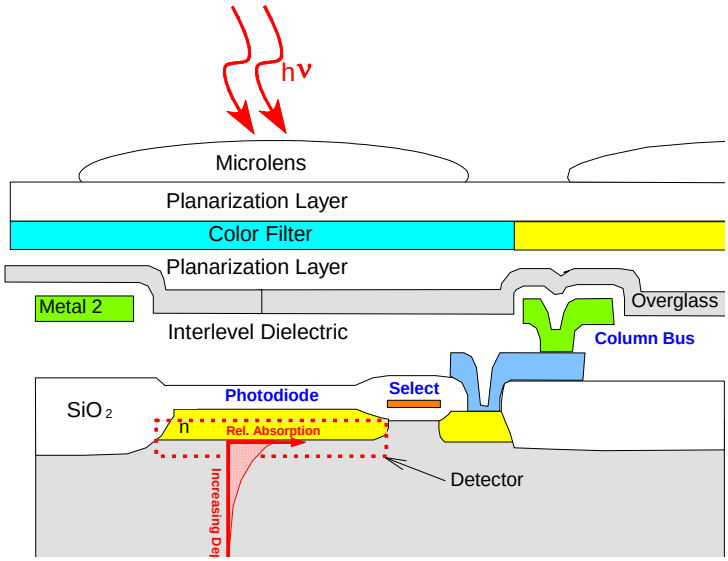

Figure 3. Cross-Section of CMOS Passive Pixel Imager

2. PASSIVE PIXEL SENSORS

The simplest passive pixel comprises a photodiode and an access transistor; the photo-generated charge is passively transferred from each pixel to downstream circuits.[1] The charge must, however, be efficiently transferred with low noise and nonuniformity. Since each column of pixels often shares a common bus (along a row or column) for reading the signal, suppression of temporal noise and offset nonuniformity are typically facilitated in the buffer servicing each bus. Plummer[2] used a buffer consisting of a transimpedance amplifier with capacitive feedback to yield reasonable sensitivity (Figure 4) considering the large bus capacitance and the MOS technology available at the time. Since such charge-amplification means were not generally practical for on-chip implementation in early MOS imaging sensors, alternative means compatible with NMOS technology were used. Koike[3] and Ohba,[4] for example, implemented a scheme which was mass-produced by Hitachi for camcorders.[5] The key refinements with respect to Plummer were anti-blooming control and circuitry for reducing fixed pattern noise. Though these imagers were proven inferior to the emerging charge coupled device (CCD) imagers available at the time due to MOS process immaturity, similar MOS imagers are still being offered commercially.[6]

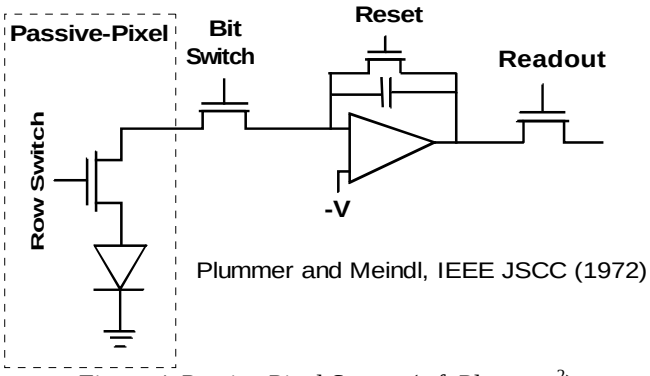

Figure 4. Passive Pixel Sensor (c.f. Plummer[2]).

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Subsequent efforts at improving passive-pixel imager performance focused on column buffer enhancements. Ando[7] improved the column buffer by using an enhancement/depletion inverter amplifier to provide reasonably large amplification in a small amount of real estate; its 40 lx sensitivity was nevertheless nearly an order of magnitude below that of competing CCD-based sensors. Sonoda[8] both enhanced sensitivity and facilitated automatic gain control via charge amplification in the column buffer. Wyles[9] and Denyer[10] have recently revisited Plummer's original capacitive-feedback transimpedance amplifier (CTIA) concept because the CTIA is nearly ideal for passive-pixel readout if issues with temporal noise pickup and fixed-pattern noise are adequately addressed.

2.1 352x288 Passive Pixel Sensor

Expanding on Plummer's original concept by using mixed-signal 0.6 µm CMOS, we have developed a 352x258 (Common Intermediate Formate; CIF) passive pixel sensor with CTIA-based column buffer with 10 µm x 9.15 µm pixel size. The imager's noise performance was modeled similarly to our other capacitive transimpedance amplifier (CTIA) designs.[11] Appropriately modifying the CTIA paradigm and applying the various device parameters which were either extracted or purposely implemented in the CIF imager design including ~1.7 pF bus capacitance, Figure 5 was generated where N_{imager} is the total noise including background shot noise (N_{photo}) at 0.35 lx, detector noise (N_{det}), and PPS read noise (N_{read}). $N_{channel}$ and $N_{amp1/f}$ are the dominant column buffer noise sources. N_{out} is the noise of camera electronics. The total predicted noise is 61 e- at the expected detector capacitance of 48 fF. We subsequently measured actual read noise of 75 e- ±10 e- on several of the PPS imagers. Though much progress has thus been made in developing passive-pixel imagers, their temporal S/N performance is fundamentally inferior to competing CCD imagers because the bus capacitance effectively translates to white noise on the order of 100 e-. CCDs, on the other hand, typically have read noise of 20 to 40 e- at video frame rates.

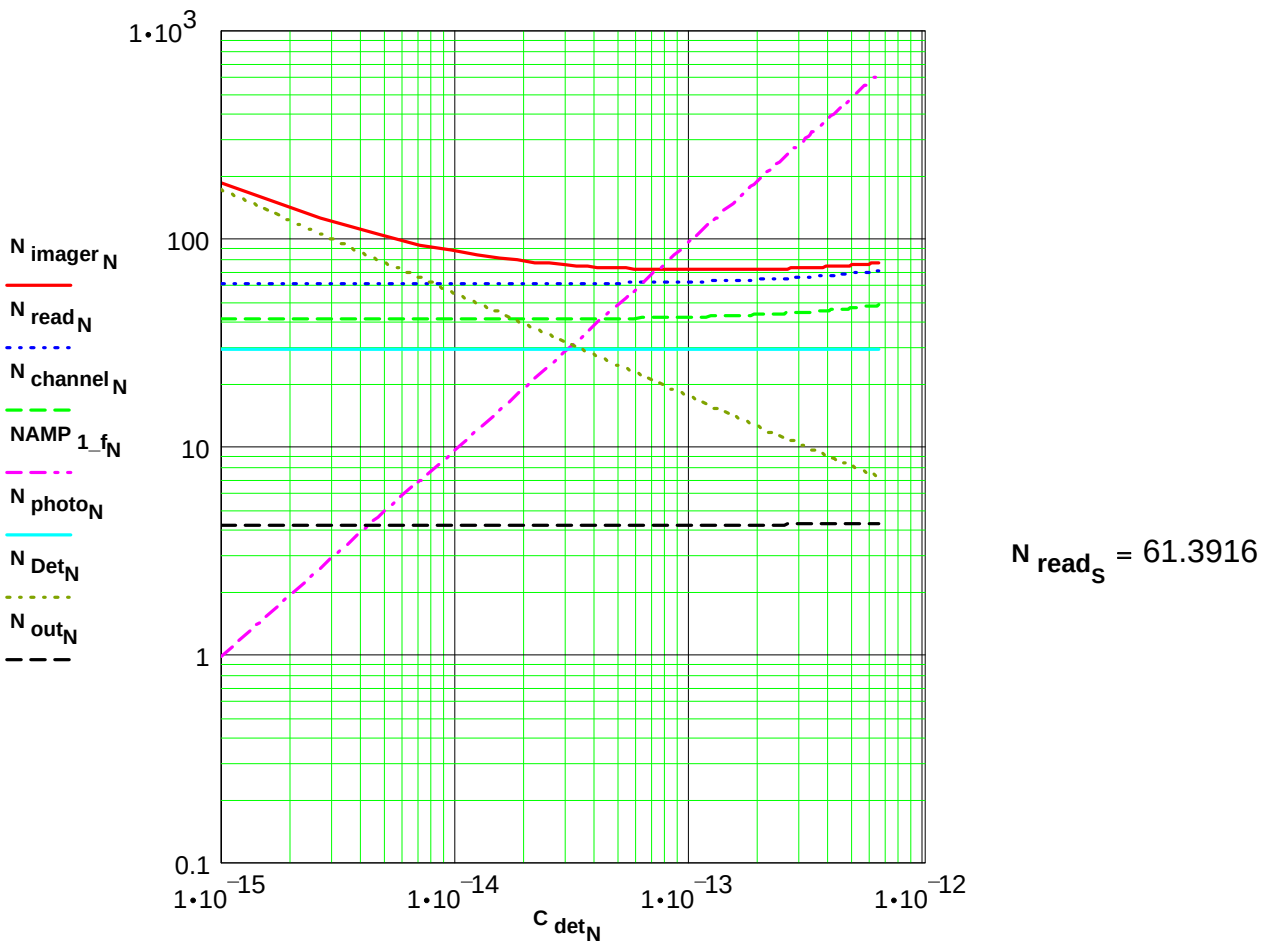

Figure 5. Passive Pixel Sensor Noise vs. Detector Capacitance.

Variable sensitivity was integrated on-chip by using several feedback capacitors in the column buffer CTIA which was programmable in 16 combinations. Figure 6 shows the measured sensitivity as a function of feedback capacitance. The minimum and maximum sensitivities are 4 and 48 µV/e-, respectively. By programming the various capacitors as a function of scene illumination, automatic gain control is facilitated. The rms gain nonuniformity of the PPS with CTIA column buffers was ≤0.6% rms with evidence that the nonuniformity was at least partially due to the light source.

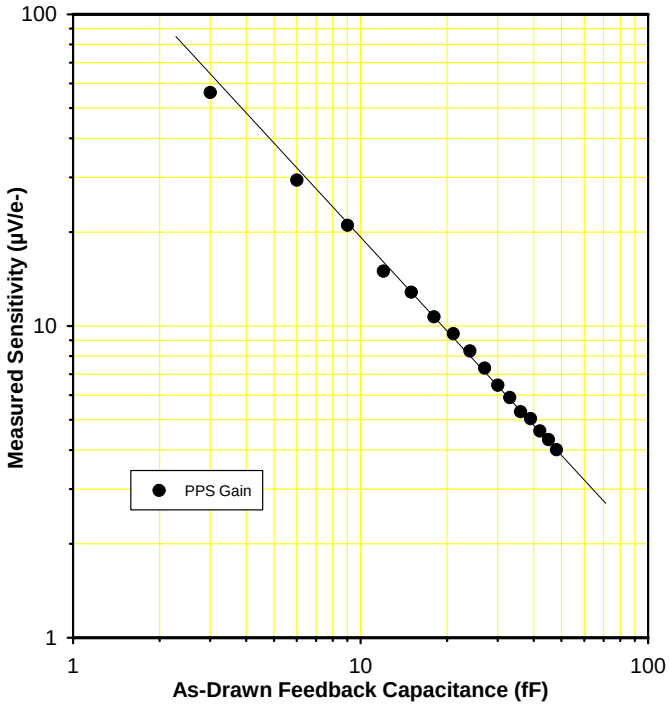

Figure 6. Measured PPS Sensitivity vs. As-drawn Feedback Capacitance.

Since each column buffer has a differing input offset voltage, on-chip offset cancellation circuitry was used to cancel these offsets. Figure 7 is an oscillogram showing the output of a typical line of video, both with the canceller enabled and for raw video. By enabling the offset canceller, the peak-to-peak nonuniformity is reduced from 14 mV to 2 mV. Using a custom digitizing acquisition system with 14-b resolution to measure the offsets, the rms nonuniformity is 160 µV. The rms nonuniformity relative to the maximum video swing of 1.2 V at 5 V supply voltage is 0.01%. Reducing the supply voltage to 3.3 V reduces the video swing to 1.1 V and thus increases the nonuniformity to 0.015%.

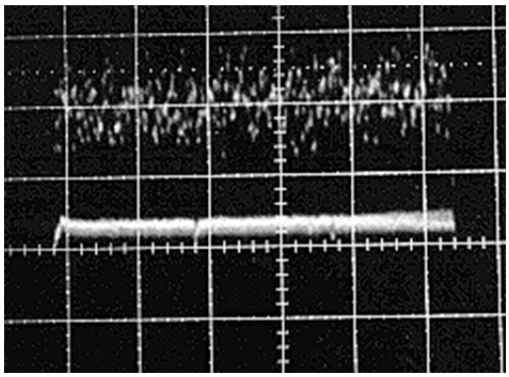

Figure 7. Oscillogram for one line of video at 10 mV/division with and without on-chip offset cancellation.

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3. ACTIVE PIXEL SENSORS

The allure of producing imagers in conventional MOS fabrication technologies rather than esoteric CCD processes (which usually require many implantation steps and complex interface circuitry in the camera) has also encouraged the development of active-pixel sensors that can directly compete with CCDs. The first key step is to mitigate the noise associated with the bus capacitance. Tanaka[12] hence added amplification to the pixel via the phototransistor as, for example, earlier proposed by Weckler.[13] Tanaka's Base-Stored Image Sensor (BASIS) used a bipolar transistor in emitter follower configuration with downstream correlated double sampler to suppress random and temporal noise. By storing the photogenerated-signal on the phototransistor's base to provide charge amplification, the minimum scene illumination was reduced to 10^{-3} lx in a linear sensor array.[14] However, the minimum scene illumination was higher (≈.01 lx) in a two-dimensional BASIS imager having 310,000 pixels[15] because the photoresponse nonuniformity was relatively high (≤2%). These MOS imagers had adequate sensitivity, but their pixel pitch was too large at about 13 µm. The second key step is to shrink the pixel pitch while simultaneously reducing photoresponse nonuniformity.

Since the incorporation of bipolar phototransistors is not strictly compatible with mainstream CMOS processes, others have segregated photodetection and signal amplification. Uno[16] and Wyles,[17] among others, describe active-pixel sensors essentially comprising a three-transistor pixel with photodiode. All offer inadequate performance. Uno, for example, augments the basic source-follower configuration of Wyles[18] with a column buffer that cancels fixed pattern noise, but adds a fourth transistor that creates a floating node vulnerable to generation of random offsets from charge-pumping and concomitant charge redistribution. Wyles offers a method for injecting charge to reduce offset errors, but perhaps not with adequate accuracy and resolution to be useful for competing with CCDs. Furthermore, these and other similar approaches requiring three transistors in the pixel (at least one of which is relatively large to minimize amplifier 1/f noise) in addition to the photodiode, also require off-chip signal processing for best S/N performance because none addresses the dominant source of temporal noise. In order to eliminate or greatly suppress the reset (or kTC) noise generated by resetting the detector capacitance, a dedicated memory element is usually needed, either on-chip or off-chip, to store the reset voltage to apply correlated double sampling and coherently subtract the correlated reset noise after the photo-generated voltage is generated.

Fossum[19] addresses this basic deficiency via an APS that uses intra-pixel charge transfer to store the reset charge at each pixel at the start of each imaging frame. Though this facilitates correlated double sampling within each pixel, the drawbacks, including the addition of several transistors and the reliance on a transparent photogate for signal detection, are likely intractable because they increase imager cost by violating the paradigm for full compatibility with standard CMOS. The former adds several transistors to each pixel; adding several million transistors to each imager reduces production yield. The latter is not compatible with standard CMOS gate fabrication so a nonstandard process must be developed. These deficiencies are partially addressed by Ackland[20,21] and Chi.[22] Ackland addresses the image lag issues associated with intra-pixel charge transfer but still requires a non-standard CMOS process. Chi reduces pixel complexity at the expense of reset noise by instead using the simplest possible active pixel comprising only a phototransistor and reset MOSFET. Chi's implementation incurs reset noise and compromises spectral response at longer wavelengths by putting the photodiode in an n-well.

3.1 960x720 Active Pixel Sensor

Exploiting the source follower per detector (SFD or three-transistor APS) technology which we have often used for infrared readouts for astronomy,[23,24,25] we have developed a 960x720 active pixel sensor (Figure 8) having 7 µm pixel pitch in 0.5 µm CMOS. The imager's noise performance was modeled similarly to our other source follower per detector designs.[26] Since this design does not currently use correlated double sampling (CDS) to suppress the reset (i.e., kTC) noise, we predicted a read noise of 56 e- for the original 15 fF detector capacitance. We subsequently measured a read noise of 28 e-, confirming that the final capacitance is actually lower than was originally conceived.

Figure 9 allows comparison of these data with other source follower designs which were earlier developed for infrared sensors. Also provided is insight into the relationship between read noise and detector capacitance. However, when comparing the measured value to the theoretical trendline, it should be noted that the theoretical trendlines (both with CDS and without) are for 80K SFD operation rather than 295K. The infrared focal plane array data shown in the figure constitute the majority of the measured data and were obtained at 78K using either correlated double sampling or Fowler sampling with 16 pairs.

The source follower per detector is one of a variety of candidate APS designs used for high performance APS imagers. Other schemes requiring three, four, and five transistors further reduce the temporal noise. Figure 10 is a plot of read noise vs. detector capacitance which includes read noise data for APS designs having three, four and five transistors.[27] Bracketed in

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the figure is the expected range in CMOS photodiode capacitance for representative CMOS imagers versus the read noise for CMOS APS and CCD. The 3T APS data are at the top end of the read noise range. A CMOS APS with five transistors, on the other hand, provides read noise at video frame rates and higher which is far superior to CCD alternatives. Adding transistors as the technology allows thus enables lower and lower read noise.

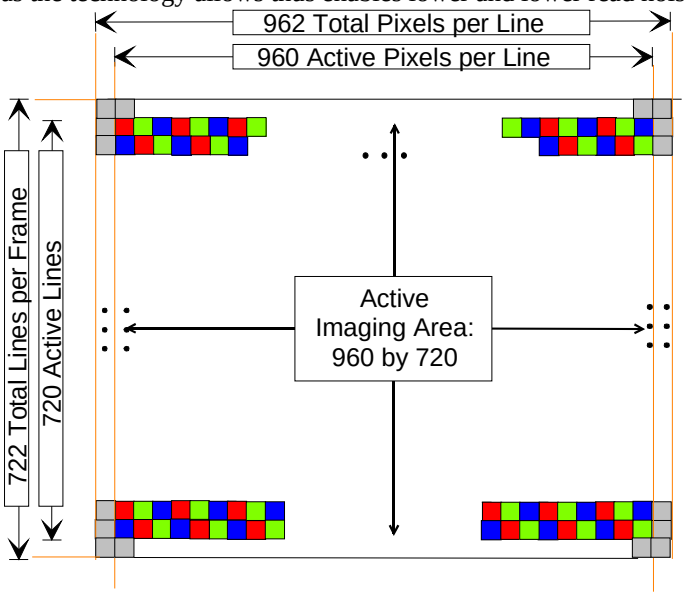

Figure 8. CMOS APS Imager in 960x720 active format with perimeter border of black pixels.

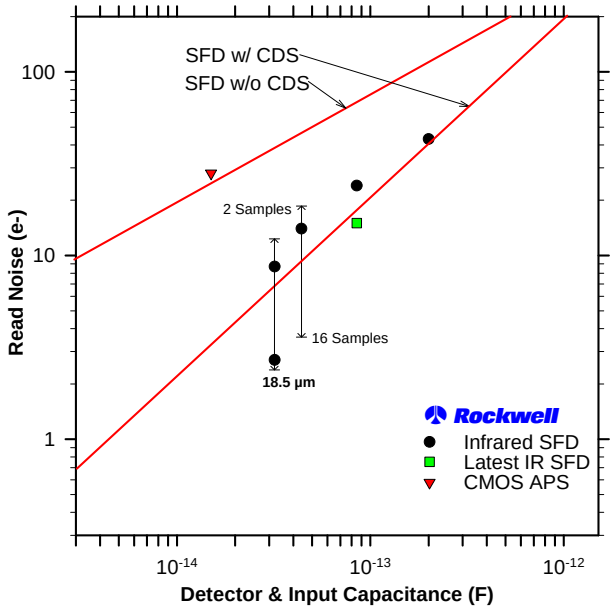

Figure 9. Source Follower per Detector Read Noise vs. Detector Capacitance.

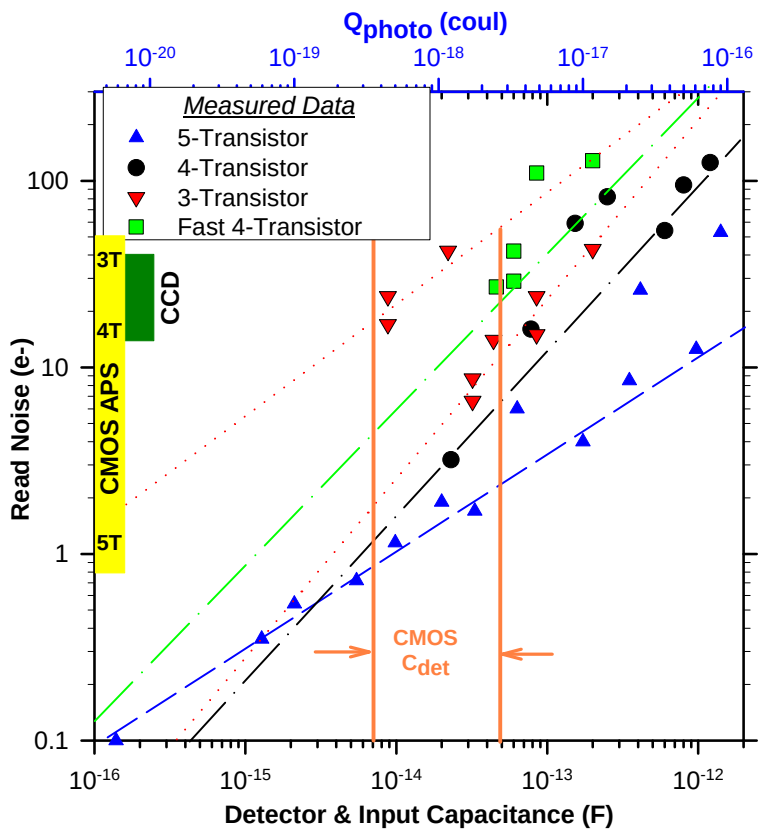

Figure 10. Read Noise vs Capacitance for Alternative APS Designs

4. SIGNAL TO NOISE RATIO COMPARISON

Rapid CMOS imager evolution is expected because these sensors can directly exploit CMOS technology improvements to successively incorporate more adept APS designs. This evolution is expected to lead to a higher level of performance (in quality and resolution of picture) than can be attained with CCDs within the next few years. CMOS imagers represent a paradigm shift in imager technology from one which is tightly controlled by a few manufacturers, i.e., the CCD, to one which exploits the global silicon wafer production infrastructure that is putting personal computers into many homes at ever lower cost and increasing functionality. Figure 11 shows the performance currently achieved with the CIF PPS and the 960x720 SFD APS. The figure is a plot of signal-to-noise ratio vs scene illuminance for f/2 optics. Plotted for green illumination (λ_{pk}= 535 nm with λ_{bp}= 80 nm FWHM and blocking filter for λ>700 nm; Figure 12) are theoretical trendlines at 10 e-. 25 e- and 60 e- read noise, along with measured data for the PPS, APS and a microlensed APS. Under typical office light illumination of 200 lx, the PPS has a 42 dB SNR, which is in very good agreement with the value expected for the measured read noise. At 100 lx, PPS SNR decreases to 36 dB, also in very good agreement. The standard APS without microlenses, denoted as 1st Gen. APS, has only slightly higher SNR of nearly 39 dB even though the read noise is only 38% of the PPS because the as-drawn fill factor is only 24%. Increasing the fill factor by adding microlenses restores the fill factor and, hence, increases the SNR to >46 dB. This performance level is comparable to a CCD having 40 e- read noise and 90% fill factor.

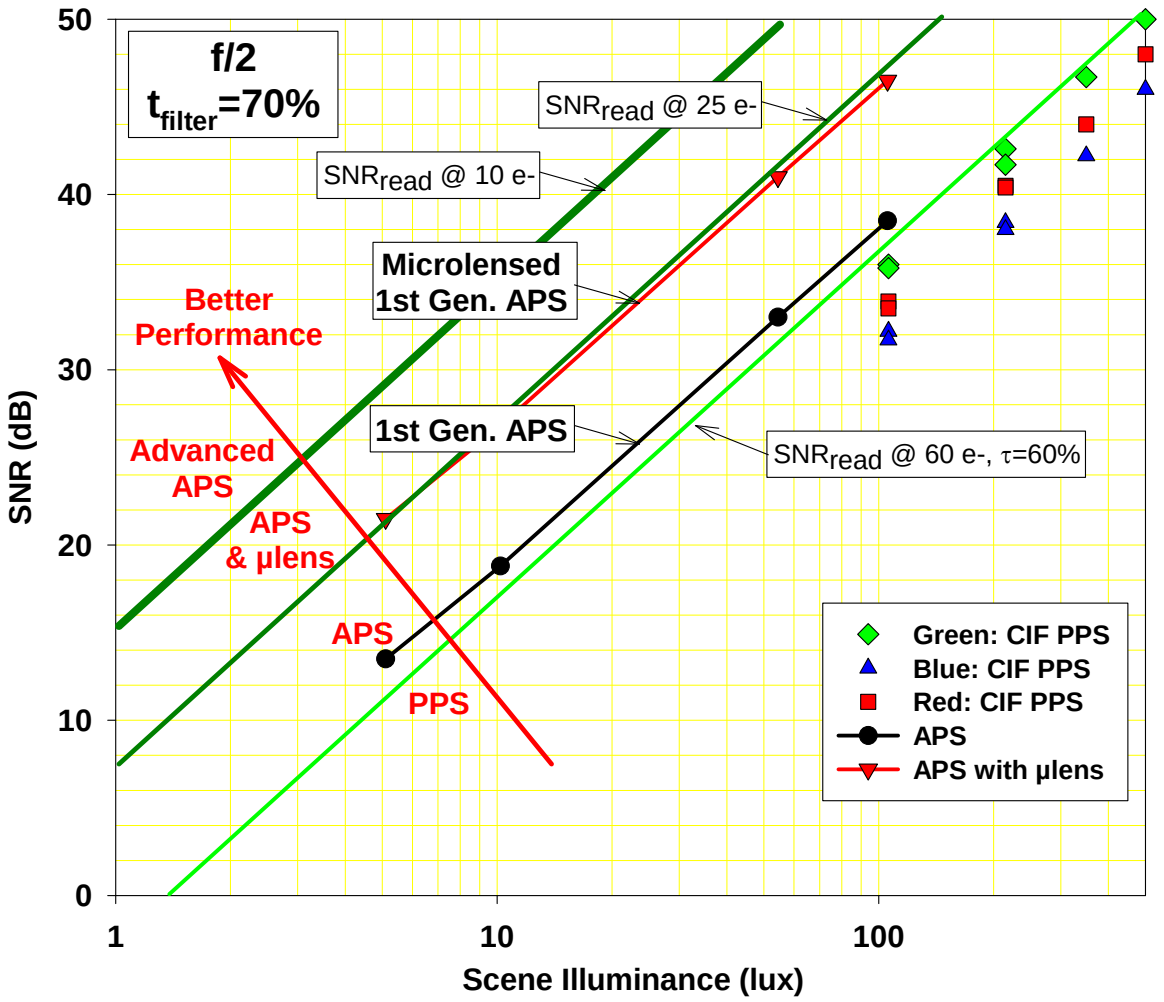

Figure 11. S/N Ratio of Active and Passive Sensors vs. Theoretical Trendlines for 40 e- and 60 e- Read Noise.

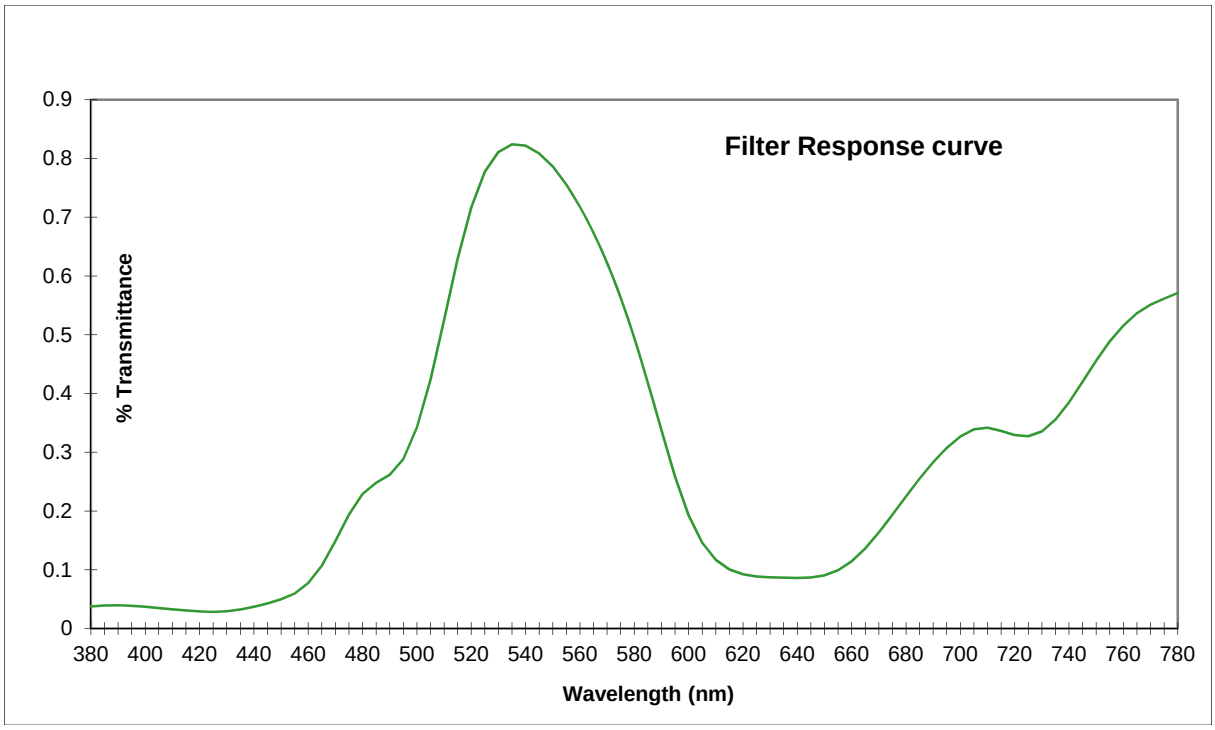

Figure 12. Typical Spectral Characteristic of Deposited Green Filters Used for S/N Measurements.

5. SUMMARY AND CONCLUSION

CMOS imagers represent a paradigm shift in imager technology from one (i.e., the charge coupled device) controlled by a few manufacturers to one which exploits the global silicon wafer production infrastructure that is putting personal computers into many homes at constantly decreasing cost and increasing functionality. Though at a very early stage in development, their performance is already adequate for video cameras. Indeed, the APS offers performance on a par with CCDs with SNR >46 dB at 100 lx scene illumination. The PPS is slightly inferior but suitable for delivering VHS quality under office-lighting conditions.

It is thus clear that CMOS imager technology can readily support future digital imaging devices because CMOS imagers are fundamentally superior to CCDs with respect to temporal noise – the key caveat is that a little more time is needed to exploit Moore's Law regarding transistor integration to enable incorporation of an optimum APS design. APS imagers can offer extremely low read noise at video frame rates because the amplifier at each pixel operates at much lower bandwidth than the output amplifier. This fundamental difference with respect to the CCD can reduce the read noise by at least a factor of 10.

The other key to successfully replacing the CCD is to integrate the necessary on-chip circuitry to eliminate the fixed pattern noise. Since CMOS readily facilitates such integration and such circuits do not require much chip real estate, CMOS imagers are poised to replace the current CCD-based paradigm.

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