

Development of a Production-Ready, Back-Illuminated CMOS Image Sensor with Small Pixels

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Abstract

A back-illuminated 2 megapixel CMOS sensor utilizing mature wafer manufacturing operations is described. Sensitivity, dark current and other key pixel performance measures are compared against an equivalent conventional sensor. Aspects of the process integration that make the technology manufacturable are described. Simulations that predict the performance of a full color sensor are discussed.

Introduction

Back-illuminated imaging is receiving increasing interest as a solution to some of the problems that limit imager performance as pixel size decreases. Several examples of SOI-based back illuminated sensors have been demonstrated in previous publications (1-5). In this work, we focus on the development of a production-worthy monolithic sensor with 2.2 μ m pixels, as a platform to extend the CMOS pixel roadmap into the sub-micron range. It was built using low-cost standard fabrication techniques, and with performance predictable from simulation. We describe a production process for these sensors using available mature technology modules, and present results from a 2 megapixel (MP) sensor exhibiting comparable dark current and noise but much higher quantum efficiency (QE) and sensitivity than a conventional sensor.

Optical Advantages of BSI Configuration

Figure 1 depicts a conventional front-side illuminated (FSI) stack and a BSI stack. The optical stack height is much lower for the BSI pixel, leading to significant advantages in the effective pixel f number. On top of this, the high refractive index of silicon causes light to converge to the center of the pixel, as shown in Figures 2(a) and (b). These are finite difference time domain (FDTD) analyses of energy coupling into the silicon at 550nm, showing the stark contrast in coupling efficiency into the target pixel for FSI and BSI cases at this pixel size (1.75 μ m). At smaller pixel sizes, the differences are even more pronounced and present a practical limit to how small conventional CMOS pixels can be using conventional technology.

Production-Ready Integration

Figure 3 is a schematic representation of the demonstration black and white imager. The fabrication process begins with a specially tailored SOI wafer that allows accurate backside thinning using oxide as an etch-stop (1-3). We use a special SOI layer configuration to suppress dark current generation at the BOX interface, to prevent QE loss at short wavelengths, to reduce cross-talk, and to provide a low resistance back-plane. An imager-compatible bulk-CMOS process (not an SOI process) was used for fabrication. Prior to thinning, a handle wafer was attached to the processed wafer for mechanical support using a low temperature oxide-oxide bonding process (6). Compared to adhesive bonding, this method allows more flexibility for subsequent processing, including higher temperature anneal steps. The acoustic micrograph of the wafer stack (figure 4) built using this process demonstrates void free bonding.

To connect the front-side metals to the bond pads on the backside (i.e. the exposed side), the fabrication process used W-filled and liner oxide isolated through-silicon vias. However, unlike that in "3D" stacked technologies (4), neither multi-wafer vias nor bonding of multiple wafers with sub-micron alignment is needed, resulting in enhanced manufacturability. Figure 5 is a SEM cross-section of the finished SOI wafer. Subsequent wafer-level thinning (backgrind to remove most of the silicon, followed by a dry silicon etch) produced a thinned monolithic imager with a planar back surface, important for subsequent color filter and microlens processing. Backside bond pads connected to the through-vias, standard oxide/nitride passivation and hydrogen anneal complete the wafer process. No special AR coating was applied. Die assembly utilized a simple wire-bonded package – similar to that utilized for an FSI part, as indicated in figure 6 that shows the pictures of two packaged black and white FSI and BSI sensors.

Demonstration Vehicle

The vehicle used to demonstrate the technology was a 2MP, 2.2 μ m pixel pitch sensor with a two-way multiplexed pinned

photodiode, and with an average of 2.5 transistors per pixel. The photodiodes are fully depleted and use conventional transfer gate readout. The conventional version of this sensor, which features column-parallel ADCs and full ISP, is one of our standard products and has been optimized to achieve industry standard FSI performance. No mask or process changes (including implants) were made in the pixel area for this demonstration. The only additional masks were for through vias, backside bond pads and backside passivation. Device simulation with the unchanged imager fabrication process clearly shows the tradeoff between crosstalk and sensitivity as device thickness is varied. The 3.3 μ m we chose for this demonstration is close to our FSI epi thickness.

Performance Summary

Table 1 is a summary comparison between the front-illuminated and back-illuminated versions of the sensor (with the same fabrication process). Neither sensor has color filters. Table 1 clearly indicates the advantages of BSI. Unlike in previous work (5), broadband QE (81% for BSI) improved 2.7x over FSI. Other imaging parameters (such as dark current, full-well, PRNU) of the BSI sensor are comparable to or better than that of the FSI sensor. The mean dark current value and the hot pixel counts were similar for BSI and FSI devices, indicating a high quality back interface has been achieved without any post-thinning backside treatment.

Figure 7 compares standard images taken at varying illumination conditions. Note that a BSI image is nearly as bright as a corresponding FSI image with three times the incident illumination. Figure 8 shows the relative spectral response of the BSI sensor compared with the simulated transmission characteristics of the passivation/oxide/silicon stack on the backside. The shape of the relative QE curve is due to the non-optimized stack on the back side of the wafer, as shown by the similarity in shapes of the two curves. We attribute the difference in peak locations to the slight discrepancy between the actual sample stack thicknesses and nominal thicknesses used in the simulation. Figure 9 shows the estimated internal quantum yield (IQE), calculated by dividing the measured response by the stack transmission. As expected, IQE drops off with wavelength due to an increasing optical penetration depth.

Simulation shows that without any additional process optimization, electrical cross-talk of BSI would be inferior to that of FSI. This was also noted by (3), and is due to the absence of inter-pixel isolation, traditionally available in form of STI and implants for FSI, where the bulk of photoelectrons are generated near the front surface of the wafer. The deterioration in BSI MTF is obvious in figure 10, and is shown as a function of primary color in figure 11. As expected from simulation, shorter wavelengths exhibit higher cross-talk - a reversal of the conventional situation. Work is ongoing to improve BSI MTF.

Optical Considerations for BSI Sensors

The optimization techniques that apply to FSI sensors clearly have to be modified for BSI sensors. One example is optimization of optical transmission into the backside. As seen in the previous section, the presence of the BOX/silicon layer in the SOI wafer presents a fresh challenge for BSI. Creating an optically ideal backside AR stack without compromising dark current is a challenging requirement and is one area of ongoing work.

The quantum efficiency measured on a black and white BSI sensor without microlenses, as in the example presented here, is the upper limit of what can be achieved. It could be argued that the addition of microlenses and color filters will only serve to decrease the measured quantum efficiency on a BSI sensor. In a front side sensor, the expectation is that the addition of a microlens above the pixel increases quantum efficiency due to concentration of photons into the photodiode area and away from the metal lines that would otherwise block much of the illumination. In our demonstration (black and white) BSI sensor, all of the incident photons that are converted to electrons are counted as part of the signal, even those that are collected by pixels that are neighbors of the target pixel. Therefore there will not be a sensitivity advantage when microlenses are added – only a cross talk reduction advantage. In fact, there will be a sensitivity penalty since the optical efficiency of a microlens is rarely over 95%.

However, in practice we have found that microlens effectiveness is limited for conventional pixel sizes of 2.2 μ m and below. The addition of a microlens and color filter increases sensitivity by less than 10% for a 2.2 μ m pixel, implying that the microlens barely compensates for the signal loss due to the color filter material. A major reason for this is that diffraction effects at smaller pixel sizes limit the classical advantage of a microlens, as shown in the earlier optical section.

Conclusion

Manufacturing feasibility of a black and white BSI CMOS image sensor has been demonstrated using a special SOI starting wafer, with no degradation in dark current and sensitivity increase as expected. Differences in optical considerations between FSI and BSI and potential advantages of BSI have been analyzed.

References

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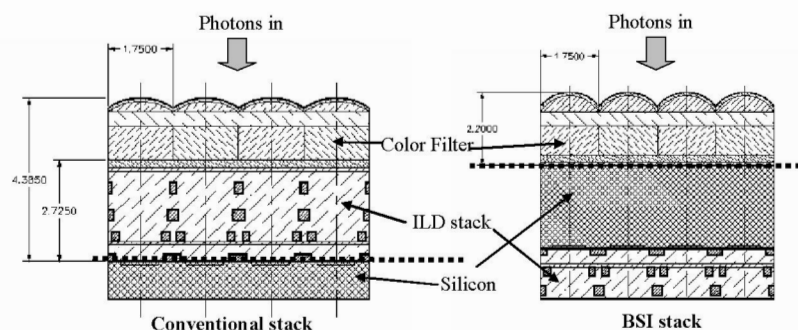


Figure 1: Schematic cross-sections of a front-illuminated (Conventional) and a back-illuminated imager (BSI) showing the optical stacks. The effective optical stack height (distance between microlens and absorbing silicon layer) is much smaller in the BSI case. The dotted line indicates the depth at which photon absorption begins. Dimensions are in microns.

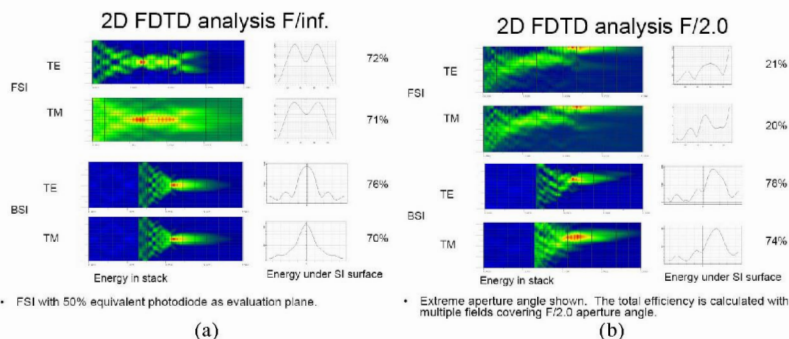


Figure 2: FDTD simulation of optical energy coupling into silicon conventional (FSI) and back-illuminated (BSI) imager under (a) normal incidence and (b) maximum incident angle for f/2.0 illumination. Even at the extreme edges of f/2.0 illumination, optical energy is well contained within the target pixel in the BSI case

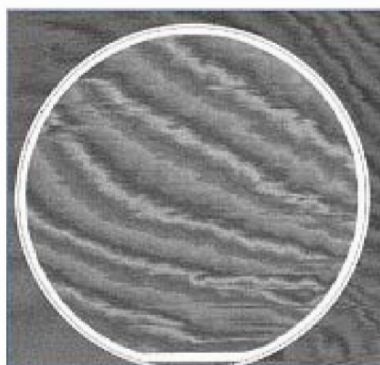


Figure 4: Acoustic micrograph of low-temperature oxide-oxide bonded interface between two 200 mm diameter wafer, revealing void-free bonding (courtesy of Ziptronix, Inc.)

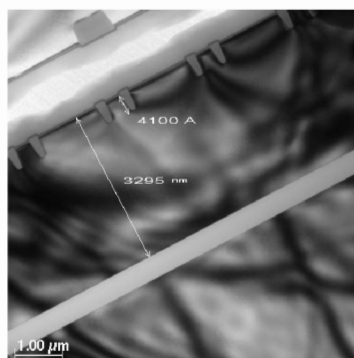


Figure 5: XSEM showing device, dielectric stack, BOX, and substrate layers of the finished SOI wafer, before removal of substrate silicon

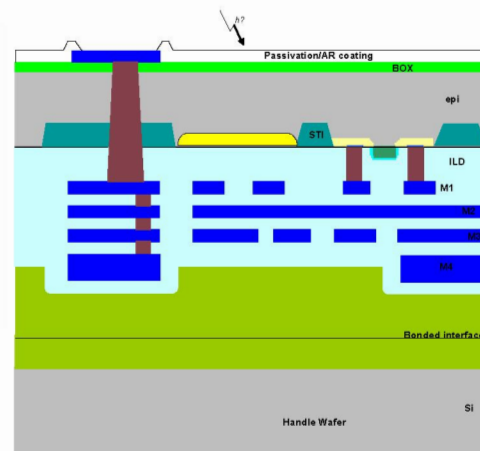


Figure 3 – Schematic cross-section of a black and white BSI sensor. The key features are the thermal oxide defining the end of the SOI device layer, the through-via providing electrical face-up connection, and the bonded handle wafer for mechanical support

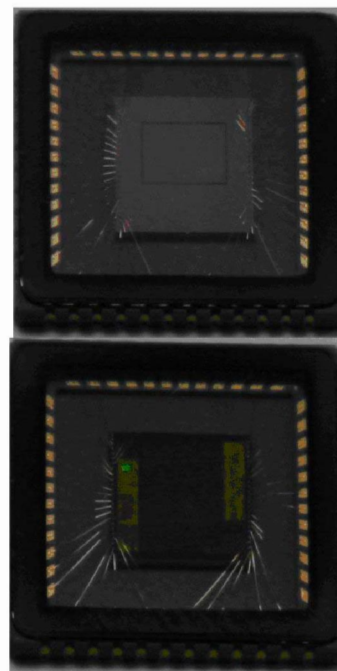


Figure 6: Picture of a packaged BSI sensor (top) next to equivalent FSI sensor (bottom) using most of the same masks. The wire bond patterns are mirror images of each other

Table 1: Measured Performance of the 2 Megapixel Back-Illuminated Imager

Parameter	BSI	FSI	Change	Units
Sensitivity (@FD, 3000 ⁰ K)	1.83	0.74	2.5x increase	V/lux-sec
QE (3000 ⁰ K)	81	30	2.7x increase	%
Full-well (linear)	16.5	13.0	26% increase	Ke ⁻
Dark Current (@ 60 ⁰ C)	126	116	8% increase	e ⁻ /pixel
Read noise	12.7	13.1	3% reduction	e ⁻
PRNU (@ 50% full-well)	1.85	1.83	unchanged	%
Dynamic Range	62.3	59.9	2.4 dB improvement	dB
Max.SNR	42.2	41.1	1.1 dB improvement	dB

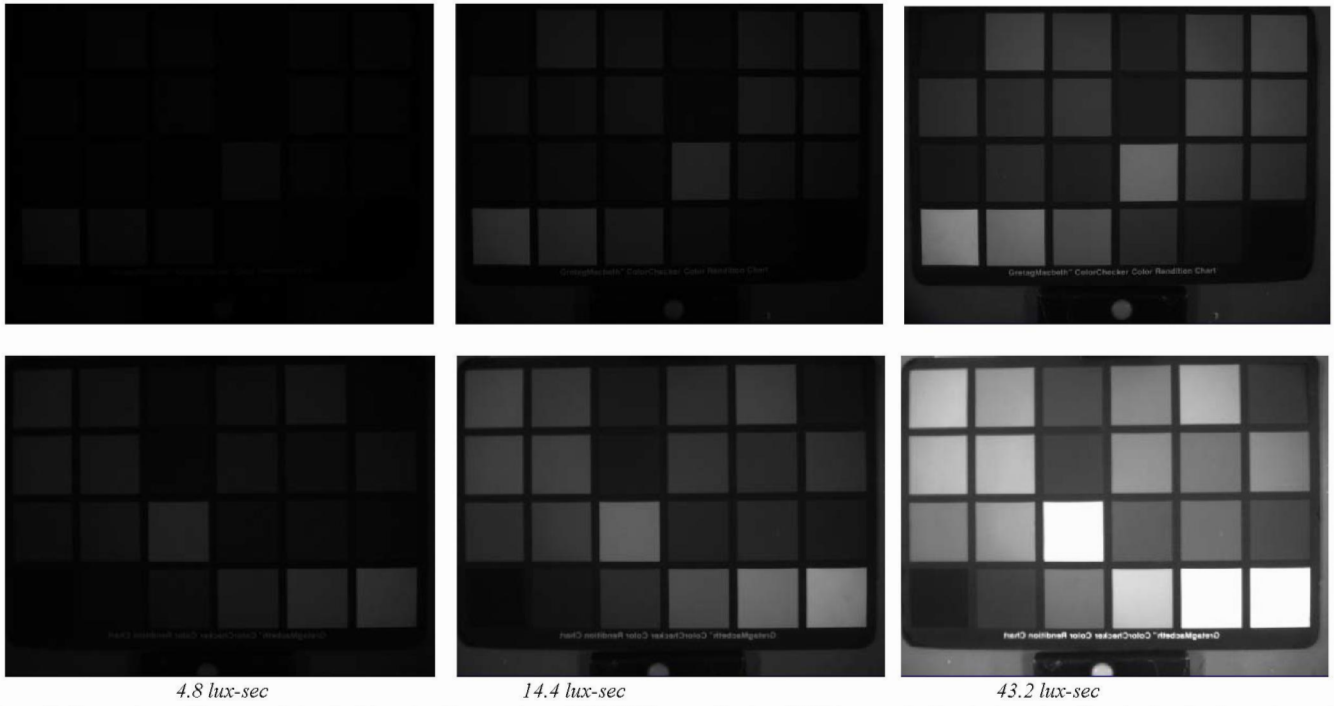


Figure 7: Comparison of images of standard target patterns using a 2MP FSI imager (top) and BSI imager (bottom) at varying illumination (unity analog and digital gain). Note that a BSI image is about as bright as an FSI image at 3X the illumination.

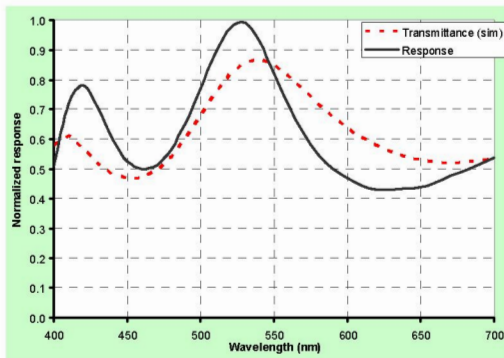


Figure 8: Relative spectral response of the BSI sensor (solid line) compared with the simulated transmission characteristics of the passivation/oxide/silicon stack (dashed line). The difference in peak locations is likely due to film thickness error in the simulation.

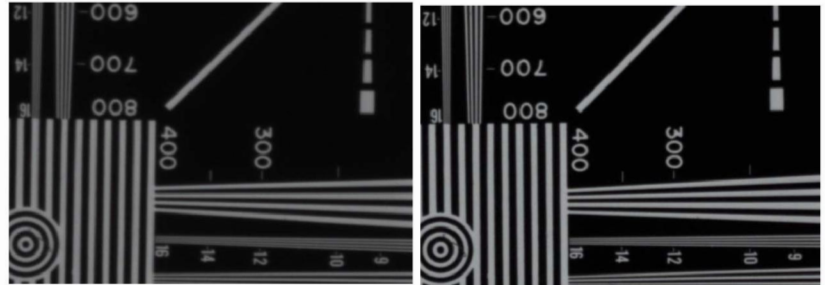


Figure 10: Resolving power comparison of BSI (left) and a FSI sensor (right). Note that BSI image is comparatively blurred (due to diffusion crosstalk).

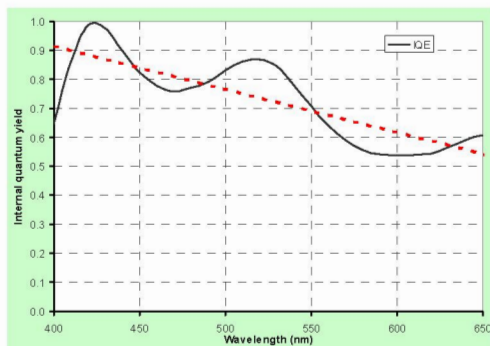


Figure 9: Relative internal quantum yield, after compensating for transmission characteristics. The dashed line is the simulated decrease in QE with wavelength, commensurate with device layer thickness

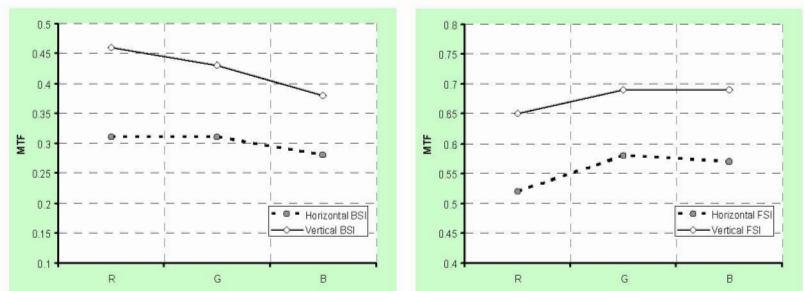


Figure 11: Horizontal and vertical components of modulation transfer function (MTF) for BSI (left) and FSI (right) as a function of illumination color