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Monolithic Pixel Sensors for Fast Particle Trackers in a Quadruple Well CMOS Technology

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Abstract—The Apse4well monolithic active pixel sensor (MAPS) chip prototype is meant as an upgrade solution for the Layer0 of the SuperB silicon vertex tracker. The design is based on a 180 nm CMOS process with quadruple well called INMAPS. This technology makes it possible to overcome the main drawbacks related to three transistors MAPS. Moreover, the presence of a high resistivity epitaxial layer is expected to lead to further improvements in terms of charge collection performance and radiation resistance. This paper, after giving some hints on the INMAPS process, focuses on the analog front-end section of the pixel readout chain. Measurement results on the main analog channel performance, like charge sensitivity and equivalent noise charge, are given along with charge collection efficiency evaluation through laser stimulation. These last characterization data were also used for validating TCAD simulation results of the sensor charge collection performance. Finally, results from a neutron irradiation campaign performed with fluences up to 2.7×10^{13} 1 MeV neutron equivalent/cm² will be shown and compared with the outcome of a Monte Carlo charge loss model of the structure useful for the rad-harder design of the next quadruple well MAPS.

Index Terms—CMOS MAPS, quadruple well process, low noise design, particle tracking.

I. INTRODUCTION

MONOLITHIC pixel sensors (MAPS) were initially proposed for application to the imaging field, where they are also referred to as CMOS APS (active pixel sensor) or as CIS (CMOS image sensors) [1]. In the last decade, their application to high energy physics experiments (like the International Linear Collider and the SuperB Factory) for the implementation of precise vertex particle trackers has been thoroughly investigated [2] [3]. One of the main advantages of the MAPS approach to particle tracking lies in the low material budget, which helps to reduce multiple scattering phenomena in multilayer tracking detectors. Actually, in MAPS devices both the detector and the readout electronics are integrated in the same silicon substrate. Moreover, the substrate can be safely ground down to a few tens of microns, since the

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operating principle of MAPS is based on the collection of charge diffusing in the mostly undepleted device bulk. The first MAPS approach ever considered adopts a small Nwell acting as a collecting electrode read out by a simple three NMOS transistors chain carrying the charge signal generated by a minimum ionizing particle (MIP) outside the pixel for further processing [4]. One of the main issues with this approach is that it can hardly be made compatible with the implementation of a pixel level sparsified readout architecture needed to comply with the large amount of data (and bandwidth requirements) expected in HEP experiments. The implementation of such an architecture actually entails the in-pixel integration of complex readout electronics, also including PMOS transistors. However, Nwells designed to host PMOS transistors, by acting as parasitic charge collectors, may degrade the pixel charge collection efficiency.

II. APSEL4WELL CHIP IN THE INMAPS PROCESS

In this work, a different approach for the implementation of MAPS, with the potential for overcoming drawbacks given by standard three transistor MAPS, is presented. The approach is based on a 180 nm CMOS planar technology with quadruple well called INMAPS in which, by means of an additional processing step, a high energy deep Pwell implant is deposited beneath the PMOS competitive Nwells (see Fig. 1) [5]. This implant represents a barrier for the charge diffusing in the epitaxial layer, preventing the carriers from being collected by the positively biased Nwells hosting the PMOS transistors of the in-pixel readout circuits. In this way, a theoretical charge collection efficiency of 100% can be reached. The NMOS transistors are designed in heavily doped Pwells located over

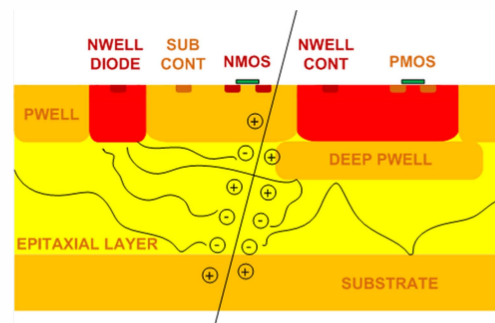


Fig. 1. Schematic cross section of a MAPS developed with INMAPS process.

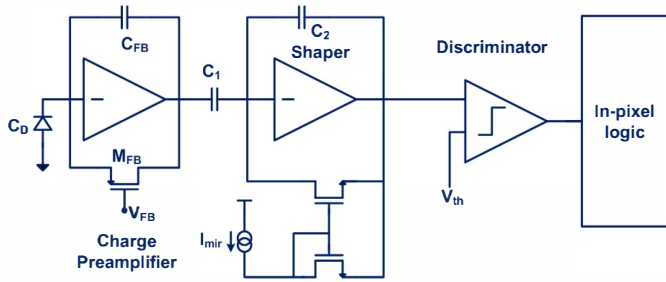


Fig. 2. Schematic of the Apse4well in-pixel readout chain.

a lightly P-doped epitaxial layer about $10\ \mu\text{m}$ thick, which has been grown upon a substrate featuring a doping in the order of $10^{18}\ \text{cm}^{-2}$. The epitaxial layer, featuring a resistivity higher than both the deep Pwell and the substrate, plays an important role in the improvement of the charge collection properties. The presence of two small potential barriers (deep Pwell/epitaxial layer or Pwell/epitaxial layer and epitaxial layer/substrate) keeps the carriers within the epitaxial layer, preventing them from diffusing through the substrate. The foundry provides different options for epitaxial layer resistivity and thickness. For the fabrication of the Apse4well chip, which is the subject of this work, three different epitaxial layer typologies have been adopted:

- $5\ \mu\text{m}$ thick standard resistivity (about $10\ \Omega\cdot\text{cm}$) epitaxial layer;
- $12\ \mu\text{m}$ thick standard resistivity epitaxial layer;
- $12\ \mu\text{m}$ thick high resistivity (about $1\ \text{k}\Omega\cdot\text{cm}$) epitaxial layer.

The Apse4well version fabricated with the high resistivity epitaxial layer is expected to give the best performance in terms of charge collection speed and amount of the collected charge, thanks both to the larger depleted volume under the inversely biased collecting electrode and to the larger lifetime of the charge carriers. Moreover, the adoption of a high resistivity epitaxial layer is expected to improve the device tolerance to bulk damage [6].

The Apse4well pixel features a $50\ \mu\text{m}$ pitch, complying with the requirements of the innermost layer (the Layer0) of the SuperB silicon vertex tracker (SVT). The collecting electrode consists of 4 interconnected Nwell square diodes, each with a $1.5\ \mu\text{m}$ side, and is read out by the charge-voltage conversion chain represented in Fig. 2. The first block of this channel is a charge preamplifier with a feedback capacitance C_{FB} continuously discharged by a PMOS transistor biased in the deep subthreshold region. The charge preamplifier is followed by a shaping stage. It features a feedback network which includes a current mirror scheme to discharge the capacitance C_2 by means of a constant current, proportional to I_{MIR} . The waveform at the output of the shaping stage is then compared to a global threshold voltage by means of a threshold discriminator. The in-pixel logic has been designed in order to enable a sparsified readout of the matrix with time stamping capabilities, in order to comply with the high background rate specifications of Layer0, including a hit rate of $100\ \text{MHz}/\text{cm}^2$ and a timestamp period of $1\ \mu\text{s}$. The out-of-pixel readout (not

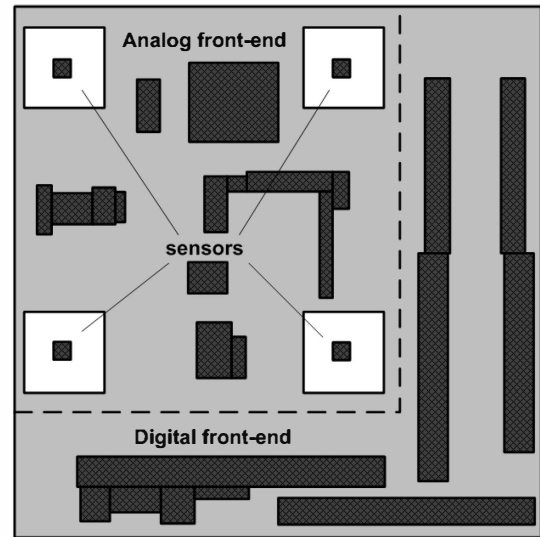


Fig. 3. Simplified layout of the Apse4well pixel: deep Pwell layer (light grey) and Nwells (dark grey).

shown in Fig. 2) can operate both in datapush and in triggered mode. The behavior of the digital readout architecture has been simulated in both the operating modes. Its efficiency in triggered mode operation is higher than 98% with a time stamp granularity down to $100\ \text{ns}$, a latency of $6\ \mu\text{s}$ and the required $100\ \text{MHz}/\text{cm}^2$ target hit rate [7].

Besides the 32×32 matrix implementing the sparsified readout architecture, the Apse4well chip also includes analog 3×3 pixel matrices and single channels for an accurate characterization of the analog readout and of the charge collection properties of the sensors. The characterization of the analog front-end and of the sensor charge collection performance represent the main concern of this work. Figure 3 shows the simplified layout of the Apse4well pixel. The 4 squared Nwell diffusions acting as sensors are laid out at the corner of the area including the analog front-end. The digital front-end has been designed along two sides of the pixel and is separated by the analog section by means of a metal guardring (not shown in the figure) in order to minimize coupling phenomena which could be harmful for the correct analog front-end operation. The deep Pwell layer (light grey) has been deposited all over the pixel, except for the area underneath the collecting electrodes, in such a way to isolate the Nwell diffusions (dark grey) hosting the PMOS transistors from the epitaxial layer.

III. APSE4WELL ANALOG FRONT-END PERFORMANCE

The analog front-end performance of the Apse4well readout channel was studied through the characterization of the analog channels included in the 3×3 sensor matrices. The charge sensitivity has been measured by injecting a $1\ \text{kHz}$ square waveform with varying amplitude at the input of the central pixel of the 3×3 matrix, featuring an injection capacitance C_{inj} with a nominal value of $30\ \text{fF}$. The relationship between the waveform amplitude V_{in} and the injected charge Q_{inj} is expressed as follows:

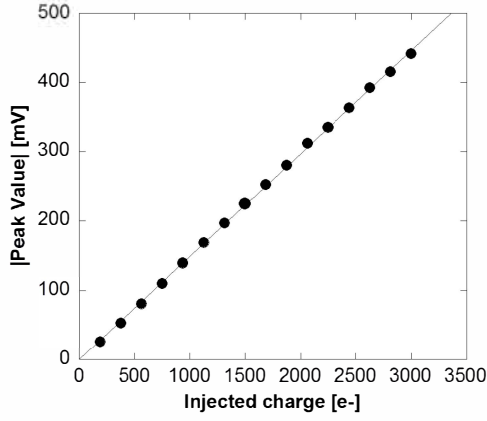


Fig. 4. Peak value of the shaper output voltage as a function of the injected charge for chip 42.

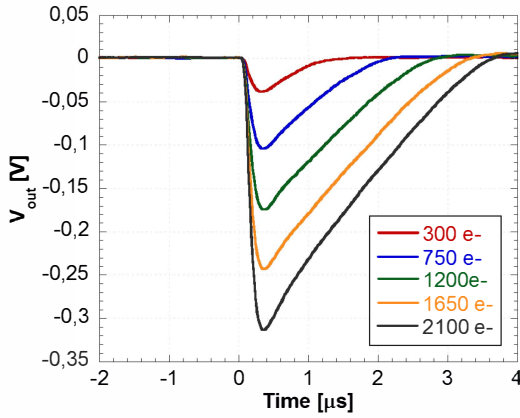


Fig. 5. Shaper output waveforms from a channel in chip 2 at varying input charge.

$$Q_{inj} = C_{inj} \cdot V_{in}. \quad (1)$$

The charge sensitivity of the tested sample is expressed as the slope of the straight line interpolating the input-output characteristic of the analog channel. As an example, Fig. 4 shows the input-output characteristic of the sample chip 42, featuring a 12 μm thick high resistivity epitaxial layer. The charge sensitivity of the tested samples ranges from about 900 mV/fC to 1100 mV/fC. In particular, it has been found that the samples fabricated with a standard resistivity epitaxial layer (both 5 and 12 μm thick) feature a charge sensitivity mean value of 940 mV/fC, while chips fabricated with the high resistivity epitaxial layer option show a value about 10-15% higher. This phenomenon might be due to slight differences in the channel doping profile of the MOS transistors in the two types of epitaxial layers, which can lead to variations in the I-V characteristic. Figure 4 also shows a good linearity of the characteristic up to about 3000 electrons. The integral non-linearity (INL) of the tested chips ranges from 1.5 to 2%. Figure 5 shows the shaper output waveform from a channel in chip 2 at varying input charge. The varying peaking time, here about 300 ns, depends on the mirror feedback configuration of the

TABLE I
SUMMARY OF THE ANALOG FRONT-END PERFORMANCE.

Performance	Value
Charge sensitivity	900-1100 mV/fC
ENC ($C_T=42$ fF)	27 e^-
INL	2%
Pixel current dissipation	10 μA
Analog power consumption	18 $\mu\text{W/pixel}$
Analog power dissipation	0.7 W/cm ²

shaper, which, as already mentioned, discharges the feedback capacitance C_2 with a constant current (equal to about 2 nA). The ENC is a figure of merit for analog processors, defined as the charge to be injected at the input of a charge measurement system to have a peak response as high as the output root mean square noise [8]. It can be operationally defined by means of the ratio between the root mean square value of the noise voltage at the output of the shaper and the charge sensitivity of the analog channel. The tested samples feature a mean value of the ENC of 27 electrons with a front-end input capacitance C_T of 42 fF. This capacitance accounts for the contributions from the gate capacitance of the charge preamplifier input device (12 fF), the parasitic capacitance of the 4 inversely biased Nwells acting as collecting electrodes (15 fF) and the metal lines interconnecting the 4 electrodes (15 fF). The analog current consumption of the pixel is 10 μA . About one half of this current is dissipated in the input device of the charge preamplifier in order to optimize noise performance of the system. Since the chip supply voltage is 1.8 V, the analog power consumption is 18 μW per pixel. Considering a pixel area of 50x50 μm^2 , the analog power dissipation density is about 0.7 W/cm². The estimated contribution to the power dissipation density given by the digital front-end is 0.8 W/cm², leading to an overall power dissipation of 1.5 W/cm², lower than the maximum value of 2 W/cm² imposed by the Layer0 requirements. Table I summarizes the performance of the ApSel4well analog readout.

IV. APSEL4WELL CHARGE COLLECTION PROPERTIES

The charge collection properties of the ApSel4well MAPS have been evaluated by testing the 3x3 matrices. Two different measurement techniques have been adopted: the first one relies upon the use of an infrared laser source, while the second one exploits a ⁹⁰Sr/⁹⁰Y radioactive source. The first technique is more suitable for the evaluation of the charge collection uniformity inside the individual pixel, while the second can be used to measure the amount of charge collected by a single pixel or a cluster, and estimate the MAPS response to a MIP. Figure 6 shows the charge collection plots relevant to pixels fabricated on a 5 μm thick standard resistivity epitaxial layer. This measurements have been obtained by using an infrared laser featuring a 1064 nm wavelength and a Gaussian intensity profile at the output of the focuser with a standard deviation of about 3 μm in both dimensions of the plane transversal to the beam direction. The laser beam position and movement is controlled by means of a precision scanning system. The samples were illuminated from the back side in order to avoid reflections from the intricate net of metal interconnections laid

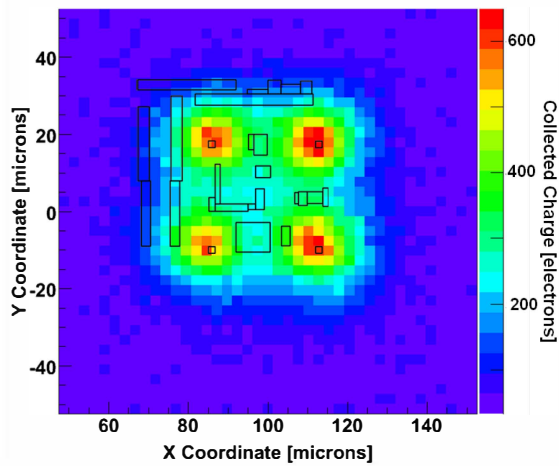
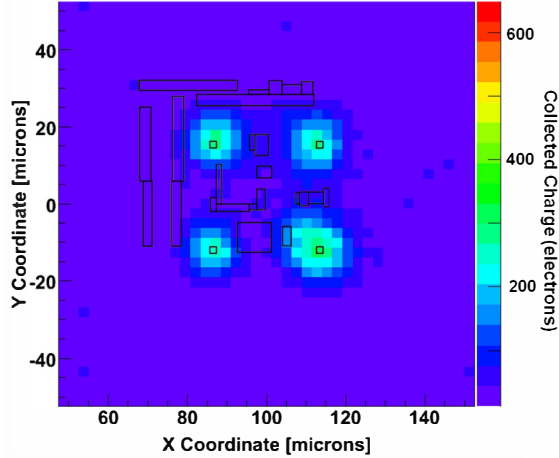


Fig. 6. Collected charge as a function of the laser beam position in a pixel designed without deep Pwell (top) and with deep Pwell (bottom). Both the pixel have been fabricated on a $5\text{ }\mu\text{m}$ thick standard resistivity epitaxial layer. Nwells from layout are superimposed to the plots.

out on the top of the chip. The upper plot in Fig. 6 shows the charge collected by the central pixel of a 3×3 matrix designed without the deep Pwell layer, while the lower plot is relevant to a pixel with the deep Pwell. Nwells from layout are superimposed to the charge collection plots. In the pixel without deep Pwell the charge collection is confined around the collecting electrode. On the other hand, in the case of the pixel with deep Pwell, a significant amount of charge is collected also when the laser beam is not close to the electrodes. This result proves the effectiveness of the deep Pwell in shielding the competitive Nwells from the epitaxial layer. Note also that the peak value of the collected charge in the pixel without deep Pwell drops to about 50% of the peak of the charge collected by the pixel with the deep Pwell implant.

Figure 7 shows the charge collection measurements performed on two 3×3 matrices belonging to two samples (chip 1 and 32) with a standard resistivity 5 and $12\text{ }\mu\text{m}$ thick epitaxial layer, respectively. This results have been obtained by using a $^{90}\text{Sr}/^{90}\text{Y}$ source, whose measurement setup is shown in [10].

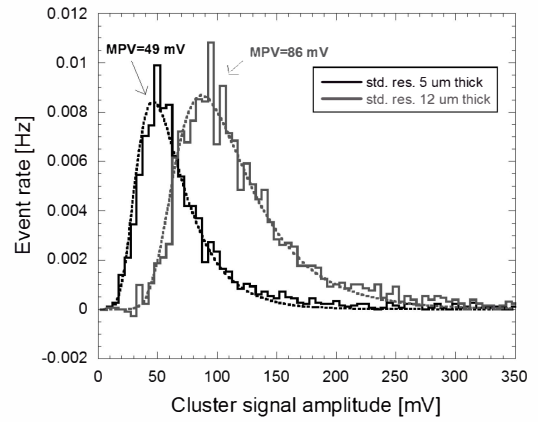


Fig. 7. Event rate distribution in two 3×3 matrices belonging to chip 1 ($5\text{ }\mu\text{m}$ thick epitaxial layer) and chip 32 ($12\text{ }\mu\text{m}$ thick epitaxial layer) tested with a $^{90}\text{Sr}/^{90}\text{Y}$ source.

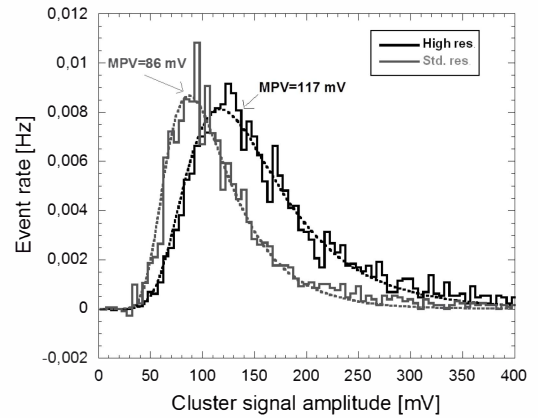


Fig. 8. Event rate distribution in two 3×3 matrices belonging to chip 32 (standard resistivity epitaxial layer) and chip 42 (high resistivity epitaxial layer) tested with a $^{90}\text{Sr}/^{90}\text{Y}$ source.

Based on the spectral characteristic of $^{90}\text{Sr}/^{90}\text{Y}$ decay, about 50% of the released electrons are minimum ionizing particles (MIPs) and produce the distinct Landau distributions shown in Fig. 7. The most probable value (MPV) of these distributions is proportional to the charge collected by the 3×3 cluster. It can be observed that the charge collected by chip 32 featuring a $12\text{ }\mu\text{m}$ thick epitaxial layer is about two times higher than the charge collected by chip 1 featuring a $5\text{ }\mu\text{m}$ standard resistivity epitaxial layer. This result is quite reasonable, since the charge collected by the cluster is almost proportional to the epitaxial layer thickness, at least in the considered thickness interval. This can be explained with the fact that the charge collected by the cluster is the one generated in the epitaxial layer, since in the heavily doped substrate the charge generated by a MIP tends to recombine due to the lower lifetime.

Figure 8 shows the Landau shaped distribution relevant to two samples (chip 32 and chip 42) with a $12\text{ }\mu\text{m}$ thick epitaxial layer featuring standard and high resistivity, respectively. As expected, the charge collected by chip 42, featuring a high resistivity epitaxial layer, is about 35% higher than chip 32 featuring a standard resistivity epitaxial layer instead, leading

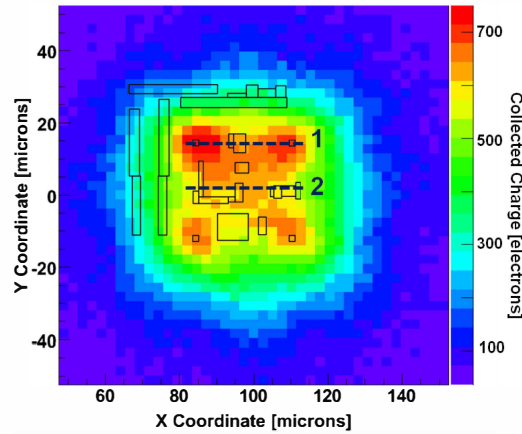


Fig. 9. Collected charge as a function of the laser beam position in the central pixel of the 3×3 matrix of chip 42. N-wells from layout are superimposed to the plot.

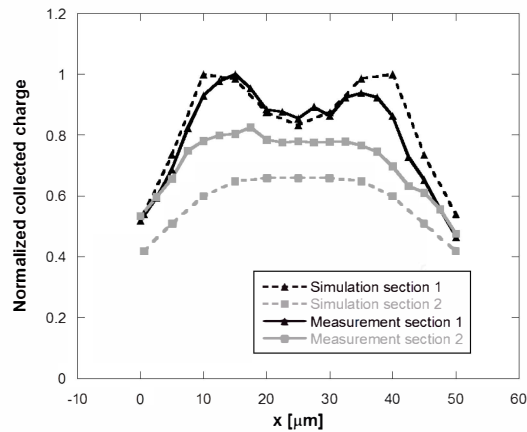


Fig. 10. Comparison between simulation and measurement results of the charge collected normalized to the peak value in the two sections of the 3×3 matrix central pixel shown in Fig. 9.

to a signal-to-noise ratio for chip 42 slightly lower than 30. The better performance of chip 42 can be easily explained with the larger depleted volume and the larger carrier lifetime in the epitaxial layer. The central pixel of the 3×3 matrix of chip 42 has also been characterized by means of the infrared laser source in order to evaluate the charge collection uniformity of a pixel fabricated on a $12 \mu\text{m}$ thick high resistivity epitaxial layer. The measurement results, shown in Fig. 9 feature a higher charge collection uniformity and collected charge peak with respect to the case of the MAPS sensor on a $5 \mu\text{m}$ thick standard resistivity epitaxial layer shown in the bottom of Fig. 6. This result points to the fact that, as expected, the amount of the collected charge is supposed to increase with the epitaxial layer thickness. Moreover, the higher resistivity of the epitaxial layer leads to an increase of the depleted volume under the collecting electrodes and of the charge carriers lifetime. This in turns increases the probability of the charge generated by the impact of a MIP in the pixel center of being collected by one of the four sensors.

The laser test results have been compared to the outcomes from physical device simulations performed by means of the Synopsys TCAD software package [9]. The simulations have been carried out on a structure modeling the Apsel4well 3×3 matrix with deep Pwell layer and a $12 \mu\text{m}$ thick high resistivity epitaxial layer. Comparison between simulation results and measurements relevant to the charge collected normalized to the peak value along the cross-sections 1 and 2 shown in Fig. 9 and normalized to the peak value is shown in Fig. 10. Quite a good agreement can be detected in the case of the cross-section passing through the collecting electrodes, while in the case of the other path, the simulation results seem to underestimate the amount of charge collected, though the charge collection trend along the x coordinate is quite similar to the experimental data.

V. APSEL4WELL BULK DAMAGE TOLERANCE

Sensors designed for application to the Layer0 of the SuperB SVT are required to withstand a fluence of 5×10^{12} 1 MeV neutron equivalent/ cm^2 per year, plus a safety factor of 5. In order to evaluate the bulk damage tolerance of the Apsel4well MAPS, different samples featuring a $12 \mu\text{m}$ thick standard and high resistivity epitaxial layer have been irradiated with neutrons from a Triga Mark II nuclear reactor at the Josef Stefan Institute in Ljubljana with fluences up to 2.7×10^{13} 1 MeV neutron equivalent/ cm^2 . The characterization of the irradiated chips involved both the analog front-end performance and the charge collection properties.

A. Effects on the analog front-end performance

Figure 11 shows the charge sensitivity (Gq) and the ENC of Apsel4well chips featuring a $12 \mu\text{m}$ thick epitaxial layer as a function of the fluence. The figure on the top shows the results in the case of a standard resistivity epitaxial layer. As expected, both the Gq and the ENC do not show any clear trend with the fluence. Actually, both Gq and ENC depend on the characteristics of MOSFETs making up the analog front-end. Since MOSFET operation principle is based on the drift of majority carriers in the surface region of the silicon substrate, its performance are not expected to change after irradiation with neutrons, whose damage effects are mainly confined in the device bulk. In the case of devices with high resistivity epitaxial layer, shown on the bottom of the figure, a 10% charge sensitivity drop can be detected after the last irradiation step. This might be explained with an increase of the leakage current of the detector, which affects the charge preamplifier gain by reducing its feedback impedance (i.e., by increasing the transconductance of transistor M_{FB} in Fig. 2). The fact that this phenomenon is detectable only in devices featuring a high resistivity epitaxial layer can be ascribed to the larger depleted volume under the collecting electrodes, which leads to a larger contribution of the radiation induced generation component to the overall leakage current in the collecting electrodes. As far as the ENC is concerned, like in the case of standard resistivity epitaxial layer, no particular trend with the fluence can be clearly detected. Fluctuations in the ENC are likely to be due to process variations, as the

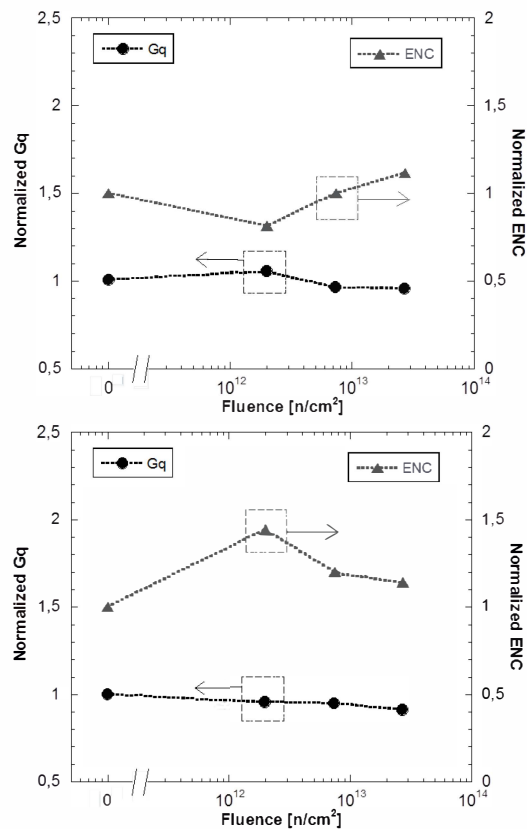


Fig. 11. Gq and ENC as a function of the fluence for samples featuring standard (top) and high resistivity (bottom) epitaxial layer.

points in Fig. 11 were obtained from the characterization of different samples irradiated at different fluences.

B. Effects on the charge collection properties

The effects of neutron irradiation on the charge collection properties of the Apsel4well MAPS have been evaluated by means of measurements with infrared laser and ⁹⁰Sr/⁹⁰Y radioactive sources. As an example, Fig. 12 shows the charge collection plot (obtained by means of infrared laser measurements) relevant to the central pixel of the 3×3 matrix belonging to a sample featuring a 12 μm thick high resistivity epitaxial layer after irradiation with 2.7×10^{13} 1 MeV neutron equivalent/cm². As compared to the results shown in Fig. 9, relevant to a non-irradiated chip with the same epitaxial layer characteristics as the device in Fig. 12, a 35% drop in the charge collected peak with respect to the pre-irradiation value can be detected at the considered fluence. More information on the normalized collected charge as a function of the fluence can be found in Fig. 13, both for chips featuring a standard and a high resistivity epitaxial layer. The beneficial effects of using a high resistivity epitaxial layer are evident. Actually, the charge collection drop experienced by the chips with standard resistivity epitaxial layer approaches 70% of the pre-irradiation value at the last irradiation step, to be compared to the 35% drop shown by the chip with the high resistivity option. In both the cases, the signal loss is correlated with the recombination of charge at neutron-induced lattice defects [11]. The results

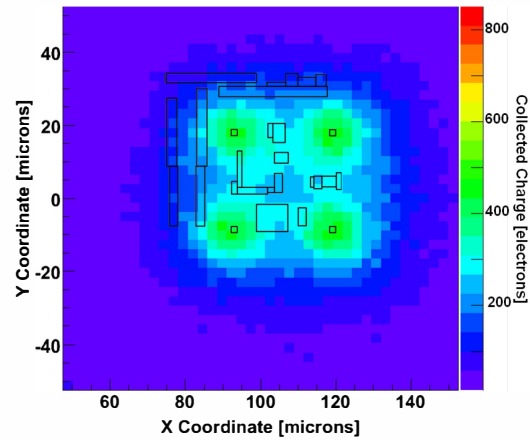


Fig. 12. Collected charge as a function of the laser beam position in the central pixel of the 3×3 matrix of chip 42 after irradiation with 2.7×10^{13} 1 MeV neutron equivalent/cm².

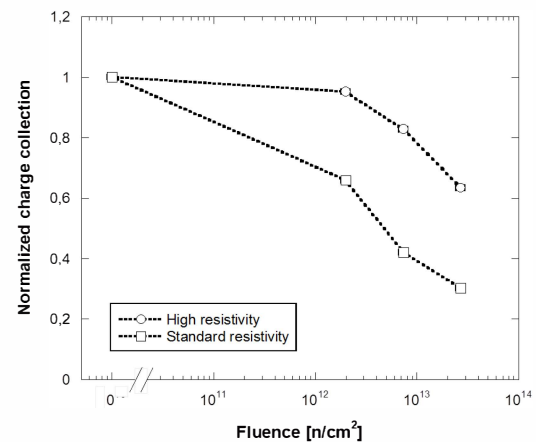


Fig. 13. Collected charge normalized to the pre-irradiation peak value as a function of the fluence (IR laser tests).

shown in Fig. 13 also confirm the higher degree of radiation tolerance offered by high resistivity substrates.

Results obtained from measurements performed with infrared laser tests are in qualitative agreement with the outcomes of the tests performed with ⁹⁰Sr/⁹⁰Y radioactive sources. Figure 14 shows the Landau shaped distributions relevant to Apsel4well samples featuring a 12 μm thick high resistivity epitaxial layer irradiated with different fluences. The variation in the MPV of the curve after irradiation is consistent with a degradation in the charge collection properties of the sensor. A drop in the order of 50% after irradiation with 2.7×10^{13} n/cm² can be detected in the amount of collected charge. In order to improve the design from the standpoint of the bulk damage tolerance, a purposely developed a Monte Carlo model [12] has been used to predict the charge collection loss in CMOS monolithic sensors after irradiation with heavy particles. The model has been validated through comparison between simulations and measurement results relevant both to the Apsel4well sensor and to the Apsel3T1 deep N-well MAPS [13] [10]. The bulk

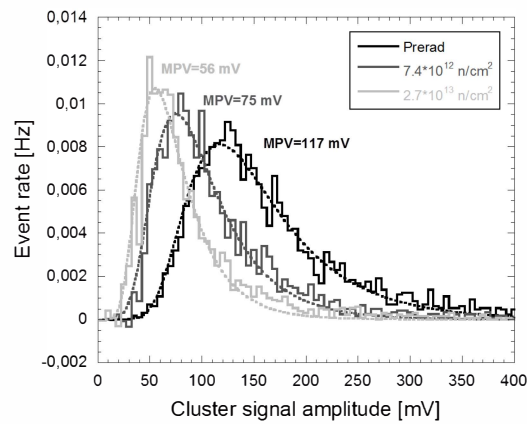


Fig. 14. Event rate distribution at varying neutron fluences relevant to Apsel4well samples with high resistivity epitaxial layer.

damage tolerance of an Apsel4well-like MAPS is expected to improve by increasing the depleted volume under the collecting electrode, since in this region the charge carriers move by drift instead of by diffusion, and are more likely to escape recombination. With the adopted front-end architecture, actually, at this moment, it is not possible to completely deplete the epitaxial layer by applying a high reverse voltage between the collecting electrodes and the substrate. A suitable solution to reach the goal of a higher radiation tolerance might be to increase the area of the collecting electrodes. Figure 15 shows the normalized MPV (black markers) of the ^{90}Sr spectra as a function of the fluence on chips with high resistivity epitaxial layer. The same figure shows the simulation results based on the above mentioned Monte Carlo model, relevant to the charge collected by an Apsel4well MAPS with the same sensor layout and with double collecting electrode area. First of all, a quite good agreement can be noticed between experimental data and the outcome of the simulation of the as designed Apsel4well pixel sensor. Figure 15 also shows that, by doubling the collecting electrode area, a 10% reduction in the charge collection drop can be found at the highest fluence step.

VI. CONCLUSION

In this paper, the design and the characterization of MAPS devices developed in the 180 nm CMOS INMAPS process have been presented and discussed. The technology features a deep Pwell implant which can significantly improve the charge collection efficiency of MAPS with respect to other CMOS planar processes by removing the parasitic collection action of N-type diffusions. The technology also offers a high resistivity epitaxial layer option, which is expected to improve both the charge collection properties of the sensor and its bulk damage tolerance. This prototype sensor has been designed for application to the Layer0 of the SuperB Factory SVT. For this reason, the pixel matrix implements a digital sparsified readout architecture with time stamping capability, designed to comply with the hit rate foreseen for this application. The analog front-end has been tested in terms of charge sensitivity and ENC by means of charge injection techniques. The charge collection

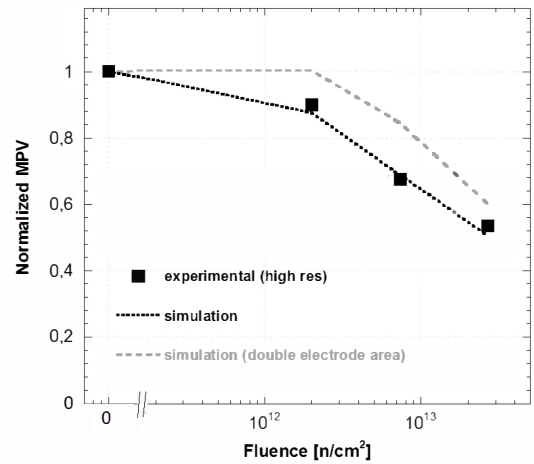


Fig. 15. Normalized MPV as a function of the fluence relevant both to measurements and simulations of a Apsel4well MAPS with high resistivity epitaxial layer and varying collecting electrode area (measurement data from ^{90}Sr tests).

properties of the Apsel4well MAPS have been evaluated both by stimulating the sensor with an infrared laser and through spectral measurements with $^{90}\text{Sr}/^{90}\text{Y}$ radioactive sources. The Apsel4well sensor fabricated on a 12 μm thick high resistivity epitaxial layer has been proven to be by far the best solution among different available options in terms both of the amount of collected charge and of charge collection uniformity. Also, Apsel4well samples have been irradiated with neutrons up to a fluence of $2.7 \times 10^{13} \text{ cm}^{-2}$. No significant variations have been found in the Apsel4well analog front-end performance after irradiation, except for a slight reduction of the charge sensitivity in the samples with a high resistivity epitaxial layer, likely due to an increase in the sensor leakage current. The charge collection drop after irradiation in the devices with standard resistivity epitaxial layer at the maximum fluence was found to be about twice that of chips with the high resistivity option, proving the effectiveness of a higher resistivity epitaxial layer in increasing the bulk damage tolerance. Based on a purposely developed Monte Carlo model, the tolerance can be further improved by increasing the collecting electrode area. The design optimization will be carried out paying attention to its implication on the device noise performance. Finally, an irradiation campaign with γ -rays will be performed to test the Apsel4well tolerance to ionizing radiation.

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