

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR
MANUFACTURING COMPANY LIMITED,
Petitioner,

v.

ALIDDOUBLE, INC.,
Patent Owner.

IPR2023-00369
Patent 9,356,169 B2

Before KRISTINA M. KALAN, CHRISTOPHER M. KAISER, and
JEFFREY W. ABRAHAM, *Administrative Patent Judges*.

KALAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Taiwan Semiconductor Manufacturing Company Limited (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1–20 of U.S. Patent No. 9,356,169 B2 (Ex. 1001, “the ’169 patent”). Alidouble, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 6, “Prelim. Resp.”).

To institute *inter partes* review, we must determine that the information presented in the Petition shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). For the reasons discussed below, after considering the parties’ submissions and the evidence of record, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one claim of the ’169 patent, and we institute *inter partes* review on all challenges raised in the Petition. 37 C.F.R. § 42.108 (2022).

A. *Related Proceedings*

The parties identify the following district court litigation as related matters: *Alidouble Inc. v. Taiwan Semiconductor Manufacturing Company Ltd.*, No. 2:22-cv-00298-JRG (E.D. Tex.) (pending) (“parallel District Court litigation”); *Alidouble Inc. v. Taiwan Semiconductor Manufacturing Company Ltd.*, No. 2:21-cv-00452-JRG (E.D. Tex.) (dismissed). Pet. 82; Paper 3, 2 (Patent Owner’s Mandatory Notices).

B. *Real Parties-in-Interest*

Petitioner identifies Taiwan Semiconductor Manufacturing Company Limited as the real party-in-interest. Pet. 82. Patent Owner identifies Alidouble Inc. as the real party-in-interest. Paper 3, 2.

C. The '169 Patent

The '169 patent is titled “Apparatus, System and Method of Back Side Illumination (BSI) Complementary Metal-Oxide-Semiconductor (CMOS) Pixel Array” and relates to image sensors for imaging devices, e.g., cameras. Ex. 1001, code (54), 1:23–25. As described by the '169 patent, an image sensor may include a pixel array having a plurality of pixels. *Id.* at 1:26–27. A pixel may include a photodiode that converts light from the image to an electronic signal for image processing, as well as transistors for performing computational operations. *Id.* at 1:27–30, 3:26–36, 4:19–22. The image sensor may be formed on a wafer, e.g., a substrate, using a Complementary Metal-Oxide-Semiconductor (CMOS) technology. *Id.* at 1:30–32. A Back Side Illumination (BSI) CMOS image sensor is illuminated from the back side of the wafer. *Id.* at 1:33–36.

According to the '169 patent, a pixel may have poor collection efficiency and reduced performance when photogenerated electrons are absorbed not by the photodiode, but by well regions of the transistors, which act as parasitic photodiodes. *Id.* at 4:41–5:23. The '169 patent seeks to address this problem by including a barrier layer that covers the transistor well regions to reduce or prevent diffusion of the photogenerated electrons to the transistor well regions. *Id.* at 5:57–60, 6:53–60.

Figure 2 of the '169 patent is reproduced below.

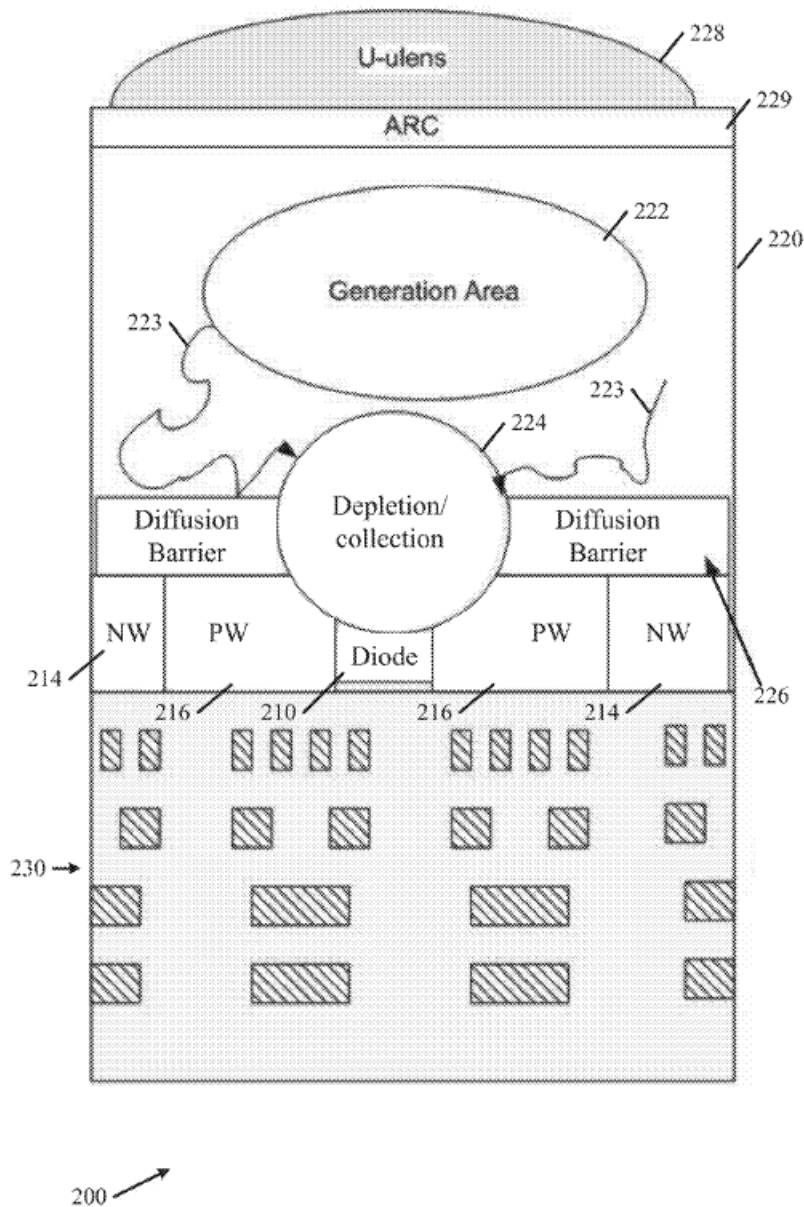


Fig. 2

Figure 2 of the '169 patent is a schematic illustration of a BSI CMOS pixel 200. *Id.* at 7:66–8:22. As shown in Figure 2, pixel 200 includes MOS transistors with N-well regions 214 and P-well regions 216, photodiode 210, epitaxial layer 220 including absorption area 222 and collection area 224,

and barrier layer 226. *Id.* at 8:8–38. Absorption area 222 absorbs incoming photons and generates electrons 223 responsive to absorbed photons, and collection area 224 connects absorption area 222 to photodiode 210 to provide electrons 223 from absorption area 222 to photodiode 210. *Id.* at code (57). Barrier layer 226 separates absorption area 222 from well regions 214, 216 to prevent diffusion of electrons 223 to well regions 214, 216. *Id.* at 6:53–60, 8:25–28.

D. Illustrative Claim

Claims 1, 16, and 19 are independent. Claim 1 is reproduced below.

1. [1pre] A back-side illumination (BSI) complementary metal-oxide-semiconductor (CMOS) pixel array comprising:
 - [1a] a plurality of pixels, a pixel of said plurality of pixels comprising:
 - [1b] one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-Well (NW) region or a P-well (PW) region;
 - [1c] a photodiode;
 - [1d] an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and
 - [1e] a barrier layer separating said absorption area from said one or more well regions.

Ex. 1001, 15:42–58 (bracketed designations added by Petitioner).

E. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability.

Ground	Claims Challenged	35 U.S.C. § ¹	Reference(s)/Basis
1	1–6, 10–15	103	Lauxtermann ²
2	2, 6, 7, 9	103	Lauxtermann, Zucca ³
3	10, 11	103	Lauxtermann, Akiyama ⁴
4	16–20	103	Lauxtermann, Wang ⁵
5	1, 3–8, 12–15	103	Ballin ⁶
6	10, 11	103	Ballin, Akiyama

In support of its unpatentability arguments, Petitioner relies on the declaration of Dr. Konstantinos P. Giapis. Ex. 1003.

II. ANALYSIS

A. Claim Construction

We apply the claim construction standard articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). 37 C.F.R. § 42.100(b). Under *Phillips*, claim terms are afforded “their ordinary and customary meaning.” *Phillips*, 415 F.3d at 1312. The “ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Id.* at 1313. Only terms that are in controversy need to be construed, and then

¹ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. § 103. Because the ’319 patent has an effective filing date after the effective date of the applicable AIA amendments, we refer to the post-AIA version of § 103.

² US 7,498,650 B2, issued March 3, 2009 (Ex. 1004).

³ S. Zucca et al., *Monolithic Pixel Sensors for Fast Particle Trackers in a Quadruple Well CMOS Technology*, 2012 IEEE Nuclear Science Symposium and Medical Imaging Conference Record (Ex. 1005).

⁴ US 8,076,172 B2, issued December 13, 2011 (Ex. 1006).

⁵ US 8,531,565 B2, issued September 10, 2013 (Ex. 1010).

⁶ J. Ballin et al., *Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixels*, Sensors 2008, 8, 5336–5351 (Ex. 1007).

only to the extent necessary to resolve the controversy. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

Petitioner “does not believe the claim terms need to be construed to resolve the prior art issues presented in [the] Petition.” Pet. 10 (citing Ex. 1003 ¶ 70). Patent Owner “reserves the right to advance its own construction for any claim term should an IPR be instituted.” Prelim. Resp. 7.

We determine we need not expressly construe any claim term at this stage of the proceeding. *See Realtime Data*, 912 F.3d at 1375.

B. Level of Ordinary Skill in the Art

Petitioner asserts that one of ordinary skill in the art “would have been a person having a Master’s degree in electrical engineering, material science, physics, or other related disciplines with at least three years of industry experience in integrated circuit design, layout, packaging or fabrication” and that a “greater level of experience may compensate for less education and vice versa.” Pet. 10 (citing Ex. 1003 ¶¶ 66–68). Patent Owner “reserves the right to dispute Petitioner’s definition of a POSA if an IPR is instituted.” Prelim. Resp. 7.

Accordingly, for the purposes of this Decision, we adopt Petitioner’s proposal regarding the level of one of ordinary skill in the art. The level of ordinary skill in the art is also reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

C. Discretion under 35 U.S.C. § 314(a)

Institution of *inter partes* review is discretionary. *See Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he [U.S. Patent and Trademark Office] is permitted, but never compelled, to institute an IPR proceeding.”). In assessing whether to exercise such discretion, the Board weighs six non-exclusive factors, known as the *Fintiv* factors. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”). Recognizing that “there is some overlap among these factors” and that “[s]ome facts may be relevant to more than one factor,” the Board “takes a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Id.* On June 21, 2022, the Director of the USPTO issued several clarifications concerning the application of the *Fintiv* factors. *See Interim Procedure For Discretionary Denials In AIA Post-Grant Proceedings With Parallel District Court Litigation*, issued June 21, 2022 (“Interim Procedure”).⁷ The Interim Procedure clarifies “the PTAB’s current application of *Fintiv* to discretionary institution where there is parallel litigation” and explains that “[c]onsistent with *Sotera Wireless, Inc.*, the PTAB will not discretionarily deny institution in view of parallel district court litigation where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB.” Interim Procedure 2–3 (internal footnote omitted) (citing *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020))

⁷ Available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf

(precedential as to § II.A). The Interim Procedure explains that such a *Sotera* stipulation “mitigates concerns of potentially conflicting decisions and duplicative efforts between the district court and the PTAB [and] allows the PTAB to review grounds that the parallel district court litigation will not resolve.” *Id.* at 7–8.

In this proceeding, Petitioner stipulates that if the PTAB institutes *inter partes* review in relation to any petition filed by [Petitioner] with respect to the ’169 patent, Petitioner will not pursue in the district court litigation any ground raised or that could have been reasonably raised in the instituted IPR with respect to the patent claim subject to the instituted IPR and argues that “[t]his stipulation precludes discretionary denial under § 314(a).” Pet. 84.

Patent Owner urges us to exercise discretion to deny institution of *inter partes* review under § 314(a) in light of the parallel District Court litigation involving the ’169 patent. Prelim. Resp. 7–10 (citing *Fintiv*). Patent Owner argues that “Petitioner has not filed a stipulation in district court.” *Id.* at 10. Patent Owner also argues that Petitioner’s stipulation is narrower than that in *Sotera* and is not the type of stipulation that should preclude discretionary denial. *Id.*

We consider the parties’ arguments in light of the *Fintiv* factors, as explained below.

1. Factor 1: Whether a Stay Exists or Is Likely to Be Granted if a Proceeding Is Instituted

Neither party has directed us to any evidence that the district court has stayed or is likely to stay the parallel proceeding, so the first factor is neutral.

2. *Factor 2: Proximity of the Court's Trial Date to the Board's Projected Statutory Deadline*

Trial in the parallel District Court litigation is scheduled to begin on May 6, 2024, approximately two and a half months before our final written decision would be due, so the second factor weighs somewhat in favor of exercising discretion to deny institution. Ex. 2001, 1.

3. *Factor 3: Investment in the Parallel Proceeding by the Court and Parties*

As of the date when our institution decision is due, there will be significant work left to do in the parallel District Court litigation, including claim construction, fact and expert discovery, and dispositive motions, so the third factor weighs against discretionary denial. *Id.* at 1–4.

4. *Factor 4: Overlap Between Issues Raised in the Petition and in the Parallel Proceeding*

According to the Interim Procedure, we should not exercise discretion to deny institution where a petitioner “stipulates not to pursue in a parallel district court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition.” Interim Procedure at 7. Here, Petitioner’s stipulation uses this language but is further limited “to the patent claim subject to the instituted IPR.” Pet. 84. We agree with Patent Owner that this stipulation is “narrower” than the stipulation “that was considered by the Board in *Sotera*,” because it adds further limiting language to the model *Sotera* stipulation. Prelim. Resp. 10. Accordingly, we do not find that this stipulation implicates the Interim Procedure’s prohibition against discretionary denial where a *Sotera*-type stipulation is presented.

We do not agree with Patent Owner that the stipulation must be filed in district court. All the Interim Procedure requires is that Petitioner “stipulate[]” or “present[] a stipulation,” not that the stipulation be filed in district court. Interim Procedure at 3, 7. Accordingly, we do not discount Petitioner’s stipulation because Petitioner failed to file it in district court.

Thus, although Petitioner’s stipulation does not track the language of the model *Sotera* stipulation, it does minimize the possibility of overlapping issues between the parallel proceeding and this proceeding, in which all claims of the ’169 patent are challenged in the Petition. Accordingly, the fourth factor weighs against discretionary denial.

5. Factor 5: Whether the Petitioner and the Defendant in the Parallel Proceeding Are the Same Party

Petitioner here is the defendant in the District Court proceeding, so the fifth factor weighs in favor of discretionary denial.

6. Factor 6: Other Circumstances that Impact the Board’s Exercise of Discretion, Including the Merits

Neither party raises additional circumstances impacting our exercise of discretion, so the sixth factor is neutral.

7. Balancing the Fintiv Factors

We have considered the circumstances and facts before us in view of the *Fintiv* factors, taking “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Fintiv* at 6. Having evaluated all of the factors, and taking into account Petitioner’s stipulation, we determine that the circumstances presented here do not warrant exercising our discretion under § 314(a) to deny institution.

D. Reasonable Likelihood under 35 U.S.C. § 314(a)

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic*, 815 F.3d at 1363 (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon).

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved based on underlying factual determinations including: (1) the scope and content of the prior art; (2) differences between the prior art and the claims at issue; (3) the level of ordinary skill in the pertinent art; and (4) when presented, objective evidence of nonobviousness, i.e., secondary considerations.⁸ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*,

⁸ At this stage, Patent Owner does not present any objective evidence of nonobviousness (i.e., secondary considerations).

829 F.3d 1364, 1380 (Fed. Cir. 2016). A reason to combine or modify the prior art may be found explicitly or implicitly in market forces; design incentives; the “interrelated teachings of multiple patents”; “any need or problem known in the field of endeavor at the time of invention and addressed by the patent”; and the background knowledge, creativity, and common sense of the person of ordinary skill. *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1329 (Fed. Cir. 2009) (quoting *KSR*, 550 U.S. at 418–21).

E. Ground 1

Petitioner argues that Lauxtermann renders obvious claims 1–6 and 10–15. Pet. 21–43. Patent Owner disagrees. PO Resp. 14–17.

1. Lauxtermann

Lauxtermann is a U.S. patent titled “Backside Illuminated CMOS Image Sensor with Pinned Photodiode.” Ex. 1004, code (54). Lauxtermann discloses photodiodes “arranged in linear or planar arrays with a plurality of photosensitive sensors, generally designated as pixels, on a semiconductor chip.” *Id.* at 2:44–46.

Figure 4 of Lauxtermann is reproduced below.

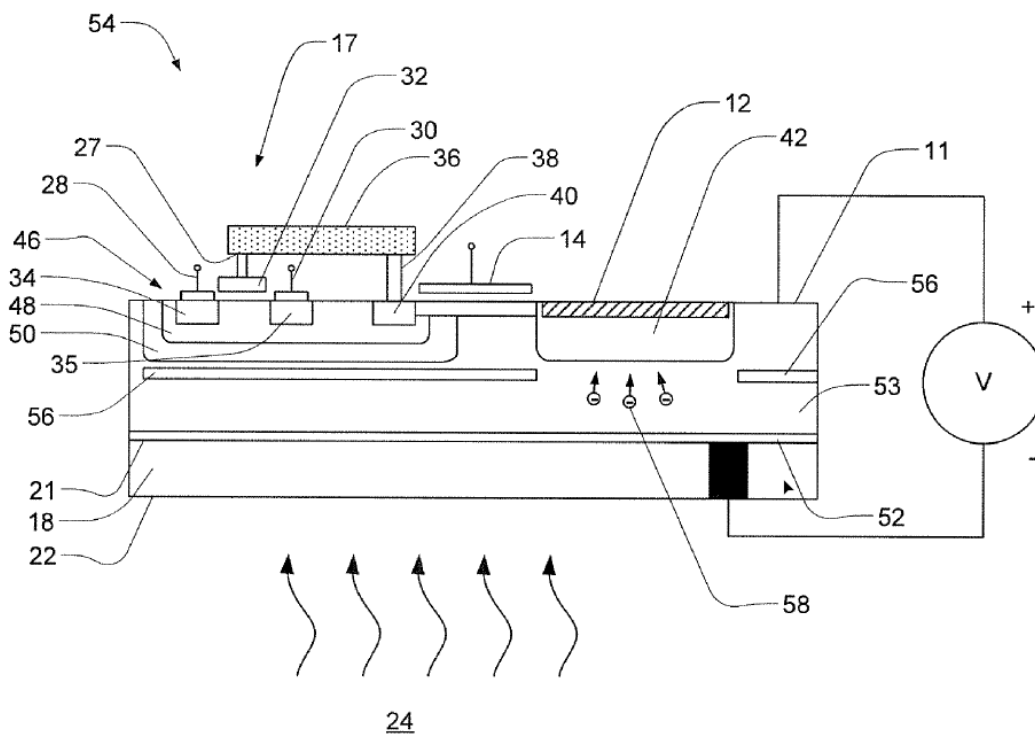


Figure 4

Figure 4 illustrates backside illuminated CMOS image sensor 54. Ex. 1004, 5:1–2. CMOS image sensor 54 includes pinned photodiode 12, which collects charge due to light 24 on the pixel, and outputs a signal to NMOS source follower transistor 17. *Id.* at 5:3–7, 5:11. Underneath pinned photodiode 12 is n-doped region 42 of high resistivity semiconductor layer 53. *Id.* at 5:7–9. Underneath transistor 17 is triple well configuration 46 with n-doped regions 34, 35, 40 isolated in p-well 48, which is further contained in n-well 50. *Id.* at 5:16–19. Lauxtermann discloses that because charges, generated due to backside illumination, diffuse toward photodiode 12 and the active pixel circuitry, some of the charges will be lost to the active pixel circuitry and photodiode 12 collects

only a fraction of the charges diffusing through semiconductor layer 43. *Id.* at 4:57–62. As a solution, Lauxtermann provides p-layer 56 to drift the charges to the charge collecting element of photodiode 12. *Id.* at 4:66–5:1. P-layer 56, which may be a deep p⁺ implant located underneath circuitry 17, “allows charge 58 to drift, rather than diffuse, to the light receiving element of the pinned photodiode 12. This improves the efficiency of the CMOS image sensor [54] by allowing the pinned photodiode 12 to collect more charges 58 liberated in the semiconductor layer 53 due to backside illumination.” *Id.* at 5:41–49.

2. *Petitioner’s Arguments*

Petitioner argues that Lauxtermann discloses the limitations of claim 1, as follows:

[1pre] A back-side illumination (BSI) complementary metal-oxide-semiconductor (CMOS) pixel array comprising:⁹ (Pet. 21 (citing Ex. 1003 ¶¶ 92–93, Ex. 1004, Abstract, 1:6–10, 5:1–3, 5:50–53, Figs. 4, 5)),

[1a] a plurality of pixels, a pixel of said plurality of pixels comprising: (Pet. 21–23 (citing Ex. 1003 ¶¶ 95–96; Ex. 1004, Figs. 4, 5));

[1b] one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-Well (NW) region or a P-well (PW) region; (Pet. 23–24 (citing 1003 ¶¶ 97–99; Ex. 1004, 3:47–50, 5:11–13, 5:16–19, 2:51–58, Fig. 4); one of ordinary skill in the art

⁹ We express no opinion on whether the preamble is limiting.

“would understand that these four transistors in Lauxtermann’s 4T structure are all **MOS transistors** because they are part of a CMOS image sensor made using a CMOS fabrication process”);

[1c] a photodiode, (Pet. 24–25 (citing 1003 ¶¶ 100–101; Ex. 1004, 5:3–10, Fig. 4); one of ordinary skill in the art “would understand the labeled ‘pinned photodiode 12’ is actually a p⁺ pinning layer, and that pinning layer 12, n-doped region 42, and the p-type layer underneath region 42 together form a **P-N-P double junction photodiode**”);

[1d] an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and (Pet. 26–28 (citing 1003 ¶¶ 102–105; Ex. 1004, 5:29–31, 3:4–8; 2:59–3:6; 5:45–49, Figs. 1, 4); one of ordinary skill in the art “would have understood that semiconductor layer 53 must be Silicon deposited epitaxially on the substrate, and thus an epitaxial layer,” and “that the **collection area** collects the charges 58 from the **absorption area** and funnels them towards the **photodiode** in conjunction with the **p-layers 56** (since p layers repel the charges)”);

[1e] a barrier layer separating said absorption area from said one or more well regions. Pet. 28–29 (citing 1003 ¶¶ 106–107; Ex. 1004, 5:16–19, 5:41–45, Fig. 4).

Petitioner presents additional arguments for dependent claims 2–6 and 10–15. Pet. 29–43 (citing Ex. 1003 ¶¶ 108–134).

3. *Patent Owner's Arguments*

First, Patent Owner argues that “Lauxtermann does not describe layer 53 as being an epitaxial (epi) layer” as in limitation [1d] but, rather, “as a ‘semiconductor layer,’” and that one of ordinary skill in the art “would not understand that layer 53 is an epi.” Prelim. Resp 14 (citing Ex. 1004, 5:30–31). Patent Owner also argues that Petitioner has not provided “‘sufficient reasoning’ to fill Lauxtermann to provide the obviously missing claim limitations for its obviousness argument.” *Id.* at 16.

Second, Patent Owner argues that the “absorption area” and “collection area” of limitation [1d] also are not disclosed by Lauxtermann. *Id.* Patent Owner disagrees that Lauxtermann discloses “[w]ithin that epitaxial layer, layer 53 includes a collection area and an absorption area, the former of which connects the absorption area to the photodiode” and disagrees with Petitioner’s footnote stating: “[a]ccording to the plain language of the claims, absorption area and collection area are parts of the epitaxial layer. They need not be separate layers.” *Id.* (citing Pet. 27, 27 n.2). According to Patent Owner, the ’169 patent clearly identifies an absorption area and a collection area in Figure 2, and against “this clear intrinsic evidence, Petitioner only relies on the attorney arguments and conclusory expert opinion, none of which are evidence.” *Id.* at 17. Patent Owner does not otherwise challenge Petitioner’s arguments or evidence regarding the remaining limitations.

4. *Analysis*

Regarding layer 53, we are persuaded by Petitioner’s argument that one of ordinary skill in the art would understand layer 53 as having been grown epitaxially. We agree with Petitioner on this record that Lauxtermann

“teaches semiconductor layer 53 is deposited just like semiconductor layer 16” and, in other embodiments, “expressly teaches that the ‘semiconductor layer’ is “an **epitaxial layer**.” Pet. 26 (citing Ex. 1003 ¶¶ 103–104; Ex. 1004, 5:29–31, 3:4–8; Fig. 1). Petitioner’s declarant supports this assertion, stating that “CMOS devices of the image sensor perform best on epitaxial Silicon” (citing Ex. 1055, 385–387), and that a “POSITA would have understood that semiconductor layer 53 must be Silicon deposited epitaxially on the substrate, and thus an epitaxial layer.” Ex. 1003 ¶ 104. Altogether, we are persuaded by Petitioner’s arguments and evidence on this record that one of ordinary skill in the art would “understand that Lauxtermann’s semiconductor layer 53 is an epitaxial layer.” *Id.*

Regarding the absorption area and the collection area, we agree with Patent Owner that the ’169 patent depicts those areas (222, 224 respectively) in Figure 2. Ex. 1001, Fig. 2. Consistent with the depiction in Figure 2, claim 1 calls for an absorption area and a collection area, not an absorption layer and a collection layer, which Petitioner points out in its disputed footnote. Pet. 27 n.2. Apart from the claim requirement of having the “collection area connecting said absorption area to said photodiode” (Ex. 1001, 15:53–54), the claim does not call for any particular orientation, layered or otherwise, of the absorption area relative to the collection area. Patent Owner also directs us to column 8, lines 29–46 to support its position, but this portion of the ’169 patent clearly refers to absorption and collection *areas*, not layers. Even if we were to agree with Patent Owner that the cited portions of the ’169 patent do refer to layers, which we do not, we do not import limitations from the specification into the claims. *See E-Pass Techs., Inc. v. 3Com Corp.*, 343 F.3d 1364, 1369 (Fed. Cir. 2003) (claims must be

interpreted “‘in view of the specification’ without unnecessarily importing limitations from the specification into the claims” (citing *Texas Digital Sys., Inc. v. Telegenix, Inc.*, 308 F.3d 1193, 1204–1205 (Fed. Cir. 2002))). On this record, Petitioner appears to demonstrate that Lauxtermann discloses this limitation, as supported by the testimony of Petitioner’s declarant. Pet. 27–28 (citing Ex. 1003 ¶ 105).

We have reviewed the parties’ arguments and the cited evidence, and, on the present record, Petitioner shows sufficiently that Lauxtermann discloses the limitations of claims 1–6 and 10–15. For the limitations undisputed by Patent Owner, we agree with Petitioner, based on the evidence and arguments presented in the Petition, that Lauxtermann teaches or suggests those limitations. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that claims 1–6 and 10–15 would have been obvious in view of Lauxtermann.

F. Ground 2

Petitioner argues that Lauxtermann and Zucca render obvious claims 2, 6, 7, and 9. Pet. 44–52. Patent Owner disagrees. PO Resp. 17–18.

1. Zucca

Zucca is an IEEE paper titled “Monolithic Pixel Sensors for Fast Particle Trackers in a Quadruple Well CMOS Technology.” Ex. 1005, 1742. Zucca discloses a pixel sensor in which “a high energy deep Pwell implant is deposited beneath the PMOS competitive Nwells” to provide “a barrier for the charge diffusing in the epitaxial layer, preventing the carriers from being collected by the positively biased Nwells hosting the PMOS transistors of the in-pixel readout circuits.” *Id.* “In this way, a theoretical charge collection efficiency of 100% can be reached.” *Id.* Zucca discloses sensor

designs including a 12 μm thick high resistivity (about 1 $\text{k}\Omega\cdot\text{cm}$) epitaxial layer. *Id.* at 1743.

2. *Analysis*

Petitioner argues that one of ordinary skill in the art would have been motivated to modify Lauxtermann to include Zucca's teachings of a low fill factor diode (as in claim 2), an epitaxial layer thickness of 12 μm (as in claims 6 and 7), and an epitaxial layer of about 1000 ohm-cm (as in claim 9), with a reasonable expectation of success. Pet. 44–49 (citing Ex. 1003 ¶¶ 135–145). Petitioner presents arguments directed to claim 2 (Pet. 49–50 (citing Ex. 1003 ¶¶ 146–149)), claims 6 and 7 (Pet. 50–51 (citing Ex. 1003 ¶¶ 150–155)), and claim 9 (Pet. 51–52 (citing Ex. 1003 ¶¶ 156–158)). Petitioner argues that one of ordinary skill in the art “would have been motivated to modify Lauxtermann to include these teachings [of Zucca] and would have had a reasonable expectation of success,” to “improve the light sensitivity and thus efficiency of its image sensor” (claims 6, 7), to “improve the efficiency of its image sensor” (claim 9), and to “improve the image processing performance of its image sensor” (claim 2). Pet. 44–47 (citing Ex. 1003 ¶¶ 136–139).

Patent Owner argues that Petitioner's reliance on Zucca to teach a low fill factor diode and epitaxial layers with certain minimum thicknesses is erroneous because Zucca “does not disclose backside illumination sensors” and nothing “in Zucca or Lauxtermann would give a POSA motivation to combine them to achieve the patented properties.” Prelim. Resp. 17.

Regarding Patent Owner's argument that Zucca does not disclose or render obvious a BSI sensor (Prelim. Resp. 17), Zucca teaches that its process is applicable to light incident on the back side of its BSI image

sensor. Ex. 1005, Fig. 1; Pet. 44–45. In addition, “Zucca discloses its MAPS image sensor is also a BSI CMOS sensor.” Pet. 17 (citing Ex. 1005, 1742, 1744–45 (“The samples were illuminated from the back side”)). This evidence could support a finding that Zucca suggests an image sensor illuminated from the back side. *Id.* Thus, on the present record, Petitioner shows sufficiently that Zucca is applicable to BSI sensors, and combinable with Lauxtermann with a reasonable expectation of success. Pet. 44–49 (citing Ex. 1003 ¶¶ 136–145).

Having evaluated the parties’ arguments and evidence on this ground, we are persuaded that Petitioner shows a reasonable likelihood of prevailing on its argument that claims 2, 6, 7, and 9 would have been obvious in light of Lauxtermann and Zucca.

G. Ground 3

Petitioner argues Lauxtermann and Akiyama render obvious claims 10 and 11. Pet. 52–58. Patent Owner disagrees. Prelim. Resp. 18.

1. Akiyama

Akiyama is a U.S. patent titled “Method of Manufacturing Solid-State Imaging Device and Method of Manufacturing Electronic Apparatus.” Ex. 1006, code (54). Akiyama discloses a unit pixel having antireflective coating and on-chip microlenses. *Id.* at 5:6–7, 5:55–6:3.

2. Analysis

Petitioner argues that one of ordinary skill in the art would have been motivated to include a microlens (as in claim 10) and an antireflective coating (ARC) layer (as in claim 11) in Lauxtermann’s BSI CMOS image sensor according to Akiyama’s teachings to improve the efficiency of its image sensor for use in electronic devices. Pet. 52 (citing Ex. 1003 ¶160).

Patent Owner argues that Lauxtermann fails to render claim 1 obvious, and the additional disclosure in Akiyama does not cure this failure. Prelim. Resp. 18.

Having evaluated the parties' arguments and evidence on this ground, we are persuaded that Petitioner shows a reasonable likelihood of prevailing on its argument that claims 10 and 11 would have been obvious in light of Lauxtermann and Akiyama.

H. Ground 4

Petitioner argues Lauxtermann and Wang render obvious claims 16–20. Pet. 58–67. Patent Owner disagrees. Prelim. Resp. 18.

1. Wang

Wang is a U.S. patent titled “Front Side Implanted Guard Ring Structure for Backside Illuminated Image Sensor.” Ex. 1010, code (54). Wang discloses a CMOS image sensor having a guard ring structure for reducing crosstalk between neighboring pixels, as well as between control circuitry and the pixels. *Id.* at 2:16–18, 3:16–26; 7:15–18; 8:10–13. Wang further discloses using BSI sensors in digital cameras. *Id.* at 1:38–41.

2. Analysis

Petitioner argues that “Wang teaches peripheral circuitry [as in claims 16 and 19], guard ring [as in claims 17 and 18] and digital camera [as in claim 20] that meet the requirements of these claims” and one of ordinary skill in the art “would have been motivated to modify Lauxtermann to include these teachings and would have had a reasonable expectation of success.” Pet. 58 (citing Ex. 1003 ¶ 176). Petitioner presents arguments directed to claim 16 (Pet. 60–62 (citing Ex. 1003 ¶¶ 182–186)), claim 17 (Pet. 63–64 (citing Ex. 1003 ¶¶ 193–195)), claim 18 (Pet. 64–65 (citing

Ex. 1003 ¶¶ 196–197)), claim 19 (Pet. 65–67 (citing Ex. 1003 ¶¶ 198–201)), and claim 20 (Pet. 67 (citing Ex. 1003 ¶ 210)). Petitioner argues that one of ordinary skill in the art “would have been motivated to include a guard ring in Lauxtermann’s BSI CMOS image sensor according to Wang’s teaching to reduce crosstalk between neighboring pixels and between the pixel array and any peripheral circuitry” (claims 17, 18), and “would have been motivated to include peripheral circuitry in Lauxtermann’s BSI CMOS image sensor according to Wang’s teaching to access the pixels in the image sensor” (claims 16, 19). Pet. 58–60 (citing Ex. 1003 ¶¶ 177–181).

Patent Owner argues that Lauxtermann fails to render claim 1 obvious, and the additional disclosure in Wang does not cure this failure. Prelim. Resp. 18.

Having evaluated the parties’ arguments and evidence on this ground, we are persuaded that Petitioner shows a reasonable likelihood of prevailing on its argument that claims 16–20 would have been obvious in light of Lauxtermann and Wang.

I. Ground 5

Petitioner argues Ballin renders obvious claims 1, 3–8, and 12–15. Pet. 67–79. Patent Owner disagrees. Prelim. Resp. 19–22.

1. Ballin

Ballin is an article titled “Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixels.” Ex. 1007, 5336. Ballin discloses a back-illuminated CMOS image sensor using “a deep P implant . . . to form a deep P-well and provide screening of N-wells from the P-doped epitaxial layer. This prevents the collection of radiation-induced charge by unrelated N-wells, typically ones

where PMOS transistors are integrated.” *Id.* at 5336–5337, 5339.

Figure 2 of Ballin is reproduced below.

Figure 2. Schematic cross-section of a CMOS wafer with the deep P-well implant. Not drawn to scale.

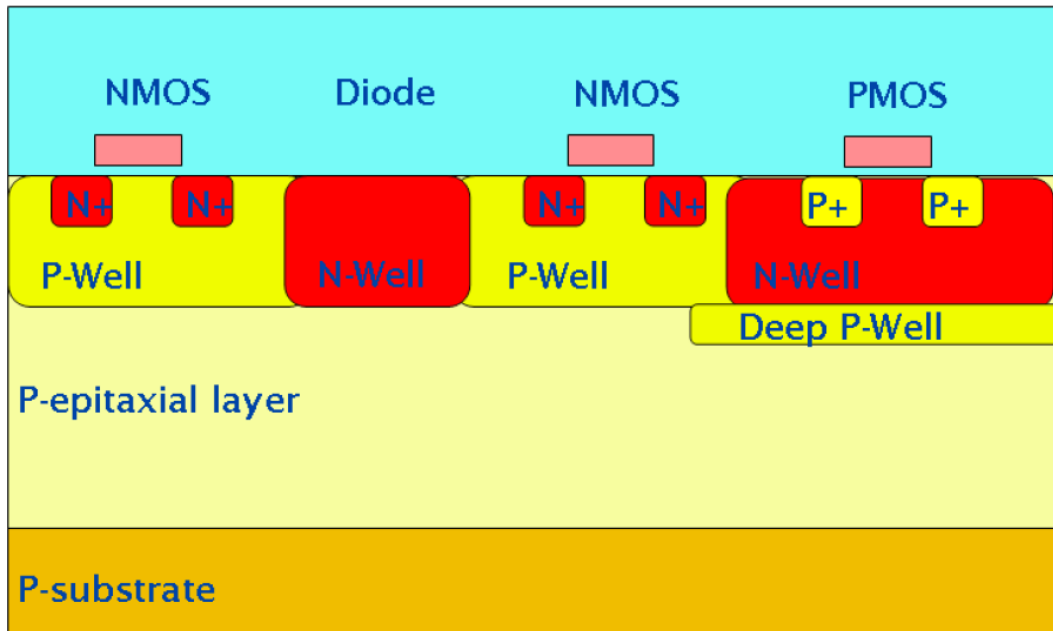


Figure 2 shows a cross-section of a CMOS wafer with the deep P-well implant. *Id.* at 5339. The illustrated pixel includes an N-well diode, NMOS and PMOS transistors occupying heavily doped P-wells and N-wells, respectively, a P-doped epitaxial layer, and a deep P-well that isolates the N-wells of the PMOS transistors from the P-doped epitaxial layer. *Id.* at 5338–5339. According to Ballin, “[b]y adding the deep P-well layer underneath all the N-wells used as substrate for PMOS transistors, it is then possible to keep the collecting PN diode junction as the only one in the pixel that is exposed to the epitaxial layer” and “enabl[e] the use of PMOS transistors in the pixel without loss of signal.” *Id.* at 5337, 5340.

2. *Petitioner's Arguments*

Petitioner argues that Ballin discloses the limitations of claim 1, as follows:

[1pre] A back-side illumination (BSI) complementary metal-oxide-semiconductor (CMOS) pixel array comprising: (Pet. 68 (citing Ex. 1003 ¶¶ 212–213; Ex. 1007, 5338–5339, Fig. 2);

[1a] a plurality of pixels, a pixel of said plurality of pixels comprising: (Pet. 68–69 (citing Ex. 1003 ¶¶ 214–215; Ex. 1007, Fig. 5));

[1b] one or more Metal-Oxide-Semiconductor (MOS) transistors comprising one or more well regions, a well region of said one or more well regions comprising an N-Well (NW) region or a P-well (PW) region; (Pet. 69–70 (citing 1003 ¶¶ 216–218; Ex. 1007, 5338, 5340, Fig. 2);

[1c] a photodiode; (Pet. 70 (citing 1003 ¶¶ 219–220; Ex. 1007, 5337–5338, Fig. 2);

[1d] an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode; and (Pet. 70–72 (citing 1003 ¶¶ 221–223; Ex. 1007, 5338, Fig. 2); one of ordinary skill in the art “would understand that the collection area collects the charges from the absorption area and funnels them towards the photodiode in conjunction with the deep P-wells (since the deep P-wells repel the charges)”);

[1e] a barrier layer separating said absorption area from said one or more well regions. Pet. 73–74 (citing 1003 ¶¶ 225–227; Ex. 1007, 5339–5340, Fig. 2).

Petitioner presents additional arguments for dependent claims 3–8 and 12–15. Pet. 74–79 (citing Ex. 1003 ¶¶ 228–248).

3. *Patent Owner’s Arguments*

First, Patent Owner argues that “Ballin does not teach a barrier layer separating the absorption area from both N-well and P-well regions as claimed by the ’169 patent,” i.e., limitation [1e]. Prelim. Resp 19–20. Patent Owner argues that “the deep P-well does not function as a barrier layer because it separates the asserted absorption area only from the N-well of the PMOS transistors, but not both the N-well and P-well regions (the ‘one or more well regions’ identified by Petitioner itself).” *Id.* at 19.

Second, Patent Owner argues that the “absorption area” and “collection area” of limitation [1d] also are not disclosed by Ballin. *Id.* at 20–21. Patent Owner highlights Petitioner’s footnote stating: “[a]ccording to the plain language of the claims, absorption area and collection area are parts of the epitaxial layer. They need not be separate layers.” *Id.* (citing Pet. 71). According to Patent Owner, the ’169 patent clearly identifies an absorption area and a collection area, and against “this clear intrinsic evidence, Petitioner only relies on the attorney arguments and conclusory expert opinion, none of which are evidence.” *Id.* at 21. Patent Owner does not otherwise challenge Petitioner’s arguments or evidence regarding the remaining limitations.

4. *Analysis*

Regarding Patent Owner’s deep P-well argument, we are persuaded on this record that Petitioner has made a sufficient showing, for purposes of institution, that Ballin discloses “a barrier layer separating said absorption area from said one or more well regions” as in limitation [1e]. Pet. 73–74. The language of the claim requires the barrier layer to separate the absorption area from “one or more” well regions, so we disagree with Patent Owner’s argument that “Ballin does not teach a barrier layer separating the absorption area from both N-well and P-well regions as claimed by the ’169 patent.” Prelim. Resp 19–20. Moreover, Petitioner’s annotated Figure 2 and accompanying argument demonstrate, on this record, that Ballin’s “deep P-well layer underneath all the N-wells” (Ex. 1007, 5339–5340) separates the absorption area from the one or more well regions, as in claim limitation [1e]. Pet. 73–74; Ex. 1007, Fig. 2 (annotated). Accordingly, at this stage in the proceeding, Petitioner sufficiently identifies in Ballin the “one or more well regions” of limitation [1b] (Pet. 69–70) and [1e] (Pet. 73–74), and the barrier layer of limitation [1e] (*id.*), notwithstanding Patent Owner’s assertion of an inconsistency or shortcoming in Petitioner’s arguments (Prelim. Resp. 19).

Regarding the absorption area and the collection area, we agree with Patent Owner that the ’169 patent depicts those areas in Figure 2. Ex. 1001, Fig. 2. We do not import limitations from the specification into the claims. *See E-Pass Techs.*, 343 F.3d at 1369. The claim calls for an absorption area and a collection area, not an absorption layer and a collection layer, which Petitioner points out in its disputed footnote. Pet. 71 n.4. Apart from the claim requirement of having the “collection area connecting said absorption

area to said photodiode” (Ex. 1001, 15:53–54), the claim does not call for any particular orientation, layered or otherwise, of the absorption area relative to the collection area. On this record, Petitioner appears to demonstrate that Lauxtermann discloses this limitation, as supported by the testimony of Petitioner’s declarant. Pet. 71–72 (citing Ex. 1003 ¶ 223).

We have reviewed the parties’ arguments and the cited evidence, and, on the present record, Petitioner shows sufficiently that Ballin discloses the limitations of claims 1, 3–8 and 12–15. For the limitations undisputed by Patent Owner, we agree with Petitioner, based on the evidence and arguments presented in the Petition, that Ballin teaches or suggests those limitations. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that claims 1, 3–8 and 12–15 would have been obvious in view of Ballin.

J. Ground 6

Petitioner argues Ballin and Akiyama render obvious claims 10 and 11. Pet. 79–81. Patent Owner disagrees. Prelim. Resp. 22.

Petitioner argues that one of ordinary skill in the art would have been motivated to include a microlens (as in claim 10) and an antireflective coating (ARC) layer (as in claim 11) in Ballin’s BSI CMOS image sensor according to Akiyama’s teachings to improve the efficiency of its image sensor. Pet. 79 (citing Ex. 1003 ¶ 250).

Patent Owner argues that Ballin fails to render claim 1 obvious, and the additional disclosure in Akiyama does not cure this failure. Prelim. Resp. 22.

Having evaluated the parties’ arguments and evidence on this ground, we are persuaded that Petitioner shows a reasonable likelihood of prevailing

on its argument that claims 10 and 11 would have been obvious in light of Ballin and Akiyama.

III. CONCLUSION

For the reasons set forth above, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one challenged claim of the '169 patent, and we institute *inter partes* review on all challenges raised in the Petition.

At this preliminary stage of the proceeding, we have not made a final determination as to the patentability of any challenged claim or any factual or legal issue underlying the patentability inquiry. Any final determination will be based on the record developed during trial. We place Patent Owner on express notice that any argument not asserted in a timely-filed Response to the Petition, or in another manner permitted during trial, shall be deemed waived, even if that argument was presented in the Preliminary Response.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that *inter partes* review is instituted on each of the grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this decision.

IPR2023-00369
Patent 9,356,169 B2

FOR PETITINER:

James Glass
John McKee
QUINN EMANUEL URQUHART & SULLIVAN, LLP
jimglass@quinnemanuel.com
johnmckee@quinnemanuel.com

FOR PATENT OWNER:

Eric Cohen
RIMON PC
Eric.cohen@rimonlaw.com