

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED,

Petitioner,

v.

ALIDDOUBLE, INC.,

Patent Owner.

IPR2023-00369

U.S. Patent No. 6,168,169

DECLARATION OF RON MALTIEL

I, **RON MALTIEL**, declare the following to be true:

I. INTRODUCTION

1. I have been retained by Alidouble Inc. through its counsel, to provide my opinions regarding U.S. Patent No. 9,356,169 Ex. 1001 (hereinafter, the “‘169 Patent”).

2. I make this declaration in support of Alidouble’s Patent Owner’s Response to the Petition in IPR2023-00369.

3. This declaration contains statements of my opinions formed to date regarding the ‘169 Patent and the bases and reasons for those opinions. I may offer additional or different opinions based on further review of materials in this IPR, including review of opinions or testimony of other expert witnesses or future positions taken by Petitioner or its witnesses.

II. PROFESSIONAL EXPERIENCE AND QUALIFICATIONS

4. My educational and professional background, patents, and professional association memberships are listed in my *curriculum vitae*, which is Exhibit 2003.

5. I am a senior member of the Institute of Electrical and Electronics Engineers (IEEE) with more than 30 years’ experience in all phases of design and implementation of semiconductor manufacturing. I have worked in the development and production of new integrated circuit technologies and semiconductor devices such as CMOS devices, used for products such as Dynamic Ram (DRAM), Flash

(NAND, NOR), EEPROM, ROM, and Static RAM (SRAM) memories which are used in microprocessors, logic, digital, analog, and image sensor products.

6. I graduated in 1977 from Ben Gurion University in Israel with a Bachelor of Science degree in Materials Science & Engineering. In 1978, I earned a Master's Degree in Materials Science & Engineering from Stanford University in Palo Alto, California.

7. In 1980, I was awarded an Engineer Degree from Stanford University in Materials Science & Engineering. At Stanford University, an Engineer Degree is an additional graduate degree that can be earned after a Master's Degree. The degree differs from a Ph.D. in that an Engineer Degree's focus is primarily on professional engineering work as opposed to a Ph.D.'s primary focus on theoretical research or university teaching.¹ An Engineer Degree requires two years of additional study beyond a Master's Degree and the completion of a thesis.² My thesis related to defects in silicon and electrical measurements of their properties and was entitled *Electrical Properties Of Gold And Titanium In Silicon*. My thesis led to my first patent.³

¹ See <http://gap.stanford.edu/4-3.html>

² See *id.*

³ [Gold-doped IC resistor region - #4,432,008, https://www.maltiel.com/ron-maltiels-patents.html](https://www.maltiel.com/ron-maltiels-patents.html)

8. Following my studies at Stanford, I worked in four semiconductor companies, focusing on the development and manufacturing of new semiconductor devices. Through the years I was responsible for integrating the work product of all the various disciplines into final manufacturing processes.

9. In 1980, my first position was at Intel. I worked to develop the first commercial non-volatile EEPROM devices. NAND memory such as Flash memory was subsequently developed using EEPROM as its basic building block. Among other responsibilities, I analyzed the manufacturing reliability and designed the production and testing of operation flow.

10. In 1982, I left Intel and joined American Micro Systems, where I was in charge of developing the manufacturing process for a new non-volatile memory product line.

11. In 1983, I joined Advanced Micro Devices (AMD) working on a project combining non-volatile with DRAM memories. I developed memory circuitry and its manufacturing process. This work led to three patents where I am named as an inventor. Following this project, I worked on several other technologies at AMD. While at AMD, I was in charge of consolidating the designs of all the test chips made by all of AMD's various divisions into one library. The test chips were used during new technology development and production to monitor the electrical properties of semiconductor products following their fabrication.

12. In 1989, I joined Maxim Integrated Products, Inc. where I was in charge of developing all the CMOS process developments for analog products and introducing them to production. When Maxim bought its first fabrication line, I developed the production process for the diffusion and etch areas.

13. I currently work as an independent consultant providing consulting services in various aspects of semiconductor technology and manufacturing.

14. In 2008, I was recognized as a Senior Member of the IEEE, the leading professional association for electrical engineers.⁴ Senior Member is the highest grade and recognizes a member with at least 10 years of industry experience including 5 years of which the member has shown “significant performance.”⁵

15. For more than 20 years, I have been managing a semiconductor industry website (www.maltiel-consulting.com) and providing to the semiconductor industry a resource full of pertinent information about new semiconductor patents as well as semiconductor products and their introduction to manufacturing. This resource addresses the informational needs of technology companies, attorneys, and investors and is used regularly by the United States Patent and Trademark Office, the Justice Department, major semiconductor companies, and universities from more than 99 countries.

⁴ See <http://www.ieee.org/about/index.html>

⁵ See <http://www.ieee.org/membership/senior/senior-requirements.html>

16. I am the named inventor of six patents. The patents are in the areas of process and circuit development. Three of my patents are related to creating new semiconductor devices and to monitoring the properties of semiconductor lines during fabrication. Two of my patents are related to measurements of wafers during fabrication. One of my patents is related to integrating resistors into doped regions in the semiconductor substrate. My patents have been referenced in other United States patents more than 150 times.

III. COMPENSATION

17. I am compensated at a rate of \$720 per hour for my work. I am also being separately reimbursed for any out-of-pocket expenses. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of any proceeding.

IV. MATERIALS CONSIDERED

18. Among the materials I considered are as follow. If there are materials that I referenced but are not listed below, they should be part of the materials considered.

No.	Document
1.	U.S. Patent No. 6,168,169
2.	Prosecution File History for the '169 Patent
3.	Declaration of Dr. Konstantinos P. Giapis

4.	U.S. Patent No. 7,498,650 (“Lauxtermann”)
5.	S. Zucca et al, <i>Monolithic Pixel Sensors for Fast Particle Trackers in a Quadruple Well CMOS Technology</i> , 2012 IEEE Nuclear Science Symposium and Medical Imaging Conference Record (“Zucca”)
6.	U.S. Patent No. 8,076,172 (“Akiyama”)
7.	J. Ballin et al, <i>Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixels</i> , Sensors 2008 (“Ballin”)
8.	U.S. Patent No. 8,723,284 (“Hynecek”)
9.	U.S. Patent App. Pub. No. 2010/0159632 (“Rhodes”)
10.	U.S. Patent No. 8,531,565 (“Wang”)
11.	U.S. Patent No. 7,944,012 (“Turchetta”)
12.	Coath et al, <i>Advanced Pixel Architectures for Scientific Image Sensors</i> , Proceedings of the 2009 Topical Workshop on Electronics for Particle Physics (“Coath I”)
13.	Coath et al, <i>A Low Noise Pixel Architecture for Scientific CMOS Monolithic Active Pixel Sensors</i> , 2009 IEEE Nuclear Science Symposium Conference Record (“Coath II”)
14.	U.S. Patent No. 7,710,477 (“Nam”)
15.	Battiato et al, <i>Image Processing for Embedded Devices</i> , 2010 (“Battiato”)
16.	Heddle, <i>Electrostatic Lens Systems</i> , 2nd ed, 2000 (“Heddle”)
17.	U.S. Patent No. 8,921,803 (“Welkie”)
18.	U.S. Patent No. 6,770,889 (“Iwasawa”)
19.	U.S. Patent Appl. Pub. No. 2011/0101201 (“Venezia”)
20.	U.S. Patent No. 7,505,206 (“Deng”)

21.	U.S. Patent App. Pub. No. 2013/0270663 (“Lin”)
22.	International Patent App. Pub. No. WO 2007/025102 (“Li”)
23.	U.S. Patent App. Pub. No. 2012/0038014 (“Tai”)
24.	Sze & Lee, <i>Semiconductor Devices: Physics and Technology</i> , 3rd ed, 2012 (“Sze&Lee”)
25.	Sze & Ng, <i>Physics of Semiconductor Devices</i> , 3rd ed, 2006 (“Sze&Ng”)
26.	U.S. Patent No. 8,736,006 (“Tsai”)
27.	U.S. Patent Appl. Pub. No. 2013/0203208 (“Shinohara”)
28.	E. R. Fossum and D. B. Hondongwa, “A review of the pinned photodiode for CCD and CMOS image sensors,” <i>IEEE J. Electron Devices Soc.</i> , vol. 2, no. 3, pp. 33-43, May 2014 (“Fossum I”)
29.	U.S. Patent No. 5,903,021 (“Lee”)
30.	https://en.wikipedia.org/wiki/Back-illuminated_sensor
31.	U.S. Patent No. 6,168,965 (“Malinovich”)
32.	E.R. Fossum, “Active Pixel Sensors: Are CCD's Dinosaurs?,” Proc. SPIE 1900, Charge-Coupled Devices and Solid State Optical Sensors III, (July, 1993) (“Fossum II”)
33.	Y. Kohyama et al., “A 1.4 μm Pixel Backside Illuminated CMOS Image Sensor with 300 mm Wafer Based on 65 nm Logic Technology,” International Image Sensor Workshop (IISW), 2009.
34.	S. Iwabuchi, et al., “A back-illuminated high-sensitivity small-pixel color CMOS image sensor with flexible layout of metal wiring”, Proc. IEEE Int. Solid State Circuits Conf.-Dig. Tech. Papers, pp. 1171-1178, Feb. 2006.
35.	N. Teranishi et al., “Evolution of optical structure in image sensors”, IEDM Tech. Dig., pp. 24, Dec. 2012.

36.	Y. Kitamura et al., “Suppression of crosstalk by using back-side deep trench isolation for 1.12μm back-side illuminated CMOS image sensor”, 2012 International Electron Devices Meeting, pp. 24.2.1-24.2.4, 2012.
37.	“Digital camera,” <i>Encyclopedia Britannica</i> (https://www.britannica.com/technology/digital-camera)
38.	https://www.tel.com/museum/exhibition/principle/cmos.html
39.	Boyd Fowler, X. Liu, P. Vu, “CMOS image sensors – past, present and future”, Proceedings ICIS 2006 – International Congress of Imaging Science (2006) (“Folwer”).
40.	L. J. Kozlowski, et al, “Comparison of passive and active pixel schemes for CMOS visible imagers,” Proc. SPIE 3360, Infrared Readout Electronics IV (September, 1998) (“Kozlowski”)
41.	U.S. Patent No. 8,063,963 (“Dierickx”)
42.	E. R. Fossum “CMOS Image Sensors: Electronic Camera-On-A-Chip,” <i>IEEE Transactions on Electron Devices</i> , no. 10, pp. 1689-98, Oct. 1997
43.	U.S. Patent No. 9,257,479 (“Koizumi”)
44.	Barbe, F., “A Tradeoff Analysis for CCD Area Imagers: Frontside Illuminated Interline Transfer vs. Backside Illuminated Frame Transfer,” in Procs., CCD Applications Conf., pp. 13-20 (1973) (“Barbe”)
45.	L. Brissot et al., “High-definition CCDs for enhanced definition television,” in High-Resolution Sensors and Hybrid Systems, SPIE, vol. 1656, pp. 427-436 (Aug. 12, 1992) (“Brissot”)
46.	https://www.photometrics.com/learn/imaging-topics/quantum-efficiency
47.	U.S. Patent No. 5,244,817 (“Hawkins”)
48.	U.S. Patent No. 5,270,221 (“Garcia”)
49.	U.S. Patent No. 5,494,833 (“Martin”)

50.	U.S. Patent No. 8,709,852 (“Hynecek852”)
51.	U.S. Patent No. 8,409,909 (“Nagaraja”)
52.	U.S. Patent No. 8,963,066 (“Sato”)
53.	Declaration of Dr. Sylvia Hall-Ellis
54.	S. Mendis et al., “CMOS Active Pixel Image Sensor”, IEEE Transactions on Electron Devices, vol. 41, No, 3, March 1994.
55.	Stanley Wolf, Silicon Processing for The VLSI Era, Volume 2: Process Integration, 1990.
56.	https://www.dpreview.com/articles/4281372431/sonycmos
57.	U.S. Patent No. 8,198,602
58.	R. Aihara, M. Obata, and H. Sawaragi, “Stabilization of An Electrostatic Lens for A Focused Ion Beam System,” Journal of Vacuum Science & Technology B: Microelectronics Processing and Phenomena 6, 958 (1988).
59.	T. Joy, et al., “Development of a Production-Ready, Back-Illuminated CMOS Image Sensor with Small Pixels,” IEDM, pp.1008-1010, 2007
60.	J. Ballin <i>et al.</i> , “Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixels.” <i>Sensors</i> , vol. 8, no. 9, 2008: 5336-5351
61.	S. Zucca <i>et al.</i> , “Monolithic Pixel Sensors for Fast Particle Trackers in a Quadruple Well CMOS Technology.” <i>2012 IEEE Nuclear Science Symposium and Medical Imaging Conference Record (NSS/MIC)</i> , pp. 1742-1749, 2012.
62.	Petition For <i>Inter Partes</i> Review of U.S. Patent No. 9,356,169
63.	Patent Owner’s Preliminary Response to Petition For <i>Inter Partes</i> Review of U.S. Patent No. 9,356,169

64.	Institution Decision For <i>Inter Partes</i> Review of U.S. Patent No. 9,356,169
65.	<i>Alidouble Inc., v. Taiwan Semiconductor Manufacturing Company Limited.</i> , Case No. 2:22-cv 00298-JRG (E.D. Tex), Docket Control Order
66.	Curriculum Vitae, Ron Maltiel

V. LEGAL PRINCIPLES

19. I am not a lawyer and I do not have formal training in patent law. I do, however, have practical experience with patents and the patenting process from my involvement in the prosecution of my U.S. patents. Any representations I make in this declaration regarding the law, however, are as I understand the law to be as explained to me by the lawyers from Rimon, P.C. I have used my understanding of these legal principles when forming my opinions.

A. Legal Principles Of Claim Construction

20. I understand that in an IPR petition filed after November 13, 2018, terms of a claim are given their plain and ordinary meaning as understood by a POSITA at the time of invention, in light of the specification and prosecution history, unless those sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent. Regarding a POSITA, I understand that a POSITA has ordinary creativity, and is not an automaton.

21. I understand that all limitations of a claim are to be interpreted with an eye to giving all limitations effect.

B. Legal Principles Of Obviousness

22. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

23. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable

results;

- whether a POSITA could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

24. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

VI. LEVEL OF ORDINARY SKILL IN THE ART

25. I understand the ‘169 Patent describes and claims an invention relating to Back Side Illumination (BSI) Complementary Metal-Oxide-Semiconductor (CMOS) pixel, ...’ ‘169 Patent, Abstract.

26. After reviewing the ‘169 Patent’s specification, claims and prosecution

history, in my opinion, a POSITA would have at least a bachelor's degree in electrical engineering, chemical engineering, or material science. A bachelor's degree in one of these subjects is necessary to have a foundation in solid state physics and integrated circuit processing technology. A degree in computer science would not include sufficient chemistry and physics to enable a person to learn the integrated circuit process technology sufficiently to be a POSITA for the '169 Patent. In addition, a POSITA would have 3-5 years' experience that includes some experience in image sensors. Three to five years' experience is necessary for a POSITA to understand the variability of processing and device interactions.

VII. TECHNOLOGY OVERVIEW

A. Semiconductor Manufacturing Processes

27. In the typical fabrication of semiconductor products, transistors are first created on the surface of a silicon substrate. Then, several layers of metal wires are fabricated above the transistors to connect them, with each layer separated from the next layer by an insulating layer.

28. The fabrication of semiconductor products is a complex process that typically begins with the creation of a silicon wafer. The wafer is then subjected to a series of steps, including deposition, lithography, etching, and metallization. These steps are used to create the transistors, capacitors, resistors, and other components of the semiconductor product.

29. A semiconductor is typically a solid chemical element or compound that conducts electricity under some specific conditions. This makes it an ideal medium to control electrical current for use in electronic products. The most commonly used semiconductor material is silicon. Semiconductor devices, typically referred to as computer chips, image sensors, die or integrated circuits, are made by depositing thin layers of metals and/or dielectrics

30. The structure of semiconductor devices requires numerous processing steps that start with a single crystal silicon wafer, called a substrate. A processed wafer has hundreds of semiconductor products called dies. Each of these dies may have millions of transistors acting as switches. Transistors are fabricated in the substrate by modifying the structure of the substrate and by building up layers of other materials that are deposited and patterned on the substrate. The fabrication processes create active regions, which readily conduct electricity, and passive regions which are non-conducting or insulating.

31. Key wafer processing technologies include the deposition of thin films of materials and also etching patterns in those materials. Deposited dielectric films are used for isolation, passivation, barrier, masking and antireflective-coating applications in ultra-large-scale integrated (ULSI) semiconductor circuits.

32. Thin films of conductors and insulators can be formed into patterns by using the processes of photolithography in combination with

etching. Photolithography is used to transfer a mask pattern etched into a photo mask onto a photosensitive film that has been applied on the silicon wafer's surface. The photosensitive film is called photoresist. During wafer exposure with visible or ultraviolet light, the photo mask with a desired opaque pattern prevents penetration of the light through the opaque pattern, while allowing radiation to pass through the mask's clear glass. The chemical structure of photoresist is such that the light changes its solubility in a developing solution. The photoresist can then be locally removed from the surface of the wafer during a subsequent developing process.

33. The process that immediately follows the photolithography process is the removal of material from areas of the wafer unprotected by photoresist. Various etching techniques are used for this purpose. Etching processes are characterized by their selectivity to a specific material and their degree of anisotropy (vertical etching). For example, the etching agent should attack silicon dioxide, but not photoresist or silicon. Upon completion of the etching, the etching mask is removed.

34. The details of the etching process depends on the etching speed and the thickness (and variation in the thickness) of the layer being etched. The etch process is typically chosen to have a fast etch rate of the layer being etched and a slow etch of the underlining layer. This ensures that we do not penetrate the underlining layer even if a portion of the layer is etched with a minimal thickness.

B. Image Sensor Technology

35. Generally, an image sensor is an electrical device which captures light and converts the light into electric signals to form an electronic representation of an image. Typically, the light receiving portions are analog circuits which, when exposed to light, create a stored charge relative to the intensity and duration of the light striking the circuit. This charge is then read out by peripheral circuitry and often converted to digital signals usable by modern computing systems to display or store the information.

36. Semiconductor imaging devices, such as described in the '169 patent, can be formed on silicon wafers. In its pure, crystalline form, silicon is a poor conductor. However, by introducing specific ions or impurities into the silicon (a process known as "doping"), silicon can be made to conduct electricity in a controlled fashion. Silicon is doped to form either an "n-type region" (a region that can donate electrons) or a "p-type region" (a region that can accept electrons, which is also referred to as donating "holes") depending on the specific ions or impurities used, with each region having unique electrical properties. To indicate relative doping concentrations, it is common to use a "+" or "-" following the doping type. Thus, a "p-type" region would have a lower doping concentration compared to a "p+ region," which in turn would have a lower doping concentration compared to a "p++ region."

37. The n-type and p-type regions in a semiconductor are formed by shooting ions into the silicon substrate. A p-type region can be formed, for example, by implanting boron into the substrate and activating the boron by a heat treatment at a high temperature. An n-type region can be formed, for example, by implanting phosphorus into the substrate and activating the phosphorus by a heat treatment at a high temperature. The ion implantation energy will determine how deep the ions will be embedded in the substrate, and the dose will determine the doping concentration. An additional heat treatment will diffuse the implanted ions deeper and, in every direction, away from the original implant location.

38. A backside-illuminated image sensor (BSI) is an image sensor where light is sensed from the back of the silicon substrate, while the circuit that monitors the sensing and digitally processes the image signal is located on the front side. Backside sensing has the advantage of being able to sense light from the entire back of the substrate, without being blocked by circuitry that covers part of the front side.

C. The Technology Of Backside Illuminated Image Sensors

39. Backside illumination has several benefits such as increasing the quantum efficiency of the sensor. As mentioned above, backside illumination can improve quantum efficiency by allowing more light to reach the sensor. This is a major advantage over front-illuminated image sensors, which can have quantum efficiencies as low as 50%.

40. Backside sensors also reduce noise in images. This is because the light that reaches the sensor is not scattered by the circuitry on the front side.

41. Backside illumination also improves the dynamic range of images. This is the range of brightness levels that an image sensor can capture. Front-illuminated image sensors often have limited dynamic range, which can lead to washed-out or dark images.

42. Solid state image sensors are used in video cameras and are in integrated circuits using a complementary metal oxide semiconductor (“CMOS”) technology. These image sensors are based on a two-dimensional array of pixels where each pixel includes a sensing element – a photo diode - that is capable of converting a portion of an optical image into an electronic signal and includes circuitry to measure the intensity of light detected by the sensing element and then to generate electronic signals are then used by other circuitry to regenerate the optical image on a display. CMOS image sensors were first developed in 1967 and utilize the photovoltaic response. The photo voltaic response occurs when silicon is exposed to light. When photons in the visible and near-IR regions of the spectrum impinge on a silicon surface and create an electron-hole pair. The number of electrons generated is proportional to the light intensity.

43. CMOS image sensors have benefited from advances in CMOS technology for microprocessors and application specific integrated circuits.

Shrinking lithography, coupled with advanced signal-processing algorithms provide for sensor arrays, sensor array control, and image processing used in integrated circuit manufactured with well-established CMOS techniques.

44. Frontside illuminated image sensors (“FSI”), the frontside surface of the semiconductor substrate includes the image sensor, the CMOS circuitry, and metal lines that connect the image sensors to the CMOS circuitry and that connect both to peripheral circuitry that controls the image sensor in general, that transmits signals to or from the image sensor, that receive, interpret, and implement control signals from off the image sensor, and that provide power and power control to all the circuits and sensors.

45. CMOS Image Sensors (CIS) may be either FSI or BSI; the difference between a BSI image sensor and an FSI image sensor is the arrangement of imaging elements in the sensor with respect to incident light to the pixel. In FSI, the photons entering the silicon from the frontside pass through the metal wiring layers before they reach the image sensors.

46. In contrast, in a BSI image sensor, the photons reach image sensors directly from the backside without passing through the metal wiring layers on the front side.

D. The Invention Of The ‘169 Patent

47. I understand that the ‘169 patent is directed generally to a unique BSI

image sensor and to methods of manufacturing the unique BSI image sensor. The '169 patent discloses an improved sensor by optimizing the collection of electrons all the way around the photodiode 110 (pink). The '169 Patent achieves its objective by implanting a "p" buried layer 126 (orange) in all the area inside the pixel under the P well and the N well surrounding the photodiode. Figure 1 below of the '169 patent is a cross-section of the wafer where the front wafer surface where the Photodiode, P well 116 (green), and N well 114 (blue) originate from is the bottom of the figure.

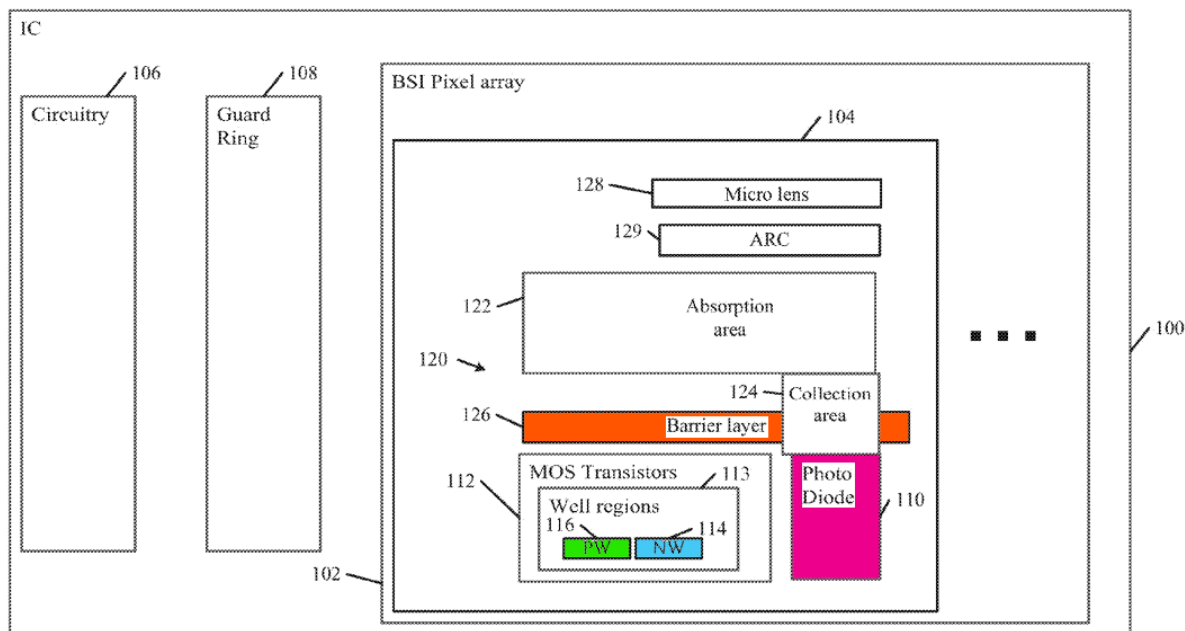


Fig. 1

48. The '169 Patent discloses that it creates the P buried layer by a high energy implant. Figure 3D is another cross-section showing the P buried layer 326 (orange) underneath all the area of the pixel. The P buried layer is underneath both P well (green) and N well (blue).

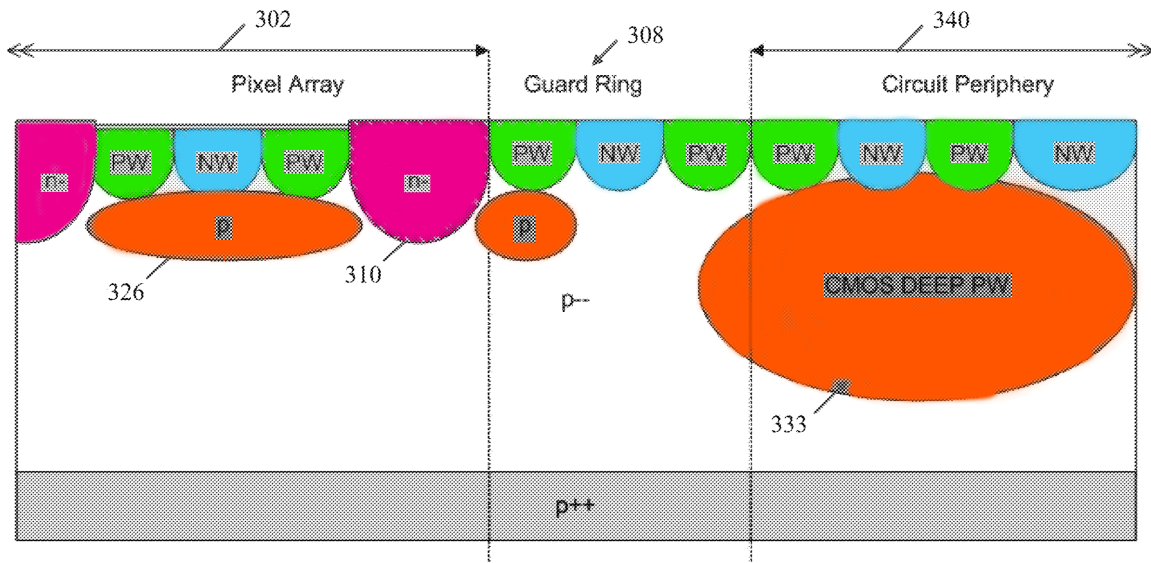


Fig. 3D

49. The '169 Patent disclose that electrons will be collected underneath both the N well and P well and drift toward the photo diode:

In one example, the electrons may be generated in the well regions 113 of pixel 104. According to this example, a substantial amount of electrons, e.g., all electrons, which may be generated in NW region 114, may be lost and/or flow to the VDD and, as a result, may not contribute to a photo signal received by photodiode 110.

'169 Patent, 5:5-10.

In one example, absorption of the electrons in the PW region 116 may increase a probability of recombination of the electrons, and as a result, a reduced number of electrons may be collected by the photodiode 110.

'169 Patent, 5:16-19.

50. The patent '169 explains how to solve this problem with a buried layer to improve the efficiency of collection. The buried layer under both P well and N well deflects electrons away from the N-well and the P-well:

a barrier layer 126 may be configured to reduce or even prevent diffusion of the electrons from absorption area 122 to the N-well region 114 and/or to the P-well region 116.

‘169 Patent, 6:57-60. In the ‘169 Patent, the “absorption area is the large area under both the “N-Well” and the “P-Well.”

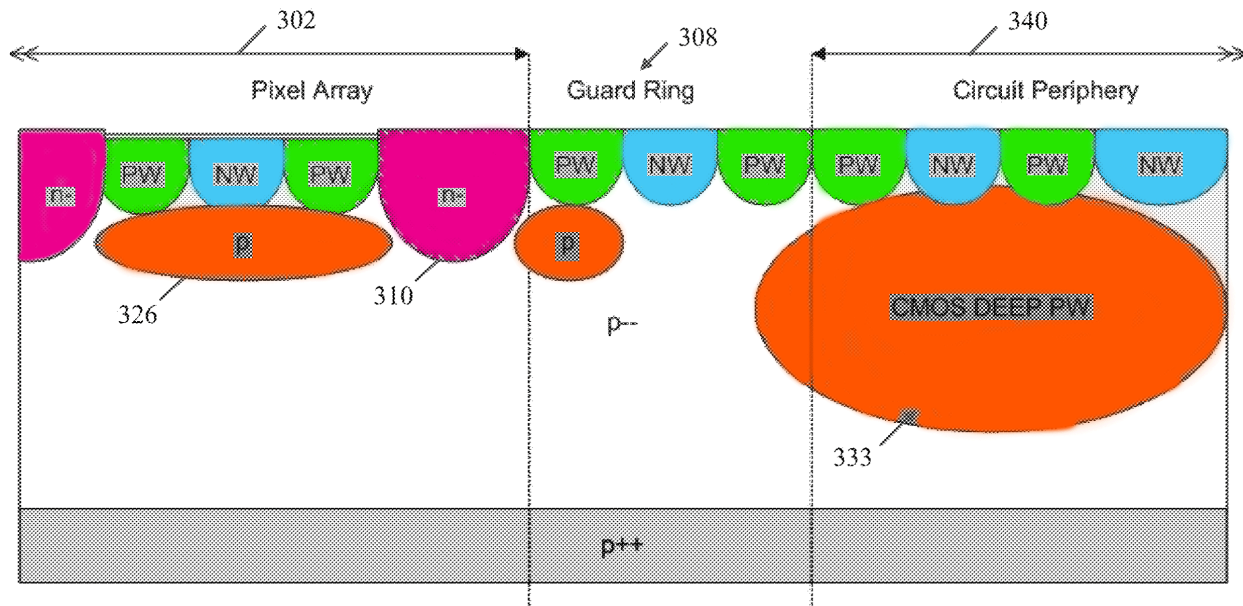


Fig. 3D

VIII. SUMMARY OF PETITIONER’S CITED REFERENCES

51. Petitioner cites five references, Lauxtermann, Ballin, Zucca, Akiyama, and Wang.

A. Lauxtermann

52. Patent 7,498,650 describes a triple well CMOS image sensor which use back bias to operate the sensor. Ex. 1004 (hereinafter, “Lauxtermann”).

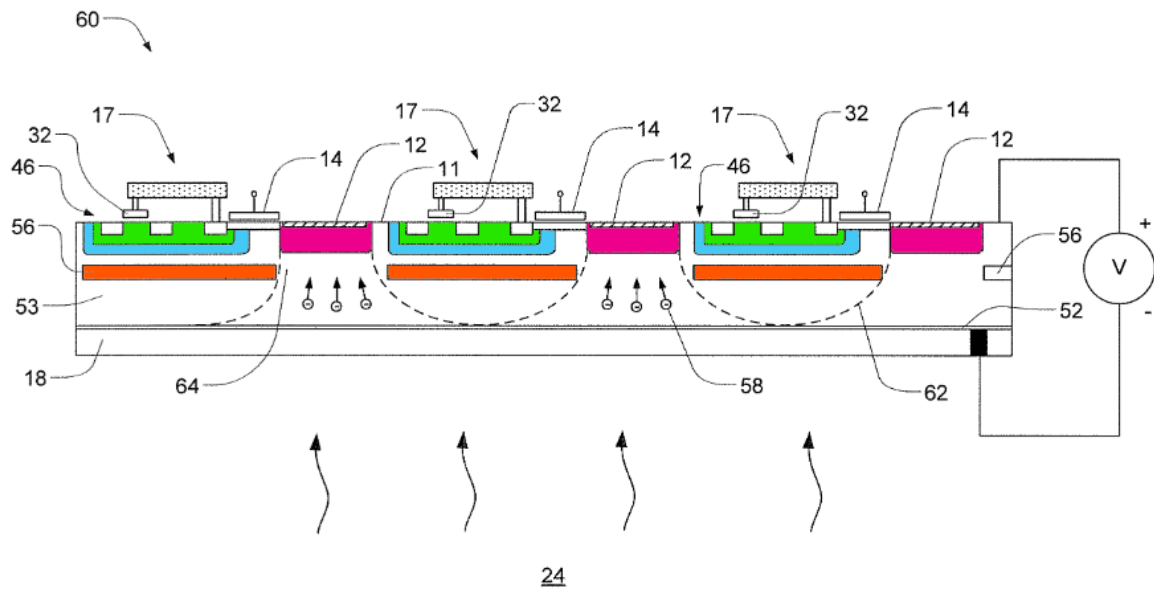


Figure 5

Lauxtermann, Fig. 5.

53. As Figure 4 shows:

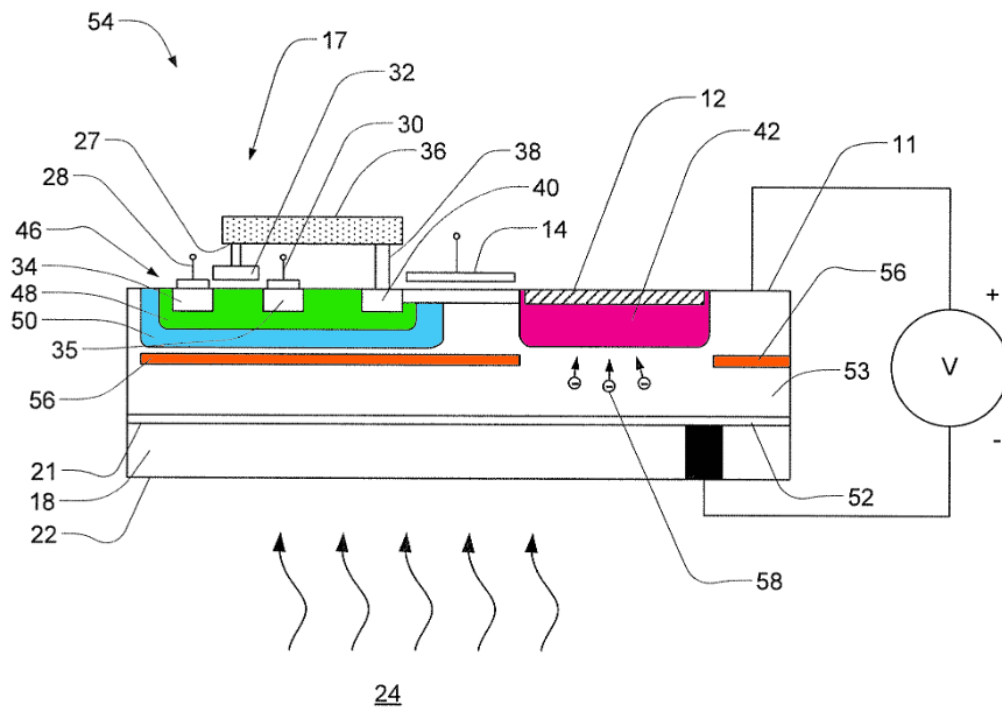


Figure 4

Lauxtermann does not have a P-well adjacent to an N-Well, so any supposed “barrier layer” does not deflect electrons from a P-Well. What Petitioner points to as the “P-Well” 48 (green) is within an N-Well 50 (blue). “N-Well” 50 (blue) shields the “P-Well” 48 (green). In addition, Lauxtermann teaches that the device is biased – as shown by the voltage source Lauxtermann shows on the right side of Figure 4 and in its text:

Underneath the source follower transistor 17 is the triple well configuration 46 with n-doped 34, 35, and 40, isolated in p-well 48 that is further contained in n-well 50 Since the source follower transistor 17 may not be operable due to a back-side bias applied to the backside electrode 52, the triple well configuration 46 may be employed to maintain a constant threshold voltage of the NMOS pixel circuitry

Lauxtermann, Fig. 5 & 4:29-36.

54. Lauxtermann does not disclose an “absorption region” and does not disclose a “collection region.” Because Lauxtermann uses an electrostatic lense:

Electrical field lines 62 form around the p-layers 56 and create electron funnels 64 that direct charge 58 to drift towards the pinned photodiode 12.

Lauxtermann, 5:52-54, the “electron funnel 64” limits the absorption to the small area directly under the pinned photodiode 12. *Id.*

55. In Lauxtermann, the photodiode is a “pinned diode.”

a p-layer may be used to drift the charges to the charge collecting element of *the pinned photodiode 12*. FIG. 4 illustrates a backside illuminated CMOS image sensor 54 with a p-layer 56. The CMOS image sensor 54 may *include pinned photo diode 12*, source follower

transistor 17, and backside electrode 52. The *pinned photodiode 12 collects charge due to light 24 incident on the pixel and outputs a signal to the source follower transistor 17*. Underneath the pinned photodiode 12 is n-doped region 42 of a high resistivity semiconductor layer 53. Transfer gate 14 transfers the signal from the pinned photodiode 12 to the NMOS source follower device 17

Lauxtermann, 4:67 – 5:10 (emphasis added).

56. Lauxtermann starts with a “SOI wafer.” Lauxtermann, 3:24-27. An “SOI wafer” is a silicon on insulator wafer where the underneath the backside surface of the wafer is a dielectric such as silicon oxide.

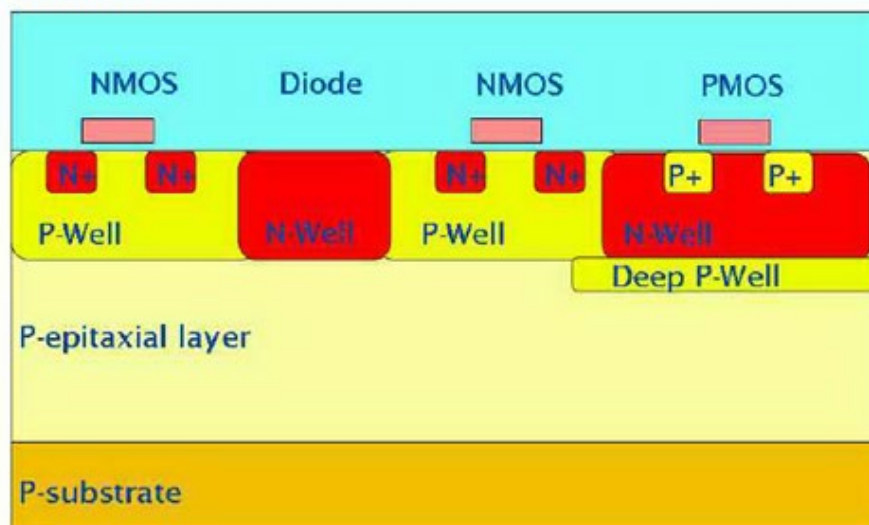
The starting SOI wafer for the CMOS image sensor 10 includes a buried oxide layer 18 between a silicon wafer and the semiconductor layer 16. The semiconductor layer 16 includes at least one pinned photodiode 12.

Id.

B. Ballin

57. Ballin discloses a “Deep P-Well” only under the “N-Well.”

Figure 2. Schematic cross-section of a CMOS wafer with the deep P-well implant. Not drawn to scale.



2.2. INMAPS CMOS

Ballin, Fig. 2. To the extent Petitioner contends that the “Deep P-Well” is a “barrier layer,” it does not extend under the P-Well. Ballin, Fig. 2. Ballin does not have a “barrier layer” that separates an absorption area from the P-Wells. Ballin does not disclose an absorption area separate from a collection area adjacent to the photodiode.

C. Zucca

58. Zucca discloses a “Deep P-Well” only under the “N-Well.” Zucca at Fig. 1.

D. Akiyama

59. I understand that Petitioner only contends that Akiyama discloses “an antireflective coating (ARC) and a microlens 21.” Pet. 19.

E. Wang

60. I understand that Petitioner only contends that Wang discloses features of a “guard ring structures.” Pet., 20.

IX. THE CITED PRIOR ART AND THE CHALLENGED CLAIMS

A. Ground 1: Lauxtermann Does Not Render Claims 1 – 6 Or 10 - 15 Obvious

a. Claim 1

i. Absorption Area

61. I understand that Claim 1 includes the limitation:

an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, and said collection area

connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode

‘169 Patent, 15:51-57. I understand that Petitioner asserts that:

“absorption area” and “collection area” are disclosed because Lauxtermann discloses [w]ithin that epitaxial layer, layer 53 includes a collection area and an absorption area, the former of which connects the absorption area to the photodiode.”

Pet. at 27. There is also a footnote stating:

[a]ccording to the plain language of the claims, absorption area and collection area are parts of the epitaxial layer. They need not be separate layers.

Id.

62. I understand, and a POSITA would understand that the ‘169 patent describes and defines separate absorption area 122 and collection area 124 as shown in FIG. 5. ‘169 Patent, 8:29-46. In the ‘169 Patent, the “absorption area” is the large area under both the “N-Well” and the “P-Well. Petitioner does not point to specific disclosure in Lauxtermann that discloses, teaches or suggests the “absorption area” as the ‘169 Patent discloses. A POSITA would not understand that Lauxtermann discloses, teaches or suggests to teach an epi layer comprising an absorption area and a collection area connecting the absorption area to the photodiode according to Claim 1. Lauxtermann does not disclose an “absorption region” and does not disclose a “collection region.” Because Lauxtermann uses an electrostatic lense:

Electrical field lines 62 form around the p-layers 56 and create electron funnels 64 that direct charge 58 to drift towards the pinned photodiode 12.

Lauxtermann, 5:52-54, the “electron funnel 64” limits the absorption to the small area directly under the pinned photodiode 12. *Id.*

ii. Barrier Layer Separating Said Absorption Area From Said One Or More Well Regions

63. The alleged barrier layer that Lauxtermann discloses does not define a separate absorption area. *See* Paragraphs 52 – 54.

b. Claim 2

64. I understand that Claim 2 depends from Claim 1. I understand that as Lauxtermann does not render Claim 1 obvious, Lauxtermann does not render Claim 2 obvious.

c. Claim 3

65. I understand that Claim 3 depends from Claim 1. I understand that as Lauxtermann does not render Claim 1 obvious, Lauxtermann does not render Claim 3 obvious.

d. Claim 4

66. I understand that Claim 4 depends from Claim 1. I understand that as, Lauxtermann does not render Claim 1 obvious because Lauxtermann does not render Claim 4 obvious.

e. Claim 5

67. I understand that Claim 5 depends from Claim 1. I understand that as, Lauxtermann does not render Claim 1 obvious because Lauxtermann does not render

Claim 5 obvious.

f. Claim 6

68. I understand that Claim 6 depends from Claim 1. I understand that as, Lauxtermann does not render Claim 1 obvious because Lauxtermann does not render Claim 6 obvious.

g. Claim 10

69. I understand that Claim 10 depends from Claim 1. I understand that as, Lauxtermann does not render Claim 1 obvious because Lauxtermann does not render Claim 10 obvious.

h. Claim 11

70. I understand that Claim 11 depends from Claim 10. I understand that as, Lauxtermann does not render Claim 10 obvious because Lauxtermann does not render Claim 11 obvious.

i. Claim 12

71. I understand that Claim 12 depends from Claim 1. I understand that as, Lauxtermann does not render Claim 1 obvious because Lauxtermann does not render Claim 12 obvious.

j. Claim 13

72. I understand that Claim 13 depends from Claim 1. I understand that as, Lauxtermann does not render Claim 1 obvious because Lauxtermann does not render Claim 12 obvious.

k. Claim 14

73. I understand that Claim 14 depends from Claim 1. I understand that as, Lauxtermann does not render Claim 1 obvious because Lauxtermann does not render Claim 14 obvious.

l. Claim 15

74. I understand that Claim 15 depends from Claim 1. I understand that as, Lauxtermann does not render Claim 1 obvious because Lauxtermann does not render Claim 15 obvious.

B. Ground 2: Lauxtermann In View of Zucca Does Not Render Claims 2, 6, 7, Or 9 Obvious

a. Claim 2

75. I understand that Petitioner contends that Zucca discloses:

discloses “a high energy deep Pwell implant is deposited beneath the PMOS competitive NWELLS.” The deep Pwell implant “represents a barrier for the charge diffusing in the epitaxial layer, preventing the carriers from being collected y he positively biased Nwells hosting the PMOS transistors

Pet., 17 – 18 (internal citations omitted).

76. I understand that Petitioner has not argued that Lauxtermann in view Zucca discloses, teaches, or suggests the limitations of Claim 1 including the “barrier layer underneath a P well”, “epitaxial layer comprising an absorption area and a collection area” or the “barrier layer” where the “barrier layer” separates “said absorption area from said one or more well regions.” ‘169 Patent, 15:51-53 & 15:57-

58. Accordingly, I understand that Lauxtermann in view of Zucca would not render Claim 1 obvious, Lauxtermann in view of Zucca would not render Claim 2 obvious.

77. I understand that Petitioner cites Zucca for the proposition that Zucca teaches a low fill factor diode and epitaxial layers with certain minimum thicknesses. Zucca, however, does not disclose backside illumination sensors. Nothing in Zucca or Lauxtermann would give a POSITA motivation to combine them to achieve the patented properties.

b. Claim 6

78. Lauxtermann in view of Zucca does not render Claim 1 obvious, see Section IX.A.a, I understand that Lauxtermann in view of Zucca does not render Claim 6 obvious.

c. Claim 7

79. Lauxtermann in view of Zucca does not render Claim 1 obvious, see Section IX.A.a, I understand that Lauxtermann in view of Zucca does not render Claim 7 obvious.

d. Claim 9

80. Lauxtermann in view of Zucca does not render Claim 1 obvious, see Section IX.A.a, I understand that Lauxtermann in view of Zucca does not render Claim 9 obvious.

C. Ground 3: Lauxtermann In View Of Akiyama Does Not Render Claims 10 Or 11 Obvious

81. As I discuss above, Lauxtermann fails to render Claim 1 obvious. The additional disclosure in Akiyama, which I understand Petitioner does not argue as being relevant to the obviousness of Claim 1, does not render Claim 1 obvious. Thus, dependent Claims 10 and 11, which depend from Claim 1, are not obvious.

D. Ground 4: Lauxtermann In View Of Wang Does Not Render Claim 16 - 20 Obvious

82. Lauxtermann fails to render claim 1 obvious. For the same reasons, Lauxtermann does not disclose the epi layer limitation in independent Claims 16 and 19. Nor does Lauxtermann disclose the “barrier layer separating said absorption area from said well regions.” The additional disclosure in Wang, which I understand Petitioner does not argue as disclosing the epi layer limitation or the barrier layer limitation, would not render independent Claims 16 or 19 obvious.

a. Claim 17

83. Claim 17 depends from Claim 16. Lauxtermann in view of Wang does not render Claim 17 obvious because Lauxtermann in view of Wang does not render Claim 16 obvious.

b. Claim 18

84. Claim 18 depends from Claim 17. Lauxtermann in view of Wang does not render Claim 18 obvious because Lauxtermann in view of Wang does not render Claim 17 obvious.

c. Claim 20

85. Claim 20 depends from Claim 19. Lauxtermann in view of Wang does not render Claim 20 obvious because Lauxtermann in view of Wang does not render Claim 19 obvious.

E. Ground 5: Ballin Does Not Render Claims 1, 3 – 8, Or 12 - 15 Obvious

a. Claim 1

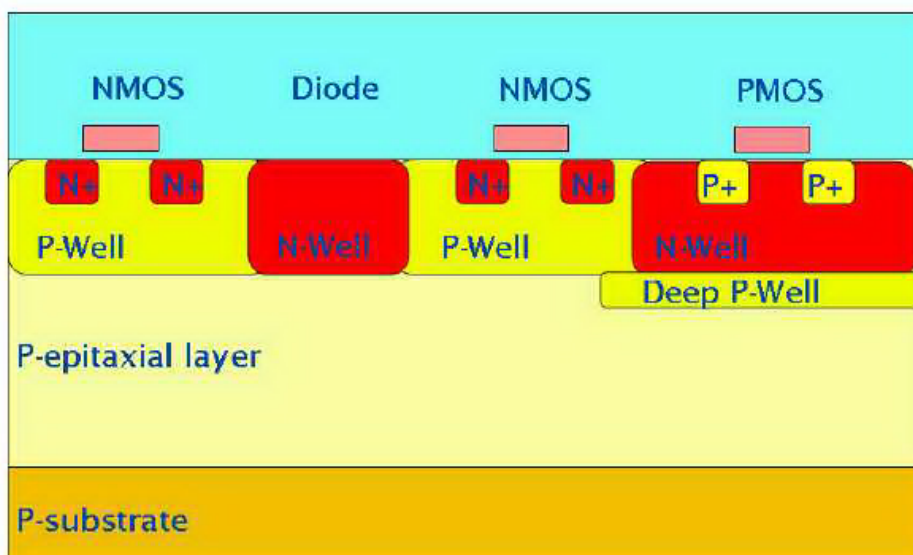
86. I understand that Claim 1 includes the limitation:

a barrier layer separating said absorption area from said one or more well regions.

‘169 Patent, 15:57-58. I understand that Petitioner argues that “Ballin’s deep P-well separates the N-wells of the PMOS transistors from the P-epitaxial layer” and “[a] POSA would have understood that Ballin’s deep P-well implant is a barrier layer separating the absorption area from the one or more well regions.” Pet. at 73-74.

87. The deep P-well does not function as a barrier layer because it separates the asserted absorption area only from the N-well of the PMOS transistors, but not both the N-well and P-well regions. A POSITA would not understand that Ballin’s deep P-well implant is barrier layer separating the absorption area from the one or more well regions Ballin describes the function of the “deep P-well” to isolate only an N-well, but not the P-well. Ballin, 4-5.

Figure 2. Schematic cross-section of a CMOS wafer with the deep P-well implant. Not drawn to scale.



2.2. INMAPS CMOS

Ballin, Fig. 2.

88. Further, the “absorption area” and “collection area” recited in Claim 1 (“an epitaxial (epi) layer comprising an absorption area and a collection area, said absorption area to absorb incoming photons and to generate electrons responsive to absorbed photons, and said collection area connecting said absorption area to said photodiode to provide said electrons from said absorption area to said photodiode”) are not also disclosed by Ballin.

89. Petitioner asserts that “absorption area” and “collection area” are disclosed because FIG. 2 of Ballin discloses “an epitaxial layer that includes an absorption area and a collection area, the latter of which connects the absorption area to a photodiode.” Pet. 71. There is also the same footnote as shown in the Petitioner’s

arguments with Lauxtermann:

[a]ccording to the plain language of the claims, absorption area and collection area are parts of the epitaxial layer. They need not be separate layers.

Id.

90. The '169 patent describes and defines the absorption area 122 (generation area) and collection area 124 as shown in FIG. 2 as separate areas with different physical locations.

91. Ballin does not teach an epi layer comprising an absorption area and a collection area connecting the absorption area to the photodiode. *See* paragraphs 57, 87.

b. Claim 2

92. Claim 2 depends from Claim 1. Ballin does not render Claim 2 obvious because Ballin does not render Claim 1 obvious.

c. Claim 3

93. Claim 2 depends from Claim 1. Ballin does not render Claim 2 obvious because Ballin does not render Claim 1 obvious.

d. Claim 4

94. Claim 2 depends from Claim 1. Ballin does not render Claim 2 obvious because Ballin does not render Claim 1 obvious.

e. Claim 5

95. Claim 2 depends from Claim 1. Ballin does not render Claim 2 obvious

because Ballin does not render Claim 1 obvious.

f. Claim 6

96. Claim 2 depends from Claim 1. Ballin does not render Claim 2 obvious because Ballin does not render Claim 1 obvious.

g. Claim 7

97. Claim 2 depends from Claim 1. Ballin does not render Claim 2 obvious because Ballin does not render Claim 1 obvious.

h. Claim 8

98. Claim 2 depends from Claim 1. Ballin does not render Claim 2 obvious because Ballin does not render Claim 1 obvious.

i. Claim 12

99. Claim 2 depends from Claim 1. Ballin does not render Claim 2 obvious because Ballin does not render Claim 1 obvious.

j. Claim 13

100. Claim 2 depends from Claim 1. Ballin does not render Claim 2 obvious because Ballin does not render Claim 1 obvious.

k. Claim 14

101. Claim 2 depends from Claim 1. Ballin does not render Claim 2 obvious because Ballin does not render Claim 1 obvious.

l. Claim 15

102. Claim 2 depends from Claim 1. Ballin does not render Claim 2 obvious

because Ballin does not render Claim 1 obvious.

F. Ground 6: Ballin In View Of Akiyama Does Not Render Claims 10 Or 11 Obvious

103. Ballin in view of Akiyama fails to render claim 1 obvious. Thus, the additional disclosure in Akiyama, which I understand that Petitioner does not argue as being relevant to the obviousness of Claim 1, does not render claim 1 obvious.

a. Claim 10

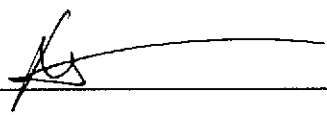
104. Akiyama does not disclose, teach, or suggest a buried P layer beneath the n-well and p-well. Akiyama does not disclose, teach, or suggest a separate absorption region connected to a collection region.

b. Claim 11

105. I understand that Claim 11 depends from Claim 10 that depends from Claim 1. As Ballin in view of Akiyama does not render Claim 10 obvious, I understand Ballin in view of Akiyama does not render Claim 11 obvious.

106. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of the '169 patent.

Dated: Oct 11, 2023



RON MALTIEL