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IEEE Std 802.3™-2002
(Revision of IEEE Std 802.3, 2000 Edition)

IEEE Standards

802.3™

IEEE Standard for Information technology—

Telecommunications and information exchange between systems—

Local and metropolitan area networks—

Specific requirements

Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications

IEEE Computer Society

Sponsored by the
LAN/MAN Standards Committee

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Abstract: The media access control characteristics for the Carrier Sense Multiple Access with Collision Detection (CSMA/CD) access method for shared medium local area networks are described. The control characteristics for full duplex dedicated channel use are also described. Specifications are provided for MAU types 1BASE5 at 1 Mb/s; Attachment Unit Interface (AUI) and MAU types 10BASE5, 10BASE2, FOIRL (fiber optic inter-repeater link), 10BROAD36, 10BASE-T, 10BASE-FL, 10BASE-FB, and 10BASE-FP at 10 Mb/s; Media Independent Interface (MII) and PHY types 100BASE-T4, 100BASE-TX, 100BASE-FX, and 100BASE-T2 at 100 Mb/s; and the Gigabit MII (GMII) and 1000BASE-X PHY types, 1000BASE-SX, 1000BASE-LX, and 1000BASE-CX, which operate at 1000 Mb/s (Gigabit Ethernet) as well as PHY type 1000BASE-T. Repeater specifications are provided at each speed. Full duplex specifications are provided at the Physical Layer for 10BASE-T, 10BASE-FL, 100BASE-TX, 100BASE-FX, 100BASE-T2, and Gigabit Ethernet. System considerations for multisegment networks at each speed and management information base (MIB) specifications and additions to support Virtual Bridged Local Area Networks (VLANs) as specified in IEEE P802.1Q are also provided. Also specified is an optional Link Aggregation sublayer which multiple physical links to be aggregated together to form a single logical link.

Keywords: Aggregated Link; Aggregator; Auto Negotiation; Category 5; copper; data processing; Ethernet; gigabit; information interchange, Link Aggregation; local area networks, management; MASTER-SLAVE; medium dependent interface; mode of data transmission; models; network interconnection; physical coding sublayer; Physical Layer; physical medium attachment; repeater; type field; VLAN TAG

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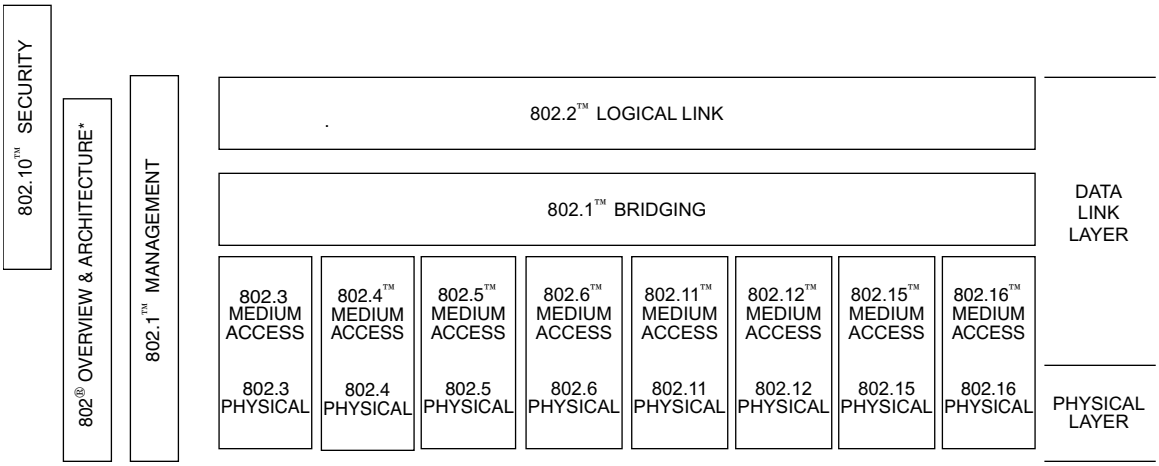
[1]Interpretations provided by 802.3 since November 1996 are available at http://www.ieee802.org/3/interp/index.html

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Introduction to IEEE Std 802.3-2002

This standard is part of a family of standards for local and metropolitan area networks. The relationship between the standard and other members of the family is shown below. (The numbers in the figure refer to IEEE standard numbers.[1])



* Formerly IEEE Std 802.1A™

This family of standards deals with the Physical and Data Link layers as defined by the International Organization for Standardization (ISO) Open Systems Interconnection (OSI) Basic Reference Model (ISO/IEC 7498-1: 1994). The access standards define seven types of medium access technologies and associated physical media, each appropriate for particular applications or system objectives. Other types are under investigation.

The standards defining the technologies noted above are as follows:

- IEEE Std 802 — *Overview and Architecture*.This standard provides an overview to the family of IEEE 802 Standards.
- IEEE Std 802.1B™ and 802.1k™ [ISO/IEC 15802-2] — *LAN/MAN Management*. Defines an OSI management-compatible architecture, and services and protocol elements for use in a LAN/MAN environment for performing remote management.
- IEEE Std 802.1D™ — *Media Access Control (MAC) Bridges*. Specifies an architecture and protocol for the interconnection of IEEE 802 LANs below the MAC service boundary.
- IEEE Std 802.1E™ [ISO/IEC 15802-4] — *System Load Protocol*. Specifies a set of services and protocol for those aspects of management concerned with the loading of systems on IEEE 802 LANs.
- IEEE Std 802.1F™ — *Common Definitions and Procedures for IEEE 802 Management Information*
- IEEE Std 802.1G™ [ISO/IEC 15802-5] — *Remote Media Access Control (MAC) Bridging*. Specifies extensions for the interconnection, using non-LAN communication technologies, of geographically separated IEEE 802 LANs below the level of the logical link control protocol.
- IEEE Std 802.1H™ [ISO/IEC TR 11802-5] — *Media Access Control (MAC) Bridging of Ethernet V2.0 in Local Area Networks*.

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- IEEE Std 802.2 [ISO/IEC 8802-2] — *Logical Link Control*.
- IEEE Std 802.3 — *CSMA/CD Access Method and Physical Layer Specifications*.
- IEEE Std 802.4 [ISO/IEC 8802-4] — *Token Passing Bus Access Method and Physical Layer Specifications*.
- IEEE Std 802.5 [ISO/IEC 8802-5] — *Token Ring Access Method and Physical Layer Specifications*.
- IEEE Std 802.6 [ISO/IEC 8802-6] — *Distributed Queue Dual Bus Access Method and Physical Layer Specifications*.
- IEEE Std 802.10 — *Interoperable LAN/MAN Security*.
- IEEE Std 802.11 [ISO/IEC DIS 8802-11] — *Wireless LAN Medium Access Control (MAC) and Physical Layer Specifications*.
- IEEE Std 802.12 [ISO/IEC 8802-12] — *Demand Priority Access Method, Physical Layer and Repeater Specifications*.
- IEEE Std 802.15 — *Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for: Wireless Personal Area Networks*.
- IEEE Std 802.16 — *Standard Air Interface for Fixed Broadband Wireless Access Systems*.

In addition to the family of standards, the following is a recommended practice for a common Physical Layer technology:

- IEEE Std 802.7™ — *IEEE Recommended Practice for Broadband Local Area Networks*.

Conformance test methodology

An additional standard, IEEE Std 1802.3™ provides conformance test information for 10BASE-T.

IEEE Std 802.3-2002

IEEE Std 802.3-2002 has been divided into three sectionss. The division is as follows:

Section One— Includes Clause 1 through Clause 20 and Annexes A through H.
Section Two—Includes Clause 21 through Clause 33 and Annexes 22A through 32A.
Section Three—Includes Clause 34 through Clause 43 and Annexes 36A through 43C.

This standard contains state-of-the-art material. The area covered by this standard is undergoing evolution. Revisions are anticipated to this standard within the next few years to clarify existing material, to correct possible errors, and to incorporate new related material. Details on the contents of this standard are provided on the following pages.

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The final conditions for approval of this standard were met on 14 January 2002. This standard was conditionally approved by the IEEE-SA Standards Board on 7 December 2001, with the following membership:

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The following individuals served as officers of IEEE 802.3 during the development of the standard:

IEEE Std 802.3 document	Date approved by IEEE and ANSI	Officers at the time of working group ballot
802.3-1985, Original 10 Mb/s standard, MAC, PLS, AUI, 10BASE5	23 June 1983 (IEEE) 31 December 1984 (ANSI)	**Donald C. Loughry,** *Working Group Chair*
802.3a ™-1988 (Clause 10), 10 Mb/s MAU 10BASE2	15 November 1985 (IEEE) 28 December 1987 (ANSI)	**Donald C. Loughry,** *Working Group Chair* **Alan Flatman,** *Task Force Chair*
802.3b ™-1985 (Clause 11), 10 Mb/s Broadband MAU, 10BROAD36	19 September 1985 (IEEE) 28 February 1986 (ANSI)	**Donald C. Loughry,** *Working Group Chair* **Menachem Abraham,** *Task Force Chair*
802.3c ™-1985 (9.1–9.8), 10 Mb/s Baseband Repeater	12 December 1985 (IEEE) 4 June 1986 (ANSI)	**Donald C. Loughry,** *Working Group Chair* **Geoffrey O. Thompson,** *Task Force Chair*
802.3d ™-1987 (9.9), 10 Mb/s Fiber MAU, FOIRL	10 December 1987 (IEEE) 9 February 1989 (ANSI)	**Donald C. Loughry,** *Working Group Chair* **Steven Moustakas,** *Task Force Chair*
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802.3j ™-1993 (Clauses 15–18), 10 Mb/s Fiber MAUs 10BASE-FP, FB, and FL	15 September 1993 (IEEE) 15 March 1994 (ANSI)	**Patricia Thaler,** *Working Group Chair* **Keith Amundsen,** *Task Force Chair (initial)* **Frederick Scholl,** *Task Force Chair (final)* **Michael E. Lee,** *Technical Editor*
802.3k ™-1993 (Clause 19), 10 Mb/s Layer Management, Repeaters	17 September 1992 (IEEE) 8 March 1993 (ANSI)	**Patricia Thaler,** *Working Group Chair* **Joseph S. Skorupa,** *Task Force Chair* **Geoffrey O. Thompson,** *Vice Chair and Editor*
802.3l ™-1992 (14.10), 10 Mb/s PICS Proforma 10BASE-T MAU	17 September 1992 (IEEE) 23 February 1993 (ANSI)	**Patricia Thaler,** *Working Group Chair* **Mike Armstrong,** *Task Force Chair and Editor* **Paul Nikolich,** *Vice Chair* **William Randle,** *Editorial Coordinator*
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802.3r ™-1996 (8.8), Type 10BASE5 Medium Attachment Unit PICS proforma	29 July 1996 (IEEE) 6 January 1997 (ANSI)	**Patricia Thaler,** *Working Group Chair* **Imre Juhász** , *Task Force Chair* **William Randle,** *Task Force Editor*

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802.3t ™-1995, 120 Ω informative annex to 10BASE-T	14 June 1995 (IEEE) 12 January 1996 (ANSI)	**Geoffrey O. Thompson,** *Working Group Chair* **Jacques Christ,** *Task Force Chair*
802.3u ™-1995 (Clauses 21–30), Type 100BASE-T MAC parameters, Physical Layer, MAUs, and Repeater for 100 Mb/s Operation	14 June 1995 (IEEE) 4 April 1996 (ANSI)	**Geoffrey O. Thompson,** *Working Group Chair* **Peter Tarrant,** *Task Force Chair (Phase 1)* **Howard Frazier,** *Task Force Chair (Phase 2)* **Paul Sherer,** *Editor-in-Chief (Phase 1)* **Howard Johnson,** *Editor-in-Chief (Phase 2)* **Colin Mick,** *Comment Editor*
802.3v ™-1995, 150 Ω informative annex to 10BASE-T	12 December 1995 (IEEE) 16 July 1996 (ANSI)	**Geoffrey O. Thompson,** *Working Group Chair* **Larry Nicholson,** *Task Force Chair*
802.3x ™-1997 and 802.3y ™-1997 (Revisions to 802.3, Clauses 31 and 32), Full Duplex Operation and Type 100BASE-T2	20 March 1997 (IEEE) 5 September 1997 (ANSI)	**Geoffrey O. Thompson,** *Chair* **David J. Law,** *Vice Chair* **Rich Seifert,** *Task Force Chair and Editor (802.3x)* **J. Scott Carter,** *Task Force Chair (802.3y)* **Colin Mick** , *Task Force Editor (802.3y)*
802.3z ™-1998 (Clauses 34–39, 41–42), Type 1000BASE-X MAC Parameters, Physical Layer, Repeater, and Management Parameters for 1000 Mb/s Operation	25 June 1998 (IEEE)	**Geoffrey O. Thompson,** *Chair* **David J. Law,** *Vice Chair* **Howard M. Frazier, Jr.,** *Task Force Chair and Editor* **Howard W. Johnson,** *Task Force Editor*
802.3aa ™-1998, Maintenance 5	25 June 1998 (IEEE)	**Geoffrey O. Thompson,** *Chair* **Colin Mick** , *Task Force Editor (100BASE-T Maintenance)*
802.3ac ™-1998, Frame Extensions for Virtual Bridged Local Area Network (VLAN) Tagging on 802.3 Networks	16 September 1998 (IEEE)	**Geoffrey O. Thompson,** *Chair* **David J. Law,** *Vice Chair* **Andy J. Luque,** *Secretary* **Ian Crayford,** *Task Force Chair* **Rich Seifert,** *Task Force Editor*
802.3ab ™-1999 (Clause 40), Physical Layer Parameters and Specifications for 1000 Mb/s Operation Over 4 Pair of Category 5 Balanced Copper Cabling, Type 1000BASE-T	26 June 1999 (IEEE)	**Geoffrey O. Thompson,** *Chair* **David J. Law,** *Vice Chair* **Robert M. Grow,** *Secretary* **George Eisler** , *Task Force Chair* **Colin Mick** , *Task Force Editor*
802.3ad ™-2000 (Clause 43), Aggregation of Multiple Link Segments	30 March 2000 (IEEE)	**Geoffrey O. Thompson,** *Chair* **David J. Law,** *Vice Chair* **Robert M. Grow,** *Secretary* **Steven Haddock,** *Task Force Chair* **Tony Jeffree,** *Co-Editor* **Rich Seifert,** *Co Editor*
802.3-2002 (Revision of the base), Carrier Sense Multiple Access with Collision Detection (CSMA/CD) access method and physical layer specifications	14 January 2002 (IEEE)	**Geoffrey O. Thompson,** *Chair* **David J. Law,** *Vice Chair* **Robert M. Grow,** *Secretary*

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ISO/IEC status

Certain portions of this standard have been approved at the international level and form standard ISO/IEC 8802-3, 2000 Edition. The remainder of IEEE Std 802.3 will be forwarded to ISO/IEC and will begin the process of ISO/IEC approval via the "fast-track" process. Any comments on the fast-track DIS will be handled in ISO/IEC JTC 1/SC 6.

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Information technology—
Telecommunications and information exchange between systems—
Local and metropolitan area networks—Specific requirements—

Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) access method and physical layer specifications

SECTION ONE: This section includes Clauses 1 through 20 and Annexes A through H.

1. Introduction

1.1 Overview

This is a comprehensive International Standard for Local Area Networks (LANs) employing CSMA/CD as the access method. This International Standard is intended to encompass several media types and techniques for signal rates from 1 Mb/s to 1000 Mb/s. This edition of the standard provides the necessary specifications for the following families of systems: a 1 Mb/s baseband system, 10 Mb/s baseband and broadband systems, a 100 Mb/s baseband system, and a 1000 Mb/s baseband system. In addition, it specifies a method for linearly incrementing a system's data rate by aggregating multiple physical links of the same speed into one logical link.

1.1.1 Basic concepts

This standard provides for two distinct modes of operation: half duplex and full duplex. A given IEEE 802.3 instantiation operates in either half or full duplex mode at any one time. The term "CSMA/CD MAC" is used throughout this standard synonymously with "802.3 MAC," and may represent an instance of either a half duplex or full duplex mode data terminal equipment (DTE), even though full duplex mode DTEs do not implement the CSMA/CD algorithms traditionally used to arbitrate access to shared-media LANs.

1.1.1.1 Half duplex operation

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If, after initiating a transmission, the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again. Each aspect of this access method process is specified in detail in subsequent clauses of this standard.

Half duplex operation can be used with all media and configurations allowed by this standard.

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1.1.1.2 Full duplex operation

Full duplex operation allows simultaneous communication between a pair of stations using point-to-point media (dedicated channel). Full duplex operation does not require that transmitters defer, nor do they monitor or react to receive activity, as there is no contention for a shared medium in this mode. Full duplex mode can only be used when all of the following are true:

a) The physical medium is capable of supporting simultaneous transmission and reception without interference.
b) There are exactly two stations connected with a full duplex point-to-point link. Since there is no contention for use of a shared medium, the multiple access (i.e., CSMA/CD) algorithms are unnecessary.
c) Both stations on the LAN are capable of, and have been configured to use, full duplex operation.

The most common configuration envisioned for full duplex operation consists of a central bridge (also known as a switch) with a dedicated LAN connecting each bridge port to a single device. Repeaters as defined in this standard are outside the scope of full duplex operation.

Full duplex operation constitutes a proper subset of the MAC functionality required for half duplex operation.

1.1.2 Architectural perspectives

There are two important ways to view local area network (LAN) design corresponding to

a) *Architecture*. Emphasizing the logical divisions of the system and how they fit together.
b) *Implementation*. Emphasizing actual components, their packaging, and interconnection.

This standard is organized along architectural lines, emphasizing the large-scale separation of the system into two parts: the Media Access Control (MAC) sublayer of the Data Link Layer and the Physical Layer. These layers are intended to correspond closely to the lowest layers of the ISO/IEC Model for Open Systems Interconnection (see Figure 1–1). (See ISO/IEC 7498-1: 1994.[1]) The Logical Link Control (LLC) sublayer and MAC sublayer together encompass the functions intended for the Data Link Layer as defined in the OSI model.

1.1.2.1 Architectural rationale

An architectural organization of the standard has two main advantages:

a) *Clarity*. A clean overall division of the design along architectural lines makes the standard clearer.
b) *Flexibility*. Segregation of medium-dependent aspects in the Physical Layer allows the LLC and MAC sublayers to apply to a family of transmission media.

Partitioning the Data Link Layer allows various media access methods within the family of LAN standards.

The architectural model is based on a set of interfaces that may be different from those emphasized in implementations. One critical aspect of the design, however, shall be addressed largely in terms of the implementation interfaces: compatibility.

1.1.2.2 Compatibility interfaces

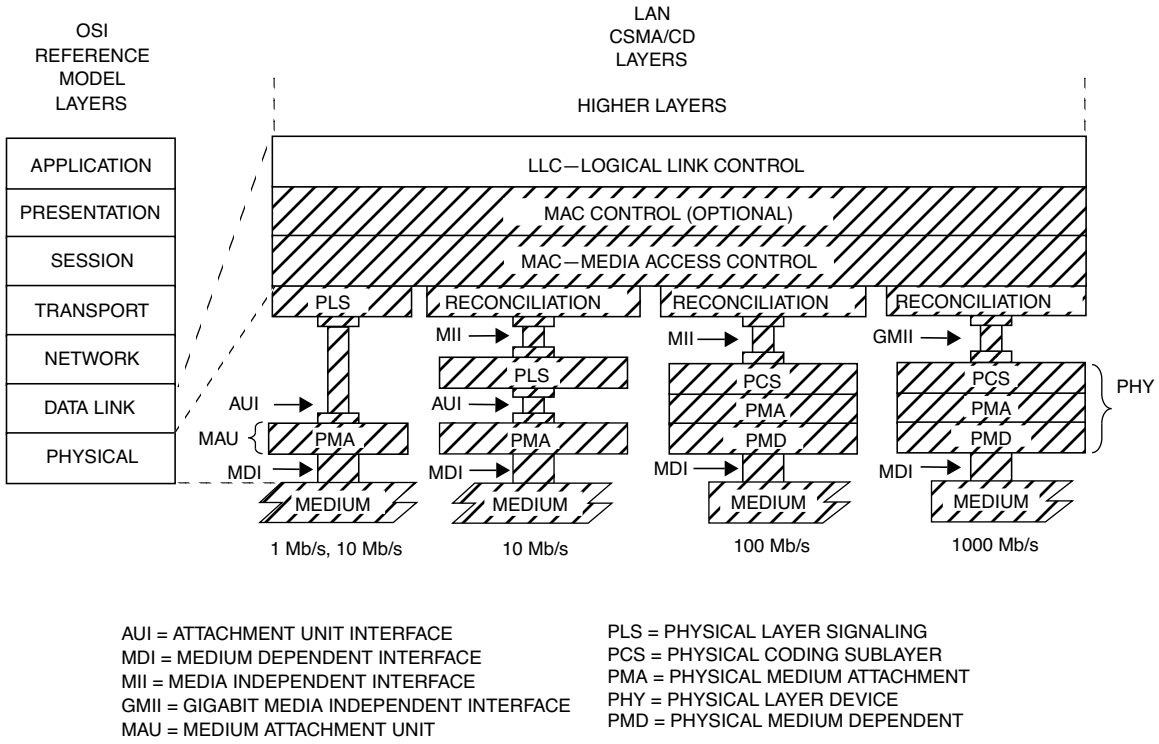
Five important compatibility interfaces are defined within what is architecturally the Physical Layer.

[1]For information about references, see 1.3.

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AUI = ATTACHMENT UNIT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MAU = MEDIUM ATTACHMENT UNIT

PLS = PHYSICAL LAYER SIGNALING
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 1–1—LAN standard relationship to the ISO/IEC Opens Systems Interconnection (OSI) reference model

a) *Medium Dependent Interfaces (MDI)*. To communicate in a compatible manner, all stations shall adhere rigidly to the exact specification of physical media signals defined in Clause 8 (and beyond) in this standard, and to the procedures that define correct behavior of a station. The medium-independent aspects of the LLC sublayer and the MAC sublayer should not be taken as detracting from this point; communication by way of the ISO/IEC 8802-3 [IEEE Std 802.3] Local Area Network requires complete compatibility at the Physical Medium interface (that is, the physical cable interface).

b) *Attachment Unit Interface (AUI)*. It is anticipated that most DTEs will be located some distance from their connection to the physical cable. A small amount of circuitry will exist in the Medium Attachment Unit (MAU) directly adjacent to the physical cable, while the majority of the hardware and all of the software will be placed within the DTE. The AUI is defined as a second compatibility interface. While conformance with this interface is not strictly necessary to ensure communication, it is highly recommended, since it allows maximum flexibility in intermixing MAUs and DTEs. The AUI may be optional or not specified for some implementations of this standard that are expected to be connected directly to the medium and so do not use a separate MAU or its interconnecting AUI cable. The PLS and PMA are then part of a single unit, and no explicit AUI implementation is required.

c) *Media Independent Interface (MII)*. It is anticipated that some DTEs will be connected to a remote PHY, and/or to different medium dependent PHYs. The MII is defined as a third compatibility interface. While conformance with implementation of this interface is not strictly necessary to ensure communication, it is highly recommended, since it allows maximum flexibility in intermixing PHYs and DTEs. The MII is optional.

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d) *Gigabit Media Independent Interface (GMII)*. The GMII is designed to connect a gigabit-capable MAC or repeater unit to a gigabit PHY. While conformance with implementation of this interface is not strictly necessary to ensure communication, it is highly recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at gigabit speeds. The GMII is intended for use as a chip-to-chip interface. No mechanical connector is specified for use with the GMII. The GMII is optional.
e) *Ten-bit Interface (TBI)*. The TBI is provided by the 1000BASE-X PMA sublayer as a physical instantiation of the PMA service interface. The TBI is highly recommended for 1000BASE-X systems, since it provides a convenient partition between the high-frequency circuitry associated with the PMA sublayer and the logic functions associated with the PCS and MAC sublayers. The TBI is intended for use as a chip-to-chip interface. No mechanical connector is specified for use with the TBI. The TBI is optional.

1.1.3 Layer interfaces

In the architectural model used here, the layers interact by way of well-defined interfaces, providing services as specified in Clauses 2 and 6. In general, the interface requirements are as follows:

a) The interface between the MAC sublayer and its client includes facilities for transmitting and receiving frames, and provides per-operation status information for use by higher-layer error recovery procedures.
b) The interface between the MAC sublayer and the Physical Layer includes signals for framing (carrier sense, receive data valid, transmit initiation) and contention resolution (collision detect), facilities for passing a pair of serial bit streams (transmit, receive) between the two layers, and a wait function for timing.

These interfaces are described more precisely in 4.3. Additional interfaces are necessary to provide for MAC Control services, and to allow higher level network management facilities to interact with these layers to perform operation, maintenance, and planning functions. Network management functions will be discussed in Clause 30.

1.1.4 Application areas

The applications environment for the LAN is intended to be commercial and light industrial. Use of CSMA/CD LANs in home or heavy industrial environments, while not precluded, is not considered within the scope of this standard.

1.2 Notation

1.2.1 State diagram conventions

The operation of a protocol can be described by subdividing the protocol into a number of interrelated functions. The operation of the functions can be described by state diagrams. Each diagram represents the domain of a function and consists of a group of connected, mutually exclusive states. Only one state of a function is active at any given time (see Figure 1–2.)

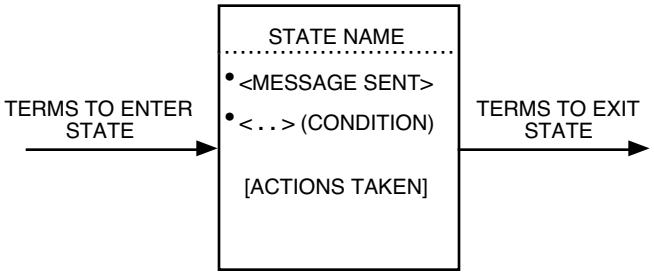
Each state that the function can assume is represented by a rectangle. These are divided into two parts by a horizontal line. In the upper part the state is identified by a name in capital letters. The lower part contains the name of any ON signal that is generated by the function. Actions are described by short phrases and enclosed in brackets.

All permissible transitions between the states of a function are represented graphically by arrows between them. A transition that is global in nature (for example, an exit condition from all states to the IDLE or RESET state) is indicated by an open arrow. Labels on transitions are qualifiers that must be fulfilled before

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Key: ( ) = condition, for example, (if no_collision)
[ ] = action, for example, [reset PLS functions]
* = logical AND
+ = logical OR
Tw = Wait Time, implementation dependent
Td = Delay Timeout
Tb = Backoff Timeout
UCT = unconditional transition

Figure 1–2—State diagram notation example

the transition will be taken. The label UCT designates an unconditional transition. Qualifiers described by short phrases are enclosed in parentheses.

State transitions and sending and receiving of messages occur instantaneously. When a state is entered and the condition to leave that state is not immediately fulfilled, the state executes continuously, sending the messages and executing the actions contained in the state in a continuous manner.

Some devices described in this standard (e.g., repeaters) are allowed to have two or more ports. State diagrams that are capable of describing the operation of devices with an unspecified number of ports, require qualifier notation that allows testing for conditions at multiple ports. The notation used is a term that includes a description in parentheses of which ports must meet the term for the qualifier to be satisfied (e.g., ANY and ALL). It is also necessary to provide for term-assignment statements that assign a name to a port that satisfies a qualifier. The following convention is used to describe a term-assignment statement that is associated with a transition:

a) The character ":" (colon) is a delimiter used to denote that a term assignment statement follows.
b) The character "⇐" (left arrow) denotes assignment of the value following the arrow to the term preceding the arrow.

The state diagrams contain the authoritative statement of the functions they depict; when apparent conflicts between descriptive text and state diagrams arise, the state diagrams are to take precedence. This does not override, however, any explicit description in the text that has no parallel in the state diagrams.

The models presented by state diagrams are intended as the primary specifications of the functions to be provided. It is important to distinguish, however, between a model and a real implementation. The models are optimized for simplicity and clarity of presentation, while any realistic implementation may place heavier emphasis on efficiency and suitability to a particular implementation technology. It is the functional behavior of any unit that must match the standard, not its internal structure. The internal details of the model are useful only to the extent that they specify the external behavior clearly and precisely.

1.2.2 Service specification method and notation

The service of a layer or sublayer is the set of capabilities that it offers to a user in the next higher (sub)layer. Abstract services are specified here by describing the service primitives and parameters that characterize each service. This definition of service is independent of any particular implementation (see Figure 1–3).

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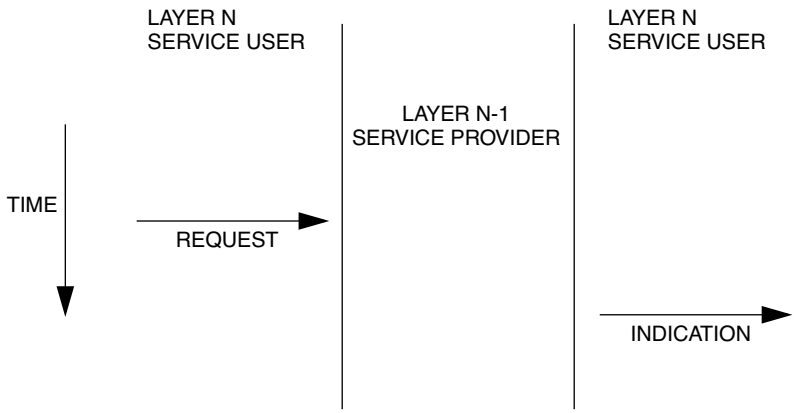


Figure 1–3—Service primitive notation

Specific implementations may also include provisions for interface interactions that have no direct end-to-end effects. Examples of such local interactions include interface flow control, status requests and indications, error notifications, and layer management. Specific implementation details are omitted from this service specification both because they will differ from implementation to implementation and because they do not impact the peer-to-peer protocols.

1.2.2.1 Classification of service primitives

Primitives are of two generic types:

a) REQUEST. The request primitive is passed from layer N to layer N-1 to request that a service be initiated.
b) INDICATION. The indication primitive is passed from layer N-1 to layer N to indicate an internal layer N-1 event that is significant to layer N. This event may be logically related to a remote service request, or may be caused by an event internal to layer N-1.

The service primitives are an abstraction of the functional specification and the user-layer interaction. The abstract definition does not contain local detail of the user/provider interaction. For instance, it does not indicate the local mechanism that allows a user to indicate that it is awaiting an incoming call. Each primitive has a set of zero or more parameters, representing data elements that shall be passed to qualify the functions invoked by the primitive. Parameters indicate information available in a user/provider interaction; in any particular interface, some parameters may be explicitly stated (even though not explicitly defined in the primitive) or implicitly associated with the service access point. Similarly, in any particular protocol specification, functions corresponding to a service primitive may be explicitly defined or implicitly available.

1.2.3 Physical Layer and media notation

Users of this standard need to reference which particular implementation is being used or identified. Therefore, a means of identifying each implementation is given by a simple, three-field, type notation that is explicitly stated at the beginning of each relevant clause. In general, the Physical Layer type is specified by these fields:

<data rate in Mb/s> <medium type> <maximum segment length (× 100 m)>

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For example, the standard contains a 10 Mb/s baseband specification identified as "TYPE 10BASE5," meaning a 10 Mb/s baseband medium whose maximum segment length is 500 m. Each successive Physical Layer specification will state its own unique TYPE identifier along similar lines.

1.2.4 Physical Layer message notation

Messages generated within the Physical Layer, either within or between PLS and the MAU (that is, PMA circuitry), are designated by an italic type to designate either form of physical or logical message used to execute the physical layer signaling process (for example, *input_idle* or *mau_available*).

1.3 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below. Members of IEC and ISO maintain registers of currently valid International Standards.

ANSI T1.601-1992, Telecommunications—Integrated Services Digital Network (ISDN)—Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification).[2]

ANSI T1.605-1991, Telecommunications—Integrated Services Digital Network (ISDN)—Basic Access Interface for S and T Reference Point (Layer 1 Specification).

ANSI X3.237-1995, Rev 2.1 (1 January 1995), FDDI Low-Cost Fibre Physical Layer—Medium Dependent (LCF-PMD) (ISO/IEC CD 9314-9).

ANSI X3.263-1995, Revision 2.2 (1 March 1995), FDDI Twisted Pair—Physical Medium Dependent (TP-PMD) (ISO/IEC CD 9314-10).

ANSI/TIA/EIA-568-A, Commercial Building Telecommunications Cabling Standard.

CISPR 22: 1993, Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment.[3]

IEC 60060 (all parts), High-voltage test techniques.[4]

IEC 60068, Basic environmental testing procedures.

IEC 60096-1: 1986, Radio-frequency cables, Part 1: General requirements and measuring methods and Amd. 2: 1993.

IEC 60169-8: 1978 and -16: 1982, Radio-frequency connectors, Part 8: R.F. coaxial connectors with inner diameter of outer conductor 6.5 mm (0.256 in) with bayonet lock—Characteristic impedance 50 ohms (Type

[2]ANSI publications are available from the Sales Department, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036, USA (www.ansi.org/).

[3]CISPR documents are available from the International Electrotechnical Commission, 3 rue de Varembé, Case Postale 131, CH 1211, Genève 20, Switzerland/Suisse (www.iec.ch/). CISPR documents are also available in the United States from the American National Standards Institute.

[4]In the 2002 edition of this standard, IEC publications have been renumbered in accordance with IEC's revised numbering system. In 1997, all existing publications were issued a designation in the 60000 series. Thus IEC 60 became IEC 60060, IEC 169-8 became IEC 60169-8, etc. IEC publications are available from IEC Sales Department, Case Postale 131, 3 rue de Varembé, CH-1211, Genève 20, Switzerland/Suisse (www.iec.ch/). IEC publications are also available in the United States from the American National Standards Institute.

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BNC); Part 16: R.F. coaxial connectors with inner diameter of outer conductor 7 mm (0.276 in) with screw coupling—Characteristic impedance 50 ohms (75 ohms) (Type N).

IEC 60603-7: 1990, Connectors for frequencies below 3 MHz for use with printed boards, Part 7: Detail specification for connectors, 8-way, including fixed and free connectors with common mating features, with assessed quality.

IEC 60793-1: 1995, Optical fibres—Part 1: Generic specification.

IEC 60793-2: 1992, Optical fibres—Part 2: Product specifications.

IEC 60794-1: 1996, Optical fibre cables—Part 1: Generic specification.

IEC 60794-2: 1989, Optical fibre cables—Part 2: Product specifications.

IEC 60807-2: 1992, Rectangular connectors for frequencies below 3 MHz, Part 2: Detail specification for a range of connectors with assessed quality, with trapezoidal shaped metal shells and round contacts—Fixed solder contact types.

IEC 60807-3: 1990, Rectangular connectors for frequencies below 3 MHz, Part 3: Detail specification for a range of connectors with trapezoidal shaped metal shells and round contacts—Removable crimp contact types with closed crimp barrels, rear insertion/rear extraction.

IEC 60825-1: 1993, Safety of laser products—Part 1: Equipment classification, requirements and user's guide.

IEC 60825-2: 1993, Safety of laser products—Part 2: Safety of optical fibre communication systems.

IEC 60874-1: 1993, Connectors for optical fibres and cables—Part 1: Generic specification.

IEC 60874-2: 1993, Connectors for optical fibres and cables—Part 2: Sectional specification for fibre optic connector, Type F-SMA.

IEC 60874-10: 1992, Connectors for optical fibres and cables—Part 10: Sectional specification, Fibre optic connector type BFOC/2,5.

IEC 60950: 1991, Safety of information technology equipment.

IEC 61000-4-3, Electromagnetic Compatibility (EMC)—Part 4: Testing and measurement techniques—Section 3: Radiated, radio-frequency, electromagnetic field immunity test.

IEC 61076-3-101: 1997, Connectors with assessed quality, for use in d.c., low-frequency analogue and in digital high-speed data applications—Part 3: Rectangular connectors—Section 101: Detail specification for a range of shielded connectors with trapezoidal shaped shells and non-removable rectangular contacts on a 1.27 mm × 2.54 mm centre-line.

IEC 61076-3-103 (48B/574/NP), Detail specification for rectangular connectors, with assessed quality, 6 and 8 way, fixed and free shielded connectors with ribbon contacts for high speed data applications.

IEC 61196-1: 1995, Radio-frequency cables—Part 1: Generic specification—General, definitions, requirements and test methods.

IEC 61754-4: 1997, Fibre optic connector interfaces—Part 4: Type SC connector family.

IEEE Std 802®-2001, IEEE Standards for Local and Metropolitan Area Networks: Overview and Architecture.[5]

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IEEE Std 802.1F™-1993 (Reaff 1998), IEEE Standards for Local and Metropolitan Area Networks: Common Definitions and Procedures for IEEE 802 Management Information.

IEEE P 802.1Q™/D11 (July 30, 1998), Draft Standard for Local and Metropolitan Area Networks: Virtual Bridged Local Area Networks.[6]

IETF RFC 1155, *Structure and Identification of Management Information for TCP/IP-based Internets,* Rose, M., and K. McCloghrie, May 1990.[7]

IETF RFC 1157, *A Simple Network Management Protocol (SNMP),* Case, J., Fedor, M., Schoffstall, M., and J. Davin, May 1990.

IETF RFC 1212, *Concise MIB Definitions,* Rose, M., and K. McCloghrie, March 1991.

IETF STD 17, RFC 1213, *Management Information Base for Network Management of TCP/IP-based internets: MIB-II,* McCloghrie K., and M. Rose, Editors, March 1991.

IETF RFC 1215, *A Convention for Defining Traps for use with the SNMP,* M. Rose, March 1991.

IETF RFC 1901, *Introduction to Community-based SNMPv2,* Case, J., McCloghrie, K., Rose, M., and S. Waldbusser, January 1996.

IETF RFC 1902, *Structure of Management Information for Version 2 of the Simple Network Management Protocol (SNMPv2),* Case, J., McCloghrie, K., Rose, M., and S. Waldbusser, January 1996.

IETF RFC 1903, *Textual Conventions for Version 2 of the Simple Network Management Protocol (SNMPv2),* Case, J., McCloghrie, K., Rose, M., and S. Waldbusser, January 1996.

IETF RFC 1904, *Conformance Statements for Version 2 of the Simple Network Management Protocol (SNMPv2),* Case, J., McCloghrie, K., Rose, M., and S. Waldbusser, January 1996.

IETF RFC 1905, *Protocol Operations for Version 2 of the Simple Network Management Protocol (SNMPv2),* Case, J., McCloghrie, K., Rose, M., and S. Waldbusser, January 1996.

IETF RFC 1906, *Transport Mappings for Version 2 of the Simple Network Management Protocol (SNMPv2),* Case, J., McCloghrie, K., Rose, M., and S. Waldbusser, January 1996.

IETF RFC 2233, *The Interfaces Group MIB using SMIv2,* McCloghrie, K., and F. Kastenholz, November 1997.

IETF RFC 2271, *An Architecture for Describing SNMP Management Frameworks,* Harrington, D., Presuhn, R., and B. Wijnen, January 1998.

IETF RFC 2272, *Message Processing and Dispatching for the Simple Network Management Protocol (SNMP),* Case, J., Harrington D., Presuhn R., and B. Wijnen, January 1998.

IETF RFC 2273, *SNMPv3 Applications,* Levi, D., Meyer, P., and B. Stewart, January 1998.

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[5]IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA (standards.ieee.org/).

[6]Numbers preceded by P are IEEE authorized standards projects that were not approved by the IEEE-SA Standards Board at the time this publication went to press. For information about obtaining drafts, contact the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA (http://standards.ieee.org/).

[7]IEFT RFCs are available from the Internet Engineering Task Force website at http://www.ietf.org/rfc.html.

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IETF RFC 2274, *User-based Security Model (USM) for version 3 of the Simple Network Management Protocol (SNMPv3),* Blumenthal, U., and B. Wijnen, January 1998.

IETF RFC 2275, *View-based Access Control Model (VACM) for the Simple Network Management Protocol (SNMP),* Wijnen, B., Presuhn, R., and K. McCloghrie, January 1998.

ISO/IEC 15802-1: 1995, Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Common specifications—Part 1: Medium Access Control (MAC) service definition.[8]

ISO/IEC 2382-9: 1995, Information technology—Vocabulary—Part 9: Data communication.

ISO/IEC 7498-1: 1994, Information technology—Open Systems Interconnection—Basic Reference Model: The Basic Model.

ISO/IEC 7498-4: 1989, Information processing systems—Open Systems Interconnection—Basic Reference Model—Part 4: Management Framework.

ISO/IEC 8824: 1990, Information technology—Open Systems Interconnection—Specification of Abstract Syntax Notation One (ASN.1).

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ISO/IEC 9314-1: 1989, Information processing systems—Fibre Distributed Data Interface (FDDI)—Part 1: Token Ring Physical Layer Protocol (PHY).

ISO/IEC 9314-2: 1989, Information processing systems—Fibre Distributed Data Interface (FDDI)—Part 2: Token Ring Media Access Control (MAC).

ISO/IEC 9314-3: 1990, Information processing systems—Fibre Distributed Data Interface (FDDI)—Part 3: Physical Layer Medium Dependent (PMD).

ISO/IEC 9646-1: 1994, Information technology—Open Systems Interconnection—Conformance testing methodology and framework—Part 1: General concepts.

ISO/IEC 9646-2: 1994, Information technology—Open Systems Interconnection—Conformance testing methodology and framework—Part 2: Abstract test suite specification.

ISO/IEC 10040: 1992, Information technology—Open Systems Interconnection—Systems management overview.

ISO/IEC 10164-1: 1993, Information technology—Open Systems Interconnection—Systems management—Part 1: Object Management Function.

ISO/IEC 10165-1: 1993, Information technology—Open Systems Interconnection—Management information services—Structure of management information—Part 1: Management Information Model.

ISO/IEC 10165-2: 1992, Information technology—Open Systems Interconnection—Structure of management information: Definition of management information.

[8]ISO/IEC publications are available from the ISO Central Secretariat, Case Postale 56, 1 rue de Varembé, CH-1211, Genève 20, Switzerland/Suisse (http://www.iso.ch/). ISO publications are also available in the United States from the Sales Department, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036, USA (http://www.ansi.org/).

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ISO/IEC 10165-4: 1992, Information technology—Open Systems Interconnection—Management information services—Structure of management information—Part 4: Guidelines for the definition of managed objects.

ISO/IEC 10742: 1994, Information technology—Telecommunications and information exchange between systems—Elements of management information related to OSI Data Link Layer standards.

ISO/IEC 11801: 1995, Information technology—Generic cabling for customer premises.

ISO/IEC 15802-2: 1995 [ANSI/IEEE Std 802.1B™-1992 and IEEE Std 802.1k™-1993], Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Common specifications—Part 2: LAN/MAN Management.

ISO/IEC 15802-3: 1998 [IEEE Std 802.1D™, 1998 Edition), Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Common specifications—Part 3: Media Access Control (MAC) bridges.

ITU-T Recommendation G.957 (1995) Digital line systems—Optical interfaces for equipments and systems relating to the synchronous digital hierarchy.[9]

ITU-T Recommendation I.430 (1995), Basic user-network interface—Layer 1 specification.

MATLAB Matrix Laboratory Software.[10]

NOTES

1—Local and national standards such as those supported by ANSI, EIA, IEEE, MIL, NPFA, and UL are not a formal part of this standard except where no international standard equivalent exists. A number of local and national standards are referenced as resource material; these bibliographical references are located in the bibliography in Annex A.

2—The IEEE standards referred to in 1.2 are trademarks of the Institute of Electrical and Electronics Engineers, Inc.

1.4 Definitions

The definitions used in this standard are consistent with ISO 2382-9: 1984.

EDITORIAL NOTE—A more specific Part 25 pertaining to LAN systems has been approved since the definitions in this standard were established. This standard is ISO/IEC 2382-25: 1992, Information technology—Vocabulary—Part 25: Local area networks.

1.4.1 10BASE2: IEEE 802.3 Physical Layer specification for a 10 Mb/s CSMA/CD local area network over RG 58 coaxial cable. (See IEEE 802.3 Clause 10)

1.4.2 10BASE5: IEEE 802.3 Physical Layer specification for a 10 Mb/s CSMA/CD local area network over coaxial cable (i.e., thicknet). (See IEEE 802.3 Clause 8.)

1.4.3 10BASE-F: IEEE 802.3 Physical Layer specification for a 10 Mb/s CSMA/CD local area network over fiber optic cable. (See IEEE 802.3 Clause 15.)

1.4.4 10BASE-FB port: A port on a repeater that contains an internal 10BASE-FB Medium Attachment Unit (MAU) that can connect to a similar port on another repeater. (See IEEE 802.3 Clause 9, Figure 15-1b and Figure 17.3.)

[9]ITU-T publications are available from the International Telecommunications Union, Place des Nations, CH-1211, Geneva 20, Switzerland (www.itu.int/).

[10]For information on MatLab contact: The MathWorks, 24 Park Way, Natick, MA, (www.mathworks.com).

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1.4.5 10BASE-FB segment: A fiber optic link segment providing a point-to-point connection between two 10BASE-FB ports on repeaters. (See link segment IEEE 802.3 Figure 15-1b and Figure 15–2.)

1.4.6 10BASE-FL segment: A fiber optic link segment providing point-to-point connection between two 10BASE-FL Medium Attachment Units (MAUs). (See link segment IEEE 802.3 Figure 15-1c and Figure 15–2.)

1.4.7 10BASE-FP segment: A fiber optic mixing segment, including one 10BASE-FP Star and all of the attached fiber pairs. (See IEEE 802.3 Figure 15–1a, Figure 1–3, and mixing segment.)

1.4.8 10BASE-FP Star: A passive device that is used to couple fiber pairs together to form a 10BASE-FP segment. Optical signals received at any input port of the 10BASE-FP Star are distributed to all of its output ports (including the output port of the optical interface from which it was received). A 10BASE-FP Star is typically comprised of a passive-star coupler, fiber optic connectors, and a suitable mechanical housing. (See IEEE 802.3, 16.5.)

1.4.9 10BASE-T: IEEE 802.3 Physical Layer specification for a 10 Mb/s CSMA/CD local area network over two pairs of twisted-pair telephone wire. (See IEEE 802.3 Clause 14.)

1.4.10 100BASE-FX: IEEE 802.3 Physical Layer specification for a 100 Mb/s CSMA/CD local area network over two optical fibers. (See IEEE 802.3 Clauses 24 and 26.)

1.4.11 100BASE-T: IEEE 802.3 Physical Layer specification for a 100 Mb/s CSMA/CD local area network. (See IEEE 802.3 Clauses 22 and 28.)

1.4.12 100BASE-T2: IEEE 802.3 specification for a 100 Mb/s CSMA/CD local area network over two pairs of Category 3 or better balanced cabling. (See IEEE 802.3 Clause 32.)

1.4.13 100BASE-T4: IEEE 802.3 Physical Layer specification for a 100 Mb/s CSMA/CD local area network over four pairs of Category 3, 4, and 5 unshielded twisted-pair (UTP) wire. (See IEEE 802.3 Clause 23.)

1.4.14 100BASE-TX: IEEE 802.3 Physical Layer specification for a 100 Mb/s CSMA/CD local area network over two pairs of Category 5 unshielded twisted-pair (UTP) or shielded twisted-pair (STP) wire. (See IEEE 802.3 Clauses 24 and 25.)

1.4.15 100BASE-X: IEEE 802.3 Physical Layer specification for a 100 Mb/s CSMA/CD local area network that uses the Physical Medium Dependent (PMD) sublayer and Medium Dependent Interface (MDI) of the ISO/IEC 9314 group of standards developed by ASC X3T12 (FDDI). (See IEEE 802.3 Clause 24.)

1.4.16 1000BASE-CX: 1000BASE-X over specialty shielded balanced copper jumper cable assemblies. (See IEEE 802.3 Clause 39.)

1.4.17 1000BASE-LX: 1000BASE-X using long wavelength laser devices over multimode and single-mode fiber. (See IEEE 802.3 Clause 38.)

1.4.18 1000BASE-SX: 1000BASE-X using short wavelength laser devices over multimode fiber. (See IEEE 802.3 Clause 38.)

1.4.19 1000BASE-T: IEEE 802.3 Physical Layer specification for a 1000 Mb/s CSMA/CD LAN using four pairs of Category 5 balanced copper cabling. (See IEEE 802.3 Clause 40.)

1.4.20 1000BASE-X: IEEE 802.3 Physical Layer specification for a 1000 Mb/s CSMA/CD LAN that uses a Physical Layer derived from ANSI X3.230-1994 (FC-PH) [B20][11]. (See IEEE 802.3 Clause 36.)

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1.4.21 10BROAD36: IEEE 802.3 Physical Layer specification for a 10 Mb/s CSMA/CD local area network over single broadband cable. (See IEEE 802.3 Clause 11.)

1.4.22 1BASE5: IEEE 802.3 Physical Layer specification for a 1 Mb/s CSMA/CD local area network over two pairs of twisted-pair telephone wire. (See IEEE 802.3 Clause 12.)

1.4.23 4D-PAM5: The symbol encoding method used in 1000BASE-T. The four-dimensional quinary symbols (4D) received from the 8B1Q4 data encoding are transmitted using five voltage levels (PAM5). Four symbols are transmitted in parallel each symbol period. (See IEEE 802.3 Clause 40.)

1.4.24 8B/10B transmission code: A dc-balanced octet-oriented data encoding specified in Table 36–1a–e and Table 36–2.

1.4.25 8B1Q4: For IEEE 802.3, the data encoding technique used by 1000BASE-T when converting GMII data (8B-8 bits) to four quinary symbols (Q4) that are transmitted during one clock (1Q4). (See IEEE 802.3 Clause 40.)

1.4.26 ability: A mode that a device can advertise using Auto-Negotiation. For modes that represent a type of data service, a device shall be able to operate that data service before it may advertise this ability. A device may support multiple abilities. (See IEEE 802.3, 28.2.1.2.2)

1.4.27 Acknowledge Bit: A bit used by IEEE 802.3 Auto-Negotiation to indicate that a station has successfully received multiple identical copies of the Link Code Word. This bit is only set after an identical Link Code Word has been received three times in succession. (See IEEE 802.3, 28.2.1.2.4.)

1.4.28 Actor: The local entity in a Link Aggregation Control Protocol exchange. (See IEEE 802.3 Clause 43.)

1.4.29 advertised ability: An operational mode that is advertised using Auto-Negotiation. (See IEEE 802.3, 28.2.1.2.2.)

1.4.30 agent: A term used to refer to the managed nodes in a network. Managed nodes are those nodes that contain a network management entity (NME), which can be used to configure the node and/or collect data describing operation of that node. The agent is controlled by a network control host or manager that contains both an NME and network management application (NMA) software to control the operations of agents. Agents include systems that support user applications as well as nodes that provide communications services such as front-end processors, bridges, and routers. (See IEEE 802.3 Clause 30.)

1.4.31 agent code: A term used to refer to network management entity software residing in a node that can be used to remotely configure the host system based on commands received from the network control host, collect information documenting the operation of the host, and communicate with the network control host. (See IEEE 802.3 Clause 30.)

1.4.32 Aggregation Key: A parameter associated with each port and with each aggregator of an Aggregation System identifying those ports that can be aggregated together. Ports in an Aggregation System that share the same Aggregation Key value are potentially able to aggregate together. (See IEEE 802.3 Clause 43.)

1.4.33 Aggregation Link: An instance of a MAC-Physical Layer-Medium Physical Layer-MAC entity between a pair of Aggregation Systems. (See IEEE 802.3 Clause 43.)

1.4.34 Aggregation Port: An instance of a MAC-Physical Layer entity within an Aggregation System. (See IEEE 802.3 Clause 43.)

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[11]The numbers in brackets preceded by the letter B correspond to those of the bibliography in Annex A.

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1.4.35 Aggregation System: A uniquely identifiable entity comprising (among other things) an arbitrary grouping of one or more ports for the purpose of aggregation. An instance of an aggregated link always occurs between exactly two Aggregation Systems. A physical device may comprise a single Aggregation System or more than one Aggregation System. (See IEEE 802.3 Clause 43.)

1.4.36 agile device: A device that supports automatic switching between multiple Physical Layer technologies. (See IEEE 802.3 Clause 28.)

1.4.37 arbitration: In 1000BASE-X, Auto-Negotiation process that ensures proper sequencing of configuration information between link partners using the Physical Coding Sublayer (PCS) Transmit and Receive functions. (See IEEE 802.3 Clauses 36 and 37.)

1.4.38 Attachment Unit Interface (AUI): In 10 Mb/s CSMA/CD, the interface between the Medium Attachment Unit (MAU) and the data terminal equipment (DTE) within a data station. Note that the AUI carries encoded signals and provides for duplex data transmission. (See IEEE 802.3 Clauses 7 and 8.)

1.4.39 Auto-Negotiation: The algorithm that allows two devices at either end of a link segment to negotiate common data service functions. (See IEEE 802.3 Clause 28.)

1.4.40 balanced cable: A cable consisting of one or more metallic symmetrical cable elements (twisted pairs or quads). (From ISO/IEC 11801.)

1.4.41 baseband coaxial system: A system whereby information is directly encoded and impressed upon the transmission medium. At any point on the medium only one information signal at a time can be present without disruption.

1.4.42 Base Link Code Word: The first 16-bit message exchanged during IEEE 802.3 Auto-Negotiation. (See IEEE 802.3, 28.2.1.2.)

1.4.43 Base Page: *See:* **Base Link Code Word**.

1.4.44 baud: A unit of signaling speed, expressed as the number of times per second the signal can change the electrical state of the transmission line or other medium. *Note*—Depending on the encoding strategies, a signal event may represent a single bit, more, or less that one bit. *Contrast with:* **bit rate**; **bits per second**. (From IEEE Std 610.7-1995 [B26].)

1.4.45 Binary Phase Shift Keying (Binary PSK or BPSK): A form of modulation in which binary data are transmitted by changing the carrier phase by 180 degrees. (See IEEE 802.3 Clause 11.)

1.4.46 bit cell: The time interval used for the transmission of a single data (CD0 or CD1) or control (CVH or CVL) symbol.

1.4.47 bit error ratio (BER): The ratio of the number of bits received in error to the total number of bits received.

1.4.48 bit rate (BR): The total number of bits per second transferred to or from the Media Access Control (MAC). For example, 100BASE-T has a bit rate of one hundred million bits per second (10^8 b/s).

1.4.49 bit rate (BR)/2: One-half of the BR in hertz.

1.4.50 bit time (BT): The duration of one bit as transferred to and from the Media Access Control (MAC). The bit time is the reciprocal of the bit rate. For example, for 100BASE-T the bit rate is 10^{-8} s or 10 ns.

1.4.51 BR/2: *See:* **bit rate (BR)/2.**

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1.4.52 branch cable: In 10BROAD36, the Attachment Unit Interface (AUI) cable interconnecting the data terminal equipment and Medium Attachment Unit (MAU) system components.

1.4.53 bridge: A layer 2 interconnection device that does not form part of a CSMA/CD collision domain but conforms to the ISO/IEC 15802-3: 1998 [ANSI/IEEE 802.1D™, 1998 Edition] International Standard. A bridge does not form part of a CSMA/CD collision domain but, rather appears as a Media Access Control (MAC) to the collision domain. (See also IEEE 100.)

1.4.54 broadband local area network (LAN): A local area network in which information is transmitted on modulated carriers, allowing coexistence of multiple simultaneous services on a single physical medium by frequency division multiplexing. (See IEEE 802.3 Clause 11.)

1.4.55 bundle: A group of signals that have a common set of characteristics and differ only in their information content.

1.4.56 carrier extension: The addition of nondata symbols to the end of frames that are less than slotTime bits in length so that the resulting transmission is at least one slotTime in duration.

1.4.57 carrier sense: In a local area network, an ongoing activity of a data station to detect whether another station is transmitting. *Note*—The carrier sense signal indicates that one or more DTEs are currently transmitting.

1.4.58 Category 3 balanced cabling: Balanced 100 Ω and 120 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 16 MHz (i.e., performance meets the requirements of a Class C link as per ISO/IEC 11801: 1995). Commonly used by IEEE 802.3 10BASE-T installations. In addition to the requirements outlined in ISO/IEC 11801: 1995, IEEE 802.3 Clauses 14, 23, and 32 specify additional requirements for cabling when used with 10BASE-T, 100BASE-TX, and 1000BASE-T.

1.4.59 Category 4 balanced cabling: Balanced 100 Ω and 120 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 20 MHz as per ISO/IEC 11801: 1995. In addition to the requirements outlined in ISO/IEC 11801: 1995, IEEE 802.3 Clauses 14, 23, and 32 specify additional requirements for this cabling when used with 10BASE-T, 100BASE-T4, and 100BASE-T2, respectively.

1.4.60 Category 5 balanced cabling: Balanced 100 Ω and 120 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 100 MHz (i.e., cabling components meet the performance specified in ISO/IEC 11801:1995). In addition to the requirements outlined in ISO/IEC 11801: 1995, IEEE 802.3 Clauses 14, 23, 25, and 40 specify additional requirements for this cabling when used with 10BASE-T and 100BASE-T.

1.4.61 CATV-type broadband medium: *See:* **Community Antenna Television (CATV)-type broadband medium.**

1.4.62 center wavelength: The average of two optical wavelengths at which the spectral radiant intensity is 50% of the maximum value. (See IEEE 802.3 Clause 11.)

1.4.63 channel: A band of frequencies dedicated to a certain service transmitted on the broadband medium. (See IEEE 802.3 Clause 11.)

1.4.64 channel insertion loss: As used in IEEE 802.3 Clause 38 for fiber optic links, the static loss of a link between a transmitter and receiver. It includes the loss of the fiber, connectors, and splices.

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1.4.65 circuit: The physical medium on which signals are carried across the Attachment Unit Interface (AUI) for 10BASE-T or Media Independent Interface (MII) for 100BASE-T. For 10BASE-T, the data and control circuits consist of an A circuit and a B circuit forming a balanced transmission system so that the signal carrier on the B circuit is the inverse of the signal carried on the A circuit.

1.4.66 Class I repeater: A type of 100BASE-T repeater set with internal delay such that only one repeater set may exist between any two DTEs within a single collision domain when two maximum length copper cable segments are used. (See IEEE 802.3 Clause 27.)

1.4.67 Class II repeater: A type of IEEE 802.3 100BASE-T repeater set with internal delay such that only two or fewer such repeater sets may exist between any two DTEs within a single collision domain when two maximum length copper cable segments are used. (See IEEE 802.3 Clause 27.)

1.4.68 Clocked Data One (CD1): A Manchester-encoded data 1. A CD1 is encoded as a LO for the first half of the bit-cell and a HI for the second half of the bit-cell. (See IEEE 802.3 Clause 12.)

1.4.69 Clocked Data Zero (CD0): A Manchester-encoded data 0. A CD0 is encoded as a HI for the first half of the bit-cell and a LO for the second half of the bit-cell. (See IEEE 802.3 Clause 12.)

1.4.70 Clocked Violation HI (CVH): A symbol that deliberately violates Manchester-encoding rules, used as a part of the Collision Presence signal. A CVH is encoded as a transition from LO to HI at the beginning of the bit cell, HI for the entire bit cell, and a transition from HI to LO at the end of the bit cell. (See IEEE 802.3 Clause 12.)

1.4.71 Clocked Violation LO (CVL): A symbol that deliberately violates Manchester-encoding rules, used as a part of the Collision Presence signal. A CVL is encoded as a transition from HI to LO at the beginning of the bit cell, LO for the entire bit cell, and a transition from LO to HI at the end of the bit cell. (See IEEE 802.3 Clause 12.)

1.4.72 coaxial cable: A two-conductor (center conductor, shield system), concentric, constant impedance transmission line used as the trunk medium in the baseband system.

1.4.73 coaxial cable interface: The electrical and mechanical interface to the shared coaxial cable medium either contained within or connected to the Medium Attachment Unit (MAU). Also known as the Medium Dependent Interface (MDI).

1.4.74 coaxial cable section: A single length of coaxial cable, terminated at each end with a male BNC connector. Cable sections are joined to other cable sections via BNC plug/receptacle barrel or Type T adapters.

1.4.75 coaxial cable segment: A length of coaxial cable made up from one or more coaxial cable sections and coaxial connectors, and terminated at each end in its characteristic impedance.

1.4.76 code-bit: Within IEEE 802.3, in 100BASE-T, the unit of data passed across the Physical Medium Attachment (PMA) service interface, and the smallest signaling element used for transmission on the medium. A group of five code-bits constitutes a code-group in the 100BASE-X Physical Coding Sublayer (PCS). (See IEEE 802.3, Clause 24.)

1.4.77 code-group: For IEEE 802.3, a set of encoded symbols representing encoded data or control information. For 100BASE-T4, a set of six ternary symbols that, when representing data, conveys an octet. For 100BASE-TX and 100BASE-FX, a set of five code-bits that, when representing data, conveys a nibble. For 100BASE-T2, a pair of PAM5×5 symbols that, when representing data, conveys a nibble. For 1000BASE-X, a set of ten bits that, when representing data, conveys an octet. For 1000BASE-T, a vector of four 8B1Q4 coded quinary symbols that, when representing data, conveys an octet. (See IEEE 802.3, Clauses 23, 24, 32, 36, and 40.)

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1.4.78 code-group alignment: In 1000BASE-X, the receiver action that resets the existing code-group boundary to that of the comma or K28.5 character currently being received. (See IEEE 802.3 Clause 36)

1.4.79 code-group slipping: In 1000BASE-X, the receiver action to align the correct receive clock and code-group containing a comma. (See IEEE 802.3 Clause 36)

1.4.80 Code Rule Violation (CRV): An analog waveform that is not the result of the valid Manchester-encoded output of a single optical transmitter. The collision of two or more 10BASE-FB optical transmissions will cause multiple CRVs. The preamble encoding of a single 10BASE-FP optical transmission contains a single CRV. (See IEEE 802.3, 16.3.1.1.)

1.4.81 collision: A condition that results from concurrent transmissions from multiple data terminal equipment (DTE) sources within a single collision domain.

1.4.82 collision domain: A single, half duplex mode CSMA/CD network. If two or more Media Access Control (MAC) sublayers are within the same collision domain and both transmit at the same time, a collision will occur. MAC sublayers separated by a repeater are in the same collision domain. MAC sublayers separated by a bridge are within different collision domains. (See IEEE 802.3.)

1.4.83 collision presence: A signal generated within the Physical Layer by an end station or hub to indicate that multiple stations are contending for access to the transmission medium. (See IEEE 802.3 Clauses 8 and 12.)

1.4.84 comma: In 1000BASE-X, the seven-bit sequence that is part of an 8B/10B code-group that is used for the purpose of code-group alignment. (See IEEE 802.3 Clause 36)

1.4.85 comma-: In 1000BASE-X, the seven-bit sequence (1100000) of an encoded data stream. (See IEEE 802.3 Clause 36)

1.4.86 comma+: In 1000BASE-X, the seven-bit sequence (0011111) of an encoded data stream. (See IEEE 802.3 Clause 36)

1.4.87 common-mode voltage: The instantaneous algebraic average of two signals applied to a balanced circuit, with both signals referenced to a common reference. Also called *longitudinal voltage* in the telephone industry.

1.4.88 Community Antenna Television (CATV)-type broadband medium: A broadband system comprising coaxial cables, taps, splitters, amplifiers, and connectors the same as those used in CATV or cable television installations. (See IEEE 802.3 Clause 11.)

1.4.89 compatibility interfaces: The Medium Dependent Interface (MDI) cable, the Attachment Unit Interface (AUI) branch cable, and the Media Independent Interface (MII); the three points at which hardware compatibility is defined to allow connection of independently designed and manufactured components to a baseband transmission medium. (See IEEE 802.3 Clause 8.)

1.4.90 continuous wave (CW): A carrier that is not modulated or switched.

1.4.91 Control mode: In 1000BASE-T, the period of operation in which the PHY is transmitting code-groups that represent control information. The end of a frame is accompanied by a transition to the Control mode, which immediately follows the Data mode and precedes the Idle mode. This occurs when the GMII signal TX_EN is set FALSE. During this time, several control fields are transmitted as code-groups to complete a stream. These include two convolutional encoder reset code-groups, two End-of-Stream delimiter (ESD) code-groups and, possibly, carrier extend code-groups. (See IEEE 802.3 Clause 40.)

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1.4.92 Control Signal One (CS1): An encoded control signal used on the Control In and Control Out circuits. A CS1 is encoded as a signal at half the bit rate (BR)/2). (See IEEE 802.3 Clause 12.)

1.4.93 Control Signal Zero (CS0): An encoded control signal used on the Control In and Control Out circuits. A CS0 is encoded as a signal at the bit rate (BR). (See IEEE 802.3 Clause 12.)

1.4.94 Conversation: A set of MAC frames transmitted from one end station to another, where all of the MAC frames form an ordered sequence, and where the communicating end stations require the ordering to be maintained among the set of MAC frames exchanged. (See IEEE 802.3 Clause 43.)

1.4.95 cross connect: A group of connection points, often wall- or rack-mounted in a wiring closet, used to mechanically terminate and interconnect twisted-pair building wiring.

1.4.96 data frame: Consists of the Destination Address, Source Address, Length Field, logical link control (LLC) Data, PAD, and Frame Check Sequence.

1.4.97 Data mode: In 1000BASE-T, the period of operation in which the PHY is transmitting code-groups that represent data. This mode is preceded by a start of a frame during which the GMII signal TX_EN is set TRUE for data transmission. This mode begins with transmission of two Start-of-Stream delimiter code-groups followed by code-groups encoded from the data octets arriving on TXD<7:0> via the GMII. (See IEEE 802.3 Clause 40.)

1.4.98 data terminal equipment (DTE): Any source or destination of data connected to the local area network.

1.4.99 dBmV: Decibels referenced to 1.0 mV measured at the same impedance. Used to define signal levels in Community Antenna Television (CATV)-type broadband systems. (See IEEE 802.3 Clause 11.)

1.4.100 dedicated service: A CSMA/CD network in which the collision domain consists of two and only two DTEs so that the total network bandwidth is dedicated to supporting the flow of information between them.

1.4.101 differential-mode voltage: The instantaneous algebraic difference between the potential of two signals applied to the two sides of a balanced circuit. Also called *metallic voltage* in the telephone industry.

1.4.102 differential skew: The difference in time between the midpoint voltage crossings of the true and complement components of a differential signal.

1.4.103 dispersion slope: The rate of change of the chromatic dispersion of a fiber with wavelength.

1.4.104 drop cable: In 10BROAD36, the small diameter flexible coaxial cable of the broadband medium that connects to a Medium Attachment Unit (MAU). (*See:* **trunk cable**.)

1.4.105 dual duplex: Within IEEE 802.3, a signaling system that supports simultaneous duplex communication over two cabling pairs.

1.4.106 duplex channel: Within IEEE 802.3, a communications channel capable of simultaneous duplex communication.

1.4.107 eight-pin modular: An eight-wire connector. (From IEC 60603-7.)

1.4.108 encapsulation: In 1000BASE-X, the process by which a MAC packet is enclosed within a PCS code-group stream. (See IEEE 802.3 Clause 36)

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1.4.109 End_of_Packet Delimiter (EPD): In 1000BASE-X, a defined sequence of three single code-group 8B/10B ordered_sets used to delineate the ending boundary of a data transmission sequence for a single packet. (See IEEE 802.3 Clause 36)

1.4.110 End-of-Stream Delimiter (ESD): Within IEEE 802.3, a code-group pattern used to terminate a normal data transmission. For 100BASE-T4, the ESD is indicated by the transmission of five predefined ternary code-groups named eop1-5. For 100BASE-X, the ESD is indicated by the transmission of the code-group/T/R. For 100BASE-T2, the ESD is indicated by two consecutive pairs of predefined PAM5×5 symbols (see Table 32–15) which are generated using unique Start-of-Stream Delimiter (SSD)/ESD coding rules. For 1000BASE-T, the ESD is indicated by two consecutive vectors of four quinary symbols as specified in Table 40–1. (See IEEE 802.3, Clauses 22, 23, 32, and 40.)

1.4.111 end station: A system attached to a LAN that is an initial source or a final destination of MAC frames transmitted across that LAN. A Network layer router is, from the perspective of the LAN, an end station; a MAC Bridge, in its role of forwarding MAC frames from one LAN to another, is not an end station. (See IEEE 802.3 Clause 43.)

1.4.112 Exception Window: A time interval during which the impedance of a mated connector and associated transmission line is allowed to exceed the impedance tolerance specification for signals passed through that connector.

1.4.113 extension bit: A bit decoded from the received carrier stream that does not map into the data space but nonetheless denotes the presence of carrier for the purposes of CSMA/CD.

1.4.114 Extinction Ratio: The ratio of the low optical power level to the high optical power level on an optical segment. (See IEEE 802.3 Clause 15.)

1.4.115 eye-opening penalty: The difference, in dB, between (a) the optical power measured at the center of the data eye, and (b) the optical power measured at a point defined by the total worst-case peak-to-peak jitter at the receiver.

1.4.116 Fast Link Pulse (FLP) Burst: A group of no more than 33 and not less than 17 10BASE-T compatible link integrity test pulses. Each FLP Burst encodes 16 bits of data using an alternating clock and data pulse sequence. (See Figure 14–14, IEEE 802.3 Clause 14 and Figure 28–4, IEEE 802.3 Clause 28)

1.4.117 Fast Link Pulse (FLP) Burst Sequence: The sequence of FLP Bursts transmitted by the local station. This term is intended to differentiate the spacing between FLP Bursts from the individual pulse spacings within an FLP Burst. (See IEEE 802.3 Clause 28)

1.4.118 fiber optic cable: A cable containing one or more optical fibers as specified in IEEE 802.3, 15.3.1.

1.4.119 Fiber Optic Inter-Repeater Link (FOIRL): A Fiber Optic Inter-Repeater Link segment and its two attached Medium Attachment Units (MAUs). (See IEEE 802.3 Clause 15)

1.4.120 Fiber Optic Inter-Repeater Link (FOIRL) bit error rate (BER): For 10BASE-F, the mean bit error rate of the FOIRL. (See IEEE 802.3 Clause 9)

1.4.121 Fiber Optic Inter-Repeater Link (FOIRL) collision: For 10BASE-F, the simultaneous transmission and reception of data in a Fiber Optic Medium Attachment Unit (FOMAU). (See IEEE 802.3 Clause 9)

1.4.122 Fiber Optic Inter-Repeater Link (FOIRL) Compatibility Interface: For 10BASE-F, the FOMDI and Attachment Unit Interface (AUI) (optional); the two points at which hardware compatibility is defined to allow connection of independently designed and manufactured components to the baseband optical fiber cable link segment. (See IEEE 802.3 Clause 9)

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1.4.123 Fiber Optic Inter-Repeater Link (FOIRL) Segment: A fiber optic link segment providing a point-to-point connection between two FOIRL Medium Attachment Units (MAUs) or between one FOIRL MAU and one 10BASE-FL MAU. *See:* **link segment**.

1.4.124 Fiber Optic Medium Attachment Unit (FOMAU): A MAU for fiber applications. (See IEEE 802.3 Clause 9)

1.4.125 Fiber Optic Medium Attachment Unit's (FOMAU's) Receive Optical Fiber: For 10BASE-F, the optical fiber from which the local FOMAU receives signals. (See IEEE 802.3 Clause 9)

1.4.126 Fiber Optic Medium Attachment Unit's (FOMAU's) Transmit Optical Fiber: For 10BASE-F, the optical fiber into which the local FOMAU transmits signals. (See IEEE 802.3 Clause 9)

1.4.127 Fiber Optic Medium Dependent Interface (FOMDI): For 10BASE-F, the mechanical and optical interface between the optical fiber cable link segment and the Fiber Optic Medium Attachment Unit (FOMAU). (See IEEE 802.3 Clause 9.)

1.4.128 Fiber Optic Physical Medium Attachment (FOPMA): For 10BASE-F, the portion of the Fiber Optic Medium Attachment Unit (FOMAU) that contains the functional circuitry. (See IEEE 802.3 Clause 9)

1.4.129 fiber pair: Optical fibers interconnected to provide two continuous light paths terminated at each end in an optical connector. Any intermediate optical connections must have insertion and return loss characteristics that meet or exceed IEEE 802.3, 15.3.2.1 and 15.3.2.2, respectively. (See IEEE 802.3, 15.3.1.)

1.4.130 Fibre Channel (FC-PH): Name used to refer to ANSI X3.230-1994 [B20]. (See IEEE 802.3 Clause 36)

1.4.131 Fibre Distributed Data Interface (FDDI): A 100 Mb/s, fiber optic-based, token-ring local area network standard (ISO/IEC 9314 series of standards).

1.4.132 FLP Burst: *See:* **Fast Link Pulse (FLP) Burst.**

1.4.133 FOIRL: *See:* **Fiber Optic Inter-Repeater Link (FOIRL).**

1.4.134 FOMAU: *See:* **Fiber Optic Medium Attachment Unit (FOMAU).**

1.4.135 full duplex: A mode of operation of a network, DTE, or Medium Attachment Unit (MAU) that supports duplex transmission as defined in IEEE 100. Within the scope of this standard, this mode of operation allows for simultaneous communication between a pair of stations, provided that the Physical Layer is capable of supporting simultaneous transmission and reception without interference. (See IEEE 802.3.)

1.4.136 Gigabit Media Independent Interface (GMII): The interface between the Reconciliation sublayer and the physical coding sublayer (PCS) for 1000 Mb/s operation. (See IEEE 802.3 Clause 35.)

1.4.137 group: A repeater port or a collection of repeater ports that can be related to the logical arrangement of ports within a repeater.

1.4.138 group delay: In 10BROAD36, the rate of change of total phase shift, with respect to frequency, through a component or system. Group delay variation is the maximum difference in delay as a function of frequency over a band of frequencies. (See IEEE 802.3 Clause 11.)

1.4.139 half duplex: A mode of operation of a CSMA/CD local area network (LAN) in which DTEs contend for access to a shared medium. Multiple, simultaneous transmissions in a half duplex mode CSMA/CD

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LAN result in interference, requiring resolution by the CSMA/CD access control protocol. (See IEEE 802.3.)

1.4.140 headend: In 10BROAD36, the location in a broadband system that serves as the root for the branching tree comprising the physical medium; the point to which all inbound signals converge and the point from which all outbound signals emanate. (See IEEE 802.3 Clause 11.)

1.4.141 header hub (HH): The highest-level hub in a hierarchy of hubs. The HH broadcasts signals transmitted to it by lower-level hubs or DTEs such that they can be received by all DTEs that may be connected to it either directly or through intermediate hubs. (See IEEE 802.3 12.2.1.)

1.4.142 hub: A device used to provide connectivity between DTEs. Hubs perform the basic functions of restoring signal amplitude and timing, collision detection, and notification and signal broadcast to lower-level hubs and DTEs. (See IEEE 802.3 Clause 12)

1.4.143 idle (IDL): A signal condition where no transition occurs on the transmission line, that is used to define the end of a frame and ceases to exist after the next LO or HI transition on the Attachment Unit Interface (AUI) or Media Independent Interface (MII) circuits. An IDL always begins with a HI signal level. A driver is required to send the IDL signal for at least 2 bit times and a receiver is required to detect IDL within 1.6 bit times. (See IEEE 802.3, 7.3 and 12.3.2.4.4 for additional details.)

1.4.144 Idle mode: In 1000BASE-T, the period of operation in which the PHY is transmitting special code-groups that use only the values {2, 0, –2}. Idle mode occurs during start-up when the PHYs at each end of a link are attempting to establish adaptive filter parameters and then synchronize both phase and timing so that normal operation can begin. Idle mode also occurs during normal operation between frames. Idle mode occurs after a control mode ends and before another Data mode begins. The Idle mode is not used between frames in a packet burst. (See IEEE 802.3 Clause 40.)

1.4.145 in-band signaling: The transmission of a signal using a frequency that is within the bandwidth of the information channel. *Contrast with:* **out-of-band signaling**. *Syn:* **in-channel signaling**. (From IEEE Std 610.7-1995 [B26].)

1.4.146 intermediate hub (IH): A hub that occupies any level below the header hub in a hierarchy of hubs. (See IEEE 802.3, 12.2.1 for details.)

1.4.147 Inter-Packet Gap (IPG): A delay or time gap between CSMA/CD packets intended to provide interframe recovery time for other CSMA/CD sublayers and for the Physical Medium. (See IEEE 802.3, 4.2.3.2.1 and 4.2.3.2.2.) For example, for 10BASE-T, the IPG is 9.6 μs (96 bit times); for 100BASE-T, the IPG is 0.96 μs (96 bit times).

1.4.148 Inter-Repeater Link (IRL): A mechanism for connecting two and only two repeater sets.

1.4.149 intersymbol interference penalty: The power penalty due to the finite bandwidth of the link. (See IEEE 802.3 Clause 38.)

1.4.150 jabber: A condition wherein a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition.

1.4.151 Jabber function: A mechanism for controlling abnormally long transmissions (i.e., jabber).

1.4.152 Jumper Cable Assembly: An electrical or optical assembly, used for the bidirectional transmission and reception of information, consisting of a pair of transmission lines terminated at their ends with plug connectors. This assembly may or may not contain additional components, located between the plug connectors, to perform equalization. (See IEEE 802.3 Clause 39.)

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1.4.153 link: The transmission path between any two interfaces of generic cabling. (From ISO/IEC 11801.)

1.4.154 Link Aggregation Group: A group of links that appear to a MAC Client as if they were a single link. All links in a Link Aggregation Group connect between the same pair of Aggregation Systems. One or more conversations may be associated with each link that is part of a Link Aggregation Group. (See IEEE 802.3 Clause 43.)

1.4.155 Link Code Word: The 16 bits of data encoded into a Fast Link Pulse (FLP) Burst. (See IEEE 802.3 Clause 28.)

1.4.156 link partner: The device at the opposite end of a link segment from the local station. The link partner device may be either a DTE or a repeater. (See IEEE 802.3 Clause 28.)

1.4.157 link penalties: For fiber optic links, the power penalties of a link not attributed to link attenuation. These power penalties include modal noise, relative intensity noise (RIN), intersymbol interference (ISI), mode partition noise, extinction ratio, and eye-opening penalties.

1.4.158 link pulse: Communication mechanism used in 10BASE-T and 100BASE-T networks to indicate link status and (in Auto-Negotiation-equipped devices) to communicate information about abilities and negotiate communication methods. 10BASE-T uses Normal Link Pulses (NLPs), which indicate link status only. 10BASE-T and 100BASE-T nodes equipped with Auto-Negotiation exchange information using a Fast Link Pulse (FLP) mechanism that is compatible with NLP. (See IEEE 802.3 Clauses 14 and 28.)

1.4.159 link segment: The point-to-point full-duplex medium connection between two and only two Medium Dependent Interfaces (MDIs).

1.4.160 Link Segment Delay Value (LSDV): A number associated with a given segment that represents the delay on that segment used to assess path delays for 100 Mb/s CSMA/CD networks. LSDV is similar to SDV; however, LSDV values do not include the delays associated with attached end stations and/or repeaters. (See IEEE 802.3, 29.3.)

1.4.161 local ability: *See:* **ability**.

1.4.162 local device: The local device that may attempt to perform Auto-Negotiation with a link partner. The local device may be either a DTE or repeater. (See IEEE 802.3 Clause 28.)

1.4.163 Management Information Base (MIB): A repository of information to describe the operation of a specific network device.

1.4.164 management interface: An interface provided by both the Media Independent Interface (MII) or Gigabit Media Independent Interface (GMII) that provides access to management parameters and services.

1.4.165 master Physical Layer (PHY): Within IEEE 802.3, in a 100BASE-T2 or 1000BASE-T link containing a pair of PHYs, the PHY that uses an external clock for generating its clock signals to determine the timing of transmitter and receiver operations. It also uses the master transmit scrambler generator polynomial for side-stream scrambling. Master and slave PHY status is determined during the Auto-Negotiation process that takes place prior to establishing the transmission link. *See also:* **slave Physical Layer (PHY) .**

1.4.166 maximum differential input: The largest value of peak-to-peak differential (ppd) amplitude at which a receiver is expected to operate, under worst-case conditions, without exceeding the objective bit error ratio.

1.4.167 Media Access Control (MAC): The data link sublayer that is responsible for transferring data to and from the Physical Layer.

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1.4.168 Media Independent Interface (MII): A transparent signal interface at the bottom of the Reconciliation sublayer. (See IEEE 802.3 Clause 22.)

1.4.169 Medium Attachment Unit (MAU): A device containing an Attachment Unit Interface (AUI), Physical Medium Attachment (PMA), and Medium Dependent Interface (MDI) that is used to connect a repeater or data terminal equipment (DTE) to a transmission medium.

1.4.170 Medium Dependent Interface (MDI): The mechanical and electrical interface between the transmission medium and the Medium Attachment Unit (MAU) (10BASE-T) or PHY (100BASE-T, 1000BASE-X, or 1000BASE-T).

1.4.171 Message Code (MC): The predefined 12-bit code contained in an Auto-Negotiation Message Page. (See IEEE 802.3 Clause 28.)

1.4.172 Message Page (MP): An Auto-Negotiation Next Page encoding that contains a predefined 12-bit Message Code. (See IEEE 802.3 Clause 28.)

1.4.173 minimum differential sensitivity: The smallest value of peak-to-peak differential (ppd) amplitude at which a receiver is expected to operate, under worst-case conditions, without exceeding the objective bit error ratio.

1.4.174 mixing segment: A medium that may be connected to more than two Medium Dependent Interfaces (MDIs).

1.4.175 multiport device: A device with multiple instances of MDI. (See IEEE 802.3 Clause 40.)

1.4.176 network control host: A network management central control center that is used to configure agents, communicate with agents, and display information collected from agents.

1.4.177 Next Page: General class of pages optionally transmitted by Auto-Negotiation able devices following the base Link Code Word negotiation. (See IEEE 802.3 Clause 28.)

1.4.178 Next Page Algorithm (NPA): The algorithm that governs Next Page communication. (See IEEE 802.3 Clause 28.)

1.4.179 Next Page Bit: A bit in the Auto-Negotiation base Link Code Word or Next Page encoding(s) that indicates that further Link Code Word transfer is required. (See IEEE 802.3 Clause 28.)

1.4.180 nibble: A group of four data bits. The unit of data exchange on the Media Independent Interface (MII). (See IEEE 802.3 Clause 22.)

1.4.181 NLP: *See:* **Normal Link Pulse (NLP).**

1.4.182 Non-Return-to-Zero, Invert on Ones (NRZI): An encoding technique used in FDDI (ISO/IEC 9314-1: 1989, ISO/IEC 9314-2: 1989, ISO/IEC 9314-3: 1989) where a polarity transition represents a logical ONE. The absence of a polarity transition denotes a logical ZERO.

1.4.183 Non-Return-to-Zero, Invert on Ones (NRZI)-bit: A code-bit transferred in NRZI format. The unit of data passed across the Physical Medium Dependent (PMD) service interface in 100BASE-X.

1.4.184 normalized amplitude: The amplitude of a signal when driving its steady-state value; i.e., not under the influence of ringing or other dynamic influences.

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1.4.185 Normal Link Pulse (NLP): An out-of-band communications mechanism used in 10BASE-T to indicate link status. (See IEEE 802.3 Figure 14–12.)

1.4.186 Normal Link Pulse (NLP) Receive Link Integrity Test function: A test function associated with Auto-Negotiation that allows backward compatibility with the 10BASE-T Link Integrity Test function of IEEE 802.3 Figure 14–6. (See IEEE 802.3 Clause 28)

1.4.187 Normal Link Pulse (NLP) sequence: A Normal Link Pulse sequence, defined in IEEE 802.3, 14.2.1.1 as TP_IDL.

1.4.188 NRZI: *See:* **Non-Return-to-Zero, Invert on Ones**.

1.4.189 offline: In 1000BASE-X, a DTE in its nonfunctional state. (See IEEE 802.3 Clause 37)

1.4.190 optical fiber: A filament-shaped optical waveguide made of dielectric materials.

1.4.191 Optical Fiber Cable Interface: *See:* **Fiber Optic Medium Dependent Interface (FOMDI)**.

1.4.192 Optical Fiber Cable Link Segment: A length of optical fiber cable that contains two optical fibers and is comprised of one or more optical fiber cable sections and their means of interconnection, with each optical fiber terminated at each end in the optical connector plug. (See IEEE 802.3, 9.9.5.1 and 9.9.5.1.)

1.4.193 Optical Idle Signal: The signal transmitted by the Fiber Optic Medium Attachment Unit (FOMAU) into its transmit optical fiber during the idle state of the DO circuit. (See IEEE 802.3 Clause 9)

1.4.194 Optical Interface: The optical input and output connection interface to a 10BASE-FP Star. (See IEEE 802.3 Clause 15.)

1.4.195 ordered_set: As used in the 1000BASE-X PCS, a single special code-group, or a combination of special and data code-groups, used for the delineation of a packet and synchronization between the transmitter and receiver circuits at opposite ends of a link. (See IEEE 802.3 Clause 36.)

1.4.196 out-of-band signaling: The transmission of a signal using a frequency that is within the pass band of the transmission facility but outside a frequency range normally used for data transmission. *Contrast with:* **in-band signaling**. (From IEEE Std. 610.7-1995 [B26].)

1.4.197 overfilled launch: The overfilled launch condition that excites both radial and azimuthal modes defined in ANSI/EIA/TIA 455-54A-1990 [B5].

1.4.198 packet: Consists of a data frame as defined previously, preceded by the Preamble and the Start Frame Delimiter, encoded, as appropriate, for the Physical Layer (PHY) type.

1.4.199 page: In Auto-Negotiation, the encoding for a Link Code Word. Auto-Negotiation can support an arbitrary number of Link Code Word encodings. The base page has a constant encoding as defined in 28.2.1.2. Additional pages may have a predefined encoding *(see:* **Message Page**) or may be custom encoded *(see:* **Unformatted Page**).

1.4.200 PAM5×5: Within IEEE 802.3, a block coding technique utilizing a 5×5 matrix (representing two 5-level signals) to generate pairs of quinary codes representing data nibbles and control characters. In 100BASE-T2, PAM5×5 code pairs are sent in parallel across two wire pairs. (See IEEE 802.3, Clause 32.)

1.4.201 parallel detection: In Auto-Negotiation, the ability to detect 100BASE-TX and 100BASE-T4 technology specific link signaling while also detecting the Normal Link Pulse (NLP) sequence or Fast Link Pulse (FLP) Burst sequence. (See IEEE 802.3 Clause 28.)

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1.4.202 Partner: The remote entity in a Link Aggregation Control Protocol exchange. (See IEEE 802.3 Clause 43.)

1.4.203 Passive-Star Coupler: A component of a 10BASE-FP fiber optic mixing segment that divides optical power received at any of N input ports among all N output ports. The division of optical power is approximately uniform. (See IEEE 802.3 Clause 15.)

1.4.204 patch cord: Flexible cable unit or element with connectors(s) used to establish connections on a patch panel. (From ISO/IEC 11801: 1995.)

1.4.205 patch panel: A cross-connect designed to accommodate the use of patch cords. It facilitates administration for moves and changes. (From ISO/IEC 11801: 1995.)

1.4.206 path: The sequence of segments and repeaters providing the connectivity between two DTEs in a single collision domain. In CSMA/CD networks there is one and only one path between any two DTEs.

1.4.207 Path Delay Value (PDV): The sum of all Segment Delay Values for all segments along a given path. (See IEEE 802.3 Clauses 13 and 29.)

1.4.208 Path Variability Value (PVV): The sum of all Segment Variability Values for all the segments along a given path. (See IEEE 802.3 Clause 13.)

1.4.209 pause: A mechanism for full duplex flow control. (See IEEE 802.3 Annex 31B.)

1.4.210 Physical Coding Sublayer (PCS): Within IEEE 802.3, a sublayer used in 100BASE-T, 1000BASE-X, and 1000BASE-T to couple the Media Independent Interface (MII) or Gigabit Media Independent Interface (GMII) and the Physical Medium Attachment (PMA). The PCS contains the functions to encode data bits into code-groups that can be transmitted over the physical medium. Three PCS structures are defined for 100BASE-T—one for 100BASE-X, one for 100BASE-T4, and one for 100BASE-T2.(See IEEE 802.3, Clauses 23, 24, and 32.) One PCS structure is defined for 1000BASE-X and one PCS structure is defined for 1000BASE-T. (See IEEE 802.3 Clauses 36 and 40.)

1.4.211 Physical Layer entity (PHY): Within IEEE 802.3, the portion of the Physical Layer between the Medium Dependent Interface (MDI) and the Media Independent Interface (MII), or between the MDI and GMII, consisting of the Physical Coding Sublayer (PCS), the Physical Medium Attachment (PMA), and, if present, the Physical Medium Dependent (PMD) sublayers. The PHY contains the functions that transmit, receive, and manage the encoded signals that are impressed on and recovered from the physical medium. (See IEEE 802.3 Clauses 23–26, 32, 36, and 40.)

1.4.212 Physical Medium Attachment (PMA) sublayer: Within 802.3, that portion of the Physical Layer that contains the functions for transmission, reception, and (depending on the PHY) collision detection, clock recovery and skew alignment. (See IEEE 802.3, Clauses 7, 12, 14, 16, 17, 18, 23, 24, 32, 36, and 40.)

1.4.213 Physical Medium Dependent (PMD) sublayer: In 100BASE-X, that portion of the Physical Layer responsible for interfacing to the transmission medium. The PMD is located just above the Medium Dependent Interface (MDI). (See IEEE 802.3 Clause 24.)

1.4.214 Physical Signaling Sublayer (PLS): In 10BASE-T, that portion of the Physical Layer contained within the data terminal equipment (DTE) that provides the logical and functional coupling between the Medium Attachment Unit (MAU) and the Data Link Layer.

1.4.215 port: A segment or Inter-Repeater Link (IRL) interface of a repeater unit.

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1.4.216 postamble: In 10BROAD36, the bit pattern appended after the last bit of the Frame Check Sequence by the Medium Attachment Unit (MAU). The Broadband End-of-Frame Delimiter (BEOFD). (See IEEE 802.3 Clause 11.)

1.4.217 power budget: The minimum optical power available to overcome the sum of attenuation plus power penalties of the optical path between the transmitter and receiver calculated as the difference between the transmitter launch power (min) and the receive power (min).

1.4.218 prepend: To append to the beginning. For example, a Media Access Control (MAC) frame is prepended with a preamble, and appended with a frame check sequence (FCS).

1.4.219 priority resolution: A mechanism that allows a local device and its link partner to resolve to a single mode of operation given a set of prioritized rules governing resolution. (See IEEE 802.3 Clause 28 and Clause 37.)

1.4.220 Priority Resolution Table: The look-up table used by Auto-Negotiation to select the network connection type where more than one common network ability exists (100BASE-TX, 100BASE-T4, 10BASE-T, etc.) The priority resolution table defines the relative hierarchy of connection types from the highest common denominator to the lowest common denominator. (See IEEE 802.3 Clause 28.)

1.4.221 Q: In the context of a fiber optic communication system, one-half of the ratio of peak-to-peak signal to rms noise.

1.4.222 QTag Prefix: The first four octets of an Ethernet-encoded Tag Header. The Ethernet-encoded Tag Header is defined in IEEE P802.1Q.

1.4.223 quad: *See:* **star quad**.

1.4.224 quinary: Five-level.

1.4.225 quinary symbol: In 1000BASE-T, one of five numeric values corresponding to five voltage levels on a single balanced twisted pair. The values come from the set {2, 1, 0, –1, –2}. Table 40–1 lists groups of four quinary symbols. Idle is a special case where numeric values are limited to the set {2, 0, and –2}. (See IEEE 802.3 Clause 40.)

1.4.226 radial overfilled launch: A launch condition created when a multimode optical fiber is illuminated by the coherent optical output of a source operating in its lowest-order transverse mode in a manner that excites predominantly the radial modes of the multimode fiber.

1.4.227 receiver training: Within IEEE 802.3, a start-up routine in 100BASE-T2 and 1000BASE-T used to acquire receiver parameters and synchronize the scramblers of two connected Physical Layers (PHYs).

1.4.228 Reconciliation Sublayer (RS): A 100BASE-T mapping function that reconciles the signals at the Media Independent Interface (MII) to the Media Access Control (MAC)-Physical Signaling Sublayer (PLS) service definitions. (See IEEE 802.3 Clause 22.)

1.4.229 relative intensity noise: The ratio of the variance in the optical power to the average optical power.

1.4.230 remote fault: The generic ability of a link partner to signal its status even in the event that it may not have an operational receive link. (See IEEE 802.3 Clause 28 and Clause 37.)

1.4.231 renegotiation: Restart of the Auto-Negotiation algorithm caused by management or user interaction. (See IEEE 802.3 Clause 28.)

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1.4.232 repeater: Within IEEE 802.3, a device as specified in Clauses 9 and 27 that is used to extend the length, topology, or interconnectivity of the physical medium beyond that imposed by a single segment, up to the maximum allowable end-to-end transmission line length. Repeaters perform the basic actions of restoring signal amplitude, waveform, and timing applied to the normal data and collision signals. For wired star topologies, repeaters provide a data distribution function. In 100BASE-T, a device that allows the interconnection of 100BASE-T Physical Layer (PHY) network segments using similar or dissimilar PHY implementations (e.g., 100BASE-X to 100BASE-X, 100BASE-X to 100BASE-T4, etc.). Repeaters are only for use in half duplex mode networks. (See IEEE 802.3, Clauses 9 and 27.)

1.4.233 repeater port: *See:* **port**.

1.4.234 repeater set: A repeater unit plus its associated Physical Layer interfaces [Medium Attachment Units (MAUs) or PHYs] and, if present, Attachment Unit (AU) or Media Independent (MI) interfaces (i.e., AUIs, MIIs).

1.4.235 repeater unit: The portion of a repeater that is inboard of its Physical Medium Attachment (PMA)/Physical Signaling Sublayer (PLS), or PMA/Physical Coding Sublayer (PCS) interfaces.

1.4.236 retraining: Within IEEE 802.3, the process of re-acquiring receiver parameters and synchronizing the scramblers of two connected 100BASE-T2 PHYs or 1000BASE-T. *See:* **receiver training, blind mode.**

1.4.237 Return Loss: In 10BROAD36, the ratio in decibels of the power reflected from a port to the power incident to the port. An indicator of impedance matching in a broadband system. (See IEEE 802.3 Clause 11.)

1.4.238 rms Spectral Width: The optical wavelength range as measured by ANSI/EIA/TIA 455-127-1991 (FOTP-127) [B8].

1.4.239 router: A layer 3 interconnection device that appears as a Media Access Control (MAC) to a CSMA/CD collision domain. (See IEEE Std 610.7-1995 [B26].)

1.4.240 run length: The number of consecutive identical bits in a code-group. For example, the pattern 0011111010 has a run length of five. (See IEEE 802.3 Clause 36.)

1.4.241 run-length-limited code: Any transmission code that has limited run-length for its transmission. (See IEEE 802.3 Clause 36.)

1.4.242 running disparity: A binary parameter having a value of + or –, representing the imbalance between the number of ones and zeros in a sequence of 8B/10B code-groups. (See IEEE 802.3 Clause 36.2.4.3.)

1.4.243 Seed: In 10BROAD36, the 23 bits residing in the scrambler shift register prior to the transmission of a packet. (See IEEE 802.3 Clause 11.)

1.4.244 segment: The medium connection, including connectors, between Medium Dependent Interfaces (MDIs) in a CSMA/CD local area network.

1.4.245 Segment Delay Value (SDV): A number associated with a given segment that represents the delay on that segment including repeaters and end stations, if present, used to assess path delays for 10 Mb/s CSMA/CD networks. (See IEEE 802.3, 13.4.)

1.4.246 Segment Variability Value (SVV): A number associated with a given segment that represents the delay variability on that segment (including a repeater) for 10 Mb/s CSMA/CD networks. The SVVs for different segment types are specified in IEEE 802.3 Table 13–3. (See IEEE 802.3, 13.4.)

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1.4.247 Selector field: A five-bit field in the Base Link Code Word encoding that is used to encode up to 32 types of messages that define basic abilities. For example, selector field 00001 indicates that the base technology is IEEE 802.3. (See IEEE 802.3 Clause 28.)

1.4.248 shared service: A CSMA/CD network in which the collision domain consists of more than two DTEs so that the total network bandwidth is shared among them.

1.4.249 shielded twisted-pair (STP) cable: An electrically conducting cable, comprising one or more elements, each of which is individually shielded. There may be an overall shield, in which case the cable is referred to as shielded twisted-pair cable with an overall shield (from ISO/IEC 11801: 1995). Specifically for IEEE 802.3 100BASE-TX, 150 Ω balanced inside cable with performance characteristics specified to 100 MHz (i.e., performance to Class D link standards as per ISO/IEC 11801: 1995). In addition to the requirements specified in ISO/IEC 11801: 1995, IEEE 802.3 Clauses 23 and 25 provide additional performance requirements for 100BASE-T operation over STP.

1.4.250 side stream scrambling: A data scrambling technique, used by 100BASE-T2 and 1000BASE-T to randomize the sequence of transmitted symbols and avoid the presence of spectral lines in the signal spectrum. Synchronization of the scrambler and descrambler of connected PHYs is required prior to operation.

1.4.251 Simplex Fiber Optic Link Segment: A single fiber path between two Medium Attachment Units (MAUs) or PHYs, including the terminating connectors, consisting of one or more fibers joined serially with appropriate connection devices, for example, patch cables and wall plates. (See IEEE 802.3 Clause 15.)

1.4.252 simplex link segment: A path between two Medium Dependent Interfaces (MDIs), including the terminating connectors, consisting of one or more segments of twisted pair cable joined serially with appropriate connection devices, for example, patch cords and wall plates. (See IEEE 802.3 Figure 14–2.)

1.4.253 single-port device: A device with a single instance of MDI. (See IEEE 802.3 Clause 40.)

1.4.254 skew between pairs: The difference in arrival times of two initially coincident signals propagated over two different pairs, as measured at the receiving end of the cable. Total skew includes contributions from transmitter circuits as well as the cable.

1.4.255 slave Physical Layer (PHY): Within IEEE 802.3, in a 100BASE-T2 or 1000BASE-T link containing a pair of PHYs, the PHY that recovers its clock from the received signal and uses it to determine the timing of transmitter operations. It also uses the slave transmit scrambler generator polynomial for side-stream scrambling. Master and slave PHY status is determined during the Auto-Negotiation process that takes place prior to establishing the transmission link. *See also:* **master Physical Layer (PHY).**

1.4.256 sliver: A pulse with a duration less than that specified for that signal (e.g., truncated clock signal).

1.4.257 special link (SL): A transmission system that replaces the normal medium. (See IEEE 802.3, 12.8.)

1.4.258 Spectral Width, Full-Width Half Maximum (FWHM): The absolute difference between the wavelengths at which the spectral radiant intensity is 50% of the maximum. (See IEEE 802.3 Clause 15.)

1.4.259 spectrum mask: A graphic representation of the required power distribution as a function of frequency for a modulated transmission.

1.4.260 star quad: A cable element that comprises four insulated connectors twisted together. Two diametrically facing conductors form a transmission pair. *Note*—Cables containing star quads can be used interchangeably with cables consisting of pairs, provided the electrical characteristics meet the same specifications. (From ISO/IEC 11801.)

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1.4.261 Start_of_Packet Delimiter (SPD): In 1000BASE-X, a single code-group 8B/10B ordered_set used to delineate the starting boundary of a data transmission sequence for a single packet. (See IEEE 802.3 Clause 36.)

1.4.262 Start-of-Stream Delimiter (SSD): Within IEEE 802.3, a pattern of defined code words used to delineate the boundary of a data transmission sequence on the Physical Layer stream. The SSD is unique in that it may be recognized independent of previously defined code-group boundaries and it defines subsequent code-group boundaries for the stream it delimits. For 100BASE-T4, SSD is a pattern of three predefined sosb code-groups (one per wire pair) indicating the positions of the first data code-group on each wire pair. For 100BASE-X, SSD consists of the code-group sequence /J/K/. For 100BASE-T2, the SSD is indicated by two consecutive pairs of predefined PAM5×5 symbols (±2, ±2) (±2, 0) which are generated using unique SSD/ESD coding rules. For 1000BASE-T, the SSD is indicated by two consecutive vectors of four quinary symbols as specified in Table 40–1.

1.4.263 stream: The Physical Layer (PHY) encapsulation of a Media Access Control (MAC) frame. Depending on the particular PHY, the MAC frame may be modified or have information appended or prepended to it to facilitate transfer through the Physical Medium Attachment (PMA). Any conversion from a MAC frame to a PHY stream and back to a MAC frame is transparent to the MAC. (See IEEE 802.3 Clauses 23 and 24.)

1.4.264 switch: A layer 2 interconnection device that conforms to the ISO/IEC 10038 [ANSI/IEEE 802.1D-1998] International Standard. *Syn:* **bridge.**

1.4.265 symbol: Within IEEE 802.3, the smallest unit of data transmission on the medium. Symbols are unique to the coding system employed. 100BASE-T4 uses ternary symbols; 10BASE-T uses Manchester symbols; 100BASE-X uses binary symbols or code bits; 100BASE-T2 and 1000BASE-T uses quinary symbols.

1.4.266 symbol period: In 1000BASE-T, the time interval for transmission of one code-group. This is equivalent to eight nanoseconds. (See IEEE 802.3 Clause 40.)

1.4.267 symbol rate (SR): Within IEEE 802.3, the total number of symbols per second transferred to or from the Medium Dependent Interface (MDI) on a single wire pair. For 100BASE-T4, the symbol rate is 25 MBd; for 100BASE-X, the symbol rate is 125 MBd; for 100BASE-T2, the symbol rate is 25 MBaud; for 1000BASE-T, the symbol rate is 125 MBaud.

1.4.268 symbol time (ST): The duration of one symbol as transferred to and from the Medium Dependent Interface (MDI) via a single wire pair. The symbol time is the reciprocal of the symbol rate.

1.4.269 tagged MAC frame: A frame that contains a QTag Prefix.

1.4.270 Technology Ability Field: Within IEEE 802.3, an eight-bit field in the Auto-Negotiation base page that is used to indicate the abilities of a local station, such as support for 10BASE-T, 100BASE-T4, and 100BASE-TX, as well as full duplex.

1.4.271 ternary symbol: In 100BASE-T4, a ternary data element. A ternary symbol can have one of three values: –1, 0, or +1. (See IEEE 802.3 Clause 23.)

1.4.272 transition density: The number of times the stream of bits within an 8B/10B code-group changes its value. (See IEEE 802.3 Clause 36.)

1.4.273 translation: In a single-cable 10BROAD36 system, the process by which incoming transmissions at one frequency are converted into another frequency for outgoing transmission. The translation takes place at the headend. (See IEEE 802.3 Clause 11.)

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1.4.274 truncation loss: In a modulated data waveform, the power difference before and after implementation filtering necessary to constrain its spectrum to a specified frequency band.

1.4.275 trunk cable: The main (often large diameter) cable of a coaxial cable system. (*See:* **drop cable**.)

1.4.276 twisted pair: A cable element that consists of two insulated conductors twisted together in a regular fashion to form a balanced transmission line. (From ISO/IEC 11801: 1995.)

1.4.277 twisted-pair cable: A bundle of multiple twisted pairs within a single protective sheath. (From ISO/IEC 11801: 1995.)

1.4.278 twisted-pair cable binder group: A group of twisted pairs within a cable that are bound together. Large telephone cables have multiple binder groups with high interbinder group near-end crosstalk loss.

1.4.279 twisted-pair link: A twisted-pair cable plus connecting hardware. (From ISO/IEC 11801: 1995.) (See also IEEE 802.3 14.1.2.)

1.4.280 twisted-pair link segment: In 100BASE-T, a twisted-pair link for connecting two Physical Layers (PHYs). (See also IEEE 802.3 14.1.2.)

1.4.281 Unformatted Page (UP): A Next Page encoding that contains an unformatted 12-bit message field. Use of this field is defined through Message Codes and information contained in the UP. (See IEEE 802.3, 28.2.1.2.)

1.4.282 unshielded twisted-pair cable (UTP): An electrically conducting cable, comprising one or more pairs, none of which is shielded. There may be an overall shield, in which case the cable is referred to as unshielded twisted-pair with overall shield. (From ISO/IEC 11801: 1995.)

1.4.283 weight of 6T code group: The algebraic sum of the logical ternary symbol values listed in the 100BASE-T4 8B6T code table. (See IEEE 802.3 Clause 23.)

1.4.284 worst-case modal bandwidth (WCMB): The lowest value of the modal bandwidth found when measured using either an overfilled launch (OFL) or a radial overfilled launch (ROFL).

1.4.285 zero dispersion wavelength: That wavelength where the chromatic dispersion of a fiber is at its minimum.

1.5 Abbreviations

This standard contains the following abbreviations:

8802-3	ISO/IEC 8802-3 (IEEE Std 802.3)
8802-5	ISO/IEC 8802-5 (IEEE Std 802.5)
ANSI	American National Standards Institute
ASIC	application-specific integrated circuit
ASN.1	abstract syntax notation one as defined in ISO/IEC 8824: 1990
AUI	attachment unit interface
BER	bit error ratio
BPSK	binary phase shift keying
BR	bit rate
BT	bit time
CAT3	Category 3 balanced cable
CAT4	Category 4 balanced cable

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CAT5	Category 5 balanced cable
CD0	clocked data zero
CD1	clocked data one
CMIP	common management information protocol as defined in ISO/IEC 9596-1: 1991
CMIS	common management information service as defined in ISO/IEC 9595: 1991
CMOS	complimentary metal oxide semiconductor
CRC	cyclic redundancy check
CRV	code rule violation
CS0	control signal zero
CS1	control signal one
CVH	clocked violation high
CVL	clocked violation low
CW	continuous wave
DFE	distributed feedback equilizer
DTE	data terminal equipment
EIA	Electronic Industries Association
ELFEXT	equal-level far-end crosstalk
EMI	Electromagnetic Interference
EPD	End_of_Packet delimiter
ESD	end of stream delimiter
FC-PH	Fibre Channel—Physical and Signaling Interface
FCS	frame check sequence
FDDI	fibre distributed data interface
FEXT	far-end crosstalk
FIFO	first in, first out
FLP	fast link pulse
FOIRL	fiber optic inter-repeater link
FOMAU	fiber optic medium attachment unit
FOMDI	fiber optic medium dependent interface
FOPMA	fiber optic physical medium attachment
FOTP	fiber optic test procedure
GMII	Gigabit Media Independent Interface
HH	header hub
IEC	International Electrotechnical Commission
IH	intermediate hub
IPG	inter-packet gap
IRL	inter-repeater link
ISI penalty	intersymbol interference penalty
ISO	International Organization for Standardization
LACP	Link Aggregation Control Protocol
LACPDU	Link Aggregation Control Protocol Data Unit
LAG	Link Aggregation Group
LAG ID	Link Aggregation Group Identifier
LAN	local area network
LLC	logical link control
LSDV	link segment delay value
MAC	medium access control
MAU	medium attachment unit
MC	message code
MDELFEXT	multiple-disturber equal-level far-end crosstalk
MDFEXT	multiple-disturber far-end crosstalk
MDI	medium dependent interface
MDNEXT	multiple-disturber near-end crosstalk
MIB	management information base

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MII	media independent interface
MMF	multimode fiber
MP	message page
Mux	Multiplexer
NEXT	near-end crosstalk
NLP	normal link pulse
NPA	next page algorithm
NRZI	non return to zero and invert on ones
NTT	Need To Transmit
OFL	overfilled launch
OFSTP	optical fiber system test procedure
PCS	physical coding sublayer
PDU	Protocol Data Unit
PDV	path delay value
PHY	Physical Layer entity sublayer
PICS	protocol implementation conformance statement
PLS	physical signaling sublayer
PMA	physical medium attachment
PMD	physical medium dependent
PMI	physical medium independent
ppd	peak-to-peak differential
PVV	path variability value
RD	running disparity
RFI	radio frequency interference
RIN	relative intensity noise
ROFL	radial overfilled launch
RS	reconciliation sublayer
SDV	segment delay value
SFD	start-of-frame delimiter
SMF	single-mode fiber
SPD	Start_of_Packet delimiter
SR	symbol rate
SSD	start-of-stream delimiter
ST	symbol time
STA	station management entity
STP	shielded twisted pair (copper)
SVV	segment variability value
TBI	Ten Bit Interface
TDR	time domain reflectometer
TIA	Telecommunications Industry Association
TLV	Type/Length/Value
UCT	unconditional transition
UP	unformatted page
UTP	unshielded twisted pair
VLAN	Virtual Bridged Local Area Network (see IEEE P802.1Q)
WCMB	worst-case modal bandwidth

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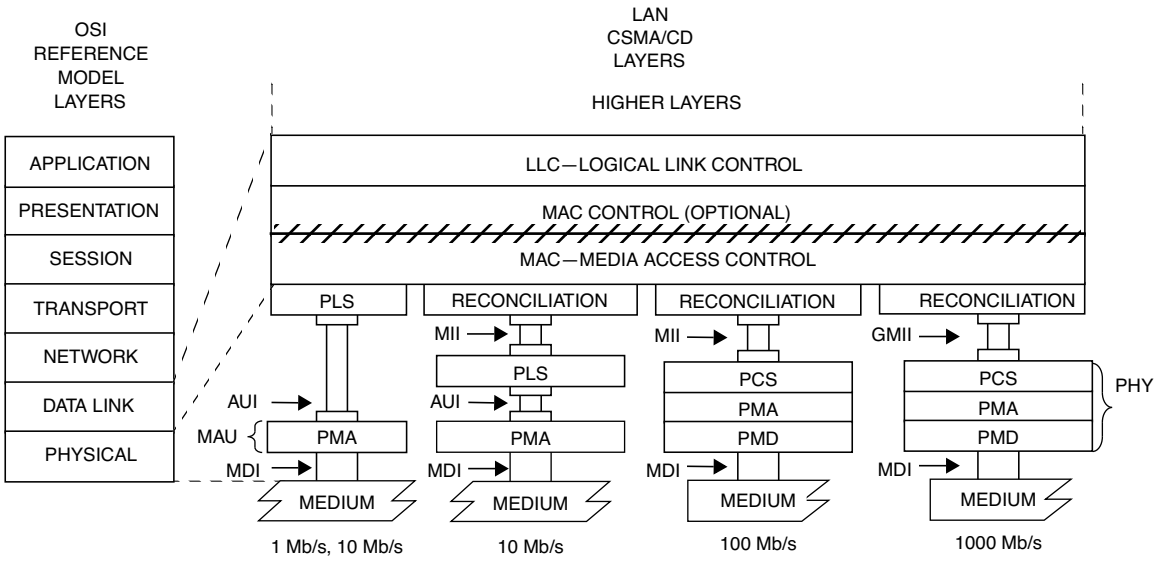
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2. Media Access Control (MAC) service specification

2.1 Scope and field of application

This clause specifies the services provided by the Media Access Control (MAC) sublayer and the optional MAC Control sublayer to the client of the MAC (MAC client) (see Figure 2–1). MAC clients may include the Logical Link Control (LLC) sublayer, Bridge Relay Entity, or other users of ISO/IEC LAN International Standard MAC services (see Figure 2–2). The services are described in an abstract way and do not imply any particular implementation, or any exposed interface. There is not necessarily a one-to-one correspondence between the primitives and the formal procedures and interfaces described in Clauses 4 and 31.



AUI = ATTACHMENT UNIT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MAU = MEDIUM ATTACHMENT UNIT

PLS = PHYSICAL LAYER SIGNALING
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 2–1—Service specification relation to the LAN model

2.2 Overview of the service

2.2.1 General description of services provided by the layer

The services provided by the MAC sublayer allow the local MAC client entity to exchange LLC data units with peer LLC sublayer entities. Optional support may be provided for resetting the MAC sublayer entity to a known state.

The optional MAC control sublayer provides an additional service for controlling MAC operation. This may be used to provide flow control between peer MAC client entities across the underlying channel.

2.2.2 Model used for the service specification

The model used in this service specification is identical to that used in 1.2.

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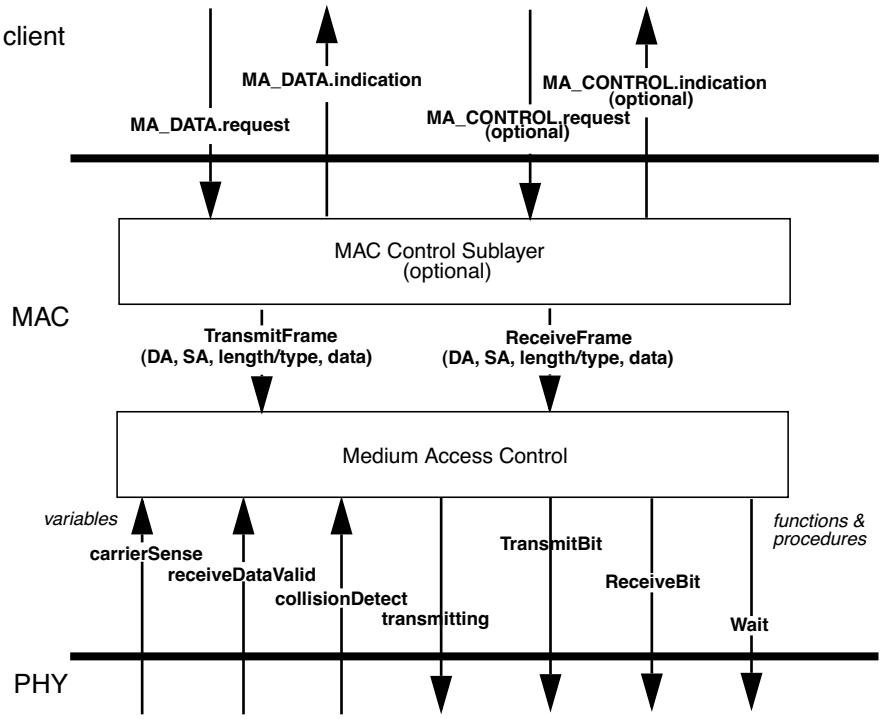


Figure 2–2—Service specification primitive relationships (optional MAC control sublayer implemented)

2.2.3 Overview of interactions

MA_DATA.request
MA_DATA.indication
MA_CONTROL.request (used by optional MAC Control sublayer)
MA_CONTROL.indication (used by optional MAC Control sublayer)

2.2.4 Basic services and options

The MA_DATA.request and MA_DATA.indication service primitives described in this subclause are mandatory. The MA_CONTROL.request and MA_CONTROL.indication service primitives are mandatory if the optional MAC Control sublayer is implemented.

2.3 Detailed service specification

2.3.1 MA_DATA.request

2.3.1.1 Function

This primitive defines the transfer of data from a MAC client entity to a single peer entity or multiple peer entities in the case of group addresses.

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2.3.1.2 Semantics of the service primitive

The semantics of the primitive are as follows:

```
MA_DATA.request     (
                    destination_address,
                    source_address,
                    m_sdu,
                    service_class
                    )
```

The destination_address parameter may specify either an individual or a group MAC entity address. It must contain sufficient information to create the DA field that is prepended to the frame by the local MAC sublayer entity and any physical information. The source_address parameter, if present, must specify an individual MAC address. If the source_address parameter is omitted, the local MAC sublayer entity will insert a value associated with that entity. The m_sdu parameter specifies the MAC service data unit to be transmitted by the MAC sublayer entity. There is sufficient information associated with m_sdu for the MAC sublayer entity to determine the length of the data unit. The service_class parameter indicates a quality of service requested by the MAC client (see 2.3.1.5).

2.3.1.3 When generated

This primitive is generated by the MAC client entity whenever data shall be transferred to a peer entity or entities. This can be in response to a request from higher protocol layers or from data generated internally to the MAC client, such as required by Type 2 LLC service.

2.3.1.4 Effect of receipt

The receipt of this primitive will cause the MAC entity to insert all MAC specific fields, including DA, SA, and any fields that are unique to the particular media access method, and pass the properly formed frame to the lower protocol layers for transfer to the peer MAC sublayer entity or entities.

2.3.1.5 Additional comments

The CSMA/CD MAC protocol provides a single quality of service regardless of the service_class requested.

2.3.2 MA_DATA.indication

2.3.2.1 Function

This primitive defines the transfer of data from the MAC sublayer entity (through the optional MAC Control sublayer, if implemented) to the MAC client entity or entities in the case of group addresses.

2.3.2.2 Semantics of the service primitive

The semantics of the primitive are as follows:

```
MA_DATA.indication     (
                       destination_address,
                       source_address,
                       m_sdu,
                       reception_status
                       )
```

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The destination_address parameter may be either an individual or a group address as specified by the DA field of the incoming frame. The source_address parameter is an individual address as specified by the SA field of the incoming frame. The m_sdu parameter specifies the MAC service data unit as received by the local MAC entity. The reception_status parameter is used to pass status information to the MAC client entity.

2.3.2.3 When generated

The MA_DATA.indication is passed from the MAC sublayer entity (through the optional MAC Control sublayer, if implemented) to the MAC client entity or entities to indicate the arrival of a frame to the local MAC sublayer entity that is destined for the MAC client. Such frames are reported only if they are validly formed, received without error, and their destination address designates the local MAC entity. Frames destined for the optional MAC Control sublayer are not passed to the MAC client if the MAC Control sublayer is implemented.

2.3.2.4 Effect of receipt

The effect of receipt of this primitive by the MAC client is unspecified.

2.3.2.5 Additional comments

If the local MAC sublayer entity is designated by the destination_address parameter of an MA_DATA.request, the indication primitive will also be invoked by the MAC entity to the MAC client entity. This characteristic of the MAC sublayer may be due to unique functionality within the MAC sublayer or characteristics of the lower layers (for example, all frames transmitted to the broadcast address will invoke MA_DATA.indication at all stations in the network including the station that generated the request).

2.3.3 MA_CONTROL.request

This primitive defines the transfer of control requests from the MAC client to the MAC Control sublayer. Implementation of the MA_CONTROL.request primitive is mandatory if the optional MAC Control sublayer is implemented in a device.

2.3.3.1 Function

This primitive defines the transfer of control commands from a MAC client entity to the local MAC Control sublayer entity.

2.3.3.2 Semantics of the service primitive

The semantics of the primitive are as follows:

```
MA_CONTROL.request      (
                        destination_address,
                        opcode,
                        request_operand_list
                        )
```

The destination_address parameter may specify either an individual or a group MAC entity address. It must contain sufficient information to create the DA field that is prepended to the frame by the local MAC sublayer entity. The opcode specifies the control operation requested by the MAC client entity. The request_operand_list is an opcode-specific set of parameters.

The valid opcodes and their respective meanings are defined in Clause 31.

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2.3.3.3 When generated

This primitive is generated by a MAC client whenever it wishes to use the services of the optional MAC Control sublayer entity.

2.3.3.4 Effect of receipt

The effect of receipt of this primitive by the MAC Control sublayer is opcode-specific. (See Clause 31.)

2.3.4 MA_CONTROL.indication

2.3.4.1 Function

This primitive defines the transfer of control status indications from the MAC Control sublayer to the MAC client. Implementation of the MA_CONTROL.indication primitive is mandatory if the optional MAC Control sublayer is implemented in a device.

2.3.4.2 Semantics of the service primitive

The semantics of the primitive are as follows:

```
MA_CONTROL.indication        (
                             opcode,
                             indication_operand_list
                             )
```

The elements of the indication_operand_list are opcode-specific, and specified in the annexes to Clause 31.

2.3.4.3 When generated

The MA_CONTROL.indication is generated by the MAC Control sublayer under conditions specific to each MAC Control operation.

2.3.4.4 Effect of receipt

The effect of receipt of this primitive by the MAC client is unspecified.

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3. Media access control frame structure

3.1 Overview

This clause defines in detail the frame structure for data communication systems using the CSMA/CD MAC. It defines the syntax and semantics of the various components of the MAC frame.

Two frame formats are specified in this clause:

a) A basic MAC frame format, and
b) An extension of the basic MAC frame format for Tagged MAC frames, i.e., frames that carry QTag Prefixes.

3.1.1 MAC frame format

Figure 3–1 shows the nine fields of a frame: the preamble, Start Frame Delimiter (SFD), the addresses of the frame's source and destination, a length or type field to indicate the length or protocol type of the following field that contains the MAC Client data, a field that contains padding if required, the frame check sequence field containing a cyclic redundancy check value to detect errors in a received frame, and an extension field if required (for 1000 Mb/s half duplex operation only). Of these nine fields, all are of fixed size except for the data, pad, and extension fields, which may contain an integer number of octets between the minimum and maximum values that are determined by the specific implementation of the CSMA/CD MAC. See 4.4 for particular implementations.

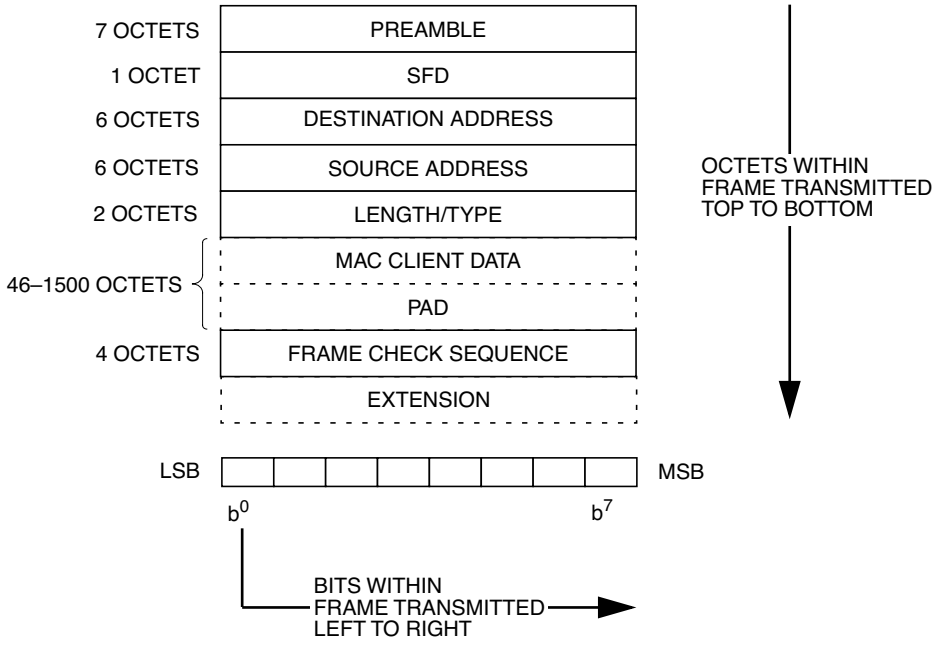


Figure 3–1—MAC frame format

The minimum and maximum frame size limits in 4.4 refer to that portion of the frame from the destination address field through the frame check sequence field, inclusive.

Relative to Figure 3–1, the octets of a frame are transmitted from top to bottom, and the bits of each octet are transmitted from left to right.

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3.2 Elements of the MAC frame

3.2.1 Preamble field

The preamble field is a 7-octet field that is used to allow the PLS circuitry to reach its steady-state synchronization with the received frame's timing (see 4.2.5).

3.2.2 Start Frame Delimiter (SFD) field

The SFD field is the sequence 10101011. It immediately follows the preamble pattern and indicates the start of a frame.

3.2.3 Address fields

Each MAC frame shall contain two address fields: the Destination Address field and the Source Address field, in that order. The Destination Address field shall specify the destination addressee(s) for which the frame is intended. The Source Address field shall identify the station from which the frame was initiated. The representation of each address field shall be as follows (see Figure 3–2):

a) Each address field shall be 48 bits in length. While IEEE 802 specifies the use of either 16- or 48-bit addresses, no conformant implementation of IEEE 802.3 uses 16-bit addresses. The use of 16-bit addresses is specifically excluded by this standard.
b) The first bit (LSB) shall be used in the Destination Address field as an address type designation bit to identify the Destination Address either as an individual or as a group address. If this bit is 0, it shall indicate that the address field contains an individual address. If this bit is 1, it shall indicate that the address field contains a group address that identifies none, one or more, or all of the stations connected to the LAN. In the Source Address field, the first bit is reserved and set to 0.
c) The second bit shall be used to distinguish between locally or globally administered addresses. For globally administered (or U, universal) addresses, the bit is set to 0. If an address is to be assigned locally, this bit shall be set to 1. Note that for the broadcast address, this bit is also a 1.
d) Each octet of each address field shall be transmitted least significant bit first.

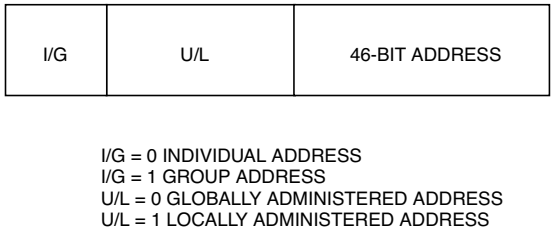


Figure 3–2—Address field format

3.2.3.1 Address designation

A MAC sublayer address is one of two types:

a) *Individual Address*. The address associated with a particular station on the network.
b) *Group Address*. A multidestination address, associated with one or more stations on a given network. There are two kinds of multicast address:
   1) *Multicast-Group Address*. An address associated by higher-level convention with a group of logically related stations.

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2) *Broadcast Address*. A distinguished, predefined multicast address that always denotes the set of all stations on a given LAN.

All 1's in the Destination Address field shall be predefined to be the Broadcast Address. This group shall be predefined for each communication medium to consist of all stations actively connected to that medium; it shall be used to broadcast to all the active stations on that medium. All stations shall be able to recognize the Broadcast Address. It is not necessary that a station be capable of generating the Broadcast Address.

The address space shall also be partitioned into locally administered and globally administered addresses. The nature of a body and the procedures by which it administers these global (U) addresses is beyond the scope of this standard.[12]

3.2.4 Destination Address field

The Destination Address field specifies the station(s) for which the frame is intended. It may be an individual or multicast (including broadcast) address.

3.2.5 Source Address field

The Source Address field specifies the station sending the frame. The Source Address field is not interpreted by the CSMA/CD MAC sublayer.

3.2.6 Length/Type field

This two-octet field takes one of two meanings, depending on its numeric value. For numerical evaluation, the first octet is the most significant octet of this field.

a) If the value of this field is less than or equal to the value of maxValidFrame (as specified in 4.2.7.1), then the Length/Type field indicates the number of MAC client data octets contained in the subsequent data field of the frame (Length interpretation).

b) If the value of this field is greater than or equal to 1536 decimal (equal to 0600 hexadecimal), then the Length/Type field indicates the nature of the MAC client protocol (Type interpretation).[13]
The Length and Type interpretations of this field are mutually exclusive.

When used as a Type field, it is the responsibility of the MAC client to ensure that the MAC client operates properly when the MAC sublayer pads the supplied data, as discussed in 3.2.7.

Regardless of the interpretation of the Length/Type field, if the length of the data field is less than the minimum required for proper operation of the protocol, a PAD field (a sequence of octets) will be added at the end of the data field but prior to the FCS field, specified below. The procedure that determines the size of the PAD field is specified in 4.2.8. The Length/Type field is transmitted and received with the high order octet first.

3.2.7 Data and PAD fields

The data field contains a sequence of n octets. Full data transparency is provided in the sense that any arbitrary sequence of octet values may appear in the data field up to a maximum number specified by the implementation of the standard that is used. A minimum frame size is required for correct CSMA/CD protocol operation and is specified by the particular implementation of the standard. If necessary, the data field is extended by appending extra bits (that is, a pad) in units of octets after the data field but prior to calculating and appending the FCS. The size of the pad, if any, is determined by the size of the data field supplied by the

[12]For information on how to use MAC addresses, see IEEE Std 802-2001, Overview and Architecture. To apply for an Organizationally Unique Identifier for building a MAC address, contact the Registration Authority, IEEE Standards Department, P.O. Box 1331, 445 Hoes Lane, Piscataway, NJ 08855-1331, USA; +1 732 562 3813; fax +1 732 562 1571. URL:http://standards.ieee.org/.

[13]Type field assignments are administered by the Registration Authority, IEEE Standards Department (see Footnote 12 for address).

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MAC client and the minimum frame size and address size parameters of the particular implementation. The maximum size of the data field is determined by the maximum frame size and address size parameters of the particular implementation.

The length of PAD field required for MAC client data that is n octets long is max [0, minFrameSize – (8 × n + 2 × addressSize + 48)] bits. The maximum possible size of the data field is maxUntaggedFrameSize – (2 × addressSize + 48)/8 octets. See 4.4 for a discussion of implementation parameters; see 4.2.3.3 for a discussion of the minFrameSize.

3.2.8 Frame Check Sequence (FCS) field

A cyclic redundancy check (CRC) is used by the transmit and receive algorithms to generate a CRC value for the FCS field. The frame check sequence (FCS) field contains a 4-octet (32-bit) cyclic redundancy check (CRC) value. This value is computed as a function of the contents of the source address, destination address, length, LLC data and pad (that is, all fields except the preamble, SFD, FCS, and extension). The encoding is defined by the following generating polynomial.

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$$

Mathematically, the CRC value corresponding to a given frame is defined by the following procedure:

a) The first 32 bits of the frame are complemented.
b) The n bits of the frame are then considered to be the coefficients of a polynomial M(x) of degree n–1. (The first bit of the Destination Address field corresponds to the $x^{(n-1)}$ term and the last bit of the data field corresponds to the x^0 term.)
c) M(x) is multiplied by x^{32} and divided by G(x), producing a remainder R(x) of degree ≤31.
d) The coefficients of R(x) are considered to be a 32-bit sequence.
e) The bit sequence is complemented and the result is the CRC.

The 32 bits of the CRC value are placed in the frame check sequence field so that the x^{31} term is the left-most bit of the first octet, and the x^0 term is the right most bit of the last octet. (The bits of the CRC are thus transmitted in the order x^{31}, x^{30},…, x^1, x^0.) See reference [B37].

3.2.9 Extension field

The Extension field follows the FCS field, and is made up of a sequence of extension bits, which are readily distinguished from data bits. The length of the field is in the range of zero to (slotTime—minFrameSize) bits, inclusive. The contents of the Extension field are not included in the FCS computation.

The Extension field may have a length of greater than zero under the conditions that are described in 4.2.3.4. The length of the Extension field will be zero under all other conditions. Implementations defined in 4.4.2 may ignore this field altogether if the number of bit times in the slotTime parameter is equal to the number of bits in the minFrameSize parameter.

3.3 Order of bit transmission

Each octet of the MAC frame, with the exception of the FCS, is transmitted low-order bit first.

3.4 Invalid MAC frame

An invalid MAC frame shall be defined as one that meets at least one of the following conditions:

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a) The frame length is inconsistent with a length value specified in the length/type field. If the length/type field contains a type value as defined by 3.2.6, then the frame length is assumed to be consistent with this field and should not be considered an invalid frame on this basis.
b) It is not an integral number of octets in length.
c) The bits of the incoming frame (exclusive of the FCS field itself) do not generate a CRC value identical to the one received.

The contents of invalid MAC frames shall not be passed to the LLC or MAC Control sublayers.[14] The occurrence of invalid MAC frames may be communicated to network management.

3.5 Elements of the Tagged MAC Frame

Figure 3–3 shows the format of a Tagged MAC Frame. This format is an extension of the MAC Frame specified in 3.1.1 and 3.2. The octet and bit ordering of the fields are identical to that specified in 3.1.1 and 3.3. The extensions for tagging are as follows:

a) A 4-octet QTag Prefix is inserted between the end of the Source Address and the MAC Client Length/Type field of the MAC frame. The QTag Prefix comprises two fields:
   1) A 2-octet constant Length/Type field value consistent with the Type interpretation and equal to the value of the 802.1Q Tag Protocol Type (802.1QTagType, see 3.5.4).
   2) A 2-octet field containing Tag Control Information.
b) Following the QTag Prefix is the MAC Client Length/Type field, MAC Client Data, Pad (if necessary), FCS, and Extension (if necessary) fields of the basic MAC frame.
c) The length of the frame is extended by 4 octets by the QTag Prefix.

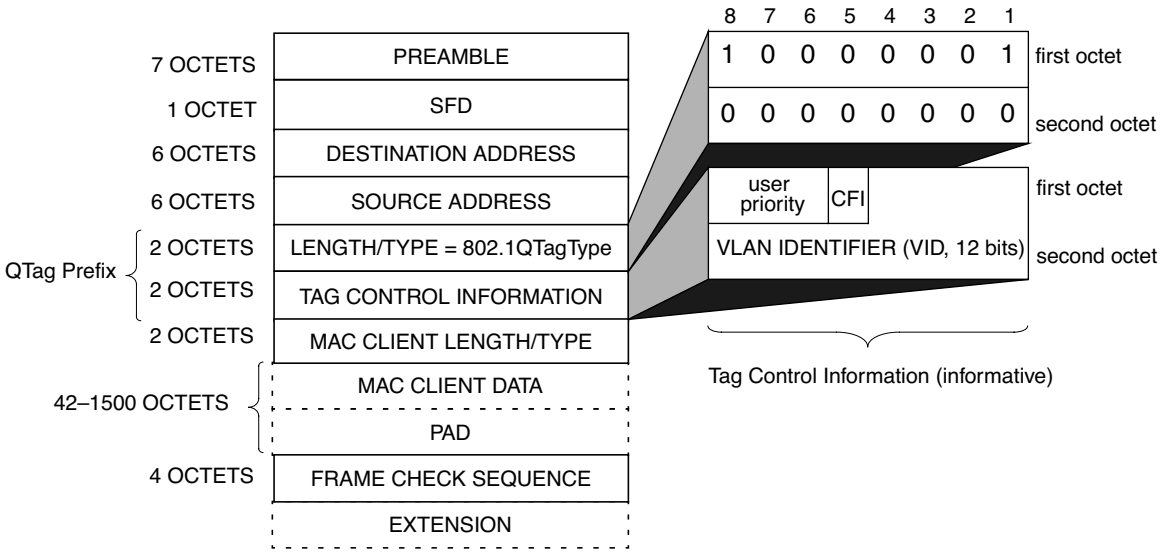


Figure 3–3—Tagged MAC frame format

NOTE—The normative definition of the Tag Control Information field shown in Figure 3–3 can be found in IEEE P802.1Q. Also, while Figure 3–1 uses the convention that the most significant bit of an octet is the rightmost bit, Figure 3–3 uses the opposite convention, i.e., the most significant bit is shown in the leftmost position. The latter convention is consistent with the specification of IEEE P802.1Q. This is a pictorial difference only; there is no difference in the actual order of bits transmitted on the LAN.

[14]Invalid MAC frames may be ignored, discarded, or used in a private manner by MAC clients other than LLC or MAC control. The use of such frames is beyond the scope of this standard.

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3.5.1 Preamble field

The Preamble field is identical in structure and semantics to the Preamble field of the basic MAC frame, described in 3.2.1.

3.5.2 Start Frame Delimiter (SFD) field

The SFD field is identical in structure and semantics to the SFD field of the basic MAC frame, described in 3.2.2.

3.5.3 Address fields

The address fields (both Destination address and Source address) are identical in structure and semantics to the address fields of the basic MAC frame, described in 3.2.3, 3.2.4, and 3.2.5.

3.5.4 Length/Type field

The Length/Type field of a tagged MAC frame always uses the Type interpretation, and contains the 802.1Q Tag Protocol Type: a constant equal to 0x81-00.

3.5.5 Tag Control Information field (informative)

The Tag Control Information field is subdivided as follows:

a) A 3-bit User Priority field,
b) A Canonical Format Indicator (CFI), and
c) A 12-bit VLAN Identifier.

The structure and semantics within the Tag Control Information field are defined in IEEE P802.1Q.

3.5.6 MAC Client Length/Type field

The MAC Client Length/Type field contains the original Length/Type field from the MAC frame prior to insertion of the QTag Prefix. The QTag Prefix offsets this field exactly 4 octets from its position in an untagged MAC frame.

3.5.7 Data and PAD fields

The Data and PAD fields are identical in structure and semantics to the Data and PAD fields of the basic MAC frame described in 3.2.7, except in the following respect: For tagged MAC frames, the value of n in the PAD field calculation may be either the length of the MAC Client Data or the combined length of MAC Client Data and QTag Prefix.

3.5.8 Frame Check Sequence (FCS) field

The FCS field is identical in structure and semantics to the FCS field of the basic MAC frame, described in 3.2.8.

3.5.9 Extension field

The Extension field is identical in structure and semantics to the Extension field of the basic MAC frame, described in 3.2.9.

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4. Media Access Control

4.1 Functional model of the MAC method

4.1.1 Overview

The architectural model described in Clause 1 is used in this clause to provide a functional description of the LAN CSMA/CD MAC sublayer.

The MAC sublayer defines a medium-independent facility, built on the medium-dependent physical facility provided by the Physical Layer, and under the access-layer-independent LAN LLC sublayer (or other MAC client). It is applicable to a general class of local area broadcast media suitable for use with the media access discipline known as Carrier Sense Multiple Access with Collision Detection (CSMA/CD).

The LLC sublayer and the MAC sublayer together are intended to have the same function as that described in the OSI model for the Data Link Layer alone. In a broadcast network, the notion of a data link between two network entities does not correspond directly to a distinct physical connection. Nevertheless, the partitioning of functions presented in this standard requires two main functions generally associated with a data link control procedure to be performed in the MAC sublayer. They are as follows:

a) Data encapsulation (transmit and receive)
   1) Framing (frame boundary delimitation, frame synchronization)
   2) Addressing (handling of source and destination addresses)
   3) Error detection (detection of physical medium transmission errors)
b) Media Access Management
   1) Medium allocation (collision avoidance)
   2) Contention resolution (collision handling)

An optional MAC control sublayer, architecturally positioned between LLC (or other MAC client) and the MAC, is specified in Clause 31. This MAC Control sublayer is transparent to both the underlying MAC and its client (typically LLC). The MAC sublayer operates independently of its client; i.e., it is unaware whether the client is LLC or the MAC Control sublayer. This allows the MAC to be specified and implemented in one manner, whether or not the MAC Control sublayer is implemented. References to LLC as the MAC client in text and figures apply equally to the MAC Control sublayer, if implemented.

This standard provides for two modes of operation of the MAC sublayer:

a) In *half duplex* mode, stations contend for the use of the physical medium, using the CSMA/CD algorithms specified. Bidirectional communication is accomplished by rapid exchange of frames, rather than full duplex operation. Half duplex operation is possible on all supported media; it is required on those media that are incapable of supporting simultaneous transmission and reception without interference, for example, 10BASE2 and 100BASE-T4.
b) The *full duplex* mode of operation can be used when all of the following are true:
   1) The physical medium is capable of supporting simultaneous transmission and reception without interference (e.g., 10BASE-T, 10BASE-FL, and 100BASE-TX/FX).
   2) There are exactly two stations on the LAN. This allows the physical medium to be treated as a full duplex point-to-point link between the stations. Since there is no contention for use of a shared medium, the multiple access (i.e., CSMA/CD) algorithms are unnecessary.
   3) Both stations on the LAN are capable of and have been configured to use full duplex operation.

The most common configuration envisioned for full duplex operation consists of a central bridge (also known as a switch) with a dedicated LAN connecting each bridge port to a single device.

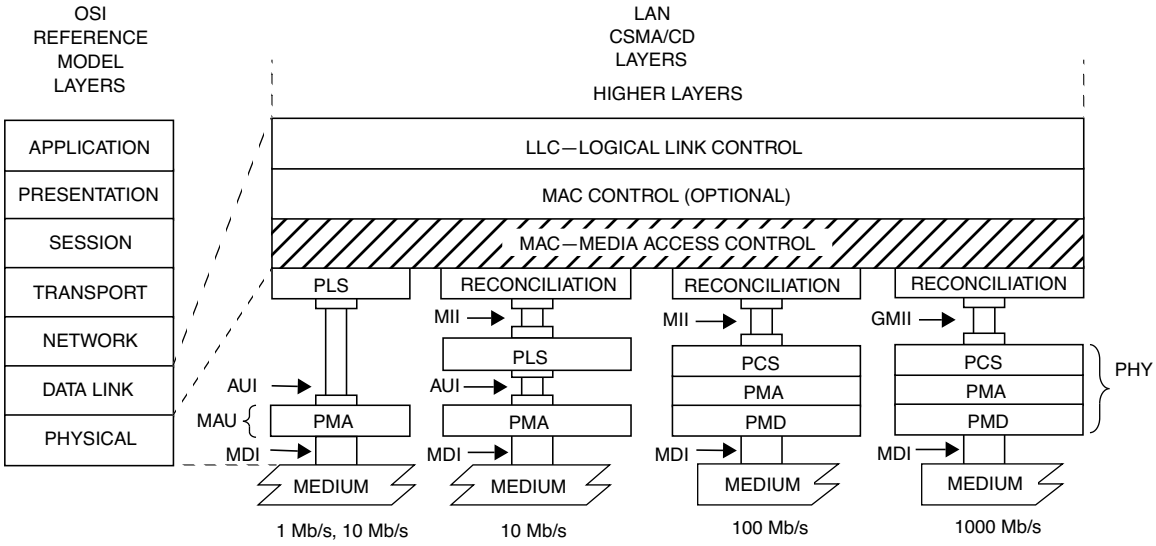
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The formal specification of the MAC in 4.2 comprises both the half duplex and full duplex modes of operation. The remainder of this clause provides a functional model of the CSMA/CD MAC method.

4.1.2 CSMA/CD operation

This clause provides an overview of frame transmission and reception in terms of the functional model of the architecture. This overview is descriptive, rather than definitional; the formal specifications of the operations described here are given in 4.2 and 4.3. Specific implementations for CSMA/CD mechanisms that meet this standard are given in 4.4. Figure 4–1 provides the architectural model described functionally in the subclauses that follow.



AUI = ATTACHMENT UNIT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MAU = MEDIUM ATTACHMENT UNIT

PLS = PHYSICAL LAYER SIGNALING
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 4–1—MAC sublayer partitioning, relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

The Physical Layer Signaling (PLS) component of the Physical Layer provides an interface to the MAC sublayer for the serial transmission of bits onto the physical media. For completeness, in the operational description that follows some of these functions are included as descriptive material. The concise specification of these functions is given in 4.2 for the MAC functions and in Clause 7 for PLS.

Transmit frame operations are independent from the receive frame operations. A transmitted frame addressed to the originating station will be received and passed to the MAC client at that station. This characteristic of the MAC sublayer may be implemented by functionality within the MAC sublayer or full duplex characteristics of portions of the lower layers.

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4.1.2.1 Normal operation

4.1.2.1.1 Transmission without contention

When a MAC client requests the transmission of a frame, the Transmit Data Encapsulation component of the CSMA/CD MAC sublayer constructs the frame from the client-supplied data. It prepends a preamble and a Start Frame Delimiter to the beginning of the frame. Using information provided by the client, the CSMA/CD MAC sublayer also appends a PAD at the end of the MAC information field of sufficient length to ensure that the transmitted frame length satisfies a minimum frame size requirement (see 4.2.3.3). It also prepends destination and source addresses, the length/type field, and appends a frame check sequence to provide for error detection. The frame is then handed to the Transmit Media Access Management component in the MAC sublayer for transmission.

In half duplex mode, Transmit Media Access Management attempts to avoid contention with other traffic on the medium by monitoring the carrier sense signal provided by the Physical Layer Signaling (PLS) component and deferring to passing traffic. When the medium is clear, frame transmission is initiated (after a brief interframe delay to provide recovery time for other CSMA/CD MAC sublayers and for the physical medium). The MAC sublayer then provides a serial stream of bits to the Physical Layer for transmission.

In half duplex mode at operating speeds above 100 Mb/s, the minimum frame size is insufficient to ensure the proper operation of the CSMA/CD protocol for the desired network topologies. To circumvent this problem, the MAC sublayer will append a sequence of extension bits to frames which are less than slotTime bits in length so that the duration of the resulting transmission is sufficient to ensure proper operation of the CSMA/CD protocol.

In half duplex mode at operating speeds above 100 Mb/s, the CSMA/CD MAC may optionally transmit additional frames without relinquishing control of the transmission medium, up to a specified limit.

In full duplex mode, there is no need for Transmit Media Access Management to avoid contention with other traffic on the medium. Frame transmission may be initiated after the interframe delay, regardless of the presence of receive activity. In full duplex mode, the MAC sublayer does not perform either carrier extension or frame bursting.

The Physical Layer performs the task of generating the signals on the medium that represent the bits of the frame. Simultaneously, it monitors the medium and generates the collision detect signal, which in the contention-free case under discussion, remains off for the duration of the frame. A functional description of the Physical Layer is given in Clause 7 and beyond.

When transmission has completed without contention, the CSMA/CD MAC sublayer so informs the MAC client and awaits the next request for frame transmission.

4.1.2.1.2 Reception without contention

At each receiving station, the arrival of a frame is first detected by the Physical Layer, which responds by synchronizing with the incoming preamble, and by turning on the receiveDataValid signal. As the encoded bits arrive from the medium, they are decoded and translated back into binary data. The Physical Layer passes subsequent bits up to the MAC sublayer, where the leading bits are discarded, up to and including the end of the preamble and Start Frame Delimiter.

Meanwhile, the Receive Media Access Management component of the MAC sublayer, having observed receiveDataValid, has been waiting for the incoming bits to be delivered. Receive Media Access Management collects bits from the Physical Layer entity as long as the receiveDataValid signal remains on. When the receiveDataValid signal is removed, the frame is truncated to an octet boundary, if necessary, and passed to Receive Data Decapsulation for processing.

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Receive Data Decapsulation checks the frame's Destination Address field to decide whether the frame should be received by this station. If so, it passes the Destination Address (DA), the Source Address (SA), the Type/Length field, and the data to the MAC client along with an appropriate status code indicating reception_complete or reception_too_long. It also checks for invalid MAC frames by inspecting the frame check sequence to detect any damage to the frame enroute, and by checking for proper octet-boundary alignment of the end of the frame. Frames with a valid FCS may also be checked for proper octet boundary alignment.

In half duplex mode at operating speeds above 100 Mb/s, frames may be extended by the transmitting station under the conditions described in 4.2.3.4. The extension is discarded by the MAC sublayer of the receiving station, as defined in the procedural model in 4.2.9.

4.1.2.2 Access interference and recovery

In half duplex mode, if multiple stations attempt to transmit at the same time, it is possible for them to interfere with each other's transmissions, in spite of their attempts to avoid this by deferring. When transmissions from two stations overlap, the resulting contention is called a collision. Collisions occur only in half duplex mode, where a collision indicates that there is more than one station attempting to use the shared physical medium. In full duplex mode, two stations may transmit to each other simultaneously without causing interference. The Physical Layer may generate a collision indication, but this is ignored by the full duplex MAC.

A given station can experience a collision during the initial part of its transmission (the collision window) before its transmitted signal has had time to propagate to all stations on the CSMA/CD medium. Once the collision window has passed, a transmitting station is said to have acquired the medium; subsequent collisions are avoided since all other (properly functioning) stations can be assumed to have noticed the signal and to be deferring to it. The time to acquire the medium is thus based on the round-trip propagation time of the Physical Layer whose elements include the PLS, PMA, and physical medium.

In the event of a collision, the transmitting station's Physical Layer initially notices the interference on the medium and then turns on the collision detect signal. In half duplex mode, this is noticed in turn by the Transmit Media Access Management component of the MAC sublayer, and collision handling begins. First, Transmit Media Access Management enforces the collision by transmitting a bit sequence called jam. In 4.4, implementations that use this enforcement procedure are provided. This ensures that the duration of the collision is sufficient to be noticed by the other transmitting station(s) involved in the collision. After the jam is sent, Transmit Media Access Management terminates the transmission and schedules another transmission attempt after a randomly selected time interval. Retransmission is attempted again in the face of repeated collisions. Since repeated collisions indicate a busy medium, however, Transmit Media Access Management attempts to adjust to the medium load by backing off (voluntarily delaying its own retransmissions to reduce its load on the medium). This is accomplished by expanding the interval from which the random retransmission time is selected on each successive transmit attempt. Eventually, either the transmission succeeds, or the attempt is abandoned on the assumption that the medium has failed or has become overloaded.

In full duplex mode, a station ignores any collision detect signal generated by the Physical Layer. Transmit Media Access Management in a full duplex station will always be able to transmit its frames without contention, so there is never any need to jam or reschedule transmissions.

At the receiving end, the bits resulting from a collision are received and decoded by the PLS just as are the bits of a valid frame. Fragmentary frames received during collisions are distinguished from valid transmissions by the MAC sublayer's Receive Media Access Management component.

4.1.3 Relationships to the MAC client and Physical Layers

The CSMA/CD MAC sublayer provides services to the MAC client required for the transmission and reception of frames. Access to these services is specified in 4.3. The CSMA/CD MAC sublayer makes a best effort

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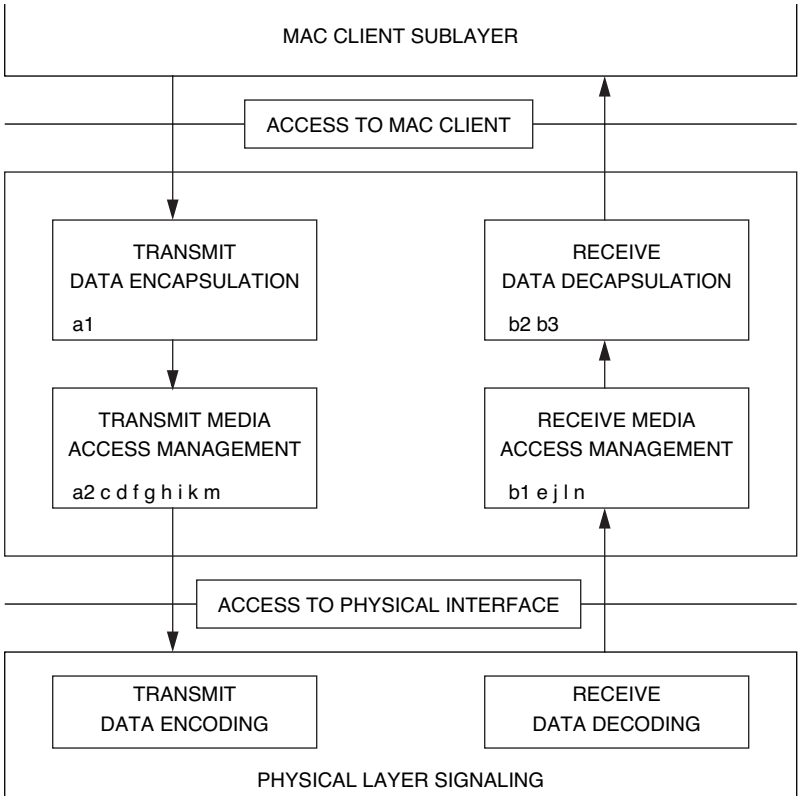
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to acquire the medium and transfer a serial stream of bits to the Physical Layer. Although certain errors are reported to the client, error recovery is not provided by MAC. Error recovery may be provided by the MAC client or higher (sub)layers.

4.1.4 CSMA/CD access method functional capabilities

The following summary of the functional capabilities of the CSMA/CD MAC sublayer is intended as a quick reference guide to the capabilities of the standard, as shown in Figure 4–2:



NOTE—a1, b2, etc., refer to functions listed in 4.1.4.

Figure 4–2—CSMA/CD Media Access Control functions

a) For Frame Transmission
   1) Accepts data from the MAC client and constructs a frame.
   2) Presents a bit-serial data stream to the Physical Layer for transmission on the medium.

   NOTE—Assumes data passed from the client sublayer are octet multiples.

b) For Frame Reception
   1) Receives a bit-serial data stream from the Physical Layer.
   2) Presents to the MAC client sublayer frames that are either broadcast frames or directly addressed to the local station.
   3) Discards or passes to Network Management all frames not addressed to the receiving station.

c) In half duplex mode, defers transmission of a bit-serial stream whenever the physical medium is busy.
d) Appends proper FCS value to outgoing frames and verifies full octet boundary alignment.
e) Checks incoming frames for transmission errors by way of FCS and verifies octet boundary alignment
f) Delays transmission of frame bit stream for specified interframe gap period.
g) In half duplex mode, halts transmission when collision is detected.

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h) In half duplex mode, schedules retransmission after a collision until a specified retry limit is reached.
i) In half duplex mode, enforces collision to ensure propagation throughout network by sending jam message.
j) Discards received transmissions that are less than a minimum length.
k) Appends preamble, Start Frame Delimiter, DA, SA, Length/Type field, and FCS to all frames, and inserts PAD field for frames whose data length is less than a minimum value.
l) Removes preamble, Start Frame Delimiter, DA, SA, Length/Type field, FCS, and PAD field (if necessary) from received frames.
m) Appends extension bits to the first (or only) frame of a burst if it is less than slotTime bits in length when in half duplex mode at speeds above 100 Mb/s.
n) Strips extension bits from received frames when in half duplex mode at speeds above 100 Mb/s.

4.2 CSMA/CD Media Access Control (MAC) method: Precise specification

4.2.1 Introduction

A precise algorithmic definition is given in this subclause, providing procedural model for the CSMA/CD MAC process with a program in the computer language Pascal. See references [B11] and [B34] for resource material. Note whenever there is any apparent ambiguity concerning the definition of some aspect of the CSMA/CD MAC method, it is the Pascal procedural specification in 4.2.7 through 4.2.10 which should be consulted for the definitive statement. Subclauses 4.2.2 through 4.2.6 provide, in prose, a description of the access mechanism with the formal terminology to be used in the remaining subclauses.

4.2.2 Overview of the procedural model

The functions of the CSMA/CD MAC method are presented below, modeled as a program written in the computer language Pascal. This procedural model is intended as the primary specification of the functions to be provided in any CSMA/CD MAC sublayer implementation. It is important to distinguish, however, between the model and a real implementation. The model is optimized for simplicity and clarity of presentation, while any realistic implementation shall place heavier emphasis on such constraints as efficiency and suitability to a particular implementation technology or computer architecture. In this context, several important properties of the procedural model shall be considered.

4.2.2.1 Ground rules for the procedural model

a) First, it shall be emphasized that *the description of the MAC sublayer in a computer language is in no way intended to imply that procedures shall be implemented as a program executed by a computer.* The implementation may consist of any appropriate technology including hardware, firmware, software, or any combination.
b) Similarly, it shall be emphasized that it is the behavior of any MAC sublayer implementations that shall match the standard, not their internal structure. The internal details of the procedural model are useful only to the extent that they help specify that behavior clearly and precisely.
c) The handling of incoming and outgoing frames is rather stylized in the procedural model, in the sense that frames are handled as single entities by most of the MAC sublayer and are only serialized for presentation to the Physical Layer. In reality, many implementations will instead handle frames serially on a bit, octet or word basis. This approach has not been reflected in the procedural model, since this only complicates the description of the functions without changing them in any way.
d) The model consists of algorithms designed to be executed by a number of concurrent processes; these algorithms collectively implement the CSMA/CD procedure. The timing dependencies introduced by the need for concurrent activity are resolved in two ways:
    1) *Processes Versus External Events*. It is assumed that the algorithms are executed "very fast" relative to external events, in the sense that a process never falls behind in its work and fails to

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respond to an external event in a timely manner. For example, when a frame is to be received, it is assumed that the Media Access procedure ReceiveFrame is always called well before the frame in question has started to arrive.

2) *Processes Versus Processes*. Among processes, no assumptions are made about relative speeds of execution. This means that each interaction between two processes shall be structured to work correctly independent of their respective speeds. Note, however, that the timing of interactions among processes is often, in part, an indirect reflection of the timing of external events, in which case appropriate timing assumptions may still be made.

It is intended that the concurrency in the model reflect the parallelism intrinsic to the task of implementing the MAC client and MAC procedures, although the actual parallel structure of the implementations is likely to vary.

4.2.2.2 Use of Pascal in the procedural model

Several observations need to be made regarding the method with which Pascal is used for the model. Some of these observations are as follows:

a) The following limitations of the language have been circumvented to simplify the specification:
   1) The elements of the program (variables and procedures, for example) are presented in logical groupings, in top-down order. Certain Pascal ordering restrictions have thus been circumvented to improve readability.
   2) The *process* and *cycle* constructs of Concurrent Pascal, a Pascal derivative, have been introduced to indicate the sites of autonomous concurrent activity. As used here, a process is simply a parameterless procedure that begins execution at "the beginning of time" rather than being invoked by a procedure call. A cycle statement represents the main body of a process and is executed repeatedly forever.
   3) The lack of variable array bounds in the language has been circumvented by treating frames as if they are always of a single fixed size (which is never actually specified). The size of a frame depends on the size of its data field, hence the value of the "pseudo-constant" frameSize should be thought of as varying in the long term, even though it is fixed for any given frame.
   4) The use of a variant record to represent a frame (as fields and as bits) follows the spirit but not the letter of the Pascal Report, since it allows the underlying representation to be viewed as two different data types.

b) The model makes no use of any explicit interprocess synchronization primitives. Instead, all interprocess interaction is done by way of carefully stylized manipulation of shared variables. For example, some variables are set by only one process and inspected by another process in such a manner that the net result is independent of their execution speeds. While such techniques are not generally suitable for the construction of large concurrent programs, they simplify the model and more nearly resemble the methods appropriate to the most likely implementation technologies (microcode, hardware state machines, etc.)

4.2.2.3 Organization of the procedural model

The procedural model used here is based on seven cooperating concurrent processes. The Frame Transmitter process and the Frame Receiver process are provided by the clients of the MAC sublayer (which may include the LLC sublayer) and make use of the interface operations provided by the MAC sublayer. The other five processes are defined to reside in the MAC sublayer. The seven processes are as follows:

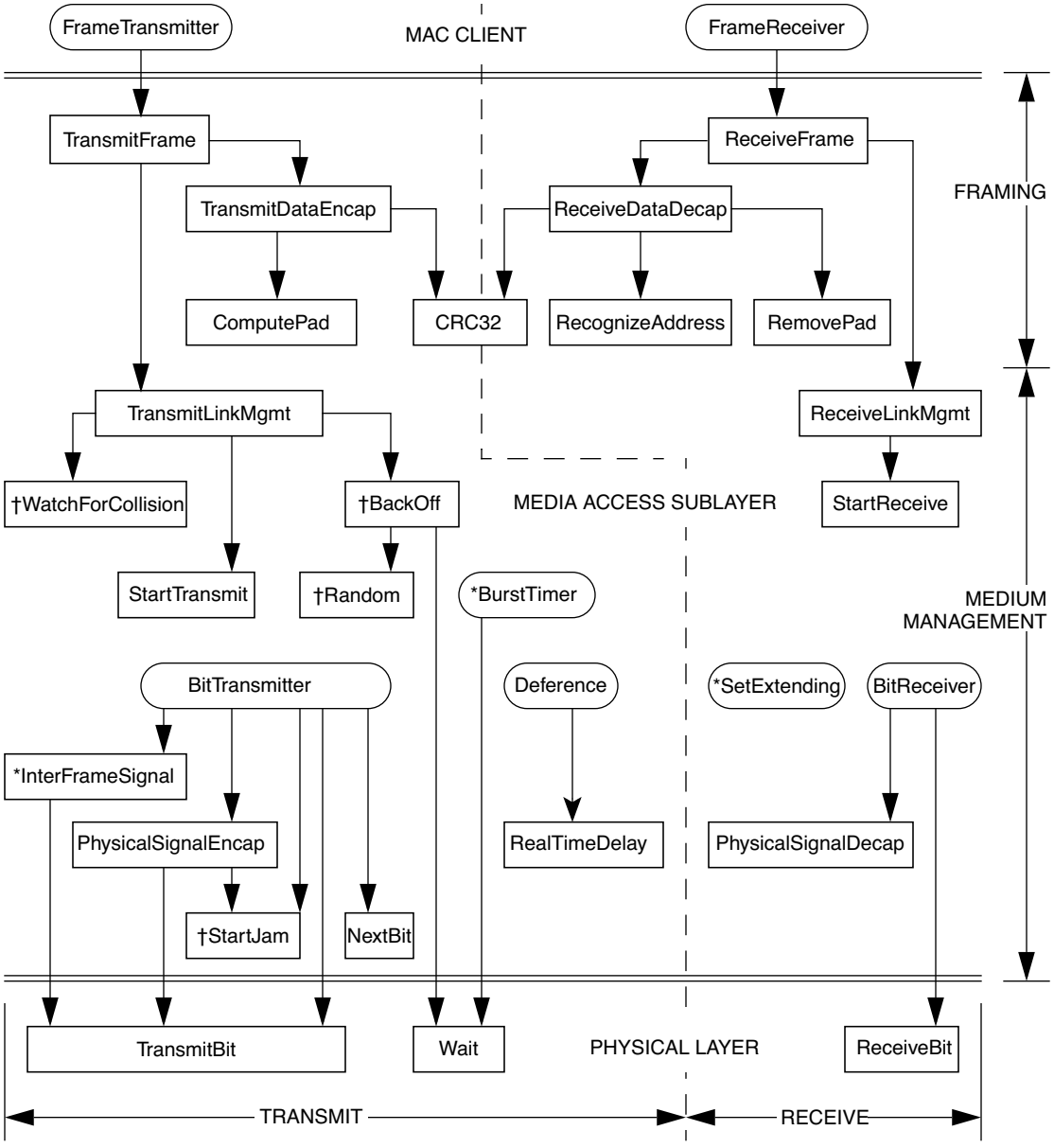
a) Frame Transmitter process
b) Frame Receiver process
c) Bit Transmitter process
d) Bit Receiver process
e) Deference process
f) BurstTimer process

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g) SetExtending process

This organization of the model is illustrated in Figure 4–3 and reflects the fact that the communication of entire frames is initiated by the client of the MAC sublayer, while the timing of collision backoff and of individual bit transfers is based on interactions between the MAC sublayer and the Physical-Layer-dependent bit time.



† Not applicable to full duplex operation
* Applicable only to half duplex operation at > 100 Mb/s

Figure 4–3—Relationship among CSMA/CD procedures

Figure 4–3 depicts the static structure of the procedural model, showing how the various processes and procedures interact by invoking each other. Figures 4–4a, 4–4b, 4–5a, and 4–5b summarize the dynamic behavior of the model during transmission and reception, focusing on the steps that shall be performed, rather than

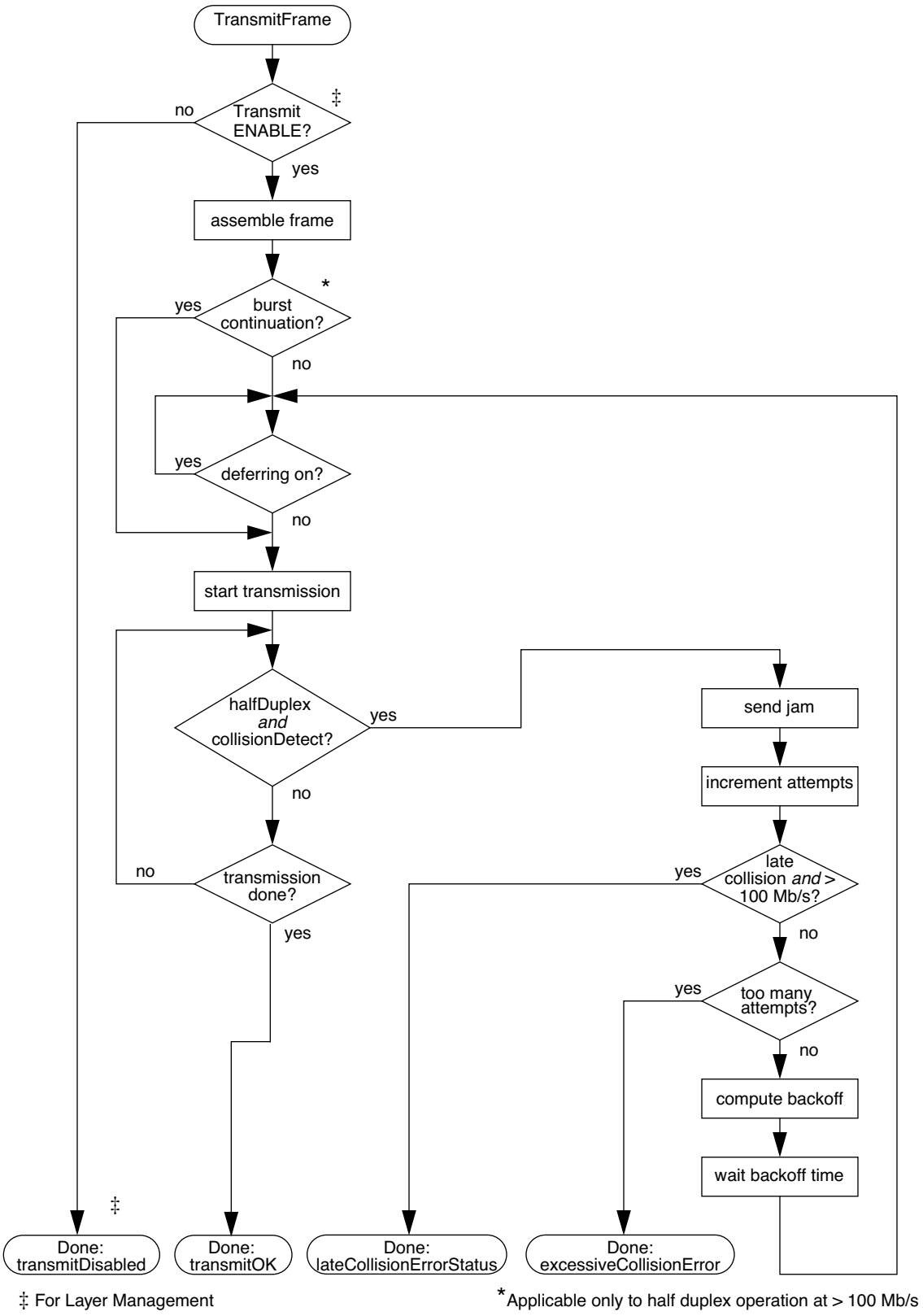
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a) TransmitFrame

Figure 4–4a—Control flow summary

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the procedural structure that performs them. The usage of the shared state variables is not depicted in the figures, but is described in the comments and prose in the following subclauses.

4.2.2.4 Layer management extensions to procedural model

In order to incorporate network management functions, this Procedural Model has been expanded beyond that provided in ISO/IEC 8802-3: 1990. Network management functions have been incorporated in two ways. First, 4.2.7–4.2.10, 4.3.2, Figure 4–4a, and Figure 4–4b have been modified and expanded to provide management services. Second, Layer Management procedures have been added as 5.2.4. Note that Pascal variables are shared between Clauses 4 and 5. Within the Pascal descriptions provided in Clause 4, a "‡" in the left margin indicates a line that has been added to support management services. These lines are only required if Layer Management is being implemented. These changes do not affect any aspect of the MAC behavior as observed at the LLC-MAC and MAC-PLS interfaces of ISO/IEC 8802-3: 1990.

The Pascal procedural specification shall be consulted for the definitive statement when there is any apparent ambiguity concerning the definition of some aspect of the CSMA/CD MAC access method.

The Layer Management facilities provided by the CSMA/CD MAC and Physical Layer management definitions provide the ability to manipulate management counters and initiate actions within the layers. The managed objects within this standard are defined as sets of attributes, actions, notifications, and behaviors in accordance with IEEE Std 802.1F-1993, and ISO/IEC International Standards for network management.

4.2.3 Frame transmission model

Frame transmission includes data encapsulation and Media Access management aspects:

a) Transmit Data Encapsulation includes the assembly of the outgoing frame (from the values provided by the MAC client) and frame check sequence generation.
b) Transmit Media Access Management includes carrier deference, interframe spacing, collision detection and enforcement, collision backoff and retransmission, carrier extension and frame bursting.

4.2.3.1 Transmit data encapsulation

4.2.3.1.1 Frame assembly

The fields of the CSMA/CD MAC frame are set to the values provided by the MAC client as arguments to the TransmitFrame operation (see 4.3) with the following exceptions: the padding field, the extension field, and the frame check sequence. The padding field is necessary to enforce the minimum frame size. The extension field is necessary to enforce the minimum carrier event duration on the medium in the half duplex mode at operating speeds above 100 Mb/s. The frame check sequence is set to the CRC value generated by the MAC sublayer.

4.2.3.1.2 Frame check sequence generation

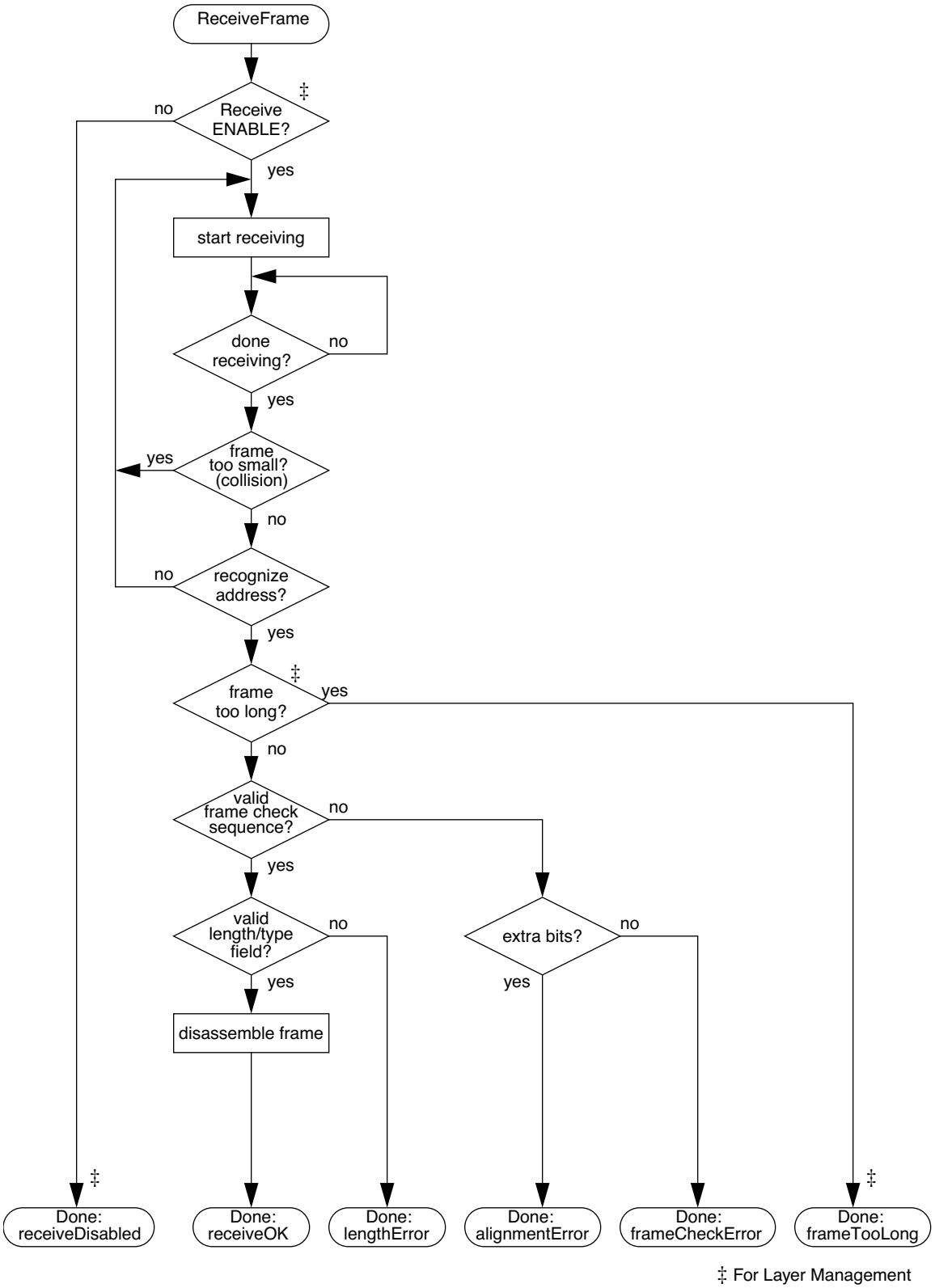
The CRC value defined in 3.2.8 is generated and inserted in the frame check sequence field, following the fields supplied by the MAC client.

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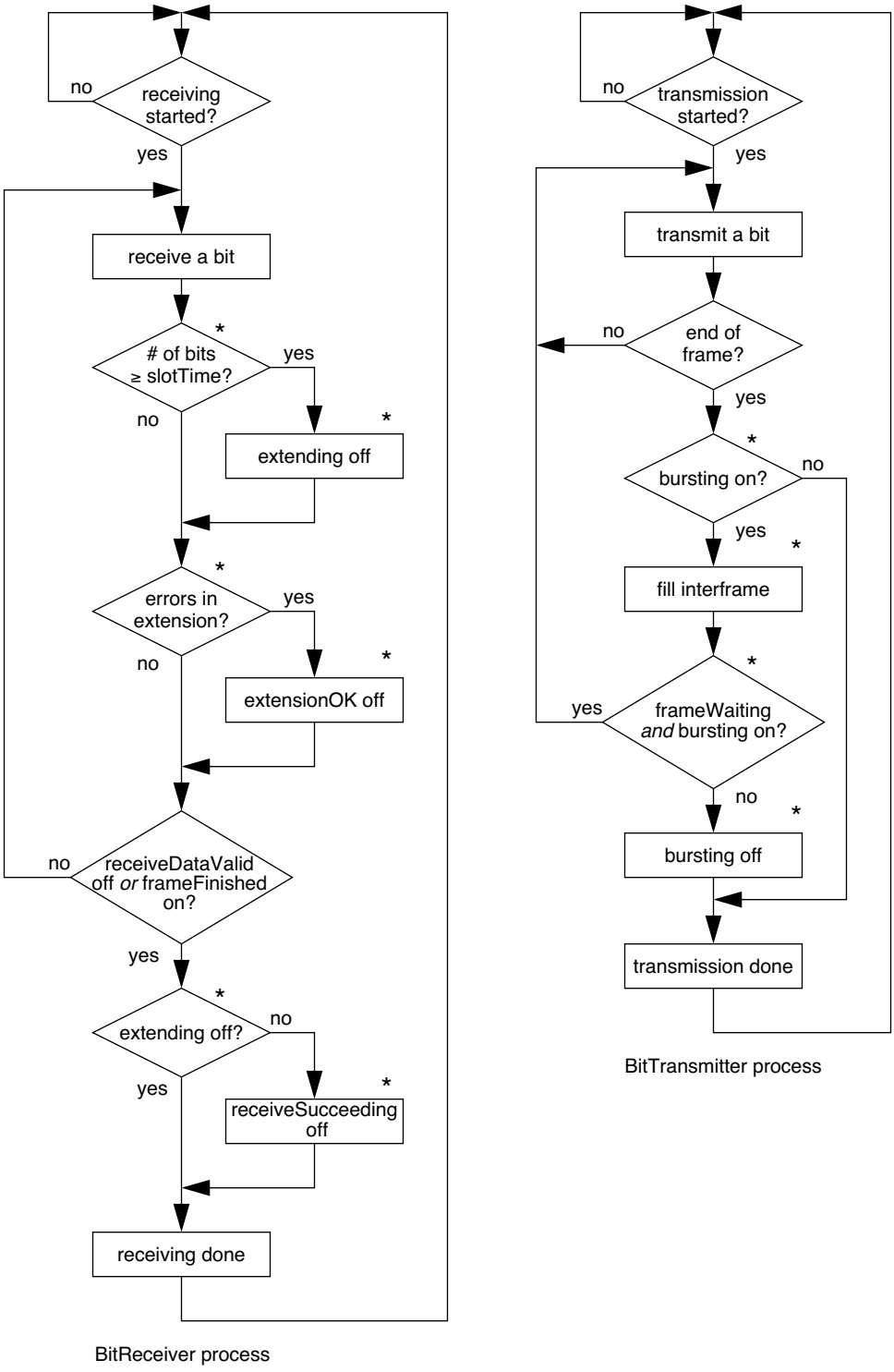
b) ReceiveFrame

Figure 4–4b—Control flow summary

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*Applicable only to half duplex operation at > 100 Mb/s

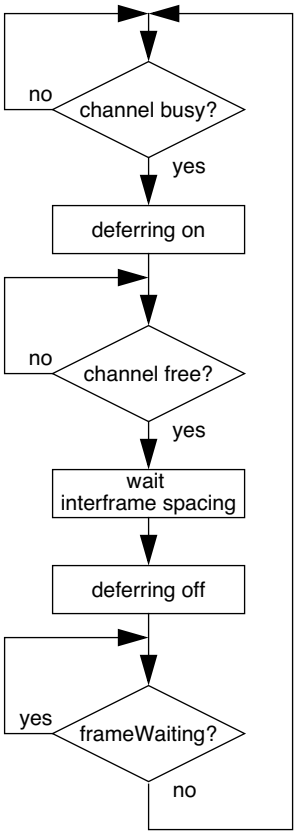
a) MAC sublayer

Figure 4–5a—Control flow

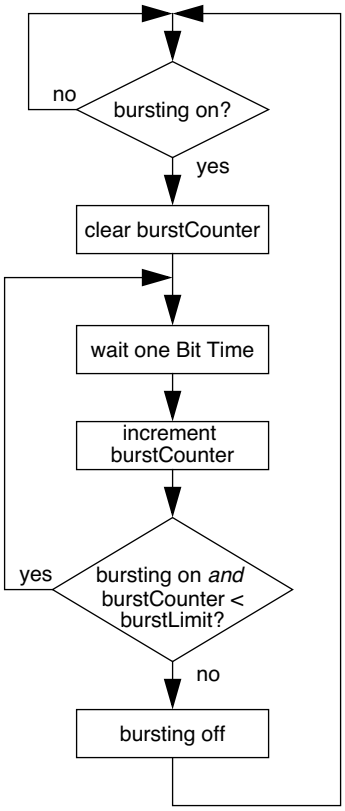
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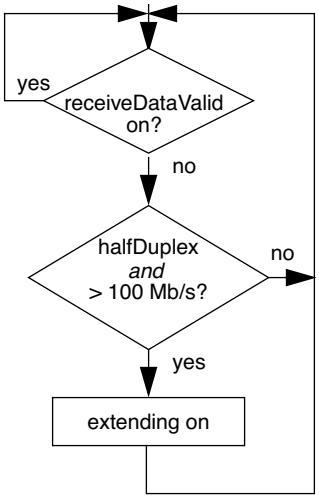
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Deference process



*BurstTimer process



*SetExtending process

*Applicable only to half duplex operation at > 100 Mb/s

b) MAC sublayer

Figure 4–5b—Control flow

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4.2.3.2 Transmit media access management

4.2.3.2.1 Deference

When a frame is submitted by the MAC client for transmission, the transmission is initiated as soon as possible, but in conformance with the rules of deference stated below. The rules of deference differ between half duplex and full duplex modes.

a) *Half duplex mode*

Even when it has nothing to transmit, the CSMA/CD MAC sublayer monitors the physical medium for traffic by watching the carrierSense signal provided by the PLS. Whenever the medium is busy, the CSMA/CD MAC defers to the passing frame by delaying any pending transmission of its own. After the last bit of the passing frame (that is, when *carrierSense* changes from true to false), the CSMA/CD MAC continues to defer for a proper interFrameSpacing (see 4.2.3.2.2).

If, at the end of the interFrameSpacing, a frame is waiting to be transmitted, transmission is initiated independent of the value of carrierSense. When transmission has completed (or immediately, if there was nothing to transmit) the CSMA/CD MAC sublayer resumes its original monitoring of carrierSense.

NOTE—It is possible for the PLS carrier sense indication to fail to be asserted briefly during a collision on the media. If the Deference process simply times the interframe gap based on this indication it is possible for a short interframe gap to be generated, leading to a potential reception failure of a subsequent frame. To enhance system robustness the following optional measures, as specified in 4.2.8, are recommended when interFrameSpacingPart1 is other than zero:

Start the timing of the interFrameSpacing as soon as transmitting and carrierSense are both false. Reset the interFrameSpacing timer if carrierSense becomes true during the first 2/3 of the interFrameSpacing timing interval. During the final 1/3 of the interval, the timer shall not be reset to ensure fair access to the medium. An initial period shorter than 2/3 of the interval is permissible including zero.

b) *Full duplex mode*

In full duplex mode, the CSMA/CD MAC does not defer pending transmissions based on the carrierSense signal from the PLS. Instead, it uses the internal variable *transmitting* to maintain proper MAC state while the transmission is in progress. After the last bit of a transmitted frame, (that is, when *transmitting* changes from true to false), the MAC continues to defer for a proper interFrameSpacing (see 4.2.3.2.2).

4.2.3.2.2 Interframe spacing

As defined in 4.2.3.1.1, the rules for deferring to passing frames ensure a minimum interframe spacing of interFrameSpacing seconds. This is intended to provide interframe recovery time for other CSMA/CD sublayers and for the physical medium.

Note that interFrameSpacing is the minimum value of the interframe spacing. If necessary for implementation reasons, a transmitting sublayer may use a larger value with a resulting decrease in its throughput. The larger value is determined by the parameters of the implementation, see 4.4.

4.2.3.2.3 Collision handling (half duplex mode only)

Once a CSMA/CD sublayer has finished deferring and has started transmission, it is still possible for it to experience contention for the medium. Collisions can occur until acquisition of the network has been accomplished through the deference of all other stations' CSMA/CD sublayers.

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The dynamics of collision handling are largely determined by a single parameter called the slot time. This single parameter describes three important aspects of collision handling:

a) It is an upper bound on the acquisition time of the medium.
b) It is an upper bound on the length of a frame fragment generated by a collision.
c) It is the scheduling quantum for retransmission.

To fulfill all three functions, the slot time shall be larger than the sum of the Physical Layer round-trip propagation time and the Media Access Layer maximum jam time. The slot time is determined by the parameters of the implementation, see 4.4.

4.2.3.2.4 Collision detection and enforcement (half duplex mode only)

Collisions are detected by monitoring the collisionDetect signal provided by the Physical Layer. When a collision is detected during a frame transmission, the transmission is not terminated immediately. Instead, the transmission continues until additional bits specified by jamSize have been transmitted (counting from the time collisionDetect went on). This collision enforcement or jam guarantees that the duration of the collision is sufficient to ensure its detection by all transmitting stations on the network. The content of the jam is unspecified; it may be any fixed or variable pattern convenient to the Media Access implementation; however, the implementation shall not be intentionally designed to be the 32-bit CRC value corresponding to the (partial) frame transmitted prior to the jam.

4.2.3.2.5 Collision backoff and retransmission (half duplex mode only)

When a transmission attempt has terminated due to a collision, it is retried by the transmitting CSMA/CD sublayer until either it is successful or a maximum number of attempts (attemptLimit) have been made and all have terminated due to collisions. Note that all attempts to transmit a given frame are completed before any subsequent outgoing frames are transmitted. The scheduling of the retransmissions is determined by a controlled randomization process called “truncated binary exponential backoff.” At the end of enforcing a collision (jamming), the CSMA/CD sublayer delays before attempting to retransmit the frame. The delay is an integer multiple of slotTime. The number of slot times to delay before the nth retransmission attempt is chosen as a uniformly distributed random integer r in the range:

$$0 \le r < 2^k$$

where

$$k = \min(n, 10)$$

If all attemptLimit attempts fail, this event is reported as an error. Algorithms used to generate the integer r should be designed to minimize the correlation between the numbers generated by any two stations at any given time.

Note that the values given above define the most aggressive behavior that a station may exhibit in attempting to retransmit after a collision. In the course of implementing the retransmission scheduling procedure, a station may introduce extra delays that will degrade its own throughput, but in no case may a station’s retransmission scheduling result in a lower average delay between retransmission attempts than the procedure defined above.

4.2.3.2.6 Full duplex transmission

In full duplex mode, there is never contention for a shared physical medium. The Physical Layer may indicate to the MAC that there are simultaneous transmissions by both stations, but since these transmissions do

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not interfere with each other, a MAC operating in full duplex mode must not react to such Physical Layer indications. Full duplex stations do not defer to received traffic, nor abort transmission, jam, backoff, and reschedule transmissions as part of Transmit Media Access Management. Transmissions may be initiated whenever the station has a frame queued, subject only to the interframe spacing required to allow recovery for other sublayers and for the physical medium.

4.2.3.2.7 Frame bursting (half duplex mode only)

At operating speeds above 100 Mb/s, an implementation may optionally transmit a series of frames without relinquishing control of the transmission medium. This mode of operation is referred to as *burst mode*. Once a frame has been successfully transmitted, the transmitting station can begin transmission of another frame without contending for the medium because all of the other stations on the network will continue to defer to its transmission, provided that it does not allow the medium to assume an idle condition between frames. The transmitting station fills the interframe spacing interval with extension bits, which are readily distinguished from data bits at the receiving stations, and which maintain the detection of carrier in the receiving stations. The transmitting station is allowed to initiate frame transmission until a specified limit, referred to as burstLimit, is reached. The value of burstLimit is specified in 4.4.2.4. Figure 4–1 shows an example of transmission with frame bursting.

The first frame of a burst will be extended, if necessary, as described in 4.2.3.4. Subsequent frames within a burst do not require extension. In a properly configured network, and in the absence of errors, collisions cannot occur during a burst at any time after the first frame of a burst (including any extension) has been transmitted. Therefore, the MAC will treat any collision that occurs after the first frame of a burst, or that occurs after the slotTime has been reached in the first frame of a burst, as a late collision.

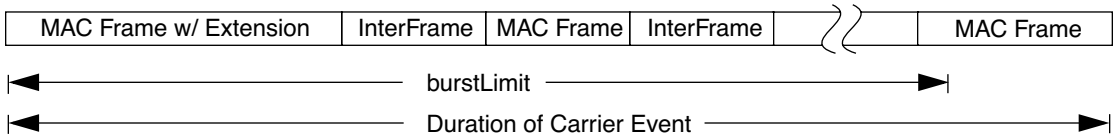


Figure 4–1—Frame bursting

4.2.3.3 Minimum frame size

The CSMA/CD Media Access mechanism requires that a minimum frame length of minFrameSize bits be transmitted. If frameSize is less than minFrameSize, then the CSMA/CD MAC sublayer shall append extra bits in units of octets, after the end of the MAC client data field but prior to calculating, and appending, the FCS. The number of extra bits shall be sufficient to ensure that the frame, from the DA field through the FCS field inclusive, is at least minFrameSize bits. The content of the pad is unspecified.

4.2.3.4 Carrier extension (half duplex mode only)

At operating speeds above 100 Mb/s, the slotTime employed at slower speeds is inadequate to accommodate network topologies of the desired physical extent. Carrier Extension provides a means by which the slotTime can be increased to a sufficient value for the desired topologies, without increasing the minFrameSize parameter, as this would have deleterious effects. Nondata bits, referred to as extension bits, are appended to frames that are less than slotTime bits in length so that the resulting transmission is at least one slotTime in duration. Carrier Extension can be performed only if the underlying physical layer is capable of sending and receiving symbols that are readily distinguished from data symbols, as is the case in most physical layers that use a block encoding/decoding scheme. The maximum length of the extension is equal to the quantity (slotTime − minFrameSize). Figure 4–2 depicts a frame with carrier extension.

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The MAC continues to monitor the medium for collisions while it is transmitting extension bits, and it will treat any collision that occurs after the threshold (slotTime) as a late collision.

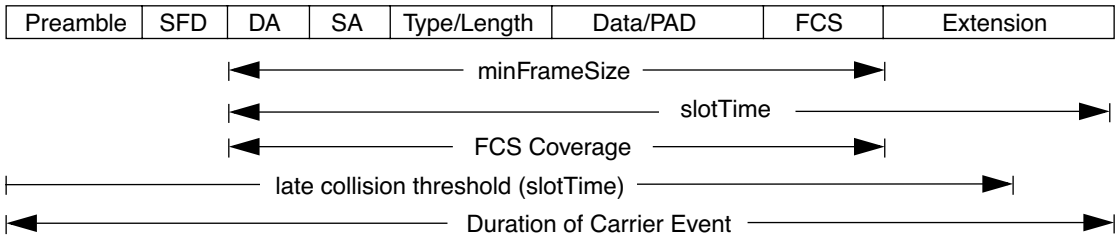


Figure 4–2—Frame with carrier extension

4.2.4 Frame reception model

CSMA/CD MAC sublayer frame reception includes both data decapsulation and Media Access management aspects:

a) Receive Data Decapsulation comprises address recognition, frame check sequence validation, and frame disassembly to pass the fields of the received frame to the MAC client.

b) Receive Media Access Management comprises recognition of collision fragments from incoming frames and truncation of frames to octet boundaries.

4.2.4.1 Receive data decapsulation

4.2.4.1.1 Address recognition

The CSMA/CD MAC sublayer is capable of recognizing individual and group addresses.

a) *Individual Addresses*. The CSMA/CD MAC sublayer recognizes and accepts any frame whose DA field contains the individual address of the station.

b) *Group Addresses*. The CSMA/CD MAC sublayer recognizes and accepts any frame whose DA field contains the Broadcast address.

The CSMA/CD MAC sublayer is capable of activating some number of group addresses as specified by higher layers. The CSMA/CD MAC sublayer recognizes and accepts any frame whose Destination Address field contains an active group address. An active group address may be deactivated.

4.2.4.1.2 Frame check sequence validation

FCS validation is essentially identical to FCS generation. If the bits of the incoming frame (exclusive of the FCS field itself) do not generate a CRC value identical to the one received, an error has occurred and the frame is identified as invalid.

4.2.4.1.3 Frame disassembly

Upon recognition of the Start Frame Delimiter at the end of the preamble sequence, the CSMA/CD MAC sublayer accepts the frame. If there are no errors, the frame is disassembled and the fields are passed to the MAC client by way of the output parameters of the ReceiveFrame operation.

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4.2.4.2 Receive media access management

4.2.4.2.1 Framing

The CSMA/CD sublayer recognizes the boundaries of an incoming frame by monitoring the receiveDataValid signal provided by the Physical Layer. Two possible length errors can occur that indicate ill-framed data: the frame may be too long, or its length may not be an integer number of octets.

a) *Maximum Frame Size*. The receiving CSMA/CD sublayer is not required to enforce the frame size limit, but it is allowed to truncate frames longer than maxUntaggedFrameSize octets and report this event as an (implementation-dependent) error. A receiving CSMA/CD sublayer that supports tagged MAC frames (see 3.5) may similarly truncate frames longer than (maxUntaggedFrameSize + qTagPrefixSize) octets in length, and report this event as an (implementation-dependent) error.

b) *Integer Number of Octets in Frame*. Since the format of a valid frame specifies an integer number of octets, only a collision or an error can produce a frame with a length that is not an integer multiple of 8 bits. Complete frames (that is, not rejected as collision fragments; see 4.2.4.2.2) that do not contain an integer number of octets are truncated to the nearest octet boundary. If frame check sequence validation detects an error in such a frame, the status code alignmentError is reported.

When a burst of frames is received while operating in half duplex mode at speeds above 100 Mb/s, the individual frames within the burst are delimited by sequences of interframe fill symbols, which are conveyed to the receiving MAC sublayer as extension bits. Once the collision filtering requirements for a given frame, as described in 4.2.4.2.2, have been satisfied, the receipt of an extension bit can be used as an indication that all of the data bits of the frame have been received.

4.2.4.2.2 Collision filtering

In the absence of a collision, the shortest valid transmission in half duplex mode must be at least one slotTime in length. Within a burst of frames, the first frame of a burst must be at least slotTime bits in length in order to be accepted by the receiver, while subsequent frames within a burst must be at least minFrameSize in length. Anything less is presumed to be a fragment resulting from a collision, and is discarded by the receiver. In half duplex mode, occasional collisions are a normal part of the Media Access management procedure. The discarding of such a fragment by a MAC is not reported as an error.

The shortest valid transmission in full duplex mode must be at least minFrameSize in length. While collisions do not occur in full duplex mode MACs, a full duplex MAC nevertheless discards received frames containing less than minFrameSize bits. The discarding of such a frame by a MAC is not reported as an error.

4.2.5 Preamble generation

In a LAN implementation, most of the Physical Layer components are allowed to provide valid output some number of bit times after being presented valid input signals. Thus it is necessary for a preamble to be sent before the start of data, to allow the PLS circuitry to reach its steady state. Upon request by TransmitLinkMgmt to transmit the first bit of a new frame, PhysicalSignalEncap shall first transmit the preamble, a bit sequence used for physical medium stabilization and synchronization, followed by the Start Frame Delimiter. If, while transmitting the preamble or Start Frame Delimiter, the collision detect variable becomes true, any remaining preamble and Start Frame Delimiter bits shall be sent. The preamble pattern is:

10101010 10101010 10101010 10101010 10101010 10101010 10101010

The bits are transmitted in order, from left to right. The nature of the pattern is such that, for Manchester encoding, it appears as a periodic waveform on the medium that enables bit synchronization. It should be noted that the preamble ends with a “0.”

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4.2.6 Start frame sequence

The receiveDataValid signal is the indication to the MAC that the frame reception process should begin. Upon reception of the sequence 10101011 following the assertion of receiveDataValid, PhysicalSignalDecap shall begin passing successive bits to ReceiveLinkMgmt for passing to the MAC client.

4.2.7 Global declarations

This subclause provides detailed formal specifications for the CSMA/CD MAC sublayer. It is a specification of generic features and parameters to be used in systems implementing this media access method. Subclause 4.4 provides values for these sets of parameters for recommended implementations of this media access mechanism.

4.2.7.1 Common constants, types, and variables

The following declarations of constants, types and variables are used by the frame transmission and reception sections of each CSMA/CD sublayer:

```
const
   addressSize = ... ; {48 bits in compliance with 3.2.3}
   lengthOrTypeSize = 16; {in bits}
   clientDataSize = ...; {in bits, MAC client Data, see 4.2.2.2, (1)(c)}
   padSize = ...; {in bits, = max (0, minFrameSize — (2 x addressSize
                + lengthOrTypeSize + clientDataSize + crcSize))}
   dataSize = ...; {in bits, = clientDataSize + padSize}
   crcSize = 32;   {32 bit CRC = 4 octets}
   frameSize = ...; {in bits, = 2 x addressSize + lengthOrTypeSize + dataSize + crcSize, see 4.2.2.2, (1)}
   minFrameSize = ... ;   {in bits, implementation-dependent, see 4.4}
   maxUntaggedFrameSize = ... ;   {in octets, implementation-dependent, see 4.4}
   qTagPrefixSize = 4; {in octets, length of QTag Prefix, see 3.5}
   extend = ...; {Boolean, true if (slotTime — minFrameSize) > 0, false otherwise}
   extensionBit = ...; {a nondata value which is used for carrier extension and interframe during bursts}
   extensionErrorBit = ...; {a nondata value which is used to jam during carrier extension}
   minTypeValue = 1536; {minimum value of the Length/Type field for Type interpretation}
   maxValidFrame = maxUntaggedFrameSize — (2 x addressSize + lengthOrTypeSize + crcSize) / 8;
                {in octets, the maximum length of the MAC client data field. This constant
                is defined for editorial convenience, as a function of other constants}
   slotTime = ... ; {unit of time for collision handling, implementation-dependent, see 4.4}
   preambleSize = ...; {56 bits, see 4.2.5}
   sfdSize = 8; {8 bit start frame delimiter}
   headerSize = ...; {64 bits, sum of preambleSize and sfdSize}
type
   Bit = 0..1;
   PhysicalBit = 0,1, extensionBit, extensionErrorBit; {bits transmitted to the Physical
                Layer can be either 0, 1, extensionBit or extensionErrorBit.
                Bits received from the Physical Layer can be either 0, 1 or extensionBit.}
   AddressValue = array [1..addressSize] of Bit;
   LengthOrTypeValue = array [1..lengthOrTypeSize] of Bit;
   DataValue = array [1..dataSize] of Bit;
   CRCValue = array [1..crcSize] of Bit;
   PreambleValue = array [1..preambleSize] of Bit;
   SfdValue = array [1..sfdSize] of Bit;
   ViewPoint = (fields, bits); {Two ways to view the contents of a frame}
```


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```
    HeaderViewPoint = (headerFields, headerBits);
    Frame = record {Format of Media Access frame}
      case view: ViewPoint of
        fields: (
          destinationField: AddressValue;
          sourceField: AddressValue;
          lengthOrTypeField: LengthOrTypeValue;
          dataField: DataValue;
          fcsField: CRCValue);
        bits: (contents: array [1..frameSize] of Bit)
      end; {Frame}

    Header = record {Format of preamble and start frame delimiter}
      case headerView : HeaderViewPoint of
        headerFields : (
          preamble : PreambleValue;
          sfd : SfdValue);
        headerBits : (
          headerContents : array [1..headerSize] of Bit)
      end; {defines header for MAC frame}
  var
    halfDuplex: Boolean; {Indicates the desired mode. halfDuplex is a static variable; its value does
                          not change between invocations of the Initialize procedure}
```

4.2.7.2 Transmit state variables

The following items are specific to frame transmission. (See also 4.4.)

```
  const
    interFrameSpacing = ... ; {minimum time between frames. Equal to interFrameGap, see 4.4}
    interFrameSpacingPart1 = ... ; {duration of first portion of interFrameSpacing. In range 0
                                    up to 2/3 interFrameSpacing}
    interFrameSpacingPart2 = ... ; {duration of remainder of interFrameSpacing. Equal to
                                    interFrameSpacing − interFrameSpacingPart1}
    interFrameSize = ... ; {in bits, length of interframe fill during a burst. Equal to interFrameGap
                                    divided by the bit period}
    attemptLimit = ... ; {Max number of times to attempt transmission}
    backOffLimit = ... ; {Limit on number of times to back off}
    burstLimit= ... ; {in bits: Limit for initiation of frame transmission in Burst Mode,
                                    implementation dependent, see 4.4}
    jamSize = ... ; {in bits: the value depends upon medium and collision detect implementation}
  var
    outgoingFrame: Frame; {The frame to be transmitted}
    outgoingHeader: Header;
    currentTransmitBit, lastTransmitBit: 1..frameSize;
                          {Positions of current and last outgoing bits in outgoingFrame}
    lastHeaderBit: 1..headerSize;
    deferring: Boolean; {Implies any pending transmission must wait for the medium to clear}
    frameWaiting: Boolean; {Indicates that outgoingFrame is deferring}
    attempts: 0..attemptLimit; {Number of transmission attempts on outgoingFrame}
    newCollision: Boolean; {Indicates that a collision has occurred but has not yet been jammed}
    transmitSucceeding: Boolean; {Running indicator of whether transmission is succeeding}
```

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wasTransmitting: Boolean; {Indicates transmission in progress or just completed}
burstMode: Boolean: {Indicates the desired mode of operation, and enables the transmission of multiple frames in a single carrier event. burstMode is a static variable; its value does not change between invocations of the Initialize procedure.}
bursting: Boolean; {In burstMode, the given station has acquired the medium and the burst timer has not yet expired}
burstStart: Boolean; {In burstMode, indicates that the first frame transmission is in progress}
extendError: Boolean; {Indicates a collision occurred while sending extension bits}

4.2.7.3 Receive state variables

The following items are specific to frame reception. (See also 4.4.)

var
incomingFrame: Frame; {The frame being received}
receiving: Boolean; {Indicates that a frame reception is in progress}
excessBits: 0..7; {Count of excess trailing bits beyond octet boundary}
receiveSucceeding: Boolean; {Running indicator of whether reception is succeeding}
validLength: Boolean; {Indicator of whether received frame has a length error}
exceedsMaxLength: Boolean; {Indicator of whether received frame has a length longer than the maximum permitted length}
extending: Boolean; {Indicates whether the current frame is subject to carrier extension}
extensionOK: Boolean; {Indicates whether any bit errors were found in the extension part of a frame, which is not checked by the CRC}

4.2.7.4 Summary of interlayer interfaces

a) The interface to the MAC client, defined in 4.3.2, is summarized below:

type
‡ TransmitStatus = (transmitDisabled, transmitOK, excessiveCollisionError, lateCollisionErrorStatus); {Result of TransmitFrame operation, reporting of lateCollisionErrorStatus is optional for MACs operating at speeds at or below 100 Mb/s}
‡ ReceiveStatus = (receiveDisabled, receiveOK, frameTooLong, frameCheckError, lengthError, alignmentError); {Result of ReceiveFrame operation}
function TransmitFrame (
destinationParam: AddressValue;
sourceParam: AddressValue;
lengthOrTypeParam: LengthOrTypeValue;
dataParam: DataValue): TransmitStatus; {Transmits one frame}
function ReceiveFrame (
var destinationParam: AddressValue;
var sourceParam: AddressValue;
var lengthOrTypeParam: LengthOrTypeValue;
var dataParam: DataValue): ReceiveStatus; {Receives one frame}

b) The interface to the Physical Layer, defined in 4.3.3, is summarized in the following:

var
receiveDataValid: Boolean; {Indicates incoming bits}
carrierSense: Boolean; {In half duplex mode, indicates that transmissions should defer}
transmitting: Boolean; {Indicates outgoing bits}
collisionDetect: Boolean; {Indicates medium contention}
procedure TransmitBit (bitParam: PhysicalBit); {Transmits one bit}
function ReceiveBit: PhysicalBit; {Receives one bit}

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procedure Wait (bitTimes: integer); {Waits for indicated number of bit-times}

4.2.7.5 State variable initialization

The procedure Initialize must be run when the MAC sublayer begins operation, before any of the processes begin execution. Initialize sets certain crucial shared state variables to their initial values. (All other global variables are appropriately reinitialized before each use.) Initialize then waits for the medium to be idle, and starts operation of the various processes.

NOTE—Care should be taken to ensure that the time from the completion of the Initialize process to when the first packet transmission begins is at least an interFrameGap.

If Layer Management is implemented, the Initialize procedure shall only be called as the result of the initializeMAC action (30.3.1.2.1).

```
procedure Initialize;
begin
   frameWaiting := false;
   deferring := false;
   newCollision := false;
   transmitting := false; {In interface to Physical Layer; see below}
   receiving := false;
   halfDuplex := ...; {true for half duplex operation, false for full duplex operation. halfDuplex is a
                       static variable; its value does not change between invocations of the Initialize
                       procedure}
   bursting := false;
   burstMode := ...; { true for half duplex operation at speeds above 100 Mb/s when multiple frames'
                       transmission in a single carrier event is desired, false otherwise. burstMode
                       is a static variable; its value does not change between invocations of the
                       Initialize procedure.}
   extending := extend and halfDuplex;
   while carrierSense or receiveDataValid do nothing
   {Start execution of all processes}
end; {Initialize}
```

4.2.8 Frame transmission

The algorithms in this subclause define MAC sublayer frame transmission. The function TransmitFrame implements the frame transmission operation provided to the MAC client:

```
function TransmitFrame (
      destinationParam: AddressValue;
      sourceParam: AddressValue;
      lengthOrTypeParam: LengthOrTypeValue;
      dataParam: DataValue): TransmitStatus;
procedure TransmitDataEncap; ... {nested procedure; see body below}
begin
      if transmitEnabled then
      begin
            TransmitDataEncap;
            TransmitFrame := TransmitLinkMgmt
      end
      else TransmitFrame := transmitDisabled
```

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```
    end; {TransmitFrame}
```

If transmission is enabled, TransmitFrame calls the internal procedure TransmitDataEncap to construct the frame. Next, TransmitLinkMgmt is called to perform the actual transmission. The TransmitStatus returned indicates the success or failure of the transmission attempt.

TransmitDataEncap builds the frame and places the 32-bit CRC in the frame check sequence field:

```
    procedure TransmitDataEncap;
    begin
        with outgoingFrame do
        begin {assemble frame}
            view := fields;
            destinationField := destinationParam;
            sourceField := sourceParam;
            lengthOrTypeField := lengthOrTypeParam;
            dataField := ComputePad (dataParam);
            fcsField := CRC32(outgoingFrame);
            view := bits
        end {assemble frame}
        with outgoingHeader do
        begin
            headerView := headerFields;
            preamble := ...; {* '1010...10,' LSB to MSB*}
            sfd := ...; {* '10101011,' LSB to MSB*}
            headerView := headerBits
        end
    end; {TransmitDataEncap}
```

ComputePad appends an array of arbitrary bits to the MAC client data to pad the frame to the minimum frame size.

```
    function ComputePad(
        var dataParam: DataValue): DataValue;
    begin
        ComputePad := {Append an array of size padSize of arbitrary bits to the MAC client dataField}
    end;{ComputePadParam}
```

TransmitLinkMgmt attempts to transmit the frame. In half duplex mode, it first defers to any passing traffic. In half duplex mode, if a collision occurs, transmission is terminated properly and retransmission is scheduled following a suitable backoff interval:

```
function TransmitLinkMgmt: TransmitStatus;
begin
    attempts := 0;
    transmitSucceeding := false;
    lateCollisionCount := 0;
    deferred := false; {initialize}
    excessDefer := false;
    while  (attempts < attemptLimit) and (not transmitSucceeding)
       and (not extend or lateCollisionCount = 0) do
            {no retransmission after late collision if operating at > 100 Mb/s}
    begin {loop}
```


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```
        if bursting then {this is a burst continuation}
            frameWaiting := true {start transmission without checking deference}
        else {non bursting case, or first frame of a burst}
            begin
                if attempts>0 then BackOff;
                if halfDuplex then frameWaiting := true;
                while deferring do {defer to passing frame, if any[15]}
                    begin
                        nothing;
‡                       if halfDuplex then deferred := true
                    end;
                burstStart := true;
                if burstMode then bursting := true
            end;
        lateCollisionError := false;
        StartTransmit;
        if halfDuplex then
        begin
            frameWaiting := false;
            while transmitting do WatchForCollision;
            if lateCollisionError then
                lateCollisionCount := lateCollisionCount + 1;
            attempts := attempts + 1
        end {half duplex mode}
        else while transmitting do nothing {full duplex mode}
    end; {loop}
    LayerMgmtTransmitCounters; {update transmit and transmit error counters in 5.2.4.2}
    if transmitSucceeding then
    begin
        if burstMode then burstStart := false; {Can't be the first frame anymore}
        TransmitLinkMgmt := transmitOK
    end
    else if (extend and lateCollisionCount > 0) then
        TransmitLinkMgmt := lateCollisionErrorStatus;
        else  TransmitLinkMgmt := excessiveCollisionError
end;{TransmitLinkMgmt}
```

Each time a frame transmission attempt is initiated, StartTransmit is called to alert the BitTransmitter process that bit transmission should begin:

```
    procedure StartTransmit;
    begin
        currentTransmitBit := 1;
        lastTransmitBit := frameSize;
        transmitSucceeding := true;
        transmitting := true;
        lastHeaderBit: = headerSize
    end; {StartTransmit}
```

In half duplex mode, TransmitLinkMgmt monitors the medium for contention by repeatedly calling WatchForCollision, once frame transmission has been initiated:

[15] The Deference process ensures that the reception of traffic does not cause deferring to be true when in full duplex mode. Deferring is used in full duplex mode to enforce the minimum interpacket gap spacing.

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```
procedure WatchForCollision;
begin
   if transmitSucceeding and collisionDetect then
   begin
      if currentTransmitBit > (slotTime − headerSize) then
         lateCollisionError := true;
      newCollision := true;
      transmitSucceeding := false;
      if burstMode then
      begin
         bursting := false;
         if not burstStart then
            lateCollisionError := true {Every collision is late, unless it hits the first frame in a burst}
      end
   end
end; {WatchForCollision}
```

WatchForCollision, upon detecting a collision, updates newCollision to ensure proper jamming by the BitTransmitter process. The current transmit bit number is checked to see if this is a late collision. If the collision occurs later than a collision window of slotTime bits into the packet, it is considered as evidence of a late collision. The point at which the collision is received is determined by the network media propagation time and the delay time through a station and, as such, is implementation-dependent (see 4.1.2.2). While operating at speeds of 100 Mb/s or lower, an implementation may optionally elect to end retransmission attempts after a late collision is detected. While operating at speeds above 100 Mb/s, an implementation shall end retransmission attempts after a late collision is detected.

After transmission of the jam has been completed, if TransmitLinkMgmt determines that another attempt should be made, BackOff is called to schedule the next attempt to retransmit the frame.

```
function Random (low, high: integer): integer;
begin
   Random := ...{uniformly distributed random integer r such that low ≤ r < high
end; {Random}
```

BackOff performs the truncated binary exponential backoff computation and then waits for the selected multiple of the slot time.

```
var maxBackOff: 2..1024; {Working variable of BackOff}
procedure BackOff;
begin
   if attempts = 1 then maxBackOff := 2
   else if attempts ≤ backOffLimit then maxBackOff := maxBackOff x 2;
   Wait(slotTime × Random(0, maxBackOff))
end; {BackOff}
```

BurstTimer is a process that does nothing unless the bursting variable is true. When bursting is true, BurstTimer increments burstCounter until the burstLimit limit is reached, whereupon BurstTimer assigns the value false to bursting.

```
process BurstTimer;
   var burstCounter: integer;
begin
   cycle
```


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```
        while not bursting do nothing; {wait for a burst}
        burstCounter := 0;
        while bursting and (burstCounter < burstLimit) do
            begin
                Wait (1);
                burstCounter := burstCounter +1
            end;
        bursting := false
    end {burstMode cycle}
end; {BurstTimer}
```

The Deference process runs asynchronously to continuously compute the proper value for the variable deferring. In the case of half duplex burst mode, deferring remains true throughout the entire burst.

```
process Deference;
begin
    if halfDuplex then cycle{half duplex loop}
        while not carrierSense do nothing; {watch for carrier to appear}
        deferring := true;  {delay start of new transmissions}
        wasTransmitting:=transmitting;
        while carrierSense or transmitting do
            wasTransmitting: = wasTransmitting or transmitting;
        if wasTransmitting then
            begin
                StartRealTimeDelay; {time out first part interframe gap}
                while RealTimeDelay(interFrameSpacingPart1) do nothing
            end
        else
            begin
                StartRealTimeDelay;
                repeat
                while carrierSense do StartRealTimeDelay
                until not RealTimeDelay(interFrameSpacingPart1)
            end;
        StartRealTimeDelay; {time out second part interframe gap}
        while RealTimeDelay(interFrameSpacingPart2) do nothing;
        deferring: = false; {allow new transmissions to proceed}
        while frameWaiting do nothing {allow waiting transmission if any}
    end {half duplex loop}
    else cycle {full duplex loop}
        while not transmitting do nothing; {wait for the start of a transmission}
        deferring := true; {inhibit future transmissions}
        while transmitting do nothing; {wait for the end of the current transmission}
        StartRealTimeDelay; {time out an interframe gap}
        while RealTimeDelay(interFrameSpacing) do nothing;
        deferring := false {don't inhibit transmission}
    end {full duplex loop}
end; {Deference}

procedure StartRealTimeDelay
    begin
        {reset the realtime timer and start it timing}
    end; {StartRealTimeDelay}
```

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```
function RealTimeDelay (μsec:real): Boolean;
  begin
    {return the value true if the specified number of microseconds have
    not elapsed since the most recent invocation of StartRealTimeDelay,
    otherwise return the value false}
  end; {RealTimeDelay}
```

The BitTransmitter process runs asynchronously, transmitting bits at a rate determined by the Physical Layer's TransmitBit operation:

```
process BitTransmitter;
begin
  cycle {outer loop}
    if transmitting then
    begin {inner loop}
      extendError := false;
      PhysicalSignalEncap;  {Send preamble and start of frame delimiter}
      while transmitting do
      begin
        if (currentTransmitBit > lastTransmitBit) then TransmitBit(extensionBit)
        else
          if extendError then
            TransmitBit(extensionErrorBit) {jam in extension}
          else
            TransmitBit(outgoingFrame[currentTransmitBit]); {send next bit to Physical Layer}
        if newCollision then StartJam else NextBit
      end;
      if bursting then
      begin
        InterFrameSignal;
        if extendError then
          if transmitting then transmitting := false {TransmitFrame may have been
                                                      called during InterFrameSignal}
          else
            IncLargeCounter(lateCollision); {count late collisions which
                                             were missed by TransmitLinkMgmt}
            bursting := bursting and (frameWaiting or transmitting)
      end
    end {inner loop}
  end {outer loop}
end; {BitTransmitter}
```

The bits transmitted to the physical layer can take one of four values: data zero (0), data one (1), extensionBit (EXTEND), or extensionErrorBit (EXTEND_ERROR). The values extensionBit and extensionErrorBit are not transmitted between the first preamble bit of a frame and the last data bit of a frame under any circumstances. The BitTransmitter calls the procedure TransmitBit with bitParam = extensionBit only when it is necessary to perform carrier extension on a frame after all of the data bits of a frame have been transmitted. The BitTransmitter calls the procedure TransmitBit with bitParam = extensionErrorBit only when it is necessary to jam during carrier extension.

```
procedure PhysicalSignalEncap;
begin
  while currentTransmitBit ≤ lastHeaderBit do
```


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```
    begin
        TransmitBit(outgoingHeader[currentTransmitBit]); {transmit header one bit at a time}
        currentTransmitBit := currentTransmitBit + 1
    end;
    if newCollision then StartJam else
    currentTransmitBit := 1
end; {PhysicalSignalEncap}
```

The procedure InterFrameSignal fills the interframe interval between the frames of a burst with extensionBits. InterFrameSignal also monitors the variable collisionDetect during the interframe interval between the frames of a burst, and will end a burst if a collision occurs during the interframe interval. The procedural model is defined such that a MAC operating in burstMode will emit an extraneous sequence of interFrameSize extensionBits in the event that there are no additional frames ready for transmission after InterFrameSignal returns. Implementations may be able to avoid sending this extraneous sequence of extensionBits if they have access to information (such as the occupancy of a transmit queue) that is not assumed to be available to the procedural model.

```
procedure InterFrameSignal;
    var interFrameCount, interFrameTotal : integer;
begin
    interFrameCount := 0;
    interFrameTotal := interFrameSize;
    while interFrameCount < interFrameTotal do
    begin
        if not extendError then
            TransmitBit(extensionBit)
        else
            TransmitBit(extensionErrorBit);
        interFrameCount := interFrameCount + 1;
        if collisionDetect and not extendError then
        begin
            bursting := false;
            extendError := true;
            interFrameCount := 0;
            interFrameTotal := jamSize
        end
    end
end; {InterFrameSignal}

procedure NextBit;
begin
    currentTransmitBit := currentTransmitBit+1;
    if halfDuplex and burstStart and transmitSucceeding then {carrier extension may be required}
        transmitting := (currentTransmitBit ≤ max(lastTransmitBit, slotTime))
    else
        transmitting := (currentTransmitBit ≤ lastTransmitBit)
end; {NextBit}

procedure StartJam;
begin
    extendError := currentTransmitBit > lastTransmitBit;
    currentTransmitBit := 1;
    lastTransmitBit := jamSize;
    newCollision := false
```

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```
    end; {StartJam}
```

BitTransmitter, upon detecting a new collision, immediately enforces it by calling StartJam to initiate the transmission of the jam. The jam should contain a sufficient number of bits of arbitrary data so that it is assured that both communicating stations detect the collision. (StartJam uses the first set of bits of the frame up to jamSize, merely to simplify this program.)

4.2.9 Frame reception

The algorithms in this subclause define CSMA/CD Media Access sublayer frame reception.

The function ReceiveFrame implements the frame reception operation provided to the MAC client:

```
    function ReceiveFrame (
            var destinationParam: AddressValue;
            var sourceParam: AddressValue;
            var lengthOrTypeParam: LengthOrTypeValue;
            var dataParam: DataValue): ReceiveStatus;
        function ReceiveDataDecap: ReceiveStatus; ... {nested function; see body below}
    begin
        if receiveEnabled then
        repeat
            ReceiveLinkMgmt;
            ReceiveFrame := ReceiveDataDecap;
        until receiveSucceeding
        else
            ReceiveFrame := receiveDisabled
    end; {ReceiveFrame}
```

If enabled, ReceiveFrame calls ReceiveLinkMgmt to receive the next valid frame, and then calls the internal function ReceiveDataDecap to return the frame's fields to the MAC client if the frame's address indicates that it should do so. The returned ReceiveStatus indicates the presence or absence of detected transmission errors in the frame.

```
    function ReceiveDataDecap: ReceiveStatus;
‡       var status : ReceiveStatus; {holds receive status information}
    begin
‡       with incomingFrame do
‡       begin
‡           view := fields;
            receiveSucceeding := RecognizeAddress (incomingFrame, destinationField);
‡           receiveSucceeding := LayerMgmtRecognizeAddress (destinationField);
        if receiveSucceeding then
            begin {disassemble frame}
                destinationParam := destinationField;
                sourceParam := sourceField;
                lengthOrTypeParam: = lengthOrTypeField;
                dataParam := RemovePad (lengthOrTypeField, dataField);
                exceedsMaxLength := ...; {{Check to determine if receive frame size exceeds the maximum
                    permitted frame size. MAC implementations may use either maxUntaggedFrameSize or
                    (maxUntaggedFrameSize + qTagPrefixSize) for the maximum permitted frame size, either
                    as a constant or as a function of whether the frame being received is a basic or tagged frame
                    (see 3.2, 3.5). In implementations that treat this as a constant, it is recommended that the
                    larger value be used. The use of the smaller value in this case may result in valid tagged
```


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```
                frames exceeding the maximum permitted frame size.}
            if exceedsMaxLength then status := frameTooLong
            else
            if fcsField = CRC32 (incomingFrame) and extensionOK then
            begin
‡               if validLength then status: = receiveOK
‡               else status: = lengthError
            end
            else
            begin
‡               if excessBits = 0 or not extensionOK then status:= frameCheckError
‡               else status := alignmentError
            end;
‡           LayerMgmtReceiveCounters(status);
                {update receive and receive error counters in 5.2.4.3}
            view: = bits
        end {disassemble frame}
‡   end; {with incomingFrame}
‡   ReceiveDataDecap := status
end; {ReceiveDataDecap}

function RecognizeAddress (address: AddressValue): Boolean;
begin
    RecognizeAddress := ... {Returns true for the set of physical, broadcast,
                             and multicast-group addresses corresponding
                             to this station}
end;{RecognizeAddress}
```

The function RemovePad strips any padding that was generated to meet the minFrameSize constraint, if possible. Length checking is provided for Length interpretations of the Length/Type field. For Length/Type field values in the range between maxValidFrame and minTypeValue, the behavior of the RemovePad function is unspecified.

```
function RemovePad(
        var lengthOrTypeParam:LengthOrTypeValue; dataParam:DataValue):DataValue;
begin
        if lengthOrTypeParam ≥ minTypeValue then
        begin
            validLength:= true; {Don't perform length checking for Type field interpretations}
            RemovePad := dataParam
        end
        else
        begin
            if lengthOrTypeParam ≤ maxValidFrame then
            begin
                validLength := {For length interpretations of the Length/Type field, check to determine if
                                value represented by Length/Type field matches the received
                                clientDataSize};
                if validLength then
                    RemovePad:={truncate the dataParam (when present) to value represented by
                                lengthOrTypeParam (in octets) and return the result}
                else
                    RemovePad:=dataParam
            end
```

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```
        end
    end; {RemovePad}
```

ReceiveLinkMgmt attempts repeatedly to receive the bits of a frame, discarding any fragments from collisions by comparing them to the minimum valid frame size:

```
    procedure ReceiveLinkMgmt;
    begin
        repeat
            StartReceive;
            while receiving do nothing; {wait for frame to finish arriving}
            excessBits := frameSize mod 8;
            frameSize := frameSize − excessBits;{truncate to octet boundary}
            receiveSucceeding := receiveSucceeding and (frameSize ≥ minFrameSize)
                                        {reject collision fragments}
        until receiveSucceeding
    end; {ReceiveLinkMgmt}

    procedure StartReceive;
    begin
        receiveSucceeding := true;
        receiving := true
    end; {StartReceive}
```

The BitReceiver process runs asynchronously, receiving bits from the medium at the rate determined by the Physical Layer's ReceiveBit operation, partitioning them into frames, and optionally receiving them:

```
    process BitReceiver;
        var b : PhysicalBit;
            incomingFrameSize: integer; {count of all bits received in frame including extension}
            frameFinished: Boolean;
            enableBitReceiver: Boolean;
            currentReceiveBit: 1..frameSize; {Position of current bit in incomingFrame}
    begin
        cycle {outer loop}
            if receiveEnabled then
            begin {receive next frame from physical layer}
                currentReceiveBit := 1;
                incomingFrameSize := 0;
                frameFinished := false;
                enableBitReceiver := receiving;
                PhysicalSignalDecap; {Skip idle and extension, strip off preamble and sfd}
                if enableBitReceiver then extensionOK := true;
                while receiveDataValid and not frameFinished do
                 {inner loop to receive the rest of an incoming frame}
                begin
                        b := ReceiveBit; {next bit from physical medium}
                        incomingFrameSize := incomingFrameSize + 1;
                        if b=0 or b= 1 then {normal case}
                            if enableBitReceiver then {append to frame}
                            begin
                                if incomingFrameSize > currentReceiveBit then extensionOK := false;
                                        {Errors in the extension get mapped to data bits on input}
```


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```
                    incomingFrame[currentReceiveBit] := b;
                    currentReceiveBit := currentReceiveBit + 1
                end
            else {b must be an extensionBit}
                if not extending then frameFinished := true;
            if incomingFrameSize ≥ slotTime then extending := false
        end; {inner loop}
        if enableBitReceiver then
        begin
            frameSize := currentReceiveBit − 1;
            receiveSucceeding := not extending;
            receiving := false
        end
    end {enabled}
  end {outer loop}
end; {BitReceiver}
```

The bits received from the physical layer can take one of three values: data zero (0), data one (1), or extensionBit (EXTEND). The value extensionBit will not occur between the first preamble bit of a frame and the last data bit of a frame in normal circumstances. Extension bits are counted by the BitReceiver but are not appended to the incoming frame. The BitReceiver checks whether the bit received from the physical layer is a data bit or an extensionBit before appending it to the incoming frame. Thus, the array of bits in incomingFrame will only contain data bits. The underlying Reconciliation Sublayer maps incoming EXTEND_ERROR bits to normal data bits. Thus, the reception of additional data bits after the frame extension has started is an indication that the frame should be discarded.

```
procedure PhysicalSignalDecap;
begin
    {Receive one bit at a time from physical medium until a valid sfd is detected,
    discard bits and return.}
end; {PhysicalSignalDecap}
```

The process SetExtending controls the extending variable, which determines whether a received frame must be at least slotTime bits in length or merely minFrameSize bits in length to be considered valid by the BitReceiver. SetExtending sets the extending variable to true whenever receiveDataValid is de-asserted, while in half duplex mode at operating speeds above 100 Mb/s.

```
process SetExtending;
begin
  cycle {loop forever}
    while receiveDataValid do nothing;
    extending := extend and halfDuplex
  end {loop}
end; {SetExtending}
```

4.2.10 Common procedures

The function CRC32 is used by both the transmit and receive algorithms to generate a 32-bit CRC value:

```
function CRC32 (f: Frame): CRCValue;
begin
    CRC32 := {The 32-bit CRC}
end; {CRC32}
```

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Purely to enhance readability, the following procedure is also defined:

procedure nothing; *begin end;*

The idle state of a process (that is, while waiting for some event) is cast as repeated calls on this procedure.

4.3 Interfaces to/from adjacent layers

4.3.1 Overview

The purpose of this clause is to provide precise definitions of the interfaces between the architectural layers defined in Clause 1 in compliance with the Media Access Service Specification given in Clause 2. In addition, the services required from the physical medium are defined.

The notation used here is the Pascal language, in keeping with the procedural nature of the precise MAC sublayer specification (see 4.2). Each interface is described as a set of procedures or shared variables, or both, that collectively provide the only valid interactions between layers. The accompanying text describes the meaning of each procedure or variable and points out any implicit interactions among them.

Note that the description of the interfaces in Pascal is a notational technique, and in no way implies that they can or should be implemented in software. This point is discussed more fully in 4.2, that provides complete Pascal declarations for the data types used in the remainder of this clause. Note also that the synchronous (one frame at a time) nature of the frame transmission and reception operations is a property of the architectural interface between the MAC client and MAC sublayers, and need not be reflected in the implementation interface between a station and its sublayer.

4.3.2 Services provided by the MAC sublayer

The services provided to the MAC client by the MAC sublayer are transmission and reception of frames. The interface through which the MAC client uses the facilities of the MAC sublayer therefore consists of a pair of functions.

Functions:
TransmitFrame
ReceiveFrame

Each of these functions has the components of a frame as its parameters (input or output), and returns a status code as its result. Note that the service_class defined in 2.3.1 is ignored by CSMA/CD MAC.

The MAC client transmits a frame by invoking TransmitFrame:

function *TransmitFrame (*
destinationParam: AddressValue;
sourceParam: AddressValue;
lengthOrTypeParam: LengthOrTypeValue;
dataParam: DataValue): TransmitStatus;

The TransmitFrame operation is synchronous. Its duration is the entire attempt to transmit the frame; when the operation completes, transmission has either succeeded or failed, as indicated by the resulting status code:

type TransmitStatus = (transmitOK, excessiveCollisionError, lateCollisionErrorStatus);

‡ *type* TransmitStatus = (transmitDisabled, transmitOK, excessiveCollisionError,

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lateCollisionErrorStatus);

The transmitDisabled status code indicates that the transmitter is not enabled. Successful transmission is indicated by the status code transmitOK; the code excessiveCollisionError indicates that the transmission attempt was aborted due to excessive collisions, because of heavy traffic or a network failure. MACs operating at speeds above 100 Mb/s are required to report lateCollisionErrorStatus in response to a late collision; MACs operating at speeds of 100 Mb/s and below are not required to do so.

The MAC client accepts incoming frames by invoking ReceiveFrame:

function *ReceiveFrame (*
var destinationParam: AddressValue;
var sourceParam: AddressValue;
var lengthOrTypeParam: LengthOrTypeValue;
var dataParam: DataValue): ReceiveStatus;

The ReceiveFrame operation is synchronous. The operation does not complete until a frame has been received. The fields of the frame are delivered via the output parameters with a status code:

type ReceiveStatus = (receiveOK, lengthError, frameCheckError, alignmentError);

‡ *type* ReceiveStatus = (receiveDisabled, receiveOK, frameTooLong, frameCheckError, lengthError, alignmentError);

The receiveDisabled status indicates that the receiver is not enabled. Successful reception is indicated by the status code receiveOK. The frameTooLong error indicates that a frame was received whose frameSize was beyond the maximum allowable frame size. The code frameCheckError indicates that the frame received was damaged by a transmission error. The lengthError indicates the lengthOrTypeParam value was both consistent with a length interpretation of this field (i.e., its value was less than or equal to maxValidFrame), and inconsistent with the frameSize of the received frame. The code alignmentError indicates that the frame received was damaged, and that in addition, its length was not an integer number of octets.

Note that maxValidFrame represents the maximum number of octets that can be carried in the MAC Client Data field of a frame and is a constant, regardless of whether the frame is a basic or tagged frame (see 3.2 and 3.5). The maximum length of a frame (including all fields from the Destination address through the FCS, inclusive) is either maxUntaggedFrameSize (for basic frames) or (maxUntaggedFrameSize + qTagPrefixSize), for tagged frames.

4.3.3 Services required from the physical layer

The interface through which the CSMA/CD MAC sublayer uses the facilities of the Physical Layer consists of a function, a pair of procedures and four Boolean variables:

Function	Procedures	Variables
ReceiveBit	TransmitBit	collisionDetect
	Wait	carrierSense
		receiveDataValid
		transmitting

During transmission, the contents of an outgoing frame are passed from the MAC sublayer to the Physical Layer by way of repeated use of the TransmitBit operation:

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procedure TransmitBit (bitParam: PhysicalBit);

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Each invocation of TransmitBit passes one new bit of the outgoing frame to the Physical Layer. The TransmitBit operation is synchronous. The duration of the operation is the entire transmission of the bit. The operation completes, when the Physical Layer is ready to accept the next bit and it transfers control to the MAC sublayer.

The overall event of data being transmitted is signaled to the Physical Layer by way of the variable transmitting:

var transmitting: Boolean*;*

Before sending the first bit of a frame, the MAC sublayer sets transmitting to true, to inform the Physical Media Access that a stream of bits will be presented via the TransmitBit operation. After the last bit of the frame has been presented, the MAC sublayer sets transmitting to false to indicate the end of the frame.

The presence of a collision in the physical medium is signaled to the MAC sublayer by the variable collisionDetect:

var collisionDetect: Boolean*;*

The collisionDetect signal remains true during the duration of the collision.

NOTE—In full duplex mode, collision indications may still be generated by the Physical Layer; however, they are ignored by the full duplex MAC.

The collisionDetect signal is generated only during transmission and is never true at any other time; in particular, it cannot be used during frame reception to detect collisions between overlapping transmissions from two or more other stations.

During reception, the contents of an incoming frame are retrieved from the Physical Layer by the MAC sublayer via repeated use of the ReceiveBit operation:

function ReceiveBit: PhysicalBit;

Each invocation of ReceiveBit retrieves one new bit of the incoming frame from the Physical Layer. The ReceiveBit operation is synchronous. Its duration is the entire reception of a single bit. Upon receiving a bit, the MAC sublayer shall immediately request the next bit until all bits of the frame have been received. (See 4.2 for details.)

The overall event of data being received is signaled to the MAC sublayer by the variable receiveDataValid:

var receiveDataValid: Boolean*;*

When the Physical Layer sets receiveDataValid to true, the MAC sublayer shall immediately begin retrieving the incoming bits by the ReceiveBit operation. When receiveDataValid subsequently becomes false, the MAC sublayer can begin processing the received bits as a completed frame. If an invocation of ReceiveBit is pending when receiveDataValid becomes false, ReceiveBit returns an undefined value, which should be discarded by the MAC sublayer. (See 4.2 for details.)

NOTE—When a burst of frames is received in half duplex mode at operating speeds above 100 Mb/s, the variable receiveDataValid will remain true throughout the burst. Furthermore, the variable receiveDataValid remains true throughout the extension field. In these respects, the behavior of the variable receiveDataValid is different from the underlying GMII signal RX_DV, from which it may be derived. See 35.2.1.7.

The overall event of activity on the physical medium is signaled to the MAC sublayer by the variable carrierSense:

var carrierSense: Boolean*;*

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In half duplex mode, the MAC sublayer shall monitor the value of carrierSense to defer its own transmissions when the medium is busy. The Physical Layer sets carrierSense to true immediately upon detection of activity on the physical medium. After the activity on the physical medium ceases, carrierSense is set to false. Note that the true/false transitions of carrierSense are not defined to be precisely synchronized with the beginning and the end of the frame, but may precede the beginning and lag the end, respectively. (See 4.2 for details.) In full duplex mode, carrierSense is undefined.

The Physical Layer also provides the procedure Wait:

procedure Wait (bitTimes: integer)*;*

This procedure waits for the specified number of bit times. This allows the MAC sublayer to measure time intervals in units of the (physical-medium-dependent) bit time.

Another important property of the Physical Layer, which is an implicit part of the interface presented to the MAC sublayer, is the round-trip propagation time of the physical medium. Its value represents the maximum time required for a signal to propagate from one end of the network to the other, and for a collision to propagate back. The round-trip propagation time is primarily (but not entirely) a function of the physical size of the network. The round-trip propagation time of the Physical Layer is defined in 4.4 for a selection of physical media.

4.4 Specific implementations

4.4.1 Compatibility overview

To provide total compatibility at all levels of the standard, it is required that each network component implementing the CSMA/CD MAC sublayer procedure adheres rigidly to these specifications. The information provided in 4.4.2 provides design parameters for specific implementations of this access method. Variations from these values result in a system implementation that violates the standard.

A DTE shall be capable of operating in half duplex mode, full duplex mode, or both. In any given instantiation of a network conforming to this standard, all stations shall be configured to use the same mode of operation, either half duplex or full duplex.

All DTEs connected to a repeater or a mixing segment shall be configured to use the half duplex mode of operation. When a pair of DTEs are connected to each other with a link segment, both devices shall be configured to use the same mode of operation, either half duplex or full duplex.

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4.4.2 Allowable implementations

4.4.2.1 Parameterized values

The following table identifies the parameter values that shall be used in the 10 Mb/s implementation of a CSMA/CD MAC procedure:

Parameters	Values
slotTime	512 bit times
interFrameGap	9.6 μs
attemptLimit	16
backoffLimit	10
jamSize	32 bits
maxUntaggedFrameSize	1518 octets
minFrameSize	512 bits (64 octets)
burstLimit	not applicable

NOTE—The spacing between two successive noncolliding packets, from start of idle at the end of the first packet to start of preamble of the subsequent packet, can have a minimum value of 47 bit times, at the AUI receive line of the DTE. This InterFrameGap shrinkage is caused by variable network delays, added preamble bits, and clock skew.

WARNING

Any deviation from the above values specified for a 10 Mb/s system may affect proper operation of the LAN.

4.4.2.2 Parameterized values

The following parameter values shall be used for 1BASE5 implementations:

Parameters	Values
slotTime	512 bit times
interFrameGap	96 μs
attemptLimit	16
backoffLimit	10
jamSize	32 bits
maxFrameSize	1518 octets
minFrameSize	512 bits (64 octets)
burstLimit	not applicable

See also DTE Deference Delay in 12.9.2.

WARNING

Any deviation from the specified values may affect proper operation of the network.

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4.4.2.3 Parameterized values

The following parameter values shall be used for 100 Mb/s implementations:

Parameters	Values
slotTime	512 bit times
interFrameGap	0.96 μs
attemptLimit	16
backoffLimit	10
jamSize	32 bits
maxUntaggedFrameSize	1518 octets
minFrameSize	512 bits (64 octets)
burstLimit	not applicable

WARNING

Any deviation from the above specified values may affect proper operation of the network.

4.4.2.4 Parameterized values

The following parameter values shall be used for 1000 Mb/s implementations:

Parameters	Values
slotTime	4096 bit times
interFrameGap	0.096 μs
attemptLimit	16
backoffLimit	10
jamSize	32 bits
maxUntaggedFrameSize	1518 octets
minFrameSize	512 bits (64 octets)
burstLimit	65 536 bits

NOTE—The spacing between two noncolliding packets, from the last bit of the FCS field of the first packet to the first bit of the preamble of the second packet, can have a minimum value of 64 BT (bit times), as measured at the GMII receive signals at the DTE. This InterFrameGap shrinkage may be caused by variable network delays, added preamble bits, and clock tolerances.

WARNING

Any deviation from the above specified values may affect proper operation of the network.

4.4.3 Configuration guidelines

The operational mode of the MAC may be determined either by the Auto-Negotiation functions specified in Clause 28 and Clause 37, or through manual configuration. When manual configuration is used, the devices on both ends of a link segment must be configured to matching modes to ensure proper operation. When Auto-Negotiation is used, the MAC must be configured to the mode determined by Auto-Negotiation before assuming normal operation.

NOTE—Improper configuration of duplex modes may result in improper network behavior.

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5. Layer Management

All parts of Clause 5, except for 5.2.4 and its subclauses, are deprecated by Clause 30.

5.1 Introduction

This clause provides the Layer Management specification for DTEs based on the CSMA/CD access method. It defines facilities comprised of a set of statistics and actions needed to provide Layer Management services. The information in this clause should be used in conjunction with the Procedural Model defined in 4.2.7–4.2.10. The Procedural Model provides a formal description of the relationship between the CSMA/CD Layer Entities and the Layer Management facilities.

This Layer Management specification has been developed in accordance with the OSI management architecture as specified in the ISO Management Framework document, ISO/IEC 7498-4: 1989. It is independent of any particular management application or management protocol.

The management facilities defined in this standard may be accessed both locally and remotely. Thus, the Layer Management specification provides facilities that can be accessed from within a station or can be accessed remotely by means of a peer management protocol operating between application entities. The encoding appropriate for use with ISO CMIP and ISO/IEC 15802-2: 1995 protocols can be found in Annex H.

In CSMA/CD no peer management facilities are necessary for initiating or terminating normal protocol operations or for handling abnormal protocol conditions. The monitoring of these activities is done by the carrier sense and collision detection mechanisms. Since these activities are necessary for normal operation of the protocol, they are not considered to be a function of Layer Management and are therefore not discussed in this clause.

Implementation of DTE Management is not a requirement for conformance to Clause 4 and Clause 7.

5.1.1 Systems Management overview

Within the ISO/IEC Open Systems Interconnection (OSI) architecture, the need to handle the special problems of initializing, terminating, and monitoring ongoing activities and assisting in their harmonious operations, as well as handling abnormal conditions, is recognized. These needs are collectively addressed by the systems management component of the OSI architecture.

A Management Protocol is required for the exchange of information between systems on a network. This Layer Management clause is independent of any particular Management Protocol.

This Layer Management clause, in conjunction with the Layer Management standards of other layers, provides the means to perform various management functions. Layer Management collects information needed from the MAC and Physical Layers. It also provides a means to exercise control over those layers.

The relationship between the various management entities and the layer entities according to the ISO model is shown in Figure 19–1.

5.1.2 Layer Management model

The Layer Management facilities provided by the CSMA/CD MAC and Physical Layer management definitions provide the ability to manipulate management counters and initiate actions within the layers.

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The managed objects within this standard are defined as sets of attributes, actions, notifications, and behaviors in accordance with IEEE Std 802-2001 and ISO/IEC International Standards for network management.

The precise semantics of the relationship between the CSMA/CD Layer Entities and the Layer Management facilities are defined in 4.2.7–4.2.10 and in 5.2.4.

5.1.3 Packages

This standard and ISO/IEC guidelines make provision for grouping attributes, operations and notifications in implementation groups or "packages" within each managed object class. DTE Management has two packages that are required for management at the minimum conformance configuration. The basic package is also useful for system configurations that wish to implement MAU Management without DTE Management. The packages for DTE Management are specified in Table 1.

5.1.4 Conformance requirements

Implementation of both the basic and the mandatory package of the MAC entity are the minimum requirements for claiming conformance to DTE Management.

5.2 Management facilities

5.2.1 Introduction

This subclause of the standard defines the Layer Management facilities for the ISO/IEC 8802-3 CSMA/CD MAC and Physical Layers. The intent of this subclause is to furnish a management specification that can be used by the wide variety of different DTE devices that may be attached to a network specified by this standard. Thus, a comprehensive list of management facilities is provided.

The improper use of some of the facilities described in this subclause may cause serious disruption of the network. In accordance with ISO management architecture, any necessary security provisions should be provided by the Agent in the Local System Environment. This can be in the form of specific security features or in the form of security features provided by the peer communication facilities.

All counters defined in this specification are assumed to be wraparound counters. Wraparound counters are those that automatically go from their maximum value (or final value) to zero and continue to operate. These unsigned counters do not provide for any explicit means to return them to their minimum (zero), i.e., reset. Because of their nature, wraparound counters should be read frequently enough to avoid loss of information.

5.2.2 DTE MAC Sublayer Management facilities

This subclause defines the Layer Management facilities specific to the MAC sublayer Managed Object Class. Note that with regard to reception-related error statistics, a hierarchical order has been established such that when multiple error statuses can be associated with one frame, only one status is returned to the LLC. This hierarchy in descending order is as follows:

frameTooLong

alignmentError

frameCheckError

lengthError

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The counters are primarily incremented based on the status returned to the LLC, and therefore the hierarchical order of the counters is determined by the order of the status. Frame fragments are not included in any of the statistics unless otherwise stated. In implementing any of the specified actions, receptions and transmissions that are in progress are completed before the action takes effect.

Table 5-1—Packages

			Basic Package (Mandatory)	Mandatory Package (Mandatory)	Recommended Package (Optional)	Optional Package (Optional)	Array Package (Optional)	Excessive Deferral Package (Optional)
oMAC-entity managed object class								
aMACID	ATTRIBUTE	GET	X					
aFramesTransmittedOK	ATTRIBUTE	GET		X				
aSingleCollisionFrames	ATTRIBUTE	GET		X				
aMultipleCollisionFrames	ATTRIBUTE	GET		X				
aFramesReceivedOK	ATTRIBUTE	GET		X				
aFrameCheckSequenceErrors	ATTRIBUTE	GET		X				
aAlignmentErrors	ATTRIBUTE	GET		X				
acInitializeMAC	ACTION		X					
aOctetsTransmittedOK	ATTRIBUTE	GET			X			
aFramesWithDeferredXmissions	ATTRIBUTE	GET			X			
aLateCollisions	ATTRIBUTE	GET			X			
aFramesAbortedDueToXSColls	ATTRIBUTE	GET			X			
aFramesLostDueToIntMACXmitError	ATTRIBUTE	GET			X			
aCarrierSenseErrors	ATTRIBUTE	GET			X			
aOctetsReceivedOK	ATTRIBUTE	GET			X			
aFramesLostDueToIntMACRcvError	ATTRIBUTE	GET			X			
aPromiscuousStatus	ATTRIBUTE	GET-SET			X			
aReadMulticastAddressList	ATTRIBUTE	GET			X			
acAddGroupAddress	ACTION				X			
acDeleteGroupAddress	ACTION				X			
aMulticastFramesXmittedOK	ATTRIBUTE	GET				X		
aBroadcastFramesXmittedOK	ATTRIBUTE	GET				X		
aFramesWithExcessiveDeferral	ATTRIBUTE	GET						X
aMulticastFramesReceivedOK	ATTRIBUTE	GET				X		
aBroadcastFramesReceivedOK	ATTRIBUTE	GET				X		
aInRangeLengthErrors	ATTRIBUTE	GET				X		
aOutOfRangeLengthField	ATTRIBUTE	GET				X		
aFrameTooLongErrors	ATTRIBUTE	GET				X		
aMACEnableStatus	ATTRIBUTE	GET-SET				X		
aTransmitEnableStatus	ATTRIBUTE	GET-SET				X		
aMulticastReceiveStatus	ATTRIBUTE	GET-SET				X		
aReadWriteMACAddress	ATTRIBUTE	GET-SET				X		
acExecuteSelfTest	ACTION					X		
aCollisionFrames	ATTRIBUTE	GET					X	
oResourceTypeID managed object class								
aResourceTypeIDName	ATTRIBUTE	GET	X					
aResourceInfo	ATTRIBUTE	GET	X					
oPHY-entity managed object class								
aPHYID	ATTRIBUTE	GET			X			
aSQETestErrors	ATTRIBUTE	GET			X			

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5.2.2.1 DTE MAC sublayer attributes

5.2.2.1.1 aMACID

ATTRIBUTE
APPROPRIATE SYNTAX:
INTEGER
BEHAVIOUR DEFINED AS:
The value of aMACID is assigned so as to uniquely identify a MAC among the subordinate managed objects of the containing object.

5.2.2.1.2 aFramesTransmittedOK

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are successfully transmitted. This counter is incremented when the TransmitStatus is reported as transmitOK. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.1.3 aSingleCollisionFrames

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 13 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are involved in a single collision and are subsequently transmitted successfully. This counter is incremented when the result of a transmission is reported as transmitOK and the attempt value is 2. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.1.4 aMultipleCollisionFrames

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 11 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are involved in more than one collision and are subsequently transmitted successfully. This counter is incremented when the TransmitStatus is reported as transmitOK and the value of the attempts variable is greater than 2 and less or equal to attemptLimit. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

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5.2.2.1.5 aFramesReceivedOK

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are successfully received (receiveOK). This does not include frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented when the ReceiveStatus is reported as receiveOK. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

5.2.2.1.6 aFrameCheckSequenceErrors

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are an integral number of octets in length and do not pass the FCS check. This counter is incremented when the ReceiveStatus is reported as frameCheckError. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

5.2.2.1.7 aAlignmentErrors

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are not an integral number of octets in length and do not pass the FCS check. This counter is incremented when the ReceiveStatus is reported as alignmentError. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

5.2.2.1.8 aOctetsTransmittedOK

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1 230 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of data and padding octets of frames that are successfully transmitted. This counter is incremented when the TransmitStatus is reported as transmitOK. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

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5.2.2.1.9 aFramesWithDeferredXmissions

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 13 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames whose transmission was delayed on its first attempt because the medium was busy. This counter is incremented when the boolean variable deferred has been asserted by the TransmitLinkMgmt function (4.2.8). Frames involved in any collisions are not counted. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.1.10 aLateCollisions

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of the times that a collision has been detected later than 512 bit times into the transmitted packet. A late collision is counted twice, i.e., both as a collision and as a lateCollision. This counter is incremented when the lateCollisionCount variable is nonzero. The actual update is incremented in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.1.11 aFramesAbortedDueToXSColls

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 3255 counts per second.
BEHAVIOUR DEFINED AS:
A count of the frames that due to excessive collisions are not transmitted successfully. This counter is incremented when the value of the attempts variable equals attemptLimit during a transmission. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.1.12 aFramesLostDueToIntMACXmitError

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that would otherwise be transmitted by the station, but could not be sent due to an internal MAC sublayer transmit error. If this counter is incremented, then none of the other counters in this subclause are incremented. The exact meaning and mechanism for incrementing this counter is implementation dependent.

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5.2.2.1.13 aCarrierSenseErrors

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of times that the carrierSense variable was not asserted or was deasserted during the transmission of a frame without collision (see 7.2.4.6). This counter is incremented when the carrierSenseFailure flag is true at the end of transmission. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.1.14 aOctetsReceivedOK

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1 230 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of data and padding octets in frames that are successfully received. This does not include octets in frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented when the result of a reception is reported as a receiveOK status. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

5.2.2.1.15 aFramesLostDueToIntMACRcvError

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that would otherwise be received by the station, but could not be accepted due to an internal MAC sublayer receive error. If this counter is incremented, then none of the other counters in this subclause are incremented. The exact meaning and mechanism for incrementing this counter is implementation dependent.

5.2.2.1.16 aPromiscuousStatus

ATTRIBUTE
APPROPRIATE SYNTAX:
BOOLEAN
BEHAVIOUR DEFINED AS:
A GET operation returns the value true for promiscuous mode enabled, and false otherwise.
Frames without errors received solely because this attribute has the value true are counted as frames received correctly; frames received in this mode that do contain errors update the appropriate error counters.
A SET operation to the value true provides a means to cause the LayerMgmtRecognizeAddress function to accept frames regardless of their destination address.

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A SET operation to the value false causes the MAC sublayer to return to the normal operation of carrying out address recognition procedures for station, broadcast, and multicast group addresses (LayerMgmtRecognizeAddress function).;

5.2.2.1.17 aReadMulticastAddressList

ATTRIBUTE
APPROPRIATE SYNTAX:
Sequence of MAC addresses.
BEHAVIOUR DEFINED AS:
Return the current multicast address list.;

5.2.2.1.18 aMulticastFramesXmittedOK

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are successfully transmitted, as indicated by the status value transmitOK, to a group destination address other than broadcast. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.1.19 aBroadcastFramesXmittedOK

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of the frames that were successfully transmitted, as indicated by the TransmitStatus transmitOK, to the broadcast address. Frames transmitted to multicast addresses are not broadcast frames and are excluded. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.1.20 aFramesWithExcessiveDeferral

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 412 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that deferred for an excessive period of time. This counter may only be incremented once per LLC transmission. This counter is incremented when the excessDefer flag is set. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).

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5.2.2.1.21 aMulticastFramesReceivedOK

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are successfully received and are directed to an active nonbroadcast group address. This does not include frames received with frame-too-long, FCS, length, or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented as indicated by the receiveOK status, and the value in the destinationField. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

5.2.2.1.22 aBroadcastFramesReceivedOK

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are successfully received and are directed to the broadcast group address. This does not include frames received with frame-too-long, FCS, length, or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented as indicated by the receiveOK status, and the value in the destinationField. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

5.2.2.1.23 aInRangeLengthErrors

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames with a length field value between the minimum unpadded LLC data size and the maximum allowed LLC data size, inclusive, that does not match the number of LLC data octets received. The counter also contains frames with a length field value less than the minimum unpadded LLC data size. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

5.2.2.1.24 aOutOfRangeLengthField

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames with a length field value greater than the maximum allowed LLC data size. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

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5.2.2.1.25 aFrameTooLongErrors

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 815 counts per second.
BEHAVIOUR DEFINED AS:
A count of frames that are received and exceed the maximum permitted frame size. This counter is incremented when the status of a frame reception is frameTooLong. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

5.2.2.1.26 aMACEnableStatus

ATTRIBUTE
APPROPRIATE SYNTAX:
BOOLEAN
BEHAVIOUR DEFINED AS:
True if MAC sublayer is enabled, and false if disabled. This is accomplished by setting or checking the values of the receiveEnabled and transmitEnabled variables.;
Setting to true provides a means to cause the MAC sublayer to enter the normal operational state at idle. The PLS is reset by this operation (see 7.2.2.2.1). This is accomplished by setting receiveEnabled and transmitEnabled to true.
Setting to false causes the MAC sublayer to end all transmit and receive operations, leaving it in a disabled state. This is accomplished by setting receiveEnabled and transmitEnabled to false.

5.2.2.1.27 aTransmitEnableStatus

ATTRIBUTE
APPROPRIATE SYNTAX:
BOOLEAN
BEHAVIOUR DEFINED AS:
True if transmission is enabled, and false otherwise. This is accomplished by setting or checking the value of the transmitEnabled variable.
Setting this to true provides a means to enable MAC sublayer frame transmission (TransmitFrame function). This is accomplished by setting transmitEnabled to true.
Setting this to false will inhibit the transmission of further frames by the MAC sublayer (TransmitFrame function). This is accomplished by setting transmitEnabled to false.

5.2.2.1.28 aMulticastReceiveStatus

ATTRIBUTE
APPROPRIATE SYNTAX:
BOOLEAN
BEHAVIOUR DEFINED AS:
True if multicast receive is enabled, and false otherwise.;
Setting this to true provides a means to cause the MAC sublayer to return to the normal operation of multicast frame reception.

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Setting this to false will inhibit the reception of further multicast frames by the MAC sublayer.

5.2.2.1.29 aReadWriteMACAddress

ATTRIBUTE
APPROPRIATE SYNTAX:
MACAddress
BEHAVIOUR DEFINED AS:
Read the MAC station address or change the MAC station address to the one supplied (RecognizeAddress function). Note that the supplied station address shall not have the group bit set and shall not be the null address.

5.2.2.1.30 aCollisionFrames

ATTRIBUTE
APPROPRIATE SYNTAX:
A SEQUENCE of 32 generalized nonresettable counters. Each counter has a maximum increment rate of 13 000 counts per second.
BEHAVIOUR DEFINED AS:
A histogram of collision activity. The indices of this array (1 to attemptLimit–1) denote the number of collisions experienced in transmitting a frame. Each element of this array contains a counter that denotes the number of frames that have experienced a specific number of collisions. When the TransmitStatus is reported as transmitOK and the value of the attempts variable equals n, then collisionFrames[n–1] counter is incremented. The elements of this array are incremented in the LayerMgmtTransmitCounters procedure (5.2.4.2).

5.2.2.2 DTE MAC Sublayer actions

5.2.2.2.1 acInitializeMAC

ACTION
APPROPRIATE SYNTAX:
None required
BEHAVIOUR DEFINED AS:
This action provides a means to call the Initialize procedure (4.2.7.5). This action also results in the initialization of the PLS.

5.2.2.2.2 acAddGroupAddress

ACTION
APPROPRIATE SYNTAX:
MACAddress
BEHAVIOUR DEFINED AS:
Add the supplied multicast group address to the address recognition filter (RecognizeAddress function).

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5.2.2.2.3 acDeleteGroupAddress

ACTION
APPROPRIATE SYNTAX:
MACAddress
BEHAVIOUR DEFINED AS:
Delete the supplied multicast group address from the address recognition filter (RecognizeAddress function).

5.2.2.2.4 acExecuteSelfTest

ACTION
APPROPRIATE SYNTAX:
None required
BEHAVIOUR DEFINED AS:
Execute a self-test and report the results (success or failure). The actual mechanism employed to carry out the self-test is not defined in this standard.

5.2.2.3 ResourceTypeID Managed Object Class

5.2.2.3.1 ResourceTypeID

Implementation of this managed object in accordance with the definition contained in IEEE Std 802.1F-1993 is a conformance requirement of this standard. A single instance of the Resource Type ID managed object exists within the DTE–MAC managed object class. The managed object itself is contained in IEEE Std 802.1F-1993; therefore, only the name binding appears in this standard.

5.2.3 DTE Physical Sublayer Management facilities

This subclause defines the Layer Management facilities specific to the Physical Layer Signalling (PLS) sublayer Managed Object Class. The PLS is required to be within a managed CSMA/CD port of a DTE. Management of that portion of the physical sublayer whose physical containment within the DTE is optional is outside the scope of this subclause.

5.2.3.1 DTE Physical Sublayer attributes

5.2.3.1.1 aPHYID

ATTRIBUTE
APPROPRIATE SYNTAX:
INTEGER
BEHAVIOUR DEFINED AS:
The value of aPHYID is assigned so as to uniquely identify a PHY, i.e., Physical Layer among the subordinate managed objects of system (systemID and system are defined in ISO/IEC 10165-2: 1992).;

5.2.3.1.2 aSQETestErrors

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second.

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BEHAVIOUR DEFINED AS:

A count of times that the SQE_TEST_ERROR was received. The SQE_TEST_ERROR is set in accordance with the rules for verification of the SQE detection mechanism in the PLS Carrier Sense Function (see 7.2.4.6).

5.2.4 DTE Management procedural model

The following model provides the descriptions for Layer Management facilities.

5.2.4.1 Common constants and types

The following are the common constants and types required for the Layer Management procedures:

const

maxUntaggedFrameSize = ... ; {in octets, implementation-dependent, see 4.4}
maxDeferTime = …; {2 × (maxUntaggedFrameSize × 8), for operating speeds of 100 Mb/s and below, and 2 × (burstLimit + maxUntaggedFrameSize × 8 + headerSize) for operating speeds greater than 100 Mb/s, in bits, error timer limit for maxDeferTime}
maxLarge = 4294967295; {maximum value ($2^{32} – 1$) of wraparound 32-bit counter}
max64 = 18446744073709551615; {maximum value ($2^{64} – 1$) of wraparound 64-bit counter}
oneBitTime = 1; {the period it takes to transmit one bit}

type

CounterLarge = 0..maxLarge--See footnote.;

5.2.4.2 Transmit variables and procedures

The following items are specific to frame transmission:

var

excessDefer: Boolean; {set in process DeferTest}
carrierSenseFailure: Boolean; {set in process CarrierSenseTest}
transmitEnabled: Boolean; {set by MAC action}
lateCollisionError: Boolean; {set in Section 4 procedure WatchForCollision}
deferred: Boolean; {set in Section 4 function TransmitLinkMgmt}
carrierSenseTestDone: Boolean; {set in process CarrierSenseTest}
lateCollisionCount: 0..attemptLimit – 1; {count of late collision that is used in Clause 4 TransmitLinkMgmt and BitTransmitter}
{MAC transmit counters}
framesTransmittedOK: CounterLarge; {mandatory}
singleCollisionFrames: CounterLarge; {mandatory}
multipleCollisionFrames: CounterLarge; {mandatory}
collisionFrames: array [1..attemptLimit – 1] of CounterLarge; {recommended}
octetsTransmittedOK: CounterLarge; {recommended}
deferredTransmissions: CounterLarge; {recommended}
multicastFramesTransmittedOK: CounterLarge; {optional}
broadcastFramesTransmittedOK: CounterLarge; {optional}
{MAC transmit error counters}
lateCollision: CounterLarge; {recommended}
excessiveCollision: CounterLarge; {recommended}
carrierSenseErrors: CounterLarge; {optional}
excessiveDeferral: CounterLarge; {optional}

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```
        halfDuplex: Boolean; {Indicates the desired mode. halfDuplex is a static variable; its value does
                              not change between invocations of the Initialize procedure}
```

Procedure LayerMgmtTransmitCounters is invoked from the TransmitLinkMgmt function and from the BitTransmitter process in 4.2.8 to update the transmit and transmit error counters.

```
procedure LayerMgmtTransmitCounters;
begin
   if halfDuplex then
      while not carrierSenseTestDone do nothing;
   if transmitSucceeding then
   begin
      IncLargeCounter(framesTransmittedOK);
      SumLarge(octetsTransmittedOK, dataSize/8); {dataSize (in bits) is defined in 4.2.7.1}
      if destinationField = … {check to see if to a multicast destination}
         then IncLargeCounter(multicastFramesTransmittedOK);
      if destinationField = … {check to see if to a broadcast destination}
         then IncLargeCounter(broadcastFramesTransmittedOK);

      if attempts > 1 then
      begin {transmission delayed by collision}
         if attempts = 2 then
            IncLargeCounter(singleCollisionFrames) {delay by 1 collision}
         else {attempts > 2, delayed by multiple collisions}
            IncLargeCounter(multipleCollisionFrames)
         IncLargeCounter(collisionFrames[attempts – 1])
      end {delay by collision}
   end; {transmitSucceeding}

   if deferred and (attempts = 1) then
      IncLargeCounter(deferredTransmissions);
   if lateCollisionCount > 0 then {test if late collision detected}
      SumLarge(lateCollision, lateCollisionCount);
   if attempts = attemptLimit and not transmitSucceeding then
      IncLargeCounter(excessiveCollision);
   if carrierSenseFailure then
      IncLargeCounter(carrierSenseErrors);
   if excessDefer then
      IncrementLargeCounter(excessiveDeferral)
end; {LayerMgmtTransmitCounters}
```

The DeferTest process sets the excessDefer flag if a transmission attempt has been deferred for a period of time longer than maxDeferTime.

```
process DeferTest;
   var deferBitTimer: 0..maxDeferTime;
begin
   cycle
   begin
      deferCount := 0;
      while frameWaiting and not excessDefer do
      begin
         Wait(oneBitTime); {see 4.3.3}
         if deferBitTimer = maxDeferTime then
```


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```
            excessDefer := true
        else
            deferBitTimer := deferBitTimer + 1
    end; {while}
    while transmitting do nothing
  end {cycle}
end; {DeferTest}
```

The CarrierSenseTest process sets the carrierSenseFailure flag if carrier sense disappears while transmitting or if it never appears during an entire transmission.

```
process CarrierSenseTest;
  var
    carrierSeen: Boolean; {Running indicator of whether or not carrierSense has been true at any
                           time during the current transmission}
    collisionSeen: Boolean; {Running indicator of whether or not the collisionDetect asserted any
                             time during the entire transmission}
begin
  cycle {main loop}
    while not transmitting do nothing; {wait for start of transmission}
    carrierSenseFailure := false;
    carrierSeen := false;
    collisionSeen := false;
    carrierSenseTestDone := false;
    while transmitting do
    begin {inner loop}
      if carrierSense then
        carrierSeen := true;
      else
        if carrierSeen then {carrierSense disappeared before end of transmission}
          carrierSenseFailure := true;
      if collisionDetect then
        collisionSeen := true
    end; {inner loop}
    if not carrierSeen then
      carrierSenseFailure := true {carrier sense never appeared}
    else
      if collisionSeen then
        carrierSenseFailure := false;
    carrierSenseTestDone := true
  end {main loop}
end; {CarrierSenseTest}
```

5.2.4.3 Receive variables and procedures

The following items are specific to frame reception:

```
var
  receiveEnabled: Boolean; {set by MAC action}
  {MAC receive counters}
  framesReceivedOK: CounterLarge; {mandatory}
  octetsReceivedOK: CounterLarge; {recommended}

  {MAC receive error counters}
```

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```
    frameCheckSequenceErrors: CounterLarge; {mandatory}
    alignmentErrors: CounterLarge; {mandatory}
    inRangeLengthErrors: CounterLarge; {optional}
    outOfRangeLengthField: CounterLarge; {optional}
    frameTooLongErrors: CounterLarge; {optional}

    {MAC receive address counters}
    multicastFramesReceivedOK: CounterLarge; {optional}
    broadcastFramesReceivedOK: CounterLarge; {optional}
```

Procedure LayerMgmtReceiveCounters is called by the ReceiveDataDecap function in 4.2.9 and increments the appropriate receive counters.

```
procedure LayerMgmtReceiveCounters (status: ReceiveStatus);
begin
  case status of
    receiveDisabled:
    begin
      nothing
    end; {receiveDisabled}
    receiveOK:
    begin
      IncLargeCounter(framesReceivedOK);
      SumLarge(octetsReceivedOK, dataSize/8); {dataSize (in bits) is defined in 4.2.7.1}
      if destinationField = … {check to see if to a multicast destination}
        then IncLargeCounter(multicastFramesReceivedOK);
      if destinationField = … {check to see if to a broadcast destination}
        then IncLargeCounter(broadcastFramesReceivedOK)
    end; {receiveOK}
    frameTooLong:
    begin
      IncLargeCounter(frameTooLongErrors)
    end; {frameTooLong}
    frameCheckError:
    begin
      IncLargeCounter(frameCheckSequenceErrors)
    end; {frameCheckError}
    alignmentError:
    begin
      IncLargeCounter(alignmentErrors)
    end; {alignmentError}
    lengthError:
    begin
      if {length field value is between the minimum unpadded LLCDataSize and maximum
        allowed LLCDataSize inclusive, and does not match the number of LLC data
        octets received} or {length field value is less than the minimum allowed unpadded
        LLC data size and the number of LLC data octets received is greater than the
        minimum unpadded LLCDataSize} then
        IncLargeCounter(inRangeLengthError);
      if {length field value is greater than the maximum allowed LLCDataSize} then
        IncLargeCounter(outOfRangeLengthField)
    end {lengthError}
  end {case status}
end; {LayerMgmtReceiveCounters}
```


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Function LayerMgmtRecognizeAddress checks if reception of certain addressing types has been enabled. Note that in Pascal, assignment to a function causes the function to return immediately.

```
function LayerMgmtRecognizeAddress(address: AddressValue): Boolean;
begin
   if {promiscuous receive enabled} then
      LayerMgmtRecognizeAddress := true;
   if address = … {MAC station address} then
      LayerMgmtRecognizeAddress := true;
   if address = … {broadcast address} then
      LayerMgmtRecognizeAddress := true;
   if address = … {one of the addresses on the multicast list and multicast reception is enabled} then
      LayerMgmtRecognizeAddress := true;
   LayerMgmtRecognizeAddress := false
end; {LayerMgmtRecognizeAddress}
```

5.2.4.4 Common procedures

Procedure LayerMgmtInitialize initializes all the variables and constants required to implement Layer Management.

```
procedure LayerMgmtInitialize;
begin
   {initialize flags for enabling/disabling transmission and reception}
   receiveEnabled := true;
   transmitEnabled := true;
   {initialize transmit flags for DeferTest and CarrierSenseTest}
   deferred := false;
   lateCollisionError := false;
   excessDefer := false;
   carrierSenseFailure := false;
   carrierSenseTestDone := false

   {Initialize all MAC sublayer management counters to zero}

end; {LayerMgmtInitialize}
```

Procedure IncLargeCounter increments a 32-bit wraparound counter.

```
procedure IncLargeCounter (var counter: CounterLarge);
begin
   {increment the 32-bit counter}
end; {IncLargeCounter}
```

Procedure SumLarge adds a value to a 32-bit wraparound counter.

```
procedure SumLarge (
   var counter: CounterLarge;
   var offset: Integer);
begin
   {add offset to the 32-bit counter}
end; {SumLarge}
```

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6. Physical Signaling (PLS) service specifications

6.1 Scope and field of application

This clause specifies the services provided by the PLS sublayer to the MAC sublayer for the CSMA/CD clause of this LAN standard, Figure 6–1. The services are described in an abstract way and do not imply any particular implementation.

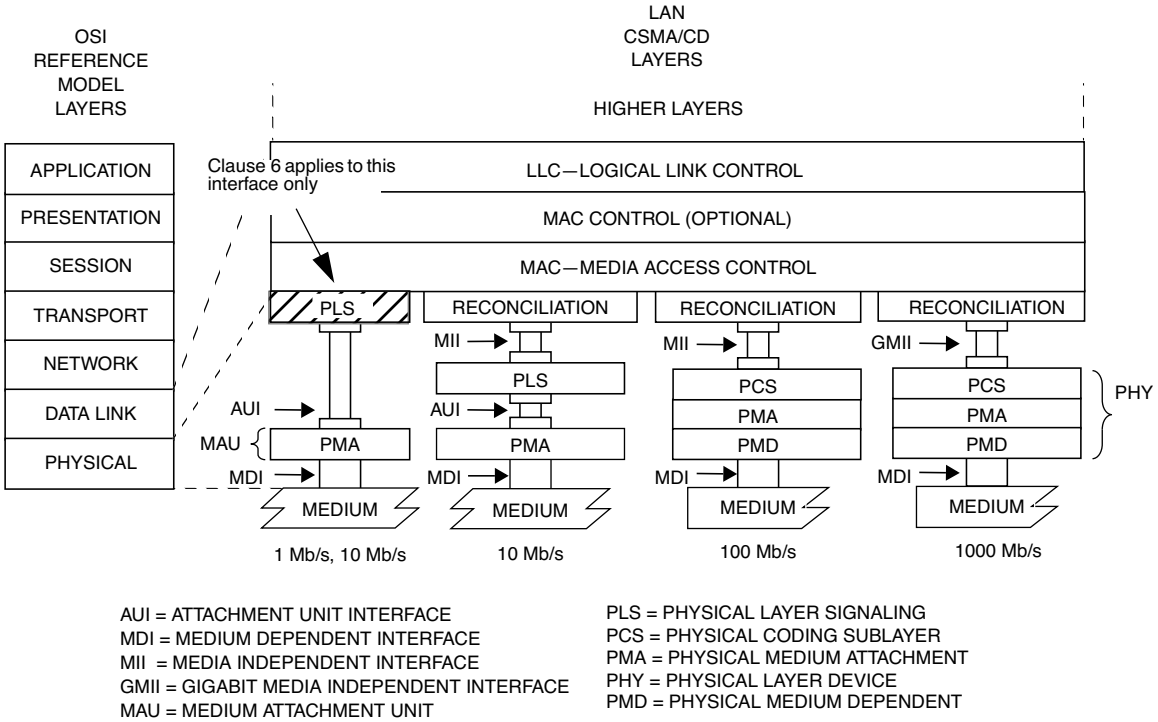


Figure 6–1—Service specification relationship to the IEEE 802.3 CSMA/CD LAN model

6.2 Overview of the service

6.2.1 General description of services provided by the layer

The services provided by the PLS sublayer allow the local MAC sublayer entity to exchange data bits (PLS data_units) with peer MAC sublayer entities.

6.2.2 Model used for the service specification

The model used in this service specification is identical to that used in 1.2.2.1.

6.2.3 Overview of interactions

The primitives associated with the MAC sublayer to PLS sublayer interface fall into two basic categories:

a) Service primitives that support MAC peer-to-peer interactions.
b) Service primitives that have local significance and support sublayer-to-sublayer interactions.

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The following primitives are grouped into these two categories:

a) Peer-to-Peer
   PLS_DATA.request
   PLS_DATA.indication
b) Sublayer-to-Sublayer
   PLS_CARRIER.indication
   PLS_SIGNAL.indication
   PLS_DATA_VALID.indication

The PLS_DATA primitives support the transfer of data from a single MAC sublayer entity to all other peer MAC sublayer entities contained within the same LAN defined by the broadcast medium.

NOTE—In half duplex mode, all bits transferred from a MAC sublayer entity will in turn be received by the entity itself.

The PLS_CARRIER, PLS_DATA_VALID, and the PLS_SIGNAL primitives provide information needed by the local MAC sublayer entity to perform the media access functions.

6.2.4 Basic services and options

All of the service primitives described in this subclause are considered mandatory.

6.3 Detailed service specification

6.3.1 Peer-to-peer service primitives

6.3.1.1 PLS_DATA.request

6.3.1.1.1 Function

This primitive defines the transfer of data from the MAC sublayer to the local PLS entity.

6.3.1.1.2 Semantics of the service primitive

The primitive shall provide the following parameters:

PLS_DATA.request (OUTPUT_UNIT)

The OUTPUT_UNIT parameter can take on one of three values: ONE, ZERO, or DATA_COMPLETE and represent a single data bit. The DATA_COMPLETE value signifies that the Media Access Control sublayer has no more data to output.

6.3.1.1.3 When generated

This primitive is generated by the MAC sublayer to request the transmission of a single data bit on the physical medium or to stop transmission.

6.3.1.1.4 Effect of receipt

The receipt of this primitive will cause the PLS entity to encode and transmit either a single data bit or to cease transmission.

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6.3.1.2 PLS_DATA.indication

6.3.1.2.1 Function

This primitive defines the transfer of data from the PLS sublayer to the MAC sublayer.

6.3.1.2.2 Semantics of the service primitive

The semantics of the service primitive are as follows:

PLS_DATA. indicate (INPUT_UNIT)

The INPUT_UNIT parameter can take one of two values each representing a single bit: ONE or ZERO.

6.3.1.2.3 When generated

The PLS_DATA.indicate is generated to all MAC sublayer entities in the network after a PLS_DATA.request is issued.

NOTE—In half duplex mode, an indication is also presented to the MAC entity that issued the request.

6.3.1.2.4 Effect of receipt

The effect of receipt of this primitive by the MAC sublayer is unspecified.

6.3.2 Sublayer-to-sublayer service primitives

6.3.2.1 PLS_CARRIER.indication

6.3.2.1.1 Function

This primitive transfers the status of the activity on the physical medium from the PLS sublayer to the MAC sublayer.

6.3.2.1.2 Semantics of the service primitive

The semantics of the primitive are as follows:

PLS_CARRIER.indication (CARRIER_STATUS)

The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF. The CARRIER_ON value indicates that the DTE Physical Layer had received an *input* message or a *signal_quality_error* message from the MAU. The CARRIER_OFF value indicates that the DTE Physical Layer had received an *input_idle* message and is not receiving an SQE *signal_quality_error* message from the MAU.

6.3.2.1.3 When generated

The PLS_CARRIER.indication service primitive is generated whenever CARRIER_STATUS makes a transition from CARRIER_ON to CARRIER_OFF or vice versa.

6.3.2.1.4 Effect of receipt

The effect of receipt of this primitive by the MAC sublayer is unspecified.

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6.3.2.2 PLS_SIGNAL.indication

6.3.2.2.1 Function

This primitive transfers the status of the Physical Layer signal quality from the PLS sublayer to the MAC sublayer.

6.3.2.2.2 Semantics of the service primitive

The semantics of the service primitive are as follows:

PLS_SIGNAL.indication (SIGNAL_STATUS)

The SIGNAL_STATUS parameter can take one of two values: SIGNAL_ERROR or NO_SIGNAL_ERROR. The SIGNAL_ERROR value indicates to the MAC sublayer that the PLS has received a *signal_quality_error* message from the MAU. The NO_SIGNAL_ERROR value indicates that the PLS has ceased to receive *signal_quality_error* messages from the MAU.

6.3.2.2.3 When generated

The PLS_SIGNAL.indication service primitive is generated whenever SIGNAL_ STATUS makes a transition from SIGNAL_ERROR to NO_SIGNAL_ERROR or vice versa.

6.3.2.2.4 Effect of receipt

The effect of receipt of this primitive by the MAC sublayer is unspecified.

6.3.2.3 PLS_DATA_VALID.indication

6.3.2.3.1 Function

This primitive provides a facility for transferring framing information to the MAC sublayer.

6.3.2.3.2 Semantics of the service primitive

The semantics of the service primitive are as follows:

PLS_DATA_VALID.indication (DATA_VALID_STATUS)

The DATA_VALID_STATUS parameter can take one of two values: DATA_VALID or DATA_NOT_VALID. The DATA_VALID value indicates that the INPUT_UNIT parameter of the PLS_DATA.indicate primitive contains valid data of an incoming frame. The DATA_NOT_VALID value indicates that the INPUT_UNIT parameter of the PLS_DATA.indicate primitive does not contain valid data of an incoming frame.

6.3.2.3.3 When generated

The PLS_DATA_VALID.indication service primitive is generated whenever the DATA_VALID_STATUS parameter makes a transition from DATA_VALID to DATA_NOT_VALID or vice versa.

6.3.2.3.4 Effect of receipt

The effect of receipt of this primitive by the MAC sublayer is unspecified.

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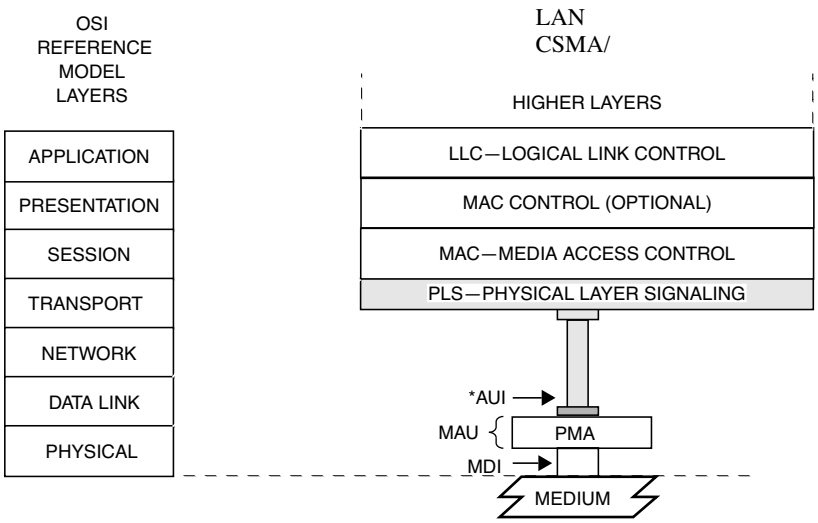
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7. Physical Signaling (PLS) and Attachment Unit Interface (AUI) specifications

7.1 Scope

This clause defines the logical, electrical, and mechanical characteristics for the PLS and AUI between Data Terminal Equipment and Medium Attachment Units used in CSMA/CD local area networks. The relationship of this specification to the entire IEEE LAN standard is shown in Figure 7–1. The purpose of this interface is to provide an interconnection that is simple and inexpensive and that permits the development of simple and inexpensive MAUs.



AUI = ATTACHMENT UNIT INTERFACE
MAU = MEDIUM ATTACHMENT UNIT
MDI = MEDIUM DEPENDENT INTERFACE
PMA = PHYSICAL MEDIUM ATTACHMENT

NOTE—For an exposed AUI residing below an MII, see 22.5.

Figure 7–1—Physical layer partitioning, relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

This interface has the following characteristics:

a) Capable of supporting one or more of the specified data rates.
b) Capable of driving up to 50 m of cable.
c) Permits the DTE to test the AUI, AUI cable, MAU, and the medium itself.
d) Supports MAUs for baseband coax, baseband twisted-pair, broadband coax, and baseband fiber.

7.1.1 Definitions

See 1.4.

7.1.2 Summary of major concepts

a) Each direction of data transfer is serviced with two (making a total of four) balanced circuits: “Data” and “Control.”

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b) The Data and Control circuits are independently self-clocked, thereby, eliminating the need for separate timing circuits. This is accomplished with encoding of all signals. The Control circuit signaling rate is nominally (but not of necessity exactly) equal to the Data circuit signaling rate.
c) The Data circuits are used only for data transfer. No control signals associated with the interface are passed on these circuits. Likewise, the Control circuits are used only for control message transfer. No data signals associated with the interface are passed on these circuits.

7.1.3 Application

This standard applies to the interface used to interconnect Data Terminal Equipment (DTE) to a MAU that is not integrated as a physical part of the DTE. This interface is used to

a) Provide the DTE with media independence for baseband coax, baseband twisted pair, broadband coax, and baseband fiber media so that identical PLS, MAC, and MAC clients may be used with any of these media.
b) Provide for the separation, by cable of up to 50 m, of the DTE and the MAU.

7.1.4 Modes of operation

The AUI can operate in two different modes. All interfaces shall support the normal mode. The monitor mode is optional.

When the interface is being operated in the *normal* mode, the AUI is logically connected to the MDI. The DTE is required to follow the media access algorithms, which provide a single access procedure compatible with all LAN media, to send data over the AUI. The MAU always sends back to the DTE whatever data the MAU receives on the MDI.

When the interface is in the optional *monitor* mode, the MAUs transmitter is logically isolated from the medium. The MAU, in this mode, functions as an observer on the medium. Both the input function and the signal quality error function are operational (see the MAU state diagrams for specific details).

The PLS and AUI as specified here are able to support DTEs and MAUs operating in either half duplex or full duplex modes without change to the PLS or AUI. Full duplex MAUs do not support the monitor mode.

7.1.5 Allocation of function

The allocation of functions in the AUI is such that the majority of the functionality required by the interface can be provided by the DTE, leaving the MAU as simple as possible. This division of functions is based upon the recognition of the fact that since, in many cases, the MAU may be located in an inaccessible location adjacent to the physical medium, service of the MAU may often be difficult and expensive.

7.2 Functional specification

The AUI is designed to make the differences among the various media as transparent as possible to the DTE. The selection of logical control signals and the functional procedures are all designed to this end. Figure 7–2 is a reference model, a generalized MAU as seen by the DTE through the AUI.

Many of the terms used in this subclause are specific to the interface between this sublayer and the MAC sublayer. These terms are defined in the Service Specification for the PLS sublayer.

7.2.1 PLS–PMA (DTE–MAU) Interface protocol

The DTE and MAU communicate by means of a simple protocol across the AUI.

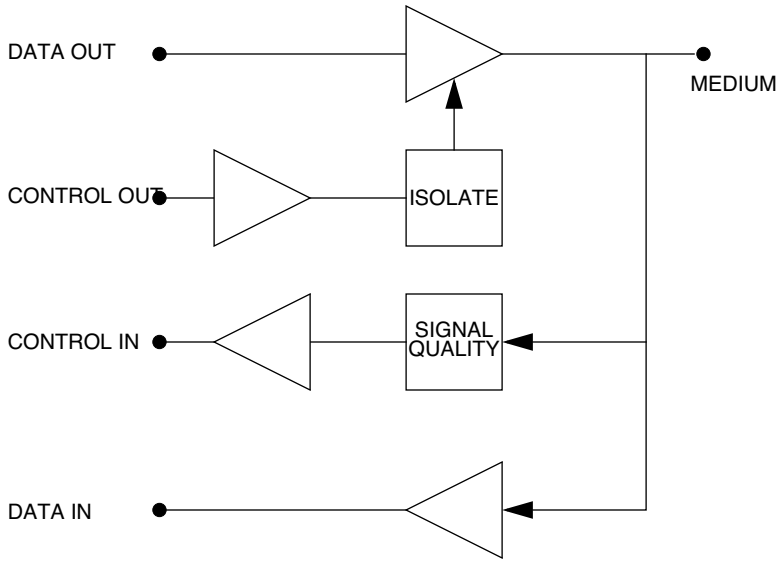
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NOTE—The AUI (comprised of DO, DI, CO, CI circuits) is not exposed when the MAU is, optionally, part of the DTE.

Figure 7–2—Generalized MAU model

7.2.1.1 PLS to PMA messages

The following messages can be sent by PLS sublayer entities in the DTE to PMA sublayer entities in the MAU:

Message	Meaning
output	Output information
output_idle	No data to be output
normal	Cease to isolate the MAU
(Optional)	
isolate	Isolate MAU
mau_request	Request that the MAU be made available

7.2.1.1.1 *output* message

The PLS sublayer sends an output message to the PMA sublayer when the PLS sublayer receives an OUTPUT_UNIT from the MAC sublayer.

The physical realization of the *output* message is a CD0 or a CD1 sent by the DTE to the MAU on the Data Out circuit. The DTE sends a CD0 if the OUTPUT_UNIT is a ZERO or a CD1 if the OUTPUT_UNIT is a ONE. This message is time coded—that is, once this message has been sent, the function is not completed over the AUI until one bit time later. The *output* message cannot be sent again until the bit cell being sent as a result of sending the previous *output* message is complete.

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7.2.1.1.2 *output_idle* message

The PLS sublayer sends an *output_idle* message to the PMA sublayer at all times when the MAC sublayer is not in the process of transferring output data across the MAC to PLS interface. The *output_idle* message is no longer sent (and the first OUTPUT_UNIT is sent using the *output* message) as soon after the arrival of the first OUTPUT_UNIT as the MAU can be made available for data output. The *output_idle* message is again sent to the MAU when the DATA_COMPLETE is received from the MAC sublayer. The detailed usage of the *output_idle* message is shown in Figure 7–5.

The physical realization of the *output_idle* message is IDL sent by the DTE to the MAU on the Data Out circuit.

7.2.1.1.3 *normal* message

The PLS sublayer sends a *normal* message to the PMA sublayer after it receives the PLS *start* message from the PLS Reset and Identify function. The *normal* message is also sent after receipt of RESET_MONITOR_MODE from the management entity. The *normal* message is sent continuously by the PLS sublayer to the MAU, unless the PLS Output function requires that the *mau_request* message be sent to permit data output. If *mau_request* is sent during data output, the sending of *normal* will be resumed when the PLS Output function returns to the IDLE state. The *normal* signal is reset by the SET_MONITOR_MODE (this reset function is described more fully by Figure 7–4).

7.2.1.1.4 *isolate* message (optional)

The PLS sublayer sends an *isolate* message to the PMA (in the MAU) whenever the PLS sublayer receives SET_MONITOR_MODE from the management entity. In response to the *isolate* message, the MAU causes the means employed to impress data on the physical medium to be positively prevented from affecting the medium. Since signaling and isolation techniques differ from medium to medium, the manner in which this positive isolation of the transmitting means is accomplished is specified in the appropriate MAU subclause. However, the intent of this positive isolation of the transmitter is to ensure that the MAU will not interfere with the physical medium in such a way as to affect transmissions of other stations even in the event that the means normally employed to prevent the transmitter from affecting the medium have failed to do so. The specification of positive isolation is not to be construed to preclude use of either active or passive devices to accomplish this function.

The physical realization of the *isolate* message is a CS0 signal sent by the DTE to the MAU over the Control Out circuit.

7.2.1.1.5 *mau_request* message (optional)

The PLS sublayer senses the *mau_request* message to the PMA sublayer if the PMA sublayer is sending the *mau_not_available* message and the MAC sublayer has sent the first OUTPUT_UNIT of a new transmission. The PLS sublayer continues to send the *mau_request* message to the MAU until the MAC sublayer sends the DATA_COMPLETE request to the PLS sublayer across the MAC to PLS interface. See Figures 7–3, 7–5, and 7–9 for details.

In addition, the *mau_request* message is used by the Reset and Identify function in the IDENTIFY 3 state to determine whether the MAU has the Isolate function.

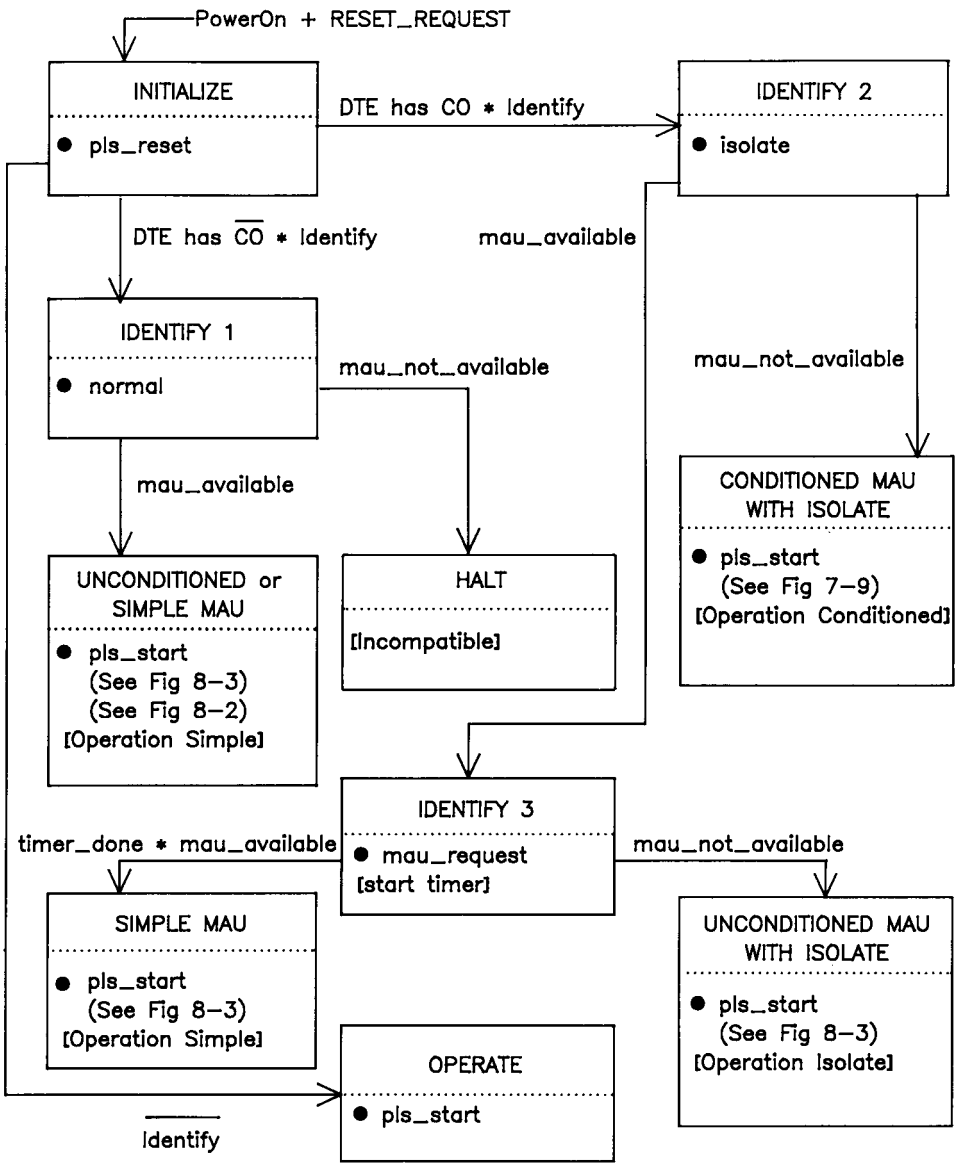
The physical realization of *mau_request* is a CS1 sent by the DTE to the MAU on the Control Out circuit.

The physical realization of the *normal* message is the IDL signal sent by the DTE to the MAU on the Control Out circuit. In the absence of the CO circuit, MAUs implementing the Isolate function shall act as if the *normal* message is present. The CO circuit components may be absent from the DTE, AUI, or MAU.

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NOTES: (1) All states may be omitted except INITIALIZE and OPERATE
(2) "Identify" means DTE can recognize uniquely all CI messages and the entire function has been implemented
(3) "Identify" with bar means DTE fails to recognize *mau_not_available* or has a partial implementation of the function

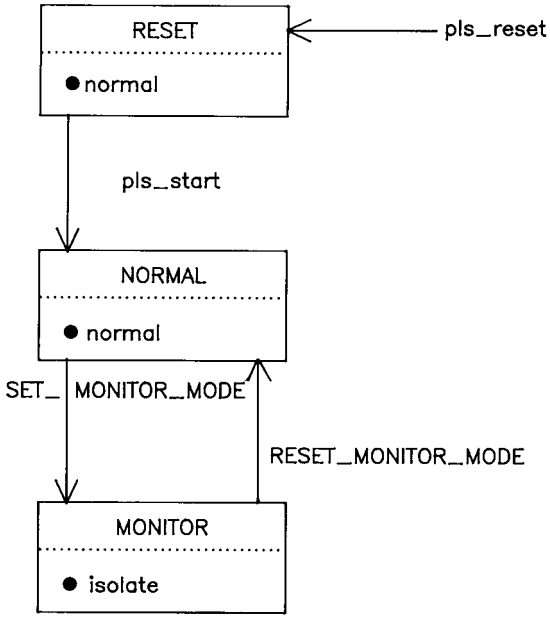
Figure 7–3—PLS Reset and Identify function

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NOTE: Monitor State is optional.

Figure 7–4—PLS Mode function

7.2.1.2 PMA to PLS interface

The following messages can be sent by the Physical Medium Attachment sublayer entities in the MAU to the PLS sublayer entities in the DTE:

Message	Meaning
input	Input information
input_idle	No input information
signal_quality_error	Error detected by MAU
mau_available	MAU is available for output
(Optional)	
mau_not_available	MAU is not available for output

In systems operating in full duplex mode, it is permitted, but not required, to implement the *signal_quality_error* message.

7.2.1.2.1 *input* message

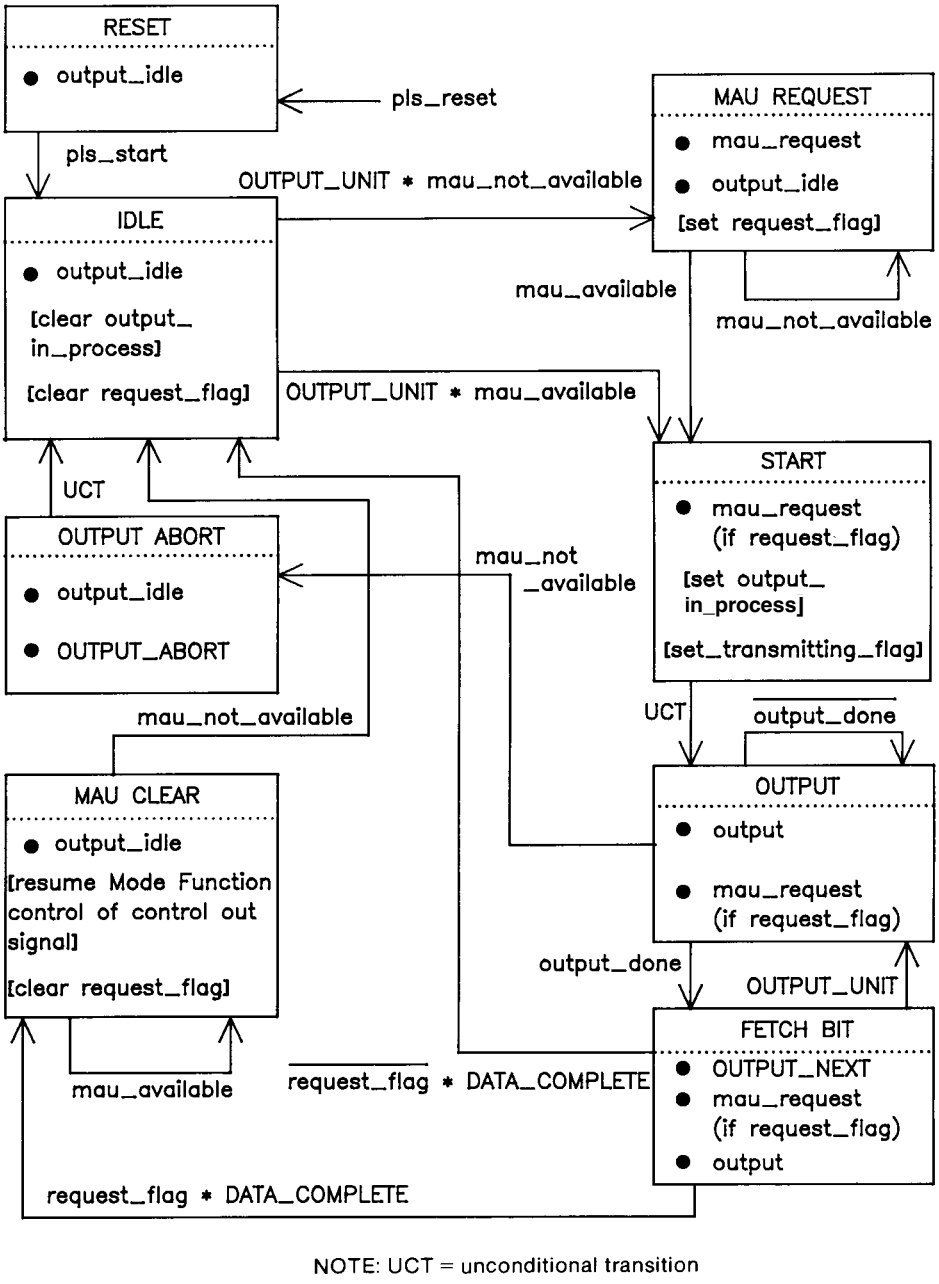
The PMA sublayer sends an *input* message to the PLS sublayer when the MAU has received a bit from the medium and is prepared to transfer this bit to the DTE. The actual mapping of the signals on the medium to the type of *input* message to be sent to the DTE is contained in the specifications for each specific MAU

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NOTE: UCT = unconditional transition

Figure 7–5—PLS Output function

type. In general, when the *signal_quality_error* message is being sent by the MAU, the symmetry specifications for circuit DI are not guaranteed to be met.

The physical realization of the *input* message consists of CD0 or CD1 waveforms. If the *signal_quality_error* message is being sent from the MAU, the input waveform is unpredictable.

NOTE—This signal is not necessarily retimed by the MAU. Consult the appropriate MAU specification for timing and jitter.

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7.2.1.2.2 *input_idle* message

The PMA sublayer sends an *input_idle* message to the PLS sublayer when the MAU does not have data to send to the DTE.

The physical realization of the *input_idle* message is an IDL sent by the MAU to the DTE on the Data In circuit.

7.2.1.2.3 *signal_quality_error* message

The PMA sublayer sends a *signal_quality_error* message to the PLS sublayer in response to any of three possible conditions. These conditions are improper signals on the medium, collision on the medium, and reception of the *output_idle* message. They are described in the lettered paragraphs that follow. The physical realization of the *signal_quality_error* message is a CS0 sent by the MAU to the DTE on the Control In circuit.

In systems operating in half duplex mode, the MAU is required to assert the *signal_quality_error* message at the appropriate times whenever the MAU is powered, and not just when the DTE is requesting data output. In systems operating in full duplex mode, it is permitted, but not required, to implement the *signal_quality_error* message. See Figures 7–9, 8–2, and 8–3 for details.

a) Improper Signals on the Medium. The MAU may send the *signal_quality_error* message at any time due to improper signals on the medium. The exact nature of these improper signals are medium-dependent. Typically, this condition might be caused by a malfunctioning MAU (for example, repeater or head-end) connected to the medium or by a break or short in the medium. See the appropriate MAU specification for specific conditions that may cause improper signals on a given medium.
b) Collision. Collision occurs when more than one MAU is transmitting on the medium. The local MAU shall send the *signal_quality_error* message in every instance when it is possible for it to ascertain that more than one MAU is transmitting on the medium. The MAU shall make the best determination possible. The MAU shall not send the *signal_quality_error* message when it is unable to determine conclusively that more than one MAU is transmitting.
c) *signal_quality_error* Message Test. The MAU sends the *signal_quality_error* message at the completion of the Output function. See Figure 7–9 and Clause 8 for a more complete description of this test.

7.2.1.2.4 *mau_available* message

The PMA sublayer sends the *mau_available* message to the PLS sublayer when the MAU is available for output. The *mau_available* message is always sent by a MAU that is always prepared to output data except when it is required to signal the *signal_quality_error* message. Such a MAU does not require *mau_request* to prepare itself for data output. See Figures 7–3, 7–5, and 7–9 for details.

The physical realization of the *mau_available* message is an IDL sent by the MAU to the DTE on the Control In circuit.

7.2.1.2.5 *mau_not_available* message (optional)

The PMA sublayer sends a *mau_not_available* message to the PLS sublayer when the MAU is not available for output. Figure 7–5 shows the relationship of *mau_not_available* to the Output function.

The *mau_not_available* message is also used by a MAU that contains the Isolate function and does not need to be conditioned for output to signal the presence of the Isolate function during the PLS Reset function (see Figure 7–3 and Figure 8–3).

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The physical realization of the *mau_not_available* message is a CS1 sent by the MAU to the DTE on the Control In circuit.

7.2.2 PLS interface to MAC and management entities

The PLS sublayer interfaces described here are for reference only. This clause specifies the services sent between the MAC sublayer and the PLS sublayer.

7.2.2.1 PLS–MAC interface

The following messages can be sent between PLS sublayer entities and MAC sublayer entities:

Message	Meaning
OUTPUT_UNIT	Data sent to the MAU
OUTPUT_STATUS	Response to OUTPUT_UNIT
INPUT_UNIT	Data received from the MAU
CARRIER_STATUS	Indication of channel activity
SIGNAL_STATUS	Indication of error/no error condition
DATA_VALID_STATUS	Indication of input activity

7.2.2.1.1 OUTPUT_UNIT

The MAC sublayer sends the PLS sublayer an OUTPUT_UNIT every time the MAC sublayer has a bit to send. Once the MAC sublayer has sent an OUTPUT_UNIT to the PLS sublayer, it may not send another OUTPUT_UNIT until it has received an OUTPUT_STATUS message from the PLS sublayer. The OUTPUT_UNIT is a ONE if the MAC sublayer wants the PLS sublayer to send a CD1 to the PMA sublayer, a ZERO if a CD0 is desired, or a DATA_COMPLETE if an IDL is desired.

7.2.2.1.2 OUTPUT_STATUS

The PLS sublayer sends the MAC sublayer OUTPUT_STATUS in response to every OUTPUT_UNIT received by the PLS sublayer. OUTPUT_STATUS sent is an OUTPUT_NEXT if the PLS sublayer is ready to accept the next OUTPUT_UNIT from the MAC sublayer, or an OUTPUT_ABORT if the PLS sublayer was not able to process the previous OUTPUT_UNIT. (The purpose of OUTPUT_STATUS is to synchronize the MAC sublayer data output with the data rate of the physical medium.)

7.2.2.1.3 INPUT_UNIT

The PLS sublayer sends the MAC sublayer an INPUT_UNIT every time the PLS receives an *input* message from the PMA sublayer. The INPUT_UNIT is a ONE if the PLS sublayer receives a CD1 from the PMA sublayer, a ZERO if the PLS sublayer receives a CD0 from the PMA sublayer.

7.2.2.1.4 CARRIER_STATUS

The PLS sublayer sends the MAC sublayer CARRIER_STATUS whenever the PLS sublayer detects a change in carrier status. The PLS sublayer sends CARRIER_ON when it receives an *input* or *signal_quality_error* message from the PMA and the previous CARRIER_STATUS that the PLS sublayer sent to the MAC sublayer was CARRIER_OFF. The PLS sublayer sends CARRIER_OFF when it receives an *input_idle* from the PMA sublayer, no *signal_quality_error* (either *mau_available* or *mau_not_available*)

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message and the previous CARRIER_STATUS that the PLS sublayer sent to the MAC sublayer was CARRIER_ON.[16]

7.2.2.1.5 SIGNAL_STATUS

The PLS sublayer sends the MAC sublayer SIGNAL_STATUS whenever the PLS sublayer detects a change in the signal quality (as reported by the PMA). The PLS sublayer sends SIGNAL_ERROR when it receives a *signal_quality_error* message from the PMA sublayer and the previous SIGNAL_STATUS the PLS sublayer sent was NO_SIGNAL_ERROR. The PLS sublayer sends NO_SIGNAL_ERROR when it receives no *signal_quality_error* (either *mau_available* or *mau_not_available)* message from the PMA sublayer and the previous CARRIER_STATUS that the PLS sent to the MAC sublayer was SIGNAL_ERROR.[17]

7.2.2.1.6 DATA_VALID_STATUS

The PLS sublayer sends the MAC sublayer DATA_VALID_STATUS whenever the PLS sublayer detects a change in receive data status. The PLS sublayer sends DATA_VALID when it receives an *input* message from the PMA and the previous DATA_VALID_STATUS that the PLS sublayer sent to the MAC sublayer was DATA_NOT_VALID. The PLS sublayer sends DATA_NOT_VALID when it is not receiving an input message from the PMA and the previous DATA_VALID_STATUS that the PLS sublayer sent to the MAC sublayer was DATA_VALID.

7.2.2.2 PLS–management entity interface

The following messages may be sent between the PLS sublayer entities and intralayer or higher layer management entities:

Message	Meaning
RESET_REQUEST	Reset PLS to initial “Power On” state
RESET_RESPONSE	Provides operational information
MODE_CONTROL	Control operation
SQE_TEST	Signal Quality Error test results

7.2.2.2.1 RESET_REQUEST

The management entity sends the PLS sublayer RESET_REQUEST when the PLS sublayer needs to be reset to a known state. Upon receipt of RESET_REQUEST, the PLS sublayer resets all internal logic and restarts all functions. See Figure 7–3 for details.

---

[16] Formerly, the Carrier Sense function described in Figure 7–8 generated the CARRIER_STATUS message described above. For the sake of consistency with common implementation practice, the variable carrierSense (see 4.3.3) is generated directly by the Carrier Sense function in recent editions of the standard.

The mapping between the CARRIER_STATUS message and the carrierSense variable is as follows. When the carrierSense variable changes from False to True, the CARRIER_STATUS message is sent with the parameter CARRIER_ON. When the value of the carrierSense variable changes from True to False, the CARRIER_STATUS message is sent with the parameter CARRIER_OFF.

[17] Formerly, the PLS Error Sense function described in Figure 7–7 generated the SIGNAL_STATUS message described above. For the sake of consistency with common implementation practice, the variable collisionDetect (see 4.3.3) is generated directly by the PLS Error Sense function in recent editions of the standard.

The mapping between the SIGNAL_STATUS message and the collisionDetect variable is as follows. When the collisionDetect variable changes from False to True, the SIGNAL_STATUS message is sent with the parameter SIGNAL_ERROR. When the value of the collisionDetect variable changes from True to False, the SIGNAL_STATUS message is sent with the parameter NO_SIGNAL_ERROR.

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7.2.2.2.2 RESET_RESPONSE

The PLS sublayer sends the management entity RESET_RESPONSE upon completion of the Reset and Identify function (see Figure 7–3 and 7.2.4.1) whether invoked due to power on or due to a RESET_REQUEST. Which RESET_RESPONSE was sent is determined by the Reset and Identify function. A RESET_RESPONSE of OPERATION SIMPLE, OPERATION ISOLATE, or OPERATION CONDITIONED is sent if the MAU is compatible with the DTE and the MAU is simple (no isolate) or if the DTE does not support Isolate even if Isolate is supported by the MAU, supports Isolate but does not require conditioning, or supports Isolate and does require conditioning to output. A RESET_RESPONSE of INCOMPATIBLE is sent if the MAU is not compatible with the DTE (that is, the MAU requires conditioning but the DTE does not support conditioning).

7.2.2.2.3 MODE_CONTROL

The management entity sends MODE_CONTROL to the PLS sublayer to control PLS functions. MODE_CONTROL capabilities are as follows:

Message	Meaning
ACTIVATE PHYSICAL	Supply power on circuit VP
DEACTIVATE PHYSICAL	Remove power from circuit VP
SET_MONITOR_MODE	Send Isolate to MAU
RESET_MONITOR_MODE	Send Normal to MAU

7.2.2.2.4 SQE_TEST

The PLS sublayer sends SQE_TEST to the management entity at the conclusion of each *signal_quality_error* test (see Output Function, 7.2.4.3). The PLS sublayer sends SQE_TEST_ERROR if the *signal_quality_error* test fails or SQE_TEST_OK if the *signal_quality_error* test passes.

In systems operating in full duplex mode, it is permitted, but not required, to implement the SQE_TEST message.[18]

7.2.3 Frame structure

Frames transmitted on the AUI shall have the following structure:

<silence><preamble><sfd><data><etd><silence>

[18]Formerly, the PLS Carrier Sense function described in Figure 7–8 generated the SQE_TEST message described above. For the sake of consistency with common implementation practice, the variable SQETestError is generated directly by the PLS Carrier Sense function in recent editions of the standard.

The mapping between the SQE_TEST message and the PLS Carrier Sense function described in Figure 7–8 is as follows. When the transition from the state WAIT 1 to the state FAILURE occurs, the SQE_TEST message is sent with the parameter SQE_TEST_ERROR. When the transition from either the state WAIT 1 or the state ABORT_TEST to the state WAIT 2 occurs, the SIGNAL_STATUS message is sent with the parameter NO_SIGNAL_ERROR.

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The frame elements shall have the following characteristics:

Element	Characteristics
<silence>	= no transitions
<preamble>	= alternating (CD1) and (CD0)	56 bit times (ending in CD0)
<sfd>	= (CD1)(CD0)(CD1)(CD0)(CD1)(CD0)(CD1)(CD1)
<data>	= 8 × N instances of CD0 or CD1
<etd>	= IDL

7.2.3.1 Silence

The <silence> delimiter provides an observation window for an unspecified period of time during which no transitions occur on the AUI. The minimum length of this period is specified by the access procedure.

7.2.3.2 Preamble

The <preamble> delimiter begins a frame transmission and provides a signal for receiver synchronization. The signal shall be an alternating pattern of (CD1) and (CD0). This pattern shall be transmitted on the Data Out circuit by the DTE to the MAU for a minimum of 56 bit times at the beginning of each frame. The last bit of the preamble (that is, the final bit of preamble before the start of frame delimiter) shall be a CD0.

The DTE is required to supply at least 56 bits of preamble in order to satisfy system requirements. System components consume preamble bits in order to perform their functions. The number of preamble bits sourced ensures an adequate number of bits are provided to each system component to correctly implement its function.

7.2.3.3 Start of Frame Delimiter (SFD)

The <sfd> indicates the start of a frame, and follows the preamble. The <sfd> element of a frame shall be

(CD1)(CD0)(CD1)(CD0)(CD1)(CD0)(CD1)(CD1)

7.2.3.4 Data

The <data> in a transmission shall be in multiples of eight (8) encoded data bits (CD0s and CD1s).

7.2.3.5 End of transmission delimiter

The <etd> delimiter indicates the end of a transmission and serves to turn off the transmitter. The signal shall be start of IDL.

7.2.4 PLS functions

The PLS sublayer functions consist of a Reset and Identify function and five simultaneous and asynchronous functions. These functions are Output, Input, Mode, Error Sense, and Carrier Sense. All of the five functions are started immediately following the completion of the Reset and Identify function. These functions are depicted in the state diagrams shown in Figure 7–3 through Figure 7–8, using notation described in 1.2.1.

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7.2.4.1 Reset and Identify function

The Reset and Identify function is executed any time either of two conditions occur. These two conditions are “power on” and the receipt of RESET_REQUEST from the management entity. The Reset and Identify function initializes all PLS functions, and (optionally) determines the capability of the MAU attached to the AUI. Figure 7–3 is the state diagram of the Reset and Identify function. The Identify portion of the function is optional.

7.2.4.2 Mode function

The MAU functions in two modes: normal and monitor. The monitor mode is optional. The state diagram of Figure 7–4 depicts the operation of the Mode function. When the MAU is operating in the normal mode, it functions as a direct connection between the DTE and the medium. Data sent from the DTE are impressed onto the medium by the MAU and all data appearing on the medium are sent to the DTE by the MAU. When the MAU is operating in the monitor mode, data appearing on the medium is sent to the DTE by the MAU as during the normal mode. *signal_quality_error* is also asserted on the AUI as during operation in the normal mode. However, in the monitor mode, the means employed to impress data on the physical medium is positively prevented from affecting the medium. Since signaling and isolation techniques differ from medium to medium, the manner in which this positive isolation of the transmitting means is accomplished is specified in the appropriate MAU document. However, the intent of this positive isolation of the transmitter is to ensure that the MAU will not interfere with the physical medium in such a way as to affect transmission of other stations even in the event of failure of the normal transmitter disabling control paths within the transmitting mechanism of the MAU.

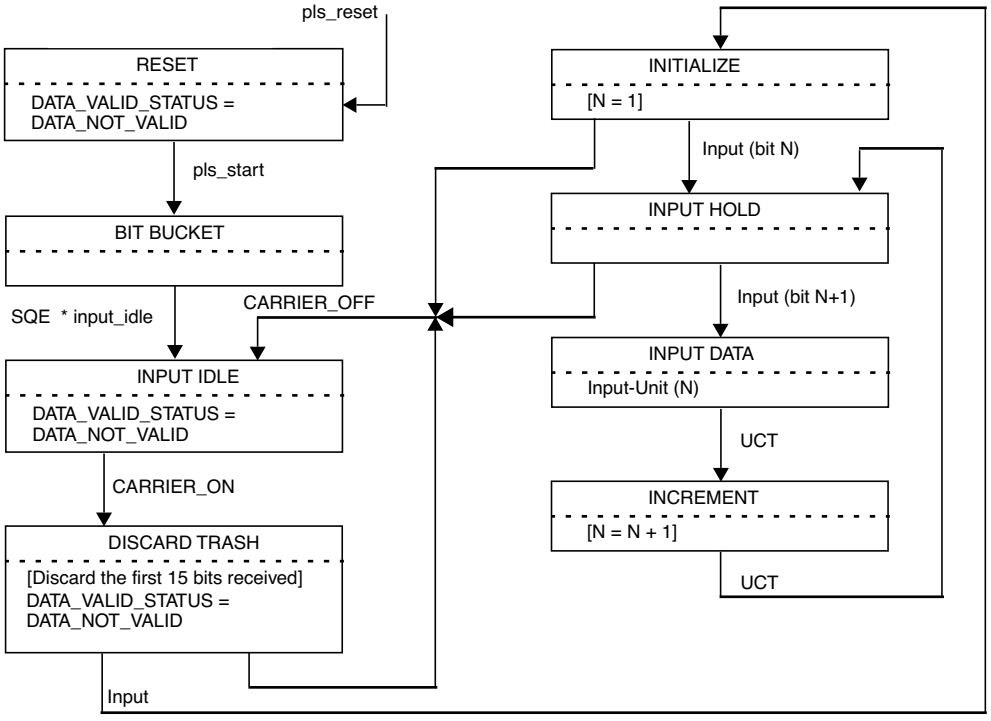


Figure 7–6—PLS Input and Data_Valid function

The monitor mode is intended to permit a network station to determine if it is the source of interference observed on the medium.

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NOTE—The monitor mode is intended to be used only by Network Management for fault isolation and network operation verification. It is intended that the *isolate* message provide direct control over the mode function so that these tasks can be performed. IMPROPER USE OF THE ISOLATE FUNCTION CAN CAUSE ERRONEOUS FRAMES. Clause 5, Layer Management, provides details on the proper use of this function.

7.2.4.3 Output function

The PLS sublayer Output function transparently performs the tasks of conditioning the MAU for output and data transfer from the MAC sublayer to the MAU. The state diagram of Figure 7–5 depicts the Output function operation.

At the conclusion of the Output function, if a collision has not occurred, a test is performed to verify operation of the signal quality detection mechanism in the MAU and to verify the ability of the AUI to pass the *signal_quality_error* message to the PLS sublayer. The operation of this test in the DTE is shown in Figure 7–8.

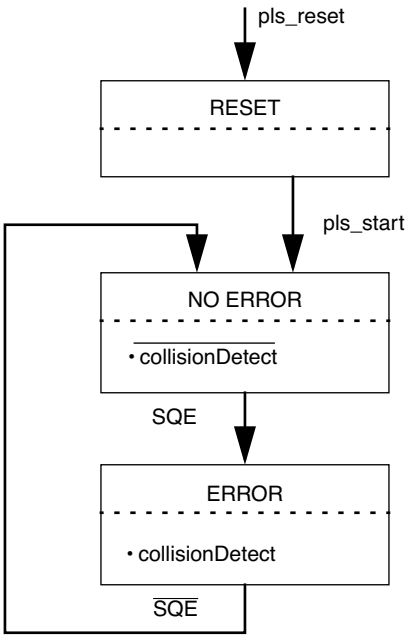
NOTE—In systems operating in full duplex mode, it is permitted, but not required, to implement the *signal_quality_error* message test.

7.2.4.4 Input function

The PLS sublayer Input function transparently performs the task of data transfer from the MAU to the MAC sublayer. Additionally, the Input function sends DATA_VALID_STATUS to the MAC sublayer, as appropriate. The state diagram of Figure 7–6 depicts the Input function operation.

7.2.4.5 Error Sense function

The PLS sublayer Error Sense function performs the task of sending collisionDetect to the MAC sublayer whenever the PLS receives the *signal_quality_error* message from the PMA sublayer. The state diagram of Figure 7–7 depicts the Error Sense function operation.



NOTE—SQE = *signal_quality_error*

Figure 7–7—PLS Error Sense function

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7.2.4.6 Carrier Sense function

The PLS sublayer Carrier Sense function performs the task of sending carrierSense and sqeTestError to the MAC sublayer. The state diagram of Figure 7–8 depicts the Carrier Sense function operation.[19]

Verification of the *signal_quality_error* detection mechanism occurs in the following manner (in the absence of a fault on the medium):

a) At the conclusion of the Output function, the DTE opens a time window during which it expects to see the *signal_quality_error* message asserted on the Control In circuit. The time window begins when carrierSense de-asserts and the variable transmitting is false. The duration of the window shall be at least 4.0 μs but no more than 8.0 μs. During the time window (depicted as carrier_inhibit_timer, Figure 7–8) the carrierSense function is inhibited.
b) The MAU, upon waiting Tw after the conclusion of output, activates as much of the *signal_quality_error* detecting mechanism as is possible without placing signals on the medium, thus sending the *signal_quality_error* message across the AUI for 10 ± 5 bit times (10/BR ± 5/BR seconds).
c) The DTE interprets the reception of the *signal_quality_error* message from the MAU as indication that the *signal_quality_error* detecting mechanism is operational and the *signal_quality_error* message may be both sent by the MAU and received by the DTE.

NOTE 1—The occurrence of multiple (overlapping) transmitters on the medium during the time that the test window is open, as specified above, will satisfy the test and will verify proper operation of the signal quality error detecting mechanism and sending and receiving of the appropriate physical error message.

NOTE 2—If *signal_quality_error* exists at the DTE before CARRIER_OFF occurs, then the Collision Presence test sequence within the PLS as described in 7.2.4.3 above shall be aborted as shown in Figure 7–8.

NOTE 3—In systems operating in full duplex mode, it is permitted, but not required, to implement the *signal_quality_error* message test.

7.3 Signal characteristics

7.3.1 Signal encoding

Two different signal encoding mechanisms may be used by the AUI. One of the mechanisms is used to encode data, the other to encode control.

7.3.1.1 Data encoding

Manchester encoding is used for the transmission of data across the AUI. Manchester encoding is a binary signaling mechanism that combines data and clock into "bit-symbols." Each bit-symbol is split into two halves with the second half containing the binary inverse of the first half; a transition always occurs in the middle of each bit-symbol. During the first half of the bit-symbol, the encoded signal is the logical complement of the bit value being encoded. During the second half of the bit-symbol, the encoded signal is the uncomplemented value of the bit being encoded. Thus, a CD0 is encoded as a bit-symbol in which the first half is HI and the second half is LO. A CD1 is encoded as a bit-symbol in which the first half is LO and the second half is HI. Examples of Manchester waveforms are shown in Figure 7–10.

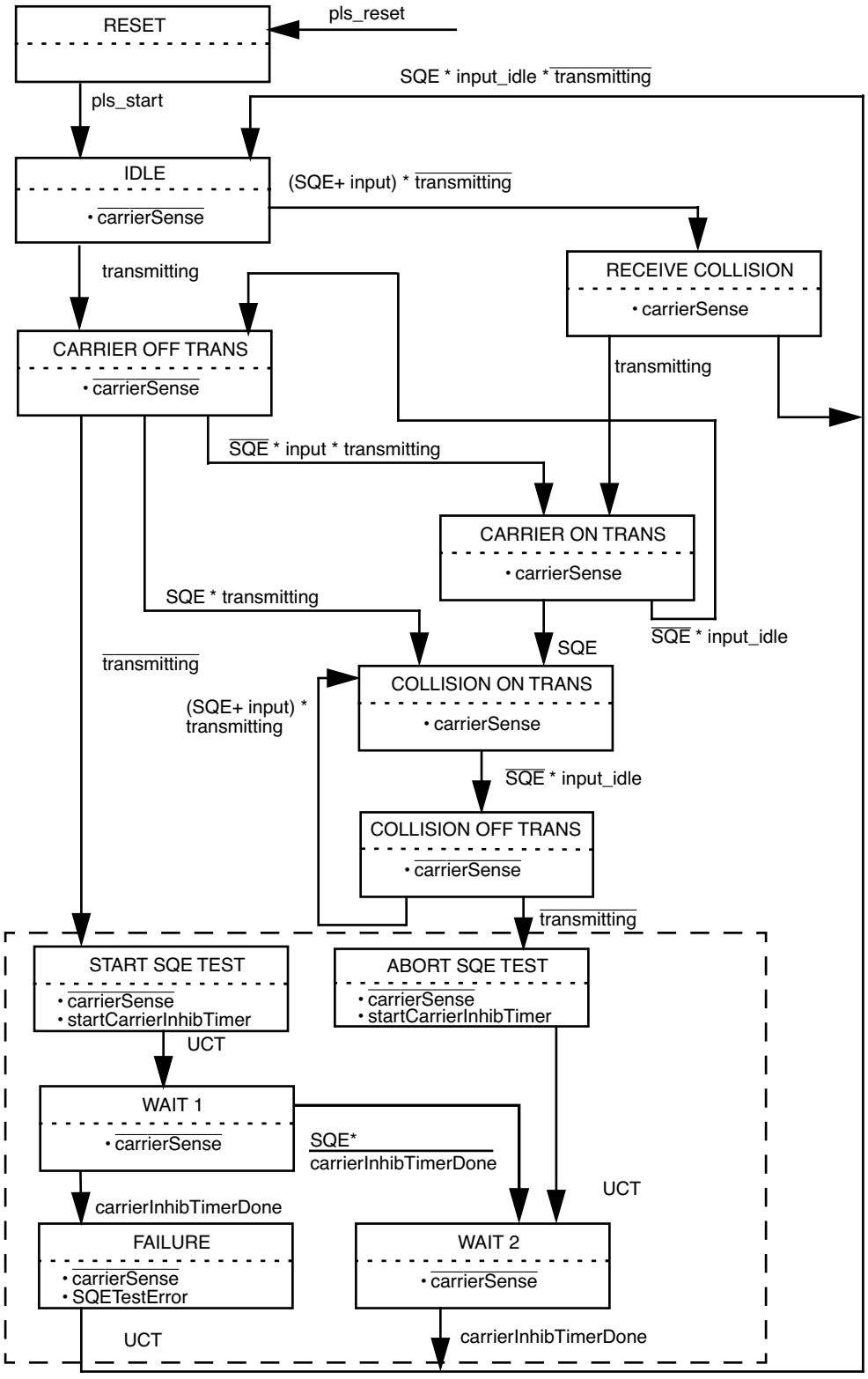
[19]Formerly, this function utilized the variable output_in_progress generated by the PLS output function described in Figure 7–5. For the sake of consistency with common implementation practice, the variable transmitting (see 4.3.3) is utilized directly by the PLS Carrier Sense function in recent editions of the standard.

The mapping between variable output_in_progress and the variable transmitting is as follows. When output_in_progress is true, transmitting is true; when output_in_progress is false, transmitting is false.

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NOTE 1—UCT is unconditional transition; SQE is *signal_quality_error*.
NOTE 2—States within the dotted box are not implemented for the PLS sublayer within a repeater port.

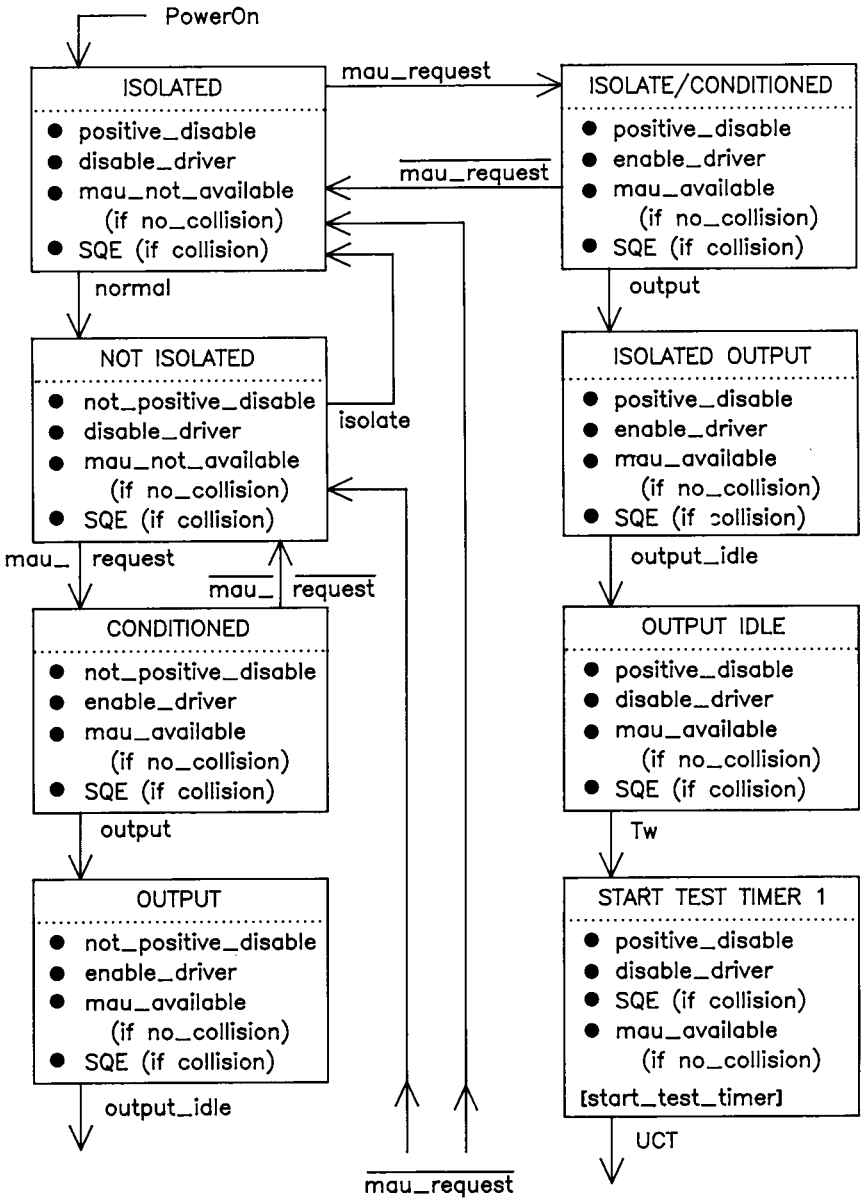
Figure 7–8—PLS Carrier Sense function

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NOTE—See Figure 8–2 and Figure 8–3 for simple and isolate type MAUs.

a)

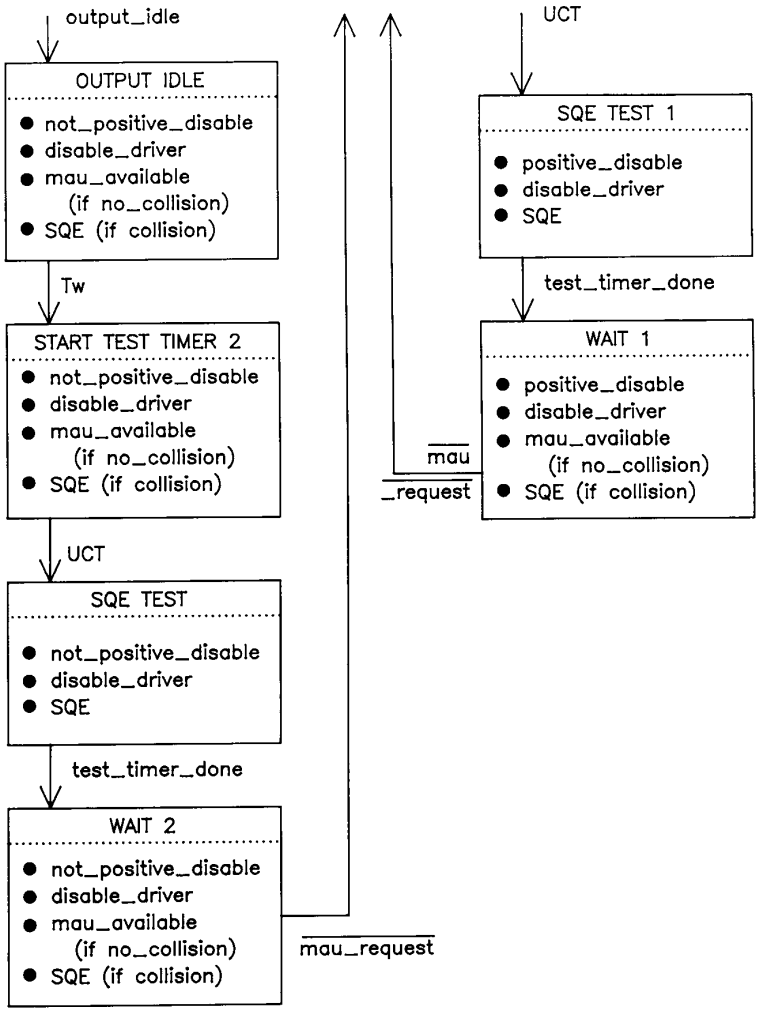
Figure 7–9—Interface function for MAU with conditioning

The line condition IDL is also used as an encoded signal. An IDL always starts with a HI signal level. Since IDL always starts with a HI signal, an additional transition will be added to the data stream if the last bit sent was a zero. This transition cannot be confused with clocked data (CD0 or CD1) since the transition will occur at the start of a bit cell. There will be no transition in the middle of the bit cell. The IDL condition, as sent by a driver, shall be maintained for a minimum of 2 bit times. The IDL condition shall be detected within l.6 bit times at the receiving device.

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NOTE—See Figure 8–2 and Figure 8–3 for simple and isolate type MAUs.

b)

Figure 7–9—*(Continued)* Interface function for MAU with conditioning

a) System jitter considerations make detection of IDL (etd, end transmission delimiter) earlier than 1.3 bit times impractical. The specific implementation of the phase-locked loop or equivalent clock recovery mechanism determines the lower bound on the actual IDL detection time. Adequate margin between lower bound and 1.6 bit times should be considered.

b) Recovery of timing implicit in the data is easily accomplished at the receiving side of the interface because of the wealth of binary transitions guaranteed to be in the encoded waveform, independent of the data sequence. A phase-locked loop or equivalent mechanism maintains continuous tracking of the phase of the information on the Data circuit.

7.3.1.2 Control encoding

A simpler encoding mechanism is used for control signaling than for data signaling. The encoded symbols used in this signaling mechanism are CS0, CS1, and IDL. The CS0 signal is a signal stream of frequency equal to the bit rate (BR). The CS1 signal is a signal stream of frequency equal to half of the bit rate (BR/2). If the interface supports more then one bit rate (see 4.2), the bit rate in use on the data circuits is the one to

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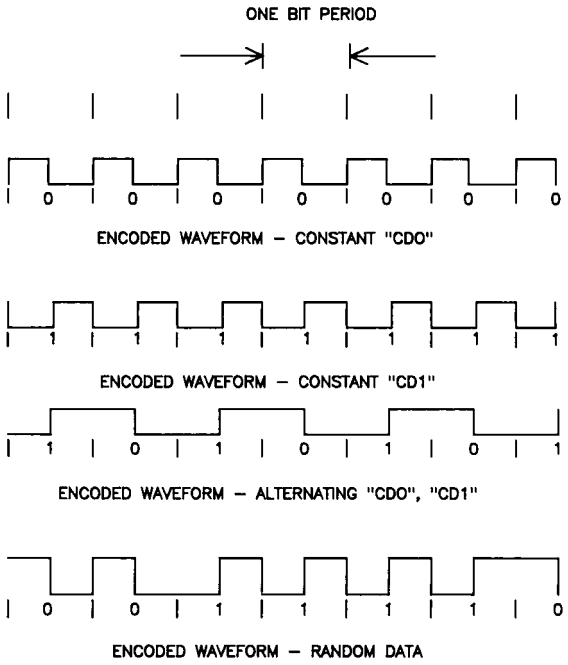


Figure 7–10—Examples of Manchester waveforms

which the control signals are referenced. The IDL signal used on the control circuits is the same as the IDL signal defined for the data circuits (see 7.3.1.1). The Control Out circuit is optional (O) as is one message on Control In.

The frequency tolerance of the CS1 and CS0 signals on the CO circuit shall be ±5% and that of the CS1 signal on the CI circuit shall be ±15%. The duty cycle of the above signals is nominally 50%/50% and shall be no worse than 60%/40%. The CS0 signal on the CI circuit shall have a frequency tolerance of BR +25%, –15% with the pulse widths no less than 35 ns and no greater than 70 ns at the zero crossing points.

The meaning of the signals on the Control Out circuit (DTE to MAU) are as follows:

Signal	Message	Description
IDL	normal	Instructs the MAU to enter (remain in) normal mode
CS1	*mau_request* (O)	Requests that the MAU should be made available
CS0	*isolate* (O)	Instructs the MAU to enter (remain in) monitor mode

The meaning of the signals on the Control In circuit (MAU to DTE) are as follows:

Signal	Message	Description
IDL	mau_available	Indicates that the MAUs ready to output data
CS1	mau_not_available	Indicates that the MAU is not ready to output data
CS0	s*ignal_quality_error*	Indicates that the MAU has detected an error output data

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7.3.2 Signaling rate

Multiple signaling rates are encompassed by this standard. The signaling rate specified here is 10 million bits per second ±0.01%.

It is intended that a given MDI operate at a single data rate. It is not precluded that specific DTE and MAU designs be manually switched or set to alternate rates. A given local network shall operate at a single signaling rate. To facilitate the configuration of operational systems, DTE and MAU devices shall be labeled with the actual signaling rate used with that device.

7.3.3 Signaling levels

Exact voltage and current specifications are listed in 7.4.

7.4 Electrical characteristics

Terms BR and BR/2 have very specific meaning as used in this subclause. The term BR is used to mean the bit rate of the highest signaling rate supported by any one implementation of this interface, BR/2 is used to mean half the bit rate of the lowest signaling rate supported by any one implementation of this interface (see 7.3.2). An interface may support one or more signaling rates.

NOTE—The characteristics of the driver and receiver can be achieved with standard ECL logic with the addition of an appropriate coupling network; however, this implementation is not mandatory.

7.4.1 Driver characteristics

The driver is a differential driver capable of driving the specified 78 Ω interface cable. Only the parameters necessary to ensure compatibility with the specified receiver and to assure personnel safety at the interface connector are specified in the following subclauses.

7.4.1.1 Differential output voltage, loaded

Drivers shall meet all requirements of this subclause under *two* basic sets of test conditions (that is, each of two resistive values). For drivers located within a DTE, a combined inductive load of 27 μH ± 1% and either a 73 Ω or 83 Ω ± 1% resistive load shall be used. For a driver located within a MAU, a combined inductive load of 50 μH ± 1% and either 73 Ω or 83 Ω ± 1% resistive load shall be used.

The differential output voltage, V_{dm}, is alternately positive and negative in magnitude with respect to zero voltage. The value of V_{dm} into either of the two test loads identified above (R = 73 Ω or 83 Ω ± 1%) at the interface connector of the driving unit shall satisfy conditions defined by values V_{min} and V_{max} shown in Figure 7–11 for signals in between BR and BR/2 meeting the frequency and duty cycle tolerances specified for the signal being driven. The procedure for measuring and applying the test condition is as follows:

a) Construct a template representing the shaded area of Figure 7–11. Once constructed, the template may be shifted along the time axis in order to accommodate differences in the 10% to 50% and 50% to 90% transition times of the driver waveform.
b) Find the peak value of V_{dm}. This is V_{max}.
c) Find the minimum value of V_{dm} during the period between the shaded regions for the waveform's rising and falling transitions (time T1 in Figure 7–11). This minimum value is V_{min}.
d) V_{max} shall be < 1315 mV, V_{min} shall be > 450 mV, and V_{max}/V_{min} shall be < 1.37.
e) V_{dm} shall remain < 1170 mV 24 ns after a zero crossing.
f) The waveform shall remain within the shaded area limits.

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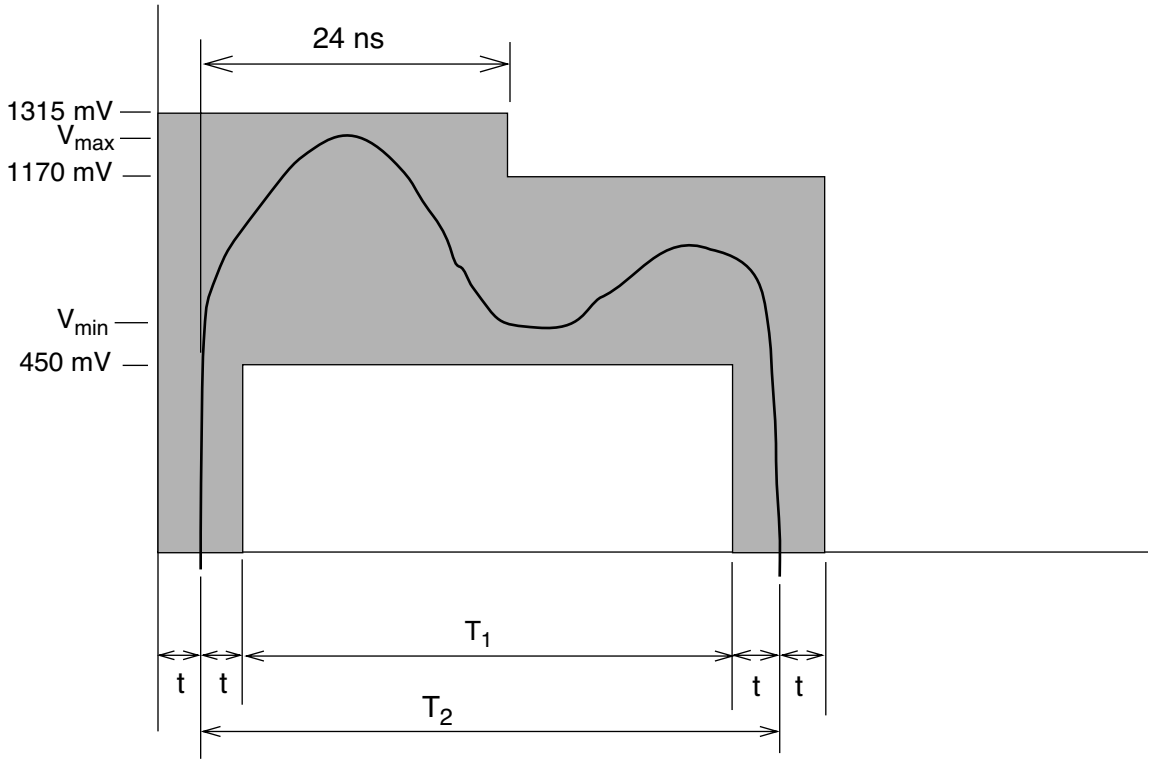
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The differential output voltage magnitude, V_{dm}, into either of the two test loads identified above, at the interface connector of the driving unit during the idle state shall be within 40 mV of 0 V. The current into either of the two test loads shall be limited to 4 mA.

When a driver, connected to the appropriate two test loads identified above, enters the idle state, it shall maintain a minimum differential output voltage of at least 380 mV for at least 2 bit times after the last low to high transition.



t = 3.5 ns at 1–10 MHz data rates
T_2 = (BT or BT/2) ± 2 × T_j, where T_j is the amount of MAU–DTE permissible edge jitter
T_1 = T_2 – 7.0 ns



Figure 7–11—Differential output voltage, loaded

For drivers on either the CO or CI circuits, the first transition or the last positive going transition may occur asynchronously with respect to the timing of the following transitions or the preceding transition(s), respectively.

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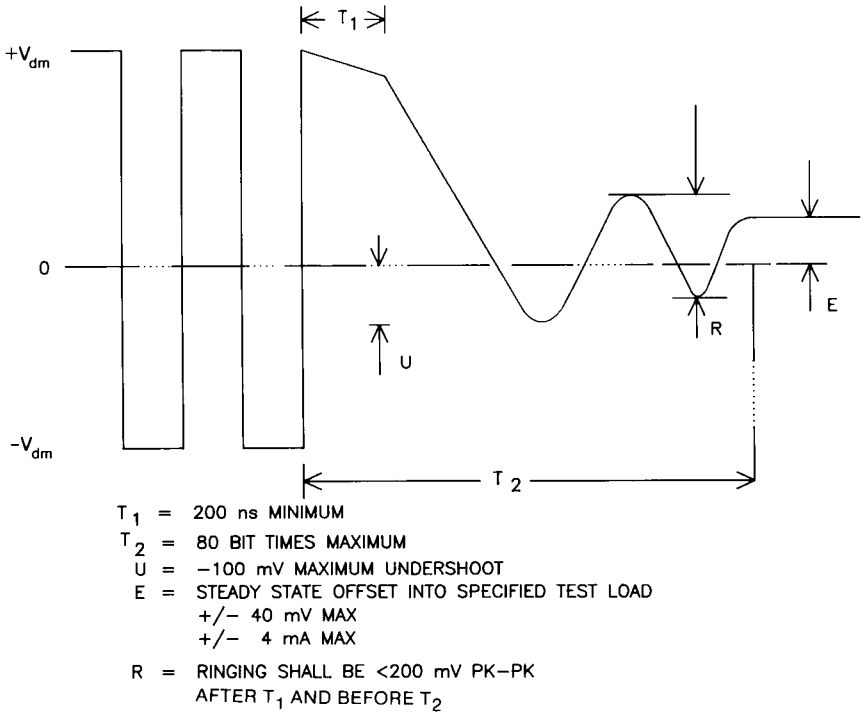


Figure 7–12—Generalized driver waveform

7.4.1.2 Requirements after idle

When the driver becomes nonidle after a period of idle on the interface circuit, the differential output voltage at the interface connector shall meet the requirements of 7.4.1.1 beginning with the second bit transmitted.The first bit sent over the driver circuit may contain phase violations or invalid data.

7.4.1.3 AC common-mode output voltage

The magnitude of the ac component of the common-mode output voltage of the driver, measured between the midpoint of a test load consisting of a pair of matched 39 Ω ± 1% resistors and circuit VC, as shown in Figure 7–13, shall not exceed 2.5 V peak from 30 Hz to 40 kHz and 160 mV peak from 40 kHz to BR.

7.4.1.4 Differential output voltage, open circuit

The differential output voltage into an open circuit, measured at the interface connector of the driving unit, shall not exceed 13 V peak.

7.4.1.5 DC common-mode output voltage

The magnitude of the dc component of the common-mode output voltage of the driver, measured between the midpoint of a test load consisting of a pair of matched 39 Ω ± 1% resistors and circuit VC, as shown in Figure 7–13, shall not exceed 5.5 V.

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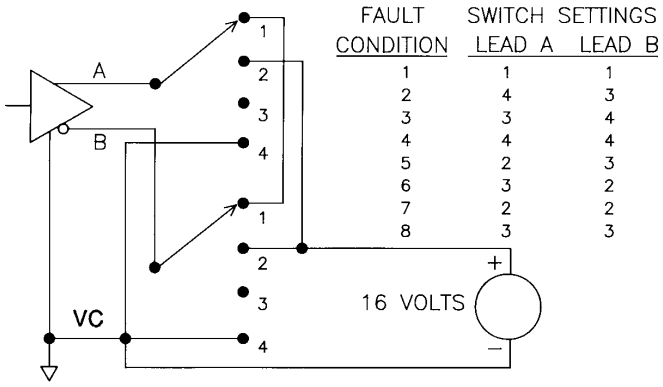


Figure 7–13—Common-mode output voltage

7.4.1.6 Fault tolerance

Any single driver in the interface, when idle or driving any permissible signal, shall tolerate the application of each of the faults specified by the switch settings in Figure 7–14 indefinitely; and after the fault condition is removed, the operation of the driver, according to the specifications of 7.4.1.1 through 7.4.1.5, shall not be impaired.

In addition, the magnitude of the output current from either output of the driver under any of the fault conditions specified shall not exceed 150 mA.

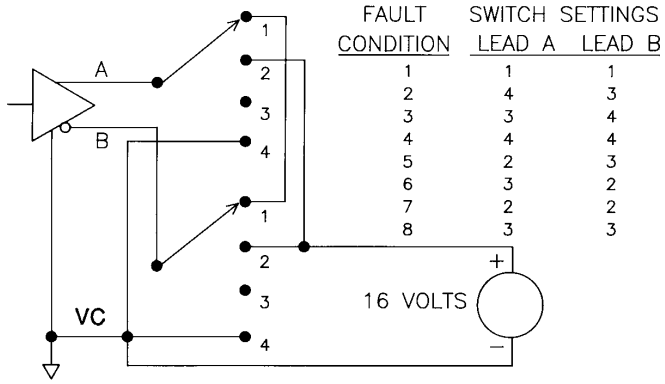


Figure 7–14—Driver fault conditions

7.4.2 Receiver characteristics

The receiver specified terminates the interface cable in its characteristic impedance. The receiver shall function normally over the specified dc and ac common-mode ranges.

7.4.2.1 Receiver threshold levels

When the receiving interface circuit at the interface connector of the receiving equipment is driven by a differential input signal at either BR or BR/2 meeting the frequency and duty cycle tolerances specified for the receiving circuit, when the A lead is 160 mV positive with respect to the B lead, the interface circuit is in the

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HI state, and when the A lead is 160 mV negative with respect to the B lead, the interface circuit is in the LO state. The receiver output shall assume the intended HI and LO states for the corresponding input conditions.

If the receiver has a squelch feature, the specified receive threshold levels apply only when the squelch is allowing the signal to pass through the receiver.

NOTE—The specified threshold levels do not take precedence over the duty cycle and jitter tolerance specified elsewhere. Both sets of specifications must be met.

7.4.2.2 AC differential input impedance

The ac differential input impedance for AUI receivers located in MAUs shall have a real part of 77.83 Ω ± 6%, with the sign of the imaginary part positive, and the phase angle of the impedance in degrees less than or equal to 0.0338 times the real part of the impedance, when measured with a 10 MHz sine wave.

The ac differential input impedance for AUI receivers located in the DTE shall have a real part of 77.95 Ω ± 6%, with the sign of the imaginary part positive, and the phase angle of the impedance in degrees less than or equal to 0.0183 times the real part of the impedance, when measured with a 10 MHz sine wave.

A 78 Ω ± 6% resistor in parallel with an inductance of greater than 27 μH or 50 μH for receivers in the MAU and DTE respectively, satisfies this requirement.

7.4.2.3 AC common-mode range

When the receiving interface circuit at the receiving equipment is driven by a differential input signal at either BR or BR/2 meeting the frequency and duty cycle tolerances specified for the circuit being driven, the receiver output shall assume the proper output state as specified in 7.4.2.1, in the presence of a peak common-mode ac sine wave voltage either of from 30 Hz to 40 kHz referenced to circuit VC in magnitude from 0 to 3 V, or in magnitude 0 to 200 mV for ac voltages of from 40 kHz to BR as shown in Figure 7–15.

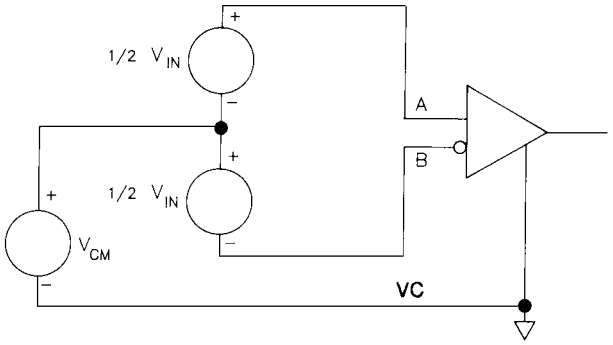


Figure 7–15—Common-mode input test

7.4.2.4 Total common-mode range

When the receiving interface circuit at the receiving equipment is driven by a differential input signal at either BR or BR/2 meeting the frequency and duty cycle tolerances specified for the circuit being driven, the receiver output shall assume the intended output state as specified in 7.4.2.1 in the presence of a total common-mode voltage, dc plus ac, referenced to circuit VC in magnitude from 0 to 5.5 V, as shown in the test setup of Figure 7–15. The ac component shall not exceed the requirements of 7.4.2.3.

The receiver shall be so designed that the magnitude of the current from the common-mode voltage source used in the test shall not exceed 1 mA.

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7.4.2.5 Idle input behavior

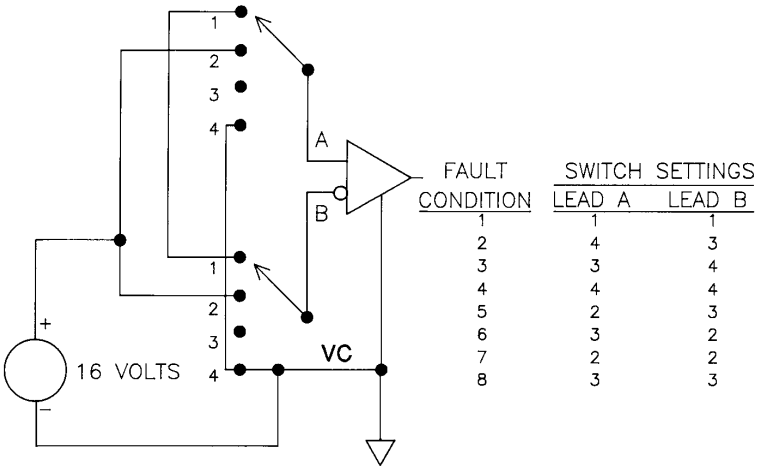
When the receiver becomes nonidle after a period of idle on the interface circuit, the characteristics of the signal at the output of the receiver shall stabilize within the startup delay allowed for the device incorporating the receiver so that it is not prevented from meeting the jitter specifications established for that device.

The receiving unit shall take precautions to ensure that a HI to idle transition is not falsely interpreted as an idle to nonidle transition, even in the presence of signal droop due to ac coupling in the interface driver or receiver circuits.

7.4.2.6 Fault tolerance

Any single receiver in the interface shall tolerate the application of each of the faults specified by the switch settings in Figure 7–16 indefinitely, and after the fault condition is removed, the operation of the receiver according to the specifications of 7.4.2.1 through 7.4.2.6 shall not be impaired.

In addition, the magnitude of the current into either input of the receiver under any of the fault conditions specified shall not exceed 3 mA.



FAULT CONDITION	SWITCH SETTINGS LEAD A	LEAD B
1	1	1
2	4	3
3	3	4
4	4	4
5	2	3
6	3	2
7	2	2
8	3	3

Figure 7–16—Receiver fault conditions

7.4.3 AUI cable characteristics

The interface cable consists of individually shielded twisted pairs of wires with an overall shield covering these individual shielded wire pairs. These shields must provide sufficient shielding to meet the requirements of protection against rf interference and the following cable parameters. Individual shields for each signal pair are electrically isolated from the outer shield but not necessarily from each other.

The overall shield shall be returned to the MAU and DTE Units via the AUI connector shell as defined in 7.6.2 and 7.6.3. If a common drain wire is used for all the signal pair shields, then it shall be connected to pin 4 and pin 1. Individual drain wire returns for each signal pair may be used (see 7.6.3). It is recommended that individual drain wires be used on all control and data circuit shields to meet satisfactory crosstalk levels. If individual drain wires are used, they shall be interconnected within the AUI cable at each end and shall be connected at least to pin 4 and pin 1 at each end of the cable.

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The presence of the Control Out signal pair is optional. If driver or receiver circuit components for CO are not provided, consideration should be given to properly terminating the CO signal pair within the DTE and MAU to preclude erroneous operation.

7.4.3.1 Conductor size

The dc power pair in the interconnecting cable, voltage common and voltage minus, shall be composed of a twisted pair of sufficient gauge stranded wires to result in a nominal dc resistance not to exceed 1.75 Ω per conductor.

Conductor size for the signal pairs shall be determined according to the ac related parameters in 7.4.3.2 through 7.4.3.6.

7.4.3.2 Pair-to-pair balanced crosstalk

The balanced crosstalk from one pair of wires to any other pair in the same cable sheath (when each pair is driven per 7.4.1.1 through 7.4.1.5) shall have a minimum value of 40 dB of attenuation measured over the range of BR/2 to BR.

7.4.3.3 Differential characteristic impedance

The differential characteristic impedance for all signal pairs shall be equal within 3 Ω and shall be 78 ± 5 Ω measured at a frequency of BR.

7.4.3.4 Transfer impedance

a) The common-mode transfer impedance shall not exceed the values shown in Figure 7–17 over the indicated frequency range.
b) The differential mode transfer impedance for all pairs shall be at least 20 dB below the common-mode transfer impedance.

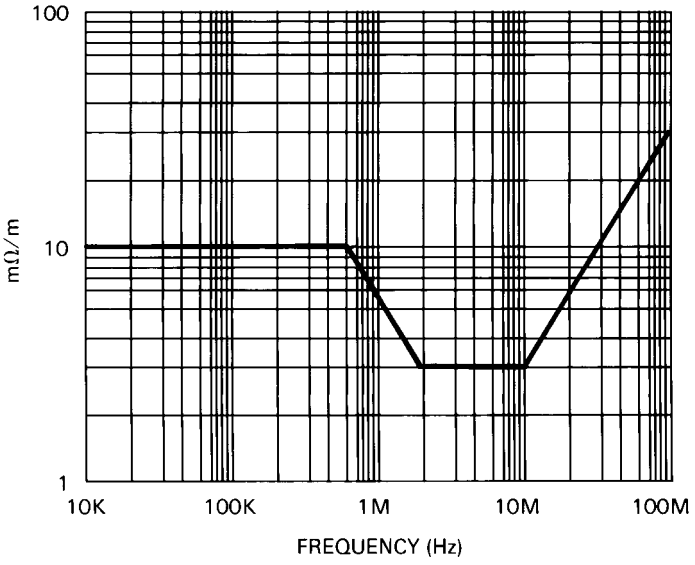


Figure 7–17—Common-mode transfer impedance

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7.4.3.5 Attenuation

Total cable attenuation levels between driver and receiver (at separate stations) for each signal pair shall not exceed 3 dB over the frequency range of BR/2 to BR (Hz) for sinewave measurements.

7.4.3.6 Timing jitter

Cable meeting this specification shall exhibit edge jitter of no more than 1.5 ns at the receiving end when the longest legal length of the cable as specified in 7.4.3.1 through 7.4.3.7 is terminated in a 78 Ω ± 1% resistor at the receiving end and is driven with pseudorandom Manchester encoded binary data from a data generator which exhibits no more than 0.5 ns of edge jitter on half bit cells of exactly 1/2 BT and whose output meets the specifications of 7.4.1.1 through 7.4.1.5. This test shall be conducted in a noise-free environment. The above specified component is not to introduce more than 1 ns of edge jitter into the system.

NOTE—Special attention will have to be applied to the cable characteristics and length at 20 Mb/s.

7.4.3.7 Delay

Total signal delay between driver and receiver (at separate stations) for each signal pair shall not exceed 257 ns.

7.5 Functional description of interchange circuits

7.5.1 General

The AUI consists of either three or four differential signal circuits, power, and ground. Two of the circuits carry encoded data and two carry encoded control information. Circuits DO (Data Out) and CO (Control Out) are sourced by the DTE, and circuits DI (Data In) and CI (Control In) are sourced by the MAU. The interface also provides for power transfer from the DTE to the MAU. The CO circuit is optional.

7.5.2 Definition of interchange circuits

The following circuits are defined by this specification:

Circuit	Name	Signal direction		Remarks
		to MAU	from MAU	
DO	Data Out	X		Encoded Data
DI	Data In		X	Encoded Data
CO	Control Out	X		Encoded Control
CI	Control In		X	Encoded Control
VP	Voltage Plus	X		12 V
VC	Voltage Common	X		Return for VP
PG	Protective Ground	X		Shield

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7.5.2.1 Circuit DO–Data Out

The Data Out (DO) circuit is sourced by the DTE. It is a differential pair consisting of DO-A (Data Out circuit A) and DO-B (Data Out circuit B).

The signal transferred over this circuit is Manchester encoded. An *output* message containing a one bit is encoded as CD1. An *output_idle* message is encoded as an IDL.

The following symmetry requirements shall be met when the DTE transfers pseudorandom Manchester encoded binary data over a DO circuit loaded by the test load specified in 7.4.1.1.

Bit cells generated internal to the DTE are required to be 1 BT within the permitted tolerance on data rate specified in 7.3.2. Half bit cells in each data bit are the be exactly 1/2 BT (that is, the reference point for edge jitter measurements) within the permitted tolerance on the data rate specified in 7.3.2. Each transition on the DO circuit is permitted to exhibit edge jitter not to exceed 0.5 ns in each direction. This means that any transition may occur up to 0.5 ns earlier or later than this transition would have occurred had no edge jitter occurred on this signal.

7.5.2.2 Circuit DI–Data In

The Data In (DI) circuit is sourced by the MAU. It is a differential pair consisting of DI-A (Data In circuit A) and DI-B (Data In circuit B).

The signal transferred over this circuit is Manchester encoded. An *input* message containing a zero bit is encoded as CD0. An *input* message containing a one bit is encoded as CD1. An *input_idle* message is encoded as an IDL.

A DTE meeting this specification shall be able to receive, on the DI circuit without a detectable FCS error, normal preamble data arranged in legal length packets as sent by another station to the DTE. The test generator for the data on the DI circuit shall meet the requirements for drivers in MAUs specified in 7.4.1.1 through 7.4.1.5 and shall drive the DI circuit through a zero length AUI cable. Random amounts of edge jitter from 0 to 12 ns on either side of each transition shall be added by the test generator to transitions in bits in the preamble, and random amounts of edge jitter of from 0 to 18 ns on either side of each transition shall be added to the transitions in all bits in the frame. Preamble length from the test generator shall be 47 bits of preamble, followed by the 8 bit SFD.

NOTE—A significant portion of the system jitter may be nonrandom in nature and consists of a steady-state shift of the midbit transitions in either direction from their nominal placement. A 16.5 ns edge jitter is expected on the transmitted signal at the receiving DTE, worst case. The difference between 16.5 ns and 18 ns jitter represents receiver design margin.

7.5.2.3 Circuit CO–Control Out (optional)

The Control Out (CO) circuit is sourced by the DTE. It is a differential pair consisting of CO-A (Control Out circuit A) and CO-B (Control Out circuit B).

The signal transferred over this circuit is encoded as described in 7.3.1.2. A *mau_request* message is encoded as CS1. A *normal* message is encoded as IDL. An *isolate* message is encoded as CS0.

7.5.2.4 Circuit CI–Control In

The Control In (CI) circuit is sourced by the MAU. It is a differential pair consisting of CI-A (Control In circuit A) and CI-B (Control In circuit B).

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The signal transferred over this circuit is encoded as described in 7.3.1.2. A *mau_available* message is encoded as IDL. A *mau_not_available* message is encoded as CS1. A *signal_quality_error* message is encoded as a CS0.

7.5.2.5 Circuit VP–Voltage Plus

The Voltage Plus (VP) circuit is sourced from the DTE. It shall be capable of operating at one fixed level between + 12 V dc – 6% and + 15 V dc + 5% with respect to circuit VC at the DTE AUI for all currents from 0 to 500 mA. The source shall provide protection for this circuit against an overload condition. The method of overload protection is not specified; however, under no conditions of operation, either normal or overload, shall the source apply a voltage to circuit VP of less than 0 or greater than + 15.75 V dc as specified above. MAU designers are cautioned that protection means employed by power sources may cause the voltage at signal VP to drop below the minimum operational voltage specified without going completely to zero volts when loads drawing in excess of the current supplied are applied between VP and VC. Adequate provisions shall be made to ensure that such a condition does not cause the MAU to disrupt the medium.

7.5.2.6 Circuit VC–Voltage Common

Circuit VC is the ground return to the power source for circuit VP, capable of sinking 2.0 A. Also, all common-mode terminators for AUI circuits shall be made to circuit VC.

7.5.2.7 Circuit PG–Protective Ground

Circuit PG shall be connected to chassis ground through a maximum dc resistance of 20 mΩ at the DTE end.

7.5.2.8 Circuit shield terminations

Individual pin terminations shall meet the following requirements:

a) Pins 1, 4, 8, 11, 14 connected to logic ground in the DTE
b) Pins 1, 4, 8, 11, 14 capacitively coupled to VC in MAU
c) Impedance to ground < 5 Ω at the lowest operational BR/2 in the MAU and at the highest BR in the DTE

7.6 Mechanical characteristics

7.6.1 Definition of mechanical interface

All connectors used shall be as specified in 7.6.2. The DTE shall have a female connector and the MAU shall have a male connector. The MAU may be plugged directly into the DTE or may be connected by one or more cable segments whose total length is less than or equal to 50 m. All cable segments shall have a male connector on one end and a female connector on the other end. All female connectors shall have the slide latch, and all male connectors shall have the locking posts (as defined in Figures 7–18, 7–19, and 7–20) as the retention system.

7.6.2 Line interface connector

A 15-pole connector having the mechanical mateability dimensions as specified in IEC 60807-2: 1992 with gold-plated contacts shall be used for the line interface connector. The shells of these connectors shall be tin plated to ensure the integrity of the cable shield to chassis current path. The resistance of the cable shield to equipment chassis shall not exceed 5 mΩ, after a minimum of 500 cycles of mating and unmaking.

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In order to ensure intermateability of connectors obtained from different manufacturers, the connector with female contacts shall conform to IEC 60807-2: 1992 and have gold-plated contacts and tin-plated shells. All additions to provide for female shell to male shell conductivity shall be on the shell of the connector with male contacts. There should be multiple contact points around the sides of this shell to provide for shield continuity.

NOTE—Use of similar metallic surfaces on connector conductors and similar metallic surfaces on the connector shells minimizes galvanic action and reduced performance.

The connector is not specified to prevent operator contact with the shield, and precautions shall be taken at installation time to ensure that the installer is warned that the shield is not to be brought into contact with any hazardous voltage while being handled by operating personnel. See reference [B30].

7.6.3 Contact assignments

The following table shows the assignment of circuits to connector contacts.

Contact	Circuit	Use
3	DO-A	Data Out circuit A
10	DO-B	Data Out circuit B
11	DO-S	Data Out circuit shield
5	DI-A	Data In circuit A
12	DI-B	Data In circuit B
4	DI-S	Data In circuit shield
7	CO-A	Control Out circuit A
15	CO-B	Control Out circuit B
8	CO-S	Control Out circuit shield
2	CI-A	Control in circuit A
9	CI-B	Control In circuit B
1	CI-S	Control In circuit shield
6	VC	Voltage Common
13	VP	Voltage Plus
14	VS	Voltage Shield
Shell	PG	Protective Ground (Conductive Shell)

NOTE—Voltage Plus and Voltage Common use a single twisted pair in the AUI cable.

As indicated in 7.4.2.1, the A lead of a circuit is positive relative to the B lead for a HI signal and negative for a LO signal.

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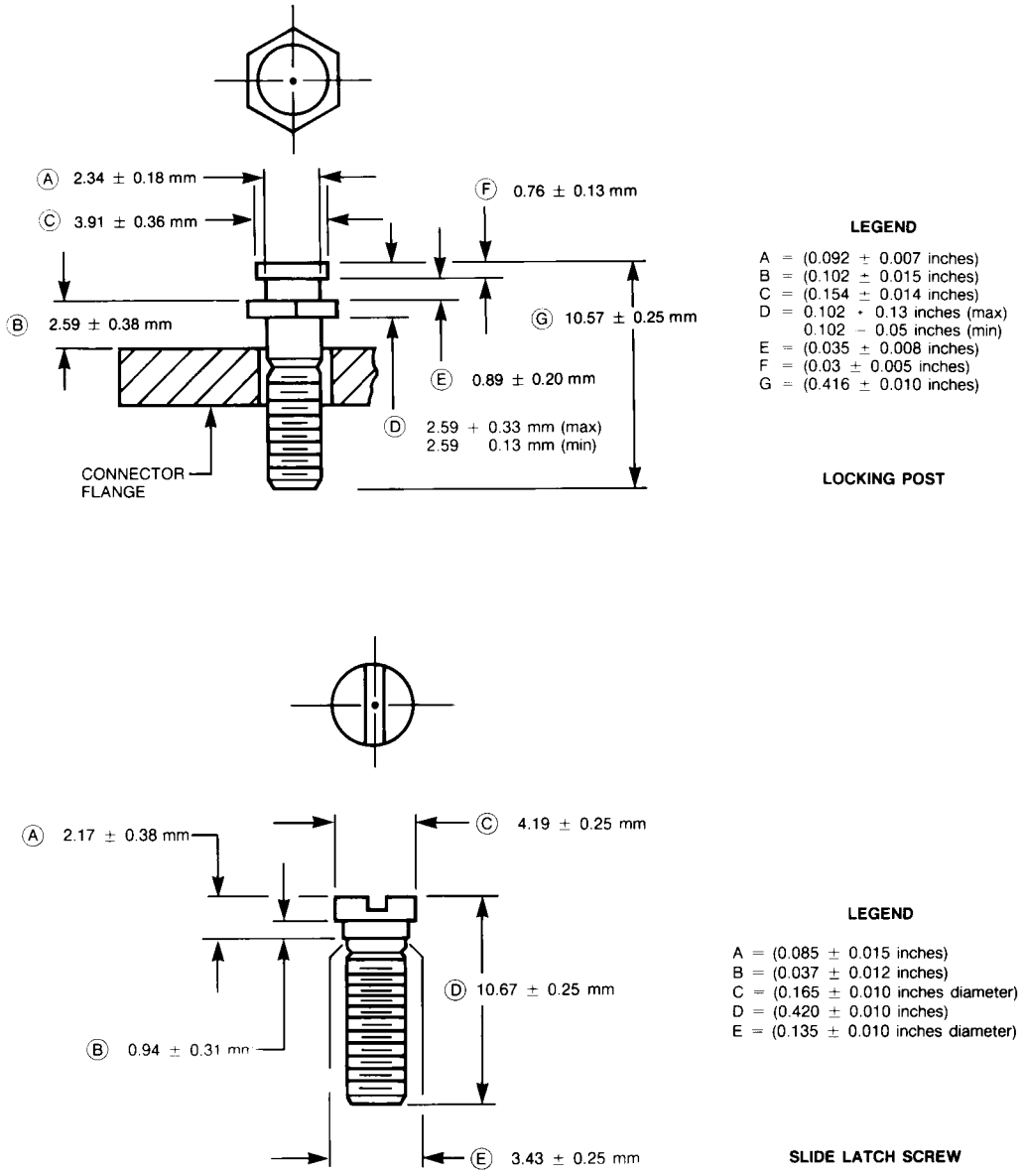


Figure 7–18—Connector locking posts

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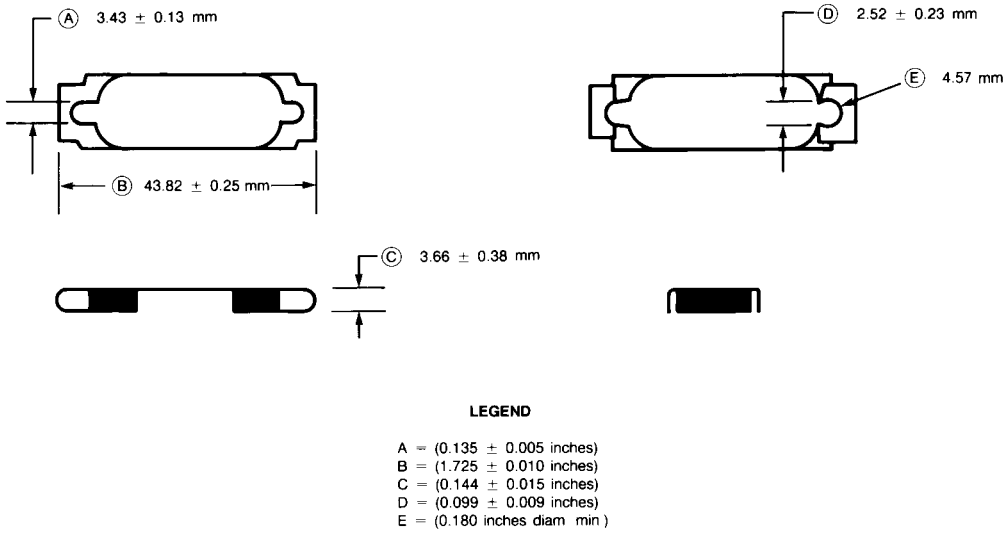


Figure 7–19—Connector slide latch

(material 24 gauge maximum)

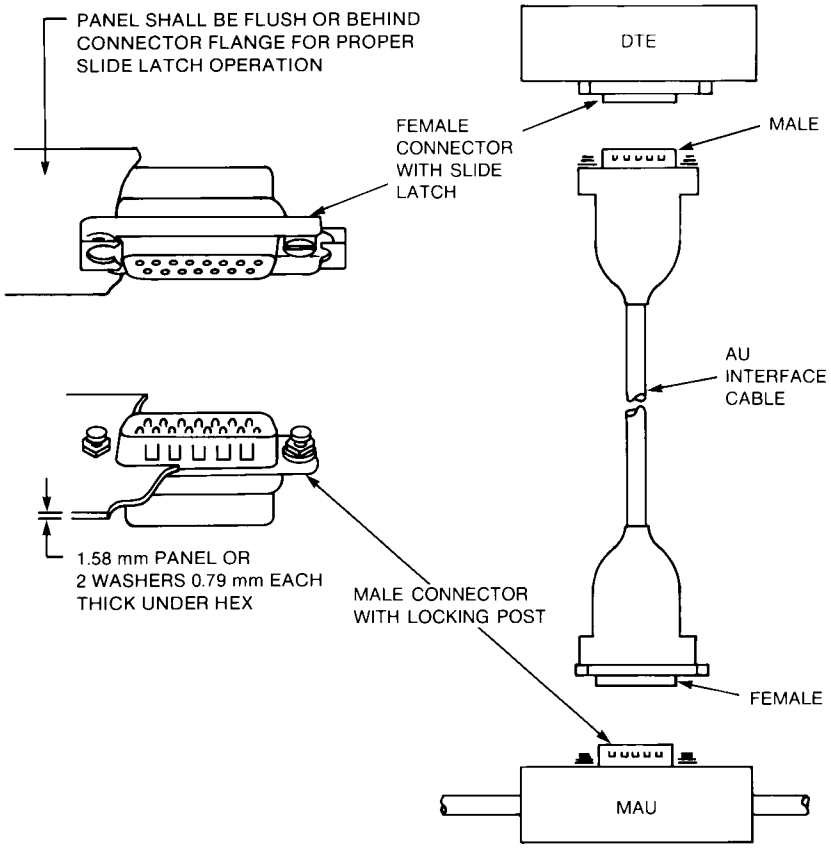


Figure 7–20—Connector hardware and AUI cable configuration

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8. Medium Attachment Unit and baseband medium specifications, type 10BASE5

NOTE—This MAU is not recommended for new installations.

8.1 Scope

8.1.1 Overview

This standard defines the functional, electrical, and mechanical characteristics of the MAU and one specific medium for use with local networks. The relationship of this specification to the entire ISO/IEC Local Network International Standard is shown in Figure 8–1. The purpose of the MAU is to provide a simple, inexpensive, and flexible means of attaching devices to the local network medium.

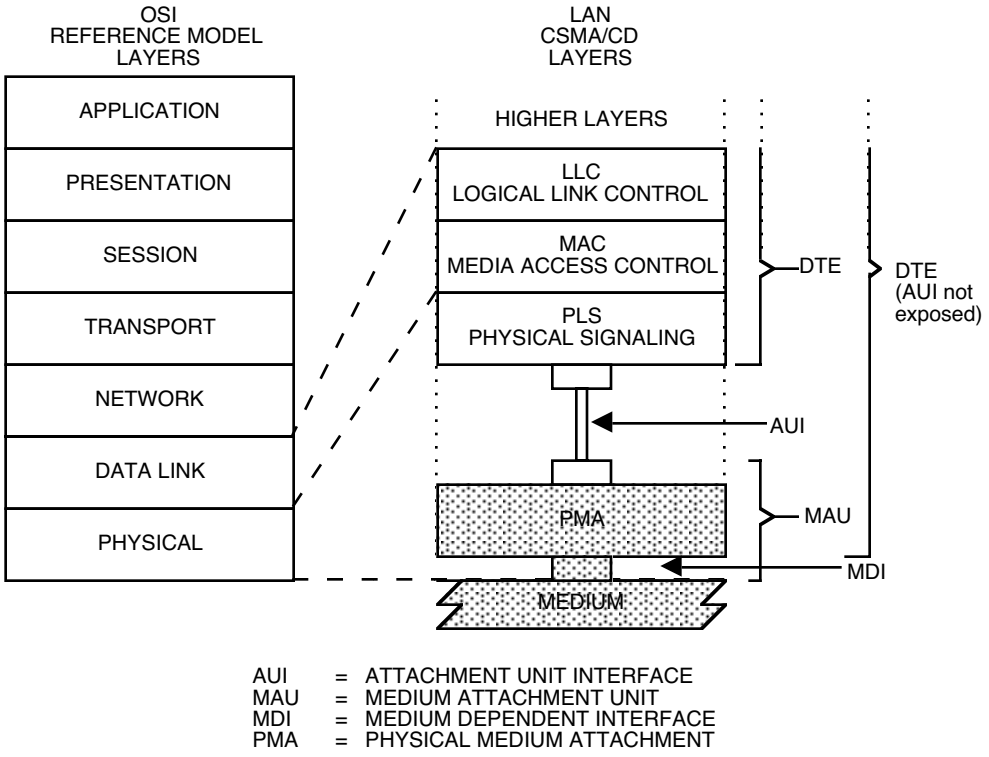


Figure 8–1—Physical Layer partitioning, relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

8.1.1.1 Medium Attachment Unit

The MAU has the following general characteristics:

a) Enables coupling the PLS by way of the AUI to the explicit baseband coaxial transmission system defined in this clause of the standard.
b) Supports message traffic at a data rate of 10 Mb/s (alternative data rates may be considered in future additions to the standard).
c) Provides for driving up to 500 m of coaxial trunk cable without the use of a repeater.
d) Permits the DTE to test the MAU and the medium itself.

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e) Supports system configurations using the CSMA/CD access mechanism defined with baseband signaling.
f) Supports a bus topology interconnection means.

8.1.1.2 Repeater unit

The repeater unit is used to extend the physical system topology, has the same general characteristics as defined in 8.1.1.1, and provides for coupling together two or more 500 m coaxial trunk cable segments. Multiple repeater units are permitted within a single system to provide a maximum trunk cable connection path of 2.5 km between any two MAUs.

8.1.2 Definitions

See 1.4.

8.1.3 Application perspective: MAU and MEDIUM objectives

This subclause states the broad objectives and assumptions underlying the specifications defined throughout this subclause of the standard.

8.1.3.1 Object

a) Provide the physical means for communication between local network data link entities.

NOTE—This standard covers a portion of the physical layer as defined in the OSI Reference Model and, in addition, the physical medium itself, which is beyond the scope of the OSI Reference Model.

b) Define a physical interface that can be implemented independently among different manufacturers of hardware and achieve the intended level of compatibility when interconnected in a common local network.
c) Provide a communication channel capable of high bandwidth and low bit error rate performance. The resultant mean bit error rate, at the physical layer service interface should be less than one part in 10^8 (on the order of one part in 10^9 at the link level).
d) Provide for ease of installation and service.
e) Provide for high network availability (ability of a station to gain access to the medium and enable the data link connection in a timely fashion).
f) Enable relatively low-cost implementations.

8.1.3.2 Compatibility considerations

All implementations of this baseband coaxial system shall be compatible at the MDI.

This standard provides one explicit trunk cable medium specification for the interconnection of all MAU devices. The medium itself, the functional capability of the MAU, and the AUI are defined to provide the highest possible level of compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the MAU in an application-dependent manner provided the MD Interface and AUI specifications are satisfied.

Subsystems based on this specification may be implemented in several different ways provided compatibility at the medium is maintained. It is possible, for example, to design an integrated station where the MAU is contained within a physical DTE system component, thereby eliminating the AUI cable. The device designer (and system user) shall then consider such factors as topological flexibility, system availability, and configurability.

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8.1.3.3 Relationship to PLS and AU interface

This subclause defines the primary physical layer for the LAN, a layer comprised of both the physical medium and the rudimentary circuitry necessary to couple a station's message path directly to/from the medium. The complete logical physical layer of the LAN may reside physically in two distinct locations, the MAU and the DTE. Therefore, a close relationship exists between this subclause and Clause 7. This subclause specifies all of the physical medium parameters, all of the PMA logical functions residing in the physical MAU, and references the AUI associated with and defined throughout Clause 7.

NOTE—The design of a physical MAU component requires the use of both this subclause and Clause 7 for the PLS and AUI specifications.

8.1.3.4 Modes of operation

The MAU is capable of operating in either a "Normal" mode or an optional "Monitor" mode.

a) *Normal mode*. The MAU functions as a direct connection between the baseband medium and the DTE. Data output from the DTE is output to the coaxial trunk medium and all data on the coaxial trunk medium is input to the DTE. This mode is the "normal" mode of operation for the intended message traffic between stations.
b) *Monitor mode*. The MAU Transmit function is disabled to prevent data from being output on the trunk coaxial medium while the receive function and collision presence function remain active for purposes of monitoring medium message traffic. This mode also serves as a limited test mode at the same time it isolates the MAU transmitter from the medium. Under most local (that is, intrastation) fault conditions the monitor mode enables continued use of the network while the local station is being serviced.

8.2 MAU functional specifications

The MAU component provides the means by which signals on the four physically separate AUI signal circuits to/from the DTE and their associated interlayer messages are coupled to the single coaxial cable baseband signal line. To achieve this basic objective, the MAU component contains the following functional capabilities to handle message flow between the DTE and the baseband medium:

a) *Transmit function*. The ability to transmit serial data bit streams on the baseband medium from the local DTE entity and to one or more remote DTE entities on the same network.
b) *Receive function*. The ability to receive serial data bit streams over the baseband medium.
c) *Collision Presence function*. The ability to detect the presence of two or more stations' concurrent transmissions.
d) *Monitor function* (Optional). The ability to inhibit the normal transmit data stream to the medium at the same time the normal receive function and collision presence function remain operational.
e) *Jabber function*. The ability to automatically interrupt the transmit function and inhibit an abnormally long output data stream.

8.2.1 MAU Physical Layer functions

8.2.1.1 Transmit function requirements

At the start of a frame transmission on the coaxial cable, no more than 2 bits (2 full bit cells) of information may be received from the DO circuit and not transmitted onto the coaxial medium. In addition, it is permissible for the first bit sent to contain encoded phase violations or invalid data; however, all successive bits of the frame shall be reproduced with no more than the specified amount of jitter. The second bit cell transmitted onto the coaxial cable shall be carried from the DO signal line and transmitted onto the coaxial trunk

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cable medium with the correct timing and signal levels. The steady-state propagation delay between the DO circuit receiver input and the coaxial cable output shall not exceed one-half bit cell. At the start of transmission, the MAU bit loss plus steady-state propagation delay between the DO and the coaxial cable shall vary by less than 2 bits between successive packets separated by 96 bit times or less. There shall be no logical signal inversions between the branch cable DO circuit and the coaxial trunk cable (for example, a "high" logic level input to the MAU shall result in the less negative current flow value on the trunk coaxial medium). A positive signal on the A signal lead of the DO circuit shall result in a more positive voltage level on the trunk coaxial medium. It is assumed that the AUI shall provide adequate protection against noise. It is recommended that the designer provide an implementation in which a minimum threshold signal is required to establish a transmit bit stream.

The Transmit function shall output a signal on the trunk coaxial medium whose levels and waveform comply with 8.3.1.3.

In addition, when the DO circuit has gone idle after a frame is output, the MAU shall then activate the collision presence function as close to the trunk coaxial cable as possible without introducing an extraneous signal on the trunk coaxial medium. The MAU shall initiate the collision presence state within 0.6 μs to 1.6 μs after the start of the output idle signal and shall maintain an active collision presence state for a time equivalent to 10 ± 5 bit cells.

8.2.1.2 Receive function requirements

The signal from the coaxial trunk cable shall be directly coupled to the receiver and subsequently ac coupled before reaching the receive circuit connected to the DTE. The receive function shall output a signal onto the DI circuit of the AUI cable that complies with the AUI specification for drivers in MAUs.

At the start of a frame reception from the coaxial cable, no more than 5 bits (five full bit cells) of information may be received from the coaxial cable and not transmitted onto the receive (DI) circuit. In addition, it is permissible for the first bit sent over the receive circuit to contain encoded phase violations or invalid data; however, all successive bits of the frame shall reproduce the incoming signal with no more than the above specified amount of jitter. This implies that the second bit cell sent onto the DI circuit presents valid data to the branch cable. The steady-state propagation delay between the coaxial cable and the receive (DI) circuit output shall not exceed one-half bit cell. At the start of reception, the MAU bit loss plus steady-state propagation delay between the coaxial cable and the DI circuit shall vary by less than 5 bits between successive packets separated by 96 bit times or less when the signal level on the coaxial cable is constant (that is, when both packets are transmitted by the same MAU). There are no logical signal inversions between the coaxial (trunk) cable and the MAU (branch) cable receive circuit.

A MAU meeting this specification shall exhibit edge jitter into the DI pair when terminated in the appropriate test load specified in 7.4.3.6, of no more than 8.0 ns in either direction when it is installed on the distant end of all lengths between 2.5 m and 500 m of the cable specified in 8.4.1.1 through 8.4.2.1.5 terminated at both ends with terminators meeting the impedance requirements of 8.5.2.1 and driven at one end with pseudorandom Manchester encoded binary data from a data generator that exhibits no more than 1.0 ns of edge jitter in either direction on half-bit cells of exactly 1/2 BT and whose output meets the specifications of 8.3.1.3 except that the risetime of the signal must be 30 ns + 0, – 2 ns. This test shall be conducted in a noise-free environment. The combination of coaxial cable and MAU receiver introduce no more than 6 ns of edge jitter into the system.

The local transmit and receive functions shall operate simultaneously while connected to the medium operating in the half duplex operating mode.

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8.2.1.3 Collision Presence function requirements

The signal presented to the CI circuit in the absence of a collision shall be the IDL signal except when the MAU is required to signal the CS1 signal.

The signal presented to the CI circuit during the presence of a collision shall be the CS0 signal encoded as specified in 7.3.1.2. Under no conditions shall the collision presence function generate an output when only one MAU is transmitting. Table 8–1 summarizes the allowable conditions under which collisions shall be detected.

a) Collision Assertion
   1) In the case where the MAU has been transmitting for at least 20 bit times before the arrival at the MAU on the coaxial cable of a transmission from another MAU, the CS0 signal shall be presented to the CI circuit no more than 17 bit times after the arrival at the MAU on the MDI of a transmission from another MAU. Arrival at the MAU shall be considered to be the time when the transmission of the other MAU causes the dc level on the MDI to become more negative.
   2) In all other cases where the MAU is transmitting, the CS0 signal shall be presented to the CI circuit no more than 29 bit times after the later of start of transmission by the MAU and the arrival of a transmission from another MAU.

b) Collision De-assertion
   1) In the case where a collision has occurred between the MAU and one other MAU, the IDL signal shall be presented to the CI circuit no more than 17 bit times after either the end of transmission by the MAU or the arrival of the end of transmission from the other MAU, whichever occurs earlier. The arrival of the end of transmission from the other MAU shall be the time when the cessation of transmission causes the dc level on the MDI to become less negative.
   2) In the case where a collision has occurred between more than two MAUs, the IDL signal shall be presented to the CI circuit no more than 29 bit times after the arrival of the end of transmission from all but one MAU.

These timing conditions shall be met for all data bit patterns and combinations of MDI, MAU transmit levels, and MAU locations on the segment.

The collision presence function may, in some implementations, be able to sense an abnormal (for example, open) medium.

Table 8–1—Generation of collision presence signal

MAU	Numbers of transmitters		
	<2	=2	>2
Transmitting	N	Y	Y
Not transmitting	N	Y	Y
Y= shall generate SQE message N= shall not generate SQE message			

8.2.1.4 Monitor function requirements (optional)

Upon receipt of the *isolate* message the MAU shall, within 20 ms (implementations: solid-state preferred, relay switched permitted), disable the transmit function in such a way as to prevent both the transmission of signals on the trunk coaxial medium and any abnormal loading by the disabled transmitter on the trunk coaxial medium itself. The monitor function is intended to prevent a malfunctioning active component (for example, transmit driver) from bringing down the network. The *isolate* message shall not interact with the receive

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or collision presence functions, thus permitting the normal operational mode wherein all data appearing on the trunk coaxial medium are carried to the DTE on the DI signal circuit.

NOTE—Verification for successful execution of the *isolate* message requires use of the trunk coaxial medium itself. This level of guaranteed performance requires use of system layers above the physical layer and implies some interruption of normal trunk coaxial medium message traffic.

8.2.1.5 Jabber function requirements

The MAU shall contain a self-interrupt capability to inhibit transmit data from reaching the medium. Hardware within the MAU (with no external message other than the detection of output data, bits, or leakage, by way of the transmit function) shall provide a nominal window of at least 20 ms to at most 150 ms during which time a normal data link frame may be transmitted. If the frame length exceeds this duration, the jabber function shall inhibit further output data from reaching the medium.

When the transmit function has been positively disabled, the MAU shall then activate the collision presence function as close to the trunk coaxial medium as possible without introducing an extraneous signal on the trunk coaxial medium. A MAU without the monitor function may reset the jabber and collision presence functions on power reset. Alternatively, a MAU without the monitor function may reset these functions after a period of 0.5 s ± 50% if the monitor function has not been implemented. If the monitor function has been implemented then it shall be used to reset the collision presence and jabber functions.

8.2.2 MAU interface messages

8.2.2.1 DTE physical layer to MAU physical layer messages

The following messages can be sent by the DTE physical layer entities to the MAU physical layer entities:

Message	Circuit	Signal	Meaning
output	DO	CD1, CD0	Output information
output_idle	DO	IDL	No data to be output
normal	CO	IDL	Assume the nonintrusive state on the trunk coaxial medium
(Optional circuit)			
isolate	CO	CS0(BR)	Positively disable the trunk coaxial medium transmitter

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8.2.2.2 MAU physical layer to DTE physical layer

The following messages can be sent by the MAU physical layer entities to the DTE physical layer entities:

Message	Circuit	Signal	Meaning
input	DI	CD1, CD0	Input information
input_idle	DI	IDL	No information to be input
mau_available	CI	IDL	MAU is available for output
signal_quality_error	CI	CS0	Error detected by MAU

8.2.2.2.1 *input* message

The MAU physical layer sends an *input* message to the DTE physical layer when the MAU has a bit of data to send to the DTE. The physical realization of the input message is a CD0 or CD1 sent by the MAU to the DTE on the data in circuit. The MAU sends CD0 if the *input* bit is a zero or CD1 if the *input* bit is a one. No retiming of the CD1 or CD0 signals takes place within the MAU.

8.2.2.2.2 *input_idle* message

The MAU physical layer sends an *input_idle* message to the DTE physical layer when the MAU does not have data to send to the DTE. The physical realization of the *input_idle* message is the IDL signal sent by the MAU to the DTE on the data in circuit.

8.2.2.2.3 *mau_available* message

The MAU physical layer sends the *mau_available* message to the DTE physical layer when the MAU is available for output. The *mau_available* message is always sent by a MAU that is always prepared to output data unless the *signal_quality_error* message shall be sent instead. Such a MAU does not require *mau_request* to prepare itself for data output. The physical realization of the *mau_available* message is an IDL signal sent by the MAU to the DTE on the control in circuit.

8.2.2.2.4 *signal_quality_error* message

The *signal_quality_error* message shall be implemented in the following fashion:

a) The *signal_quality_error* message shall not be sent by the MAU if no MAU or only one MAU is transmitting on the trunk coaxial medium in the normal mode.
b) If two or more remote MAUs are transmitting on the trunk coaxial medium, but the MAU connected to the local node is not transmitting, then the local MAU shall send the *signal_quality_error* message.
c) When the local MAU is transmitting on the trunk coaxial medium, all occurrences of one or more additional MAUs transmitting shall cause the *signal_quality_error* message to be sent by the local MAU to its DTE.
d) When the MAU has completed each output frame it shall perform an SQE test sequence, as defined in Figures 8–2 and 8–3.
e) When the MAU has inhibited the transmit function it shall send the *signal_quality_error* message in accordance with the jabber function requirements of 8.2.1.5.

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The physical realization of the *signal_quality_error* message is the CS0 signal sent by the MAU to the DTE on the control in circuit. See 8.2.1.3 for timing requirements on the assertion and de-assertion of the CS0 signal in a collision.

Note that the MAU is required to assert the *signal_quality_error* message at the appropriate times whenever the MAU is powered and not just when the DTE is providing output data.

8.2.3 MAU state diagrams

The state diagrams, Figures 8–2 (a–d), 8–3, and 8–4, depict the full set of allowed MAU state functions relative to the control circuits of the DTE-MAU interface for MAUs without conditioning requirements. Messages used in these state diagrams are explained below:

a) *positive_disable*. Activates the positive means provided in the MAU transmitter to prevent interference with the trunk coaxial medium.
b) *enable_driver*. Activates the path employed during normal operation to cause the MAU transmitter to impress data onto the trunk coaxial medium.
c) *disable_driver*. Deactivates the path employed during normal operation to cause the MAU transmitter to impress data onto the trunk coaxial medium.
d) *no_collision*. Signifies that the condition of multiple transmitters simultaneously active on the trunk coaxial medium does not exist.
e) *collision*. Signifies that the condition of multiple transmitters simultaneously active on the trunk coaxial medium does exist.
f) *not_positive_disable*. Deactivates the positive means provided in the MAU transmitter to prevent interference with the trunk coaxial medium.

When no state is asserting the message *signal_quality_error*, the message *MAU_input_idle* is sent.

8.3 MAU–medium electrical characteristics

8.3.1 MAU-to-coaxial cable interface

The following subclauses describe the interface between the MAU and the coaxial cable. Negative current is defined as current into the MAU (out of the center conductor of the cable).

8.3.1.1 Input impedance

The shunt capacitance presented to the coaxial cable by the MAU circuitry (not including the means of attachment to the coaxial cable) is recommended to be no greater than 2 pF. The resistance to the coaxial cable shall be greater than 100 kΩ.

The total capacitive load due to MAU circuitry and the mechanical connector as specified in 8.5.3.2 shall be no greater than 4 pF.

These conditions shall be met in the power-off and power-on, not transmitting states (over the frequencies BR/2 to BR).

The magnitude of the reflection from a MAU shall not be more than that produced by a 4 pF capacitance when measured by both a 25 ns rise time and 25 ns fall time waveform. This shall be met in both the power on and power off, not transmitting states.

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8.3.1.2 Bias current

The MAU shall draw (from the cable) between +2 μA and –25 μA in the power-off and the power-on, not transmitting states.

8.3.1.3 Coaxial cable signaling levels

The signal on the coaxial cable due to a single MAU as measured at the MAU transmitter output is composed of an ac component and an offset component. Expressed in terms of current immediately adjacent to the MAU connection (just prior to splitting the current flow in each direction) the signal has an offset component (direct current including the effects of timing distortion) of from –37 mA minimum to –45 mA maximum and an ac component from +28 mA up to the offset value.

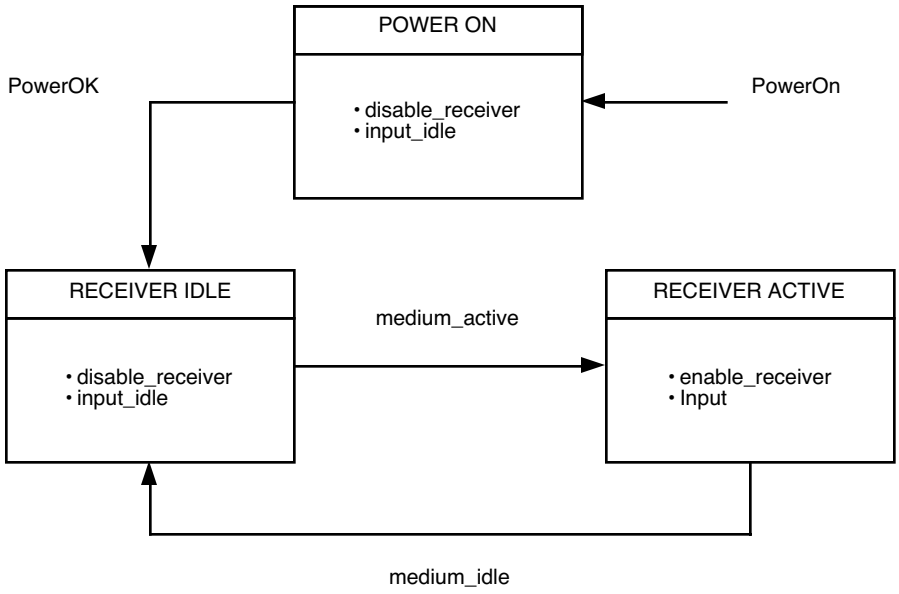
The current drive limit shall be met even in the presence of one other MAU transmitter. A MAU shall be capable of maintaining at least 2.2 V of average dc level on the coaxial cable in the presence of two or more other MAUs transmitting concurrently. The MAU shall, in addition, sink no more than ±250 μA when the voltage on the center conductor of the cable drops to –10 V when the MAU is transmitting.

The MAU shall sink no more than –25 μA when the voltage on the center conductor of the cable drops to –7 V when the MAU is transmitting.

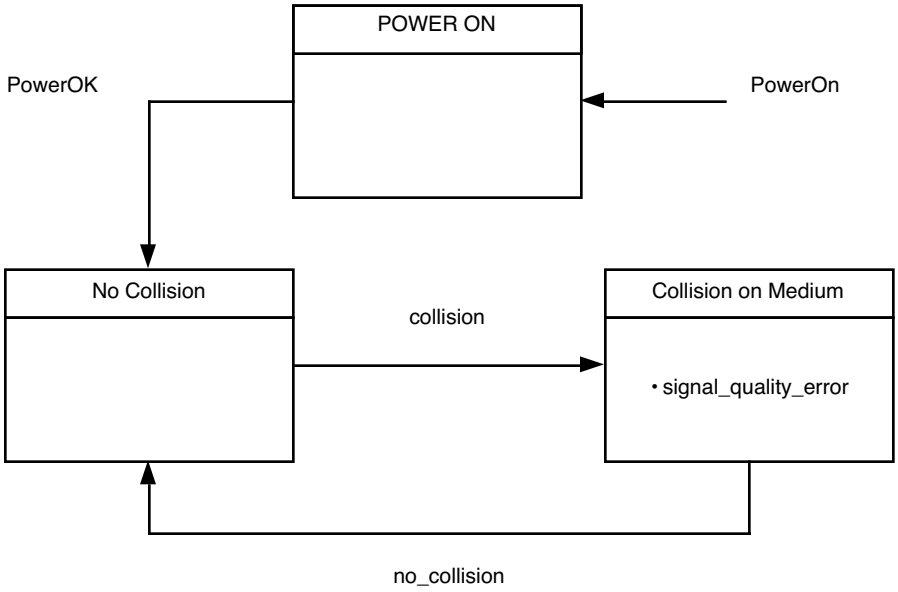
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a) Receive function state diagram



b) Collision Presence function state diagram

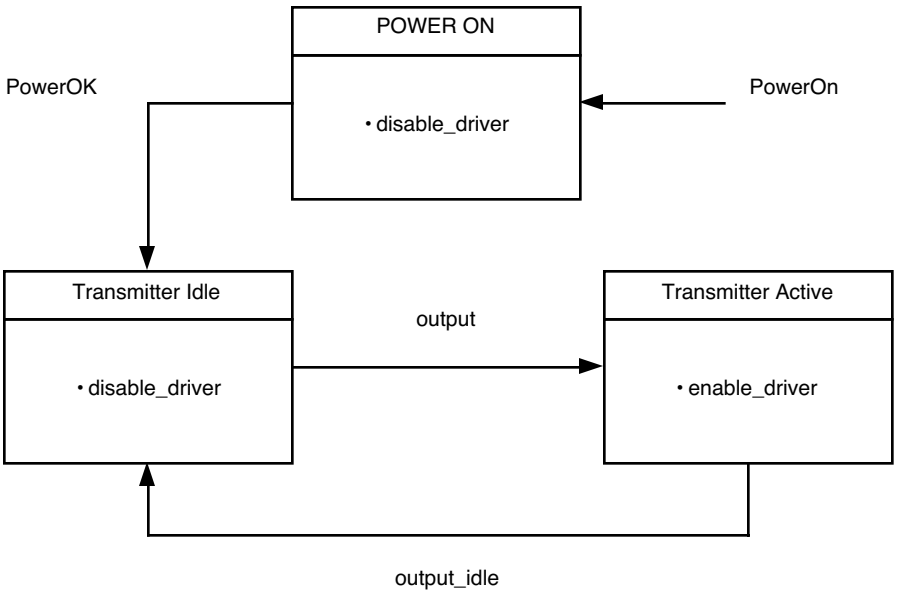
Figure 8–2—Interface function: Simple MAU without isolate capability

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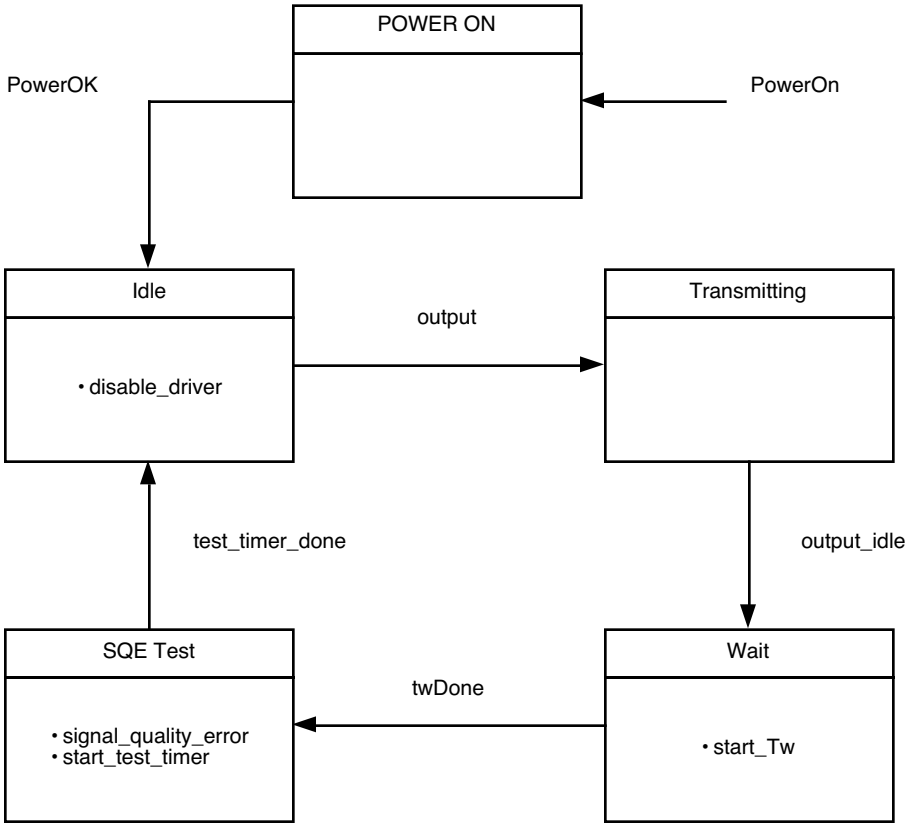
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c) Transmit function state diagram



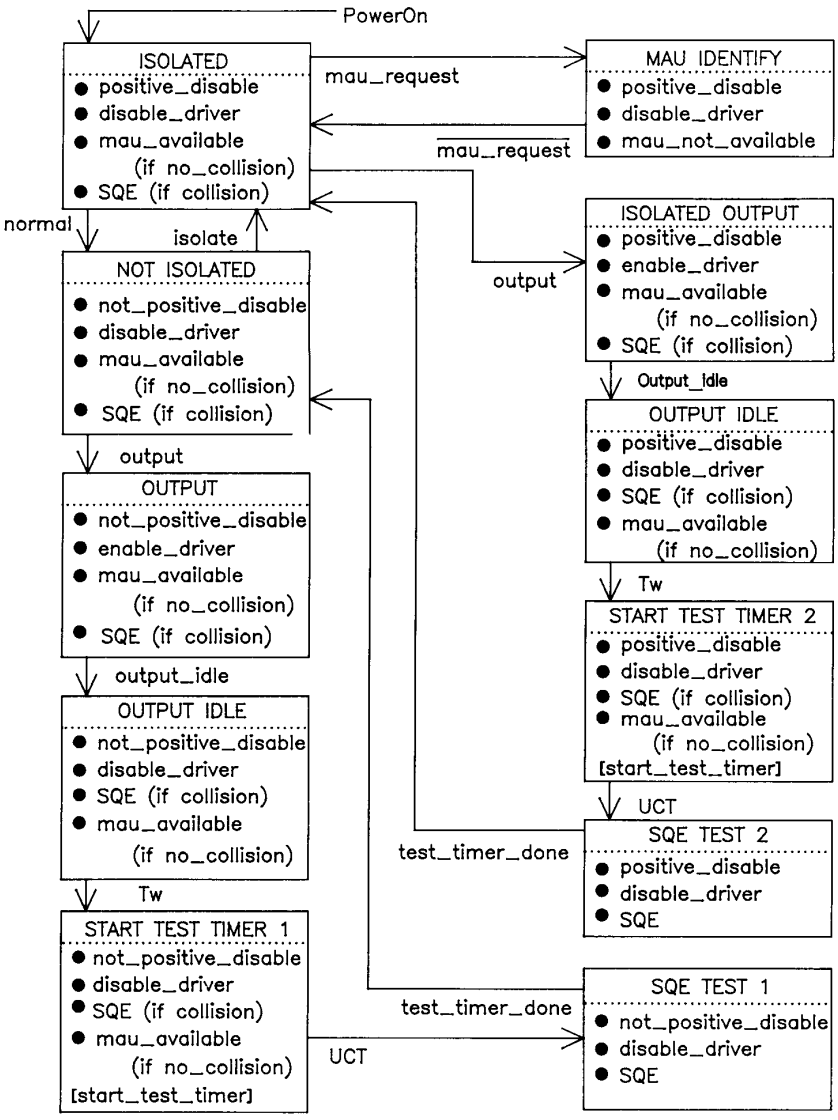
d) SQE test state diagram

Figure 8–2—*(Continued)*
Interface function: Simple MAU without isolate capability

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NOTE: UCT = unconditional transition
Tw = wait time, see 8.2.1.1

Figure 8–3—Interface function: Simple MAU with isolate capability

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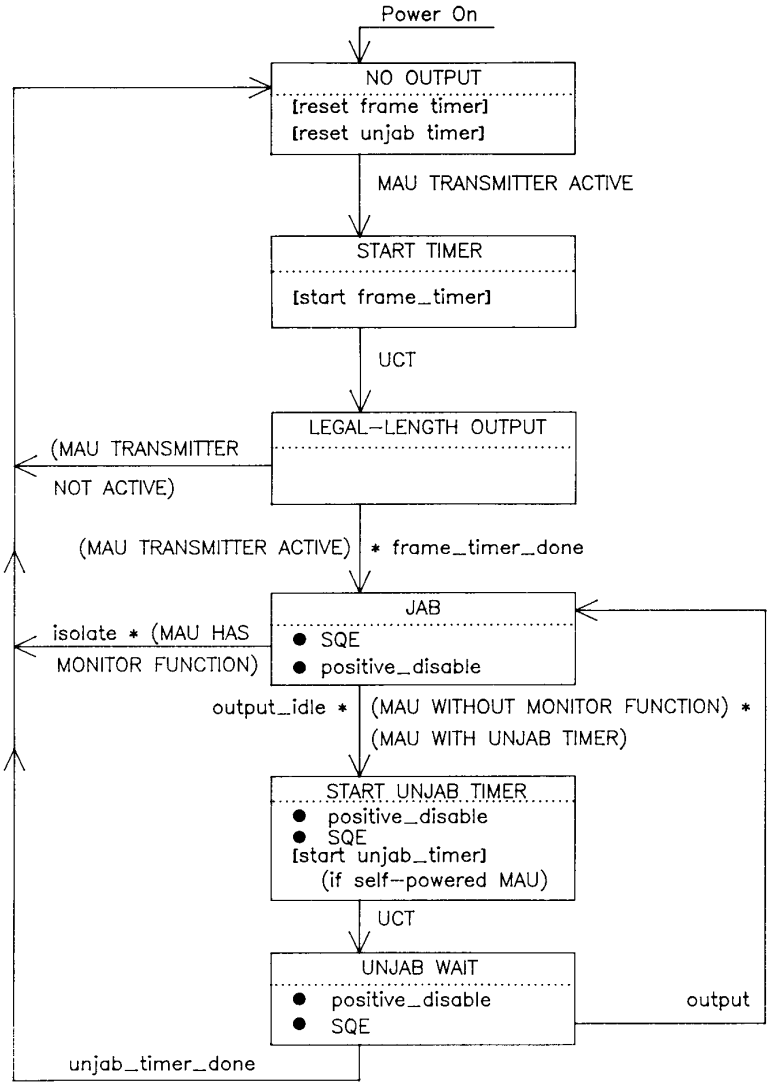


Figure 8–4—Jabber function

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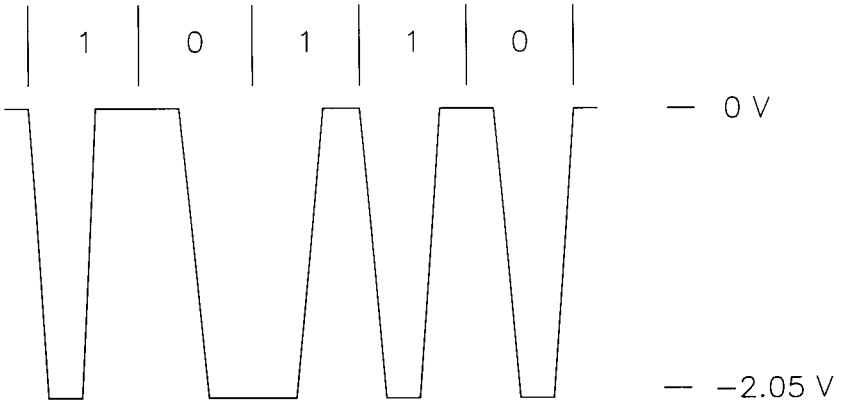
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The actual current measured at a given point on the cable is a function of the transmitted current and the cable loss to the point of measurement. Negative current is defined as current out of the center conductor of the cable (into the MAU). The 10–90% rise/fall times shall be 25 ± 5 ns at 10 Mb/s. The rise and fall times shall match within 2 ns. Figures 8–5 and 8–6 shows typical waveforms present on the cable. Harmonic content generated from the BR fundamental periodic input shall meet the following requirements:

2nd and 3rd Harmonics:at least 20 dB below fundamental
4th and 5th Harmonics:at least 30 dB below fundamental
6th and 7th Harmonics:at least 40 dB below fundamental
All higher Harmonics:at least 50 dB below fundamental

NOTE—Even harmonics are typically much lower.

The above specifications concerning harmonics cannot be satisfied by a square-wave with a single-pole filter, nor can they be satisfied by an output waveform generator employing linear ramps without additional waveshaping. The signals as generated from the encoder within PLS shall appear on the coaxial cable without any inversions (see Figure 8–6).



NOTES: (1) Voltages given are nominal, for a single transmitter
(2) Rise and fall time is 25 ns nominal at 10 Mb/s rate
(3) Voltages are measured on terminated coaxial cable adjacent to transmitting MAU
(4) Manchester coding

Figure 8–5—Typical coaxial trunk cable signal waveform

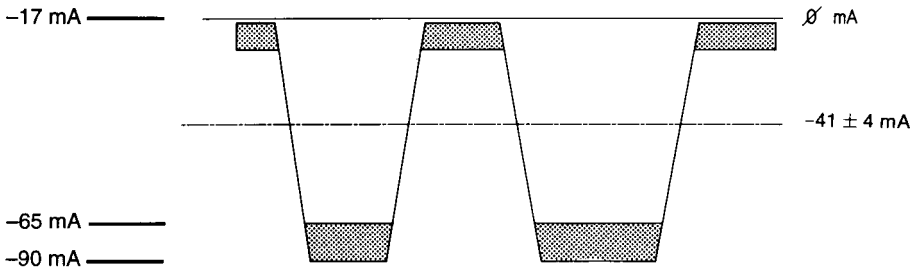


Figure 8–6—Recommended driver current signal levels

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8.3.1.4 Transmit output levels symmetry

Signals received from the AUI DO circuit shall be transmitted onto the coaxial cable with the characteristics specified in 8.3.1.3. Since the coaxial cable proceeds in two directions from the MAU, the current into the MAU is nominally twice the current measured on the coaxial cable.

The output signal of a MAU meeting this specification shall exhibit edge jitter of no more than 2.5 ns into a 25 Ω ± 1% resistor substituted for the connection to the coaxial cable when the DO circuit into the MAU is driven through a zero length AUI cable with pseudorandom Manchester encoded binary data from a data generator that exhibits no more than 0.5 ns of edge jitter on half bit cells of exactly 1/2 BT whose output meets the specifications of 7.4.1.1 through 7.4.1.5. The above specified component is not to introduce more than 2 ns of edge jitter into the system.

The MAU shall not transmit a negative going edge after cessation of the CD output data stream on DO or before the first edge of the next frame on the DO circuit.

8.3.1.5 Collision detect thresholds

Receive mode collision detection indicates that a nontransmitting MAU has the capability to detect collisions when two or more MAUs are transmitting simultaneously. For receive mode collision detection, the MAU's collision detection threshold shall be within the range –1448 mV to –1590 mV. The actual dc voltage on the cable during a noncollision transmission has a maximum value of –1293 mV. The lower threshold limit of –1448 mV allows 55 mV for sending end overshoot during preamble and filter impulse response during the remainder of the packet. These limits take account of up to 12% collision detect filter impulse response. If a specific filter implementation has a higher value of impulse response, the lower threshold limit of 1448 mV shall be replaced by 1293 mV × [1 + impulse response].

All MAUs are required to implement receive mode collision detection.

NOTE—The above threshold limits are measured at the coaxial cable center conductor with respect to the shield at the MAU connector. The MAU designer must take into account circuit offsets, low-frequency noise (for example, 50 Hz, 60 Hz), and 5 MHz ripple at the filter output in determining the actual internal threshold value and its tolerance.

8.3.2 MAU electrical characteristics

8.3.2.1 Electrical isolation

The MAU must provide isolation between the AUI cable and the coaxial trunk cable. This isolation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50 to 60 Hz for 60 s, applied as specified in 5.3.2 of IEC 60950: 1991.
b) 2250 Vdc for 60 s, applied as specified in 5.3.2 of IEC 60950: 1991.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

There shall be no isolation breakdown, as defined in 5.3.2 of IEC 60950: 1991, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 Vdc. In addition, the isolation impedance between the DTE and the coaxial cable shield shall be less than 15 Ω between 3 MHz and 30 MHz.

8.3.2.2 Power consumption

The current drawn by the MAU shall not exceed 0.5 A as powered by the AUI source. The MAU shall be capable of operating from all possible voltage sources as supplied by the DTE through the resistance of all

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permissible AUI cables. The MAU shall not disrupt the trunk coaxial medium should the DTE power source fall below the minimum operational level under abnormal MAU load conditions.

The MAU shall be labeled externally to identify the maximum value of current required by the device at any specified input voltage.

8.3.2.3 Reliability

The MAU shall be designed to provide an MTBF of at least 1 million hours of continuous operation without causing communication failure among other stations attached to the local network medium. Component failures within the MAU electronics should not prevent communication among other MAUs on the coaxial cable. Connectors and other passive components comprising the means of connecting the MAU to the coaxial cable shall be designed to minimize the probability of total network failure.

It should be noted that a fault condition that causes a MAU to draw in excess of 2 mA may cause communication failure among other stations.

8.3.3 MAU–DTE electrical characteristics

The electrical characteristics for the driver and receiver components connected to the branch cable within the MAU shall be identical to those as specified in Clause 7 of this standard.

8.3.4 MAU–DTE mechanical connection

The MAU shall be provided with a 15-pin male connector as specified in detail in the AUI specification, Clause 7.

8.4 Characteristics of the coaxial cable

The trunk cable is of constant impedance, coaxial construction. It is terminated at each end by a terminator (see 8.5.2), and provides the transmission path for MAU device connection. Coaxial cable connectors are used to make the connection from the cable to the terminators, and between cable sections (if needed). The cable has various electrical and mechanical requirements that shall be met to ensure proper operation.

8.4.1 Coaxial cable electrical parameters

8.4.1.1 Characteristic impedance

The average characteristic cable impedance shall be 50 ± 2 Ω, measured at 10 MHz according to IEC 60096-1: 1986 and Amd. 2: 1993. Periodic variations in impedance along a single piece of cable may be up to ±3 Ω sinusoidal centered around the average value, with a period of less than 2 m.

NOTE—If the requirements of 8.4.2.1.1 b), 8.4.2.1.2, 8.4.2.1.3, 8.4.2.1.4 b) are met, then it is expected that the characteristic impedance periodicity requirement shall be considered met.

8.4.1.2 Attenuation

The attenuation of a 500 m cable segment shall not exceed 8.5 dB (17 dB/km) measured with a 10 MHz sine wave, nor 6.0 dB (12 dB/km) measured with a 5 MHz sine wave.

8.4.1.3 Velocity of propagation

The minimum required velocity of propagation is 0.77 c.

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8.4.1.4 Edge jitter, untapped cable

Untapped coaxial cable meeting this specification shall exhibit edge jitter of no more the 8.0 ns in either direction at the receiving end when 500 m of the cable is terminated at both ends with terminators meeting the impedance requirements of 8.5.2.1 and is driven at one end with pseudorandom Manchester-encoded binary data from a data generator that exhibits no more than 1.0 ns of edge jitter in either direction on half bit cells of exactly 1/2 BT and whose output meets the specifications of 8.3.1.3 except that the rise time of the signal must be 30 ns + 0, – 2 ns, and no offset component in the output current is required. This test shall be conducted in a noise-free environment. The above specified component is not to introduce more than 7 ns of edge jitter into the system.

8.4.1.5 Transfer impedance

The coaxial cable medium shall provide sufficient shielding capability to minimize its susceptibility to external noise and also to minimize the generation of interference by the medium and related signals. While the cable construction is not mandated, it is necessary to indicate a measure of performance expected from the cable component. A cable's EMC performance is determined, to a large extent, by the transfer impedance value of the cable. See reference [B29].

The transfer impedance of the cable shall not exceed the values shown in Figure 8–7 as a function of frequency.

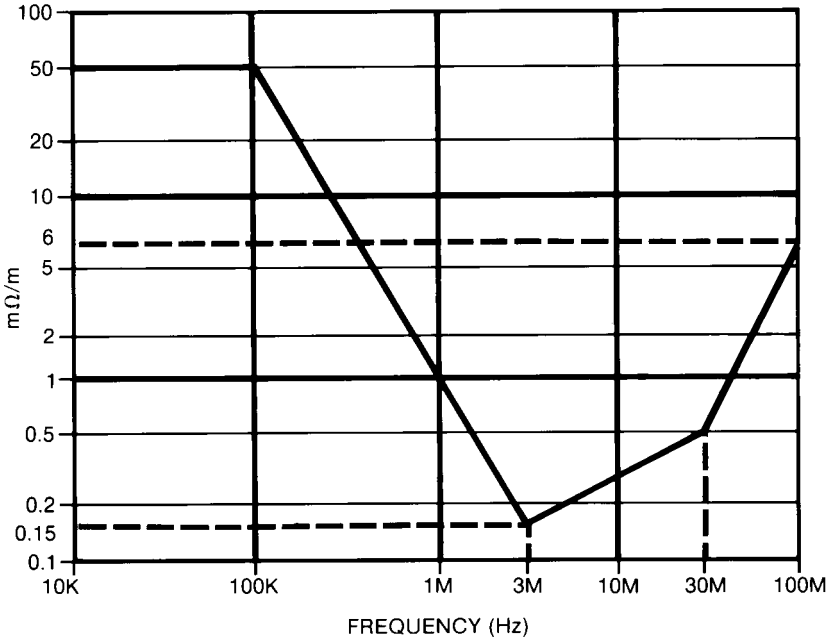


Figure 8–7—Maximum coaxial cable transfer impedance

8.4.1.6 Cable dc loop resistance

The sum of the center conductor resistance plus the shield resistance, measured at 20 °C, shall not exceed 10 mΩ/m.

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8.4.2 Coaxial cable properties

8.4.2.1 Mechanical requirements

The cable used should be suitable for routing in various environments, including but not limited to, dropped ceilings, raised floors, cable troughs, and throughout open floor space. The jacket shall provide insulation between the cable sheath and any building structural metal. Also, the cable shall be capable of accepting coaxial cable connectors, described in 8.5. The cable shall conform to the following requirements.

8.4.2.1.1 General construction

a) The coaxial cable shall consist of a center conductor, dielectric, shield system, and overall insulating jacket.
b) The concentricity (for example, positional relationship between center conductor to shield system and outer jacket) of the coaxial cable elements shall be greater than 92% as measured in accordance with the following general configuration:

$$\frac{(\text{jacket radius}) - (\text{center offset})}{\text{jacket radius}} \times 100 \geq 92\%$$

It is assumed that the offset and radius values are worst case at any point within the measured system.
c) The coaxial cable jacket, shield system, and dielectric material shall be pierceable either by means of the connector type specified in 8.5.3.2 or by an external core tool. Overall cable system pierceability (the ability of a tap probe to pierce the jacket, shields, and dielectric cable system without substantial dielectric deformation and without causing a short circuit between center conductor and shield system) is a vital parameter affecting tap connection reliability.

Pierceability of the cable system can be measured in terms of the probe's load versus displacement signature. A pierceable cable exists where the displacement is ≥ 1.52 mm (0.06 in) between rupture (piercing) of the shield system and contact with the center conductor.
d) The coaxial cable shall be sufficiently flexible to support a bend radius of 254 mm (10 in).

8.4.2.1.2 Center conductor

The center conductor shall be 2.17 mm ± 0.013 mm (0.0855 ± 0.0005 in) diameter tinned or plain solid copper.

8.4.2.1.3 Dielectric material

The dielectric may be of any type provided the conditions of 8.4.1.2, 8.4.1.3, and 8.4.2.1.1d) are met.

8.4.2.1.4 Shielding system

a) The shielding system may contain both braid and foil elements sufficient to meet the transfer impedance of 8.4.1.5 and the EMC specifications of 8.7.2.
b) The inside diameter of the innermost shield shall be 6.00 mm (0.236 in) minimum.
c) The outside diameter of the outermost shield shall be 8.00 mm ± 0.40 mm (0.315 ± 0.016 in).
d) The outermost shield shall be a tinned copper braid. The percent coverage shall be sufficient to meet 8.4.1.5, 8.4.1.6, 8.5.3.2.3, and 8.7.2.

8.4.2.1.5 Overall jacket

a) Any one of several jacket materials shall be used provided the specifications of 8.4.1 and 8.4.2 are met.

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b) Either of two jacket dimensions may be used for the two broad classes of materials, provided the specification of 8.4.2.1.1 are met:
   1) Polyvinyl Chloride (for example, PVC) or equivalent having an OD of 10.3 mm ± 0.25 mm (0.406 nominal ± 0.010 in).
   2) Fluoropolymer (for example, FEP, E-CTFE) or equivalent having an OD of 9.525 mm ± 0.254 mm (0.375 nominal ± 0.010 in).

The cable shall meet applicable flammability and smoke criteria and local and national codes for the installed environment. See 8.7.4. Different types of cable sections (for example, polyvinyl chloride and fluoropolymer dielectric) may be interconnected, while meeting the sectioning requirements of 8.6. See references [B18] and [B39].

8.4.2.2 Jacket marking

The cable jacket shall be marked in a color contrasting with the background color of the jacket. The markings shall be spaced at 2.5 m ± 5 cm regularly along the entire length of the cable. It is permissible for the 2.5 m spacing to be interrupted at discontinuities between cable sections joined by connectors. (See 8.6.2.2 for MAU placement rules that mandate cable markings.) It is recommended that the base color of the jacket itself be a bright color (for example, yellow) other than that normally used for power mains.

8.4.3 Total segment dc loop resistance

The sum of the center conductor, connectors, and shield resistance shall not exceed 5 Ω total per segment.

Each in-line connector pair or MAU shall be no more than 10 mΩ. Use of these components reduces the overall allowable segment length accordingly. Values given above are at 20 °C. For temperature variations, cable length shall be adjusted accordingly such that the 5 Ω total is not exceeded.

If a trunk coaxial cable segment consists of several cable sections, then all connectors and internal resistance of the shield and center conductor shall be included in the loop resistance measurement.

8.5 Coaxial trunk cable connectors

The trunk coaxial medium requires termination and may be extended or partitioned into sections. Devices to be attached to the medium as MAUs require a means of connection to the medium. Two basic connector types provide the necessary connection means:

a) Standard Type N connectors (IEC 60169-16)
b) A coaxial “tap” connector

All Type N connectors shall be of the 50 Ω constant impedance type. Since the frequencies present in the transmitted data are well below UHF range (being band-limited to approximately 20 MHz), high-quality versions of the connectors are not required (but are recommended).

All of the coaxial tap connectors shall follow the requirements as defined in 8.5.3.

8.5.1 Inline coaxial extension connector

All coaxial cables shall be terminated with the Type N plug connectors. A means shall be provided to ensure that the connector shell (which connects to the cable sheath) does not make contact with any building metal or other unintended conductor. An insulating sleeve or boot slipped over the connector at installation time is suitable.

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Inline coaxial extensions between two sections of coaxial cable shall be made with a pair of Type N receptacle connectors joined together to form one "barrel." An insulating sleeve or boot shall also be provided with each barrel assembly.

8.5.2 Coaxial cable terminator

8.5.2.1 Termination

Coaxial cable terminators are used to provide a termination impedance for the cable equal in value to its characteristic impedance, thereby minimizing reflection from the ends of the cables. Terminators shall be packaged within an inline female receptacle connector. The termination impedance shall be 50 Ω ± 1% measured from 0 – 20 MHz, with the magnitude of the phase angle of the impedance not to exceed 5°. The terminator power rating shall be 1 W or greater.

8.5.2.2 Earthing

Either the coaxial cable terminator or inline extension connector provides a convenient location for meeting the earth grounding requirement of 8.6.2.3. It is recommended that a ground lug with current rating of at least 1500 ampacity be provided on one of the two terminators or on one extension connector used within a cable segment.

NOTE 1—A single ground return lug on an inline connector located in the center of the cable transmission system may be used to satisfy this requirement.

NOTE 2—Alternatively, terminators might be supplied in pairs, one with and one without the ground lug connection point.

8.5.3 MAU-to-coaxial cable connection

A means shall be provided to allow for attaching a MAU to the coaxial cable. The connection shall not disturb the transmission line characteristics of the cable significantly; it shall present a predictably low shunt capacitance, and therefore a negligibly short stub length. This is facilitated by the MAU being located as close to its cable connection as possible; the MAU and connector are normally considered to be one assembly. Long (greater than 30 mm) connections between the coaxial cable and the input of the MAU jeopardize this objective.

Overall system performance is dependent largely on the MAU-to-coaxial cable connection being of low shunt capacitance.

If the design of the connection is such that the coaxial cable is to be severed to install the MAU, the coaxial cable segment shall still meet the sectioning requirements of 8.6.2.1. Coaxial connectors used on a severed cable shall be Type N, as specified in 8.5.1.

The Type N connectors selected should be of high quality (that is, low contact resistance) to minimize the impact on system performance.

If the design of the connection is such that the piercing tap connector is to be used without severing the cable, then the tap connector and cable assembly shall conform to the mechanical and electrical requirements as defined throughout 8.5.3.1 and 8.5.3.2.

8.5.3.1 Electrical requirements

Requirements for the coaxial tap connector are as follows:

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a) *Capacitance:* 2 pF nominal connector loading measured at 10 MHz.

NOTE—**Total** capacitance of tap and active circuitry connected directly shall be no greater than 4 pF. Specific implementations may allocate capacitance between tap and circuitry as deemed appropriate.

b) *Contact resistance (*applies to center conductor and shield contacts): 50 mΩ maximum for both shield and center conductor over useful connector lifetime.
c) *Contact material:* surface material on signal probe or shield sufficient to meet contact resistance requirements in environment and over time.
d) *Voltage rating:* 600 V dc or ac rms maximum.
e) *Insulation:* dc leakage resistance of tap housing shall be higher than 1 GΩ between braid and external conductors in the normal operating environment.
f) *Probe current rating:* 0.1 A per contact (probe and shield)
g) *Shield current rating:* 1 A surge for 1 s

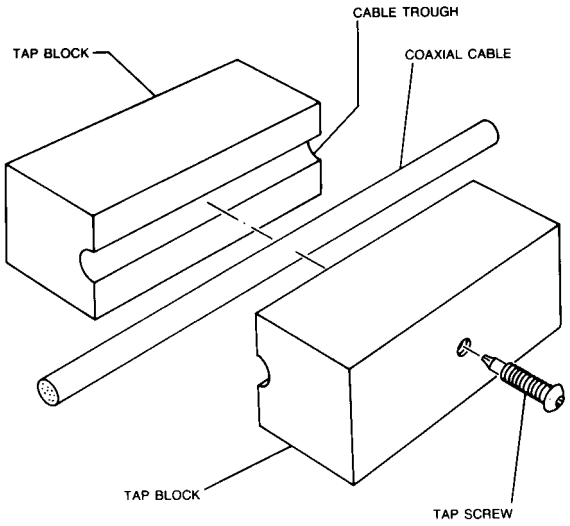
8.5.3.2 Mechanical requirements

8.5.3.2.1 Connector housing

Shielding characteristics: > 40 dB at 50 MHz.

8.5.3.2.2 Contact reliability

Overall performance of the LAN system depends to a large extent on the reliability of the coaxial cable medium and the connection to that medium. Tap connection systems should consider the relevant electrical and mechanical parameters at the point of electrical connection between tap probe and cable center conductor to ensure that a reliable electrical contact is made and retained throughout the useful life of these components. It is recommended that some means be provided to ensure relatively constant contact loading over time, with creep, in temperature, and typical environment. Typical coaxial tap connector configurations are shown in Figures 8–8 and 8–9. See references [B1], [B32], and [B33].



NOTE: **Tutorial only** and **not** part of specification

Figure 8–8—Coaxial tap connector configuration concepts

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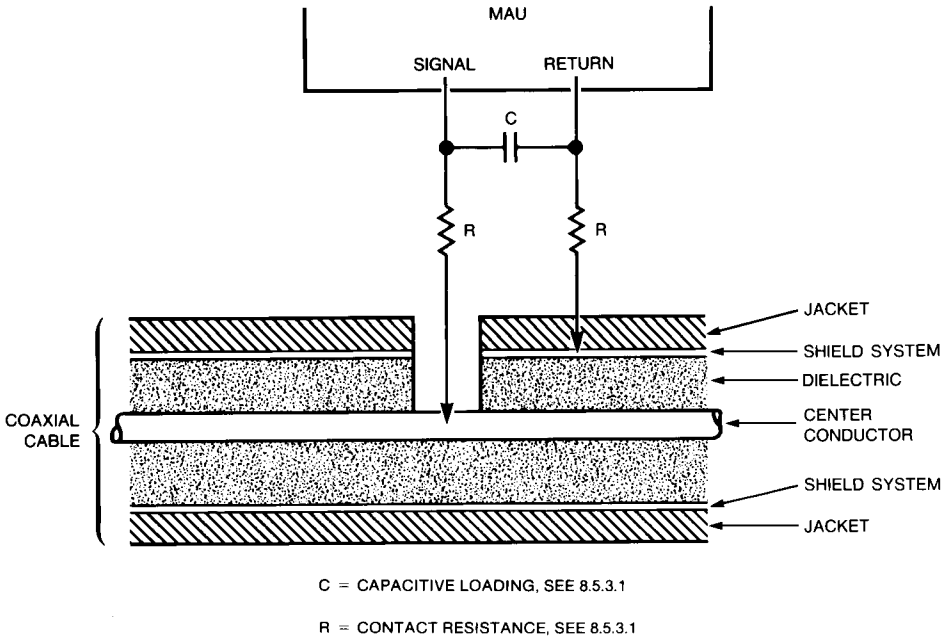


Figure 8–9—Typical coaxial tap connection circuit

8.5.3.2.3 Shield probe characteristics

The shield probe shall penetrate the cable jacket and outer layer(s) of the shield system to make effective capture of the outer braid (pick 2 or more typical strands).

8.6 System considerations

8.6.1 Transmission system model

The maximum configuration for the physical transmission system is as follows:

a) A trunk coaxial cable, terminated in its characteristic impedance at each end, constitutes a coaxial cable segment. A coaxial cable segment may contain a maximum of 500 m of coaxial cable and a maximum of 100 MAUs. The propagation velocity of the coaxial cable is assumed to be 0.77 c minimum (c = 300 000 km/s). The maximum end-to-end propagation delay for a coaxial cable segment is 2165 ns.

b) Repeater sets are required for segment interconnection. Repeater sets occupy MAU positions on coaxial cable segments and count toward the maximum number of MAUs on a coaxial cable segment. Repeater sets may be located in any MAU position on a coaxial cable segment.

c) The repeater unit specified in Clause 9 provides the means for connecting 10 Mb/s baseband segments into a CSMA/CD network. The proper operation of a CSMA/CD network requires network size to be limited to control round-trip propagation delay to meet the requirements of 4.2.3.2.3 and 4.4.2.1, and the number of repeaters between any two DTEs to be limited in order to limit the shrinkage of interpacket gap as it travels through the network. Configuration rules, which ensure that these limits are not exceeded, are given in Clause 13.

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8.6.2 Transmission system requirements

8.6.2.1 Cable sectioning

The 500 m maximum length coaxial cable segment need not be made from a single, homogeneous length of cable. The boundary between two cable sections (joined by coaxial connectors: two male plugs and a barrel) represents a signal reflection point due to the impedance discontinuity caused by the batch-to-batch impedance tolerance of the cable. Since the worst-case variation from 50 Ω is 2 Ω, a possible worst-case reflection of 4% may result from the joining of two cable sections. The configuration of long cable segments (up to 500 m) from smaller sections must be made with care. The following *recommendations* apply, and are *given in order of preference*:

a) If possible, the total segment should be made from one homogeneous (no breaks) cable. This is feasible for short segments, and results in minimal reflections from cable impedance discontinuities.
b) If cable segments are built up from smaller sections, it is recommended that all sections come from the same manufacturer and lot. This is equivalent to using a single cable, since the cable discontinuities are due to extruder limitations, and not extruder-to-extruder tolerances. There are no restrictions in cable sectioning if this method is used. However, if a cable section in such a system is later replaced, it shall be replaced either with another cable from the same manufacturer and lot, or with one of the standard lengths described below.
c) If uncontrolled cable sections must be used in building up a longer segment, the lengths should be chosen so that reflections, when they occur, do not have a high probability of adding in phase. This can be accomplished by using lengths that are odd integral multiples of a half wavelength in the cable at 5 MHz; this corresponds to using lengths of 23.4 m, 70.2 m, and 117 m (± 0.5 m) for all sections. These are considered to be the standard lengths for all cable sections. Using these lengths exclusively, any mix or match of cable sections may be used to build up a 500 m segment without incurring excessive reflections.

NOTE—If cable segments are to be added to existing installations, then care shall be taken (explicit physical or TDR measurements) to ensure that no more than a 500 m cable segment results.

d) As a last resort, an arbitrary configuration of cable sections may be employed, if it has been confirmed by analysis or measurement that the worst-case signal reflection due to the impedance discontinuities at any point on the cable does not exceed 7% of the incident wave when driven by a MAU meeting these specifications.

8.6.2.2 MAU placement

MAU components and their associated connections to the cable cause signal reflections due to their noninfinite bridging impedance. While this impedance shall be implemented as specified in Clause 7, placement of MAUs along the coaxial cable must also be controlled to ensure that reflections from the MAU do not add in phase to a significant degree.

Coaxial cables marked as specified in 8.4.2.2 have marks at regular 2.5 m spacing; a MAU shall only be placed at a mark on the cable. This guarantees both a minimum spacing between MAUs of 2.5 m, and controlling the relative spacing of MAUs to ensure nonalignment on fractional wavelength boundaries.

The total number of MAUs on a cable segment shall not exceed 100.

8.6.2.3 Trunk cable system grounding

The *shield conductor* of each coaxial cable segment *shall make electrical contact with an effective earth reference* (see [B12], Articles 250 and 800) *at one point and shall not make electrical contact with earth elsewhere* on such objects as building structural metal, ducting, plumbing fixture, or other unintended

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conductor. Insulators may be used to cover any coaxial connectors used to join cable sections and terminators, to ensure that this requirement is met. A sleeve or boot attached at installation time is acceptable.

This specification is intended for use within (intraplant) buildings. Applications requiring interplant connections by way of external (outdoors) means may require special consideration beyond the scope of the standard.

The sheath conductor of the AUI cable shall be connected to the earth reference or chassis of the DTE.

8.6.3 Labeling

It is recommended that each MAU (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Data rate capability in megabits per second
b) Power level in terms of maximum current drain
c) Safety warning (for example, shock hazard)

8.7 Environmental specifications

8.7.1 General safety requirements

All stations meeting this standard shall conform to IEC 60950: 1991.

8.7.2 Network safety requirements

This subclause sets forth a number of recommendations and guidelines related to safety concerns, the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate standards. References [B12] and [B21] provide additional guidance.

LAN trunk cable systems as described in this standard are subject to at least four direct electrical safety hazards during their use. These hazards are

a) Direct contact between local network components and power or lighting circuits.
b) Static charge buildup on local network cables and components.
c) High-energy transients coupled onto the local network cabling system.
d) Potential differences between safety grounds to which various network components are connected.

These electrical safety hazards, to which all similar cabling systems are subject, should be alleviated properly for a local network to perform properly. In addition to provisions for properly handling these faults in an operational system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification of an existing network.

Proper implementation of the following provisions will greatly decrease the likelihood of shock hazards to persons installing and operating the LAN.

8.7.2.1 Installations

Sound installation practice, as defined by applicable local codes and regulations, shall be followed in every instance in which such practice is applicable.

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8.7.2.2 Grounding

The shield of the trunk coaxial cable shall be effectively grounded at only one point along the length of the cable. Effectively grounded means permanently connected to earth through a ground connection of sufficiently low impedance and having sufficient ampacity to prevent the building up of voltages that may result in undue hazard to connected equipment or to persons.

8.7.2.3 Safety

All portions of the trunk cabling system that are at the same potential as the trunk cable shall be insulated by adequate means to prevent their contact by either persons or by unintended conductors or grounds. The insulation employed shall provide the same or greater dielectric resistance to current flow as the insulation required between the outermost shield of the trunk cable and the above-mentioned unintended conductors. The use of insulating boots is permitted, provided that such boots (or sleeves) are mechanically and electrically equivalent to the trunk cable outer insulation characteristics and are not removed easily (that is, they shall prevent inadvertent removal by a system operator).

The MAU shall be so designed that the provisions of 8.7.2.3 and 8.7.2.4 are not defeated if the connector affixing the AUI cable to the MAU is removed.

Portions of the trunk cabling system that may become live during the dissipation of a high-energy transient by the cabling system shall also be insulated as described in 8.7.2.3.

8.7.2.4 Breakdown path

MAUs meeting this standard should provide a controlled breakdown path that will shunt high-energy transients to an effective ground either through a separate safety ground connection or through the overall shield of the branch cable. The breakdown voltage of this controlled breakdown path must meet the isolation requirements for the MAU specified in 8.3.2.1.

8.7.2.5 Isolation boundary

The isolation boundary between the branch cable and trunk cable specified in 8.3.2.1 shall be maintained to properly meet the safety requirements of this standard.

WARNING

It is assumed that the DTE equipment is properly earthed and not left floating or serviced by “doubly insulated ac power distribution system.” The use of floating or insulated DTEs is beyond the scope of this standard.

8.7.2.6 Installation and maintenance guidelines

a) When exposing the shield of the trunk coaxial cable for any reason, care shall be exercised to ensure that the shield does not make electrical contact with any unintended conductors or grounds. Personnel performing the operation should not do so if dissipation of a high energy transient by the cabling system is likely during the time the shield is to be exposed. Personnel should not contact both the shield and any grounded conductor at any time.
b) Before breaking the trunk coaxial cable for any reason, a strap with ampacity equal to that of the shield of the coaxial cable shall be affixed to the cable shield in such a manner as to join the two pieces and to maintain continuity when the shield of the trunk cable is severed. This strap shall not be removed until after normal shield continuity has been restored.
c) At no time should the shield of any portion of the coaxial trunk cable to which an MAU or MAUs are attached be permitted to float without an effective ground connection. If a section of floating

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cable is to be added to an existing cable system, the installer shall take care not to complete the circuit between the shield of the floating cable section and the grounded cable section through body contact.

d) The installation instructions for network components shall contain language which familiarizes the installer with the cautions mentioned in the above paragraphs.

e) Network components shall contain prominent warning labels that refer installers and service personnel to the safety notes in the installation instructions.

8.7.3 Electromagnetic environment

8.7.3.1 Susceptibility levels

Sources of interference from the environment include electromagnetic fields, electrostatic discharge, transient voltages between earth connections, and similar interference. Multiple sources of interference may contribute to voltage buildup between the coaxial cable and the earth connection of a DTE.

The physical channel hardware shall meet its specifications when operating in either of the following conditions:

a) Ambient plane wave field of 2 V/m from 10 kHz through 30 MHz, 5 V/m from 30 MHz through 1 GHz.

NOTE—Levels typically 1 km from broadcast stations.

b) Interference voltage of 1 V/ns peak slope, between coaxial cable shield and DTE earth connection; for example, 15.8 V peak for a 10 MHz sine wave with a 50 Ω source resistance.

MAUs meeting this standard should provide adequate rf ground return to satisfy the referenced EMC specifications.

8.7.3.2 Emission levels

The physical MAU and trunk cable system shall comply with applicable local and national codes such as FCC Docket 20780-1980 [B23] in the USA. Equipment shall comply with local and national requirements for limitation of electromagnetic interference. Where no local or national requirements exist, equipment shall comply with CISPR 22: 1993.

8.7.4 Temperature and humidity

The MAU and associated connector/cable systems are expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling such as shock and vibration. Specific requirements and values for these parameters are considered to be beyond the scope of this standard. Manufacturers are requested to indicate in the literature associated with the MAU (and on the MAU if possible) the operating environment specifications to facilitate selection, installation, and maintenance of these components. See reference [B22] for specification terminology.

8.7.5 Regulatory requirements

The design of MAU and medium components should take into consideration applicable local or national requirements. See references [B12], [B18], [B19], [B21], [B23], and Annex B for helpful resource material.

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8.8 Protocol Implementation Conformance Statement (PICS) proforma for Clause 8, Medium Attachment Unit and baseband medium specifications, type 10BASE5[20]

8.8.1 Overview

The supplier of a protocol implementation that is claimed to conform to Clause 8, Medium Attachment Unit and baseband medium specifications, type 10BASE5, shall complete the following PICS proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. The PICS can be used for a variety of purposes by various parties, including the following:

— As a checklist by the protocol implementor, to reduce the risk of failure to conform to the standard through oversight;
— As a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard PICS proforma, by the supplier and acquirer, or potential acquirer, of the implementation;
— As a basis for intially checking the possibility of interworking with another implementation by the user, or potential user, of the implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible PICs);
— As the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation, by a protocol tester.

8.8.2 Abbreviations and special symbols

8.8.2.1 Status symbols

The following abbreviations are used in the PICS proforma tables:

M mandatory

O optional

O. <n> optional, but support of at least one of the group of options labeled by the same numeral <n> is required

X prohibited

<item>: conditional-item symbol, dependent upon the support for <item>

! logical negation, applied to a conditional item symbol

8.8.2.2 Abbreviations

Ref reference section

8.8.3 Instructions for completing the PICS proforma

8.8.3.1 General structure of the PICS proforma

The structure of this PICS proforma is based on the guidelines given in ISO/IEC 9646-1: 1994 and ISO/IEC 9646-2: 1994. The first part of the PICS proforma, Implementation Identification and Protocol Summary, is

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to be completed as indicated with the information necessary to identify fully both the supplier and the particular MAU.

The main part of the PICS proforma is a fixed-format questionnaire. Each item is identified by an item reference in the first column; the second column contains the question to be asked or the parameter to be measured; the third column contains the reference(s) to the material that specifies the item in the main body of this standard; the fourth column records the status of the item—whether support is mandatory, optional, prohibited, or conditional—and provides space for the answers; the fifth column provides additional comments and/or value(s) for measurable parameters. The tables below group related items into separate subsubclauses. This satisfies the requirement of ISO/IEC 9646-2 that all PICS proforma clauses be individually identified.

A supplier wishing to submit a 10BASE5 MAU for conformance testing against this standard must fill in the column headed Support in the PICS proforma tables and submit the resulting PICS with the equipment for test. One of the boxes in this column must be checked, with Yes indicating that the implementation is intended to meet the particular mandatory or optional requirement, No indicating that the option has not been implemented (or enabled where switchable) or that the requirement is not met, or N/A indicating the item is not applicable (for example, an item that is conditional). It should be noted that any instances of No checked against a mandatory requirement will result in the implementation failing the static conformance test.

8.8.3.2 Additional information

Any additional information that is needed to ensure that the MAU or the coaxial cable submitted for test is configured as a 10BASE5 MAU or coaxial cable should be entered into the PIXIT (Protocol Implementation eXtra Information for Testing) document supplied by the conformance testing organization. Relevant information on 10BASE5 MAUs includes the following:

a) Enable/disable mechanisms for SQE Test
b) Enable/disable mechanisms for features that allow compatibility with nonstandard implementations
c) Operational instructions for DTEs or repeaters in cases where the MAU is embedded
d) Environmental conditions
e) Power supply voltage range

The above list is illustrative and is neither mandatory nor exhaustive.

8.8.3.3 Exception information

It may occasionally happen that a supplier will wish to answer an item with mandatory or prohibited status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No preprinted answer will be found in the Support column for this. Instead, the supplier shall write the missing answer into the Support column, together with an X<i> reference to an item of Exception Information, and shall provide the appropriate rationale in the Exception item itself.

An implementation for which an Exception item is required in this way does not conform to this standard.

8.8.3.4 Conditional items

The PICS proforma contains a number of conditional items. These are items for which both the applicability of the item itself, and its status if it applies—mandatory, optional, or prohibited—are dependent upon whether or not certain other items are supported.

Individual conditional items are indicated by a conditional symbol of the form “<item>:<s>” in the Status column, where “<item>” is the section number and item reference that appears in the first column of the

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table for some other item, and "<s>" is a status symbol, M, O, O.<n>, or X. The "!" symbol, prefixed to an item reference, means logical negation.

If the item referred to by the conditional symbol is marked as supported, the conditional item is applicable, and its status is given by "<s>"; the support column is to be completed in the usual way. Otherwise, the conditional item is not relevant and the Not Applicable (N/A) answer is to be marked.

Each item whose reference is used in a conditional symbol is indicated by an asterisk in the Item column.

8.8.4 Identification

8.8.4.1 Implementation identification

The MAU supplier shall complete the relevant fields in this section to identify the supplier and the particular MAU.

Supplier	
Contact point for queries about the PICS	
Implementation name(s) and version(s)	

8.8.4.2 Protocol summary

The supplier will complete this section to identify the precise protocol implemented.

Identification of protocol specification	IEEE Std 802.3-2002, Clause 8, Medium Attachment Unit and baseband medium specifications, type 10BASE5
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exception items been required? (The answer Yes means that the implementation does not conform to this standard.)	Yes [ ] No [ ]

Date of Statement	

8.8.5 Global statement of conformance

The supplier must indicate below whether or not the implementation implements all the mandatory requirements. Answering No to this question indicates nonconformance to the protocol specification. Nonsupported mandatory capabilities are to be identified in the PICS, with an explanation of why the implementation is non-conforming.

This implementation meets all mandatory requirements	Yes [ ] No [ ]

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8.8.6 PICS proforma tables for MAU

8.8.6.1 MAU compatibility

Item	Parameter	Reference	Status	Support	Value/comment
*1	MAU intended for attachment to repeater		O	Yes [ ]No [ ]	
*2	Monitor Function supported		O	Yes [ ]No [ ]	
*3	AUI Circuit CO supported		8.8.6.1/2 :M !8.8.6.1/2 :O	N/A [ ] Yes [ ]No [ ] N/A [ ] Yes [ ]No [ ]	Required for Monitor function
4	SQE Test supported	9.4.1	8.8.6.1/1 :X !8.8.6.1/1 :M	N/A [ ] Yes [ ]No [ ] N/A [ ] Yes [ ]No [ ]	Function not performed for MAUs attached to repeaters

8.8.6.2 Transmit function

Item	Parameter	Reference	Status	Support	Value/comment
1	Transmit path	8.2.1.1	M	Yes [ ]No [ ]	DO circuit to coaxial cable
2	Transmit signal polarity	8.2.1.1	M	Yes [ ] No [ ]	DO A positive relative to DO B causes more positive voltage on the coaxial medium
3	Start-up bit loss (DO to coaxial cable)	8.2.1.1	M	Yes [ ]No [ ]	2 bits max
4	Transmit settling time	8.2.1.1	M	Yes [ ]No [ ]	Second and following bits meet amplitude and jitter specifications
5	Transmit steady-state delay	8.2.1.1	M	Yes [ ]No [ ]	1/2 bit times max
6	Start-up bit loss (DO to coaxial cable) variability	8.2.1.1	M	Yes [ ]No [ ]	2 bits max between packets separated by ≤ 96 BT
7	No extraneous signal on the coaxial media after DO idle	8.2.1.1	M	Yes [ ]No [ ]	
8	Start collision presence state	8.2.1.1	M	Yes [ ]No [ ]	Within 0.6 μs to 1.6 μs after idle
9	Collision presence state duration	8.2.1.1	M	Yes [ ]No [ ]	5–15 bit times

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8.8.6.3 Receive function

Item	Parameter	Reference	Status	Support	Value/comment
1	Direct coupling of signal from medium to the receiver	8.2.1.2	M	Yes [ ] No [ ]	
2	AC coupling from the receiver to AUI interface	8.2.1.2	M	Yes [ ] No [ ]	
3	Start-up bit loss (coaxial cable to DI)	8.2.1.2	M	Yes [ ] No [ ]	5 bits max
4	Receive settling time	8.2.1.2	M	Yes [ ] No [ ]	Second and following bits meet jitter specifications
5	Receive steady-state delay	8.2.1.2	M	Yes [ ] No [ ]	1/2 bit times max
6	Start-up bit loss (coaxial cable to DI) variability	8.2.1.2	M	Yes [ ] No [ ]	5 bits max between packets separated by ≤ 96 BT
7	Receive signal polarity	8.2.1.2	M	Yes [ ] No [ ]	More positive voltage on the coaxial cable will convert as DI A positive relative to DI B on the DI circuits
8	Edge jitter	8.2.1.2	M	Yes [ ] No [ ]	MAU receiver + cable introduce ≤ 6 ns
9	Receive function while transmitting	8.2.1.2	M	Yes [ ] No [ ]	

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8.8.6.4 Collision function

Item	Parameter	Reference	Status	Support	Value/comment
1	Collision absence	8.2.1.3	M	Yes [ ] No [ ]	IDL signal on the CI circuit, unless sending *mau_not_available*
2	Collision Presence function requirements	8.2.1.3	8.8.6.1/1 :X !8.8.6.1/1 :M	N/A [ ] Yes [ ] No [ ] N/A [ ] Yes [ ] No [ ]	CS0 on CI circuit at BR +25%, −15% with a duty cycle not worse than 40/60 ratio with ≥ 2 MAUs transmitting
3	No collision detection with single transmitter	8.2.1.3 8.2.2.2.4	M	Yes [ ] No [ ]	No CS0 on CI
4	Collision assertion after transmission of ≥ 20 bit times	8.2.1.3 8.2.2.2.4	8.8.6.1/1 :X !8.8.6.1/1 :M	N/A [ ] Yes [ ] No [ ] N/A [ ] Yes [ ] No [ ]	CS0 on CI ≤ 17 BT after collision
5	Collision assertion by transmission < 20 bit times	8.2.1.3 8.2.2.2.4	8.8.6.1/1 :X !8.8.6.1/1 :M	N/A [ ] Yes [ ] No [ ] N/A [ ] Yes [ ] No [ ]	CS0 on CI ≤ 29 BT after collision
6	Collision deassertion after end of collision between second MAU	8.2.1.3	M	Yes [ ] No [ ]	IDL on CI ≤ 17 BT after arrival of end of transmission
7	Collision deassertion after end of collision between more than two MAUs	8.2.1.3	M	Yes [ ] No [ ]	IDL on CI ≤ 29 BT after arrival of end of transmission from all but one MAU

8.8.6.5 Monitor function

Item	Parameter	Reference	Status	Support	Value/comment
1	Signal path	8.2.1.4	8.8.6.1/2 :M	N/A [ ] Yes [ ] No [ ]	From DTE to MAU through CO circuit
2	Transmit disable delay	8.2.1.4	8.8.6.1/2 :M	N/A [ ] Yes [ ] No [ ]	≤ 20 ms
3	MAU function in isolated state	8.2.1.4	8.8.6.1/2 :M	N/A [ ] Yes [ ] No [ ]	Receive and collision functions are normal, XMIT disabled

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8.8.6.6 Jabber function

Item	Parameter	Reference	Status	Support	Value/comment
1	Jabber function implementation	8.2.1.5	M	Yes [ ] No [ ]	Self-interruption of the transmitter
2	Frame timer range	8.2.1.5	M	Yes [ ] No [ ]	20 ms min, 150 ms max
3	CI circuit during jabber	8.2.1.5 8.2.2.2.4	8.8.6.1/1 :X !8.8.6.1/1 :M	N/A [ ] Yes [ ] No [ ] N/A [ ] Yes [ ] No [ ]	CS0 signal
4	Collision presence function activated after transmit disable	8.2.1.5	M	Yes [ ] No [ ]	No extraneous signal on the coaxial media
5	Unjab timer range	8.2.1.5	O	Yes [ ] No [ ]	0.5 s ± 50%
6	MAU unjab (reset) with monitor function	8.2.1.5	8.8.6.1/2 :M	N/A [ ] Yes [ ] No [ ]	Isolate message
7	MAU jabber lockup protection	9.4.1	8.8.6.1/1 :M !8.8.6.1/1 :O	N/A [ ] Yes [ ] No [ ] N/A [ ] Yes [ ] No [ ]	Jabber function not activated under worst case conditions in 9.6.5

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8.8.6.7 MAU to coaxial cable interface

Item	Parameter	Reference	Status	Support	Value/comment
1	Input impedance	8.3.1.1	M	Yes [ ] No [ ]	R ≥ 100 kΩ
2	Total capacitive load	8.3.1.1	M	Yes [ ] No [ ]	C ≤ 4 pF
3	Bias current	8.3.1.2	M	Yes [ ] No [ ]	Max +2 μA Min –25 μA
4	Transmit offset current	8.3.1.3	M	Yes [ ] No [ ]	–37 mA to – 45 mA
5	Transmit ac component	8.3.1.3	M	Yes [ ] No [ ]	+28 mA to offset value
6	Transmitter sink current during collision	8.3.1.3	M	Yes [ ] No [ ]	No more than –25 μA at –7 V; no more than ±250 μA at –10 V
7	Rise and fall time at 10 Mb/s	8.3.1.3	M	Yes [ ] No [ ]	25 ± 5 ns (10–90%)
8	Rise and fall time match	8.3.1.3	M	Yes [ ] No [ ]	Within 2 ns at 10 Mb/s
9	Harmonic content at BR	8.3.1.3	M	Yes [ ] No [ ]	2nd and 3rd harmonics ≥ 20 dB below fundamental, 4th and 5th harmonics ≥ 30 dB below fundamental, 6th and 7th harmonics ≥ 40 dB below fundamental, all higher harmonics ≥ 50 dB below fundamental
10	Transmit signal polarity	8.3.1.4	M	Yes [ ] No [ ]	No inversion of signal from PLS to coaxial cable
11	Transmit signal edge jitter	8.3.1.4	M	Yes [ ] No [ ]	MAU introduce no more than 2 ns of edge jitter
12	Receive collision detection threshold	8.3.1.5	M	Yes [ ] No [ ]	–1.448 V to –1.59 V
13	Receive collision detection threshold, large impulse response	8.3.1.5	M	Yes [ ] No [ ]	–1293 mV * [1+ impulse response] if filter impulse response is larger than nominal
14	No negative edge transmission	8.3.1.4	M	Yes [ ] No [ ]	After cessation of CD output stream on DO or before first edge of next frame on DO

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8.8.6.8 MAU electrical characteristics

Item	Parameter	Reference	Status	Support	Value/comment
1	Isolation impedance between MDI and AUI cable (each conductor, including shields)	8.3.2.1	M	Yes [ ] No [ ]	> 250 kΩ at 60 Hz, < 15 Ω for 3 MHz to 30 MHz
2	Breakdown voltage	8.3.2.1	M	Yes [ ] No [ ]	≥ 1.5 kV ac, rms
3	Current drawn from AUI sources	8.3.2.2	M	Yes [ ] No [ ]	≤ 0.5 A
4	Operation over VP voltage range	8.3.2.2	M	Yes [ ] No [ ]	11.28–15.75 V, any permissible AUI cable
5	Low VP circuit behavior	8.3.2.2	M	Yes [ ] No [ ]	No disruption of media
6	MAU current labeling	8.3.2.2	M	Yes [ ] No [ ]	Current consumption shall be labeled externally
7	Reliability	8.3.2.3	M	Yes [ ] No [ ]	MTBF ≥ 1 million hours of continuous operation

8.8.6.9 MAU-DTE requirements

Item	Parameter	Reference	Status	Support	Value/comment
1	AUI electrical characteristics	8.3.3	M	Yes [ ] No [ ]	As specified in Clause 7; refer to 8.8.7.1–5
2	AUI mechanical connection	8.3.4	M	Yes [ ] No [ ]	As specified in Clause 7; refer to 8.8.7.6

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8.8.6.10 MAU to coaxial cable connection

Item	Parameter	Reference	Status	Support	Value/comment
1	Standard N-type connector	8.5	O.1	Yes[ ] No [ ]	50 Ω, according to IEC 60169-16: 1982 and Amd. 1: 1996
*2	Coaxial tap connector	8.5.3	O.1	Yes[ ] No [ ]	
3	Capacitance	8.5.3.1	8.8.6.10/2 :M	N/A[ ] Yes[ ] No [ ]	2 pF nominal at 10 MHz
4	Contact resistance	8.5.3.1	8.8.6.10/2 :M	N/A[ ] Yes[ ] No [ ]	≤ 50 mΩ for shield and center conductor
5	Voltage rating	8.5.3.1	8.8.6.10/2 :M	N/A[ ] Yes[ ] No [ ]	600 V dc or ac rms max
6	Dc leakage resistance between braid and external conductors	8.5.3.1	8.8.6.10/2 :M	N/A[ ] Yes[ ] No [ ]	> 1 GΩ
7	Probe current rating	8.5.3.1	8.8.6.10/2 :M	N/A[ ] Yes[ ] No [ ]	0.1 A per contact (probe and shield)
8	Shield current rating	8.5.3.1	8.8.6.10/2 :M	N/A[ ] Yes[ ] No [ ]	1 A surge for 1 s
9	Connector housing	8.5.3.2.1	8.8.6.10/2 :M	N/A[ ] Yes[ ] No [ ]	Shielding > 40 dB at 50 MHz
10	Shield probe characteristics	8.5.3.2.3	8.8.6.10/2 :M	N/A[ ] Yes [ ] No [ ]	Effective capture of outer braid

8.8.6.11 Safety requirements

Item	Parameter	Reference	Status	Support	Value/comment
1	MAU labeling	8.6.3	O	Yes [ ] No [ ]	Data rate, current, any applicable safety warnings (recommended)
2	General safety	8.7.1	M	Yes [ ] No [ ]	Conforms to IEC 60950: 1991
3	Susceptibility levels	8.7.3.1	M	Yes [ ] No [ ]	Either ambient plane wave field of 2 V/m from 10 kHz through 30 MHz, 5 V/m from 30 MHz through 1 GHz, or interference voltage of 1 V/ns peak slope, between coaxial cable shield and DTE earth connection
4	Emission levels	8.7.3.2	M	Yes [ ] No [ ]	Comply with applicable local and national standards

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8.8.7 PICS proforma tables for MAU AUI characteristics

8.8.7.1 Signal characteristics

Item	Parameter	Reference	Status	Support	Value/comment
1	Signaling rate (stated on label)	7.3.2	M	Yes [ ] No [ ]	10 Mb/s
2	CS0 signal frequency (on CI)	7.3.1.2	M	Yes [ ] No [ ]	10 MHz +25%, –15%
3	CS0 signal duty cycle	7.3.1.2	M	Yes [ ] No [ ]	60:40 worst case

8.8.7.2 DI and CI driver characteristics

Item	Parameter	Reference	Status	Support	Value/comment
1	Differential output voltage, loaded	7.4.1.1	M	Yes [ ] No [ ]	Figure 7–11
2	Differential output voltage, idle state	7.4.1.1	M	Yes [ ] No [ ]	≤ 40 mV into test load
3	Differential output voltage, start of idle	7.4.1.1	M	Yes [ ] No [ ]	Figure 7–12
4	Current into test load while idle	7.4.1.1	M	Yes [ ] No [ ]	4 mA max after 80 BT
5	Requirements after idle	7.4.1.2	M	Yes [ ] No [ ]	Second bit to Figure 7–11
6	Common-mode output voltage, ac	7.4.1.3	M	Yes [ ] No [ ]	≤ 40 mV peak, Figure 7–13
7	Differential output voltage, open circuit	7.4.1.4	M	Yes [ ] No [ ]	13 V peak max
8	Common-mode output voltage, dc	7.4.1.5	M	Yes [ ] No [ ]	≤ 5.5 V, Figure 7–13
9	Fault tolerance	7.4.1.6	M	Yes [ ] No [ ]	Figure 7–14
10	Fault current	7.4.1.6	M	Yes [ ] No [ ]	≤ 150 mA, any Figure 7–14 state

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8.8.7.3 DO receiver characteristics

Item	Parameter	Reference	Status	Support	Value/comment
1	Unsquelched threshold	7.4.2.1	M	Yes [ ] No [ ]	160 mV max differential
2	High-to-idle transition on DO circuit	7.4.1.1	M	Yes [ ] No [ ]	Must not cause output
3	Differential input impedance at 10 MHz	7.4.2.2	M	Yes [ ] No [ ]	Real part: 77.83 Ω ± 6%; 0 ≤ phase angle (deg) ≤ real part × 0.0338
4	Common-mode range, ac	7.4.2.3	M	Yes [ ] No [ ]	3 V min 30 Hz to 40 kHz, 100 mV min 40 kHz to 10 MHz
5	Total common-mode range	7.4.2.4	M	Yes [ ] No [ ]	Magnitude of 0 to 5.5 V ac + dc
6	Common-mode current limit	7.4.2.4	M	Yes [ ] No [ ]	≤ 1 mA
7	IDL detection	7.3.1.1	M	Yes [ ] No [ ]	≤ 1.6 bit times
8	Requirements after idle	7.4.2.5	M	Yes [ ] No [ ]	Receiver in spec after start-up delay
9	Receiver fault tolerance	7.4.2.6	M	Yes [ ] No [ ]	Figure 7–16
10	Input fault current	7.4.2.6	M	Yes [ ] No [ ]	3 mA max

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8.8.7.4 CO receiver characteristics

Item	Parameter	Reference	Status	Support	Value/comment
1	Unsquelched threshold	7.4.2.1	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	160 mV max differential
2	High-to-idle transition on DO circuit	7.4.1.1	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	Must not cause output
3	Differential input impedance at 10 MHz	7.4.2.2	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	Real part: 77.83 Ω ± 6%; 0 ≤ phase angle (deg) ≤ real part × 0.0338
4	Common-mode range, ac	7.4.2.3	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	3 V min 30 Hz to 40 kHz, 100 mV min 40 kHz to 10 MHz
5	Total common-mode range	7.4.2.4	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	Magnitude of 0 to 5.5 V ac + dc
6	Common-mode current limit	7.4.2.4	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	≤ 1 mA
7	IDL detection	7.3.1.1	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	≤ 1.6 bit times
8	Requirements after idle	7.4.2.5	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	Receiver in spec after start-up delay
9	Receiver fault tolerance	7.4.2.6	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	Figure 7–16
10	Input fault current	7.4.2.6	8.8.6.1/3 :M	N/A[ ] Yes[ ] No [ ]	3 mA max

8.8.7.5 Circuit termination

Item	Parameter	Reference	Status	Support	Value/comment
1	Common-mode termination	7.4.2.6	M	Yes [ ] No [ ]	If used, must be to VC
2	Pins 1, 4, 8, 11, 14 impedance to VC circuit	7.5.2.8	M	Yes [ ] No [ ]	≤ 5 Ω at 5 MHz
3	Pins 1, 4, 8, 11, 14 coupling to VC circuit	7.5.2.8	M	Yes [ ] No [ ]	Capacitive

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8.8.7.6 Mechanical characteristics

Item	Parameter	Reference	Status	Support	Value/comment
1	D-type connector dimensions	7.6.2	M	Yes [ ] No [ ]	IEC 60807-2: 1992 15-pole male
2	Shell plating material	7.6.2	M	Yes [ ] No [ ]	Conductive
3	Shell multiple contact points	7.6.2	O	Yes [ ] No [ ]	Number not defined (recommended)
4	Shell life expectancy	7.6.2	M	Yes [ ] No [ ]	≤ 5 mΩ/500 matings
5	Locking posts and mounting	7.6.1	M	Yes [ ] No [ ]	Figures 7–18, 7–20
	Pin connections:				Circuit
6	3	7.6.3	M	Yes [ ] No [ ]	Data out A
7	10	7.6.3	M	Yes [ ] No [ ]	Data out B
8	11	7.6.3	M	Yes [ ] No [ ]	Capacitor to VC
9	5	7.6.3	M	Yes [ ] No [ ]	Data in A
10	12	7.6.3	M	Yes [ ] No [ ]	Data in B
11	4	7.6.3	M	Yes [ ] No [ ]	Capacitor to VC
12	7	7.6.3	M	Yes [ ] No [ ]	Control out A
13	15	7.6.3	M	Yes [ ] No [ ]	Control out B
14	8	7.6.3	M	Yes [ ] No [ ]	Capacitor to VC
15	2	7.6.3	M	Yes [ ] No [ ]	Control in A
16	9	7.6.3	M	Yes [ ] No [ ]	Control in B
17	1	7.6.3	M	Yes [ ] No [ ]	Capacitor to VC
18	6	7.6.3	M	Yes [ ] No [ ]	Voltage common
19	13	7.6.3	M	Yes [ ] No [ ]	Voltage plus
20	14	7.6.3	M	Yes [ ] No [ ]	Capacitor to VC
21	Shell	7.6.3	M	Yes [ ] No [ ]	Protective ground (conductive shell)

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8.8.8 PICS proforma tables for 10BASE5 coaxial cable

8.8.8.1 10BASE5 coaxial cable characteristics

Item	Parameter	Reference	Status	Support	Value/comment
1	Characteristic impedance	8.4.1.1	M	Yes [ ] No [ ]	50 ± 2 Ω, measured according to IEC 60096-1: 1986 and Amd. 2: 1993
2	Impedance variation per 2 m segment	8.4.1.1	O	Yes [ ] No [ ]	±3 Ω
3	Attenuation of 500 m segment	8.4.1.2	M	Yes [ ] No [ ]	≤8.5 dB with 10 MHz sine wave, ≤6.0 dB with 5 MHz sine wave
4	Velocity of propagation	8.4.1.3	M	Yes [ ] No [ ]	Min 0.77 c
5	Edge jitter of 500 m cable	8.4.1.4	M	Yes [ ] No [ ]	≤7 ns
6	Transfer impedance	8.4.1.5	M	Yes [ ] No [ ]	According to Figure 8–7
7	Cable DC loop resistance (center conductor plus shield)	8.4.1.6	M	Yes [ ] No [ ]	≤10 mΩ/m at 20 °C
Coaxial cable properties:					
8	a) Center conductor, dielectric, shield system, insulating jacket	8.4.2.1.1	M	Yes [ ] No [ ]	
9	b) Concentricity	8.4.2.1.1	M	Yes [ ] No [ ]	≥ 92%
10	c) Jacket, shield, dielectric	8.4.2.1.1	M	Yes [ ] No [ ]	pierceable
11	d) Cable flexibility	8.4.2.1.1	M	Yes [ ] No [ ]	support bend radius of 254 mm
12	Center conductor	8.4.2.1.2	M	Yes [ ] No [ ]	2.17 mm ± 0.013 mm
13	Dielectric material	8.4.2.1.3	M	Yes [ ] No [ ]	meets 8.4.1.2, 8.4.1.3 and 8.4.2.1.1 c)
Shielding system:					
14	a) Inside diameter	8.4.2.1.4	M	Yes [ ] No [ ]	≥ 6.15 mm
15	b) Outside diameter	8.4.2.1.4	M	Yes [ ] No [ ]	8.28 mm ± 0.178 mm
16	c) Outermost shield	8.4.2.1.4	M	Yes [ ] No [ ]	> 90% coverage
17	Jacket material	8.4.2.1.5	M	Yes [ ] No [ ]	meets 8.4.1 and 8.4.2 specs

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Item	Parameter	Reference	Status	Support	Value/comment
18	Jacket dimensions, Polyvinyl Chloride	8.4.2.1.5	O.2	Yes [ ] No [ ]	OD of 10.287 mm ± 0.178 mm
19	Jacket dimensions, Fluoropolymer	8.4.2.1.5	O.2	Yes [ ] No [ ]	OD of 9.525 mm ± 0.254 mm
20	Flammability and smoke criteria	8.4.2.1.5	M	Yes [ ] No [ ]	Meet applicable local and national codes
21	Jacket marking	8.4.2.2	M	Yes [ ] No [ ]	Annular rings spaced 2.5 m ± 5 cm
22	Color of jacket	8.4.2.2	O	Yes [ ] No [ ]	Bright (example: yellow)
Total segment dc loop resistance:					
23	a) Sum of center conductor, connector and shield	8.4.3	M	Yes [ ] No [ ]	≤5 Ω at 20° C
24	b) Inline connector pair or MAU	8.4.3	M	Yes [ ] No [ ]	≤10 mΩ at 20° C
25	Inline coaxial extension connector	8.5.1	M	Yes [ ] No [ ]	Type N plug connector
26	Coaxial cable termination	8.5.2.1	M	Yes [ ] No [ ]	50 Ω ± 1% at 0–20 MHz, phase angle ≤ 5°, power rating ≥1 Ω

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9. Repeater unit for 10 Mb/s baseband networks

9.1 Overview

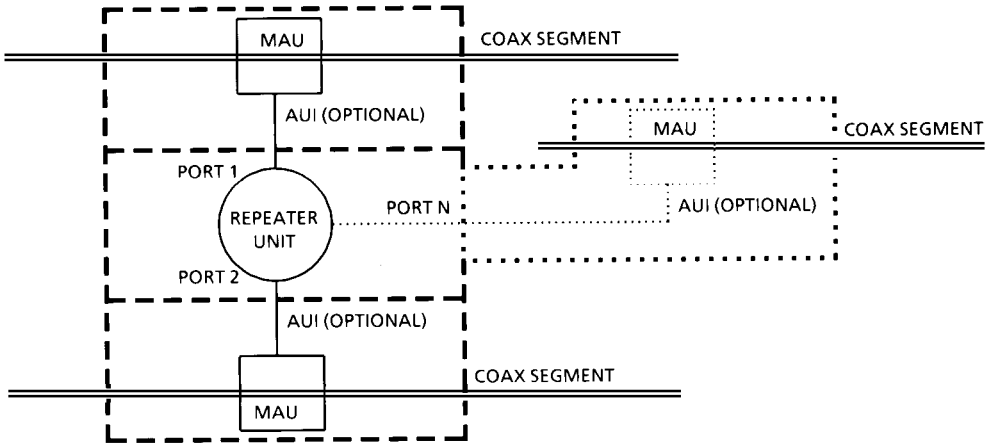
This clause specifies a repeater for use with IEEE 802.3 10 Mb/s baseband networks. A repeater for any other IEEE 802.3 network type is beyond the scope of this clause.

A repeater set connects segments of network medium together, thus allowing larger topologies and a larger MAU base than are allowed by rules governing individual segments.

Repeater sets are used to extend the network length and topology beyond what could be achieved by a single mixing segment. Mixing segments may be connected directly by a repeater set (Figure 9–1) or by several repeater units that are, in turn, connected by link segments. Repeater sets are also used as the hub in a star topology network in which DTEs attach directly to link segments (e.g., 10BASE-T, Clause 14). Allowable topologies shall contain only one operative signal path between any two points on the network. The proper operation of a CSMA/CD network requires network size to be limited to control round-trip propagation delay to meet the requirements of 4.2.3.2.3 and 4.4.2.1, and the number of repeaters between any two DTEs to be limited in order to limit the shrinkage of interpacket gap as it travels through the network. The method for validating networks with respect to these requirements is specified in Clause 13.

If the repeater set uses MAUs connected via AUIs to a repeater unit, these MAUs shall not perform the *signal_quality_error* Test function. A manufacturer may, optionally, integrate one or all MAUs into a single package with the repeater unit (internal MAUs). In all cases, the MAU portion of the repeater set must be counted toward the maximum number of MAUs on each segment. A repeater set is not a station and does not count toward the overall limit of 1024 stations on a network.

A repeater set can receive and decode data from any segment under worst-case noise, timing, and signal amplitude conditions. It retransmits the data to all other segments attached to it with timing and amplitude restored. The retransmission of data occurs simultaneously with reception. If a collision occurs, the repeater set propagates the collision event throughout the network by transmitting a Jam signal.



NOTE: The AUI is not necessarily exposed when the MAU is, optionally, part of the physical repeater.

Figure 9–1—Repeater set, coax-to-coax configuration

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9.2 References

See 1.3.

9.3 Definitions

See 1.4.

9.4 Compatibility interface

The repeater shall attach to its network segments by any of the means specified below.

9.4.1 AUI compatibility

The repeater unit shall be compatible at its AUI connector (if so equipped) as specified in Clause 7 with the exception of the *signal_quality_error* message Test, 7.2.1.2.3, which shall not be implemented.

10BASE5 and 10BASE2 MAUs associated with the repeater unit shall be as specified in Clause 8 for type 10BASE5 and Clause 10 for type 10BASE2 with the following restrictions:

a) The MAU shall implement receive mode collision detect as defined in 8.3.1.5 or 10.4.1.5.
b) The MAU shall not implement the *signal_quality_error* Message Test function as defined in 8.2.1.1 and 10.3.1.1. The MAU shall not activate its Jabber function when operated under the worst-case Jabber Lockup Protection condition as specified in 9.6.5.
c) The MAU shall operate only in the normal mode as defined in 8.1.3.4, not in the monitor mode.

All other MAUs associated with the repeater unit shall be as specified in their respective clauses and shall not perform the *signal_quality_error* Message Test function.

9.4.2 Mixing segment compatibility

The repeater set, which includes MAUs integrated with the repeater package (internal MAUs), may have any of the interfaces specified in the following subclauses. The MAUs associated with the repeater that are connected in this manner shall be subject to the restrictions of MAUs as specified in 9.4.1.

9.4.2.1 Direct coaxial cable attachment compatibility

The repeater shall be compatible at its coaxial tap connector (if so equipped) as specified in 8.5.3 of the 10BASE5 standard.

9.4.2.2 “N” connector compatibility

The repeater shall be compatible at its Type N connector (if so equipped) as specified in 8.5.

9.4.2.3 BNC compatibility

The repeater shall be compatible at its BNC connector (if so equipped) as specified in 10.6.

9.4.2.4 BFOC/2.5 (10BASE-FP) compatibility

The repeater shall be compatible at its BFOC/2.5 10BASE-FP connector (if so equipped) as specified in 15.3.2 (also see 15.1).

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9.4.3 Link segment compatibility

The compatibility interfaces for link segments including IRL segments are either vendor-dependent, as specified in 9.4.3.1, or are vendor-independent MDI, as defined in the remainder of this clause. The MAUs associated with the repeater that are connected in this manner shall be subject to the restrictions of MAUs as specified in 9.4.1.

9.4.3.1 Vendor-dependent IRL

The budget allowances for the topology supported by the IRL shall ensure that the total network round-trip delay requirement is met and the maximum collision frame size of 511 bits is not exceeded. (See 13.4.1.)

9.4.3.2 Fiber optic FOIRL compatibility

The repeater shall be compatible at its FSMA connector (if so equipped) as specified in 9.9.

9.4.3.3 Twisted-pair jack compatibility

The repeater set shall be compatible at its 8-pin modular jack (if so equipped), as specified in 14.5.

9.4.3.4 Fiber optic 10BASE-FB and 10BASE-FL compatibility

The repeater shall be compatible at its BFOC/2.5 (10BASE-FB and/or 10BASE-FL) connector (if so equipped) as specified in 15.3.2 (also see 15.1).

9.5 Basic functions

9.5.1 Repeater set network properties

The repeater set shall be transparent to all network acquisition activity and to all DTEs. The repeater set shall not alter the basic fairness criterion for all DTEs to access the network or weigh it toward any DTE or group of DTEs regardless of network location. A repeater set shall not attempt to be a packet store and forward device.

Repeaters are not addressable. An addressable station on the network that controls a repeater is outside the scope of this standard.

9.5.2 Signal amplification

The repeater set (including its associated or integral MAUs) shall ensure that the amplitude characteristics of the signals at the MDI outputs of the repeater set are within the tolerance of the specification for the appropriate MAU type. Therefore, any loss of signal-to-noise ratio due to cable loss and noise pickup is regained at the output of the repeater set as long as the incoming data is within the system specification.

9.5.3 Signal symmetry

The repeater set shall ensure that the symmetry characteristics of the signals at the MDI outputs of a repeater set are within the tolerance of the specification for the appropriate MAU type. Therefore, any loss of symmetry due to MAUs and media distortion is regained at the output of the repeater set.

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9.5.4 Signal retiming

The repeater unit shall ensure that the encoded data output from the repeater unit is within the jitter tolerance of a transmitting DTE as specified in 7.3. Therefore jitter cannot accumulate over multiple segments.

9.5.5 Data handling

The repeater unit, when presented a packet at any of its ports, shall pass the data frame of said packet intact and without modification, subtraction, or addition to all other ports connected with the repeater unit. The only exceptions to this rule are when contention exists among any of the ports or when the receive port is partitioned as defined in 9.6.6. Between unpartitioned ports, the rules for collision handling (9.5.6) take precedence.

9.5.5.1 Start-of-packet propagation delays

The start-of-packet propagation delay for a repeater set is the time delay between the first edge transition of the packet on its repeated from (input) port to the first edge transition of the packet on its repeated to (output) port (or ports).

For a repeater unit with AUI connectors at input and output ports, this time shall be less than or equal to 8 bit times.

For a repeater set with internal MAUs on input and output ports, additional delays shall be allowed as enumerated in Table 9–1.

Table 9–1—Start-of-packet propagation delays (Repeater unit delay of 8 BT plus)

MAU type	Input (BT)	Output (BT)
10BASE5	6.5	3.5
10BASE2	6.5	3.5
FOIRL	3.5	3.5
10BASE-T	8	5
10BASE-FP	3	4
10BASE-FB	2	2
10BASE-FL	5	5

9.5.5.2 Start-of-packet variability

The start-of-packet variability, defined as the total worst-case difference between start-of-packet propagation delays for successive packets separated by 96 bit times or less, shall be less than 4 bit times for a repeater unit. For a 10BASE-FB repeater set the total worst-case difference between start-of-packet propagation delays for successive packets separated by 96 bit times or less, shall be less than 2 bit times for a repeater set, all of which is allocated to the repeater unit.

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9.5.6 Collision handling

9.5.6.1 Collision presence

All MAUs connected to the repeater unit shall provide uninterrupted Carrier Sense. Uninterrupted Carrier Sense means that the input messages remain valid during activity on the medium even in the presence of a collision. 10BASE5 and 10BASE2 MAUs shall provide this capability by implementing Receive Mode Collision Detection.

9.5.6.2 Jam generation

If a collision is detected on any of the ports to which the repeater set is transmitting, the repeater set shall transmit a Jam to all of the ports to which it is connected. The Jam shall be transmitted in accordance with the Repeater Unit State Diagram in Figure 9–2 and shall be as specified in 4.2.3.2.4 with the further constraint that the first 62 bits transmitted to any port shall be a pattern of alternate 1's and 0's starting with the first bit transmitted as a 1.

9.5.6.3 Collision-jam propagation delays

The start-of-collision propagation delay for a repeater set is the time delay between the first edge transition of the *signal_quality_error* signal on any of its ports to the first edge transition of the Jam on its (output) port (or ports).

For a repeater unit with AUI connectors at input and output ports, this time shall be less than or equal to 6.5 bit times.

For a repeater set with internal MAUs on input and output ports, additional delays shall be allowed as enumerated in Table 9–2.

Table 9–2—Start-of-collision jam delays (repeater unit delay of 6.5 BT plus)

MAU type	Input (BT)	Output (BT)
10BASE5	9[a]	3.5
10BASE2	9[a]	3.5
FOIRL	3.5	3.5
10BASE-T	9	5
10BASE-FP	11.5	1
10BASE-FB	3.5	2
10BASE-FL	3.5	5

[a] This does not include collision rise time on the coaxial media. For the worst-case round-trip delay calculation, collision rise time plus MAU propagation delay = 17 bit times.

The cessation-of-jam propagation delay for a repeater unit is the time delay between the input signals at its ports reaching a state such that Jam should end at a port and the last transition of Jam at that port. The states of the input signals that should cause Jam to end are covered in detail in the repeater state diagrams.

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For a repeater unit with AUI connectors at input and output ports, this time shall be less than or equal to 5 bit times when not extending fragments. When extending fragments, this delay may be longer as required by the fragment extension algorithm. See 9.6.4.

For a repeater set with internal MAUs on input and output ports, an additional allowance for cessation-of-Jam propagation shall be allowed as specified in Table 9–3.

For a repeater set with internal MAUs on its input ports, an additional delay allowance for DI and for *signal_quality_error* de-assertion shall be made as specified in Table 9–3.

Table 9–3—Cessation-of-jam delays (repeater unit delay of 5 BT plus)

MAU type	Cessation-of-Collision jam from DI (BT)		Cessation-of-Collision jam from SQE (BT)	
	Input	Output	Input	Output
10BASE5	0.5	0.5	20	0.5
10BASE2	0.5	0.5	20	0.5
FOIRL	0.5	0.5	7	0.5
10BASE-T	2	2	9	2
10BASE-FP	3	3	36	3
10BASE-FB	5	2	5	2
10BASE-FL	2	2	7	2

9.5.6.4 Transmit recovery time

It is essential that the repeater unit not monitor a port for input for a short time after the repeater stops transmitting to that port. This recovery time prevents the repeater from receiving its own transmission as a new receive activity. The minimum recovery time allowable for a repeater is implementation-dependent, but must be greater than the sum of the delays in the transmit and receive paths for the port. In all cases the recovery time must be less than 10 bit times from the last transition on the transmitting AU interface.

9.5.6.5 Carrier recovery time

During a collision, the *input_idle* signal is unreliable for short periods of time (bits) because of the possibility of signal cancellation on the collision segment. In order to prevent premature detection of the true end of the collision, the repeater unit must wait for data to become sensed from a port for a short time after *signal_quality_error* has gone inactive from that port. This recovery time prevents the repeater from prematurely ending a Jam on an active network. The minimum carrier recovery time allowable for a repeater is implementation-dependent, but shall be greater than the CARRIER ON time after *signal_quality_error* is de-asserted. In all cases, the carrier recovery time shall be less than 4 bit times from the last transition on the AU Interface.

9.5.7 Electrical isolation

Network segments that have different isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of the repeater set.

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9.6 Detailed repeater functions and state diagrams

A precise algorithmic definition is given in this subclause, providing a complete procedural model for the operation of a repeater, in the form of state diagrams. Note that whenever there is any apparent ambiguity concerning the definition of repeater operation, the state diagrams should be consulted for the definitive statement.

The model presented in this subclause is intended as a primary specification of the functions to be provided by any repeater unit. It is important to distinguish, however, between the model and a real implementation. The model is optimized for simplicity and clarity of presentation, while any realistic implementation should place heavier emphasis on such constraints as efficiency and suitability to a particular implementation technology.

It is the functional behavior of any repeater unit implementation that shall match the standard, not the internal structure. The internal details of the procedural model are useful only to the extent that they help specify the external behavior clearly and precisely. For example, the model uses a separate Transmit Timer state machine for each port. However, in an actual implementation, the hardware may be shared.

9.6.1 State diagram notation

The notation used in the state diagrams (Figures 9–2 through 9–5) follows the conventions in 1.2.1.

Description of state diagram variables

Input/Output variables

DataIn (X)

Status of DataIn input at port X.
Values: **II** ; *input_idle*; i.e., indicates no activity
–II ; indicates activity
Note that DataIn (X) may be undefined during collision but that it is a don't care in all instances when this is true.

CollIn (X)

Status of ControlIn input at port X.
Values: **SQE** ; *signal_quality_error*; i.e., indicates collision
–SQE ; indicates no collision

Out (X)

Type of output repeater is sourcing at port X.
Values: **Idle** ; Repeater is not transmitting
–Idle ; Repeater is transmitting Preamble Pattern or Data or Jam or TwoOnes.
Preamble Pattern ; Repeater is sourcing alternating 1's and 0's on port X.
Data ; Repeater is repeating data frame on port X.
Jam ; Repeater is sourcing Jam on port X.
TwoOnes ; Repeater is sourcing two consecutive Manchester-encoded ones on port X.

DisableOut (X)

Override of Out (X)
Values: **ON** ; Disable repeater transmission regardless of value of Out (X).
–ON ; Repeater transmission depends on the value of Out (X).

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Port variables

TT (X)

Transmit Timer indicates number of bits transmitted on port X.
Values: Positive integers

Inter-Process flags

AllDataSent

All received data frame bits have been sent.

Bit Transmitted

Indicates a bit has been transmitted by the repeater unit.

DataRdy

Indicates the repeater has detected the SFD and is ready to send the received data. The search for SFD shall not begin before 15 bits have been received. Note, transmit and receive clock differences shall also be accommodated.

Tw1

Wait Timer for the end of transmit recovery time (see 9.5.6.4). It is started by StartTw1. Tw1Done is satisfied when the end of transmit recovery time is completed.

Tw2

Wait Timer for the end of carrier recovery time (see 9.5.6.5). It is started by StartTw2. Tw2Done is satisfied when the timer has expired.

Tw3

Wait Timer for length of continuous output (see 9.6.5). It is started by StartTw3. Tw3Done is satisfied when the timer has expired.

Tw4

Wait Timer for time to disable output for Jabber Lockup Protection (see 9.6.5). It is started by StartTw4. Tw4Done is satisfied when the timer has expired.

Port functions

Port (*Test*)

A function that returns the designation of a port passing the test condition. For example, Port (CollIn=SQE) returns the designation: X for a port that has SQE true. If multiple ports meet the test condition, the Port function will be assigned one and only one of the acceptable values.

Port designation

Ports are referred to by number. Port information is obtained by replacing the X in the desired function with the number of the port of interest. Ports are referred to in general as follows:

ALL — Indicates all repeater ports are to be considered. All ports shall meet test conditions in order for the test to pass.

ANY — Indicates all ports are to be considered. One or more ports shall meet the test conditions in order for the test to pass.

ONLY1 — Indicates all ports are to be considered. One, but not more than one, port shall meet the test condition in order for the test to pass.

X — Generic port designator. When X is used in a state diagram, its value is local to that diagram and not global to the set of state diagrams.

N — Is defined by the Port function on exiting the IDLE state of Figure 9–2. It indicates a port that caused the exit from the IDLE state.

M — Is defined by the Port function on exiting the TRANSMIT COLLISION state of Figure 9–2. It indicates the only port where CollIn=SQE.

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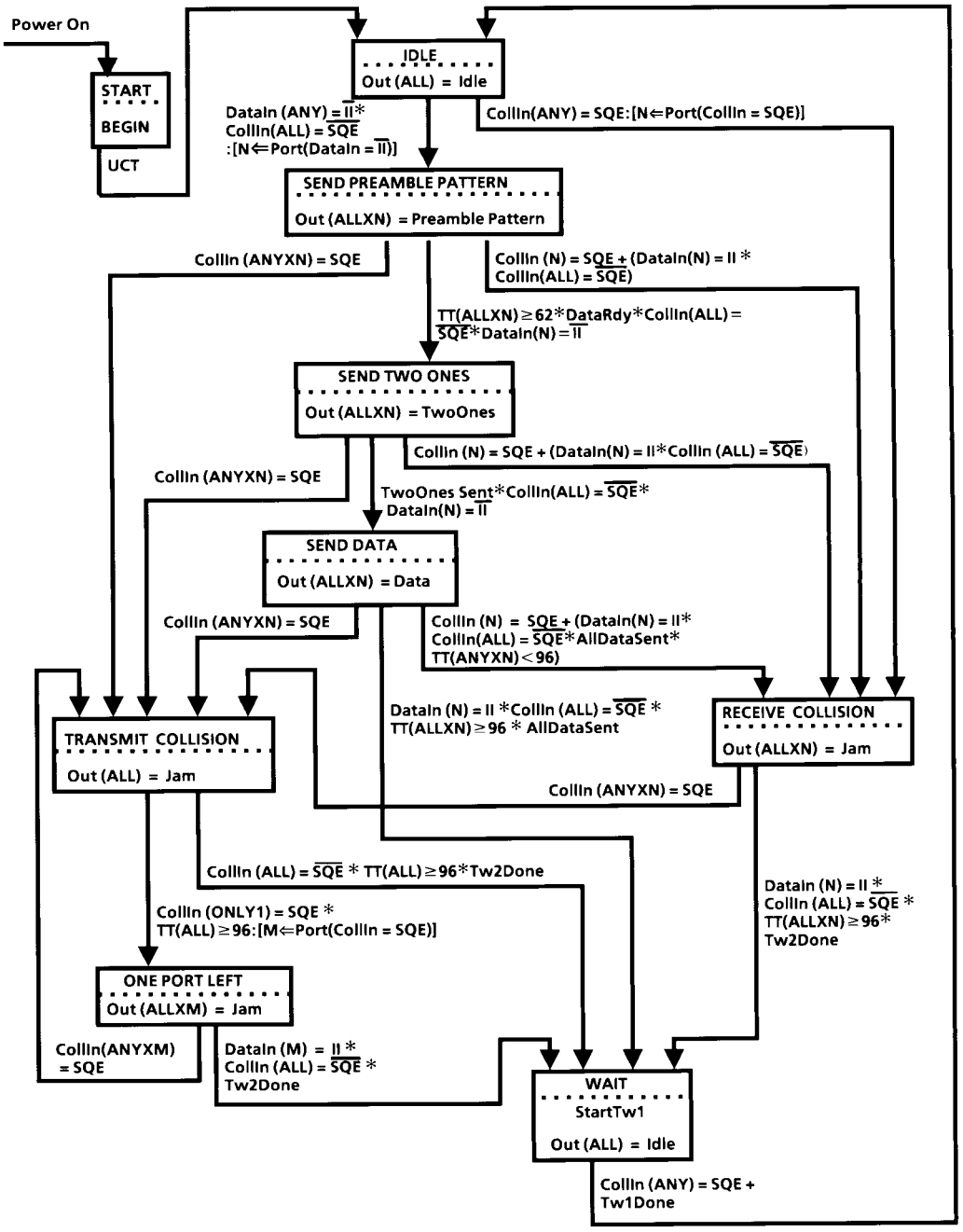
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ALLXN Indicates all ports except N should be considered. All ports considered shall meet the test conditions in order for the test to pass.

ALLXM Indicates all ports except M should be considered. All ports considered shall meet the test conditions in order for the test to pass.

ANYXN Indicates any port other than N meeting the test conditions shall cause the test to pass.

ANYXM Indicates any port other than M meeting the test conditions shall cause the test to pass.



NOTE: Out (X) = Idle in all instances unless specified otherwise.

Figure 9–2—Repeater unit state diagram

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9.6.2 Data and collision handling

The repeater unit shall implement the CARRIER_ON function for all its ports. Upon detection of carrier from one port, the repeater unit shall repeat all received signals in the Data Frame from that port to the other port (or ports).

The repeater unit data and collision-handling algorithm shall be as defined in Figure 9–2.

9.6.3 Preamble regeneration

The repeater unit shall output at least 56 bits of preamble followed by the SFD. When the repeater unit must send more than 56 bits, the maximum length preamble pattern it shall send is the number received plus 6. If the receive port is type 10BASE-FB, then the maximum length preamble pattern it shall send is the number received plus 2.

NOTE—Type 10BASE-FB ports always receive at least 56 bits of preamble due to the constraints on the transmitter and link.

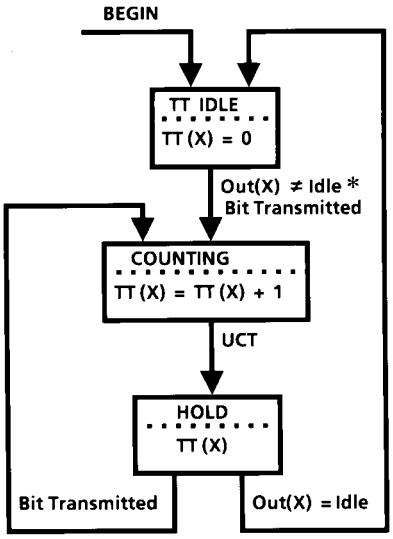


Figure 9–3—Transmit timer state diagram for Port X

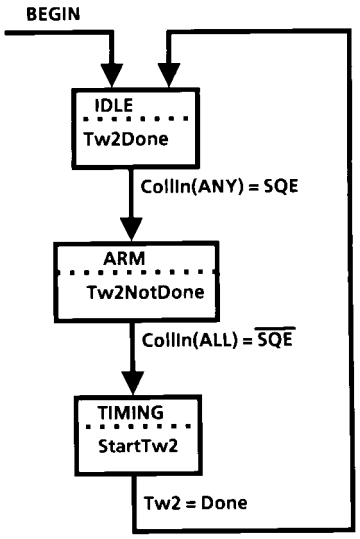


Figure 9–4—Tw2 state diagram

9.6.4 Fragment extension

If the received bit sequence from CARRIER_ON to CARRIER_OFF is fewer than 96 bits in length, including preamble, the repeater unit shall extend the output bit sequence with Jam such that the total number of bits output from the repeater unit shall equal 96.

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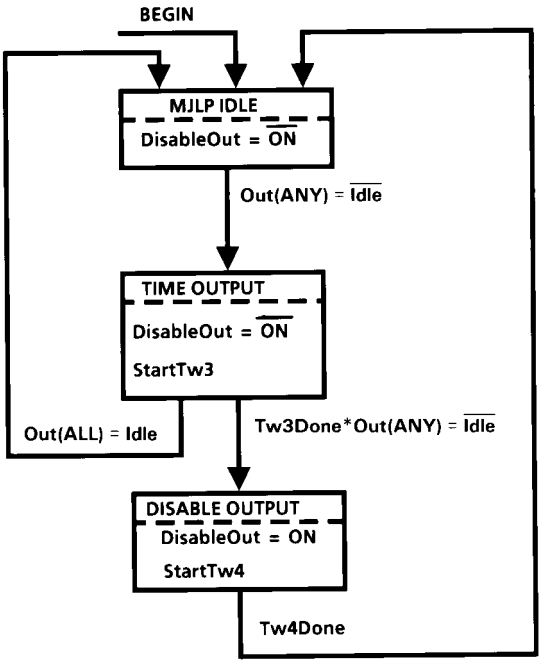


Figure 9–5—MAU jabber lockup protection state diagram

9.6.5 MAU Jabber Lockup Protection

MAU Jabber Lockup Protection must operate as shown in the MAU Jabber Lockup Protection state diagram. The repeater unit shall interrupt its output if it has transmitted continuously for longer than 5 ms or 50 000 bit times – 20% + 50%. The repeater unit shall then, after 96 to 116 bit times (9.6 to 11.6 μs), re-enable transmissions.

9.6.6 Auto-Partitioning/Reconnection (optional)

9.6.6.1 Overview

In large multisegment networks it may be desirable that the repeater unit protect the network from some fault conditions that would halt all network communication. A potentially likely cause of this condition could be due to a cable break, a faulty connector, or a faulty or missing termination.

In order to isolate a faulty segment's collision activity from propagating through the network, the repeater unit may optionally implement an auto-partition algorithm and, on detection of the malfunction being cleared, an auto-reconnection algorithm.

9.6.6.2 Detailed auto-partition/reconnection algorithm state diagram

Repeater sets with 10BASE-T MAUs shall implement an auto-partition/reconnection algorithm on those parts. The repeater unit may optionally implement an auto-partition/reconnection algorithm that protects the rest of the network from an open-circuited segment. If the repeater unit provides this function, it shall conform to the state diagram of Figure 9–6.

The algorithm defined in Figure 9–6 shall isolate a segment from the network when one of the following two conditions has occurred on the segment:

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a) When a consecutive collision count has been reached; or
b) When a single collision duration has exceeded a specific amount of time.

When a segment is partitioned, DataIn (X) and CollIn (X) from that segment are forced to II (input idle) and –SQE (no collision), respectively, so that activity on the port will not affect the repeater unit. Output from the repeater to the segment is not blocked.

The segment will be reinstated when the repeater has detected activity on the segment for more than the number of bits specified for Tw5 without incurring a collision.

Description of state diagram variables and constants

Port constants

CCLimit

The number of consecutive collisions that must occur before a segment is partitioned. The value shall be greater than 30.

Input/Output variables

DIPresent(X)

Data in from the MAU on port X. (This input is gated by the partition state machine to produce Dataln (X) to the main state machine.)

Values: II = *input_idle* ; no activity
–II = Input not idle ; activity

CIPresent(X)

Control input from the MAU on port X. (This input is gated by the partition state machine to produce CollIn (X) to the main state machine.)

Values: SQE = *signal_quality_error* ; indicates collision
–SQE ; indicates no collision

Port variables

CC(X)

Consecutive port collision count on a particular port X. Partitioning occurs on a terminal count of CCLimit being reached.
Values: Positive integers up to a terminal count of CCLimit.

Inter-Process Flags

Tw5

Wait Timer for length of packet without collision. Its value shall be between 450 and 560 bit times. It is started by StartTw5. Tw5Done is satisfied when the timer has expired.

Tw6

Wait Timer for excessive length of collision. Its value shall be between 1000 and 30 000 bit times. It is started by StartTw6. Tw6Done is satisfied when the timer has expired.

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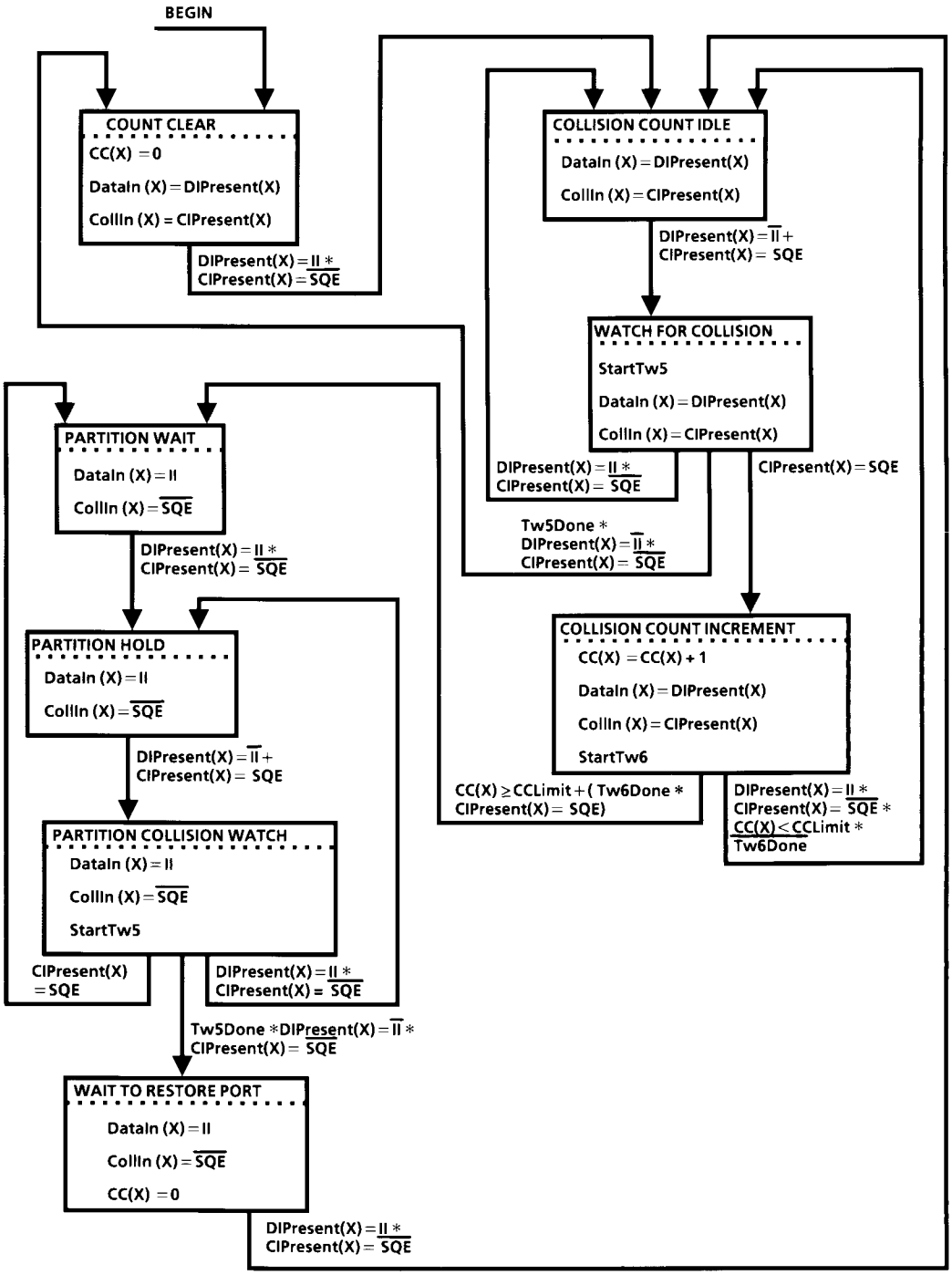


Figure 9–6—Partitioning state diagram for Port X

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9.7 Electrical isolation

There are two electrical power distribution environments to be considered that require different electrical isolation properties.

Environment A—When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.

Environment B—When a LAN crosses the boundary between separate power distribution systems or the boundaries of a single building.

The repeater unit shall comply with applicable local and national codes related to safety. See [B21].

9.7.1 Environment A requirements

Attachment of network segments via repeaters (sets) possessing internal MAUs requires electrical isolation of 500 V rms, 1 min withstand, between the segment and the protective ground of the repeater unit.

For repeater ports that connect to external MAUs via an AU Interface, the requirement for isolation is encompassed within the isolation requirements of the basic MAU/medium standard. (See 8.3.2.1, 9.9.3.1, 10.4.2.1, 14.3.1.1, and 15.3.4.) The repeater unit shall not require any electrical isolation between exposed AU Interfaces or between exposed AU Interfaces and chassis ground of the repeater unit. No isolation boundary need therefore exist at any AUI compatible interface (that is, "D" connector) provided by a repeater unit.

9.7.2 Environment B requirements

The attachment of network segments, which cross environment A boundaries, requires electrical isolation of 1500 V rms, 1 min withstand, between each segment and all other attached segments and also the protective ground of the repeater unit.

If segments are of an electrically conductive medium, it is recommended that this isolation be provided by the use of external MAUs connected by AU Interfaces. If internal MAUs are used for attachment to conductive media segments, then the segments shall be installed such that it is not possible for an equipment user to touch the trunk cable screen or signal conductor. A repeater of this variety requires professional installation.

The requirements for interconnected electrically conducting LAN segments that are partially or fully external to a single building environment may require additional protection against lightning strike hazards. Such requirements are beyond the scope of this standard.

It is recommended that the above situation be handled by the use of a nonelectrically conducting LAN segment (see 9.9 or Clause 15).

9.8 Reliability

A 2-port repeater set shall be designed to provide a mean time between failure (MTBF) of at least 50 000 hours of continuous operation without causing a communication failure among stations attached to the network medium. Repeater sets with more than two ports shall add no more than 3.46×10^{-6} failures per hour for each additional port.

The repeater set electronics shall be designed to minimize the probability of component failures within the repeater electronics that prevent communication among the other MAUs on the individual coaxial cable

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segments. Connectors and other passive components comprising the means of connecting the repeater to the coaxial cable shall be designed to minimize the probability of total network failure.

9.9 Medium attachment unit and baseband medium specification for a vendor-independent FOIRL

9.9.1 Scope

9.9.1.1 Overview

A vendor-independent FOIRL provides a standard means for connecting a repeater via optical fiber to another repeater or to a DTE. It thus extends the network length and topology beyond that which could be achieved by interconnecting coaxial cable segments via repeater sets only, as defined in 8.6 or 10.7. A vendor-independent FOIRL is suited for interconnecting repeaters and their respective segments located in different buildings. FOMAUs that are used for the DTE end of the link segment are beyond the scope of this clause. See Clause 18.

NOTE—The FOMAU specified in 9.9 has been superseded by the specification to be found in Clause 18. The new specification is fully compatible (except for media connector) with the specifications of 9.9 at the MDI. The new specification calls out more recent practice in connectors and state machines. It also provides improved performance for long link segments and reflects more recent industry input on flux parameters.

In particular, this clause defines the following:

a) The functional, optical, electrical, and mechanical characteristics of a fiber optic MAU (FOMAU) suitable for interfacing to a repeater unit, either directly (FOMAU and repeater unit integrated into a single package) or via an AUI mechanical connection.
b) Various optical fiber sizes suitable for connecting only two FOMAUs.

A schematic of the vendor-independent FOIRL and its relationship to the repeater unit is shown in Figure 9–7. The vendor-independent FOIRL comprises an optical fiber cable link segment, a vendor-independent FOMAU at each end of the link segment and, if present, AUI cables.

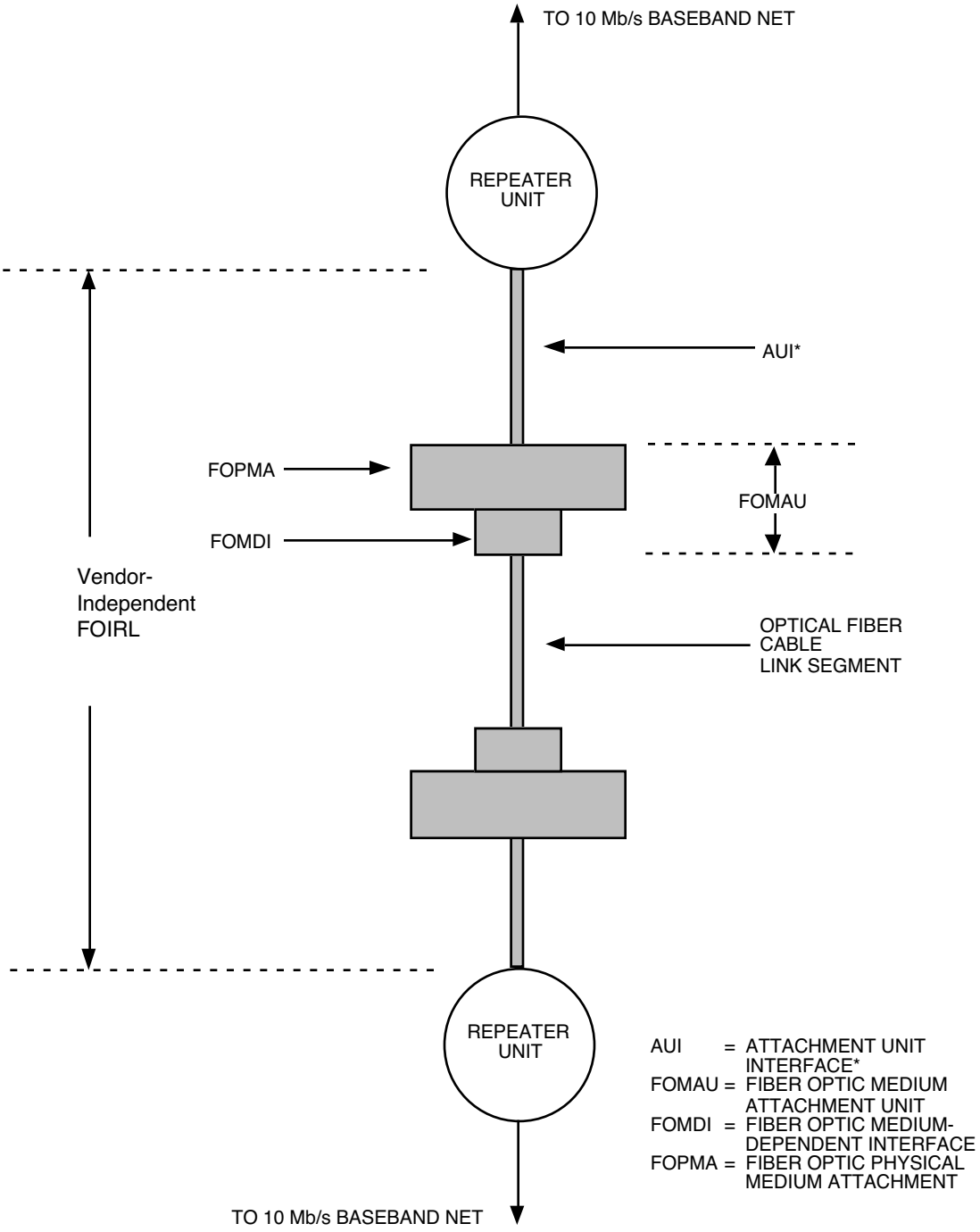
The purpose of this specification is to enable interoperability of FOMAUs that originate from different manufacturers, thereby facilitating the development of simple and inexpensive inter-repeater links (IRLs). To satisfy this objective, the FOMAU has the following general characteristics:

— Enables coupling the repeater unit PLS directly, or by way of the AUI mechanical connection, to the explicit baseband optical fiber cable link segment defined in this clause of the standard.
— Supports signaling at a data rate of 10 Mb/s.
— Provides for driving up to 1000 m of an optical fiber cable link segment.
— Operates indistinguishably from other types of repeater set MAUs, as defined in their respective 10 Mb/s baseband MAU sections when viewed from the AU Interface.
— Supports 10 Mb/s baseband system configurations as defined in Clause 13 of this standard.
— Allows integration of the FOMAU into a single package with the repeater unit, thereby eliminating the need for an AUI mechanical connection.

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See 9.9.1.3 for implementation requirements

Figure 9–7—Schematic of the vendor-independent FOIRL and its relationship to the repeater unit

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9.9.1.2 Application perspective: FOMAU and medium objectives

This clause states the broad objectives underlying the vendor-independent FOIRL specification defined throughout this clause of the standard. These are as follows:

a) Provide the physical means for connecting a repeater via fiber to another repeater or to a DTE.
b) Define a physical interface for the vendor-independent FOMAU component of the vendor-independent FOIRL that can be implemented independently among different manufacturers of hardware and achieve the intended level of compatibility when interconnected in a common IRL.
c) Provide a communication channel capable of high bandwidth and low bit error rate performance. The resultant BER of the FOIRL should be less than one part in 10^{10}.
d) Provide a means to prevent packet transmission through an FOIRL when transmission capability in one or both directions is disrupted.

9.9.1.3 Compatibility considerations

All implementations of the vendor-independent FOMAU shall be compatible at the FOMDI and at the AUI (when physically and mechanically implemented).

This standard provides an optical fiber cable link segment specification for the interconnection of only two FOMAU devices. The medium itself, the functional capability of the FOMAU, and the AUI are defined to provide the highest possible level of compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the FOMAU in an application-dependent manner provided the FOMDI and AUI are satisfied. (The provision of the physical and mechanical implementation of the AUI is optional.)

9.9.1.4 Relationship to AUI

A close relationship exists between this subclause and Clause 7. This subclause specifies all of the physical medium parameters, all of the FOPMA logical functions residing in the FOMAU, and references the AUI defined in Clause 7 with the exception of the *signal_quality_error* message Test of 7.2.1.2.3(3), which shall not be implemented, that is, shall not be enabled when connected to a repeater unit.

NOTE—The specification of a FOMAU component requires the use of both this subclause and Clause 7 for the AUI specifications.

9.9.1.5 Mode of operation

The FOMAU functions as a direct connection between the optical fiber cable link segment and the repeater unit. During collision-free operation, data from the repeater unit is transmitted into the FOMAU's transmit optical fiber, and all data in the FOMAU's receive optical fiber is transmitted to the repeater unit.

9.9.2 FOMAU functional specifications

The FOMAU component provides the means by which signals on the three AUI signal circuits are coupled:

a) From the repeater unit into the FOMAU's transmit optical fiber, and
b) From the FOMAU's receive optical fiber to the repeater unit.

To achieve this basic objective, the FOMAU component contains the following functional capabilities to handle message flow between the repeater unit and the optical fiber cable link segment:

a) *Transmit function*: The ability to receive serial bit streams from the attached repeater unit and transmit them into the FOMAU's optical fiber.

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b) *Receive function*: The ability to receive serial data bit streams from the FOMAU's receive optical fiber and transmit them to the attached repeater unit.

c) *Collision Presence function*: The ability to detect, and report to the attached repeater unit, an FOIRL collision.

d) *Jabber function*: The ability to automatically interrupt the Transmit function and inhibit an abnormally long output data stream.

e) *Low Light Level Detection function*: The ability to automatically interrupt the Receive function and Inhibit the reception of signals from the FOMAU's receive optical fiber which could result in abnormally high BERs.

9.9.2.1 Transmit function requirements

At the start of a packet transmission into the FOMAU's transmit optical fiber, no more than two bits (two full bit cells) of information may be received from the DO circuit and not transmitted into the FOMAU's transmit optical fiber. In addition, it is permissible for the first bit sent to contain encoded phase violations or invalid data. All successive bits of the packet shall be transmitted into the FOMAU's transmit optical fiber and shall exhibit the following:

a) No more edge jitter than that given by the sum of the worst-case edge jitter components specified in 7.4.3.6, 7.5.2.1, and 9.9.4.1.7, and
b) The levels and waveforms specified in 9.9.4.1.

The FOMAU DO circuit shall comply with the AUI specification for receivers given in 7.4.2. The FOMAU's DI circuit driver shall comply with the AUI specification for drivers given in 7.4.1.

The steady-state propagation delay between the DO circuit receiver input and the FOMAU's transmit optical fiber input shall not exceed one-half a bit cell. It is recommended that the designer provide an implementation in which a minimum threshold level is required on the DO circuit to establish a transmit bit stream.

The higher optical power level transmitted into the FOMAU's transmit optical fiber shall be defined as the low (LO) logic state on the optical fiber link segment. There shall be no logical signal inversions between the DO circuit and the FOMAU's transmit optical fiber, as specified in 9.9.4.1.5.

The difference in the start-up delay (bit loss plus invalid bits plus steady-state propagation delay), as distinct from the absolute start-up delays, between any two packets that are separated by 9.6 μs or less shall not exceed 2 bit cells.

The FOMAU shall loop back a packet received from the DO circuit into the DI circuit. At the start of a packet transmission, no more than five bits of information may be received from the DO circuit and not transmitted into the DI circuit. It is permissible for the first bit sent to contain encoded phase violations or invalid data. All successive bits of the packet shall be transmitted into the DI circuit and shall exhibit no more edge jitter than that specified for signals transmitted into the DI circuit by the Receive function, as specified in 9.9.2.2. The steady-state propagation delay between the DO circuit receiver input and the DI circuit driver output for such signals shall not exceed one bit cell. There shall be no logical signal inversions between the DO circuit and the DI circuit during collision-free transmission.

When the DO circuit has gone idle after a packet has been transmitted into the FOMAU's transmit optical fiber, the FOMAU shall not activate the Collision Presence function so as not to send the *signal_quality_error* message Test of 7.2.1.2.3(3) to the repeater unit.

During the idle state of the DO circuit, the Transmit function shall output into the transmit optical fiber an optical idle signal as specified in 9.9.4.1.4. The transmitted optical signals shall exhibit the optical power levels specified in 9.9.4.1.8. At the end of a packet transmission, the first optical idle signal pulse transition to the higher optical power level must occur no sooner than 400 ns and no later than 2100 ns after the

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packet's last transition to the lower optical power level. This first optical pulse must meet the timing requirements of 9.9.4.1.4.

The FOMAU shall not introduce extraneous optical signals into the transmit optical fiber under normal operating conditions, including powering-up or powering-down of the FOMAU.

9.9.2.2 Receive function requirements

At the start of a packet reception from the FOMAU's receive optical fiber, no more than two bits (two full bit cells) of information may be received from the FOMAU's receive optical fiber and not transmitted into the DI circuit. It is permissible for the first bit transmitted into the DI circuit to contain encoded phase violations or invalid data. All successive bits of the packet shall be transmitted into the DI circuit and shall exhibit the following:

a) The levels and waveforms specified in 7.4.1, and
b) No more edge jitter than that given by the sum of the worst-case edge jitter components specified in 7.4.3.6, 7.5.2.1, 9.9.4.1.7, 9.9.4.2.2, and 9.9.5.1.

The steady-state propagation delay between the output of the FOMAU's receive optical fiber and the output of the DI circuit driver shall not exceed one-half a bit cell. There shall be no logical signal inversions between the FOMAU's receive optical fiber and the DI circuit during collision-free operation, as specified in 9.9.4.2.3.

The difference in the start-up delay (bit loss plus invalid bits plus steady-state propagation delay), as distinct from the absolute start-up delays, between any two packets that are separated by 9.6 μs or less shall not exceed 2 bit cells.

The FOMAU shall not introduce extraneous signals into the DI circuit under normal operating conditions, including powering-up or powering-down of the FOMAU.

9.9.2.3 Collision Presence function requirements

The signal presented to the CI circuit in the absence of an SQE signal shall be the IDL signal.

The signal presented to the CI circuit during the presence of a collision shall be the CS0 signal, a periodic pulse waveform of frequency 10 MHz +25% –15% with pulse transitions that are no less than 35 ns and no greater than 70 ns apart at the zero crossing points. This signal shall be presented to the CI circuit no more than 3.5 bit times after the simultaneous appearance of signals at both the input of the FOMAU's transmit optical fiber and the output of the FOMAU's receive optical fiber. This signal shall be de-asserted no earlier than 4.5 bit times and no later than 7 bit times after the above defined collision condition ceases to exist.

During a collision, if a packet is received at the DO circuit before a packet is received at the FOMAU's receive optical fiber, then only the packet received at the DO circuit shall be transmitted into the DI circuit, as specified in 9.9.2.1. Conversely, if during a collision a packet is received at the FOMAU's receive optical fiber before a packet is received at the DO circuit, then only the packet received at the FOMAU's receive optical fiber shall be transmitted into the DI circuit, as specified in 9.9.2.2. In the event of both packets being received at their respective ports within 3.5 bit times of each other, then either one, but only one, of the packets shall be selected to be transmitted into the DI circuit.

The Collision function shall not introduce extraneous signals into the CI circuit under normal operating conditions, including powering-up or powering-down of the FOMAU.

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9.9.2.4 Jabber function requirements

The FOMAU shall have the capability, as defined in Figure 9–9, to interrupt a transmission from the repeater unit that exceeds a time duration determined by the FOMAU. This time duration shall not be less than 20 ms nor more than 150 ms. If the packet being transmitted is still being transmitted after the specified time duration, the FOMAU shall activate the Jabber function by the following:

a) First inhibiting the transmission of bits from its DO circuit into its transmit optical fiber,
b) Then transmitting into its transmit optical fiber the optical idle signal specified in 9.9.4.1.4, and
c) Presenting the CS0 signal to the CI circuit.

Once the error condition has been cleared, the FOMAU shall reset the Jabber function and present the IDL signal to the CI circuit:

a) On power reset, and
b) Optionally, automatically after a continuous period of 0.5 s ± 50% of inactivity on the DO circuit.

The FOMAU shall not activate its Jabber function when operated under the worst-case Jabber Lockup Protection condition specified in 9.6.5.

When both the Jabber function and the Low Light Level Detection function (see 9.9.2.5) have been activated, the Jabber function shall override the Low Light Level Detection function.

9.9.2.5 Low Light Level Detection function requirements

The FOMAU shall have a low light level detection capability, as defined in Figure 9–10, whereby it shall interrupt the reception of both the optical idle signal and packets from the FOMAU's receive optical fiber when reliable reception can no longer be assured. This error condition shall not be activated if the peak optical power level at the output of the FOMAU's receive optical fiber exceeds –27 dBm. It shall be activated before the peak optical power level at the output of the FOMAU's receive optical fiber has fallen to a level that is lower than the peak optical power level that corresponds to a BER = 10^{-10} for the FOMAU under consideration. Once this error condition has been activated, the FOMAU shall, no earlier than 30 bit times and no later than 200 bit times

a) Disable its Receive function so that the transmission of bits from its receive optical fiber to the DI circuit is inhibited.
b) Assure that only the optical idle signal is transmitted into its transmit optical fiber, irrespective of the state of the DO circuit.
c) Disable its Transmit function during the period of time that the FOMAU recognizes the presence of a packet on the DO circuit such that the transmission of the packet from the DO circuit into the DI circuit is inhibited.

Once this error condition has been cleared, the FOMAU shall return automatically to its normal mode of operation within 40 bit times once the DO circuit is in the idle state.

When both the Jabber function (see 9.9.2.4) and the Low Light Level Detection function have been activated, the Jabber function shall override the Low Light Level Detection function.

NOTE—It is recommended that, for diagnostic purposes, the status of the Low Light Level Detection function be indicated on the exterior of the FOMAU package.

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9.9.2.6 Repeater Unit to FOMAU physical layer messages

The following messages can be received by the FOMAU physical layer entities from the repeater unit:

Message	Circuit	Signal	Meaning
output	DO	CD1, CD0	Output information
output_idle	DO	IDL	No data to be output

9.9.2.7 FOMAU physical layer to repeater unit messages

The following messages can be sent by the FOMAU physical layer entities to the repeater unit:

Message	Circuit	Signal	Meaning
input	**DI**	**CD1, CD0**	**Input information**
input_idle	DI	IDL	No information to be input
fomau_available	CI	IDL	FOMAU is available for output
signal_quality_error	CI	CS0	Collision or error detected by FOMAU

9.9.2.7.1 *input* message

The FOMAU physical layer sends an *input* message to the repeater unit when the FOMAU has a bit of data to send to the repeater unit. The physical realization of the *input* message is a CD0 or CD1 sent by the FOMAU to the repeater unit on the DI circuit. The FOMAU sends CD0 if the input bit is a zero, or CD1 if the input bit is a one. No retiming of the CD1 or CD0 signals takes place within the FOMAU.

9.9.2.7.2 *input_idle* message

The FOMAU physical layer sends an *input_idle* message to the repeater unit when the FOMAU does not have data to send to the repeater unit. The physical realization of the *input_idle* message is the IDL signal sent by the FOMAU to the repeater unit on the DI circuit.

9.9.2.7.3 *fomau_available* message

The FOMAU physical layer sends the *fomau_available* message to the repeater unit when the FOMAU is available for output, and when the FOMAU has activated the Low Light Level Detection function in accordance with the Low Light Level Detection function requirements of 9.9.2.5 and Figure 9–10. The *fomau_available* message shall be sent by a FOMAU that is prepared to output data. The physical realization of the *fomau_available* message is an IDL signal sent by the FOMAU to the repeater unit on the CI circuit.

9.9.2.7.4 *signal_quality_error* message

The *signal_quality_error* message shall be implemented in the following fashion:

a) When the FOMAU has completed the transmission of a packet into its transmit optical fiber, it shall not send any *signal_quality_error* message Test sequence.
b) The simultaneous appearance of packets at both the input of a FOMAU's transmit optical fiber and the output of its receive optical fiber shall cause the *signal_quality_error* message to be sent by the FOMAU to the repeater unit.

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c) When the FOMAU has activated the Jabber function, it shall send the *signal_quality_error* message in accordance with the Jabber function requirements of 9.9.2.4 and Figure 9–9.

The physical realization of the *signal_quality_error* message is the CS0 signal sent by the FOMAU to the repeater unit on the CI circuit.

The FOMAU is required to assert the *signal_quality_error* message at the appropriate times whenever the FOMAU is powered and not just when the repeater unit is providing output data.

9.9.2.8 FOMAU state diagrams

The state diagrams, Figures 9–8, 9–9, and 9–10, depict the full set of allowed FOMAU state functions relative to the control circuits of the repeater unit/FOMAU interface for FOMAUs. Messages used in these state diagrams are explained as follows:

NOTE—Figures 9–8, 9–9, and 9–10 must all be considered together.

a) *enable_opt_driver* : Activates the path employed during normal operation to cause the FOMAU transmitter to impress the packet data received from the DO circuit into the FOMAU's transmit optical fiber.

b) *disable_opt_driver* : Deactivates the path employed during normal operation to cause the FOMAU transmitter to impress the packet data received from the DO circuit into the FOMAU's transmit optical fiber.

c) *enable_opt_idle_driver* : Causes the FOMAU transmitter to impress the optical idle signal into the FOMAU's transmit optical fiber.

d) *disable_opt_idle_driver* : Causes the FOMAU to stop transmitting the optical idle signal into the FOMAU's transmit optical fiber.

e) *enable_loop_back* : Activates the path employed during normal operation to cause the FOMAU Transmit function to impress the packet data received from the DO circuit into the DI circuit.

f) *disable_loop_back* : Deactivates the path employed during normal operation to cause the FOMAU Transmit function to impress the packet data received from the DO circuit into the DI circuit.

g) *enable_opt_receiver* : Activates the path employed during normal operation to cause the FOMAU to impress the packet data received from the FOMAU's receive optical fiber into the DI circuit.

h) *disable_opt_receiver* : Deactivates the path employed during normal operation to cause the FOMAU to impress the packet data received from the FOMAU's receive optical fiber into the DI circuit.

i) [*start_packet_timer*] : Starts a timing function which is used to monitor the amount of time the FOMAU is transmitting a packet into the transmit optical fiber. The timing function is maintained as long as *output* is true and is stopped on the transition to *output_idle true*. The term *packet_timer_done* is satisfied when the timing function has run to expiration (see 9.9.2.4).

j) [*start_unjab_timer*] : Starts a timing function that is used to monitor the amount of time that the Jabber error condition has been clear. The timing function is maintained as long as *output_idle* is true and is stopped on the transition to *output true*. The term *unjab_timer_done* is satisfied when the timing function has run to expiration (see 9.9.2.4).

k) *opt_input* : Signifies that a packet is present at the FOMAU's receive optical fiber.

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l) *opt_input_idle* : Signifies that a packet is no longer present at the FOMAU's receive optical fiber.

m) *opt_input_coll_select* : Signifies that, during a collision, a packet has been received at the DO circuit within 3.5 bit times of a packet being received at the FOMAU's receive optical fiber, and that only the packet received at the FOMAU's receive optical fiber is to be transmitted into the DI circuit.

n) *output_coll_select* : Signifies that, during a collision, a packet has been received at the DO circuit within 3.5 bit times of the packet being received at the FOMAU's receive optical fiber, and that only the packet received at the DO circuit is to be transmitted into the DI circuit.

The following abbreviations have been used in Figures 9–8, 9–9, and 9–10:

— LLP = Low Light Level Condition Present
— LLNP = Low Light Level Condition Not Present
— p_t_d = *packet_timer_done*
— p_t_n_d = *packet_timer_not_done*
— * = logical AND operator

9.9.3 FOMAU electrical characteristics

9.9.3.1 Electrical isolation

Electrical isolation shall be provided between FOMAUs attached to the FOIRL by the optical fiber cable link segment. There shall be no conducting path between the optical medium connector plug and any conducting element within the optical fiber cable link segment. This isolation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50–60 Hz for 60 s, applied as specified in 5.3.2 of IEC 60950: 1991.
b) 2250 V dc for 60 s, applied as specified in 5.3.2 of IEC 60950: 1991.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time of half value), as defined IEC 60060.

There shall be no isolation breakdown, as defined in 5.3.2 of IEC 60950: 1991, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 V dc.

NOTE—Although isolation is provided by the optical fiber cable link segment, it is recommended that the normal noise immunity provided by common-mode isolation on the AUI be retained.

9.9.3.2 Power consumption

The current drawn by the FOMAU shall not exceed 0.5 A when powered by the AUI source. The FOMAU shall be capable of operating from all possible voltage sources as supplied by the repeater unit (7.5.2.5 and 7.5.2.6) through the resistance of all permissible AUI cables. The surge current drawn by the FOMAU on power-up shall not exceed 5 A peak for a period of 10 ms. In addition, the FOMAU shall be capable of powering-up from 0.5 A current limited sources.

It is permissible as an option to provide a separate power source for the FOMAU. If a separate power source is implemented, provision will be made to assure that power shall under no circumstances be sourced on pin 13 (Circuit VP) of the AUI.

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The FOMAU shall be labeled externally to identify the maximum value of power supply current required by the device when the AUI mechanical connection is implemented.

The FOMAU shall not introduce into the FOMAU's transmit optical fiber or onto the DI or CI circuits of the AUI any extraneous signal on routine power-up or power-down under normal operating conditions.

The FOMAU shall be fully functional no later than 0.5 s after power is applied to it.

9.9.3.3 Reliability

The FOMAU shall be designed to provide a MTBF of at least 200 000 hours of operation without causing a communication failure amongst DTEs attached to the network. The FOMAU electronics shall be designed to minimize the probability of component failures within the FOMAU that prevent communication amongst other MAUs on the 10BASE5 and 10BASE2 segments. Connectors and other passive means of connection shall be designed to minimize the probability of total network failure.

9.9.3.4 FOMAU/Repeater unit electrical characteristics

The electrical characteristics of the driver and receiver components connected to the AUI cable shall be identical to those specified in Clause 7.

9.9.3.5 FOMAU/Repeater unit mechanical connection

The FOMAU, if it implements the AUI mechanical connection, shall be provided with a 15-pin male connector, as specified in the AUI specification of Clause 7.

9.9.4 FOMAU/Optical medium interface

9.9.4.1 Transmit optical parameters

9.9.4.1.1 Wavelength

The center wavelength of the optical source emission shall be between 790 and 860 nm. See 15.2.1.1.

9.9.4.1.2 Spectral width

The spectral width of the optical source shall be less than 75 nm full width half maximum (FWHM).

9.9.4.1.3 Optical modulation

The optical modulation during packet transmission shall be on-off keying of the optical source power. The minimum extinction ratio shall be 13 dB.

9.9.4.1.4 Optical idle signal

During the idle state of the DO circuit, the Transmit function shall input into the FOMAU's transmit optical fiber an optical idle signal. This signal shall consist of a periodic pulse waveform of frequency 1 MHz +25% –15% with a duty cycle ratio between 45/55 and 55/45.

9.9.4.1.5 Transmit optical logic polarity

The higher optical power level transmitted into the FOMAU's transmit optical fiber shall correspond to the low (LO) logic state (see 7.4.2.1) of the AUI DO circuit.

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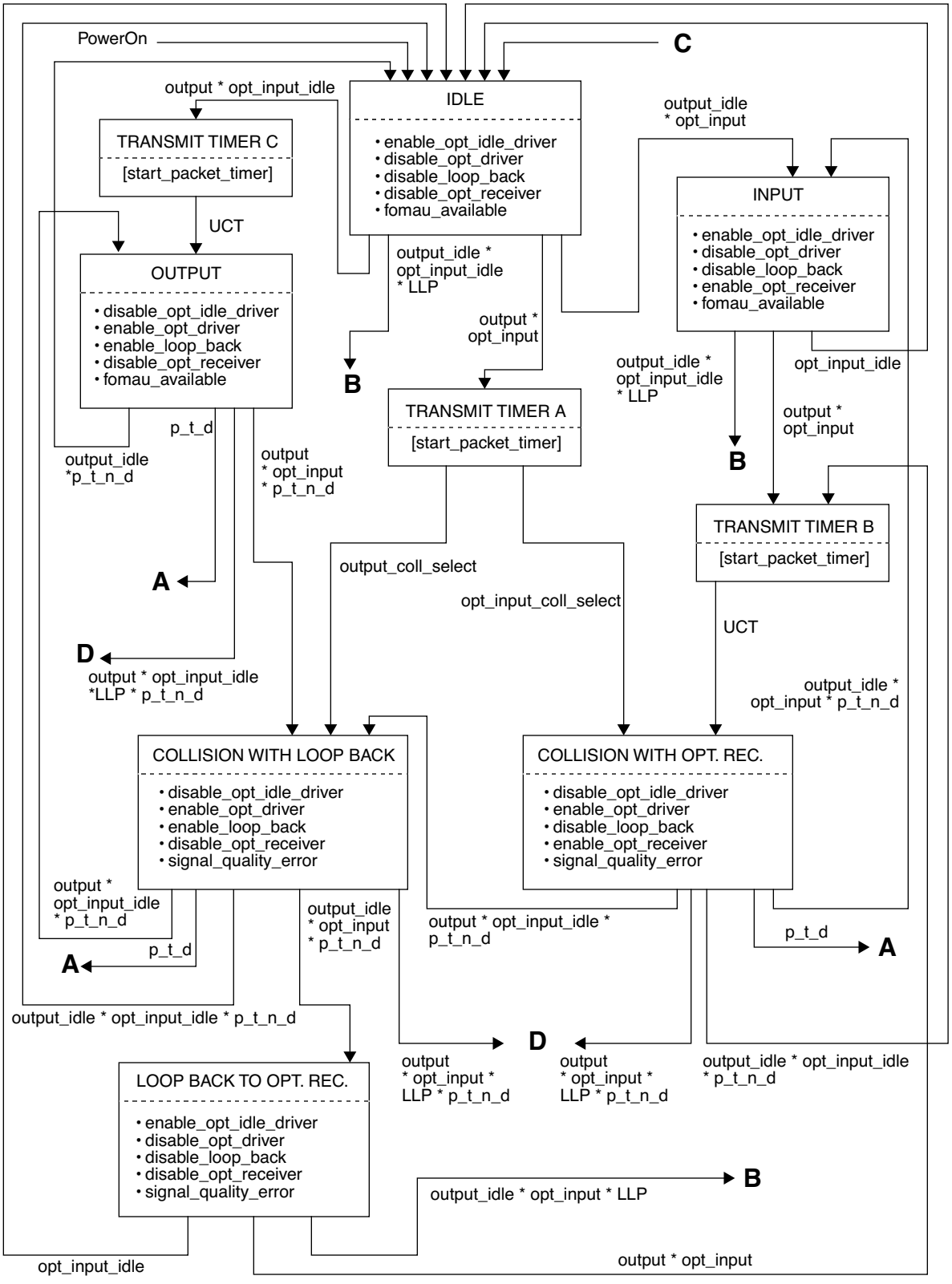


Figure 9–8—FOMAU Transmit, Receive, and Collision functions state diagram

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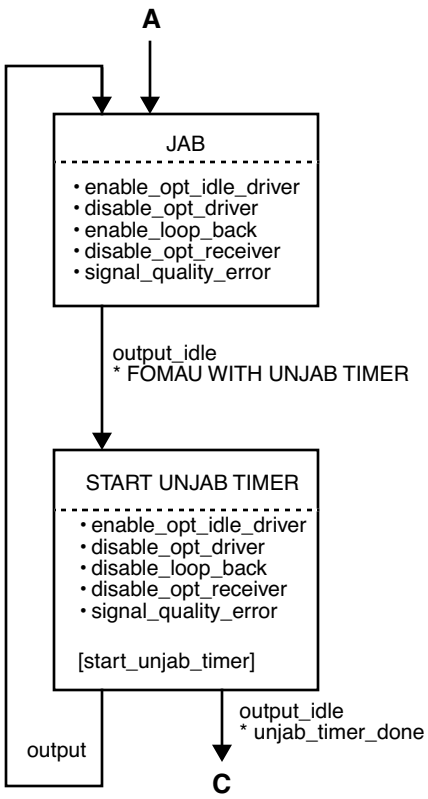


Figure 9–9—
FOMAU Jabber function state diagram

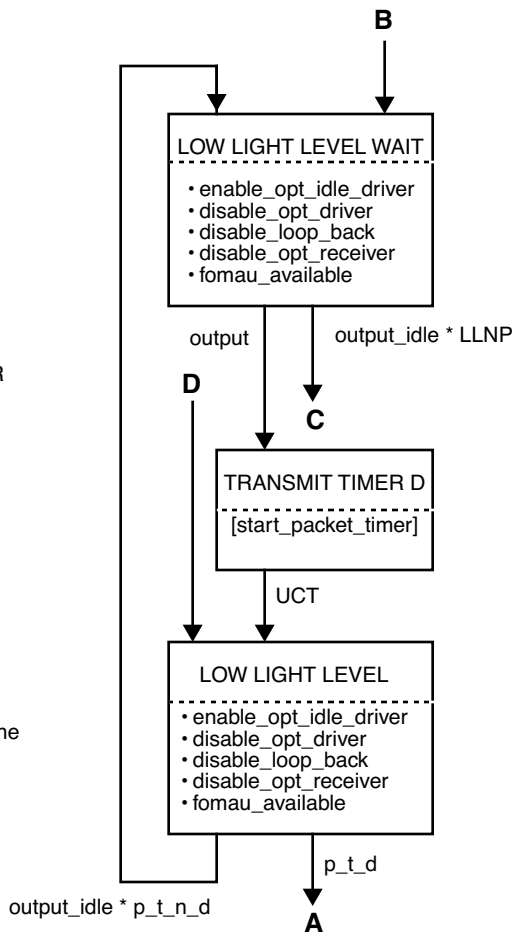


Figure 9–10—
Low Light Level Detection function state diagram

9.9.4.1.6 Optical rise and fall times

The optical rise and fall times of the FOMAU shall be no more than 10 ns from the 10% to the 90% levels. There shall be no more than 3 ns difference between the rise and fall times.

9.9.4.1.7 Transmit optical pulse edge jitter

The additional edge jitter introduced by the FOMAU from the input of the DO circuit receiver to the output of the electro-optic source shall be no more than 2 ns. The jitter measured at the input of the DO circuit receiver shall be measured at the zero crossing points, as determined from the previous 16 or more transitions in any valid bit stream. The jitter measured at the output of the electro-optic source shall be measured at the power level median of the optical waveform's upper and lower power levels, as determined from the previous 16 or more transitions in any valid optical bit stream.

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9.9.4.1.8 Peak coupled optical power

At the beginning of the FOMAU's lifetime, the peak optical power coupled into the FOMAU's transmit optical fiber, when terminated with an optical connector as specified in 9.9.5.2, shall be –12 dBm ± 2 dB, when measured with a graded index optical fiber of nominal dimension of 62.5 μm core diameter and 0.275 nominal numerical aperture. The actual optical power, which will be coupled into other fiber sizes listed in 9.9.5.1, may differ from the above value. The peak optical power shall be measured in the steady state, and the measurement shall be independent of optical pulse ringing effects. Peak optical overshoot shall not exceed 10%.

NOTE 1—The source is allocated an aging margin of 3 dB over its operating lifetime. Thus, with respect to an optical fiber of nominal dimension of 62.5 μm core diameter and 0.275 nominal numerical aperture, the minimum launch peak power at the end of life is –17 dBm and the maximum initial launch peak power is –10 dBm. The variation in the peak coupled optical power into any of the optical fibers specified in 9.9.5.1 is ±1 dB with respect to the above-mentioned nominal optical fiber. Hence, with respect to any of the optical fibers specified in 9.9.5.1, the minimum possible launch peak power at the end of life is –18 dBm and the maximum possible initial launch peak power is –9 dBm. The start of life minimum possible launch peak power is then –15 dBm.

NOTE 2—The transmit optical power range specified above is the power coupled into the core of the optical fiber. Typical current fibers require 1 m to 5 m to remove optical power from the cladding. For links under 5 m in length, it may be necessary to use techniques such as attenuators or mode-stripping filters to attenuate optical power coupled into the cladding in order to meet the requirements of 9.9.4.2.1.

9.9.4.2 Receive optical parameters

9.9.4.2.1 Receive peak optical power range

The BER shall be $< 10^{-10}$ for peak optical powers at the output of the FOMAU's receive optical fiber between –27 dBm and –9 dBm.

9.9.4.2.2 Receive optical pulse edge jitter

The additional edge jitter introduced by the FOMAU from the input of the opto-electric detector to the output of the DI circuit driver shall be no more than 4 ns. The jitter measured at the input of the opto-electric receiver shall be measured at the power level median of the optical waveform's upper and lower power levels as determined from the previous 16 or more transitions in any valid optical bit stream. The jitter measured at the output of the DI circuit driver shall be measured at the zero crossing points as determined from the previous 16 or more transitions in any valid bit stream. This requirement shall apply when the optical receive peak power level is in the range –27 to –9 dBm.

9.9.4.2.3 Receive optical logic polarity

The low (LO) logic state (see 7.4.2.1) on the DI circuit shall correspond to the presence of the higher optical power level at the output of the FOMAU's receive optical fiber.

9.9.5 Characteristics of the optical fiber cable link segment

The optical fiber cable link segment is a length of optical fiber cable (IEC 60794-1: 1993 and IEC 60794-2: 1989) containing two optical fibers, as specified in 9.9.5.1, and comprising one or more optical fiber cable sections and their means of interconnection. Each optical fiber is terminated at each end in the optical connector plug specified in 9.9.5.2. The two optical fibers correspond to the FOMAU's transmit and receive optical fibers.

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9.9.5.1 Optical fiber medium

The FOMAU can operate with a variety of optical fiber sizes, e.g., 50/125 μm, 62.5/125 μm, 85/125 μm, 100/140 μm.

Interoperability of FOMAUs that originate from different manufacturers, using any of these fiber sizes, is assured provided that the received peak optical power is between –27 dBm and –9 dBm and the optical fiber cable link segment bandwidth is greater than or equal to 150 MHz.

In order to satisfy the above attenuation and bandwidth criteria for all allowable FOIRL lengths, and assuming up to 4 dB of connection losses within the optical fiber cable link segment, it is recommended that the cabled optical fiber have an attenuation ≤ 4 dB/km and a bandwidth of ≥ 150 MHz referred to 1 km at a wavelength of 850 nm.

The total incremental optical pulse edge jitter introduced by the optical fiber cable link segment shall be less than 1 ns when driven by an optical transmitter as specified in 9.9.4.1. The pulse delay introduced by the optical fiber cable shall not exceed 50 bit times for a 1 km length.

In the specific case of 62.5/125 μm fiber, to ensure interoperability of FOMAUs that originate from different manufacturers:

a) The two cabled optical fibers contained in the optical fiber cable link segment shall satisfy the optical fiber parameters specified in IEC 60793-2: 1992 type A1b (62.5/125 μm), and
b) The optical fiber cable link segment shall have an attenuation less than or equal to 8 dB and a bandwidth greater than or equal to 150 MHz.

NOTE—For newer fiber installations, it is recommended that the requirements of 15.3 be used.

9.9.5.2 Optical medium connector plug and socket

The two optical fibers contained in the optical fiber cable link segment shall be terminated at each end in an optical connector plug as specified in IEC 60874-1: 1993 and 60874-2: 1993.

The corresponding mating connector socket shall conform with the specifications given in IEC 60874-1: 1993 and 60874-2: 1993. This document specifies the mechanical mating face dimensions to ensure mechanical intermateability without physical damage, of all F-SMA connectors covered by the document. In addition, the optical insertion loss when interconnecting two optical connector plugs shall not exceed 2.5 dB (measured using a socket adaptor conforming to the mechanical specifications given in IEC 60874-1: 1993 and 60874-2: 1993 and also using two identical fibers, as specified in 9.9.5.1, assuming uniform mode distribution launch conditions).

9.9.6 System requirements

9.9.6.1 Optical transmission system considerations

Subclause 9.9.4.2.1 specifies that the BER shall be $<10^{-10}$ for peak optical powers at the output of the FOMAU's receive optical fiber between –27 dBm and –9 dBm. The value of –9 dBm corresponds to the maximum allowable peak optical power that can be coupled into the worst-case optical fiber specified in 9.9.5.1 at the beginning of the FOMAU's lifetime (see 9.9.4.1.8), and assumes zero optical loss between the optical source output and the optical detector input.

The value of –27 dBm is calculated by subtracting the FOIRL flux budget from the minimum allowable peak optical power that can be coupled into the FOMAU's transmit optical fiber at the beginning of the FOMAU's lifetime (see 9.9.4.1.8). The flux budget is the maximum loss allowed within the FOIRL to guarantee a BER

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$< 10^{-10}$ assuming worst-case link components. A portion of the flux budget has been allocated as a design margin to allow for degradation and tolerance effects in the optical source. This is noted in the table below as the optical source lifetime degradation. The remaining flux budget of 9 dB assumes a system margin allowance for the optical fiber cable link segment over its lifetime, and may be allocated to the optical fiber cable link segment loss at the discretion of the network planner/installer. The following summarizes the allocated optical flux budgets for the example graded index optical fiber of worst-case dimensions 62.5 μm – 3 μm (i.e., 59.5 μm) core diameter and 0.275 – 0.015 (i.e., 0.260) numerical aperture:

Start of life minimum peak coupled optical power (9.9.4.1.8)	:–15 dBm
Optical source lifetime degradation	: 3 dB
Maximum optical fiber cable link segment loss including system margin allowance	: 9 dB
Resultant required receive peak optical power	: –27 dBm

9.9.6.2 Timing considerations

Table 9–4 summarizes the maximum allowable timing budget contributions to the system timing budget for the FOIRL. The last bit in to last bit out delay shall equal the Steady-State Propagation Delay.

Table 9–4—Maximum allowable timing budget contributions to the FOIRL system timing budget

Symbol	Function	Bit Loss (bit times)	Invalid Bits (bit times)	Steady-State Propagation Delay (bit times)	Start-Up Delay (bit times)
I1	OPTICAL DATA IN ASSERT→INPUT	2.0	1.0	0.5	3.5
I2	OUTPUT→OPTICAL DATA OUT ASSERT	2.0	1.0	0.5	3.5
LOOP BACK	DO CIRCUIT ASSERT →DI CIRCUIT ASSERT	5.0	1.0	1.0	7.0
I3	OPTICAL COLLISION →SQE ASSERT	—	—	—	3.5
I4	COLLISION DE-ASSERT →SQE DE-ASSERT	—	—	—	7.0[a]
A1	AUI propagation	—	—	2.57	2.57
F1	Optical fiber propagation per kilometer	—	—	50	50

[a]Minimum start-up delay for I4 is 4.5 bit times.

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9.9.7 Environmental specifications

9.9.7.1 Safety requirements

9.9.7.1.1 Electrical safety

A major application for the vendor-independent FOIRL is interconnecting electrically conductive cable segments located within different buildings. The level of isolation provided by the optical fiber cable link segment shall be consistent with this application and provide adequate personnel and equipment safety from earth faults and lightning strike hazards.

9.9.7.1.2 Optical source safety

The recommendations of IEC 60825: 1993, if applicable, shall be adhered to in determining the optical source safety and user warning requirements.

9.9.7.2 Electromagnetic environment

9.9.7.2.1 Susceptibility levels

Sources of interference from the environment include electromagnetic fields, electrostatic discharge, and transient voltages between earth connections. Several sources of interference contribute to voltage between the optical fiber cable link segment (either a metallic strength member in the cable, a metallic optical connector plug, or the outermost conducting element of the FOMAU for the case of no metallic strength member) and the earth connection of a DTE.

For information on limits and methods of measurements of radio interference characteristics of information technology equipment, see 1.3 in CISPR 22: 1993.

The physical channel hardware shall meet its specifications when operating in both of the following conditions:

a) Ambient plane wave field of 2 V/m from 10 kHz through 30 MHz and 5 V/m from 30 MHz through 1 GHz.

NOTE—These are the levels typically found 1 km from radio broadcast stations.

b) Interference source voltage of 15.8 V peak sine wave of frequency 10 MHz in series with a 50 Ω source resistance applied between the optical fiber cable link segment (either a metallic strength member in the cable, a metallic optical connector plug, or the outermost conducting element of the FOMAU for the case of no metallic strength member) and the earth connection of a DTE.

NOTE—The optical fiber link segment is capable of withstanding higher levels of electromagnetic interference. The above specifications are the minimum requirements for the environment in which the FOMAU is required to operate.

9.9.7.2.2 Emission levels

The FOMAU and optical fiber cable link segment shall comply with CISPR 22: 1993.

9.9.7.3 Temperature and humidity

The FOMAU and associated connector/cable systems are expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling such as shock and vibration. Specific requirements and values for these parameters are beyond the scope of this standard. Manufacturers should indicate in the literature associated with the FOMAU (and on the FOMAU if possible) the operating environment specifications to facilitate selection, installation, and maintenance of these components. It is further recommended that such specifications be stated in standard terms, as specified in IEC 60068, IEC 60793-1: 1992, IEC 60794-1: 1993, and IEC 60874-1: 1993.

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10. Medium attachment unit and baseband medium specifications, type 10BASE2

10.1 Scope

10.1.1 Overview

This standard defines the functional, electrical, and mechanical characteristics of the Medium Attachment Unit (MAU) and one specific medium for use with LANs. The relationship of this specification to the entire ISO/IEC 8802-3 CSMA/CD LAN International Standard is shown in Figure 10–1.

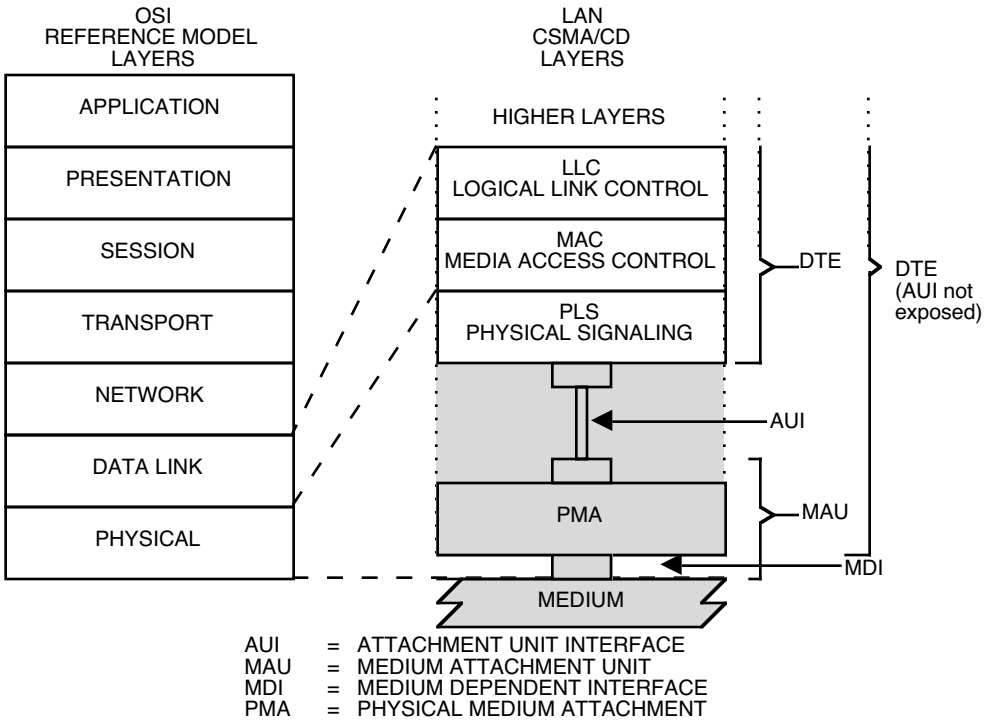


Figure 10–1—Physical Layer partitioning, relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

The purpose of the MAU is to provide a simple, inexpensive, and flexible means of attaching devices to the LAN medium. This standard defines a means of incorporating the MAU function within the DTE and bringing the trunk coaxial cable directly to the DTE. Interconnection of DTE units is easily achieved by the use of industry standard coaxial cables and BNC connectors.

This MAU and medium specification is aimed primarily at applications where there are a relatively small number of devices located in a work area. Installation and reconfiguration simplicity is achieved by the type of cable and connectors used. An inexpensive implementation is achieved by eliminating the MAU and Attachment Unit Interface (AUI) as separate components and using widely available interconnection components.

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10.1.1.1 Medium attachment unit (normally contained within the data terminal equipment [DTE])

The MAU has the following general characteristics:

a) Enables coupling the PLS to the explicit baseband coaxial transmission system defined in this clause of the standard.
b) Supports message traffic at a data rate of 10 megabits per second (Mb/s).
c) Provides for driving up to 185 m coaxial trunk cable segment without a repeater.
d) Permits the DTE to test the MAU and the medium itself.
e) Supports system configurations using the CSMA/CD access mechanism defined in IEEE 802.3.
f) Supports a bus topology interconnection means.
g) Supports low-cost capability by incorporating the MAU function within the physical bounds of the DTE, thereby eliminating the need for a separate AU connector and cable but containing the remaining AU interface functionality.

10.1.1.2 Repeater unit

The Repeater Unit is used to extend the physical system topology and provides for coupling two or more coaxial trunk cable segments. Multiple Repeater Units are permitted within a single system to provide the maximum trunk cable connection path specified in 10.7. The repeater is not a DTE and therefore has slightly different attachment requirements.

10.1.2 Definitions

See 1.4.

10.1.3 Application perspective: MAU and medium objectives

This subclause states the broad objectives and assumptions underlying the specifications defined throughout Clause 10 of the standard.

10.1.3.1 Object

a) Provide the physical means for communication between local network Data Link entities.

NOTE—This specification covers a portion of the Physical Layer as defined in the OSI Reference Model and, in addition, the physical medium itself, which is beyond the scope of the OSI Reference Model.

b) Define a physical interface that can be implemented independently among different manufacturers of hardware and achieves the intended level of compatibility when interconnected in a common local network.
c) Provide a communication channel capable of high bandwidth and low bit error rate performance. The resultant mean bit error rate, at the Physical Layer service interface, should be less than one part in 10^7 (on the order of one part in 10^8 at the link level).
d) Provide for ease of installation and service.
e) Provide for high network availability (ability of a station to gain access to the medium and enable the Data Link connection in a timely fashion).
f) Enable low-cost implementations.

NOTE—The figures and numerous textual references throughout this clause refer to terminology associated with the AUI (that is, DO, DI, CI). Since the normal embodiment of the type 10BASE2 configuration does not require an AUI, actual existence of the DO, DI, CI circuit may not be required. Use of this terminology, however, is retained throughout Clause 10 for purposes of clarity and consistency.

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10.1.3.2 Compatibility considerations

All implementations of this baseband coaxial system shall be compatible at the Medium Dependent Interface (MDI).

This standard provides one explicit trunk cable medium specification for the interconnection of all MAU devices. The medium itself, and the functional capability of the MAU, are defined to provide the highest possible level of compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the MAU in an application-dependent manner provided the MDI specifications are satisfied.

10.1.3.3 Relationship to PLS and AUI

This clause defines the Primary Physical Layer for the LAN, a layer comprised of both the physical medium and the rudimentary circuitry necessary to couple a station's message path directly to/from the medium. The complete Logical Physical Layer of the LAN resides within the DTE. Therefore, a close relationship exists between this subclause and Clause 7. This subclause specifies the physical medium parameters, the PMA logical functions residing in the MAU, and references the signal circuits associated with the AUI as defined in Clause 7.

The design of a MAU component requires the use of both this clause and parts of the PLS and AUI specifications contained in Clause 7.

10.1.3.4 Mode of operation

The MAU functions as a direct connection between the baseband medium and the DTE. Data from the DTE is output to the coaxial trunk medium and all data on the coaxial trunk medium is input to the DTE.

10.2 References

References to such local or national standards that may be useful resource material for the reader are identified and located in Annex A.

10.3 MAU functional specifications

The MAU component provides the means by which signals on the three AUI signal circuits to/from the DTE and their associated interlayer messages are coupled to the single coaxial cable baseband signal line. To achieve this basic objective, the MAU component contains the following functional capabilities to handle message flow between the DTE and the baseband medium:

a) *Transmit function*. The ability to transmit serial data bit streams on the baseband medium from the local DTE entity to one or more remote DTE entities on the same network.
b) *Receive function*. The ability to receive serial data bit streams over the baseband medium.
c) *Collision Presence function*. The ability to detect the presence of two or more stations' concurrent transmissions.
d) *Jabber function*. The ability to automatically interrupt the Transmit function and inhibit an abnormally long output data stream.

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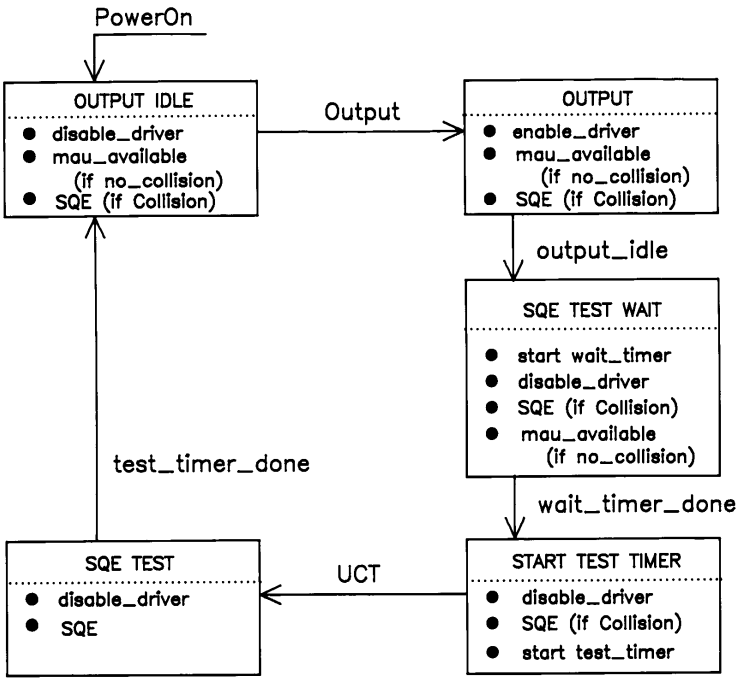
10.3.1 MAU Physical Layer functional requirements

10.3.1.1 Transmit function requirements

At the start of a frame transmission on the coaxial cable, no more than 2 bits (2 full bit cells) of information may be received from the DO circuit and not transmitted onto the coaxial medium. In addition, it is permissible for the first bit sent to contain invalid data or timing; however, all successive bits of the frame shall be reproduced with no more than the specified amount of jitter. The 4th bit cell shall be carried from the DO signal line and transmitted onto the coaxial trunk cable medium with the correct timing and signal levels. The steady-state propagation delay between the DO circuit receiver input and the coaxial cable output shall not exceed 1/2 bit cell. There shall be no logical signal inversions between the branch cable DO circuit and the coaxial trunk cable (for example, a "high" logic level input to the MAU shall result in the less negative current flow value on the trunk coaxial medium). A positive signal on the A signal lead of the DO circuit shall result in a more positive voltage level on the trunk coaxial medium. It is assumed that the AUI shall provide adequate protection against noise. It is recommended that the designer provide an implementation in which a minimum threshold signal is required to establish a transmit bit stream.

The Transmit function shall output a signal on the trunk coaxial medium whose levels and waveform comply with 10.4.1.3.

In addition, when the DO circuit has gone idle after a frame is output, the MAU shall then activate the Collision Presence Function as close to the trunk coaxial cable as possible without introducing an extraneous signal on the trunk coaxial medium. The MAU shall initiate the Collision Presence state within 0.6 μs to 1.6 μs after the Output Idle signal (Wait_Timer_Done in Figure 10–2) and shall maintain an active Collision Presence state for a time equivalent to 10 ± 5 bit cells.



(UCT = unconditional transition)
(Wait_Timer_Done is specified in 10.3.1.1)

Figure 10–2—MAU Interface function

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10.3.1.2 Receive function requirements

The signal from the coaxial trunk cable shall be ac coupled before reaching the receive DI circuit. The Receive Function shall output a signal onto the DI circuit that complies with the specification for drivers in MAUs (7.5).

At the start of a frame reception from the coaxial cable, no more than 5 bits (5 full bit cells) of information may be received from the coaxial cable and not transmitted onto the receive DI circuit. In addition, it is permissible for the first bit sent over the receive circuit to contain invalid data or timing; however, all successive bits of the frame shall reproduce the incoming signal with no more than the amount of jitter specified below. This implies that the 7th bit cell presents valid data to the PLS. The steady-state propagation delay between the coaxial cable and the receive DI circuit output shall not exceed 1/2 bit cell. There are no logical signal inversions between the coaxial (trunk) cable and the MAU receive circuit.

A MAU meeting this specification shall exhibit edge jitter into the DI pair when terminated in the appropriate test load specified in 7.4.1.1, of no more than 7.0 ns in either direction when it is installed on the distant end of all lengths up to 185 m of the cable specified in 10.5.1.1 through 10.5.2.1.5 terminated at both ends with terminators meeting the impedance requirements of 10.6.2 and driven at one end with pseudorandom Manchester encoded binary data from a data generator that exhibits no more than 1.0 ns of edge jitter in either direction on half bit cells of exactly 1/2 BT and whose output meets the specifications of 10.4.1.3 except that the rise time of the signal shall be 30 ns + 0, – 2 ns. The combination of coaxial cable and MAU receiver introduce no more than 6 ns of edge jitter into the system.

The local Transmit and Receive functions shall operate simultaneously while connected to the medium.

10.3.1.3 Collision Presence function requirements

The signal presented to the CI circuit in the absence of a collision shall be the IDL signal.

The signal presented to the CI circuit during the presence of a collision shall be the CS0 signal encoded as specified in 7.3.1.2. Under no conditions shall the Collision Presence function generate an output when only one MAU is transmitting. Table 10–1 summarizes the allowable conditions under which collisions shall be detected.

a) Collision Assertion
   1) In the case where the MAU has been transmitting for at least 20 bit times, the CS0 signal shall be presented to the CI circuit no more than 17 bit times after the arrival at the MAU on the coaxial cable of a transmission from another MAU. Arrival at the MAU shall be considered to be the time when the transmission of the other MAU causes the dc level on the coaxial cable to become more negative.
   2) In all other cases where the MAU is transmitting, the CS0 signal shall be presented to the CI circuit no more than 29 bit times after the later of start of transmission by the MAU and the arrival of a transmission from another MAU.

b) Collision De-assertion
   1) In the case where a collision has occurred between the MAU and one other MAU, the IDL signal shall be presented to the CI circuit no more than 17 bit times after either the end of transmission by the MAU or the arrival of the end of transmission from the other MAU, whichever occurs earlier. The arrival of the end of transmission from the other MAU shall be the time when the cessation of transmission causes the dc level on the coaxial cable to become less negative.
   2) In the case where a collision has occurred between more than two MAUs, the IDL signal shall be presented to the CI circuit no more than 29 bit times after the arrival of the end of transmission from all but one MAU.

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These timing conditions shall be met for all data bit patterns and combinations of MDI, MAU transmit levels, and MAU locations on the segment.

The Collision Presence function may, in some implementations, be able to sense an abnormal (for example, open) medium.

Table 10–1—Generation of collision presence signal

MAU	Numbers of transmitters		
	<2	=2	>2
Transmitting	N	Y	Y
Not transmitting	N	Y	Y

Y = shall generate SQE message
N = shall not generate SQE message

10.3.1.4 Jabber functional requirements

The MAU shall contain the capability as defined in Figure 10–3 to interrupt a transmission from a DO circuit that exceeds a time duration determined by the MAU. This time duration shall not be less than 20 ms nor more than 150 ms. If the frame being transmitted continues longer than the specified time duration, the MAU shall inhibit transmission and assume its not-transmitting state on the coaxial cable.

When the Transmit function has been positively disabled, the MAU shall then activate the Collision Presence function without introducing an extraneous signal on the trunk coaxial medium. A MAU may reset the Jabber and Collision Presence functions on power reset once the error condition has been cleared. Alternately, a MAU may reset these functions automatically after a period of 0.5 s ± 50%.

10.3.2 MAU interface messages

10.3.2.1 DTE to MAU messages

The following messages can be sent by the DTE Physical Layer (PLS Sublayer) Entities to the MAU Entities:

Message	Circuit	Signal	Meaning
output	DO	CD1, CD0	Output information
output_IDL	DO	IDL	No data to be output

10.3.2.2 MAU to DTE messages

The following messages can be sent by the MAU Physical Layer Entities to the DTE Physical Layer Entities:

Message	Circuit	Signal	Meaning
input	DI	CD1, CD0[a]	Input information
input_idle	DI	IDL	No information to be input
mau_available	CI	IDL	MAU is available for output
SQE	CI	CS0	Error detected by MAU

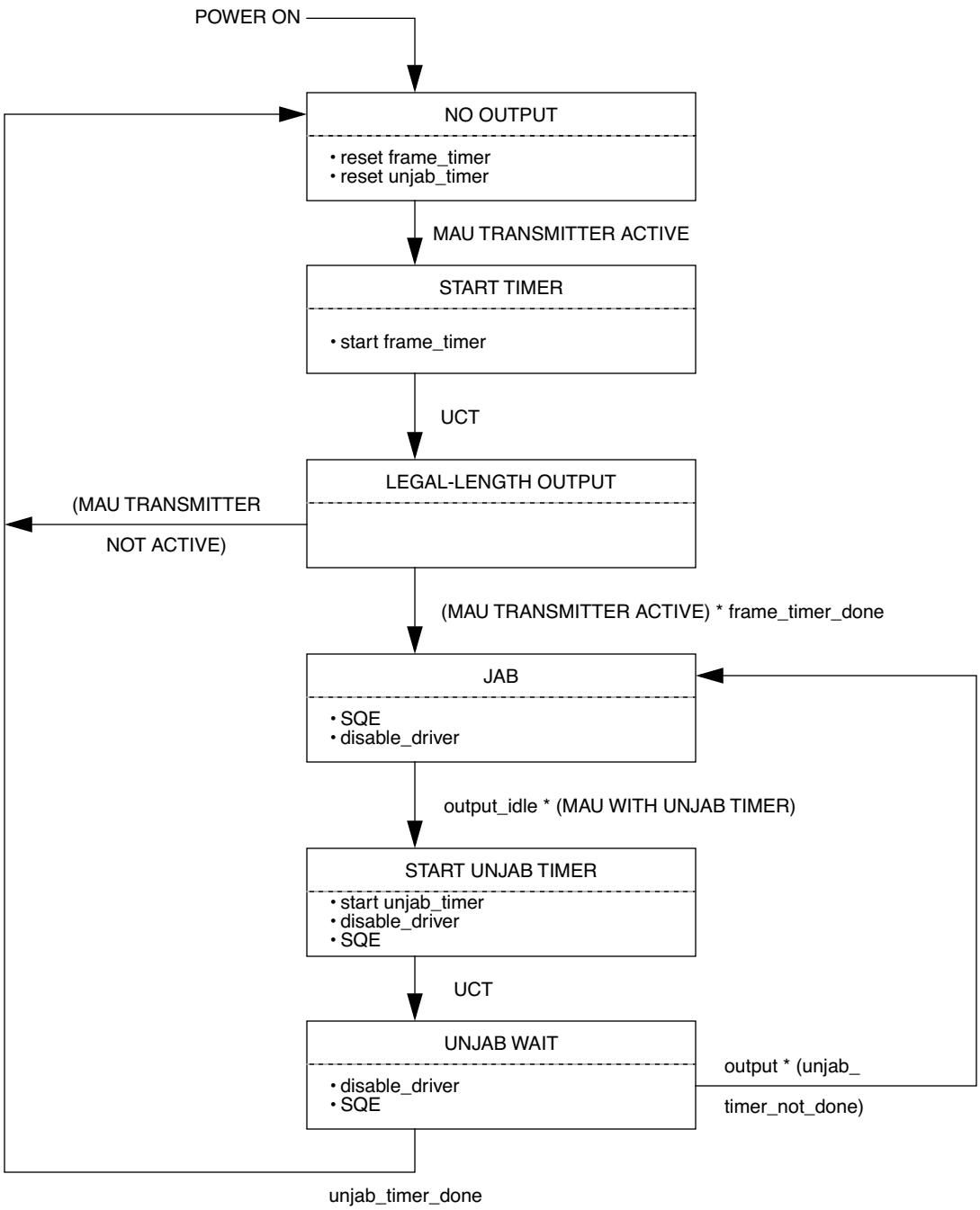
[a]It is assumed that no retiming of these clocked data signals takes place within the MAU.

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(Figure 10–3 outputs override those in Figure 10–2.
Optional states: START UNJAB TIMER, UNJAB WAIT.)

Figure 10–3—Jabber function state diagram

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10.3.2.2.1 *input* message

The MAU sends an input message to the DTE Physical Layer when the MAU has a bit of data to send to the DTE. The physical realization of the input message is a CD0 or CD1 sent by the MAU to the DTE on the Data In circuit. The MAU sends CD0 if the input bit is a zero or CD1 if the input bit is a one. No retiming of the CD1 or CD0 signals takes place within the MAU.

10.3.2.2.2 *input_idle* message

The MAU sends an *input_idle* message to the DTE Physical Layer when the MAU does not have data to send to the DTE. The physical realization of the *input_idle* message is the IDL signal sent by the MAU to the DTE on the Data In circuit.

10.3.2.2.3 *mau_available* message

The MAU sends the *mau_available* message to the DTE Physical Layer when the MAU is available for output. The *mau_available* message is always sent by a MAU that is always prepared to output data unless the SQE message should be sent instead. Such a MAU does not require *mau_request* to prepare itself for data output. The physical realization of the *mau_available* message is an IDL signal sent by the MAU to the DTE on the Control In circuit.

10.3.2.2.4 *signal_quality_error* (SQE) message

The SQE message shall be implemented in the following fashion:

a) The SQE message shall not be sent by the MAU if no or only one MAU is transmitting on the trunk coaxial medium.
b) If two or more remote MAUs are transmitting on the trunk coaxial medium, but the MAU connected to the local DTE is not transmitting, then the local MAU shall send the SQE message.
c) When the local MAU is transmitting on the trunk coaxial medium, all occurrences of one or more additional MAUs transmitting shall cause the SQE to be sent by the local MAU to its DTE.
d) When the MAU has completed each output frame it shall perform an SQE test sequence. Note that MAUs associated with repeaters shall not generate the SQE test sequence.
e) When the MAU has inhibited the Transmit function, it shall send the SQE message in accordance with the Jabber function requirements of 10.3.1.4 and Figure 10–3.

The physical realization of the SQE message is the CS0 signal sent by the MAU to the DTE physical layers on the Control In circuit.

NOTE—The MAU is required to assert the SQE at the appropriate times whenever the MAU is powered and not just when the DTE physical layer is providing data output.

10.3.3 MAU state diagrams

The state diagrams, Figures 10–2 and 10–3, depict the full set of allowed MAU state functions relative to the control circuits of the DTE-MAU interface for MAUs without conditioning requirements. Messages used in these state diagrams are explained as follows:

enable_driver. Activates the path employed during normal operation to cause the MAU transmitter to impress data onto the trunk coaxial medium.

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disable_driver. Deactivates the path employed during normal operation to cause the MAU transmitter to impress data onto the trunk coaxial medium.

no_collision. Signifies that the condition of multiple transmitters simultaneously active on the trunk coaxial medium does not exist.

collision. Signifies that the condition of multiple transmitters simultaneously active on the trunk coaxial medium does exist.

frame_timer. Measures the time the MAU transmits on the trunk coaxial cable.

test_timer. Measures the length of the SQE Test.

unjab_timer. Measures the amount of time the MAU has been in Jab mode.

wait_timer. Measures the time between output idle and the start of the SQE Test.

10.4 MAU–medium electrical characteristics

10.4.1 MAU-to-coaxial cable interface

The following subclauses describe the interface between the MAU and the coaxial cable. Negative current is defined as current into the MAU (out of the center conductor of the cable).

10.4.1.1 Input impedance

The shunt capacitance presented to the coaxial cable by the MAU circuitry (not including the means of attachment to the coaxial cable) is recommended to be not greater than 6 pF. The magnitude of the reflection from a MAU plus the cable connection specified in 10.6.3 shall not be more than that produced by an 8 pF capacitance when measured by both a 25 ns rise time and 25 ns fall time waveform. The resistance presented to the coaxial cable shall be greater than 100 kΩ.

These conditions shall be met in both the power-off and power-on, not-transmitting states.

10.4.1.2 Bias current

The MAU must draw (from the cable) between +2 μA and –25 μA in the power-off and the power-on, not-transmitting states.

10.4.1.3 Coaxial cable signaling levels

The signal on the coaxial cable due to a single MAU as measured at the MAU's transmitter output is composed of an ac component and an offset component. Expressed in terms of current immediately adjacent to the MAU connection (just prior to splitting the current flow in each direction), the signal has an offset component (average dc current including the effects of timing distortion) of from –37 mA min to –45 mA max and an ac component from ± 28 mA up to the offset value.

The current drive limit shall be met even in the presence of one other MAU transmitter. The MAU shall be capable of generating at least 2.2 V of average dc level on the coaxial cable in the presence of two or more other MAUs transmitting concurrently. The MAU shall, in addition, sink no more than ± 250 μA when the voltage on the center conductor of the cable drops to –10 V when the MAU is transmitting.

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The actual current measured at a given point on the cable is a function of the transmitted current and the cable loss to the point of measurement. Negative current is defined as current out of the center conductor of the cable (into the MAU). The 10 – 90% rise/fall times shall be 25 ± 5 ns at 10 Mb/s. The rise and fall times must match within 2 ns. Figure 10–4 shows typical waveforms present on the cable. Harmonic content generated from the 10 MHz fundamental periodic input shall meet the following requirements:

Second and Third Harmonics: At least 20 dB below fundamental
Fourth and Fifth Harmonics: At least 30 dB below fundamental
Sixth and Seventh Harmonics: At least 40 dB below fundamental
All Higher Harmonics: At least 50 dB below fundamental

NOTE—Even harmonics are typically much lower.

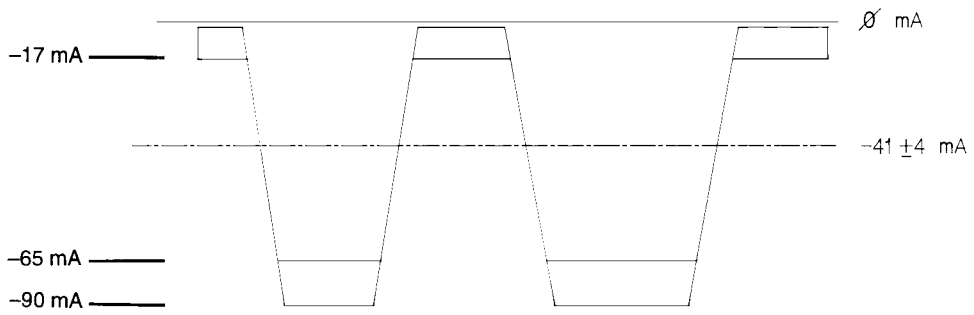
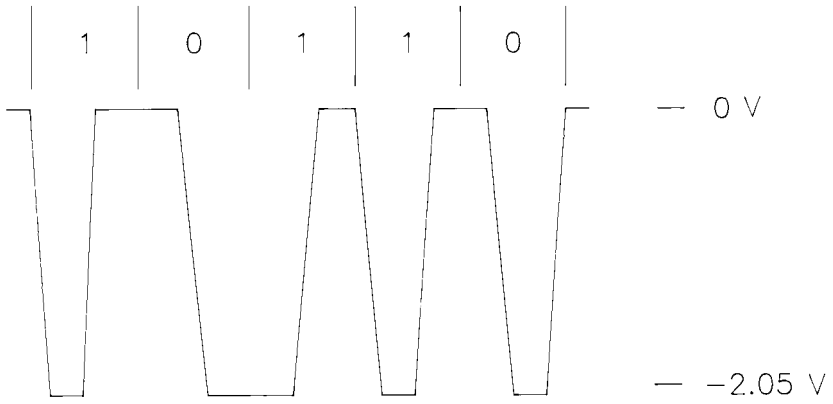


Figure 10–4—Driver current signal levels

The above specifications concerning harmonics cannot be satisfied by a square wave with a single-pole filter, nor can they be satisfied by an output waveform generator employing linear ramps without additional waveshaping. The signals, as generated from the encoder within PLS, shall appear on the coaxial cable without any inversions (see Figure 10–5).



NOTE: (1) Voltages given are nominal, for a single transmitter.
(2) Rise time is 25 ns nominal at 10 Mb/s rate.
(3) Voltages are measured on terminated coaxial cable adjacent to transmitting MAU.
(4) Manchester coding.

Figure 10–5—Coaxial trunk cable signal waveform

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10.4.1.4 Transmit output levels symmetry

Signals received from the DO circuit must be transmitted onto the coaxial cable with the characteristics specified in 10.4.1.3. Since the coaxial cable proceeds in two directions from the MAU, the current into the MAU is nominally twice the current measured on the coaxial cable.

The output signal of a MAU meeting this specification shall exhibit edge jitter of no more than 2.5 ns into a 25 Ω ± 1% resistor substituted for the connection to the coaxial cable when the DO circuit into the MAU is driven with pseudo-random Manchester encoded binary data from a data generator that exhibits no more than 0.5 ns of edge jitter on half bit cells of exactly 1/2 BT, whose output meets the specifications of 7.4.1.1 through 7.4.1.5. The above specified component shall not introduce more than 2 ns of edge jitter into the system.

The MAU shall not transmit a negative going edge after cessation of the CD output data stream or before the first valid edge of the next frame.

10.4.1.5 Collision detect thresholds

For receive mode collision detection the MAU shall have its collision detection threshold set in the range –1404 mV and –1581 mV. These limits take account of up to 8% collision detect filter impulse response. If a specific filter implementation has a higher value of impulse response, the lower threshold limit of –1404 mV is required to be replaced by –1300 mV × [1 + impulse response].

Receive mode collision detection indicates that a nontransmitting MAU has the capability to detect collisions when two or more MAUs are transmitting simultaneously.

All MAUs are required to implement receive mode collision detection.

NOTE—The above threshold limits are measured at the coaxial cable center conductor with respect to the shield at the MAU connector. The MAU designer must take into account circuit offsets, low-frequency noise (for example, 50 Hz, 60 Hz), and 5 MHz ripple at the filter output in determining the actual internal threshold value and its tolerance.

10.4.2 MAU electrical characteristics

10.4.2.1 Electrical isolation

The MAU must provide isolation between the DTE Physical Layer circuits and the coaxial trunk cable. The isolation impedance measured between any conductor in the DTE Physical Layer circuitry and either the center conductor or shield of the coaxial cable shall be greater than 250 kΩ at 50 Hz, 60 Hz. In addition, the isolation impedance between the DTE ground and the coaxial cable shield shall be less than 15 Ω between 3 MHz and 30 MHz. The isolation means provided shall withstand 500 V ac, rms for one minute.

10.4.2.2 Power consumption

The current drawn by the MAU shall not exceed 0.5 A if powered by the AUI source. The MAU shall be capable of operating from all permissible voltage sources as supplied by the DTE through the resistance of all permissible AUI cables. The MAU shall not disrupt the trunk coaxial medium should the DTE power source fall below the minimum operational level under abnormal MAU load conditions.

The MAU shall be labeled externally to identify the maximum value of current required by the device. This requirement only applies to MAUs that are external to DTEs.

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10.4.2.3 Reliability

The MAU shall be designed to provide an MTBF of at least 100 000 hours of continuous operation without causing communication failure among other stations attached to the local network medium. Component failures within the MAU electronics should not impede the communication among other MAUs on the coaxial cable. Connectors and other passive components comprising the means of connecting the MAU to the coaxial cable shall be designed to minimize the probability of total network failure.

It should be noted that a fault condition that causes a MAU to draw in excess of 2 mA from the coaxial cable may cause communication failure among other stations.

10.4.3 MAU–DTE electrical characteristics

If the AUI is exposed, the electrical characteristics for the driver and receiver components connected between the DTE Physical Layer circuitry and the MAU shall be identical with those as specified in Clause 7 of this standard.

10.5 Characteristics of coaxial cable system

The trunk cable is of constant impedance, coaxial construction. It is terminated at each of the two ends by a terminator (see 10.6.2), and provides the transmission path for connection of MAU devices. Coaxial cable connectors are used to make the connection from the cable to the terminators and between cable sections. The cable has various electrical and mechanical requirements that shall be met to ensure proper operation.

10.5.1 Coaxial cable electrical parameters

The parameters specified in 10.5.1 are met by cable types RG 58 A/U or RG 58 C/U.

10.5.1.1 Characteristic impedance

The average characteristic cable impedance shall be 50 ± 2 Ω. Periodic variations in impedance along a single piece of cable may be up to ±3 Ω sinusoidal, centered around the average value, with a period of less than 2 m.

10.5.1.2 Attenuation

The attenuation of a 185 m cable segment shall not exceed 8.5 dB measured at 10 MHz, or 6.0 dB measured at 5 MHz.

10.5.1.3 Velocity of propagation

The minimum required velocity of propagation is 0.65 c.

10.5.1.4 Edge jitter; entire segment without DTEs attached

A coaxial cable segment meeting this specification shall exhibit edge jitter of no more than 8.0 ns in either direction at the receiving end when 185 m of the cable is terminated at both ends with terminators meeting the impedance requirements of 10.6.2 and is driven at one end with pseudorandom Manchester encoded binary data from a data generator that exhibits no more than 1.0 ns of edge jitter in either direction on half bit cells of exactly $^1/_2$ BT and whose output meets the specifications of 10.4.1.3, except that the rise time of the signal must be 30 ns + 0, – 2 ns, and no offset component in the output current is required. This test shall be conducted in a noise-free environment. The above specified component is not to introduce more than 7 ns of edge jitter into the system.

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10.5.1.5 Transfer impedance

The coaxial cable medium shall provide sufficient shielding capability to minimize its susceptibility to external noise and also to minimize the generation of interference by the medium and related signals. While the cable construction is not mandated, it is necessary to indicate a measure of performance expected from the cable component. A cable's EMC performance is determined, to a large extent, by the transfer impedance value of the cable.

The transfer impedance of the cable shall not exceed the values shown in Figure 10–6 as a function of frequency.

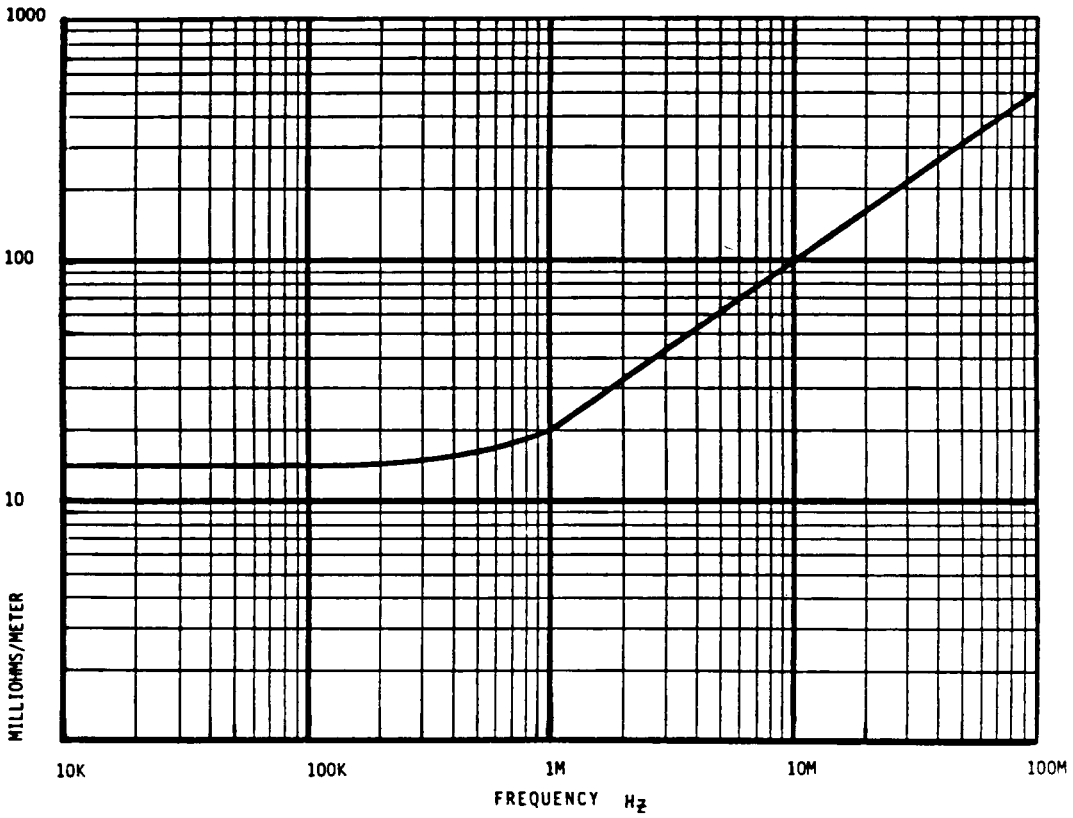


Figure 10–6—Maximum coaxial cable transfer impedance

10.5.1.6 Cable dc loop resistance

The sum of the center conductor resistance plus the shield resistance measured at 20 °C shall not exceed 50 mΩ/m.

10.5.2 Coaxial cable physical parameters

10.5.2.1 Mechanical requirements

The cable used should be suitable for routing in various environments, including but not limited to, dropped ceilings, raised floors, and cable troughs as well as throughout open floor space. The jacket shall provide insulation between the cable sheath and any building structural metal. Also, the cable shall be capable of accepting coaxial cable connectors, described in 10.6. The cable shall conform to the following requirements.

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10.5.2.1.1 General construction

a) The coaxial cable shall consist of a center conductor, dielectric, shield system, and overall insulating jacket.
b) The coaxial cable shall be sufficiently flexible to support a bend radius of 5 cm.

10.5.2.1.2 Center conductor

The center conductor shall be stranded, tinned copper with an overall diameter of 0.89 mm ± 0.05 mm.

10.5.2.1.3 Dielectric material

The dielectric may be of any type, provided that the conditions of 10.5.1.2 and 10.5.1.3 are met; however, a solid dielectric is preferred.

10.5.2.1.4 Shielding system

The shielding system may contain both braid and foil elements sufficient to meet the transfer impedance of 10.5.1.5 and the EMC specifications of 10.8.2.

The inside diameter of the shielding system shall be 2.95 mm ± 0.15 mm.

The shielding system shall be greater than 95% coverage. The use of tinned copper braid is recommended to meet the contact resistance and shielding requirements.

10.5.2.1.5 Overall jacket

a) Any one of several jacket materials shall be used provided the specifications of 10.5.1 and 10.5.2 are met.
b) Either of two jacket dimensions may be used for the two broad classes of materials provided the specification of 10.5.2.1.1 are met:
    1) Polyvinyl chloride (for example, PVC) or equivalent having an OD of 4.9 mm ± 0.3 mm.
    2) Fluoropolymer (for example, FEP, ECTFE) or equivalent having an OD of 4.8 mm ± 0.3 mm.

The cable shall meet applicable flammability and smoke criteria to meet the local and national codes for the installed environment (see 10.8.3).

Different types of cable sections (for example, polyvinyl chloride and fluoropolymer dielectric) may be interconnected, while meeting the sectioning requirements of 10.7.2.1.

10.5.2.2 Jacket marking

It is recommended that the cable jacket be marked with manufacturer and type at a nominal frequency of at least once per meter along the cable.

10.5.3 Total segment dc loop resistance

The sum of the center conductor, connectors, and shield resistance shall not exceed 10 Ω total per segment. Each in-line connector pair or MAU shall contribute no more than 10 mΩ.

As a trunk coaxial cable segment consists of several cable sections, all connectors and internal resistance of the shield and center conductor shall be included in the loop resistance measurement.

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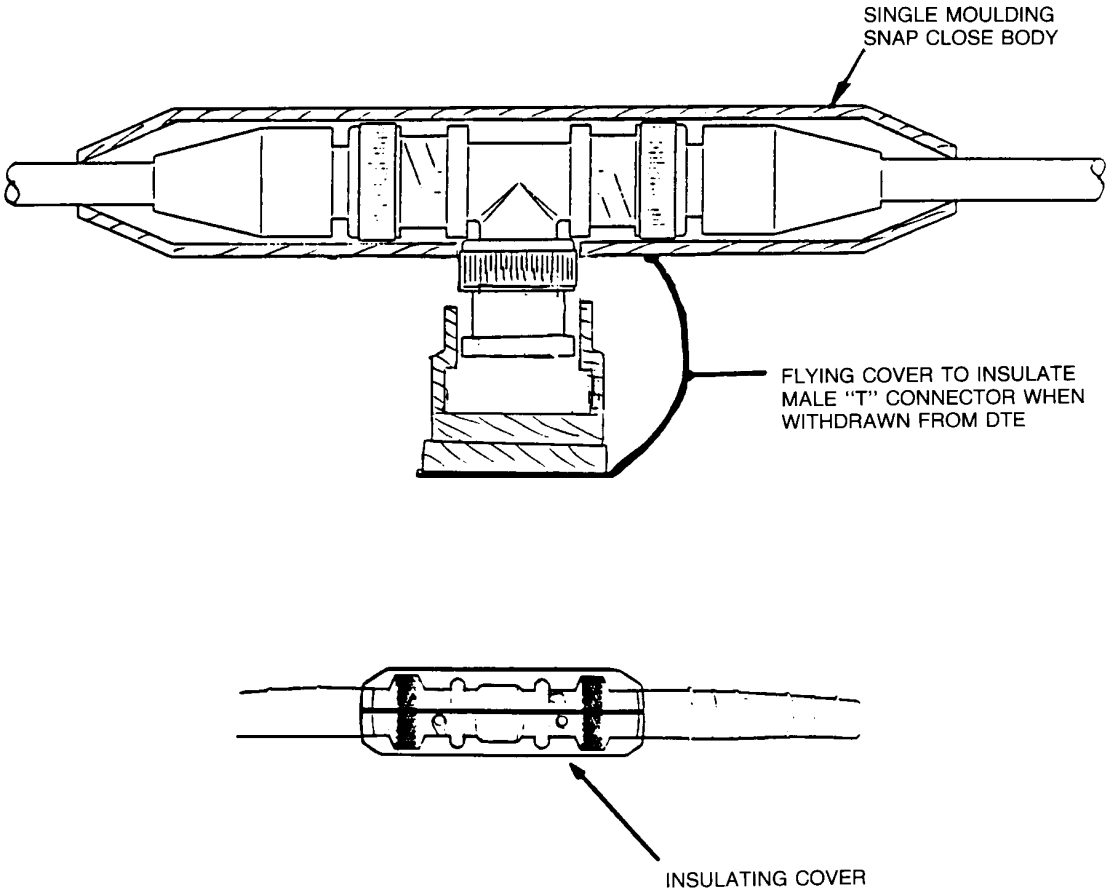
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10.6 Coaxial trunk cable connectors

The trunk coaxial medium requires termination and is partitioned into sections. Devices to be attached to the medium require a means of connection to the medium. This means is provided by a BNC "T" adapter, as shown in Figure 10–7.



(Tutorial only and not part of the standard.)

Figure 10–7—Examples of insulated connector cover

The BNC connectors shall be of the 50 Ω constant impedance type. High-quality versions of these connectors (per IEC 169-8) are recommended in order to meet dc loop resistance and reliability considerations. All of the coaxial connectors shall follow the requirements as defined in 10.6.3.

10.6.1 In-line coaxial extension connector

All coaxial cables shall be terminated with BNC plug connectors. A means shall be provided to ensure that the connector shell (which connects to the cable sheath) does not make contact with any building metal (at ground potential) or other unintended conductor.

An insulating sleeve or boot slipped over the connector at installation time is suitable.

In-line coaxial extensions shall be made with BNC receptacle-to-receptacle connectors joined together to form one "barrel." An insulating sleeve or boot shall also be provided with each barrel assembly.

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10.6.2 Coaxial cable terminator

Coaxial cable terminators are used to provide a termination impedance for the cable equal in value to its characteristic impedance, thereby minimizing reflection from the ends of the cables. Terminators shall be packaged within a male or female connector. The termination impedance shall be 50 Ω ± 1% measured from 0–20 MHz, with the magnitude of the phase angle of the impedance not to exceed 5°. The terminator power rating shall be 0.5 W or greater. A means of insulation shall be provided with each terminator.

10.6.3 MAU-to-coaxial cable connection

A BNC "T" (plug, receptacle, plug) adaptor provides a means of attaching a MAU to the coaxial cable. The connection shall not disturb the transmission line characteristics of the cable significantly; it shall present a low shunt capacitance, and therefore a negligibly short stub length. This is facilitated by the MAU being located as close to its cable connection as possible; the MAU and connector are normally considered to be one assembly. Long (greater than 4 cm) connections between the coaxial cable and the input of the MAU jeopardize this objective.

Overall system performance is dependent largely on the MAU-to-coaxial cable connection being of low shunt capacitance.

The design of the connection shall meet the electrical requirements contained in 10.4.1.1 and the reliability specified in 10.4.2.3. The use of BNC "T" adaptors and connectors satisfies these requirements. Figure 10–7 shows a MAU-to-coaxial cable attachment.

A means shall be provided to ensure that the connector assembly (that is, BNC "T" plus male connectors) does not make contact with any building metalwork (at ground potential) or any other unintended conductors. An insulating cover should therefore be applied after connection. A possible design is depicted in Figure 10–7. The insulating cover should have these characteristics:

a) It should guard against accidental grounding of the connector assembly.
b) It should allow ease of attachment and detachment of an assembled "T" connector to the MAU without necessitating the removal of section cable connectors (that is, segment integrity is maintained).
c) It should be a simple moulding that attaches firmly to a connector assembly.

10.7 System considerations

10.7.1 Transmission system model

The maximum configuration for the physical transmission system is as follows:

a) A trunk coaxial cable, terminated in its characteristic impedance at each end, constitutes a coaxial cable segment. A coaxial cable segment may contain a maximum of 185 m of coaxial cable and a maximum of 30 MAUs. The propagation velocity of the coaxial cable is assumed to be 0.65 c minimum ($c = 3 \times 10^8$ m/s). The maximum end-to-end propagation delay for a coaxial cable segment is 950 ns.
b) The maximum transmission path permitted between any two MAUs is limited by the number of repeater sets that can be connected in series.

   NOTE—Care should be taken to ensure that the safety requirements are met when extending the trunk cable by the use of repeaters (see 10.7.2.4.1).

c) The repeater unit specified in Clause 9 provides the means for connecting 10 Mb/s baseband segments into a CSMA/CD network. The proper operation of a CSMA/CD network requires network

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size to be limited to control round-trip propagation delay to meet the requirements of 4.2.3.2.3 and 4.4.2.1, and the number of repeaters between any two DTEs to be limited in order to limit the shrinkage of the interpacket gap as it travels through the network. Configuration rules, which ensure that these limits are not exceeded, are given in Clause 13.

NOTE—Care should be taken to ensure that the safety requirements are met when extending the trunk cable by the use of repeaters (see 10.7.2.4.1)

Figures 10–8 and 10–9 show minimal single segment and repeatered transmission systems. For specifications on the boundary conditions on topologies, see Clause 13.

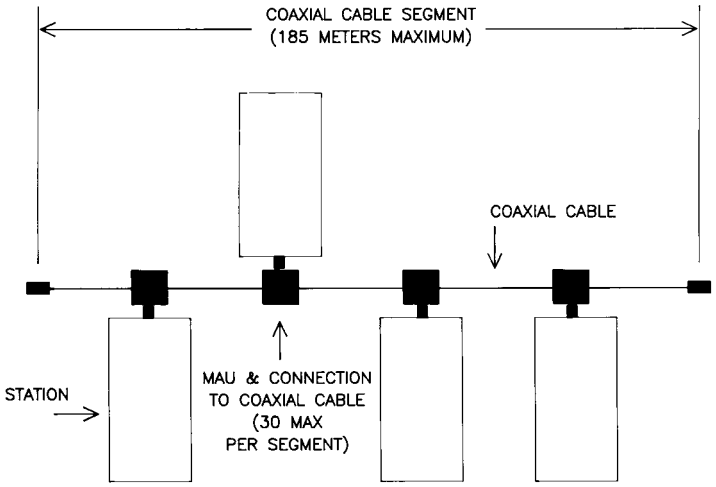


Figure 10–8—The minimum system configuration

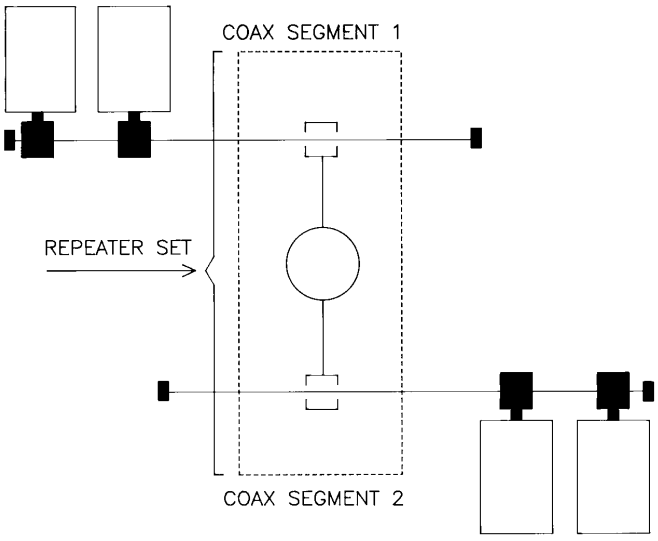


Figure 10–9—The minimum system configuration requiring a repeater set

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10.7.2 Transmission system requirements

10.7.2.1 Cable sectioning

The 185 m maximum length coaxial cable segment will be made from a number of cable sections. As the variation on cable characteristic impedance is ±2 Ω on 50 Ω, a possible worst-case reflection of 4% may result from the mismatch between two adjacent cable sections. The MAU will add to this reflection by the introduction of its noninfinite bridging impedance.

The accumulation of this reflection can be minimized by observing a minimum distance between MAUs (and between cable sections). In order to maintain reflections at an acceptable level, the minimum length cable section shall be 0.5 m.

10.7.2.2 MAU placement

MAU components and their associated connections to the cable cause signal reflections due to their noninfinite bridging impedance. While this impedance must be implemented as specified in 10.6, the placement of MAUs along the coaxial cable must also be controlled to ensure that reflections from the MAU do not accumulate to a significant degree.

Coaxial cable sections as specified in 10.7.2.1 shall be used to connect MAUs. This guarantees a minimum spacing between MAUs of 0.5 m.

The total number of MAUs on a cable segment shall not exceed 30.

10.7.2.3 Trunk cable system earthing

The shield conductor of each coaxial cable segment may make electrical contact with an effective earth reference[21] at one point and shall not make electrical contact with earth elsewhere on such objects as building structural metal, ducting, plumbing fixture, or other unintended conductor. Insulators should be used to cover any coaxial connectors used to join cable sections and terminators, to ensure that this requirement is met. A sleeve or boot attached at installation time is acceptable. (See 10.6.3.)

10.7.2.4 Static discharge path

A static discharge path shall be provided. The shield of the trunk coaxial cable is required to be connected to each DTE earth (within the DTE) via a 1 MΩ, 0.25 W resistor that has a voltage rating of at least 750 V dc.

10.7.2.4.1 Installation environment

This specification is intended for networks in use within a single building and within an area served by a single low-voltage power distribution system. Applications requiring interplant connections via external (outdoors) means may require special considerations. Repeaters and nonconducting IRL components may provide the means to satisfy these isolation requirements.

NOTE—The reader is advised that devices should not be operated at significantly different frame potentials. The 10BASE2 connection system may not be capable of handling excessive earth currents.

[21] See local or national regulations for guidance on these matters and reference [B29].

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10.8 Environmental specifications

10.8.1 Safety requirements

The designer should consult relevant local and national safety regulations to assure compliance with the appropriate standards (for example, see Annex A for reference material).

10.8.1.1 Installations

If the trunk coaxial cable is to be installed in close proximity to electrical power cables, then installation practice according to local and national code shall be followed (see Annex A for resource material).

10.8.1.2 Earthing

Where earthing is mandated by locally or nationally prescribed codes of practice, the shield of the trunk coaxial cable shall be effectively earthed at only one point along the length of the cable. Effectively earthed means permanently connected to earth through an earth connection of sufficiently low impedance and having sufficient ampacity to prevent the building up of voltages that may result in undue hazard to connected equipment or to persons.

10.8.2 Electromagnetic environment

10.8.2.1 Susceptibility levels

Sources of interference from the environment include electromagnetic fields, electrostatic discharge, transient voltages between earth connections, etc.

Several sources of interference will contribute to voltage buildup between the coaxial cable and the earth connection of a DTE.

The physical channel hardware shall meet its specifications when operating in either of the following conditions:

a) Ambient plane wave field of 1 V/m from 10 kHz through 1 GHz.

   NOTE—Levels typically >1 km from broadcast stations.

b) Interference source voltage of 15.10 V peak 10 MHz sine wave with a 50 Ω source resistance applied between the coaxial cable shield and the DTE ground connection.

MAUs meeting this standard should provide adequate RF ground return (coaxial cable shield to DTE ground) to satisfy the referenced EMC specifications.

10.8.2.2 Emission levels

The physical MAU and trunk cable system shall comply with local and national regulations (see Annex A for resource material).

10.8.3 Regulatory requirements

The MAU and medium should consider IEC 60950 in addition to local and national regulations. See IEC 60950 and [B29].

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11. Broadband medium attachment unit and broadband medium specifications, type 10BROAD36

NOTE—This MAU is not recommended for new installations.

11.1 Scope

11.1.1 Overview

This clause defines the functional, electrical, and mechanical characteristics of the Broadband Medium Attachment Unit (MAU) and the specific single- and dual-cable broadband media for use with LANs. The headend frequency translator for single-cable broadband systems is also defined. The relationship of this clause to all of the ISO/IEC LAN International Standards is shown in Figure 11–1. Repeaters as defined in Clause 9 are not relevant for 10BROAD36.

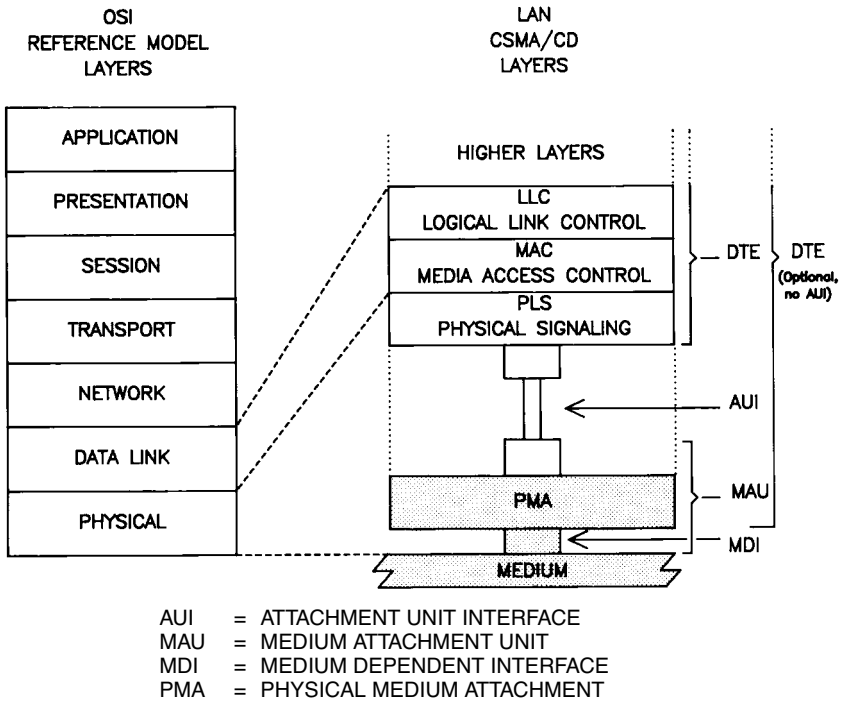


Figure 11–1—Physical Layer partitioning, relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

The purpose of the MAU is to provide a means of attaching devices to a broadband local network medium. The medium comprises CATV-type cable, taps, connectors, and amplifiers. A coaxial broadband system permits the assignment of different frequency bands to multiple applications. For example, a band in the spectrum can be utilized by LANs while other bands are used by point-to-point or multidrop links, television, or audio signals.

The physical tap is a passive directional device such that the MAU transmission is directed toward the headend location (reverse direction). On a single-cable system the transmission from the MAU is at a carrier frequency f1. A frequency translator (or remodulator) located at the headend up-converts to a carrier frequency

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f2, which is sent in the forward direction to the taps (receiver inputs). On a dual-cable system the transmit and receive carrier frequencies are identical (both f1) and the MAU connects to the medium via two taps, one on the receive cable and the other on the transmit cable. The transmit and receive cables are connected to each other at the headend location. Figure 11–2 shows broadband single- and dual-cable systems.

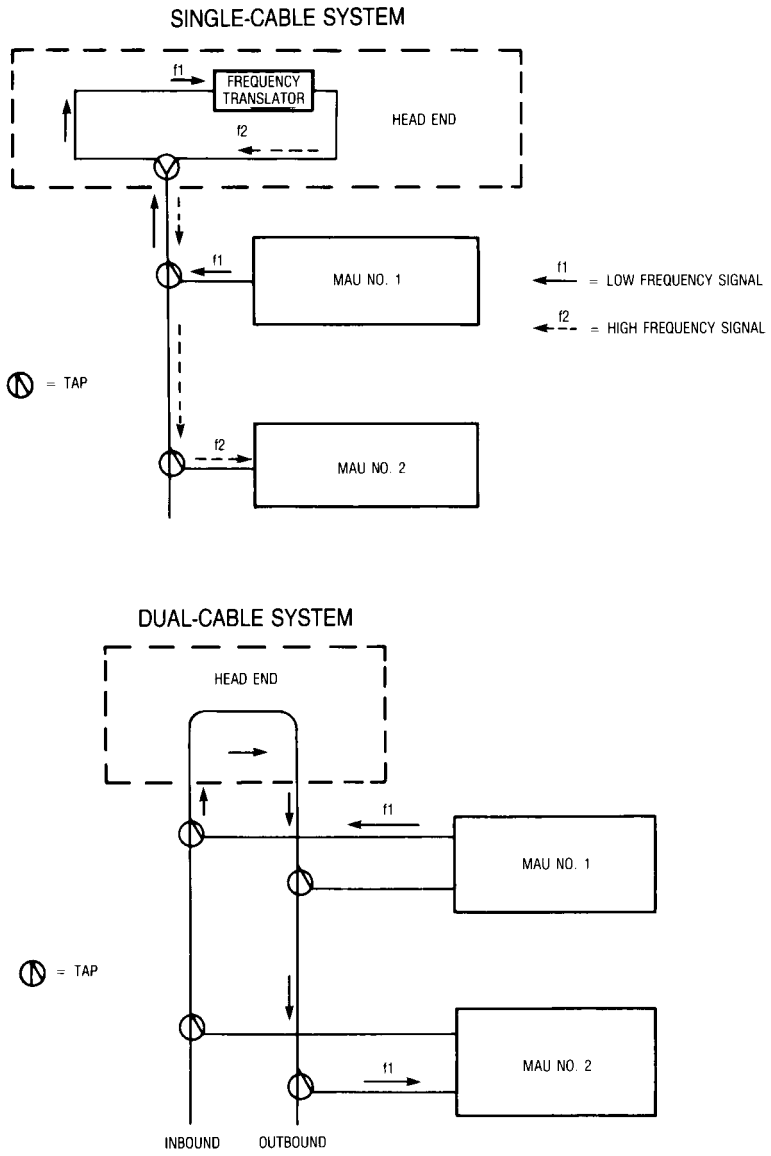


Figure 11–2—Broadband cable systems

The broadband MAU operates by accepting data from the attached Data Termination Equipment (DTE) and transmitting a modulated radio frequency (RF) data signal in a data band on the broadband coaxial cable system. All MAUs attached to the cable system receive and demodulate this RF signal and recover the DTE data. The broadband MAU emulates a baseband MAU except for delay between transmission and reception, which is inherent in the broadband cable system.

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A transmitting MAU logically compares the beginning of the received data with the data transmitted. Any difference between them, which may be due to errors caused by colliding transmissions, or reception of an earlier transmission from another MAU, or a bit error on the channel, is interpreted as a collision.

When a collision is recognized, the MAU stops transmission in the data band and begins transmission of an RF collision enforcement (CE) signal in a separate CE band adjacent to the data band. The CE signal is detected by all MAUs and informs them that a collision has occurred. All MAUs signal to their attached Medium Access Controllers (MACs) the presence of the collision. The transmitting MACs then begin the collision handling process.

Collision enforcement is necessary because RF data signals from different MAUs on the broadband cable system may be received at different power levels. During a collision between RF data signals at different levels, the MAU with the higher received power level may see no errors in the detected data stream. However, the MAU with the lower RF signal will see a difference between transmitted and received data; this MAU transmits the CE signal to force recognition of the collision by all transmitting MAUs.

11.1.2 Definitions

See 1.4.

11.1.3 MAU and medium objectives

This subclause states the broad objectives and assumptions underlying the specifications defined throughout this clause of the standard.

a) Provide the physical means for communication among local network Data Link Entities using a broadband coaxial medium.
b) Provide a broadband Medium Attachment Unit (MAU) that is compatible at the Attachment Unit Interface (AUI) with DTEs used on a baseband medium.
c) Provide a broadband MAU that emulates the baseband MAU except for the signal delay from Circuit DO to Circuit DI.
d) Provide a broadband MAU that detects collisions within the timing constraints specified in the baseband case.
e) Provide a broadband network diameter no less than 2800 m.
f) Provide a broadband Physical Layer that ensures that no MAU is allowed to capture the medium during a collision due to signal level advantage (that is, ensures fairness of the physical layer).
g) Provide a broadband MAU that detects collisions in both receive and transmit modes.
h) Provide a broadband MAU that requires a transmission bandwidth no wider than 18 MHz.
i) Define a physical interface that can be implemented independently among different manufacturers of hardware and achieve the intended level of compatibility when interconnected in a common broadband LAN.
j) Provide a communication channel capable of high bandwidth and low bit error rate performance. The resultant mean bit error rate at the physical layer service interface should be less than one part in 10^8 (on the order of one part in 10^9 at the link level) in a worst-case signal-to-noise ratio of 26 dB.
k) Provide a broadband medium physical layer that allows for implementation in both dual- and single-cable systems.
l) Provide for ease of installation and service.
m) Provide a communication channel that coexists with other channels on the same physical medium.

It is not an objective of this broadband MAU to allow its use with the baseband repeater defined in Clause 9 of this standard.

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11.1.4 Compatibility considerations

All implementations of the broadband coaxial system shall be compatible at the Medium Dependent Interface (MDI). This standard provides medium specifications for the interconnection of all MAU devices. The medium itself, the functional capability of the MAU and the AU Interface are defined to provide the highest possible level of compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the MAU in an application-dependent manner provided the MDI and AUI specifications are satisfied. Subsystems based on this specification may be implemented in several different ways provided compatibility at the medium is maintained. It is possible, for example, to design an integrated station where the MAU is contained within a physical DTE system component, thereby eliminating the AUI cable.

11.1.5 Relationship to PLS and AUI

The broadband MAU and cable system specifications are closely related to Clause 7 (Physical Signaling and Attachment Unit Interface Specifications). The design of a physical MAU component requires the use of both this clause and the PLS and AUI specifications in Clause 7.

11.1.6 Mode of operation

In its normal mode of operation, the MAU functions as a direct connection between the DTE and the broadband medium. Data from the DTE are transmitted onto the broadband coaxial system and all inband data on the coaxial cable system is received by the DTE. This mode is the mode of operation for the intended message traffic between stations. Other operating modes, such as a loopback mode or a monitor mode, may be provided but are not defined by this standard.

11.2 MAU functional specifications

11.2.1 MAU functional requirements

The MAU component provides the means by which signals on the physically separate AUI signal circuits to and from the DTE and their associated interlayer messages are coupled to the broadband coaxial medium. To achieve this basic objective, the MAU component contains the following capabilities to handle message flow between the DTE and the broadband medium:

a) *Transmit function*. The ability to transmit serial data bit streams originating at the local DTE in a band-limited modulated RF carrier form, to one or more remote DTEs on the same network.
b) *Receive function*. The ability to receive a modulated RF data signal in the band of interest from the broadband coaxial medium and demodulate it into a serial bit stream.
c) *Collision Presence function*. The ability to detect the presence of two or more stations' concurrent transmissions.
d) *Jabber function*. The ability of the MAU itself to interrupt the Transmit function and inhibit an abnormally long output data stream.

11.2.1.1 Transmit function requirements

The Transmit function shall include the following capabilities:

a) Receive Manchester encoded data sent by the local DTE to the attached MAU on Circuit DO (transmit data pair).
b) Decode the Manchester encoded data received on Circuit DO to produce NRZ (Non-Return to Zero) data and a recovered clock signal.

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c) Scramble the NRZ data using a CCITT V.29-type scrambler with seed changed on each transmitted packet.
d) Transform the incoming bits (prior to modulation) to provide an unscrambled alternating zero-one pattern terminated by an Unscrambled Mode Delimiter (UMD); scramble the remainder of the incoming preamble, Start Frame Delimiter (SFD), and data frame; and append an unscrambled postamble (Broadband End of Frame Delimiter [BEOFD]).
e) Differentially encode the packet generated above.
f) Produce a bandlimited, double sideband suppressed carrier, binary PSK modulated RF signal representing the above generated differentially encoded packet.
g) Drive the coaxial cable with the modulated RF signal.

Figure 11–3 functionally represents these capabilities. The order of the functional blocks may be altered provided that the result is the same.

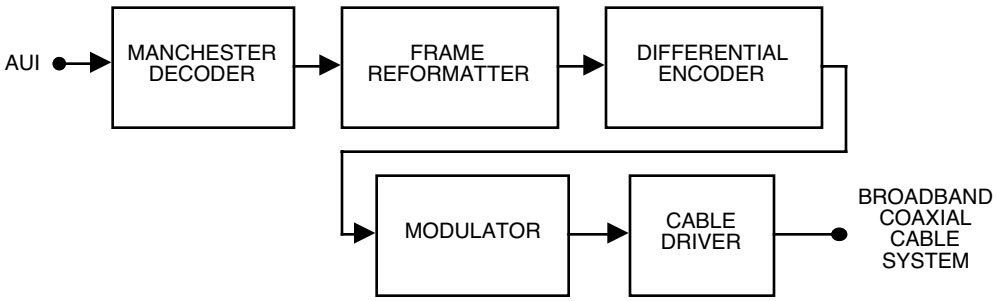


Figure 11–3—Transmit function requirements

11.2.1.2 Receive function requirements

The receive function shall include the following:

a) Receive the differentially encoded binary PSK modulated RF signal from the broadband coaxial medium.
b) Receive the data band RF signals and reject signals in bands other than the data band (rejection of signals in the adjacent collision enforcement band is optional).
c) Demodulate and differentially decode the incoming RF data signal from the coaxial medium to provide a receive bit stream that represents the scrambled bit stream at the transmitter.
d) Descramble the receive bit stream using a self-synchronizing descrambler.
e) Manchester encode the descrambled bit stream.
f) Send to the DTE, using Circuit DI (receive data pair), an additional, locally-generated, Manchester encoded preamble equal to the number of preamble bits lost in the receive data path (plus or minus one bit), followed by the Manchester encoded bit stream. No more than 6 preamble bits may be lost from the preamble presented to Circuit DO at the transmitting MAU.
g) Detect end of frame, using the postamble (BEOFD), and ensure that no extraneous bits are sent to the DTE on Circuit DI.
h) Receive signals in the collision enforcement band and reject signals in the data band and all other bands on the broadband medium.

11.2.1.3 Collision Detection function requirements

The MAU shall perform the following functions to meet the collision detection requirements:

a) Store the scrambled bits (not differentially encoded) in the transmit section through to the last bit in the source address.

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b) Detect the UMD in the transmit and receive paths.
c) Compare received scrambled bits after the received UMD with transmitted scrambled bits after the transmit UMD through to the last bit in the source address.
d) A Receive UMD Timer function shall be performed by the MAU. The timer shall be as long as the time required from initial detection of RF data signal presence to detection of a UMD in a normally received (no collision) packet.
e) Enter a LOCAL COLLISION DETection state if one of the following occurs:
   1) A bit error is found in the bit compare process through the last bit in the source address.
   2) The Receive UMD Timer expires before a UMD is detected in the received bit stream.
   3) The MAU receives the *output* (that is, transmit) signal from the AUI AFTER having received an RF signal from the coaxial cable.
f) Upon entering the LOCAL COLLISION DET state, cease transmission in the data band and commence transmission in the collision enforcement band for as long as the DTE continues to send data to the MAU.
g) Upon entering the LOCAL COLLISION DET state send the *signal_quality_error* (SQE) message on Circuit CI (collision presence pair) using the CS0 signal for as long as RF signals are detected on the broadband coaxial medium in either the data or collision enforcement bands.
h) Detect power in the collision enforcement band and send the SQE message on Circuit CI using the CS0 signal. Send the SQE message for as long as energy is detected in the collision enforcement band.
i) Ensure that during collisions, due to phase cancellations of the colliding carriers, Circuit DI does not become inactive before Circuit CI becomes active.
j) Test the collision detection circuitry following every transmission that does not encounter a collision. This test consists of transmitting a burst of collision enforcement RF signal after the end of the postamble transmission and detecting this burst on the receive side. If the burst is detected, the CS0 (BR) signal is sent on Circuit CI of the transmitting MAU.

11.2.1.3.1 Collision enforcement transmitter requirements

The MAU shall provide a collision enforcement (CE) transmitter that generates a constant amplitude RF signal in the CE band at the same power level as the data signal postamble.

11.2.1.3.2 Collision enforcement detection requirements

The MAU shall detect energy in the CE band that is within the specified range of receive levels, irrespective of the signal power level in the data band.

11.2.1.4 Jabber function requirements

The MAU shall have a Jabber function that inhibits transmission onto the coaxial cable interface if the MAU attempts to transmit an RF signal longer than 150 ms. The MAU shall provide an MTBF of at least 1 million hours of continuous operation without rendering the transmission medium unusable by other transceivers. Transmissions of less then 20 ms shall not be affected. When the jabber circuit is activated, *signal_quality_error* shall be sent on Circuit CI.

Circuit DO shall also be monitored for transmissions in excess of the maximum packet length. If the packet is longer than 20 ms, an attempt shall be made to deactivate the transmitter before the jabber circuit is activated, to avoid locking up the unit due to a non-MAU failure.

State diagrams defining the Jabber function may be found in 11.2.3.

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11.2.2 DTE PLS to MAU and MAU to DTE PLS messages

11.2.2.1 DTE Physical Layer to MAU Physical Layer messages

The following messages can be sent by the DTE Physical Layer entities to the MAU Physical Layer entities (refer to 7.3 of this standard for the definitions of the signals):

Message	Circuit	Signal	Meaning
output	DO	CD1, CD0	Output information
output_idle	DO	IDL	No data to be output

11.2.2.2 MAU Physical Layer to DTE Physical Layer messages

The following messages can be sent by the MAU Physical Layer entities to the DTE Physical Layer entities:

Message	Circuit	Signal	Meaning
input	DI	CD1, CD0	Input information
input_idle	DI	IDL	No input information
mau_available	CI	IDL	MAU is available for output
signal_quality_error	CI	CS0 (BR)	Error detected by MAU

11.2.2.2.1 *input* message

The MAU Physical Layer sends an *input* message to the DTE Physical Layer when the MAU has a bit of data to send to the DTE. The physical realization of the *input* message is a CD0 or CD1 sent by the MAU to the DTE on Circuit DI. The MAU sends CD0 if the input bit is a zero or CD1 if the input bit is a one. The jitter and asymmetry on CD0 and CD1 shall be no more than that specified in 7.5.2.1.

11.2.2.2.2 *input_idle* message

The MAU Physical Layer sends an *input_idle* message to the DTE Physical Layer when the MAU does not have data to send to the DTE. The physical realization of the *input_idle* message is the IDL signal sent by the MAU to the DTE on Circuit DI.

11.2.2.2.3 *mau_available* message

The MAU Physical Layer sends a *mau_available* message to the DTE Physical Layer when the MAU is available for output. The *mau_available* message is always sent by an MAU that is prepared to output data. The physical realization of the *mau_available* message is an IDL signal sent by the MAU to the DTE on Circuit CI.

11.2.2.3 *signal_quality_error* message

The *signal_quality_error* message shall be implemented in the following fashion:

a) The *signal_quality_error* (SQE) message shall not be sent by the MAU if no or only one MAU is transmitting a legal length packet (as specified in this standard) on the coaxial medium, except as a part of the SQE self test.

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b) If the MAU connected to the local node is not transmitting, then the local MAU shall send the *signal_quality_error* message in every instance when it detects power in the collision enforcement band earlier than the time equivalent for reception of a 512 bit data frame plus preamble and SFD.
c) When the local MAU is transmitting on the coaxial medium, all occurrences of one or more additional MAUs transmitting shall cause the *signal_quality_error* message to be sent by the local MAU to the attached DTE.
d) When the MAU has completed a successful transmission of a packet it shall perform an SQE Test sequence. In this instance, the collision enforcement RF signal is interpreted as an SQE Test signal.

11.2.3 MAU state diagrams

The operation of the MAU during normal transmission and reception can be described by a state diagram that relates the functions of transmission, reception, collision detection, and collision detection testing. Figure 11–4, at the end of this subclause, shows the state transitions for normal operation. Abnormal conditions are implementation-specific.

The state diagram in Figure 11–4 does not describe the operation of the MAU in detail. This is found in 11.2 and 11.3.

The operation of the Jabber function is described by the state diagram of Figure 11–5. When the MAU Jabber state machine is in the INTERRUPT or JAB state, outputs of the MAU Jabber state machine shall override those of the MAU state machine.

11.2.3.1 MAU state diagram messages

The following messages are used in the state diagram:

a) disable_data_driver. Deactivates the mechanism by which the RF data signal is impressed onto the coaxial cable.
b) enable_data_driver. Activates the mechanism by which the RF data signal is impressed onto the coaxial cable.
c) disable_CE_driver. Deactivates the mechanism by which collision enforcement RF signals are impressed onto the coaxial cable.
d) enable_CE_driver. Activates the mechanism by which collision enforcement RF signals are impressed onto the coaxial cable.
e) *mau_available*. Signifies that the MAU is available for transmission (that is, there is no SQE active).
f) *signal_quality_error* (SQE). Signifies that the MAU has detected a collision, it has successfully completed the SQE Test sequence, or the jabber circuit is active.
g) start_SQE_test_timer. Causes a timer to begin counting so that the SQE Test signal may be sent to the coaxial cable interface.
h) positive_disable. Prevents any RF signal from being sent onto the coaxial cable.

11.2.3.2 MAU state diagram signal names

The signal names used in the state diagram are as follows:

a) PowerOn. This signal signifies that power has been applied to the unit.
b) rx_energy. When this signal is active, an RF signal on the coaxial cable has been detected either in the data band or in the collision enforcement band or in both. The delay in asserting or de-asserting this signal is sufficiently short that the delays specified in 11.3.4.5 are met.
c) output. Signifies that data from the DTE is being presented for transmission at the AUI.
d) tx_umd (Transmit Unscrambled Mode Delimiter). When the Unscrambled Mode Delimiter has been detected in the transmit data sequence, this signal is asserted.

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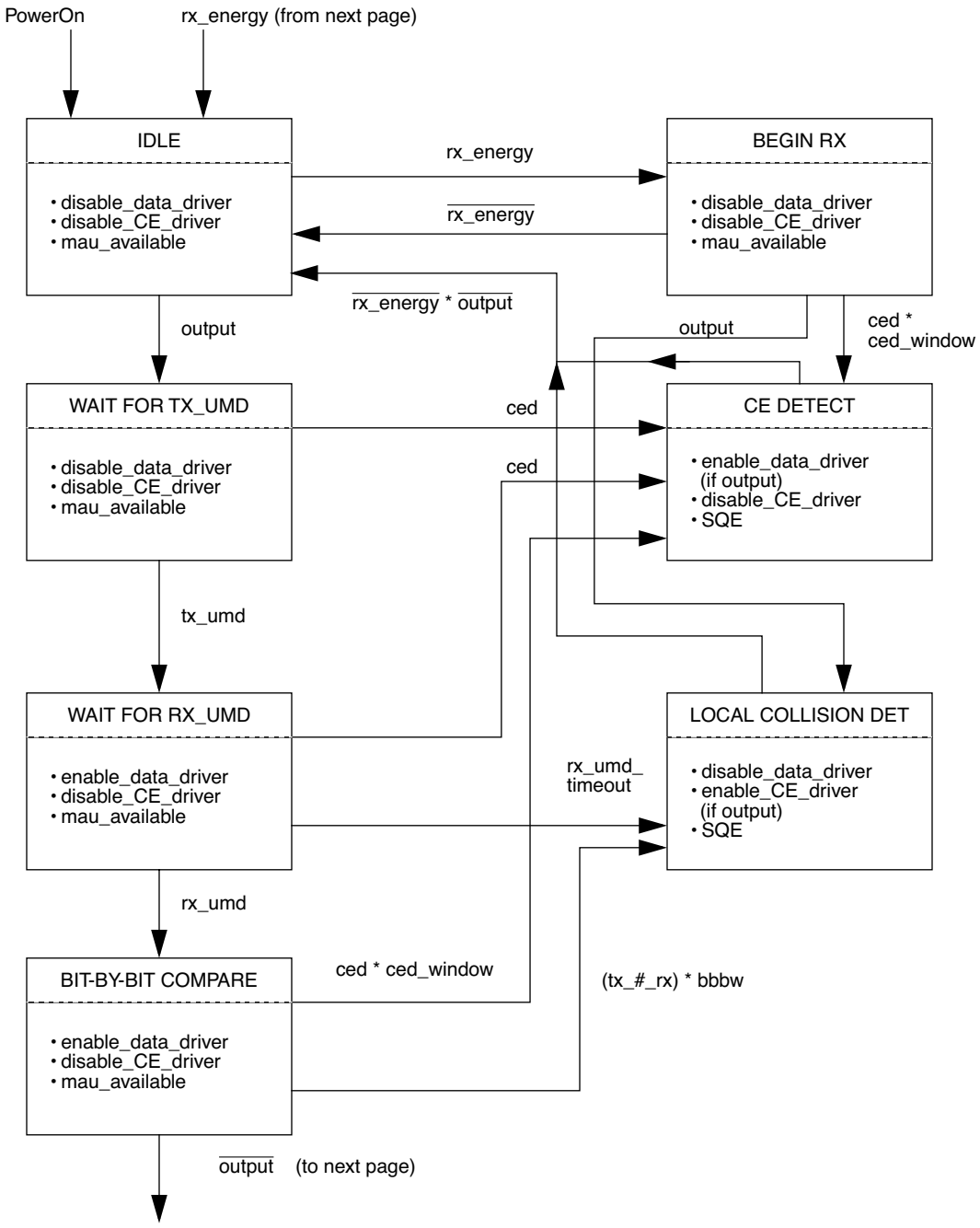


Figure 11–4—MAU state diagram

e) rx_umd (Receive Unscrambled Mode Delimiter). When the Unscrambled Mode Delimiter has been detected in the receive data sequence as it is conveyed from the coaxial cable interface, this signal is asserted.

f) SQE_test_timer. This signal is on during the time that the SQE Test Timer is engaged. At the end of the time, this signal is de-asserted.

g) rx (Receive). As long as data is being presented by the MAU to Circuit DI of the AUI, this signal is active. When the last bit of the receive data has been presented to the AUI, this signal is de-asserted.

h) ced (Collision Enforcement Detection). RF signal power in the collision enforcement band causes this signal to be asserted.

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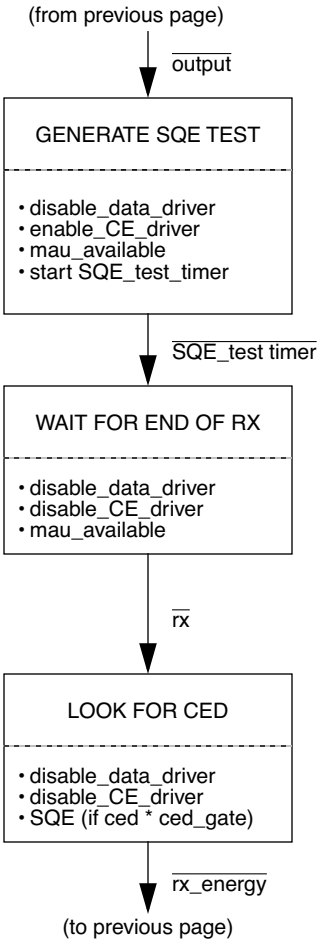


Figure 11-4—MAU state diagram *(continued)*

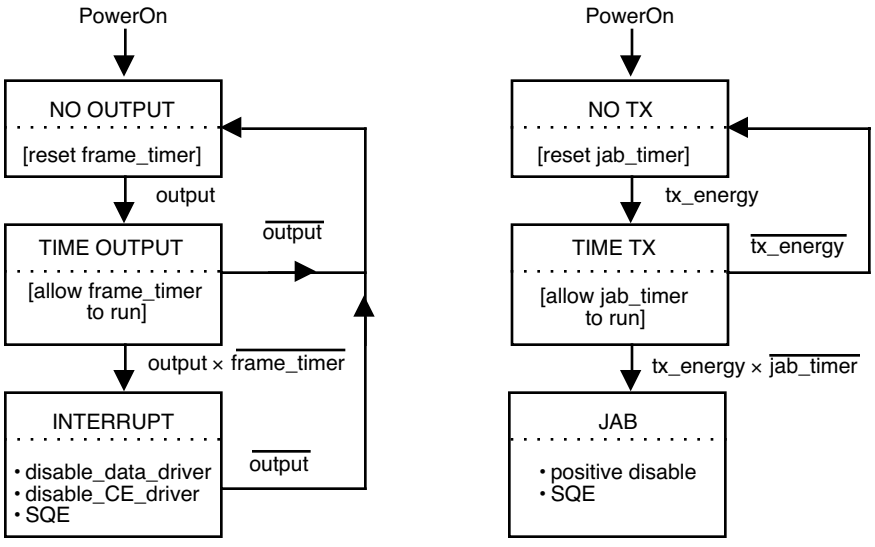


Figure 11–5—MAU jabber state diagram

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i) ced_window (Collision Enforcement Detection Window). This signal defines a period of time (a "window") during which collisions may occur. Its purpose is to distinguish collision enforcements from SQE Test sequences on the coaxial cable. The window opens when rx_energy goes active and closes a minimum of 365 bit times later. The maximum time the window may be open is the minimum frame length, plus preamble and SFD: 576 bits.

j) rx_umd_timeout (Receive Unscrambled Mode Delimiter Timeout). It is possible that the Receive Unscrambled Mode Delimiter may be corrupted by a collision such that the bit-by-bit comparison may not begin. This signal forces detection of a collision due to failure to detect the rx_umd within a maximum time. The timeout begins upon receipt of RF signal in the data band and expires 32 bit times later.

k) tx_#_rx (Transmit Not Equal to Receive). Assertion of this signal occurs when a difference is detected between the received data stream and the transmitted data stream.

l) bbbw (Bit-by-Bit Window). Bit-by-bit comparison shall be performed only for a time long enough to guarantee that the last bit of the source address has been examined. This signal is asserted after the UMD is received and throughout the bit-by-bit comparison process. To place a bound on the location of the source address relative to the UMD, the maximum preamble length permitted for operation with the broadband MAU is 62 bits. This places the last bit of the source address no later than 143 bits after the UMD.

m) ced_gate. This signal is a gating function that serves to shape the timing of ced during an SQE Test. It becomes true a minimum of 6 and a maximum of 16 bit times after the last bit has been presented to Circuit DI and stays active 10 ± 5 bit times.

n) tx_energy. This signal signifies that the MAU is attempting to transmit an RF signal onto the coaxial cable.

o) frame_timer. This signal is on from the beginning of output until it is reset or until it has been on continuously for timeout1 s. The value of timeout1 shall be greater than 20 ms and less than timeout2.

p) jab_timer. This signal turns on when tx energy turns on and lasts until it is reset or until it has been on continuously for timeout2 s. The value of timeout2 shall be greater than timeout1 and less than 150 ms.

11.3 MAU characteristics

11.3.1 MAU-to-coaxial cable interface

The following subclauses describe the interface between the MAU and the broadband coaxial medium. The medium is a 75 Ω CATV-type broadband cable installation employing a single bidirectional cable with band-split amplifiers and filters, or dual unidirectional cables with line amplifiers.

11.3.1.1 Receive interface

11.3.1.1.1 Receive input impedance

The nominal input impedance at the receive port shall be 75 Ω. The return loss within the data and collision enforcement frequency bands shall be at least 14 dB with power applied to the MAU.

11.3.1.1.2 Receiver squelch requirements

There shall be a receiver squelch that inhibits reception of RF signals that are too low in level. This squelch shall permit reception of RF data or collision enforcement signals that are greater than or equal to –7 dBmV rms as measured by the method of 11.3.1.2.5. RF signals (data, collision enforcement, noise, or other signals) of levels lower than –15 dBmV rms shall be ignored.

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The receive squelch for CE signals shall be derived from a power detector with noise bandwidth greater than or equal to 1.5 MHz centered at the CE center frequency.

11.3.1.1.3 Receive level requirements

The receiver shall operate with RF data and CE signals having levels from –4 dBmV to +16 dBmV rms. The nominal receive level shall be +6 dBmV rms.

11.3.1.1.4 Receiver selectivity and linearity requirements

The MAU shall operate in the presence of single frequency (CW) signals adjacent to the receive band of the MAU and offset from the band edges, received at the following levels:

a) 0 dBmV rms at 0.25 MHz below and above the band
b) 10 dBmV rms at 1.25 MHz below and above the band

The receiver shall be capable of operating in a cable environment loaded with TV signals (for example, every 6 MHz in the USA). The TV signals shall be no higher than +10 dBmV peak video at the receiver coaxial cable interface.

11.3.1.1.5 Receive input mechanical requirements

The receiver mechanical interface shall be a 75 Ω female F-series coaxial connector. The connection to the broadband medium shall be through a coaxial drop cable with a mating male F-series connector. For single-cable configurations, the same connector may be used for receive and transmit.

11.3.1.2 Transmit interface

11.3.1.2.1 Transmit output impedance

The nominal output impedance at the transmit port shall be 75 Ω. The return loss within the data and collision enforcement frequency bands shall be at least 14 dB with power applied.

11.3.1.2.2 Transmitted RF packet format

Figure 11–6 shows the transmitted RF packet format.

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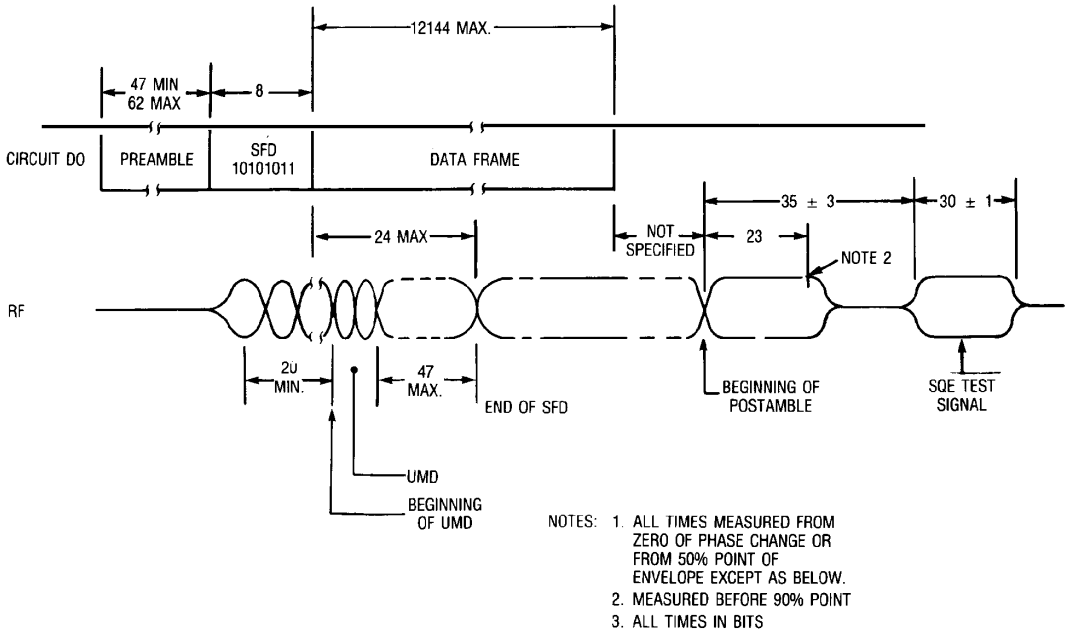


Figure 11–6—Packet format and timing diagram (AUI to coaxial cable interface)

11.3.1.2.3 Transmit spectrum and group delay characteristics

The transmit RF data signal shall be binary phase-shift-keyed (PSK) modulated and shall have a frequency spectrum equivalent to baseband raised-cosine Nyquist filtering with a rolloff factor (a) of 0.4, and within the limits of Figure 11–7. For rectangular pulses, the filter characteristic is

$$H(jw) \begin{cases} \dfrac{w(T/2)}{\sin\left(w\dfrac{T}{2}\right)}; & \left[0 <= w < \dfrac{\pi}{T}(1-a)\right] \\ \dfrac{w(T/2)}{\sin(wT/2)} \quad ;\cos^2\left(\dfrac{T}{4a}\left[w - \dfrac{\pi(1-a)}{T}\right]\right); & \\ & \left[\dfrac{\pi}{t}(1-a) <= w < \dfrac{\pi}{T}(1+a)\right] \\ 0; & \left[w >= \dfrac{\pi}{T}(1+a)\right] \end{cases}$$

where T = one symbol time (100 ns for 10 Mb/s) and a = 0.4, and the first term accounts for the sin x/x spectrum of NRZ random data.

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The total variation in group delay from Circuit DO to the RF coaxial medium interface shall not exceed 20 ns in the frequency band from the carrier frequency to ± 5 MHz, and 32 ns to ± 5.5 MHz.

The collision enforcement (CE) signal shall be a constant amplitude pulse with controlled turn-on and turn-off times. Random modulation may be added to reduce the probability of cancellation when more than one CE signal is received simultaneously. The modulated signal shall have an instantaneous frequency within 0.75 MHz of the CE band center frequency and shall conform to the spectrum mask specified in 11.3.1.2.4. The random modulation may be derived from the transmit NRZ data stream.
The CE signal rise and fall times shall approximate a Gaussian shape of the form

$$f(t) = \exp\left(-\frac{1}{2}\left[\frac{t}{T}\right]^2\right)$$

where T = one symbol time and $t < 0$ for the rise time and $t > 0$ for the fall time.

The CE and data RF signals shall not be transmitted simultaneously.

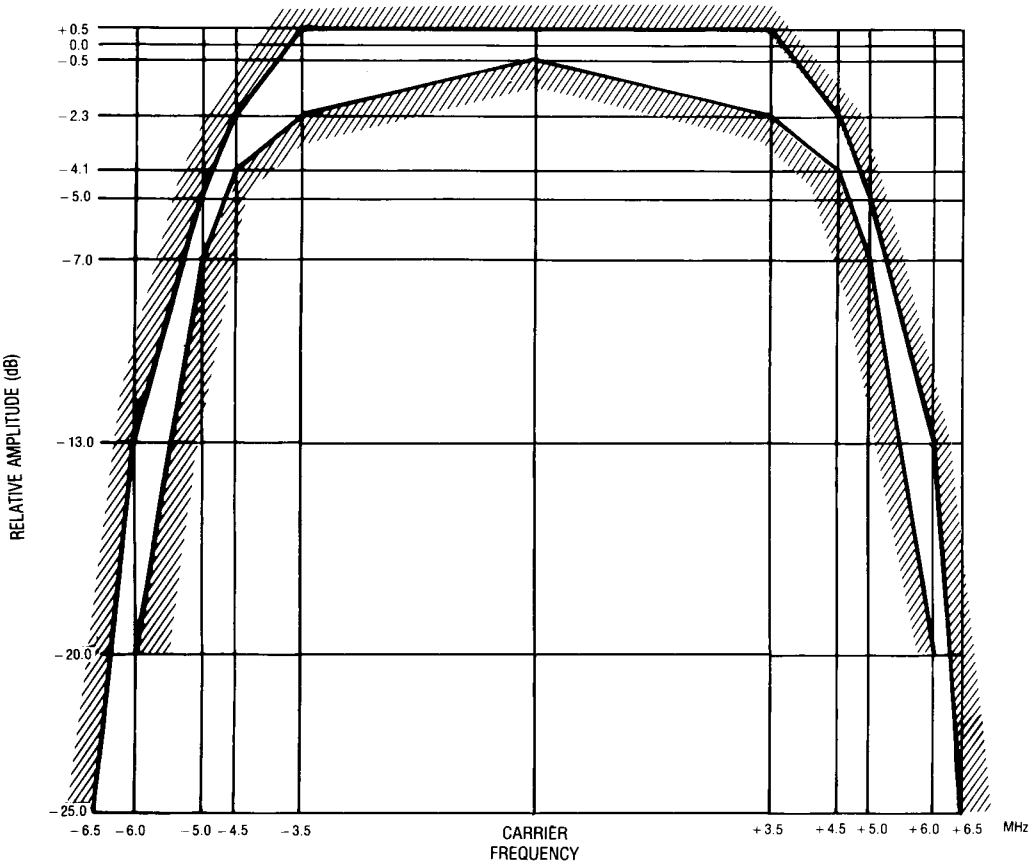


Figure 11–7—Spectrum mask for RF data signal

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11.3.1.2.4 Transmit out-of-band spectrum

The transmitted power outside the specified band shall meet or exceed the relative attenuation (RA) specified below, under the following conditions:

a) Transmitted packet length is 256 bits with a 25.6 μs interval between packets, for 50% duty cycle on the cable.
b) Reference level is an unmodulated carrier, equivalent to the postamble transmitted level.
c) RA is the attenuation in decibels relative to the reference level outside the specified band, measured in a 30 kHz noise bandwidth with a video filter of 300 Hz bandwidth or less.
d) B is 18 MHz, the width of data plus collision enforcement bands.
e) MF is the measurement frequency in MHz.
f) NCEF is the frequency of the nearest edge of the band, in MHz.

$$RA = \min (63, 55 + 30 \times | (MF - NCEF) / B|)$$

Figure 11–8 graphically shows the attenuation requirement for out-of-band power.

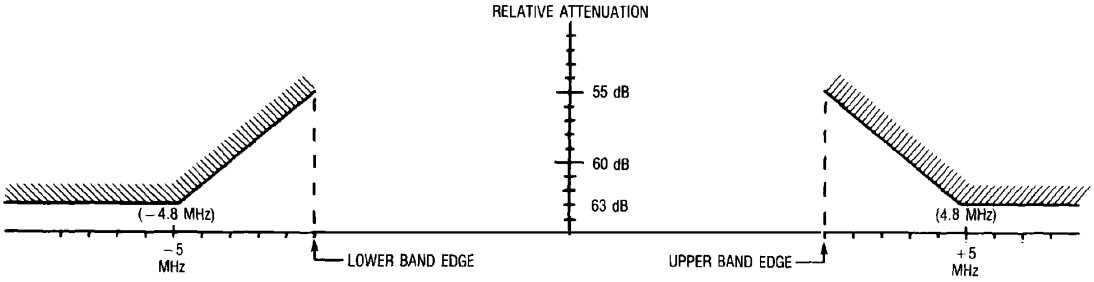


Figure 11–8—Transmit out-of-band power attenuation

11.3.1.2.5 Transmit level requirements

The transmitter output power during the postamble and during the SQE Test of the collision enforcement signal shall be 1000 mV peak-to-peak into a 75 Ω load (51 dBmV rms). Truncation loss due to the specified data filtering is 1 dB; transmitted RF data signal power is 50 dBmV rms. Transmit output power variations shall not exceed ± 2 dB.

11.3.1.2.6 Nontransmitting signal leakage requirement

The RF data signal and collision enforcement signal leakage to the coaxial cable interface while the MAU is not in its transmission mode shall be less than –20 dBmV rms.

11.3.1.2.7 Transmit spurious output requirement

All spurious signals from the transmitter (inband and out-of-band) while not transmitting shall be less than –20 dBmV rms. All spurious signals from the transmitter while transmitting data or collision enforcement shall be below the spectrum mask specified in 11.3.1.2.4.

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11.3.1.2.8 Collision enforcement signal leakage requirement

The collision enforcement RF signal leakage to the coaxial cable during data transmission and while the MAU is not enforcing collisions shall be less than 5 dBmV rms. Leakage shall be less than –20 dBmV rms when the MAU is not in the transmission mode.

11.3.1.2.9 Transmit output mechanical requirements

The transmit mechanical interface shall be a 75 Ω female F-series coaxial connector. The connection to the broadband medium shall be through a coaxial drop cable with a mating male F-series connector. For single cable installations, the same connector may be used for transmit and receive.

11.3.2 MAU frequency allocations

The broadband MAU uses a data band 14 MHz wide and an adjacent collision enforcement band 4 MHz wide. A single cable midsplit configuration with a frequency offset of 156.25 MHz or 192.25 MHz between forward and reverse channels is recommended. Other configurations, including dual-cable, where forward and reverse channels are on separate unidirectional cables, also are permitted.[22] The preferred pairing for the usual North American 6 MHz channels is specified in Table 11–1 and Table 11–2. The tables also specify the data carrier or collision enforcement center frequency for each band, and for single-cable systems, the frequency translation and the headend local oscillator frequency.

11.3.2.1 Single-cable systems frequency allocations

Table 11–1 lists the permissible frequency band allocations for single-cable systems. The 192.25 MHz translation is recommended for all new designs. The 156.25 MHz translation is allowed for compatibility with some existing systems. The 156.25 MHz translation results in a reversal of the data and collision enforcement bands, as the lower sideband is used.

Table 11–1—Single-cable frequency allocations (frequencies in MHz)

TRANSMITTER				RECEIVER		
Data carrier	Coll enf center freq	Transmit band	Translation 156.25 MHz		Translation 192.25 MHz	
			Headend local osc	Receive band	Headend local osc	Receive band
43	52	35.75–53.75	245.75	192-210	192.25	228-246
49	58	41.75–59.75	257.75	198-216	192.25	234-252
55	64	47.75–65.75	269.75	204-222	192.25	240-258
+61	70	53.75–71.75	281.75	210-228	192.25	246-264
67	76	59.75–77.75	293.75	216-234	192.25	252-270
73	82	65.75-83.75	305.75	222-240	192.25	258-276

NOTES
1—Some of these optional bands are overlapping.
2—Frequency tolerance of the data carrier and headend local oscillator shall each be ± 25 kHz.
3—+ denotes the preferred frequency allocation.

[22] The remainder of 11.3.2 and all of 11.3.2.1 and 11.3.2.2 are not part of the ISO/IEC International Standard. Frequency allocations are a subject for national standardization.

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11.3.2.2 Dual-cable systems frequency allocations[23]

In nontranslated dual-cable systems transmit and receive frequencies are identical. Table 11–2 lists the permissible frequency band allocations. In some instances translated dual-cable systems are installed. In such cases the single-cable frequency allocations may be used.

Table 11–2—Dual-cable frequency allocations (frequencies in MHz)

Data carrier	Coll enf center freq	Data band	Coll enf band
43	52	36–50	50–54
49	58	42–56	56–60
55	64	48–62	62–66
+61	70	54–68	68–72
67	76	60–74	74–78
73	82	66–80	80–84
235.25	244.25	228–242	242–246
241.25	250.25	234–248	248–252
247.25	256.25	240–254	254–258
253.25	262.25	246–260	260–264
259.25	268.25	252–266	266–270
265.25	274.25	258–272	272–276

NOTE 1— Some of these optional bands are overlapping.
NOTE 2—Frequency tolerance of the data carrier shall be ± 25 kHz.
NOTE 3— + denotes the preferred frequency allocations.

11.3.3 AUI electrical characteristics

11.3.3.1 Electrical isolation requirements

The MAU must provide isolation between the AUI cable and the broadband coaxial medium. The isolation impedance shall be greater than 250 kΩ at 60 Hz, measured between any conductor (including shield) of the AU Interface cable and either the center conductor or shield of the coaxial cable. The isolation means provided shall be able to withstand 500 Vac rms for one minute.

The MAU power supply, if provided, shall meet the appropriate national requirements. See IEC 950: 1991 for guidance.

11.3.3.2 Current consumption

The MAU may have its own power supply but is also allowed to use the power supplied by the DTE through the AUI cable. When drawing current from the AUI, the current shall not exceed 0.5 A as provided by the AUI source. The MAU shall be capable of operating from all possible voltage sources as supplied by the DTE through the resistance of all permissible AUI cables. The MAU shall not disrupt the broadband coaxial medium should the DTE power source fall below the minimum operational level under abnormal MAU load conditions. The MAU shall be labeled externally to identify the nominal value of current required by the device at the AUI.

[23] See Footnote 22.

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11.3.3.3 Driver and receiver requirements

The requirements for AUI cable driver and receiver components within the MAU are identical with those specified in Clause 7 of this standard. The drivers shall provide signals that meet the symmetry and jitter requirements of Circuit DI defined in Clause 7 and the receivers shall accept signals that have traversed the worst-case lengths of AUI cable.

11.3.3.4 AUI mechanical connection

The MAU shall be provided with a 15-pin male connector as specified in detail in the PLS/AUI specifications, in 7.6 of this standard.

11.3.4 MAU transfer characteristics

Signals presented on Circuit DO are transformed into signals at the coaxial cable interface by delaying them and by reformatting them. Signals at the coaxial cable interface are transformed into signals on Circuit DI and Circuit CI by a different framing change and by additional delay.

11.3.4.1 AUI to coaxial cable framing characteristics.

Data presented on Circuit DO shall first be received differentially, then Manchester decoded into an NRZ data stream. The framing of the data shall then be transformed into a new packet for presentation to the RF modulator in the following way (see Figure 11–6 and Figure 11–9):

a) Up to 5 bits of the incoming data stream may be dropped for detection and Manchester decoding purposes.
b) Beginning with the first zero, 20 bits of zero-one pattern shall be sent for receiver synchronization and clock recovery.

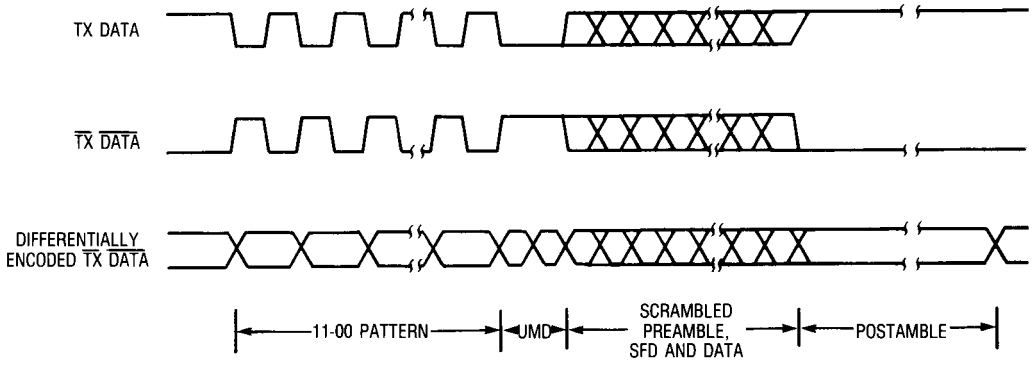


Figure 11–9—Packet format at modulator input

c) The next two bits (zero-one in the incoming pattern) shall both be set to zero and form the Unscrambled Mode Delimiter (UMD). The UMD shall take the place of the zero-one in the incoming pattern; it shall not be inserted into the data stream.
d) All remaining bits in the preamble, SFD, and data fields shall be scrambled (using a CCITT V.29 scrambler plus a differential encoder per 11.3.4.1).
e) A postamble (BEOFD) consisting of a zero followed by 22 ones shall be added immediately after the last scrambled data bit (the postamble is not scrambled). The postamble may be extended to allow controlled turnoff of the transmitted signal, as shown in Figure 11–6.

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f) All bits (unmodified preamble; UMD; scrambled preamble, SFD, and data; and postamble) are inverted.
g) All bits sent to the RF modulator are differentially encoded. Figure 11–9 shows the appearance of the data before and after the differential encoder.
h) The SQE Test sequence shall be generated after a successful data transmission by transmitting a collision enforcement RF signal with the timing shown in Figure 11–6.

Because the preamble of the incoming data on Circuit DO is modified, it is assumed that DTEs generate a minimum length preamble of 47 bits. The maximum preamble length is allowed to be 62 bits, as shown in Figure 11–6.

11.3.4.1.1 Scrambler and differential encoding requirements

The NRZ data shall be scrambled (using a CCITT V.29-type scrambler). A new seed shall be used by the scrambler for every new packet presented by the DTE to the MAU. Figure 11–10 is a diagram of a typical scrambler implementation.

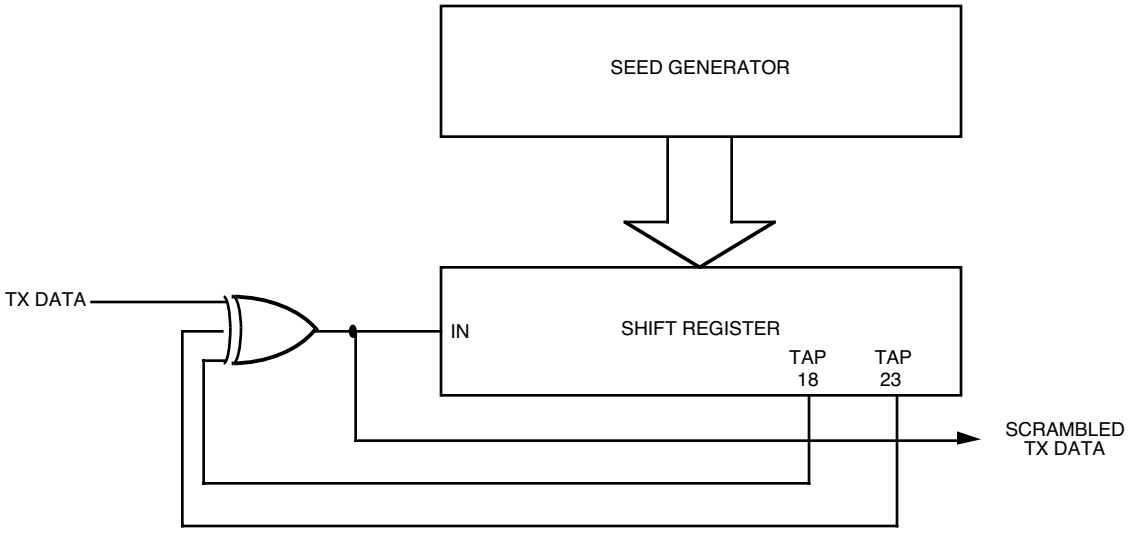


Figure 11–10—Scrambler

The scrambled NRZ data shall be differentially encoded (see Figure 11–11 for a typical implementation).

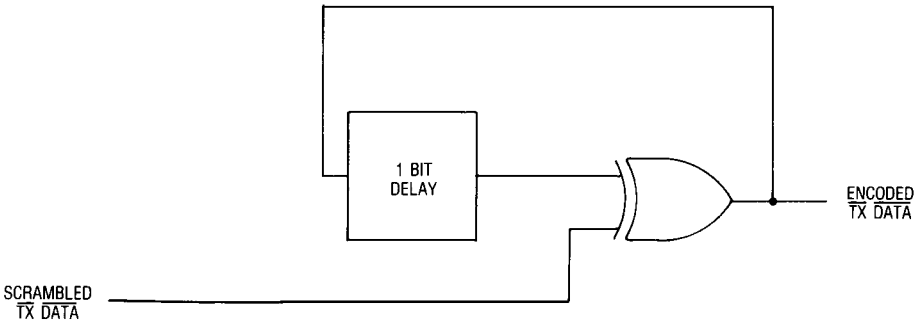


Figure 11–11—Differential encoder

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The entire encoding process comprising the scrambling and differential encoding is essentially equivalent to a division of the polynomial representing the data to be transmitted by the following polynomial:

$$G(x) = 1 + x^{-1} + x^{-18} + x^{-19} + x^{-23} + x^{-24}$$

11.3.4.2 Coaxial cable to AUI framing characteristics

The MAU shall demodulate, differentially decode, and invert the received RF data signal to recover the scrambled and inverted data stream. Clock shall be recovered and a replica of the unfiltered and noninverted transmitted data stream shall be created. The restored data shall be forced to a logic "one" state whenever no RF data signal is detected. This prevents false UMD detection and forces postamble detection when no carrier is present.

The framing information contained in the RF data stream shall be used to reconstruct the received data so that no more than 6 bits are lost and no more than one bit added to the preamble field, and no bits are added to or lost from the end of the transmit data. Detection of the UMD in the receive data shall initiate, after a fixed delay, a locally generated preamble sequence of zero-one pattern. This pattern "fills in" the preamble bits altered due to the framing information at the beginning of the packet: the zero-one synchronization and clock recovery sequence, the UMD, and the descrambler synchronization sequence.

The MAU shall descramble the received data using a self-synchronizing (CCITT V.29-type) descrambler. No prior knowledge of the seed used by the scrambler shall be assumed by the descrambler circuit. The descrambler shall have valid output no later than 23 bit intervals after the UMD is detected by the receiver. An example of a descrambler is shown in Figure 11–12. The differential decoding performed by the demodulator and the descrambling function are essentially equivalent to multiplying the received polynomial by G(x) as defined in the scrambling and differential encoding requirements subclause above.

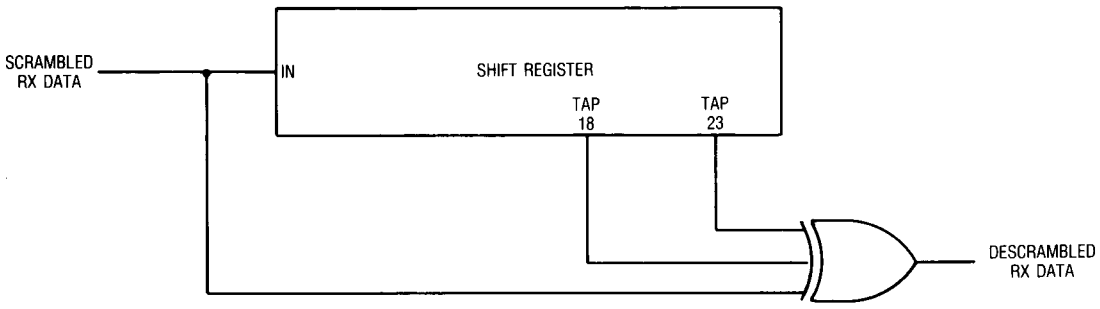


Figure 11–12—Descrambler

After the descrambler is synchronized, 23 bits after the UMD, the correctly descrambled receive data, starting with the 24th bit after the UMD, shall be transferred to the Manchester encoder and therefrom to the AUI. The delay from the detection of the UMD to the beginning of the locally generated zero-one pattern shall be chosen so that no more than 6 bits of preamble are lost, and no more than one bit added, in transmission from Circuit DO to Circuit DI.

The MAU shall detect the "zero" followed by 22 "ones" (the postamble pattern) and, in conjunction with the loss of carrier detection in the data band or the presence of a collision enforcement detection signal, shall ensure that the packet presented to the local DTE has no extraneous bits added by the MAU to the end of the packet.

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The SQE Test signal shall be detected on the RF interface and the SQE signal shall be presented to Circuit CI of the transmitting MAU, subject to the timing restrictions of 11.3.4.5.4. If the signal is not observed at the RF interface due to failure of any element in the transmitter or receiver, no SQE signal may be presented to the AUI. In the event of a collision enforcement, energy will appear in the collision enforcement band within the ced_window time after energy first appears in the data band. Circuit CI shall be asserted when collision enforcement is first detected and shall continue to be active until after the RF signal on the RF port has subsided. Note that an SQE Test signal appended to a packet whose length is less than the ced_window time (less than the minimum allowed packet length) will be indistinguishable from a collision enforcement, except by the MAU transmitting. The transmitting MAU shall take this into account and shall not interpret energy in the collision enforcement band to be a collision when the length of the transmitted packet is less than the ced_window time and the SQE Test sequence has been transmitted. See the discussion in 11.4.2 for more information on ced_window.

11.3.4.3 Circuit DO to circuit DI framing characteristics

In the absence of a collision, the packet format of the receive data at the AUI is identical to that of the transmit data, except that there may be one more preamble bit than was sent at the transmit port and up to 6 bits of the preamble lost. In the presence of a collision, the receive data is undefined, but shall still be properly Manchester encoded.

11.3.4.4 AUI to coaxial cable delay characteristics

The timing and delays associated with the transmitter of the MAU are identified below. To ensure compatibility with all MAUs the delays identified below cannot be exceeded nor traded off with other delays in the system.

11.3.4.4.1 Circuit DO to RF data signal delay

The delay from a transition on Circuit DO at the end of a bit to the corresponding phase change of the RF data signal (such bit chosen so that an RF burst phase change does exist) shall be no more than 24 bit times. The delay from the first transition on Circuit DO to the first appearance of RF energy, however, is not specified except as it is determined by other timing constraints.

11.3.4.4.2 Circuit DO to CE RF output delay

In the event that the MAU begins receiving energy on the coaxial medium just before the DTE presents data to the AUI, a collision shall be detected locally, as described in Figure 11–4. The delay from the first bit at Circuit DO of the AUI to the presentation of collision enforcement at the coaxial cable interface in this circumstance shall be 32 bit times maximum.

11.3.4.4.3 Transmit postamble to SQE test signal delay

The delay from the initial transition of the first bit of the postamble (Broadband End of Frame Delimiter) measured at the RF port to the 50% point of the rising edge of the SQE Test signal shall be 35 ± 3 bit times.

11.3.4.4.4 SQE test signal length

The SQE Test signal length shall be 30 ± 1 bit times as measured at the 50% points of the RF signal.

11.3.4.5 Coaxial cable to AUI delay characteristics

The MAU receiver timing and delays described below shall not be exceeded or traded off against any other delays in the system.

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11.3.4.5.1 Received RF to circuit DI delay

When there is no collision in progress, the delay from the end of the SFD in the received RF data signal at the coaxial cable interface to the end of the SFD on Circuit DI, shall be a maximum of 75 bit times (see Figure 11–13). The minimum is not specified, nor is the delay specified at other locations in the packet. The end of the SFD in the received RF data signal (at the coaxial cable interface) is defined as the time at which the envelope of the carrier would pass through the midpoint if the first bit following the SFD was a zero and the scrambler disabled.

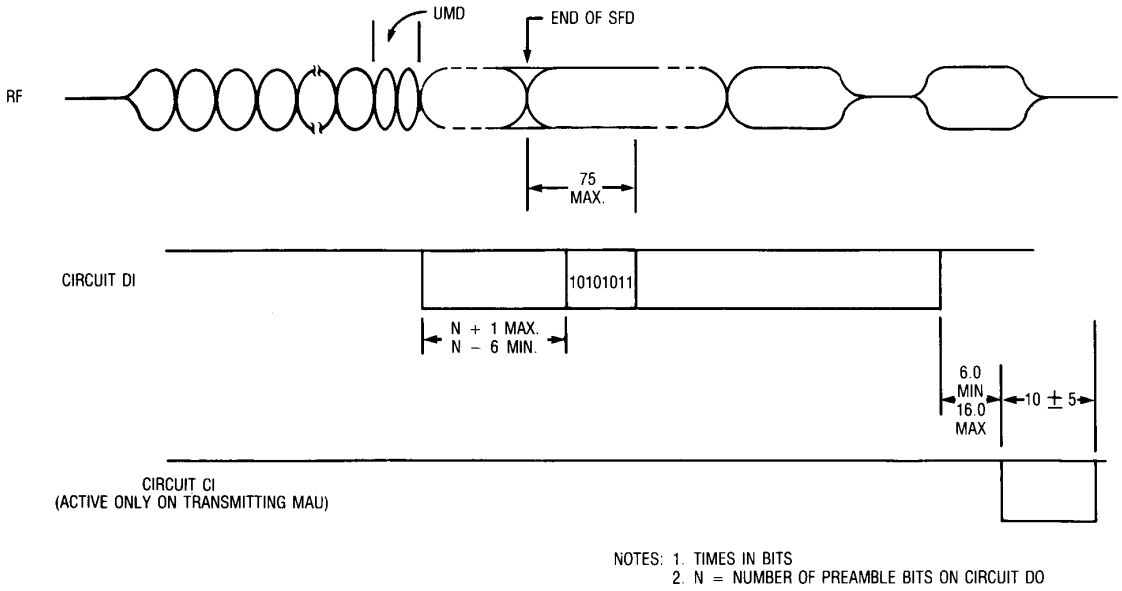


Figure 11–13—No collision timing diagram (coax to AUI)

11.3.4.5.2 Received RF to CE RF output and circuit CI delay

In the event that a collision is detected via the bit-by-bit comparison, the delay from the end of the bit in which the collision was detected, as represented by the RF signal, to the 50% point on the rising edge of the collision enforcement signal shall not exceed 34 bit times. The delay from the same point to the first transition of Circuit CI shall not exceed 27 bit times. Circuit CI shall cease activity no more than 31 bit times after activity on the RF interface (in both data channel and collision enforcement channel) ceases. See Figure 11–14 and Figure 11–15.

11.3.4.5.3 Collision enforcement to circuit CI delay

In the event of a collision enforcement by another MAU, the delay from the 50% point on the rising edge of the RF collision enforcement signal to the first transition of Circuit CI shall be no more than 31 bit times. Circuit CI shall be active for a minimum of 5 bit times and shall become inactive within 31 bit times of the cessation of activity on the RF coaxial cable interface, as shown in Figure 11–15.

11.3.4.5.4 Receive data to SQE test delay

If a collision enforcement signal is received after the ced_window signal becomes inactive (see i) in 11.2.3.2), or if the MAU has transmitted an SQE Test sequence, the MAU is to interpret the collision enforcement signal as an SQE Test signal. If the SQE Test sequence is correctly detected (that is, the test passes), then the delay from the last transition of Circuit DI to the first transition of Circuit CI shall be at

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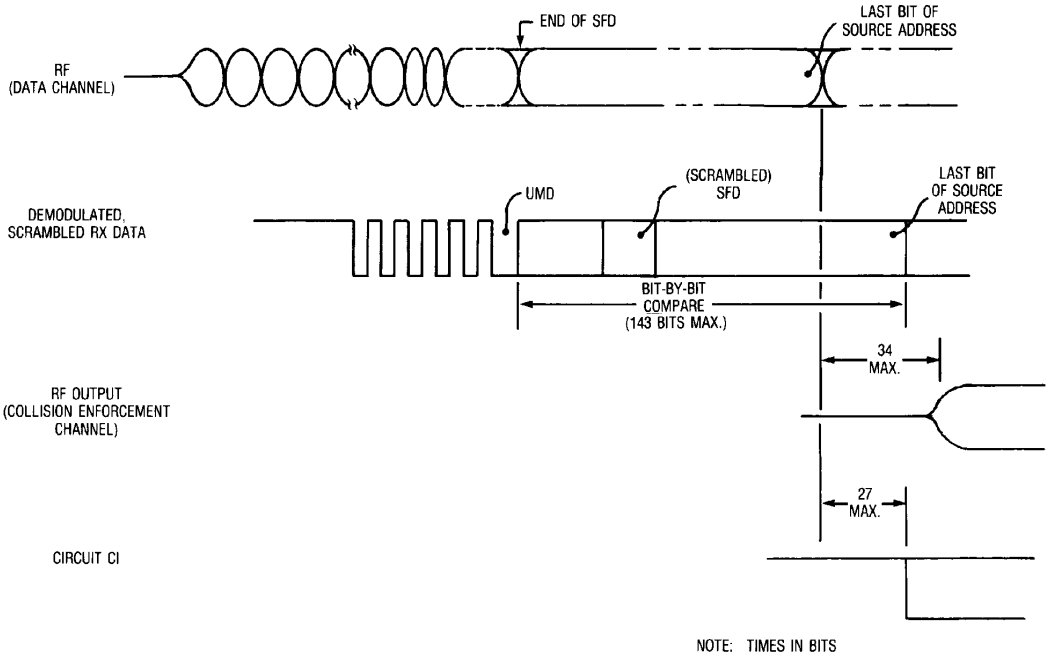


Figure 11–14—Collision timing diagram (RF data to RF collision enforcement)

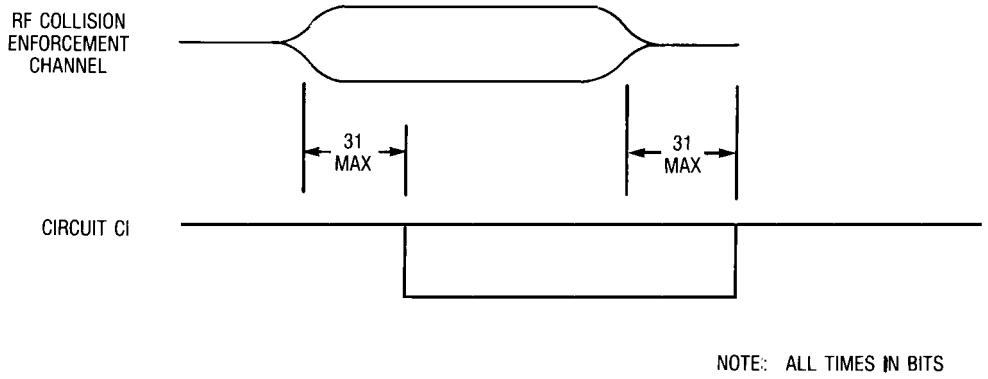


Figure 11–15—Collision timing diagram (coaxial cable interface to AUI circuit)

least 6 but not more than 16 bit times. Circuit CI shall remain active for 10 ± 5 bit times. Only the transmitting MAU shall assert its Circuit CI as a result of successful completion of the SQE Test sequence.

If a collision enforcement signal is received before the ced_window signal becomes inactive, the MAU shall interpret it as a collision enforcement and the timing of 11.3.4.5.3 shall apply.

11.3.4.6 Delay from circuit DO to circuit DI

The time delay from a bit on Circuit DO at the AU Interface to the corresponding bit on Circuit DI at the AU Interface is equal to the round trip delay of the MAU connected back-to-back with itself (that is, in RF loopback) plus the round trip delay through the cable system at the location of the MAU. Therefore, the delay is a function of the location of the MAU on the cable system. It is never less than the transmitter delay plus the postamble length plus the time to detect loss of carrier or presence of the SQE Test signal. See Figure 11–16 for the timing relationship when the cable has zero length.

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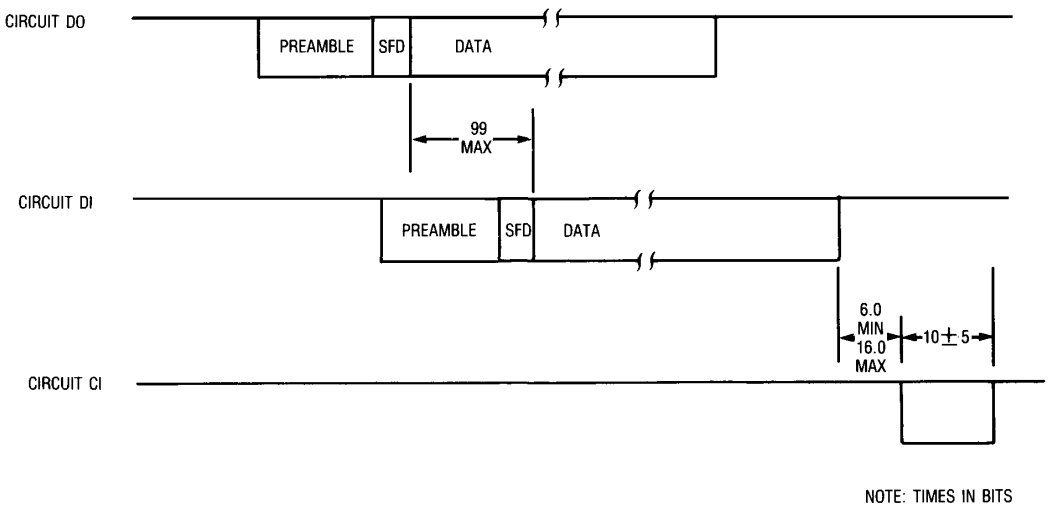


Figure 11–16—Timing at AUI for zero-length coax

When the MAU is transmitting a short packet (less than 576 bits), the timing for Circuit CI during the SQE Test sequence shall be the same as it is for normal length packets. If the MAU transmits a short packet (less than 576 bits) that encounters a collision and if the SQE Test sequence has not been transmitted when the collision is detected by the MAU, then the timing for Circuit CI shall be the same as it is for any normal collision.

11.3.4.7 Interpacket gap requirement

The MAU shall be able and ready to transmit data presented to it by the DTE no later than 90 bit times after the last bit of a received packet was presented by the MAU at its AUI.

11.3.4.8 Bit error rate

The MAU shall have a Bit Error Rate (BER) as measured at the AUI lower than one error in 10^8 in a "zero-length coax" test environment (that is, a coaxial cable connection sufficiently short to have negligible delay and transmission impairments). It shall have this BER for receive signal levels in the range specified in 11.3.1.1.3 and in the presence of –28.3 dBmV rms/14 MHz white Gaussian noise. This represents a 24.3 dB signal-to-noise ratio for the specified minimum signal level, –4 dBmV rms. For the same BER in a "system" environment (as opposed to zero-length coax), a 26 dB signal-to-noise ratio is required.

The MAU shall meet the BER requirements specified above when receiving strings of up to 33 consecutive identical bits.

11.3.5 Reliability

Component failures within the MAU electronics should not impede communication among other MAUs on the broadband coaxial cable. Connectors and other passive components comprising the means of connecting the MAU to the coaxial cable shall be designed to minimize the probability of total network failure. The MAU shall be designed to provide an MTBF of at least 1 000 000 hours without causing communication failure among other stations attached to the broadband local network medium.

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11.4 System considerations

11.4.1 Delay budget and network diameter

The delay budget for the broadband MAU and rest of the Physical Layer is tabulated in Table 11–3. This table includes allocations for trunk cables (the backbone cables in the system), drop cables (a length of 25 m is assumed), etc. The velocities of propagation assumed are included in the table; use of other types of cables will alter the system diameter accordingly. The types of cables, including the mix of drop and trunk cable lengths, can be altered as long as the total propagation delay from the most distant MAU to the headend does not exceed 70 bit times. The total delay budget of 576 bit times includes allowance for the preamble and SFD (64 bits).

Table 11–3 tabulates delay allocations for a dual-cable system with no headend delay. In translated single-cable systems, the headend translator delay reduces the maximum trunk cable distance by [D/(2 × CV)], where D is the delay in nanoseconds, and CV is the cable velocity in nanoseconds per meter. For 3.83 ns/m velocity trunk cable, this reduction is [Delay (ns) / 7.66] m.

Table 11–3—Broadband dual-cable systems—Physical Layer delay budget

Delay element	Maximum allowed value (bits)
DTE1 starts to put out first bit	0.00
First bit from DTE1 at AUI	3.00
AUI cable (50 m at 5.13 ns/m)	2.57
Circuit DO to Tx RF out	24.00
Tx drop cable (25 m at 4.27 ns/m)	1.05
Tx trunk cable (1800 m at 3.83 ns/m)	68.95
Rx trunk cable (25 m at 4.27 ns/m)	68.95
Rx drop cable (25 m at 4.27 ns/m)	1.05
End of bit comparison (last bit of source address)	160.00
Rx RF to collision enforcement RF out (from RX bit that is found to be in error to collision enforcement out)	34.00
Tx drop cable (25 m at 4.27 ns/m)	1.05
Tx trunk cable (1800 m at 3.83 ns/m)	68.95
Rx trunk cable (1800 m at 3.83 ns/m)	68.95
Rx drop cable (25 m at 4.27 ns/m)	1.05
Rx collision enforcement to circuit Ci	31.00
AUI cable (50 m at 5.13 ns/m)	2.57
DTE1 detects collision presence	3.00
DTE1 jams channel	32.00
Allowance for traps, splitters, amplifiers, and margin	3.86
Total	576.00

11.4.2 MAU operation with packets shorter than 512 bits

The MAU transmits an SQE Test sequence onto the RF medium after every transmitted packet. If the frame plus preamble and SFD is less than the ced_window in length, a receiving MAU cannot distinguish the SQE

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Test signal from a collision enforcement signal due to a collision. Therefore, operation of the MAU with data frames shorter than 512 bits may cause all other receiving MAUs to see a collision. The transmitting MAU, however, recognizes the SQE Test because that MAU was the one that transmitted the test. An MAU transmitting a short packet that encounters a collision can distinguish the resulting collision enforcement from an SQE Test signal by the fact that the transmitting MAU will not have transmitted the SQE Test sequence unless the packet is shorter than the round trip delay on the cable plant. In the latter instance, the transmitting MAU may not detect a collision enforcement.

11.5 Characteristics of the coaxial cable system

The cable system upon which the broadband MAU operates shall meet the following electrical and mechanical requirements.

11.5.1 Electrical requirements

The electrical requirements of the cable system are listed in Table 11–4. Each parameter is applicable over the frequency range to be used by the broadband MAU.

Table 11–4—Cable system electrical requirements

Impedance	75 Ω
Return loss	14 dB min
Transmit level	+50 dBmV ±2 dB
Receive level	+6 dBmV ±10 dB
Maximum receive noise level	–30 dBmV/14 MHz
Loss variation[a] (per 18 MHz band)	2 dB min, 52 dB max
Path loss (between any transmit port and receive port, including loss variation)	36 dB min, 52 dB max
Group delay variation —around data carrier —over 18 MHz band	 20 ns/10 MHz max 34 ns max

[a]Not including headend.

Adjacent channel signal levels shall be consistent with the requirements of 11.3.1.1.4.

11.5.2 Mechanical requirements

The connection of the cable system to the broadband MAU is via a standard F-series screw-on male connector. For the dual-cable case, two such connectors are required: one for transmit and the other for receive.

11.5.3 Delay requirements

The maximum length of the cable system is constrained by the allowable round trip delay from the farthest transmitting MAU to the farthest receiving MAU. Table 11–3 allows 140 bit times round trip delay in the cable system. For trunk cable propagation velocity of 3.83 ns/m, this allows 3600 m of trunk cable (round trip; 1800 m from the farthest point to the headend), and 25 m of 4.27 ns/m velocity drop cable at each MAU. In addition, 50 m of AUI cable is allowed on each MAU, therefore allowing, in this case, a maximum

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of 3750 m DTE to DTE separation. These lengths will be different if cables of different propagation velocity are used. This is acceptable so long as the maximum delay is not exceeded.

For single-cable systems, the maximum delay of 140 bit times includes the delay through the headend. The maximum cable system length must be reduced appropriately, as described in 11.4.1.

11.6 Frequency translator requirements for the single-cable version

11.6.1 Electrical requirements

The headend frequency translator performance is included in the cable system characteristics specified in 11.5, except as defined in Table 11–5.

Table 11–5—Frequency translator requirements

Group delay variation —around data carrier frequency —between data carrier and CE center frequency	 20 ns/10 MHz max 50 ns max
Amplitude variation (from 6 MHz below the input data carrier frequency to 1 MHz above the CE center frequency)	2 dB max
Translation frequency	per Table 11–1

The frequency translator contributes to total cable system delay and shall be labeled by the vendor with the input-to-output delay in the band of operation. The effect on network length can then be computed per 11.4.1.

11.6.2 Mechanical requirements

The input and output mechanical interface shall be 75 Ω female F-series coaxial connectors. The connection to the broadband medium shall be through a coaxial cable with a mating male F-series connector.

11.7 Environmental specifications

11.7.1 Safety requirements

This subclause sets forth a number of recommendations and guidelines related to safety concerns. This list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to assure compliance with the appropriate standards.

LAN cable systems, as described in this clause, are subject to at least four direct electrical safety hazards during their use, and designers of connecting equipment should be aware of these hazards. The hazards are as follows:

a) Direct contact between local network components and power or lighting circuits
b) Static charge buildup on local network cables and components
c) High-energy transients coupled onto the local network cabling system
d) Potential differences between safety grounds to which various network components are connected

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These electrical safety hazards, to which all similar cabling systems are subject, should be alleviated for a local network to perform properly. In addition to provisions for properly handling these faults in an operational system, special measures shall be taken to ensure that the intended safety features are not negated when attaching or detaching equipment from the LAN medium of an existing network.

Sound installation practice, as defined in applicable national and local codes and regulations, shall be followed in every instance in which such practice is applicable.

11.7.2 Electromagnetic environment

11.7.2.1 Susceptibility levels

Sources of interference from the environment include electromagnetic fields, electrostatic discharge, transient voltages between earth connections, etc.

The physical MAU hardware shall meet its specifications when operating in an ambient plane wave field of:

a) 2 V/m from 10 kHz through 30 MHz
b) 5 V/m from 30 MHz through 1 GHz

MAUs meeting this clause should provide adequate RF ground return to satisfy the EMC specification.

11.7.2.2 Emission levels

The physical MAU hardware shall comply with the applicable national and local regulations for emission levels.

11.7.3 Temperature and humidity

The MAU and associated cable system are expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling such as shock and vibration. Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

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12. Physical signaling, medium attachment, and baseband medium specifications, type 1BASE5

NOTE—This MAU is not recommended for new installations.

12.1 Introduction

12.1.1 Overview

1BASE5 is a 1 Mb/s CSMA/CD network based on twisted-pair wiring. Each DTE (Data Terminal Equipment) is star-connected to a shared hub through two pairs that function as transmit and receive channels. Hubs can be cascaded, and DTEs can be connected to any hub. Packets transmitted by a DTE are propagated by the hub to a higher-level hub if one exists; otherwise the hub broadcasts the packet back down to all DTEs and lower-level hubs. Packets received by a hub from a higher-level hub are retransmitted to all attached DTEs and lower-level hubs. If two or more DTEs or lower-level hubs transmit concurrently, the hub generates a collision-presence signal that the DTEs detect as a collision. Hubs between a transmitting DTE and the header (highest level) hub propagate data or the collision-presence signal to the header hub; this hub in turn broadcasts the packet or collision signal to all DTEs and lower-level hubs.

12.1.2 Scope

The 1BASE5 specification builds upon the first six major clauses of this standard; the remaining major clauses (other than this one, of course) do not apply to 1BASE5. That is, the Media Access Control (MAC) and Physical Signaling (PLS) Service Specifications are used in common with the other implementations of this standard, but the Physical Medium Attachment (PMA) sublayer, transmission medium, and hub functions for type 1BASE5 are specified in this clause. The relationship of the 1BASE5 specification to the OSI reference model and the IEEE 802.3 CSMA/CD LAN model is shown in Figure 12–1.

12.1.3 Definitions

See 1.4.

12.1.4 General characteristics

Type 1BASE5 has the following general characteristics:

a) 1 Mb/s signaling rate, Manchester encoded
b) Twisted-pair wiring
c) Point-to-point interconnection of DTEs to hubs, with one twisted-pair serving as the upward link, the other as the downward link
d) Data pairs can coexist in the same telephone cable bundles as voice pairs
e) When a hub receives signals from a DTE or lower-level hub, it propagates them to a higher-level hub if one exists; otherwise, the hub broadcasts the signals back down to the DTEs and lower-level hubs
f) When a hub receives signals concurrently from two or more DTEs or lower-level hubs, it generates a unique collision presence signal, and distributes it as in item e) above
g) DTE-to-hub and hub-to-hub interfaces are electrically isolated at both ends
h) Up to five hub levels are allowed
i) Hubs serve as repeaters
j) Maximum DTE-to-hub and hub-to-hub distance is approximately 250 m for telephone wiring (cable-type dependent; see 12.7)
k) Special links may be used to extend some DTE-to-hub or hub-to-hub distances to 4 km

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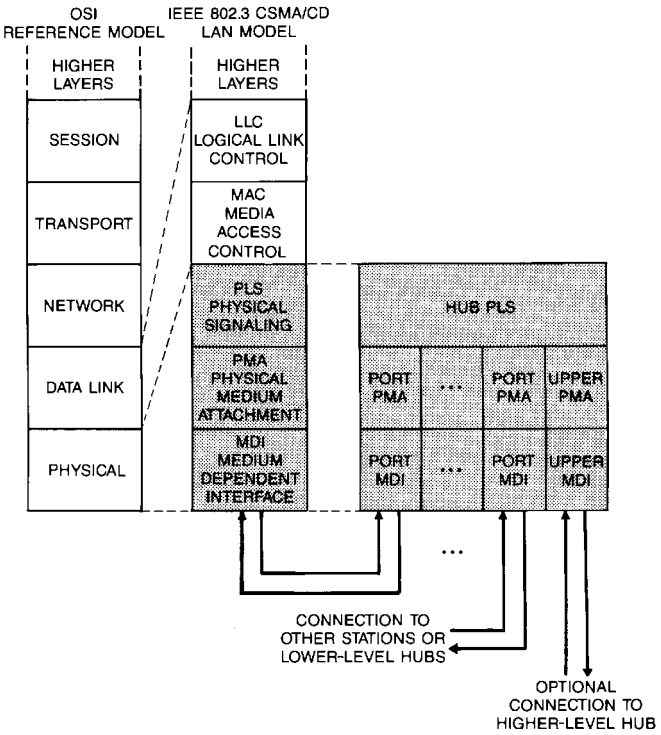


Figure 12–1—1BASE5 relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

12.1.5 Compatibility

This specification calls out one principal compatibility interface, namely PMA-to-Medium. It is intended that different implementations of DTEs and hubs be able to interoperate in 1BASE5 networks.

12.1.6 Objectives of type 1BASE5 specification

a) Provide for low-cost networks, as related to both equipment and cabling
b) Make it possible to use telephone-type building wiring, and in particular spare wiring when available
c) Provide for easy installability, reconfigurability, and service
d) Ensure interconnectability of independently developed DTEs and hubs
e) Ensure fairness of DTE access
f) Provide a communication channel with a resultant mean bit error rate, at the physical layer service interface, of less than one part in 10^8 (on the order of one part in 10^9 at the link level)

12.2 Architecture

12.2.1 Major concepts

Type 1BASE5 is a 1 Mb/s CSMA/CD network. DTEs are connected to hubs (and hubs to other hubs) by point-to-point wiring, resulting in a star topology network. Data transmissions are Manchester encoded.

An elementary configuration is illustrated in Figure 12–2. In this instance, each DTE is connected to the hub via separate transmit and receive channels (normally two twisted pairs). The hub serves as the point of con-

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centration and performs two major functions: signal regeneration/retiming (repeating) and collision detection. When only one DTE transmits, the hub repeats the signals, compensating for amplitude and phase distortion, and broadcasts to all DTEs. When a hub detects two or more DTEs transmitting concurrently, the hub generates a unique Collision Presence (CP) signal, which it broadcasts instead of the originally transmitted signals. The hub continues to send CP until it receives IDL from all lower-level DTEs. CP has the property that it can be detected by DTEs as a Manchester code violation.

The interconnection architecture does not imply any minimum, typical, or maximum number of DTEs to be connected to a given hub; this is an implementation or installation detail.

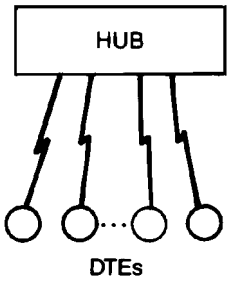


Figure 12–2—Single hub network

Up to five levels of hubs may be cascaded. A two-level configuration is illustrated in Figure 12–3, with a header hub (HH) and intermediate hubs (IH). There can be a number of IHs; there must be one and only one HH. Each DTE or IH is connected to a hub via separate transmit and receive channels (normally two twisted pairs). An IH propagates signals from its DTEs toward the HH; it sends CP toward the HH in the event of a collision. The HH repeats the signals it receives from DTEs or IHs back down to all DTEs and IHs. The HH generates CP if more than one of its inputs becomes active. The IHs repeat the signals received from the HH, and broadcast to all the connected DTEs' receivers. Hubs do not distinguish whether input signals along the upward path emanate from DTEs or lower-level IHs. If a single input is active, the hub repeats the signal regardless of its source; if more than one is active, it generates CP.

A configuration involving four hub levels and a special link is illustrated in Figure 12–4. In this example, one IH is used for simple repeating (one connection upward and one connection downward). Other than having one link in and one link out, repeaters are identical to other hubs. Special links are connections, possibly containing active devices, that are used for situations requiring extra propagation delay or special transmission media.

12.2.2 Application perspective

The primary application area for type 1BASE5 is expected to be in office environments for networking DTEs such as personal computers or other workstations. In many cases, spare wiring contained in existing telephone wire bundles will be used.

12.2.3 Packet structure

Packets are transmitted from the PLS to the PMA as follows:

<silence> <preamble> <sfd> <data> <etd> <silence>

The packet elements shall have the following characteristics:

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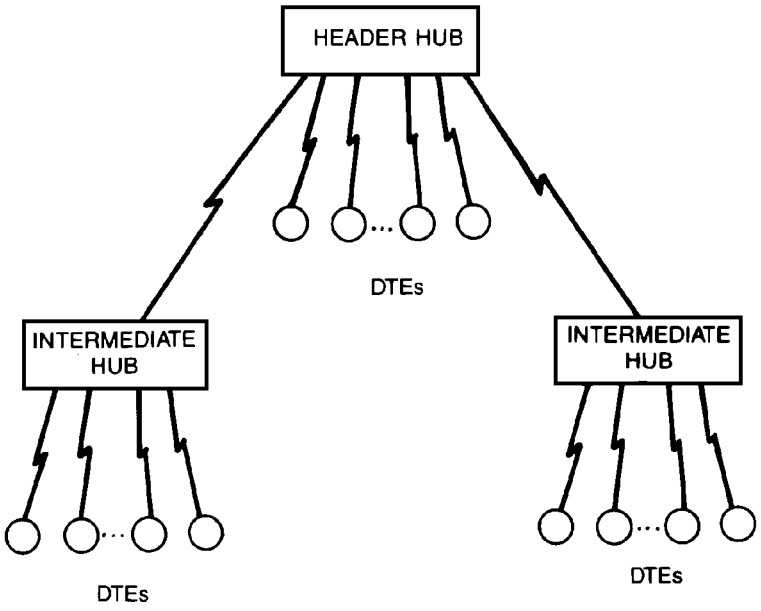


Figure 12–3—Network with two levels of hubs

Element	Characteristics
<silence>	No transitions
<preamble>	Alternating CD1 and CD0 for ≥56 bit times (ending in CD0)
<sfd>	CD1 CD0 CD1 CD0 CD1 CD0 CD1 CD1
<data>	8 × N instances of CD0 or CD1
<etd>	First part of IDL

12.2.3.1 Silence

The <silence> delimiter provides an observation window for an unspecified period of time during which no transitions occur. The minimum duration of <etd> followed by <silence> is the interFrameGap defined in 4.4.2.2.

12.2.3.2 Preamble

The <preamble> delimiter begins a packet transmission and provides a signal for receiver synchronization. The signal shall be an alternating pattern of CD1 and CD0. This pattern shall be transmitted by the DTE for a minimum of 56 bit times at the beginning of each packet. The last bit of the preamble (that is, the final bit of preamble before the start-of-frame delimiter) shall be a CD0.

The DTE is required to supply at least 56 bits of preamble in order to satisfy system requirements. System components consume preamble bits in order to perform their functions. The number of preamble bits sourced ensures an adequate number of bits are provided to each system component to correctly implement its function.

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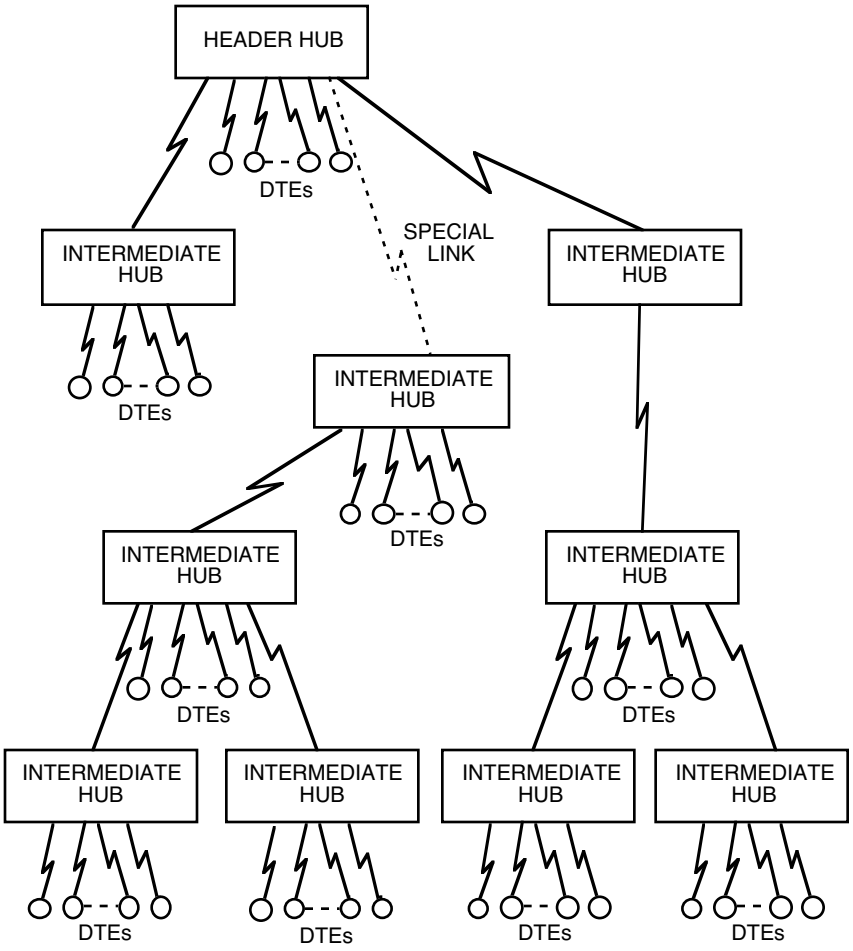


Figure 12–4—Network with four levels of hubs

12.2.3.3 Start-of-frame delimiter

The <sfd> indicates the start of a frame, and follows the preamble.

12.2.3.4 Data

The <data> in a transmission shall be in multiples of eight (8) encoded data bits (CD0s and CD1s).

12.2.3.5 End-of-transmission delimiter

The <etd> indicates the end of a transmission and serves to turn off the transmitter. The signal shall be the first part of an IDL.

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12.3 DTE physical signaling (PLS) specification

12.3.1 Overview

This subclause defines logical characteristics of the DTE PLS sublayer for IBASE5. The relationship of this specification to the entire standard is shown in Figure 12–5. The sublayer and its relationship to the MAC and PMA sublayers are described in an abstract way and do not imply any particular implementation.

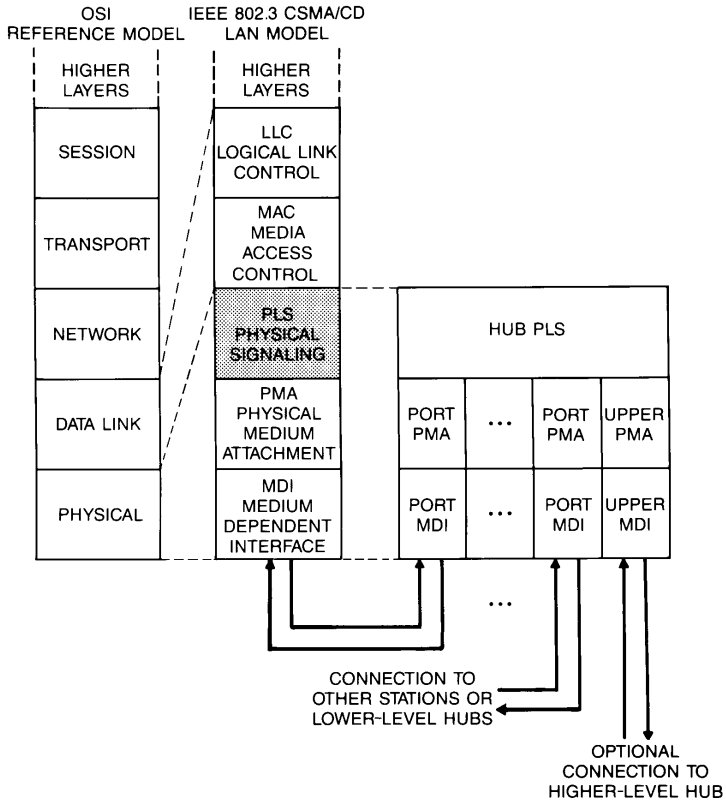


Figure 12–5—Station physical signaling, relationship to the ISO OSI reference model and the IEEE 802.3 CSMA/CD LAN model

12.3.1.1 Summary of major concepts

a) There are two channels between the PLS and PMA sublayers. Output data are passed through the output channel and input data and control (CP) are passed through the input channel.
b) Each direction of data transfer through the PLS operates independently and simultaneously (that is, the PLS is full duplex).

12.3.1.2 Application perspective

The DTE PLS sublayer performs the following functions:

a) Encodes OUTPUT_UNITs from the MAC sublayer into a Manchester encoded waveform that it sends to the PMA sublayer output circuit
b) Decodes a Manchester encoded waveform from the PMA sublayer input circuit into INPUT_ UNITS, CARRIER_STATUS, and SIGNAL_STATUS

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12.3.2 Functional specification

This subclause provides a detailed model for the DTE PLS sublayer.

Many of the terms used in this subclause are specific to the interface between this sublayer and the MAC sublayer. These terms are defined in the service specification for the PLS sublayer (see 6.3).

12.3.2.1 PLS-PMA interface

The PLS and PMA communicate by means of the following messages:

Message	Meaning	Source
output	Output information	PLS
output_idle	No data to be output	PLS
input	Input information	PMA
input_idle	No input information	PMA

12.3.2.1.1 *output* message

The PLS sublayer sends an *output* message to the PMA sublayer when the PLS sublayer receives an OUTPUT_UNIT from the MAC sublayer.

The physical realization of the *output* message is a CD0 or a CD1 sent by the PLS to the PMA. The PLS sends a CD0 if the OUTPUT_UNIT is a ZERO or a CD1 if the OUTPUT_UNIT is a ONE. This message is time-coded. That is, once this message has been sent, the function is not completed until one bit time later. The *output* message cannot be sent again until the bit cell being sent as a result of sending the previous *output* message is complete.

12.3.2.1.2 *output_idle* message

The PLS sublayer sends an *output_idle* message to the PMA sublayer at all times when the MAC sublayer is not in the process of transferring output data across the MAC to PLS interface. The *output_idle* message is no longer sent (and the first OUTPUT_UNIT is sent using the *output* message) when the first OUTPUT_UNIT of a packet is received from the MAC sublayer. The *output_idle* message is again sent to the PMA when DATA_COMPLETE is received from the MAC sublayer.

The physical realization of the *output_idle* message is IDL sent by the PLS to the PMA.

12.3.2.1.3 *input* message

The PMA sublayer sends an *input* message to the PLS sublayer when the PMA has received a bit from the medium and is prepared to transfer this bit to the PLS.

The physical realization of the *input* message consists of data units, CD0, CD1, CVL, or CVH, derived from the incoming data stream. If ambiguity exists due to excessive noise or jitter, the PMA may send an arbitrary combination of these.

12.3.2.1.4 *input_idle* message

The PMA sublayer sends an *input_idle* message to the PLS sublayer when the PMA sublayer does not have data to send to the PLS sublayer. This condition exists when carrier is lost or IDL is received.

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12.3.2.2 PLS-MAC interface

The PLS and MAC communicate by means of the following messages:

Message	Meaning	Source
OUTPUT_UNIT	Data sent to the PMA	MAC
OUTPUT_STATUS	Response to OUTPUT_UNIT	PLS
INPUT_UNIT	Data received from the PMA	PLS
CARRIER_STATUS	Indication of input activity	PLS
SIGNAL_STATUS	Indication of error/no error condition	PLS

12.3.2.2.1 OUTPUT_UNIT

The MAC sublayer sends the PLS sublayer an OUTPUT_UNIT every time the MAC sublayer has a bit to send. Once the MAC sublayer has sent an OUTPUT_UNIT to the PLS sublayer, it may not send another OUTPUT_UNIT until it has received an OUTPUT_STATUS message from the PLS sublayer. The OUTPUT_ UNIT is a ONE if the MAC sublayer wants the PLS sublayer to send a CD1 to the PMA sublayer, a ZERO if a CD0 is desired, or a DATA_COMPLETE if an IDL is desired.

12.3.2.2.2 OUTPUT_STATUS

The PLS sublayer sends the MAC sublayer an OUTPUT_STATUS in response to every OUTPUT_UNIT received by the PLS sublayer. OUTPUT_STATUS sent is an OUTPUT_NEXT when the PLS sublayer is ready to accept the next OUTPUT_UNIT from the MAC sublayer. (The purpose of OUTPUT_STATUS is to synchronize the MAC sublayer data output with the data rate of the physical medium.)

12.3.2.2.3 INPUT_UNIT

The PLS sublayer sends the MAC sublayer an INPUT_UNIT every time the PLS receives an *input* message from the PMA sublayer. The INPUT_UNIT is a ONE if the PLS sublayer receives a CD1 from the PMA sublayer or a ZERO if the PLS sublayer receives a CD0 from the PMA sublayer. The INPUT_UNIT may be either ZERO or ONE if the PLS sublayer receives a CVL or CVH from the PMA sublayer.

12.3.2.2.4 CARRIER_STATUS

The PLS sublayer sends the MAC sublayer_CARRIER_STATUS whenever there is a change in carrier status, as detected by the PMA. The PLS sublayer sends CARRIER_ON when it receives an *input* message from the PMA and the previous CARRIER_STATUS that the PLS sublayer sent to the MAC sublayer was CARRIER_OFF. The PLS sublayer sends CARRIER_OFF when it receives an *input_idle* message from the PMA sublayer, and the previous CARRIER_STATUS that the PLS sublayer sent to the MAC sublayer was CARRIER_ON.

12.3.2.2.5 SIGNAL_STATUS

The PLS sublayer sends the MAC sublayer SIGNAL_STATUS whenever it detects the beginning or end of Collision Presence. The PLS sublayer sends SIGNAL_ERROR when it receives *input* message CVL or CVH from the PMA sublayer and the previous SIGNAL_STATUS the PLS sublayer sent was NO_SIGNAL_ERROR. The PLS sublayer sends NO_SIGNAL_ERROR when it receives an *input_idle* message from the PMA sublayer and the previous SIGNAL_STATUS that the PLS sent to the MAC sublayer was SIGNAL_ERROR. The PLS shall send SIGNAL_ERROR to the MAC sublayer when the Collision

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Presence pattern is detected; it may send SIGNAL_ERROR any time it receives an *input* message that is neither CD0 nor CD1.

12.3.2.3 PLS functions

The PLS sublayer functions consist of four simultaneous and asynchronous functions. These functions are Output, Input, Error Sense, and Carrier Sense. All of the four functions are started immediately following PowerOn. These functions are depicted in the state diagrams shown in Figure 12–6 through Figure 12–9, using the notation described in 1.2.1.

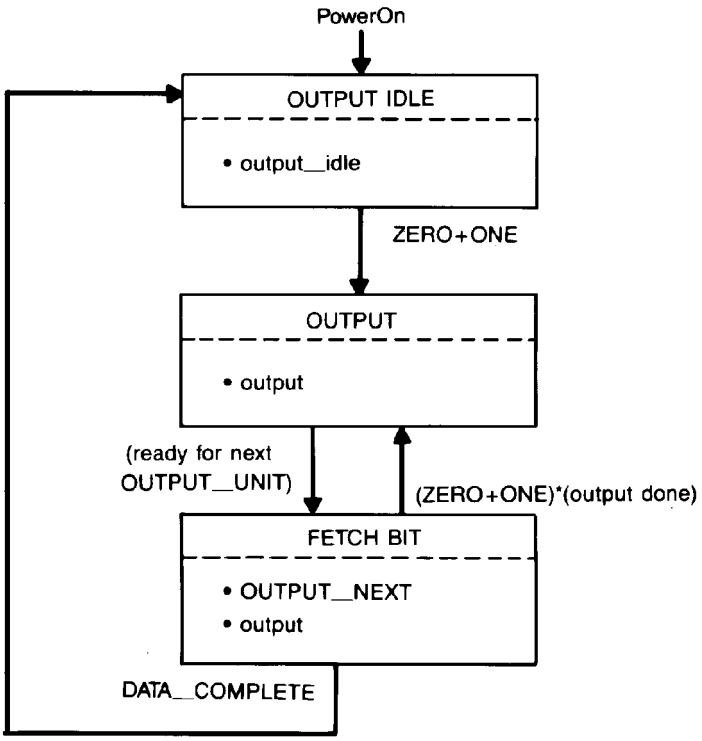


Figure 12–6—DTE PLS Output function

12.3.2.3.1 State diagram variables

The variables used in the state diagrams and the corresponding descriptions are the following:

a) Inter Process Flags

disable_SIGNAL_ERRORUsed in the state diagrams and functions. It is used by the Input function to prevent false collision detection by the Error Sense function during preamble startup.

protectTimer Used by the Carrier Sense function to implement the protection period described in 12.5.3.2.3. It is started by "start-protectTimer." "protectTimer_done" is satisfied when the timer has expired.

12.3.2.3.2 Output function

The Output function transparently performs the task of data transfer from the MAC sublayer to the PMA sublayer. The state diagram of Figure 12–6 depicts the Output function operation.

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12.3.2.3.3 Input function

The Input function transparently performs the task of data transfer from the PMA sublayer to the MAC sublayer. The state diagram of Figure 12–7 depicts the Input function operation.

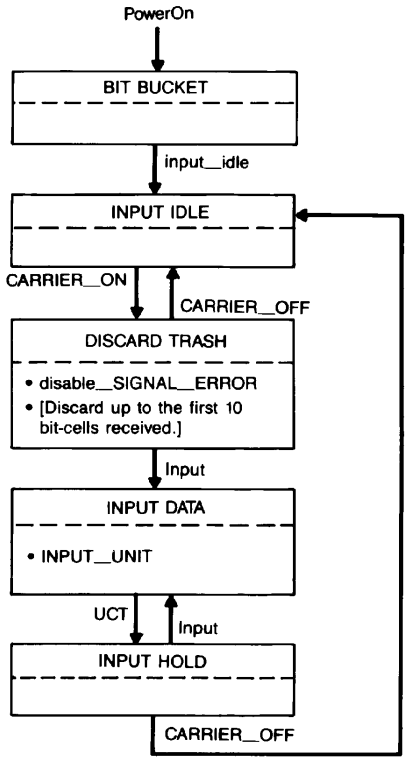


Figure 12–7—DTE PLS Input function

12.3.2.3.4 Error Sense function

The Error Sense function performs the task of sending SIGNAL_STATUS to the MAC sublayer at the beginning and end of the Collision Presence pattern. The state diagram of Figure 12–8 depicts the Error Sense function operation.

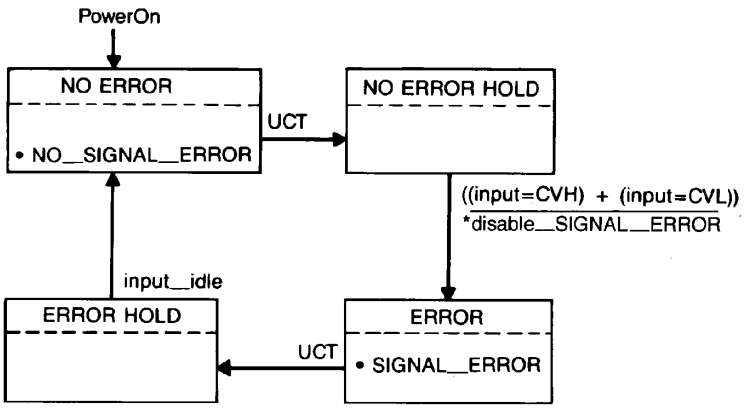


Figure 12–8—DTE PLS Error Sense function

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12.3.2.3.5 Carrier Sense function

The Carrier Sense function performs the task of sending CARRIER_STATUS to the MAC sublayer whenever the input becomes active or idle, as detected by the PMA sublayer. The state diagram of Figure 12–9 depicts the Carrier Sense function operation.

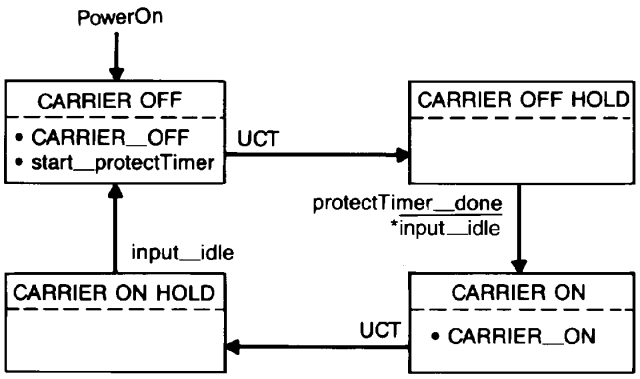


Figure 12–9—DTE PLS Carrier Sense function

A timer may be used by the Carrier Sense function to implement the protection period described in 12.5.3.2.3. It is started by "start-protectTimer" and asserts "protectTimer_done" after 0 to 30 μs since starting.

12.3.2.4 Signal encoding

Five distinct symbols can be transmitted on the line: CD0, CD1, CVL, CVH, and IDL. Of these, CVL and CVH are transmitted only as part of the collision presence reporting pattern CP.

12.3.2.4.1 Data transmission rate

The data transmission rate (BR) is 1 Mb/s ± 0.01%. A bit time (BT) is therefore nominally 1 μs.

12.3.2.4.2 Data symbol encoding

Manchester encoding is used for the transmission of packets. Manchester encoding is a binary signaling mechanism that combines data and clock into bit cells. Each bit cell is split into two halves with the second half containing the binary inverse of the first half; a transition always occurs in the middle of each bit cell. During the first half of the bit cell, the encoded signal is the logical complement of the bit value being encoded. During the second half of the bit cell, the encoded signal is the uncomplemented value of the bit being encoded. Thus, a CD0 is encoded as a bit cell in which the first half is HI and the second half is LO. A CD1 is encoded as a bit cell in which the first half is LO and the second half is HI. Examples of Manchester waveforms are shown in Figure 12–10. The zero crossings of an ideal Manchester waveform occur on precise half-bit-cell boundaries. The zero crossings of real waveforms may include timing jitter that causes deviation from these "idealized zero crossings."

12.3.2.4.3 Collision presence encoding

Two signals, CVL and CVH, that are transmitted only as part of the collision presence reporting pattern, CP, violate the normal Manchester encoding rule requiring a transition in the middle of each symbol. A CVH is encoded as a transition from LO to HI at the beginning of the bit cell, HI for the entire bit cell, and transition

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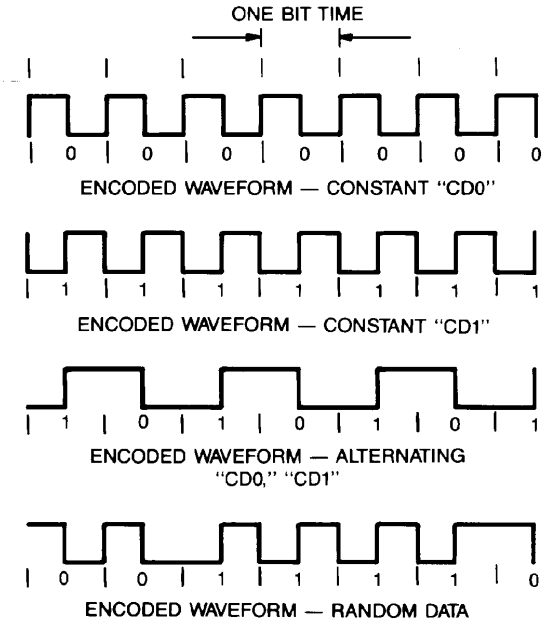


Figure 12–10—Examples of Manchester waveforms

from HI to LO at the end of the bit cell. A CVL is encoded as a transition from HI to LO at the beginning of the bit cell, LO for the entire bit cell, and transition from LO to HI at the end of the bit cell.

The Collision Presence reporting signal, CP, is a special sequence that differs from any legitimate Manchester-encoded signal. CP is encoded as a repeating sequence of 1 bit time LO, 1/2 bit time HI, 1 bit time LO, 1 bit time HI, 1/2 bit time LO, and 1 bit time HI. This may also be interpreted as repetitions of the five-symbol sequence CVL, CD0, CD1, CD0, CVH. Should a transmitter's or receiver's timing be shifted by 1/2 bit time, then the same sequence will be interpretable as repetitions of CD1, CVL, CVH, CD1, CD0. In either case, the presence of non-Manchester symbols distinguishes the sequence from data. Examples of Collision Presence waveforms are shown in Figure 12–11. See 12.3.2.2.5 and 12.4.3.2 for further details on the detection and generation of CP.

NOTE—CP is the minimal length sequence that meets the following design criteria:

a) The sequence should not look like legitimate Manchester-encoded data even if the receiver does not lock onto the correct bit-cell boundaries.
b) The sequence should maintain overall dc balance. That is, it should be HI 50% of the time and LO the other 50%.
c) The signal should occupy the same part of the frequency spectrum as normal data. That is, transitions should occur every half or whole bit time so that the fundamental signaling frequencies of BR/2 and BR are maintained. Furthermore, allowing more than one bit time to pass without a transition would introduce ambiguity with the idle line condition (IDL).

12.3.2.4.4 Idle line encoding

The line condition IDL is also used as an encoded signal. An IDL always starts with a HI signal level. Since IDL always starts with a HI signal, an additional transition will be added to the data stream if the last bit sent was a zero. This transition cannot be confused with clocked data (CD0 or CD1) since the transition will occur at the start of a bit cell. There will be no transition in the middle of the bit cell. The HI signal level, as sent by a transmitter, shall be maintained for a minimum of 2 bit times.

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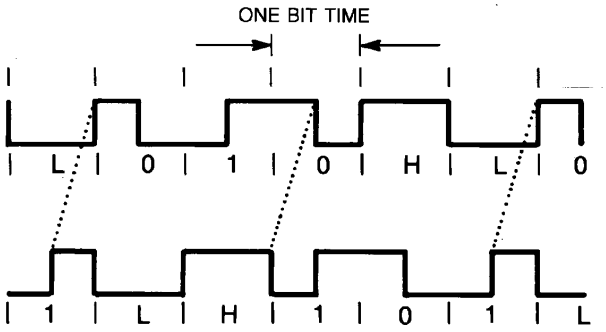


Figure 12–11—Examples of collision presence waveforms

12.4 Hub specification

12.4.1 Overview

This subclause defines the logical characteristics of the hub used in 1BASE5. The relationship of this specification to the entire standard is shown in Figure 12–12.

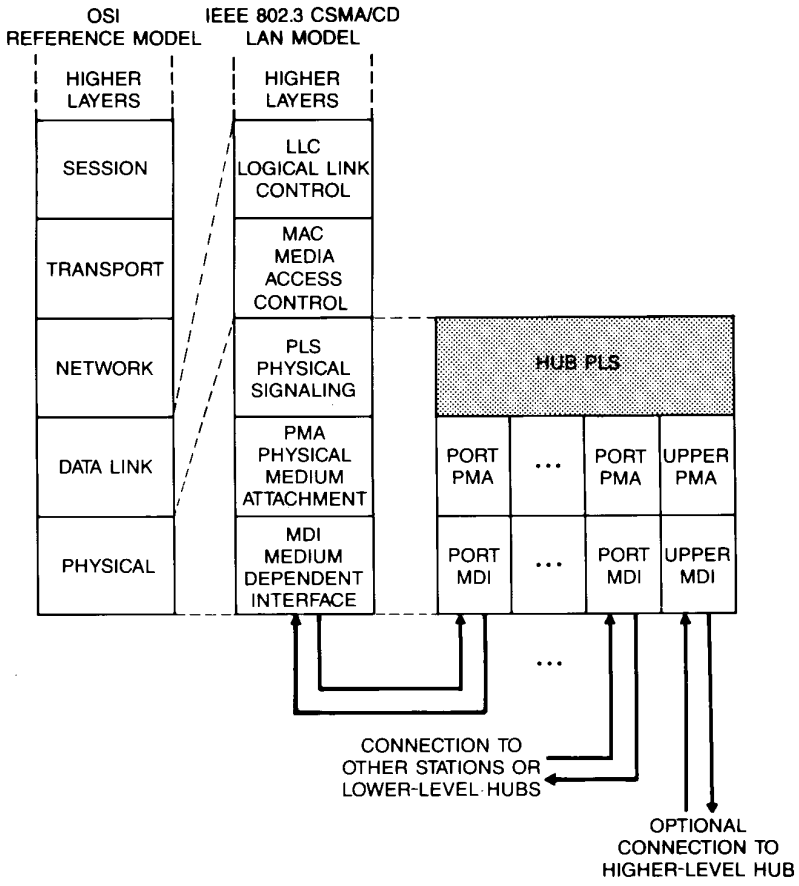


Figure 12–12—Hub relationship to the OSI reference model and the IEEE 802.3 CSMA/CD LAN model

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12.4.1.1 Summary of major concepts

a) A hub consists of a Hub PLS sublayer and a number of instances of the PMA sublayer.
b) One instance of the PMA sublayer, the "upper PMA," provides a connection to a higher-level hub. This PMA is not required for the header hub.
c) Each of the remaining instances of the PMA sublayer, called "port PMAs," provides a connection to a DTE or a lower-level hub.
d) The Hub PLS transfers data in two directions: upward from the port PMAs, to the upper PMA and downward from the upper PMA to the port PMAs.
e) The upward and downward "sides" of the hub operate independently and simultaneously.

12.4.1.2 Application perspective

The hub is a physical layer entity that performs two functions:

a) It retransmits incoming signals with amplitude and timing restored.
b) It detects collisions between any two or more ports and reports knowledge of the collision by transmitting a special collision presence reporting pattern.

12.4.2 Hub structure

Each hub is functionally divided into two parts: the upward side and the downward side. The upward side is responsible for combining the transmissions from DTEs and hubs lower in the network into a single transmission to the next level up. The downward side is responsible for distributing the combined signal (which is wrapped around from the upward side of the header hub) to each of the DTEs and hubs below. Except as specified in 12.4.3.2.3 and 12.4.3.2.6, the two sides function independently.

There is an upward input channel and a corresponding downward output channel for each DTE or hub immediately below the hub. Although there is no electrical connection between the two lines, they do share a connector and cable (see 12.6 and 12.7) and are collectively known as a hub port. Each port is accessed through an instance of the PMA sublayer referred to as a "port PMA."

The one output channel from the upward side and the one input channel to the downward side of a hub are similarly paired and, for all but the header hub, are connected to a port of the next-higher-level hub, They are accessed through an instance of the PMA sublayer referred to as the "upper PMA."

NOTE—A hub that includes n hub ports should be called an n-port hub, even though it may have an extra jack for the upper PMA. The latter connection should never be counted as a port, despite common engineering usage, because it does not meet the specific definition of a 1BASE5 hub port given above.

12.4.2.1 Upward side

The primary function of the upward side of a hub is to propagate signals from each of its inputs to its single output. If more than one input is active, then the Collision Presence signal CP is transmitted instead. In addition, the signals are retimed to restore the transitions to half-bit-time boundaries; see 12.4.3.2.5 for the details of retiming.

12.4.2.2 Downward side

The primary function of the downward side of a hub is to repeat signals from its one input to each of its outputs. In addition, the signals are retimed to restore the transitions to half-bit-time boundaries; see 12.4.3.2.5 for the details of retiming.

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12.4.3 Hub PLS functional specification

This subclause provides a detailed model for the Hub PLS sublayer.

12.4.3.1 Hub PLS to PMA interface

The interface between the Hub PLS and the PMA is the same as that specified in 12.3.2.1 for use between the DTE PLS and the PMA except that the *output* message from the Hub PLS to the PMA is used to transmit CVL and CVH in addition to CD0 and CD1.

12.4.3.2 Hub PLS functions

The Hub PLS sublayer functions consist of three asynchronous functions. These functions are Upward Transfer, Jabber, and Downward Transfer. All three functions are started immediately following PowerOn; an independent copy of the Jabber function is started for each port PMA. These functions are depicted in the state diagrams shown in Figure 12–13 through Figure 12–15, using the notation described in 1.2.1.

12.4.3.2.1 State diagram variables

The variables used in the state diagrams and the corresponding descriptions are the following:

a) *Port designators:* Instances of the PMA sublayer are referred to by index. PMA information is obtained by replacing the X in the desired function with the index of the PMA of interest. Furthermore, PMAs may be referenced by several special designators used as indices:

X Generic port PMA designator. When X is used in a state diagram its value indicates the particular instance of a generic function.

UPPER Indicates the upper PMA.

ALLPORTS Indicates that all port PMAs are to be considered. All port PMAs must meet a test condition in order for that test to pass.

ALLENABLEDPORTS Indicates that all port PMAs that are not disabled by the Jabber function are to be considered. All such port PMAs must meet a test condition in order for that test to pass.

ONEPORT Indicates that all port PMAs that are not disabled by the Jabber function are to be considered. One, but not more than one, such port PMA must meet a test condition in order for that test to pass.

>ONEPORT Indicates that all port PMAs that are not disabled by the Jabber function are to be considered. Two or more such port PMAs must meet a test condition in order for that test to pass.

N Defined by the PORT function on exiting from the UPWARD IDLE state of Figure 12–13. It indicates which port PMA caused the exit from the UPWARD IDLE state.

b) *Port functions*:

PORT(TestCondition) Returns the index of a port PMA passing the indicated test condition. If multiple port PMAs meet the test condition, the PORT function will return one and only one of the acceptable values.

c) *Input variables:*

INPUT(X) Indicates the state of activity on the designated PMA input channel. It may be either “idle” or “active.” The former indicates that *input_idle* is asserted; the latter indicates that it is not asserted.

input(X) Used to receive an *input* message (see 12.3.2.1) from the designated PMA input channel.

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probation_alternative Used to distinguish between the two allowed alternatives for exiting the JABBER JAM state of Figure 12–14 when an active port becomes idle. The implementor of a hub may treat the variable as either true or false.

d) *Output variables:*

output(X)Used to send an *output* message (see 12.3.2.1 and 12.4.3.1) to the designated PMA output channel.

output_idle(X)Used to send an *output_idle* message (see 12.3.2.1) on the designated PMA output channel.

e) *Inter process flags:*

send_collisionUsed by the Upward Signal Transfer function to indicate a series of *output* messages to the upper PMA sublayer, the effect of which is to transmit the CP signal, as described in 12.3.2.4.2, 12.3.2.4.3, and 12.4.3.2.7.

jabber_collisionUsed by the various instances of the Jabber function to signal the Upward Signal Transfer function that CP should be generated.

disable_input(X)Used to disable the designated PMA input channel. The input is re-enabled when disable-input(X) is no longer asserted. Only the Upward Signal Transfer function is affected by the disabling of a port (via the ALLENABLEDPORTS, ONEPORT, and >ONEPORT designators).

jabberTime1Used by the Jabber function (see 12.4.3.2.3) to detect excessively long transmissions. It is started by "start_jabberTime1." "jabberTime1_done" is satisfied when the timer has expired.

jabberTime2Used by the Jabber function (see 12.4.3.2.3) to determine when to disable ports due to excessively long transmissions. It is started by "start_jabberTime2." "jabberTime2_done" is satisfied when the timer has expired.

12.4.3.2.2 Upward Signal Transfer function

The Upward Signal Transfer function combines signals from the various port inputs and passes them on to the upper output. It also detects and reports collisions as appropriate. The state diagram of Figure 12–13 depicts its operation.

Signals are propagated upward according to the following rules, except as controlled by the Jabber function (see 12.4.3.2.3):

a) If IDL is present on all port inputs, then transmit IDL.
b) If IDL is present on all but one of the port inputs, then repeat the signal received from that one line. If that one signal is CP, then a hub may generate its own CP signal instead of repeating the received CP signal.
c) If two or more inputs are active (non-IDL) at the same time, then transmit CP and continue transmitting CP until all inputs indicate IDL again.

Whenever the hub finishes transmitting CP, it shall then transmit IDL, including the extended HI period.

12.4.3.2.3 Jabber function

The Jabber function detects abnormally long transmissions and takes appropriate action to abort them. The state diagram of Figure 12–14 depicts its operation.

Two timers are used by the Jabber function. They may be implemented either as local timers for each instance of the Jabber function or as global timers shared by all instances. Furthermore, because the two timers are always started concurrently, an implementation may share circuitry between the two.

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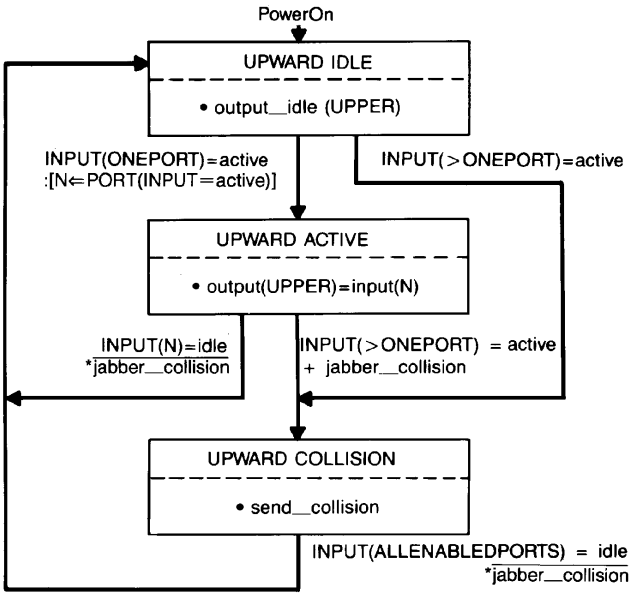


Figure 12–13—Hub PLS Upward Transfer function

The first timer is started by "start_jabberTime1" and asserts "jabberTime1_done" after 25 to 50 ms since starting. If implemented as a single global timer, assertion of start_jabberTime1 by any instance of the Jabber function with any other instance(s) still waiting for that timer shall not restart the timer, thereby shortening the waiting period for the latest instance.

Similarly, the second timer is started by "start_jabberTime2" and asserts "jabberTime2_done" after 51 to 100 ms since starting. If implemented as a single global timer, assertion of start_jabberTime2 by any instance of the Jabber function with any other instance(s) still waiting for that timer shall not restart the timer, thereby shortening the waiting period for the latest instance. Furthermore, if this second timer is implemented as a single global timer, then assertion of start_jabberTime1 by any instance of the Jabber function with any other instance(s) still waiting for just the second timer (in the JABBER JAM state) shall be treated as if the first timer expires immediately (asserting jabberTime1_done) for the latest instance, thereby causing that instance to join the other instance(s) waiting for the second timer.

Hardware within the upward side of a hub shall provide a window of 25 to 50 ms, during which time a normal packet or CP sequence may be propagated upward. If any port input (or, as an alternative implementation, the hub's combined upward signal) exceeds this duration without becoming idle, then the hub shall switch to transmitting CP until 51 to 100 ms after the beginning of the window and then, if that input is still active, disable that input (or all nonidle inputs) until it once again becomes active while the downward side is idle.

The "probation_alternative" input variable is used to distinguish between the two allowed alternatives for exiting the JABBER JAM state of Figure 12–14 when an active port becomes idle. The implementor of a hub may treat the variable as either true or false. If true, the port will enter the JABBER PROBATION state (via the JABBER SHUTOFF state); if false, the port will instead return to the JABBER IDLE state.

12.4.3.2.4 Downward Signal Transfer function

The Downward Signal Transfer function repeats signals from the upper input to the various port outputs. The state diagram of Figure 12–15 depicts its operation.

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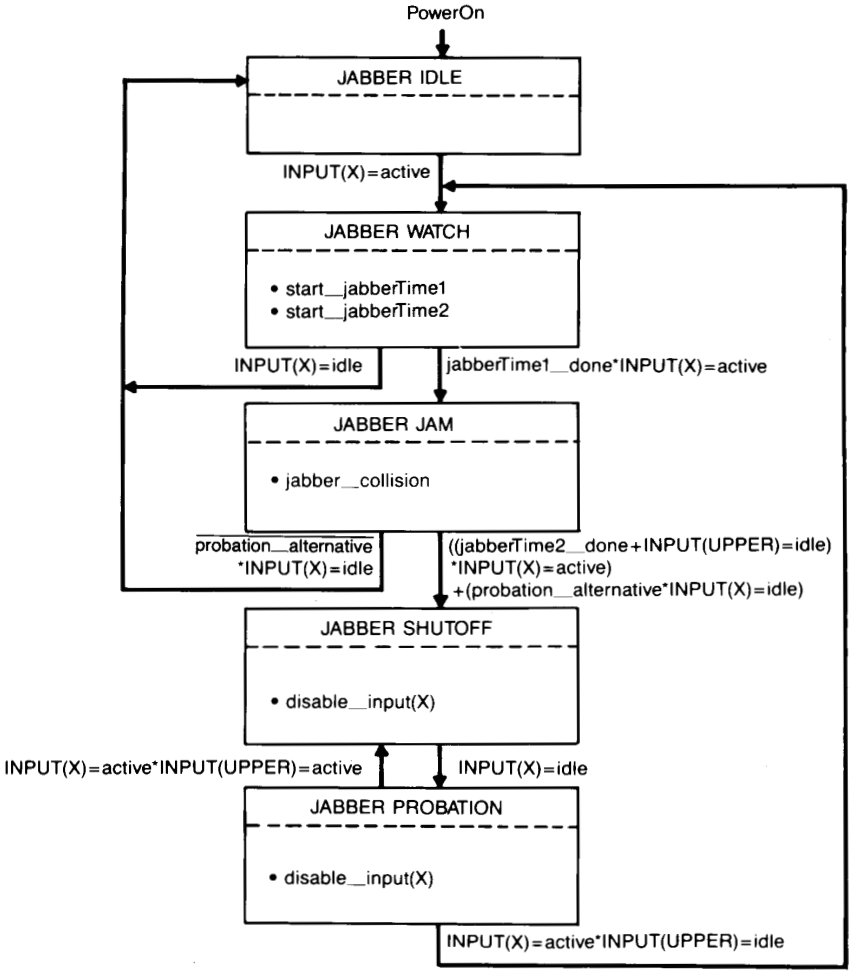


Figure 12–14—Hub PLS Jabber function for port X

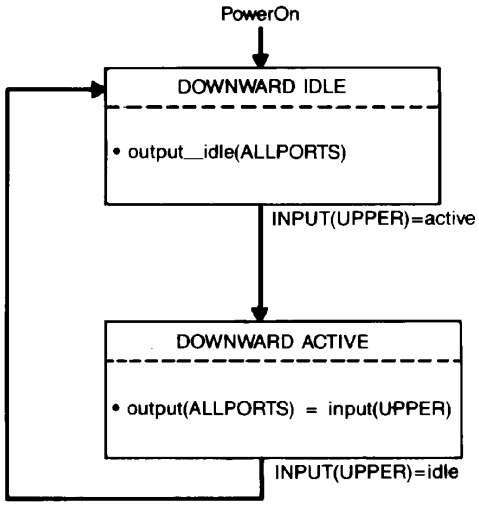


Figure 12–15—Hub PLS Downward Transfer function

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The downward side of a hub may detect the Collision Presence signal at the upper input and generate its own CP signal to be transmitted at the port outputs (in place of repeating the received CP signal).

Whenever the hub finishes transmitting CP, it shall then transmit IDL, including the extended HI period.

12.4.3.2.5 Retiming (jitter removal)

Each side of each hub shall retime any clocked signals that it propagates so that the transitions occur on half-bit-time boundaries, thereby avoiding accumulation of excessive jitter. Such retiming shall preserve the sequence of CD0, CD1, CVL, and CVH symbols being propagated.

If an ambiguity exists in the incoming bit cells due to excessive noise or jitter, than the appropriate side of the hub may either switch to generating CP or replace the erroneous bit cell with an arbitrary combination of half or whole bit cells.

Retiming also accounts for differences (if any) in clock rates between that used to send bit cells to the hub and that used to send them out from the hub. Excessive differences in clock rates (caused by clocks not meeting 12.3.2.4.1) and excessively long packets (caused by exceeding maxFrameSize) may each cause the capacity of the retiming function to be exceeded. In such circumstances, the appropriate side of the hub may either switch to transmitting CP or add or delete half or whole bit cells as needed.

Whenever bit cells are added, deleted, or replaced, the hub shall maintain synchronization of the outgoing bit cells to a half or whole bit cell boundary. Furthermore, it shall not generate periods of more than one bit time without a transition.

12.4.3.2.6 Header hub wrap-around

For each particular network configuration, one hub operates as the header hub and all others as intermediate hubs. It is suggested, but not required, that hub implementations be capable of being used for either purpose. Methods for switching between these two modes are beyond the scope of this standard.

For an intermediate hub, the upper output shall be connected to a port input of the next higher-level hub and the upper input shall be connected to a port output of a higher-level hub.

For the header hub, the upper output shall be connected to the upper input. This wraparound may appropriately bypass parts of the PMA specification so long as the resulting implementation is functionally equivalent to one with a wired connection. For example, signals internal to the hub need not be translated to the corresponding external levels and then translated back to internal levels. Similarly, it shall not be necessary to retime the wrapped signal twice, once in the upward side and then again in the downward side of the same header hub; a single retiming is permissible.

12.4.3.2.7 Collision presence startup

When a hub starts generating CP (as specified in 12.4.3.2.2 through 12.4.3.2.5) it shall synchronize the startup to a half or whole bit-cell boundary of any immediately preceding signal. If it was sending IDL immediately before the CP, no synchronization or preamble is required.

A hub may start transmission of CP at any point in the sequence that does not result in periods of more than one bit time without a transition during the switch from passing on data to sending CP. Depending on the preceding signal, it may start with L010H, 010HL, 10HL0, 0HL01, or HL010. Because startup may be synchronized to any half-bit-cell boundary, a hub may also transmit the shifted version of CP starting with 1LH10, LH101, H101L, 101LH, or 01LH1.

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12.4.3.3 Reliability

Hubs shall be designed to provide a mean time between failure (MTBF) of at least 45 000 hours of operation. Hubs, including the associated connectors and other passive components, should be designed to minimize the probability that, a particular failure results in total network failure. Furthermore, the port electronics of each hub should be designed so as to minimize the probability that the failure of one port prevents communication by equipment attached to the other ports.

12.5 Physical medium attachment (PMA) specification

12.5.1 Overview

This subclause defines the Physical Medium Attachment (PMA) sublayer for 1BASE5. The relationship of this specification to the entire International Standard is shown in Figure 12–16. The PMA sublayer connects the PLS sublayer to the Medium Dependent Interface (MDI).

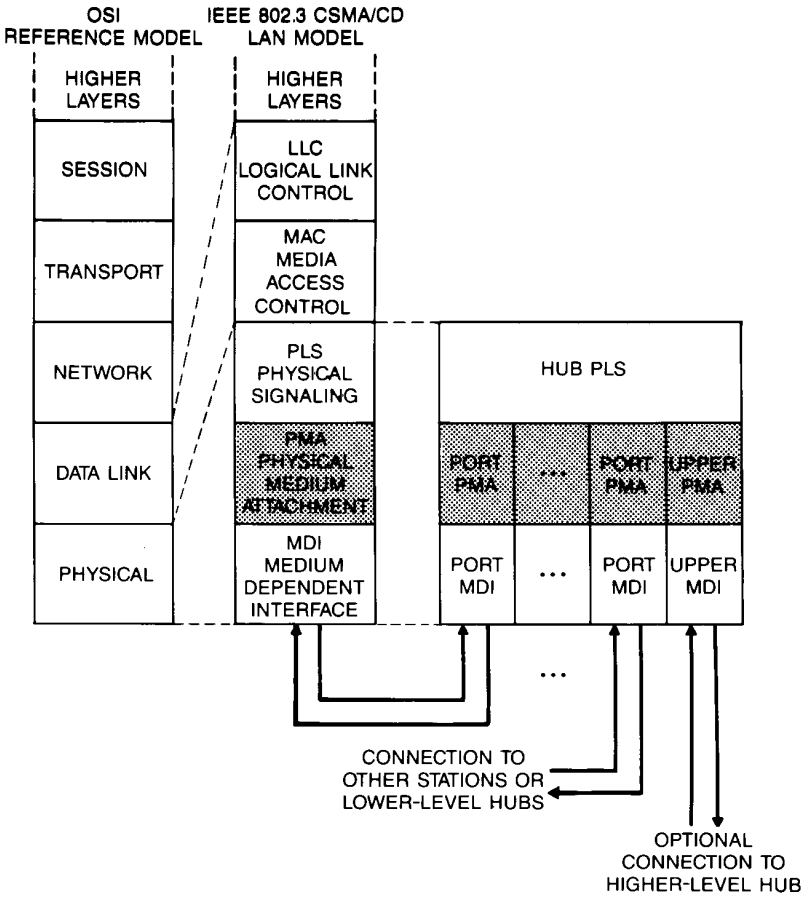


Figure 12–16—Physical medium attachment, relationship to the OSI reference model and the IEEE 802.3 CSMA/CD LAN model

12.5.2 PLS–PMA interface

The interface between the PLS and the PMA sublayers is specified in 12.3.2.1 for DTEs and in 12.4.3.1 for hubs.

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12.5.3 Signal characteristics

12.5.3.1 Transmitter characteristics

Transmitters should operate properly when loaded with any cable meeting the requirements of 12.7. To approximate the boundary conditions of such loading, two specific test loads are specified. Transmitters shall meet all requirements of this subclause when connected to both the "light" (115 Ω) load shown in Figure 12–17 and the "heavy" (approximately 80 Ω) load shown in Figure 12–18. It is expected that transmitters that perform correctly with these two loads will also perform acceptably under intermediate loading conditions.

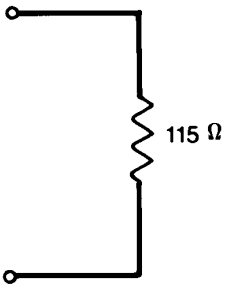


Figure 12–17—Simulated light load

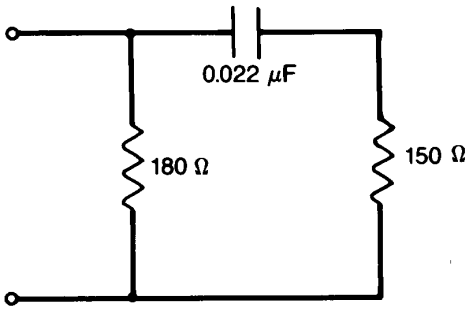


Figure 12–18—Simulated heavy load

12.5.3.1.1 Differential output voltage

For simplicity of explanation, the text and figures of this subclause describe the differential output voltage in terms of voltage magnitudes. The requirements of this subclause apply to the negative pulses as well as the positive ones.

Beginning with the second bit of the preamble (or CP, if no preamble is present), pulses of duration BT/2 shall meet the conditions of Figure 12–19. Pulses of duration BT shall meet the conditions of Figure 12–20. After the zero-crossing, the output shall exceed the voltage of a signal rising from the zero-crossing to 2.0 V with a slope of magnitude 20 mV/ns. The output shall remain above 2.0 V until 100 ns before the next, zero-crossing. The peak output voltage shall not exceed 3.65 V. While falling from 2.0 V to the zero-crossing, the signal shall exceed the voltage of a signal falling from 2.0 V to the zero-crossing with a slope of magnitude 20 mV/ns.

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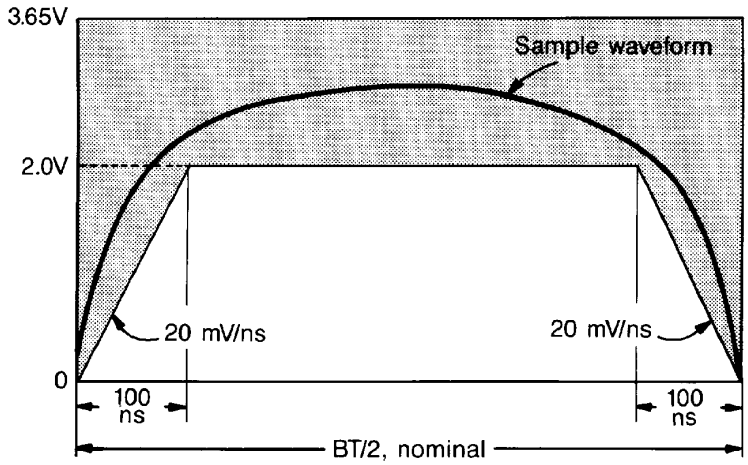


Figure 12–19—Differential output voltage, nominal duration BT/2

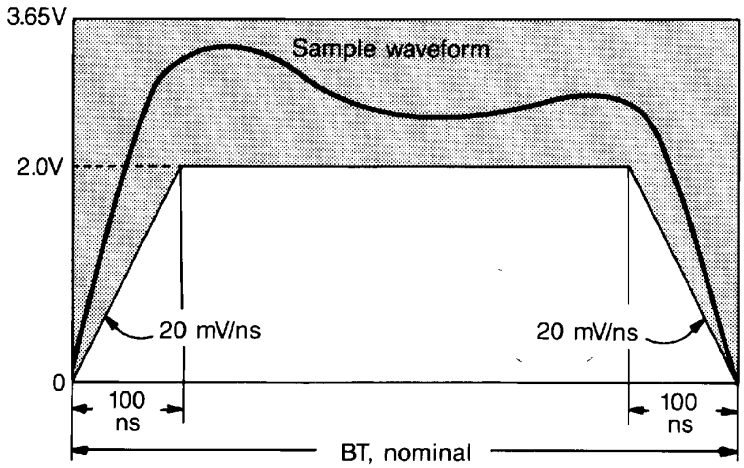


Figure 12–20—Differential output voltage, duration BT

For pulses of duration BT, the average voltage that appears from 100 ns after the zero-crossing through BT/2 shall be between 0.95 and 1.8 times the average voltage that appears from time BT/2 through 100 ns before the following zero-crossing. Similarly, for pulses of duration BT, the peak voltage that appears from 100 ns after the zero-crossing through BT/2 shall be between 0.95 and 1.8 times the peak voltage that appears from time BT/2 through 100 ns before the following zero-crossing.

NOTE—The purpose of the above restrictions on average and peak voltages is to avoid transmitter waveforms that peak excessively during the second half of signals of duration BT, resulting in excessive jitter at the receiver. Some equalization to produce slight droop in the second half of signals of duration BT, on the other hand, may help decrease jitter at the far end of long cables.

The amplitude of the power spectrum at the output of the transmitter for all possible sequences of signals shall not exceed that produced by an idealized transmitter sending corresponding rectangular waveforms with magnitude 3.65 V at any frequency.

When a transmitter enters the idle state, it shall maintain a minimum differential output, voltage of 2.0 V from 100 ns through 2 BT after the last low-to high transition, as illustrated in Figure 12–21. The differential

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output voltage shall then fall to 1.1 V within 3 BT after that same low-to-high transition. Starting when the differential output voltage first reaches 1.1 V, the magnitude of the output voltage driven into the test loads indicated in Figure 12–22 and Figure 12–23 shall then remain within the limits indicated in Figure 12–21 until the transmitter leaves the idle state.

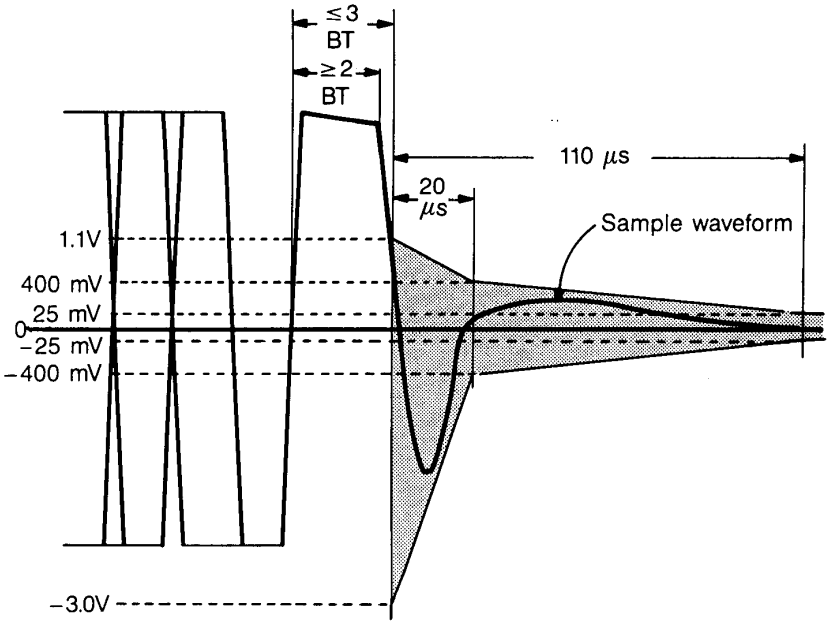


Figure 12–21—Transmitter waveform for idle

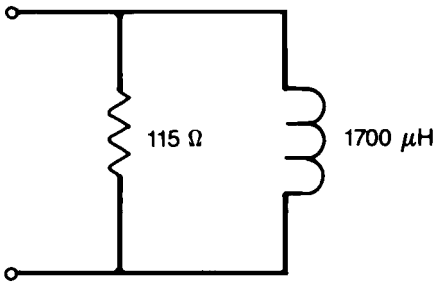


Figure 12–22—Start-of-idle test load #1

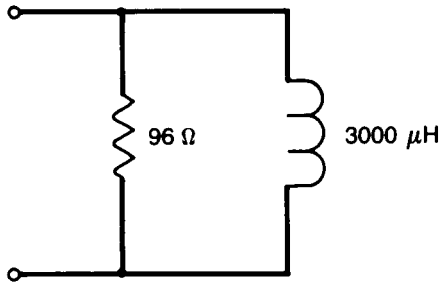


Figure 12–23—Start-of-idle test load #2

The transmitter output at the start of idle may exhibit overshoot, ringing, slow voltage decay, or a combination thereof due to the following factors:

a) Change in transmitter source impedance between the active and idle states
b) Difference in the magnitudes of the differential output voltage between the high and low output states (ΔV_{OD})
c) Waveform asymmetry at the transmitter (ΔT)
d) Transmitter and receiver (transformer) inductance (L)

NOTE 1—The contribution to the undershoot from each of these can be computed with the following equations:

$$V_{\Delta V_{OD}} = \pm V_{OD} \bullet (R_{OFF}/2R_N)$$

$$V_{\Delta T} = (\pm \Delta T/1000\ ns) \bullet V_P(R_{OFF}/R_{ON})$$

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$$V_L = V_P \bullet (1 - e^{-2.75\ \mu s/(L_P/R_{ON})}) \bullet (R_{OFF}/R_{ON})$$

where

$R_{OFF} = (R_{SRC\text{-}OFF} \parallel R_L)$

$R_{ON} = (R_{SRC\text{-}ON} \parallel R_L)$

$R_{SRC\text{-}OFF}$ = source impedance (Ω) when the driver is off

$R_{SRC\text{-}ON}$ = source impedance (Ω) when the driver is on

R_L = load impedance (Ω)

L_P = combined inductance (μH) of the transmitter and receiver transformers

ΔV_{OD} = the difference (V) in in magnitude of the HI and LO output voltages

ΔT = asymmetry of the waveform equals the difference between the average HI and average LO pulse widths (ns) at the transmitter

VP = the maximum output voltage (V) during the start of IDL

NOTE 2—The waveform shown in Figure 12–21 and the equations in the preceding note apply to a transmitter connected to the test loads of Figures 12–22 and 12–23. An actual receiver may present a more complex termination impedance and so the undershoot or overshoot may exceed that encountered with the test loads.

12.5.3.1.2 Output timing jitter

The transmitted signal zero-crossings shall deviate from the idealized zero-crossings by no more than ± 10 ns.

12.5.3.1.3 Transmitter impedance balance

The longitudinal to metallic impedance balance of the transmitter, defined as 20 $\log_{10}(E_{test}/E_{dif})$, where E_{test} is an externally applied ac voltage, as shown in Figure 12–24, shall exceed 44 dB at all frequencies up to and including 4BR in the idle and nonidle states.

NOTE—It may be difficult to measure the transmitter impedance balance in the nonidle state. A frequency-selective wavemeter or other measurement technique may be required. Furthermore, the balance of the test equipment (such as the matching of the 400 Ω resistors) must exceed that required of the transmitter.

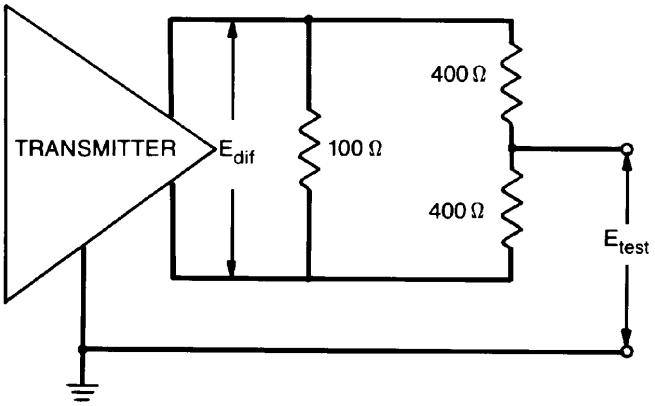


Figure 12–24—Transmitter impedance balance

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12.5.3.1.4 Common-mode output voltage

The magnitude of the total common-mode output voltage of the transmitter, E_{cm}, measured as shown in Figure 12–25, shall not exceed 300 mV.

NOTE—The implementor should consider any applicable local, national, or international regulations and standards concerning RF emission. Driving unshielded twisted pairs with high-frequency common-mode voltages may result in interference to other equipment.

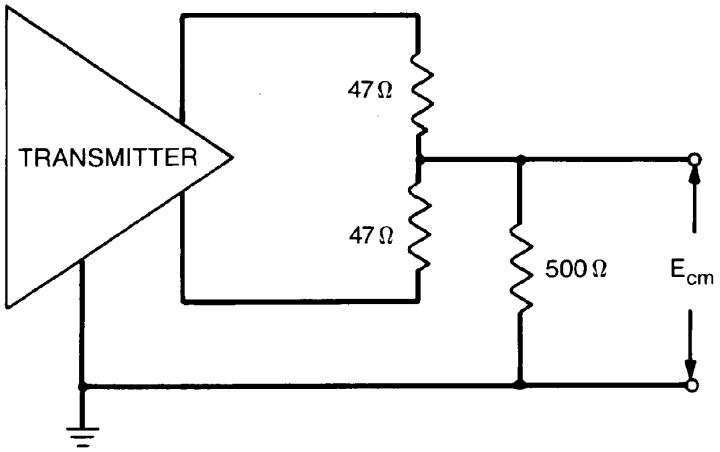


Figure 12–25—Common-mode output voltage

12.5.3.1.5 Common-mode tolerance

Transmitters shall meet the requirements of 12.5.3.1.1 and 12.5.3.1.2 even in the presence of common-mode sinusoidal voltage, E_{cm} (as shown in Figure 12–26), of ± 20 V peak at frequencies from 40 kHz through 6BR.

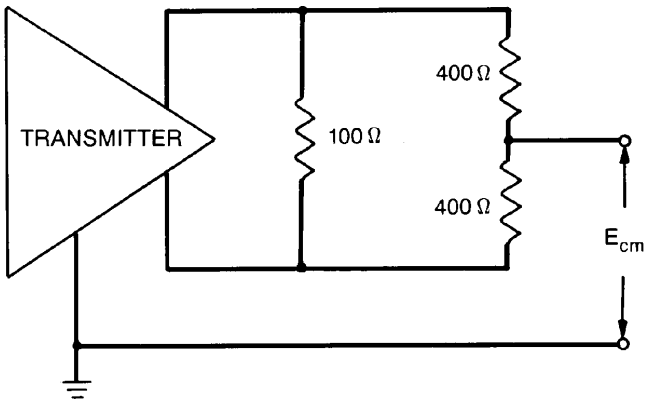


Figure 12–26—Transmitter common-mode tolerance

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12.5.3.1.6 Transmitter fault tolerance

Transmitters, both when idle and when nonidle, shall tolerate the application of short circuits across their outputs for an indefinite period of time without damage and shall resume normal operation after such faults are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

Transmitters, both when idle and when nonidle, shall withstand, without damage, a 1000 V common-mode impulse of either polarity, applied as indicated in Figure 12–27. The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

NOTE—Tolerance of, and recovery from, the application of the telephony voltages described in 12.10.2 is optional, but the safety requirements of that subclause are mandatory.

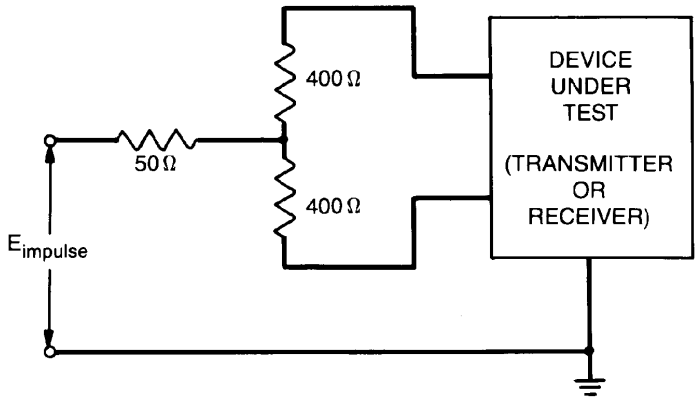


Figure 12–27—Common-mode impulse test

12.5.3.2 Receiver characteristics

12.5.3.2.1 Differential input voltage

The receiver shall operate properly when a signal meeting the minimum magnitude requirements of Figure 12–28 is received. When less than 300 mV, the magnitude of the voltage will exceed that of a straight line through the nearest zero-crossing with slope of magnitude 9 mV/ns. That is, the average slew rate near each zero-crossing will exceed 9 mV/ns. The magnitude of the voltage will also remain at or above 1.0 V for some period lasting at least 150 ns (650 ns for pulses of duration BT) that starts within 250 ns of the preceding zero-crossing and its peak will be at least 1.1 V.

12.5.3.2.2 Input timing jitter

Receivers shall operate properly with zero-crossing jitter of up to ± 32 ns from the ideal.

12.5.3.2.3 Idle input behavior

The IDL condition shall be detected within 1.8 bit times of the last low-to-high transition at the receiver.

NOTE 1—It is necessary to distinguish CVH from IDL.
NOTE 2—System jitter considerations make it impractical to detect IDL (<etd>, end-of-transmission delimiter) any sooner than 1.3 bit times. The specific implementation of the clock recovery mechanism, or equivalent, determines the lower bound on the actual IDL detection time. Adequate margin should be provided between the lower bound and 1.8 bit times.

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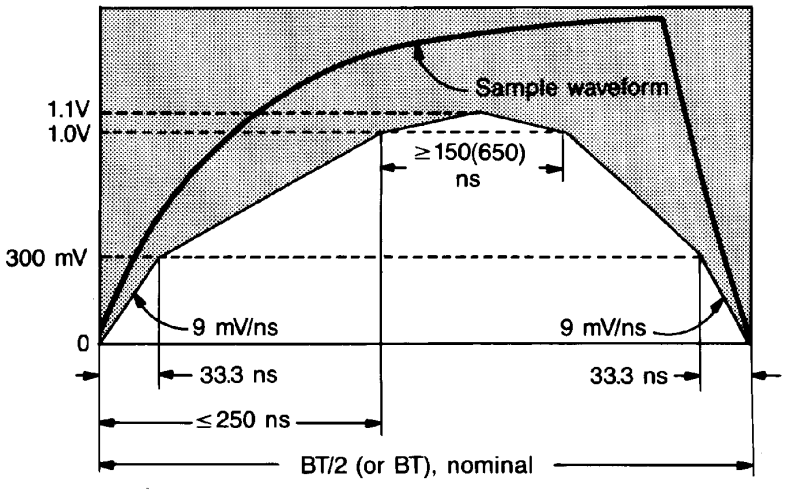


Figure 12–28—Receiver signal envelope

The receiver shall take precautions to ensure that the HI-to-silence transition of the start of IDL is not falsely interpreted as a silence-to-nonidle transition, even in the presence of signal droop, overshoot, ringing, slow voltage decay, or a combination thereof due to capacitive and inductive effects in the transmitter, cable, and receiver, including those discussed in 12.5.3.1.1.

To this end, a receiver in a hub shall treat its input as if it were idle for between 20 and 30 μs after detecting IDL. The timing of this "protection" period for the port PMAs may use a single timer that is started when all ports have become idle or disabled by the Jabber function. Receivers in DTEs may include a similar protection period of up to 30 μs.

NOTE—The protection period is required in hubs because erroneously interpreting the start-of-idle as a new transmission will result in propagation of the error to DTEs, despite any precautions taken in those DTEs. The protection period is optional in DTEs because any implementation error in a DTE will affect only that particular DTE.

12.5.3.2.4 Differential input impedance

The (complex) differential input impedance of the receiver, $Z_{receiver}$, shall be such that the reflection attenuation, defined as 20 $\log_{10}$ ($|Z_{receiver} + Z_{cable}|/|Z_{receiver} - Z_{cable}|$), where Z_{cable} is the differential characteristic impedance of the attached cable, exceeds 16 dB over the range BR/2 through 2BR for all cables meeting the requirements of 12.7.2.

12.5.3.2.5 Common-mode rejection

Receivers shall assume the proper output state for any differential input signal, E_s, that results in a signal, E_{dif}, that meets 12.5.3.2.1 and 12.5.3.2.2, even in the presence of common-mode sinusoidal, voltages, E_{cm} (as shown in Figure 12–29), of ±20 V peak at frequencies from 40 kHz through 6BR.

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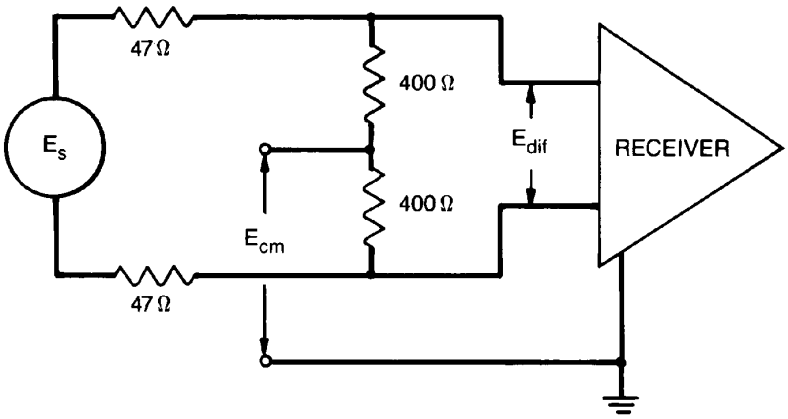


Figure 12–29—Receiver common-mode rejection

12.5.3.2.6 Noise immunity

Receivers shall meet the following limits on average error, rates when the noise described in 12.7.4 is added to the signals described in 12.5.3.2.1 and 12.5.3.2.2:

a) When nonidle, the receiver error rate shall not exceed one error in 10^8 bits.
b) When idle, a receiver used in a DTE shall not falsely detect carrier more than one in 100 s.
c) When idle, a receiver used in a hub shall not falsely detect carrier more than once in 1500 s.

NOTE—Receivers whose inputs include a 2–4 MHz, 2-pole, low-pass, Butterworth filter and a 560 mV squelch level will meet this last requirement for idle-mode noise immunity yet still perform properly with the weakest signal allowed by 12.5.3.2.1.

12.5.3.2.7 Receiver fault tolerance

Receivers shall tolerate the application of short circuits across their inputs for an indefinite period of time without damage and shall resume normal operation after such faults are removed.

Receivers shall withstand, without damage, a 1000 V common-mode impulse of either polarity, applied as indicated in Figure 12–27. The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

NOTE—Tolerance of, and recovery from, the application of the telephony voltages described in 12.10.2 is optional, but the safety requirements of that subclause are mandatory.

12.6 Medium Dependent Interface (MDI) specification

12.6.1 Line interface connector

8-pin connectors meeting the requirements of Clause 3 and Figures 1 through 5 of ISO/IEC 8877: 1992 shall be used as the compatibility interface between the PMA and the medium. The use of other types of connectors, if any, within a PMA or within the medium, although not explicitly prohibited, is outside the scope of this standard.

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12.6.2 Connector contact assignments

The contacts of the connectors, as depicted in Figure 12–32 and Figure 12–31, shall correspond to signaling circuits as indicated below:

Contact	Signal
1	Upward Data+ (positive for HI signal)
2	Upward Data– (negative for HI signal)
3	Downward Data+ (positive for HI signal)
4	not used by 1BASE5
5	not used by 1BASE5
6	Downward Data– (negative for HI signal)
7	reserved
8	reserved

For DTEs and the upper MDI of hubs, contacts 1 and 2 are used for transmitting and contacts 3 and 6 are used for receiving. For the port MDIs of hubs, however, contacts 1 and 2 are used for receiving and contacts 3 and 6 are used for transmitting.

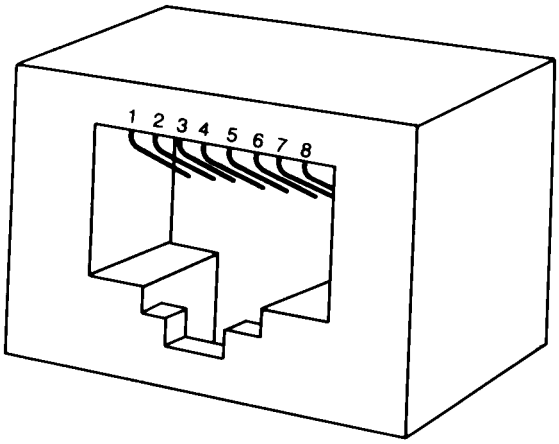


Figure 12–30—DTE and hub connector

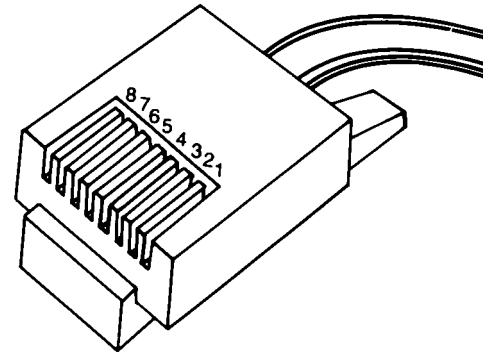


Figure 12–31—Cable connector

12.6.3 Labeling

To distinguish 1BASE5 connectors from those used for other purposes, it is recommended that appropriate labels be affixed to wall outlets and other connectors. This is particularly important in environments in which the specified 8-contact connectors are used for more than one purpose.

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12.7 Cable medium characteristics

12.7.1 Overview

A significant number of IBASE5 networks are expected to utilize in-place building wiring. In this environment, DTEs connect to wall outlets using twisted-pair telephone cord. The wall outlets, in turn, connect to wiring closets, where hubs could be located, using standard telephone wiring. This wiring typically consists of 0.4–0.6 mm diameter (26–22 gauge) unshielded twisted pairs.

12.7.2 Transmission parameters

Each wire pair used to interconnect DTEs and hubs shall meet the requirements of 12.9.3 and also have the following characteristics.

12.7.2.1 Attenuation

Total cable attenuation between a transmitter and the corresponding receiver shall be no more than 6.5 dB at all frequencies between BR/2 and BR, 9.2 dB at frequencies between BR and 2BR, and 13.8 dB at frequencies between 2BR and 4BR.

12.7.2.2 Differential characteristic impedance

The magnitude of the differential characteristic impedance at frequency BR, Z_{BR}, of each wire pair used shall be between 80 Ω and 115 Ω. In addition, the magnitude and phase angle of the characteristic impedance at each of the following frequencies shall be within the corresponding ranges indicated:

Magnitude			Phase angle	
Frequency	**Minimum**	**Maximum**	**Minimum**	**Maximum**
BR/4	Z_{BR}	Z_{BR} + 7 Ω	–10°	0°
BR/2	Z_{BR}	Z_{BR} + 5 Ω	–8°	0°
BR	Z_{BR}	Z_{BR}	–6°	0°
2BR	Z_{BR} – 4 Ω	Z_{BR}	–4°	0°
4BR	Z_{BR} – 5 Ω	Z_{BR}	–3°	0°

12.7.2.3 Medium timing jitter

Intersymbol interference and reflections due to impedance mismatches between the sections of a cable segment can introduce jitter in the timing of the zero-crossings. A cable segment terminated in 96 Ω shall add no more than ± 17 ns, referenced to the transmit clock, of edge jitter when driven with a rectangular signal of magnitude 2.5 V through a source impedance 22 Ω. The driving signal shall be a Manchester-encoded pseudo-random sequence of data with a repetition period of at least 511 bits.

NOTE 1—The reflections caused by splicing two cable sections that have different characteristic impedances (but that each meet the requirements of 12.7.2.2) will not contribute significantly to timing jitter if the splice is within 10 m of either end of the segment.
NOTE 2—Branches off a wire pair (often referred to as “bridged taps” or “stubs”) will generally cause excessive jitter and so should be avoided.
NOTE 3—Jitter can be measured at the receiving end of a segment using an oscilloscope. The oscilloscope is triggered

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on zero-crossings; the deviation of subsequent zero-crossings from multiples of BT/2 is then observed. The deviation of each zero-crossing must not exceed ±34 ns.

12.7.2.4 Dispersion

Each wire pair shall produce an output signal that meets the zero-crossing edge rate described in 12.5.3.2.1 when driven with a 1 MHz trapezoidal signal of magnitude 2.0 V (that is, 4.0 V peak-to-peak) with edge rate 20 mV/ns.

12.7.3 Coupling parameters

To avoid excessive coupling of signals between pairs of a cable, the crosstalk and imbalance must be limited.

Crosstalk attenuation is specified with the far end of both the disturbed and the disturbing pairs and the near end of the disturbed pair terminated in 96 Ω.

12.7.3.1 Pair-to-pair crosstalk

The near-end, differential, crosstalk attenuation between each wire pair and each other pair in the same cable shall be at least 45 dB frequencies up to BR and at least $45 - 15 \log_{10} (f/\mathrm{BR})$ dB for each frequency f between BR and 4BR.

12.7.3.2 Multiple-disturber crosstalk

The near-end, differential, crosstalk attenuation between multiple disturbing wire pairs and a disturbed pair in the same cable shall be at least 38.5 dB at frequency BR and at least $38.5 - 15 \log_{10} (f/\mathrm{BR})$ dB for each frequency f between BR and 4BR.

When two or more disturbers are present in a common cable sheath, the multiple-disturber, near-end, crosstalk attenuation (MDNEXT) into each pair, measured in dB, may be determined using the following equations:

$$H_j = \sum_{i \neq j} 10^{(-X_{ij}/20)} \cos\theta_{ij}$$

$$V_j = \sum_{i \neq j} 10^{(-X_{ij}/20)} \sin\theta_{ij}$$

$$\mathrm{MDNEXT}_j = 10 \log_{10}(H_j^2 + V_j^2)$$

where

i	iterates over each disturbing pair
j	is the disturbed pair
X_{ij}	is the magnitude of the near-end, differential, crosstalk attenuation from pair i to pair j
θ_{ij}	is the phase angle of the near-end, differential, crosstalk attenuation from pair i to pair j

If only the probability distribution of X_{ij} is known, then the distribution of MDNEXT can be determined using Monte Carlo methods with that X_{ij} distribution and a phase angle uniformly distributed between 0 and 2π rad.

NOTE—See B.3 for example computations of MDNEXT distributions.

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12.7.3.3 Balance

The longitudinal to metallic balance of the cable, defined as 20 $\log_{10}$ (E_{test}/ 2E_x), where E_{test} is an externally applied voltage, as shown in Figure 12–32, shall exceed 44 dB at all frequencies up to 4BR.

NOTE—The balance of the test equipment (such as the balance of the transformer and the matching of the 300 Ω resistors) must exceed that required of the cable.

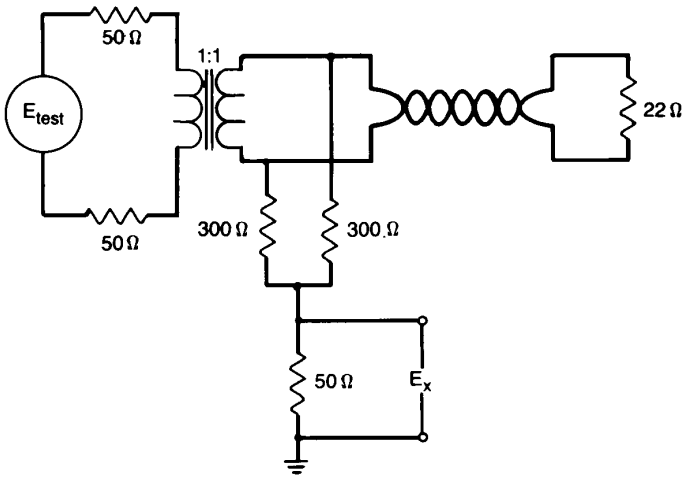


Figure 12–32—Cable balance test

12.7.4 Noise environment

Links used with 1BASE5 shall provide a noise environment no worse than that described below. The total noise environment generally results from two primary contributions: self-crosstalk from other 1BASE5 wire pairs and externally induced impulse noise, typically from telephone ringing and dialing signals, and office machinery. For the purposes of this standard, it can be assumed that the two components contribute independently and so the total error rate can be appropriately split between the two.

12.7.4.1 Impulse noise

The noise voltage on wire pairs terminated at both ends in 96 Ω, as measured through the following specified filters, shall not exceed the corresponding threshold voltages more than 9 times per 1800 s interval. Following the start of any particular impulse that is counted, any additional impulses shall be ignored (that is, not counted) for a period of 100 μs. Each filter is a 2-pole Butterworth low-pass filter with the indicated cut-off (3 dB point) frequency.

Cut-off frequency	Threshold
2 MHz	170 mV
4 MHz	275 mV
10 MHz	560 mV

The impulse noise occurrence rate changes inversely by one decade for each 7 dB change in the threshold voltage. That is, if the noise occurrence rate is 9 counts per 1800 s at a particular threshold voltage, then a rate of 9 counts per 18 000 s will occur at a threshold 7 dB above that voltage. If a count rate of N counts per

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1800 s is measured on a specific cable and filter at the specified voltage threshold, the media noise margin is $7 \log_{10}(9/N)$ dB.

12.7.4.2 Crosstalk

The level of crosstalk noise on a pair depends on the level of the disturbing signal(s) and the crosstalk attenuation from the pair(s) carrying the signal(s). With the maximum transmit level specified in 12.5.3.1, the sinusoidal crosstalk attenuations specified in 12.7.3.1 and 12.7.3.2, and multiple, synchronized, random Manchester disturbers, the peak self-crosstalk (that is, crosstalk from other 1BASE5 signals) noise levels, as measured through the following specified filters, shall be less than or equal to the levels indicated below. Each filter is a 2-pole Butterworth low-pass filter with the indicated cut-off (3 dB point) frequency.

Cut-off frequency	Level
2 MHz	105 mV
4 MHz	160 mV

12.8 Special link specification

12.8.1 Overview

Some 1BASE5 networks may require extension beyond the limits imposed by 12.7 or, due to the installation environment, may require special media such as optical fiber, high-grade cable, or even free-space transmission. The detailed design of special links that replace standard links for use in such circumstances is beyond the scope of this standard, but the end-to-end characteristics are specified. It shall be the responsibility of the supplier to ensure the proper operation of special links with other 1BASE5 equipment.

12.8.2 Transmission characteristics

Special links shall meet the overall attenuation, jitter, and dispersion specifications of 12.7.2.1, 12.7.2.3, and 12.7.2.4, respectively. Total noise introduced due to crosstalk or other sources shall not exceed that allowed for standard media, as specified in 12.7.4. To the extent that it affects operability with 1BASE5 transmitters and receivers, special links shall also meet the impedance and balance requirements of 12.7.2.2 and 12.7.3. The delay and preamble loss allowed for special links is specified in 12.9.4.

12.8.3 Permitted configurations

No more than one special link is permitted in the path between any DTE and the header hub. That is, special links may be installed in parallel but not in series.

NOTE—Special links may be combined with other 1BASE5 components, such as hubs. Such combinations are subject to the performance specifications of this standard only as visible at their external interfaces. For example, explicit MDIs are not required internal to such combinations.

12.9 Timing

12.9.1 Overview

The successful interconnection of multivendor system components mandates that delay and bit loss be allocated fairly and realistically among the various system elements. The balance of this subclause defines the upper limits of delay and bit loss allocated to each component. These values allow proper operation with the

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worst-case system configuration of five levels of hubs, special links, maximum-length cable segments throughout the network, and colliding DTEs at extremes of the network.

12.9.2 DTE timing

DTE Initial Transmit Delay is the time from the first full transition (due to the first OUTPUT_UNIT of preamble) from the MAC to the first full transition (after startup bit loss, if any) at the MDI. This delay shall not exceed 3 BT. The start bit loss shall not exceed 1 bit.

DTEs shall correctly receive frames that are preceded by 13 or more bits of preamble plus 8 bits of <sfd>.

There is a delay between the reception of signal at the PMA input of a DTE and operation of the deferral process in the MAC. Therefore, there is a window in which a DTE may fail to defer to a transmission even after it has arrived at the input. The DTE Deference Delay is the time from the receipt of the first transition of the preamble at the MDI until the last moment that the DTE might start transmitting at the MDI. This delay includes the following components:

a) The delay from the first input transition at the MDI to CARRIER_ON at the PLS-MAC interface
b) The delay through the MAC processes from CARRIER_ON to the last moment that a new transmission would miss being deferred
c) The delay from the first OUTPUT_UNIT at the MAC-PLS interface to the first output transition at the MDI

The DTE Deference Delay shall be no more than 21 BT.

The DTE Collision Shutdown Delay is the time from the first CVL or CVH arriving at the MDI of a transmitting DTE until that DTE transmits IDL at that interface. This time shall be no more than 26 BT + jamSize=58 BT. This limit shall not start until after the <sfd> has been transmitted.

12.9.3 Medium timing

The Medium Transit Delay is the time from when a signal enters the medium until that signal leaves the medium. This delay shall not exceed 4 BT.

12.9.4 Special link timing

The Special Link Transit Delay is the time from when a signal enters a special link until that signal leaves the special link. This delay shall not, exceed 15 BT. The preamble leaving a special link shall be no more than 2 bit cells longer than the preamble sent to that special link and no more than 1 bit cell shorter than the preamble sent to that special link. For the purposes of these limits only, the first bit transmitted shall be considered part of the silence of the preceding IDL unless it meets the requirements for the succeeding bits specified in 12.5.3.1.1 and 12.5.3.1.2.

12.9.5 Hub timing

Hub Startup Delay is the time from when the first bit cell of the preamble arrives at a hub until the first bit cell (also preamble) leaves that hub. This time shall be no greater than 12 BT. The preamble sent by a hub shall be no more than 1 bit cell longer than the preamble sent to that hub or more than 4 bit cells shorter than the preamble sent to that hub. For the purposes of these limits only, the first bit transmitted shall be considered part of the silence of the preceding IDL unless it meets the requirements for the succeeding bits specified in 12.5.3.1.1 and 12.5.3.1.2.

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Hub Idle Collision Startup Delay applies to any case in which CP arrives preceded by fewer (or no) bit times of preamble than the Hub Startup Delay. The time from arrival of the first bit cell (either preamble or CP) until the first bit cell leaves the hub shall be no greater than 12 BT.

Hub Transit Delay is the time from the arrival of any bit cell at a hub to the transmission of the corresponding bit cell from the hub. This delay shall not exceed 9 BT, excluding the cumulative effects of clock tolerance.

The transit (propagation) delay between the upward and downward sides of the Header Hub shall be negligible.

Hub Delay Stretch/Shrink is the increase or decrease in a hub's transit delay due to the effects of differing clock rates. The clock rate tolerance of 0.01% specified in 12.3.2.4.1 and the maximum frame size of 1518 octets specified in 4.4.2.2 yield a maximum stretch or shrink of $(56 + 8 + 1518 \cdot 8) \cdot 0.01\% \cdot 2 < 3$ BT, both at any given hub and through an entire network.

Hub Collision Detect Delay is the time required for a hub to detect multiple incoming signals and initiate transmission of CP. The time until transmission of the first CVH or CVL shall be no greater than 21 BT.

Hub Active Collision Startup Delay is the time from the arrival of the first CVH or CVL of a CP pattern at a hub that is repeating bit cells until transmission of the first CVH or CVL from the hub. This delay shall be no greater than 12 BT in either the upward or downward direction.

Hub Collision Shutdown Delay is the time from IDL arriving at a hub that is passing on or generating CP until that hub starts transmitting IDL. This delay shall be limited to 9 BT. The limit is relaxed to 25 BT, however, for the upward side of a hub that is generating CP. This extra allowance is made to avoid requiring implementation of a separate <etd> detection mechanism in each port of the hub.

12.10 Safety

Implementors are urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate standards. EIA CB8-1981 (see [B22]) provides additional guidance concerning many relevant regulatory requirements.

Sound installation practice, as defined by applicable codes and regulations, shall be followed. ECMA-97 (see [B21]) describes safety requirements for local area networks.

12.10.1 Isolation

Each PMA/MDI interface lead shall be isolated from frame ground. This electrical separation shall withstand at least one of the following electrical strength tests:

a) 1500 V (rms) at 50 to 60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC 60950: 1991.
b) 2250 V (dc) for 60 s, applied as specified in Section 5.3.2 of IEC 60950: 1991.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC 60950: 1991, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 Vdc.

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12.10.2 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 1BASE5 equipment. Other than voice signals (which are very low voltage), the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard that constrains them, the following maximums generally apply:

a) Battery voltage to an on-hook telephone line is about –56 Vdc applied to the line through a balanced 400 Ω source impedance. This voltage is used to power the telephone instrument and detect the off-hook condition. Source inductance can cause large spikes on disconnect.
b) Battery voltage to an off-hook telephone line is also about –56 Vdc applied to the line through a balanced 400 Ω source impedance, but most of the voltage appears across the source impedance because the telephone instrument's impedance is relatively much lower.
c) Ringing voltage is a composite signal. The first portion can be up to 175 V peak at 20 to 66 Hz, limited by a 100 Ω source resistance or a 400 to 600 Ω source inductive impedance. The second portion is –56 Vdc limited by a 300 to 600 Ω source impedance. Large spikes can occur at the start and end of each ring.

Although 1BASE5 equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE—Wiring errors may impose telephony voltages differentially across the 1BASE5 transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, however, receivers will generally appear to the telephone system as off-hook telephones. Full ring voltages, therefore, will be applied for only short periods of time. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to low resistance of the transformer coil.

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13. System considerations for multisegment 10 Mb/s baseband networks

13.1 Overview

This clause provides information on building 10 Mb/s multisegment baseband networks within a single collision domain. The proper operation of a CSMA/CD network requires network size to be limited to control round-trip propagation delay to meet the requirements of 4.2.3.2.3 and 4.4.2.1, and the number of repeaters between any two DTEs to be limited in order to limit the shrinkage of the interpacket gap as it travels through the network.

This clause provides two network models. Transmission System Model 1 is a set of configurations that have been validated under conservative rules and have been qualified as meeting the two requirements set forth above. Transmission System Model 2 is a set of calculation aids that allow a configuration to be qualified against the two requirements. This set of calculation aids allows those configuring a network to test a proposed configuration against a simple set of criteria that allows it to be qualified. The Model 2 Transmission System Model validates an additional broad set of topologies that are fully functional and do not fit within the simpler but more restrictive rules of Model 1.

The physical size of a CSMA/CD network is limited by the characteristics of individual network components. These characteristics include the following:

a) Media lengths and their associated propagation time delay
b) Delay of repeater units (start-up and steady-state)
c) Delay of MAUs (start-up and steady-state)
d) Interpacket gap shrinkage due to repeater units
e) Delays within the DTE associated with the CSMA/CD access method
f) Collision detect and deassertion times associated with MAUs

Table 13–1 summarizes the delays for the various network media segments. In addition, Clause 14 summarizes the delays for the 10BASE-T MAU (Table 14–2); Clause 8, the delays for the 10BASE5 MAU; Clause 10, the delays for the 10BASE2 MAU; Clause 9, the delays of the Fiber Optic Inter Repeater Link (FOIRL) and the repeater (Tables 9–1, 9–2, and 9–3); Clause 16, the delays for the 10BASE-FP MAU (Table 16–1, also see 15.1); Clause 17, the delays for the 10BASE-FB MAU (Table 17–1, also see 15.1), and Clause 18, the delays for the 10BASE-FL MAU (Table 18–1, also see 15.1).

Table 13–1—Delays for network media segments

Media type	Maximum number of MAUs per segment	Maximum segment length (m)	Maximum medium delay per segment (ns)
Mixing segment			
10BASE5	100	500	2165
10BASE2	30	185	950
10BASE-FP	33[a]	1000[b]	5000
Link segment			
FOIRL	2	1000	5000
10BASE-T	2	100[c]	1000
10BASE-FB	2	2000	10 000
10BASE-FL	2	2000	10 000
AUI[d] 1 DTE/1 MAU		50	257

[a]Actual number depends on the passive-star characteristics; see 16.5.2.1.
[b]In addition, a MAU to passive-star link will not exceed 500 m.
[c]Actual maximum segment length depends on cable characteristics; see 14.1.1.3.
[d]AUI is not a segment.

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For a more detailed description of the calculation methods used to arrive at Transmission System Model 2, see B.1.5.

13.1.1 Repeater usage

Repeaters are the means used to connect segments of network medium together, thus allowing larger topologies and a larger MAU base than are allowed by the rules governing individual segments. Different media/segment types can only be connected to each other using repeaters.

13.2 Definitions

See 1.4.

13.3 Transmission System Model 1

The following network topology constraints apply to networks using Transmission System Model 1. If no segment length constraints are given for a segment type, the maximum segment length, as defined in the relevant MAU clause, applies.

a) Repeater sets are required for all segment interconnection.
b) MAUs that are part of repeater sets count toward the maximum number of MAUs on a segment.
c) The transmission path permitted between any two DTEs may consist of up to five segments, four repeater sets (including optional AUIs), two MAUs, and two AUIs.
d) AUI cables for 10BASE-FP and 10BASE-FL shall not exceed 25 m. (Since two MAUs per segment are required, 25 m per MAU results in a total AUI cable length of 50 m per segment.)
e) When a transmission path consists of four repeater sets and five segments, up to three of the segments may be mixing and the remainder must be link segments (Figures 13–1, 13–2, and 13–5). When five segments are present, each fiber optic link segment (FOIRL, 10BASE-FB, or 10BASE-FL) shall not exceed 500 m, and each 10BASE-FP segment shall not exceed 300 m.
f) When a transmission path consists of three repeater sets and four segments (Figures 13–3 and 13–4), the following restrictions apply:
    1) The maximum allowable length of any inter-repeater fiber segment shall not exceed 1000 m for FOIRL, 10BASE-FB, and 10BASE-FL segments and shall not exceed 700 m for 10BASE-FP segments.
    2) The maximum allowable length of any repeater to DTE fiber segment shall not exceed 400 m for 10BASE-FL segments and shall not exceed 300 m for 10BASE-FP segments and 400 m for segments terminated in a 10BASE-FL MAU.
    3) There is no restriction on the number of mixing segments in this case.

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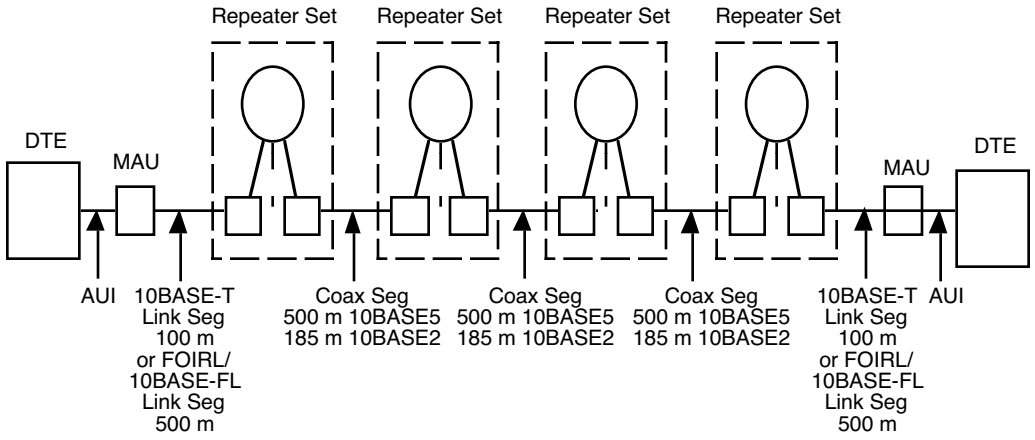


Figure 13–1—Maximum transmission path with three coaxial cable segments and two link segments

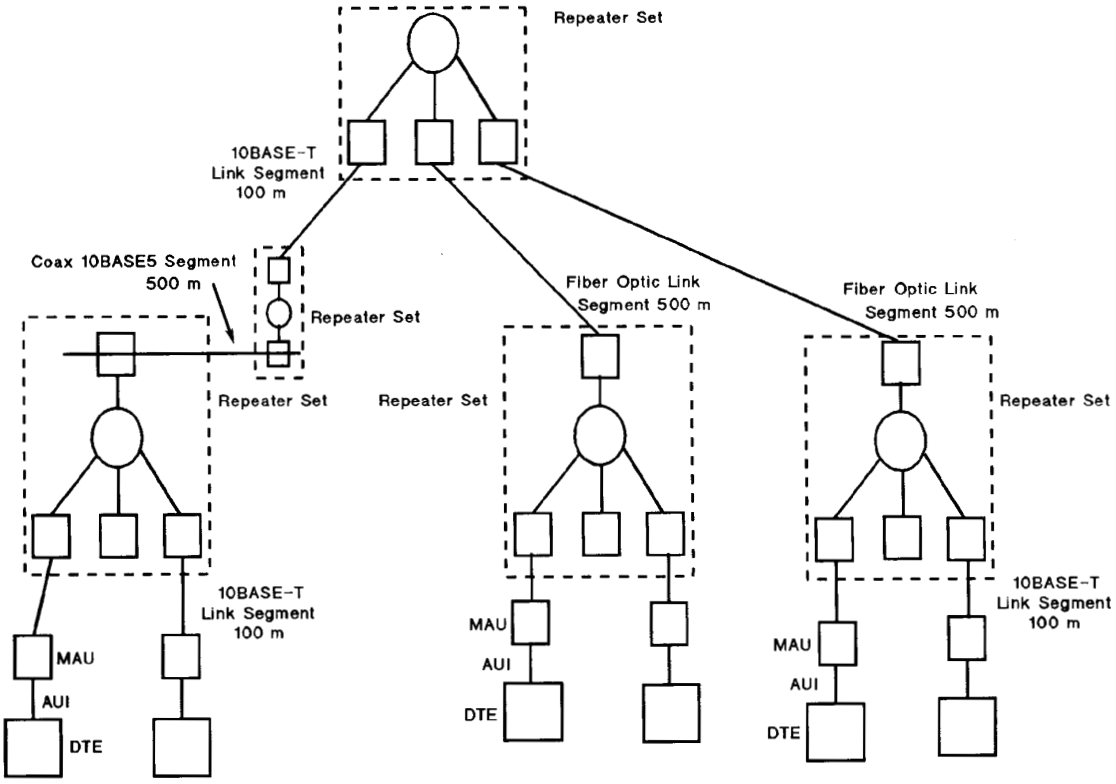


Figure 13–2—Example of maximum transmission path using coaxial cable segments, 10BASE-T link segments, and fiber optic link segments

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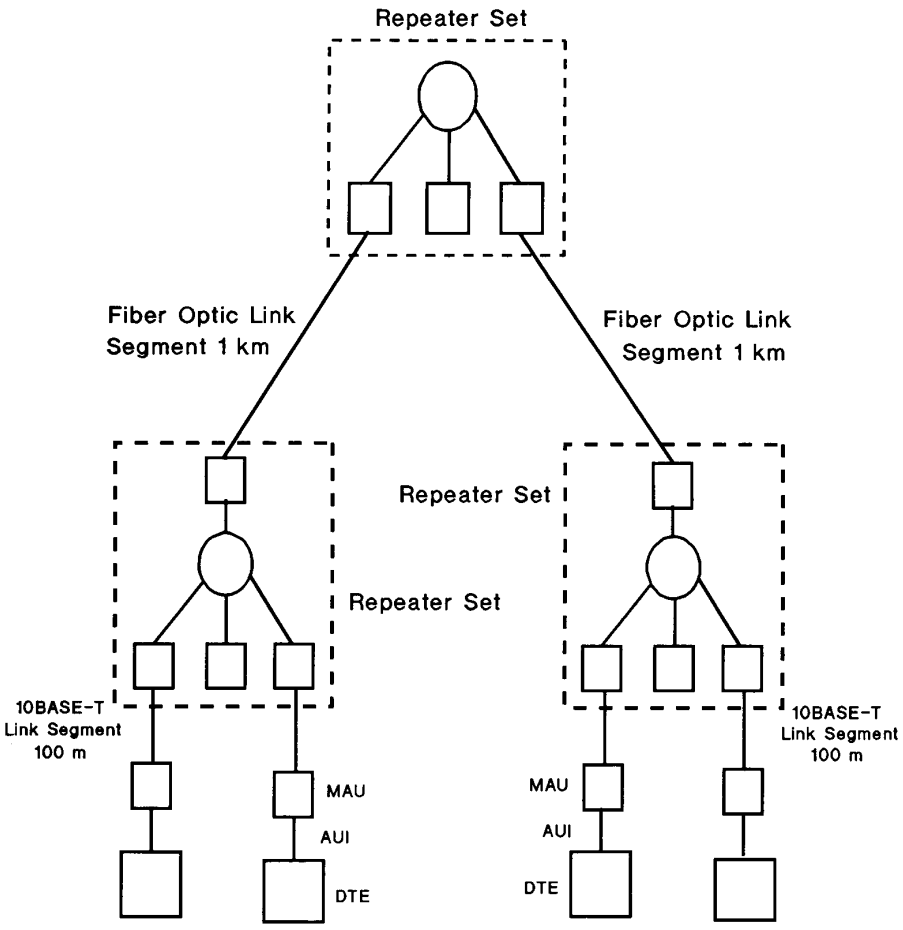


Figure 13–3—Example of maximum transmission path with three repeater sets, four link segments (two are 100 m 10BASE-T and two are 1 km fiber)

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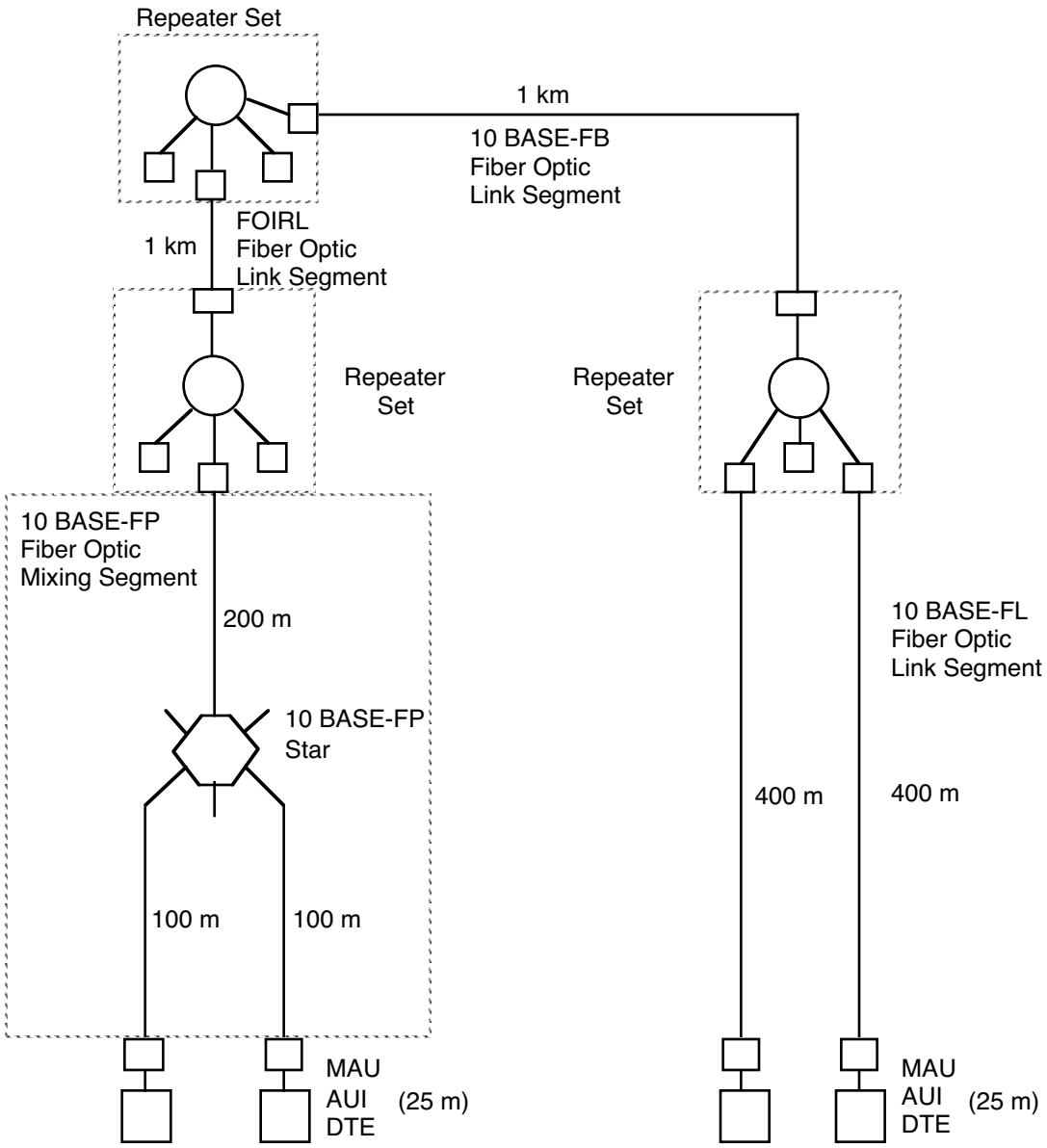


Figure 13–4—Example of maximum transmission path with three repeater sets, four segments (one 1 km 10BASE-FB, one 1 km FOIRL, one 400 m 10BASE-FL, and one 300 m 10BASE-FP)

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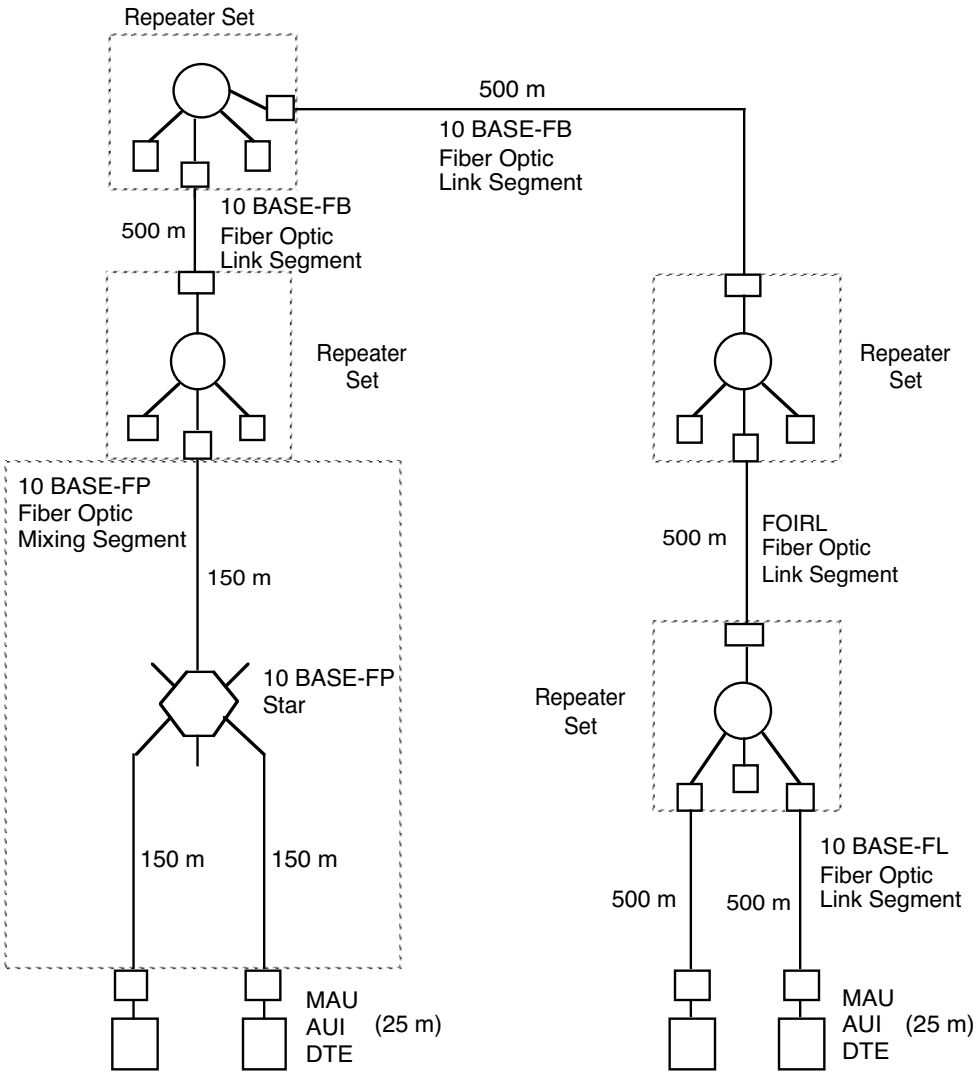


Figure 13–5—Example of maximum transmission path with four repeater sets, five segments (two 500 m 10BASE-FB, one 500 m FOIRL, one 500 m 10BASE-FL, and one 300 m 10BASE-FP)

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13.4 Transmission System Model 2

The physical size and number of topological elements in a 10 Mb/s baseband network is limited by two factors, round-trip collision delay and interpacket gap shrinkage. A network configuration must be validated against each of these separately. A model of the network is required for each of the calculations. The model consists of a series of segments consisting of a left-end segment, mid-segments, and a right-end segment. The model of the network used in the calculations consists of the worst-case path through the network for that particular calculation. The calculations are sufficiently straightforward that they can be done manually. They are also easy to implement in a spreadsheet. In general, the worst-case path for the two calculations is not the same for any single network. The requirements for each calculation and its respective model are detailed in the following subclauses and in Figure 13–6.

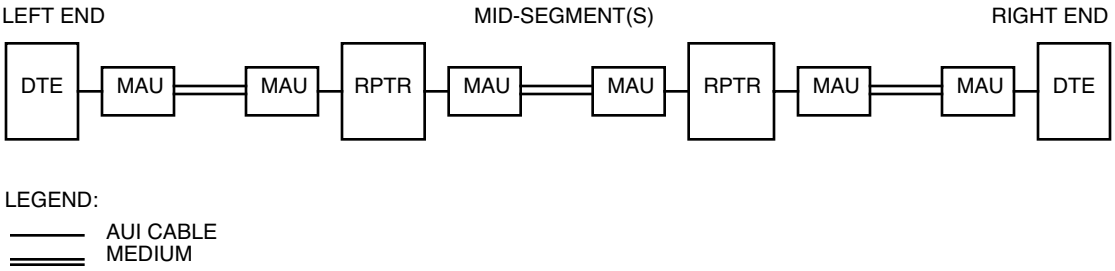


Figure 13–6—Generalized transmission path model

13.4.1 Round-trip collision delay

For a network to be valid, it must be possible for any two DTEs on that network to contend for the network at the same time. Each station attempting to transmit must be notified of the contention by the returned "collision" signal within the "collision window" (see 4.1.2.2 and 5.2.2.1.10). Additionally, the maximum length fragment created must contain less than 511 bits after the Start Frame Delimiter (SFD). This requirement limits the physical diameter (maximum distance between DTEs) of a network. The maximum round-trip delay must be qualified between all pairs of DTEs in the network. In practice this means that the qualification must be done between those that, by inspection of the topology, are candidates for the longest delay.

The following network modeling methodology is provided to assist that calculation.

13.4.1.1 Worst-case path delay value (PDV) selection

The worst-case path through a network to be validated shall be identified. The worst case consists of the path between the two DTEs at opposite ends of the network that have the longest round-trip time (see Figure 13–6).

13.4.1.2 Worst-case PDV calculation

Once a set of paths is chosen for calculation, each shall be checked for validity against the following formulas. (If a candidate for worst-case path has end segments of different types, calculations for the path must be performed twice, considering first one end segment as the left end, and then the other, and the maximum value obtained used as the PDV.)

a) Determine the Segment Delay Value (SDV) from Table 13–2 for each of the segments in the path.

$$SDV = \text{Base} + [\text{Length} * (\text{Round-Trip Delay/meter})]$$

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(For mixing segments, length is the length between the repeater and the farthest end of the segment for end segments, or the length between two repeaters for mid-segments.)

or

$SDV = \text{Max}$

(Max is equal to the value above for the maximum media segment length. It is provided for ease of calculation with segments that are at their maximum length or as a default value when the length is not known).

NOTE—The SDV figure in the table includes allowance for an AUI at each end of the segment (except for 10BASE-FB) and up to 2 m of drop cable. In 10BASE5 segments, AUI cables are normally longer than 2 m. Care should be exercised to assure that provision is made for the delay associated with their actual length.

b) From Table 13–2, determine the SDV for the sum of all AUI cables in excess of 2 m (except the AUI associated with the left end DTE, which does not contribute to the PDV).

c) Sum all SDVs from item a) and item b) plus a margin of up to 5 bits to form the PDV. The margin may be from 0 to 5 bits; 5 bits is recommended. If the PDV is less than or equal to 575, the path is qualified in terms of worst-case delay.

Table 13–2—Segment round-trip delay values in bit times (PDV not to exceed 572)

Segment type	Max length	Left end		Mid-segment		Right end		RT delay/ meter
		Base	Max	Base	Max	Base	Max	
10BASE5 Coax	500	11.75	55.05	46.5	89.8	169.5	212.8	0.0866
10BASE2 Coax	185	11.75	30.731	46.5	65.48	169.5	188.48	0.1026
FOIRL	1000	7.75	107.75	29	129	152	252	0.1
10BASE-T	100[a]	15.25	26.55	42	53.3	165	176.3	0.113
10BASE-FP	1000	11.25	111.25	61	161	183.5	284	0.1
10BASE-FB	2000	N/A[b]	N/A[b]	24	224	N/A[b]	N/A[b]	0.1
10BASE-FL	2000	12.25	212.25	33.5	233.5	156.5	356.5	0.1
Excess length AUI	48	0	4.88	0	4.88	0	4.88	0.1026

[a]Actual maximum segment length depends on cable characteristics; see 14.1.1.3.
[b]Not Applicable, 10BASE-FB does not support end connections.

13.4.2 Interpacket gap (IPG) shrinkage

The worst-case variabilities of transmission elements in the network plus some of the signal reconstruction facilities required in the 10 Mb/s baseband repeater specification combine in such a way that the gap between two packets travelling across the network may be reduced below the interFrameGap specified in 4.4.2.1. This parameter limits the equipment (i.e., number of repeaters) between any two DTEs. Again this limit applies to all combinations of DTEs on any network but the worst case is apparent from an inspection of a map or schematic representation of the topology in question.

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13.4.2.1 Worst-case path variability value (PVV) selection

A worst-case path through a network to be validated shall be identified.

It should be noted that the receive end segment is not counted in this scenario. This means that in an asymmetrical network where the end segments are of different types, the end segment with the worst variability shall be designated as the "Transmitting End" for this evaluation.

13.4.2.2 Worst-case path variability value (PVV) calculation

Once a set of paths is chosen for calculation each shall be checked for qualification by the following method:

a) Determine the Segment Variability Value (SVV) from Table 13–3 for each of the segments in the Path, excluding the end segment with the lower SVV.
b) Sum all of the SVVs from item 1 to form the PVV. If the PVV is less than or equal to 49, the path is qualified in terms of worst-case variability.

Table 13–3—Segment variability values in bit times (PVV not to exceed 49)

Segment type	Transmitting end	Mid-segment
Coax	16	11
Link except 10BASE-FB	10.5	8
10BASE-FB	N/A[a]	2
10BASE-FP	11	8

[a]Not Applicable, 10BASE-FB does not support end connections.

13.5 Full duplex topology limitations

Unlike half duplex CSMA/CD networks, the physical size of full duplex 10 Mb/s networks is not limited by the round-trip collision propagation delay. Instead, the maximum link length between DTEs is limited only by the signal transmission characteristics of the specific cable.

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14. Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T

14.1 Scope

14.1.1 Overview

Clause 14 defines the functional, electrical, and mechanical characteristics of the type 10BASE-T MAU and one specific medium for use with that MAU. The relationship of this clause to the entire ISO/IEC 8802-3 LAN International Standard is shown in Figure 14–1. The purpose of the MAU is to provide a simple, inexpensive, and flexible means of attaching devices to the medium.

This MAU and medium specification is aimed primarily at office applications where twisted-pair cable is often installed. Installation and reconfiguration simplicity is allowed by the type of cable and connectors used.

The 10BASE-T specification builds upon Clauses 1 through 7 and Clause 9 of this standard.

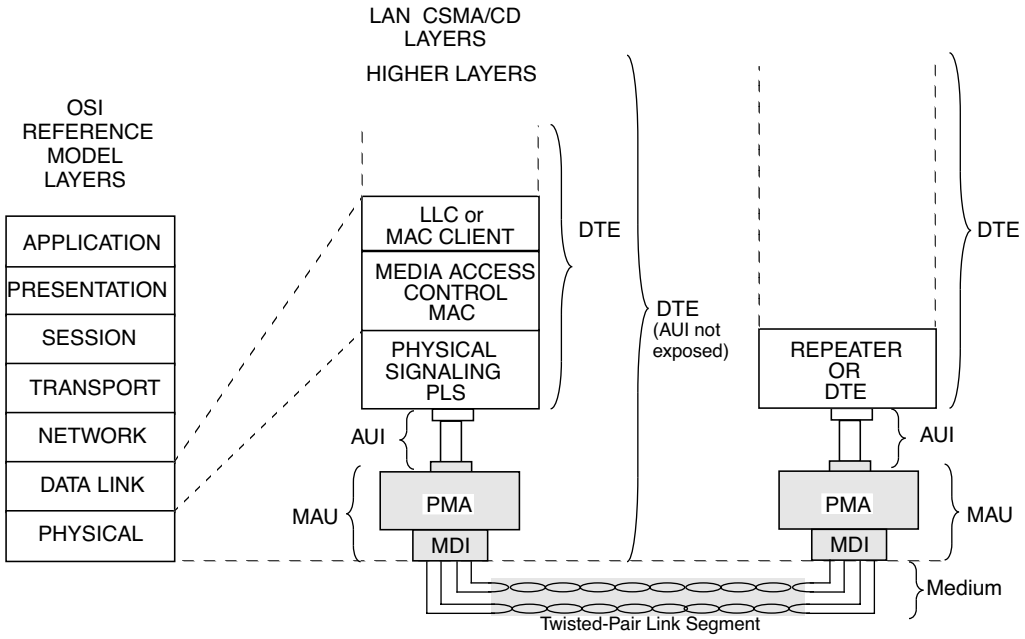


Figure 14–1—10BASE-T relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

14.1.1.1 Medium Attachment Unit (MAU)

The MAU has the following general characteristics:

a) Enables coupling the Physical Signaling (PLS) sublayer by way of the Attachment Unit Interface (AUI) to the baseband twisted-pair link defined in Clause 14.
b) Supports message traffic at a data rate of 10 Mb/s.
c) Provides for operating over 0 m to at least 100 m of twisted pair without the use of a repeater.
d) Permits the Data Terminal Equipment (DTE) or repeater to confirm operation of the MAU and availability of the medium.

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e) Supports network configurations using the CSMA/CD access method defined in this standard with baseband signaling.
f) Supports a point-to-point interconnection between MAUs and, when used with repeaters having multiple ports, supports a star wiring topology.
g) Allows incorporation of the MAU within the physical bounds of a DTE or repeater.
h) Allows for either half duplex operation, full duplex operation, or both.

14.1.1.2 Repeater unit

The repeater unit is used to extend the physical system topology and provides for coupling two or more segments. Repeaters are an integral part of all 10BASE-T networks with more than two DTEs (see Figures 13–1 and 13–2). The repeater unit is defined in Clause 9. Multiple repeater units are permitted within a single collision domain to provide the maximum connection path length specified in Clause 13. The repeater unit is not a DTE and therefore has slightly different requirements for its attached MAUs, as defined in 9.4.1. Repeater sets with 10BASE-T MAUs are required to provide the auto-partition/reconnection algorithm on those ports, as specified in 9.6.6.2.

14.1.1.3 Twisted-pair media

The medium for 10BASE-T is twisted-pair wire. The performance specifications of the simplex link segment are contained in 14.4. This wiring normally consists of 0.4 mm to 0.6 mm diameter [26 AWG to 22 AWG] unshielded wire in a multipair cable. The performance specifications are generally met by 100 m of 0.5 mm telephone twisted pair. Longer lengths are permitted providing the simplex link segment meets the requirements of 14.4. A length of 100 m, the design objective, will be used when referring to the length of a twisted-pair link segment.

14.1.2 Definitions

See 1.4.[24]

14.1.2.1<=0>twisted-pair link: A twisted-pair link segment and its two attached MAUs (see Figure 14–2).

14.1.2.2<=0>twisted-pair link segment (duplex link segment): Two simplex link segments for connecting two MAUs (see Figure 14–2).

14.1.3 Application perspective

This clause states the broad objectives and assumptions underlying the specifications defined throughout Clause 14.

14.1.3.1 Objectives

a) Provide the physical means for communication between LAN Data Link Layer Entities.
b) Ensure compatibility of independently developed physical and electrical interfaces.
c) Provide a communication channel with a mean bit error rate, at the physical layer service interface of less than one part in 10^8.
d) Provide for ease of installation and service.
e) Ensure that fairness of DTE access is not compromised.
f) Provide for low-cost networks, as related to both equipment and cabling.
g) Make use of telephone twisted-pair building wiring and telephony wiring practices.

[24]The definitions included in this subclause are a topic under consideration for maintenance work. They are not included in 1.4.

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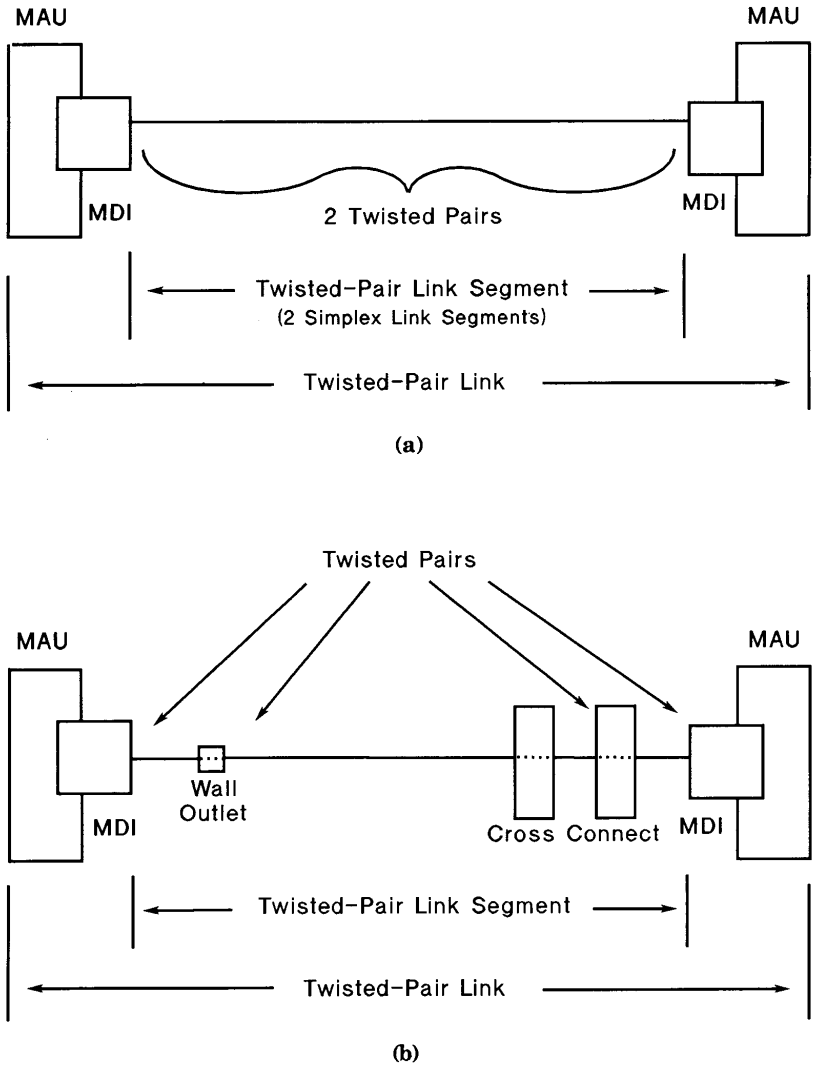


Figure 14–2—Twisted-pair link

14.1.3.2 Compatibility considerations

All implementations of the twisted-pair link shall be compatible at the MDI. The MAU and the medium are defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the MAU in an application-dependent manner provided the MDI and AUI (when implemented) specifications are met.

14.1.3.3 Modes of operation

The 10BASE-T MAU is capable of operating in *normal* mode only (see 7.1.4). The MAU shall not operate in *monitor* mode.

When normal mode is in operation, the MAU functions as a direct connection between the medium and the DTE or repeater. Data from the DTE or repeater is output to one of the simplex link segments of the link segment, and data received on the other simplex link segment is input to the DTE or repeater.

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The operation of a 10BASE-T MAU differs depending on whether the attached DTE is operating in the half duplex or full duplex mode (see 1.1.1). In the full duplex mode, functions relating to the loopback of transmitted data (DO) onto the receive path (DI) are disabled (see 14.2.1.3 and 14.2.1.6). The requirements specified in subclauses of this standard labeled "half duplex mode only" do not apply to a MAU used with a DTE configured for full duplex operation.

14.1.4 Relationship to PLS and AUI

A close relationship exists between Clause 14 and Clause 7. Clause 14 specifies the physical medium parameters and the PMA logical functions residing in the physical MAU. The MAU provides services to the PLS defined in Clause 7 by means of the AUI. 10BASE-T MAUs support a subset of the AUI services specified in Clause 7. 10BASE-T MAUs do not support the optional isolate function, the optional CO circuit, or the optional CS1 signal on the CI circuit.

The design of an external MAU component requires the use of both Clause 14 and Clause 7 for the PLS and AUI specifications.

The figures and numerous textual references throughout Clause 14 refer to terminology associated with the AUI (that is, DO, DI, and CI). Since an embodiment of the 10BASE-T MAU does not require the implementation of an AUI, the DO, DI, and CI circuits may not physically exist. However, they are logically present and MAU operation is defined in terms of them.

14.2 MAU functional specifications

The MAU provides the means by which signals on the three AUI signal circuits to and from the DTE or repeater and their associated interlayer messages are coupled to the twisted-pair link segment. The MAU provides the following functional capabilities to handle message flow between the DTE or repeater and the twisted-pair link segment:

a) Transmit function. Provides the ability to transfer Manchester-encoded data from the DO circuit to the TD circuit. While not sending Manchester-encoded data on the TD circuit, the MAU sends an idle signal, TP_IDL, on the TD circuit.
b) Receive function. Provides the ability to transfer Manchester-encoded data from the RD circuit to the DI circuit. While not sending Manchester-encoded data on the DI circuit, the MAU sends an idle signal, IDL, on the DI circuit.
c) Loopback function (half duplex mode only). Provides the ability to transfer Manchester-encoded data from the DO to the DI circuit when the MAU is sending Manchester-encoded data to the TD circuit.
d) Collision Presence function. Provides the ability to detect simultaneous occurrence of Manchester-encoded data on the RD and DO circuits and to report such an occurrence as a collision. MAUs connected to full duplex mode DTEs are permitted, but not required, to implement the Collision Presence function.
e) *signal_quality_error* Message (SQE) Test function. Provides the ability to indicate to the DTE that the Collision Presence function is operational and that the *signal_quality_error* message can be sent by the MAU.
f) Jabber function. Provides the ability to prevent abnormally long reception of Manchester-encoded data on the DO circuit from indefinitely disrupting transmission on the network. While such a condition is present, transfer of Manchester-encoded data by the Transmit and Loopback functions is disabled.
g) Link Integrity Test function. Provides the ability to protect the network from the consequences of failure of the simplex link attached to the RD circuit. While such a failure is present, transfer of Manchester-encoded data by the Transmit, Receive, and Loopback functions is disabled.

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h) Auto-Negotiation. Optionally provides the capability for a device at one end of a link segment to advertise its abilities to the device at the other end (its link partner), to detect information defining the abilities of the link partner, and to determine if the two devices are compatible.

14.2.1 MAU functions

The MAU shall provide the Transmit, Receive, Loopback, Collision Presence, Jabber, and Link Integrity Test functions for half duplex mode DTEs and repeater units. The MAU shall provide the Transmit, Receive, Jabber, and Link Integrity Test functions, and shall not provide the Loopback function for full duplex mode DTEs. The SQE Test function shall be performed by MAUs that are connected to half duplex DTEs and shall not be performed by MAUs that are connected to repeaters.

MAUs connected to full duplex mode DTEs are permitted, but not required, to implement the Collision Presence function, the SQE Test function, and the generation of the CS0 signal on the CI circuit by the Jabber function. If these optional capabilities are implemented in a MAU connected to a full duplex mode DTE, either all of the optional functions shall be implemented, or none of them shall be.

The MAU function requirements are summarized in the table below:

MAU connected to:			
Functions	**Repeater**	**Half duplex DTE**	**Full duplex DTE**
Transmit	Required	Required	Required
Receive	Required	Required	Required
Loopback	Required	Required	Required
Jabber	Required	Required	Required
Link Integrity Test	Required	Required	Required
Collision Presence	Required	Required	Optional (Note 2)
SQE Test	Required	Required	Optional (Note 2)
Generation of CS0 signal on the CI circuit by jabber	Required	Required	Optional (Note 2)

NOTE 1—The functional requirements of a MAU connected to a full duplex DTE are a proper subset of the requirements for half duplex operation.

NOTE 2—Optional capabilities, if implemented, must be implemented as a group (i.e., all or none).

A capability may be provided in the MAU to activate or inhibit the SQE Test function, or to configure the MAU for full or half duplex operation. It is not required that a MAU determine that it is connected to either a DTE or a repeater and automatically activate or inhibit the SQE Test function. It is also not required that a MAU determine that it is connected to either a half duplex or full duplex DTE and automatically activate or inhibit the appropriate functions for those modes. The use of the Auto-Negotiation algorithm of Clause 28 in 10BASE-T MAUs is discussed in 14.2.1.8. The MAU may optionally provide the Auto-Negotiation algorithm. When provided, the Auto-Negotiation algorithm shall be implemented in accordance with Clause 28.

14.2.1.1 Transmit function requirements

The MAU shall receive the signals on the DO circuit and send them to the TD circuit of the MDI. A positive signal on the A lead relative to the B lead of the DO circuit shall result in a positive signal on the TD+ (Transmit Data +) lead of the MDI with respect to the TD– lead.

At the start of a packet transmission, no more than 2 bits may be received from the DO circuit and not transmitted on the TD circuit. In addition, it is permissible for the first bit sent to contain phase violations or invalid amplitude. All subsequent bits of the packet shall be reproduced with the differential voltage specified in 14.3.1.2.1 and with no more jitter than is specified in 14.3.1.2.3. The second bit transmitted on the TD

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circuit shall be transmitted with the correct timing and signal levels. The steady-state propagation delay between the DO circuit input and the TD circuit shall not exceed 2 BT.

For any two packets that are separated by 9.6 μs or less, the start-up delay (bit loss plus steady-state propagation delay) of the first packet shall not exceed that of the second packet by more than 2 BT.

Whenever data is not being transmitted on the TD circuit, an idle signal, TP_IDL, shall be transmitted on the TD circuit. TP_IDL is a start of idle, as defined in 14.3.1.2.1, followed by a repeating sequence of a 16 ms ± 8 ms period of silence (the time where the differential voltage remains at 0 mV ± 50 mV) and a link test pulse (see 14.3.1.2.1). Following a packet and start of idle, the repeating sequence shall start with a period of silence.

Transmission of TP_IDL may be terminated at any time with respect to the link test pulse. It shall be terminated such that no more than the first transmitted bit of a packet is corrupted, and with no more delay than is specified for bit loss and steady-state propagation.

For a MAU that implements the Auto-Negotiation algorithm defined in Clause 28, Clause 28 shall define the allowable transmitted link pulse sequence.

14.2.1.2 Receive function requirements

The MAU shall receive the signals on the RD circuit of the MDI and send them to the DI circuit. A positive signal on the RD+ (Receive Data +) lead relative to the RD– lead of the MDI shall result in a positive signal on the A lead with respect to the B lead of the DI circuit.

At the start of a packet reception from the RD circuit, no more than 5 bits may be received on the RD circuit and not transmitted onto the DI circuit. In addition, it is permissible for the first bit sent on the DI circuit to contain phase violations or invalid data; however, all successive bits of the packet shall be sent with no more than the amount of jitter specified in 14.3.1.3.1. The steady-state propagation delay between the RD circuit and the DI circuit shall not exceed 2 BT.

For any two packets that are separated by 9.6 μs or less, the start-up delay of the first packet shall not exceed that of the second packet by more than 2 BT.

14.2.1.3 Loopback function requirements (half duplex mode only)

When the MAU is transmitting on the TD circuit and is not receiving *RD_input* messages (14.2.2.4) on the RD circuit, the MAU shall transmit on the DI circuit the signals received on the DO circuit in order to provide loopback of the transmitted signal. At the start of packet transmission on the TD circuit, no more than 5 bits of information may be received from the DO circuit and not transmitted to the DI circuit. In addition, it is permissible for the first bit sent on the DI circuit to contain phase violations or invalid data; however, all successive bits of the packet shall meet the jitter specified in 14.3.1.3.1 (that is, 13.5 ns plus 1.5 ns). The steady-state propagation delay between the DO circuit and the DI circuit shall not exceed 1 BT.

14.2.1.4 Collision Presence function requirements (half duplex mode only)

The MAU shall detect as a collision the simultaneous occurrence of activity on the DO circuit and the RD circuit while in the Link Test Pass state. While a collision is detected, a CS0 signal (see 7.3.1.2) shall be sent on the CI circuit. The signal shall be presented to the CI circuit no more than 9 BT after the occurrence of a collision. The signal shall be deasserted within 9 BT after the DO circuit or the RD circuit changes from active to idle.

When CS0 is asserted on the CI circuit due to a collision, the data on the RD circuit shall be sent to the DI circuit within 9 BT.

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When the RD circuit changes from active to idle and data is present on the DO circuit, the data on the DO circuit shall be sent to the DI circuit within 9 BT.

The signal presented on the CI circuit in the absence of collision, SQE test, or Jabber shall be the IDL signal.

MAUs connected to full duplex mode DTEs are permitted, but not required, to implement the Collision Presence function (see 14.2.1).

14.2.1.5 *signal_quality_error* Message (SQE) Test function requirements

The SQE Test function shall be performed by MAUs that are connected to DTEs in half duplex mode, and shall not be performed by MAUs that are connected to repeaters. When the SQE test is performed, the MAU shall send CS0 on the CI circuit for a time "SQE_test" beginning a time "SQE_test_wait" after the last positive transition of a packet on the DO circuit. The value of "SQE_test" shall be 10 BT ± 5 BT and the value of "SQE_test_wait" shall be between 0. μs and 1.6 μs. This function should use as much of the normal collision detection and signaling circuitry as possible without introducing extraneous signals on the TD circuit or the DI circuit.

The CS0 signal shall not be sent by the SQE Test function while in any of the Link Test Fail states.

MAUs connected to full duplex mode DTEs are permitted, but not required, to implement the SQE Test function (see 14.2.1).

14.2.1.6 Jabber function requirements

The MAU shall contain a self-interrupt capability to prevent an illegally long transmission by a DTE from permanently disrupting transmission on the network and to disable loopback to the DI circuit (Figure 14–5). The MAU shall provide a window "xmit_max" during which time the Transmit function may continuously transmit *TD_output* messages to the TD circuit. The value of "xmit_max" shall be between 20 and 150 ms. If a transmission exceeds this duration, the Jabber function shall

a) Inhibit the Loopback function and the transmission of *TD_output* messages by the Transmit function, and shall
b) Send the CS0 signal on the CI circuit, when the MAU is connected to a DTE operating in half duplex mode. MAUs connected to DTEs operating in full duplex mode are permitted, but not required, to send the CS0 signal on the CI circuit in this manner (see 14.2.1).

These actions shall continue until *output_idle* has been continuously present on the DO circuit for a time "unjab." The value of "unjab" shall be 0.5 ± 0.25 s.

It is permissible to activate the Jabber function when the TD circuit transmitter is sending *TD_output* messages for longer than "xmit_max."

The MAU shall not activate its Jabber function when the repeater's MAU Jabber Lockup Protection function operates at its longest permitted time as specified in 9.6.5.

14.2.1.7 Link Integrity Test function requirements

In order to protect the network from the consequences of a simplex link segment failure, the MAU shall monitor the RD circuit for *RD_input* and link test pulse activity. If neither *RD_input* nor a link test pulse is received for a time "link_loss," the MAU shall enter the Link Test Fail state and cause the *input_idle* message to be sent on the DI circuit and the *TD_idle* message to be sent on the TD circuit (Figure 14–6). The value of "link_loss" shall be between 50 ms and 150 ms. When RD_input or a number "lc_max" of consec-

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utive link test pulses is received on the RD circuit, the MAU shall exit the Link Test Fail state. The value of "lc_max" shall be between 2 and 10 inclusive.

Only link test pulses that occur within time "link_test_max" of each other shall be considered consecutive. The value of "link_test_max" shall be between 25 ms and 150 ms. In addition, detected pulses that occur within a time "link_test_min" of a previous pulse or packet shall be ignored while in the Link Test Pass state. In the Link Test Fail state, such pulses shall reset the counted number of consecutive link test pulses to zero. The value of "link_test_min" shall be between 2 ms and 7 ms. Re-enabling shall be deferred until the signals on the RD and DO circuits become idle. The MAU shall not detect a link test pulse as *RD_input*. Additionally, a MAU may exit the Link Test Fail Extend state and enter the Link Test Pass state when the RD circuit becomes idle and the Jabber function has disabled transmission on the TD circuit.

While the MAU is not in the Link Test Pass state, the Link Integrity Test function shall disable the bit transfer of the Transmit, Receive, and Loopback functions, and the Collision Presence and SQE Test functions.

At PowerOn, in place of entering the Link Test Pass state as shown in Figure 14–6, a MAU may optionally enter the Link Test Fail Reset state.

For a MAU that implements the Auto-Negotiation algorithm defined in Clause 28, the MAU shall enter the LINK TEST FAIL RESET state at power-on as specified in Clause 28. For a MAU that does not implement the Auto-Negotiation algorithm defined in Clause 28, it is highly recommended that it also power-on in the LINK TEST FAIL RESET state, although implementations may power-on in the LINK TEST PASS state. For a MAU that implements the Auto-Negotiation function defined in Clause 28, the Auto-Negotiation Technology Dependent Interface shall be supported. Supporting the Technology Dependent Interface requires that in the Link Integrity Test function state diagram "link_status=OK" is added to the LINK TEST PASS state and "link_status=FAIL" is added to the LINK TEST FAIL RESET state. Note these ISO message variables follow the conventions of Clause 21.

If a visible indicator is provided on the MAU to indicate the link status, it is recommended that the color be green and that the indicator be labeled appropriately. It is further recommended that the indicator be on when the MAU is in the Link Test Pass state and off otherwise.

14.2.1.8 Auto-Negotiation

It is strongly recommended that Auto-Negotiation be used for the determination of half or full duplex operation. When Auto-Negotiation is used in an exposed AUI-based MAU implementation, the MAU must be capable of operating in the half duplex mode, and shall not advertise the ability to operate in full duplex mode.

10BASE-T MAUs used in an embedded system (i.e., where the MAU is incorporated within the physical bounds of the DTE), or incorporating a physical implementation of the MII interface of Clause 22 with a DTE operating in full duplex mode, may indicate the capability to operate in full duplex mode using the Auto-Negotiation algorithm in accordance with Clause 28.

NOTE—Since there is no way to communicate the half or full duplex abilities between a DTE or repeater and a MAU separated by an AUI, caution must be used when connecting full duplex capable DTEs or MAUs that are manually configured.

Manual configuration is not recommended. Connecting incompatible DTE/MAU combinations such as a full duplex mode DTE to a half duplex mode MAU, or a full-duplex mode station (DTE and MAU) to a repeater or other half duplex network, can lead to severe network performance degradation, increased collisions, late collisions, CRC errors, and undetected data corruption.

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14.2.2 PMA interface messages

The messages between the PLS in the DTE and the PMA in the MAU shall comply with the PMA interface messages described in 7.2.1. These messages also are used in repeater unit to PMA communication. These and the messages between the PMAs over the MDI are summarized below.

14.2.2.1 PLS to PMA messages

The following messages are sent by the PLS in the DTE or repeater to the PMA in the MAU:

Message	Circuit	Signal	Meaning
output	DO	CD1,CD0	Output information
output_idle	DO	IDL	No data to be output

14.2.2.1.1 PMA to PLS messages

The following messages are sent by the MAU to the PLS in the DTE or repeater:

Message	Circuit	Signal	Meaning
input	DI	CD1,CD0	Input information
input_idle	DI	IDL	No information to input
mau_available	CI	IDL	MAU is available for output
signal_quality_error	CI	CS0	Error detected by MAU

Retiming of CD1 and CD0 signals within the MAU is neither prohibited nor required. Considerable jitter may be present (see 14.3.1.3.1).

14.2.2.2 PMA to twisted-pair link segment messages

Message	Circuit	Signal	Meaning
TD_output	TD	CD1,CD0	Output information
TD_idle	TD	TP_IDL	No information to output

The encoding for TP_IDL is defined in 14.2.1.1. The encoding for CD1 and CD0 is the same as that used on the AUI. Retiming of CD1 and CD0 signals within the MAU is neither prohibited nor required.

14.2.2.3 Twisted-pair link segment to PMA messages

Message	Circuit	Signal	Meaning
RD_input	RD	CD1,CD0	Input information
RD_idle	RD	TP_IDL	No information to input

The encoding for TP_IDL is defined in 14.2.1.1. The encoding for CD1 and CD0 is the same as that used on the AUI.

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14.2.2.4 Interface message time references

Delay and bit loss specifications are measured from the occurrence of messages at the MDI and MAU AUI. The following describes the point where each message starts:

Message	Reference
output	leading bit cell boundary (BCB) of first valid CD1 or CD0
output_idle	last positive-going transition prior to start of IDL
input	leading BCB of first valid CD1 or CD0
input_idle	last positive-going transition prior to start of IDL
signal_quality_error	first transition of valid amplitude
mau_available	last positive-going transition prior to start of IDL
TD_output	leading BCB of first valid CD1 or CD0
TD_idle	last positive-going transition prior to start of TP_IDL
RD_output	leading BCB of first valid CD1 or CD0
RD_idle	last positive-going transition prior to start of TP_IDL

14.2.3 MAU state diagrams

The state diagrams of Figures 14–3a), 14–3b), 14–4, 14–5, and 14–6 depict the full set of allowed MAU state functions relative to the circuits of the AUI and MDI.

The notation used in the state diagrams follows the conventions in 1.2.1. The variables and timers used in the state diagrams are defined in the following subclauses.

14.2.3.1 State diagram variables

Variables are used in the state diagrams to indicate the status of MAU inputs and outputs, to control MAU operation, and to pass state information between functions.

In the variable definitions, the name of the variable is followed by a brief description of the variable and a list of values the variable may take. For those variables that are state diagram outputs, one value will be identified as the default. The variable has the default value when no active state contains a term assigning a different value.

For example, the variable “xmit” has the value “disable” whenever the Jabber function or the Link Integrity Test function is in a state that asserts “xmit=disable.” The variable has the default value “enable” all other times.

The variables used in the state diagrams are defined as follows:

DI. Controls the signal sent by the MAU on the DI circuit.
Values:idle; MAU is sending *input_idle*, IDL (default).
DO; MAU sends the signal received on the DO circuit.
lpbk = disable overrides this and causes *input_idle* to be sent.
RD; MAU sends the signal received on the RD circuit.
rcv = disable overrides this and causes *input_idle* to be sent.

CI. Controls the signal sent by the MAU on the CI circuit.
Values:idle; MAU sends *mau_available*, IDL (default).

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SQE; MAU sends *signal_quality_error*, CS0.

DO. Status of the signal received by the MAU on the DO circuit.
Values:idle; MAU is receiving *output_idle*, IDL.
active; MAU is receiving *output*, CD0 or CD1.

TD. Controls the signal sent by the MAU on the TD circuit.
Values:idle; MAU sends *TD_idle*, TP_IDL (default).
DO; MAU sends the signal received on the DO circuit.
xmit = disable overrides this and causes *TD_idle* to be sent.

RD. Status of the signal received by the MAU on the RD circuit.
Values:idle; MAU is receiving silence or a link test pulse.
active; MAU is detecting signals which meet the requirements of 14.3.1.3.2.

link_test_rcv. Status of the link test signal received by the MAU on the RD circuit.
Values:false; MAU is not detecting a link test pulse.
true; MAU is detecting a link test pulse.

link_count. Count of the number of consecutive link test pulses received while in the Link Fail state.
Values:non-negative integers.

lc_max. The number of consecutive link test pulses required before exit from the Link Fail state.
Values:positive integer between 2 and 10 inclusive.

rcv. Controls the path from the RD circuit to the DI circuit.
Values:enable; receive is enabled (default).
disable; the output to the DI circuit is *input_idle* when DI=RD.

lpbk. Controls the path from the DO circuit to the DI circuit.
Values:enable; loopback is enabled (default).
disable; the output to the DI circuit is *input_idle* when DI=DO.

xmit. Controls the path from the DO circuit to the TD circuit.
Values:enable; transmit is enabled (default).
disable; transmit is disabled and the signal sent on the TD circuit is TP_IDL.

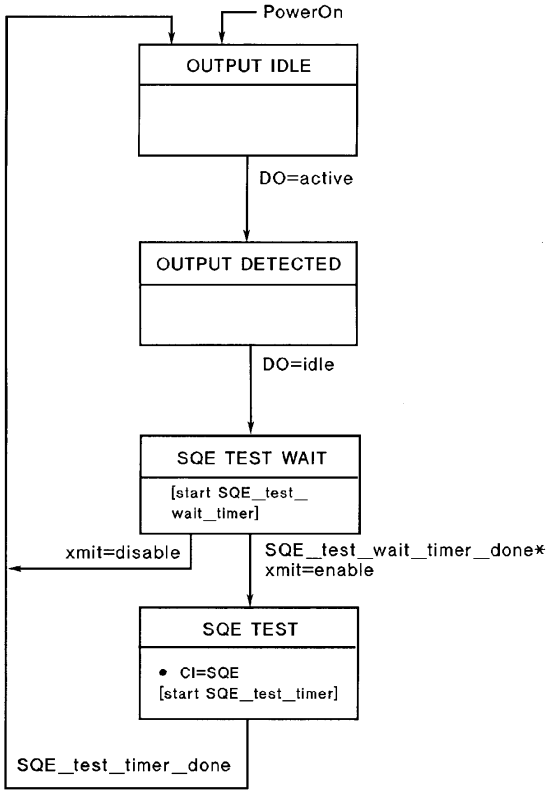
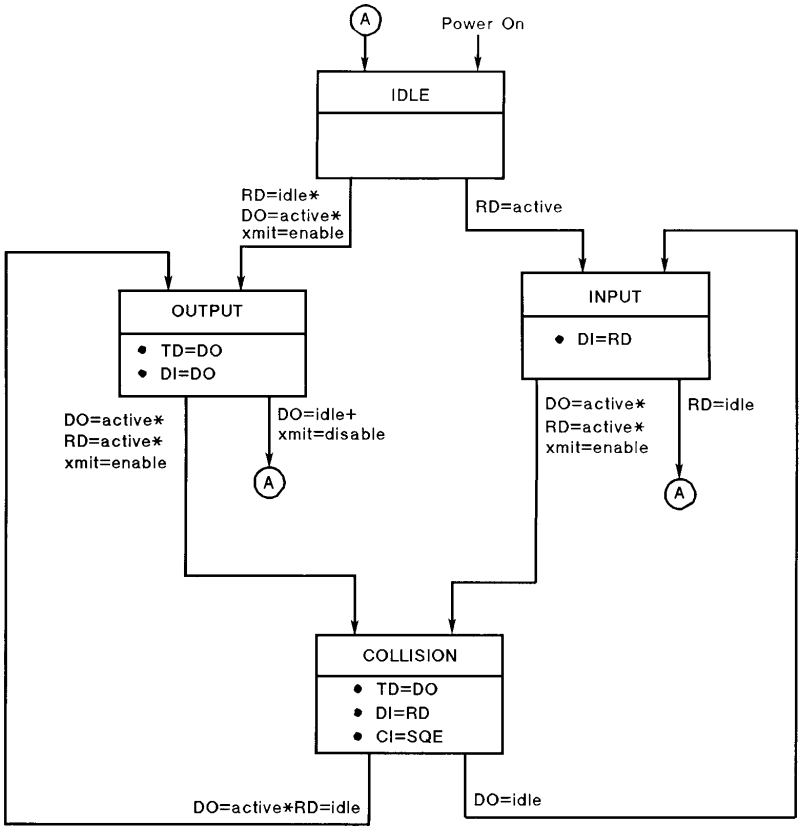


Figure 14–4—*signal_quality_error* Message Test function state diagram

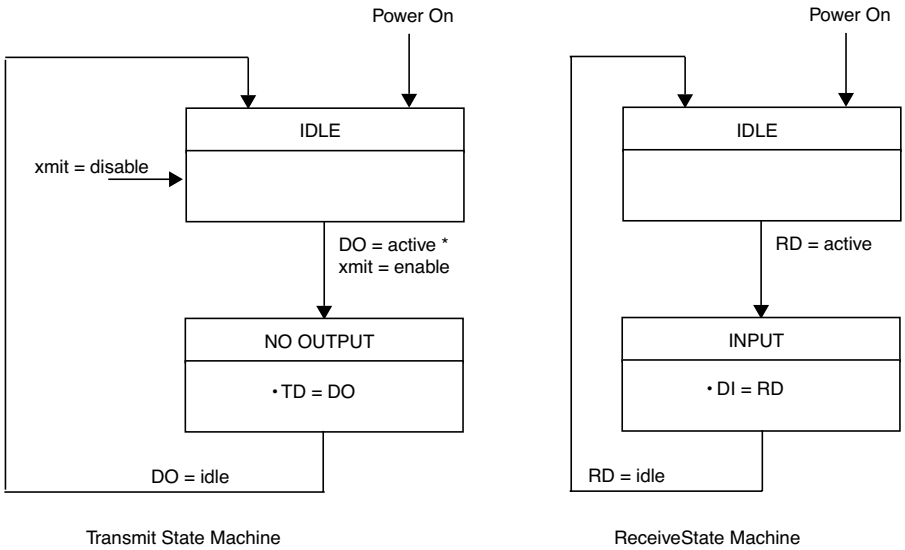
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a) MAU Transmit, Receive, Loopback, and Collision Presence functions (half duplex mode)



b) MAU Transmit and Receive functions (full duplex mode)

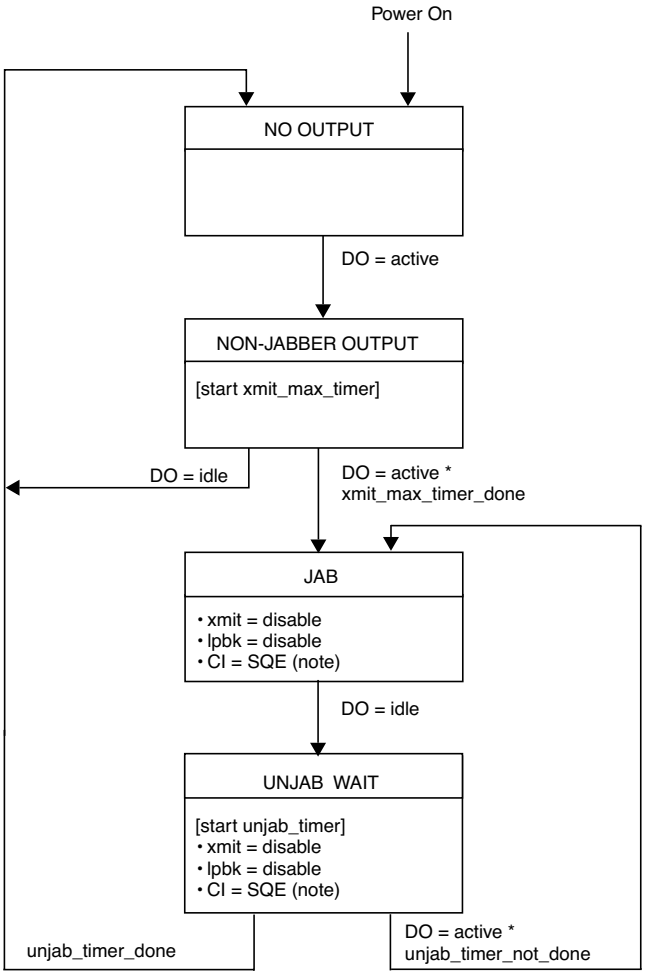
Figure 14–3—MAU state diagrams

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NOTE 1— Sending SQE on CI is optional for MAUs connected to DTEs operating in full duplex mode.

NOTE 2—The implementation of the Collision Presence function is not required in a MAU connected to a full duplex mode DTE, and is not shown in Figure 14–3b).

NOTE 3—The implementation of the SQE Test function shown in Figure 14–4 is not required in a MAU connected to a full duplex mode DTE.

NOTE 4—The enabling of the variable *lpbk* in Figure 14–6 is applicable only in half duplex mode.

Figure 14–5—Jabber function state diagram

14.2.3.2 State diagram timers

All timers operate in the same fashion. A timer is reset and starts counting upon entering a state where "start x_timer" is asserted. Time "x" after the timer has been started, "x_timer_done" is asserted and remains asserted until the timer is reset. At all other times, "x_timer_not_done" is asserted.

When entering a state where "start x_timer" is asserted, the timer is reset and restarted even if the entered state is the same as the exited state; for example, when in the Link Test Pass state of the Link Integrity Test function state diagram, the "link_loss_timer" and the "link_test_min_timer" are reset each time the term "RD = active + (link_test_rcv=true * link_test_min_timer_done)" is satisfied.

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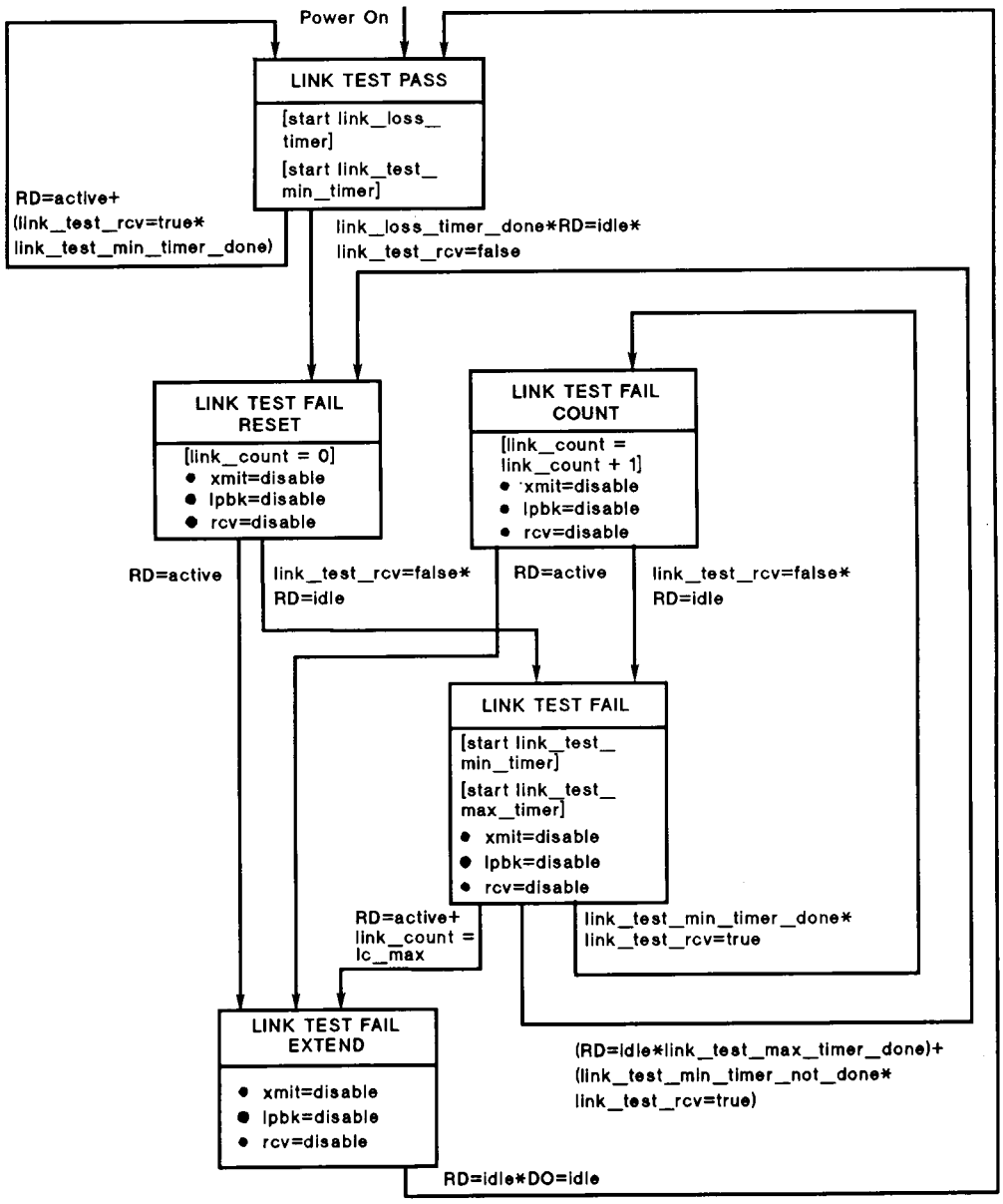


Figure 14–6—Link Integrity Test function state diagram

link_loss_timer. Timer for longest time input activity can be missing before the MAU determines that a link fail condition exists (14.2.1.7).

link_test_min_timer. Timer for the minimum time between valid link test pulses (14.2.1.7).

link_test_max_timer. Timer for maximum time input activity can be missing before Link Fail state is exited (14.2.1.7).

SQE_test_timer. Timer for the duration of the CS0 signal used for the SQE Test function (14.2.1.5).

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SQE_test_wait_timer. Timer for the delay from end of packet to the start of the CS0 signal used for the SQE Test function (14.2.1.5).

unjab_timer. Timer for the length of time the DO circuit must be continuously idle to allow transmission to be re-enabled (14.2.1.6).

xmit_max_timer. Timer for excessively long transmit time (14.2.1.6).

14.3 MAU electrical specifications

This subclause defines the electrical characteristics of the MAU at the MDI and the AUI. The MAU shall also meet the AUI requirements specified in Clause 7 when the AUI is implemented.

Additional information relative to conformance testing is given in B.4.3.

The ground for all common-mode tests is circuit PG, Protective Ground of the AUI. In implementations without an AUI, chassis ground is used as circuit PG. All components in test circuits shall be ±1% unless otherwise stated.

14.3.1 MAU-to-MDI interface characteristics

14.3.1.1 Isolation requirement

The MAU shall provide isolation between the DTE Physical Layer circuits including frame ground and all MDI leads including those not used by 10BASE-T. This electrical separation shall withstand at least one of the following electrical strength tests.

a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC 60950: 1991.
b) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC 60950: 1991.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC 60950: 1991, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 Vdc.

14.3.1.2 Transmitter specifications

The MAU shall provide the Transmit function specified in 14.2.1.1 in accordance with the electrical specifications of this subclause.

Where a load is not specified, the transmitter shall meet requirements of this subclause when connected to a 100 Ω resistive load. The use of 100 Ω terminations simplifies the measurement process when using 50 Ω measurement equipment as 50 Ω to 100 Ω impedance matching transformers are readily available.

Some tests in this subclause require the use of an equivalent circuit that models the distortion introduced by a simplex link segment. This twisted-pair model shall be constructed according to Figure 14–7 with component tolerances as follows: Resistors, ±1%; capacitors, ±5%; inductors, ±10%. Component tolerance specifications shall be met from 5.0 MHz to 15 MHz. For all measurements, the TD circuit shall be connected through a balun to section 1 and the signal measured across a load connected to section 4 of the model. The balun shall not affect the peak differential output voltage specified in 14.3.1.2.1 by more than 1% when inserted between the 100 Ω resistive load and the TD circuit.

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The insertion loss of the twisted-pair model when measured with a 100 Ω source and 100 Ω load shall be between 9.70 dB and 10.45 dB at 10 MHz, and between 6.50 dB and 7.05 dB at 5 MHz.

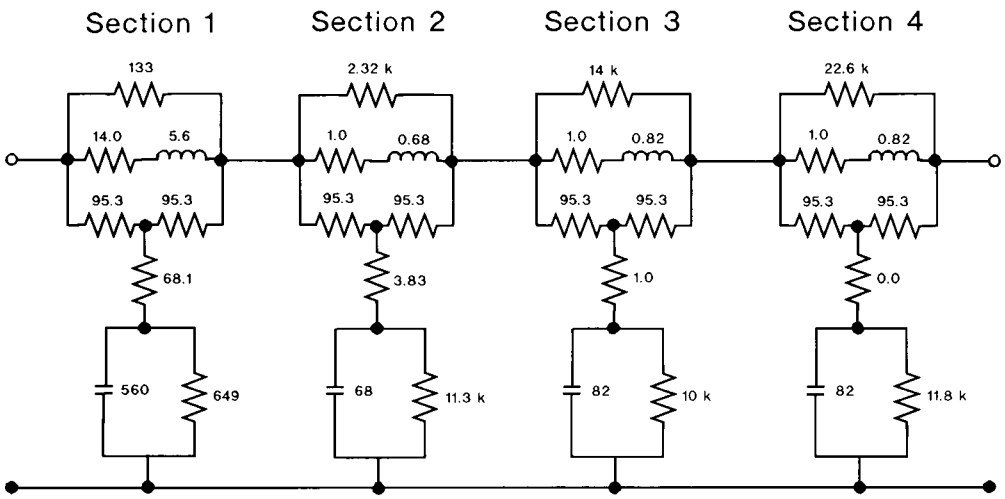


Figure 14–7—Twisted-pair model

14.3.1.2.1 Differential output voltage

Some of the text and figures of this subclause describe the differential voltage in terms of magnitudes. These requirements apply to negative as well as positive pulses.

The peak differential voltage on the TD circuit when terminated with a 100 Ω resistive load shall be between 2.2 V and 2.8 V for all data sequences. When the DO circuit is driven by an all-ones Manchester-encoded signal, any harmonic measured on the TD circuit shall be at least 27 dB below the fundamental.

NOTE—The specification on maximum spectral components is not intended to ensure compliance with regulations concerning RF emissions. The implementor should consider any applicable local, national, or international regulations. Additional filtering of spectral components may therefore be necessary.

The output signal V_o, is defined at the output of the twisted-pair model as shown in Figure 14–8. The TD transmitter shall provide equalization such that the output waveform shall fall within the template shown in Figure 14–9 for all data sequences. Voltage and time coordinates for inflection points on Figure 14–9 are given in Table 14–1. (Zero crossing points are different for external and internal MAUs. The zero crossings depicted in Figure 14–9 apply to an external MAU.) The template voltage may be scaled by a factor of 0.9 to 1.1 but any scaling below 0.9 or above 1.1 shall not be allowed. The recommended measurement procedure is described in B.4.3.1. Time t = 0 on the template represents a zero crossing, with positive slope, of the output waveform. During this test the twisted-pair model shall be terminated in 100 Ω and driven by a transmitter with a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits.

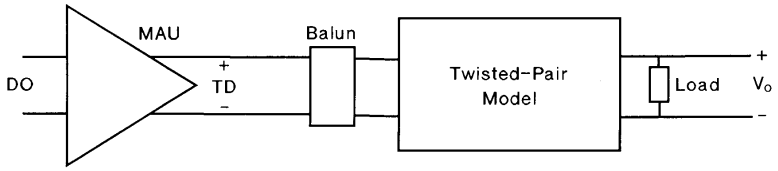


Figure 14–8—Differential output voltage test

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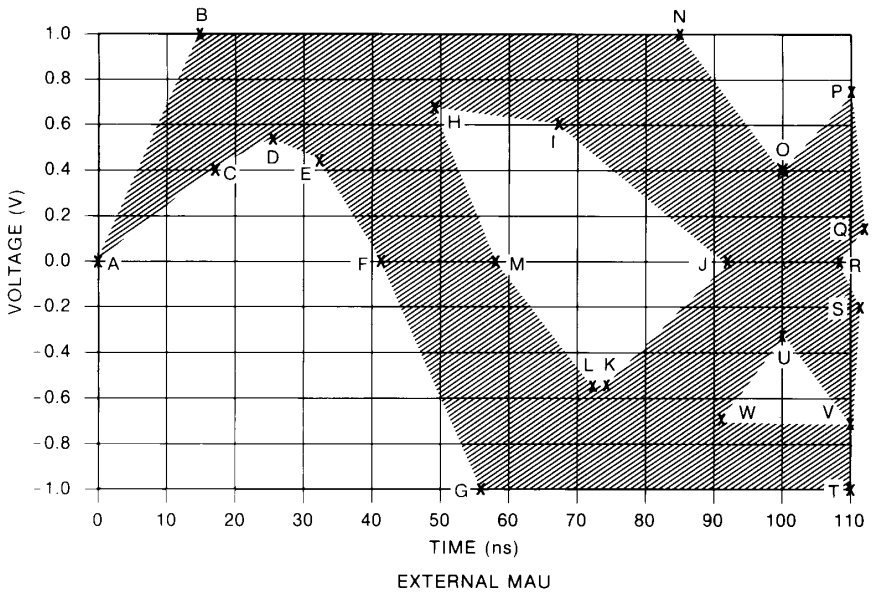


Figure 14–9—Voltage template

Table 14–1—Voltage template values for Figure 14–9

Reference	Time (ns)		Voltage (V)
	External MAU	Internal MAU	
A	0	0	0
B	15	15	1.0
C	15	15	0.4
D	25	25	0.55
E	32	32	0.45
F	42	39	0
G	57	57	–1.0
H	48	48	0.7
I	67	67	0.6
J	92	89	0
K	74	74	–0.55
L	73	73	–0.55
M	58	61	0
N	85	85	1.0
O	100	100	0.4
P	110	110	0.75
Q	111	111	0.15
R	108	111	0
S	111	111	–0.15
T	110	110	–1.0
U	100	100	–0.3
V	110	110	–0.7
W	90	90	–0.7

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This test shall be repeated with the template inverted about the time axis. In that case, t = 0 on the template represents a zero crossing, with negative slope, of the output waveform. When testing an external MAU the input waveform to the DO circuit of the MAU shall contribute no more than 0.5 ns of jitter. Adherence to this template does not verify that the requirements of 14.3.1.2.3 are met. (See B.4.3.3 for modification of the template to test jitter.)

The TP_IDL shall always start with a positive waveform when a waveform conforming to Figure 7–12 is applied to the DO circuit. If the last bit transmitted was a CD1, the last transition will be at the bit cell center of the CD1. If the last bit transmitted was a CD0, the PLS will generate an additional transition at the bit cell boundary following the CD0. After the zero crossing of the last transition, the differential voltage shall remain within the shaded area of Figure 14–10. Once the differential voltage has gone more negative than –50 mV, it shall not exceed +50 mV. The template requirements of Figure 14–10 shall be met when measured across each of the test loads defined in Figure 14–11, both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figures 14–7 and 14–8.

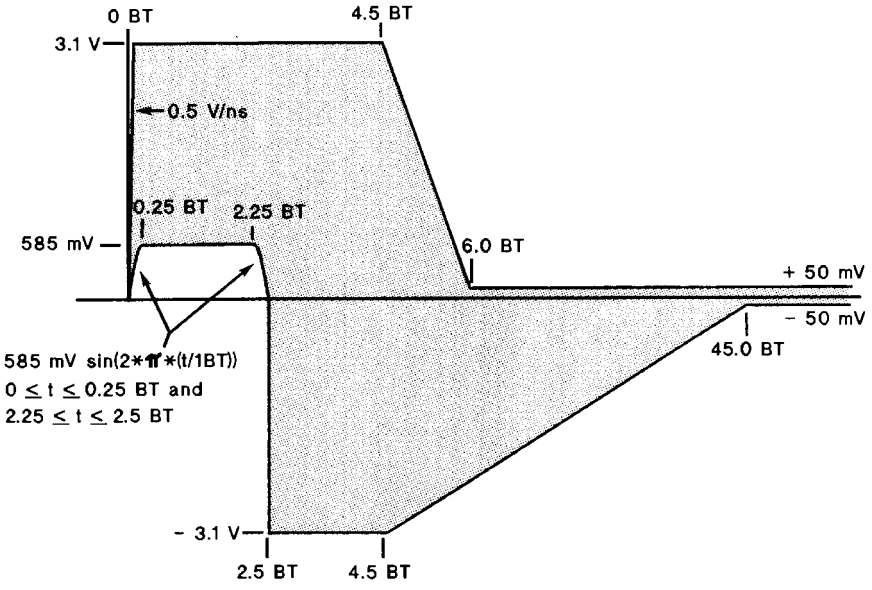


Figure 14–10—Transmitter waveform for start of TP_IDL

The link test pulse shall be a single positive (TD+ lead positive with respect to TD– lead) pulse, which falls within the shaded area of Figure 14–12. Once the differential output voltage has become more negative than –50 mV, it shall remain less than +50 mV. The template requirements of Figure 14–12 shall be met when measured across each of the test loads defined in Figure 14–11; both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figures 14–7 and 14–8.

For a MAU that implements the Auto-Negotiation algorithm defined in Clause 28, the FLP Burst Sequence will consist of multiple link test pulses. All link test pulses in the FLP Burst sequence shall meet the template requirements of Figure 14–12 when measured across each of the test loads defined in Figure 14–11; both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figures 14–7 and 14–8.

14.3.1.2.2 Transmitter differential output impedance

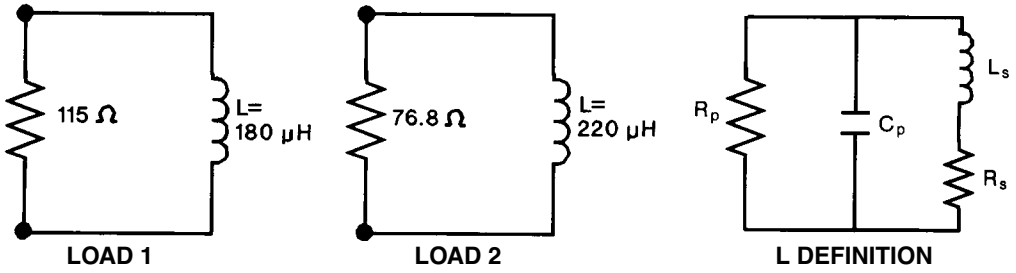
The differential output impedance as measured on the TD circuit shall be such that any reflection, due to differential signals incident upon the TD circuit from a simplex link segment having any impedance within the range specified in 14.4.2.2, shall be at least 15 dB below the incident, over the frequency range of 5.0 MHz

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All parameters are defined over the frequency range of 250 kHz to 6 MHz.

$L_s = L \pm 1\%$ $R_p \geq 2\ k\Omega$
$C_p = 12\ pF \pm 20\%$ $R_s \leq 0.5\ \Omega$

Figure 14–11—Start-of-TP_IDL test load

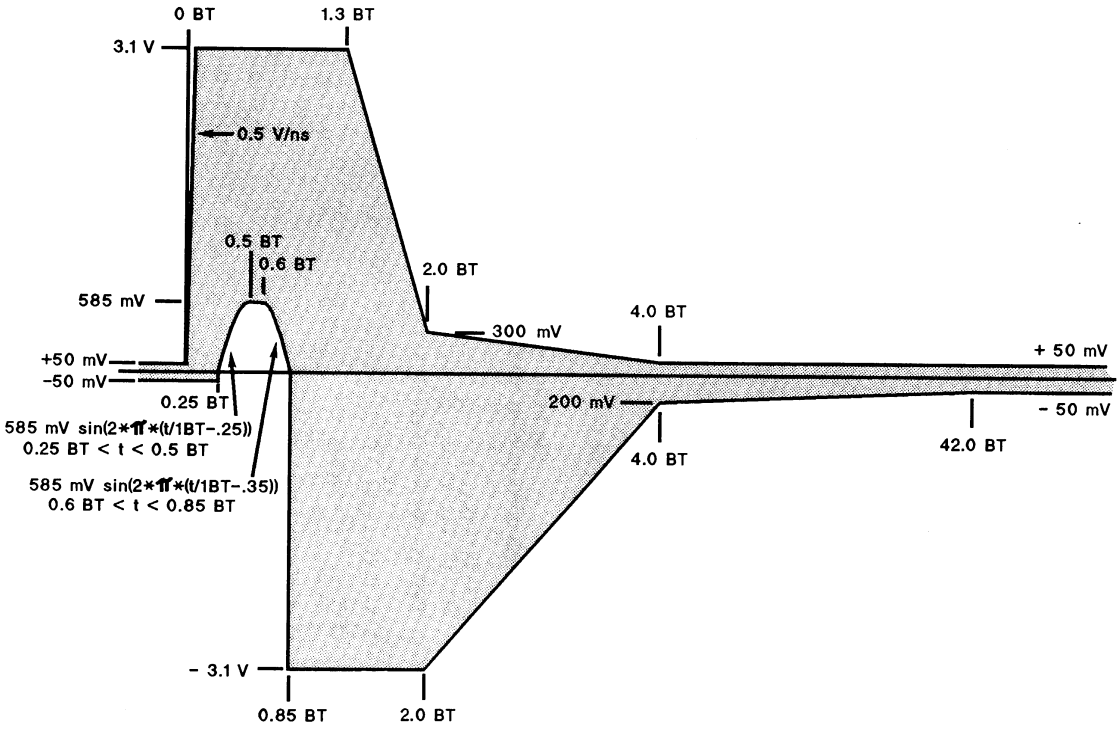


Figure 14–12—Transmitter waveform for link test pulse

to 10 MHz. This return loss shall be maintained at all times when the MAU is powered, including when the TD circuit is sending TP_IDL.

14.3.1.2.3 Output timing jitter

The transmitter output jitter is measured at the output of the twisted-pair model terminated in a 100 Ω load, as shown in Figure 14–8. The jitter added to the signal on the DO circuit as it propagates through the MAU and the twisted-pair model shall be no more than ±3.5 ns. Additionally, the MAU shall add no more than ±8 ns of jitter to the signal received on the DO circuit when the TD circuit is directly driving a 100 Ω resistive load.

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14.3.1.2.4 Transmitter impedance balance

The common-mode to differential-mode impedance balance of the TD circuit shall exceed $29-17\log_{10}(f/10)$ dB (where f is the frequency in MHz) over the frequency range 1.0 MHz to 20 MHz. This balance is defined as $20\log_{10}(E_{cm}/E_{dif})$, where E_{cm} is an externally applied sine wave voltage as shown in Figure 14–13.

NOTE—The balance of the test equipment (such as the matching of the 147 Ω resistors) must exceed that required of the transmitter.

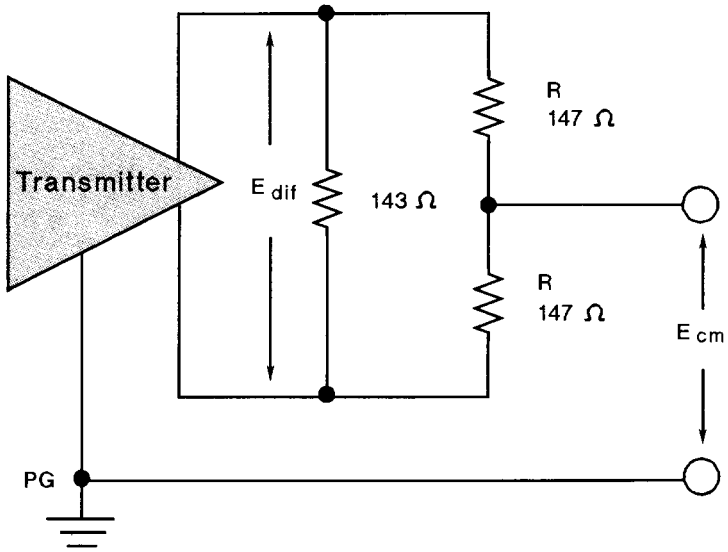


Figure 14–13—Transmitter impedance balance and common-mode rejection test circuit

14.3.1.2.5 Common-mode output voltage

The magnitude of the total common-mode output voltage of the transmitter, E_{cm}, measured as shown in Figure 14–14, shall be less than 50 mV peak.

NOTE—This specification is not intended to ensure compliance with regulations concerning RF emissions. The implementor should consider any applicable local, national, or international regulations. Driving unshielded twisted pairs with high-frequency, common-mode voltages may result in interference to other equipment.

14.3.1.2.6 Transmitter common-mode rejection

The application of E_{cm}, as shown in Figure 14–13, shall not change the differential voltage at the TD circuit, E_{dif}, by more than 100 mV for all data sequences. Additionally, the edge jitter added by the application of E_{cm} shall be no more than 1.0 ns. E_{cm} shall be a 15 V peak 10.1 MHz sine wave.

14.3.1.2.7 Transmitter fault tolerance

Transmitters, when either idle or non-idle, shall withstand without damage the application of short circuits across the TD circuit for an indefinite period of time and shall resume normal operation after such faults are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

Transmitters, when either idle or non-idle, shall withstand without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity (as indicated in Figure 14–15). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

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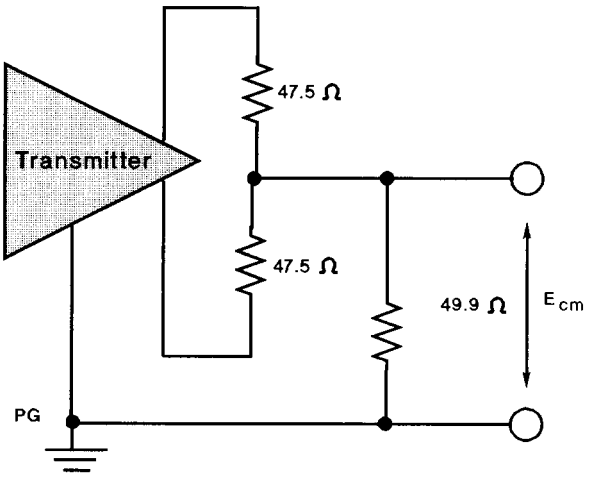


Figure 14–14—Common-mode output voltage test circuit

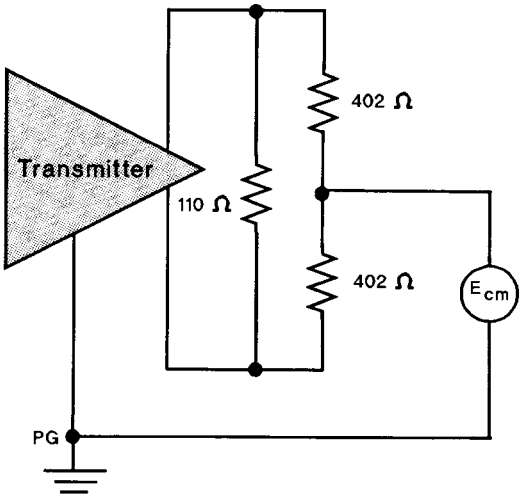


Figure 14–15—Transmitter fault tolerance test circuit

14.3.1.3 Receiver specifications

The MAU shall provide the Receive function specified in 14.2.1.2 in accordance with the electrical specifications of this clause.

14.3.1.3.1 Receiver differential input signals

Differential signals received on the RD circuit that are within the envelope of Figure 14–16 and Figure 14–17, and have a maximum zero crossing jitter up to ±13.5 ns from the ideal shall be sent to the DI circuit. The 13.5 ns includes jitter caused by an encoder, AUI cable and transmitting MAU, the twisted pair, and noise. Additionally, the MAU receiver shall add no more than ±1.5 ns jitter to the receive signal before sending the signal to the DI circuit.

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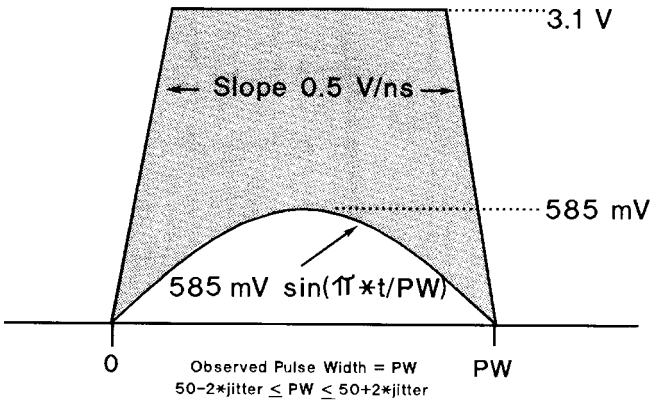


Figure 14–16—Receive differential input voltage—narrow pulse

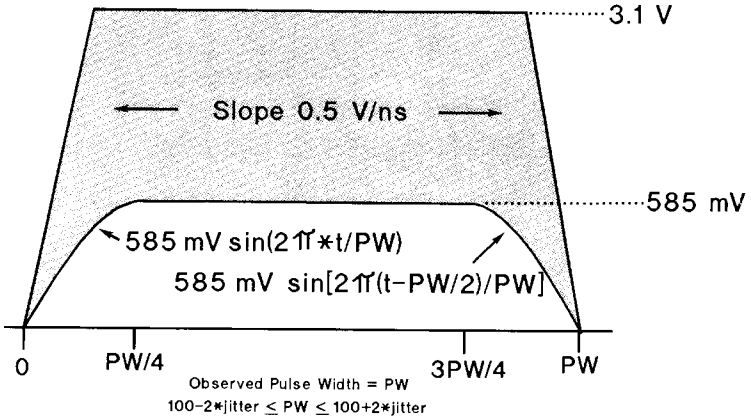


Figure 14–17—Receiver differential input voltage—wide pulse

14.3.1.3.2 Receiver differential noise immunity

The receiver, when presented with Manchester-encoded data meeting the requirements of 14.3.1.3.1, shall send this data to the DI circuit with a bit loss of no more than that specified in 14.2.1.2. In addition, the receiver, when presented with a signal meeting the requirements of 14.2.1.1 and within the envelope of Figure 14–12, shall accept it as a link test pulse.

The receiver, while in the Idle state, shall reject as *RD_input* the following signals:

a) All signals that when measured at the output of the following filter would produce a peak magnitude less than 300 mV. The filter is a 3-pole low-pass Butterworth with a 3 dB cutoff at 15 MHz (refer to B.4.2).
b) All continuous sinusoidal signals of amplitude less than 6.2 V peak-to-peak and frequency less than 2 MHz.
c) All sine waves of single cycle duration, starting with phase 0 or 180 degrees, and of amplitude less than 6.2 V peak-to-peak where the frequency is between 2 MHz and 15 MHz. For a period of 4 BT before and after this single cycle, the signal shall be less than 300 mV when measured through the filter specified in a) above.

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14.3.1.3.3 Idle input behavior

The idle condition shall be detected within 2.3 BT of the last low-to-high transition at the receiver. The receiver shall take precautions to ensure that the high-to-silence transition of the start of idle is not falsely interpreted as a silence-to-non-idle-transition, even in the presence of signal droop, overshoot, ringing, slow voltage decay, or a combination thereof due to capacitive and inductive effects in the transmitter, link segment, and receiver.

14.3.1.3.4 Receiver differential input impedance

The differential input impedance shall be such that any reflection, due to differential signals incident upon the RD circuit from a twisted pair having any impedance within the range specified in 14.4.2.2 shall be at least 15 dB below the incident over the frequency range of 5.0 MHz to 10 MHz. The return loss shall be maintained when the MAU is powered.

14.3.1.3.5 Common-mode rejection

Receivers shall assume the proper state on DI for any differential input signal E_s that results in a signal E_{dif} that meets 14.3.1.3.1 even in the presence of common-mode voltages E_{cm} (applied as shown in Figure 14–18). E_{cm} shall be a 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%–80%). Additionally, E_{cm} shall contribute no more than 2.5 ns of edge jitter to the signal transmitted on the DI circuit. The combination of the receiver timing jitter of 14.3.1.3.1 and the common-mode induced jitter are such that the MAU shall add no more than 4.0 ns of edge jitter to E_s before sending the signal on the DI circuit.

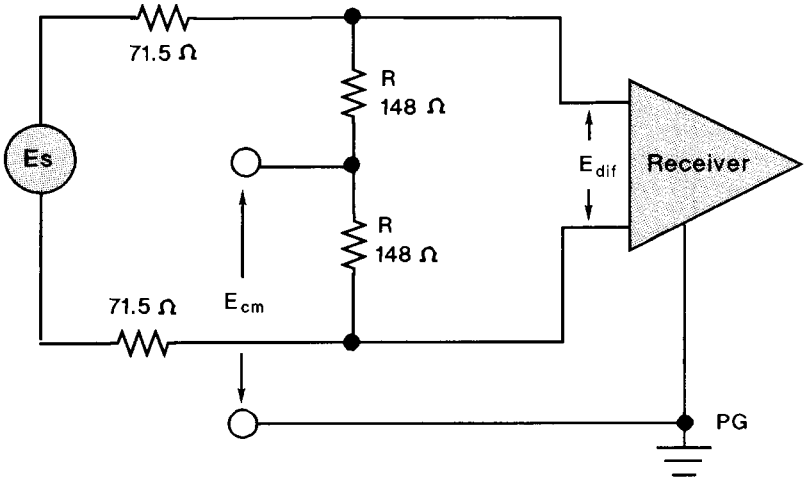


Figure 14–18—Receiver common-mode rejection test circuit

14.3.1.3.6 Receiver fault tolerance

The receiver shall tolerate the application of short circuits between the leads of the RD circuit for an indefinite period of time without damage and shall resume normal operation after such faults are removed. Receivers shall withstand without damage a 1000 V common-mode impulse of either polarity ($E_{impulse}$ as indicated in Figure 14–19). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

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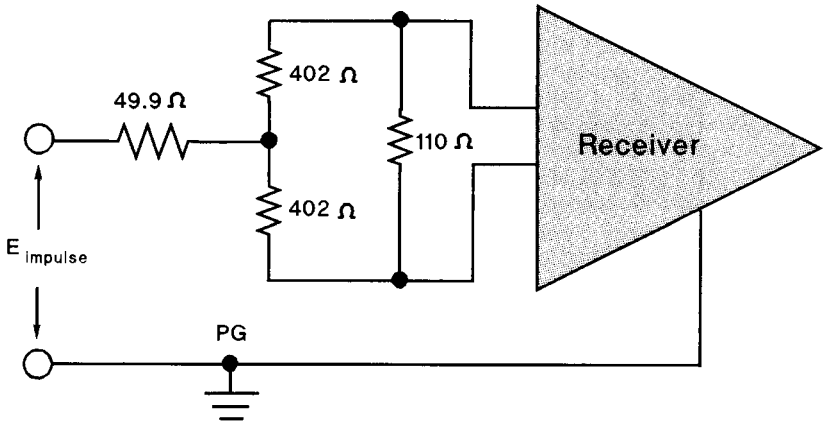


Figure 14–19—Common-mode impulse test circuit

14.3.2 MAU-to-AUI specification

When a MAU contains a physical AUI connector, the following specifications shall be met.

14.3.2.1 MAU-AUI electrical characteristics

The electrical characteristics for the driver and receiver components within the MAU that are connected to the AUI shall be identical to those specified in 7.4 and 7.5. Additionally, the AUI DO receiver, while in the Idle state, shall reject an input waveform of less than ±160 mV differential.

14.3.2.2 MAU–AUI mechanical connection

The MAU shall be provided with a 15-pin male connector as specified in 7.6.

14.3.2.3 Power consumption

Following PowerOn, the surge current drawn by the MAU shall be such that $I_p \times T_w$ is less than or equal to 2×10^{-3} ampere-seconds, where I_p is the peak surge current and T_w is the time during which the current exceeds the larger of 0.5 A or $0.5 \times I_p$. After the 100 ms following PowerOn, the current drawn by the MAU shall not exceed 0.5 A when powered by the AUI.

The MAU shall be capable of operating from all possible voltage sources, including those current limited to 0.5 A, as supplied by the DTE or repeater through the resistance of all permissible AUI cables.

The MAU shall not introduce extraneous signals on the TD, CI, or DI circuits during normal power-up and power-down.

14.4 Characteristics of the simplex link segment

Except where otherwise stated, the simplex link segment shall be tested with source and load impedances of 100 Ω.

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14.4.1 Overview

The medium for 10BASE-T is twisted-pair wiring. Since a significant number of 10BASE-T networks are expected to be installed utilizing in-place unshielded telephone wiring and typical telephony installation practices, the end-to-end path including different types of wiring, cable connectors, and cross connects must be considered. Typically, a DTE connects to a wall outlet using a twisted-pair patch cord. Wall outlets connect through building wiring and a cross connect to the repeater MAU in a wiring closet.

NOTE—ANSI/TIA/EIA-568-A-1995 [B16] provides specifications for media and installation practices suitable for use with this standard.

14.4.2 Transmission parameters

Each simplex link segment shall have the following characteristics. All characteristics specified apply to the total simplex link segment unless otherwise noted. These characteristics are generally met by 100 m of unshielded twisted-pair cable composed of 0.5 mm [24 AWG] twisted pairs.

14.4.2.1 Insertion loss

The insertion loss of a simplex link segment shall be no more than 11.5 dB at all frequencies between 5.0 and 10 MHz. This consists of the attenuation of the twisted pairs, connector losses, and reflection losses due to impedance mismatches between the various components of the simplex link segment. The insertion loss specification shall be met when the simplex link segment is terminated in source and load impedances that satisfy 14.3.1.2.2 and 14.3.1.3.4.

NOTE—Multipair PVC-insulated 0.5 mm [24 AWG] cable typically exhibits an attenuation of 8 dB to 10 dB/100 m at 20 °C. The loss of PVC-insulated cable exhibits significant temperature dependence. At temperatures greater than 40 °C, it may be necessary to use a less temperature-dependent cable, such as most plenum-rated cables.

14.4.2.2 Differential characteristic impedance

The magnitude of the differential characteristic impedance of a 3 m length of twisted pair used in a simplex link segment shall be between 85 Ω and 111 Ω for all frequencies between 5.0 MHz and 10 MHz. Since characteristic impedance tends to decrease with increasing frequency, the above requirement is generally implied by the condition that the magnitude of the characteristic impedance over the frequency band 1 MHz to 16 MHz is 100 Ω ± 15 Ω. Also, the magnitude of the input impedance averaged over the 5.0 MHz to 10 MHz frequency band of a simplex link segment terminated in 100 Ω shall be between 85 Ω and 111 Ω.

14.4.2.3 Medium timing jitter

Intersymbol interference and reflections due to impedance mismatches between tandem twisted pairs of a twisted-pair link segment and effects of connection devices can introduce jitter to the CD1 and CD0 signals received on the RD circuit. No more than ±5.0 ns of jitter shall be introduced to a test signal by a simplex link segment. The test signal shall have a peak amplitude of 3.0 V and 10% to 90% rise and fall times of 12 ns. The content of the test signal shall be a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits.

NOTE—Branches off a twisted pair (often referred to as “bridged taps” or “stubs”) will generally cause excessive jitter and so should be avoided.

14.4.2.4 Delay

The maximum propagation delay of twisted pair shall be 5.7 ns/m (minimum velocity of 0.585 × c). The maximum propagation delay of a link segment shall not exceed 1000 ns.

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14.4.3 Coupling parameters

To avoid excessive coupling of signals between twisted pairs of a twisted-pair cable, the crosstalk must be limited. Crosstalk loss is specified for the twisted pairs in a twisted-pair cable or twisted-pair cable binder group that are used as 10BASE-T twisted-pair links. Crosstalk loss is specified with the far ends of both the disturbed and the disturbing pairs and the near end of the disturbed pair terminated in 100 Ω. Drivers of disturbing pairs shall have a source impedance of 100 Ω.

14.4.3.1 Differential near-end crosstalk (NEXT) loss

The NEXT loss between any two twisted pairs of a twisted-pair cable is dependent upon the geometry of the twisted-pair cable. Since the proximity of any two twisted pairs is influenced by the size of the twisted-pair cable, the NEXT loss is affected by twisted-pair cable size.

14.4.3.1.1 Twenty-five-pair cable and twenty-five-pair binder groups

The NEXT loss between any two twisted pairs in a twenty-five-pair twisted-pair cable or binder group used for 10BASE-T applications shall be at least $30 - 15 \log_{10}(f/10)$ dB (where f is the frequency in MHz) over the frequency range 5.0 MHz and 10 MHz.

14.4.3.1.2 Four-pair cable

The NEXT loss between any two twisted pairs in a four-pair twisted-pair cable used for 10BASE-T applications shall be at least $26 - 15 \log_{10}(f/10)$ dB (where f is the frequency in MHz) over the frequency range 5.0 MHz and 10 MHz.

14.4.3.1.3 Other cables

The NEXT loss requirement for all other twisted-pair cables shall be the multiple-disturber NEXT loss of 14.4.3.2.

14.4.3.2 Multiple-disturber NEXT (MDNEXT) loss

When a twisted-pair cable or twisted-pair cable binder group contains twisted pairs from multiple 10BASE-T twisted-pair link segments, the multiple-disturber crosstalk loss is dependent upon the specific selection of disturbing and disturbed pairs. For each 10BASE-T receive pair, MDNEXT is measured by having the remaining near-end transmit pairs (excluding the transmit pair associated with the receive pair under test) driven with identical and synchronized sine wave signals. MDNEXT may then be determined from the signal level observed on the receive pair under test. By examining all pair combinations with a fixed number of disturbers, a cumulative distribution of MDNEXT is obtained at each frequency of interest. The one percentile of this cumulative distribution shall be at least $23 - 15 \log_{10}(f/10)$ (where f is the frequency in MHz) at 5.0 MHz, 7.5 MHz, and 10 MHz. When the number of possible combinations allowed by a cable is fewer than 100, the MDNEXT loss for all combinations shall be at least $23 - 15 \log_{10}(f/10)$ (where f is the frequency in MHz) at 5.0 MHz, 7.5 MHz, and 10 MHz. Refer to 12.7.3.2 and B.3 for a tutorial and method for estimating the MDNEXT loss for a complete n-pair cable.

14.4.4 Noise environment

The noise level on the link segments shall be such that the objective error rate is met. The noise environment consists generally of two primary contributors: crosstalk from other 10BASE-T circuits; and externally induced impulse noise, typically from telephone ringing and dialing signals, and other office and building equipment.

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14.4.4.1 Impulse noise

The average rate of occurrence of impulses greater than 264 mV shall be less than or equal to 0.2/s as measured at the output of the following specified filter. Following the start of any particular impulse that is counted, any additional impulse shall be ignored for a period of 1 μs. The simplex link segment shall be terminated at the far end in 100 Ω. The filter is a 3-pole Butterworth low-pass with a 3 dB cutoff at 15 MHz (refer to B.4.2).

NOTE—Typically, the impulse noise occurrence rate changes inversely by one decade for each 5 dB to 9 dB change in the threshold voltage. If a count rate of N counts/s is measured on a specific twisted pair and filter at the specified voltage threshold, the media noise margin is approximately 7 $\log_{10}(0.2/N)$ dB. Impulse noise may be a burst phenomenon and should be measured over an extended period of time.

14.4.4.2 Crosstalk noise

The level of crosstalk noise on a simplex link segment depends on the level of the disturbing signal(s) and the crosstalk loss between the pair(s) carrying the signal(s) and the disturbed pair. With the maximum transmit level (14.3.1.2), the sinusoidal crosstalk loss (14.4.3.2), and multiple, random Manchester-encoded disturbers, the peak self-crosstalk noise levels as measured at the output of the following specified filter shall be less than or equal to 264 mV. The filter is a 3-pole Butterworth low-pass with a 3 dB cutoff at 15 MHz (refer to B.4.2).

14.5 MDI specification

This subclause defines the MDI for the twisted-pair link segment. The link topology requires a crossover function between PMAs. Implementation and location of this crossover is also defined in this clause.

14.5.1 MDI connectors

Eight-pin connectors meeting the requirements of Clause 3 and Figures 1 through 5 of IEC 60603-7 shall be used as the mechanical interface to the twisted-pair link segment. The plug connector shall be used on the twisted-pair link segment and the jack on the MAU. These connectors are depicted (for informational use only) in Figure 14–20 and Figure 14–21. The following table shows the assignment of signals to connector contacts.

Contact	MDI signal
1	TD+
2	TD–
3	RD+
4	Not used by 10BASE-T
5	Not used by 10BASE-T
6	RD–
7	Not used by 10BASE-T
8	Not used by 10BASE-T

14.5.2 Crossover function

A crossover function shall be implemented in every twisted-pair link. The crossover function connects the transmitter of one MAU to the receiver of the MAU at the other end of the twisted-pair link. Crossover functions may be implemented internally to a MAU or elsewhere in the twisted-pair link. For MAUs that do not implement the crossover function, the signal names of 14.5.1 refer to their own internal circuits. For MAUs

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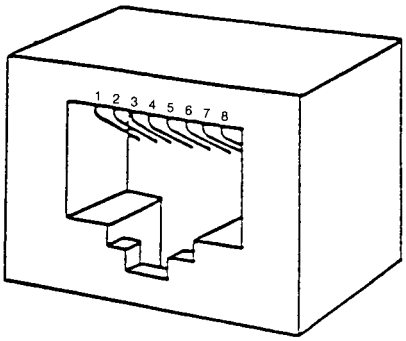


Figure 14–20—MAU MDI connect

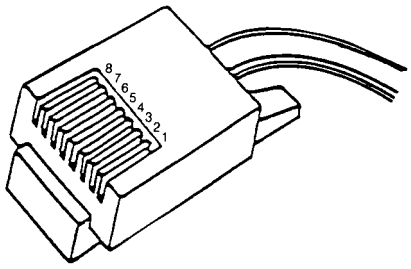


Figure 14–21—Twisted-pair link segment connector

that do implement the crossover function, the signal names refer to the remote MAU of the twisted-pair link. Additionally, the MDI connector for a MAU that implements the crossover function shall be marked with the graphical symbol "X". Internal and external crossover functions are shown in Figure 14–22.

When a twisted-pair link connects a DTE to a repeater, it is recommended that the crossover be implemented in the MAU local to the repeater. If both MAUs of a twisted-pair link contain internal crossover functions, an additional external crossover is necessary. It is recommended that the crossover be visible to an installer from one of the MAUs. When both MAUs contain internal crossovers, it is further recommended in networks in which the topology identifies either a central backbone segment or a central hub that the MAU furthest from the central element be assigned the external crossover to maintain consistency.

Implicit implementation of the crossover function within a twisted-pair cable, or at a wiring panel, while not expressly forbidden, is beyond the scope of this standard.

14.6 System considerations

The repeater unit specified in Clause 9 forms the central unit for interconnecting 10BASE-T twisted-pair links in networks of more than two nodes. It also provides the means for connecting 10BASE-T twisted-pair links to other 10 Mb/s baseband segments. The proper operation of a CSMA/CD network requires network size to be limited to control round-trip propagation delay to meet the requirements of 4.2.3.2.3 and 4.4.2.1, and the number of repeaters between any two DTEs to be limited in order to limit the shrinkage of the interpacket gap as it travels through the network. Configuration rules, which ensure that these limits are not exceeded, are given in Clause 13.

14.7 Environmental specifications

14.7.1 General safety

All equipment meeting this standard shall conform to IEC 60950: 1991.

14.7.2 Network safety

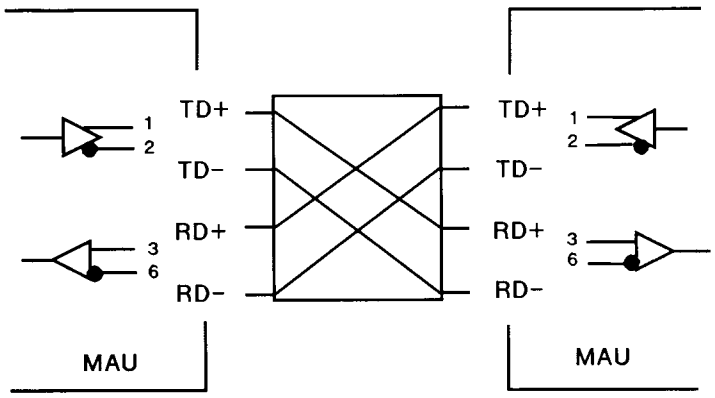
This subclause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

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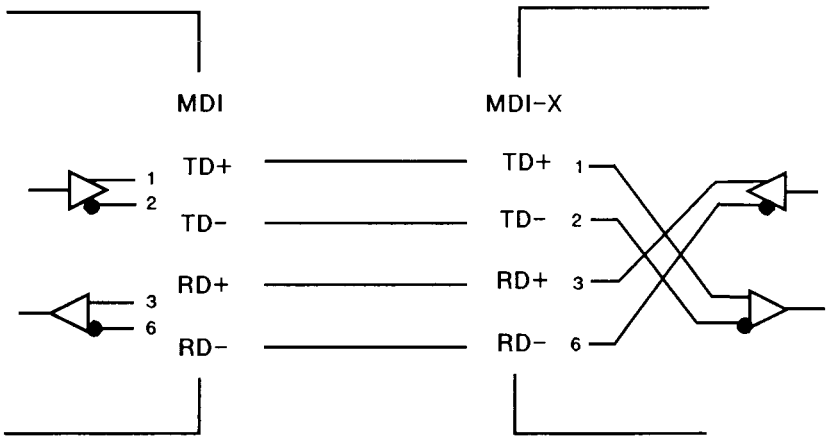
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a) External Crossover function



b) MAU-Embedded Crossover function

Figure 14–22—Crossover function

LAN cable systems described in this subclause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cables and components.
c) High-energy transients coupled onto the LAN cable system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network. Isolation requirements are defined in 14.3.1.1.

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14.7.2.1 Installation

Sound installation practice, as defined by applicable local codes and regulations, shall be followed in every instance in which such practice is applicable.

14.7.2.2 Grounding

Any safety grounding path for the MAU shall be provided through the circuit PG of the AUI connection.

WARNING

It is assumed that the equipment to which the MAU is attached is properly earthed, and not left floating nor serviced by a "doubly insulated ac power distribution system." The use of floating or insulated equipment, and the consequent implications for safety are beyond the scope of this standard.

14.7.2.3 Installation and maintenance guidelines

During installation and maintenance of the cable plant, care shall be taken to ensure that uninsulated network cable conductors do not make electrical contact with unintended conductors or ground.

14.7.2.4 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 10BASE-T equipment. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply.

Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400 Ω source impedance.

Ringing voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 Ω source resistance. The dc component is 56 Vdc with a 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 10BASE-T equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE—Wiring errors may impose telephony voltages differentially across 10BASE-T transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, receivers will generally appear to the telephone system as off-hook telephones. Therefore, full-ring voltages will be applied for only short periods. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to the low resistance of the transformer coil.

14.7.3 Environment

14.7.3.1 Electromagnetic emission

The twisted-pair link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

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14.7.3.2 Temperature and humidity

The twisted-pair link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the MAU the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the twisted-pair link segment, the distance and operating environmental conditions over which the specifications of 14.4 will be met.

14.8 MAU labeling

It is recommended that each MAU (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Data rate capability in Mb/s,
b) Power level in terms of maximum current drain (for external MAUs),
c) Any applicable safety warnings, and
d) Duplex capabilities.

See also 14.5.2.

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14.9 Timing summary

Table 14–2 summarizes the timing requirements for the 10BASE-T twisted-pair link. This table is a summary; for complete descriptions of the timing requirements, refer to the referenced subclauses.

Table 14–2—Maximum timing parameters

Symbol	Function	Bit Loss[a]	Invalid Bits[b]	Steady-State Propagation Delay[b]	Start-up Delay[b]		Specified in
					Maximum	Variability	
M1	*RD_input* to *input* on DI	5.0	1.0	2.0	8.0	2.0	14.2.1.2
M2	*output* on DO to *TD_output*	2.0	1.0	2.0	5.0	2.0	14.2.1.1
M3	RD_input * output to signal_quality_error	—	—	—	9.0	—	14.2.1.4
M4	*RD_idle* + *output_idle* (end of collision) to *mau_available*	—	—	—	9.0	—	14.2.1.4
M5	*RD_input* * *output* to *input* on DI from circuit RD	—	—	—	9.0	—	14.2.1.4
M6	*RD_idle* * *output* to *input* on DI from circuit DO	—	—	—	9.0	—	14.2.1.4
M7	*output_idle* on DO to *signal_quality_error*	—	—	—	6 < × < 16	—	14.2.1.5
M8	signal_quality_error duration for SQE test	—	—	—	5 < × < 15	—	14.2.1.5
M9	*output* on DO to *input* on DI	5.0	1.0	1.0	7.0	—	14.2.1.3
T1	twisted-pair propagation	0	0	10.00	10.00	—	14.4.2.4
A1	AUI cable propagation (50 m)	0	0	2.57	2.57	—	7.4.3.7

[a]All time in BT.

[b]For an explanation of the meaning of variability, see 14.2.1.1 and 14.2.1.2.

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14.10 Protocol Implementation Conformance Statement (PICS) proforma for Clause 14, Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T[25]

14.10.1 Introduction

To evaluate conformance of a particular implementation, it is necessary to state which capabilities and options have been implemented for a given OSI protocol. Such a statement is called a Protocol Implementation Conformance Statement (PICS).

This PICS proforma defines conformance requirements for type 10BASE-T MAU implementations. When the supplier completes this proforma, this document becomes the PICS for the specified implementation. The PICS is then used to perform a static conformance review of the implementation to determine that all mandatory features are implemented and that all conditional features are correctly supported dependent on the options claimed to be implemented. The PICS is used also as an aid in test-case selection and result analysis during the dynamic conformance testing.

Separate MAU and link segment implementations are expected; submissions of either for testing do not require submission of the other. Furthermore, there is no current intention to produce an Abstract Test Suite from the subclause of the PICS proforma that discusses the link segment.

14.10.1.1 Scope

This subclause provides the PICS proforma for type 10BASE-T MAU specifications in accordance with the relevant guidance given in ISO/IEC 9646-2: 1994.

14.10.1.2 Reference

Type 10BASE-T MAU requirements referenced in this PICS proforma are found in 14.2 through 14.8 and in 7.3 through 7.6 of this standard. Subclauses 7.3 through 7.6 and 14.2 through 14.8 take precedence over 14.10 in case of any conflict.

The use and the requirements for PICS proforma are defined in ISO/IEC 9646-1: 1994 and ISO/IEC 9646-2: 1994.

14.10.1.3 Definitions

This document uses the following terms defined in ISO/IEC 9646-1: 1994:

PICS proforma
Protocol Implementation Conformance Statement (PICS)
static conformance review
dynamic conformance testing

14.10.1.4 Conformance

The supplier of a MAU that is claimed to conform to type 10BASE-T MAU specifications shall complete a copy of the PICS proforma provided in this document and shall provide the information necessary to identify both the supplier and the implementation.

[25]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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14.10.2 Identification of implementation

The MAU supplier shall complete the relevant fields in this subclause to identify the supplier and the particular MAU.

14.10.2.1 Supplier information

The MAU supplier shall complete the relevant fields in this subclause to identify the supplier and the particular MAU.

Company name:	
Representative name:	
Address:	
Phone:	
Fax:	
E-mail:	

14.10.2.2 Implementation information

Implementation name:	
Implementation identifier (including version/release):	

14.10.3 Identification of the protocol

The supplier will complete this subclause to identify the precise portocol implemented.

Check Y [ ] if the MAU identified in the previous subclause implements the following protocol standard; check N [ ] if otherwise and attach an explanation.

IEEE Std 802.3-2002,Clause 14, Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T	Y [ ]	N [ ]

List any other addenda or amendment documents implemented.

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14.10.4 PICS proforma for 10BASE-T

14.10.4.1 Abbreviations

The following abbreviations are used in the PICS proforma tables:

Req=Requirement. This column indicates whether the conformance requirement of a particular clause in the standard is mandatory, optional, or conditional.
Imp=Implementation. This column is filled in for a particular implementation with a "Y" or an "N" to indicate claimed conformance.
M=Mandatory. Conformance cannot be met unless the parameter is implemented as specified.
O=Optional. The parameter may be implemented or not but, if implemented, it must be as stated in the standard.
C=Conditional. If an associated major option is implemented, this parameter must be implemented.

NOTE—Recommendations in the standard become "Optional" parameters in the context of a PICS proforma.

14.10.4.2 PICS Completion instructions and implementation statement

A supplier wishing to submit a 10BASE-T MAU for conformance testing against this standard must fill in the column headed "Imp" in the PICS proforma tables and submit the resulting PICS with the equipment for test. This column must be filled in either with a "Y" for yes, indicating that the implementation is intended to meet the particular mandatory or optional requirement, or "N" for no, indicating that the option has not been implemented (or enabled where switchable) or that the requirement is not met. It should be noted that any instances of "N" entered against a mandatory requirement will result in the implementation failing the static conformance test. In addition, the supplier must indicate below whether or not the implementation implements all the mandatory requirements.

This implementation implements all mandatory requirements	Y [ ]	N [ ]

14.10.4.3 Additional information

Any additional information that is needed to ensure that the MAU or link segment submitted for test is configured as a 10BASE-T MAU or link segment should be entered into the PIXIT (Protocol Implementation eXtra Information for Testing) document supplied by the conformance testing organization. Relevant information on 10BASE-T MAUs or link segments includes the following:

a) Enable/disable mechanisms for SQE Test
b) Enable/disable mechanisms for features that allow compatibility with nonstandard implementations
c) Operational instructions for DTEs or repeaters in cases where the MAU is embedded
d) Environmental conditions
e) Input voltage range for implementations with embedded MAUs

The above list is illustrative and is not intended to be either mandatory or exhaustive.

14.10.4.4 References

ISO/IEC 9646-2: 1994 requires that all PICS proforma clauses be individually identified. Tables have subclause headings and numbered clauses in order to meet this requirement.

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14.10.4.5 PICS proforma tables for MAU

14.10.4.5.1 MAU functions

	Parameter	Subclause	Req	Imp	Value/comment
	MAU functions:	14.2.1			
1	Transmit		M		
2	Receive		M		
3	Loopback		C		Function performed by MAUs attached to half duplex mode DTEs and repeaters, not performed by MAUs attached to full duplex mode DTEs.
4	Collision Presence		C		Function performed by MAUs attached to half duplex mode DTEs and repeaters, optionally performed by MAUs attached to full duplex mode DTEs that fully support this option as described in 14.2.1.
5	Jabber		M		
6	Link Integrity Test		M		
7	SQE Test		C		Function performed by MAUs attached to half duplex DTEs, optionally performed by MAUs attached to full duplex DTEs that fully support this option as described in 14.2.1, not performed by MAUs attached to repeaters.
8	Auto-Negotiation		C		Function provided by MAUs implementing the Auto-Negotiation algorithm, as defined in Clause 28.

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14.10.4.5.2 Transmit function

	Parameter	Subclause	Req	Imp	Value/comment
1	Transmit path	14.2.1.1	M		DO circuit to TD circuit
2	Transmit signal polarity	14.2.1.1	M		DO A positive relative to DO B causes TD+ positive relative to TD–
3	Start-up bit loss (DO to TD circuits)	14.2.1.1	M		2 bits max
4	Transmit settling time	14.2.1.1	M		Second and following bits meet amplitude and jitter specifications
5	Transmit steady-state delay	14.2.1.1	M		2 bit times max
6	Transmit delay variability	14.2.1.1	M		2 bit times max
7	TP_IDL	14.2.1.1	M		Start of idle followed by a repeating sequence of silence and link test pulse
8	Silence duration	14.2.1.1	M		16 ms ± 8 ms, ≤ ±50 mV
9	TP_IDL termination with respect to start of packet	14.2.1.1	M		Normal start of packet requirements apply

14.10.4.5.3 Receive function

	Parameter	Subclause	Req	Imp	Value/comment
1	Receive path	14.2.1.2	M		RD circuit to DI circuit
2	Receive signal polarity	14.2.1.2	M		RD+ positive relative to RD– causes DI A positive relative to DI B
3	Start-up bit loss (RD to DI circuits)	14.2.1.2	M		5 bits max
4	Receive settling time	14.2.1.2	M		Second and following bits meet jitter specifications
5	Receive steady-state delay	14.2.1.2	M		2 bit times max
6	Receive delay variability	14.2.1.2	M		2 bit times max

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14.10.4.5.4 Loopback function

The following are conditional based on whether the Loopback function is to be performed (14.10.4.5.1, item 3).

	Parameter	Subclause	Req	Imp	Value/comment
1	Loopback function requirements when RD = idle and DO = active	14.2.1.3	C		DO signals to DI circuit
2	Loopback bit loss (DO to DI circuits)	14.2.1.3	C		5 bits max
3	Loopback settling time	14.2.1.3	C		Second and following bits meet jitter specifications
4	Loopback steady-state delay	14.2.1.3	C		1 bit time max

14.10.4.5.5 Collision Detect function

The following are conditional based on whether the Collision Presence function is to be performed (14.10.4.5.1, item 4).

	Parameter	Subclause	Req	Imp	Value/comment
1	Collision Presence function requirements	14.2.1.4	C		CS0 on CI circuit if DO=active, RD=active and in Link Test Pass state
2	Collision indication delay	14.2.1.4	C		9 bit times max
3	Collision indicate de-assert delay	14.2.1.4	C		9 bit times max
4	CI circuit with no collision, SQE Test, or jabber	14.2.1.4	C		IDL signal
5	DI circuit source switch delay from CS0 assert	14.2.1.4	C		9 bit times max
6	DI circuit source switch delay from CS0 de-assert	14.2.1.4	C		9 bit times max

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14.10.4.5.6 *signal_quality_error* Message Test function

The following are conditional based on whether the *signal_quality_error* Message Test is to be performed (14.10.4.5.1, item 7).

	Parameter	Subclause	Req	Imp	Value/comment
1	SQE Test induced TD or DI circuit signals	14.2.1.5	C		No extraneous signals permitted
2	SQE_test _wait timer range	14.2.1.5	C		0.6 to 1.6 μs
3	SQE_test timer range	14.2.1.5	C		5 to 15 bit times
4	CI circuit during SQE Test	14.2.1.5	C		CS0 signal
5	SQE Test in Link Fail state	14.2.1.5	C		CS0 must not be sent

14.10.4.5.7 Jabber function

	Parameter	Subclause	Req	Imp	Value/comment
1	Jabber Function implementation	14.2.1.6	M		Self-interrupt of transmit and loopback
2	Xmit_max timer range	14.2.1.6	M		20 ms min, 150 ms max
3	CI circuit during jabber	14.2.1.6	M		CS0 signal
4	Unjab timer range	14.2.1.6	M		0.5 ± 0.25 s
5	MAU Jabber Lockup Protection	14.2.1.6	M		Jabber not activated by the longest permitted output specified in 9.6.5

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14.10.4.5.8 Link Integrity Test function

	Parameter	Subclause	Req	Imp	Value/comment
1	Link_loss timer	14.2.1.7	M		50 ms min, 150 ms max
	Signals during detected failure:	14.2.1.7			
2	TD circuit		M		TP_IDL
3	DI circuit		M		IDL
4	CI circuit		M		IDL (except when jabber condition is also present)
5	Link Test Fail state exit conditions	14.2.1.7	M		RD = active or consecutive link test pulses = 2 min, 10 max
6	Link_test_min timer range	14.2.1.7	M		2 to 7 ms
7	Link_test_max timer range	14.2.1.7	M		25 to 150 ms
	Pulses outside acceptance window:	14.2.1.7			
8	Early while in Link Test Pass state		M		Ignore
9	Early or late while not in Link Test Pass state		M		Reset link test pulse counter
	Link fail effect on MAU functions:	14.2.1.7			
10	Transmit		M		Disable
11	Receive		M		Disable
12	Loopback		M		Disable
13	Collision Presence		M		Disable
14	SQE Test		M		Disable
15	Link Test Fail Extend state exit condition	14.2.1.7	M		Deferred until RD = idle and DO = idle
16	Power-on state	14.2.1.7	O		Link Test Fail Reset
17	Pulse/data discrimination	14.2.1.7	M		Link test pulse not detected as data

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14.10.4.5.9 MAU state diagram requirements

	Parameter	Subclause	Req	Imp	Value/comment
1	Transmit, Receive, Loopback, and Collision Presence Functions state diagram	14.2.3	C		Meets requirements of Figure 14–3. Conditional on whether or not the function is to be performed (14.10.4.5.1/3 and 14.10.4.5.1/4).
2	MAU Transmit and Receive Functions state diagram (full duplex mode)	14.2.3	C		Conditional on whether or not the function is to be performed (14.10.4.5.1/3 and 14.10.4.5.1/4).
3	*signal_quality_error* Message Test Function state diagram	14.2.3	C		Meets requirements of Figure 14–4. Conditional on whether or not the function is to be performed (14.10.4.5.1/7).
4	Jabber Function state diagram	14.2.3	M		Meets requirements of Figure 14–5.
5	Link Integrity Test Function state diagram	14.2.3	M		Meets requirements of Figure 14–6.

14.10.4.5.10 AUI requirements

	Parameter	Subclause	Req	Imp	Value/comment
1	AUI implementation	14.3	O		If implemented, refer to 14.10.4.6.
2	AUI messages	14.2.2	M		Comply to 7.2.1.

14.10.4.5.11 Isolation requirements

	Parameter	**Subclause**	**Req**	**Imp**	**Value/comment**
1	Isolation, MDI leads to DTE Physical Layer circuits	14.3.1.1	M		Any one of three tests listed in 14.3.1.1
2	Resistance after breakdown test	14.3.1.1	M		≥ 2 MΩ at 500 Vdc

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14.10.4.5.12 Transmitter specification

	Parameter	Subclause	Req	Imp	Value/comment
1	Peak differential output voltage on TD circuit	14.3.1.2.1	M		2.2 to 2.8 V
2	Harmonic content, all-ones signal	14.3.1.2.1	M		All harmonics ≥ 27 dB below fundamental
3	Output waveform, with scaling of voltage template	14.3.1.2.1	M		Within Figure 14–9 template
4	Start of TP_IDL waveform, with each specified load, with and without twisted-pair model	14.3.1.2.1	M		Within Figure 14–10 template, overshoot ≤ +50 mV after excursion below –50 mV
5	Link test pulse waveform, with each specified load, with and without twisted-pair model	14.3.1.2.1	M		Within Figure 14–10 template, overshoot ≤ +50 mV after excursion below –50 mV
6	TD circuit differential output impedance	14.3.1.2.2	M		Reflection ≥ 15 dB below incident, any simplex link segment
7 8	Transmitter added timing jitter: Into 100 Ω through twisted-pair model Into 100 Ω	14.3.1.2.3	 M M		 ±3.5 ns max ±8 ns max
9	Common-mode to differential-mode conversion	14.3.1.2.4	M		≥ 29 – 17 $\log_{10}$(f/10) dB, f=1–20 MHz, f in MHz
10	TD circuit common-mode output voltage	14.3.1.2.5	M		< 50 mV peak
11	TD circuit common-mode rejection, 15 V peak 10.1 MHz sinusoid	14.3.1.2.6	M		≤ 100 mV differential and ≤ 1 ns jitter
12	TD circuit fault tolerance	14.3.1.2.7	M		No damage from a short circuit
13	TD circuit short-circuit current	14.3.1.2.7	M		300 mA max
14	TD circuit common-mode voltage withstand	14.3.1.2.7	M		1000 V min, applied per Figure 14–15
15	Power cycle behavior	14.3.2.3	M		No extraneous signals on the TD circuit

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14.10.4.5.13 Receiver specification

	Parameter	Subclause	Req	Imp	Value/comment
1	RD circuit signal acceptance	14.3.1.3.1	M		Figures 14–16, 14–17, template
2	Received signal jitter accept	14.3.1.3.1	M		At least ±13.5 ns
3	Receiver added jitter	14.3.1.3.1	M		≤ ±1.5 ns, RD to DI circuits
4	RD circuit link test pulse acceptance	14.3.1.3.2	M		Figure 14–12 template
	RD circuit differential noise rejection:	14.3.1.3.2			
5	Signal (1)		M		≤ 300 mV peak
6	Signal (2)		M		≤ 6.2 V peak-to-peak, ≤ 2 MHz
7	Signal (3)		M		Single cycle ≤ 6.2 V, either phase, 2–15 MHz
8	Idle detection, RD circuit	14.3.1.3.3	M		Within 2.3 bit times
9	RD circuit differential input impedance	14.3.1.3.4	M		Reflected signal ≥ 15 dB below incident, any simplex link segment
10	RD circuit common-mode rejection	14.3.1.3.5	M		25 V peak-to-peak square wave to add ≤ 2.5 ns jitter
	RD circuit fault tolerance:	14.3.1.3.6			
11	Short circuit		M		Indefinite short circuit
12	Common-mode voltage		M		1000 V impulse, applied per Figure 14–19

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14.10.4.5.14 MDI requirements

	Parameter	Subclause	Req	Imp	Value/comment
1	MDI connector	14.5.1	M		ISO/IEC 8877: 1992 jack
2 3 4 5	MDI connector contact assignment: 1 2 3 6	14.5.1	 M M M M		 TD+ TD– RD+ RD–
6	Crossover function implemented	14.5.2	O		Remote MAU from DTE (recommended)
7	Crossover function indication	14.5.2	C		X symbol on MDI connector. Conditional on crossover function implementation. Refer to response to 14.10.4.5.14/6
8 9 10 11	MDI-X connector contact assignment: 1 2 3 6	14.5.2	 C C C C		 RD+ RD– TD+ TD– Conditional on crossover function implementation. Refer to response to 14.10.4.5.14/6.

14.10.4.5.15 Safety requirements

	Parameter	Subclause	Req	Imp	Value/comment
1	Safety grounding path	14.7.2.2	C		Must be via PG circuit. Conditional on AUI implementation. Refer to response for 14.10.4.5.10/1 or PIXIT
2	MAU labeling	14.8	O		Data rate, current, any applicable safety warnings (recommended)
3	General safety	14.7.1	M		Conforms to IEC 60950: 1991
4	Application of telephony voltages	14.7.2.4	M		Creates no safety hazard

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14.10.4.6 PICS proforma tables for MAU AUI characteristics

The whole of 14.10.4.6 is conditional on the AUI being implemented and accessible for testing. Refer to response for Clause 14.10.4.5.10/1 or PIXIT.

14.10.4.6.1 Signal characteristics

	Parameter	Subclause	Req	Imp	Value/comment
1	Signaling rate (stated on label)	7.3.2	C		10 Mb/s
2	CS0 signal frequency (on CI)	7.3.1.2	C		10 MHz ± 15%
3	CS0 signal duty cycle	7.3.1.2	C		60:40 worst case

14.10.4.6.2 DI and CI driver characteristics

	Parameter	Subclause	Req	Imp	Value/comment
	Differential output voltage:	7.4.1.1			
1	Loaded		C		Figure 7–11
2	Idle state		C		≤ 40 mV into test load
3	Start of idle		C		Figure 7–12
4	Current into test load while idle	7.4.1.1	C		4 mA max after 80 BT
5	Requirements after idle	7.4.1.2	C		First bit to Figure 7–11
6	Common-mode output voltage, ac	7.4.1.3	C		≤ 40 mV peak. Figure 7–13
7	Differential output voltage, open circuit	7.4.1.4	C		13 V peak max
8	Common-mode output voltage, dc	7.4.1.5	C		≤ 5.5 V. Figure 7–13
9	Fault tolerance	7.4.1.6	C		Figure 7–14
10	Fault current	7.4.1.6	C		≤ 150 mA, any Figure 7–14 state

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14.10.4.6.3 DO receiver characteristics

	Parameter	Subclause	Req	Imp	Value/comment
1	Unsquelched threshold	7.4.2.1	C		160 mV max differential
2	Squelch	14.3.2.1	C		Reject signals ≤ 160 mV magnitude
3	High-to-idle transition on DO circuit	7.4.1.1	C		Must not cause output
4	Differential input impedance at 10 MHz	7.4.2.2	C		Real part: 77.83 Ω ± 6%, 0 ≤ phase angle in degrees ≤ real part × 0.0338
5	Common-mode range, ac	7.4.2.3	C		3 V min 30 Hz to 40 kHz, 100 mV min 40 kHz to 10 MHz
6	Total common-mode range	7.4.2.4	C		Magnitude of 0 to 5.5 V ac + dc
7	Common-mode current limit	7.4.2.4	C		≤ 1 mA
8	IDL detection	7.3.1.1	C		≤ 1.6 bit times
9	Requirements after idle	7.4.2.5	C		Receiver in specification after start-up delay
10	Receiver fault tolerance	7.4.2.6	C		Figure 7–15
11	Input fault current	7.4.2.6	C		3 mA max for Figure 7–15

14.10.4.6.4 Power consumption

	Parameter	Subclause	Req	Imp	Value/comment
1	Power surge limitation	14.3.2.3	C		≤2×10^{-3} A·s
2	Power surge duration	14.3.2.3	C		100 ms max
3	Steady-state current drawn	14.3.2.3	C		≤ 500 mA
4 5	Power-up capability: Current limited sources Voltage sources	 14.3.2.3 7.5.2.5	 C C		 500 mA limited 11.28 to 15.75 V, any permissible AUI cable
6	Power cycle behavior	14.3.2.3	C		No extraneous signals on CI nor DI circuits
7	Low VP circuit behavior	7.5.2.5	C		No disruption of media

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14.10.4.6.5 Circuit termination

	Parameter	Subclause	Req	Imp	Value/comment
1	Common-mode termination	7.5.2.6	C		If used must be to VC
2	Pins 1,4,11,14 impedance to VC circuit	7.5.2.8	C		≤ 5 Ω at 5 MHz
3	Pins 1,4,11,14 coupling to VC circuit	7.5.2.8	C		Capacitive

14.10.4.6.6 Mechanical characteristics

	Parameter	Subclause	Req	Imp	Value/comment
1	D-type connector dimensions	7.6.2	C		IEC 60807-2: 1992 15-pole male
2	Shell plating material	7.6.2	C		Conductive
3	Shell multiple contact points	7.6.2	O		Number not defined (recommended)
4	Shell life expectancy	7.6.2	C		≤5 mΩ / 500 matings
5	Locking posts and mounting	7.6.1	C		Figures 7–17, 7–19
	Pin connections:	7.6.3			Circuit
6	3		C		Data out A
7	10		C		Data out B
8	11		C		Capacitor to VC
9	5		C		Data in A
10	12		C		Data in B
11	4		C		Capacitor to VC
12	7		C		No connection
13	15		C		No connection
14	8		C		Capacitor to VC
15	2		C		Control in A
16	9		C		Control in B
17	1		C		Capacitor to VC
18	6		C		Voltage common
19	13		O		Voltage plus
20	14		C		Capacitor to VC
21	Shell		C		Protective Ground (Conductive Shell)

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14.10.4.7 PICS proforma tables for 10BASE-T link segment

14.10.4.7.1 10BASE-T link segment characteristics

	Parameter	Subclause	Req	Imp	Value/comment
	Cable size:				Cable size affects NEXT limits
1	25-pair cable or binder groups	14.4.3.1.1	O		
2	4-pair cable	14.4.3.1.2	O		
3	Other	14.4.3.1.3	O		
4	Insertion loss, 5.0 to 10 MHz	14.4.2.1	M		≤ 11.5 dB
5	Differential characteristic impedance of a 3 m cable section, 5.0 to 10 MHz	14.4.2.2	M		85 to 111 Ω
6	Input impedance averaged, 5.0 to 10 MHz	14.4.2.2	M		85 to 111 Ω
7	Medium timing jitter (for defined test signal)	14.4.2.4	M		±5.0 ns max
	Delay:				
8	Per meter		M		≤ 5.7 ns/m
9	Link segment		M		≤ 1000 ns
	NEXT loss, pair-to-pair, 5.0 to 10 MHz:				
10	25-pair cable and binder groups	14.4.3.1.1	C		≥ 30 – 15 $\log_{10}$(f/10) dB
11	4-pair cable	14.4.3.1.2	C		≥ 26 – 15 $\log_{10}$(f/10) dB These requirements are conditional on the responses in clauses 14.10.4.7.1/1 and 14.10.4.7.1/2, f in MHz
12	MDNEXT at 5.0, 7.5, and 10 MHz	14.4.3.2	M		≥ 23 – 15 $\log_{10}$(f/10) dB, f in MHz
	Noise environment:				
13	Impulse noise (into defined circuit)	14.4.4.1	M		Fewer than 0.2 impulses/s of ≥ 264 mV
14	Crosstalk noise	14.4.4.2	M		≤ 264 mV
15	Connectors	14.5.1	M		ISO/IEC 8877: 1992 plug
16	Literature indicates the distance and environmental conditions over which 14.4 specifications are met	14.7.3.2	O		

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14.10.4.8 PICS proforma tables for Auto-Negotiation able MAUs

The following are conditional on whether the Auto-Negotiation algorithm is provided (Clause 28).

	Parameter	Subclause	Req	Imp	Value/Comment
1	TP_IDL	14.2.1.1	C		Defined in 28.2.1
2	Link Integrity Test Function State Diagram power-on default	14.2.1.7	C		Power-on in Link Test Fail Reset state
3	Link Test Fail state exit conditions	14.2.1.7	C		autoneg_wait_timer expired and either RD = active or consecutive link test pulses = 3 min., 10 max
4	Technology Dependent Interface support	14.2.1.7	C		In the Link Integrity Test state diagram function “link_status=OK” is added to the LINK TEST PASS state and “link_status=FAIL” is added to the LINK TEST FAIL RESET state
5	Link test pulse waveform for FLP Burst with and without twisted-pair model	14.3.1.2.1	C		Within Figure 14–10 template for, all pulses in FLP Burst, overshoot ≤ +50 mV after excursion below –50 mV
6	MAU indicates full duplex mode capability during Auto-Negotiation	14.2.1.8	C		Function optionally performed by embedded MAUs, not performed by MAUs that implement an AUI connector.

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15. Fiber optic medium and common elements of medium attachment units and star, type 10BASE-F

15.1 Scope

15.1.1 Overview

Clauses 15, 16, 17, and 18 define the functional, electrical, optical, and mechanical characteristics of the type 10BASE-FP (Passive) MAU, the type 10BASE-FB Backbone (Synchronous Active) MAU, the type 10BASE-FL Link (Asynchronous Active) MAU, the type 10BASE-FP (Passive) Star, and one common medium for use with those MAUs and the star. The purpose of the MAUs is to provide a means of attaching full duplex DTEs (10BASE-FL only), half duplex DTEs (10BASE-FP and 10BASE-FL only), or repeaters to the local network medium. The purpose of the 10BASE-FP Star is to provide the means of interconnecting 10BASE-FP MAUs into a star topology segment. The IEEE 802.3 repeaters are used to interconnect the star segment to other 10 Mb/s baseband segments. Information on selecting segment types for various applications is provided in 15.1.3.4.

The 10BASE-F specification builds upon Clause 1 through Clause 7 and Clause 9 of this standard. The relationship of this clause to the entire ISO/IEC 8802-3 LAN International Standard is shown in Figures 15–1a), 15-1b), and 15-1c) for 10BASE-FP, 10BASE-FB, and 10BASE-FL, respectively.

10BASE-F is specifically intended to be interoperable and compliant with the requirements for attachment to DTEs and repeaters via the 10 Mb/s Attachment Unit Interface (AUI). The use of 10BASE-F in networks with other IEEE 802.3, 10 Mb/s baseband segments is governed by the system considerations detailed in Clause 13.

15.1.1.1 Fiber optic medium attachment units (MAUs)

The MAUs specified in this clause, Clause 16 (10BASE-FP), Clause 17 (10BASE-FB), and Clause 18(10BASE-FL) have the following general characteristics:

a) They provide a means of coupling the PLS through the AUI to the fiber optic segment by way of the MDI.
b) They support message traffic at a data rate of 10 Mb/s.
c) They provide for driving up to 1 km of fiber optic cable with a 10BASE-FP Star connected in the middle between two 10BASE-FP MAUs. Provide for driving up to 2 km of fiber optic cable between two repeaters that have embedded 10BASE-FB MAUs. Provide for driving up to 2 km of fiber optic cable between two 10BASE-FL MAUs. Provide backward compatibility for communicating between FOIRL MAUs and 10BASE-FL MAUs over up to 1 km of fiber optic cable.
d) They permit the DTE to test the MAU and the availability of the medium.
e) They support system configurations using the CSMA/CD access mechanism defined in this standard.
f) They provide uninterrupted carrier sense during collisions.
g) They support a star cabling topology.
h) They allow incorporation of the MAU within the physical bounds of a DTE or repeater. (See Clause 17 for 10BASE-FB restrictions.)

15.1.1.2 Fiber optic passive star

The 10BASE-FP Star is a passive optical device that receives optical signals from, and distributes them to, connected devices (see Figure 15–2b). The 10BASE-FP Star is not a repeater.

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15.1.1.3 Repeater unit

The repeater unit has the characteristics defined in Clause 9. Repeater units are used as a hub in a star topology network in which DTEs attach directly to link segments. Repeater units are also used to extend the physical system topology of mixing segments by connecting 10BASE-FP or coaxial cable segments to other segments. Repeater units are used to connect 10BASE-F segments of any type to other 10BASE-F segments, and to any other 10 Mb/s baseband media types. 10BASE-FB segments connect only 10BASE-FB ports on repeaters.

NOTE—While 9.6.6 autopartitioning is not required as a mandatory feature on 10BASE-FB ports, it should be recognized that it could be of benefit where there is a high probability of misconnections of incompatible ports, e.g., patch panels shared between 10BASE-FB and other fiber optic communication technologies.

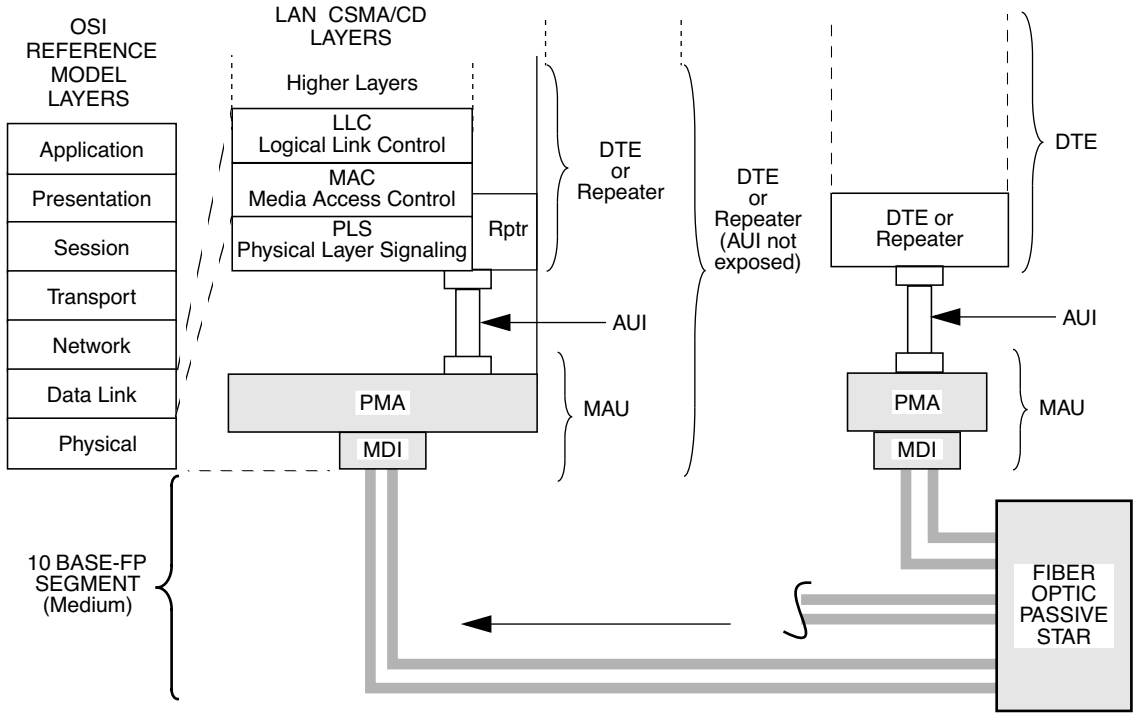
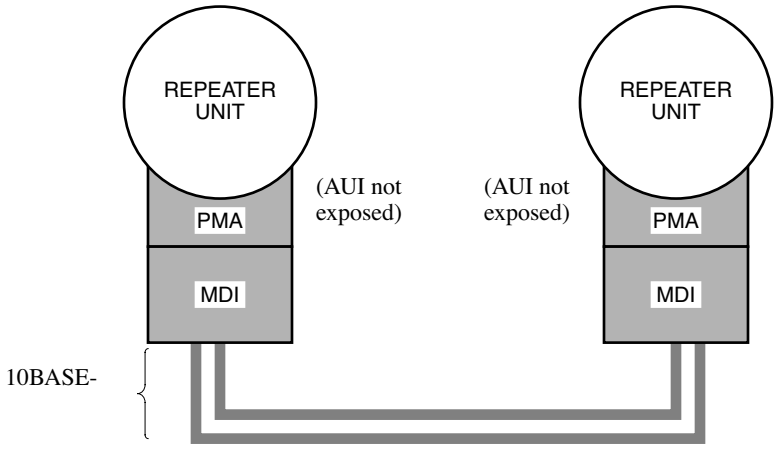


Figure 15–1—10BASE-F relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

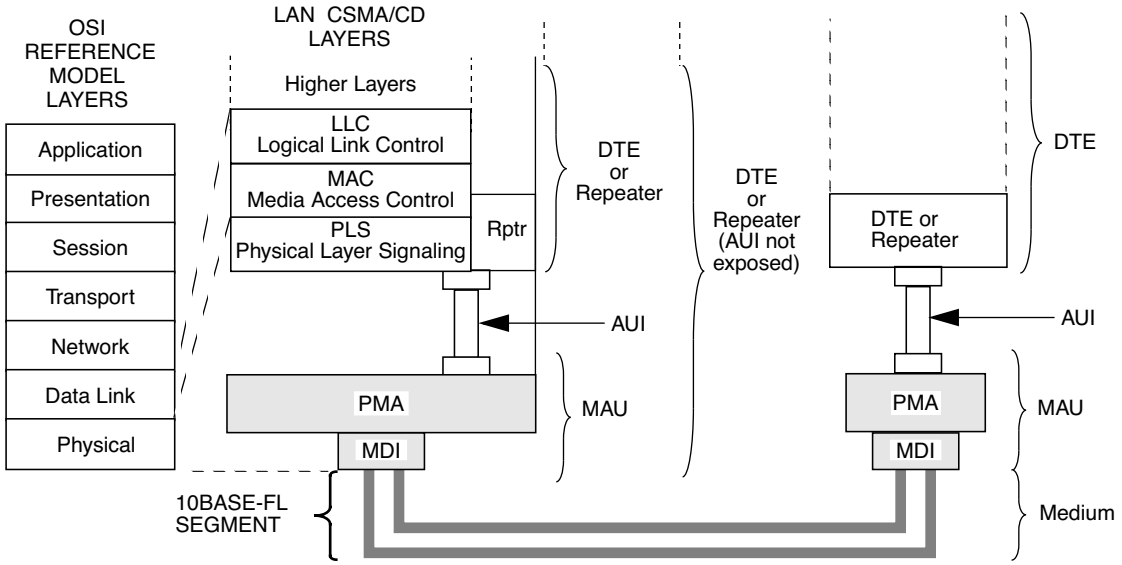


b) 10BASE-FB relationship to CSMA/CD LAN

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c) 10BASE-FL relationship to OSI and CSMA/CD LAN

Figure 15-1—(*Continued*)
10BASE-FL relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the ISO/IEC CSMA/CD LAN model

15.1.2 Definitions

See 1.4.

15.1.3 Applications perspective: MAUs, stars, and fiber optic medium

This clause states the broad objectives and assumptions underlying the specifications defined in Clauses 15, 16, 17, and 18.

15.1.3.1 Objectives

a) To provide a physical means for communication between LAN data link entities using fiber optic media connected in a star topology.
b) To ensure compatibility of independently developed physical, electrical, and optical interfaces.
c) To provide a communication channel capable of high bandwidth and low bit-error rate performance. The resultant mean bit-error rate, between AUIs over a fiber segment, should be less than one part in 10^9.
d) To provide for ease of installation and service.
e) To ensure that fairness of DTE access is not compromised.

15.1.3.2 Compatibility considerations

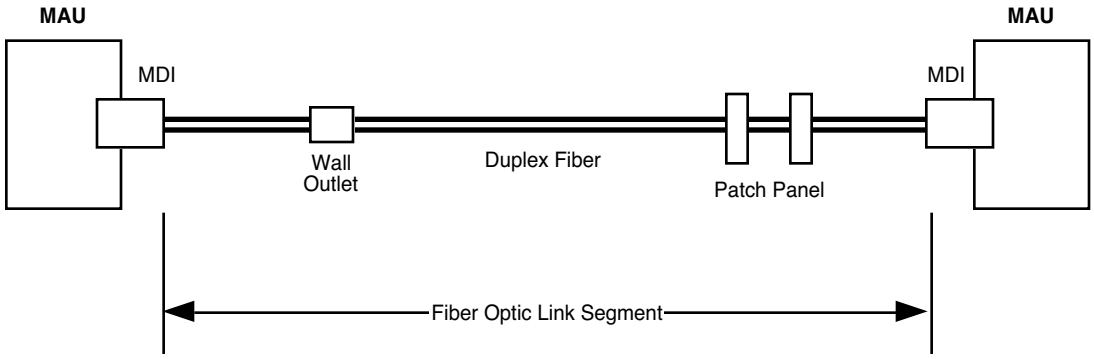
All implementations of 10BASE-FP, 10BASE-FB, and 10BASE-FL fiber optic systems shall be compatible at their respective MDIs when used in accordance with the restrictions of Clause 9 and subclause 16.5 where appropriate. When FOIRL segments are used, all 10BASE-FL MAUs shall be compatible with the FOIRL MDI specified in 9.9 except for the media connector, which shall be as specified in 15.3.2.

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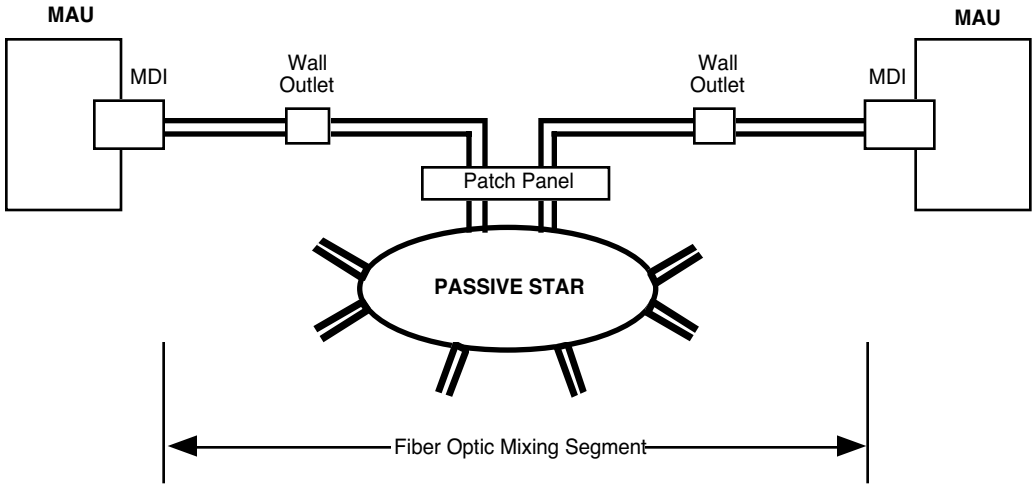
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a) Example fiber optic link segment, 10BASE-FB and 10BASE-FL



b) Example fiber optic mixing segment, 10BASE-FP

Figure 15–2—Fiber optic link and mixing segments

Implementations of 10BASE-F of any one type are not compatible with 10BASE-F of any other type at the MDI.

Clause 15 provides medium specifications for interconnection of the fiber optic MAUs and star defined in Clauses 16, 17, and 18. The star specified in 16.5 completes the specification of the media for a 10BASE-FP segment. The medium itself, the functional capability of the 10BASE-FP, 10BASE-FB, and 10BASE-FL MAUs, and the AUI are defined to provide the highest possible level of compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the MAU in an application-dependent manner provided that the MDI and AUI specifications are satisfied. The provision of the physical and mechanical implementation of the AUI is optional for Clause 16 and 18 MAUs, and is not applicable for Clause 17 MAUs.

15.1.3.3 Relationship to PLS and AUI

Clause 15, together with Clauses 16, 17, or 18, defines the portion of the physical layer and medium for the LAN necessary to couple a DTE or repeater message path to and from the medium.

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A close relationship exists between Clause 7 and the 10BASE-FP, 10BASE-FB, and 10BASE-FL MAUs defined in Clauses 16, 17, and 18, respectively. Clause 15 specifies the physical medium parameters, and Clauses 16, 17, and 18 the PMA logical functions residing in the physical MAU. The MAU provides services to the PLS defined in Clause 7 by means of the AUI. 10BASE-F MAUs support a subset of the AUI services specified in Clause 7. 10BASE-F MAUs do not support the optional *isolate* function, the optional CO circuit, or the optional CS1 signal on the CI circuit.

The design of an external MAU component requires the use of Clause 15, Clauses 16 or 18, and Clause 7 for the PLS and AUI specifications.

The figures and numerous textual references throughout Clauses 15, 16, 17, and 18 refer to terminology associated with the AUI (that is, DO, DI, and CI). Since an embodiment of the 10BASE-FP, 10BASE-FB, or 10BASE-FL MAU does not require implementation of an AUI, the DO, DI, and CI circuits may not physically exist. However, they are logically present, and MAU operation is defined in terms of their messages.

15.1.3.4 Guidelines for implementation of systems

The fiber optic systems defined herein cover a wide range of LAN applications in which the advantages of fiber optics are paramount. These advantages include noise immunity, low attenuation, bandwidth upgradeability, data security, and use in environments where the use of electric circuits would be hazardous. These systems allow construction of complex networks according to the system topology rules in Clause 13. Choice of system approach may be aided by the following guidelines:

— 10BASE-FP, Clause 16: A passive-star system for interconnecting repeaters or DTEs with up to 1 km per segment, useful where central power is unavailable or not sufficiently reliable for the intended application.
— 10BASE-FB, Clause 17: A system for interconnecting repeaters with up to 2 km per segment and for backbone applications where a large number of repeaters must be cascaded.
— 10BASE-FL, Clause 18: A system for interconnecting repeaters or DTEs with up to 2 km per segment and where backward compatibility with 9.9 (FOIRL) (up to 1 km per segment) is desirable. This system also supports full duplex operation (see 1.1.1).

Repeaters (Clause 9) must be used to connect other media to the above fiber optic segments. Repeaters also must be used to interconnect FOIRL, 10BASE-FB, 10BASE-FP, and 10BASE-FL segments. 10BASE-FB segments can be used only between 10BASE-FB ports on repeaters.

15.1.3.5 Modes of operation

10BASE-F MAUs are capable of operating in normal mode only (see 7.1.4). They shall not operate in monitor mode. A MAU attached to a repeater shall not be in full duplex mode.

The operation of a 10BASE-FL MAU differs depending on whether the attached DTE is operating in the half duplex or full duplex mode (see 1.1.1). In the full duplex mode, functions relating to the loopback of transmitted data (DO) onto the receive path (DI) are disabled (see 18.3.1.3, 18.3.1.6).

The requirements specified in clauses of this standard labeled “half duplex mode only” do not apply to a MAU used with a DTE configured for full duplex operation. It is the responsibility of the designer and/or user of equipment operating in full duplex mode to ensure that the 10BASE-FL MAU used or incorporated is properly configured for full duplex operation.

10BASE-FP and 10BASE-FB MAUs are capable of operating in half duplex mode only.

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15.2 MDI optical characteristics

The transmit and receive optical parameters for the 10BASE-FP, 10BASE-FB, and 10BASE-FL fiber optic systems are summarized in Table 15–1. Optical measurements shall be made with the MDI terminated with the optical connector specified in 15.3.2 and the optical fiber specified in 15.3.1. Fiber length shall be sufficient to attenuate cladding mode distribution.

NOTE—Transmit and receive optical parameters refer to optical power in the core of the respective fiber (15.3.1). Fibers currently available typically require 1 m to 5 m to remove optical power from the cladding.

15.2.1 Transmit optical parameters

15.2.1.1 Center wavelength

The center wavelength of the optical source emission shall be as specified in Table 15–1.

15.2.1.2 Spectral width

The full width half maximum (FWHM) spectral width of the optical source shall be as specified in Table 15–1.

15.2.1.3 Optical modulation extinction ratio

The optical modulation method is on-off keying of the optical power source. The minimum extinction ratio shall be as specified in Table 15–1, measured at the normalization points (15.2.1.11).

15.2.1.4 Optical Idle Signal amplitude

The optical Idle Signal shall be as specified in Table 15–1.

15.2.1.5 Optical transmit pulse logic polarity

LO on the AUI DO circuit shall be represented at the MDI as LO and as the higher optical power level transmitted at the MDI. HI on the AUI DO circuit shall be represented at the MDI as HI and as the lower optical power level transmitted at the MDI (see 7.4.2.1). A 10BASE-FP Star by its nature is noninverting from any input to any output.

15.2.1.6 Optical transmit pulse rise and fall times

The optical rise and fall times at the MDI transmitter shall be measured from the 10% to 90% levels. The rise and fall times and their difference shall be as specified in Table 15–1.

15.2.1.7 Optical transmit pulse overshoot and undershoot

The maximum optical overshoot and undershoot shall be as specified in Table 15–1.

15.2.1.8 Optical transmit pulse edge jitter

The total transmitted edge jitter measured at the MDI shall be as specified in Table 15–1 for a transmitted waveform consisting of a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits. The jitter at the MDI shall be measured at the power level median of the optical waveform's upper and lower power levels (as determined from the previous 16 or more transitions in any valid optical bit stream). This does not include any effects from variations of Optical Transmit Pulse Duty Cycle (15.2.1.9).

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Table 15–1—MDI parameters

Subclause	Parameter	Units	10BASE-FP	10BASE-FB	10BASE-FL
15.2.1	TRANSMIT OPTICAL PARAMETERS				
15.2.1.1	Center wavelength —min. —max.	 nm nm	 800 910	 800 910	 800 910
15.2.1.2	Spectral width (FWHM)	nm	<75	<75	<75
15.2.1.3	Optical modulation extinction ratio	dB	≤13	≤13	≤13
15.2.1.4	Optical idle signal amplitude	dBm	≤57	see 15.2.1.10	see 15.2.1.10
15.2.1.6	Optical transmit pulse rise and fall times —max. (data) —min. (data) —max. difference (data) —max. (idle) —min. (idle) —max. difference (idle)	 ns ns ns ns ns ns	 10 2 3 N/A N/A N/A	 10 0 3 10 0 3	 10 0 3 25 0 25
15.2.1.7	Optical transmit pulse —overshoot —undershoot	 % %	 5 5	 25 10	 25 10
15.2.1.8	Optical transmit pulse edge jitter —added, DO circuit to MDI —total at MDI (data) —total at MDI (idle)	 ns ns ns	 N/A ±1 N/A	 N/A ±2 ±2	 ±2 ±4 N/A
15.2.1.9	Optical transmit pulse Duty cycle distortion —data —idle	 ns ns	 ±1 N/A	 ±2.5 ±2.5	 ±2.5 ±50.0
15.2.1.10	Optical transmit average power range —min. —max.	 dBm dBm	 –15 –11	 –20 –12	 –20 –12
15.2.2	RECEIVE OPTICAL PARAMETERS				
15.2.2.1	Optical receive average power range —min. —max.	 dBm dBm	 –41 –27	 –32.5 –12.0	 –32.5 –12.0
15.2.2.2	MAU optical receive edge jitter (data) —received at MDI —added, MDI to DI circuit —total at DI circuit (MAU end of AUI)	 ns ns ns	 ±4.5 N/A N/A	 ±2.0 N/A ±6.5	 ±6.5 ±8.5 ±15.0
15.2.2.4	Optical receive pulse rise and fall times —max. (data) —min. (data) —max. difference (data) —max. (idle) —min. (idle) —max. difference (idle)	 ns ns ns ns ns ns	 18.5 2.0 3.0 N/A N/A N/A	 31.5 0.0 3.0 31.5 0.0 3.0	 31.5 0.0 3.0 41.0 0.0 25.0

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15.2.1.9 Optical transmit pulse duty cycle distortion

The optical pulse duty cycle shall be as specified in Table 15–1. The duty cycle distortion measured at the output of the electro-optic source shall be measured at the power level median of the optical waveform's upper and lower power levels (as determined in 15.2.1.10).

15.2.1.10 Optical transmit average power range

The optical transmit average power coupled into the core of the fiber shall be in the range specified in Table 15–1 at the MDI.

To meet the 10BASE-FP power range, the use of one or more techniques such as emitters with a focused radiation pattern, optical power setting, or temperature compensation may be necessary.

NOTE—The optical power ranges shown in Table 15–1 can be met by the following:

10BASE-FB and 10BASE-FL MDI
- Nominal average power, beginning of life–15 dBm
- Transmit power tolerance*±3 dB
- Transmit power degradation, end of life–2 dB

10BASE-FP MDI
- Nominal average power, beginning of life–12.5 dBm
- Transmit power tolerance*±1.5 dB
- Transmit power degradation, end of life–1 dB

* Transmit power tolerance includes emitter, optical connector, and optical fiber tolerances.

15.2.1.11 Optical transmit signal templates

The transmitted optical waveforms for the 10BASE-FP MAU, 10BASE-FB MAU, and 10BASE-FL MAU shall fall within the templates shown in Figure 15–3, Figure 15–4, and Figure 15–5, respectively, when normalized. Normalization is achieved by linearly scaling and shifting the waveform amplitude and shifting the waveform timebase so that it intersects the two normalization points indicated by the black dots on the templates. These templates show a graphical representation of the transmit parameters described in 15.2.1.3, 15.2.1.6, 15.2.1.8, and 15.2.1.9. Table 15–1 lists the appropriate numerical values for these parameters. If any conflict exists between the templates and Table 15–1, the table shall take precedence.

The definition of "normalized optical power" is indicated on Figures 15–3, 15–4, and 15–5. The measured optical power is scaled and shifted so that the definition of "0" optical power and "1" optical power is determined by the average signal value at the points indicated by the black dots on the figures.

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15.2.1.11.1 10BASE-FP optical transmit signal template

The points of inflection for the template of Figure 15–3 are defined by the coordinate pairs contained in Table 15–2.

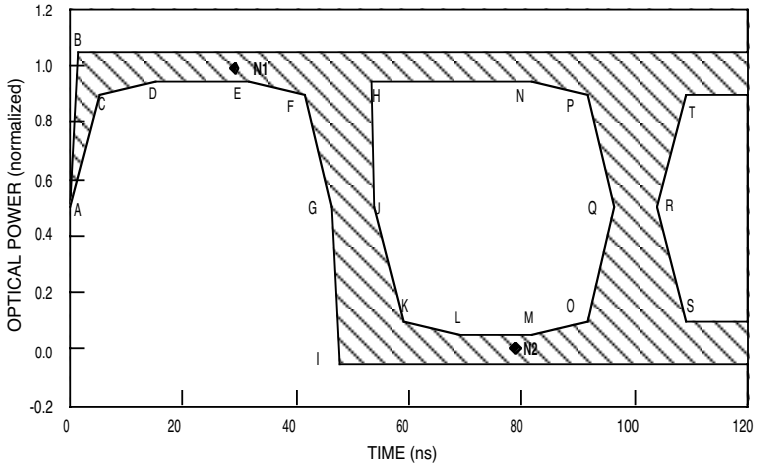


Figure 15–3—10BASE-FP MAU transmit waveform template

Table 15–2—Transmitted optical waveform values for Figure 15–3

Reference	Time (ns)	Optical power (normalized)
A	0.0	0.5
B	1.375	1.05
C	5.0	0.9
D	15.0	0.95
E	31.0	0.95
F	41.0	0.9
G	46.0	0.5
H	52.875	0.95
I	47.375	–0.05
J	54.0	0.50
K	59.0	0.10
L	69.0	0.05
M	81.0	0.05

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Table 15–2—Transmitted optical waveform values for Figure 15–3

Reference	Time (ns)	Optical power (normalized)
N	81.0	0.95
O	91.0	0.10
P	91.0	0.90
Q	96.0	0.50
R	104.0	0.50
S	109.0	0.10
T	109.0	0.90
N1	29.0	1.00
N2	79.0	0.00

15.2.1.11.2 10BASE-FB optical transmit signal template

The points of inflection for the template of Figure 15–4 are defined by the coordinate pairs contained in Table 15–3.

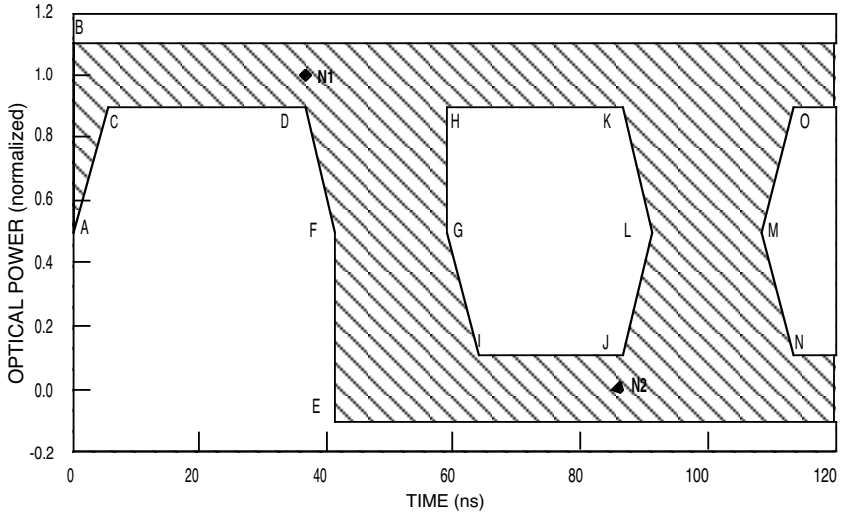


Figure 15–4—10BASE-FB MAU transmit waveform template

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Table 15–3—Transmitted optical waveform for Figure 15–4

Reference	Time (ns)	Optical power (normalized)
A	0.0	0.5
B	0.0	1.1
C	5.0	0.9
D	36.0	0.9
E	41.0	–0.1
F	41.0	0.5
G	59.0	0.5
H	59.0	0.9
I	64.0	0.1
J	86.0	0.1
K	86.0	0.9
L	91.0	0.5
M	109.0	0.5
N	114.0	0.1
O	114.0	0.9
N1	36.0	1.00
N2	86.0	0.00

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15.2.1.11.3 10BASE-FL Optical transmit signal template

The points of inflection for the template of Figure 15–5 are defined by the coordinate pairs contained in Table 15–4. This template is for data only.

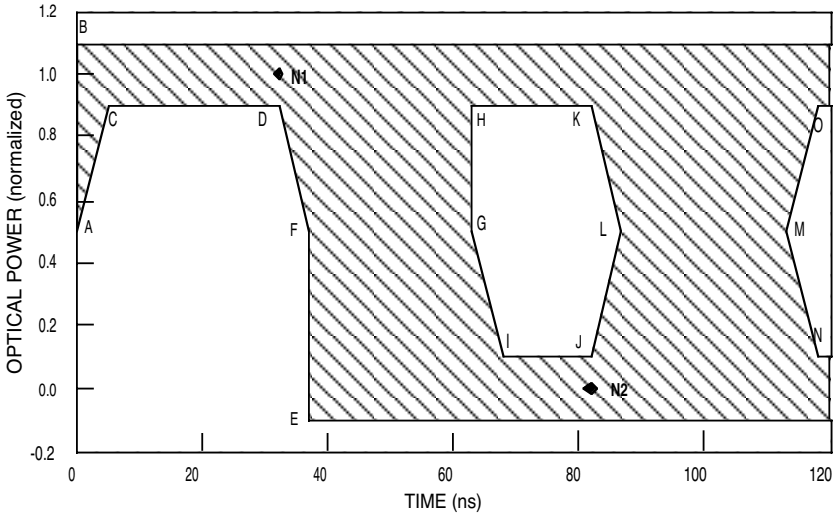


Figure 15–5—10BASE-FL MAU transmit waveform template (data only)

Table 15–4—Transmitted optical waveform values for Figure 15–5

Reference	Time (ns)	Optical power (normalized)
A	0.0	0.5
B	0.0	1.1
C	5.0	0.9
D	32.0	0.9
E	37.0	–0.1
F	37.0	0.5
G	63.0	0.5
H	63.0	0.9

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Table 15–4—Transmitted optical waveform values for Figure 15–5

Reference	Time (ns)	Optical power (normalized)
I	68.0	0.1
J	82.0	0.1
K	82.0	0.9
L	87.0	0.5
M	113.0	0.5
N	118.0	0.1
O	118.0	0.9
N1	32.0	1.00
N2	82.0	0.00

15.2.2 Receive optical parameters

The bit-error rate (BER) shall be less than one part in 10^9, when measured between two AUIs attached to a single 10BASE-FP, 10BASE-FB, or 10BASE-FL segment for all combinations of valid optical receive parameters specified in the following subclauses and valid optical transmit pulse duty cycle distortion (15.2.1.9). For the case of integrated MAUs this measurement must be made by inference.

15.2.2.1 Optical receive average power range

The optical receive average power shall be in the range specified in Table 15–1 at the MDI when a single transmitter is transmitting on the medium.

15.2.2.2 Optical receive pulse edge jitter

The received edge jitter shall be as specified for a received waveform consisting of a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits. The jitter at the input MDI shall be measured at the power level median of the optical waveform's upper and lower power levels (as determined from the previous 16 or more transitions in any valid bit stream). The jitter measured at the output of the DI circuit driver shall be measured at the zero crossing points (as determined from the previous 16 or more transitions in any valid bit stream).

NOTE—For the transmit optical parameters of Table 15–1 and the fiber parameters of 15.3.1, the contribution to jitter for a 2 km long fiber is less than 10 ps (.01 ns). For purposes of calculation and specifications, no jitter contribution is allocated to the fiber optic segment (including any 10BASE-FP Star).

Optical signals at the input of the MDI receiver shall be received and sent to the DI circuit if they have total received jitter of no more than that specified in Table 15–1.

The maximum additional edge jitter introduced at a MAU from the input of the MDI receiver to the output of the DI circuit driver shall be as specified in Table 15–1.

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The total edge jitter at the output of the DI circuit driver shall be no more than that given by the sum of the worst-case edge jitter components specified in Table 15–1.

15.2.2.3 Optical receive pulse logic polarity

The higher optical power level received at the MDI shall be represented by LO at both the MDI and the AUI DI circuit. The lower optical power level received at the MDI shall be represented by HI at both the MDI and the AUI DI circuit (see 7.4.2.1).

15.2.2.4 Optical receive pulse rise and fall times

The optical rise and fall times at the MDI receiver shall be measured from the 10% to 90% levels. The rise and fall times and their maximum difference shall be as specified in Table 15–1 at the MDI.

15.3 Characteristics of the fiber optic medium

The fiber optic transmission medium consists of one or more sections of fiber optic cables with any intermediate connectors required to connect sections together and terminated at each end in the optical connector plug as specified in 15.3.2. The fiber optic medium spans from one MDI to another MDI.

15.3.1 Optical fiber and cable

The optical medium requirements are satisfied by the 62.5/125 μm nominal diameter fiber specified in IEC 60793-2: 1992, type A1b with the exceptions noted in 15.3.1.1 to 15.3.1.4. For links under 5 m in length it may be necessary to use techniques such as attenuators or mode-stripping filters to attenuate optical power coupled into the cladding in order to meet the requirements of 15.2.2.1. The system can operate, subject to certain restrictions, with a variety of optical fibers. Information on other fiber sizes is contained in D.4. However, conformance to this standard and interoperability between different vendors' equipment is assured only through the use of the optical fiber specified in this subclause.

15.3.1.1 Attenuation

This standard was developed on the basis of an attenuation value of less than or equal to 3.75 dB/km, when measured at a wavelength of 850 nm. Higher loss fiber may be used for shorter fiber pair lengths as long as the requirements in 15.3.3 are met.

NOTE—This value of attenuation is a relaxation of the standard (IEC 60793-2: 1992, type A1b, category ≤3.5 dB/km), and is the same as ANSI/TIA/EIA-568-A-1995 [B16].

15.3.1.2 Modal bandwidth

Each optical fiber shall have a modal bandwidth-length product of not less than 160 MHz-km at a wavelength of 850 nm.

NOTE—This value of modal bandwidth is a relaxation of the standard IEC 60793-2: 1992, type A1b, category >200 MHz-km) and is the same as ANSI/TIA/EIA-568-A-1995 [B16].

15.3.1.3 Chromatic dispersion

Each optical fiber shall have a dispersion characteristic in the range shown in the following table:

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Zero dispersion wavelength λ (0); nm	Maximum dispersion slope S_0; ps/nm^2–km
1320–1348	0.11
1348–1365	[1458–λ(0)]/1000
NOTE—This characteristic is an addition to the values specified by IEC 60793-2: 1992, Type A1b, and is the same as ANSI/TIA/EIA-568-A-1995 [B16].	

15.3.1.4 Propagation delay

The propagation delay shall be ≤5 μs/km. (This is equivalent to a velocity of propagation of 0.67c.)

15.3.2 Optical medium connector plug and socket

Each end of the fiber optic cable that is to be connected to a 10BASE-FP, 10BASE-FB, or 10BASE-FL MAU or a 10BASE-FP Star shall be terminated in the BFOC/2.5 connector plug shown in Figure 15–6 (for informational use only) (one per fiber), as specified in IEC 60874-10: 1992. The corresponding mating connector sockets shown in Figure 15–7 (for informational use only) shall be used on all network elements covered by this specification (10BASE-FP MAU, 10BASE-FB MAU, 10BASE-FL MAU, and 10BASE-FP Star) to which the fiber optic cable attaches. In-line or patch panel connectors may be of other types, but must meet the requirements of 15.3.2.1 and 15.3.2.2.

NOTE—It is good practice to cap unused connectors to protect the system from ambient light and the connector interface from contamination.

15.3.2.1 Optical connector insertion loss

This standard was developed on the basis of a maximum insertion loss of 1.0 dB (see note below). Connectors with different loss characteristics may be used as long as the requirements in 15.3.2.2 and either 15.3.3.1 or 15.3.3.2 are met. Use of connectors with greater than 1.0 dB insertion loss is likely to reduce achievable transmission distances below those mentioned in 15.1.3.4.

NOTE—Per test method ANSI/EIA/TIA 455-34-1985 [B3], Method A, or ANSI/EIA/TIA 455-59-1989 [B6]. (No ISO/IEC test method was available at the time this standard was developed.)

15.3.2.2 Optical connector return loss

The return loss of optical connectors for 10BASE-FP segments shall be greater than 25 dB.

NOTE—The number of intermediate connectors in a fiber pair may have system implications because of return loss considerations (see B.5.2).

15.3.3 Fiber optic medium insertion loss

The optical insertion loss may be allocated between the elements of the fiber optic cable plant in any manner as long as the requirements of 15.3.3.1 and 15.3.3.2 are met. The optical insertion loss shall be measured in accordance with ANSI/EIA/TIA 526-14-1990 [B10], Method A, Two Reference Jumpers.

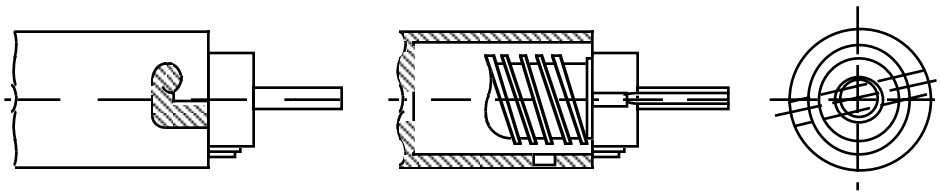
NOTE—No ISO/IEC test method was available at the time this standard was developed.

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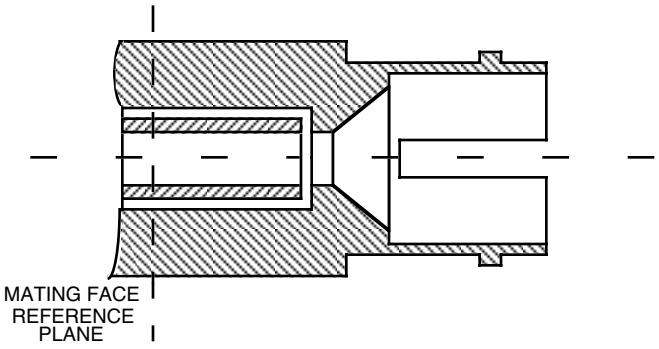
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(informative only)

Figure 15–6—BFOC/2.5 connector plug



(informative only)

Figure 15–7—BFOC/2.5 connector socket

15.3.3.1 10BASE-FP segment insertion loss

The optical insertion loss of the 10BASE-FP segment including 10BASE-FP Star shall be between 16 dB and 26 B, measured using an optical signal source with a center wavelength of 850 nm and spectral width of 75 nm. The range of measured insertion losses across the 10BASE-FP segment shall be less than 6 dB for any given star output port with respect to all input ports (see note in 16.5.2.2). See B.5.2 for examples of system implementation.

15.3.3.2 10BASE-FB and 10BASE-FL segment insertion loss

The optical insertion loss of the 10BASE-FB and 10BASE-FL segment shall be less than 12.5 dB, measured using an optical signal source with a center wavelength of 850 nm and spectral width of 75 nm.

15.3.4 Electrical isolation

Electrical isolation shall be provided between MDIs attached to the fiber optic cable. There shall be no conducting path between the optical medium connector plug and any conducting element within the fiber optic cable. This isolation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in 5.3.2 of IEC 60950: 1991.
b) 2250 Vdc for 60 s, applied as specified in 5.3.2 of IEC 60950: 1991.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μm (1.2 μm virtual front time, 50 μm virtual time of half value) as defined in IEC 60060.

There shall be no isolation breakdown, as defined in 5.3.2 of IEC 60950: 1991, during the test. The resistance after the test shall be at least 2 MΩ measured at 500 Vdc.

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15.4 MAU reliability

The MAU shall be designed to have a Mean Time Before Failure (MTBF) of at least 10 million hours of continuous operation without causing communication failure among other stations attached to the network. Component failures within the MAU electronics should not prevent communication among other MAUs on the network.

15.5 MAU–AUI specification

When a MAU contains a physical AUI connector, the following specifications shall be met.

15.5.1 MAU–AUI electrical characteristics

The electrical characteristics for the driver and receiver components within the MAU that are connected to the AUI shall be identical to those specified in 7.4 and 7.5. Additionally, the AUI DO receiver shall reject an input waveform of less than ± 160 mV differential.

15.5.2 MAU–AUI mechanical connections

The MAU shall be provided with a 15-pin male connector as specified in 7.6.

15.5.3 Power consumption

Following power on, the surge current drawn by the MAU through the AUI shall be such that $I_p \times T_w$ is less than or equal to 2×10^{-3} Ampere-seconds, where I_p is the peak surge current and T_w is the time during which the current exceeds the larger of 0.5 A or $0.5 \times I_p$. After 100 ms following power on, the current drawn by the MAU shall not exceed 0.5 A when powered by the AUI.

The MAU shall be capable of operating from all possible AUI voltage sources, including those current-limited to 0.5 A, as supplied by the DTE or repeater through the resistance of all permissible AUI cables.

It is permissible, as an option, to provide a separate power source for the MAU. If a separate power source is implemented, provision shall be made to assure that under no circumstances power can be sourced on pin 13 (Circuit VP) of the AUI. The separate power source if implemented shall withstand at least one of the tests of 15.3.4.

The MAU shall be labeled externally to identify the maximum value of power supply current required by the device when the AUI is implemented.

The MAU shall not introduce at the MDI or onto the DI or CI circuits of the AUI any extraneous signals on power-up or power-down.

15.5.4 MAU–AUI messages

The messages between the PLS in the DTE and the PMA in the MAU shall comply with 7.2.1. These messages also are used in repeater unit to PMA communications.

15.5.4.1 PLS to PMA messages

The following messages are sent by the PLS in the DTE or repeater to the PMA in the MAU (see 7.2.1.1):

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Message	Circuit*	Signal	Meaning
output	DO	CD1, CD0	Output information
output_idle	DO	IDL	No data to be output
* Or virtual equivalent for an embedded MAU.			

15.5.4.2 PMA to PLS messages

The following messages are sent by the PMA in the MAU to the PLS in the DTE or repeater (see 7.2.1.2):

Message	Circuit*	Signal	Meaning
input	DI	CD1, CD0	Input information
input_idle	DI	IDL	No input information
signal_quality_error	CI	CS0	Collision or error detected by MAU
mau_available	CI	IDL	MAU is available for output
* Or virtual equivalent for an embedded MAU.			

15.5.4.2.1 *signal_quality_error* message

The *signal_quality_error* (SQE) message shall operate in the following fashion:

a) The SQE message shall be sent whenever a collision exists, as described in 16.3.4, 17.3.3 or 18.3.1.4.
b) The SQE message shall be sent whenever a jabber condition exists, as described in 16.3.6 or 18.3.1.6.
c) The SQE message shall be sent as a result of SQE Test, as described in 16.3.5 or 18.3.1.5. SQE Test shall not be performed by MAUs connected to repeaters.
d) Under all other conditions, the MAU shall send the *mau_available* message.

The MAU is required to assert the SQE message at the appropriate times, as described in a) through c) above, whenever the MAU is powered.

15.6 Environmental specifications

15.6.1 Safety requirements

An application of the equipment specified herein is for interconnecting equipment in different buildings. This may present hazards beyond the range of protection assured by 15.3.4. Installation practice shall be consistent with this application and provide adequate personnel and equipment safety from earth faults and lightning strike hazards.

Installation practice shall be in accordance with local and national regulations.

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NOTE—While optical fibers are nonconducting, some fiber optic cables do contain metallic strength members or sheathing that must be considered during installation. However, since grounding of these metallic members does not involve the signal path, it is beyond the scope of this standard.

15.6.2 Electromagnetic environment

Sources of interference from the environment include electromagnetic fields, electrostatic discharge, and transient voltages between earth connections. The MAUs shall meet their specifications when operating in an ambient plane wave field of 2 V/m from 10 kHz through 30 MHz, and 5 V/m from 30 MHz through 1 GHz.

NOTE—These are levels typically found 1 km from radio broadcast stations.

The MAUs, stars, and associated connector/cable systems shall comply with applicable local and national codes, such as FCC Docket 20780-1980 [B23] in the USA. Equipment shall comply with local and national requirements for limitation of electromagnetic interference and susceptibility. Where no local or national requirements exist, equipment shall comply with CISPR 22: 1993.

15.6.3 Other environmental requirements

The MAUs, stars, and associated connector/cable systems are expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling such as shock and vibration. Specific requirements and values for these parameters are considered to be beyond the scope of this standard. Manufacturers should indicate in the literature associated with a unit (and on the unit if possible) the operating environment specifications to facilitate selection, installation, and maintenance of these components. It is further recommended that such specifications be stated in standard terms, as specified in IEC 60068, IEC 60874-10: 1992, IEC 60793-1: 1992, and IEC 60794-1: 1993.

15.7 MAU labeling

It is recommended that each MAU (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Whether 10BASE-FP MAU, 10BASE-FB MAU, or 10BASE-FL MAU
b) Data rate capability in Mb/s
c) Power level in terms of maximum current drain (for external MAUs as required by 15.5.3)
d) Any applicable safety warnings
e) Which connector is input and which is output
f) For 10BASE-FP MAUs, the Manufacturer ID and the MAU ID in two separate fields (see 16.3.1.1.3)
g) For 10BASE-FL MAUs, if capable of full duplex operation

15.7.1 10BASE-FP star labeling

It is recommended that each 10BASE-FP Star (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Label as 10BASE-FP Star
b) Label input/output connectors

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15.8 Protocol implementation conformance statement (PICS) proforma for Clause 15, Fiber optic medium and common elements of medium attachment units and star, type 10BASE-F[26]

15.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 15, Fiber optic medium and common elements of medium attachment units and star, type 10BASE-F, shall complete the following PICS proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. The PICS can be used for a variety of purposes by various parties, including the following:

— As a checklist by the protocol implementor, to reduce the risk of failure to conform to the standard through oversight;
— As a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard PICS proforma, by the supplier and acquirer, or potential acquirer, of the implementation;
— As a basis for initially checking the possibility of interworking with another implementation by the user, or potential user, of the implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible PICs);
— As the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation, by a protocol tester.

15.8.2 Abbreviations and special symbols

15.8.2.1 Status symbols

The following symbols are used in the PICS proforma:

M is mandatory field/function
O is optional field/function
O.<n> is optional field/function, but at least one of the group of options labeled by the same numeral <n> is required
O/<n> is optional field/function, but one and only one of the group of options labeled by the same numeral <n> is required
X is prohibited field/function
<item> is simple-predicate condition, dependent on the support marked for <item>

15.8.2.2 Abbreviations

N/A Not applicable

15.8.3 Instructions for completing the pics proforma

15.8.3.1 General structure of the PICS proforma

The first part of the PICS proforma, Implementation Identification and Protocol Summary, is to be completed as indicated with the information necessary to identify fully both the supplier and the implementation.

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The main part of the PICS proforma is a fixed-format questionnaire divided into subsubclauses, each containing a group of items. Answers to the questionnaire items are to be provided in the right-most column, either by simply marking an answer to indicate a restricted choice (usually Yes, No, or Not Applicable), or by entering a value or a set or range of values. (Note that there are some items where two or more choices from a set of possible answers can apply; all relevant choices are to be marked.)

Each item is identified by an item reference in the first column; the second column contains the question to be answered; the third column contains the reference or references to the material that specifies the item in the main body of the standard; the fourth column contains values and/or comments pertaining to the question to be answered. The remaining columns record the status of the item—whether the support is mandatory, optional, or conditional—and provide the space for the answers; see also 15.8.3.4.

The supplier may also provide, or be required to provide, further information, categorized as either Additional Information or Exception Information. When present, each kind of further information is to be provided in a further subsubclause of items labeled A<i> or X<i>, respectively, for cross-referencing purposes, where <i> is any unambiguous identification for the item (e.g., simply a numeral); there are no other restrictions on its format or presentation.

A completed PICS proforma, including any Additional Information and Exception Information, is the Protocol Implementation Conformance Statement for the implementation in question.

Note that where an implementation is capable of being configured in more than one way, according to the items listed under 15.8.5, Major Capabilities/Options, a single PICS may be able to describe all such configurations. However, the supplier has the choice of providing more than one PICS, each covering some subset of the implementation's configuration capabilities, if that would make presentation of the information easier and clearer.

15.8.3.2 Additional information

Items of Additional Information allow a supplier to provide further information intended to assist the interpretation of the PICS. It is not intended or expected that a large quantity will be supplied, and the PICS can be considered complete without any such information. Examples might be an outline of the ways in which a (single) implementation can be set up to operate in a variety of environments and configurations; or a brief rationale, based perhaps upon specific application needs, for the exclusion of features which, although optional, are nonetheless commonly present in implementations of the 10BASE-F protocol.

References to items of Additional Information may be entered next to any answer in the questionnaire, and may be included in items of Exception Information.

15.8.3.3 Exception information

It may occasionally happen that a supplier will wish to answer an item with mandatory or prohibited status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No preprinted answer will be found in the Support column for this; instead, the supplier is required to write into the Support column an X<i> reference to an item of Exception Information, and to provide the appropriate rationale in the Exception item itself.

An implementation for which an Exception item is required in this way does not conform to this standard.

Note that a possible reason for the situation described above is that a defect in the standard has been reported, a correction for which is expected to change the requirement not met by the implementation.

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15.8.3.4 Conditional items

The PICS proforma contains a number of conditional items. These are items for which both the applicability of the item itself, and its status if it does apply—mandatory, optional, or prohibited—are dependent upon whether or not certain other items are supported.

Individual conditional items are indicated by a conditional symbol of the form "<item>:<s>" in the Status column, where "<item>" is an item reference that appears in the first column of the table for some other item, and "<s>" is a status symbol, M, O, or X.

If the item referred to by the conditional symbol is marked as supported, the conditional item is applicable, and its status is given by "<s>"; the support column is to be completed in the usual way. Otherwise, the conditional item is not relevant and the Not Applicable (N/A) answer is to be marked.

Each item whose reference is used in a conditional symbol is indicated by an asterisk in the Item column.

15.8.4 Identification

15.8.4.1 Implementation identification

Supplier	
Contact point for queries about the PICS	
Implementation name(s) and version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

15.8.4.2 Protocol summary

Identification of protocol specification	IEEE Std 802.3-2002, Clause 15, 10 Mb/s Fiber Optic Medium Attachment Unit (MAU) and Medium Specification, type 10BASE-F
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exception items been required?No [ ]Yes [ ] (See 15.8.3.3; The answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of statement	

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15.8.5 Major capabilities/options

Item	Feature	Reference	Value/comment	Status	Support
*FP	10BASE-FP Implementation	15.1.1	N/A	0.1	Yes[ ] No [ ]
*FB	10BASE-FB Implementation	15.1.1	N/A	0.1	Yes[ ] No [ ]
*FL	10BASE-FL Implementation	15.1.1	N/A	0.1	Yes[ ] No [ ]

In addition, the following predicate name is defined for use when different implementations from the set above have common parameters:

*FA: FB or FL

15.8.6 PICS Proforma for the fiber optic medium

15.8.6.1 Characteristics of the fiber optic medium

Item	Feature	Reference	Value/Comment	Status	Support
*M1	Fiber size	15.3.1	62.5/125 μm	O	Yes [ ]No [ ]
M2	Attenuation of fiber	15.3.1.1	≤ 3.75 dB/km at 850 nm when 62.5/125 μm fiber is used	M1: M	N/A [ ]M: Yes [ ]
M3	Fiber modal bandwidth	15.3.1.2	≥160 MHz–km at 850 nm	M	Yes [ ]
M4	Fiber dispersion slope For fiber with a zero dispersion wavelength in the range 1320 nm to 1348 nm	15.3.1.3	0.11 ps/nm^2–km	O/2	Yes [ ]No [ ]
M5	For fiber with a zero dispersion wavelength in the range 1348 nm to 1365 nm		[1458-l(0)]/1000 ps/nm^2–km	O/2	Yes [ ]No [ ]
M6	Velocity of propagation	15.3.1.4	≤ 5 μs/km	M	Yes [ ]

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15.8.6.2 Optical medium connector plug and socket

Item	Feature	Subclause	Value/comment	Status	Support
MC1	Connector plug for termination of fiber	15.3.2	BFOC/2.5—see IEC 60874-10: 1992	M	Yes [ ]
MC2	Optical connector loss	15.3.2.1	< 1.0 dB	O	Yes [ ]No [ ]
MC3	Optical connector return loss (10BASE-FP only)	15.3.2.2	> 25 dB	FP: M	N/A [ ]M: Yes [ ]

15.8.6.3 Fiber optic medium insertion loss

Item	Feature	Subclause	Value/comment	Status	Support
	Fiber optic medium insertion loss		Measured as per ANSI/EIA/TIA 526-14-1990 [B10], Method A, using optical signal with center wavelength of 850 nm and spectral width of 75 nm		
IL1	10BASE-FP segment insertion loss (including 10BASE-FP Star)	15.3.3.1	Between 16 dB and 26 dB	FP: M	N/A [ ] M: Yes [ ]
IL2	10BASE-FB and 10BASE-FL segment insertion loss	15.3.3.2	< 12.5 dB	FA: M	N/A [ ] M: Yes [ ]
IL3	Range of insertion losses measured across one 10BASE-FP segment or one star output port	15.3.3.1	< 6 dB	FP: M	N/A [ ] M: Yes [ ]

15.8.6.4 Electrical isolation requirements

Item	Feature	Subclause	Value/comment	Status	Support
IR1	Electrical isolation, optical connector plug to any electrically conducting element in cable	15.3.4	Any one of three tests listed in 15.3.4	M	Yes [ ]
IR2	Resistance after breakdown test	15.3.4	> 2 MΩ measured at 500 Vdc	M	Yes [ ]

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16. Fiber optic passive star and medium attachment unit, type 10BASE-FP

NOTE—This MAU is not recommended for new installations.

16.1 Scope

16.1.1 Overview

This clause, along with Clause 15, defines the functional, electrical, optical, and mechanical characteristics of a fiber optic passive-star system for interconnecting DTEs and repeaters. The relationship of this clause to the entire ISO/IEC 8802-3 International Standard is shown in Figure 15–1a). This system, which may be interconnected to other 10 Mb/s baseband segments using repeaters, consists of the 10BASE-FP MAU (including a fiber optic MDI specified in 15.2), a 10BASE-FP fiber optic Star, and the fiber optic medium specified in 15.3. The 10BASE-FP MAU provides the means for attaching DTEs and repeaters to a 10BASE-FP Star LAN, and a 10BASE-FP Star provides the only means to interconnect 10BASE-FP MAUs via their MDIs.

16.1.1.1 10BASE-FP medium attachment unit

The 10BASE-FP MAU has the following general characteristics:

a) It supports a totally passive-star topology interconnection means.
b) It connects a DTE or repeater to a 10BASE-FP fiber optic segment.
c) It supports message traffic at a data rate of 10 Mb/s.
d) It permits up to 500 m of fiber optic cable, as specified in 15.3, between 10BASE-FP MAUs and a 10BASE-FP Star. (See B.5.2.)
e) It permits the DTE or repeater to confirm operation of the MAU and availability of the medium.
f) It permits the DTE to test the collision detection circuitry of the MAU.
g) It recodes the preamble prior to transmission at the MDI to allow passive-system collision detection and restores normal preamble to packets received at the MDI.
h) It transmits coded jam during collision for deterministic detection of end of collision.
i) It supports network configurations using the CSMA/CD access mechanism defined in this standard.

16.1.1.2 10BASE-FP Star

The star has the following general characteristics:

a) It supports a totally passive-star topology interconnection means.
b) It receives an optical signal from any 10BASE-FP MAU connected to the passive fiber optic segment and distributes the signal uniformly to all 10BASE-FP MAUs connected to the passive fiber optic segment, including the one from which the transmission originated.
c) It supports message traffic at a data rate of 10 Mb/s.
d) It permits segments of up to 500 m radius of fiber optic cable, as specified in 15.3, among MAUs and the star. (See B.5.2.)
e) It supports system configurations using the CSMA/CD access mechanism defined in this standard.

16.1.1.3 Repeater unit

The repeater unit (Clause 9), along with 10BASE-FP MAUs (making a repeater set), is used to interconnect 10BASE-FP segments to achieve the maximum 10BASE-FP connection path. The repeater is also used to extend the physical system topology by connecting 10BASE-FP segments to 10BASE-FB and 10BASE-FL segments as well as all other 10 Mb/s baseband media types.

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Multiple repeater units are permitted within a single collision domain to provide the maximum connection path length specified in Clause 13. The repeater is not a DTE and therefore has slightly different requirements for its attached MAUs as defined in 9.4.1. It is recommended that repeater sets with 10BASE-FP MAUs provide the auto partition/reconnection algorithm on those ports as specified in 9.6.6.2.

16.2 PMA interface messages

The messages between PLS in the DTE or the repeater and the PMA in the MAU shall comply with the PMA interface messages in 7.2.1 and 15.5.4. The messages between the PMAs over the MDI are summarized below.

16.2.1 PMA-to-MDI interface signal encodings

The following signals are used by the interface messages between the PMA and the MDI.

Code Rule Violation, CRV. See 15.1.2.

Manchester-Coded Data One, CD1. A clocked bit symbol in which the first half is LO and the second half is HI.

Manchester-Coded Data Zero, CD0. A clocked bit symbol in which the first half is HI and the second half is LO.

Manchester Code Violation Zero, MV0. A clocked bit symbol in which the symbol is LO for the bit duration.

Received Idle, RDARK. See 15.2.1.4 and 16.2.3.2.

Transmitted Idle, TDARK. See 15.2.1.4 and 16.2.2.2.

16.2.2 PMA-to-MDI OTD messages

The following messages can be sent by the MAU PMA to the MDI OTD (Optical Transmit Data) circuit:

Message	Circuit	Signal	Meaning
OTD_output	OTD	CD1, CD0	Output information
OTD_idle	OTD	TDARK	No data to be output
OTD_manch_violation	OTD	MV0	Manchester violation to be output

16.2.2.1 OTD_output

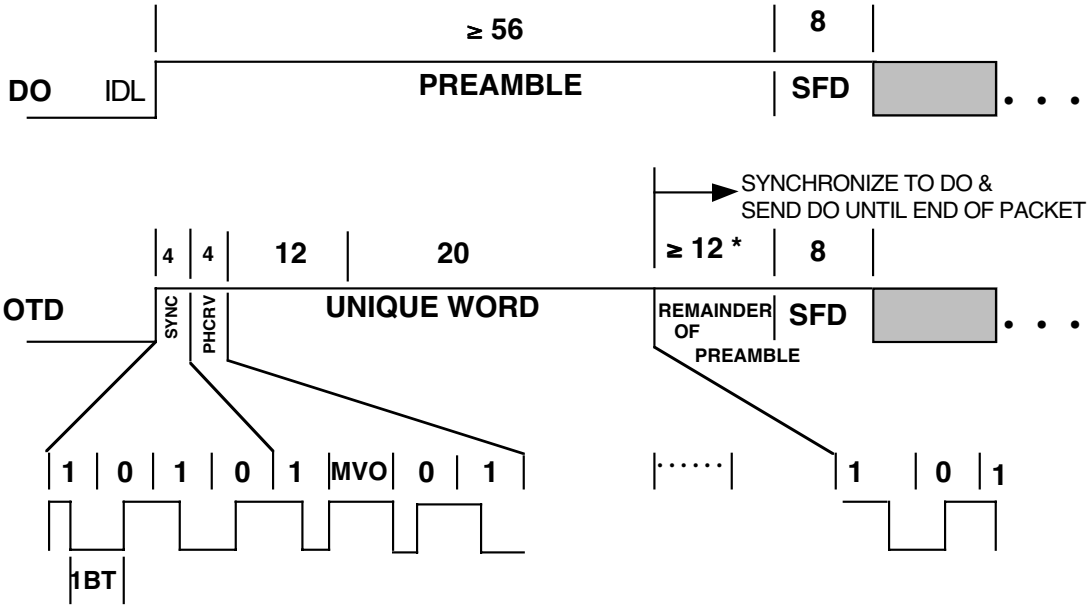
The PMA sublayer shall send the *OTD_output* message to the OTD circuit when the DTE or repeater outputs a bit of data, as modified by the Preamble Encoding function (see 16.3.1.1 and Figure 16–1), and neither link fault nor jabber has been detected. The physical realization of the *OTD_output* message shall be a CD0 or CD1 signal sent by the PMA.

16.2.2.2 *OTD_idle*

The PMA sublayer shall send the *OTD_idle* message to the OTD circuit when the DTE or repeater sends idle or if either link fault or jabber has been detected. The physical realization of the *OTD_idle* message shall be a TDARK signal sent by the PMA. TDARK shall be a signal with an optical level as specified in 15.2.1.4, Optical Idle Signal Amplitude, and shall have a duration of 1.5 Bit Times (BT) or greater.

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* This is always an even number and is the number of preamble bits received on DO minus 40 to 42.

NOTE—This OTD waveform shows no light as the baseline and light as the high level.

Figure 16–1—10BASE-FP MAU preamble encoding

16.2.2.3 *OTD_manch_violation*

The PMA shall send the *OTD_manch_violation* message whenever the Preamble Encoding function (16.3.1.1) or the Collision Encoding function (16.3.1.3) requires it to do so. The physical realization of the *OTD_manch_violation* message shall be an MV0 signal sent by the PMA.

16.2.3 MDI ORD-to-PMA messages

The following messages can be received by the MAU PMA from the MDI ORD (Optical Receive Data) circuit:

Message	Circuit	Signal	Meaning
ORD_input	ORD	CD1, CD0	Input information
ORD_idle	ORD	RDARK	No information to input
ORD_crv	ORD	CRV	Detected Manchester violation

16.2.3.1 *ORD_input*

When the PMA sublayer receives the *ORD_input* message on its ORD circuit, it detects a bit of data. The physical realization of the *ORD_input* message shall be a CD0 or CD1 signal.

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16.2.3.2 *ORD_idle*

When the PMA sublayer receives the *ORD_idle* message on its ORD circuit, it detects idle. The physical realization of the *ORD_idle* message shall be an RDARK signal. RDARK shall be a signal with an optical level as specified in 15.2.1.4, Idle Signal Amplitude, and shall have a duration of 1.25 BT or greater.

16.2.3.3 *ORD_crv*

When the PMA sublayer receives the *ORD_crv* message on its ORD circuit, it detects a code rule violation. The physical realization of the *ORD_crv* message shall be a CRV signal. CRV is defined in 15.1.2.

16.3 10BASE-FP MAU functional specifications

The MAU component provides the means by which signals on the DO and DI circuits are coupled:

a) From the DTE or repeater to the MAU's transmit MDI, and
b) From the MAU's receive MDI to the DTE or repeater.

Further, simultaneous transmissions from two or more MAUs are reported as a collision on the CI circuit.

To achieve this basic objective, the MAU component shall contain the following functional capabilities to handle message flow between the DTE or repeater and the MDI:

— Transmit function: Provides the ability to transmit serial data bit streams from the attached device into the MAU's transmit MDI.
— Receive function: Provides the ability to receive serial data bit streams from the MAU's receive MDI and transmit them to the attached device.
— Loopback function: Provides the ability to transfer serial data bit streams from the DO to the DI circuit when the MAU is sending data to the OTD circuit.
— Collision Presence function: Provides the ability to detect, and report to the attached device, a collision.
— *signal_quality_error* Message (SQE) Test function: Provides the ability to indicate to the DTE that the Collision Presence function is operational and that the *signal_quality_error* message can be sent by the MAU.
— Jabber function: Provides the ability to detect abnormally long data streams on the DO circuit and inhibit Data Transmit and Receive, SQE Test, Data Loopback, and the Collision Presence function.
— Link Fault Detection and Low Light function: Provides the ability to detect faults in the 10BASE-FP fiber optic segment and inhibit Data Transmit and Receive, SQE Test, Data Loopback, and the Collision Presence function.

16.3.1 Transmit function requirements

The function of the MAU transmitter shall be to transmit the data received at the DO circuit of the AUI onto the MDI. The Transmit function has four purposes:

a) To convert the electrical signals to optical signals.
b) To recode the preamble to guarantee collision detection.
c) To generate a unique jam signal to facilitate deterministic end of collision detection.
d) To retime signals received on the DO circuit.

The levels and timing of the optical signal shall be as specified in 15.2.1. When a packet is received at the DO interface, transmission of encoded preamble at the MDI shall begin within 5.5 BT. The first bit transmit-

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ted onto the fiber from the MDI shall be a CD1 (see 16.3.1.1.1). The signaling rate at the MDI shall be 10 Mb/s ± 0.005%.

NOTE—The tolerance of ±0.005% simplifies the detection of data and collision in the MAU receiver. It may not be necessary to retime signals in an embedded MAU.

16.3.1.1 Preamble encoding

The Transmit function shall replace the first 40 bits of preamble with a pattern consisting of a 4-bit synchronization pattern, a 4-bit packet header Manchester-coding violation pattern (see 16.3.1.1.2), and a 32-bit unique word (see 16.3.1.1.3) as shown in Figure 16–1. Following the unique word, the remainder of the preamble received on the DO shall be transmitted as received subject to the following rules:

a) The encoded preamble shall be aligned with the preamble received from the DO circuit in such a way that the first bit of the remainder is a Manchester-encoded 1; i.e., the remainder of the preamble is CD1, CD0, CD1, CD0,….
b) The number of bits of preamble received from the DO circuit and sent to the MDI prior to the transmission of SFD shall be no less than the total number received from the DO circuit minus 42 bits and no greater than the total number received from the DO circuit minus 40 bits. The above ensures that the preamble transmitted on the OTD circuit is no more than 2 bits shorter than the preamble received from the DO circuit.

The purpose of preamble encoding is to provide synchronization and collision detection information to the Receive function. This unique encoding exists only on the medium and is removed by the receiving MAU.

16.3.1.1.1 Synchronization pattern

The synchronization pattern shall be a Manchester-encoded 1010 (SYNC=CD1 CD0 CD1 CD0). No other pattern, including 0101, is allowed.

16.3.1.1.2 Packet header code rule violation

The packet header code rule violation pattern shall be a fixed, 4-bit pattern that contains a single violation of the Manchester coding rules. The pattern consists of a CD1, MV0, CD0, CD1. The single Manchester violation in the pattern is the only violation allowed in a properly transmitted packet.

16.3.1.1.3 Unique word

The unique word shall be a 32-bit long Manchester-encoded data pattern that is used to guarantee that the preambles sent by any two 10BASE-FP MAUs are different. The word consists of a 12-bit Manufacturer ID assigned by a Registration Authority and a 20-bit 10BASE-FP MAU ID assigned by the manufacturer to ensure that the 32-bit word is unique. The nature of the Registration Authority[27] and the procedure by which it administers these 12-bit manufacturer identifiers is beyond the scope of this standard. Each of the elements of the unique word shall be transmitted least significant bit first, starting with the Manufacturer ID followed by the MAU ID.

16.3.1.2 Data transmit

The Data Transmit function shall receive the data signals on the DO circuit and send them on the MDI following the encoded preamble.

[27]For the purpose of assigning organizationally unique identifiers (OUIs), the Institute of Electrical and Electronics Engineers has been designated by the ISO Council as the Registration Authority. Communications on this subject should be addressed to the Registration Authority for ISO/IEC 8802-3, The Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331 USA, tel. (732) 562-3813; fax (732) 562-1571.URL:http://standards.ieee.org/.

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The steady-state delay between the DO circuit and transmission on the MDI at the time of the start bit in the SFD, shall be no more than 3.5 BT. The difference between start-of-packet propagation delay for any two packets that are separated by 9.6 μs or less shall not exceed 3 BT.

16.3.1.3 Collision encoding (unique word jam)

After the start of collision (see 16.3.4.2), the Transmit function shall, within 3.5 BT, cease to send the encoded preamble or data from the DO circuit and shall send a repeating, unique, 33-bit pattern. This pattern shall consist of MV0 followed by the 32-bit unique word. In the presence of a collision, a MAU will detect at least two *ORD_crv* within 33 BT and can thereby guarantee accurate detection of end of collision. This pattern shall be repeatedly transmitted at the MDI OTD until the MAU ceases to receive data on the DO circuit. When this occurs, the MAU shall begin sending *OTD_idle* at the MDI within 3.5 BT of the last bit on the DO circuit.

16.3.2 Receive function requirements

The function of the MAU Receive function is to transmit the data received on the MDI ORD circuit into the DI circuit. The Receive function has three purposes:

a) To convert optical signals to electrical signals.
b) To replace the coded preamble with normal preamble as specified in 4.2.5.
c) To provide uninterrupted carrier sense during collision presence.

The optical-to-electrical conversion shall be as specified in 15.2.2.3.

16.3.2.1 Preamble reconstruction and alignment

When a packet is received on the MDI ORD circuit, transmission of the reconstructed preamble to the DI circuit shall begin within 2.5 BT. The difference between start-of-packet propagation delay for any two packets that are separated by 9.6 μs or less shall not exceed 1 BT.

The reconstructed preamble shall consist of exactly 40 bits of standard preamble (CD1, CD0, CD1,…CD0) followed by the preamble remainder received on the ORD circuit. The Receive function shall align the preamble remainder such that the 41st bit transmitted on the DI circuit is a Manchester-encoded 1 (CD1).

16.3.2.2 Data receive

The Data Receive function shall receive data signals on the MDI ORD circuit and send them into the DI circuit following the reconstructed preamble.

At the start of SFD reception at the MDI ORD circuit, the steady-state delay between the MDI ORD circuit and the DI circuit shall not exceed 2.5 BT.

16.3.2.3 Signal presence during collision

When a collision is detected (see 16.3.4.2), the Receive function shall transmit Manchester Fill, a sequence of Manchester-encoded alternating CD1s and CD0s on the DI circuit. This Manchester sequence shall be sent on the DI circuit for the duration of activity on the MDI ORD circuit and shall be deasserted within 3 BT from the start of RDARK on the MDI ORD circuit. In addition, the data being sent to the DI circuit shall be monitored and altered to be a valid Manchester sequence if any sequence besides a valid Manchester sequence or RDARK is seen, in the absence of collision yet being signaled.

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16.3.3 Loopback function requirements

The MAU shall transmit the bit stream received from the DO circuit into the DI circuit. At the start-of-packet transmission, no more than 2 bits of information shall be received from the DO circuit and not transmitted into the DI circuit. It is permissible for the first bit sent to contain encoded phase violations or invalid data. All successive bits shall be transmitted into the DI circuit and shall exhibit no more edge jitter than that specified for signals transmitted into the DI circuit by the Receive function, as specified in 15.2.2.2. The steady-state propagation delay between the DO circuit receiver input and the DI circuit driver output for such signals shall not exceed 1 BT. The MAU's DI circuit driver shall comply with the specification for AUI drivers in 7.4.1. There shall be no logical signal inversions between the DO circuit and the DI circuit during collision-free transmission.

16.3.4 Collision presence function requirements

16.3.4.1 CI Circuit signaling

CI circuit signaling and timing shall meet the requirements of 7.3.1.2, as modified by 15.1.3.3, and 15.5.4.1.

16.3.4.2 Collision detection

The MAU shall detect as a collision the following two cases (see Figure 16–6)

a) DO becoming active while ORD is active, except for the instance where ORD is still active from a previous transmission's loopback from the star.
b) The detection of a second *ORD_crv* without an intervening *ORD_idle*.

The start of collision is measured from the time DO becomes active in case a) above and from the occurrence of the second *ORD_crv* for case b) above.

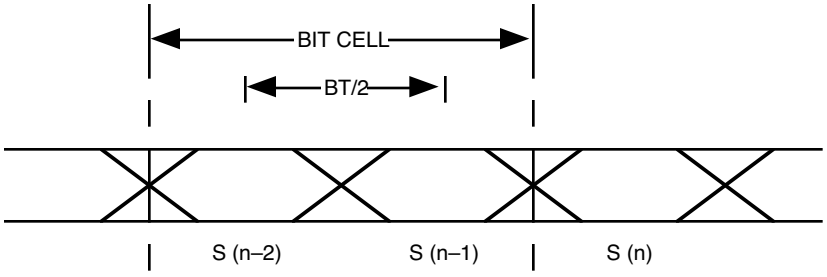
The MAU shall detect *ORD_crv*'s over the received optical power ranges specified in 15.2.2.1. In addition, *ORD_crv* detection shall occur over a differential power range of 8.0 dB.

While a collision is occurring, a CS0 (7.3.1.2) signal shall be sent on the CI circuit. The signal shall be presented to the CI circuit no more than 3.5 BT after start of collision.

If two or more packets arrive simultaneously at the MDI, then the MAU will receive the packet header *ORD_crv* and at least one additional *ORD_crv* during reception of the overlapping unique word patterns. Otherwise the MAU will receive the multiple packet header *ORD_crv*'s from the interfering packet(s).

In order to meet the performance requirements, *ORD_crv* detection needs to be performed in the analog portion of the receiver, as the amplitude information that is essential for *ORD_crv* detection is lost after converting the analog signal into a digital (binary) waveform.

One possible way to detect *ORD_crv* is to compare the amplitudes of three consecutive samples separated by one half BT. The samples are obtained by using a recovered 20 MHz receive clock as shown below.



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The differences d1 = | S(n) – S(n-1) | and d2 = | S(n) – S(n-2) | are produced. The computation must be done once per bit cell, with S(n) being the sample from the first half of the bit cell. In a valid Manchester-encoded sequence, one of these differences must be zero. Thus, if both differences are above a certain threshold, a Manchester code rule violation (*ORD_crv* message) is detected. The actual value of the threshold is implementation dependent but needs to be such that the probability of obtaining an *ORD_crv* when two or more MAUs are sending simultaneously is 100% (also see 15.2.2). Also, at least one of S(n), S(n–1), or S(n–2) must be HI.

The approach described above may not be the only approach that may meet the requirements for reliable collision detection through *ORD_crv*. The implementor may choose any approach that satisfies the requirements.

NOTE—Implementors are cautioned that optical waveforms received during collisions are the superpositions of multiple transmitted waveforms and that any receive clock synchronization may then be undefined. Under these conditions, collisions will continue to be detected and indicated correctly.

16.3.4.3 End of collision

After detection of a collision (16.3.4.2), CI shall send CS0 until (see Figures 16–2 and 16–6[28])

a) Either DO becomes inactive,
b) ORD becomes idle, or,
c) After waiting for a delay of 54 BT for the unique word jam to loop back from the star, 33 BT have passed with no more than one *ORD_crv*.

The CS0 signal shall be deasserted within 3 BT after any of the above conditions has occurred (see Figure 16–6).

The signal presented on the CI circuit in the absence of collision, SQE Test, or Jabber shall be the IDL signal.

NOTE—The Transmit function (16.3.1) encodes the signal transmitted to guarantee that
a)All transmissions received without collision contain one and only one *ORD_crv*.
b)All transmissions received with collision contain more than one *ORD_crv*.
c)During a collision, spacing between *ORD_crv* events is no more than 32 BT (UWJ has an MV0 every 33 BT).

If a collision is in progress, either the MV0s are in alignment and at least one additional *ORD_crv* will occur during (and because of) the superposition of the unique words, or the MV0s are not in alignment and will be detected in each of the UWJs as *ORD_crv*.

16.3.5 *signal_quality_error* Message (SQE) Test function requirements

The SQE Test function shall be performed by MAUs connected to DTEs and shall not be performed by MAUs connected to repeaters. A capability may be provided in the MAU to activate or inhibit the SQE Test function. It is not required that a MAU determine that it is connected to either a DTE or a repeater and automatically activate or inhibit the SQE Test function. When the SQE test is performed, the MAU shall send CS0 on the CI circuit for a time "SQE_test" beginning a time "SQE_test_wait" after the last positive transition of a packet on the DO circuit. The value of "SQE_test" shall be 10 BT + 5 BT and the value of SQE_test_wait shall be between 0.6 μs and 1.6 μs. This function should use as much of the normal collision detection and signaling circuitry as possible without introducing extraneous signals on the OTD circuit or DI circuit.

16.3.6 Jabber function requirements

The MAU shall contain a self-interrupting capability to prevent an illegally long transmission by the DTE from permanently disrupting transmission on the network (see Figure 16–5). If the transmission exceeds time "xmit_max", then Jabber shall be detected. The value of "xmit_max" shall be in the range of 20 ms to 150 ms.

[28]The MAU state diagrams, Figures 16–2 through 16–6, follow 16.3.4.3.

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Upon detection of the Jabber condition, the MAU shall perform the following:

a) Disable Data Transmit,
b) Send the CS0 signal on the CI circuit, and
c) Disable the Loopback function (16.3.1.3) from the DO circuit to the DI circuit.

The MAU shall reset the Jabber function after a continuous period of IDL on the DO circuit of time "unjab". The value of "unjab" shall be 0.5 s $\pm$ 0.25 s.

The MAU shall not activate its Jabber function when the repeater's MAU Jabber Lockup Protection function operates at its longest permitted time as specified in 9.6.5.

NOTE—It is recommended that the Jabber function be activated when the OTD circuit transmitter is sending *OTD_output* messages for longer than the value of "xmit_max_timer".

16.3.7 Link fault detection and low light function requirements

The MAU shall have the capability, as defined in Figure 16–4, to detect faults in the passive fiber optic segment that may affect the reliable carrier sense required by the CSMA/CD access method. The Link Fault Detection and Low Light function ascertains the integrity of the link, during packet transmission, by detecting the presence, at the MDI ORD circuit, of an optical signal that meets the requirements of 15.2.2.1 returned from the star. The MAU shall detect a Link Fault if, after the start of a packet onto the OTD circuit, time "link_test" elapses with no optical signal having been received on the ORD circuit. The value of "link_test" shall be 10 μs $\pm$ 2.5 μs. A Link Fault shall also be detected if the optical power of a received optical signal is not sufficient to maintain a BER of one part in 10^7.

On detection of the Link Fault condition, the MAU shall perform the following:

a) Disable its Data Transmit,
b) Disable its Data Receive, and
c) Disable the Loopback (16.3.1.3) from the DO circuit to the DI circuit.

The MAU shall reset the Link Fault function after time "link_heal", followed by the presence of an optical signal on the ORD circuit having sufficient optical power to maintain a BER of one part in 10^7, and then followed by DO circuit and ORD circuit becoming idle. The value of "link_heal" shall be 0.5 s $\pm$ 0.25 s.

The Link Fault state diagram (Figure 16–4) controls the measurement of optical loopback time. The value for link_test has been chosen to ensure that a correctly operating 10BASE-FP MAU attached to a 10BASE-FP Star via an unbroken fiber pair 500 m long will always exit the START LINK TEST state before link_test_ timer_done is asserted.

When not transmitting, and not receiving idle, if the optical power of the received optical signal is not sufficient to maintain a BER of one part in 10^7, the MAU shall set CRV to *true* and send the *ORD_crv* message.

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16.3.8 Interface message time references

Delay and bit loss specifications are measured from the occurrence of messages at the MDI and MAU AUI. A "positive-going" transition is from LO to HI. The following describes the point where each message starts:

Message	Reference
output	leading bit cell boundary (BCB) of first valid CD1 or CD0
output_idle	last positive-going transition prior to start of IDL
input	leading BCB of first valid CD1 or CD0
input_idle	last positive-going transition prior to start of IDL.
signal_quality_error	first transition of valid amplitude
mau_available	last positive-going transition prior to start of IDl
OTD_output	leading BCB of first (valid) CD1 or CD0
OTD_idle	last positive-going transition prior to start of TDARK
OTD_manch_violation	leading BCB of valid MV0
ORD_input	leading BCB of first (valid) CD1 or CD0
ORD_idle	last positive-going transition prior to start of RDARK
ORD_crv	leading BCB of a Manchester code rule violated bit

16.3.9 MAU state diagram

The state diagrams, Figures 16–2 through 16–6, depict the full set of allowed MAU state functions relative to the circuits of the AUI and MDI.

The notation used in the state diagrams follows the conventions in 1.2.1. The variables, timers, and counters used in the state diagrams are defined in the following subclauses.

16.3.9.1 MAU state diagram variables

Variables are used in the state diagrams to indicate the status of MAU inputs and outputs, to control MAU operation, and to pass state information between functions.

In the variable definitions, the name of the variable is followed by a brief description of the variable and a list of values the variable may take. For those variables that are state diagram outputs, one value will be identified as the default. The variable has the default value when no active state contains a term assigning a different value.

The variables used in the state diagrams are as follows:

begin

The interprocess flag controlling state diagram initialization values.
Values: false (default).
true.

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DI

Controls the signal sent by the MAU on the DI circuit.
Values: idle; MAU sends *input_idle*, IDL (default)
DO; MAU sends the signal received on the DO circuit.
Manchester fill; (16.3.2.3).
ORD; MAU sends the Manchester-encoded data received on the ORD circuit.
STANDARD PREAMBLE; MAU sends CD1 CD0 CD1 CD0 etc., preamble as defined in 4.2.5 and described in 16.3.2.1.

CI

Controls the signal sent by the MAU on the CI circuit.
Values: idle; MAU sends *mau_available*, IDL (default).
SQE; MAU sends *signal_quality_error*, CS0.

DO

Status of the signal received by the MAU on the DO circuit.
Values: idle; MAU receives *output_idle*, IDL.
active; MAU receives output, CD0 or CD1.

OTD

Controls the signal sent by the MAU on the OTD circuit.
Values: idle; MAU sends TDARK (default).
MP; MAU sends MODIFIED PREAMBLE (16.3.1.1).
DO; MAU sends the Manchester-encoded data received on the DO circuit.
UWJ; MAU sends UNIQUE WORD JAM (16.3.1.3).

ORD

Status of the signal received by the MAU on the ORD circuit.
Values: idle; MAU receives RDARK.
active; MAU receives CD0, CD1 or CRV.

jab

Interprocess variable that indicates whether a jabber has been detected.
Values: not_detect; jabber not detected (default).
detect; jabber detected.

link_status

Interprocess variable that indicates whether a link fault has been detected.
Values: good; no link fault detected (default).
bad; link fault detected.

col_status

Interprocess variable that indicates whether a CRV *(ORD_crv)* was received near the beginning of a received packet.
Values: good; no CRV fault detected (default).
fault; CRV fault detected.

status

Interprocess variable that indicates if a CRV fault, link fault or a jabber is detected.
Values: ok; link_status=good $*$ jab=not_detect $*$ col_status=good.
fault; link_status=bad + jab=detect + col_status=fault.

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collision

Status of the Collision Detect function.
Values: false; no collision detected (default).
true; collision detected (16.3.4.2).

E_col

Status indicating that a collision was detected in the electrical domain.
Values: false; no electrical collision detected (default).
true; electrical collision detected.

CRV

Status of the code rule violation detector.
Values: false; no code rule violation.
true; a code rule violation has occurred.

SQE_test

A capability may be provided in the MAU to activate or inhibit the SQE Test function. It is not required that a MAU determine that it is connected to either a DTE or a repeater and automatically activate or inhibit the SQE Test function.
Values: false; MAU is connected to a repeater.
true; MAU is connected to a DTE.

MPT

Status indicator for transmission of Modified Preamble.
Values: not done; Modified Preamble being transmitted.
done; transmission of Modified Preamble complete.

MPR

Status indicator for reception of Modified Preamble.
Values: not done; Modified Preamble being received.
done; reception of Modified Preamble complete.

low_light

Status indicator for low light detection.
Values: false; low_light not detected (16.3.7).
true; low_light detected (16.3.7).

16.3.9.2 MAU state diagram timers

All timers operate in the same fashion. A timer is reset and starts counting upon entering a state where “start x_timer” is asserted. At time “x” after the timer has been started, “x_timer_done” is asserted and remains asserted until the timer is reset. At all other times “x_timer_not_done” is asserted.

When entering a state where “start x_timer” is asserted, the timer is reset and restarted even if the entered state is the same as the exited state.

The timers used in the MAU state diagrams are defined as follows:

link_test_timer. The timer for longest time between start of DO and start of ORD before Link Fault state is entered (16.3.7).

link_heal_timer. The timer that defines the time delay from Link Fault detection to start of qualification procedure that resets link_fault (16.3.7 and Figure 16–4).

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SQE_test_timer. The timer for the duration of the Signal Quality Error test signal (16.3.5).

SQE_test_wait_timer. The timer for the delay from end of packet to the start of the SQE test signal (16.3.5).

xmit_max_timer. The timer for excessively long transmit time (16.3.6).

unjab_timer. The timer for the length of time the DO circuit must be continuously idle to allow transmission to be re-enabled (16.3.6).

16.3.9.3 MAU state diagram counters

All counters operate in the same fashion. A counter is reset (set to zero) upon entering a state where "start_x_cntr" is asserted. The counter then increments each time the associated event occurs until the counter reaches its maximum value.

The counters used in the MAU state diagrams are defined as follows:

CRV_cntr. Counts the number of CRVs. Used to differentiate between collision and UWJ. *Values:* Integers between and including 0 and 2.

EOC_cntr. Counts the number of BTs since last CRV. Used to identify end of collision (when EOC_cntr = 33). *Values:* Integers between and including 0 and 33.

DELAY_cntr. Counts BTs. Used to control the state transition after receiving MV0 in the preamble as a CRV. *Values:* Integers between and including 0 and 108.

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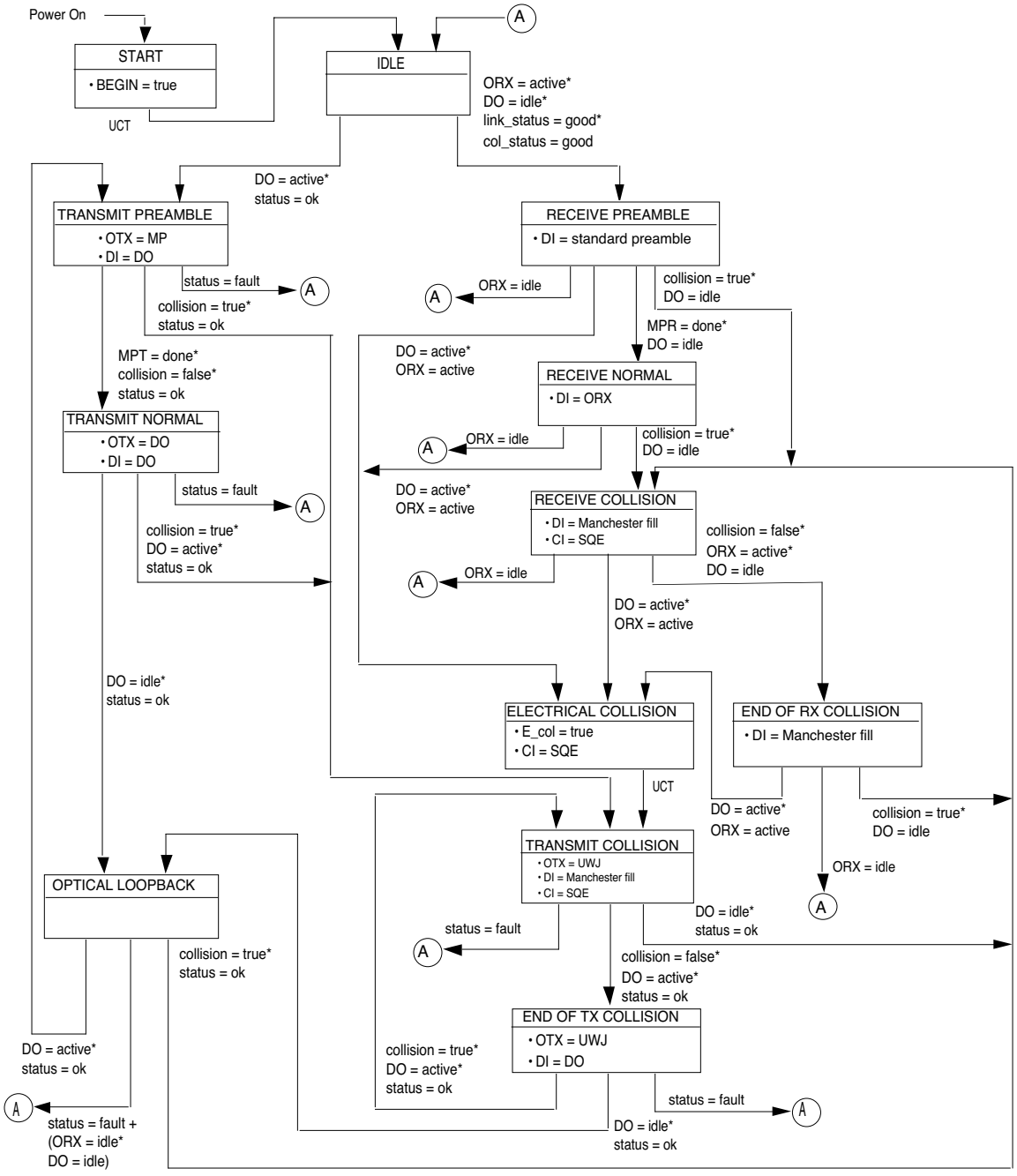


Figure 16–2—Transmit and Receive function state diagram

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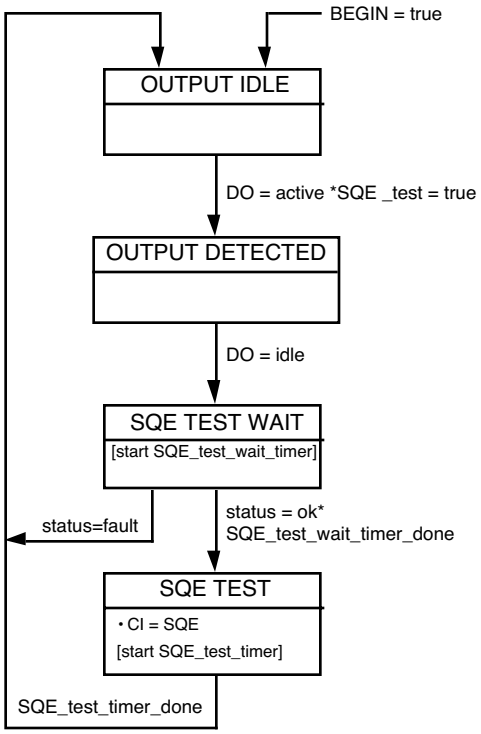


Figure 16–3—*signal_quality_error* Message Test function state diagram

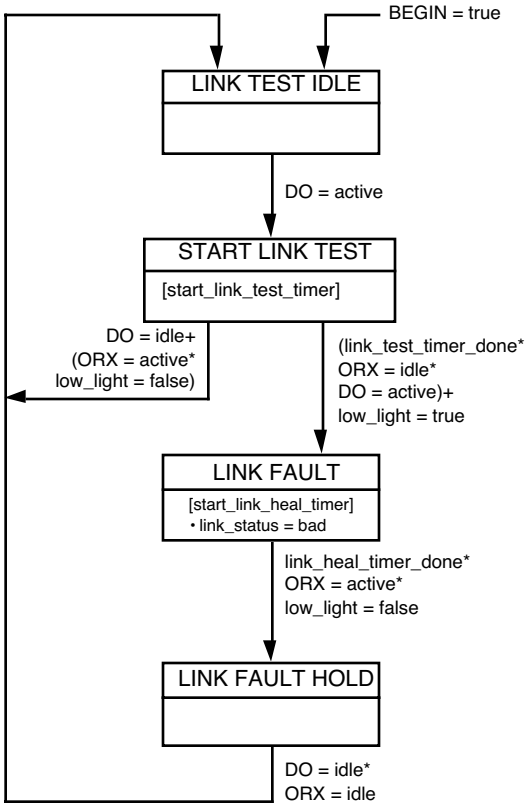


Figure 16–4—Link fault state diagram

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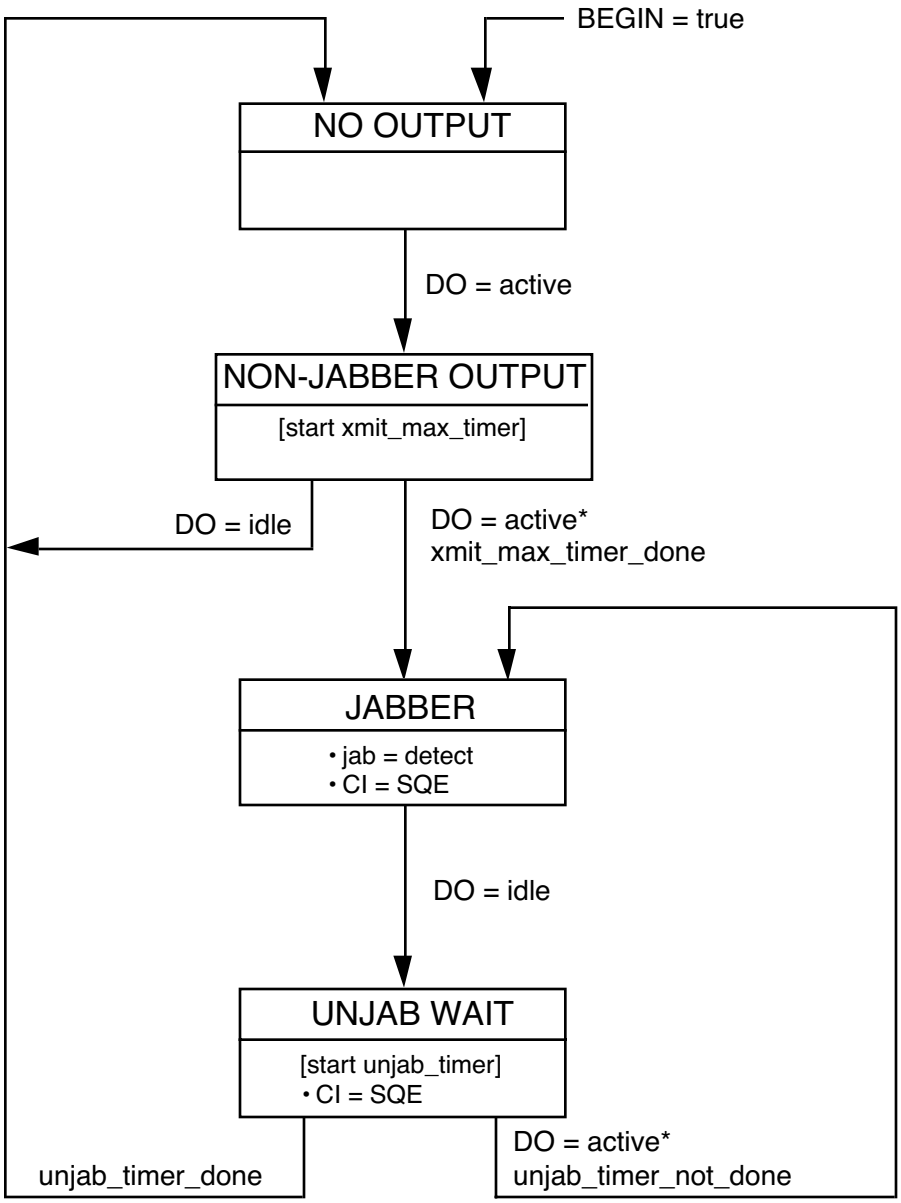


Figure 16–5—Jabber function state diagram

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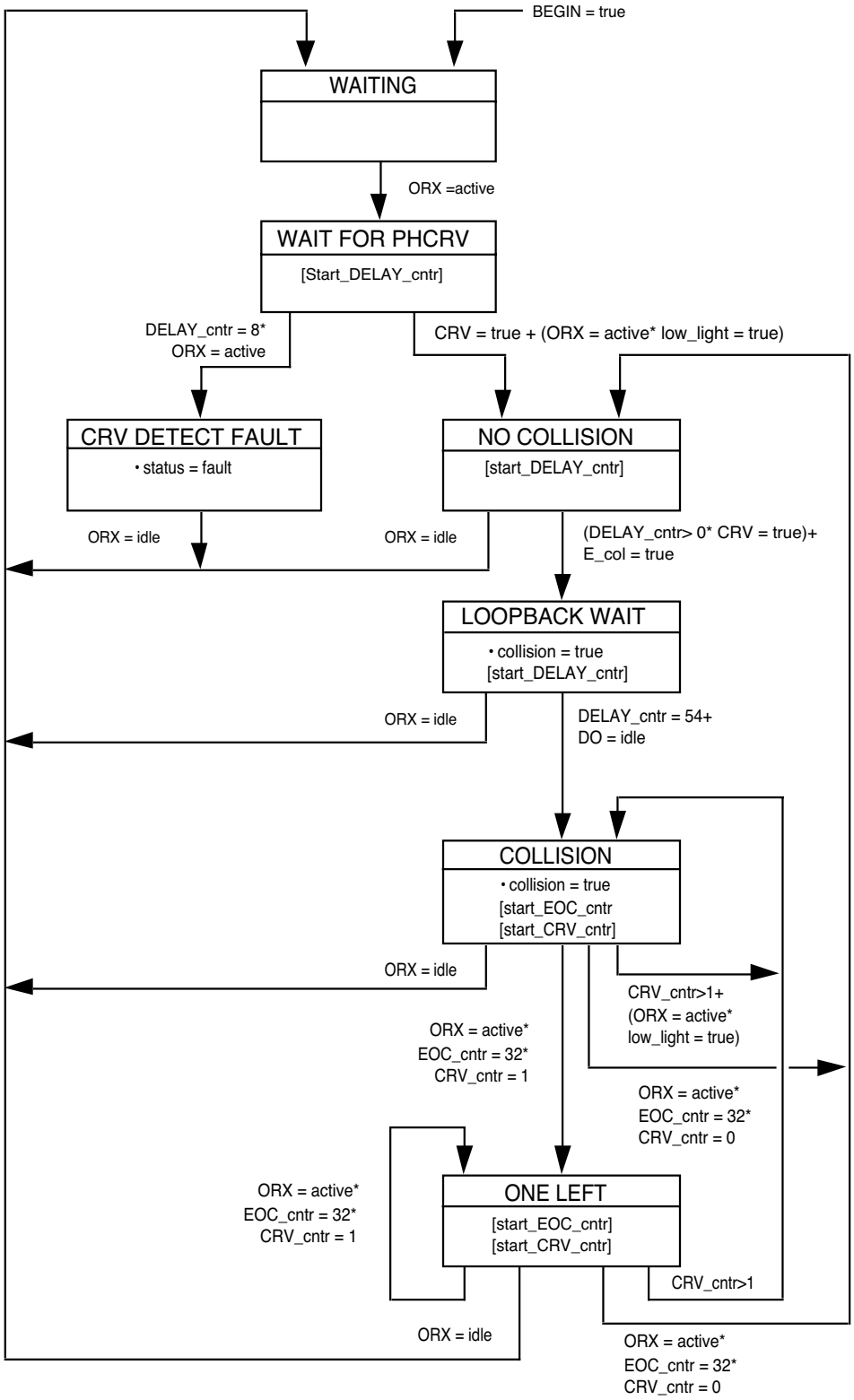


Figure 16–6—Collision detect state diagram

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16.4 Timing summary

Table 16–1 summarizes the timing requirements for 10BASE-FP. This table is a summary; for complete descriptions of the timing to the referenced subclauses. All times are in Bit Times (BT).

Table 16–1—Maximum timing parameters

Symbol	Function	Bit Loss	Invalid Bits	Steady-state Prop. Delay	Start-up delay		
					Max. / Var.		Specified in
M1	*ORD_input* to *input* on DI	0.0	0.0	2.5	2.5	1.0	16.3.2
M2	*output* on DO to *OTD_output*	2.0	0.0	3.5	5.5	3.0	16.3.1
M3	non-looped-back *ORD_input*, and then *output* on DO, to *signal_quality_error* or two *ORD_ crv*, without intervening *ORD_idle*, to *signal_quality_error*				3.5		16.3.4.2
M4a	33 BT with only one *ORD_crv* to *mau_available*			3.0			16.3.4.3
M4b	non-looped-back *ORD_input*, and then *output* on DO, to UWJ as *OTD_output*				3.5		16.3.1.3
M5	while transmitting: two *ORD_crv*, without intervening *ORD_idle*, to UWJ as *OTD_output*			3.5			16.3.1.3
M6	while UWJ as *OTD_output*: *output_idle* to *OTD_idle*			3.5			16.3.1.3
M7	*output_idle* on DO to *signal_quality_error*			6 to 16			16.3.5
M8	*signal_quality_error* duration for SQE test			5 to 15			16.3.5
M9	*output* on DO to *input* on DI	2.0	1.0	1.0	4.0		16.3.3
F1	Fiber Optic Cable Propagation (1000 m)	0	0	50	50		15.3.1.4
A1	AUI Cable Propagation (50 m)	0	0	2.57	2.57		7.4.3.7

16.5 10BASE-FP Star functional specifications

The 10BASE-FP Star provides a means by which the optical signal output from any 10BASE-FP MAU is coupled to the inputs of all 10BASE-FP MAUs attached to the same 10BASE-FP fiber optic segment.

16.5.1 Star functions

16.5.1.1 Number of ports

A star may contain any number of input/output optical interfaces as long as the requirements of 16.5.2 are met.

16.5.1.2 Optical power division

A star shall divide optical power incident on an input port uniformly (within the limits defined in 16.5.2.2) among all output ports without any amplification of the input optical signal.

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16.5.1.3 Configuration

A 10BASE-FP fiber optic segment is configured by attaching a fiber pair between each MAU MDI and a star optical interface. Each MAU OTD circuit shall be connected to an input port of the star, and each MAU ORD circuit shall be connected to an output port. It is recommended for media management purposes to use each output port of the star with its corresponding input port.

16.5.1.4 Reliability

The star shall be designed to provide an MTBF of at least 10 million hours of continuous operation without causing a communication failure among stations attached to the network medium.

16.5.2 Star optical characteristics

16.5.2.1 Star insertion loss

The insertion loss between each input/output optical interface (including the loss of one connector pair) shall be in the range 16 dB to 20 dB, when measured in accordance with ANSI/EIA/TIA 455-180-1990 [B9] using the optical fiber, wavelength, and connector specifications of 15.2.1.1, 15.2.1.2, 15.3.1, and 15.3.2. This insertion loss can generally be met by a star with 33 or fewer input/output optical interfaces. Small-port-count stars may need attenuation in addition to that of the star coupler in order to meet this requirement. A star with more than 33 input/output optical interfaces is not precluded as long as the insertion loss, uniformity, and directivity requirements of this subclause, 16.5.2.2, and 16.5.2.3 are met.

NOTE—The mixing segment insertion loss specified in 15.3.3.1 is generally met by a 33-port star coupler constructed from optical fiber (15.3.1) with connectors 15.3.2) and up to 500 m of optical fiber (15.3.1) on each port. Different sizes and grades of fiber and star coupler may also meet this insertion loss and, while not prohibited, are beyond the scope of this standard.

16.5.2.2 Star single output port uniformity

Single output port uniformity is defined to be the difference between the maximum and minimum insertion loss values (measured according to 16.5.2.1) of any given output port and all input ports. Star single output port uniformity for each output port shall be less than 2.5 dB.

NOTE—Optical uniformity of a star refers to the variation in insertion loss of all input/output port combinations. In the 10BASE-FP system, the uniformity requirement is determined by the receiver. The variation between any given output port and all the input ports needs to be specified. Therefore, it is recommended that each output port connection remain constant during the insertion loss measurements involving that output port. This single output port uniformity is typically better than the overall uniformity of the star.

16.5.2.3 Star directivity

Directivity is the portion of light which is incident on an input port that appears as light emitted from another input port. For the star, directivity for all input optical interface combinations shall be greater than 35 dB. Directivity is measured in accordance with ANSI/EIA/TIA 455-180-1990 [B9] using the optical fiber and wavelength specifications of 15.2.1.1, 15.2.1.2, and 15.3.1.

NOTE—Although passive-star couplers are bidirectional (i.e., light can be transmitted in both directions on one fiber simultaneously), a 10BASE-FP Star cannot use this attribute to support two LANs simultaneously.

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16.6 Protocol Implementation Conformance Statement (PICS) proforma for Clause 16, Fiber optic passive star and medium attachment unit, type 10BASE-FP[29]

16.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 16, Fiber optic passive star and medium attachment unit, type 10BASE-FP, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. The PICS can be used for a variety of purposes by various parties, including the following:

— As a checklist by the protocol implementor, to reduce the risk of failure to conform to the standard through oversight;
— As a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard PICS proforma, by the supplier and acquirer, or potential acquirer, of the implementation;
— As a basis for initially checking the possibility of interworking with another implementation by the user, or potential user, of the implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible PICs);
— As the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation, by a protocol tester.

16.6.2 Abbreviations and special symbols

16.6.2.1 Status symbols

The following symbols are used in the PICS proforma:

M	mandatory field/function
O	optional field/function
O.<n>	is optional field/function, but at least one of the group of options labeled by the same numeral <n> is required
O/<n>	is optional field/function, but one and only one of the group of options labeled by the same numeral <n> is required
X	is prohibited field/function
<item>:	is simple-predicate condition, dependent on the support marked for <item>

16.6.2.2 Abbreviations

N/A	not applicable

16.6.3 Instructions for completing the PICS proforma

16.6.3.1 General structure of the PICS proforma

The first part of the PICS proforma, Implementation Identification and Protocol Summary, is to be completed as indicated with the information necessary to identify fully both the supplier and the implementation.

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The main part of the PICS proforma is a fixed-format questionnaire divided into subclauses, each containing a group of items. Answers to the questionnaire items are to be provided in the right-most column, either by simply marking an answer to indicate a restricted choice (usually Yes, No, or Not Applicable), or by entering a value or a set or range of values. (Note that there are some items where two or more choices from a set of possible answers can apply; all relevant choices are to be marked.)

Each item is identified by an item reference in the first column; the second column contains the question to be answered; the third column contains the reference or references to the material that specifies the item in the main body of the standard; the fourth column contains values and/or comments pertaining to the question to be answered. The remaining columns record the status of the item—whether the support is mandatory, optional, or conditional—and provide the space for the answers; see also 16.6.3.4 below.

The supplier may also provide, or be required to provide, further information, categorized as either Additional Information or Exception Information. When present, each kind of further information is to be provided in a further subclause of items labeled A<i> or X<i>, respectively, for cross-referencing purposes, where <i> is any unambiguous identification for the item (e.g., simply a numeral); there are no other restrictions on its format or presentation.

A completed PICS proforma, including any Additional Information and Exception Information, is the Protocol Implementation Conformance Statement for the implementation in question.

Note that where an implementation is capable of being configured in more than one way, according to the items listed under 16.6.5, Major Capabilities/Options, a single PICS may be able to describe all such configurations. However, the supplier has the choice of providing more than one PICS, each covering some subset of the implementation's configuration capabilities, if that would make presentation of the information easier and clearer.

16.6.3.2 Additional information

Items of Additional Information allow a supplier to provide further information intended to assist the interpretation of the PICS. It is not intended or expected that a large quantity will be supplied, and the PICS can be considered complete without any such information. Examples might be an outline of the ways in which a (single) implementation can be set up to operate in a variety of environments and configurations; or a brief rationale, based perhaps upon specific application needs, for the exclusion of features which, although optional, are nonetheless commonly present in implementations of the 10BASE-FP protocol.

References to items of Additional Information may be entered next to any answer in the questionnaire, and may be included in items of Exception Information.

16.6.3.3 Exception information

It may occasionally happen that a supplier will wish to answer an item with mandatory or prohibited status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No preprinted answer will be found in the Support column for this; instead, the supplier is required to write into the Support column an X<i> reference to an item of Exception Information, and to provide the appropriate rationale in the Exception item itself.

An implementation for which an Exception item is required in this way does not conform to this standard.

Note that a possible reason for the situation described above is that a defect in the standard has been reported, a correction for which is expected to change the requirement not met by the implementation.

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16.6.3.4 Conditional items

The PICS proforma contains a number of conditional items. These are items for which both the applicability of the item itself, and its status if it does apply—mandatory, optional, or prohibited—are dependent upon whether or not certain other items are supported.

Individual conditional items are indicated by a conditional symbol of the form "<item>:<s>" in the Status column, where "<item>" is an item reference that appears in the first column of the table for some other item, and "<s>" is a status symbol, M, O, or X.

If the item referred to by the conditional symbol is marked as supported, the conditional item is applicable, and its status is given by "<s>"; the support column is to be completed in the usual way. Otherwise, the conditional item is not relevant and the Not Applicable (N/A) answer is to be marked.

Each item whose reference is used in a conditional symbol is indicated by an asterisk in the Item column.

16.6.4 Identification

16.6.4.1 Implementation identification

Supplier	
Contact point for queries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

16.6.4.2 Protocol summary

Identification of protocol specification	IEEE Std 802.3-2002,Clause 16, Fiber optic passive star and medium attachment unit, type 10BASE-FP
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See 17.5.3.3; The answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of statement	

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16.6.5 Major capabilities/options

Item	Feature	Reference	Value/comment	Status	Support
*DTE	MAU supports DTE connections	15.1.1	N/A	O.1	Yes [ ] No [ ]
*RPT	MAU supports repeater connections	15.1.1	N/A	O.1	Yes [ ] No [ ]
*AUI	AUI connection physically exists and is accessible for test	15.1.3.2	N/A	O	Yes [ ] No [ ]

16.6.6 PICS proforma for the type 10BASE-FP MAU

16.6.6.1 Compatibility considerations

Item	Feature	Subclause	Value/comment	Status	Support
CC1	Compatibility Considerations: 10BASE-FP Systems compatible at 10BASE-FP MDI	15.1.3.2		M	Yes [ ]
CC2	Mode of operation	15.1.3.5	normal mode only	M	Yes [ ]

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16.6.6.2 Optical transmit parameters

Item	Feature	Subclause	Value/comment	Status	Support
OT1	Center Wavelength	15.2.1.1	min 800 nm max 910 nm	M	Yes [ ]
OT2	Spectral Width (FWHM)	15.2.1.2	< 75 nm	M	Yes [ ]
OT3	Optical Modulation Extinction Ratio	15.2.1.3	< –13 dB	M	Yes [ ]
OT4	Optical Idle Signal Amplitude	15.2.1.4	< 57 dBm	M	Yes [ ]
OT5	Optical Transmit Pulse Logic Polarity	15.2.1.5	High Optical Power = LO on AUI DO and MDI. Low Optical Power = HI on AUI DO and MDI.	M	Yes [ ]
	Optical Transmit Pulse Rise and Fall times	15.2.1.6	Measured from 10% to 90% level		
OT6	Max. (Data)		10.0 ns	M	Yes [ ]
OT7	Min. (Data)		2.0 ns	M	Yes [ ]
OT8	Max. Difference (Data)		3.0 ns	M	Yes [ ]
OT9	Optical Transmit Pulse Over-shoot	15.2.1.7	< 5%	M	Yes [ ]
OT10	Optical Transmit Pulse Under-shoot	15.2.1.7	< 5%	M	Yes [ ]
OT11	Optical Transmit Pulse Edge Jitter, Total at MDI (Data)	15.2.1.8	± 1.0 ns Measured as in 15.2.1.8	M	Yes [ ]
OT12	Optical Transmit Pulse Duty Cycle Distortion (Data)	15.2.1.9	± 1.0 ns max Measured at median power level	M	Yes [ ]
	Optical Transmit Average Power	15.2.1.10			
OT13	Min.		–15 dBm	M	Yes [ ]
OT14	Max.		–11 dBm	M	Yes [ ]
OT15	Transmit signal template	Figure 15–3	Optical signal within template	M	Yes [ ]

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16.6.6.3 Optical receive parameters

Item	Feature	Subclause	Value/comment	Status	Support
OR1	BER between two AUIs attached to a single segment	15.2.2	< one part in 10^9	M	Yes [ ]
 OR2 OR3	Optical Receive Average Power Min. Max.	15.2.2.1	When a single transmitter transmits on the medium –41.0 dBm –27.0 dBm	 M M	 Yes [ ] Yes [ ]
OR4	MAU optical receive Edge Jitter (Data) Received at MDI	15.2.2.2	± 4.5 ns at median power. Measured as in 15.2.2.2.	M	Yes [ ]
OR5	Optical Receive Pulse Logic Polarity	15.2.2.3	High Optical Power = LO on AUI DI and MDI. Low Optical Power = HI on AUI DI and MDI.	M	Yes [ ]
 OR6 OR7	Optical Receive Pulse Rise and Fall Times: Max. (Data) Min. (Data)	15.2.2.4	Measured from 10% to 90% level 18.5 ns 2.0 ns	 M M	 Yes [ ] Yes [ ]

16.6.6.4 Optical medium connector plug and socket

Item	Feature	Subclause	Value/comment	Status	Support
CS1	Connector Socket	15.3.2	BFOC/2.5—see IEC 60874-10: 1992	M	Yes [ ]

16.6.6.5 MAU functions

Item	Feature	Subclause	Value/comment	Status	Support
MF1	Transmit	16.3.1		M	Yes [ ]
MF2	Data Loopback	16.3.3		M	Yes [ ]
MF3	Receive	16.3.2		M	Yes [ ]
MF4	Collision Presence	16.3.4		M	Yes [ ]
MF5	Jabber	16.3.6		M	Yes [ ]
MF6	Link Fault Detection	16.3.7		M	Yes [ ]
MF7	Low Light Detection	16.3.7		M	Yes [ ]
MF8	SQE Test	16.3.5		DTE: M RPT: X	N/A [ ] M: Yes [ ] N/A [ ] X: Yes [ ]

16.6.6.6 PMA interface messages

Item	Feature	Subclause	Value/comment	Status	Support
PIM1	Messages between DTE or repeater PLS and MAU PMA	16.2	As in 7.2.1 and 15.5.4	M	Yes [ ]

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16.6.6.7 PMA to MDI OTD messages

Item	Feature	Subclause	Value/comment	Status	Support
OTD1	Signal sent on OTD corresponding to *OTD_output* message	16.2.2.1	CD1,CD0	M	Yes [ ]
OTD2	Signal sent on OTD corresponding to *OTD_idle* message	16.2.2.2	TDARK	M	Yes [ ]
OTD3	TDARK optical level	16.2.2.2	As in 15.2.1.4	M	Yes [ ]
OTD4	TDARK duration	16.2.2.2	≥ 1.5 BT	M	Yes [ ]
OTD5	Signal sent on OTD to ensure detection of collisions: *OTD_manch_violation* message	16.2.2.3	MV0	M	Yes [ ]

16.6.6.8 MDI ORD to PMA messages

Item	Feature	Subclause	Value/comment	Status	Support
OTD1	Signal received on ORD corresponding to *ORD_input* message	16.2.3.1	CD1,CD0	M	Yes [ ]
OTD2	Signal received on ORD corresponding to *ORD_idle* message	16.2.3.2	RDARK	M	Yes [ ]
OTD3	RDARK Optical Level	16.2.3.2	As in 15.2.1.4	M	Yes [ ]
OTD4	RDARK Duration	16.2.3.2	≥ 1.25 BT	M	Yes [ ]
OTD5	Signal received on ORD corresponding to *ORD_crv* message	16.2.3.3	CRV	M	Yes [ ]

16.6.6.9 Transmit functions

Item	Feature	Subclause	Value/comment	Status	Support
XT1	Signaling rate	16.3.1	10 Mb/s ± 0.005%	M	Yes [ ]
XT2	Optical transmit levels and timing	16.3.1	As in 15.2.1	M	Yes [ ]
XT3	Transmit start-up delay	16.3.1	≤ 5.5 BT	M	Yes [ ]
XT4	First bit transmitted	16.3.1	CD1	M	Yes [ ]
XT5	Transmit path	16.3.1	DO circuit to transmit MDI	M	Yes [ ]
XT6	Preamble encoding	16.3.1.1	Replace first 40 bits of preamble with pattern as described	M	Yes [ ]
XT7	Remainder of preamble	16.3.1.1	Transmitted as received	M	Yes [ ]
XT8	Alignment of remainder of preamble	16.3.1.1	CD1,CD0,…	M	Yes [ ]

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16.6.6.9 Transmit functions *(continued)*

XT9	Number of preamble bits received from DO and sent to the transmit MDI prior to transmission of SFD	16.3.1.1	≥ total number received from DO minus 42 bits and ≤ total number received from DO minus 40 bits	M	Yes [ ]
XT10	Synchronization pattern	16.3.1.1.1	CD1,CD0,CD1,CD0	M	Yes [ ]
XT11	Packet header code rule violation	16.3.1.1.2	CD1,MV0,CD0,CD1	M	Yes [ ]
XT12	Unique Word	16.3.1.1.3	32 bit word as described	M	Yes [ ]
XT13	Unique Word order of transmission	16.3.1.1.3	Least significant bit first	M	Yes [ ]
XT14	Data transmit	16.3.1.2	Following preamble, all data received from DO is sent to transmit MDI	M	Yes [ ]
XT15	Transmit steady-state delay	16.3.1.2	3.5 BT max	M	Yes [ ]
XT16	Transmit delay variability	16.3.1.2	3 BT max for packets ≤ 9.6 μs apart	M	Yes [ ]

16.6.6.10 Collision Encoding (Unique Word Jam) function

Item	Feature	Subclause	Value/comment	Status	Support
CE1	Collision detection to Unique Word Jam transmission delay	16.3.1.3	3.5 BT max	M	Yes [ ]
CE2	Unique Word Jam composition	16.3.1.3	MV0,Unique Word, MV0,Unique Word, MV0,Unique Word, etc.…	M	Yes [ ]
CE3	End of data on DO to end of Unique Word Jam transmission delay	16.3.1.3	3.5 BT max	M	Yes [ ]

16.6.6.11 Receive functions

Item	Feature	Subclause	Value/comment	Status	Support
RCV1	Optical to Electrical conversion	16.3.2	As specified in 15.2.2.3	M	Yes [ ]

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16.6.6.12 Preamble reconstruction and alignment function

Item	Feature	Subclause	Value/comment	Status	Support
PRA1	Start-up delay (receive MDI to DI)	16.3.2.1	2.5 BT max	M	Yes [ ]
PRA2	Receive delay variability	16.3.2.1	1 BT max for any two packets ≤ 9.6 μs apart	M	Yes [ ]
PRA3	Reconstructed preamble composition	16.3.2.1	40 bits of CD1,CD0,CD1,…,CD0 followed by remainder of preamble received on receive MDI	M	Yes [ ]
PRA4	Reconstructed preamble alignment	16.3.2.1	41st bit is CD1	M	Yes [ ]

16.6.6.13 Data receive function

Item	Feature	Subclause	Value/comment	Status	Support
DR1	Receive path (following reconstructed preamble)	16.3.2.2	Receive MDI to DI circuit	M	Yes [ ]
DR2	Steady-state delay (receive MDI to DI)	16.3.2.2	2.5 BT max	M	Yes [ ]

16.6.6.14 Signal presence during collision

Item	Feature	Subclause	Value/comment	Status	Support
SPC1	Signal transmitted on DI during Collision	16.3.2.3	Manchester Fill (CD1,CD0,CD1, etc.)	M	Yes [ ]
SPC2	Transmit valid Manchester during collision	16.3.2.3	For duration of activity on receive MDI	M	Yes [ ]
SPC3	RDARK to end of valid Manchester delay on DI	16.3.2.3	3 BT max	M	Yes [ ]
SPC4	Signal transmitted on DI during invalid data on receive MDI	16.3.2.3	Valid Manchester sequence	M	Yes [ ]

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16.6.6.15 Loopback function

Item	Feature	Subclause	Value/comment	Status	Support
LP1	Data Loopback function	16.3.3	DO signals to DI circuit	M	Yes [ ]
LP2	Loopback bit loss (DO to DI)	16.3.3	2 bits max at start of packet	M	Yes [ ]
LP3	Loopback settling time	16.3.3	2nd and following bits shall meet jitter specifications in 15.2.2.2	M	Yes [ ]
LP4	Loopback steady-state delay	16.3.3	1 BT max	M	Yes [ ]
LP5	DI circuit driver	16.3.3	See 7.4.1	M	Yes [ ]
LP6	Loopback polarity	16.3.3	No signal inversion from DO to DI	M	Yes [ ]

16.6.6.16 Collision presence function

Item	Feature	Subclause	Value/comment	Status	Support
CP1	CI signaling and timing	16.3.4.1	As specified in 7.3.1.2, and modified by 15.1.3.3 and 15.5.4.1	M	Yes [ ]
CP2	Collision Detection	16.3.4.2	CS0 on CI if DO = active and ORD = active (if IPG ≥ OTD to ORD loopback time) or two CRVs detected with no intervening *ORD_idle*	M	Yes [ ]
CP3	Collision indication delay	16.3.4.2	3.5 BT max after second CRV or 3.5 BT max after presence of DO = active and ORD = active	M	Yes [ ]
CP4	Received Power range for detection of CRV	16.3.4.2	As specified in 15.2.2.1	M	Yes [ ]
CP5	Received Differential Power Range for detection of CRV	16.3.4.2	8.0 dB	M	Yes [ ]
CP6	End of Collision determination	16.3.4.3	CS0 on CI until DO = inactive or ORD = idle; or after waiting 54 BT, 33 BT with no more than one CRV detected	M	Yes [ ]
CP7	End of Collision deassertion delay	16.3.4.3	3 BT max	M	Yes [ ]
CP8	CI circuit with no collision, SQE Test or jabber	16.3.4.3	IDL	M	Yes [ ]

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16.6.6.17 *signal_quality_error* Message (SQE) test function

Item	Feature	Subclause	Value/comment	Status	Support
STF1	SQE Test induced OTD or DI signal	16.3.5	No extraneous signals permitted	DTE: M	N/A [ ] M: Yes [ ]
STF2	SQE Test timing (after last positive edge on DO) of CS0 on CI	16.3.5	Start 0.6 μs to 1.6 μs. Duration 5 bits to 15 bits	DTE: M	N/A [ ] M: Yes [ ]

16.6.6.18 Jabber function

Item	Feature	Subclause	Value/comment	Status	Support
JAB1	Jabber function implementation	16.3.6	Self-interrupt of transmit and loopback	M	Yes [ ]
JAB2	Excessive frame timer for jabber detection	16.3.6	20 ms min., 150 ms max.	M	Yes [ ]
JAB3	CI circuit during jabber	16.3.6	CS0 signal	M	Yes [ ]
JAB4	MAU jabber reset delay	16.3.6	0.5 s ± 0.25 s	M	Yes [ ]
JAB5	State of Loopback function during jabber	16.3.6	Disabled	M	Yes [ ]
JAB6	State of Transmit function during jabber	16.3.6	Disabled	M	Yes [ ]
JAB7	Jabber inhibit	16.3.6	Jabber not activated by the longest permitted output specified in 9.6.5	M	Yes [ ]

16.6.6.19 Link Fault Detect function

Item	Feature	Subclause	Value/comment	Status	Support
LF1	Link Test Timer	16.3.7	10 μs ± 2.5 μs	M	Yes [ ]
LF2 LF3 LF4	Actions during detected failure: Data Transmit function Data Receive function Loopback function	16.3.7	 Disabled Disabled Disabled	 M M M	 Yes [ ] Yes [ ] Yes [ ]
LF5	Link heal timer	16.3.7	0.5 s ± 0.25 s	M	Yes [ ]
LF6	Receive power level for link fault detect	16.3.7	Not sufficient to maintain BER $< 10^{-7}$	M	Yes [ ]
LF7	Action if receive power level not sufficient to maintain BER $< 10^{-7}$	16.3.7	CRV = true	M	Yes [ ]
LF8	Link fault reset	16.3.7	Expiration of link_heal_timer followed by optical signal of sufficient power to maintain BER $\leq 10^{-7}$	M	Yes [ ]

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16.6.6.20 MAU state diagram requirements

Item	Feature	Subclause	Value/comment	Status	Support
SD1	Transmit and Receive function state diagram	16.3.9	Meets requirements of Figure 16–2	M	Yes [ ]
SD2	SQE Message Test function state diagram	16.3.9	Meets requirements of Figure 16–3	DTE: M	N/A [ ] M: Yes [ ]
SD3	Link Fault state diagram	16.3.9	Meets requirements of Figure 16–4	M	Yes [ ]
SD4	Jabber function state diagram	16.3.9	Meets requirements of Figure 16–5	M	Yes [ ]
SD5	Collision Detect state diagram	16.3.9	Meets requirements of Figure 16–6	M	Yes [ ]

16.6.6.21 MAU-to-AUI signal characteristics

Item	Feature	Subclause	Value/comment	Status	Support
ASC1	Signaling rate (stated on label)	7.3.2	10 Mb/s	AUI: M	N/A [ ] M: Yes [ ]
ASC2	CS0 signal frequency (on CI)	7.3.1.2	10 MHz ± 15%	AUI: M	N/A [ ] M: Yes [ ]
ASC3	CS0 signal duty cycle	7.3.1.2	60:40 worst case	AUI: M	N/A [ ] M: Yes [ ]

16.6.6.22 MAU-to-AUI DI and CI driver characteristics

Item	Feature	Subclause	Value/comment	Status	Support
ADC1 ADC2	Differential output voltage: Idle state Start of idle	7.4.1.1	 ≤ 40 mV after 80 BT. Figure 7–12	 AUI: M AUI: M	 N/A [ ] M: Yes [ ] N/A [ ] M: Yes [ ]
ADC3	Current into test load while idle	7.4.1.1	4 mA max after 80 BT	AUI: M	N/A [ ] M: Yes [ ]
ADC4	Requirements after idle	7.4.1.2	1st bit to Figure 7–11	AUI: M	N/A [ ] M: Yes [ ]
ADC5	Common-mode output voltage, ac	7.4.1.3	≤ 2.5 V peak for 30 Hz to 40 kHz, ≤ 160 mV peak for 40 kHz to 10 MHz, Figure 7–13	AUI: M	N/A [ ] M: Yes [ ]
ADC6	Differential output voltage, open circuit	7.4.1.4	13 V peak max	AUI: M	N/A [ ] M: Yes [ ]
ADC7	Common-mode output voltage, dc	7.4.1.5	≤ 5.5 V, Figure 7–1	AUI: M	N/A [ ] M: Yes [ ]
ADC8	Fault tolerance	7.4.1.6	Figure 7–14	AUI: M	N/A [ ] M: Yes [ ]
ADC9	Fault current	7.4.1.6	≤ 150 mA, any state, Figure 7–14	AUI: M	N/A [ ] M: Yes [ ]

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16.6.6.23 AUI-to-MAU DO receiver characteristics

Item	Feature	Subclause	Value/comment	Status	Support
DO1	Unsquelched threshold	7.4.2.1	160 mV max diff	AUI: M	N/A [ ] M: Yes [ ]
DO2	Squelch	15.5.1	Reject signals < ±160 mV differential	AUI: M	N/A [ ] M: Yes [ ]
DO3	High to idle transition	7.4.1.1	Must not cause output	AUI: M	N/A [ ] M: Yes [ ]
DO4	Differential input impedance	7.4.2.2	Real part: 77.83 Ω ± 6%, 0 ≤ phase angle ≤ real part ∗ 0.0338	AUI: M	N/A [ ] M: Yes [ ]
DO5	Common-mode range, ac	7.4.2.3	3 V min for 30 Hz to 40 kHz, 200 mV min for 40 kHz to 10 MHz	AUI: M	N/A [ ] M: Yes [ ]
DO6	Total common-mode range	7.4.2.4	Magnitude of 0 to 5.5 Vac+dc	AUI: M	N/A [ ] M: Yes [ ]
DO7	Common-mode current limit	7.4.2.4	≤ 1 mA	AUI: M	N/A [ ] M: Yes [ ]
DO8	IDL detection	7.3.1.1	≤ 1.6 BT	AUI: M	N/A [ ] M: Yes [ ]
DO9	Requirements after idle	7.4.2.5	Receiver in specification after start-up delay	AUI: M	N/A [ ] M: Yes [ ]
DO10	Receiver fault tolerance	7.4.2.6	Figure 7–16	AUI: M	N/A [ ] M: Yes [ ]
DO11	Input fault current	7.4.2.6	3 mA max for Figure 7–16	AUI: M	N/A [ ] M: Yes [ ]

16.6.6.24 MAU-to-AUI circuit termination

Item	Feature	Subclause	Value/comment	Status	Support
ACT1	Common-mode termination	7.5.2.6	If used, must be to VC	AUI: M	N/A [ ] M: Yes [ ]
ACT2	Pins 1, 4, 8, 11, 14 impedance to VC circuit	7.5.2.8	≤ 5 Ω at 5 MHz	AUI: M	N/A [ ] M: Yes [ ]
ACT3	Pins 1, 4, 8, 11, 14 coupling to VC circuit	7.5.2.8	Capacitive	AUI: M	N/A [ ] M: Yes [ ]

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16.6.6.25 MAU-to-AUI mechanical connections

Item	Feature	Sublause	Value/comment	Status	Support
AM1	D-type connector dimensions	7.6.2	IEC 60807-2: 1992 15-pole male	AUI: M	N/A [ ] M: Yes [ ]
AM2	Shell plating material	7.6.2	Conductive	AUI: M	N/A [ ] M: Yes [ ]
AM3	Shell multiple contact points	7.6.2	Number not defined (recommended)	AUI: O	N/A [ ] O: Yes [ ] O: No [ ]
AM4	Shell life expectancy	7.6.2	≤ 5 mΩ after 500 matings	AUI: M	N/A [ ] M: Yes [ ]
AM5	Locking posts and mounting	7.6.1	Figures 7–18 and 7–20	AUI: M	N/A [ ] M: Yes [ ]
	Pin connections	7.6.3	Circuit		
AM6	3		Data Out A	AUI: M	N/A [ ] M: Yes [ ]
AM7	10		Data Out B	AUI: M	N/A [ ] M: Yes [ ]
AM8	11		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM9	5		Data In A	AUI: M	N/A [ ] M: Yes [ ]
AM10	12		Data In B	AUI: M	N/A [ ] M: Yes [ ]
AM11	4		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM12	7		No connection	AUI: M	N/A [ ] M: Yes [ ]
AM13	15		No connection	AUI: M	N/A [ ] M: Yes [ ]
AM14	8		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM15	2		Control In A	AUI: M	N/A [ ] M: Yes [ ]
AM16	9		Control In B	AUI: M	N/A [ ] M: Yes [ ]
AM17	1		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM18	6		Voltage common	AUI: M	N/A [ ] M: Yes [ ]
AM19	13		Voltage plus	AUI: M	N/A [ ] M: Yes [ ]
AM20	1		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM21	Shell		Isolated from all pins	AUI: M	N/A [ ] M: Yes [ ]

16.6.6.26 MAU reliability

Item	Feature	Subclause	Value/comment	Status	Support
MR1	Mean Time Before Failure	15.4	$> 10^7$ hours without causing communications failure among other stations	M	Yes [ ]

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16.6.6.27 Power consumption

Item	Feature	Subclause	Value/comment	Status	Support
PC1	Power surge limitation	15.5.3	$< 2 \times 10^{-3}$ A–s	APW: M	N/A [ ] M: Yes [ ]
PC2	Power surge duration	15.5.3	100 ms max	APW: M	N/A [ ] M: Yes [ ]
PC3	Steady-state current drawn	15.5.3	≤ 0.5 A	APW: M	N/A [ ] M: Yes [ ]
PC4 PC5	Power-up capability: Current-limited sources Voltage-limited sources	15.5.3 7.5.2.5	0.5 A limited. 11.28 to 15.75 V via any AUI cable	APW: M APW: M	N/A [ ] M: Yes [ ] N/A [ ] M: Yes [ ]
PC6	Labeling	15.5.3	As in 15.5.3	APW: M	N/A [ ] M: Yes [ ]
PC7	Power cycle behavior	15.5.3	No extraneous signals on MDI, DI, or CI	AUI: M	
PC8	Low VP behavior	7.5.2.5	No disruption of media	APW: M	N/A [ ] M: Yes [ ]
PC9	Power sourced on pin 13 of AUI	15.5.3	None if separate power source is implemented	SPW: X	N/A [ ] X: Yes [ ]
PC10	Optional power source isolation	15.5.3	If implemented, shall withstand one of 15.3.4 tests	SPW: M	N/A [ ] M: Yes [ ]

16.6.6.28 PLS–PMA requirements

Item	Feature	Subclause	Value/comment	Status	Support
PMA1	Messages between PLS in DTE or Repeater and PMA	15.5.4	As in 7.2.1	M	Yes [ ]

16.6.6.29 *signal_quality_error* message (SQE)

Item	Feature	Subclause	Value/comment	Status	Support
SQE1	Local MAU Transmitting and no Collision or Fault Detected	15.5.4.2.1	*MAU_available* sent on CI	M	Yes [ ]
SQE2	Whenever a Collision exists as described in 16.3.4	15.5.4.2.1	SQE sent	M	Yes [ ]
SQE3	SQE Test as described in 16.3.5	15.5.4.2.1	SQE sent	DTE: M RPT: X	N/A [ ] M: Yes [ ] N/A [ ] X: Yes [ ]
SQE4	Jabber Condition exists as described in 16.3.6	15.5.4.2.1	SQE sent	M	Yes [ ]
SQE5	Message sent in the absence of SQE	15.5.4.2.1	*MAU_available* message	M	Yes [ ]

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16.6.6.30 Environmental requirements

Item	Feature	Subclause	Value/comment	Status	Support
E1	Ambient plane wave field in which MAU meets specification	15.6.2	2 V/m from 10 kHz to 30 MHz. 5 V/m from 30 MHz to 1 GHz	M	Yes [ ]
E2	Electromagnetic emissions and susceptibility	15.6.2	Comply with local and/or national requirements. If none exist, comply with CISPR 22: 1993.	M	Yes [ ]

16.6.6.31 MAU labeling

Item	Feature	Subclause	Value/comment	Status	Support
LBL1	MAU Type	15.7	10BASE-FP	O	Yes [ ] No [ ]
LBL2	Data Rate	15.7	10 Mb/s	O	Yes [ ] No [ ]
LBL3	Power Level	15.7	Maximum current drain	O	Yes [ ] No [ ]
LBL4	Safety Warnings	15.7	Any applicable	O	Yes [ ] No [ ]
LBL5	Port Labeling	15.7	Input and output	O	Yes [ ] No [ ]
LBL6	Manufacturer ID and MAU ID	15.7	12-bit Manufacturer ID and 20-bit MAU ID in separate fields	O	Yes [ ] No [ ]

16.6.7 PICS proforma tables for 10BASE-FP stars

16.6.7.1 Star basic functions

Item	Feature	Subclause	Value/comment	Status	Support
SB1	Optical power division	16.5.1.2	Divide optical power from an input among all outputs (as described in 16.5.2.2)	M	Yes [ ]
SB2	Configuration of 10BASE-FP Stars and MAUs	16.5.1.3	MAU OTD to star input port. MAU ORD to star output port.	M	Yes [ ]
SB3	MTBF without causing communications failure among attached stations	16.5.1.4	10^7 hrs	M	Yes [ ]

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16.6.7.2 Star optical characteristics

Item	Feature	Subclause	Value/comment	Status	Support
SO1	Insertion loss	16.5.2.1	16 dB min 20 dB max	M	Yes [ ]
SO2	Single output port uniformity	16.5.2.2	2.5 dB max	M	Yes [ ]
SO3	Directivity	16.5.2.3	35 dB min	M	Yes [ ]
SO4	Connector socket	15.3.2	BFOC/2.5—see IEC 60874-10: 1992	M	Yes [ ]
SO5	Optical connector loss	15.3.2.1	< 1.0 dB	O	Yes [ ] No [ ]
SO6	Optical connector return loss	15.3.2.2	> 25 dB	M	Yes [ ]

16.6.7.3 Star environmental requirements

Item	Feature	Subclause	Value/comment	Status	Support
SE1	Ambient plane wave field in which star meets specification	15.6.2	2 V/m from 10 kHz to 30 MHz. 5 V/m from 30 MHz to 1 GHz	M	Yes [ ]
SE2	Electromagnetic emissions and susceptibility	15.6.2	Comply with local and/or national requirements. If none exist, comply with CISPR 22: 1993.	M	Yes [ ]

16.6.7.4 10BASE-FP star labeling

Item	Feature	Subclause	Value/comment	Status	Support
SL1	Device type	15.7.1	10BASE-FP Star	O	Yes [ ] No [ ]
SL2	Port labeling	15.7.1	Input and output	O	Yes [ ] No [ ]

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17. Fiber optic medium attachment unit, type 10BASE-FB

17.1 Scope

17.1.1 Overview

This clause, along with Clause 15, defines the functional, electrical, optical, and mechanical characteristics of an optimized fiber optic link for interconnecting repeaters. The relationship of this specification to the entire ISO/IEC 8802-3 CSMA/CD International Standard is shown in Figure 15-1b). This fiber optic link may be used to interconnect repeaters in star topologies and consists of a new PMA specific to the repeater (including a fiber optic MDI specified in 15.2), and the fiber optic medium specified in 15.3. This clause defines a MAU that extends the link distances beyond MAUs specified in 9.9 and significantly increases the number of allowable repeaters in series. While this clause defines a MAU, the AUI shall exist only as a logical service interface.

17.1.1.1 Medium attachment unit

The 10BASE-FB MAU has the following general characteristics:

a) It enables coupling of the Physical Layer Signaling (PLS) messages to the baseband fiber optic link defined in Clause 15.
b) It supports message traffic at a data rate of 10 Mb/s.
c) It provides for operating over 0 to at least 2000 m of fiber optic cable specified in 15.3.
d) It transmits both data and idle signals synchronously with the bit clock and receives data without resynchronizing on each packet.
e) It connects a repeater to a fiber optic backbone link segment.
f) It provides point-to-point signaling of status via synchronous signaling as defined in 17.2.1.
g) It transmits synchronous signals as defined in 17.2.1.
h) It supports network configurations using the CSMA/CD access method defined in IEEE 802.3 with baseband signaling.
i) It supports a point-to-point interconnection between repeaters, and when used with repeaters having multiple ports, supports a star wiring topology.

17.1.1.2 Relationship to repeater

A close relationship exists between Clause 17 and Clause 9. Clause 17 specifies the PMA logical functions residing in the MAU that exist as an integrated MAU in the repeater. A logical interface using messages associated with the AUI is provided as the interface with the repeater. In addition, the Data Loopback function is provided to ensure proper operation of the Partition function defined in 9.6.6.

17.1.1.3 Remote diagnostic messages

The MAU implements remote status signaling during fault conditions. The MAU transmits status messages defined in 17.2.2 and detects the messages described in 17.2.3.

17.1.2 Relationship to AUI

There is no physical implementation of AUI associated with the MAU. Implementation of an AUI, while possible, is beyond the scope of the International Standard. Messages associated with the AUI, however, are used throughout this document as a means to interface with the repeater. Thus, the sole purpose of the use of the messages associated with the AUI is as a service interface. The PMA uses the variables In, Out, and Col and their associated messages to communicate with a port in the repeater.

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17.2 PMA interface messages

The messages between a port in the repeater and the PMA in the MAU shall comply with the PMA interface messages in 17.2.1 and 15.5.4. The messages between the PMAs over the MDI are summarized below.

17.2.1 PMA-to-MDI interface signal encodings

The following signals are used by the interface messages between the PMA and the MDI:

Manchester-Encoded Data One, CD. A clocked bit symbol in which the first half is LO and the second half is HI.

Manchester-Encoded Data Zero, CD0. A clocked bit symbol in which the first half is HI and the second half is LO.

Manchester Code Violation One, MV1. A clocked bit symbol in which the symbol is HI for the bit duration.

Manchester Code Violation Zero, MV0. A clocked bit symbol in which the symbol is LO for the bit duration.

Synchronous Idle, SIDL. Control symbol series coded as the repeating sequence of MV1, MV1, MV0, MV0, starting with the first MV1, resulting in 2.5 MHz signal.

Remote Fault, RF. Control symbol series coded as the repeating sequence of MV1, MV1, MV1, MV0, MV0, MV0, starting with the first MV1, resulting in 1.667 MHz signal.

17.2.2 PMA-to-MDI OTD messages

The signals SIDL and RF shall be made up of sequences of the symbols MV1 and MV0 listed in the table and illustrated in Figure 17–1. All signals shall be transmitted synchronized to the local bit clock. SIDL and RF appear only between PMAs. The following messages can be sent by the MAU PMA to the MDI OTD (Optical Transmit Data) circuit:

Message	Circuit	Signal	Meaning
OTD_output	OTD	CD1, CD0	Output information
OTD_sync_idle	OTD	SIDL (MV1, MV1, MV0, MV0)	Synchronous idle
OTD_remote_fault	OTD	RF (MV1, MV1, MV1, MV0, MV0,MV0)	Jabber, Low Light, Invalid Data, or Lock Lost detected

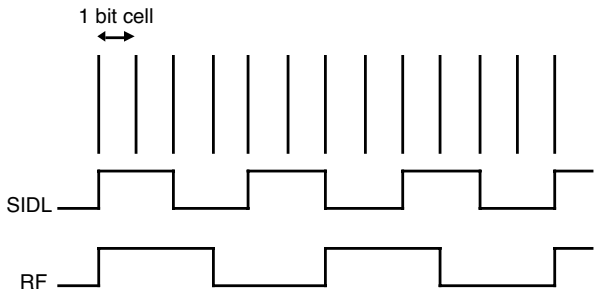


Figure 17–1—MDI status signaling messages

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17.2.2.1 OTD_output

The PMA sublayer sends the *OTD_output* message to the OTD circuit when the repeater outputs a bit of data to the MDI's OTD circuit and the MDI's OTD circuit and the PMA is not sending the *OTD_remote_fault* message. The physical realization of the *OTD_output* message is a CD0 or CD1 signal sent by the PMA.

17.2.2.2 OTD_sync_idle

The PMA sublayer sends the *OTD_sync_idle* message to the OTD circuit when the repeater sends idle and the PMA is not sending *OTD_remote_fault* message. The physical realization of the *OTD_sync_idle* message is a repeating sequence of the SIDL signal sent by the PMA.

17.2.2.3 OTD_remote_fault

The PMA sublayer sends *OTD_remote_fault* message to the OTD circuit when receive jabber is detected, low light has been detected, invalid data has been detected, or continuous clock recovery condition per 17.3.8 is not met ("lock_lost" = true). The physical realization of the *OTD_remote_fault* message is a repeating sequence of the RF signal sent by the PMA. The *OTD_remote_fault* message may be sent when local faults other than the receive jabber, low light or invalid data are present on the ORD circuit. However, the partition condition of the repeater port shall not cause *OTD_remote_fault* to be sent.

17.2.3 MDI ORD-to-PMA messages

17.2.3.1 Status decoding

The following messages shall be received by the MAU PMA from the MDI ORD (Optical Receive Data) circuit.

17.2.3.2 ORD_input

When the PMA sublayer receives the *ORD_input* message on its ORD circuit, it detects a bit of data. The physical realization of the *ORD_input* message is the CD0 or CD1 signal.

17.2.3.3 ORD_sync_idle

When the PMA sublayer receives the *ORD_sync_idle* message on its ORD circuit, it detects idle. The physical realization of the *ORD_sync_idle* message is the SIDL signal.

17.2.3.4 ORD_remote_fault

When the PMA sublayer receives the *ORD_remote_fault* message on its ORD circuit, it detects remote fault. The physical realization of the *ORD_remote_fault* message is the RF signal.

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17.2.3.5 ORD_invalid_data

When the PMA sublayer receives signals other than CD0, CD1, SIDL, or RF while low light is not detected, or input signals that do not meet the requirements in 17.2.4 and 17.3.8, it detects invalid data. The physical realization of the *ORD_invalid_data* message is a signal not meeting the above allowed set.

Message	Circuit	Signal	Meaning
ORD_input	ORD	CD1, CD0	Input Information
ORD_sync_idle	ORD	SIDL (MV1, MV1, MV0, MV0)	Synchronous Idle
ORD_remote_fault	ORD	RF (MV1, MV1, MV1, MV0, MV0, MV0)	Jabber, Low Light, Invalid Data, or LockLost=true detected by the far-end MAU
ORD_invalid_data	ORD	Any signal other than CD0, CD1, SIDL or RF	Undefined or asynchronous signal

17.2.4 Transitions between signals

The SIDL to data (CD0 or CD1) transition shall occur at any bit cell boundary. SIDL shall begin with its first MV1 immediately following the last bit cell of a packet. When a fault is detected during data transmission, the RF signal shall be transmitted immediately following the next bit cell boundary, starting with the first MV1. When a signal that contains alternating MV0 and MV1, starting with a MV0, is detected during a data reception, it shall be interpreted as alternating CD0 and CD1 as long as the sequence persists. When a fault is detected during idle, the SIDL sequence shall be completed before sending RF. Other than defined above, any transition from one status signal to another status signal shall begin only after the previous signal has been sent in its entirety.

17.2.5 Signaling rate

The signaling rate shall conform to 7.3.2.

17.3 MAU functional specifications

The MAU provides the means by which repeaters can be connected for backbone applications by the use of synchronous signaling. In addition, the MAU provides the means by which status on one end of the link may be signaled to the other end to provide media diagnostics.

17.3.1 Transmit function requirements

The Transmit function shall transmit the output message received from the repeater unit onto the MDI. The Transmit function has three purposes:

a) To convert the electrical signals to optical signals.
b) To generate the SIDL signal when receiving the *output_idle* message from the repeater.
c) To generate the RF signal.

The levels and timing of the optical signal shall be as specified in 15.2.1, and any transition from one signal to another shall meet the requirements in 17.2.4.

17.3.1.1 Data transmit

The Transmit function shall receive the output messages from the repeater unit and send them onto the MDI OTD circuit. When a packet is received at this interface, no bit of information shall be received from the repeater and not transmitted to the MDI. In addition, only the bits of information received from the repeater shall be transmitted to the MDI. The start-up and steady-state delay between output message and

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transmission on the MDI shall each be no more than 2 BT. If a fault is detected during data transmission, data transmission shall cease and the RF signal shall be transmitted as specified in 17.2.4 and 17.3.1.3.

17.3.1.2 Synchronous idle

Whenever the repeater unit sends the *idle* message, SIDL signal shall be sent on the OTD circuit of the MDI, when the PMA is not sending the *OTD_remote_fault* message.

17.3.1.3 Fault signaling

Upon detecting receive jabber as specified in 17.3.6, or low light as specified in 17.3.7, or unqualified input signal as specified in 17.3.8, the Transmit function shall output RF signal on the OTD circuit of the MDI.

17.3.2 Receive function requirements

The Receive function shall receive optical signals from the ORD circuit of the MDI and send *input* or *idle* messages to the repeater unit. The Receive function has two purposes:

a) To convert optical signals to electrical signals.
b) To detect and interpret CD0, CD1, SIDL, and RF.

The optical to electrical conversion shall be as specified in 15.2.2.3.

17.3.2.1 Data receive

The Receive function shall receive the CD0 or CD1 signals from the ORD circuit of the MDI and send *input* messages to the repeater unit. When a packet is received, all bits of information shall be received from the ORD circuit and sent to the repeater unit. In addition, only the bits of information received from the ORD circuit shall be sent to the repeater unit. Any transition of one signal to another not meeting the requirements in 17.2.4 shall be detected as *ORD_invalid_data* message. When *ORD_invalid _data* message is received, data transmission shall be prevented. The start-up and steady-state delay between reception on MDI to *input* message shall be no more than 2 BT.

17.3.2.2 Remote status message handling

The Receive function shall recognize the signals SIDL or RF at the MDI and send the *input_idle* message to the repeater unit. The reception of the RF signal at the MDI shall prevent data transmissions.

17.3.3 Collision function requirements

17.3.3.1 Collision detection

The MAU shall detect as a collision the simultaneous occurrence of *ORD_input* message on the ORD circuit and the *output* message from the repeater. When a collision has occurred, the *signal_quality_error* message shall be sent to the repeater within 3.5 BT.

17.3.3.2 End of collision

The MAU shall detect as the end of collision either the *output_idle* message or messages other than *ORD_input* received from the ORD circuit. When the end of a collision occurs, the *mau_available* message shall be sent to the repeater within 5 BT and the *input_idle* message shall be sent to the repeater within 5 BT.

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17.3.4 Loopback function requirements

The Loopback function is defined to provide the same service interface as other MAUs between the PMD and the repeater. Since this MAU does not have a physical AUI, this function is logically present but not necessarily physically implemented.

When the MAU is transmitting on the OTD circuit and is not receiving *ORD_input* messages on the ORD circuit, the MAU shall transmit either *output* messages as *input* messages or *output_idle* messages as *input_idle* messages. The steady-state propagation delay of this message transfer shall not exceed 2 BT.

17.3.5 Fault-handling function requirements

There are two types of faults that shall be detected: local and remote. The local faults are detection of low light, receive jabber, and invalid data conditions. The remote status signals consist of receptions of normal idle (indicated by the signal SIDL), and remote faults (indicated by the signal RF). Table 17–1 defines the signals that shall be sent onto the media at the port's MDI during fault conditions.

Table 17–1—MDI fault conditions and their states

Fault types	Signal at OTD MDI
Low Light detected	RF
Receive Jabber detected	RF
Invalid Data detected	RF
Receive RF	SIDL

During reception of RF, SIDL shall be transmitted at the MDI, unless there is a local fault.

17.3.6 Jabber function requirements

A MAU shall contain a self-interrupt capability, as described in Figure 17–3, to prevent an illegally long reception of data from reaching the Data-Handling function of the repeater. The MAU shall provide a window "rcv_max" during which the *input* messages may be sent to the repeater unit. The value of "rcv_max" shall be between 8 ms and 12 ms. If a reception exceeds this duration, the jabber condition shall be detected.

Upon detection of the jabber condition, the MAU shall perform the following:

a) Inhibit sending further *input* messages to the repeater unit,
b) Disable the *OTD_sync_idle* message (17.2.2.2) to the MDI, and
c) Send the *OTD_remote_fault* message (17.2.2.3) to the MDI.

The MAU shall reset the Jabber function and reassert *OTD_sync_idle* message when one of the following conditions is met:

— On power-up reset, or
— After a continuous time "rcv_unjab" of not detecting jabber on the ORD circuit of the MAU (see Figure 17–3).

The value of "rcv_unjab" shall be 0.5 s ± 0.25 s.

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17.3.7 Low light level detection function requirements

The MAU shall have the capability to interrupt a port's reception at the MDI ORD circuit when reliable reception can no longer be assured at that port based on the incoming optical power level.

The MAU shall have a low light level detection capability as defined in Figure 17–2. It shall interrupt reception of any signals from the ORD circuit of the MDI when reliable detection can no longer be assured. This error condition shall not be detected if the average receive optical power level at the MDI exceeds –32.5 dBm in the frequency band between 0.5 MHz to 25 MHz. It shall also not be detected if the low light condition remains for less than 30 BT. It shall be detected before the average receive optical power level at the MDI has fallen to a level that is lower than the average receive optical power level that corresponds to a BER of one part in 10^{10} for the MAU for a duration of 2000 BT. The low light level detected condition shall cease to exist when the received optical power level exceeds the power level required to maintain a BER of one part in 10^{10} and the requirements in 17.3.8 are met.

On detection of the low light level detection condition at its MDI, the MAU shall perform the following:

a) Inhibit sending further input messages to the repeater unit,
b) Inhibit the Data Transmit function,
c) Disable the *OTD_sync_idle* message (17.2.2.2) to the MDI, and
d) Send the *OTD_remote_fault* message (17.2.2.3) to the MDI.

Once the low light condition continuously ceases to exist at the port for a time "low_light_heal" of 0.5 s ± 0.25 s, the MAU shall reset the Low Light function.

17.3.8 Synchronous qualification function requirements

The MAU shall have the capability in Figure 17–2 to interrupt reception at the MDI when reliable reception can no longer be assured based on the loss of clock recovery. The synchronous signaling condition shall be detected at a port if SIDL or RF is detected for the entire duration of the time "validation" of successful and continuous clock recovery. The value of time "validation" shall be between 64 BT and 128 BT. The clock recovery shall tolerate the jitter specified in 15.2.2.2 at the MDI and recover clocks with proper frequency and tolerances. The variable "lock_lost" shall not take the value "true" when the input meets the requirements of 15.2.2. The variable "lock_lost" shall take the value true within 20 μs after the input frequency on the ORD circuit is less than or equal to 1.55 MHz or greater than or equal to 15.5 MHz.

On qualifying the synchronous signaling condition for signals received on the ORD circuit of the MAU, Data Transmit and Data Receive for that port shall be enabled. On loss of synchronous signaling qualification for the MAU, Data Transmit and Data Receive for that port shall be disabled, and the PMA sublayer shall send *OTD_remote_fault* on the MDI.

17.3.9 Interface message time references

Delay and bit loss specification are measured from the occurrence of messages at the MDIs. The following describes the point where each message starts:

Message	Reference
OTD_output	leading Bit Cell Boundary of of first CD1 or CD0
OTD_sync_idle	last positive-going transition prior to start of SIDL
OTD_remote_fault	last positive-going transition prior to start of RF
ORD_input	leading Bit Cell Boundary of first CD1 or CD0
ORD_sync_idle	last positive-going transition prior to start of SIDL
ORD_remote_fault	last positive-going transition prior to start of RF

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17.3.10 MAU state diagrams

The state diagrams of Figures 17–2, 17–3, and 17–4[30] depict the full set of allowed MAU state functions relative to the circuits of the MDI and AUI Service Interface. The notation used in the state diagrams follows the conventions in 1.2.1. The variables, counters, and timers used in the state diagrams are defined in the following subclauses.

17.3.10.1 MAU state diagram variables

Variables are used in the state diagrams to indicate the status of the MAU's inputs and outputs, to control its operation, and to pass state information between functions.

In the variable definitions, the name of the variables is followed by a brief description of the variable and a list of values the variable may take. For those variables that are state diagram outputs, one value will be identified as the default. The variable has the default value when no active state contains a term assigning a different value.

The variables used in the state diagrams are as follows:

begin

The interprocess flag controlling state diagram initialization values.
Values: false (default).
true.

OTD

Controls the signal sent by the MAU's PMA to the OTD circuit.
Values: idle; the MAU sends *OTD_sync_idle*, SIDL (default).
output; the MAU sends *OTD_output*; CD0 or CD1, based on the *output* message from the repeater unit.
remote_fault; the MAU sends *OTD_remote_fault*, RF.

ORD

Status of the signal sent by the MAU's ORD circuit to the PMA.
Values: idle; the MAU receives *ORD_sync_idle*, SIDL.
input; the MAU receives *ORD_input*; CD0, CD1, or MV0,MV1 signal sequence meeting 17.2.4.
remote_fault; the MAU receives *ORD_remote_fault*, RF.
invalid_data; the MAU receives *ORD_invalid_data*, all signals not meeting 17.2.4. and 17.3.8.

OUT

Status of the messages sent by the repeater to the PMA.
Values: idle; receives *output_idle* message from the repeater unit.
output; receives *output* message from the repeater unit.

IN

Controls the signal sent by the MAUs PMA to the repeater.
Values: idle; the MAU sends the *input_idle* message to the repeater (default).
input; the MAU sends the *input* message to the repeater.
OUT; the MAU sends messages from the repeater back to the repeater.

[30]The MAU state diagrams, Figures 17–2 through 17–4, follow 17.3.10.2.

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COL

Controls the signal sent by the MAUs PMA to the repeater.
Values: mau_available; the MAU sends the *mau_available* message to the repeater (default).
signal_quality_error; The MAU sends the *signal_quality_error* message to the repeater.

low_light_detected

Controls the paths of the signals received from the ORD circuit.
Values: true; low light condition is being detected.
false; low light condition is not being detected (default).

rcv_jab_detected

Also controls the path of the signals received from the ORD circuit.
Values: false; receive jabber condition is not being detected (default).
true; receive jabber condition is being detected.

low_light_level

Status of the optical signal level received on the ORD circuit.
Values: true; insufficient light is being received for reliable reception (see 17.3.7).
false; sufficient light is being received for reliable reception.

lock_lost

Status of the Synchronous Qualification function of the ORD circuit.
Values: true; clock has not been recovered.
false; clock has been recovered.

link_valid

Interprocess flag indicating that the link is valid.
Values: false; link is determined to be invalid (default).
true; link is determined to be valid.

17.3.10.2 MAU state diagram timers

All timers operate in the same fashion. A timer is reset and starts counting upon entering a state where "start x_timer" is asserted. When the timer has expired, x_timer_done is asserted and remains asserted until the timer is reset. At all other times, x_timer_not_done is asserted. The timer is reset and restarted even if the entered state is the same as the exited state.

The timers used in the MAU state diagrams are defined as follows:

validation_timer. Timer for synchronous link detection (17.3.8).

rcv_max_timer. Timer for excessively long reception (17.3.6).

rcv_unjab_timer. Timer for the length of time the ORD circuit must have no excessively long activity to exit the jabber state (17.3.6).

low_light_heal_timer. Timer for low light condition cessation (17.3.7).

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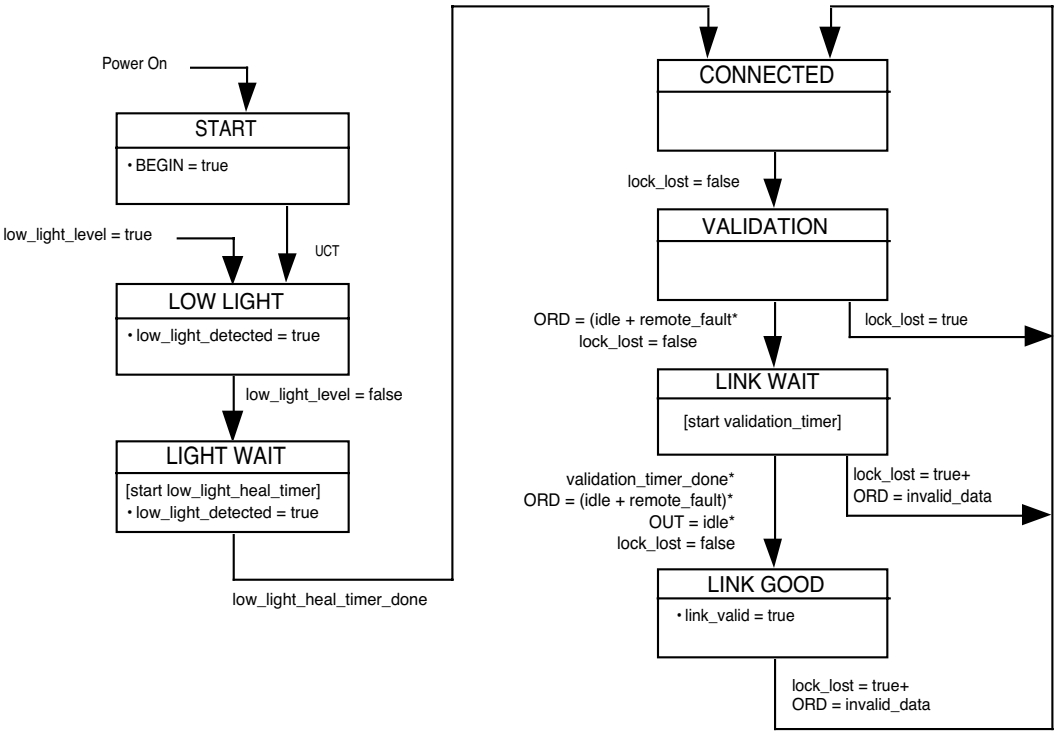


Figure 17–2—Synchronous qualification state machine

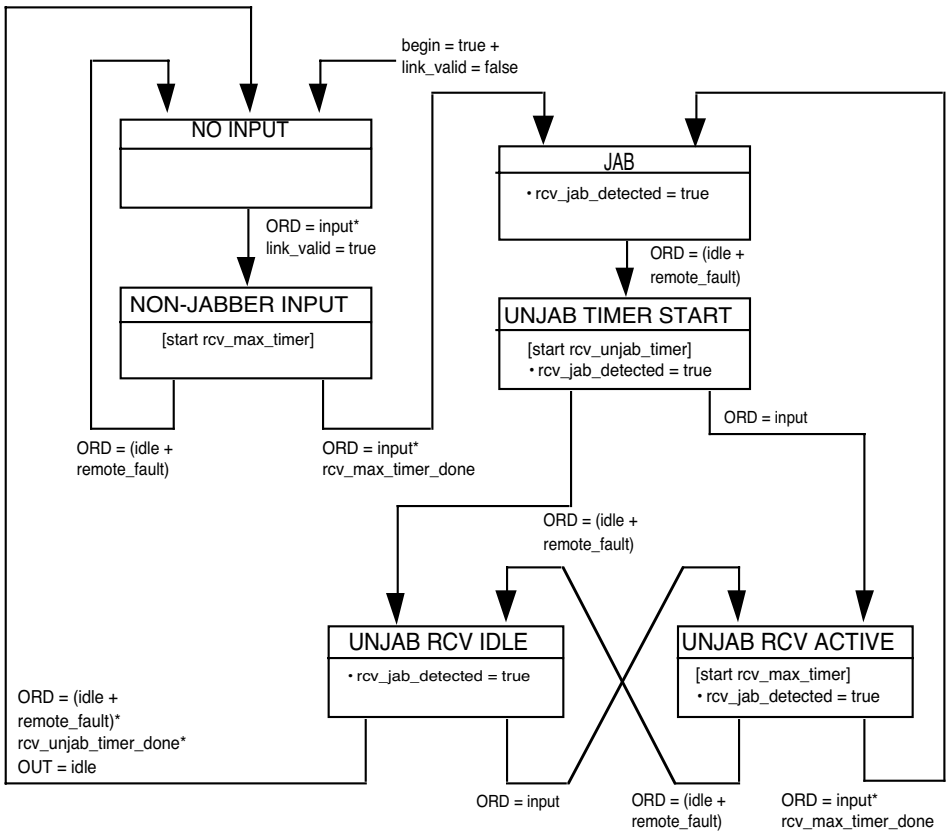


Figure 17–3—Receive jabber state machine

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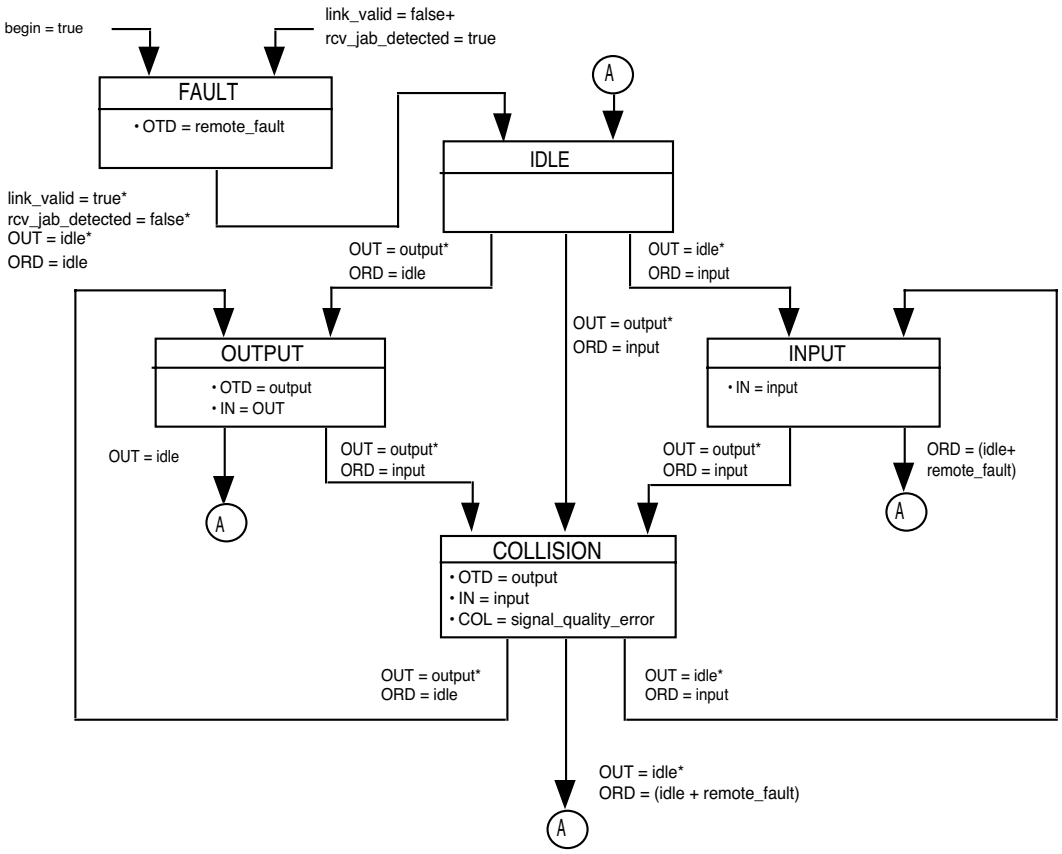


Figure 17–4—MAU transmit, receive, loopback, and collision presence functions state diagram

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17.4 Timing summary

Table 17–2 summarizes the timing requirements for the 10BASE-FB fiber link. This table is a summary; for complete descriptions of the timing requirements, refer to the referenced subclauses. All times are in Bit Times.

Table 17–2—Maxiumum timing parameters

Symbol	Function	Bit loss	Invalid bits	Steady-state prop. delay	Start-up delay		Specified in
					Max	/ Var	
M1	*ORD_input* to *input* to PMA	0.0	0.0	2.0	2.0	2.0	17.3.2.1
M2	*output* on PMAto *OTD_output*	0.0	0.0	2.0	2.0	2.0	17.3.1.1
M3	ORD_*input* * *output* to *signal_quality_error*				3.5		17.3.3.1
M4	*ORD_sync_idle* + *output_idle* (end of collision) to *mau_available*				5.0		17.3.3.2
M5	*ORD_input* * *output* to *input* to PMA from circuit ORD				5.0		17.3.3.2
M6	*ORD_sync_idle* **output* to *input* to PMA from PMA output circuit				5.0		17.3.3.2
M9	*output* on PMA to *input* to PMA	0.0	0.0	2.0			17.3.4
F1	Fiber Optic Cable Propagation (2000 m)	0	0	100	100		15.3.1.4

17.5 Protocol implementation conformance statement (PICS) proforma for Clause 17, Fiber optic medium attachment unit, type 10BASE-FB[31]

17.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 17, Fiber optic medium attachment unit, type 10BASE-FB, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. The PICS can be used for a variety of purposes by various parties, including the following:

— As a checklist by the protocol implementor, to reduce the risk of failure to conform to the International Standard through oversight;
— As a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard PICS proforma, by the supplier and acquirer, or potential acquirer, of the implementation;

[31]*Copyright release for PICS Proformas:* Users of this International Standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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— As a basis for initially checking the possibility of interworking with another implementation by the user, or potential user, of the implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible PICs);
— As the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation, by a protocol tester.

17.5.2 Abbreviations and special symbols

17.5.2.1 Status symbols

The following symbols are used in the PICS proforma:

M	mandatory field/function
O	optional field/function
O.<n>	optional field/function, but at least one of the group of options labeled by the same numeral <n> is required
O/<n>	optional field/function, but one and only one of the group of options labeled by the same numeral <n> is required
X	prohibited field/function
<item>:	simple-predicate condition, dependent on the support marked for <item>

17.5.2.1.1 Abbreviations

N/A	not applicable

17.5.3 Instructions for completing the PICS proforma

17.5.3.1 General structure of the PICS proforma

The first part of the PICS proforma, Implementation Identification and Protocol Summary, is to be completed as indicated with the information necessary to identify fully both the supplier and the implementation.

The main part of the PICS proforma is a fixed-format questionnaire divided into subclauses, each containing a group of items. Answers to the questionnaire items are to be provided in the right-most column, either by simply marking an answer to indicate a restricted choice (usually Yes, No, or Not Applicable), or by entering a value or a set or range of values. (Note that there are some items where two or more choices from a set of possible answers can apply; all relevant choices are to be marked.)

Each item is identified by an item reference in the first column; the second column contains the question to be answered; the third column contains the reference or references to the material that specifies the item in the main body of the International Standard; the fourth column contains values and/or comments pertaining to the question to be answered. The remaining columns record the status of the item—whether the support is mandatory, optional, or conditional—and provide the space for the answers; see also 17.5.3.4 below.

The supplier may also provide, or be required to provide, further information, categorized as either Additional Information or Exception Information. When present, each kind of further information is to be provided in a further subclause of items labeled A<i> or X<i>, respectively, for cross-referencing purposes, where <i> is any unambiguous identification for the item (e.g., simply a numeral); there are no other restrictions on its format or presentation.

A completed PICS proforma, including any Additional Information and Exception Information, is the Protocol Implementation Conformance Statement for the implementation in question.

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Note that where an implementation is capable of being configured in more than one way, according to the items listed under 17.5.5, Major Capabilities/Options, a single PICS may be able to describe all such configurations. However, the supplier has the choice of providing more than one PICS, each covering some subset of the implementation's configuration capabilities, if that would make presentation of the information easier and clearer.

17.5.3.2 Additional information

Items of Additional Information allow a supplier to provide further information intended to assist the interpretation of the PICS. It is not intended or expected that a large quantity will be supplied, and the PICS can be considered complete without any such information. Examples might be an outline of the ways in which a (single) implementation can be set up to operate in a variety of environments and configurations; or a brief rationale, based perhaps upon specific application needs, for the exclusion of features which, although optional, are nonetheless commonly present in implementations of the 10BASE-FB protocol.

References to items of Additional Information may be entered next to any answer in the questionnaire, and may be included in items of Exception Information.

17.5.3.3 Exception information

It may occasionally happen that a supplier will wish to answer an item with mandatory or prohibited status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No preprinted answer will be found in the Support column for this; instead, the supplier is required to write into the Support column an X<i> reference to an item of Exception Information, and to provide the appropriate rationale in the Exception item itself.

An implementation for which an Exception item is required in this way does not conform to this International Standard.

Note that a possible reason for the situation described above is that a defect in the International Standard has been reported, a correction for which is expected to change the requirement not met by the implementation.

17.5.3.4 Conditional items

The PICS proforma contains a number of conditional items. These are items for which both the applicability of the item itself, and its status if it does apply—mandatory, optional, or prohibited—are dependent upon whether or not certain other items are supported.

Individual conditional items are indicated by a conditional symbol of the form "<item>:<s>" in the Status column, where "<item>" is an item reference that appears in the first column of the table for some other item, and "<s>" is a status symbol, M, O, or X.

If the item referred to by the conditional symbol is marked as supported, the conditional item is applicable, and its status is given by "<s>"; the support column is to be completed in the usual way. Otherwise, the conditional item is not relevant and the Not Applicable (N/A) answer is to be marked.

Each item whose reference is used in a conditional symbol is indicated by an asterisk in the Item column.

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17.5.4 Identification

17.5.4.1 Implementation identification

Supplier	
Contact point for queries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

17.5.4.2 Protocol summary

Identification of protocol specification	IEEE Std 802.3-2002, Clause 17, Fiber optic medium attachment unit, type 10BASE-FB
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exception items been required? No [ ]Yes [ ] (See 17.5.3.3; The answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

17.5.5 PICS proforma for the type 10BASE-FB MAU

None.

17.5.6 PICS proforma for the type 10BASE-FB MAU

17.5.6.1 Compatibility considerations

Item	Feature	Subclause	Value/comment	Status	Support
CC1	Compatibility Considerations: 10BASE-FB Systems compatible at 10BASE-FB MDI	15.1.3.2		M	Yes [ ]
CC2	Mode of operation	15.1.3.5	normal mode only	M	Yes [ ]

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17.5.6.2 Optical transmit parameters

Item	Feature	Subclause	Value/comment	Status	Support
OT1	Center wavelength	15.2.1.1	min. 800 nm max. 910 nm	M	Yes [ ]
OT2	Spectral width (FWHM)	15.2.1.2	< 75 nm	M	Yes [ ]
OT3	Optical modulation extinction ratio	15.2.1.3	< –13 dB	M	Yes [ ]
OT4	Optical idle signal amplitude	15.2.1.4	See 15.2.1.10	M	Yes [ ]
OT5	Optical transmit pulse logic polarity	15.2.1.5	High Optical Power=LO on AUI DO and MDI. Low Optical Power =HI on AUI DO and MDI	M	Yes [ ]
	Optical transmit pulse rise and fall times	15.2.1.6	Measured from 10% to 90% level		
OT6	Max. (Data)		10.0 ns	M	Yes [ ]
OT7	Min. (Data)		0.0 ns	M	Yes [ ]
OT8	Max. difference (Data)		3.0 ns	M	Yes [ ]
OT9	Max. (Idle)		10.0 ns	M	Yes [ ]
OT10	Min. (Idle)		0.0 ns	M	Yes [ ]
OT11	Max. difference (Idle)		3.0 ns	M	Yes [ ]
OT12	Optical Transmit Pulse Overshoot	15.2.1.7	< 25%	M	Yes [ ]
OT13	Optical Transmit Pulse Undershoot	15.2.1.7	< 10%	M	Yes [ ]
	Optical Transmit Pulse Edge Jitter Added	15.2.1.8	Measured as in 15.2.1.8		
OT14	Total at MDI (Data)		± 2.0 ns	M	Yes [ ]
OT15	Total at MDI (Idle)		± 4.0 ns	M	Yes [ ]
	Optical Transmit Pulse Duty Cycle Distortion	15.2.1.9	Measured at median power level		
OT16	Max. (Data)		± 2.5 ns	M	Yes [ ]
OT17	Max. (Idle)		± 2.5 ns	M	Yes [ ]
	Optical Transmit Average Power Range	15.2.1.10			
OT18	Min.		–20 dBm	M	Yes [ ]
OT19	Max.		–12 dBm	M	Yes [ ]
OT20	Transmit Signal Templates	Figure 15–4	Optical signals within template	M	Yes [ ]

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17.5.6.3 Optical receive parameters

Item	Feature	Subclause	Value/comment	Status	Support
OR1	BER between two AUIs attached to a single segment	15.2.2	< one part in 10^9 (measurement made by inference)	M	Yes [ ]
	Optical Receive Average Power	15.2.2.1	When a single transmitter transmits on the medium		
OR2	Min.		–32.5 dBm	M	Yes [ ]
OR3	Max.		–12.0 dBm	M	Yes [ ]
	MAU optical receive Edge Jitter (Data)	15.2.2.2	Measured as in 15.2.2.2		
OR4	Received at MDI		± 2.0 ns at median	M	Yes [ ]
OR5	Total at DI circuit (MAU end of AUI)		± 6.5 ns at zero crossing points	M	Yes [ ]
OR6	Optical Receive Pulse Logic Polarity	15.2.2.3	High Optical Power = LO on AUI DI and MDI. Low Optical Power = HI on AUI DI and MDI.	M	Yes [ ]
	Optical Receive Pulse Rise and Fall Times	15.2.2.4	Measured from 10% to 90% level		
OR7	Max. (Data)		31.5 ns	M	Yes [ ]
OR8	Min. (Data)		0.0 ns	M	Yes [ ]
OR9	Max. difference (Data)		3.0 ns	M	Yes [ ]
OR10	Max. (Idle)		31.5 ns	M	Yes [ ]
OR11	Min. (Idle)		2.0 ns	M	Yes [ ]
OR12	Max. difference (Idle)		3.0 ns	M	Yes [ ]

17.5.6.4 Optical medium connector plug and socket

Item	Feature	Subclause	Value/comment	Status	Support
CS1	Connector socket	15.3.2	BFOC/2.5—see IEC 60874-10: 1992	M	Yes [ ]

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17.5.6.5 MAU functions

Item	Feature	Subclause	Value/comment	Status	Support
MF1	Transmit data	17.3.1.1		M	Yes [ ]
MF2	Transmit SIDL	17.3.1.2		M	Yes [ ]
MF3	Transmit RF	17.3.1.3		M	Yes [ ]
MF4	Data Loopback	17.3.4		M	Yes [ ]
MF5	Receive data	17.3.2.1		M	Yes [ ]
MF6	Receive SIDL	17.3.2.2		M	Yes [ ]
MF7	Receive RF	17.3.2.2		M	Yes [ ]
MF8	Collision Presence	17.3.3		M	Yes [ ]
MF9	Fault Handling	17.3.5		M	Yes [ ]
MF10	Jabber	17.3.6		M	Yes [ ]
MF11	Low light level detect	17.3.7		M	Yes [ ]

17.5.6.6 PMA-to-MDI OTD messages and signaling

Item	Feature	Subclause	Value/comment	Status	Support
OTD1	Repeater port to MAU PMA messages	17.2	As in 7.2.1 and 15.5.4	M	Yes [ ]
OTD2	Signal sent on OTD corresponding to *OTD_output* message	17.2.2	CD1,CD0	M	Yes [ ]
OTD3	Signal sent on OTD corresponding to *OTD_sync_idle* message	17.2.2	SIDL (i.e., MV1, MV1,MV0,MV0)	M	Yes [ ]
OTD4	Signal sent on OTD corresponding to *OTD_remote_fault* message	17.2.2	RF (i.e., MV1,MV1, MV1,MV0,MV0,MV0)	M	Yes [ ]
OTD5	Signal sent on OTD when repeater port is partitioned	17.2.2.3	SIDL (i.e., MV1 MV1,MV0,MV0)	M	Yes [ ]
OTD6	Synchronization of transmitted signals	17.2.2	To local bit clock	M	Yes [ ]
OTD7	AUI	17.1.1	Logical service interface only	M	Yes [ ]

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17.5.6.7 MDI ORD-to-PMA messages and signaling

Item	Feature	Subclause	Value/comment	Status	Support
ORD1	Signal received on ORD corresponding to *ORD_input* message	17.2.3.2	CD1, CD0	M	Yes [ ]
ORD2	Signal received on ORD corresponding to *ORD_sync_idle* message	17.2.3.3	SIDL (i.e., MV1,MV1, MV0,MV0)	M	Yes [ ]
ORD3	Signal received on ORD corresponding to *ORD_remote_fault* message	17.2.3.4	RF (i.e., MV1,MV1, MV1, MV0,MV0,MV0)	M	Yes [ ]
ORD4	Signal received on ORD corresponding to *ORD_invalid_data* message	17.2.3.5	Not CD0, CD1, SIDL, or RF	M	Yes [ ]

17.5.6.8 Transitions between signals

Item	Feature	Subclause	Value/comment	Status	Support
TBS1	SIDL to data transition	17.2.4	Only at any bit cell boundary	M	Yes [ ]
TBS2	Start of SIDL	17.2.4	End of last bit cell of packet. Start with first MV1 of signal.	M	Yes [ ]
TBS3	Start of RF	17.2.4	Next bit cell boundary following fault detection. Start with first MV1 of signal.	M	Yes [ ]
TBS4	Transition between status signals	17.2.4	Only after signal sequence has been completed	M	Yes [ ]
TBS5	Interpretation of signal containing alternating MV0 and MV1, starting with MV0	17.2.4	CD0, CD1	M	Yes [ ]

17.5.6.9 Signaling rate

Item	Feature	Subclause	Value/comment	Status	Support
SR1	Signaling rate	17.2.5	As in 7.3.2	M	Yes [ ]

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17.5.6.10 Transmit functions

Item	Feature	Subclause	Value/comment	Status	Support
XT1	Data Transmit Path for *output* message	17.3.1	Repeater unit to MDI OTD circuit	M	Yes [ ]
XT2	Levels and timing of optical signal	17.3.1	15.2.1	M	Yes [ ]
XT3	Transition from one signal to another	17.3.1	17.2.4	M	Yes [ ]
XT4	Data Transmit	17.3.1.1	Receives *output* message and sends it on the MDI OTD circuit	M	Yes [ ]
XT5	Information received from repeater and passed to MDI OTD	17.3.1.1	All	M	Yes [ ]
XT6	Information passed to MDI OTD that was not received from repeater	17.3.1.1	None	M	Yes [ ]
XT7	Conditions for SIDL transmission on OTD circuit of the MDI	17.3.1.2	Whenever repeater sends *idle* message and the PMA is not sending the *OTD_remote_fault* message	M	Yes [ ]
XT8	Conditions for RF transmission on OTD circuit of the MDI	17.3.1.3	Whenever *receive_jabber*, *low_light*, or unqualified input signal is detected at port's receive MDI	M	Yes [ ]
XT9	Maximum start-up and steady-state delay circuit of the MDI	17.3.1.1	2 BT between *output* message and transmission on MDI	M	Yes [ ]

17.5.6.11 Receive functions

Item	Feature	Subclause	Value/comment	Status	Support
RCV1	Data Receive Path for *input* or *idle* message	17.3.2	MDI ORD circuit to repeater unit	M	Yes [ ]
RCV2	Optical to Electrical conversion	17.3.2	15.2.2.3	M	Yes [ ]

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17.5.6.12 Data receive function

Item	Feature	Subclause	Value/comment	Status	Support
DR1	Bits of information received from ORD MDI and not passed to repeater	17.3.2.1	None	M	Yes [ ]
DR2	Bits of information passed to repeater other than those received from ORD MDI	17.3.2.1	None	M	Yes [ ]
DR3	Signals detected as *ORD_invalid_data*	17.3.2.1	Signals with transitions not meeting 17.2.4 requirements	M	Yes [ ]
DR4	Action when CD0 or CD1 is received on ORD MDI	17.3.2.1	Send *input* message to repeater	M	Yes [ ]
DR5	Maximum start-up and steady-state delay	17.3.2.1	2 BT from reception on MDI to *input* message	M	Yes [ ]
DR6	Action when *ORD_invalid_data* message is received	17.3.2.1	Prevent data transmission	M	Yes [ ]

17.5.6.13 Remote status message handling

Item	Feature	Subclause	Value/comment	Status	Support
RSM1	Action when SIDL or RF is received on ORD MDI	17.3.2.2	Send *input_idle* message to repeater	M	Yes [ ]
RSM2	Action when RF is received on ORD MDI	17.3.2.2	Prevent data transmission	M	Yes [ ]
RSM3	Action when *ORD_remote_fault* or *ORD_invalid_data* is received	17.3.2.2	Prevent *output* message from the repeater	M	Yes [ ]

17.5.6.14 Collision function requirements

Item	Feature	Subclause	Value/comment	Status	Support
CF1	Collision Detected	17.3.3.1	Simultaneous occurrence of *output* and *ORD_input*.	M	Yes [ ]
CF2	Action when collision detected	17.3.3.1	Send *signal_quality_error* to repeater within 3.5 BT	M	Yes [ ]

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17.5.6.15 End of collision

Item	Feature	Subclause	Value/comment	Status	Support
EOC1	End of collision determination	17.3.3.2	*OTD_sync_idle* or messages other than *ORD_input* received from ORD circuit	M	Yes [ ]
EOC2	Action when end of collision is detected	17.3.3.2	Send *mau_available* message and idle message to repeater within 5 BT	M	Yes [ ]

17.5.6.16 Loopback function

Item	Feature	Subclause	Value/comment	Status	Support
LP1	MAU transmitting on OTD and not receiving *ORD_input* message on the ORD circuit	17.3.4	Transmit *output* messages as *input* messages or transmit *output_idle* messages as *input_idle* messages	M	Yes [ ]
LP2	Steady-state propagation delay	17.3.4	≤ 2 BT	M	Yes [ ]

17.5.6.17 Fault-handling function

Item	Feature	Subclause	Value/comment	Status	Support
FH1	Types of faults detected	17.3.5	Local and remote	M	Yes [ ]
FH2	Signal at OTD MDI for different fault conditions	17.3.5	See 17.3.5	M	Yes [ ]
FH3	Action during reception of remote fault signals	17.3.5	Transmit SIDL unless local fault detected	M	Yes [ ]

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17.5.6.18 Jabber-handling function

Item	Feature	Subclause	Value/comment	Status	Support
JAB1	Sending of *input* message to repeater during jabber	17.3.6	Inhibit	M	Yes [ ]
JAB2	Transmission of *OTD_sync_idle* during jabber	17.3.6	Disabled	M	Yes [ ]
JAB3	rcv_max_timer	17.3.6	8 ms min., 12 ms max.	M	Yes [ ]
JAB4	Message sent to repeater during jabber	17.3.6	signal_quality error	M	Yes [ ]
JAB5	Receive unjabber timer duration	17.3.6	0.5 s ± 0.25 s	M	Yes [ ]
JAB6	Detection of jabber	17.3.6	Reception ≥ rcv_max_timer	M	Yes [ ]
JAB7	MAU self-interrupt	17.3.6	As in Figure 17–3	M	Yes [ ]
JAB8	Message sent to OTD MDI during jabber	17.3.6	OTD_remote_fault	M	Yes [ ]
JAB9	Message sent to OTD MDI on power reset or after rcv_unjab_timer	17.3.6	OTD_sync_idle	M	Yes [ ]

17.5.6.19 Low light detection

Item	Feature	Subclause	Value/comment	Status	Support
LLD1	Low light detection	17.3.7	Interrupt reception of signals from ORD MDI when receive optical power does not support BER of 1 part in 10^{10} for between 30 BT and 2000 BT	M	Yes [ ]
LLD2	Low light not detected	17.3.7	Average receive optical power > –32.5 dBm for 0.5 MHz to 25 MHz frequency band	M	Yes [ ]
LLD3	End of low light	17.3.7	Resume reception of signals from ORD MDI when receive optical power is more than needed to support BER of 1 part in 10^{10}	M	Yes [ ]
LLD4	State of Data Receive	17.3.7	Disabled	M	Yes [ ]
LLD5	State of Data Transmit	17.3.7	Disabled	M	Yes [ ]
LLD6	Signal sent on OTD MDI during low light	17.3.7	RF	M	Yes [ ]
LLD7	Low light state exit timer	17.3.7	0.5 s ± 0.25 s	M	Yes [ ]

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17.5.6.20 Synchronous qualification

Item	Feature	Subclause	Value/comment	Status	Support
SQ1	Condition for interrupt of reception at MDI	17.3.8	When reliable reception cannot be assured	M	Yes [ ]
SQ2	Synchronous signaling qualification	17.3.8	SIDL or RF detected for the duration of a period between 64 BT and 128 BT of clock recovery valid	M	Yes [ ]
SQ3	Action on successful synchronous signaling qualification	17.3.8	Data Transmit = enabled Data Receive = enabled	M	Yes [ ]
SQ4	Action on loss of synchronous signaling qualification	17.3.8	Data Transmit = disabled Data Receive = disabled *OTD_remote_fault* sent on MDI	M	Yes [ ]
SQ5	Clock recovery jitter tolerance	17.3.8	As in 15.2.2.1	M	Yes [ ]
SQ6	*lock_lost* not true	17.3.8	As in 15.2.2	M	Yes [ ]
SQ7	*lock_lost* true	17.3.8	Within 20 μs when input frequency on ORD $\geq$ 15.5 MHz or $\leq$ 1.55 MHz	M	Yes [ ]

17.5.6.21 MAU state diagram requirements

Item	Feature	Subclause	Value/comment	Status	Support
SD1	Synchronous Qualification function state diagram	17.3.10	Meets requirements of Figure 17–2	M	Yes [ ]
SD2	Receive Jabber function state diagram	17.3.10	Meets requirements of Figure 17–3	M	Yes [ ]
SD3	MAU Transmit, Receive, Loopback and Collision Presence Functions state diagram	17.3.10	Meets requirements of Figure 17–4	M	Yes [ ]

17.5.6.22 MAU reliability

Item	Feature	Subclause	Value/comment	Status	Support
MR1	Mean Time Before Failure	15.4	$> 10^7$ hours without causing communications failure among other stations	M	Yes [ ]

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17.5.6.23 PLS–PMA requirements

Item	Feature	Subclause	Value/comment	Status	Support
PMA1	Messages between PLS in Repeater and PMA	15.5.4	As in 7.2.1	M	Yes [ ]

17.5.6.24 *signal_quality_error* message (SQE)

Item	Feature	Subclause	Value/comment	Status	Support
SQE1	Local MAU transmitting and no collision or fault detected	15.5.4.2.1	*MAU_available* message sent to repeater	M	Yes [ ]
SQE2	Whenever a collision exists as described in 17.3.3	15.5.4.2.1	*signal_quality_error* message sent to repeater	M	Yes [ ]
SQE3	Message sent in the absence of SQE	15.5.4.2.1	*MAU_available* message	M	Yes [ ]

17.5.6.25 Environmental requirements

Item	Feature	Subclause	Value/comment	Status	Support
E1	Ambient plane wave field in which MAU meets specification	15.6.2	2 V/m from 10 kHz to 30 MHz. 5 V/m from 30 MHz to 1 GHz.	M	Yes [ ]
E2	Electromagnetic emissions and susceptibility	15.6.2	Comply with local and/or national requirements. If none exist, comply with CISPR 22: 1993.	M	Yes [ ]

17.5.6.26 MAU labeling

Item	Feature	Subclause	Value/comment	Status	Support
LBL1	MAU Type	15.7	10BASE-FB	O	Yes [ ] No [ ]
LBL2	Data Rate	15.7	10 Mb/s	O	Yes [ ] No [ ]
LBL3	Safety Warnings	15.7	Any applicable	O	Yes [ ] No [ ]
LBL4	Port Labeling	15.7	Input and output	O	Yes [ ] No [ ]

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18. Fiber optic medium attachment unit, type 10BASE-FL

18.1 Scope

18.1.1 Overview

This clause, along with Clause 15, defines the functional, electrical, optical, and mechanical characteristics of a fiber optic link for interconnecting DTEs and repeaters. The relationship of this specification to the entire ISO/IEC 8802-3 LAN International Standard is shown in Figure 15-1c). This link, which may be interconnected to other 10 Mb/s baseband segments using repeaters, consists of a 10BASE-FL MAU (including a fiber optic MDI specified in 15.2), and the fiber optic medium specified in 15.3. The purpose of the MAU is to provide a simple, inexpensive, and flexible means of attaching devices to the LAN medium.

18.1.1.1 10BASE-FL medium attachment unit (MAU)

The 10BASE-FL MAU has the following general characteristics:

a) It enables coupling the PLS by way of the AUI to the baseband fiber link defined in Clause 15.
b) It supports message traffic at a data rate of 10 Mb/s.
c) It provides for operating over 0 to at least 2000 m of the fiber optic cable specified in 15.3 without the use of a repeater.
d) It permits the DTE or repeater to confirm operation of the MAU and availability of the medium.
e) It supports network configurations using the CSMA/CD access method defined in ISO/IEC 8802-3 with baseband signaling.
f) It supports a point-to-point interconnection between MAUs and, when used with repeaters having multiple ports, supports a star wiring topology.
g) It allows incorporation of the MAU within the physical bounds of a DTE or repeater.

18.1.1.2 Repeater unit

The repeater unit is used to extend the physical system topology and provides for coupling two or more segments. Repeaters are an integral part of all 10BASE-FL networks with more than two DTEs (see Figures 13–1 and 13–2). The repeater unit is defined in Clause 9. Multiple repeater units are permitted within a single collision domain to provide the maximum connection path length specified in Clause 13. The repeater unit is not a DTE and therefore has slightly different requirements for its attached MAUs as defined in 9.4.1. It is recommended that repeater sets with 10BASE-FL MAUs provide the Auto Partition/Reconnection algorithm on those ports as specified in 9.6.6.2.

18.2 PMA interface messages

The messages between the PLS in the DTE and the PMA in the MAU shall comply with the PMA interface messages described in 7.2.1. These messages also are used in repeater unit to PMA communication. The messages between the PMA and the PLS in the DTE are specified in 15.5.4.1 and 15.5.4.2. These messages are also used in repeater unit to PMA communications. The messages between the PMAs and the fiber optic link segment are summarized in the following subclauses.

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18.2.1 PMA to fiber optic link segment messages

The following messages can be sent by the MAU PMA to the Fiber Optic Link Segment:

Message	Circuit	Signal	Meaning
OTD_output	OTD	CD1, CD0	Output information
OTD_idle	OTD	OPT_IDL	No information to output

18.2.1.1 *OTD_output.*

The PMA sublayer sends the *OTD_output* message to the OTD (Optical Transmit Data) circuit when the DTE or repeater outputs a bit of data, the MAU is available and is in the link test pass state. The physical realization of the *OTD_output* message shall be a CD0 or CD1 signal sent by the PMA. The encoding for CD1 and CD0 is the same as used on the AUI. Retiming of the CD1 and CD0 signals within the MAU is neither prohibited nor required.

18.2.1.2 OTD_idle

The PMA sublayer sends the *OTD_idle* message to the OTD circuit when the DTE or repeater sends idle; or upon detection of jabber or link integrity test failure. The physical realization of the *OTD_idle* message shall be the OPT_IDL defined in 18.3.1.1.

18.2.2 Fiber optic link segment to PMA messages

The following messages can be received by the MAU PMA from the Fiber Optic Link Segment:

Message	Circuit	Signal	Meaning
ORD_input	ORD	CD1, CD0	Input information
ORD_idle	ORD	OPT_ILD	No information to input

18.2.2.1 ORD_input

When the PMA sublayer receives the *ORD_input* message on its ORD (Optical Receive Data) circuit, it detects a bit of data. The physical realization of the *ORD_input* message shall be a CD0 or CD1 signal.

18.2.2.2 ORD_idle

When the PMA sublayer receives the *ORD_idle* message on its ORD circuit, it detects idle. The physical realization of the *ORD_idle* message shall be the OPT_IDL signal defined in 18.3.1.1.

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18.2.3 Interface message time references

Delay and bit loss specifications are measured from the occurrence of messages at the MDI and MAU AUI. A "positive-going" transition is from LO to HI. The following describes the point where each message starts:

Message	Reference
output	leading bit cell boundary (BCB) of first valid CD1 or CD0
output_idle	last positive-going transition prior to start of IDL
input	leading BCB of first valid CD1 or CD0
input_idle	last positive-going transition prior to start of IDL
signal_quality_error	first transition of valid amplitude
mau_available	last positive-going transition prior to start of IDL
OTD_output	leading BCB of first valid CD1 or CD0
OTD_idle	last positive going_transition prior to start of OPT_IDL
ORD_output	leading BCB of first valid CD1 or CD0
ORD_idle	last posititve-going transition prior to start of OPT_IDL

18.3 MAU functional specifications

The MAU provides the means by which signals on the three AUI signal circuits to and from the DTE or repeater and their associated interlayer messages are coupled to the fiber optic link segment. The MAU provides the following functional capabilities to handle message flow between the DTE or repeater and the fiber optic link segment:

a) Transmit function. Provides the ability to transfer Manchester-encoded data from the DO circuit to the OTD circuit. While not sending Manchester-encoded data on the OTD circuit, an idle signal, OPT_IDL, is sent on the OTD circuit.
b) Receive function. Provides the ability to transfer Manchester-encoded data from the ORD circuit to the DI circuit. While not sending Manchester-encoded data on the DI circuit, an idle signal, IDL, is sent on the DI circuit.
c) Loopback function (half duplex mode only). Provides the ability to transfer Manchester-encoded data from the DO to the DI circuit when the MAU is sending Manchester-encoded data to the OTD circuit.
d) Collision Presence function. Provides the ability to detect simultaneous occurrence of Manchester-encoded data on the ORD and DO circuits and to report such an occurrence as a collision.
e) *signal_quality_error* Message (SQE) Test function. Provides the ability to indicate to the DTE that the Collision Presence function is operational and that the *signal_quality_error* message can be sent by the MAU.
f) Jabber function. Provides the ability to prevent abnormally long reception of Manchester-encoded data on the DO circuit from indefinitely disrupting transmission on the network. While such a condition is present, transfer of Manchester-encoded data by the Transmit and Loopback functions is disabled.
g) Link Integrity Test function. Provides the ability to protect the network from the consequences of failure of the simplex link attached to the ORD circuit. While such a failure is present, transfer of Manchester-encoded data by the Transmit, Receive, and Loopback functions is disabled.

18.3.1 MAU functions

The MAU shall provide the Transmit, Receive, Loopback, Collision Presence, Jabber, and Link Integrity Test functions for half duplex mode DTEs and repeater units. The MAU shall provide the Transmit, Receive,

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Jabber, and Link Integrity Test functions, and shall not provide the Loopback function, for full duplex mode DTEs. The SQE Test function shall be performed by MAUs that are connected to half duplex DTEs and shall not be performed by MAUs that are connected to repeaters.

MAUs connected to full duplex mode DTEs are permitted, but not required, to implement the Collision Presence function, the SQE Test function, and the generation of the CS0 signal on the CI circuit by the Jabber function. If these optional capabilities are implemented in a MAU connected to a full duplex mode DTE, either all of the optional functions shall be implemented, or none of them shall be.

The MAU function requirements are summarized in the table below:

MAU connected to:			
Function	**Repeater**	**Half duplex DTE**	**Full duplex DTE**
Transmit	Required	Required	Required
Receive	Required	Required	Required
Loopback	Required	Required	Prohibited
Jabber	Required	Required	Required
Link Integrity Test	Required	Required	Required
Collision Presence	Required	Required	Optional (note 2)
SQE Test	Prohibited	Required	Optional (note 2)
Generation of CS0 signal on the CI circuit by Jabber	Required	Required	Optional (note 2)

NOTE 1—The functional requirements of a MAU connected to a full duplex DTE are a proper subset of the requirements for half duplex operation.
NOTE 2—Optional capabilities, if implemented, must be implemented as a group (i.e., all or none).

A capability may be provided in the MAU to activate or inhibit the SQE Test function or to configure the MAU for full or half duplex operation. It is not required that a MAU determine that it is connected to either a DTE or a repeater and automatically activate or inhibit the SQE Test function. It is also not required that a MAU determine that it is connected to either a half duplex or full duplex DTE and automatically activate or inhibit the appropriate functions for those modes.

18.3.1.1 Transmit function requirements

The MAU shall receive messages on the DO circuit and send the appropriate signals to the OTD circuit of the MDI.

At the start of a packet transmission, no more than 2 bits shall be received from the DO circuit and not transmitted on the OTD circuit. In addition, it is permissible for the first bit sent to contain phase violations or invalid amplitude. All subsequent bits of the packet shall be reproduced with levels and timing meeting the specifications of 15.2.1. The second bit transmitted on the OTD circuit shall be transmitted with the correct timing and signal levels. The steady-state propagation delay between the DO circuit input and the OTD circuit shall not exceed 2.0 BT.

For any two packets that are separated by 9.6 ms or less, the start-up delay (bit loss plus steady-state propagation delay) of the first packet shall not exceed that of the second packet by more than 2.0 BT.

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Whenever data is not being transmitted on the OTD circuit, an idle signal, OPT_IDL, shall be transmitted on the OTD circuit. OPT_IDL consists of a start of idle (4 BT to 21 BT of the lower light level) followed by a periodic pulse waveform of frequency 1 MHz +25%, –15%. Following a packet and the start of idle, the periodic pulse wave form shall start with a transition to the higher optical light level.

Transmission of OPT_IDL may be terminated at any time with respect to the periodic pulse waveform. It shall be terminated such that no more than the first transmitted bit of a packet is corrupted, and with no more delay than is specified for bit loss and steady-state propagation.

18.3.1.2 Receive function requirements

The MAU shall receive the signals on the ORD circuit of the MDI and send the appropriate message to the DI circuit. The optical-to-electrical conversion shall be as specified in 15.2.2.3.

At the start of a packet reception from the ORD circuit, no more than 2 bits shall be received on the ORD circuit and not transmitted onto the DI circuit. In addition, it is permissible for the first bit sent on the DI circuit to contain phase violations or invalid data; however, all successive bits of the packet shall be sent with no more than the amount of jitter specified in 15.2. The steady-state propagation delay between the ORD circuit and the DI circuit shall not exceed 2.0 BT.

For any two packets that are separated by 9.6 μs or less, the start-up delay of the first packet shall not exceed that of the second packet by more than 2.0 BT.

18.3.1.3 Loopback function requirements (half duplex mode only)

When the MAU is transmitting on the OTD circuit and is not receiving *ORD_input* messages (18.2.2.1) on the ORD circuit, the MAU shall transmit on the DI circuit the signals received on the DO circuit in order to provide loopback of the transmitted signal. At the start-of-packet transmission on the OTD circuit, no more than 5 bits of information shall be received from the DO circuit and not transmitted to the DI circuit. In addition, it is permissible for the first bit sent on the DI circuit to contain phase violations or invalid data; however, all successive bits of the packet shall meet the jitter specified in 15.2. The steady-state propagation delay between the DO circuit and the DI circuit shall not exceed 1.0 BT.

18.3.1.4 Collision Presence function requirements (half duplex mode only)

The MAU shall detect as a collision the simultaneous occurrence of activity on the DO circuit and the ORD circuit while in the Link Test Pass state. While a collision is detected, a CS0 signal (see 7.3.1.2) shall be sent on the CI circuit. The signal shall be presented to the CI circuit no more than 3.5 BT after the occurrence of a collision. The signal shall be de-asserted within 7.0 BT after the DO circuit or the ORD circuit changes from active to idle.

When CS0 is asserted on the CI circuit due to a collision, the data on the ORD circuit shall be sent to the DI circuit within 9.0 BT.

When the ORD circuit changes from active to idle and data is present on the DO circuit, the data on the DO circuit shall be sent to the DI circuit within 7.0 BT.

The signal presented on the CI circuit in the absence of collision, SQE test, or Jabber shall be the IDL signal.

MAUs connected to full duplex mode DTEs are permitted, but not required, to implement the Collision Presence function (see 18.3.1).

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18.3.1.5 *signal_quality_error* Message (SQE) Test function requirements

The SQE Test function shall be performed by MAUs that are connected to DTEs and shall not be performed by MAUs that are connected to repeaters. When the SQE test is performed, the MAU shall send CS0 on the CI circuit for a time "SQE_test" beginning a time "SQE_test_wait" after the last positive transition of a packet on the DO circuit. The value of "SQE_test" shall be 10 ±5 BT and the value of "SQE_test_wait" shall be between 0.6 and 1.6 μs. This function should use as much of the normal collision detection and signaling circuitry as possible without introducing extraneous signals on the OTD circuit or the DI circuit.

The CS0 signal shall not be sent by the SQE Test function while in any of the Link Test Fail states.

MAUs connected to full duplex mode DTEs are permitted, but not required to implement the SQE Test function (see 18.3.1).

18.3.1.6 Jabber function requirements

The MAU shall contain a self-interrupt capability to prevent an illegally long transmission by a DTE from permanently disrupting transmission on the network and to disable loopback to the DI circuit (Figure 18–3). The MAU shall provide a window "xmit_max" during which time the Transmit function may continuously transmit *OTD_output* messages to the OTD circuit. The value of "xmit_max" shall be between 20 and 150 ms. If a transmission exceeds this duration, the Jabber function shall

a) Inhibit the Loopback function and the transmission of *OTD_output* messages by the Transmit function, and shall
b) Send the CS0 signal on the CI circuit, when the MAU is connected to a DTE operating in half duplex mode. MAUs connected to DTEs operating in full duplex mode are permitted, but not required, to send the CS0 signal on the CI circuit in this manner (see 18.3.1).

These actions shall continue until *output_idle* has been continuously present on the DO circuit for a time "unjab." The value of "unjab" shall be 0.5 ± 0.25 s.

It is permissible to activate the Jabber function when the OTD circuit transmitter is sending *OTD_output* messages for longer than "xmit_max."

The MAU shall not activate its Jabber function when the repeater's MAU Jabber Lockup Protection function operates at its longest permitted time as specified in 9.6.5.

18.3.1.7 Link Integrity Test function requirements

In order to protect the network from the consequences of a simplex fiber optic link segment failure, the MAU shall monitor the light level on the ORD circuit. When a light level below that required for reliable reception (low light) is detected, the MAU shall enter the Link Test Fail Low Light state and cause the *input_idle* message to be sent on the DI circuit and the *OTD_idle* message to be sent on the OTD circuit (Figure 18–4).

Low light shall not be detected if the optical power level at the ORD circuit exceeds –32.5 dBm. Low light shall also not be detected if the low light condition remains for less than 30 BT. It shall be detected and the Link Test Fail Low Light state entered if the optical power level at ORD circuit has fallen to a level lower than the optical power level that corresponds to a BER = 10^{-10} for the MAU for a duration of 2000 BT. Additionally, when the optical receive average power has maintained a value less than –30 dBm for 2000 BT and then falls lower than the level that corresponds to a BER = 10^{-10} for the MAU for a duration of 500 BT, low light shall be detected and the Link Test Fail Low Light state entered.

The MAU shall exit the Link Test Fail Low Light state once the optical power level on the ORD circuit exceeds –32.5 dBm for 0.5 s ±0.25 s. Exiting the Link Test Fail Extend state and entering the Link Test Pass state (thus,

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re-enabling the OTD and DI circuits) shall be deferred until the signals on the ORD and DO circuits become idle. Optionally, a MAU may exit the Link Test Fail Extend state and enter the Link Test Pass state when the ORD circuit becomes idle and the Jabber function has disabled transmission on the OTD circuit.

While the MAU is not in the Link Test Pass state, the Link Integrity Test function shall disable the bit transfer of the Transmit, Receive, and Loopback functions, and the Collision Presence and SQE Test functions.

At power-on, in place of entering the Link Test Pass state as shown in Figure 18–4,[32] a MAU may optionally enter the Link Test Fail Low Light state.

If a visible indicator is provided on the MAU to indicate the link status, it is recommended that the color be green and that the indicator be labeled appropriately. It is further recommended that the indicator be on when the MAU is in the Link Test Pass state and off otherwise.

18.3.1.8 Auto-Negotiation

The Auto-Negotiation algorithm of Clause 28, while the preferred method for the determination of half or full duplex operation, is not currently defined for fiber MAUs.

Manual configuration, while not recommended for copper-based MAUs, is the only practical choice for fiber implementations. Connecting incompatible DTE/MAU combinations such as a full duplex mode DTE to a half duplex mode MAU, or a full duplex mode station (DTE and MAU) to a half duplex network, can lead to severe network performance degradation, increased collisions, late collisions, CRC errors, and undetected data corruption.

18.3.2 MAU state diagrams

The state diagrams of Figures 18–1a), 18–1b), 18–2, 18–3, and 18–4 depict the full set of allowed MAU state functions relative to the circuits of the AUI and MDI.

The notation used in the state diagrams follows the conventions in 1.2.1. The variables and timers used in the state diagrams are defined in the following subclauses.

18.3.2.1 MAU state diagram variables

Variables are used in the state diagrams to indicate the status of MAU inputs and outputs, to control MAU operation, and to pass state information between functions.

In the variable definitions, the name of the variable is followed by a brief description of the variable and a list of values the variable may take. For those variables which are state diagram outputs, one value will be identified as the default. The variable has the default value when no active state contains a term assigning a different value.

For example, the variable “xmit” has the value “disable” whenever the Jabber function or the Link Integrity Test function is in a state that asserts “xmit=disable”. The variable has the default value “enable” all other times.

[32]The MAU state diagrams, Figures 18–1 through 18–4, follow 18.3.2.2.

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The variables used in the state diagrams are defined as follows:

DI

Controls the signal sent by the MAU on the DI circuit.
Values: idle; MAU is sending *input_idle*, IDL (default).
DO; MAU sends the signal received on the DO circuit.
lpbk = disable overrides this and causes *input_idle* to be sent.
ORD; MAU sends the signal received on the ORD circuit.
rcv = disable overrides this and causes *input_idle* to be sent.

CI

Controls the signal sent by the MAU on the CI circuit.
Values: idle; MAU sends *mau_available*, IDL (default).
SQE; MAU sends *signal_quality_error*, CS0.

DO

Status of the signal received by the MAU on the DO circuit.
Values: idle; MAU is receiving *output_idle*, IDL.
active; MAU is receiving *output*, CD0 or CD1.

OTD

Controls the signal sent by the MAU on the OTD circuit.
Values: idle; MAU sends *OTD_idle*, OPT_IDL (default).
DO; MAU sends the signal received on the DO circuit.
xmit = disable overrides this and causes *OTD_idle* to be sent.

ORD

Status of the signal received by the MAU on the ORD circuit.
Values: idle; MAU is receiving *ORD_idle*; OPT_idle.
active; MAU is receiving *ORD_input*; CD0 or CD1.

low_light_level

Status of the light level received by the MAU on the ORD circuit.
Values: false; MAU is receiving sufficient light level for reliable reception.
true; MAU is not receiving sufficient light level for reliable reception (see 18.3.1.7).

rcv

Controls the path from the ORD circuit to the DI circuit.
Values: enable; receive is enabled (default).
disable; the output to the DI circuit will be input_idle when DI=ORD.

lpbk

Controls the path from the DO circuit to the DI circuit.
Values: enable; loopback is enabled (default).
disable; the output to the DI circuit will be input_idle when DI=DO.

xmit

Controls the path from the DO circuit to the OTD circuit.
Values: enable; transmit is enabled (default).
disable; transmit is disabled and the signal sent on the OTD circuit will be OPT_IDL.

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18.3.2.2 MAU state diagram timers

All timers operate in the same fashion. A timer is reset and starts counting upon entering a state where start x_timer is asserted. Time x after the timer has been started, x_timer_done is asserted and remains asserted until the timer is reset. At all other times, x_timer_not_done is asserted.

When entering a state where start x_timer is asserted, the timer is reset and restarted even if the entered state is the same as the exited state.

low_light_heal_timer. Timer for low light condition cessation.

SQE_test_timer. Timer for the duration of the CS0 signal used for the SQE Test function (18.3.1.5).

SQE_test_wait_timer. Timer for the delay from end of packet to the start of the CS0 signal used for the SQE Test function (18.3.1.5).

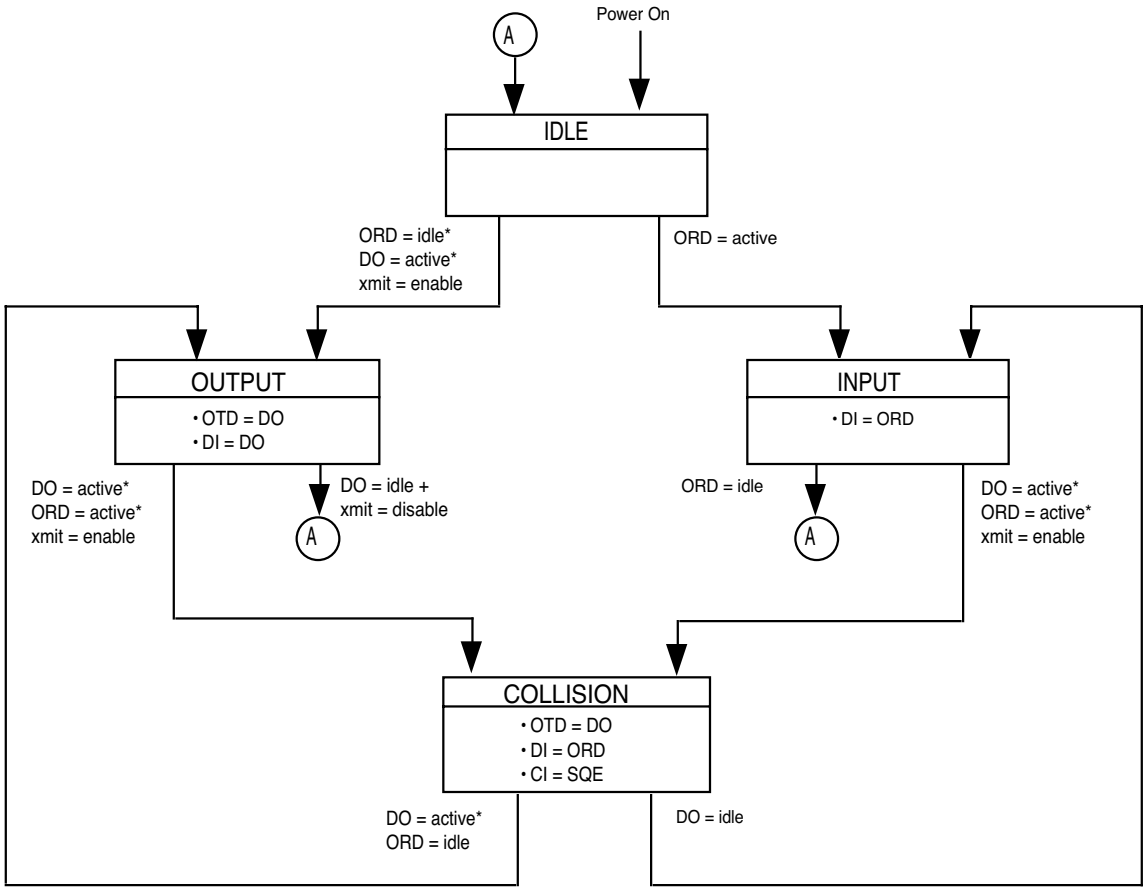
unjab_timer. Timer for the length of time the DO circuit must be continuously idle to allow transmission to be re-enabled (18.3.1.6).

xmit_max_timer. Timer for excessively long transmit time (18.3.1.6).

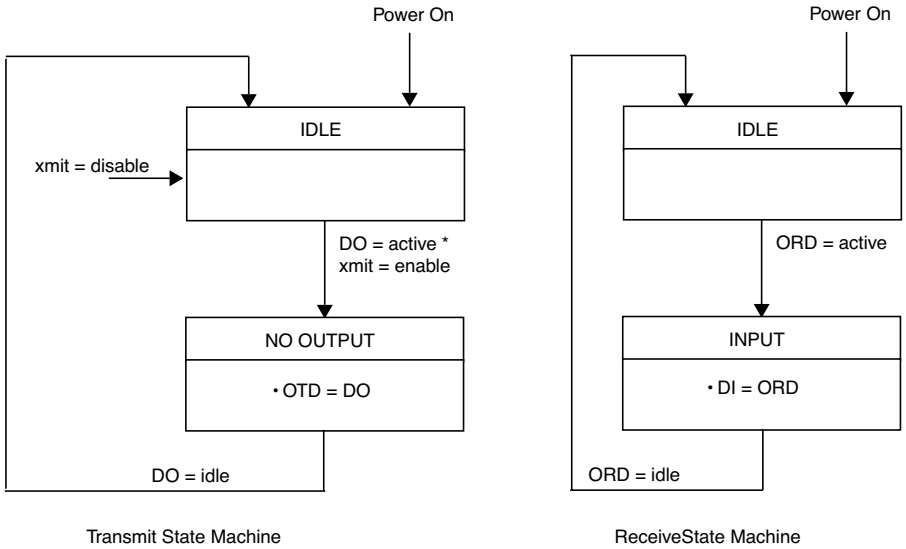
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a) MAU Transmit, Receive, Loopback, and Collision Presence functions (half duplex mode)



b) MAU Transmit and Receive functions (full duplex mode)

Figure 18–1—MAU state diagrams

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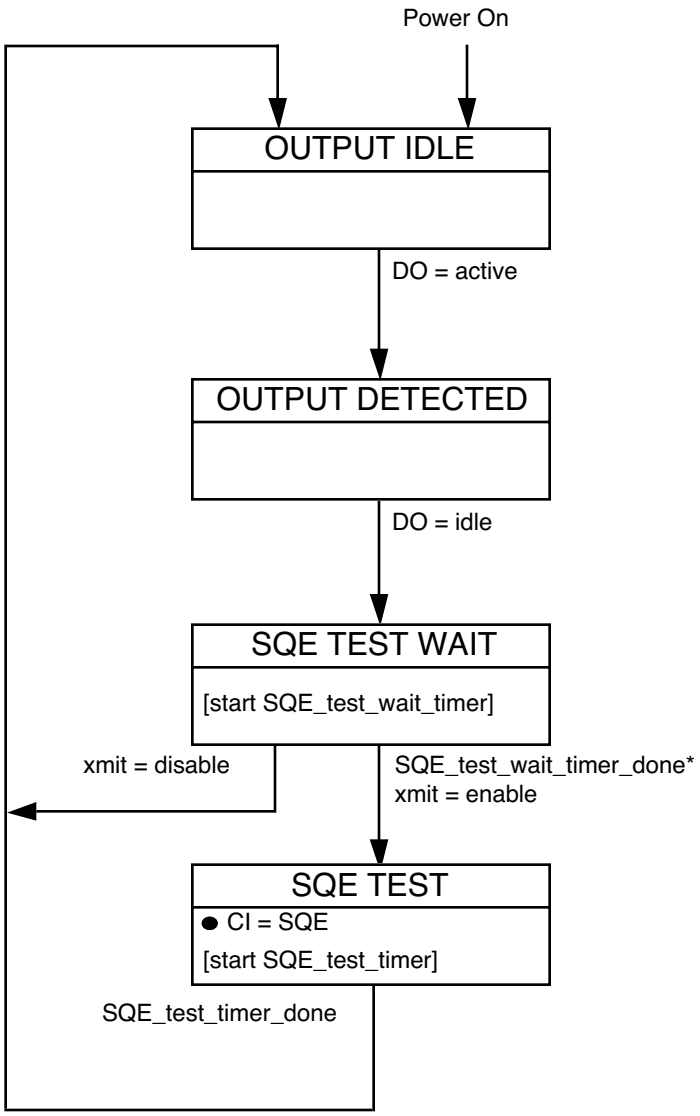
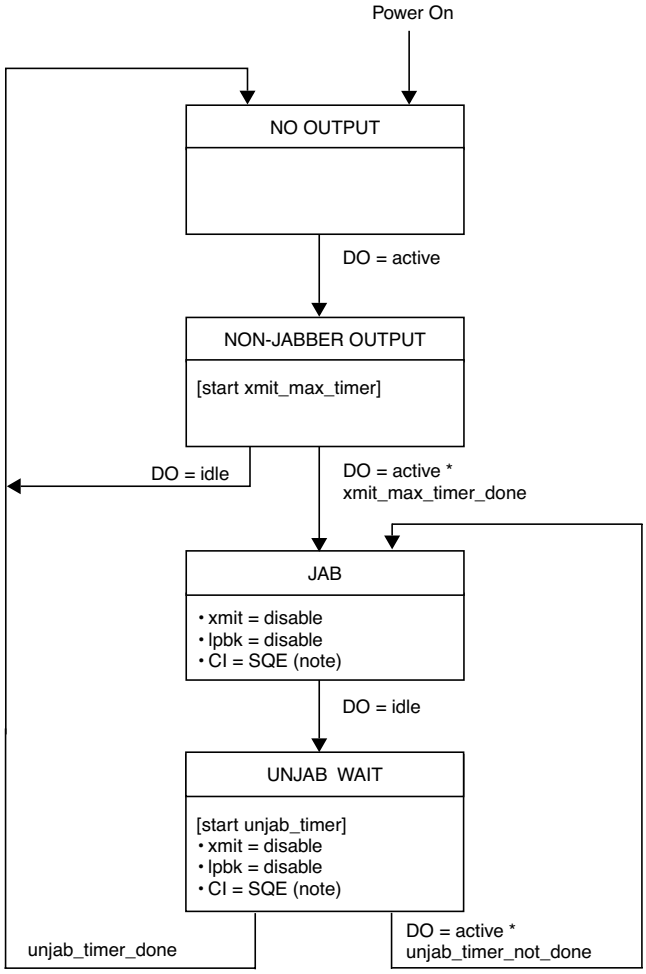


Figure 18–2—*signal_quality_error* Message Test function state diagram

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NOTES

1—Optional for MAUs connected to DTEs operating in full duplex mode.

2—The implementation of the Collision Presence function is not required in a MAU connected to a full duplex mode DTE, and is not shown in Figure 18–1b).

3—The implementation of the SQE Test function shown in Figure 18–2 is not required in a MAU connected to a full duplex mode DTE.

4—The enabling of the variable *lpbk* in Figure 18–4 is applicable in half duplex mode only.

Figure 18–3—Jabber function state diagram

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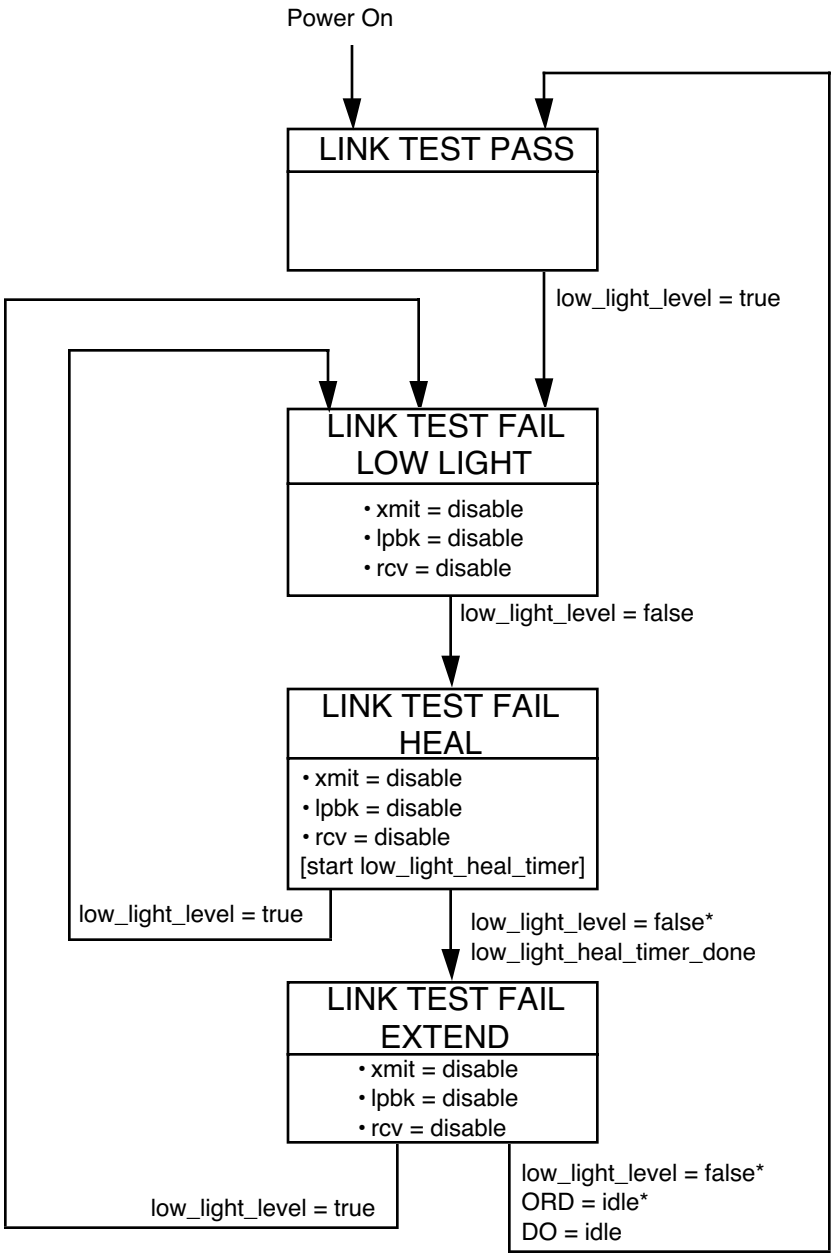


Figure 18–4—Link Integrity Test function state diagram

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18.4 Timing summary

Table 18–1 summarizes the timing requirements for the 10BASE-FL fiber link. This table is a summary; for complete descriptions of the timing requirements, refer to the referenced clauses. All times are in Bit Times.

Table 18–1—Maximum timing parameters

Symbol	Function	Bit Loss	Invalid Bits	Steady-state Prop. Delay	Start-up delay		
					Max.	/ Var	Specified in
M1	*ORD_input* to *input* on DI	2.0	1.0	2.0	5.0	2.0	18.3.1.2
M2	*output* on DO to *OTD_output*	2.0	1.0	2.0	5.0	2.0	18.3.1.1
M3	*ORD_input* **output* to *signal_quality_error*				3.5		18.3.1.4
M4	*ORD_idle* + *output_idle* (end of collision) to *mau_available*				7.0		18.3.1.4
M5	*ORD_input* **output* to *input* on DI from circuit ORD				9.0		18.3.1.4
M6	*ORD_idle* **output* to *input* on DI from circuit DO				7.0		18.3.1.4
M7	*output_idle* on DO to *signal_quality_error*				6<x<16		18.3.1.5
M8	*signal_quality_error* duration for SQE test				5≤x≥15		18.3.1.5
M9	*output* on DO to *input* on DI	5.0	1.0	1.0	7.0		18.3.1.3
F1	Fiber Optic Cable Propagation (2000 m)	0	0	100	100		15.3.1.4
A1	AUI Cable Propagation (50 m)	0	0	2.57	2.57		7.4.3.7

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18.5 Protocol implementation conformance statement (PICS) proforma for Clause 18, Fiber optic medium attachment unit, type 10BASE-FL[33]

18.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 18, Fiber optic medium attachment unit, type 10BASE-FL, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. The PICS can be used for a variety of purposes by various parties, including the following:

— As a checklist by the protocol implementor, to reduce the risk of failure to conform to the standard through oversight;
— As a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard PICS proforma, by the supplier and acquirer, or potential acquirer, of the implementation;
— As a basis for initially checking the possibility of interworking with another implementation by the user, or potential user, of the implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible PICs);
— As the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation, by a protocol tester.

18.5.2 Abbreviations and special symbols

18.5.2.1 Status symbols

The following symbols are used in the PICS proforma:

M	mandatory field/function
O	optional field/function
O.<n>	optional field/function, but at least one of the group of options labeled by the same numeral <n> is required
O/<n>	optional field/function, but one and only one of the group of options labeled by the numeral <n> is required
X	prohibited field/function
<item>:	simple-predicate condition, dependent on the support marked for <item>

18.5.2.2 Abbreviations

N/A	Not applicable

In addition, the following predicate names are defined for use when different implementations from the set above have common parameters:

*HRP : HDX or RPT
*HDS : HDX or FDS
*HFC : HDX or FDS or RPT

[33] *Copyright release for PICS Proformas:* Users of this standard may freely reproduce the PICS proforma in this clause so that it can be used for its intended purpose and may further publish the completed PICS.

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18.5.3 Instructions for completing the PICS proforma

18.5.3.1 General structure of the PICS proforma

The first part of the PICS proforma, Implementation Identification and Protocol Summary, is to be completed as indicated with the information necessary to identify fully both the supplier and the implementation.

The main part of the PICS proforma is a fixed-format questionnaire divided into subclauses, each containing a group of items. Answers to the questionnaire items are to be provided in the right-most column, either by simply marking an answer to indicate a restricted choice (usually Yes, No, or Not Applicable), or by entering a value or a set or range of values. (Note that there are some items where two or more choices from a set of possible answers can apply; all relevant choices are to be marked.)

Each item is identified by an item reference in the first column; the second column contains the question to be answered; the third column contains the reference or references to the material that specifies the item in the main body of the standard; the fourth column contains values and/or comments pertaining to the question to be answered. The remaining columns record the status of the item—whether the support is mandatory, optional, or conditional—and provide the space for the answers; see also 18.5.3.4 below.

The supplier may also provide, or be required to provide, further information, categorized as either Additional Information or Exception Information. When present, each kind of further information is to be provided in a further subclause of items labeled A<i> or X<i>, respectively, for cross-referencing purposes, where <i> is any unambiguous identification for the item (e.g., simply a numeral); there are no other restrictions on its format or presentation.

A completed PICS proforma, including any Additional Information and Exception Information, is the Protocol Implementation Conformance Statement for the implementation in question.

Note that where an implementation is capable of being configured in more than one way, according to the items listed under 18.5.5, Major Capabilities/Options, a single PICS may be able to describe all such configurations. However, the supplier has the choice of providing more than one PICS, each covering some subset of the implementation's configuration capabilities, if that would make presentation of the information easier and clearer.

18.5.3.2 Additional information

Items of Additional Information allow a supplier to provide further information intended to assist the interpretation of the PICS. It is not intended or expected that a large quantity will be supplied, and the PICS can be considered complete without any such information. Examples might be an outline of the ways in which a (single) implementation can be set up to operate in a variety of environments and configurations; or a brief rationale, based perhaps upon specific application needs, for the exclusion of features which, although optional, are nonetheless commonly present in implementations of the 10BASE-FL protocol.

References to items of Additional Information may be entered next to any answer in the questionnaire, and may be included in items of Exception Information.

18.5.3.3 Exception information

It may occasionally happen that a supplier will wish to answer an item with mandatory or prohibited status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No preprinted answer will be found in the Support column for this; instead, the supplier is required to write into the Support column an X<i> reference to an item of Exception Information, and to provide the appropriate rationale in the Exception item itself.

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An implementation for which an Exception item is required in this way does not conform to this standard.

Note that a possible reason for the situation described above is that a defect in the standard has been reported, a correction for which is expected to change the requirement not met by the implementation.

18.5.3.4 Conditional items

The PICS proforma contains a number of conditional items. These are items for which both the applicability of the item itself, and its status if it does apply—mandatory, optional, or prohibited—are dependent upon whether or not certain other items are supported.

Individual conditional items are indicated by a conditional symbol of the form "<item>:<s>" in the Status column, where "<item>" is an item reference that appears in the first column of the table for some other item, and "<s>" is a status symbol, M, O, or X.

If the item referred to by the conditional symbol is marked as supported, the conditional item is applicable, and its status is given by "<s>"; the support column is to be completed in the usual way. Otherwise, the conditional item is not relevant and the Not Applicable (N/A) answer is to be marked.

Each item whose reference is used in a conditional symbol is indicated by an asterisk in the Item column.

18.5.4 Identification

18.5.4.1 Implementation identification

Supplier	
Contact point for queries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

18.5.4.2 Protocol summary

Identification of protocol specification	IEEE Std 802.3-2002, Clause 18, Fiber optic medium attachment unit, Type 10BASE-FL
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See 17.5.3.3; The answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

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18.5.5 Major capabilities/options

Item	Feature	Subclause	Value/comment	Status	Support
*DTE	MAU supports DTE connections	15.1.1	N/A	O.1	Yes [ ] No [ ]
*RPT	MAU supports repeater connections	15.1.1	N/A	O.1	Yes [ ] No [ ]
*AUI	AUI connection physically exists and is accessible for test.	15.1.3.2	N/A	O	Yes [ ] No [ ]
*APW	AUI powers MAU	15.5.3	N/A	AUI: O.2	N/A [ ] Yes [ ] No [ ]
*SPW	AUI implemented but MAU powered separately	15.5.3	N/A	AUI: O.2	N/A [ ] Yes [ ] No [ ]
*FDX	MAU supports full duplex mode DTE connections	15.1.3.5	N/A	DTE: O.3	N/A [ ] Yes [ ] No [ ]
*HDX	MAU supports half duplex mode DTE connections	15.1.3.5	N/A	DTE: O.3	N/A [ ] Yes [ ] No [ ]
*FDS	MAU supports optional set of SQE related function for full duplex mode DTE connections	18.3.1	N/A	FDX: O	N/A [ ] Yes [ ] No [ ]

18.5.6 PICS proforma tables for the type 10BASE-FL MAU

18.5.6.1 Compatibility considerations

Item	Feature	Subclause	Value/comment	Status	Support
CC1	Compatibility Considerations: 10BASE-FL Systems compatible at 10BASE-FL MDI	15.1.3.2		M	Yes [ ]
CC2	10BASE-FL MAUs interoperable with FOIRL MAUs except for media connector	15.1.3.2		M	Yes [ ]
CC3	Mode of operation	15.1.3.5	normal mode only	M	Yes [ ]

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18.5.6.2 Optical transmit parameter

Item	Feature	Sublause	Value/comment	Status	Support
OT1	Center Wavelength	15.2.1.1	min. 800 nm; max. 910 nm	M	Yes [ ]
OT2	Spectral Width (FWHM)	15.2.1.2	< 75 nm	M	Yes [ ]
OT3	Optical Modulation Extinction Ratio	15.2.1.3	< –13 dB	M	Yes [ ]
OT4	Optical Idle Signal Amplitude	15.2.1.4	See 15.2.1.10	M	Yes [ ]
OT5	Optical Transmit Pulse Logic Polarity	15.2.1.5	High Optical Power = LO on AUI DO and MDI. Low Optical Power = HI on AUI DO and MDI.	M	Yes [ ]
	Optical Transmit Pulse Rise and Fall times	15.2.1.6	Measured from 10% to 90% level		
OT6	Max. (Data)		10.0 ns	M	Yes [ ]
OT7	Min. (Data)		0.0 ns	M	Yes [ ]
OT8	Max. Difference (Data)		3.0 ns	M	Yes [ ]
OT9	Max. (Idle)		25.0 ns	M	Yes [ ]
OT10	Min. (Idle)		0.0 ns	M	Yes [ ]
OT11	Max. Difference (Idle)		25.0 ns	M	Yes [ ]
OT12	Optical Transmit Pulse Overshoot	15.2.1.7	< 25%	M	Yes [ ]
OT13	Optical Transmit Pulse Undershoot	15.2.1.7	< 10%	M	Yes [ ]
	Optical Transmit Pulse Edge Jitter Added	15.2.1.8	Measured as in 15.2.1.8		
OT14	DO circuit to MDI		± 2.0 ns	M	Yes [ ]
OT15	Total at MDI		±4.0 ns	M	Yes [ ]
	Optical Transmit Pulse Duty Cycle Distortion	15.2.1.9	Measured at median power level		
OT16	Max. (Data)		± 2.5 ns	M	Yes [ ]
OT17	Max. (Idle)		± 50.0 ns	M	Yes [ ]
	Optical Transmit Average Power Range	15.2.1.10			
OT18	Min.		–20 dBm	M	Yes [ ]
OT19	Max.		–12 dBm	M	Yes [ ]
OT20	Transmit Signal Templates	Figure 15–5	Optical signals within template	M	Yes [ ]

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18.5.6.3 Optical receive parameters

Item	Feature	Subclause	Value/comment	Status	Support
OR1	BER between two AUIs attached to a single segment	15.2.2	< one part in 10^9	M	Yes [ ]
	Optical Receive Average Power	15.2.2.1	When a single transmitter transmits on the medium		
OR2	Min.		–32.5 dBm	M	Yes [ ]
OR3	Max.		–12.0 dBm	M	Yes [ ]
	MAU optical receive Edge Jitter (Data)	15.2.2.2	Measured as in 15.2.2.2		
OR4	Received at MDI		± 6.5 ns at median power	M	Yes [ ]
OR5	Added MDI to DI circuit		± 8.5 ns	M	Yes [ ]
OR6	Total at DI circuit (MAU end of AUI)		± 15.0 ns at zero crossing points	M	Yes [ ]
OR7	Optical Receive Pulse Logic Polarity	15.2.2.3	High Optical Power = LO on AUI DI and MDI. Low Optical Power = HI on AUI DI and MDI	M	Yes [ ]
	Optical Receive Pulse Rise and Fall Times:	15.2.2.4	Measured from 10% to 90% level		
OR8	Max. (Data)		31.5 ns	M	Yes [ ]
OR9	Min. (Data)		0.0 ns	M	Yes [ ]
OR10	Max. Difference (Data)		3.0 ns	M	Yes [ ]
OR11	Max. (Idle)		41.0 ns	M	Yes [ ]
OR12	Min. (Idle)		0.0 ns	M	Yes [ ]
OR13	Max. Difference (Idle):		25.0 ns	M	Yes [ ]

18.5.6.4 Optical medium connector plug and socket

Item	Feature	Subclause	Value/comment	Status	Support
CS1	Connector Socket for MAU	15.3.2	BFOC/2.5—see IEC 60874-10: 1992	M	Yes [ ]

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18.5.6.5 MAU functions

Item	Feature	Subclause	Value/comment	Status	Support
MF1	Transmit	18.3.1.1		M	Yes [ ]
MF2	Receive	18.3.1.2		M	Yes [ ]
MF3	Loopback	18.3.1.3		HRP: M FDX: X	N/A [ ] M: Yes [ ] N/A [ ] X:Yes [ ]
MF4	Collision Presence	18.3.1.4		HFC: M	N/A [ ] M: Yes [ ]
MF5	Jabber	18.3.1.6		M	Yes [ ]
MF6	Link Integrity Test	18.3.1.7		M	Yes [ ]
MF7	SQE Test	18.3.1.5		HDS: M RPT: X	N/A [ ] M: Yes [ ] N/A [ ] X: Yes [ ]

18.5.6.6 PMA interface messages

Item	Feature	Subclause	Value/comment	Status	Support
PIM1	Messages between the PLS in the DTE and the PMA in the MAU	18.2	As described in 7.2.1	M	Yes [ ]

18.5.6.7 PMA-to-MDI OTD messages

Item	Feature	Subclause	Value/comment	Status	Support
OTD1	Signal sent on OTD corresponding to *OTD_output* message	18.2.1.1	CD1,CD0	M	Yes [ ]
OTD2	Signal sent on OTD corresponding to *OTD_idle* message	18.2.1.2	OPT_IDL	M	Yes [ ]

18.5.6.8 MDI ORD-to-PMA messages

Item	Feature	Subclause	Value/comment	Status	Support
ORD1	Signal received on ORD corresponding to *ORD_input* message	18.2.2.1	CD1,CD0	M	Yes [ ]
ORD2	Signal received on ORD corresponding to *ORD_idle* message	18.2.2.2	OPT_IDL or signal other than valid Manchester Data	M	Yes [ ]

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18.5.6.9 Transmit function

Item	Feature	Subclause	Value/comment	Status	Support
XT1	Data Transmit path for *output* message	18.3.1.1	DO circuit to OTD circuit	M	Yes [ ]
XT2	Levels and timing of optical signal	18.3.1.1	As in 15.2.1	M	Yes [ ]
XT3	Start-up bit loss (DO to OTD circuits)	18.3.1.1	2 bits max.	M	Yes [ ]
XT4	Transmit settling time	18.3.1.1	Second and following bits meet jitter, level, and waveform specifications of 15.2.1	M	Yes [ ]
XT5	Transmit steady-state delay	18.3.1.1	2 BT max.	M	Yes [ ]
XT6	Transmit delay variability	18.3.1.1	2 BT max.	M	Yes [ ]
XT7	Signal sent on OTD corresponding to OPT_IDL message	18.3.1.1	Start of idle followed by a periodic pulse waveform	M	Yes [ ]
XT8	Periodic pulse waveform	18.3.1.1	1 MHz +25%, –15%	M	Yes [ ]
XT9	OPT_IDL termination with respect to start of packet	18.3.1.1	Normal start-of-packet requirement apply	M	Yes [ ]

18.5.6.10 Receive function

Item	Feature	Subclause	Value/comment	Status	Support
RCV1	Optical to electrical	18.3.1.2	As specified in 15.2.2.3	M	Yes [ ]
RCV2	Receive path	18.3.1.2	ORD circuit to DI circuit	M	Yes [ ]
RCV3	Start-up bit loss (ORD to DI circuits)	18.3.1.2	2 bits max.	M	Yes [ ]
RCV4	Receive settling time	18.3.1.2	Second and following bits meet jitter specifications of 15.2	M	Yes [ ]
RCV5	Receive steady-state delay	18.3.1.2	2 BT max.	M	Yes [ ]
RCV6	Receive delay variability	18.3.1.2	2 BT max.	M	Yes [ ]

18.5.6.11 Loopback function

Item	Feature	Subclause	Value/comment	Status	Support
LP1	Loopback function requirements when ORD = idle and DO = active	18.3.1.3	DO signals to DI circuit.	HRP: M	N/A [ ] M: Yes [ ]
LP2	Loopback bit loss (DO to DI circuits)	18.3.1.3	5 bits max	HRP: M	N/A [ ] M: Yes [ ]
LP3	Loopback settling time	18.3.1.3	Second and following bits meet jitter specifications.	HRP: M	N/A [ ] M: Yes [ ]
LP4	Loopback steady-state delay	18.3.1.3	1 BT max	HRP: M	N/A [ ] M: Yes [ ]

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18.5.6.12 Collision Presence function

Item	Feature	Subclause	Value/comment	Status	Support
CP1	Collision Presence function requirements	18.3.1.4	CS0 on CI circuit if DO=active, ORD=active and in Link Test Pass state.	HFC: M	N/A [ ] M: Yes [ ]
CP2	Collision indication delay	18.3.1.4	3.5 BT max.	HFC: M	N/A [ ] M: Yes [ ]
CP3	Collision indicate deassert delay	18.3.1.4	7 BT max.	HFC: M	N/A [ ] M: Yes [ ]
CP4	CI circuit with no collision, SQE Test, or jabber	18.3.1.4	IDL signal	HFC: M	N/A [ ] M: Yes [ ]
CP5	DI circuit source switch delay from CS0 assert	18.3.1.4	9 BT max.	HFC: M	N/A [ ] M: Yes [ ]
CP6	DI circuit source switch delay from CS0 deassert	18.3.1.4	7 BT max.	HFC: M	N/A [ ] M: Yes [ ]

18.5.6.13 *signal_quality_error* Message (SQE) Test function

Item	Feature	Subclause	Value/comment	Status	Support
STF1	SQE Test induced OTD or DI circuit signals	18.3.1.5	No extraneous signals permitted	HDS: M	N/A [ ] M: Yes [ ]
STF2	SQE_test_wait timer range	18.3.1.5	0.6 to 1.6 μs	HDS: M	N/A [ ] M: Yes [ ]
STF3	SQE_test timer range	18.3.1.5	5 to 15 BT	HDS: M	N/A [ ] M: Yes [ ]
STF4	CI circuit during SQE Test	18.3.1.5	CS0 signal	HDS: M	N/A [ ] M: Yes [ ]
STF5	SQE Test in Link Fail states	18.3.1.5	CS0 must not be sent	HDS: M	N/A [ ] M: Yes [ ]

18.5.6.14 Jabber function

Item	Feature	Subclause	Value/comment	Status	Support
JAB1	Jabber function implementation	18.3.1.6	Self-interrupt of transmit and loopback.	M	Yes [ ]
JAB2	Xmit_max. timer range	18.3.1.6	20 ms min., 150 ms max.	M	Yes [ ]
JAB3	CI circuit during jabber	18.3.1.6	CS0 signal	HFC: M	N/A [ ] M: Yes [ ]
JAB4	Unjab timer range	18.3.1.6	0.5 ± 0.25 s	M	Yes [ ]
JAB5	MAU Jabber Lockup Protection	18.3.1.6	Jabber not activated by the longest permitted output specified in 9.6.5	M	Yes [ ]

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18.5.6.15 Link Integrity Test function

Item	Feature	Subclause	Value/comment	Status	Support
LI1	Low light detected	18.3.1.7	ORD optical power does not support a BER of 10^{-10} for a duration of 2000 BT, or ORD optical power is < –30 dBm for 2000 BT and does not support a BER of 10^{-10} for a duration of 500 BT	M	Yes [ ]
LI2	Low light not detected	18.3.1.7	ORD optical power exceeds –32.5 dBm or low light condition remains < 30 BT	M	Yes [ ]
	Signals during detected failure	18.3.1.7			
LI3	OTD circuit		OPT_IDL	M	Yes [ ]
LI4	DI circuit		IDL	M	Yes [ ]
LI5	CI circuit		IDL (except when jabber condition is also present)	M	Yes [ ]
LI6	Link Test Fail state exit conditions	18.3.1.7	ORD optical power exceeds –32.5 dBm for 0.5 ± 0.25 s	M	Yes [ ]
	Link fail effect on MAU functions	18.3.1.7			
LI7	Transmit		Disable	M	Yes [ ]
LI8	Receive		Disable	M	Yes [ ]
LI9	Loopback		Disable	M	Yes [ ]
LI10	Collision Presence		Disable	M	Yes [ ]
LI11	SQE Test		Disable	M	Yes [ ]
LI12	Link Test Fail Extend state exit condition	18.3.1.7	Deferred until ORD = idle and DO = idle	M	Yes [ ]
LI13	Power-on state	18.3.1.7	Link Test Fail Low Light	O	Yes [ ] No [ ]
LI14	Link status indicator	18.3.1.7	Color=green on=Link Test Pass	O	Yes [ ] No [ ]

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18.5.6.16 MAU state diagram requirements

Item	Feature	Subclause	Value/comment	Status	Support
SD1	Full duplex mode MAU Transmit and Receive functions state diagram	18.3.2	Meets requirements of Figure 18–1b)	FDX: M	N/A [ ] M: Yes [ ]
SD2	Half duplex Transmit, Receive, Loopback, and Collision Presence functions state diagrams	18.3.2	Meets requirements of Figure 18–1a)	HFC:M	N/A [ ] M: Yes [ ]
SD3	*signal_quality_error* Message Test function state diagram	18.3.2	Meets requirements of Figure 18–2	HDS: M	N/A [ ] M: Yes [ ]
SD4	Jabber function state diagram	18.3.2	Meets requirements of Figure 18–3	M	Yes [ ]
SD5	Link Integrity Test function state diagram	18.3.2	Meets requirements of Figure 18–4	M	Yes [ ]

18.5.6.17 MAU-to-AUI signal characteristics

Item	Feature	Subclause	Value/comment	Status	Support
ASC1	Signaling rate (stated on label)	7.3.2	10 Mb/s	AUI: M	N/A [ ] M: Yes [ ]
ASC2	CS0 signal frequency (on CI)	7.3.1.2	10 MHz ± 15%	AUI: M	N/A [ ] M: Yes [ ]
ASC3	CS0 signal duty cycle	7.3.1.2	60:40 worst case	AUI: M	N/A [ ] M: Yes [ ]

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18.5.6.18 MAU-to-AUI DI and CI driver characteristics

Item	Feature	Sublause	Value/comment	Status	Support
ADC1 ADC2	Differential output voltage Idle state Start of idle	7.4.1.1	 ≤ 40 mV after 80 BT Figure 7–12	AUI: M	N/A [ ] M: Yes [ ]
ADC3	Current into test load while idle	7.4.1.1	4 mA max. after 80 BT	AUI: M	N/A [ ] M: Yes [ ]
ADC4	Requirements after idle	7.4.1.2	1st bit to Figure 7–11	AUI: M	N/A [ ] M: Yes [ ]
ADC5	Common-mode output voltage, ac	7.4.1.3	≤ 2.5 V peak for 30 Hz to 40 kHz, ≤ 160 mV peak for 40 kHz to 10 MHz, Figure 7–13	AUI: M	N/A [ ] M: Yes [ ]
ADC6	Differential output voltage, open circuit	7.4.1.4	13 V peak max.	AUI: M	N/A [ ] M: Yes [ ]
ADC7	Common-mode output voltage, dc	7.4.1.5	≤ 5.5 V, Figure 7–13	AUI: M	N/A [ ] M: Yes [ ]
ADC8	Fault tolerance	7.4.1.6	Figure 7–14	AUI: M	N/A [ ] M: Yes [ ]
ADC9	Fault current	7.4.1.6	≤ 150 mA, any state, Figure 7–14	AUI: M	N/A [ ] M: Yes [ ]

18.5.6.19 AUI-to-MAU DO receiver characteristics

Item	Feature	Subclause	Value/comment	Status	Support
DO1	Unsquelched threshold	7.4.2.1	160 mV max. differential	AUI: M	N/A [ ] M: Yes [ ]
DO2	Squelch	15.5.1	Reject signals < ±160 mV differential	AUI: M	N/A [ ] M: Yes [ ]
DO3	High to idle transition	7.4.1.1	Must not cause output	AUI: M	N/A [ ] M: Yes [ ]
DO4	Differential input impedance	7.4.2.2	Real part: 77.83 Ω ± 6%, 0 ≤ phase angle ≤ real part ∗ 0.0338	AUI: M	N/A [ ] M: Yes [ ]
DO5	Common-mode range, ac	7.4.2.3	3 V min. for 30 Hz to 40 kHz, 200 mV min. for 40 kHz to 10 MHz	AUI: M	N/A [ ] M: Yes [ ]
DO6	Total common-mode range	7.4.2.4	Magnitude of 0 to 5.5 V ac+dc	AUI: M	N/A [ ] M: Yes [ ]
DO7	Common-mode current limit	7.4.2.4	≤ 1 mA	AUI: M	N/A [ ] M: Yes [ ]
DO8	IDL detection	7.3.1.1	≤ 1.6 BT	AUI: M	N/A [ ] M: Yes [ ]
DO9	Requirements after idle	7.4.2.5	Receiver in specification after start-up delay	AUI: M	N/A [ ] M: Yes [ ]
DO10	Receiver fault tolerance	7.4.2.6	Figure 7–16	AUI: M	N/A [ ] M: Yes [ ]
DO11	Input fault current	7.4.2.6	3 mA max. for Figure 7–16	AUI: M	N/A [ ] M: Yes [ ]

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18.5.6.20 AUI circuit termination

Item	Feature	Subclause	Value/comment	Status	Support
ACT1	Common-mode termination	7.5.2.6	If used, must be to VC	AUI: M	N/A [ ] M: Yes [ ]
ACT2	Pins 1, 4, 8, 11, 14 impedance to VC circuit	7.5.2.8	≤ 5 Ω at 5 MHz	AUI: M	N/A [ ] M: Yes [ ]
ACT3	Pins 1, 4, 8, 11, 14 coupling to VC circuit	7.5.2.8	Capacitive	AUI: M	N/A [ ] M: Yes [ ]

18.5.6.21 MAU-to-AUI mechanical connections

Item	Feature	Subclause	Value/comment	Status	Support
AM1	D-type connector dimensions	7.6.2	IEC 60807-2: 1992 15-pole male	AUI: M	N/A [ ] M: Yes [ ]
AM2	Shell plating material	7.6.2	Conductive	AUI: M	N/A [ ] M: Yes [ ]
AM3	Shell multiple contact points	7.6.2	Number not defined (recommended)	AUI: M	N/A [ ] M: Yes [ ]
AM4	Shell life expectancy	7.6.2	≤ 5 mΩ after 500 matings	AUI: M	N/A [ ] M: Yes [ ]
AM5	Locking posts and mounting	7.6.1	Figures 7–18 and 7–20	AUI: M	N/A [ ] M: Yes [ ]
	Pin connections	7.6.3	Circuit		
AM6	3		Data Out A	AUI: M	N/A [ ] M: Yes [ ]
AM7	10		Data Out B	AUI: M	N/A [ ] M: Yes [ ]
AM8	11		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM9	5		Data In A	AUI: M	N/A [ ] M: Yes [ ]
AM10	12		Data In B	AUI: M	N/A [ ] M: Yes [ ]
AM11	4		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM12	7		No connection	AUI: M	N/A [ ] M: Yes [ ]
AM13	15		No connection	AUI: M	N/A [ ] M: Yes [ ]
AM14	8		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM15	2		Control In A	AUI: M	N/A [ ] M: Yes [ ]
AM16	9		Control In B	AUI: M	N/A [ ] M: Yes [ ]
AM17	1		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM18	6		Voltage common	AUI: M	N/A [ ] M: Yes [ ]
AM19	13		Voltage plus	AUI: M	N/A [ ] M: Yes [ ]
AM20	1		Capacitor to VC	AUI: M	N/A [ ] M: Yes [ ]
AM21	Shell		Isolated from all pins	AUI: M	N/A [ ] M: Yes [ ]

18.5.6.22 MAU reliability

Item	Feature	Subclause	Value/comment	Status	Support
MR1	Mean Time Before Failure	15.4	$> 10^7$ hours without causing communications failure among other stations	M	Yes [ ]

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18.5.6.23 Power consumption

Item	Feature	Subclause	Value/comment	Status	Support
PC1	Power surge limitation	15.5.3	$< 2 \times 10^{-3}$ A–s	APW: M	N/A [ ] M: Yes [ ]
PC2	Power surge duration	15.5.3	100 ms max.	APW: M	N/A [ ] M: Yes [ ]
PC3	Steady-state current drawn power-up capability:	15.5.3	≤ 0.5 A	APW: M	N/A [ ] M: Yes [ ]
PC4	Current-limited sources	15.5.3	0.5 A limited	APW: M	N/A [ ] M: Yes [ ]
PC5	Voltage-limited sources	7.5.2.5	11.28 to 15.75 V via any AUI cable	APW: M	N/A [ ] M: Yes [ ]
PC6	Labeling	15.5.3	As in 15.5.3	APW: M	N/A [ ] M: Yes [ ]
PC7	Power cycle behavior	15.5.3	No extraneous signals on MDI, DI, or CI	AUI: M	N/A [ ] M: Yes [ ]
PC8	Low VP behavior	7.5.2.5	No disruption of media	APW: M	N/A [ ] M: Yes [ ]
PC9	Power sourced on pin 13 of AUI	15.5.3	None if separate power source is implemented	SPW: X	N/A [ ] X: Yes [ ]
PC10	Optional power source isolation	15.5.3	If implemented, shall withstand one of 15.3.4 tests	SPW: M	N/A [ ] M: Yes [ ]

18.5.6.24 PLS–PMA requirements

Item	Feature	Subclause	Value/comment	Status	Support
PMA1	Messages between PLS in DTE or Repeater and PMA	15.5.4	As in 7.2.1	M	Yes [ ]

18.5.6.25 *signal_quality_error* message (SQE)

Item	Feature	Subclause	Value/comment	Status	Support
SQE1	Local MAU transmitting and no collision or fault detected	15.5.4.2.1	*MAU_available* sent on CI	M	Yes [ ]
SQE2	Whenever a collision exists as described in 18.3.1.4	15.5.4.2.1	SQE sent	HFC: M	N/A [ ] M: Yes [ ]
SQE3	SQE Test as described in 18.3.1.5	15.5.4.2.1	SQE sent	HDS:M RPT: X	N/A [ ] M: Yes [ ] N/A [ ] X: Yes [ ]
SQE4	Jabber Condition exists as described in 18.3.1.6	15.5.4.2.1	SQE sent	HFC:M	N/A [ ] M: Yes [ ]
SQE5	Message sent in the absence of SQE	15.5.4.2.1	*MAU_available* message	M	Yes [ ]

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18.5.6.26 Environmental requirements

Item	Feature	Subclause	Value/comment	Status	Support
E1	Ambient Plane Wave field in which MAU meets specification	15.6.2	2 V/m from 10 kHz to 30 MHz. 5 V/m from 30 MHz to 1 GHz.	M	Yes [ ]
E2	Electromagnetic Emissions and Susceptibility	15.6.2	Comply with local and/or national requirements. If none exist, comply with CISPR 22: 1993.	M	Yes [ ]

18.5.6.27 MAU labeling

Item	Feature	Subclause	Value/comment	Status	Support
LBL1	MAU type	15.7	10BASE-FL	O	Yes [ ] No [ ]
LBL2	Data rate	15.7	10 Mb/s	O	Yes [ ] No [ ]
LBL3	Power level	15.7	Maximum current drain	O	Yes [ ] No [ ]
LBL4	Safety warnings	15.7	Any applicable	O	Yes [ ] No [ ]
LBL5	Port labeling	15.7	Input and output	O	Yes [ ] No [ ]
LBL6	Full duplex mode	15.7	Full duplex capable	FDX: O	N/A [ ] Yes [ ] No [ ]

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19. Layer Management for 10 Mb/s baseband repeaters

Clause 19 is deprecated by Clause 30.

19.1 Introduction

The Repeater Management specification has been developed in accordance with the OSI management architecture as specified in ISO/IEC 7498-4: 1989 and the specific requirements of IEEE Std 802.1F-1993. Implementation of this clause is not a requirement for conformance to Clause 9.

19.1.1 Scope

This clause defines a set of mechanisms that enable management of ISO/IEC 8802-3 10 Mb/s baseband repeater units. The managed objects within this International Standard are defined in terms of their behaviour, attributes, actions, notifications, and packages in accordance with IEEE 802.1 and ISO/IEC International Standards for network management. Managed objects are grouped into mandatory and optional packages.

This International Standard is defined to be independent of any particular management application or management protocol. The means by which the managed objects defined in this International Standard are accessed is beyond the scope of this International Standard.

19.1.2 Relationship to objects in IEEE Std 802.1F-1993

The following managed object classes, if supported by an implementation, shall be as specified in IEEE Std 802.1F-1993: oResourceTypeID, oEWMAMetricMonitor:

a) **oResourceTypeID.** This object class is mandatory and shall be implemented as defined in IEEE Std 802.1F-1993. This object is bound to repeater as defined by the NAMEBINDING in 19.2.4 and H.2.2.1.
b) **oEWMAMetricMonitor.** This object class is optional. When implemented, it shall be implemented as defined in IEEE Std 802.1F-1993, subject to the specific requirements described below. This object is bound to system as defined by the NAMEBINDING in H.2.2.1.

Implementations of Repeater Management that support the oEWMAMetricMonitor managed object class are required to support values of aGranularityPeriod as small as one second. Implementations are required to support at least one sequence of low and high thresholds. The granularity period may be set to equal to the moving time period as a minimal conformant implementation.

19.1.3 Definitions

See 1.4.

19.1.4 Symbols and abbreviations

See 1.5.

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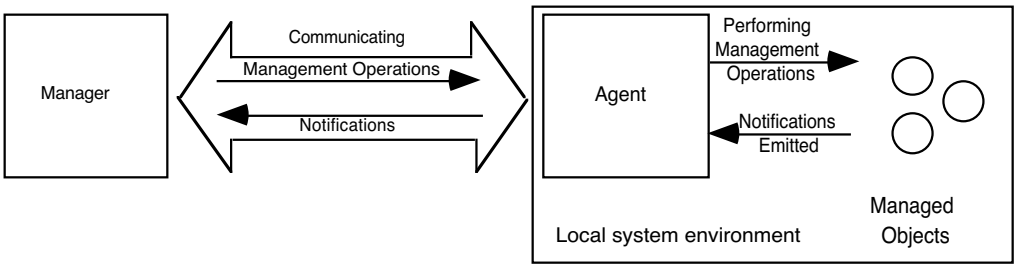
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19.1.5 Management model

This International Standard describes management of repeaters in terms of a general model of management of resources within the open systems environment. The model is described in ISO/IEC 10040: 1992, a brief summary of the model is included here.

Management is viewed as a distributed application modeled as a set of interacting management processes. These processes are executed by systems within the open environment. A managing system executes a managing process that invokes management operations. A managed system executes a process that is receptive to these management operations and provides an interface to the resources to be managed. A managed object is the abstraction of a resource that represents its properties as seen by (and for the purpose of) management. Managed objects respond to a defined set of management operations. Managed objects are also capable of emitting a defined set of notifications. This interaction of processes is shown in Figure 19–1.



NOTE—Figure 1 of ISO/IEC 10040 has been reproduced with the permission of ISO. Copies of the complete standard may be obtained from the International Organization for Standardization, Case Postale 56, 1 rue de Varembé, CH-1211, Genève 20, Switzerland/Suisse.

Figure 19–1—Interaction between manager, agent, and objects

A managed object is a management view of a resource. The resource may be a logical construct, function, physical device, or anything subject to management. Managed objects are defined in terms of four types of elements:

a) *Attributes*. Data-like properties (as seen by management) of a managed object.
b) *Actions*. Operations that a managing process may perform on an object or its attributes.
c) *Notifications*. Unsolicited reports of events that may be generated by an object.
d) *Behaviour.* The way in which managed objects, attributes, and actions interact with the actual resources they model and with each other.

The above items are defined in 19.2.3 through 19.2.6 of this International Standard in terms of the template requirements of ISO/IEC 10165-4: 1992 in Annex H.

Some of the functions and resources within a repeater are appropriate targets for management. They have been identified by specifying managed objects that provide a management view of the functions or resources. Within this general model, a repeater is viewed as a managed device. It performs functions as defined by the applicable standard for such a device. Managed objects providing a view of those functions and resources appropriate to the management of a repeater are specified. The purpose of this International Standard is to define the object classes associated with repeaters in terms of their attributes, operations, notifications, and behaviour.

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19.2 Managed objects

19.2.1 Introduction

This document defines the management of IEEE 802.3 repeaters by defining associated managed objects. This management encompasses two distinct aspects of repeater management.

The first aspect provides the means to monitor and control the functions of a repeater. These functions include, but are not limited to, identifying a repeater, testing and initializing a repeater, and enabling/disabling a port.

The second aspect provides the means to monitor traffic from attached segments, and to measure traffic sourced by DTEs connected to these segments. This is done by gathering statistics on packets that enter a repeater and maintaining those statistics on a per-port basis.

19.2.2 Overview of managed objects

Managed objects provide a means to

a) Identify a resource
b) Control a resource
c) Monitor a resource

19.2.2.1 Text description of managed objects

In case of conflict, the formal behaviour definitions in 19.2.3 through 19.2.6 take precedence over the text descriptions in this subclause.

a) **repeater.** The topmost managed object class of that portion of the containment tree shown in Figure 19–3. All other managed objects and their attributes defined in this clause are contained within the repeater managed object.
b) **repeaterMonitor.** A managed object class called out by IEEE Std 802.1F-1993.
c) **resourceTypeID.** A managed object class called out by IEEE Std 802.1F-1993.
d) **group.** The group managed object class is a view of a collection of ports.
e) **port.** The port managed object class provides a view of the functional link between the data transfer service and a single PMA. The attributes associated with port deal with the monitoring of traffic being handled by the repeater from the port and control of the operation of the port. The port enable/disable function as reported by portAdminState is preserved across events involving loss of power.

NOTE—Attachment to nonstandard PMAs is outside the scope of this International Standard.

19.2.2.2 Port functions to support management

The port object class contains seven functions that are used to collect statistics on the activity received by the port. The relationship of the functions to the port and to the port attributes is shown in Figure 19–2.

a) **Activity Timing function.** Measures the duration of the assertion of the CarrierEvent signal. This duration value must be adjusted by removing the value of Carrier Recovery Time (see 9.5.6.5) to obtain the true duration of activity on the network. The output of the Activity Timing function is the ActivityDuration value, which represents the duration of the CarrierEvent signal as expressed in units of bit times.
b) **Carrier Event function.** Asserts the CarrierEvent signal when the repeater exits the IDLE state (see Figure 9–2) and the port has been determined to be port N. It de-asserts the CarrierEvent signal when, for a duration of at least Carrier Recovery Time (see 9.5.6.5), both the DataIn(N) variable has

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the value II and the CollIn(N) variable has the value -SQE. The value N is the port assigned at the time of transition from the IDLE state.

c) **Collision Event function.** Asserts the CollisionEvent signal when the CollIn(X) variable has the value SQE. The CollisionEvent signal remains asserted until the assertion of any CarrierEvent signal due to the reception of the following event.

d) **Cyclic Redundancy Check function.** Verifies that the sequence of octets output by the framing function contains a valid frame check sequence field. The frame check sequence field is the last four octets received from the output of the framing function. The algorithm for generating an FCS from the octet stream is specified in 3.2.8. If the FCS generated according to this algorithm is not the same as the last four octets received from the framing function, then the FCSError signal is asserted. The FCSError signal is cleared upon the assertion of the CarrierEvent signal due to the reception of the following event.

e) **Framing function.** Recognizes the boundaries of an incoming frame by monitoring the CarrierEvent signal and the decoded data stream. Data bits are accepted while the CarrierEvent signal is asserted. The framing function strips preamble and start of frame delimiter from the received data stream. The remaining bits are aligned along octet boundaries. If there is not an integral number of octets, then FramingError shall be asserted. The FramingError signal is cleared upon the assertion of the CarrierEvent signal due to the reception of the following event.

f) **Octet Counting function.** Counts the number of complete octets received from the output of the framing function. The output of the octet counting function is the OctetCount value. The OctetCount value is reset to zero upon the assertion of the CarrierEvent signal due to the reception of the following event.

g) **Source Address function.** Extracts octets from the stream output by the framing function. The seventh through twelfth octets shall be extracted from the octet stream and output as the SourceAddress variable. The SourceAddress variable is set to an invalid state upon the assertion of the CarrierEvent signal due to the reception of the following event.

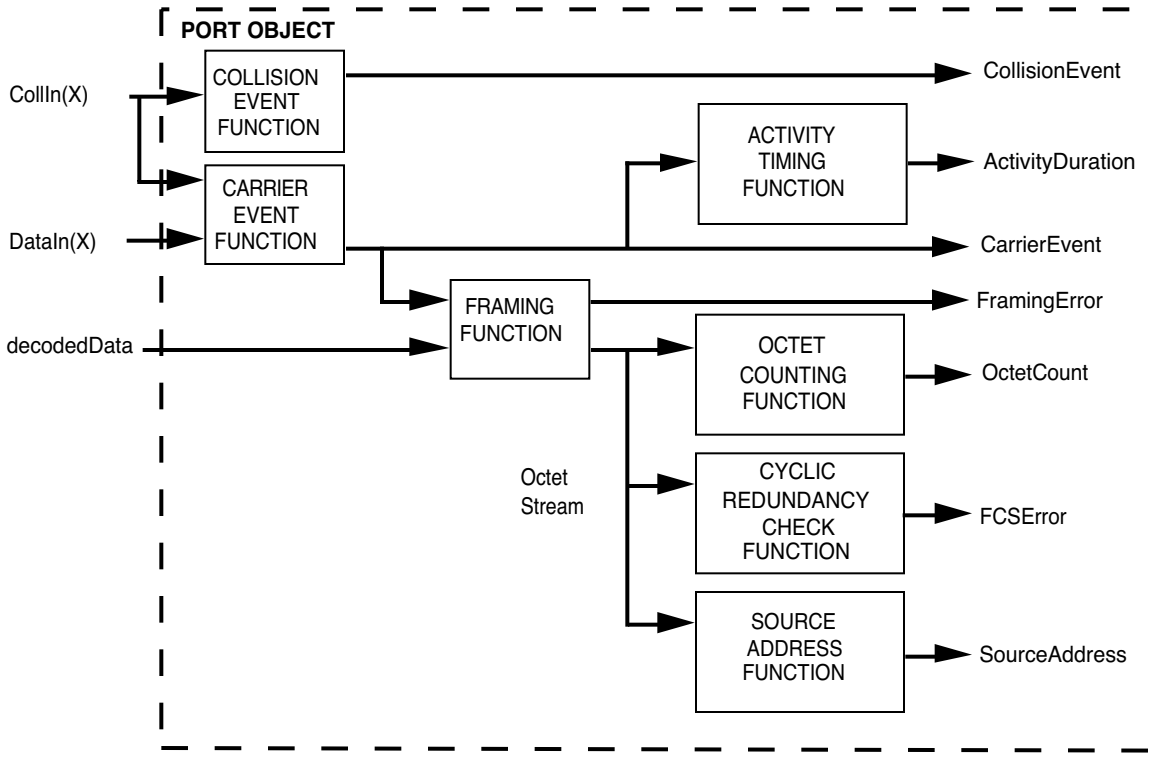


Figure 19–2—Functions relationship

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19.2.2.3 Containment

A containment relationship is a structuring relationship for managed objects in which the existence of a managed object is dependent on the existence of a containing managed object. The contained managed object is said to be the subordinate managed object and the containing managed object the superior managed object. The containment relationship is used for naming managed objects. The local containment relationships among object classes are depicted in Figure 19–3. This figure also shows the names, naming attributes, and data attributes of the object classes as well as whether a particular containment relationship is one-to-one or one-to-many. For further requirements on this topic, see IEEE Std 802.1F-1993.

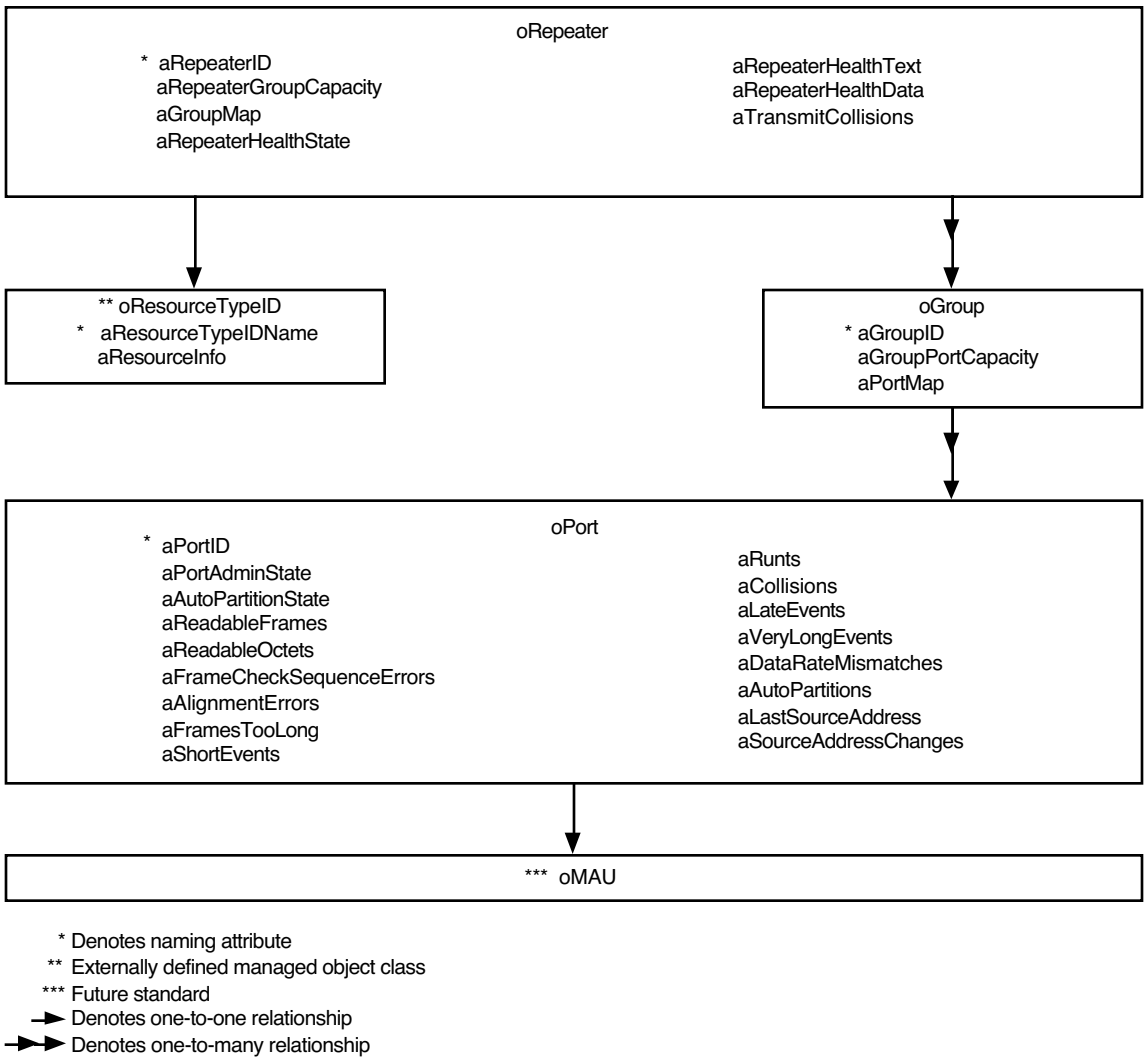


Figure 19–3—Entity relationship diagram

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19.2.2.4 Naming

The name of an individual managed object is hierarchically defined within a managed system. For example, a port might be identified as "repeater 3, group 01, port 13," that is, port 13 of group 01 of a repeater with repeaterID 3 within the managed system. This is represented in the relationship of the naming attributes in Figure 19–3.

19.2.2.5 Packages and capabilities

This International Standard makes use of the concept of "packages" as defined in ISO/IEC 10165-4: 1992 as a means of grouping behaviour, attributes, actions, and notifications within a managed object class definition. Packages may either be mandatory or conditional, that is to say, present if a given condition is true. Within this International Standard, "capabilities" are defined, each of which corresponds to a set of packages, which are components of a number of managed object class definitions and which share the same condition for presence. The "Basic Control Capability" consists of the set of mandatory packages. All other capabilities are optional and comprise sets of conditional packages. For a managed repeater to be conformant to this International Standard, it shall fully implement the Basic Control Capability. For the repeater to be conformant to an optional capability, it shall implement that entire capability. The capabilities and their associated packages are summarized in Table 19–1 (see facing page).

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Table 19–1—Packages and capabilities

		Basic Control Capability (Mandatory)	Performance Monitor Capability (Optional)	Address Tracking Capability (Optional)
oRepeater managed object class				
aRepeaterID	ATTRIBUTE GET	X		
aRepeaterGroupCapacity	ATTRIBUTE GET	X		
aGroupMap	ATTRIBUTE GET	X		
aRepeaterHealthState	ATTRIBUTE GET	X		
aRepeaterHealthText	ATTRIBUTE GET	X		
aRepeaterHealthData	ATTRIBUTE GET	X		
aTransmitCollisions	ATTRIBUTE GET		X	
acResetRepeater	ACTION	X		
acExecuteNonDisruptiveSelfTest	ACTION	X		
nRepeaterHealth	NOTIFICATION	X		
nRepeaterReset	NOTIFICATION	X		
nGroupMapChange	NOTIFICATION	X		
oResourceTypeID managed object class				
aResourceTypeIDName	ATTRIBUTE GET	X		
aResourceInfo	ATTRIBUTE GET	X		
oGroup managed object class				
aGroupID	ATTRIBUTE GET	X		
aGroupPortCapacity	ATTRIBUTE GET	X		
aPortMap	ATTRIBUTE GET	X		
nPortMapChange	NOTIFICATION	X		
oPort managed object class				
aPortID	ATTRIBUTE GET	X		
aPortAdminState	ATTRIBUTE GET	X		
aAutoPartitionState	ATTRIBUTE GET	X		
aReadableFrames	ATTRIBUTE GET		X	
aReadableOctets	ATTRIBUTE GET		X	
aFrameCheckSequenceErrors	ATTRIBUTE GET		X	
aAlignmentErrors	ATTRIBUTE GET		X	
aFramesTooLong	ATTRIBUTE GET		X	
aShortEvents	ATTRIBUTE GET		X	
aRunts	ATTRIBUTE GET		X	
aCollisions	ATTRIBUTE GET		X	
aLateEvents	ATTRIBUTE GET		X	
aVeryLongEvents	ATTRIBUTE GET		X	
aDataRateMismatches	ATTRIBUTE GET		X	
aAutoPartitions	ATTRIBUTE GET		X	
aLastSourceAddress	ATTRIBUTE GET			X
aSourceAddressChanges	ATTRIBUTE GET			X
acPortAdminControl	ACTION	X		
Common Attributes Template				
aRMCounter	ATTRIBUTE GET		X	X

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19.2.3 Repeater managed object class

This subclause formally defines the behaviours for Repeater managed object classes, attributes, actions, and notifications.

19.2.3.1 Repeater attributes

19.2.3.1.1 aRepeaterID

ATTRIBUTE
APPROPRIATE SYNTAX
INTEGER
BEHAVIOUR DEFINED AS:
The value of aRepeaterID is assigned so as to uniquely identify a repeater among the subordinate managed objects of system (systemID and system are defined in ISO/IEC 10165-2: 1992).

19.2.3.1.2 aRepeaterGroupCapacity

ATTRIBUTE
APPROPRIATE SYNTAX
INTEGER
BEHAVIOUR DEFINED AS:
The aRepeaterGroupCapacity is the number of groups that can be contained within the repeater. Within each managed repeater, the groups are uniquely numbered in the range from 1 to aRepeaterGroupCapacity. Some groups may not be present in a given repeater instance, in which case the actual number of groups present is less than aRepeaterGroupCapacity. The number of groups present is never greater than aRepeaterGroupCapacity.

19.2.3.1.3 aGroupMap

ATTRIBUTE
APPROPRIATE SYNTAX
BITSTRING
BEHAVIOUR DEFINED AS:
A string of bits which reflects the current configuration of units which are viewed by group managed objects. The length of the bitstring is "aRepeaterGroupCapacity" bits. The first bit relates to group 1. A "1" in the bitstring indicates presence of the group, "0" represents absence of the group.

19.2.3.1.4 aRepeaterHealthState

ATTRIBUTE
APPROPRIATE SYNTAX:
An ENUMERATED VALUE LIST that has the following entries:

other	--undefined or unknown
ok	--no known failures
repeaterFailure	--known to have a repeater related failure
groupFailure	--known to have a group related failure
portFailure	--known to have a port related failure
generalFailure	--has a failure condition, unspecified type

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BEHAVIOUR DEFINED AS:

The aRepeaterHealthState attribute indicates the operational state of the repeater. The aRepeaterHealthData and aRepeaterHealthText attributes may be consulted for more specific information about the state of the Repeater's health. In case of multiple kinds of failures (e.g., repeater failure and port failure), the value of this attribute shall reflect the highest priority in the following order:

repeater failure
group failure
port failure
general failure.

19.2.3.1.5 aRepeaterHealthText

ATTRIBUTE
APPROPRIATE SYNTAX:

A PrintableString, 255 characters max.

BEHAVIOUR DEFINED AS:

The aRepeaterHealthText attribute is a text string that provides information relevant to the operational state of the repeater. Repeater vendors may use this mechanism to provide detailed failure information or instructions for problem resolution.
The contents are vendor specific.

19.2.3.1.6 aRepeaterHealthData

ATTRIBUTE
APPROPRIATE SYNTAX:

OCTET STRING, 0–255.

BEHAVIOUR DEFINED AS:

The aRepeaterHealthData attribute is a block of data octets that provides information relevant to the operational state of the repeater. The encoding of this data block is vendor dependent. Repeater vendors may use this mechanism to provide detailed failure information or instructions for problem resolution.

19.2.3.1.7 aTransmitCollisions

ATTRIBUTE
APPROPRIATE SYNTAX:

Generalized non-resettable counter. This counter has a maximum increment rate of 75 000 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented every time the repeater state machine enters the TRANSMIT COLLISION state from any state other than ONE PORT LEFT (see Figure 9–2).

19.2.3.2 Repeater actions

19.2.3.2.1 acResetRepeater

ACTION
APPROPRIATE SYNTAX

None required

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BEHAVIOUR DEFINED AS:

This is the transition to the START state of Figure 9–2 in Clause 9. The repeater performs a disruptive self-test that has the following characteristics:

a) The components are not specified.
b) The test resets the repeater but without affecting management information about the repeater.
c) The test does not inject packets onto any segment.
d) Packets received during the test may or may not be transferred.
e) The test does not interfere with management functions.

This causes an nRepeaterReset notification to be sent.

19.2.3.2.2 acExecuteNonDisruptiveSelfTest

ACTION

APPROPRIATE SYNTAX

None required

BEHAVIOUR DEFINED AS:

The repeater performs a vendor-specific, non-disruptive self-test that has the following characteristics:

a) The components are not specified.
b) The test does not change the state of the repeater or management information about the repeater.
c) The test does not inject packets onto any segment.
d) The test does not prevent the transfer of any packets.
e) Completion of the test causes an nRepeaterHealth to be sent.

19.2.3.3 Repeater notifications

19.2.3.3.1 nRepeaterHealth

NOTIFICATION

APPROPRIATE SYNTAX

A SEQUENCE of 3 data types. The first is mandatory, the following two are optional. The first is value of the attribute aRepeaterHealthState. The second is the value of the attribute aRepeaterHealthText. The third is the value of the attribute aRepeaterHealthData.

BEHAVIOUR DEFINED AS:

This notification conveys information related to the operational state of the repeater. See the aRepeaterHealthState, aRepeaterHealthText, and aRepeaterHealthData attributes for descriptions of the information that is sent. The nRepeaterHealth notification is sent only when the health state of the repeater changes. The nRepeaterHealth notification shall contain repeaterHealthState. repeaterHealthData and repeaterHealthText may or may not be included. The nRepeaterHealth notification is not sent as a result of powering up a repeater.

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19.2.3.3.2 nRepeaterReset

NOTIFICATION
APPROPRIATE SYNTAX
A SEQUENCE of 3 data types. The first is mandatory, the following two are optional. The first is value of the attribute aRepeaterHealthState. The second is the value of the attribute aRepeaterHealthText. The third is the value of the attribute aRepeaterHealthData.
BEHAVIOUR DEFINED AS:
This notification conveys information related to the operational state of the repeater. The nRepeaterReset notification is sent when the repeater is reset as the result of a power-on condition or upon completion of the acResetRepeater action. The nRepeaterReset notification shall contain repeaterHealthState. repeaterHealthData and RepeaterHealthText may, or may not be included.

19.2.3.3.3 nGroupMapChange

NOTIFICATION
APPROPRIATE SYNTAX
BITSTRING
BEHAVIOUR DEFINED AS:
This notification is sent when a change occurs in the group structure of a repeater. This occurs only when a group is logically removed from or added to a repeater. The nGroupMapChange notification is not sent when powering up a repeater. The value of the notification is the updated value of the aGroupMap attribute.

19.2.4 ResourceTypeID Managed Object Class

Implementation of this managed object in accordance with the definition contained in IEEE Std 802.1F-1993 is a conformance requirement of this International Standard. A single instance of the Resource Type ID managed object exists within the Repeater managed object class. The managed object itself is contained in IEEE Std 802.1F-1993; therefore, only the name binding appears in this International Standard.

19.2.5 Group managed object class

This subclause formally defines the behaviours for Group managed object classes attributes and notification.

19.2.5.1 Group attributes

19.2.5.1.1 aGroupID

ATTRIBUTE
APPROPRIATE SYNTAX
INTEGER
BEHAVIOUR DEFINED AS:
A value unique within the repeater. This value is never greater than aRepeaterGroupCapacity.

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19.2.5.1.2 aGroupPortCapacity

ATTRIBUTE
APPROPRIATE SYNTAX
INTEGER
BEHAVIOUR DEFINED AS:
The aGroupPortCapacity is the number of ports contained within the group. Valid range is 1–1024. Within each group, the ports are uniquely numbered in the range from 1 to aGroupPortCapacity. Some ports may not be present in a given group instance, in which case the actual number of ports present is less than aGroupPortCapacity. The number of ports present is never greater than aGroupPortCapacity.

19.2.5.1.3 aPortMap

ATTRIBUTE
APPROPRIATE SYNTAX
BitString
BEHAVIOUR DEFINED AS:
A string of bits which reflects the current configuration of port managed objects within this group. The length of the bitstring is "aGroupPortCapacity" bits. The first bit relates to group 1. A "1" in the bitstring indicates presence of the port, "0" represents absence of the port.

19.2.5.2 Group Notifications

19.2.5.2.1 nPortMapChange

NOTIFICATION
APPROPRIATE SYNTAX
BitString
BEHAVIOUR DEFINED AS:
This notification is sent when a change occurs in the port structure of a group. This occurs only when a port is logically removed from or added to a group. The nPortMapChange notification is not sent when powering up a repeater. The value of the notification is the updated value of the aPortMap attribute.

19.2.6 Port managed object class

This subclause formally defines the behaviours for Port managed object classes attributes and action.

19.2.6.1 Port Attributes

19.2.6.1.1 aPortID

ATTRIBUTE
APPROPRIATE SYNTAX
INTEGER
BEHAVIOUR DEFINED AS:
A value unique in the group. It is assumed that ports are partitioned into groups that also have IDs. This value can never be greater than aGroupPortCapacity.

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19.2.6.1.2 aPortAdminState

ATTRIBUTE
APPROPRIATE SYNTAX:
An ENUMERATED VALUE LIST that has the following entries.
disabled
enabled
BEHAVIOUR DEFINED AS:
A disabled port neither transmits nor receives. The port shall be explicitly enabled to restore operation. The acPortAdminControl action provides this ability. The port enable/disable function as reported by this attribute is preserved across repeater reset including loss of power. aPortAdminState takes precedence over auto-partition and functionally operates between the auto-partition mechanism and the AUI/PMA. Auto-partition is reinitialized whenever acPortAdminControl is enabled.

19.2.6.1.3 aAutoPartitionState

ATTRIBUTE
APPROPRIATE SYNTAX:
An ENUMERATED VALUE LIST that has the following entries.
autoPartitioned
notAutoPartitioned
BEHAVIOUR DEFINED AS:
The aAutoPartitionState flag indicates whether the port is currently partitioned by the repeater's auto-partition protection. The conditions that cause port partitioning are specified in partition state machine in Clause 9. They are not differentiated here.

19.2.6.1.4 aReadableFrames

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 15 000 counts per second.
BEHAVIOUR DEFINED AS:
A representation of the total frames of valid frame length. Increment counter by one for each frame whose OctetCount is greater than or equal to minFrameSize and less than or equal to maxFrameSize (see 4.4.2.1) and for which the FCSError and CollisionEvent signals are not asserted.

NOTE—This statistic provides one of the parameters necessary for obtaining the packet error rate.

19.2.6.1.5 aReadableOctets

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 1 240 000 counts per second.
BEHAVIOUR DEFINED AS:
Increment counter by OctetCount for each frame which has been determined to be a readable frame.

NOTE—This statistic provides an indicator of the total data transferred.

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19.2.6.1.6 aFrameCheckSequenceErrors

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 15 000 counts per second.
BEHAVIOUR DEFINED AS:
Increment counter by one for each frame with the FCSError signal asserted and the FramingError and CollisionEvent signals deasserted and whose OctetCount is greater than or equal to minFrameSize and less than or equal to maxFrameSize (see 4.4.2.1).

19.2.6.1.7 aAlignmentErrors

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 15 000 counts per second.
BEHAVIOUR DEFINED AS:
Increment counter by one for each frame with the FCSError and FramingError signals asserted and CollisionEvent signal deasserted and whose OctetCount is greater than or equal to minFrameSize and less than or equal to maxFrameSize (see 4.4.2.1). If aAlignmentErrors is incremented then the aFrameCheckSequenceErrors attribute shall not be incremented for the same frame.

19.2.6.1.8 aFramesTooLong

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 815 counts per second.
BEHAVIOUR DEFINED AS:
Increment counter by one for each frame whose OctetCount is greater than maxFrameSize (see 4.4.2.1). If aFrameTooLong is counted then neither the aAlignmentErrors nor the aFrameCheckSequenceErrors attribute shall be incremented for the frame.

19.2.6.1.9 aShortEvents

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 75 000 counts per second.
BEHAVIOUR DEFINED AS:
Increment counter by one for each CarrierEvent with ActivityDuration less than ShortEventMaxTime. ShortEventMaxTime is greater than 74 bit times and less than 82 bit times. ShortEventMaxTime has tolerances included to provide for circuit losses between a conformance test point at the AUI and the measurement point within the state machine.

NOTE—shortEvents may indicate externally generated noise hits which will cause the repeater to transmit Runts to its other ports, or propagate a collision (which may be late) back to the transmitting DTE and damaged frames to the rest of the network.

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Implementors may wish to consider selecting the ShortEventMaxTime towards the lower end of the allowed tolerance range to accommodate bit losses suffered through physical channel devices not budgeted for within this International Standard.

19.2.6.1.10 aRunts

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 75 000 counts per second.
BEHAVIOUR DEFINED AS:
Increment counter by one for each CarrierEvent that meets one of the following two conditions. Only one test need be made. (1) The ActivityDuration is greater than ShortEventMaxTime and less than ValidPacketMinTime and the CollisionEvent signal is deasserted. (2) The OctetCount is less than 64, the ActivityDuration is greater than ShortEventMaxTime and the CollisionEvent signal is deasserted. ValidPacketMinTime is greater than or equal to 552 bit times and less than 565 bit times. An event whose length is greater than 74 bit times but less than 82 bit times shall increment either the aShortEvents attribute or the aRunts attribute but not both. A CarrierEvent greater than or equal to 552 bit times but less than 565 bit times may or may not be counted as a runt. ValidPacketMinTime has tolerances included to provide for circuit losses between a conformance test point at the AUI and the measurement point within the state machine.

NOTE—Runts usually indicate collision fragments, a normal network event. In certain situations associated with large diameter networks a percentage of runts may exceed ValidPacketMinTime.

19.2.6.1.11 aCollisions

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 75 000 counts per second.
BEHAVIOUR DEFINED AS:
Increment counter by one for each CarrierEvent in which the CollisionEvent signal is asserted.
Increment counter by one for any CarrierEvent signal on any port in which the CollisionEvent signal on this port is asserted.

19.2.6.1.12 aLateEvents

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 75 000 counts per second.
BEHAVIOUR DEFINED AS:
Increment counter by one for each CarrierEvent in which the CollIn(X) variable transitions to the value SQE (see 9.9.6.2) while the ActivityDuration is greater than the LateEventThreshold. Such a CarrierEvent is counted twice, as both a aCollision and as a aLateEvent. The LateEventThreshold is greater than 480 bit times and less than 565 bit times. LateEventThreshold has tolerances included to permit an

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implementation to build a single threshold to serve as both the LateEventThreshold and ValidPacketMinTime threshold.

19.2.6.1.13 aVeryLongEvents

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter. This counter has a maximum increment rate of 250 counts per second.
BEHAVIOUR DEFINED AS:
Increment counter by one for each CarrierEvent whose ActivityDuration is greater than the MAU Jabber Lockup Protection timer TW3 (see 9.6.1, 9.6.5). Other counters may be incremented as appropriate.

19.2.6.1.14 aDataRateMismatches

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter.
BEHAVIOUR DEFINED AS:
Increment counter by one for each frame received by this port that meets all of the conditions required by only one of the following two measurement methods: Measurement method A: 1) The CollisionEvent signal is not asserted. 2) The ActivityDuration is greater than ValidPacketMinTime. 3) The frequency (data rate) is detectably mismatched from the local transmit frequency. Measurement method B: 1) The CollisionEvent signal is not asserted. 2) The OctetCount is greater than 63. 3) The frequency (data rate) is detectably mismatched from the local transmit frequency. The exact degree of mismatch is vendor specific and is to be defined by the vendor for conformance testing.
When this event occurs, other counters whose increment conditions were satisfied may or may not also be incremented, at the implementor's discretion.

NOTE—Whether or not the repeater was able to maintain data integrity is beyond the scope of this International Standard.

19.2.6.1.15 aAutoPartitions

ATTRIBUTE
APPROPRIATE SYNTAX:
Generalized non-resettable counter.
BEHAVIOUR DEFINED AS:
Increment counter by one for each time that the repeater has automatically partitioned this port. The conditions that cause port partitioning are specified in the partition state machine in Clause 9. They are not differentiated here.

19.2.6.1.16 aLastSourceAddress

ATTRIBUTE
APPROPRIATE SYNTAX:
MACAddress
BEHAVIOUR DEFINED AS:

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The aLastSourceAddress attribute is the Source Address of the last readableFrame received by this port.

19.2.6.1.17 aSourceAddressChanges

ATTRIBUTE
APPROPRIATE SYNTAX:

Generalized non-resettable counter. This counter has a maximum increment rate of 15 000 counts per second.

BEHAVIOUR DEFINED AS:

Increment counter by one each time that the aLastSourceAddress attribute has changed.

NOTE—This may indicate whether a link is connected to a single DTE or another multiuser segment.

19.2.6.2 Port Actions

19.2.6.2.1 acPortAdminControl

ACTION
APPROPRIATE SYNTAX:

Same as aPortAdminState.

BEHAVIOUR DEFINED AS:

This action provides a means to alter aPortAdminState and exert a BEGIN on the Auto-Partition state machine (Figure 9–6) upon taking the value “enabled”.

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20. Layer Management for 10 Mb/s baseband medium attachment units

Clause 20 is deprecated by Clause 30.

20.1 Introduction

The MAU Management specification has been developed in accordance with the Open Systems Interconnection (OSI) management architecture as specified in ISO/IEC 7498-4: 1989.

20.1.1 Scope

This clause defines a set of mechanisms that enable management of IEEE 802.3 10 Mb/s integrated Medium Attachment Units (MAUs). In addition, for ports without integral MAUs, attributes are provided for characteristics observable from the AUI of the connected DTE or repeater. Direct management of MAUs that are external to their respective DTEs or repeaters is beyond the scope of this standard. The managed objects within this standard are defined as sets of attributes, actions, notifications, and behaviours in accordance with IEEE Std 802.1-1990 and ISO/IEC International Standards for network management. This clause builds upon the concepts and terminology that are defined more fully in Clause 19.

This standard is defined to be independent of any particular management application or management protocol. The means by which the managed objects defined in this standard are accessed is beyond the scope of this standard.

20.1.2 Management model

See 19.1.5.

20.2 Managed objects

20.2.1 Text description of managed objects

In case of conflict, the formal behaviour definitions in Annex H.3 take precedence over the text descriptions in this clause.

a) **oRepeaterPort.** The managed object that contains the MAU managed object in a repeater set.
b) **oDTEPort.** The managed object that contains the MAU managed object in a DTE.
c) **oMAU.** The managed object of that portion of the containment tree shown in Figure 20–1. The attributes, notifications and actions defined in this clause are contained within the MAU managed object.

Neither counter values nor the value of aMAUadminState is required to be preserved across events involving the loss of power.

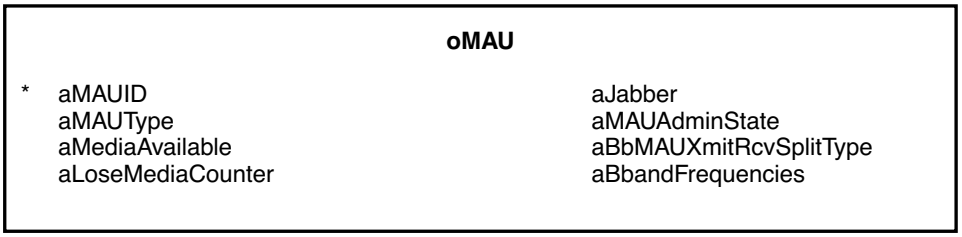
20.2.1.1 Naming

The name of an individual managed object is hierarchically defined within a managed system. In the case of MAU management, this will present itself in one of the two forms that are appropriate for a MAU's use, that is, as associated with a CSMA/CD interface of a DTE or with a particular port of a managed repeater. For example, a MAU could be identified as "repeater 3, group 01, port 13, mau 1," that is, the MAU associated with port 13 of group 01 of a repeater with repeaterID 3 within the managed system. An example of this is represented in the relationship of the naming attributes in the Entity Relationship Diagram, Figure 19–3.

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NOTE—The * denotes naming attribute.

Figure 20–1—Entity relationship diagram

20.2.1.2 Containment

A containment relationship is a structuring relationship for managed objects in which the existence of a managed object is dependent on the existence of a containing managed object. The contained managed object is said to be the subordinate managed object, and the containing managed object the superior managed object. MAU management is only valid in a system that provides management at the next higher containment level, that is, either a DTE or Repeater with Layer Management. The containment relationships among object classes are depicted in the Entity Relationship Diagram, Figure 20–1, and specified in the name bindings in Annex H, H.3.1.

20.2.1.3 Packages

This standard and ISO/IEC guidelines make provision for grouping attributes, actions, and notifications in implementation groups, or "packages," within each managed object class. The "Basic Control Package" is mandatory; all other packages are optional. For a managed MAU to be conformant to this standard, it shall fully implement the Basic Control Package. For a MAU to be conformant to an optional package, it shall implement that entire package. While nonconformant (reference aMAUType = "other") MAUs may utilize some or all of this clause to specify their management, conformance to this clause requires both a conformant MAU and conformant management. MAU Management is optional with respect to all other CSMA/CD Management. The packages are summarized in Table 20–1.

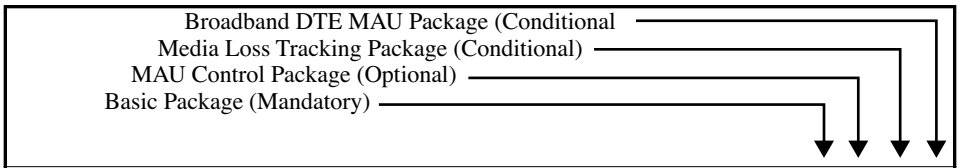
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Table 20–1—Packages



MAU managed object class						
aMAUID	ATTRIBUTE	GET	X			
aMAUType	ATTRIBUTE	GET	X			
aMediaAvailable	ATTRIBUTE	GET	X			
aLoseMediaCounter	ATTRIBUTE	GET			X	
aJabber	ATTRIBUTE	GET	X			
aMAUAdminState	ATTRIBUTE	GET	X			
aBbMAUXmitRcvSplitType	ATTRIBUTE	GET				X
aBroadbandFrequencies	ATTRIBUTE	GET				X
acResetMAUAction	ACTION			X		
acMAUAdminControl	ACTION			X		
nJabber	NOTIFICATION		X			

20.2.2 MAU Managed object class

This subclause formally defines the behaviours for MAU Management objects, attributes, actions, and notifications.

20.2.2.1 MAU attributes

20.2.2.1.1 aMAUID

ATTRIBUTE
APPROPRIATE SYNTAX:
INTEGER
BEHAVIOUR DEFINED AS:
The value of aMAUID is assigned so as to uniquely identify a MAU among the subordinate managed objects of the containing object.

20.2.2.1.2 aMAUType

ATTRIBUTE
APPROPRIATE SYNTAX:
An INTEGER that meets the requirements of the description below. Additional values are needed for following types:

global	--reserved for future use
other	--see 20.2.1.3
unknown	--initializing, true state or type not yet known

BEHAVIOUR DEFINED AS:
Returns a value that identifies the 10 Mb/s internal MAU type. The enumeration of the type is such that the value matches the clause number of the standard that specifies the particular MAU. If an AUI is to be identified to access an external MAU, then type “AUI” is returned.

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20.2.2.1.3 aMediaAvailable

ATTRIBUTE
APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

other	--undefined
unknown	--initializing, true state not yet known
available	--link or light normal, loopback normal
not available	--link loss or low light, no loop back
remote fault	--remote fault, applies only to 10BASE-FB
invalid signal	--invalid signal, applies only to 10BASE-FB

BEHAVIOUR DEFINED AS:

If the MAU is a link or fiber type (FOIRL, 10BASE-T, 10BASE-F), then this is equivalent to the link test fail state/low light function. For an AUI or a coaxial cable (including broadband) MAU, this indicates whether or not loopback is detected on the DI circuit. The value of this attribute persists between packets for MAU types AUI, 10BASE5, 10BASE2, 10BROAD36, and 10BASE-FP.

At power-up or following a reset, the value of this attribute will be "unknown" for AUI, 10BASE5, 10BASE2, 10BROAD36, and 10BASE-FP MAUs. For these MAUs, loopback will be tested on each transmission during which no collision is detected. If DI is receiving *input* when DO returns to IDL after a transmission and there has been no collision during the transmission, then loopback will be detected. The value of this attribute will only change during noncollided transmissions for AUI, coaxial cable, and 10BASE-FP MAUs.

20.2.2.1.4 aLoseMediaCounter

ATTRIBUTE
APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 10 counts per second.

BEHAVIOUR DEFINED AS:

Counts the number of times that the MAU leaves MediaAvailState "available." Mandatory for MAU type "AUI," optional for all others.

20.2.2.1.5 aJabber

ATTRIBUTE
APPROPRIATE SYNTAX:

A SEQUENCE of two indications.

The first, JabberFlag, consists of an ENUMERATED value list that has the following entries:

other	--undefined
unknown	--initializing, true state not yet known
normal	--state is true or normal
fault	--state is false, fault, or abnormal

The second, jabberCounter, is a generalized nonresettable counter. This counter has a maximum increment rate of 40 counts per second.

BEHAVIOUR DEFINED AS:

If the MAU is in the jabber state, the jabberFlag portion of the attribute is set to the "fault" value. The jabberCounter portion of the attribute is incremented each time the flag is set to the "fault" value. This attribute returns the value "other" for type AUI.

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20.2.2.1.6 aMAUAdminState

ATTRIBUTE
APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

other	--undefined
unknown	--initializing, true state not yet known
operational	--powered and connected
standby	--inactive but on
shutdown	--similar to power down

BEHAVIOUR DEFINED AS:

A MAU in management state “standby” forces DI and CI to idle and the media transmitter to idle or fault, if supported. The management state “standby” only applies to link type MAUs. The state of MediaAvailable is unaffected. A MAU or AUI in the management state “shutdown” assumes the same condition on DI, CI, and the media transmitter as if it were powered down or not connected. For an AUI, this management state will remove power from the AUI. The MAU may return the value “undefined” for Jabber and MediaAvailable attributes when it is in this management state. A MAU in the management state “operational” is fully functional, and operates and passes signals to its attached DTE or repeater port in accordance to its specification.

20.2.2.1.7 aBbMAUXmitRcvSplitType

ATTRIBUTE
APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

other	--undefined
single	--single-cable system
dual	--dual-cable system, offset normally zero

BEHAVIOUR DEFINED AS:

Returns a value that indicates the type of frequency multiplexing/cabling system used to separate the transmit and receive paths for the 10BROAD36 MAU. All other types return “undefined.”

20.2.2.1.8 aBroadbandFrequencies

ATTRIBUTE
APPROPRIATE SYNTAX:

A SEQUENCE of two instances of the type INTEGER.
The first INTEGER represents the Transmitter Carrier Frequency. The value of its integer represents the frequency of the carrier divided by 250 kHz.
The second INTEGER represents the Translation Offset Frequency. The value of its integer represents the frequency of the offset divided by 250 kHz.

BEHAVIOUR DEFINED AS:

Returns a value that indicates the transmit carrier frequency and translation offset frequency in MHz/4 for the 10BROAD36 MAU. This allows the frequencies to be defined to a resolution of 250 kHz.

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20.2.2.2 MAU actions

20.2.2.2.1 acResetMAU

ACTION
APPROPRIATE SYNTAX:
None required.
BEHAVIOUR DEFINED AS:
Resets the MAU in the same manner as would a power-off, power-on cycle of at least 0.5 s duration. During the 0.5 s DO, DI, and CI should be idle.

20.2.2.2.2 acMAUAdminControl

ACTION
APPROPRIATE SYNTAX:
The same as used for **aMAUAdminState**
BEHAVIOUR DEFINED AS:
Executing an acMAUAdminControl action causes the MAU to assume the aMAUAdminState attribute value of one of the defined valid management states for control input. The valid inputs are “standby,” “operational,” and “shutdown” state (see the behaviour definition bMAUAdminState for the description of each of these states) except that a “standby” action to a mixing type MAU or an AUI will cause the MAU to enter the “shutdown” management state.

20.2.2.3 MAU notifications

20.2.2.3.1 nJabber

NOTIFICATION
APPROPRIATE SYNTAX:
The same as used for **aJabber**
BEHAVIOUR DEFINED AS:
The notification is sent whenever a managed MAU enters the jabber state.

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Annex A

(informative)

Additional reference material

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Annex B

(informative)

System guidelines

B.1 Baseband system guidelines and concepts, 10 Mb/s

B.1.1 Overall system objectives

The CSMA/CD Access Method, supported by baseband technology, depends on a variety of analog system components at and below the physical level of the OSI Reference Model. These components provide basic interconnection facilities for the CSMA/CD access mechanism itself and are defined throughout Clauses 6, 7, and 8.

Overall performance of the analog baseband medium and related physical layer capabilities depends on an optimal and known set of analog capabilities within each of these critical system elements: the coaxial trunk cable, MAUs, branch cables, DTEs, and repeater units. These system elements affect the integrity with which the serial data bit stream analog signals are carried between open systems. There are at least three critical parameters of interest: bits lost in the transmission system, signal delays, and phase jitter. It is important that these be apportioned properly among the affected system elements.

The successful interconnection of multivendor system components mandates that the values for bits lost, signal delays, and phase jitter be allocated fairly and realistically among the various system elements. The balance of Annex B identifies the upper limits of values to be placed on the subject parameters. These values are based on the maximal system configuration (for example, four repeater units, 2.5 km trunk coaxial cable medium).

B.1.2 Analog system components and parameter values

The values given in the following table are in terms of bits and are stated as maximum values except for values given within ranges.

The initial mnemonic under each component entry refers to the system component as identified in Figure B–1. System parameters are stated in terms of the intralayer or interlayer messages sent within a station. Specific delays are called out as = delay.

The repeater concepts described throughout this annex are considered to be an acceptable set of specifications for a multirepeatered system. It is noted that the exact parametric values specified for the repeater environment are subject to minor refinement.

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Component and parameter	Start-up delay	Last in to last out delay	Start-up loss
MEDIUM			
Trunk Coaxial Cable			
C1 Propagation	0.0	21.65	0.0
POINT TO POINT LINK			
P1 Propagation	0.0	25.64	0.0
AUI			
A1 Propagation	0.0	2.57	0.0
MEDIUM ACCESS UNIT			
M1 DATA IN ASSERT → INPUT	6.0	0.5	5.0
M2 OUTPUT → DATA OUT ASSERT	3.0	0.5	2.0
M3 DATA IN COLLISION → SQE ASSERT	17.0	—	—
M4 COLLISION DEASSERT → SQE DEASSERT	20.0	—	—
M5 OUTPUT IDLE → SQE ASSERT	$6 < x < 16$	—	—
M6 SQE TEST ASSERT → SQE DEASSERT	$5 \le x \le 15$	—	—
DTE			
D1 INPUT → INPUT UNIT	18.0	—	18.0
D2 OUTPUT UNIT → OUTPUT	—	3.0	—
D3 INPUT → CARRIER STATUS = CARRIER ON	3.0	—	—
D4 INPUT IDLE → CARRIER STATUS = OFF	$3.0 < x \le 6.0$	—	—
D5 SQE ASSERT → CARRIER STATUS = ON	3.0	—	—
D6 SQE DEASSERT → CARRIER STATUS = OFF	$3.0 < x \le 6.0$	—	—
D7 SQE ASSERT → SIGNAL STATUS = ERROR	3.0	—	—
D8 SQE DEASSERT → SIGNAL STATUS = NO ERROR	$3.0 < x \le 6.0$	—	—
D9 CARRIER STATUS = OFF → OUTPUT UNIT	$96 \le x \le$	—	—
D10 INPUT → OUTPUT	100	—	—
D11 SIGNAL STATUS = ERROR → JAM OUTPUT	8.0	—	—
D12 JAM OUTPUT DURATION	16.0	—	—
	=32.0		
REPEATER UNIT			$22 < x < 34$
R1 INPUT 1,2 → OUTPUT 2,1	7.5	—	—
R2 INPUT IDLE 1,2 → OUTPUT IDLE 2,1	—	12.5	—
R3 INPUT 1,2 → CARRIER STATUS = ON	3.0	—	—
R4 SQE → SOURCED OUTPUT	6.5	—	—
R5 JAM OUTPUT → OUTPUT IDLE	=96.0	—	—

Figure B–1 indicates the maximal system configuration and identifies the various system component parameters considered critical in determining analog system performance.

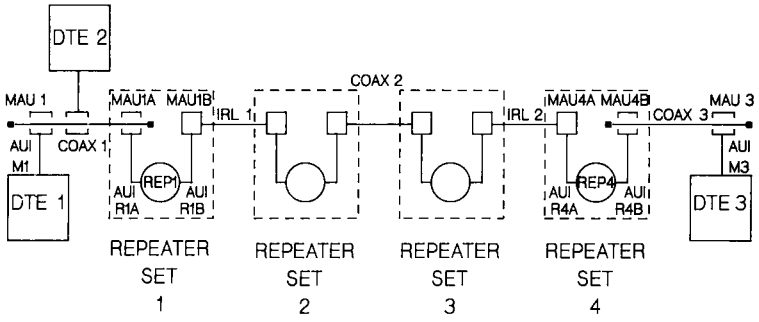


Figure B–1—Maximal system configuration bit budget apportionments

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B.1.3 Minimum frame length determination

The following table indicates the system elements that make up the minimum frame length calculation based on the worst-case numbers as outlined in the bit budget of B.1.2. The compilation in the following table is based on the following scenario:

a) DTE 1 transmits to an adjacent DTE 2 on coaxial segment 1.
b) DTE 3 transmission collides with DTE 1 transmission.
c) DTE 3 is assumed to be the worst-case distance from DTE 1 and its transmission just misses deferring to the DTE 1 message.
d) The collision fragment travels back down the network to inform DTE 1 that a collision has occurred on its message.

Component and function	Direction	Table entry	Delay	Total delay
DTE 1 STARTS TO PUT OUT FIRST BIT				0.0
DTE 1	FWD	D2	3.0	3.0
AUI M1	FWD	A1	2.57	5.57
MAU1	FWD	M2	3.0	8.6
COAX1	FWD	C1	21.65	30.2
REPEATER SET 1				
MAU 1A	FWD	M1	6.0	36.2
AUI R1A	FWD	A1	2.57	38.8
REP 1	FWD	R1	7.5	46.3
AUI R1B	FWD	A1	2.57	48.9
MAU 1B	FWD	M2	3.0	51.9
REPEATER SET TOTAL			21.64	
IRL 1	FWD	P1	25.64	77.5
REPEATER SET 2	FWD		21.6	99.1
COAX 2	FWD	C1	21.65	120.8
REPEATER SET 3	FWD		21.6	142.4
IRL 2	FWD	P1	25.64	168.1
REPEATER SET 4	FWD		21.6	189.7
COAX 3	FWD	C1	21.65	211.4
MAU 3	FWD	M1	6.0	217.4
AUI 3	FWD	A1	2.57	219.9
DTE 3 PUTS OUT A BIT	REV	D10	8.0	227.9
AUI 3	REV	A1	2.57	230.5
MAU 3	REV	M2	3.0	233.5
COAX 3	REV	C1	21.65	255.1
REPEATER SET 4				
MAU 4B	REV	M3	17.0	272.1
AUI 4B	REV	A1	2.57	274.7
REP 4	REV	R4	6.5	281.2
AI 4A	REV	A1	2.57	283.8
MAU 4A	REV	M2	3.0	286.8
REPEATER SET TOTAL			31.64	
IRL 2	REV	P1	25.64	312.4
REPEATER SET 3	REV		31.64	344.1
COAX 2	REV	C1	21.65	365.7
REPEATER 2	REV		31.64	397.4
IRL 1	REV	P1	25.64	423.0
REPEATER SET 1	REV		31.64	454.6
COAX 1	REV	C1	21.65	476.3
MAU 1	REV	M3	17.0	493.3
AUI M1	REV	A1	2.57	495.9
DTE 1	REV	D7	3.0	498.9

The frame length is constrained by two parameters:

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— The message from DTE 1 shall be long enough so that it is still sending when the collision is detected.
— The message from DTE 1 shall be short enough such that DTE 2 can throw out the message on the basis of being too short.

The above table provides the scenario that enables DTE 1 to determine a collision is taking place. DTE 1 shall transmit for at least 499 bit times. To determine how much longer DTE 2 will continue to receive bits, assume that DTE 1 is the last transmitter to provide bits to the DTE 2 MAU. DTE 2 then sees the following:

Component and function	Direction	Table entry	Delay	Total delay
DTE 1	FWD	D11	16.0	514.9
DTE 1	FWD	D12	32.0	547.9
AUI M1	FWD	A1	2.57	549.4

If Repeater Set 1 is the last system component to provide bits to DTE 2, then DTE 2 will see the following:

Component and function	Direction	Table entry	Delay	Total delay
REPEATER SET 1 (1st JAM BIT)				454.6
REP 1	REV	R5	96.0	550.6
COAX 1	REV	C1	21.65	572.3

The Repeater Set is the last transmitter to provide a bit to DTE 2. The DTE 2 MAU starts seeing bits at time 8.6, which means that DTE 2 sees 563.7 bits (572.3 – 8.6). DTE 2 sees a minimum of 61 preamble bits and 8 SFD bits. The preamble and SFD bits can be deleted from the 563.7 total because they are not counted in minimum frame length.

The minimum frame length determination from the above scenario is then 564.7 – 69.0 = 494.7 bits. The 10 Mb/s system value for minimum frame length has been set at 512 bits.

B.1.4 System jitter budgets

The typical jitter budget expected for the baseband system is apportioned in the following manner:

Encoder	0.5 ns
AUI Cable	1.0 ns (transmit end)
MAU Transmit	2.0 ns
Trunk Coax	7.0 ns
MAU Receive	–1.0 ns (with compensation)
AUI Cable	1.0 ns (receive end)
SNR on COAX	5.0 ns (SNR = 5:1)
SNR on AUI	0.5 ns (SNR = 5:1, transmit end)
SNR on AUI	0.5 ns (SNR = 5:1, receive end)
	16.5 ns

The 18 ns jitter budget leaves adequate design margin for implementation-dependent considerations.

B.1.4.1 Nominal jitter values

The jitter budget values given above are not expected to accommodate all step changes in phase jitter due to system parameter variations within one or a few bit times.

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B.1.4.2 Decoder evaluation

The phase decoder in the PLS sublayer should correctly decode a Manchester-encoded signal whose data transition point (center of a bit cell) has a peak-to-peak jitter of no more than 36 ns (± 18 ns deviation from the bit cell center). Figure B–2 and Figure B–3 show the test method.

Evaluation of decoder performance may be simulated and tested by application of three distinct waveforms representing worst-case and normal conditions. The waveforms contain Manchester-encoded bits whose center transitions represent the extremes of maximum skew. A 5 MHz (repetition rate) pulse train whose pulse width is either 64 ns or 136 ns simulates the two worst-case jitter conditions. The data output from the decoder should remain stable for each of the three test patterns and shifts between these extremes where there is a low rate of change in center transition skew. Note that the actual transmission system is not expected to permit sudden drastic changes in the steady-state edge deviation during the reception of any given frame. The above evaluation process is not intended to guarantee proper decoder performance under all operating conditions.

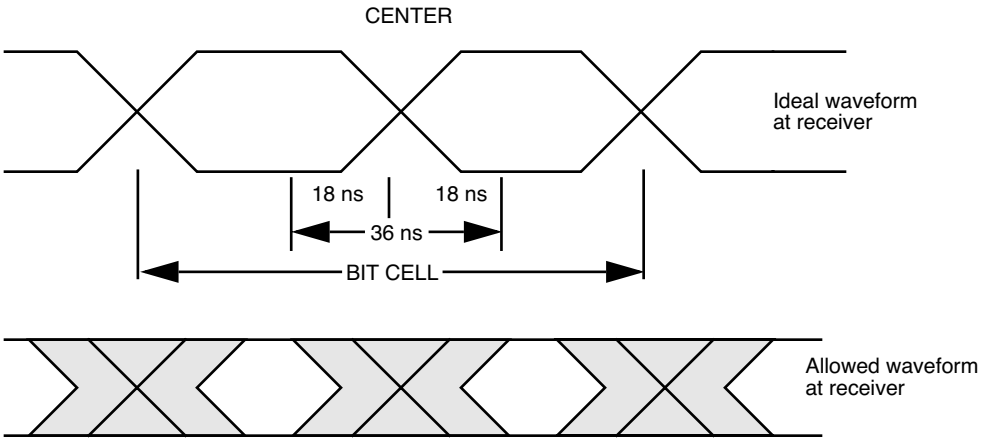


Figure B–2—Typical signal waveforms

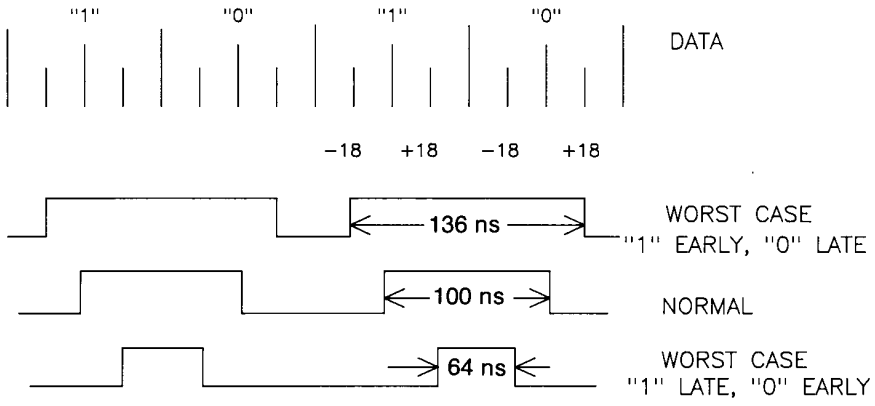


Figure B–3—Worst-case signal waveform variations

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B.1.5 Systems consideration calculations

B.1.5.1 Overview

Subclause B.1.3 contains a calculation of maximum fragment size for a network of 10BASE5 and IRL segments. That calculation was based on the maximum delay for a transmission to reach the far end of the network and for a collision to propagate back. Since that calculation was written, many new media and MAU types have been added to this standard. Also, the calculation of B.1.3 did not address the interpacket gap shrinkage, which can limit the network size. It is not practical to perform a separate calculation for each possible combination of segment types.

Some new segment types also support much longer media (up to 2 km). Introduction of longer media also required a more flexible calculation method that allowed trading segment length for repeaters. The method in this section was developed to meet these needs.

Actual numbers used to calculate delay and variability are tabulated (Table B–1) at the end of this subclause.

B.1.5.2 Maximum collision fragment size

The round-trip delay must be calculated to determine that collision will be received within the collision window of transmitting DTEs and that collision fragments will be less than the minimum frame size. The following scenario is used for the calculations (see Figure B–4):

a) DTE1 transmits.
b) DTE1's transmission propagates to DTE2.
c) DTE2 begins transmitting at the last possible time, colliding and transmitting 96 bits.
d) DTE2's transmission propagates to DTE1.
e) DTE1 detects collision, jams, and stops transmitting.

The following conditions must be met for proper network operation:

— DTE1 must detect collision before having transmitted the 512th bit (including preamble and SFD bits).
— DTE1 must stop transmitting before having transmitted a minimum length frame, 576 bits (512 bits after SFD).
— The overlap between DTE1's transmission and DTE2's transmission must be less than 575 bits (511 bits after the SFD transmitted by DTE1).

For all existing segment types, the last condition is the limiting factor; if it is met then the other two conditions are also met.

The maximum time between the first bit and the last bit of the overlapping transmissions of the two DTEs colliding across a path will be called the Path Delay Value (PDV). Many factors contribute to this delay. Simplification of the delay calculation, as compared to the method used in B.1.3, can be achieved by using a set of base numbers, Segment Delay Values (SDV), for each segment type that combines the factors that contribute to the round-trip delay associated with that segment. The PDV is the sum of SDVs of the segments that comprise the path.

For each segment type, one of three base SDVs is used depending on the position of the segment: left-end, mid-, or right-end. The left-end segment is connected to the DTE that transmits first (DTE1). The right-end segment is connected to the colliding DTE (DTE2). All segments between these are mid-segments.

For this calculation, the left-end base SDV contains all delays from DTE1 through the MAU and its AUI connected to the repeater unit. Each mid-base SDV includes the delays from the repeater unit on the left

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through the MAU and its AUI connected to the right repeater unit. The right-end base SDV includes the delays from the repeater unit immediately to its left through DTE2. (See Figure B–4.)

Only the bit loss of DTE1's MAU on the left-end segment contributes to fragment size. The steady-state delay of that MAU and the AUI cable delay do not contribute. For the remainder of the network, start-up delay (the sum of steady-state delay and bit loss) contribute. Therefore, the left-end base SDV uses MAU transmit bit loss and 1 AUI delay. In all other cases, start-up delay and 2 AUI delays are used.

Propagation delays for media are not included in the base SDVs. These are added in separately to allow for various segment lengths (see 13.4.1). The base SDVs for the mid- and right-end segments (except 10BASE-FB) include two 2 m AUI cables and the delay of each one is experienced twice, once in the forward path and once in the reverse path. Therefore, a delay of 0.5 BT per segment is added and corresponds to the round-trip delay through two 2 m AUI cables. The base numbers for the left segment include one 2 m AUI cable, 0.25 BT.

For each segment type, both the delay to transmission of the 96th bit after collision rise and delay to transmission of the last bit due to collision fall are calculated. The base SDV is the larger of these two.

The maximum allowed sum of SDVs plus media propagation delays is 575 BT.

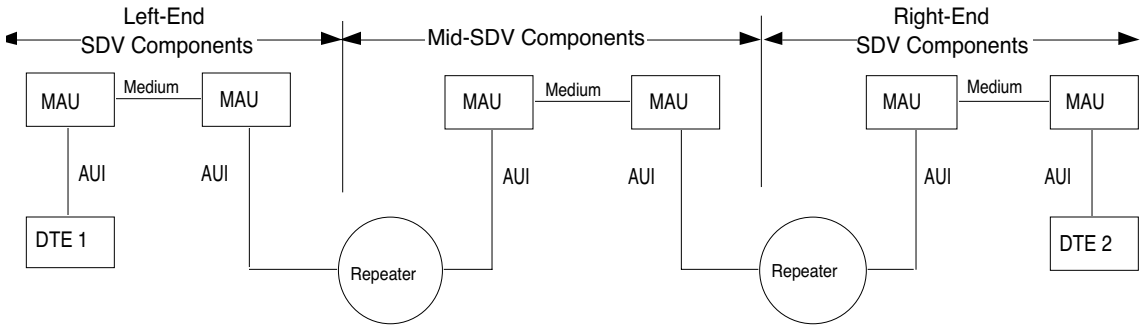


Figure B–4—Round-trip delay calculation model

B.1.5.2.1 Left-end base SDV

The Left-End Segment collision delay is the sum of the following:

Forward delay:
- AUI
- MAU transmit bit-loss delay
- Media rise time
- MAU receive start-up delay

Reverse delay:
- MAU transmit fall delay after collision
- MAU receive fall delay after collision

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B.1.5.2.2 Mid-base SDV

The Mid-Segment collision rise delay is the sum of the following:

Forward delay:
- AUI * 2
- Repeater start-of-packet propagation delay
- MAU transmit start-up delay
- Media rise time
- MAU receive start-up delay

Reverse delay:
- MAU transmit start-up delay
- MAU collision detect delay
- Repeater start-of-collision propagation delay

The Mid-Segment collision fall delay is the sum of the following:

Forward delay:
- AUI * 2
- Repeater start-of-packet propagation delay
- MAU transmit start-up delay
- Media rise time
- MAU receive start-up delay

Reverse delay:
- MAU transmit fall delay
- MAU collision fall delay
- Repeater cessation-of-jam propagation delay

B.1.5.2.3 Right-end base SDV

The Right-End Segment collision rise delay is the sum of the following:

Forward delay:
- AUI * 2
- Repeater start-of-packet propagation delay
- MAU transmit start-up delay
- Media rise time
- MAU receive start-up delay
- DTE receive-to-transmit-not-deferred delay

Reverse delay:
- MAU transmit start-up delay
- MAU collision detect delay
- Repeater start-of-collision propagation delay
- Repeater minimum transmit length

The Right-End Segment collision fall delay is the sum of the following:

Forward delay:
- AUI * 2
- Repeater start-of-packet propagation delay
- MAU transmit start-up delay

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Media rise time
MAU receive start-up delay
DTE receive-to-transmit-not-deferred delay
DTE minimum transmit length

Reverse delay:
MAU transmit fall delay
MAU collision fall delay
Repeater cessation-of-jam propagation delay

B.1.5.3 Interpacket Gap (IPG) shrinkage

IPG shrinkage occurs because two successive packets may experience differing bit loss on the same path. When the packet passes through a repeater, the lost preamble bits are regenerated. If the first packet experiences greater bit loss than the second, the IPG between them will shrink.

IPG shrinkage is also calculated using a lumped number for each segment, the Segment Variability Value (SVV). For each segment type, one of two SVVs is used depending on the position of the segment: transmitting end or mid. The transmitting end segment is connected to the transmitting DTE or DTEs. The mid-segments are all the remaining segments except the one connected to the receiving DTE.

The transmitting end segment and the mid-segment SVVs each include the variability from the transmitting MAU through the repeater unit. Since, IPG shrinkage only occurs when a repeater restores the lost bits, the final segment does not contribute any variability (see Figure B–5).

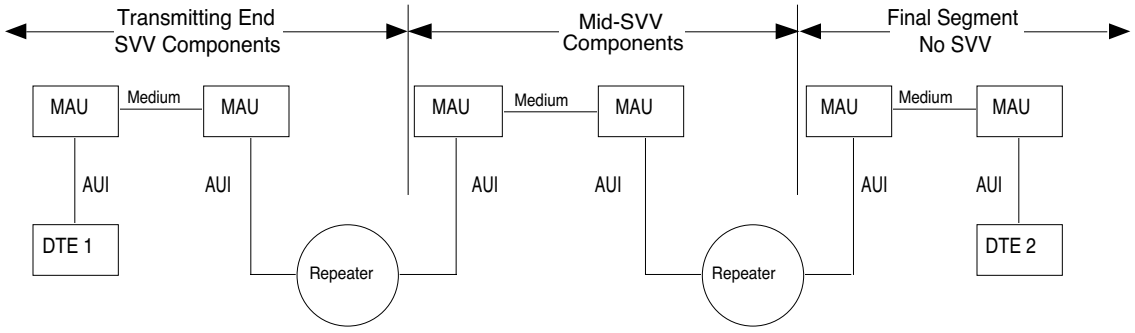


Figure B–5—Variability calculation model

B.1.5.3.1 Transmitting end segment variability value

The transmitting end segment variability value is the sum of the following:
MAU transmit start-up-delay variability
MAU transmit start-up-delay variability correction
MAU receive start-up-delay variability
MAU receive start-up-delay variability correction
Repeater start-of-packet propagation delay variability
Clock skew (2.5 BT)

NOTE—The variability correction values account for the possibility that on mixing segments the two successive packets can be originated by two different MAUs.

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B.1.5.3.2 Mid-segment variability value

The mid-segment variability value is the sum of the following:

MAU transmit start-up-delay variability
MAU receive start-up-delay variability
Repeater start-of-packet propagation delay variability

B.1.5.4 Timing parameters for round-trip delay and variability calculations

Table B–1 contains the timing parameters used in the calculation of SDVs and SVVs. The values in the table for MAU Collision Rise and MAU Collision Fall are those specific to the worst-case scenario. The parameters are defined in the following subclauses.

B.1.5.4.1 MAU parameters

Transmit Bit Loss: Number of bits received on the DO circuit and not transmitted to the MDI.

Transmit Start-up Delay: Delay from the first bit received on the DO circuit to the first bit transmitted to the MDI. This is the sum of transmit bit loss and steady-state delay.

Receive Start-up Delay: Delay from the first bit received on the MDI to the first bit transmitted to the DI circuit. This is the sum of receive bit loss and steady-state delay.

Collision Detect Delay: Delay from the arrival of collision at the MDI to transmission of signal_quality_error to the CI circuit. For 10BASE2 and 10BASE5, this includes the DC rise time on the media, given that the MAU has been transmitting for at least 20 BT when the collision arrives. For 10BASE-FP, this includes the delay until the second CRV occurs on the media (16.3.4.3).

Transmit Fall Delay: Delay from the last bit received on the DO circuit to the last bit transmitted to the MDI. This is the same as the steady-state delay.

Collision Fall Delay: Delay from arrival of end of collision at the MDI to end of transmission of signal_quality_error to the CI circuit. For 10BASE2 and 10BASE5, it includes the DC fall time of the media. For 10BASE-FP it includes the delay of 33 BT to pass with no more than one ORD_crv.

Transmit Start-up Delay Variability: Packet-to-packet variations in transmit start-up delay.

Transmit Start-up Delay Variability Correction: Additional variability, when the transmitting end segment is a mixing segment, due to two MAUs transmitting with different start-up delays. For 10BASE5 and 10BASE2, start-up delay variability plus transmit start-up delay variability correction equal transmit start-up delay since these MAUs may transmit with as little as 0 BT delay. For 10BASE-FP MAUs, implementation considerations imposed by the requirements of 16.3.1.1 require the MAU to have at least 2 BT start-up delay. Therefore, the transmit start-up delay variability correction equals the transmit start-up delay minus 2 BT.

Receive Start-up Delay Variability: Packet-to-packet variability in receive start-up delay.

Transmit Fall Delay After Collision: Delay from the last bit received on the DO circuit to the last bit transmitted to the MDI after the MAU has detected a collision. For all MAUs except 10BASE-FB, this is the same as transmit fall delay.

Receive Fall Delay After Collision: Delay from the last bit received on the MDI to the last bit transmitted to DI. For all MAUs except 10BASE-FB and 10BASE-FP, this is the same as receive steady-state delay.

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B.1.5.4.2 Repeater parameters

Start-of-Packet Propagation Delay: Delay from first bit received on DI to first bit transmitted on DO.

Start-of-Collision Propagation Delay: Delay from start of signal_quality_error on CI to first bit transmitted on DO.

Cessation-of-Jam Propagation Delay: Delay from end of signal_quality_error on CI to last bit transmitted on DO.

Minimum Transmit Length: Minimum delay from first bit transmitted on DO to last bit transmitted on DO.

Start-of-Packet Propagation Delay Variability: Packet-to-packet variation in start-of-packet propagation delay.

B.1.5.4.3 Media parameters

Media Rise Time: Start-of-packet DC rise time on 10BASE2 and 10BASE5 segments.

B.1.5.4.4 DTE parameters

Receive-to-Transmit-Not-Deferred Delay: Delay from first bit on DI to first bit on DO when the DTE does not detect carrier in time to defer.

Minimum Transmit Length: Minimum delay from first bit transmitted on DO to last bit transmitted on DO.

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Table B–1—Timing parameters for round-trip delay and variability calculations in bit times (BT)

Parameter	10BASE 5	10BASE 2	FOIRL	10BASE -T	10BASE-FP	10BASE-FB	10BASE-FL
AUI (2 m)	0.25	0.25	0.25	0.25	0.25	0.00	0.25
MAU							
Transmit bit loss	3.00	3.00	3.00	3.00	2.00	0.00	3.00
Transmit start-up delay	3.50	3.50	3.50	5.00	5.50	2.00	5.00
Receive start-up delay	6.50	6.50	3.50	8.00	2.50	2.00	5.00
Collision detect delay	17.00	17.00	3.50	9.00	9.50	3.50	3.50
Transmit fall delay	0.50	0.50	0.50	2.00	3.50	2.00	2.00
Collision fall delay	20.00	20.00	7.00	9.00	36.00	5.00	7.00
Transmit start-up delay variability	2.00	2.00	2.00	2.00	3.00	0.00	2.00
Transmit start-up delay variability correction	1.50	1.50	0.00	0.00	0.50	0.00	0.00
Receive start-up delay variability	5.00	5.00	2.00	2.00	1.00	0.00	2.00
Receive start-up delay variability correction	1.00	1.00	0.00	0.00	0.00	0.00	0.00
Transmit fall delay after collision	0.50	0.50	0.50	2.00	3.50	5.00	2.00
Receive fall delay after collision	0.50	0.50	0.50	2.00	3.00	5.00	2.00
REPEATER							
Start-of-packet propagation delay	8.00	8.00	8.00	8.00	8.00	8.00	8.00
Start-of-collision propagation delay	6.50	6.50	6.50	6.50	6.50	6.50	6.50
Cessation-of-jam propagation delay	5.00	5.00	5.00	5.00	5.00	5.00	5.00
Minimum transmit length	96.00	96.00	96.00	96.00	96.00	96.00	96.00
Start-of-packet propagation delay variability	4.00	4.00	4.00	4.00	4.00	2.00	4.00
MEDIA RISE TIME	1.00	1.00	0.00	0.00	0.00	0.00	0.00
DTE							
Receive-to-transmit-not-deferred delay	27.00	27.00	27.00	27.00	27.00	N/A[a]	27.00
Minimum transmit length	96.00	96.00	96.00	96.00	96.00	N/A[a]	96.00

[a]Not applicable; 10 BASE-FB does not support end (DTE) connections.

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B.2 System parameters and budgets for 1BASE5

B.2.1 Delay budget

The successful interconnection of multivendor system components mandates that the values for bits lost and signal delays be allocated fairly and realistically among the various system elements. The following table summarizes and indicates the derivation of some of the delays specified in 12.9. The breakdowns shown for the parameters are illustrative only; implementors are free to make other allocations of delay *within* a device so long as the specifications of 12.9 are not violated.

Component	Delay (BT)
DTE Initial Transmit Delay (see 12.9.2)	**3**
DTE Deference Delay (see 12.9.2)	**21**
unsquelch	3
Carrier detect	5
MAC detects carrier and defers	10
DTE Initial Transmit Delay	3
DTE Collision Shutdown Delay (see 12.9.2)	**58**
detect CP and report SIGNAL_ERROR	10
detect SIGNAL_ERROR and start jamming	16
jamSize	32
Medium Transit Delay (see 12.9.3)	**4**
Special Link Transit Delay (see 12.9.4)	**15**
Hub Startup Delay (see 12.9.5)	**12**
unsquelch	4
half fill FIFO	6
analogue of DTE Initial Transmit Delay	3
Hub Idle Collision Startup Delay (see 12.9.5) (same as Hub Startup Delay)	**12**
Hub Transit Delay (see 12.9.5)	**9**
half fill FIFO	6
analogue of DTE Initial Transmit Delay	3
Hub Delay Stretch/Shrink (see 12.9.5) ((preamble + <sfd> + maxFrameSize) · 0.01% · 2)	**3**
Hub Collision Detect Delay (see 12.9.5)	**21**
unsquelch	3
detect collision	6
Hub Transit Delay	9
First CVL or CVH may be preceded by CD0s and CD1s	3
Hub Active Collision Startup Delay (see 12.9.5)	**12**
Hub Transit Delay	9
First CVL or CVH may be preceded by CD0s and CD1s	3
Hub Collision Shutdown Delay (downward) (see 12.9.5) (same as Hub Transit Delay)	**9**
Hub Collision Shutdown Delay (upward) (see 12.9.5)	**25**
detect loss of carrier	20
clear FIFO, if necessary	2
analogue of DTE Initial Transmit Delay	3

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B.2.2 Minimum frame length determination

The minimum frame length for 1BASE5 is determined using the values specified in 4.4.2.2 and 12.9, applied to the following (worst) case:

a) DTE 1, connected to Hub 1 at a network extremity, transmits a message upward toward Hub 5.
b) There is a special link in the path between Hub 1 and Hub 5.
c) DTE 2, also connected to Hub 1, transmits, just missing deferring to the downward signal from DTE 1 that was wrapped around at Hub 5.
d) DTE 3, also connected to Hub 1, receives the transmission from DTE 1.
e) Hub 1 generates CP, which travels up and then back down the network to inform DTE 1 and DTE 2 that a collision has occurred on their messages.
f) DTE 1 and DTE 2 continue to transmit until they have received CP, reacted to it, and completed their jams.
g) DTE 3 continues to receive until the end of CP.

The minimum frame length must allow both of the following conditions to be met:

— DTE 1 is still sending when CP is received and recognized.
— DTE 3 can discard the message fragment it receives because it is too short.

Event	Bits	Total
DTE 1 → DTE 2		
DTE Initial Transmit Delay	3	3
8 · Medium Transit Delay	32	35
2 · Special Link Transit Delay	30	65
10 · Hub Startup Delay	120	185
DTE Deference Delay	21	206
DTE 2 → HUB 1 CP		
Medium Transit Delay	4	210
Hub Collision Detect Delay	21	231
HUB 1 CP → HUB 5 CP		
3 · Medium Transit Delay	12	243
Special Link Transit Delay	15	358
4 · max(Hub Startup Delay, Hub Active Collision Startup Delay, Hub Idle Collision Startup Delay)	48	306
HUB 5 CP → DTE 1 receives CP		
5 · Hub Active Collision Startup Delay	60	366
4 · Medium Transit Delay	16	382
Special Link Transit Delay	15	397
DTE 1 receives CP → DTE 1 stops transmitting DTE Collision Shutdown Delay	58	455
COMPUTATION OF MINIMUM FRAME SIZE	–64	391 =
original preamble + <sfd>		data bits transmitted
5 · (Hub Collision Shutdown Delay (upward) – Hub Transit Delay)	80	471
5 · (Hub Collision Shutdown Delay (downward) – Hub Transit Delay)	0	471
Tiny fraction of Hub Delay Stretch/Shrink	0	471 = data bits received

The minimum frame length must exceed both the maximum number of bits sent before recognizing CP (391 – jamsize = 359) and the maximum collision fragment size (471), as computed above. The 1BASE5 system

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value for minimum frame length has been set at 512 bits, which exceeds both of these values with a margin for error.

B.2.3 Jitter budget

The total edge jitter of the signals on each link must be limited to allow proper decoding at the receiver. The following budget has been used to allocate jitter to the indicated components that contribute to the total jitter on each link:

Component	Jitter (ns)
Transmitter skew	±10
Cable intersymbol interference	9
Cable reflections	8
Reflections due to receiver termination mismatch	5
Total	±32

The cable intersymbol interference and reflection allowances form the basis for the limit specified in 12.7.2.3; the reflection component is sufficient to allow a single 20 Ω impedance mismatch anywhere along a cable segment. The receiver-mismatch allowance is derived from the reflection attenuation specified in 12.5.3.2.4. The total forms the basis for the specification in 12.5.3.2.2.

The remainder of the jitter that can be tolerated by the Manchester decoder in a receiver is reserved to allow for distortion of the signal due to noise, receiver threshold offset, receiver skew, and receiver sampling timing error.

A simple clocked receiver/decoder with an 8 MHz sampling rate (the worst case allowed for in the design of this standard), can achieve proper decoding with up to ± 125 ns of jitter between two edges, which is equivalent to ±62.5 ns on each edge. Other receiver designs may tolerate more edge jitter. For example, a 6 MHz sampling rate would allow up to ±83.33 ns of jitter on each edge and a 16 MHz sampling rate allows up to ±93.75 ns of jitter.

It may be necessary to use a low-pass filter as part of the receiver to reduce the noise level seen by that receiver (see 12.7.4 for a description of the noise environment). A filter that reduces the noise may also have an effect on the amplitude and edge rate of the received signal. The filtered signal's edge rate near the zero-crossing is used in the critical translation from mV of noise and receiver offset into ns of jitter.

An example receiver design using an 8 MHz sampling rate and a 2 MHz Butterworth input filter might be based on the following jitter budget:

Component	Jitter (ns)
Input jitter (from above)	±32
Noise and receiver threshold offset	19.5
Receiver skew (analog)	4
Receiver skew (digital)	7
Total	±62.5

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The two primary contributors to noise in a 1BASE5 cable are self-crosstalk and impulse noise (see 12.7.4). Because it is unlikely that both will be present at their 1% worst-case levels on any particular cable, the required bit error rate attributable to each source can be set at half of the one in 10^8 error rate required by 12.5.3.2.6.

Crosstalk noise is specified to be no more than 105 mV (peak) through a 2 MHz filter (see 12.7.4.2). Because crosstalk is present for the entire transmission of a packet, some crosstalk will coincide with the most sensitive part of the received signal. Therefore, the receiver must operate without error in the presence of this 105 mV of noise.

Impulse noise has a peak amplitude of 170 mV for ≤0.005 counts/s through the 2 MHz filter (see 12.7.4.1). This threshold does not directly correlate to jitter, however, because the derivation of the 62.5 ns jitter tolerance for an 8 MHz clock assumed worst-case sampling error. Assuming a random phasing of the sampling clock to the received signals, it can be shown that the 170 mV of noise is equivalent to a level of 85 mV with a worst-phase clock.

Jitter due to noise should be computed using the larger of the above two levels. The 105 mV for crosstalk noise, therefore, should be added to 50 mV for receiver threshold offset and the result should be divided by the edge rate of the filtered signal near the zero-crossing (7.9 mV/ns for the 2 MHz filter), yielding the 19.5 ns indicated above.

B.3 Example crosstalk computation for multiple disturbers, balanced-pair cable

A method for computing multiple-disturber, near end, crosstalk attenuation (MDNEXT) into each 1BASE5 pair is specified in 12.7.3.2. This annex provides example computations of MDNEXT using that method when only the distribution of X_{ij} is known.

The single-disturber probability distribution curve (labelled "1") shown in Figure B–6 is based on actual measurement of 25-pair, 24-gauge, unshielded, twisted pair cable. The remaining probability distribution curves (labelled with the number of disturbing pairs) were computed using Monte Carlo simulation. To compute each sample $MDNEXT_j$ for N disturbers, N values of crosstalk attenuation (X_i) were chosen from the single-disturber distribution and N values of crosstalk phase (θ_i) were chosen from a uniform distribution between 0 and 2π rad. These values were then used with the following equations to compute $MDNEXT_j$:

$$H_j = \sum_{1 \le i \le N} 10^{(-X_i/20)} \cos\theta_i$$

$$V_j = \sum_{1 \le i \le N} 10^{(-X_i/20)} \sin\theta_i$$

$$MDNEXT_j = 10\log_{10}(H_j^2 + V_j^2)$$

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Iterating this process several hundred times, each time producing a single $MDNEXT_j$ sample, resulted in distributions for MDNEXT that are summarized in the following table and Figure B–6:

Disturbers	Iterations	MDNEXT: Mean (dB)	Std. Dev. (dB)	99% (dB)
1		61.2	7.0	48.6
2	500	57.2	6.2	46.4
3	500	55.1	5.8	45.2
6	500	52.0	5.7	42.5
13	1000	48.5	5.4	39.1
18	500	47.1	5.3	37.8
24	500	45.9	5.9	36.2

Because two pairs are used for each 1BASE5 connection, the entries in this table for 18 and 24 disturbers are not applicable for normal installation of 25-pair cables. Furthermore, telephone cables with larger numbers of pairs are often constructed using sub-bundles of 25 pairs each and so might yield similar results (for example, the curves for 13 or fewer disturbers would be the most applicable ones).

The calculation method of this annex, though not the numeric values, applies to 10BASE-T.

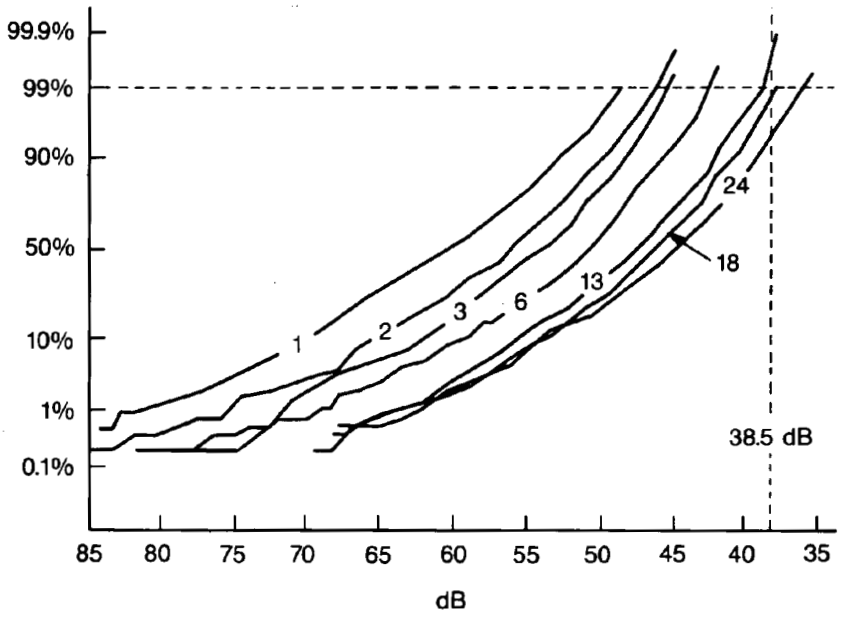


Figure B–6—MDNEXT cumulative probability distribution

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B.4 10BASE-T guidelines

B.4.1 System jitter budget

The jitter budget for 10BASE-T is apportioned as follows:

Jitter budget	Maximum-length twisted-pair link	Short-length twisted-pair link
	(jitter expressed in ±ns)	
Encoder	0.5	0.5
AUI cable including SNR (DO pair)	1.5	1.5
MAU transmitter	2.0	2.0
Twisted-pair medium with equalization	1.5	6.0
Noise jitter on twisted-pair medium	8.0	2.5
MAU receiver	1.5	1.5
AUI cable including SNR (DI pair)	1.5	1.5
Total	16.5	15.5

NOTE—Total transmit jitter for the combination of the MAU transmitter and link segment (14.3.1.2.3) is ±3.5 ns and ±8.0 ns for maximum- and short-length twisted-pair link segments, respectively. It is the sum of the entries for MAU transmitter and twisted-pair medium with equalization. The individual components cannot be easily observed on MAUs. Short-length segment is defined as a short, non-zero-length twisted-pair link. A short- rather than a zero-length segment is used in the calculation since a zero-length segment will have no significant noise and is a less severe case.

B.4.2 Filter characteristics

The implementation of the 3-pole, low-pass Butterworth filter should have the following characteristics:

3 dB cutoff frequency	15 MHz
Insertion loss (5 MHz to 10 MHz)	≤1.0 dB
30 MHz attenuation	≥17.5 dB
Input impedance (5 MHz to 10 MHz)	100 Ω
Return loss with 100 Ω load (5 MHz to 10 MHz)	≥20 dB

This filter is only used for the tests described in 14.3.1.3.2, 14.4.4.1, and 14.4.4.2. A buffer may be needed to achieve the above return loss when using an LC implementation of this filter.

B.4.3 Notes for conformance testing

The following notes are provided to assist in developing the conformance test.

B.4.3.1 Notes for 14.3.1.2.1 on differential output voltage

For testing harmonics measured on the TD circuit when the DO circuit is driven by an all-ones Manchester-encoded signal, it is acceptable to use a pattern of maximum length packets whose data field is all ones.

For testing of the maximum and minimum output signal to the template in Figure 14–9, the recommended measurement procedure is described as follows. An oscilloscope set for a zero voltage trigger with a positive slope is allowed to accumulate an eye pattern that must be within the template. Acquisition must be long

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enough to ensure that all data variations have been observed. When using packetized data, the TP_IDL and the first transmitted bit should be excluded from this measurement. Also, the interpacket interval may be adjusted so that transition-to-idle transient effects are excluded. When testing with the inverted template, the slope of the scope trigger should be negative.

B.4.3.2 Note for 14.3.1.2.2 on transmitter differential output impedance

The return loss (RL) is defined as follows:

$$RL = 20\log_{10}\frac{|Z_{transmitter} + Z_{cable}|}{|Z_{transmitter} - Z_{cable}|}$$

and also

$$RL = 20\log_{10}\frac{|V_i|}{|V_r|}$$

where

$Z_{transmitter}$ is the impedance of the transmitter
Z_{cable} is the impedance of the cable
V_i is the differential voltage incident upon the transmitter
V_r is the differential voltage reflected from the transmitter

a) A transmitter with a purely resistive source impedance of 96 Ω ± 20% will satisfy this requirement.
b) The requirement of 14.3.1.2.2 is equivalent to the following two constraints:
   1) The return loss when measured with an 85 Ω resistive source is at least 15 dB in the frequency range of 5 MHz to 10 MHz.
   2) The return loss when measured with a 111 Ω resistive source is at least 15 dB in the frequency range of 5 MHz to 10 MHz.

B.4.3.3 Note for 14.3.1.2.3 on output timing jitter

Adherence to the template of 14.3.1.2.1 with a jitterless source driving DO and the zero crossings constrained to 46.5 ns to 53.5 ns and 96.5 ns to 103.5 ns is sufficient to demonstrate compliance with the 3.5 ns jitter requirement. When measuring an integrated MAU, the zero crossing time interval should be constrained to 44.5 ns to 55.5 ns and 94.5 ns to 105.5 ns due to the additional allocation for encoder and AUI jitter. This test is simpler to perform than the test which follows, but failure of this test does not demonstrate noncompliance.

When triggering on one edge of the transmitted signal and observing another edge, the observed jitter measures the difference between the jitter of the triggering edge and the observed edge. When the two edges are separated such that the jitter of the edges is independent and clock drift is insignificant, the observed jitter is twice that of a single edge.

Therefore, a test that demonstrates compliance or noncompliance is as follows: Observe the zero crossings 8 BT and 8.5 BT from the triggering zero crossing while transmitting a pseudo-random data sequence of at least 511 bits. An external MAU with a jitterless source driving DO is compliant when all zero crossings fall within the time intervals 8.0 BT ± 7 ns and 8.5 BT ± 7 ns. An integrated MAU is compliant when all zero crossings fall within the time intervals 8.0 BT ± 11 ns and 8.5 BT ± 11 ns.

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When using packetized data, the TP_IDL and the first transmitted bit should be excluded from these measurements.

B.4.3.4 General note on common-mode tests

When performing tests specified as balanced or common-mode, the balance of the test equipment (such as matching resistors) must exceed that required by the test.

B.4.3.5 Note for 14.3.1.3.4 on receiver differential input impedance

The return loss (RL) is defined as follows:

$$RL = 20\log_{10}\frac{|Z_{receiver} + Z_{cable}|}{|Z_{receiver} - Z_{cable}|}$$

and also

$$RL = 20\log_{10}\frac{|V_i|}{|V_r|}$$

where

$Z_{receiver}$ is the impedance of the receiver
Z_{cable} is the impedance of the cable
V_i is the differential voltage incident upon the receiver
V_r is the differential voltage reflected from the receiver

a) A receiver with a resistive input impedance of 96 Ω ± 20% will satisfy this requirement.
b) The requirement of 14.3.1.3.4 is equivalent to the following two constraints:
   1) The return loss when measured with an 85 Ω resistive source is at least 15 dB in the frequency range of 5 MHz to 10 MHz.
   2) The return loss when measured with a 111 Ω resistive source is at least 15 dB in the frequency range of 5 MHz to 10 MHz.

B.4.3.6 Note for 14.3.1.3.3 on receiver idle input behavior

For conformance testing of receivers, the start of idle shall conform to the template shown in Figure 14–10. Additionally, the magnitude of the voltage-time integral of the undershoot (measured from the negative zero crossing that ends the positive idle pulse to the time when the differential signal settles to 0.0 mV ± 50 mV) shall be no greater than 1.2 times the voltage-time integral of the positive idle pulse (measured from the last positive zero crossing to the negative zero crossing).

B.4.3.7 Note for 14.3.1.3.5 on receiver common-mode rejection

For a stand-alone MAU, the receiver common-mode test may be performed with a jitterless E_s, so that the DI circuit should have no more than 4.0 ns of edge jitter.

For an integrated MAU, the common-mode test is performed with an E_s that has zero crossing jitter up to 11 ns from the ideal.

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B.5 10BASE-F

B.5.1 System jitter budget

The jitter budgets for 10BASE-FP, 10BASE-FB, and 10BASE-FL are apportioned as shown in Table B–2.

Table B–2—System jitter budgets

Encoder	10BASE-FP	10BASE-FB	10BASE-FL
Encoder	0.5	0.5	0.5
AUI Cable including SNR (DO Pair)	1.5	N/A	1.5
MAU DO Receiver (10BASE-FP only)	2.0	N/A	N/A
10BASE-FP Total at Retiming	4.0	N/A	N/A
Subtotal (10BASE-FP Retimes)	0.0	0.5	2.0
Transmitter*	2.0	4.0	4.5
Subtotal (at the MDI)	2.0	4.5	6.5
Fiber Optic Medium	0.0	0.0	0.0
10BASE-FP Passive Star	0.0	N/A	N/A
Fiber Optic Medium (10BASE-FP return)	0.0	N/A	N/A
Receiver**	1.0	2.0	8.5
10BASE-FP Total at Retiming	3.0	N/A	N/A
Subtotal (10BASE-FP Retimes)	0.0	6.5	15.0
Unallocated	8.5	10.0	0.0
MAU DI Transmitter (10BASE-FP only)	6.5	N/A	N/A
AUI Cable incl-SNR (DI Pair)	1.5	N/A	1.5
Total	16.5 ns	16.5 ns	16.5 ns
*Includes jitter plus duty cycle distortion.			
** 10BASE-FL figure includes MAU DI Transmitter jitter allocation.			

B.5.2 10BASE-FP fiber optic segment loss budget

The 10BASE-FP MDI optical parameters specified in 15.2.1 and 15.2.2 have been selected to guarantee operation using a properly specified system of up to 500 m radius segment. This annex illustrates how the

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loss budget may be allocated to star, optical fiber, and patch panel connectors, including examples at 100 m and 500 m radius.

The allowed system attenuation values are determined by the average transmit and receive power ranges specified in Table 15–1. The average optical power launched into a 62.5 μm fiber must be greater than –15 dBm and less than –11 dBm. (This includes any launch power variation and source degradation.) Receiver operation is specified for average received power greater than –41 dBm and less than –27 dBm. Thus the maximum attenuation allowed for optical plant, including star, is 26 dB, and the minimum allowed attenuation is 16 dB.

This attenuation can be allocated between the star, fiber optic cable, and patch panel connectors in any manner as long as the maximum and minimum losses are within the limits stated in Table B–3. Note that the 10BASE-FP Star insertion loss includes the loss of one optical connector pair as specified in 16.5.2.1.

Table B–3—10BASE-FP fiber optic segment loss budget

Item	Min (dB)	Max (dB)
Star	16	20
Fiber and Connectors	0	6
Totals	16	26

Example 1: For a 500 m radius segment (1 km MDI to MDI) of 3.75 dB/km (measured at 850 nm) optical fiber and a connector system with a maximum loss of 2 dB, the worst-case optical fiber and connector loss would be 5.75 dB. This would fall within the 6 dB limit, and result in a worst-case margin of 0.25 dB.

Example 2: A horizontal structured building wiring system (e.g., as detailed in ANSI/TIA/EIA-568-A-1995) of 100 m from the wiring closet to the desk top (100 m radius segment, 200 m MDI to MDI) of 3.75 dB/km optical fiber would have a loss of 0.75 dB. With four connector pairs in the path from MDI to MDI (wall plate, patch panel, patch panel, wall plate [see Figure 15–2]) and one connector pair at the 10BASE-FP Star (the other star connector pair is already included in the star loss [see 16.5.2.1)], and using a worst-case loss of 1 dB for each connector pair, the worst-case optical fiber and connector loss would be 5.75 dB. This would fall within the 6 dB limit, and would result in a worst-case margin of 0.25 dB.

In addition to these loss budgets, the overall system return loss must be greater than 27 dB. The return loss is the ratio of the desired signal to all undesired, multiple reflected signals, observed at a 10BASE-FP MAU MDI. Use of connectors with less return loss than specified in 15.3.2.2 as well as use of more than two patch panels on each side of the star is permitted, as long as the overall system return loss requirement is met.

The 8.0 dB differential flux budget (16.3.4.2) can be allocated as shown in Table B–4.

Table B–4—Eight decibel differential flux budget

Contribution	(dB)
Variation at Star Input due to combined effects	4.8
1/2 star connector	0.5
Star including 1/2 connector	2.5
Wavelength in ORD leg	0.2
Total	8.0

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Each of these contributions to the differential budget is a measurable quantity. For example, the variation in the optical power at the star input due to combined effects of launch power, LED lifetime degradation, connectors, distance from 10BASE-FP MAU to Star, and wavelength of transmitter can be measured at the star input port. Also, star differential loss measurement is described in 16.5.2.2.

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Annex C

(informative)

State diagram, MAC sublayer

This annex was deleted by IEEE Std 802.3x-1997 and IEEE Std 802.3y-1997.

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Annex D

(informative)

Application context, selected medium specifications

D.1 Introduction

This annex provides general guidance, to both the design engineer and the eventual user of specific product implementations, on what particular clauses of the ISO/IEC 8802-3 International Standard might be considered useful for different application environments. It is to be emphasized that the material in this annex is very general, as the standard specifications are intended to be relatively application-independent. Nevertheless, certain specifications may apply more to one application environment than another. What follows are brief descriptions of application environments and lists of those generic parameters of the physical layer specifications thought to be useful in relating a general set of user requirements to a specific standard specification and its related medium. *Once a basic relationship is identified, the reader is directed to a specific clause of the standard for detailed design specifications*.

D.2 Type 10BASE5 applications

One of the major arenas for local area networks is the interconnection of work stations throughout a large department or single building. The ability to handle all kinds of message traffic at relatively high data rates among a large set of work stations are typical characteristics of these environments. Usually the basic interconnection trunk cable is installed and left in place permanently or for extended periods while work station placement may shift from time to time. The Type 10BASE5 specification provides the primary baseband backbone for intraplant CSMA/CD interconnections. Clauses 7 and 8 of the standard provide detailed specifications for the physical layers associated with Type 10BASE5 environments. The generic physical layer parameters are as follows:

Maximum unrepeatered cable segment	500 m
Maximum number of MAUs per segment	100
Connector type	Type N or coaxial “tap”
Breakdown voltage, MAU function	250 V ac rms
MTBF	1 million hours
Total Segment Resistance	5 Ω
MAU separation	2.5 m
Connection shunt capacitance	4 pF
AUI functionality	DO, DI, CI, (CO optional)

D.3 Type 10BASE2 applications

Another major arena for local area networks is the interconnection of work stations throughout a small department or work area. The ability to handle all kinds of message traffic at relatively high data rates among a selected set of locally clustered work stations are the typical characteristics of these environments. In addition, the basic interconnection trunk cable is likely to be moved frequently by the local users of the equipment to suit evolving needs. The Type 10BASE2 specification provides an interconnection schema that complements the Type 10BASE5 backbone in a hierarchical manner for intradepartment or work area CSMA/CD interconnections. Clauses 7 and 10 of the standard provide detailed specifications for the physi-

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cal layers associated with Type 10BASE2 environments. The generic physical layer parameters are as follows:

Maximum unrepeatered cable segment	185 m
Maximum number of MAUs per segment	30
Connector type	Type BNC "T"
Breakdown voltage, MAU function	500 V ac rms
MTBF	100 000 hours
Total Segment Resistance	10 Ω
MAU separation	0.5 m
Connection shunt capacitance	8 pF
AUI functionality	DO, DI, CI

D.4 Type FOIRL and 10BASE-F Applications; alternative fiber optic medium applications

D.4.1 Alternative fiber types

Table D–1 provides a listing of other fiber types that may be used in an FOIRL or a 10BASE-F Cable Link Segment. These fiber types have not been studied, and details for their use are not provided for in the main body of the standard. Therefore, using these fiber types may reduce the maximum achievable distance.

Table D–1—Alternative fiber types

Nominal Core diameter (μm) IEC 60793-2: 1992	Nominal cladding diameter (μm) IEC 60793-2: 1992	Nominal Numerical aperture IEC 60793-2: 1992
50	125	0.2
50	125	0.21
50	125	0.22
85	125	0.26
100	140	0.29

D.4.1.1 Theoretical coupling losses

The body of the standard references a single fiber type to facilitate interoperability and conformance testing; however, other fiber types may also be used. The use of an alternate fiber type with a particular implementation may have the following consequences. At the transmit MDI, more or less light may be launched into the fiber, depending on whether the optics are optimized for a core size and a numerical aperture (NA) that are smaller or larger than that of the alternate fiber size. At the receive MDI, the sensitivity may be increased or decreased depending on the optimization of the collecting optics. Table D–2 summarizes the potential effects of the use of alternate fiber sizes and provides the loss budget remaining for cable plant attenuation. All adjustments are relative to an implementation using the minimum diameter and NA 62.5 μm core fiber as specified in IEC 60793-2: 1992, Type A1b, Category ≤ 3.5 dB/km. This cable plant has a loss budget of 9 dB for FOIRL segments and 12.5 dB for 10BASE-FL and 10BASE-FB link segments.

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The worst-case loss budget in Table D–2 is calculated on the assumption that the transmitter and receiver core diameter and NA are 62.5 μm and 0.275, respectively. Launching into a smaller core diameter or NA will incur a loss. Launching into a larger core diameter or NA will not result in a gain.

Similarly, receiving from a larger core diameter or NA incurs a loss, but receiving from smaller core diameter or NA provides no gain.

The values for transmit powers assume a worst-case condition that no additional power is launched into an increased core diameter and NA link fiber when referred to the 62.5 μm core fiber. This assumption is valid for underfilled launch conditions such as may occur from a MAU containing a pigtailed or laser emitter.

Table D–2—Worst-case loss budget

Fiber type	Transmit loss (dB)	Receive loss (dB)	Loss budget remaining (dB)	
			FOIRL	10BASE-FB/L
50 μm/NA=0.20	5.7	0	3.3	6.8
50 μm/NA=0.21	5.2	0	3.8	7.3
50 μm/NA=0.22	4.8	0	4.2	7.7
85 μm/NA=0.26	1.6	2.6	4.8	8.3
100 μm/NA=0.29	0.5	4.5	4.0	7.5

D.4.1.2 Maximum launch power

When large core diameter and NA launch conditions are used in conjunction with a launch fiber of larger core diameter and NA than the 62.5 μm reference, significantly greater launch power can occur. For example, this is typically the case with wide area surface emitter LED devices that are directly aligned with a fiber in a device mount header.

Table D–3 summarizes the maximum launch power into fibers with larger core diameters than 62.5 μm and the corresponding excess power that can result with a receiver utilizing all the optical power from the fiber.

Table D–3—Worst-case launch power

Fiber type	Maximum transmit power (dBm)	Maximum excess power (dBm)
85 μm/NA=0.26	–6.1	2.9
100 μm/NA=0.29	–3.8	5.2

In this case, sufficient attenuation should be installed in the link segment to ensure that for FOIRL segments the peak received optical power does not exceed –9 dBm, and for 10BASE-F segments the average received optical power does not exceed the appropriate optical Receive Average Power (Max) in Table 15–1.

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D.4.2 Type 10BASE-FP applications using 50/125 μm fiber

It is recognized that, in some cases, designers are constrained to use fiber sizes other than 62.5/125 μm in LAN designs. Such LAN designs are beyond the scope of this standard but can operate properly if optical power and loss budgets are adjusted to compensate for the different fiber characteristics. The following guidance is provided for system implementors who are constrained to design LANs with the 50/125 μm fiber described in D.4.1.

WARNING

Interoperability of nonconforming implementations cannot be ensured. It is the responsibility of the designer(s) of nonconforming implementation(s) to assure LAN operation. The following is only advisory information for implementations outside the scope of this standard.

D.4.2.1 Coupled transmit power

As shown in D.4.1, reduction of coupled power introduces the greatest difference between LANs using 62.5/125 μm and those using 50/125 μm fiber. Typically, for an emitter technology that produces a uniform, overfilled launch condition, this difference will be 3.5 dB. Implementors of 50/125 μm systems may choose to deal with this by trying one of the following alternatives:

a) Selecting an emitter technology with coupled power that is less susceptible to variation with fiber size, or
b) Increasing receiver sensitivity and dynamic range, or
c) Reducing the star coupler loss to compensate for the reduction in coupled transmit power. This may be accomplished by reducing the number of ports on the star coupler, or
d) Reducing the connector losses in the system, either by reducing the number of in-line connectors or reducing the loss per connector.

D.4.2.2 Star coupler loss

Also in accordance with D.4.1, the transmission loss of 50/125 μm star couplers may be as much as 1 dB greater than their 62.5/125 μm counterparts. Implementors of 50/125 μm systems may choose to deal with this by trying one of the following alternatives:

a) Procurement—specification of coupler loss characteristics to be the same as those shown for 62.5/125 μm star couplers, per 16.5, or
b) Compensation—all items shown in D.4.2.1 a) to d) may be used to compensate for an increase in coupler loss.

For example, a passive-star coupler (with connectors) with 33 ports typically has the following losses:

Contributor	Loss (dB)
Splitting:	–15
Connector (1):	–1
Excess:	0 to –4
Total:	–16 to –20

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If, in a LAN that used 50/125 μm fiber, the maximum allowable number of ports per passive-star coupler was reduced to 17, the appropriate losses would be as follows:

Contributor	Loss (dB)
Splitting:	–12
Connector (1):	–1
Excess:	0 to –3
Total:	–13 to –16

The 3.5 dB lost to the MDI OTD would then be recovered allowing this "reduced nodes" LAN to still operate at the proposed maximum of 500 m MAU to the star.

It should be noted that the MAU parameters remain unchanged.

D.4.2.3 Collision detection

Reliable collision detection requires that designers of systems using nonconforming fiber optic cable ensure that the optical power levels of all possible colliding signals on the LAN differ at the mixing element (passive-star coupler) by no more than that specified in 16.3.4.2. This requires that
$10 * \text{abs}\,(\log((P_{Ti} - L_{Ti} - U_{Ti})/(P_{Tj} - L_{Tj} - U_{Tj}))) \leq$ that specified in 16.3.4.2.

for all *i* not equal *j*, and

where

P_{Tn} is coupled optical transmit power, MAU *n*
L_{Tn} is optical cable and connector and transmit fiber loss, from MAU n to star input port *m*
U_{Tm} is input port uniformity, port *m*

D.5 10BASE-T use of cabling systems with a nominal differential characteristic impedance of 120 Ω

Clause 14 specifies the use of 100 Ω link segments. This subclause specifies the conditions for the use of cabling with a nominal characteristic impedance of 120 Ω by 10BASE-T conformant stations.

The use of cables with a characteristic impedance outside the range specified in 14.4.2.2 will generally increase the mismatching effects in the link components, inducing additional jitter in the received signal.

In particular, the use of a homogeneous link segment having a characteristic impedance of 120 Ω ± 15 Ω over the frequency band 1 to 16 MHz may add from 0.15 ns (maximum-length segment) up to 0.63 ns (short-length segment) of additional jitter to the signal at the input of the receiver.

Consequently, in order to keep the overall jitter budget at the same value as for a 100 Ω link segment when using a 120 Ω link segment, the following modifications to the specifications of 14.4 apply:

a) The maximum medium timing jitter specified in 14.4.2.3 for a simplex link segment is increased from 5 ns to 5.5 ns.

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b) The NEXT loss values specified in 14.4.3 are increased by 3 dB, i.e., the applicable formulas are replaced by the following:

1) in 14.4.3.1.1 for 25-pair cables/binder groups: $33–15 \log_{10}(f/10)$ dB.
2) in 14.4.3.1.2 for 4-pair cables: $29–15 \log_{10}(f/10)$ dB.
3) in 14.4.3.2 for MDNEXT: $26–15 \log_{10}(f/10)$ dB.

NOTE—In addition to the case of 120 Ω homogeneous link segments, the above figures encompass the case where 100 Ω terminal cords are used in conjunction with 120 Ω premises cabling. This configuration results in adding up to 0.5 ns of jitter for a maximum-length segment (instead of 0.15 ns) and up to 1.3 ns for a short-length segment (instead of 0.63 ns).

The use of 100 Ω cords at any intermediate cross-connects on 120 Ω links as well as the use of cords with a characteristic impedance of 120 Ω ± 15 Ω in conjunction with 100 Ω ±15 Ω premises cabling is not allowed since it would result in worst-case jitter greater than that allowed in the standard.

D.6 10BASE-T use of cabling systems with a nominal differential characteristic impedance of 150 Ω

This subclause outlines the philosophy and methodology for allowing 10BASE-T stations to support transmission on 150 Ω balanced STP cabling, installed in accordance with ANSI/TIA/EIA-568-A-1995 [B16], Clause 4, and ISO/IEC 11801: 1995, Clause 8, with the use of impedance matching transformers.

The 10BASE-T specification was designed to support Manchester signaling over a link segment consisting of 100 Ω cabling system. The MAU link interface specifications were designed to ensure that jitter due to impedance discontinuities were minimized as specified in 14.4.2.3. In theory and in practice, a 150 Ω cabling system may be used to provide the link segment function provided the proper impedance match (100 Ω) with the MAU over the frequency range of interest as specified in 14.4, and the resultant transmission characteristics of the cabling system used to provide the link segment function meet or exceed those specified in 14.4. Therefore, to ensure the jitter specification of 14.4.2.3 and the jitter budget of B.4.1 are met, the following approach is recommended when using 150 Ω balanced STP cabling (as specified in ISO/IEC 11801: 1995):

a) The 150 Ω section included in the link segment shown in Figure D–1 meets the specifications of ISO/IEC 11801: 1995, 7.2, and ANSI/TIA/EIA-568-A-1995 [B16].

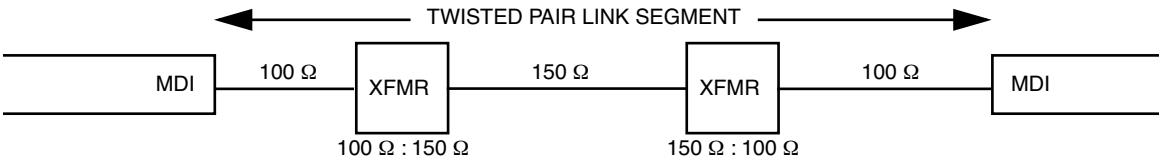


Figure D–1—Link segment incorporating 150 Ω cable section

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b) The link segment, including impedance matching transformers as shown in Figure D–2, meets all applicable specifications of 14.4.

c) A link test point is shown in Figure D–2. The transformers shown are the same as the ones shown in Figure D–1. The attaching cables between the MAU and the link test point should be the minimum required to attach the components. As tested in this configuration, the MAU transmitter requirements meet all applicable requirements for the MAU as specified in Clause 14, except for signal levels which may be up to 1.0 dB lower than that specified there.

NOTE—This 1.0 dB (0.5 dB per transformer) effectively requires the attenuation of the 150 Ω cable section of the twisted-pair link segment (see Figure D–1) to be less than or equal to 10.5 dB in order to meet the requirements of 14.4.2.

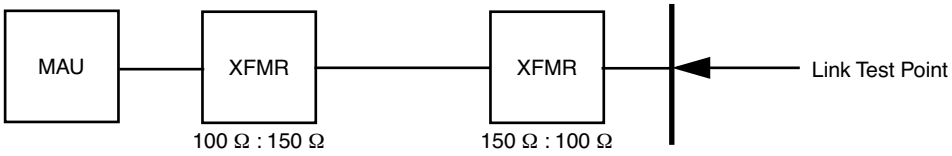


Figure D–2—Link test point for 150 Ω cabling

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Annex E

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Receiver wavelength design considerations (FOIRL)

The center wavelength of the optical source emission is specified in 9.9.4.1.1 to be between 790 nm and 860 nm. Although these limits are acceptable, it is currently recognized, through the examination of manufacturers' current data, that greater choices of emitters can be obtained by extending the allowable wavelength to 910 nm.

An upper limit of 910 nm allows the selection of devices nominally centered at a lower wavelength, for example, 880 nm. This allows a tolerance for manufacturing variations, for example, ±20 nm, and a tolerance for an operating temperature range (typically, 0.3 nm/°C).

It is anticipated that future fiber optic applications including Local Area Networks will use the 910 nm upper limit for first window systems. It is therefore recommended that implementors specify receiver sensitivity over a center wavelength range from 790 nm to 910 nm.

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Annex F

(normative)

Additional attributes required for systems

F.1 Introduction

During the development of Repeater Management, some attributes and operations were identified as items that were necessary to fill out the management of a complete intermediate system such as a repeater. These items are generic in the sense that they are required for managed systems in general. They are not normally specified as attributes of the lower layers. In repeater management, the entire system is at the lowest layers so there is no other group to turn to for systems management. The following items are defined to aid in the completeness of this standard, although it is recognized that they are outside the bounds of the definition area for a layer1/2 device.

F.1.1 Scope

This annex defines additional managed objects and attributes that have been identified by the IEEE 802.3 Repeater Management Task Force as being necessary to the management of an IEEE 802.3 repeater. These objects and attributes, while necessary to the management of an IEEE 802.3 repeater, are not specifically related to the CSMA/CD access method or to Clause 9 repeaters; rather, they are objects and attributes that are appropriate for any managed system.

This annex does not necessarily define the complete set of generic objects and attributes required to support a managed system. It contains only those objects and attributes that were identified in the process of developing the repeater management standard and were identified as not being uniquely appropriate to a CSMA/CD layer management standard.

When a generic systems management standard is available that is appropriate for managed systems of the complexity of a repeater, it is expected that this portion of the standard will no longer be appropriate and will be deprecated.

F.2 Objects/Attributes/Actions/Notifications

F.2.1 TimeSinceSystemReset attribute

aTimeSinceSystemReset **ATTRIBUTE**
DERIVED FROM AttributeModule.ResettableCounter32;
BEHAVIOUR bTimeSinceSystemReset;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) sysResetTime(47)};

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bTimeSinceSystemReset **BEHAVIOUR**
DEFINED AS The time in tens of milliseconds since the last time that the system including network management was reset. This may have been caused by ResetSystemAction or other means. This counter has a value of 0 when initialized.

Though the count is reported in tens of milliseconds, the required resolution is to the nearest 100 ms. The clocking source for the counter shall be accurate to within 1% throughout the full counting range.;

NOTE—The approximate minimum time for counter rollover is 497 days.

F.2.2 RepeaterResetTimeStamp attribute

aRepeaterResetTimeStamp **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX AttributeModule.Integer32;
BEHAVIOUR bRepeaterResetTimeStamp;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) repeaterResetTimeStamp(48)};

bRepeaterResetTimeStamp **BEHAVIOUR**
DEFINED AS Not a counter, this attribute provides the value of aTimeSinceSystemReset when the repeater was last reset. This value is recorded whenever the repeater enters the START state of Figure 9–2 in the 802.3 repeater standard. This value may never be greater than aTimeSinceSystemReset.;

F.2.3 ResetSystemAction action

acResetSystemAction **ACTION**
BEHAVIOUR acResetSystem;
MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) action(9) resetSystem(49)};

acResetSystem **BEHAVIOUR**
DEFINED AS This action initializes the resettable management counters of the system and also of all contained objects. The value of non-resettable counters may change as a result of this action.;

NOTE—This action may result in the loss of packets.

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Annex G

(normative)

Additional material required for conformance testing

G.1 Introduction

This material was generated during the development of Clause 19. It was felt that it was required to support the development of conformance test material that was not included in the charter of the development of the original repeater management standard.

G.1.1 Material in support of the aDataRateMismatches attribute

A vendor submitting equipment for conformance testing under Clause 19 shall provide minimum frequency difference data (two values) such that a test can be done for exertion and another test can be done for non-exertion of the aDataRateMismatch attribute (see 19.2.6.2).

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Annex H

(normative)

GDMO specifications for CSMA/CD managed objects

H.1 Use of MAC and PLS Sublayer Management Definitions with CMIS/CMIP and ISO/IEC 15802-2: 1995 Management Protocols

NOTE—The arcs (that is, object identifier values) defined in Annex 30A deprecate the arcs previously defined in H.1 (Layer Management), H.2 (Repeater Management), and H.3 (MAU Management). See IEEE Std 802.1F-1993, Annex C4.

This annex clause formally defines the protocol encodings for CMIP and ISO/IEC 15802-2: 1995 for the DTE Management objects using the templates specified in ISO/IEC 10165-4: 1992.

Each attribute definition in this clause references directly by means of the WITH ATTRIBUTE SYNTAX construct or indirectly by means of the DERIVED FROM construct an ASN.1 type or subtype that defines the attribute's type and range. Those ASN.1 types and subtypes defined exclusively for CSMA/CD Management are included in H.4.

H.1.1 DTE MAC sublayer managed object class

H.1.1.1 DTE MAC sublayer formal definition

```
oMAC-entity                          MANAGED OBJECT CLASS
    DERIVED FROM                     "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 :
                                     1992":top;

    CHARACTERIZED BY
        pBasic                       PACKAGE
            ATTRIBUTES               aMACID                                  GET;
            ACTIONS                  acInitializeMAC;
        ;
    ;
    CONDITIONAL PACKAGES
        pMandatory                   PACKAGE
            ATTRIBUTES               aFramesTransmittedOK                    GET,
                                     aSingleCollisionFrames                  GET,
                                     aMultipleCollisionFrames                GET,
                                     aFramesReceivedOK                       GET,
                                     aFrameCheckSequenceErrors               GET,
                                     aAlignmentErrors                        GET;
            REGISTERED AS            {iso(1) member-body(2) us(840) 802dot3(10006)
                                     csmadtemgt(5) package(4) macMandatoryPkg(103)};
            PRESENT IF               Conformance to DTE Management is desired.;
        pRecommended                 PACKAGE
            ATTRIBUTES               aOctetsTransmittedOK                    GET,
                                     aFramesWithDeferredXmissions            GET,
                                     aLateCollisions                         GET,
                                     aFramesAbortedDueToXSColls              GET,
                                     aFramesLostDueToIntMACXmitError         GET,
```


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aCarrierSenseErrors GET,
aOctetsReceivedOK GET,
aFramesLostDueToIntMACRcvError GET,
aPromiscuousStatus GET-SET,
aReadMulticastAddressList GET;

ACTIONS acAddGroupAddress,
acDeleteGroupAddress;

REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) package(4) macRecommendedPkg(104)};

PRESENT IF The Recommended Package is implemented.;

pOptional **PACKAGE**

ATTRIBUTES aMulticastFramesXmittedOK GET,
aBroadcastFramesXmittedOK GET,
aMulticastFramesReceivedOK GET,
aBroadcastFramesReceivedOK GET,
aInRangeLengthErrors GET,
aOutOfRangeLengthField GET,
aFrameTooLongErrors GET,
aMACEnableStatus GET-SET,
aTransmitEnableStatus GET-SET,
aMulticastReceiveStatus GET-SET,
aReadWriteMACAddress GET-SET;

ACTIONS acExecuteSelfTest;

REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) package(4) optionalPkg(105)};

PRESENT IF The Optional Package and the Recommended Package is implemented.;

pArray **PACKAGE**

ATTRIBUTES aCollisionFrames GET;

REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) package(4) arrayPkg(106};

PRESENT IF The Array Package and the Recommended Package are implemented.;

pExcessiveDeferral **PACKAGE**

ATTRIBUTES aFramesWithExcessiveDeferral GET;

REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) package(4) excessiveDeferralPkg(107)};

PRESENT IF The ExcessiveDeferral Package and the Recommended Package are implemented.;

REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) managedObjectClass(3) macObjectClass(101)};

nbMACName **NAME BINDING**

SUBORDINATE OBJECT CLASS oMAC-entity;

NAMED BY SUPERIOR OBJECT CLASS "ISO/IEC 10165-2":system;

WITH ATTRIBUTE aMACID;

REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) nameBinding(6) macName(109)};

nbMACMonitor **NAME BINDING**

SUBORDINATE OBJECT CLASS "IEEE802.1F":ewmaMetricMonitor;

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NAMED BY SUPERIOR OBJECT CLASS
"ISO/IEC 10165-2":system;
WITH ATTRIBUTE aScannerId;
CREATE WITH-AUTOMATIC-INSTANCE-NAMING;
DELETE ONLY-IF-NO-CONTAINED-OBJECTS;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) nameBinding(6) macMonitor(110)};

H.1.1.2 DTE MAC sublayer attributes

aMACID **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY;
BEHAVIOUR bMACID;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) macID(114)};

bMACID **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.1.;

aFramesTransmittedOK **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bFramesTransmittedOK;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) framesTransmittedOK(115)};

bFramesTransmittedOK **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.2.;

NOTES
1—The approximate minimum time between counter rollovers is 80 h.;
2—This maps to framesSent (of the mandatory macPackage) in ISO/IEC 10742: 1994.;

aSingleCollisionFrames **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bSingleCollisionFrames;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) singleCollisionFrames(116)};

bSingleCollisionFrames **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.3.;

NOTE—The approximate minimum time between counter rollovers is 103 h.;

aMultipleCollisionFrames **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bMultipleCollisionFrames;

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REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) multipleCollisionFrames(117)};

bMultipleCollisionFrames **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.4.;

NOTE—The approximate minimum time between counter rollovers is 125 h.;

aFramesReceivedOK **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bFramesReceivedOK;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) framesReceivedOK(118)};

bFramesReceivedOK **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.5.;

NOTES
1—The approximate minimum time between counter rollovers is 80 h.;
2—This maps to framesReceived (of the mandatory macPackage) in ISO/IEC 10742: 1994.;

aFrameCheckSequenceErrors **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bFrameCheckSequenceErrors;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) frameCheckSequenceErrors(119)};

bFrameCheckSequenceErrors **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.6.;

NOTE—The approximate minimum time between counter rollovers is 80 h.;

aAlignmentErrors **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bAlignmentErrors;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) alignmentErrors(120)};

bAlignmentErrors **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.7.;

NOTE—The approximate minimum time between counter rollovers is 80 h.;

aOctetsTransmittedOK **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bOctetsTransmittedOK;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) octetsTransmittedOK(121)};

bOctetsTransmittedOK **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.8.;

NOTES
1—The approximate minimum time between counter rollovers is 58 min.
2—This maps to octetsSent (of the mandatory macPackage) in ISO/IEC 10742: 1994.;

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aFramesWithDeferredXmissions **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bFramesWithDeferredXmissions;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) framesWithDeferredXmissions(122)};

bFramesWithDeferredXmissions **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.9.;

NOTE—The approximate minimum time between counter rollovers is 103 h.;

aLateCollisions **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bLateCollisions;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) lateCollisions(123)};

bLateCollisions **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.10.;

NOTE—The approximate minimum time between counter rollovers is 80 h.;

aFramesAbortedDueToXSColls **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bFramesAbortedDueToXSColls;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) framesAbortedDueToXSColls(124)};

bFramesAbortedDueToXSColls **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.11.;

NOTE—The approximate minimum time between counter rollovers is 53 days.;

aFramesLostDueToIntMACXmitError **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bFramesLostDueToIntMACXmitError;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) framesLostDueToIntMACXmitError(125)};

bFramesLostDueToIntMACXmitError **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.12.;

NOTE—The approximate minimum time between counter rollovers is 16 h.;

aCarrierSenseErrors **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bCarrierSenseErrors;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) carrierSenseErrors(126)};

bCarrierSenseErrors **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.13.;

NOTE—The approximate minimum time between counter rollovers is 80 h.;

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aOctetsReceivedOK **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bOctetsReceivedOK;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) octetsReceivedOK(127)};

bOctetsReceivedOK **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 5.2.2.1.14.;

NOTES
1—The approximate minimum time between counter rollovers is 58 min.
2—This maps to octetsReceived (of the mandatory macPackage) in ISO/IEC 10742: 1994.;

aFramesLostDueToIntMACRcvError **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bFramesLostDueToIntMACRcvError;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) framesLostDueToIntMACRcvError(128)};

bFramesLostDueToIntMACRcvError **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 5.2.2.1.15.;

NOTE—The approximate minimum time between counter rollovers is 80 h.;

aPromiscuousStatus **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.TrueFalse;
BEHAVIOUR bPromiscuousStatus;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) promiscuousStatus(129)};

bPromiscuousStatus **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in5.2.2.1.16.;

aReadMulticastAddressList **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MulticastAddressList
BEHAVIOUR bReadMulticastAddressList;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) readMulticastAddressList(130)};

bReadMulticastAddressList **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 5.2.2.1.17.;

aMulticastFramesXmittedOK **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bMulticastFramesXmittedOK;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) multicastFramesXmittedOK(131)};

bMulticastFramesXmittedOK **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 5.2.2.1.18.;

NOTE—The approximate minimum time between counter rollovers is 80 h.;

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aBroadcastFramesXmittedOK **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bBroadcastFramesXmittedOK;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) broadcastFramesXmittedOK(132)};

bBroadcastFramesXmittedOK **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 5.2.2.1.19.;

NOTE—The approximate minimum time between counter rollovers is 80 h.;

aFramesWithExcessiveDeferral **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bFramesWithExcessiveDeferral;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) framesWithExcessiveDeferral(133)};

bFramesWithExcessiveDeferral **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 5.2.2.1.20.;

NOTE—The approximate minimum time between counter rollovers is 58 days.;

aMulticastFramesReceivedOK **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bMulticastFramesReceivedOK;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) multicastFramesReceivedOK(134)};

bMulticastFramesReceivedOK **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 5.2.2.1.21.;

NOTE—The approximate minimum time between counter rollovers is 80 h.;

aBroadcastFramesReceivedOK **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bBroadcastFramesReceivedOK;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) broadcastFramesReceivedOK(135)};

bBroadcastFramesReceivedOK **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 5.2.2.1.22.;

NOTE—The approximate minimum time between counter rollovers is 80 h.;

aInRangeLengthErrors **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bInRangeLengthErrors;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) inRangeLengthErrors(136)};

bInRangeLengthErrors **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 5.2.2.1.23.;

NOTE—The approximate minimum time between counter rollovers is 80 h.;

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aOutOfRangeLengthField **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bOutOfRangeLengthField;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) outOfRangeLengthField(137)};

bOutOfRangeLengthField **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.24.;

NOTE—The approximate minimum time between counter rollovers is 80 h.;

aFrameTooLongErrors **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bFrameTooLongErrors;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) frameTooLongErrors(138)};

bFrameTooLongErrors **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.25.;

NOTE—The approximate minimum time between counter rollovers is 61 days.;

aMACEnableStatus **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.TrueFalse;
BEHAVIOUR bMACEnableStatus;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) mACEnableStatus(139)};

bMACEnableStatus **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.26.;

aTransmitEnableStatus **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.TrueFalse;
BEHAVIOUR bTransmitEnableStatus;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) transmitEnableStatus(140)};

bTransmitEnableStatus **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.27.;

aMulticastReceiveStatus **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.TrueFalse;
BEHAVIOUR bMulticastReceiveStatus;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) multicastReceiveStatus(141)};

bMulticastReceiveStatus **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.28.;

aReadWriteMACAddress **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802CommonDefinitions.MACAddress;
BEHAVIOUR bReadWriteMACAddress;

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REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) modifyMACAddress(142)};

bReadWriteMACAddress **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.29.;

NOTE—This maps to localMACAddress (of the mandatory macPackage) in ISO/IEC 10742: 1994.;

aCollisionFrames **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AttemptArray;
BEHAVIOUR bCollisionFrames;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) collisionFrames(143)};

bCollisionFrames **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.1.30.;

NOTE—The approximate minimum time for any single counter rollover is 103 h.;

H.1.1.3 DTE MAC sublayer actions

acInitializeMAC **ACTION**
BEHAVIOUR bInitializeMAC;
MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) action(9) initializeMAC(146)};

bInitializeMAC **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.2.1.;

acAddGroupAddress **ACTION**
BEHAVIOUR bAddGroupAddress;
MODE CONFIRMED;
WITH INFORMATION SYNTAX IEEE802CommonDefinitions.MACAddress;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) action(9) addGroupAddress(147)};

bAddGroupAddress **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.2.2.;

acDeleteGroupAddress **ACTION**
BEHAVIOUR bDeleteGroupAddress;
MODE CONFIRMED;
WITH INFORMATION SYNTAX IEEE802CommonDefinitions.MACAddress;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) action(9) deleteGroupAddress(148)};

bDeleteGroupAddress **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.2.3.;

acExecuteSelfTest **ACTION**
BEHAVIOUR bExecuteSelfTestMAC;

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MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) action(9) executeSelfTestMAC(149)};

bExecuteSelfTest **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.2.2.4.;

H.1.2 ResourceTypeID managed object class

H.1.2.1 ResourceTypeID, formal definition

-- Implementation of this managed object in accordance with the definition contained in
-- IEEE Std 802.1F-1993 is a conformance requirement of this standard.
-- NOTE—A single instance of the Resource Type ID managed object exists within the
-- DTE–MAC managed object class. The managed object itself is contained in IEEE Std 802.1F-1993;
-- therefore, only the name binding appears in this standard;

nbResourceTypeID **NAME BINDING**
SUBORDINATE OBJECT CLASS "IEEE802.1F":oResourceTypeID;
NAMED BY SUPERIOR OBJECT CLASS
oMAC-Entity;
WITH ATTRIBUTE "IEEE802.1F":aResourceTypeIDName;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) nameBinding(6) resourceTypeID(111)};

H.1.3 DTE physical layer managed object class

H.1.3.1 DTE physical layer formal definition

oPHY-entity **MANAGED OBJECT CLASS**
DERIVED FROM "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992":top;
CHARACTERIZED BY
pMandatory **PACKAGE**
--There are no mandatory Attributes, Actions, or Notifications;
--therefore, management of this object is not required if only
--the mandatory package is implemented.
;
;
CONDITIONAL PACKAGES
pRecommended **PACKAGE**
ATTRIBUTES aPHYID GET,
aSQETestErrors GET;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) package(4) phyRecommendedPkg(108)};
PRESENT IF The Recommended Package is implemented.;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) managedObjectClass(3) phyObjectClass(102)};

nbPHYName **NAME BINDING**
SUBORDINATE OBJECT CLASS oPHY-entity;
NAMED BY SUPERIOR OBJECT CLASS

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oMAC-entity;;
WITH ATTRIBUTE aPHYID;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) nameBinding(6) phyName(112)};

nbPHYMonitor **NAME BINDING**
SUBORDINATE OBJECT CLASS "IEEE802.1F":ewmaMetricMonitor;
NAMED BY SUPERIOR OBJECT CLASS
"ISO/IEC 10165-2":system;
WITH ATTRIBUTE aScannerId;
CREATE **WITH-AUTOMATIC-INSTANCE-NAMING;**
DELETE **ONLY-IF-NO-CONTAINED-OBJECTS;**
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) nameBinding(6) phyMonitor(113)};

H.1.3.2 DTE physical sublayer attributes

aPHYID **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY;
BEHAVIOUR bPHYID;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) phyID(144)};

bPHYID **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.3.1.1;

aSQETestErrors **ATTRIBUTE**
DERIVED FROM aLMCounter;
BEHAVIOUR bSQETestErrors;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmadtemgt(5) attribute(7) sqeTestErrors(145)};

bSQETestErrors **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 5.2.3.1.2.;

NOTE—The approximate minimum time between counter rollovers is 80 h.;

H.2 GDMO specification for Repeater Management Object Class

NOTE—The arcs (that is, object identifier values) defined in Annex 30A deprecate the arcs previously defined in H.1 (Layer Management), H.2 (Repeater Management), and H.3 (MAU Management). See IEEE Std 802.1F-1993, Annex C4.

This subclause formally defines the Repeater Management Objects using the templates specified in ISO/IEC 10165-4: 1992.

The protocol encodings for CMIP, and therefore ISO/IEC 15802-2: 1995 can be derived from H.2.1 to H.2.5 directly. The template defined in ISO/IEC 10165-4 specifies precisely the syntax used in this document to define the operation, objects and attributes. The application of a GDMO template compiler against H.2.1 to H.2.5 will produce the proper protocol encodings.

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Each attribute definition in this clause references directly by means of the WITH ATTRIBUTE SYNTAX construct or indirectly by means of the DERIVED FROM construct an ASN.1 type or subtype that defines the attribute's type and range. Those ASN.1 types and subtypes defined exclusively for CSMA/CD Management are appear in a single ASN.1 module in Annex H.

H.2.1 Repeater managed object class

H.2.1.1 Repeater, formal definition

```
oRepeater                                   MANAGED OBJECT CLASS
        DERIVED FROM                        "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2
                                            1992":top;
        CHARACTERIZED BY
                pRepeaterBasicControl       PACKAGE
                        ATTRIBUTES          aRepeaterID                     GET,
                                            aRepeaterGroupCapacity          GET,
                                            aGroupMap                       GET,
                                            aRepeaterHealthState            GET,
                                            aRepeaterHealthText             GET,
                                            aRepeaterHealthData             GET;
                        ACTIONS             acResetRepeater,
                                            acExecuteNonDisruptiveSelfTest;
                        NOTIFICATIONS       nRepeaterHealth,
                                            nRepeaterReset,
                                            nGroupMapChange;
                ;
        ;
        CONDITIONAL PACKAGES
                pRepeaterPerfMonitor        PACKAGE
                        ATTRIBUTES          aTransmitCollisions             GET;
                        REGISTERED AS       {iso(1) member-body(2) us(840) 802dot3(10006)
                                            repeaterMgt(19) package(4)
                                            repeaterPerfMonitorPkg(4)};
                        PRESENT IF          The Performance Monitor Capability is implemented.;
        REGISTERED AS       {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19)
                            managedObjectClass(3) repeaterObjectClass(1)};

nbRepeaterName                              NAME BINDING
        SUBORDINATE OBJECT CLASS            repeater;
        NAMED BY SUPERIOR OBJECT CLASS
                                            "ISO/IEC 10165-2":system AND SUBCLASSES;
        WITH ATTRIBUTE                      aRepeaterID;
        REGISTERED AS       {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19)
                            nameBinding(6) repeaterName(7)};

nbRepeaterMonitor                           NAME BINDING
        SUBORDINATE OBJECT CLASS            "IEEE802.1F":oEWMAMetricMonitor;
        NAMED BY SUPERIOR OBJECT CLASS
                                            "ISO/IEC 10165-2":system AND SUBCLASSES;
        WITH ATTRIBUTE                      aScannerId;
        CREATE                              WITH-AUTOMATIC-INSTANCE-NAMING;
        DELETE                              ONLY-IF-NO-CONTAINED-OBJECTS;
        REGISTERED AS       {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19)
```

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nameBinding(6) repeaterMonitor(8)};

H.2.1.2 Repeater attributes

aRepeaterID **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY;
BEHAVIOUR bRepeaterID;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) repeaterID(13)};

bRepeaterID **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.3.1.1.;

aRepeaterGroupCapacity **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bRepeaterGroupCapacity;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) repeaterGroupCapacity(14)};

bRepeaterGroupCapacity **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.3.1.2;

aGroupMap **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.BitString;
MATCHES FOR EQUALITY;
BEHAVIOUR bGroupMap;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) groupMap(15)};

bGroupMap **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.3.1.3.;

aRepeaterHealthState **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.RepeaterHealthState;
MATCHES FOR EQUALITY;
BEHAVIOUR bRepeaterHealthState;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) repeaterHealthState(16)};

bRepeaterHealthState **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.3.1.4.;

aRepeaterHealthText **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.RepeaterHealthText;
MATCHES FOR EQUALITY;
BEHAVIOUR bRepeaterHealthText;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) repeaterHealthText(17)};

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bRepeaterHealthText **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.3.1.5.;

aRepeaterHealthData **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.
RepeaterHealthData;
MATCHES FOR EQUALITY;
BEHAVIOUR bRepeaterHealthData;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) repeaterHealthData(18)};

bRepeaterHealthData **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.3.1.6.;

aTransmitCollisions **ATTRIBUTE**
DERIVED FROM aRMCounter;
BEHAVIOUR bTransmitCollisions;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) transmitCollisions (19)};

bTransmitCollisions **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.3.1.7.;

NOTE—The approximate minimum time for counter rollover is 16 h.;

H.2.1.3 Repeater actions

acResetRepeater **ACTION**
BEHAVIOUR bResetRepeater;
MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) action(9) resetRepeater(40)};

bResetRepeater **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.3.2.1.;

acExecuteNonDisruptiveSelfTest **ACTION**
BEHAVIOUR bExecuteNonDisruptiveSelfTest;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) action(9) executeNonDisruptiveSelfTestAction(41)};

bExecuteNonDisruptiveSelfTest **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.3.2.2.;

H.2.1.4 Repeater notifications

nRepeaterHealth **NOTIFICATION**
BEHAVIOUR bRepeaterHealth;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.
RepeaterHealthInfo
AND ATTRIBUTE IDS fnRepeaterHealthState aRepeaterHealthState,
fnRepeaterHealthText aRepeaterHealthText,
fnRepeaterHealthData aRepeaterHealthData
;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19)

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notification(10) repeaterHealth(43)};

bRepeaterHealth **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 19.2.3.3.1.;

nRepeaterReset **NOTIFICATION**
BEHAVIOUR bRepeaterReset;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.RepeaterHealthInfo
AND ATTRIBUTE IDS fnRepeaterHealthState aRepeaterHealthState, fnRepeaterHealthText aRepeaterHealthText, fnRepeaterHealthData aRepeaterHealthData
;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) notification(10) repeaterReset(44)};

bRepeaterReset **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 19.2.3.3.2.;

nGroupMapChange **NOTIFICATION**
BEHAVIOUR bGroupMapChange;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.BitString;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) notification(10) groupMapChange(45)};

bGroupMapChange **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 19.2.3.3.3.;

H.2.2 ResourceTypeID managed object class

H.2.2.1 ResourceTypeID formal definition

-- Implementation of this managed object in accordance with the definition contained in
-- IEEE Std 802.1F-1993 is a conformance requirement of this standard.
-- NOTE—A single instance of the Resource Type ID managed object exists within the
-- Repeater managed object class. The managed object itself is contained in
-- IEEE Std. 802.1F-1993; therefore, only the name binding appears in this standard.

nbResourceTypeId **NAME BINDING**
SUBORDINATE OBJECT CLASS "IEEE802.1F":oResourceTypeID;
NAMED BY SUPERIOR OBJECT CLASS oRepeater AND SUBCLASSES;
WITH ATTRIBUTE "IEEE802.1F":aResourceTypeIDName;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) nameBinding(6) resourceTypeID(9)};

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H.2.3 Group managed object class

H.2.3.1 Group formal definition

```
oGroup                                  MANAGED OBJECT CLASS
    DERIVED FROM                        "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2
                                        1992":top;
    CHARACTERIZED BY
        pGroupBasicControl              PACKAGE
            ATTRIBUTES                  aGroupID                    GET,
                                        aGroupPortCapacity          GET,
                                        aPortMap                    GET;
            NOTIFICATIONS               nPortMapChange;
        ;
    ;
    REGISTERED AS       {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19)
                        managedObjectClass(3) groupObjectClass(2)};

nbGroupName                             NAME BINDING
    SUBORDINATE OBJECT CLASS            oGroup;
    NAMED BY SUPERIOR OBJECT CLASS
                                        oRepeater AND SUBCLASSES;
    WITH ATTRIBUTE                      aGroupID;
    REGISTERED AS       {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19)
                        nameBinding(6) groupName(10)};
```

H.2.3.2 Group attributes

```
aGroupID                                ATTRIBUTE
    WITH ATTRIBUTE SYNTAX               IEEE802Dot3-MgmtAttributeModule.
                                        OneOfName;
    MATCHES FOR                         EQUALITY;
    BEHAVIOUR                           bGroupID;
    REGISTERED AS       {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19)
                        attribute(7) groupID(20)};

bGroupID                                BEHAVIOUR
    DEFINED AS                          See "BEHAVIOUR DEFINED AS" in 19.2.5.1.1.;

aGroupPortCapacity                      ATTRIBUTE
    WITH ATTRIBUTE SYNTAX               IEEE802Dot3-MgmtAttributeModule.
                                        OneOfName;
    MATCHES FOR                         EQUALITY, ORDERING;
    BEHAVIOUR                           bGroupPortCapacity;
    REGISTERED AS       {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19)
                        attribute(7) groupPortCapacity(21)};

bGroupPortCapacity                      BEHAVIOUR
    DEFINED AS                          See "BEHAVIOUR DEFINED AS" in 19.2.5.1.2.;

aPortMap                                ATTRIBUTE
    WITH ATTRIBUTE SYNTAX               IEEE802Dot3-MgmtAttributeModule.
                                        BitString;
    MATCHES FOR                         EQUALITY;
    BEHAVIOUR                           bPortMap;
```

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REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) portMap(22)};

bPortMap **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.5.1.3.;

H.2.3.3 Group notifications

nPortMapChange **NOTIFICATION**
BEHAVIOUR bPortMapChange;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.BitString;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) notification(10) portMapChange(46)};

bPortMapChange **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.5.2.1.;

H.2.4 Port managed object class

H.2.4.1 Port formal definition

oPort **MANAGED OBJECT CLASS**
DERIVED FROM "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 1992":top;

CHARACTERIZED BY
pPortBasicControl **PACKAGE**
ATTRIBUTES aPortID GET,
aPortAdminState GET,
aAutoPartitionState GET;
ACTIONS acPortAdminControl;
;
;
CONDITIONAL PACKAGES
pPortPerfMonitor **PACKAGE**
ATTRIBUTES aReadableFrames GET,
aReadableOctets GET,
aFrameCheckSequenceErrors GET,
aAlignmentErrors GET,
aFramesTooLong GET,
aShortEvents GET,
aRunts GET,
aCollisions GET,
aLateEvents GET,
aVeryLongEvents GET,
aDataRateMismatches GET,
aAutoPartitions GET;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) package(4) portPerfMonitorPkg(5)};
PRESENT IF The Performance Monitor Capability is implemented.;

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pPortAddrTracking **PACKAGE**
ATTRIBUTES aLastSourceAddress GET,
aSourceAddressChanges GET;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) package(4) portAddrTrackPkg(6)};
PRESENT IF The Address Tracking and Performance Monitor capabilities are implemented.;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) managedObjectClass(3) portObjectClass(3)};

nbPortName **NAME BINDING**
SUBORDINATE OBJECT CLASS oPort;
NAMED BY SUPERIOR OBJECT CLASS
oGroup AND SUBCLASSES;
WITH ATTRIBUTE aPortID;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) nameBinding(6) portName(11)};

H.2.4.2 Port attributes

aPortID **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
BEHAVIOUR bPortID;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) portID(23)};

bPortID **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.6.1.1.;

aPortAdminState **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PortAdminState;
MATCHES FOR EQUALITY;
BEHAVIOUR bPortAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) portAdminState(24)};

bPortAdminState **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.6.1.2.;

aAutoPartitionState **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AutoPartitionState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAutoPartition;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) autoPartitionState(25)};

bAutoPartition **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.6.1.3.;

aReadableFrames **ATTRIBUTE**
DERIVED FROM aRMCounter;
BEHAVIOUR bReadableFrames;

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REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) readableFrames(26)};

bReadableFrames **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 19.2.6.1.4.

NOTE—The approximate minimum time between counter rollovers is 80 h.;

aReadableOctets **ATTRIBUTE**
DERIVED FROM aRMCounter;
BEHAVIOUR bReadableOctets;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) readableOctets(27)};

bReadableOctets **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 19.2.6.1.5.

NOTE—The approximate minimum time between counter rollovers is 58 min.;

aFrameCheckSequenceErrors **ATTRIBUTE**
DERIVED FROM aRMCounter;
BEHAVIOUR bFCSErrors;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) frameCheckSequenceErrors(28)};

bFCSErrors **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 19.2.6.1.6.

NOTE—The approximate minimum time between counter rollovers is 80 h.;

aAlignmentErrors **ATTRIBUTE**
DERIVED FROM aRMCounter;
BEHAVIOUR bAlignmentErrors;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) alignmentErrors(29)};

bAlignmentErrors **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 19.2.6.1.7.

NOTE—The approximate minimum time between counter rollovers is 80 h.;

aFramesTooLong **ATTRIBUTE**
DERIVED FROM aRMCounter;
BEHAVIOUR bFramesTooLong;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) framesTooLong(30)};

bFramesTooLong **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 19.2.6.1.8.

NOTE—The approximate minimum time between counter rollovers is 61 days.;

aShortEvents **ATTRIBUTE**
DERIVED FROM aRMCounter;
BEHAVIOUR bShortEvents;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) shortEvents(31)};

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bShortEvents **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.6.1.9.

NOTE—The approximate minimum time between counter rollovers is 16 h;

aRunts **ATTRIBUTE**
DERIVED FROM aRMCounter;
BEHAVIOUR bRunts;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) runts(32)};

bRunts **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.6.1.10.

NOTE—The approximate minimum time for counter rollover is 16 h.;

aCollisions **ATTRIBUTE**
DERIVED FROM aRMCounter;
BEHAVIOUR bCollisions;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) collisions(33)};

bCollisions **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.6.1.11.

NOTE—The approximate minimum time for counter rollover is 16 h.;

aLateEvents **ATTRIBUTE**
DERIVED FROM aRMCounter;
BEHAVIOUR bLateEvents;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) lateEvents(34)};

bLateEvents **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.6.1.12.

NOTE—The approximate minimum time between counter rollovers is 81 h.;

aVeryLongEvents **ATTRIBUTE**
DERIVED FROM aRMCounter;
BEHAVIOUR bVeryLongEvents;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) veryLongEvents(35)};

bVeryLongEvents **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.6.1.13.;

NOTE—The approximate minimum time between counter rollovers is 198 days.;

aDataRateMismatches **ATTRIBUTE**
DERIVED FROM aRMCounter;
BEHAVIOUR bDataRateMismatches;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) dataRateMismatches(36)};

bDataRateMismatches **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 19.2.6.1.14.;

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aAutoPartitions **ATTRIBUTE**
DERIVED FROM aRMCounter;
BEHAVIOUR bAutoPartitions;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) autoPartitions(37)};

bAutoPartitions **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 19.2.6.1.15.;

aLastSourceAddress **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802CommonDefinitions.MACAddress;
MATCHES FOR EQUALITY;
BEHAVIOUR bLastSourceAddress;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) lastSourceAddress(38)};

bLastSourceAddress **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 19.2.6.1.16.;

aSourceAddressChanges **ATTRIBUTE**
DERIVED FROM aRMCounter;
BEHAVIOUR bSourceAddressChanges;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) sourceAddressChanges(39)};

bSourceAddressChanges **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 19.2.6.1.17.

NOTE—The approximate minimum time for counter rollover is 81 h.;

H.2.4.3 Port actions

acPortAdminControl **ACTION**
BEHAVIOUR bPortAdminControl;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.PortAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) action(9) portAdminControl(42)};

bPortAdminControl **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 19.2.6.2.1.;

H.2.5 Common Attributes Template

aRMCounter **ATTRIBUTE**
DERIVED FROM "ISO/IEC 10165-2":GenericSettableCounter
BEHAVIOUR bRMCounter
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) rmCounter(12)};

bRMCounter **BEHAVIOUR**
DEFINED AS The internal event that is counted is specified by each calling attribute.
The maximum value is 4 294 967 295 (i.e., wraps at 32 bits).
The estimated minimum wrap time is called out in a note included in the

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behaviour of each calling attribute.
The counter that this is derived from initializes to zero. Initialization to zero is not a requirement of this standard, this standard only supports a GET operation of this counter.;

H.3 GDMO specification for MAU Management Objects

NOTE—The arcs (that is, object identifier values) defined in Annex 30A deprecate the arcs previously defined in H.1 (Layer Management), H.2 (Repeater Management), and H.3 (MAU Management). See IEEE Std 802.1F-1993, Annex C4.

This clause formally defines the MAU Management Objects using the templates specified in ISO/IEC 10165-4: 1992.

Each attribute definition in this clause references directly by means of the WITH ATTRIBUTE SYNTAX construct or indirectly by means of the DERIVED FROM construct an ASN.1 type or subtype that defines the attribute's type and range. Those ASN.1 types and subtypes defined exclusively for CSMA/CD Management are included in H.4.

H.3.1 MAU Managed Object Class

H.3.1.1 MAU formal definition

```
oMAU                                MANAGED OBJECT CLASS
    DERIVED FROM                    "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992":top;
    CHARACTERIZED BY
        pMAUBasic                   PACKAGE
            ATTRIBUTES              aMAUID                  GET,
                                    aMAUType                GET,
                                    aMediaAvailable         GET,
                                    aJabber                 GET,
                                    aMAUAdminControl        GET;
            NOTIFICATIONS           nJabber;
        ;
    ;
    CONDITIONAL PACKAGES
        pMAUControl                 PACKAGE
            ACTIONS                 acResetMAU,
                                    acMAUAdminState;
            REGISTERED AS           {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) package(4) mau-
                                    ControlPkg(202)};
            PRESENT IF              The pMAUControl package is implemented.;

        pMediaLossTracking          PACKAGE
            ATTRIBUTES              aLoseMediaCounter       GET;
            REGISTERED AS           {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) package(4) media-
                                    LossTrackingPkg(203)};
            PRESENT IF              MAU TypeValue = AUI or if the pMediaLossTracking package is
                                    implemented.;

        pBroadbandDTEMAU            PACKAGE
            ATTRIBUTES              aBbMAUXmitRcvSplitType  GET,
                                    aBroadbandFrequencies   GET;
            REGISTERED AS           {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) package(4) broad-
                                    bandMAUPkg(204)};
```

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PRESENT IF The MAU is of type 10BROAD36.;

REGISTERED AS {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) managedObjectClass(3) mauObjectClass(201)};

nbRepeaterMAUName NAME BINDING
SUBORDINATE OBJECT CLASS oMAU;
NAMED BY SUPERIOR OBJECT CLASS (of oRepeaterPort)
oPort AND SUBCLASSES;
--{1.2.840.10006.19.3.3}
WITH ATTRIBUTE aMAUID;
REGISTERED AS {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) nameBinding(6) repeaterName(205)};

nbDTEMAUName NAME BINDING
SUBORDINATE OBJECT CLASS oMAU;
NAMED BY SUPERIOR OBJECT CLASS (of oDTEPort)
oDTECSMACDInterface AND SUBCLASSES
(1.2.840.10006.5.3.X};
WITH ATTRIBUTE aMAUID;
REGISTERED AS {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) nameBinding(6) dteName(206)};

H.3.1.2 MAU attributes

aMAUID **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR BEHAVIOUR EQUALITY;
bMAUID;
REGISTERED AS {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) attribute(7) mauID(207)};

bMAUID **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 20.2.2.1.1.;

aMAUType **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.TypeValue;
MATCHES FOR BEHAVIOUR EQUALITY, ORDERING;
bMAUType;
REGISTERED AS {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) attribute(7) mauType(208)};

bMAUType **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 20.2.2.1.2.;

aMediaAvailable **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MediaAvailState;
MATCHES FOR BEHAVIOUR EQUALITY, ORDERING;
bMediaAvailable;
REGISTERED AS {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) attribute(7) mauMediaAvailable(209)};

bMediaAvailable **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 20.2.2.1.3.;

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aLoseMediaCounter **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.aRMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bLoseMediaCounter;
REGISTERED AS {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) attribute(7) mauLoseMediaCounter(201)};

bLoseMediaCounter **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 20.2.2.1.4.;

aJabber **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.Jabber;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bJabberAttribute;
REGISTERED AS {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) attribute(7) jabber(211)};

bJabberAttribute **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 20.2.2.1.5.;

aMAUAdminState **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AdminState;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bMAUAdminState;
REGISTERED AS {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) attribute(7) mauAdminState(212)};

bMAUAdminState **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 20.2.2.1.6.;

aBbMAUXmitRcvSplitType **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.BbandXmitRcvSplitType;
MATCHES FOR EQUALITY;
BEHAVIOUR bBbMAUXmitRcvSplitType;
REGISTERED AS {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) attribute(7) bBandSplitType(213)};

bBbMAUXmitRcvSplitType **BEHAVIOUR**
DEFINED AS See "BEHAVIOUR DEFINED AS" in 20.2.2.1.7.;

aBroadbandFrequencies **ATTRIBUTE**
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.BbandFrequency;
MATCHES FOR EQUALITY;
BEHAVIOUR bBroadbandFrequencies;
REGISTERED AS {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) attribute(7) bBandFrequencies(214)};

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bBroadbandFrequencies **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 20.2.2.1.8.;

H.3.1.3 MAU actions

acResetMAU **ACTION**
BEHAVIOUR bResetMAU;
MODE CONFIRMED;
REGISTERED AS {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) action(9) resetMAU(215)};

bResetMAU **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 20.2.2.2.1.;

acMAUAdminControl **ACTION**
BEHAVIOUR bMAUAdminControl;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.AdminState;
MODE CONFIRMED;
REGISTERED AS {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) action(9) mauAdminCtrl(216)};

bMAUAdminControl **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 20.2.2.2.2.;

H.3.1.4 MAU notifications

nJabber **NOTIFICATION**
BEHAVIOUR bJabberNotification;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.Jabber;
;
REGISTERED AS {iso(1) std(0) iso8802(8802) csma(3) mauMgt(20) notification(10) jabber(217)};

bJabberNotification **BEHAVIOUR**
DEFINED AS See “BEHAVIOUR DEFINED AS” in 20.2.2.3.1.;

H.4 GDMO and ASN.1 definitions for management

H.4.1 Common Attributes Template

aRMCounter **ATTRIBUTE**
DERIVED FROM “ISO/IEC 10165-5”:genericWrappingCounter;
BEHAVIOUR bRMCounter;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) repeaterMgt(19) attribute(7) rmCounter(12)};

bRMCounter **BEHAVIOUR**
DEFINED AS Wraps at 32 bits, that is, this counter reaches its maximum value at $2^{32}-1$ (decimal 4 294 967 295) and then rolls over to zero on the next increment. The counter from which this is derived initializes to zero. Initialization to zero is not a requirement of this standard;

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```
aLMCounter                  ATTRIBUTE
    DERIVED FROM            "ISO/IEC 10165-5":genericWrappingCounter;
    BEHAVIOUR               bRMCounter;
    REGISTERED AS       {iso(1) member-body(2) us(840) 802dot3(10006) csmalayermgt(5)
                        attribute(7) lmCounter(150)};
```

H.4.2 ASN.1 module

This ASN.1 module defines the ASN.1 types and subtypes that are referred to immediately after the WITH ATTRIBUTE SYNTAX construct in this document's uses of the attribute template defined in ISO/IEC 10165-4 : 1992.

```
IEEE802Dot3-MgmtAttributeModule {iso(1) member-body(2) us(840) 802dot3(10006)
global(1) asn1Module(2) commonDefinitions(X) version(X)} DEFINITIONS IMPLICIT TAGS::= BEGIN

EXPORTS     --everything
IMPORTS     --implicitly imports ISO 8824
        MACAddress      FROM IEEE802CommonDefinitions
                        {iso(1) member-body(2) us(840) ieee802-1partf(x) asn1Module(2)
                        commonDefinitions(0) version1(0)};

AdminState::= ENUMERATED {
    other               (1),    --undefined
    unknown             (2),    --initializing, true state not yet known
    operational         (3),    --powered and connected
    standby             (4),    --inactive but on
    shutdown            (5)     --similar to power down
    }

AttemptArray::= SEQUENCE OF aLMCounter--array [1..attempt limit – 1]

AutoPartitionState::= ENUMERATED {
    autoPartitioned     (1),
    notAutoPartitioned  (2)
    }

BbandFrequency::= SEQUENCE {
    xmitCarrierFrequency    [1]  INTEGER , --Freq. in MHz times 4, (250 kHz resolution)
    translationFrequency    [2]  INTEGER   --Freq. in MHz times 4, (250 kHz resolution)
    }

BbandXmitRcvSplitType::= ENUMERATED {
    other               (1),    --undefined
    single              (2),    --single-cable system
    dual                (3)     --dual-cable system, offset normally zero
    }

BitString ::= BIT STRING (SIZE (1..1024))

Jabber::= SEQUENCE {
    jabberFlag          [1]  JabberFlag,
    jabberCounter       [2]  JabberCounter
    }
```

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```
JabberFlag::= ENUMERATED {
    other                   (1),    --undefined
    unknown                 (2),    --initializing, true state not yet known
    normal                  (3),    --state is true or normal
    fault                   (4)     --state is false, fault or abnormal
    }
JabberCounter::= INTEGER (0..2^32 –1)

MediaAvailState::= ENUMERATED {
    other                   (1),    --undefined
    unknown                 (2),    --initializing, true state not yet known
    available               (3),    --link or light normal, loopback normal
    not available           (4),    --link loss or low light, no loopback
    remote fault            (5),    --remote fault, applies only to 10BASE-FB
    invalid signal          (6)     --invalid signal, applies only to 10BASE-FB
    }

MulticastAddressList::= SEQUENCE OF MACAddress

OneOfName ::= INTEGER (1..1024)

PortAdminState::= ENUMERATED {
    disabled                (1),
    enabled                 (2)
    }
RepeaterHealthData ::= OCTET STRING (SIZE (0..255))

RepeaterHealthInfo::= SEQUENCE {
    repeaterHealthState     [1]   RepeaterHealthState,
    repeaterHealthText      [2]   RepeaterHealthText  OPTIONAL,
    repeaterHealthData      [3]   RepeaterHealthData  OPTIONAL
    }

RepeaterHealthState::= ENUMERATED {
    other                   (1),    --undefined or unknown
    ok                      (2),    --no known failures
    repeaterFailure         (3),    --known to have a repeater-related failure
    groupFailure            (4),    --known to have a group-related failure
    portFailure             (5),    --known to have a port-related failure
    generalFailure          (6)     --has a failure condition, unspecified type
    }

RepeaterHealthText ::= PrintableString (SIZE (0..255))

TrueFalse ::= BOOLEAN

TypeValue::= ENUMERATED {
    global                  (0),    --undefined
    other                   (1),    --undefined
    unknown                 (2),    --initializing, true state not yet known
    AUI                     (7),    --no internal MAU, view from AUI
    10BASE5                 (8),    --Thick coaxial cable MAU as specified in Clause 8
    FOIRL                   (9),    --FOIRL MAU as specified in 9.9
    10BASE2                 (10),   --Thin coaxial cable MAU as specified in Clause 10
```


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```
    10BROAD36       (11),  --Broadband DTE MAU as specified in Clause 11
    10BASE-T        (14),  --UTP MAU as specified in Clause 14
    10BASE-FP       (16),  --Passive fiber MAU, specified in Clause 16
    10BASE-FB       (17),  --Synchronous fiber MAU, specified in Clause 17
    10BASE-FL       (18)   --Asynchronous fiber  MAU, specified in Clause 18
    }

END
```

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Information technology—
Telecommunications and information exchange between systems—
Local and metropolitan area networks—Specific requirements—

Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) access method and physical layer specifications

SECTION TWO: This section includes Clauses 21 through 33 and Annexes 22A through 32A.

21. Introduction to 100 Mb/s baseband networks, type 100BASE-T

21.1 Overview

100BASE-T couples the IEEE 802.3 CSMA/CD MAC with a family of 100 Mb/s Physical Layers. While the MAC can be readily scaled to higher performance levels, new Physical Layer standards are required for 100 Mb/s operation.

The relationships between 100BASE-T, the existing IEEE 802.3 (CSMA/CD MAC), and the ISO/IEC Open System Interconnection (OSI) reference model is shown in Figure 21–1.

100BASE-T uses the existing IEEE 802.3 MAC layer interface, connected through a Media-Independent Interface layer to a Physical Layer entity (PHY) sublayer such as 100BASE-T4, 100BASE-TX, or 100BASE-FX.

100BASE-T extends the IEEE 802.3 MAC to 100 Mb/s. The bit rate is faster, bit times are shorter, packet transmission times are reduced, and cable delay budgets are smaller—all in proportion to the change in bandwidth. This means that the ratio of packet duration to network propagation delay for 100BASE-T is the same as for 10BASE-T.

21.1.1 Reconciliation Sublayer (RS) and Media Independent Interface (MII)

The Media Independent Interface (Clause 22) provides an interconnection between the Media Access Control (MAC) sublayer and Physical Layer entities (PHY) and between PHY Layer and Station Management (STA) entities. This MII is capable of supporting both 10 Mb/s and 100 Mb/s data rates through four bit wide (nibble wide) transmit and receive paths. The Reconciliation sublayer provides a mapping between the signals provided at the MII and the MAC/PLS service definition.

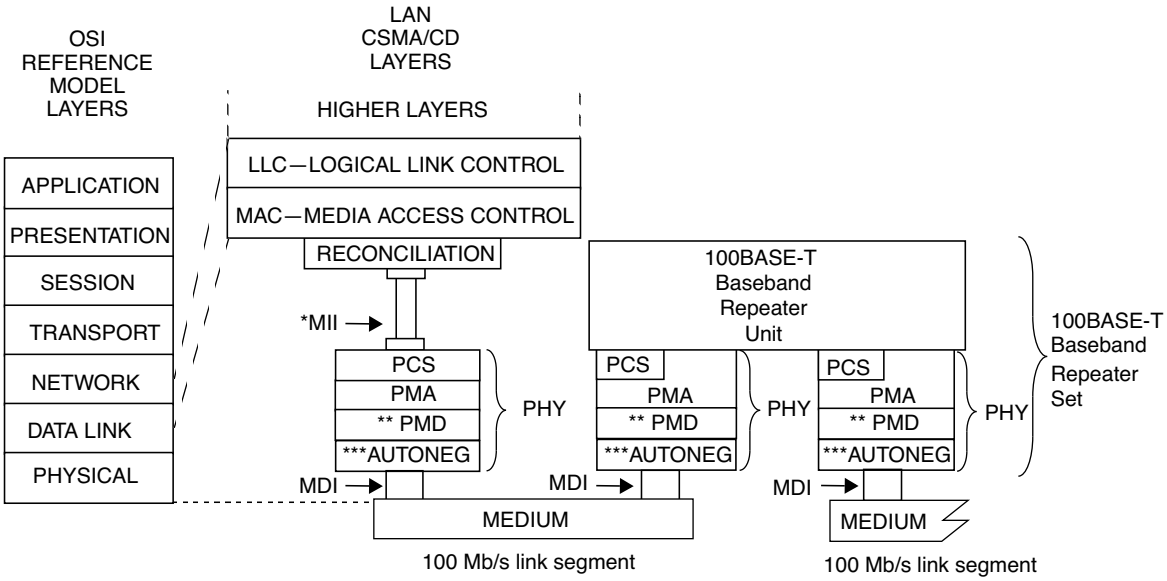
21.1.2 Physical Layer signaling systems

The following portion of this standard specifies a family of Physical Layer implementations. 100BASE-T4 (Clause 23) uses four pairs of ISO/IEC 11801 Category 3, 4, or 5 balanced cabling. 100BASE-TX (Clauses

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MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* MII is optional for 10 Mb/s DTEs and for 100 Mb/s systems and is not specified for 1 Mb/s systems.
** PMD is specified for 100BASE-X only; 100BASE-T4 does not use this layer.
Use of MII between PCS and Baseband Repeater Unit is optional.
*** AUTONEG is optional.

Figure 21–1—Architectural positioning of 100BASE-T

24 and 25) uses two pairs of Category 5 balanced cabling or 150 Ω shielded balanced cabling as defined by ISO/IEC 11801. 100BASE-FX (Clauses 24 and 26) uses two multi-mode fibers. FDDI (ISO/IEC 9314 and ANSI X3T12) Physical Layers are used to provide 100BASE-TX and 100BASE-FX physical signaling channels, which are defined under 100BASE-X (Clause 24). 100BASE-T2 (Clause 32) uses two pairs of ISO/IEC 11801 Category 3, 4, or 5 balanced cabling.

21.1.3 Repeater

Repeater sets (Clause 27) are an integral part of any 100BASE-T network with more than two DTEs in a collision domain. They extend the physical system topology by coupling two or more segments. Multiple repeaters are permitted within a single collision domain to provide the maximum path length.

21.1.4 Auto-Negotiation

Auto-Negotiation (Clause 28) provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determine common abilities, and configure for joint operation. Auto-Negotiation is performed out-of-band using a pulse code sequence that is compatible with the 10BASE-T link integrity test sequence.

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21.1.5 Management

Managed objects, attributes, and actions are defined for all 100BASE-T components (Clause 30). This clause consolidates all IEEE 802.3 management specifications so that 10 Mb/s, 100 Mb/s or 10/100 Mb/s agents can be managed by existing 10 Mb/s-only network management stations with little or no modification to the agent code.

21.2 References

See 1.3.

21.3 Definitions

See 1.4.

21.4 Abbreviations

See 1.5.

21.5 State diagrams

State machine diagrams take precedence over text.

The conventions of 1.2 are adopted, with the following extensions.

21.5.1 Actions inside state blocks

The actions inside a state block execute instantaneously. Actions inside state blocks are atomic (i.e., uninterruptible).

After performing all the actions listed in a state block one time, the state block then continuously evaluates its exit conditions until one is satisfied, at which point control passes through a transition arrow to the next block. While the state awaits fulfillment of one of its exit conditions, the actions inside do not implicitly repeat.

The characters • and [bracket] are *not* used to denote any special meaning.

Valid state actions may include .indicate and .request messages.

No actions are taken outside of any state block.

21.5.2 State diagram variables

Once set, variables retain their values as long as succeeding blocks contain no references to them.

Setting the parameter of a formal interface message assures that, on the next transmission of that message, the last parameter value set will be transmitted.

Testing the parameter of a formal interface messages tests the value of that message parameter that was received on the last transmission of said message. Message parameters may be assigned default values that persist until the first reception of the relevant message.

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21.5.3 State transitions

The following terms are valid transition qualifiers:

a) Boolean expressions
b) An event such as the expiration of a timer: timer_done
c) An event such as the reception of a message: PMA_UNITDATA.indicate
d) An unconditional transition: UCT
e) A branch taken when other exit conditions are not satisfied: ELSE

Any open arrow (an arrow with no source block) represents a global transition. Global transitions are evaluated continuously whenever any state is evaluating its exit conditions. When a global transition becomes true, it supersedes all other transitions, including UCT, returning control to the block pointed to by the open arrow.

21.5.4 Operators

The state machine operators are shown in Table 21–1.

Table 21–1—State machine operators

Character	Meaning
*	Boolean AND
+	Boolean OR
∧	Boolean XOR
!	Boolean NOT
<	Less than
≤	Less than or equal to
=	Equals (a test of equality)
≠	Not equals
≥	Greater than or equal to
>	Greater than
( )	Indicates precedence
⇐	Assignment operator
∈	Indicates membership
∉	Indicates nonmembership
|	Catenate
ELSE	No other state condition is satisfied

21.6 Protocol Implementation Conformance Statement (PICS) proforma

21.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to any 100 Mb/s portion of this standard shall complete a Protocol Implementation Conformance Statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. The PICS can be used for a variety of purposes by various parties, including the following:

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a) As a checklist by the protocol implementor, to reduce the risk of failure to conform to the standard through oversight;
b) As a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard PICS proforma, by the supplier and acquirer, or potential acquirer, of the implementation;
c) As a basis for initially checking the possibility of interworking with another implementation by the user, or potential user, of the implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible PICS);
d) As the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation, by a protocol tester.

21.6.2 Abbreviations and special symbols

The following symbols are used in the PICS proforma:

M	mandatory field/function
!	negation
O	optional field/function
O.<n>	optional field/function, but at least one of the group of options labeled by the same numeral <n> is required
O/<n>	optional field/function, but one and only one of the group of options labeled by the same numeral <n> is required
X	prohibited field/function
<item>:	simple-predicate condition, dependent on the support marked for <item>
<item1>*<item2>:	AND-predicate condition, the requirement must be met if both optional items are implemented

21.6.3 Instructions for completing the PICS proforma

The first part of the PICS proforma, Implementation Identification and Protocol Summary, is to be completed as indicated with the information necessary to identify fully both the supplier and the implementation.

The main part of the PICS proforma is a fixed-format questionnaire divided into subclauses, each containing a group of items. Answers to the questionnaire items are to be provided in the right-most column, either by simply marking an answer to indicate a restricted choice (usually Yes, No, or Not Applicable), or by entering a value or a set or range of values. (Note that there are some items where two or more choices from a set of possible answers can apply; all relevant choices are to be marked.)

Each item is identified by an item reference in the first column; the second column contains the question to be answered; the third column contains the reference or references to the material that specifies the item in the main body of the standard; the sixth column contains values and/or comments pertaining to the question to be answered. The remaining columns record the status of the items—whether the support is mandatory, optional or conditional—and provide the space for the answers.

The supplier may also provide, or be required to provide, further information, categorized as either Additional Information or Exception Information. When present, each kind of further information is to be provided in a further subclause of items labeled A<i> or X<i>, respectively, for cross-referencing purposes, where <i> is any unambiguous identification for the item (e.g., simply a numeral); there are no other restrictions on its format or presentation.

A completed PICS proforma, including any Additional Information and Exception Information, is the Protocol Implementation Conformance Statement for the implementation in question.

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Note that where an implementation is capable of being configured in more than one way, according to the items listed under Major Capabilities/Options, a single PICS may be able to describe all such configurations. However, the supplier has the choice of providing more than one PICS, each covering some subset of the implementation's configuration capabilities, if that would make presentation of the information easier and clearer.

21.6.4 Additional information

Items of Additional Information allow a supplier to provide further information intended to assist the interpretation of the PICS. It is not intended or expected that a large quantity will be supplied, and the PICS can be considered complete without any such information. Examples might be an outline of the ways in which a (single) implementation can be set up to operate in a variety of environments and configurations; or a brief rationale, based perhaps upon specific application needs, for the exclusion of features that, although optional, are nonetheless commonly present in implementations.

References to items of Additional Information may be entered next to any answer in the questionnaire, and may be included in items of Exception Information.

21.6.5 Exceptional information

It may occasionally happen that a supplier will wish to answer an item with mandatory or prohibited status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No pre-printed answer will be found in the Support column for this; instead, the supplier is required to write into the Support column an X<i> reference to an item of Exception Information, and to provide the appropriate rationale in the Exception item itself.

An implementation for which an Exception item is required in this way does not conform to this standard.

Note that a possible reason for the situation described above is that a defect in the standard has been reported, a correction for which is expected to change the requirement not met by the implementation.

21.6.6 Conditional items

The PICS proforma contains a number of conditional items. These are items for which both the applicability of the item itself, and its status if it does apply—mandatory, optional, or prohibited—are dependent upon whether or not certain other items are supported.

Individual conditional items are indicated by a conditional symbol of the form "<item>:<s>" in the Status column, where "<item>" is an item reference that appears in the first column of the table for some other item, and "<s>" is a status symbol, M (Mandatory), O (Optional), or X (Not Applicable).

If the item referred to by the conditional symbol is marked as supported, then 1) the conditional item is applicable, 2) its status is given by "<s>", and 3) the support column is to be completed in the usual way. Otherwise, the conditional item is not relevant and the Not Applicable (N/A) answer is to be marked.

Each item whose reference is used in a conditional symbol is indicated by an asterisk in the Item column.

21.7 Relation of 100BASE-T to other standards

Suitable entries for Table G.1 of ISO/IEC 11801, Annex G would be as follows:

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a) Within the section Balanced Cabling Link Class C (specified up to 16 MHz):
   CSMA/CD 100BASE-T2 ISO/IEC 8802-3/DAD 1995 2
   CSMA/CD 100BASE-T4* ISO/IEC 8802-3/DAD 1995 4
b) Within the section Optical Link:
   CSMA/CD 100BASE-FX ISO/IEC 8802-3/DAD 1995 2
c) Within the section Balanced Cabling Link Class D (defined up to 100 MHz):
   CSMA/CD 100BASE-TX ISO/IEC 8802-3/DAD 1995 2

*To support 100BASE-T4 applications, Class C links shall have a NEXT value of at least 3 dB in excess of the values specified in 6.2.4.

Suitable entries for Table G.4 of ISO/IEC 11801, Annex G, would be as follows:

	Balanced cabling per Clauses 5, 7, and 8							**Performance based cabling per Clause 6**											
								Class A			**Class B**			**Class C**			**Class D**		
	Cat 3 100 Ω	**Cat 4 100 Ω**	**Cat 5 100 Ω**	**Cat 3 120 Ω**	**Cat 4 120 Ω**	**Cat 5 120 Ω**	**150 Ω**	**100 Ω**	**120 Ω**	**150 Ω**	**100 Ω**	**120 Ω**	**150 Ω**	**100 Ω**	**120 Ω**	**150 Ω**	**100 Ω**	**120 Ω**	**150 Ω**
802.3: 100BASE-T2	I[a]	I	I	I	I	I	I							I			I[a]	I	I
802.3: 100BASE-T4	I[a]	I	I		I	I								I			I[a]	I	
802.3: 100BASE-TX			I[a]				I[a]										I[a]		I[a]

[a]802.3 imposes additional requirements on propagation delay.

A suitable entry for Table G.5 of ISO/IEC 11801, Annex G, would be as follows:

	Fibre per 5, 7, and 8			**Optical link per Clause 8**								
				Horizontal			**Building backbone**			**Campus backbone**		
	62.5/125 mm MMF	**50/125 mm MMF**	**10/125 mm MMF**	**62.5/125 mm MMF**	**50/125 mm MMF**	**10/125 mm MMF**	**62.5/125 mm MMF**	**50/125 mm MMF**	**10/125 mm MMF**	**62.5/125 mm MMF**	**50/125 mm MMF**	**10/125 mm MMF**
802.3: 100BASE-FX	N	I		N	I		N	I		N	I	

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21.8 MAC delay constraints (exposed MII)

100BASE-T makes the following assumptions about MAC performance. These assumptions apply to any MAC operating in half duplex mode with an exposed MII.

Table 21–2—MAC delay assumptions (exposed MII)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MAC ⇔ MII	MAC transmit start to TX_EN sampled		4		TX_CLK rising
	CRS assert to MAC detect	0	8		
	CRS de-assert to MAC detect	0	8		
	CRS assert to TX_EN sampled (worst case nondeferred transmit)		16		TX_CLK rising
	COL assert to MAC detect	0	8		
	COL de-assert to MAC detect	0	8		
	COL assert to TXD = Jam sampled (worst-case collision response)		16		TX_CLK rising; first nibble of jam

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22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

22.1 Overview

This clause defines the logical, electrical, and mechanical characteristics for the Reconciliation Sublayer (RS) and Media Independent Interface (MII) between CSMA/CD media access controllers and various PHYs. Figure 22–1 shows the relationship of the Reconciliation sublayer and MII to the ISO/IEC OSI reference model.

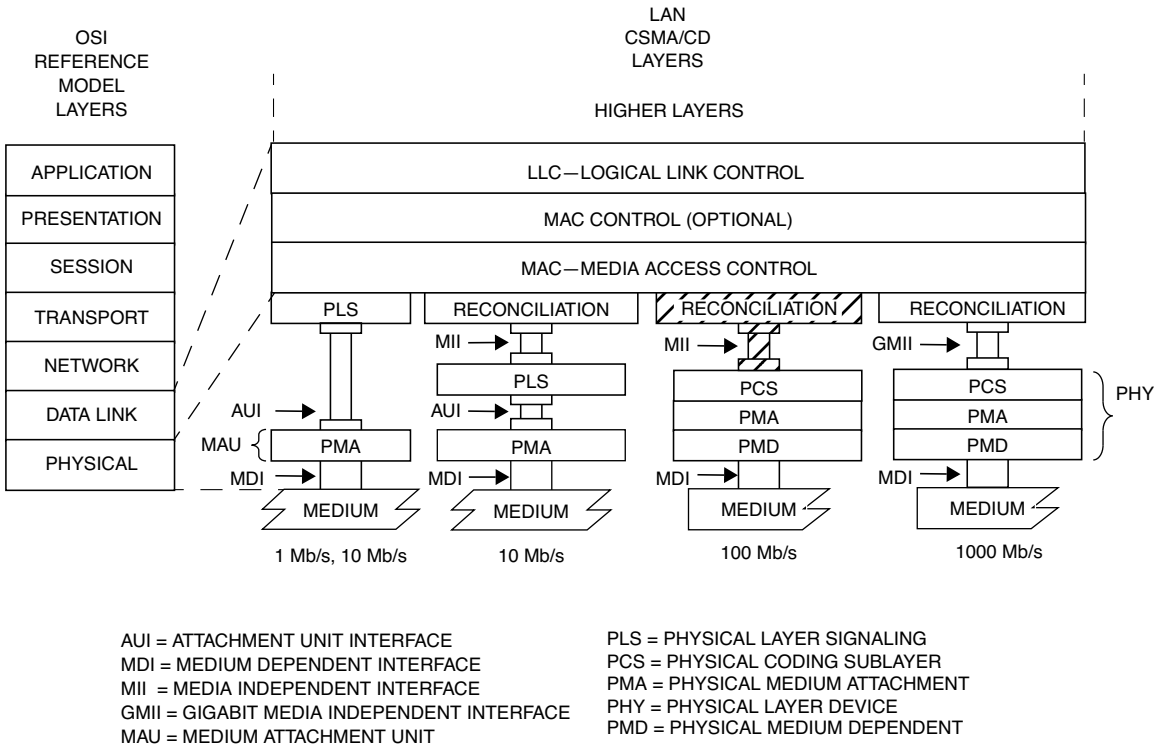


Figure 22–1—MII location in the protocol stack

The purpose of this interface is to provide a simple, inexpensive, and easy-to-implement interconnection between Media Access Control (MAC) sublayers and PHYs for data transfer at 10 Mb/s and 100 Mb/s, and between Station Management (STA) and PHY entities supporting data transfer at 10 Mb/s or above (see 22.2.4).

This interface has the following characteristics:

a) It is capable of supporting 10 Mb/s and 100 Mb/s rates for data transfer, and management functions for PHYs supporting data transfer at 10 Mb/s of above (see 22.2.4).
b) Data and delimiters are synchronous to clock references.
c) It provides independent four bit wide transmit and receive data paths.
d) It uses TTL signal levels, compatible with common digital CMOS ASIC processes.
e) It provides a simple management interface.
f) It is capable of driving a limited length of shielded cable.
g) It provides full duplex operation.

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22.1.1 Summary of major concepts

a) Each direction of data transfer is serviced with seven (making a total of 14) signals: Data (a four-bit bundle), Delimiter, Error, and Clock.
b) Two media status signals are provided. One indicates the presence of carrier, and the other indicates the occurrence of a collision.
c) A management interface comprised of two signals provides access to management parameters and services.
d) The Reconciliation sublayer maps the signal set provided at the MII to the PLS service definition specified in Clause 6.

22.1.2 Application

This clause applies to the interface between MAC sublayer and PHYs, and between PHYs and Station Management entities. The implementation of the interface may assume any of the following three forms:

a) A chip-to-chip (integrated circuit to integrated circuit) interface implemented with traces on a printed circuit board.
b) A motherboard to daughterboard interface between two or more printed circuit boards.
c) An interface between two printed circuit assemblies that are attached with a length of cable and an appropriate connector.

Figure 22–2 provides an example of the third application environment listed above. All MII conformance tests are performed at the mating surfaces of the MII connector, identified by the line A-A.

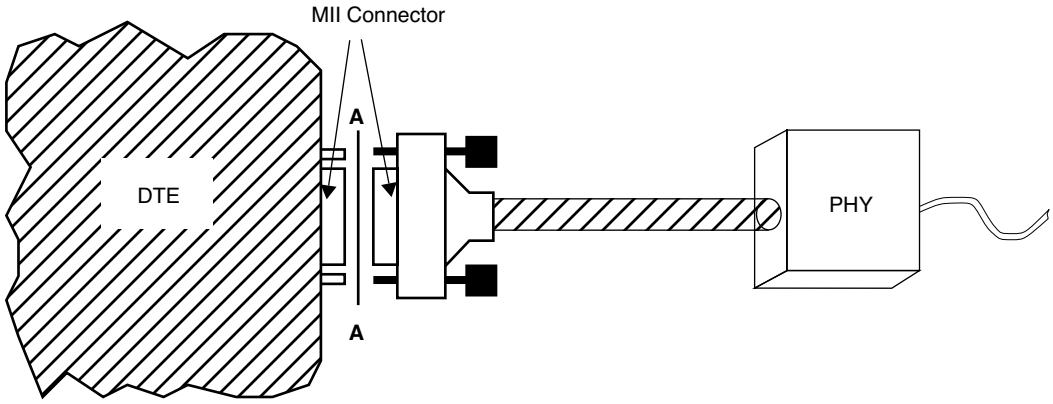


Figure 22–2—Example application showing location of conformance test

This interface is used to provide media independence for various forms of unshielded twisted-pair wiring, shielded twisted-pair wiring, fiber optic cabling, and potentially other media, so that identical media access controllers may be used with any of these media.

To allow for the possibility that multiple PHYs may be controlled by a single Station Management entity, the MII management interface has provisions to accommodate up to 32 PHYs, with the restriction that a maximum of one PHY may be attached to a management interface via the mechanical interface defined in 22.6.

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22.1.3 Rates of operation

The MII can support two specific data rates, 10 Mb/s and 100 Mb/s. The functionality is identical at both data rates, as are the signal timing relationships. The only difference between 10 Mb/s and 100 Mb/s operation is the nominal clock frequency.

PHYs that provide an MII are not required to support both data rates, and may support either one or both. PHYs must report the rates they are capable of operating at via the management interface, as described in 22.2.4.

22.1.4 Allocation of functions

The allocation of functions at the MII is such that it readily lends itself to implementation in both PHYs and MAC sublayer entities. The division of functions balances the need for media independence with the need for a simple and cost-effective interface.

While the Attachment Unit Interface (AUI) was defined to exist between the Physical Signaling (PLS) and Physical Media Attachment (PMA) sublayers for 10 Mb/s DTEs, the MII maximizes media independence by cleanly separating the Data Link and Physical Layers of the ISO (IEEE) seven-layer reference model. This allocation also recognizes that implementations can benefit from a close coupling of the PLS or PCS sublayer and the PMA sublayer.

22.1.5 Relationship of MII and GMII

The Gigabit Media Independent Interface (GMII) is similar to the MII. The GMII uses the MII management interface and register set specified in 22.2.4. These common elements of operation allow Station Management to determine PHY capabilities for any supported speed of operation and configure the station based on those capabilities. In a station supporting both MII and GMII operation, configuration of the station would include enabling either the MII or GMII operation as appropriate for the data rate of the selected PHY.

Most of the MII and GMII signals use the same names, but the width of the RXD and TXD data bundles and the semantics of the associated control signals differ between MII and GMII operation. The GMII transmit path clocking also differs significantly from MII clocking. MII operation of these signals and clocks is specified within Clause 22 and GMII operation is specified within Clause 35.

22.2 Functional specifications

The MII is designed to make the differences among the various media absolutely transparent to the MAC sublayer. The selection of logical control signals and the functional procedures are all designed to this end. Additionally, the MII is designed to be easily implemented at minimal cost using conventional design techniques and manufacturing processes.

22.2.1 Mapping of MII signals to PLS service primitives and Station Management

The Reconciliation sublayer maps the signals provided at the MII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the Reconciliation sublayer behave in exactly the same manner as defined in Clause 6. The MII signals are defined in detail in 22.2.2.

Figure 22–3 depicts a schematic view of the Reconciliation sublayer inputs and outputs, and demonstrates that the MII management interface is controlled by the Station Management entity (STA).

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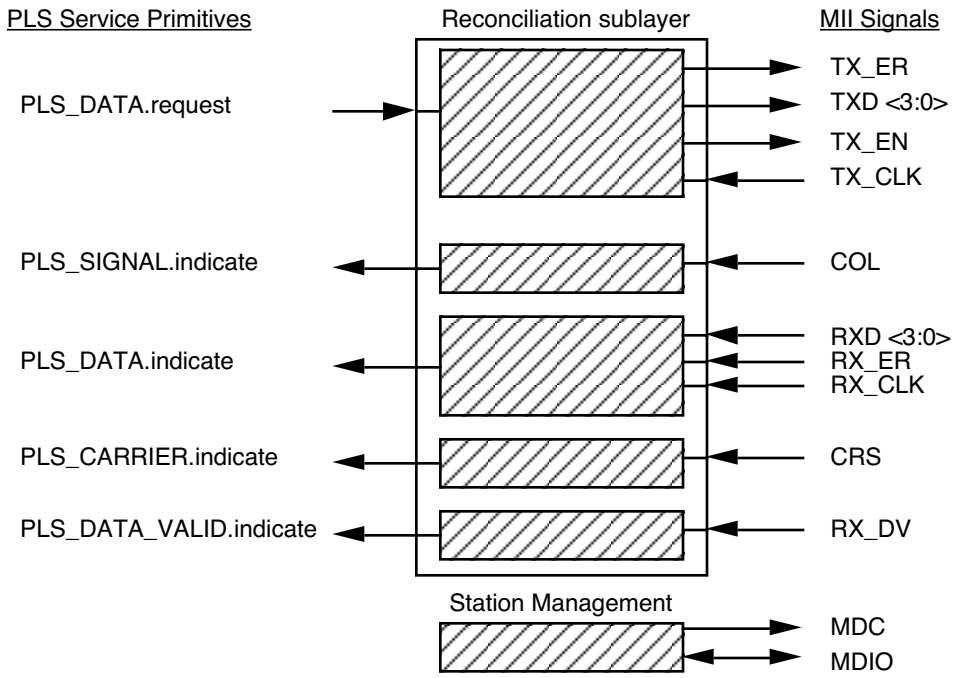


Figure 22–3—Reconciliation Sublayer (RS) inputs and outputs, and STA connections to MII

22.2.1.1 Mapping of PLS_DATA.request

22.2.1.1.1 Function

Map the primitive PLS_DATA.request to the MII signals TXD<3:0>, TX_EN and TX_CLK.

22.2.1.1.2 Semantics of the service primitive

PLS_DATA.request (OUTPUT_UNIT)

The OUTPUT_UNIT parameter can take one of three values: ONE, ZERO, or DATA_COMPLETE. It represents a single data bit. The values ONE and ZERO are conveyed by the signals TXD<3>, TXD<2>, TXD<1> and TXD<0>, each of which conveys one bit of data while TX_EN is asserted. The value DATA_COMPLETE is conveyed by the de-assertion of TX_EN. Synchronization between the Reconciliation sublayer and the PHY is achieved by way of the TX_CLK signal.

22.2.1.1.3 When generated

The TX_CLK signal is generated by the PHY. The TXD<3:0> and TX_EN signals are generated by the Reconciliation sublayer after every group of four PLS_DATA.request transactions from the MAC sublayer to request the transmission of four data bits on the physical medium or to stop transmission.

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22.2.1.2 Mapping of PLS_DATA.indicate

22.2.1.2.1 Function

Map the primitive PLS_DATA.indicate to the MII signals RXD<3:0>, RX_DV, RX_ER, and RX_CLK.

22.2.1.2.2 Semantics of the service primitive

PLS_DATA.indicate (INPUT_UNIT)

The INPUT_UNIT parameter can take one of two values: ONE or ZERO. It represents a single data bit. The values ONE and ZERO are derived from the signals RXD<3>, RXD<2>, RXD<1>, and RXD<0>, each of which represents one bit of data while RX_DV is asserted.

The value of the data transferred to the MAC is controlled by the RX_ER signal, see 22.2.1.5, Response to RX_ER indication from MII.

Synchronization between the PHY and the Reconciliation sublayer is achieved by way of the RX_CLK signal.

22.2.1.2.3 When generated

This primitive is generated to all MAC sublayer entities in the network after a PLS_DATA.request is issued. Each nibble of data transferred on RXD<3:0> will result in the generation of four PLS_DATA.indicate transactions.

22.2.1.3 Mapping of PLS_CARRIER.indicate

22.2.1.3.1 Function

Map the primitive PLS_CARRIER.indicate to the MII signal CRS.

22.2.1.3.2 Semantics of the service primitive

PLS_CARRIER.indicate (CARRIER_STATUS)

The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF. The values CARRIER_ON and CARRIER_OFF are derived from the MII signal CRS.

22.2.1.3.3 When generated

The PLS_CARRIER.indicate service primitive is generated by the Reconciliation sublayer whenever the CARRIER_STATUS parameter changes from CARRIER_ON to CARRIER_OFF or vice versa.

While the RX_DV signal is de-asserted, any transition of the CRS signal from de-asserted to asserted must cause a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and any transition of the CRS signal from asserted to de-asserted must cause a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value. At any time after CRS and RX_DV are both asserted, de-assertion of RX_DV must cause CARRIER_STATUS to transition to the CARRIER_OFF value. This transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value must be recognized by the MAC sublayer, even if the CRS signal is still asserted at the time.

NOTE—The behavior of the CRS signal is specified within this clause so that it can be mapped directly (with the appropriate implementation-specific synchronization) to the carrierSense variable in the MAC process Deference, which is

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described in 4.2.8. The behavior of the RX_DV signal is specified within this clause so that it can be mapped directly to the carrierSense variable in the MAC process BitReceiver, which is described in 4.2.9, provided that the MAC process BitReceiver is implemented to receive a nibble of data on each cycle through the inner loop.

22.2.1.4 Mapping of PLS_SIGNAL.indicate

22.2.1.4.1 Function

Map the primitive PLS_SIGNAL.indicate to the MII signal COL.

22.2.1.4.2 Semantics of the service primitive

PLS_SIGNAL.indicate (SIGNAL_STATUS)

The SIGNAL_STATUS parameter can take one of two values: SIGNAL_ERROR or NO_SIGNAL_ERROR. SIGNAL_STATUS assumes the value SIGNAL_ERROR when the MII signal COL is asserted, and assumes the value NO_SIGNAL_ERROR when COL is de-asserted.

22.2.1.4.3 When generated

The PLS_SIGNAL.indicate service primitive is generated whenever SIGNAL_STATUS makes a transition from SIGNAL_ERROR to NO_SIGNAL_ERROR or vice versa.

22.2.1.5 Response to RX_ER indication from MII

If, during frame reception, both RX_DV and RX_ER are asserted, the Reconciliation sublayer shall ensure that the MAC will detect a FrameCheckError in that frame.

This requirement may be met by incorporating a function in the Reconciliation sublayer that produces a result that is guaranteed to be not equal to the CRC result, as specified by the algorithm in 3.2.8, of the sequence of nibbles comprising the received frame as delivered to the MAC sublayer. The Reconciliation sublayer must then ensure that the result of this function is delivered to the MAC sublayer at the end of the received frame in place of the last nibble(s) received from the MII.

Other techniques may be employed to respond to RX_ER, provided that the result is that the MAC sublayer behaves as though a FrameCheckError occurred in the received frame.

22.2.1.6 Conditions for generation of TX_ER

If, during the process of transmitting a frame, it is necessary to request that the PHY deliberately corrupt the contents of the frame in such a manner that a receiver will detect the corruption with the highest degree of probability, then the signal TX_ER may be generated.

For example, a repeater that detects an RX_ER during frame reception on an input port may propagate that error indication to its output ports by asserting TX_ER during the process of transmitting that frame.

Since there is no mechanism in the definition of the MAC sublayer by which the transmit data stream can be deliberately corrupted, the Reconciliation sublayer is not required to generate TX_ER.

22.2.1.7 Mapping of PLS_DATA_VALID.indicate

22.2.1.7.1 Function

Map the primitive PLS_DATA_VALID.indicate to the MII signal RX_DV.

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22.2.1.7.2 Semantics of the service primitive

PLS_DATA_VALID.indicate (DATA_VALID_STATUS)

The DATA_VALID_STATUS parameter can take one of two values: DATA_VALID or DATA_NOT_VALID. DATA_VALID_STATUS assumes the value DATA_VALID when the MII signal RX_DV is asserted, and assumes the value DATA_NOT_VALID when RX_DV is de-asserted.

22.2.1.7.3 When generated

The PLS_DATA_VALID.indicate service primitive is generated by the Reconciliation sublayer whenever the DATA_VALID_STATUS parameter changes from DATA_VALID to DATA_NOT_VALID or vice versa.

22.2.2 MII signal functional specifications

22.2.2.1 TX_CLK (transmit clock)

TX_CLK (Transmit Clock) is a continuous clock that provides the timing reference for the transfer of the TX_EN, TXD, and TX_ER signals from the Reconciliation sublayer to the PHY. TX_CLK is sourced by the PHY.

The TX_CLK frequency shall be 25% of the nominal transmit data rate ± 100 ppm. For example, a PHY operating at 100 Mb/s must provide a TX_CLK frequency of 25 MHz, and a PHY operating at 10 Mb/s must provide a TX_CLK frequency of 2.5 MHz. The duty cycle of the TX_CLK signal shall be between 35% and 65% inclusive.

NOTE—See additional information in 22.2.4.1.5.

22.2.2.2 RX_CLK (receive clock)

RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV, RXD, and RX_ER signals from the PHY to the Reconciliation sublayer. RX_CLK is sourced by the PHY. The PHY may recover the RX_CLK reference from the received data or it may derive the RX_CLK reference from a nominal clock (e.g., the TX_CLK reference).

The minimum high and low times of RX_CLK shall be 35% of the nominal period under all conditions.

While RX_DV is asserted, RX_CLK shall be synchronous with recovered data, shall have a frequency equal to 25% of the data rate of the received signal, and shall have a duty cycle of between 35% and 65% inclusive.

When the signal received from the medium is continuous and the PHY can recover the RX_CLK reference and supply the RX_CLK on a continuous basis, there is no need to transition between the recovered clock reference and a nominal clock reference on a frame-by-frame basis. If loss of received signal from the medium causes a PHY to lose the recovered RX_CLK reference, the PHY shall source the RX_CLK from a nominal clock reference.

Transitions from nominal clock to recovered clock or from recovered clock to nominal clock shall be made only while RX_DV is de-asserted. During the interval between the assertion of CRS and the assertion of RX_DV at the beginning of a frame, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition until the PHY has successfully locked onto the recovered clock. Following the de-assertion of RX_DV at the end of a frame, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition for an interval that shall not exceed twice the nominal clock period.

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NOTE—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and TX_CLK signals. See additional information in 22.2.4.1.5.

22.2.2.3 TX_EN (transmit enable)

TX_EN indicates that the Reconciliation sublayer is presenting nibbles on the MII for transmission. It shall be asserted by the Reconciliation sublayer synchronously with the first nibble of the preamble and shall remain asserted while all nibbles to be transmitted are presented to the MII. TX_EN shall be negated prior to the first TX_CLK following the final nibble of a frame. TX_EN is driven by the Reconciliation sublayer and shall transition synchronously with respect to the TX_CLK.

Figure 22–4 depicts TX_EN behavior during a frame transmission with no collisions.

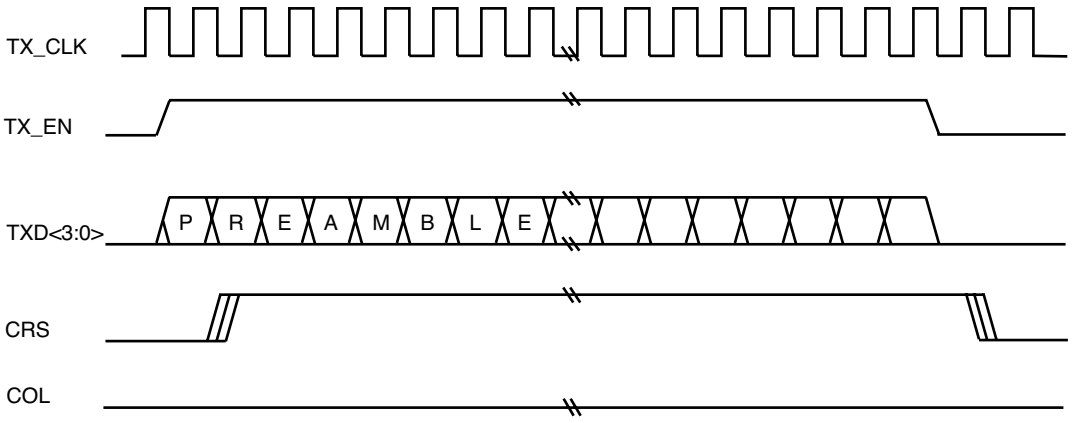


Figure 22–4—Transmission with no collision

22.2.2.4 TXD (transmit data)

TXD is a bundle of 4 data signals (TXD<3:0>) that are driven by the Reconciliation sublayer. TXD<3:0> shall transition synchronously with respect to the TX_CLK. For each TX_CLK period in which TX_EN is asserted, TXD<3:0> are accepted for transmission by the PHY. TXD<0 >is the least significant bit. While TX_EN is de-asserted, TXD<3:0> shall have no effect upon the PHY.

Figure 22–4 depicts TXD<3:0> behavior during the transmission of a frame.

Table 22–1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

Table 22–1—Permissible encodings of TXD<3:0>, TX_EN, and TX_ER

TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

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22.2.2.5 TX_ER (transmit coding error)

TX_ER shall transition synchronously with respect to the TX_CLK. When TX_ER is asserted for one or more TX_CLK periods while TX_EN is also asserted, the PHY shall emit one or more symbols that are not part of the valid data or delimiter set somewhere in the frame being transmitted. The relative position of the error within the frame need not be preserved.

Assertion of the TX_ER signal shall not affect the transmission of data when a PHY is operating at 10 Mb/s, or when TX_EN is de-asserted.

Figure 22–5 shows the behavior of TX_ER during the transmission of a frame propagating an error.

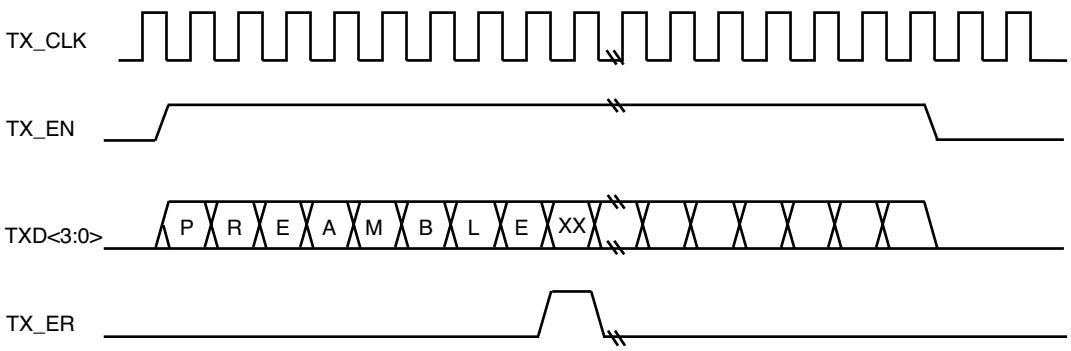


Figure 22–5—Propagating an error

Table 22–1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

The TX_ER signal shall be implemented at the MII of a PHY, may be implemented at the MII of a repeater that provides an MII port, and may be implemented in MAC sublayer devices. If a Reconciliation sublayer or a repeater with an MII port does not actively drive the TX_ER signal, it shall ensure that the TX_ER signal is pulled down to an inactive state at all times.

22.2.2.6 RX_DV (Receive Data Valid)

RX_DV (Receive Data Valid) is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on the RXD<3:0> bundle and that the data on RXD<3:0> is synchronous to RX_CLK. RX_DV shall transition synchronously with respect to the RX_CLK. RX_DV shall remain asserted continuously from the first recovered nibble of the frame through the final recovered nibble and shall be negated prior to the first RX_CLK that follows the final nibble. In order for a received frame to be correctly interpreted by the Reconciliation sublayer and the MAC sublayer, RX_DV must encompass the frame, starting no later than the Start Frame Delimiter (SFD) and excluding any End-of-Frame delimiter.

Figure 22–6 shows the behavior of RX_DV during frame reception.

22.2.2.7 RXD (receive data)

RXD is a bundle of four data signals (RXD<3:0>) that transition synchronously with respect to the RX_CLK. RXD<3:0> are driven by the PHY. For each RX_CLK period in which RX_DV is asserted, RXD<3:0> transfer four bits of recovered data from the PHY to the Reconciliation sublayer. RXD<0> is the

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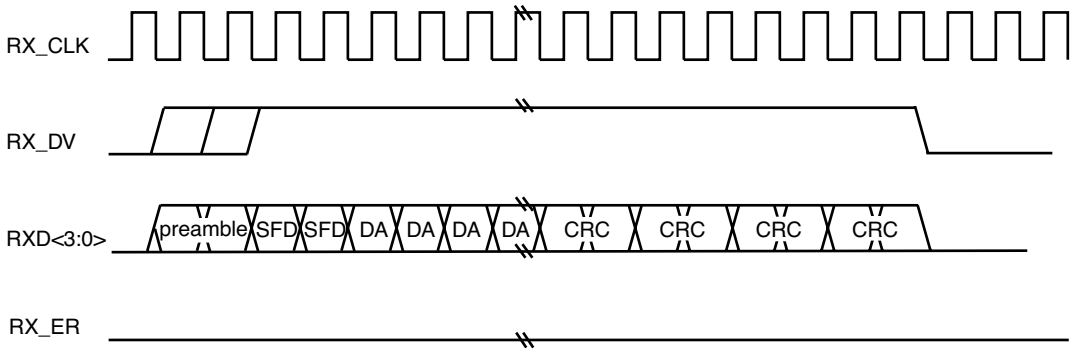


Figure 22–6—Reception with no errors

least significant bit. While RX_DV is de-asserted, RXD<3:0> shall have no effect on the Reconciliation sublayer.

While RX_DV is de-asserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal while driving the value <1110> onto RXD<3:0>. See 22.2.4.4.2 for a description of the conditions under which a PHY will provide a False Carrier indication.

In order for a frame to be correctly interpreted by the MAC sublayer, a completely formed SFD must be passed across the MII. In a DTE operating in half duplex mode, a PHY is not required to loop data transmitted on TXD<3:0> back to RXD<3:0> unless the loopback mode of operation is selected as defined in 22.2.4.1.2. In a DTE operating in full duplex mode, data transmitted on TXD <3:0> must not be looped back to RXD <3:0> unless the loopback mode of operation is selected.

Figure 22–6 shows the behavior of RXD<3:0> during frame reception.

Table 22–2 summarizes the permissible encoding of RXD<3:0>, RX_ER, and RX_DV, along with the specific indication provided by each code.

Table 22–2—Permissible encoding of RXD<3:0>, RX_ER, and RX_DV

RX_DV	RX_ER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001 through 1101	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

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22.2.2.8 RX_ER (receive error)

RX_ER (Receive Error) is driven by the PHY. RX_ER shall be asserted for one or more RX_CLK periods to indicate to the Reconciliation sublayer that an error (e.g., a coding error, or any error that the PHY is capable of detecting, and that may otherwise be undetectable at the MAC sublayer) was detected somewhere in the frame presently being transferred from the PHY to the Reconciliation sublayer. RX_ER shall transition synchronously with respect to RX_CLK. While RX_DV is de-asserted, RX_ER shall have no effect on the Reconciliation sublayer.

While RX_DV is de-asserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal for at least one cycle of the RX_CLK while driving the appropriate value onto RXD<3:0>, as defined in 22.2.2.7. See 24.2.4.4.2 for a description of the conditions under which a PHY will provide a False Carrier indication.

The effect of RX_ER on the Reconciliation sublayer is defined in 22.2.1.5, Response to RX_ER indication from MII.

Figure 22–7 shows the behavior of RX_ER during the reception of a frame with errors.

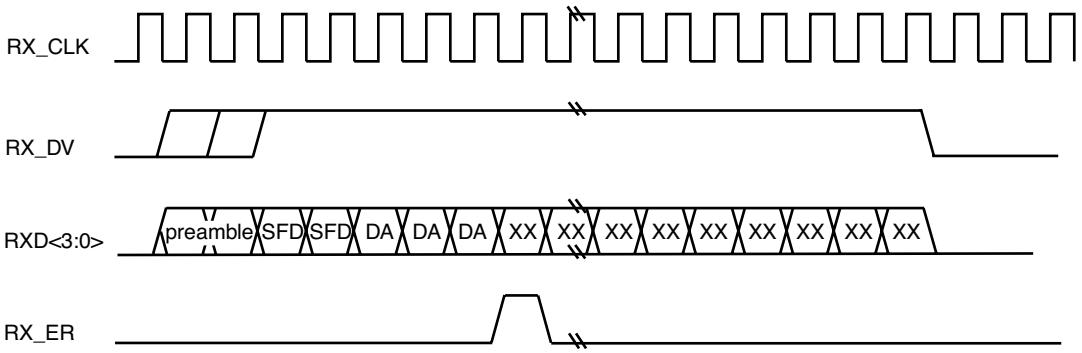


Figure 22–7—Reception with errors

Figure 22–8 shows the behavior of RX_ER, RX_DV and RXD<3:0> during a False Carrier indication.

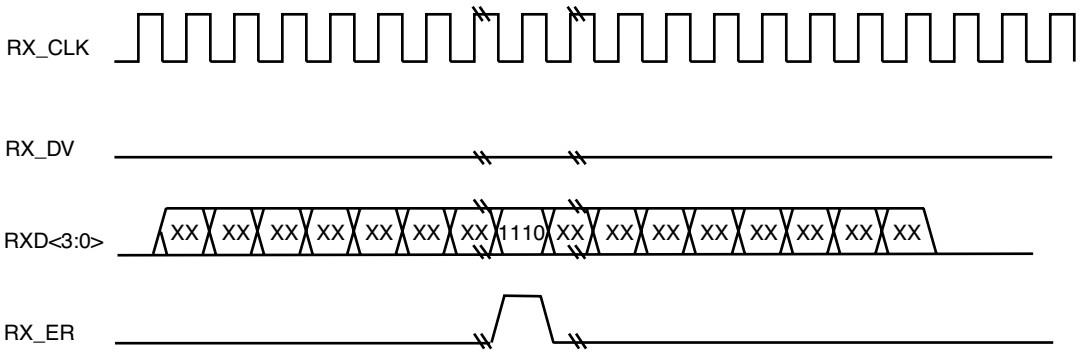


Figure 22–8—False Carrier indication

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22.2.2.9 CRS (carrier sense)

CRS shall be asserted by the PHY when either the transmit or receive medium is nonidle. CRS shall be de-asserted by the PHY when both the transmit and receive media are idle. The PHY shall ensure that CRS remains asserted throughout the duration of a collision condition.

CRS is not required to transition synchronously with respect to either the TX_CLK or the RX_CLK.

The behavior of the CRS signal is unspecified when the duplex mode bit 0.8 in the control register is set to a logic one, as described in 22.2.4.1.8, or when the Auto-Negotiation process selects a full duplex mode of operation.

Figure 22–4 shows the behavior of CRS during a frame transmission without a collision, while Figure 22–9 shows the behavior of CRS during a frame transmission with a collision.

22.2.2.10 COL (collision detected)

COL shall be asserted by the PHY upon detection of a collision on the medium, and shall remain asserted while the collision condition persists.

COL shall be asserted by a PHY that is operating at 10 Mb/s in response to a *signal_quality_error* message from the PMA.

COL is not required to transition synchronously with respect to either the TX_CLK or the RX_CLK.

The behavior of the COL signal is unspecified when the duplex mode bit 0.8 in the control register is set to a logic one, as described in 22.2.4.1.8, or when the Auto-Negotiation process selects a full duplex mode of operation.

Figure 22–9 shows the behavior of COL during a frame transmission with a collision.

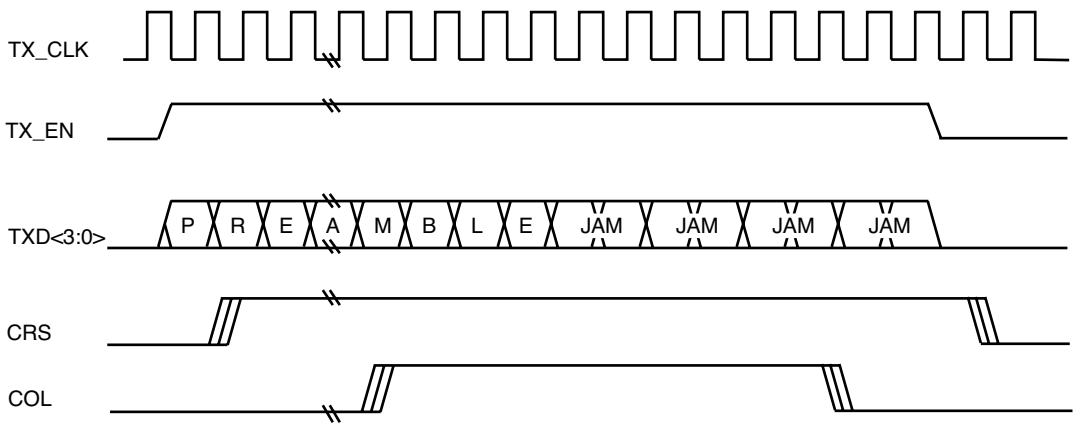


Figure 22–9—Transmission with collision

NOTE—The circuit assembly that contains the Reconciliation sublayer may incorporate a weak pull-up on the COL signal as a means of detecting an open circuit condition on the COL signal at the MII. The limit on the value of this pull-up is defined in 22.4.4.2.

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22.2.2.11 MDC (management data clock)

MDC is sourced by the Station Management entity to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal that has no maximum high or low times. The minimum high and low times for MDC shall be 160 ns each, and the minimum period for MDC shall be 400 ns, regardless of the nominal period of TX_CLK and RX_CLK.

22.2.2.12 MDIO (management data input/output)

MDIO is a bidirectional signal between the PHY and the STA. It is used to transfer control information and status between the PHY and the STA. Control information is driven by the STA synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the STA.

MDIO shall be driven through three-state circuits that enable either the STA or the PHY to drive the signal. A PHY that is attached to the MII via the mechanical interface specified in 22.6 shall provide a resistive pull-up to maintain the signal in a high state. The STA shall incorporate a resistive pull-down on the MDIO signal and thus may use the quiescent state of MDIO to determine if a PHY is connected to the MII via the mechanical interface defined in 22.6. The limits on the values of these pull-ups and pull-downs are defined in 22.4.4.2.

22.2.3 Frame structure

Data frames transmitted through the MII shall have the frame format shown in Figure 22–10.

<inter-frame><preamble><sfd><data><efd>

Figure 22–10—MII frame format

For the MII, transmission and reception of each octet of data shall be done a nibble at a time with the order of nibble transmission and reception as shown in Figure 22–11.

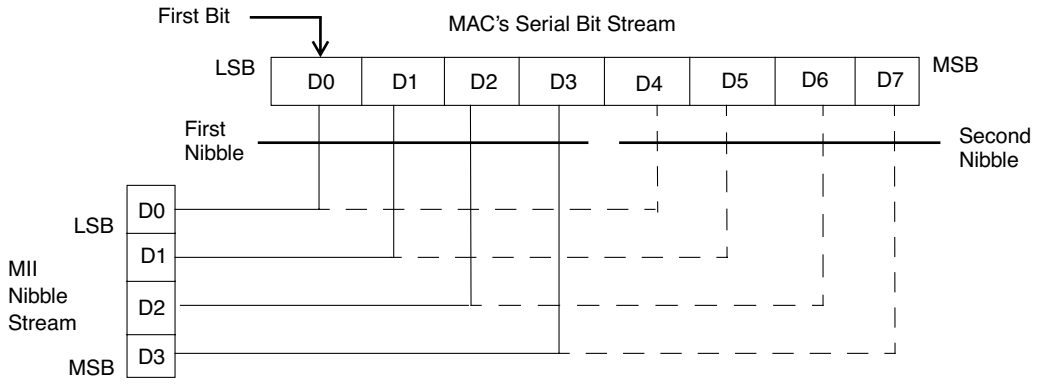


Figure 22–11—Octet/nibble transmit and receive order

The bits of each octet are transmitted and received as two nibbles, bits 0 through 3 of the octet corresponding to bits 0 through 3 of the first nibble transmitted or received, and bits 4 through 7 of the octet corresponding to bits 0 through 3 of the second nibble transmitted or received.

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22.2.3.1 Inter-frame

The inter-frame period provides an observation window for an unspecified amount of time during which no data activity occurs on the MII. The absence of data activity is indicated by the de-assertion of the RX_DV signal on the receive path, and the de-assertion of the TX_EN signal on the transmit path. The MAC inter-FrameSpacing parameter defined in Clause 4 is measured from the de-assertion of the CRS signal to the assertion of the CRS signal.

22.2.3.2 Preamble and start of frame delimiter

22.2.3.2.1 Transmit case

The preamble <preamble> begins a frame transmission. The bit value of the preamble field at the MII is unchanged from that specified in 7.2.3.2 and shall consist of 7 octets with the following bit values:

10101010 10101010 10101010 10101010 10101010 10101010 10101010

In the preceding example, the preamble is displayed using the bit order it would have if transmitted serially. This means that for each octet the leftmost l value represents the LSB of the octet, and the rightmost 0 value the octet MSB.

The SFD (Start Frame Delimiter) <sfd> indicates the start of a frame and follows the preamble. The bit value of the SFD at the MII is unchanged from that specified in 7.2.3.3 and is the bit sequence:

10101011

The preamble and SFD shall be transmitted through the MII as nibbles starting from the assertion of TX_EN as shown in Table 22–3.

Table 22–3—Transmitted preamble and SFD

Signal	Bit values of nibbles transmitted through MII																		
TXD0	X	1[a]	1	1	1	1	1	1	1	1	1	1	1	1	1	1[b]	1	D0[c]	D4[d]
TXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
TXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
TXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
TX_EN	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

[a]1st preamble nibble transmitted.
[b]1st SFD nibble transmitted.
[c]1st data nibble transmitted.
[d]D0 through D7 are the first eight bits of the data field from the Protocol Data Unit (PDU).

22.2.3.2.2 Receive case

The conditions for assertion of RX_DV are defined in 22.2.2.6.

The alignment of the received SFD and data at the MII shall be as shown in Table 22–4 and Table 22–5. Table 22–4 depicts the case where no preamble nibbles are conveyed across the MII, and Table 22–5 depicts the case where the entire preamble is conveyed across the MII.

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Table 22–4—Start of receive with no preamble preceding SFD

Signal	Bit values of nibbles received through MII										
RXD0	X	X	X	X	X	X	X	1[a]	1	D0[b]	D4[c]
RXD1	X	X	X	X	X	X	X	0	0	D1	D5
RXD2	X	X	X	X	X	X	X	1	1	D2	D6
RXD3	X	X	X	X	X	X	X	0	1	D3	D7
RX_DV	0	0	0	0	0	0	0	1	1	1	1

[a]1st SFD nibble received.
[b]1st data nibble received.
[c]D0 through D7 are the first eight bits of the data field from the PDU.

Table 22–5—Start of receive with entire preamble preceding SFD

Signal	Bit values of nibbles received through MII																		
RXD0	X	1[a]	1	1	1	1	1	1	1	1	1	1	1	1	1	1[b]	1	D0[c]	D4[d]
RXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
RXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
RXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
RX_DV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

[a]1st preamble nibble received.
[b]1st SFD nibble received.
[c]1st data nibble received.
[d]D0 through D7 are the first eight bits of the data field from the PDU.

22.2.3.3 Data

The data in a well formed frame shall consist of N octets of data transmitted as 2N nibbles. For each octet of data the transmit order of each nibble is as specified in Figure 22–11. Data in a collision fragment may consist of an odd number of nibbles.

22.2.3.4 End-of-Frame delimiter (EFD)

De-assertion of the TX_EN signal constitutes an End-of-Frame delimiter for data conveyed on TXD<3:0>, and de-assertion of RX_DV constitutes an End-of-Frame delimiter for data conveyed on RXD<3:0>.

22.2.3.5 Handling of excess nibbles

An excess nibble condition occurs when an odd number of nibbles is conveyed across the MII beginning with the SFD and including all nibbles conveyed until the End-of-Frame delimiter. Reception of a frame containing a non-integer number of octets shall be indicated by the PHY as an excess nibble condition.

Transmission of an excess nibble may be handled by the PHY in an implementation-specific manner. No assumption should be made with regard to truncation, octet padding, or exact nibble transmission by the PHY.

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22.2.4 Management functions

The management interface specified here provides a simple, two-wire, serial interface to connect a management entity and a managed PHY for the purposes of controlling the PHY and gathering status from the PHY. This interface is referred to as the MII Management Interface.

The management interface consists of a pair of signals that physically transport the management information across the MII or GMII, a frame format and a protocol specification for exchanging management frames, and a register set that can be read and written using these frames. The register definition specifies a basic register set with an extension mechanism. The MII uses two basic registers. The GMII also uses the same two basic registers and adds a third basic register.

The MII basic register set consists of two registers referred to as the Control register (Register 0) and the Status register (Register 1). All PHYs that provide an MII shall incorporate the basic register set. All PHYs that provide a GMII shall incorporate an extended basic register set consisting of the Control register (Register 0), Status register (Register 1), and Extended Status register (Register 15). The status and control functions defined here are considered basic and fundamental to 100 Mb/s and 1000 Mb/s PHYs. Registers 2 through 10 are part of the extended register set. The format of Registers 4 through 10 are defined for the specific Auto-Negotiation protocol used (Clause 28 or Clause 37). The format of these registers is selected by the bit settings of Registers 1 and 15.

The full set of management registers is listed in Table 22–6.

Table 22–6—MII management register set

Register address	Register name	Basic/Extended	
		MII	GMII
0	Control	B	B
1	Status	B	B
2,3	PHY Identifier	E	E
4	Auto-Negotiation Advertisement	E	E
5	Auto-Negotiation Link Partner Base Page Ability	E	E
6	Auto-Negotiation Expansion	E	E
7	Auto-Negotiation Next Page Transmit	E	E
8	Auto-Negotiation Link Partner Received Next Page	E	E
9	MASTER-SLAVE Control Register	E	E
10	MASTER-SLAVE Status Register	E	E
11 through 14	Reserved	E	E
15	Extended Status	Reserved	B
16 through 31	Vendor Specific	E	E

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22.2.4.1 Control register (Register 0)

The assignment of bits in the Control Register is shown in Table 22–7 below. The default value for each bit of the Control Register should be chosen so that the initial state of the PHY upon power up or reset is a normal operational state without management intervention.

Table 22–7—Control register bit definitions

Bit(s)	Name	Description	R/W[a]
0.15	Reset	1 = PHY reset 0 = normal operation	R/W SC
0.14	Loopback	1 = enable loopback mode 0 = disable loopback mode	R/W
0.13	Speed Selection (LSB)	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W
0.12	Auto-Negotiation Enable	1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process	R/W
0.11	Power Down	1 = power down 0 = normal operation[b]	R/W
0.10	Isolate	1 = electrically Isolate PHY from MII or GMII 0 = normal operation[b]	R/W
0.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation Process 0 = normal operation	R/W SC
0.8	Duplex Mode	1 = Full Duplex 0 = Half Duplex	R/W
0.7	Collision Test	1 = enable COL signal test 0 = disable COL signal test	R/W
0.6	Speed Selection (MSB)	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W
0.5:0	Reserved	Write as 0, ignore on Read	R/W

[a]R/W = Read/Write, SC = Self-Clearing.
[b]For normal operation, both 0.10 and 0.11 must be cleared to zero; see 22.2.4.1.5.

22.2.4.1.1 Reset

Resetting a PHY is accomplished by setting bit 0.15 to a logic one. This action shall set the status and control registers to their default states. As a consequence this action may change the internal state of the PHY and the state of the physical link associated with the PHY. This bit is self-clearing, and a PHY shall return a value of one in bit 0.15 until the reset process is completed. A PHY is not required to accept a write transaction to the control register until the reset process is completed, and writes to bits of the control register other than 0.15 may have no effect until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 0.15.

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The default value of bit 0.15 is zero.

NOTE—This operation may interrupt data communication.

22.2.4.1.2 Loopback

The PHY shall be placed in a loopback mode of operation when bit 0.14 is set to a logic one. When bit 0.14 is set, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII or GMII shall not result in the transmission of data on the network medium. When bit 0.14 is set, the PHY shall accept data from the MII or GMII transmit data path and return it to the MII or GMII receive data path in response to the assertion of TX_EN. When bit 0.14 is set, the delay from the assertion of TX_EN to the assertion of RX_DV shall be less than 512 BT. When bit 0.14 is set, the COL signal shall remain de-asserted at all times, unless bit 0.7 is set, in which case the COL signal shall behave as described in 22.2.4.1.9. Clearing bit 0.14 to zero allows normal operation.

The default value of bit 0.14 is zero.

NOTE—The signal path through the PHY that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PHY circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths through a PHY may be enabled via the extended register set, in an implementation-specific fashion.

22.2.4.1.3 Speed selection

Link speed can be selected via either the Auto-Negotiation process, or manual speed selection. Manual speed selection is allowed when Auto-Negotiation is disabled by clearing bit 0.12 to zero. When Auto-Negotiation is disabled and bit 0.6 is cleared to a logic zero, setting bit 0.13 to a logic one configures the PHY for 100 Mb/s operation, and clearing bit 0.13 to a logic zero configures the PHY for 10 Mb/s operation. When Auto-Negotiation is disabled and bit 0.6 is set to a logic one, clearing bit 0.13 to a logic zero selects 1000 Mb/s operation. The combination of both bits 0.6 and 0.13 set to a logic one is reserved for future standardization. When Auto-Negotiation is enabled, bits 0.6 and 0.13 can be read or written, but the state of bits 0.6 and 0.13 have no effect on the link configuration, and it is not necessary for bits 0.6 and 0.13 to reflect the operating speed of the link when it is read. If a PHY reports via bits 1.15:9 and bits 15.15:12 that it is not able to operate at all speeds, the value of bits 0.6 and 0.13 shall correspond to a speed at which the PHY can operate, and any attempt to change the bits to an invalid setting shall be ignored.

The default value of bits 0.6 and 0.13 are the encoding of the highest data rate at which the PHY can operate as indicated by bits 1.15:9 and 15.15:12.

22.2.4.1.4 Auto-Negotiation enable

The Auto-Negotiation process shall be enabled by setting bit 0.12 to a logic one. If bit 0.12 is set to a logic one, then bits 0.13, 0.8, and 0.6 shall have no effect on the link configuration, and station operation other than that specified by the Auto-Negotiation protocol. If bit 0.12 is cleared to a logic zero, then bits 0.13, 0.8, and 0.6 will determine the link configuration, regardless of the prior state of the link configuration and the Auto-Negotiation process.

If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, the PHY shall return a value of zero in bit 0.12. If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, bit 0.12 should always be written as zero, and any attempt to write a one to bit 0.12 shall be ignored.

The default value of bit 0.12 is one, unless the PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, in which case the default value of bit 0.12 is zero.

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22.2.4.1.5 Power down

The PHY may be placed in a low-power consumption state by setting bit 0.11 to a logic one. Clearing bit 0.11 to zero allows normal operation. The specific behavior of a PHY in the power-down state is implementation specific. While in the power-down state, the PHY shall respond to management transactions. During the transition to the power-down state and while in the power-down state, the PHY shall not generate spurious signals on the MII or GMII.

A PHY is not required to meet the RX_CLK and TX_CLK signal functional requirements when either bit 0.11 or bit 0.10 is set to a logic one. A PHY shall meet the RX_CLK and TX_CLK signal functional requirements defined in 22.2.2 within 0.5 s after both bit 0.11 and 0.10 are cleared to zero.

The default value of bit 0.11 is zero.

22.2.4.1.6 Isolate

The PHY may be forced to electrically isolate its data paths from the MII or GMII by setting bit 0.10 to a logic one. Clearing bit 0.10 allows normal operation. When the PHY is isolated from the MII or GMII it shall not respond to the TXD data bundle, TX_EN, TX_ER and GTX_CLK inputs, and it shall present a high impedance on its TX_CLK, RX_CLK, RX_DV, RX_ER, RXD data bundle, COL, and CRS outputs. When the PHY is isolated from the MII or GMII it shall respond to management transactions.

A PHY that is connected to the MII via the mechanical interface defined in 22.6 shall have a default value of one for bit 0.10 so as to avoid the possibility of having multiple MII output drivers actively driving the same signal path simultaneously.

NOTE—This clause neither requires nor assumes any specific behavior at the MDI resulting from setting bit 0.10 to a logic one.

22.2.4.1.7 Restart Auto-Negotiation

If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, the PHY shall return a value of zero in bit 0.9. If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, bit 0.9 should always be written as zero, and any attempt to write a one to bit 0.9 shall be ignored.

Otherwise, the Auto-Negotiation process shall be restarted by setting bit 0.9 to a logic one. This bit is self-clearing, and a PHY shall return a value of one in bit 0.9 until the Auto-Negotiation process has been initiated. The Auto-Negotiation process shall not be affected by writing a zero to bit 0.9.

The default value of bit 0.9 is zero.

22.2.4.1.8 Duplex mode

The duplex mode can be selected via either the Auto-Negotiation process, or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by clearing bit 0.12 to zero. When Auto-Negotiation is disabled, setting bit 0.8 to a logic one configures the PHY for full duplex operation, and clearing bit 0.8 to a logic zero configures the PHY for half duplex operation. When Auto-Negotiation is enabled, bit 0.8 can be read or written, but the state of bit 0.8 has no effect on the link configuration. If a PHY reports via bits 1.15:9 and 15.15:12 that it is able to operate in only one duplex mode, the value of bit 0.8 shall correspond to the mode in which the PHY can operate, and any attempt to change the setting of bit 0.8 shall be ignored.

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When a PHY is placed in the loopback mode of operation via bit 0.14, the behavior of the PHY shall not be affected by the state of bit 0.8.

The default value of bit 0.8 is zero, unless a PHY reports via bits 1.15:9 and 15.15:12 that it is able to operate only in full duplex mode, in which case the default value of bit 0.8 is one.

22.2.4.1.9 Collision test

The COL signal at the MII or GMII may be tested by setting bit 0.7 to a logic one. When bit 0.7 is set to one, the PHY shall assert the COL signal within 512 BT in response to the assertion of TX_EN. While bit 0.7 is set to one, the PHY shall de-assert the COL signal within 4 BT when connected to an MII, or 16 BT when connected to a GMII, in response to the de-assertion of TX_EN. Clearing bit 0.7 to zero allows normal operation.

The default value of bit 0.7 is zero.

NOTE—It is recommended that the Collision Test function be used only in conjunction with the loopback mode of operation defined in 22.2.4.1.2.

22.2.4.1.10 Speed selection

Bit 0.6 is used in conjunction with bits 0.13 and 0.12 to select the speed of operation as described in 22.2.4.1.3.

22.2.4.1.11 Reserved bits

Bits 0.5:0 are reserved for future standardization. They shall be written as zero and shall be ignored when read; however, a PHY shall return the value zero in these bits.

22.2.4.2 Status register (Register 1)

The assignment of bits in the Status register is shown in Table 22–8. All of the bits in the Status register are read only, a write to the Status register shall have no effect.

22.2.4.2.1 100BASE-T4 ability

When read as a logic one, bit 1.15 indicates that the PHY has the ability to perform link transmission and reception using the 100BASE-T4 signaling specification. When read as a logic zero, bit 1.15 indicates that the PHY lacks the ability to perform link transmission and reception using the 100BASE-T4 signaling specification.

22.2.4.2.2 100BASE-X full duplex ability

When read as a logic one, bit 1.14 indicates that the PHY has the ability to perform full duplex link transmission and reception using the 100BASE-X signaling specification. When read as a logic zero, bit 1.14 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 100BASE-X signaling specification.

22.2.4.2.3 100BASE-X half duplex ability

When read as a logic one, bit 1.13 indicates that the PHY has the ability to perform half duplex link transmission and reception using the 100BASE-X signaling specification. When read as a logic zero, bit 1.13 indicates that the PHY lacks the ability to perform half duplex link transmission and reception using the 100BASE-X signaling specification.

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Table 22–8—Status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.15	100BASE-T4	1 = PHY able to perform 100BASE-T4 0 = PHY not able to perform 100BASE-T4	RO
1.14	100BASE-X Full Duplex	1 = PHY able to perform full duplex 100BASE-X 0 = PHY not able to perform full duplex 100BASE-X	RO
1.13	100BASE-X Half Duplex	1 = PHY able to perform half duplex 100BASE-X 0 = PHY not able to perform half duplex 100BASE-X	RO
1.12	10 Mb/s Full Duplex	1 = PHY able to operate at 10 Mb/s in full duplex mode 0 = PHY not able to operate at 10 Mb/s in full duplex mode	RO
1.11	10 Mb/s Half Duplex	1 = PHY able to operate at 10 Mb/s in half duplex mode 0 = PHY not able to operate at 10 Mb/s in half duplex mode	RO
1.10	100BASE-T2 Full Duplex	1 = PHY able to perform full duplex 100BASE-T2 0 = PHY not able to perform full duplex 100BASE-T2	RO
1.9	100BASE-T2 Half Duplex	1 = PHY able to perform half duplex 100BASE-T2 0 = PHY not able to perform half duplex 100BASE-T2	RO
1.8	Extended Status	1 = Extended status information in Register 15 0 = No extended status information in Register 15	RO
1.7	Reserved	ignore when read	RO
1.6	MF Preamble Suppression	1 = PHY will accept management frames with preamble suppressed. 0 = PHY will not accept management frames with preamble suppressed.	RO
1.5	Auto-Negotiation Complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO
1.4	Remote Fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO/ LH
1.3	Auto-Negotiation Ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO
1.2	Link Status	1 = link is up 0 = link is down	RO/ LL
1.1	Jabber Detect	1 = jabber condition detected 0 = no jabber condition detected	RO/ LH
1.0	Extended Capability	1 = extended register capabilities 0 = basic register set capabilities only	RO

[a]RO = Read Only, LL = Latching Low, LH = Latching High

22.2.4.2.4 10 Mb/s full duplex ability

When read as a logic one, bit 1.12 indicates that the PHY has the ability to perform full duplex link transmission and reception while operating at 10 Mb/s. When read as a logic zero, bit 1.12 indicates that the PHY lacks the ability to perform full duplex link transmission and reception while operating at 10 Mb/s.

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22.2.4.2.5 10 Mb/s half duplex ability

When read as a logic one, bit 1.11 indicates that the PHY has the ability to perform half duplex link transmission and reception while operating at 10 Mb/s. When read as a logic zero, bit 1.11 indicates that the PHY lacks the ability to perform half duplex link transmission and reception while operating at 10 Mb/s.

22.2.4.2.6 100BASE-T2 full duplex ability

When read as a logic one, bit 1.10 indicates that the PHY has the ability to perform full duplex link transmission and reception using the 100BASE-T2 signaling specification. When read as a logic zero, bit 1.10 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 100BASE-T2 signaling specification.

22.2.4.2.7 100BASE-T2 half duplex ability

When read as a logic one, bit 1.9 indicates that the PHY has the ability to perform half duplex link transmission and reception using the 100BASE-T2 signaling specification. When read as a logic zero, bit 1.9 indicates that the PHY lacks the ability to perform half duplex link transmission and reception using the 100BASE-T2 signaling specification.

22.2.4.2.8 Reserved bits

Bit 1:7 is reserved for future standardization, shall be written as zero, and shall be ignored when read; however, a PHY shall return the value zero in this bit.

22.2.4.2.9 MF preamble suppression ability

When read as a logic one, bit 1.6 indicates that the PHY is able to accept management frames regardless of whether they are or are not preceded by the preamble pattern described in 22.2.4.5.2. When read as a logic zero, bit 1.6 indicates that the PHY is not able to accept management frames unless they are preceded by the preamble pattern described in 22.2.4.5.2.

22.2.4.2.10 Auto-Negotiation complete

When read as a logic one, bit 1.5 indicates that the Auto-Negotiation process has been completed, and that the contents of the extended registers implemented by the Auto-Negotiation protocol (either Clause 28 or Clause 37) are valid. When read as a logic zero, bit 1.5 indicates that the Auto-Negotiation process has not been completed, and that the contents of the extended registers are as defined by the current state of the Auto-Negotiation protocol, or as written for manual configuration. A PHY shall return a value of zero in bit 1.5 if Auto-Negotiation is disabled by clearing bit 0.12. A PHY shall also return a value of zero in bit 1.5 if it lacks the ability to perform Auto-Negotiation.

22.2.4.2.11 Remote fault

When read as a logic one, bit 1.4 indicates that a remote fault condition has been detected. The type of fault as well as the criteria and method of fault detection is PHY specific. The Remote Fault bit shall be implemented with a latching function, such that the occurrence of a remote fault will cause the Remote Fault bit to become set and remain set until it is cleared. The Remote Fault bit shall be cleared each time Register 1 is read via the management interface, and shall also be cleared by a PHY reset.

If a PHY has no provision for remote fault detection, it shall maintain bit 1.4 in a cleared state. Further information regarding the remote fault indication can be found in 37.2.1.5, 22.2.1.2, and in 24.3.2.1.

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22.2.4.2.12 Auto-Negotiation ability

When read as a logic one, bit 1.3 indicates that the PHY has the ability to perform Auto-Negotiation. When read as a logic zero, bit 1.3 indicates that the PHY lacks the ability to perform Auto-Negotiation.

22.2.4.2.13 Link Status

When read as a logic one, bit 1.2 indicates that the PHY has determined that a valid link has been established. When read as a logic zero, bit 1.2 indicates that the link is not valid. The criteria for determining link validity is PHY specific. The Link Status bit shall be implemented with a latching function, such that the occurrence of a link failure condition will cause the Link Status bit to become cleared and remain cleared until it is read via the management interface. This status indication is intended to support the management attribute defined in 30.5.1.1.4, aMediaAvailable.

22.2.4.2.14 Jabber detect

When read as a logic one, bit 1.1 indicates that a jabber condition has been detected. This status indication is intended to support the management attribute defined in 30.5.1.1.6, aJabber, and the MAU notification defined in 30.5.1.3.1, nJabber. The criteria for the detection of a jabber condition is PHY specific. The Jabber Detect bit shall be implemented with a latching function, such that the occurrence of a jabber condition will cause the Jabber Detect bit to become set and remain set until it is cleared. The Jabber Detect bit shall be cleared each time Register 1 is read via the management interface, and shall also be cleared by a PHY reset.

PHYs specified for 100 Mb/s operation or above do not incorporate a Jabber Detect function, as this function is defined to be performed in the repeater unit at these speeds. Therefore, PHYs specified for 100 Mb/s operation and above shall always return a value of zero in bit 1.1.

22.2.4.2.15 Extended capability

When read as a logic one, bit 1.0 indicates that the PHY provides an extended set of capabilities which may be accessed through the extended register set. When read as a logic zero, bit 1.0 indicates that the PHY provides only the basic register set.

22.2.4.2.16 Extended status

When read as a logic one, bit 1.8 indicates that the base register status information is extended into Register 15. All PHYs supporting 1000 Mb/s operation shall have this bit set to a logic one. When read as a logic zero, bit 1.8 indicates that the extended status is not implemented and that the PHY lacks the ability to perform transmission and reception at 1000 Mb/s.

22.2.4.3 Extended capability registers

In addition to the basic register set defined in 22.2.4.1 and 22.2.4.2, PHYs may provide an extended set of capabilities that may be accessed and controlled via the MII management interface. Nine registers have been defined within the extended address space for the purpose of providing a PHY-specific identifier to layer management, and to provide control and monitoring for the Auto-Negotiation process.

If an attempt is made to perform a read transaction to a register in the extended register set, and the PHY being read does not implement the addressed register, the PHY shall not drive the MDIO line in response to the read transaction. If an attempt is made to perform a write transaction to a register in the extended register set, and the PHY being written does not implement the addressed register, the write transaction shall be ignored by the PHY.

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22.2.4.3.1 PHY Identifier (Registers 2 and 3)

Registers 2 and 3 provide a 32-bit value, which shall constitute a unique identifier for a particular type of PHY. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier.

Bit 2.15 shall be the MSB of the PHY Identifier, and bit 3.0 shall be the LSB of the PHY Identifier.

The PHY Identifier shall be composed of the third through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the PHY manufacturer by the IEEE,[1] plus a six-bit manufacturer's model number, plus a four-bit manufacturer's revision number. The PHY Identifier is intended to provide sufficient information to support the oResourceTypeID object as required in 30.1.2.

The third bit of the OUI is assigned to bit 2.15, the fourth bit of the OUI is assigned to bit 2.14, and so on. Bit 2.0 contains the eighteenth bit of the OUI. Bit 3.15 contains the nineteenth bit of the OUI, and bit 3.10 contains the twenty-fourth bit of the OUI. Bit 3.9 contains the MSB of the manufacturer's model number. Bit 3.4 contains the LSB of the manufacturer's model number. Bit 3.3 contains the MSB of the manufacturer's revision number, and bit 3.0 contains the LSB of the manufacturer's revision number.

Figure 22–12 depicts the mapping of this information to the bits of Registers 2 and 3. Additional detail describing the format of OUIs can be found in IEEE Std 802-1990.

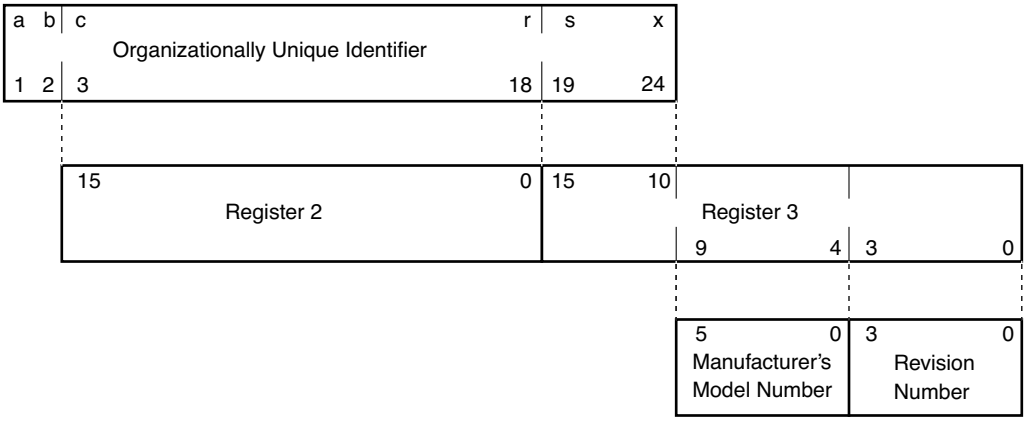


Figure 22–12—Format of PHY Identifier

22.2.4.3.2 Auto-Negotiation advertisement (Register 4)

Register 4 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1 and 37.2.5.1.

22.2.4.3.3 Auto-Negotiation link partner ability (Register 5)

Register 5 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1 and 37.2.5.1.

22.2.4.3.4 Auto-Negotiation expansion (Register 6)

Register 6 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1 and 37.2.5.1.

[1]Interested applicants should contact the IEEE Standards Department, Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA.

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22.2.4.3.5 Auto-Negotiation next page (Register 7)

Register 7 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1 and 37.2.5.1.

22.2.4.3.6 Auto-Negotiation link partner Received Next Page (Register 8)

Register 8 provides 16 bits that are used by the Auto-Negotiation process. See 32.5.1 and 37.2.5.1.

22.2.4.3.7 MASTER-SLAVE control register (Register 9)

Register 9 provides bit values by 100BASE-T2 (as specified in 32.5) and 1000BASE-T (as specified in 40.5).

22.2.4.3.8 MASTER-SLAVE status register (Register 10)

Register 10 provides bit values by 100BASE-T2 (as specified in 32.5) and 1000BASE-T (as specified in 40.5).

22.2.4.3.9 PHY specific registers

A particular PHY may provide additional registers beyond those defined above. Register addresses 16 through 31 (decimal) may be used to provide vendor-specific functions or abilities. The definition of Registers 4 through 14 are dependent on the version (Clause 28 or Clause 37) of Auto-Negotiation protocol used by the PHY.

22.2.4.4 Extended Status register (Register 15)

The Extended Status register is implemented for all PHYs capable of operation at speeds above 100 Mb/s. The assignment of bits in the Extended Status register is shown in Table 22–9 below. All of the bits in the Extended Status register are read only; a write to the Extended Status register shall have no effect.

Table 22–9—Extended status register bit definitions

Bit(s)	Name	Description	R/W[a]
15.15	1000BASE-X Full Duplex	1 = PHY able to perform full duplex 1000BASE-X 0 = PHY not able to perform full duplex 1000BASE-X	RO
15.14	1000BASE-X Half Duplex	1 = PHY able to perform half duplex 1000BASE-X 0 = PHY not able to perform half duplex 1000BASE-X	RO
15.13	1000BASE-T Full Duplex	1 = PHY able to perform full duplex 1000BASE-T 0 = PHY not able to perform full duplex 1000BASE-T	RO
15.12	1000BASE-T Half Duplex	1 = PHY able to perform half duplex 1000BASE-T 0 = PHY not able to perform half duplex 1000BASE-T	RO
15.11:0	Reserved	ignore when read	RO

[a]RO = Read Only

22.2.4.4.1 1000BASE-X full duplex ability

When read as a logic one, bit 15.15 indicates that the PHY has the ability to perform full duplex link transmission and reception using the 1000BASE-X signaling specification. When read as a logic zero, the bit

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15.15 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 1000BASE-X signaling specification.

22.2.4.4.2 1000BASE-X half duplex ability

When read as a logic one, bit 15.14 indicates that the PHY has the ability to perform half duplex link transmission and reception using the 1000BASE-X signaling specification. When read as a logic zero, the bit 15.14 indicates that the PHY lacks the ability to perform half duplex link transmission and reception using the 1000BASE-X signaling specification.

22.2.4.4.3 1000BASE-T full duplex ability

When read as a logic one, bit 15.13 indicates that the PHY has the ability to perform full duplex link transmission and reception using the 1000BASE-T signaling specification. When read as a logic zero, the bit 15.13 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 1000BASE-T signaling specification.

22.2.4.4.4 1000BASE-T half duplex ability

When read as a logic one, bit 15.12 indicates that the PHY has the ability to perform half duplex link transmission and reception using the 1000BASE-T signaling specification. When read as a logic zero, the bit 15.12 indicates that the PHY lacks the ability to perform half duplex link transmission and reception using the 1000BASE-T signaling specification.

22.2.4.4.5 Reserved bits

Bits 15:11:0 are reserved for future standardization. They shall be written as zero and shall be ignored when read; however, a PHY shall return the value zero in these bits.

22.2.4.5 Management frame structure

Frames transmitted on the MII Management Interface shall have the frame structure shown in Table 22–10. The order of bit transmission shall be from left to right.

Table 22–10—Management frame format

	Management frame fields							
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

22.2.4.5.1 IDLE (IDLE condition)

The IDLE condition on MDIO is a high-impedance state. All three state drivers shall be disabled and the PHY's pull-up resistor will pull the MDIO line to a logic one.

22.2.4.5.2 PRE (preamble)

At the beginning of each transaction, the station management entity shall send a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC to provide the PHY with a pattern that it can

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use to establish synchronization. A PHY shall observe a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction.

If the STA determines that every PHY that is connected to the MDIO signal is able to accept management frames that are not preceded by the preamble pattern, then the STA may suppress the generation of the preamble pattern, and may initiate management frames with the ST (Start of Frame) pattern.

22.2.4.5.3 ST (start of frame)

The start of frame is indicated by a <01> pattern. This pattern assures transitions from the default logic one line state to zero and back to one.

22.2.4.5.4 OP (operation code)

The operation code for a read transaction is <10>, while the operation code for a write transaction is <01>.

22.2.4.5.5 PHYAD (PHY Address)

The PHY Address is five bits, allowing 32 unique PHY addresses. The first PHY address bit transmitted and received is the MSB of the address. A PHY that is connected to the station management entity via the mechanical interface defined in 22.6 shall always respond to transactions addressed to PHY Address zero <00000>. A station management entity that is attached to multiple PHYs must have a priori knowledge of the appropriate PHY Address for each PHY.

22.2.4.5.6 REGAD (Register Address)

The Register Address is five bits, allowing 32 individual registers to be addressed within each PHY. The first Register Address bit transmitted and received is the MSB of the address. The register accessed at Register Address zero <00000> shall be the control register defined in 22.2.4.1, and the register accessed at Register Address one <00001> shall be the status register defined in 22.2.4.2.

22.2.4.5.7 TA (turnaround)

The turnaround time is a 2 bit time spacing between the Register Address field and the Data field of a management frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY shall remain in a high-impedance state for the first bit time of the turnaround. The PHY shall drive a zero bit during the second bit time of the turnaround of a read transaction. During a write transaction, the STA shall drive a one bit for the first bit time of the turnaround and a zero bit for the second bit time of the turnaround. Figure 22–13 shows the behavior of the MDIO signal during the turnaround field of a read transaction.

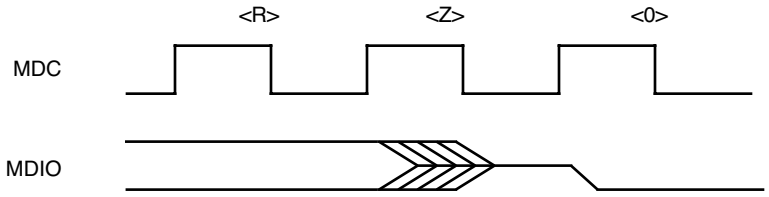


Figure 22–13—Behavior of MDIO during TA field of a read transaction

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22.2.4.5.8 DATA (data)

The data field is 16 bits. The first data bit transmitted and received shall be bit 15 of the register being addressed.

22.3 Signal timing characteristics

All signal timing characteristics shall be measured using the techniques specified in Annex 22C. The signal threshold potentials $V_{ih(min)}$ and $V_{il(max)}$ are defined in 22.4.4.1.

The HIGH time of an MII signal is defined as the length of time that the potential of the signal is greater than or equal to $V_{ih(min)}$. The LOW time of an MII signal is defined as the length of time that the potential of the signal is less than or equal to $V_{il(max)}$.

The setup time of an MII signal relative to an MII clock edge is defined as the length of time between when the signal exits and remains out of the switching region and when the clock enters the switching region. The hold time of an MII signal relative to an MII clock edge is defined as the length of time between when the clock exits the switching region and when the signal enters the switching region.

The propagation delay from an MII clock edge to a valid MII signal is defined as the length of time between when the clock exits the switching region and when the signal exits and remains out of the switching region.

22.3.1 Signals that are synchronous to TX_CLK

Figure 22–14 shows the timing relationship for the signals associated with the transmit data path at the MII connector. The clock to output delay shall be a minimum of 0 ns and a maximum of 25 ns.

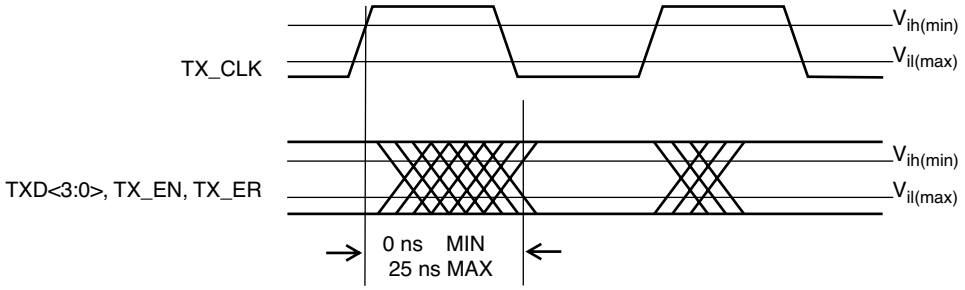


Figure 22–14—Transmit signal timing relationships at the MII

22.3.1.1 TX_EN

TX_EN is transitioned by the Reconciliation sublayer synchronously with respect to the TX_CLK rising edge with the timing as shown in Figure 22–14.

22.3.1.2 TXD<3:0>

TXD<3:0> is transitioned by the Reconciliation sublayer synchronously with respect to the TX_CLK rising edge with the timing as depicted in Figure 22–14.

22.3.1.3 TX_ER

TX_ER is transitioned synchronously with respect to the rising edge of TX_CLK as shown in Figure 22–14.

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22.3.2 Signals that are synchronous to RX_CLK

Figure 22–15 shows the timing relationship for the signals associated with the receive data path at the MII connector. The timing is referenced to the rising edge of the RX_CLK. The input setup time shall be a minimum of 10 ns and the input hold time shall be a minimum of 10 ns.

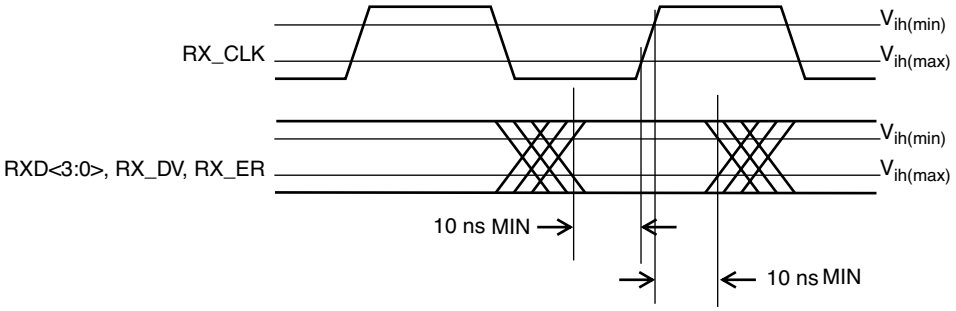


Figure 22–15—Receive signal timing relationships at the MII

22.3.2.1 RX_DV

RX_DV is sampled by the Reconciliation sublayer synchronously with respect to the rising edge of RX_CLK with the timing shown in Figure 22–15.

22.3.2.2 RXD<3:0>

RXD<3:0> is sampled by the Reconciliation sublayer synchronously with respect to the rising edge of RX_CLK as shown in Figure 22–15. The RXD<3:0> timing requirements must be met at all rising edges of RX_CLK.

22.3.2.3 RX_ER

RX_ER is sampled by the Reconciliation sublayer synchronously with respect to the rising edge of RX_CLK as shown in Figure 22–15. The RX_ER timing requirements must be met at all rising edges of RX_CLK.

22.3.3 Signals that have no required clock relationship

22.3.3.1 CRS

CRS is driven by the PHY. Transitions on CRS have no required relationship to either of the clock signals provided at the MII.

22.3.3.2 COL

COL is driven by the PHY. Transitions on COL have no required relationship to either of the clock signals provided at the MII.

22.3.4 MDIO timing relationship to MDC

MDIO (Management Data Input/Output) is a bidirectional signal that can be sourced by the Station Management Entity (STA) or the PHY. When the STA sources the MDIO signal, the STA shall provide a minimum

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of 10 ns of setup time and a minimum of 10 ns of hold time referenced to the rising edge of MDC, as shown in Figure 22–16, measured at the MII connector.

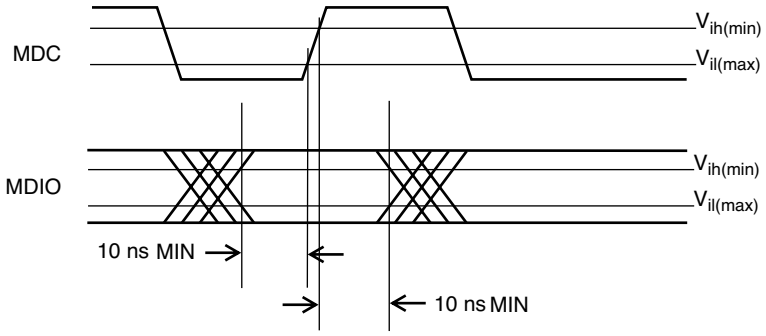


Figure 22–16—MDIO sourced by STA

When the MDIO signal is sourced by the PHY, it is sampled by the STA synchronously with respect to the rising edge of MDC. The clock to output delay from the PHY, as measured at the MII connector, shall be a minimum of 0 ns, and a maximum of 300 ns, as shown in Figure 22–17.

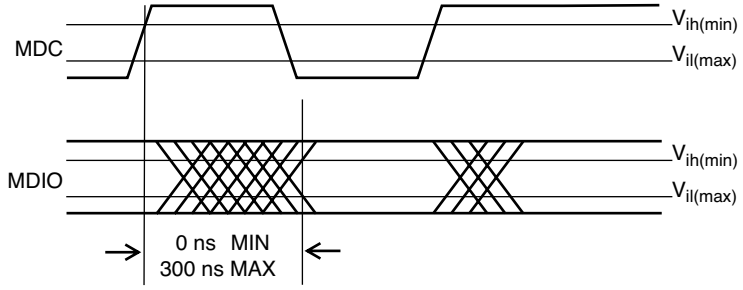


Figure 22–17—MDIO sourced by PHY

22.4 Electrical characteristics

The electrical characteristics of the MII are specified such that the three application environments described in 22.1 are accommodated. The electrical specifications are optimized for the integrated circuit to integrated circuit application environment, but integrated circuit drivers and receivers that are implemented in compliance with the specification will also support the mother board to daughter board and short cable application environments, provided those environments are constrained to the limits specified in this clause.

NOTE—The specifications for the driver and receiver characteristics can be met with TTL compatible input and output buffers implemented in a digital CMOS ASIC process.

22.4.1 Signal levels

The MII uses TTL signal levels, which are compatible with devices operating at a nominal supply voltage of either 5.0 or 3.3 V.

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NOTE—Care should be taken to ensure that all MII receivers can tolerate dc input potentials from 0.00 V to 5.50 V, referenced to the COMMON signal, and transient input potentials as high as 7.3 V, or as low as –1.8 V, referenced to the COMMON signal, which can occur when MII signals change state. The transient duration will not exceed 15 ns. The dc source impedance will be no less than $R_{oh(min)}$. The transient source impedance will be no less than (68 × 0.85 =) 57.8 Ω .

22.4.2 Signal paths

MII signals can be divided into two groups: signals that go between the STA and the PHY, and signals that go between the Reconciliation sublayer and the PHY.

Signals between the STA and the PHY may connect to one or more PHYs. When a signal goes between the STA and a single PHY, the signal's path is a point-to-point transmission path. When a signal goes between the STA and multiple PHYs, the signal's transmission path has drivers and receivers attached in any order along the length of the path and is not considered a point-to-point transmission path.

Signals between the Reconciliation sublayer and the PHY may also connect to one or more PHYs. However, the transmission path of each of these signals shall be either a point-to-point transmission path or a sequence of point-to-point transmission paths connected in series.

All connections to a point-to-point transmission path are at the path ends. The simplest point-to-point transmission path has a driver at one end and a receiver at the other. Point-to-point transmission paths can also have more than one driver and more than one receiver if the drivers and receivers are lumped at the ends of the path, and if the maximum propagation delay between the drivers and receivers at a given end of the path is a very small fraction of the 10%–90% rise/fall time for signals driven onto the path.

The MII shall use unbalanced signal transmission paths. The characteristic impedance Z_o of transmission paths is not specified for electrically short paths where transmission line reflections can be safely ignored.

The characteristic impedance Z_o of electrically long transmission paths or path segments shall be 68 Ω ± 15%.

The output impedance of the driver shall be used to control transmission line reflections on all electrically long point-to-point signal paths.

NOTE—In the context of this clause, a transmission path whose round-trip propagation delay is less than half of the 10%–90% rise/fall time of signals driven onto the path is considered an electrically short transmission path.

22.4.3 Driver characteristics

The driver characteristics defined in this clause apply to all MII signal drivers. The driver characteristics are specified in terms of both their ac and dc characteristics.

NOTE—Rail-to-rail drivers that comply with the driver output V-I diagrams in Annex 22B will meet the following ac and dc characteristics.

22.4.3.1 DC characteristics

The high (one) logic level output potential V_{oh} shall be no less than 2.40 V at an output current I_{oh} of –4.0 mA. The low (zero) logic level output potential V_{ol} shall not be greater than 0.40 V at an output current I_{ol} of 4.0 mA.

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22.4.3.2 AC characteristics

Drivers must also meet certain ac specifications in order to ensure adequate signal quality for electrically long point-to-point transmission paths. The ac specifications shall guarantee the following performance requirements.

The initial incident potential change arriving at the receiving end of a point-to-point MII signal path plus its reflection from the receiving end of the path must switch the receiver input potential monotonically from a valid high (one) level to $V_{il} \leq V_{il(max)} - 200$ mV, or from a valid low (zero) level to $V_{ih} \geq V_{ih(min)} + 200$ mV.

Subsequent incident potential changes arriving at the receiving end of a point-to-point MII signal path plus their reflections from the receiving end of the path must not cause the receiver input potential to reenter the range $V_{il(max)} - 200$ mV $< V_i < V_{ih(min)} + 200$ mV except when switching from one valid logic level to the other. Such subsequent incident potential changes result from a mismatch between the characteristic impedance of the signal path and the driver output impedance.

22.4.4 Receiver characteristics

The receiver characteristics are specified in terms of the threshold levels for the logical high (one) and logical low (zero) states. In addition, receivers must meet the input current and capacitance limits.

22.4.4.1 Voltage thresholds

An input potential V_i of 2.00 V or greater shall be interpreted by the receiver as a logical high (one). Thus, $V_{ih(min)} = 2.00$ V. An input potential V_i of 0.80 V or less shall be interpreted by the receiver as a logical low (zero). Thus, $V_{il(max)} = 0.80$ V. The switching region is defined as signal potentials greater than $V_{il(max)}$ and less than $V_{ih(min)}$. When the input signal potential is in the switching region, the receiver output is undefined.

22.4.4.2 Input current

The input current requirements shall be measured at the MII connector and shall be referenced to the +5 V supply and COMMON pins of the connector. The input current requirements shall be met across the full range of supply voltage specified in 22.5.1.

The bidirectional signal MDIO has two sets of input current requirements. The MDIO drivers must be disabled when the input current measurement is made.

The input current characteristics for all MII signals shall fall within the limits specified in Table 22–11.

NOTE—These limits for dc input current allow the use of weak resistive pull-ups or pull-downs on the input of each MII signal. They allow the use of weak resistive pull-downs on the signals other than COL, MDC, and MDIO. They allow the use of a weak resistive pull-up on the signal COL. They allow the use of a resistive pull-down of 2 kΩ ± 5% on the MDIO signal in the STA. They require a resistive pull-up of 1.5 kΩ ± 5% on the MDIO signal in a PHY that is attached to the MII via the mechanical interface specified in 22.6. The limits on MDC and MDIO allow the signals to be "bused" to several PHYs that are contained on the same printed circuit assembly, with a single PHY attached via the MII connector.

22.4.4.3 Input capacitance

For all signals other than MDIO, the receiver input capacitance C_i shall not exceed 8 pF.

For the MDIO signal, the transceiver input capacitance shall not exceed 10 pF.

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Table 22–11—Input current limits

Symbol	Parameter	Condition	Signal(s)	Min (μA)	Max (μA)
I_{ih}	Input High Current	V_i=5.25 V	All except COL, MDC, MDIO[a]	—	200
			COL[b]	—	20
			MDC[c]	—	20
			MDIO[d]	—	3000
			MDIO[e]	—	20
I_{il}	Input Low Current	V_i=0.00 V	All except COL, MDC, MDIO[a]	–20	—
			COL[b]	–200	—
			MDC[c]	–20	—
			MDIO[d]	–180	—
			MDIO[e]	–3800	—
I_{iq}	Input Quiescent Current	V_i=2.4 V	MDIO[d]	—	1450
			MDIO[e]	–1450	—

[a]Measured at input of Reconciliation sublayer for CRS, RXD<3:0>, RX_CLK, RX_DV, RX_ER, and TX_CLK. Measured at inputs of PHY for TXD<3:0>, TX_EN, and TX_ER.
[b]Measured at input of Reconciliation sublayer.
[c]Measured at input of PHY.
[d]Measured at input of STA.
[e]Measured at input of PHY, which can be attached via the mechanical interface specified in 22.6.

22.4.5 Cable characteristics

The MII cable consists of a bundle of individual twisted pairs of conductors with an overall shield covering this bundle. Each twisted pair shall be composed of a conductor for an individual signal and a return path dedicated to that signal.

NOTE—It is recommended that the signals RX_CLK and TX_CLK be connected to pairs that are located in the center of the cable bundle.

22.4.5.1 Conductor size

The specifications for dc resistance in 22.4.5.6 and characteristic impedance in 22.4.5.2 assume a conductor size of 0.32 mm (28 AWG).

22.4.5.2 Characteristic impedance

The single-ended characteristic impedance of each twisted pair shall be 68 Ω ± 10%. The characteristic impedance measurement shall be performed with the return conductor connected to the cable's overall shield at both ends of the cable.

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22.4.5.3 Delay

The propagation delay for each twisted pair, measured from the MII connector to the PHY, shall not exceed 2.5 ns. The measurement shall be made with the return conductor of the pair connected to the cable's overall shield at both ends of the cable. The propagation delay shall be measured at a frequency of 25 MHz.

22.4.5.4 Delay variation

The variation in the propagation delay of the twisted pairs in a given cable bundle, measured from the MII connector to the PHY, shall not exceed 0.1 ns. The measurement shall be made with the return conductor of the pair connected to the cable's overall shield at both ends of the cable.

22.4.5.5 Shielding

The overall shield must provide sufficient shielding to meet the requirements of protection against electromagnetic interference.

The overall shield shall be terminated to the connector shell as defined in 22.6.2. A double shield, consisting of both braid and foil shielding, is strongly recommended.

22.4.5.6 DC resistance

The dc resistance of each conductor in the cable, including the contact resistance of the connector, shall not exceed 150 mΩ measured from the MII connector to the remote PHY.

22.4.6 Hot insertion and removal

The insertion or removal of a PHY from the MII with power applied (hot insertion or removal) shall not damage the devices on either side of the MII. In order to prevent contention between multiple output buffers driving the PHY output signals, a PHY that is attached to the MII via the mechanical interface defined in 22.6 shall ensure that its output buffers present a high impedance to the MII during the insertion process, and shall ensure that this condition persists until the output buffers are enabled via the Isolate control bit in the management interface basic register.

NOTE—The act of inserting or removing a PHY from an operational system may cause the loss of one or more packets or management frames that may be in transit across the MII or MDI.

22.5 Power supply

When the mechanical interface defined in 22.6 is used to interconnect printed circuit subassemblies, the Reconciliation sublayer shall provide a regulated power supply for use by the PHY.

The power supply shall use the following MII lines:

+5 V: The plus voltage output to the PHY.
COMMON: The return to the power supply.

22.5.1 Supply voltage

The regulated supply voltage to the PHY shall be 5 Vdc ± 5% at the MII connector with respect to the COMMON circuit at the MII over the range of load current from 0 to 750 mA. The method of over/under voltage protection is not specified; however, under no conditions of operation shall the source apply a voltage to the +5 V circuit of less than 0 V or greater than +5.25 Vdc.

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Implementations that provide a conversion from the MII to the Attachment Unit Interface (AUI) to support connection to 10 Mb/s Medium Attachment Units (MAUs) will require a supplemental power source in order to meet the AUI power supply requirements specified in 7.5.2.5.

22.5.2 Load current

The sum of the currents carried on the +5 V lines shall not exceed 750 mA, measured at the MII connector. The surge current drawn by the PHY shall not exceed 5 A peak for a period of 10 ms. The PHY shall be capable of powering up from 750 mA current limited sources.

22.5.3 Short-circuit protection

Adequate provisions shall be made to ensure protection of the power supply from overload conditions, including a short circuit between the +5 V lines and the COMMON lines.

22.6 Mechanical characteristics

When the MII is used to interconnect two printed circuit assemblies via a short length of cable, the cable shall be connected to the circuit assembly that implements the Reconciliation sublayer by means of the mechanical interface defined in this clause.

22.6.1 Definition of mechanical interface

A 40-pole connector having the mechanical mateability dimensions as specified in IEC 61076-3-101: 1997 shall be used for the MII connector. The circuit assembly that contains the MAC sublayer and Reconciliation sublayer shall have a female connector with screw locks, and the mating cable shall have a male connector with jack screws.

No requirements are imposed on the mechanical interface used to connect the MII cable to the PHY circuit assembly when the MII cable is permanently attached to the PHY circuit assembly, as shown in Figure 22–2. If the cable is not permanently attached to the PHY circuit assembly, then a male connector with jack screws shall be used for the MII connector at the PHY circuit assembly.

NOTE—All MII conformance tests are performed at the mating surfaces of the MII connector at the Reconciliation sublayer end of the cable. If a PHY circuit assembly does not have a permanently attached cable, the vendor must ensure that all of the requirements of this clause are also met when a cable that meets the requirements of 22.4.5 is used to attach the PHY circuit assembly to the circuit assembly that contains the Reconciliation sublayer.

22.6.2 Shielding effectiveness and transfer impedance

The shells of these connectors shall be plated with conductive material to ensure the integrity of the current path from the cable shield to the chassis. The transfer impedance of this path shall not exceed the values listed in Table 22–12, after a minimum of 500 cycles of mating and unmating. The shield transfer impedance values listed in the table are measured in accordance with the procedure defined in Annex L of IEEE Std 1394-1995 [B28][2].

All additions to provide for female shell to male shell conductivity shall be on the shell of the connector with male contacts. There should be multiple contact points around the sides of this shell to provide for shield continuity.

[2]The numbers in brackets correspond to those of the bibliography in Annex A in Section One of this standard.

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Table 22–12—Transfer impedance performance requirements

Frequency	Value
30 MHz	–26 dBΩ
159 MHz	–13 dBΩ
500 MHz	–5 dBΩ

22.6.3 Connector pin numbering

Figure 22–18 depicts the MII connector pin numbering, as seen looking into the contacts of a female connector from the mating side.

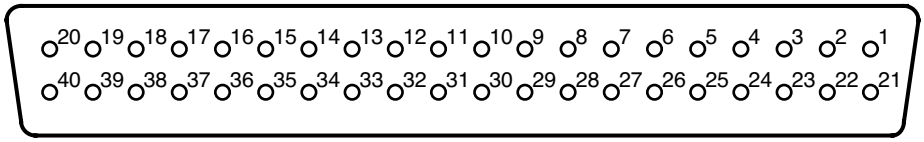


Figure 22–18—MII connector pin numbering

22.6.4 Clearance dimensions

The circuit assembly that contains the MAC sublayer and Reconciliation sublayer shall provide sufficient clearance around the MII connector to allow the attachment of cables that use die cast metal backshells and overmold assemblies. This requirement may be met by providing the clearance dimensions shown in Figure 22–19.

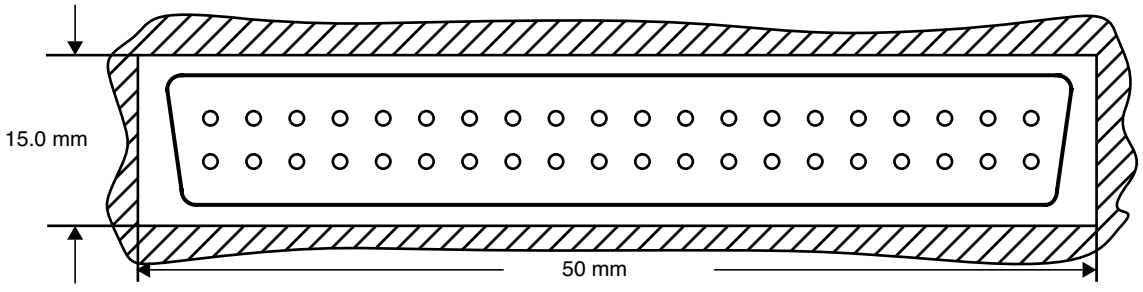


Figure 22–19—MII connector clearance dimensions

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22.6.5 Contact assignments

Table 22–13 shows the assignment of circuits to connector contacts.

Table 22–13—MII connector contact assignments

Contact	Signal name	Contact	Signal name
1	+5 V	21	+5 V
2	MDIO	22	COMMON
3	MDC	23	COMMON
4	RXD<3>	24	COMMON
5	RXD<2>	25	COMMON
6	RXD<1>	26	COMMON
7	RXD<0>	27	COMMON
8	RX_DV	28	COMMON
9	RX_CLK	29	COMMON
10	RX_ER	30	COMMON
11	TX_ER	31	COMMON
12	TX_CLK	32	COMMON
13	TX_EN	33	COMMON
14	TXD<0>	34	COMMON
15	TXD<1>	35	COMMON
16	TXD<2>	36	COMMON
17	TXD<3>	37	COMMON
18	COL	38	COMMON
19	CRS	39	COMMON
20	+5 V	40	+5 V

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22.7 Protocol Implementation Conformance Statement (PICS) proforma for Clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII)[3]

22.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII), shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

22.7.2 Identification

22.7.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requμements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

22.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2002, Clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required?No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

22.7.2.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*GM	Implementation of GMII	22.2.4	O	Yes [ ] No [ ]	

[3]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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22.7.3 PICS proforma tables for reconciliation sublayer and media independent interface

22.7.3.1 Mapping of PLS service primitives

Item	Feature	Subclause	Status	Support	Value/Comment
PL1	Response to RX_ER	22.2.1.5	M		Must produce FrameCheckError at MAC

22.7.3.2 MII signal functional specifications

Item	Feature	Subclause	Status	Support	Value/Comment
SF1	TX_CLK frequency	22.2.2.1	M		25% of transmitted data rate (25 MHz or 2.5 MHz)
SF2	TX_CLK duty cycle	22.2.2.1	M		35% to 65%
SF3	RX_CLK min high/low time	22.2.2.2	M		35% of nominal period
SF4	RX_CLK synchronous to recovered data	22.2.2.2	M		
SF5	RX_CLK frequency	22.2.2.2	M		25% of received data rate (25 MHz or 2.5 MHz)
SF6	RX_CLK duty cycle	22.2.2.2	M		35% to 65%
SF7	RX_CLK source due to loss of signal	22.2.2.2	M		Nominal clock reference (e.g., TX_CLK reference)
SF8	RX_CLK transitions only while RX_DV de-asserted	22.2.2.2	M		
SF9	RX_CLK max high/low time following de-assertion of RX_DV	22.2.2.2	M		max 2 times the nominal period
SF10	TX_EN assertion	22.2.2.3	M		On first nibble of preamble
SF11	TX_EN remains asserted	22.2.2.3	M		Stay asserted while all nibbles are transmitted over MII
SF12	TX_EN transitions	22.2.2.3	M		Synchronous with TX_CLK
SF13	TX_EN negation	22.2.2.3	M		Before first TX_CLK after final nibble of frame
SF14	TXD<3:0> transitions	22.2.2.4	M		Synchronous with TX_CLK
SF15	TXD<3:0> effect on PHY while TX_EN is de-asserted	22.2.2.4	M		No effect
SF16	TX_ER transitions	22.2.2.5	M		Synchronous with TX_CLK
SF17	TX_ER effect on PHY while TX_EN is asserted	22.2.2.5	M		Cause PHY to emit invalid symbol
SF18	TX_ER effect on PHY while operating at 10 Mb/s, or when TX_EN is de-asserted	22.2.2.5	M		No effect on PHY
SF19	TX_ER implementation	22.2.2.5	M		At MII of a PHY

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22.7.3.2 MII signal functional specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
SF20	TX_ER pulled down if not actively driven	22.2.2.5	M		At MII of a repeater or MAC/RS only
SF21	RX_DV transitions	22.2.2.6	M		Synchronous with RX_CLK
SF22	RX_DV assertion	22.2.2.6	M		From first recovered nibble to final nibble of a frame per Figure 22–6
SF23	RX_DV negation	22.2.2.6	M		Before the first RX_CLK follows the final nibble per Figure 22–6
SF24	RXD<3:0> effect on Reconciliation sublayer while RX_DV is de-asserted	22.2.2.7	M		No effect
SF25	RX_ER assertion	22.2.2.8	M		By PHY to indicate error
SF26	RX_ER transitions	22.2.2.8	M		Synchronous with RX_CLK
SF27	RX_ER effect on Reconciliation sublayer while RX_DV is de-asserted	22.2.2.8	M		No effect
SF28	CRS assertion	22.2.2.9	M		By PHY when either transmit or receive is NON-IDLE
SF29	CRS de-assertion	22.2.2.9	M		By PHY when both transmit and receive are IDLE
SF30	CRS assertion during collision	22.2.2.9	M		Remain asserted throughout
SF31	COL assertion	22.2.2.10	M		By PHY upon detection of collision on medium
SF32	COL remains asserted while collision persists	22.2.2.10	M		
SF33	COL response to SQE	22.2.2.10	M		Assertion by PHY
SF34	MDC min high/low time	22.2.2.11	M		160 ns
SF35	MDC min period	22.2.2.11	M		400 ns
SF36	MDIO uses three-state drivers	22.2.2.12	M		
SF37	PHY pullup on MDIO	22.2.2.12	M		1.5 kΩ ± 5% (to +5 V)
SF38	STA pulldown on MDIO	22.2.2.12	M		2 kΩ ± 5% (to 0 V)

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22.7.3.3 Frame structure

Item	Feature	Subclause	Status	Support	Value/Comment
FS1	Format of transmitted frames	22.2.3	M		Per Figure 22–10
FS2	Nibble transmission order	22.2.3	M		Per Figure 22–11
FS3	Preamble 7 octets long	22.2.3.2.1	M		10101010 10101010 10101010 10101010 10101010 10101010 10101010
FS4	Preamble and SFD transmission	22.2.3.2.1	M		Per Table 22–3
FS5	Preamble and SFD reception	22.2.3.2.2	M		Per Table 22–4, Table 22–5
FS6	N octets transmitted as 2N nibbles	22.2.3.3	M		Per Figure 22–11
FS7	Indication of excess nibbles	22.2.3.5	M		Frame contains non-integer number of octets is received

22.7.3.4 Management functions

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	Incorporate of basic register set	22.2.4	M		Two 16-bit registers as Control register (Register 0) and Status register (Register 1)
MF2	Action on reset	22.2.4.1.1	M		Reset the entire PHY including Control and Status to default value and set bit 0.15 = 1
MF3	Return 1 until reset completed	22.2.4.1.1	M		Yes (when reset is done, 0.15 is self clearing)
MF4	Reset completes within 0.5 s	22.2.4.1.1	M		
MF5	Loopback mode	22.2.4.1.2	M		Whenever 0.14 is 1
MF6	Receive circuitry isolated from network in loopback mode	22.2.4.1.2	M		
MF7	Effect of assertion of TX_EN in loopback mode	22.2.4.1.2	M		No transmission
MF8	Propagation of data in loopback mode	22.2.4.1.2	M		PHY accepts transmit data and return it as receive data
MF9	Delay from TX_EN to RX_DV in loopback mode	22.2.4.1.2	M		Less than 512 BT
MF10	Behavior of COL in loopback mode	22.2.4.1.2	M		De-asserted (for 0.7 = 0)
MF11	Behavior of COL in loopback mode	22.2.4.1.2	M		If 0.7 = 1, see MF33 and MF34
MF12	Value of speed selection bits	22.2.4.1.3	M	Yes [ ]	Set to match a valid PHY speed

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22.7.3.4 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF13	Ignore writes to speed selection bits for unsupported speed	22.2.4.1.3	M	Yes [ ]	
MF14	Auto-Negotiation enable	22.2.4.1.4	M		By setting 0.12 = 1
MF15	Duplex mode, speed selection have no effect when Auto-Negotiation is enabled	22.2.4.1.4	M	Yes [ ]	If 0.12=1, bits 0.13, 0.8 and 0.6 have no effect on link configuration
MF16	PHY without Auto-Negotiation returns value of zero	22.2.4.1.4	M		Yes (if 1.3=0, then 0.12=0)
MF17	PHY without Auto-Negotiation ignores writes to enable bit	22.2.4.1.4	M		Yes (if 1.3=0, 0.12 always = 0 and cannot be changed)
MF18	Response to management transactions in power down	22.2.4.1.5	M		Remains active
MF19	Spurious signals in power down	22.2.4.1.5	M		None (not allowed)
MF20	TX_CLK and RX_CLK stabilize within 0.5 s	22.2.4.1.5	M		Yes (after both bits 0.11 and 0.10 are cleared to zero)
MF21	PHY Response to input signals while isolated	22.2.4.1.6	M		NONE
MF22	High impedance on PHY output signals while isolated	22.2.4.1.6	M	Yes [ ]	Yes (TX_CLK, RX_CLK, RX_DV, RX_ER, RXD bundle, COL, and CRS)
MF23	Response to management transactions while isolated	22.2.4.1.6	M		Remains active
MF24	Default value of isolate	22.2.4.1.6	M		0.10 =1
MF25	PHY without Auto-Negotiation returns value of zero	22.2.4.1.7	M		0.9 = 0 if 1.3 = 0 or 0.12 = 0
MF26	PHY without Auto-Negotiation ignores writes to restart bit	22.2.4.1.7	M		0.9 = 0, cannot be changed if 1.3 = 0 or 0.12 = 0
MF27	Restart Auto-Negotiation	22.2.4.1.7	M		When 0.9 = 1 if 0.12 = 1 and 1.3 = 1
MF28	Return 1 until Auto-Negotiation initiated	22.2.4.1.7	M		0.9 is self clearing to 0
MF29	Auto-Negotiation not effected by clearing bit	22.2.4.1.7	M		
MF30	Value of duplex mode bit for PHYs with one duplex mode	22.2.4.1.8	M		Set 0.8 to match the correct PHY duplex mode
MF31	PHY with one duplex mode ignores writes to duplex bit	22.2.4.1.8	M		Yes (0.8 remains unchanged)
MF32	Loopback not affected by duplex mode	22.2.4.1.8	M		Yes (0.8 has no effect on PHY when 0.14 = 1)
MF33	Assertion of COL in collision test mode	22.2.4.1.9	M		Within 512 BT after TX_EN is asserted

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22.7.3.4 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF34	De-assertion of COL in collision test mode	22.2.4.1.9	M	Yes [ ]	After TX_EN is de-asserted within: MII = 4 BT, GMII = 16 BT
MF35	Reserved bits written as zero	22.2.4.1.11	M		
MF36	Reserved bits ignored when read	22.2.4.1.11	M		
MF37	PHY returns 0 in reserved bits	22.2.4.1.11	M		
MF38	Effect of write on status register	22.2.4.2	M		No effect
MF39	Reserved bits ignored when read	22.2.4.2.8	M		
MF40	PHY returns 0 in reserved bits	22.2.4.2.8	M		
MF41	PHY returns 0 if Auto-Negotiation disabled	22.2.4.2.10	M		Yes (1.5 = 0 when 0.12 = 0)
MF42	PHY returns 0 if it lacks ability to perform Auto-Negotiation	22.2.4.2.10	M		Yes (1.5 = 0 when 1.3 = 0)
MF43	Remote fault has latching function	22.2.4.2.11	M		Yes (once set will remain set until cleared)
MF44	Remote fault cleared on read	22.2.4.2.11	M		Yes
MF45	Remote fault cleared on reset	22.2.4.2.11	M		Yes (when 0.15 = 1)
MF46	PHY without remote fault returns value of zero	22.2.4.2.11	M		Yes (1.4 always 0)
MF47	Link status has latching function	22.2.4.2.13	M		Yes (once cleared by link failure will remain cleared until read by MII)
MF48	Jabber detect has latching function	22.2.4.2.14	M		Yes (once set will remain set until cleared)
MF49	Jabber detect cleared on read	22.2.4.2.14	M		
MF50	Jabber detect cleared on reset	22.2.4.2.14	M		
MF51	All PHYs operating at rates of 100 Mb/s or above return 0 for jabber detect	22.2.4.2.14	M	Yes [ ]	Yes (1.1 always = 0 for all PHYs operating at rates of 100 Mb/s or above)
MF52	MDIO not driven if register read is unimplemented	22.2.4.3	M		Yes (MDIO remain high impedance)
MF53	Write has no effect if register written is unimplemented	22.2.4.3	M		
MF54	Registers 2 and 3 constitute unique identifier for PHY type	22.2.4.3.1	M		
MF55	MSB of PHY identifier is 2.15	22.2.4.3.1	M		
MF56	LSB of PHY identifier is 3.0	22.2.4.3.1	M		

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22.7.3.4 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF57	Composition of PHY identifier	22.2.4.3.1	O	Yes [ ] No [ ]	22-bit OUI, 6-bit model, 4-bit version per Figure 22–12
MF58	Format of management frames	22.2.4.5	M		Per Table 22–9
MF59	Idle condition on MDIO	22.2.4.5.1	M		High impedance state
MF60	MDIO preamble sent by STA	22.2.4.5.2	M		32 contiguous logic one bits
MF61	MDIO preamble observed by PHY	22.2.4.5.2	M		32 contiguous logic one bits
MF62	Assignment of PHYAD 0	22.2.4.5.5	M		Address of PHY attached via Mechanical Interface
MF63	Assignment of REGAD 0	22.2.4.5.6	M		MII control register address
MF64	Assignment of REGAD 1	22.2.4.5.6	M		MII status register address
MF65	High impedance during first bit time of turnaround in read transaction	22.2.4.5.7	M		
MF66	PHY drives zero during second bit time of turnaround in read transaction	22.2.4.5.7	M		
MF67	STA drives MDIO during turnaround in write transaction	22.2.4.5.7	M		
MF68	First data bit transmitted	22.2.4.5.8	M		Bit 15 of the register being addressed
MF69	Incorporate Extended Status register	22.2.4	GM:M	Yes [ ] NA [ ]	16-bit register Extended Status register (Register 15)
MF70	Reserved bits written as zero	22.2.4.2.8	GM:M	Yes [ ] NA [ ]	
MF71	Extended Status	22.2.4.2.16	GM:M	Yes [ ] NA [ ]	Yes (1.8 always = 1 for 1000 Mb/s operation)
MF72	Write to Extended Status register	22.2.4.4	GM:M	Yes [ ] NA [ ]	No effect
MF73	Reserved bits written as zero	22.2.4.4.5	GM:M	Yes [ ] NA [ ]	
MF74	Reserved bits ignored when read	22.2.4.4.5	GM:M	Yes [ ] NA [ ]	
MF75	PHY returns 0 in reserved bits	22.2.4.4.5	GM:M	Yes [ ] NA [ ]	

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22.7.3.5 Signal timing characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
ST1	Timing characteristics measured in accordance with Annex 22C	22.3	M		
ST2	Transmit signal clock to output delay	22.3.1	M		Min = 0 ns; Max = 25 ns per Figure 22–14
ST3	Receive signal setup time	22.3.2	M		Min = 10 ns per Figure 22–15
ST4	Receive signal hold time	22.3.2	M		Min = 10 ns per Figure 22–15
ST5	MDIO setup and hold time	22.3.4	M		Setup min = 10 ns; Hold min = 10 ns per Figure 22–16
ST6	MDIO clock to output delay	22.3.4	M		Min = 0 ns; Max = 300 ns per Figure 22–17

22.7.3.6 Electrical characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
EC1	Signal paths are either point to point, or a sequence of point-to-point transmission paths	22.4.2	M		
EC2	MII uses unbalanced signal transmission paths	22.4.2	M		
EC3	Characteristic impedance of electrically long paths	22.4.2	M		68 Ω ± 15%
EC4	Output impedance of driver used to control reflections	22.4.2	M		On all electrically long point to point signal paths
EC5	V_{oh}	22.4.3.1	M		≥ 2.4 V (I_{oh} = –4 mA)
EC6	V_{ol}	22.4.3.1	M		≤ 0.4 V (I_{ol} = 4 mA)
EC7	Performance requirements to be guaranteed by ac specifications	22.4.3.2	M		Min switching potential change (including its reflection) ≥ 1.8 V
EC8	$V_{ih(min)}$	22.4.4.1	M		2 V
EC9	$V_{il(max)}$	22.4.4.1	M		0.8 V
EC10	Input current measurement point	22.4.4.2	M		At MII connector
EC11	Input current reference potentials	22.4.4.2	M		Reference to MII connector +5 V and COMMON pins
EC12	Input current reference potential range	22.4.4.2	M		0 V to 5.25 V
EC13	Input current limits	22.4.4.2	M		Per Table 22–10

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22.7.3.6 Electrical characteristics *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
EC14	Input capacitance for signals other than MDIO	22.4.4.3	M		≤ 8 pF
EC15	Input capacitance for MDIO	22.4.4.3	M		≤ 10 pF
EC16	Twisted-pair composition	22.4.5	M		Conductor for each signal with dedicated return path
EC17	Single-ended characteristic impedance	22.4.5.2	M		68 Ω ± 10%
EC18	Characteristic impedance measurement method	22.4.5.2	M		With return conductor connected to cable shield
EC19	Twisted-pair propagation delay	22.4.5.3	M		≤ 2.5 ns
EC20	Twisted-pair propagation delay measurement method	22.4.5.3	M		With return conductor connected to cable shield
EC21	Twisted-pair propagation delay measurement frequency	22.4.5.3	M		25 MHz
EC22	Twisted-pair propagation delay variation	22.4.5.4	M		≤ 0.1 ns
EC23	Twisted-pair propagation delay variation measurement method	22.4.5.4	M		With return conductor connected to cable shield
EC24	Cable shield termination	22.4.5.5	M		To the connector shell
EC25	Cable conductor DC resistance	22.4.5.6	M		≤ 150 mΩ
EC26	Effect of hot insertion/removal	22.4.6	M		Causes no damage
EC27	State of PHY output buffers during hot insertion	22.4.6	M		High impedance
EC28	State of PHY output buffers after hot insertion	22.4.6	M		High impedance until enabled via Isolate bit

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22.7.3.7 Power supply

Item	Feature	Subclause	Status	Support	Value/Comment
PS1	Regulated power supply provided	22.5	M		To PHY by Reconciliation sublayer
PS2	Power supply lines	22.5	M		+5 V and COMMON (return of +5 V)
PS3	Regulated supply voltage limits	22.5.1	M		5 Vdc ± 5%
PS4	Over/under voltage limits	22.5.1	M		Over limit = 5.25 Vdc Under limit = 0 V
PS5	Load current limit	22.5.2	M		750 mA
PS6	Surge current limit	22.5.2	M		≤ 5 A peak for 10 ms
PS7	PHY can power up from current limited source	22.5.2	M		From 750 mA current limited source
PS8	Short-circuit protection	22.5.2	M		When +5 V and COMMON are shorted

22.7.3.8 Mechanical characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
*MC1	Use of Mechanical Interface	22.6	O		Optional
MC2	Connector reference standard	22.6.1	MC1:M		IEC 61076-3-101: 1997
MC3	Use of female connector	22.6.1	MC1:M		At MAC/RS side
MC4	Use of male connector	22.6.1	MC1:M		At PHY mating cable side
MC5	Connector shell plating	22.6.2	MC1:M		Use conductive material
MC6	Shield transfer impedance	22.6.2	MC1:M		After 500 cycles of mating/ unmating, per Table 22–11
MC7	Additions to provide for female shell to male shell conductivity	22.6.2	MC1:M		On shell of conductor with male contacts
MC8	Clearance dimensions	22.6.4	MC1:M		15 mm × 50 mm, per Figure 22–19

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23. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T4

NOTE—This PHY is not recommended for new installations.

23.1 Overview

The 100BASE-T4 PCS, PMA, and baseband medium specifications are aimed at users who want 100 Mb/s performance, but would like to retain the benefits of using voice-grade twisted-pair cable. 100BASE-T4 signaling requires four pairs of Category 3 or better cable, installed according to ISO/IEC 11801: 1995, as specified in 23.6. This type of cable, and the connectors used with it, are simple to install and reconfigure. 100BASE-T4 does not transmit a continuous signal between packets, which makes it useful in battery powered applications. The 100BASE-T4 PHY is one of the 100BASE-T family of high-speed CSMA/CD network specifications.

23.1.1 Scope

This clause defines the type 100BASE-T4 Physical Coding Sublayer (PCS), type 100BASE-T4 Physical Medium Attachment (PMA) sublayer, and type 100BASE-T4 Medium Dependent Interface (MDI). Together, the PCS and PMA layers comprise a 100BASE-T4 Physical Layer (PHY). Provided in this document are full functional, electrical, and mechanical specifications for the type 100BASE-T4 PCS, PMA, and MDI. This clause also specifies the baseband medium used with 100BASE-T4.

23.1.2 Objectives

The following are the objectives of 100BASE-T4:

a) To support the CSMA/CD MAC in the half duplex mode of operation.
b) To support the 100BASE-T MII, Repeater, and optional Auto-Negotiation.
c) To provide 100 Mb/s data rate at the MII.
d) To provide for operating over unshielded twisted pairs of Category 3, 4, or 5 cable, installed as horizontal runs in accordance with ISO/IEC 11801: 1995, as specified in 23.6, at distances up to 100 m (328 ft).
e) To allow for a nominal network extent of 200 m, including:
   1) Unshielded twisted-pair links of 100 m.
   2) Two-repeater networks of approximately a 200 m span.
f) To provide a communication channel with a mean ternary symbol error rate, at the PMA service interface, of less than one part in 10^8.

23.1.3 Relation of 100BASE-T4 to other standards

Relations between the 100BASE-T4 PHY and the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model are shown in Figure 23–1. The PHY Layers shown in Figure 23–1 connect one Clause 4 Media Access Control (MAC) layer to a Clause 27 repeater. This clause also discusses other variations of the basic configuration shown in Figure 23–1. This whole clause builds on Clauses 1 through 4 of this standard.

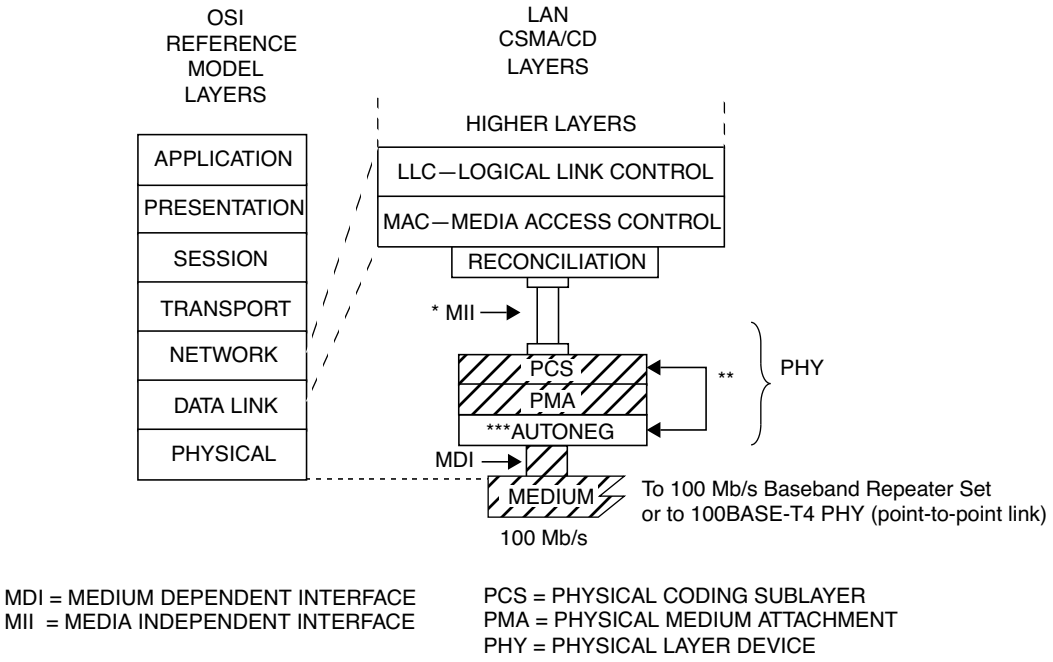
23.1.4 Summary

The following paragraphs summarize the PCS and PMA clauses of this standard.

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* MII is optional.
** AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indicate.
*** AUTONEG is optional.

Figure 23–1—Type 100BASE-T4 PHY relationship to the ISO Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

23.1.4.1 Summary of Physical Coding Sublayer (PCS) specification

The 100BASE-T4 PCS couples a Media Independent Interface (MII), as described in Clause 22, to a Physical Medium Attachment sublayer (PMA).

The PCS Transmit function accepts data nibbles from the MII. The PCS Transmit function encodes these nibbles using an 8B6T coding scheme (to be described) and passes the resulting ternary symbols to the PMA. In the reverse direction, the PMA conveys received ternary symbols to the PCS Receive function. The PCS Receive function decodes them into octets, and then passes the octets one nibble at a time up to the MII. The PCS also contains a PCS Carrier Sense function, a PCS Error Sense function, a PCS Collision Presence function, and a management interface.

Figure 23–2 shows the division of responsibilities between the PCS, PMA, and MDI layers.

Physical level communication between PHY entities takes place over four twisted pairs. This specification permits the use of Category 3, 4, or 5 unshielded twisted pairs, installed according to ISO/IEC 11801: 1995, as specified in 23.6. Figure 23–3 shows how the PHY manages the four twisted pairs at its disposal.

The 100BASE-T4 transmission algorithm always leaves one pair open for detecting carrier from the far end (see Figure 23–3). Leaving one pair open for carrier detection in each direction greatly simplifies media access control. All collision detection functions are accomplished using only the unidirectional pairs TX_D1 and RX_D2, in a manner similar to 10BASE-T. This collision detection strategy leaves three pairs in each direction free for data transmission, which uses an 8B6T block code, schematically represented in Figure 23–4.

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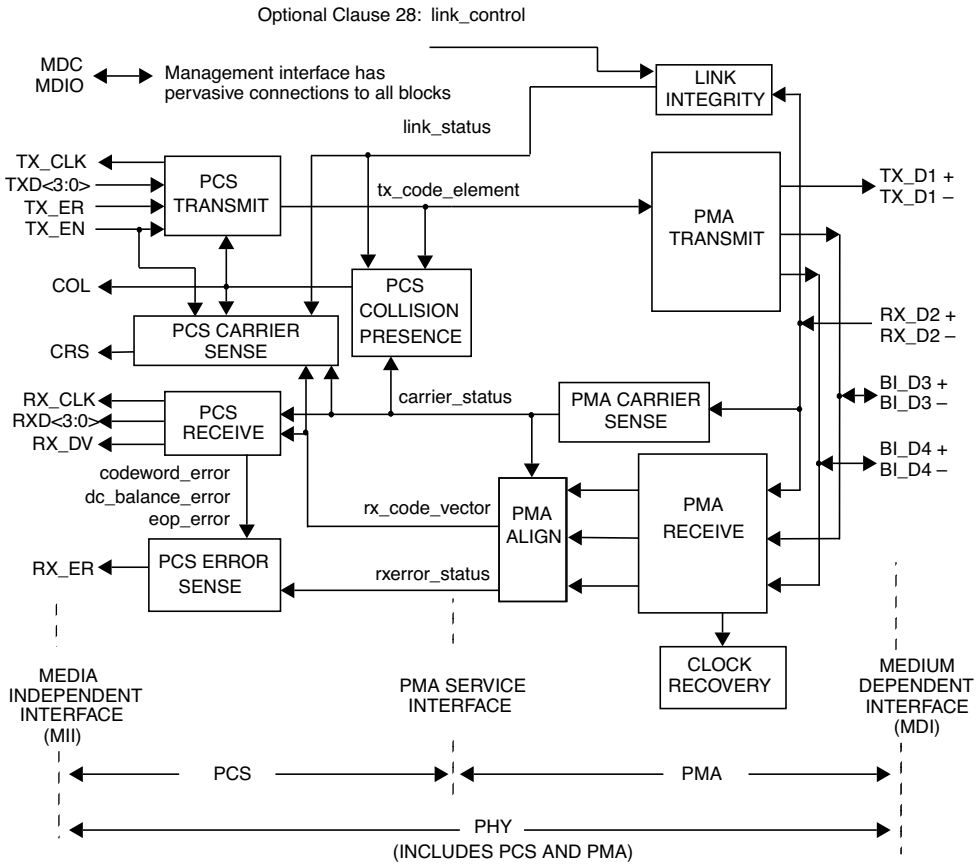


Figure 23–2—Division of responsibilities between 100BASE-T4 PCS and PMA

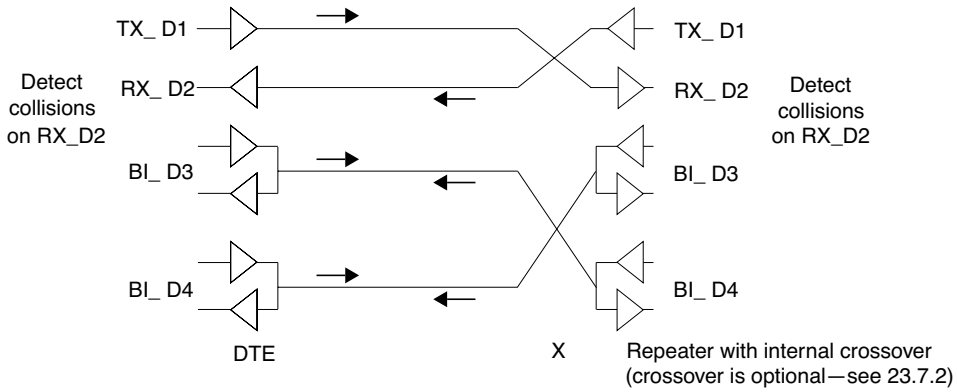


Figure 23–3—Use of wire pairs

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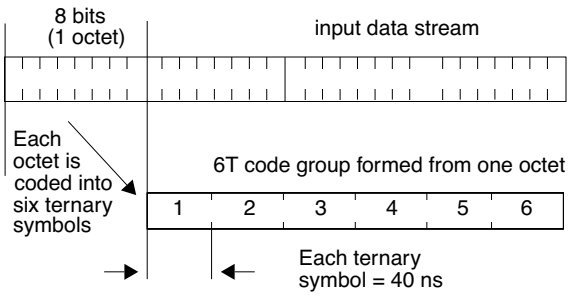


Figure 23–4—8B6T coding

8B6T coding, as used with 100BASE-T4 signaling, maps data octets into ternary symbols. Each octet is mapped to a pattern of 6 ternary symbols, called a 6T code group. The 6T code groups are fanned out to three independent serial channels. The effective data rate carried on each pair is one third of 100 Mb/s, which is 33.333... Mb/s. The ternary symbol transmission rate on each pair is 6/8 times 33.33 Mb/s, or precisely 25.000 MHz.

Refer to Annex 23A for a complete listing of 8B6T code words.

The PCS functions and state diagrams are specified in 23.2. The PCS electrical interface to the MII conforms to the interface requirements of Clause 21. The PCS interface to the PMA is an abstract message-passing interface specified in 23.3.

23.1.4.2 Summary of physical medium attachment (PMA) specification

The PMA couples messages from the PMA service interface onto the twisted-pair physical medium. The PMA provides communications, at 100 Mb/s, over four pairs of twisted-pair wiring up to 100 m in length.

The PMA Transmit function, shown in Figure 23–2, comprises three independent ternary data transmitters. Upon receipt of a PMA_UNITDATA.request message, the PMA synthesizes one ternary symbol on each of the three output channels (TX_D1, BI_D3, and BI_D4). Each output driver has a *ternary* output, meaning that the output waveform can assume any of three values, corresponding to the transmission of ternary symbols CS0, CS1 or CS-1 (see 23.4.3.1) on each of the twisted pairs.

The PMA Receive function comprises three independent ternary data receivers. The receivers are responsible for acquiring clock, decoding the Start of Stream Delimiter (SSD) on each channel, and providing data to the PCS in the synchronous fashion defined by the PMA_UNITDATA.indicate message. The PMA also contains functions for PMA Carrier Sense and Link Integrity.

PMA functions and state diagrams appear in 23.4. PMA electrical specifications appear in 23.5.

23.1.5 Application of 100BASE-T4

23.1.5.1 Compatibility considerations

All implementations of the twisted-pair link shall be compatible at the MDI. The PCS, PMA, and the medium are defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the PCS and PMA (in an application-dependent manner) provided the MDI (and MII, when implemented) specifications are met.

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23.1.5.2 Incorporating the 100BASE-T4 PHY into a DTE

The PCS is required when used with a DTE. The PCS provides functions necessary to the overall system operation (such as 8B6T coding) and cannot be omitted. Refer to Figure 23–1.

When the PHY is incorporated within the physical bounds of a DTE, conformance to the MII interface is optional, provided that the observable behavior of the resulting system is identical to a system with a full MII implementation. For example, an integrated PHY may incorporate an interface between PCS and MAC that is logically equivalent to the MII, but does not have the full output current drive capability called for in the MII specification.

23.1.5.3 Use of 100BASE-T4 PHY for point-to-point communication

The 100BASE-T4 PHY, in conjunction with the MAC specified in Clauses 1 through 4 (including parameterized values in 4.4.2.3 to support 100 Mb/s operation), may be used at both ends of a link for point-to-point applications between two DTEs. Such a configuration does not require a repeater. In this case each PHY may connect through an MII to its respective DTE. Optionally, either PHY (or both PHYs) may be incorporated into the DTEs without an exposed MII.

23.1.5.4 Support for Auto-Negotiation

The PMA service interface contains primitives used by the Auto-Negotiation algorithm (Clause 28) to automatically select operating modes when connected to a like device.

23.2 PCS functional specifications

The 100BASE-T4 PCS couples a Media Independent Interface (MII), as described in Clause 22, to a 100BASE-T4 Physical Medium Attachment sublayer (PMA).

At its interface with the MII, the PCS communicates via the electrical signals defined in Clause 22.

The interface between PCS and the next lower level (PMA) is an abstract message-passing interface described in 23.3. The physical realization of this interface is left to the implementor, provided the requirements of this standard, where applicable, are met.

23.2.1 PCS functions

The PCS comprises one PCS Reset function and five simultaneous and asynchronous operating functions. The PCS operating functions are PCS Transmit, PCS Receive, PCS Error Sense, PCS Carrier Sense, and PCS Collision Presence. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 23–5, shows how the five operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive, and are not shown in Figure 23–5. The management functions are specified in Clause 30. See also Figure 23–6, which defines the structure of frames passed from PCS to PMA. See also Figure 23–7, which presents a reference model helpful for understanding the definitions of PCS Transmit function state variables ohr1-4 and tsr.

23.2.1.1 PCS Reset function

The PCS Reset function shall be executed any time either of two conditions occur. These two conditions are “power on” and the receipt of a reset request from the management entity. The PCS Reset function initializes

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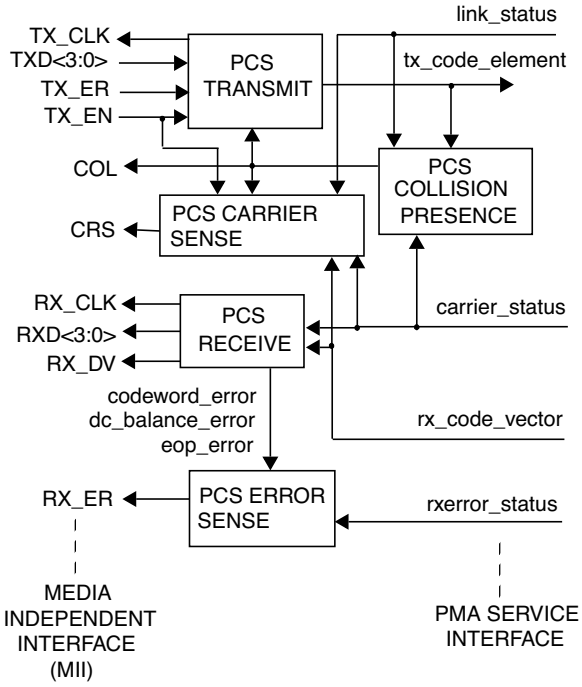


Figure 23–5—PCS reference diagram

all PCS functions. The PCS Reset function sets pcs_reset=ON for the duration of its reset function. All state diagrams take the open-ended pcs_reset branch upon execution of the PCS Reset function. The reference diagrams do not explicitly show the PCS Reset function.

23.2.1.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 23–8.

The PCS Transmit function receives nibbles from the TXD signals of the MII, assembles pairs of nibbles to form octets, converts the octets into 6T code groups according to the 8B6T code table, and passes the resulting ternary data to the PMA using the PMA_UNITDATA.request message. The state diagram of Figure 23–8 depicts the PCS Transmit function operation. Definitions of state variables tsr, ohr, sosa, sosb, eop1-5, and tx_extend used in that diagram, as well as in the following text, appear in 23.2.4.1. The physical structure represented in Figure 23–7 is not required; it merely serves to explain the meaning of the state diagram variables ohr and tsr in Figure 23–8. Implementors are free to construct any logical devices having functionality identical to that described by this functional description and the PCS Transmit state diagram, Figure 23–8.

PCS Transmit makes use of the tsr and ohr shift registers to manage nibble assembly and ternary symbol transmission. Nibbles from the MII go into tsr, which PCS Transmit reads as octets. PCS Transmit then encodes those octets and writes 6T code groups to the ohr registers. The PMA_UNITDATA.request message passes ternary symbols from the ohr registers to the PMA. In each state diagram block, the ohr loading operations are conducted first, then tx_code_vector is loaded and the state diagram waits 40 ns.

The first 5 octets assembled by the PCS Transmit function are encoded into the sosa code word and the next 3 octets assembled are encoded into the sosb code word. This guarantees that every packet begins with a valid preamble pattern. This is accomplished by the definition of tsr. In addition, the PCS Transmit state

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diagram also specifies that at the start of a packet all three output holding registers ohr1, ohr3 and ohr4 will be loaded with the same value (sosa). This produces the ternary symbols labeled P3 and P4 in Figure 23–6

At the conclusion of the MAC frame, the PCS Transmit function appends eop1-5. This is accomplished by defining a variable tx_extend to stretch the TX_EN signal, and defining tsr during this time to be a sequence of constants that decodes to the proper eop code groups.

The encoding operation shall use the 8B6T code table listed in Annex 23A, and the dc balance encoding rules listed below. Encoding is performed separately for each transmit pair.

23.2.1.2.1 DC balance encoding rules

The encoding operation maintains dc balance on each transmit pair by keeping track of the cumulative weight of all 6T code groups (see *weight of 6T code group*, Annex 23A) transmitted on that pair. For each pair, it initiates the cumulative weight to 0 when the PCS Transmit function is in the AWAITING DATA TO TRANSMIT state. All 6T code groups in the code table have weight 0 or 1. The dc balance algorithm conditionally negates transmitted 6T code groups, so that the code weights transmitted on the line include 0, +1, and –1. This dc balance algorithm ensures that the cumulative weight on each pair at the conclusion of each 6T code group is always either 0 or 1, so only one bit per pair is needed to store the cumulative weight. As used below, the phrase “invert the cumulative weight bit” means “if the cumulative weight bit is zero then set it to one, otherwise set it to zero.”

After encoding any octet, except the constants sosa, sosb, eop1-5 or bad_code, update the cumulative weight bit for the affected pair according to rules a) through c):

a) If the 6T code group weight is 0, do not change the cumulative weight.
b) If the 6T code group weight is 1, and the cumulative weight bit is 0, set the cumulative weight bit to 1.
c) If the 6T code group weight is 1, and the cumulative weight bit is also 1, set the cumulative weight bit to 0, and then algebraically negate all the ternary symbol values in the 6T code group.

After encoding any of the constants sosa, sosb, or bad_code, update the cumulative weight bit for the affected pair according to rule d):

d) Do not change the cumulative weight. Never negate sosa, sosb or bad_code.

After encoding any of the constants eop1-5, update the cumulative weight bit for the affected pair according to rules e) and f):

e) If the cumulative weight is 0, do not change the cumulative weight; algebraically negate all the ternary symbol values in eop1-5.
f) If the cumulative weight is 1, do not change the cumulative weight.

NOTE—The inversion rules for eop1-5 are opposite rule b). That makes eop1-5 look very unlike normal data, increasing the number of errors required to synthesize a false end-of-packet marker.

23.2.1.3 PCS Receive function

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 23–9.

The PCS Receive function accepts ternary symbols from the PMA, communicated via the PMA_UNITDATA.indicate message, converts them using 8B6T coding into a nibble-wide format and passes them up to the MII. This function also generates RX_DV. The state diagram of Figure 23–9 depicts the PCS Receive function. Definitions of state variables ih2, ih3, and ih4 used in that diagram, as well as in the following text, appear in 23.2.4.1.

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The last 6 values of the rx_code_vector are available to the decoder. PCS Receive makes use of these stored rx_code_vector values as well as the ih2-4 registers to manage the assembly of ternary symbols into 6T code groups, and the conversion of decoded data octets into nibbles. The last 6 ternary symbols for pair BI_D3 (as extracted from the last 6 values of rx_code_vector) are referred to in the state diagram as BI_D3[0:5]. Other pairs are referenced accordingly.

The PCS Receive state diagram starts the first time the PCS receives a PMA_UNITDATA.indicate message with rx_code_vector=DATA (as opposed to IDLE or PREAMBLE). The contents of this first PMA_UNITDATA.indicate (DATA) message are specified in 23.4.1.6.

After the sixth PMA_UNITDATA.indicate (DATA) message (state DECODE CHANNEL 3), there is enough information to decode the first data octet. The decoded data is transmitted across the MII in two parts, a least significant nibble followed by a most significant nibble (see Clause 22).

During state COLLECT 4TH TERNARY SYMBOL the PCS Receive function raises RX_DV and begins shifting out the nibbles of the 802.3 MAC SFD, least significant nibble first (SFD:LO). The most significant nibble of the 802.3 MAC SFD, called SFD:HI, is sent across the MII during the next state, COLLECT 5TH TERNARY SYMBOL.

Once eop is signaled by the decode operation, the state diagram de-asserts RX_DV, preventing the end-of-packet bits from reaching the MII. At any time that RX_DV is de-asserted, RXD<3:0> shall be all zeroes.

The decode operation shall use the 8B6T code table listed in Annex 23A, and the error-detecting rules listed in 23.2.1.3.1. Decoding and maintenance of the cumulative weight bit is performed separately for each receive pair.

23.2.1.3.1 Error-detecting rules

The decoding operation checks the dc balance on each receive pair by keeping track of the cumulative weight of all 6T code group received on that pair. For each pair, initialize the cumulative weight to 0 when the PCS Receive function is in the AWAITING INPUT state. As in the encoding operation, only one bit per pair is needed to store the cumulative weight.

Before decoding each octet, check the weight of the incoming code group and then apply rules a) through h) in sequence:

a) If the received code group is eop1 (or its negation), set eop=ON. Then check the other pairs for conformance to the end-of-packet rules as follows: Check the last four ternary symbols of the next pair, and the last two ternary symbols from the third pair for exact conformance with the end-of-packet pattern specified by PCS Transmit, including the cumulative weight negation rules. If the received data does not conform, set the internal variable eop_error=ON. Skip the other rules.
b) If the received code group weight is greater than 1 or less than –1, set the internal variable dc_balance_error=ON. Decode to all zeros. Do not change the cumulative weight.
c) If the received code group weight is zero, use the code table to decode. Do not change the cumulative weight.
d) If the received code group weight is +1, and the cumulative weight bit is 0, use the code table to decode. Invert the cumulative weight bit.
e) If the received code group weight is –1, and the cumulative weight bit is 1, algebraically negate each ternary symbol in the code group and then use the code table to decode. Invert the cumulative weight bit.
f) If the received code group weight is +1 and the cumulative weight bit is 1, set the internal variable dc_balance_error=ON. Decode to all zeros. Do not change the cumulative weight.
g) If the received code group weight is –1 and the cumulative weight bit is 0, set the internal variable dc_balance_error=ON. Decode to all zeros. Do not change the cumulative weight.

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h) If the (possibly negated) code group is not found in the code table, set codeword_error =ON. Decode to all zeros. Do not change the cumulative weight.

The variables dc_balance_error, eop_error and codeword_error shall remain OFF at all times other than those specified in the above error-detecting rules.

The codeword_error=ON indication for a (possibly negated) code group not found in the code table shall set RX_ER during the transfer of both affected data nibbles across the MII.

The dc_balance_error=ON indication for a code group shall set RX_ER during the transfer of both affected data nibbles across the MII.

The eop_error=ON indication shall set RX_ER during the transfer of the last decoded data nibble of the previous octet across the MII. That is at least one RX_CLK period earlier than the requirement for codeword_error and dc_balance_error.

These timing requirements imply consideration of implementation delays not specified in the PCS Receive state diagram.

RX_DV is asserted coincident with the transmission across the MII of valid packet data, including the Clause 4 MAC SFD, but not including the 100BASE-T4 end-of-packet delimiters eop1-5. When a packet is truncated due to early de-assertion of carrier_status, an RX_ER indication shall be generated and RX_DV shall be de-asserted, halting receive processing. The PCS Receive Function may use any of the existing signals codeword_error, dc_balance_error, or eop_error to accomplish this function.

23.2.1.4 PCS Error Sense function

The PCS Error Sense function performs the task of sending RX_ER to the MII whenever rxerror_status=ERROR is received from the PMA sublayer or when any of the PCS decoding error conditions occur. The PCS Error Sense function shall conform to the PCS Error Sense state diagram in Figure 23–10.

Upon detection of any error, the error sense process shall report RX_ER to the MII before the last nibble of the Clause 4 MAC frame has been passed across the MII. Errors attributable to a particular octet are reported to the MII coincident with the octet in which they occurred.

The timing of rxerror_status shall cause RX_ER to appear on the MII no later than the last nibble of the first data octet in the frame.

23.2.1.5 PCS Carrier Sense function

The PCS Carrier Sense function shall perform the function of controlling the MII signal CRS according to the rules presented in this clause.

While link_status = OK, CRS is asserted whenever rx_crs=ON or TX_EN=1, with timing as specified in 23.11.2, and Table 23-6.

23.2.1.6 PCS Collision Presence function

A PCS collision is defined as the simultaneous occurrence of tx_code_vector≠IDLE and the assertion of carrier_status=ON while link_status=OK. While a PCS collision is detected, the MII signal COL shall be asserted, with timing as specified in 23.11.2 and Table 23–7.

At other times COL shall remain de-asserted.

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23.2.2 PCS interfaces

23.2.2.1 PCS–MII interface signals

The following signals are formally defined in 22.2.2. Jabber detection as specified in 22.2.4.2.12 is not required by this standard.

Table 23–1—MII interface signals

Signal name	Meaning
TX_CLK	Transmit Clock
TXD<3:0>	Transmit Data
TX_ER	Forces transmission of illegal code
TX_EN	Frames Transmit Data
COL	Collision Indication
CRS	Non-Idle Medium Indication
RX_CLK	Receive Clock
RXD<3:0>	Receive Data
RX_DV	Frames Receive SFD and DATA
RX_ER	Receive Error Indication
MDC	Management Data Clock
MDIO	Management Data

23.2.2.2 PCS–Management entity signals

The management interface has pervasive connections to all functions. Operation of the management control lines MDC and MDIO, and requirements for managed objects inside the PCS and PMA, are specified in Clauses 22 and 30, respectively.

The loopback mode of operation shall be implemented in accordance with 22.2.4.1.2. The loopback mode of operation loops back transmit data to receive data, thus providing a way to check for the presence of a PHY.

No spurious signals shall be emitted onto the MDI when the PHY is held in power-down mode as defined in 22.2.4.1.5 (even if TX_EN is ON) or when released from power-down mode, or when external power is first applied to the PHY.

23.2.3 Frame structure

Frames passed from the PCS sublayer to the PMA sublayer shall have the structure shown in Figure 23–6. This figure shows how ternary symbols on the various pairs are synchronized as they are passed by the PMA_UNITDATA.indicate and PMA_UNITDATA.request messages. Time proceeds from left to right in the figure.

In the frame structure example, the last 6T code group, DATA N, happens to appear on transmit pair BI_D3. It could have appeared on any of the three transmit pairs, with the five words eop1 through eop5 appended afterward as the next five octets in sequence. The end of packet as recognized by the PCS is defined as the end of the last ternary symbol of eop1. At this point a receiver has gathered enough information to locate the last word in the packet and check the dc balance on each pair.

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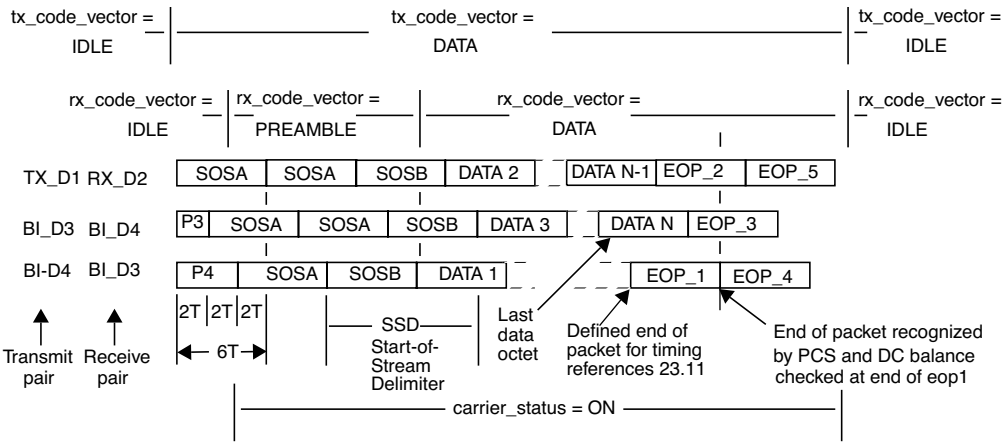


Figure 23–6—PCS sublayer to PMA sublayer frame structure

If the PMA service interface is exposed, data carried between PCS and PMA by the PMA_UNITDATA.indicate and PMA_UNITDATA.request messages shall have a clock in each direction. Details of the clock implementation are left to the implementor. The choice of binary encoding for each ternary symbol is left to the implementor.

The following frame elements appear in Figure 23–6 (ternary symbols are transmitted leftmost first):

SOSA	The succession of six ternary symbols: `[ 1 -1 1 -1 1 -1]`, which is the result of encoding the constant sosa.
SOSB	The succession of six ternary symbols: `[ 1 -1 1 -1 -1 1]`, which is the result of encoding the constant sosb.
P3	The succession of two ternary symbols: `[ 1 -1]`.
P4	The succession of four ternary symbols: `[ 1 -1 1 -1]`.
DATA	A 6T code group that is the result of encoding a data octet in a packet that is not part of the Clause 4 MAC preamble or SFD.
EOP1-5	A 6T code group that is the result of encoding one of the end-of-packet patterns eop1-5.

23.2.4 PCS state diagrams

The notation used in the state diagrams follows the conventions of 21.5. Transitions shown without source states are evaluated continuously and take immediate precedence over all other conditions.

23.2.4.1 PCS state diagram constants

Register tsr may take on any of the nine constant values listed below (sosa through eop5, bad_code, and zero_code). These values are used to describe the functional operation of the coding process.

NOTE—Implementors are under no obligation to implement these constants in any particular way. For example, some implementors may choose to implement these codes as special flag bits attached to MII TXD nibble registers. Other implementors may choose to implement insertion of these codes on the downstream side of the coder function, using precoded 6T sequences.

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All 6T code words are sent leftmost ternary symbol first.

sosa	A constant that encodes to:	[1 -1 1 -1 1 -1].
sosb	A constant that encodes to:	[1 -1 1 -1 -1 1].
eop1	A constant that encodes to:	[1 1 1 1 1 1].
eop2	A constant that encodes to:	[1 1 1 1 -1 -1].
eop3	A constant that encodes to:	[1 1 -1 -1 0 0].
eop4	A constant that encodes to:	[-1 -1 -1 -1 -1 -1].
eop5	A constant that encodes to:	[-1 -1 0 0 0 0].
bad_code	A constant that encodes to:	[-1 -1 -1 1 1 1].
zero_code	A constant that encodes to:	[0 0 0 0 0 0].

23.2.4.2 PCS state diagram variables

codeword_error

Indicates reception of invalid 6T code group.

Values: ON and OFF

Set by: PCS Receive; error-detecting rules

dc_balance_error

Indicates reception of dc coding violation.

Values: ON and OFF

Set by: PCS Receive; error-detecting rules

eop

Indicates reception of eop1.

A state variable set by the decoding operation. Reset to OFF when in PCS Receive state AWAITING INPUT. When the decoder detects eop1 on any pair, it sets this flag ON. The timing of eop shall be adjusted such that the last nibble of the last decoded data octet in a packet is the last nibble sent across the MII by the PMA Receive state diagram with RX_DV set ON.

Values: ON and OFF

Set by: PCS Receive; error-detecting rules

eop_error

Indicates reception of data with improper end-of-packet coding.

Values: ON and OFF

Set by: PCS Receive; error-detecting rules

ih2, ih4, and ih3 (input holding registers)

A set of holding registers used for the purpose of holding decoded data octets in preparation for sending across the MII one nibble at a time. One register is provided for each of the three receive pairs RX_D2, BI_D4, and BI_D3, respectively.

Value: octet

Set by: PCS Receive

Each time the PCS Receive function decodes a 6T code group, it loads the result (an octet) into one of the ih2-4 registers. These three registers are loaded in round-robin fashion, one register being loaded every two ternary symbol times.

The PCS Receive state diagram reads nibbles as needed from the ih2-4 registers and stuffs them

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into RXD.

ohr1, ohr3, and ohr4 (output holding registers)

(See Figure 23–7.) A set of shift registers used for the purpose of transferring coded 6T ternary symbol groups one ternary symbol at a time into the PMA. One register is provided for each of the three transmit pairs TX_D1, BI_D3, and BI_D4, respectively.

Value: 6T code group. Each of the six cells holds one ternary symbol (i.e., –1, 0, or 1).

Set by: PCS Transmit

Each time the PCS Transmit function encodes a data octet, it loads the result (a 6T code group) into one of the ohr registers. Three registers are loaded in round-robin fashion, one register being loaded every two ternary symbol times. The PCS shall transmit octets on the three transmit pairs in round-robin fashion, in the order TX_D1, BI_D3, and BI_D4, starting with TX_D1.

The PMA_UNITDATA.request (DATA) message picks the least significant (rightmost) ternary symbol from each ohr register and sends it to the PMA, as shown below. (Note that 6T code words in Annex 23A are listed with lsb on the left, not the right.)

tx_code_vector[TX_D1] = the LSB of ohr1, also called ohr1[0]

tx_code_vector[BI_D3] = the LSB of ohr3, also called ohr3[0]

tx_code_vector[BI_D4] = the LSB of ohr4, also called ohr4[0]

After each PMA_UNITDATA.request message, all three ohr registers shift right by one ternary symbol, shifting in zero from the left. The PCS Transmit function loads a new 6T code group into each ohr immediately after the last ternary symbol of the previous group is shifted out.

At the beginning of a preamble, the PCS Transmit function loads the same value (sosa) into all three output holding registers, which causes alternating transitions to immediately appear on all three output pairs. The result on pairs BI_D3 and BI_D4 is depicted by code words P3 and P4 in Figure 23–6.

pcs_reset

Causes reset of all PCS functions when ON.

Values: ON and OFF

Set by: PCS Reset

rx_crs

A latched asynchronous variable. Timing for the MII signal CRS is derived from rx_crs.

Values: ON and OFF

Set ON when: carrier_status changes to ON

Set OFF when: either of two events occurs:
carrier_status changes to OFF, or
detection of eop1, properly framed, on any of the lines RX_D2, BI_D4, or BI_D3

Additionally, if, 20 ternary symbol times after rx_crs falls, carrier_status remains set to ON then set rx_crs=ON.

NOTE—A special circuit for the detection of eop1 and subsequent de-assertion of rx_crs, faster than the full 8B6T decoding circuits, is generally required to meet the timing requirements for CRS listed in 23.11.

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tsr (transmit shift register)

(See Figure 23–7.) A shift register defined for the purpose of assembling nibbles from the MII TXD into octets.

Values: The variable tsr always contains both the current nibble of TXD and the previous nibble of TXD. Valid values for tsr therefore include all octets. Register tsr may also take on any of the nine constant values listed in 23.2.4.1.

Nibble order: When encoding the tsr octet, the previous TXD nibble is considered the least significant nibble.

Set by: PCS Transmit

During the first 16 TX_CLK cycles after TX_EN is asserted, tsr shall assume the following values in sequence regardless of TXD: sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosb, sosb, sosb, sosb, sosb, sosb. This action substitutes the 100BASE-T4 preamble for the Clause 4 MAC preamble. The PCS Transmit state diagram samples the tsr only every other clock, which reduces the number of sosa and sosb constants actually coded to 5 and 3, respectively.

During the first 10 TX_CLK cycles after TX_EN is de-asserted, tsr shall assume the following values in sequence, regardless of TXD: eop1, eop1, eop2, eop2, eop3, eop3, eop4, eop4, eop5, eop5. This action appends the 100BASE-T4 end-of-packet delimiter to each pair. The PCS Transmit state diagram samples the tsr only every other clock, which reduces the number of eop1-5 constants actually coded to 1 each.

Except for the first 16 TX_CLK cycles after TX_EN is asserted, any time TX_ER and TX_EN are asserted, tsr shall assume the value bad_code with such timing as to cause both nibbles of the affected octet to be encoded as bad_code. If TX_ER is asserted at any time during the first 16 TX_CLK cycles after TX_EN is asserted, tsr shall during the 17th and 18th clock cycles assume the value bad_code.

If TX_EN is de-asserted on an odd nibble boundary, the PCS shall extend TX_EN by one TX_CLK cycle, and behave as if TX_ER were asserted during that additional cycle.

Except for the first 10 TX_CLK cycles after TX_EN is de-asserted, any time TX_EN is not asserted, tsr shall assume the value zero_code.

tx_extend

A latched, asynchronous state variable used to extend the TX_EN signal long enough to ensure complete transmission of all nonzero ternary symbols in eop1-5.

Values: ON and OFF

Set ON upon: rising edge of TX_EN

Set OFF upon: either of two conditions:
a) In the event of a collision (COL is asserted at any time during transmission) set tx_extend=OFF when TX_EN de-asserts.
b) In the event of no collision (COL remains de-asserted throughout transmission) set tx_extend=OFF upon completion of transmission of last ternary symbol in eop4.

NOTE 1—The 6T code group eop5 has four zeroes at the end. The 6T code group eop4 contains the last nonzero ternary symbol to be transmitted.

NOTE 2—The effect of a collision, if present, is to truncate the frame at the original boundary determined by TX_EN. Noncolliding frames are extended, while colliding frames are not.

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23.2.4.3 PCS state diagram timer

tw1_timer

A continuous free-running timer.

Values: The condition tw1_timer_done goes true when the timer expires.

Restart when: Immediately after expiration (restarting the timer resets condition tw1_timer_done).

Duration: 40 ns nominal.

TX_CLK shall be generated synchronous to tw1_timer (see tolerance required for TX_CLK in 23.5.1.2.10).

On every occurrence of tw1_timer_done, the state diagram advances by one block. The message PMA_UNITDATA.request is issued concurrent with tw1_timer_done.

23.2.4.4 PCS state diagram functions

encode()

The encode operation of 23.2.1.2.

Argument: octet

Returns: 6T code group

decode()

The decode operation of 23.2.1.3.

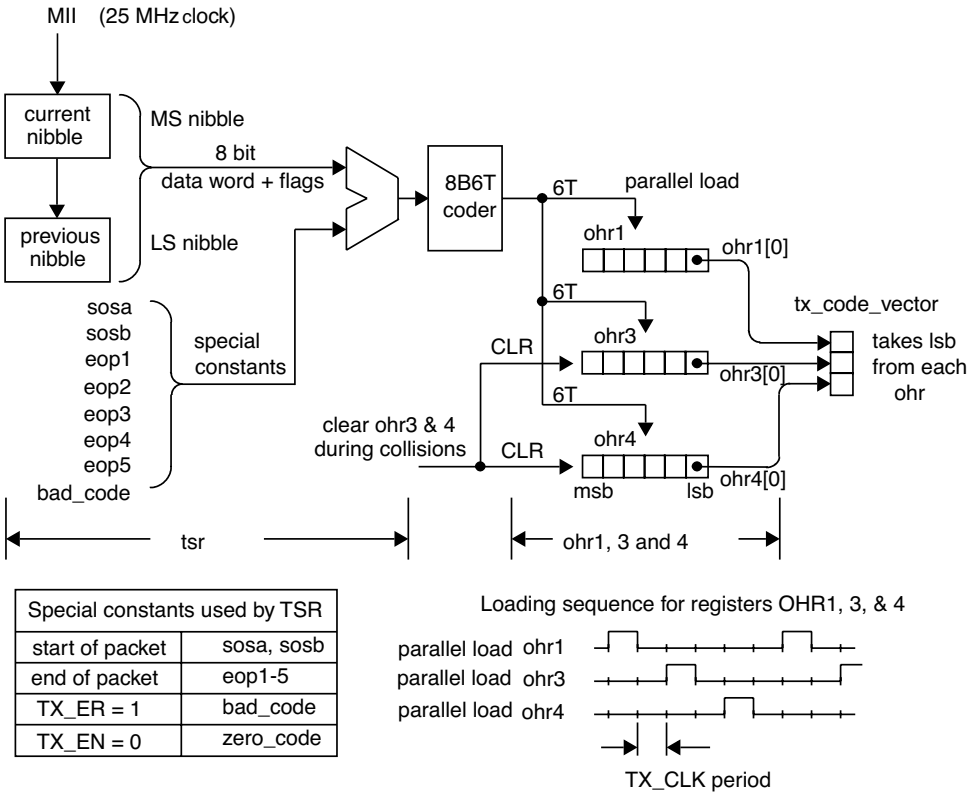
Argument: 6T code group

Returns: octet

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Special constants used by TSR	
start of packet	sosa, sosb
end of packet	eop1-5
TX_ER = 1	bad_code
TX_EN = 0	zero_code

Figure 23–7—PCS Transmit reference diagram

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23.2.4.5 PCS state diagrams

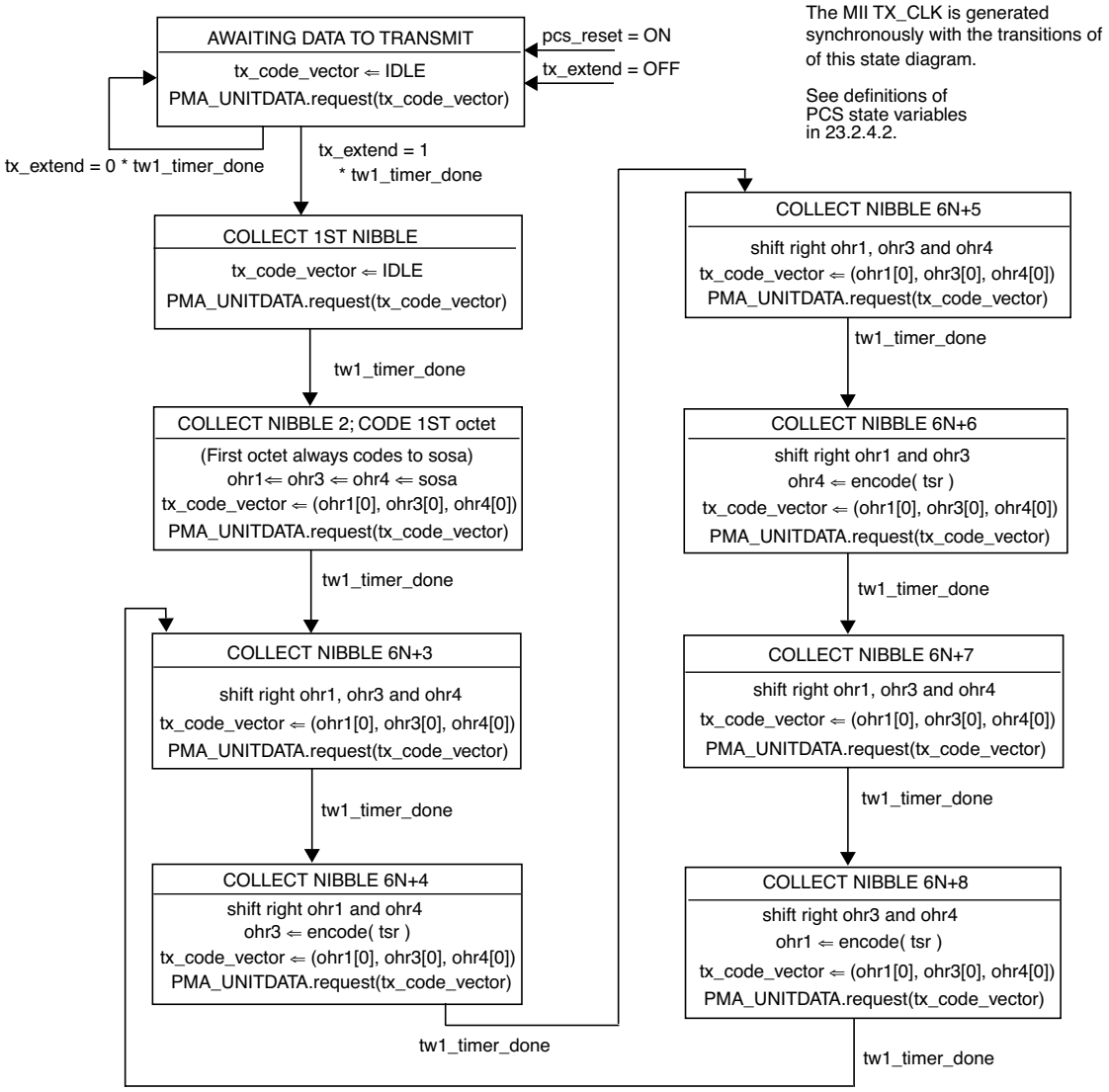


Figure 23–8—PCS Transmit state diagram

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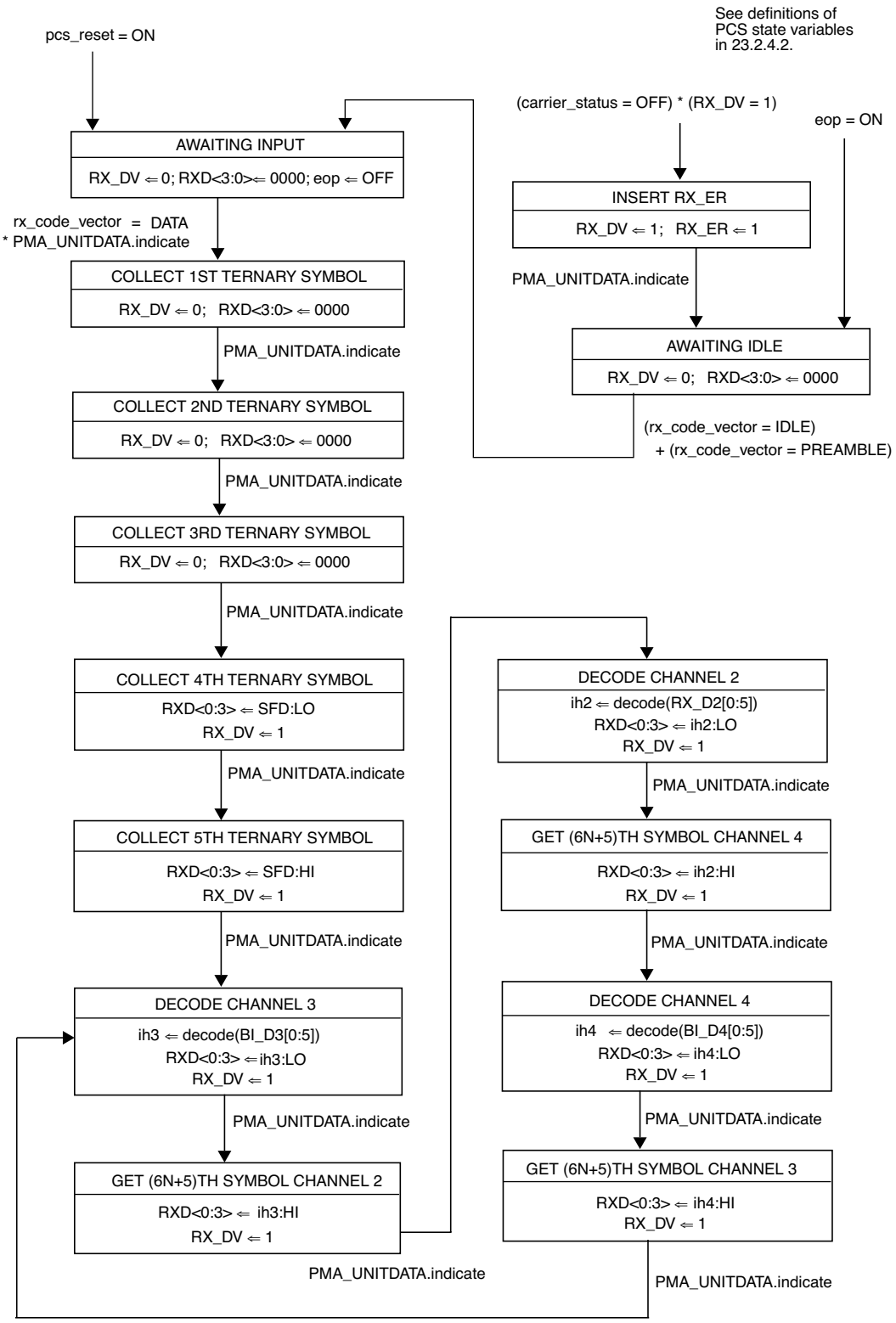


Figure 23–9—PCS Receive state diagram

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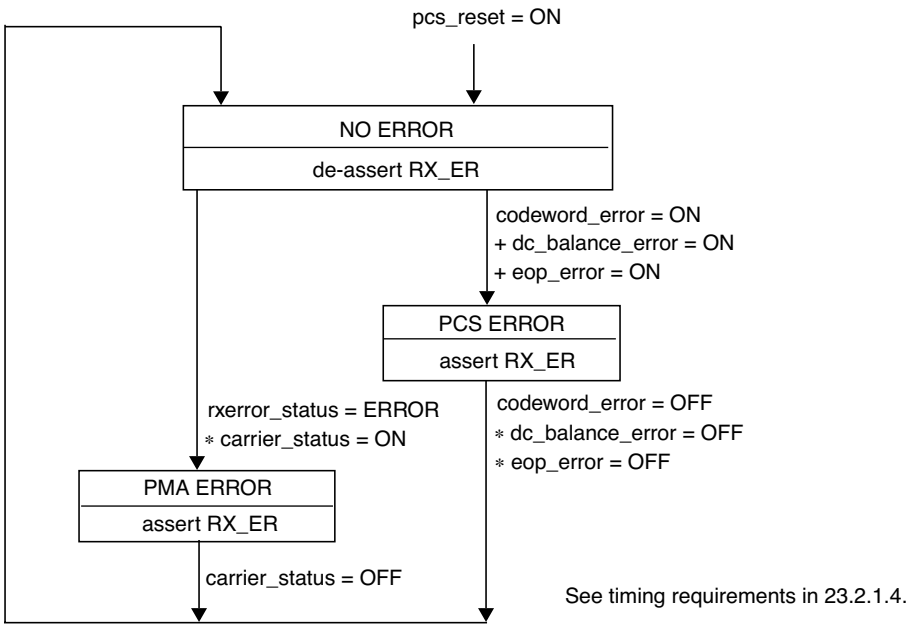


Figure 23–10—PCS Error Sense state diagram

23.2.5 PCS electrical specifications

The interface between PCS and PMA is an abstract message-passing interface, having no specified electrical properties.

Electrical characteristics of the signals passing between the PCS and MII may be found in Clause 22.

23.3 PMA service interface

This clause specifies the services provided by the PMA to either the PCS or a Repeater client. These services are described in an abstract manner and do not imply any particular implementation.

The PMA Service Interface supports the exchange of code vectors between the PMA and its client (either the PCS or a Repeater). The PMA also generates status indications for use by the client.

The following primitives are defined:

PMA_TYPE.indicate
PMA_UNITDATA.request
PMA_UNITDATA.indicate
PMA_CARRIER.indicate
PMA_LINK.indicate
PMA_LINK.request
PMA_RXERROR.indicate

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23.3.1 PMA_TYPE.indicate

This primitive is generated by the PMA to indicate the nature of the PMA instantiation. The purpose of this primitive is to allow clients to support connections to the various types of 100BASE-T PMA entities in a generalized manner.

23.3.1.1 Semantics of the service primitive

PMA_TYPE.indicate (pma_type)

The pma_type parameter for use with the 100BASE-T4 PMA is T4.

23.3.1.2 When generated

The PMA shall continuously generate this primitive to indicate the value of pma_type.

23.3.1.3 Effect of receipt

The client uses the value of pma_type to define the semantics of the PMA_UNITDATA.request and PMA_UNITDATA.indicate primitives.

23.3.2 PMA_UNITDATA.request

This primitive defines the transfer of data (in the form of tx_code_vector parameters) from the PCS or repeater to the PMA.

23.3.2.1 Semantics of the service primitive

PMA_UNITDATA.request (tx_code_vector)

When transmitting data using 100BASE-T4 signaling, the PMA_UNITDATA.request conveys to the PMA simultaneously the logical output value for each of the three transmit pairs TX_D1, BI_D3, and BI_D4. The value of tx_code_vector during data transmission is therefore a three-element vector, with one element corresponding to each output pair. Each of the three elements of the tx_code_vector may take on one of three logical values: 1, 0, or –1, corresponding to the three ternary possibilities +, 0, and - listed for each ternary symbol in the 8B6T code table (see Annex 23A).

Between packets, the 100BASE-T4 PMA layer sends the 100BASE-T4 idle signal, TP_IDL_100. The PCS informs the PMA layer that it is between packets, thus enabling the PMA idle signal, by setting the tx_code_vector parameter to IDLE.

For pma_type 100BASE-T4, the tx_code_vector parameter can take on either of two forms:

IDLE	A single value indicating to the PMA that there is no data to convey. The PMA generates link integrity pulses during the time that tx_code_vector = IDLE.
DATA	A vector of three ternary symbols, one for each of the three transmit pairs TX_D1, BI_D3, and BI_D4. The ternary symbol for each pair may take on one of three values, 1, 0, or –1.

The ternary symbols comprising tx_code_vector, when they are conveyed using the DATA format, are called, according to the pair on which each will be transmitted, tx_code_vector[BI_D4], tx_code_vector[TX_D1], and tx_code_vector[BI_D3].

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23.3.2.2 When generated

The PCS or Repeater client generates PMA_UNITDATA.request synchronous with every MII TX_CLK.

For the purposes of state diagram descriptions, it may be assumed that at the time PMA_UNITDATA.request is generated, the MII signals TX_EN, and TX_ER, and TXD instantly become valid and that they retain their values until the next PMA_UNITDATA.request.

In the state diagrams, PMA_UNITDATA.request is assumed to occur at the conclusion of each tw1 wait function.

23.3.2.3 Effect of receipt

Upon receipt of this primitive, the PMA transmits the indicated ternary symbols on the MDI.

23.3.3 PMA_UNITDATA.indicate

This primitive defines the transfer of data (in the form of rx_code_vector parameters) from the PMA to the PCS or repeater during the time that link_status=OK.

23.3.3.1 Semantics of the service primitive

PMA_UNITDATA.indicate (rx_code_vector)

When receiving data using 100BASE-T4 signaling, the PMA_UNITDATA.indicate conveys to the PCS simultaneously the logical input value for each of the three receive pairs RX_D2, BI_D4, and BI_D3. The value of rx_code_vector during data reception is therefore a three-element vector, with one element corresponding to each input pair. Each of the three elements of the rx_code_vector may take on one of three logical values: 1, 0, or –1, corresponding to the three ternary possibilities +, 0, and - listed for each ternary symbol in the 8B6T code table (see Annex 23A).

Between packets, the rx_code_vector is set by the PMA to the value IDLE.

From the time the PMA asserts carrier_status=ON until the PMA recognizes the SSD pattern (not all of the pattern need be received in order for the PMA to recognize the pattern), the PMA sets rx_code_vector to the value PREAMBLE.

For pma_type 100BASE-T4, the rx_code_vector parameter can take on any of three forms:

IDLE	A single value indicating that the PMA has no data to convey.
PREAMBLE	A single value indicating that the PMA has detected carrier, but has not received a valid SSD.
DATA	A vector of three ternary symbols, one for each of the three receive pairs RX_D2, BI_D3, and BI_D4. The ternary symbol for each pair may take on one of three values, 1, 0, or –1.

The ternary symbols comprising rx_code_vector, when they are conveyed using the DATA format, are called, according to the pair upon which each symbol was received, rx_code_vector[BI_D3], rx_code_vector[RX_D2], and rx_code_vector[BI_D4].

23.3.3.2 When generated

The PMA shall generate PMA_UNITDATA.indicate (DATA) messages synchronous with data received at the MDI.

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23.3.3.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

23.3.4 PMA_CARRIER.indicate

This primitive is generated by the PMA to indicate the status of the signal being received from the MDI. The purpose of this primitive is to give the PCS or repeater client the earliest reliable indication of activity on the underlying medium.

23.3.4.1 Semantics of the service primitive

PMA_CARRIER.indicate (carrier_status)

The carrier_status parameter can take on one of two values: OFF or ON, indicating whether the incoming signal should be interpreted as being between packets (OFF) or as a packet in progress (ON).

23.3.4.2 When generated

The PMA shall generate this primitive to indicate the value of carrier_status.

23.3.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

23.3.5 PMA_LINK.indicate

This primitive is generated by the PMA to indicate the status of the underlying medium. The purpose of this primitive is to give the PCS or repeater client or Auto-Negotiation algorithm a means of determining the validity of received code elements.

23.3.5.1 Semantics of the service primitive

PMA_LINK.indicate (link_status)

The link_status parameter can take on one of three values: FAIL, READY, or OK:

FAIL	The link integrity function does not detect a valid 100BASE-T4 link.
READY	The link integrity function detects a valid 100BASE-T4 link, but has not been enabled by Auto-Negotiation.
OK	The 100BASE-T4 link integrity function detects a valid 100BASE-T4 link, and has been enabled by Auto-Negotiation.

23.3.5.2 When generated

The PMA shall generate this primitive to indicate the value of link_status.

23.3.5.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

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23.3.6 PMA_LINK.request

This primitive is generated by the Auto-Negotiation algorithm. The purpose of this primitive is to allow the Auto-Negotiation algorithm to enable and disable operation of the PHY.

23.3.6.1 Semantics of the service primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

SCAN_FOR_CARRIER	Used by the Auto-Negotiation algorithm prior to receiving any fast link pulses. During this mode the PHY reports link_status=READY if it recognizes 100BASE-T4 carrier from the far end, but no other actions are enabled.
DISABLE	Used by the Auto-Negotiation algorithm to disable PHY processing in the event fast link pulses are detected. This gives the Auto-Negotiation algorithm a chance to determine how to configure the link.
ENABLE	Used by Auto-Negotiation to turn control over to the PHY for data processing functions. This is the default mode if Auto-Negotiation is not present.

23.3.6.2 Default value of parameter link_control

Upon power-on, reset, or release from power-down, the link_control parameter shall revert to ENABLE. If the optional Auto-Negotiation algorithm is not implemented, no PMA_LINK.request message will arrive and the PHY will operate indefinitely with link_control=ENABLE.

23.3.6.3 When generated

The Auto-Negotiation algorithm generates this primitive to indicate to the PHY how to behave.

Upon power-on, reset, or release from power down, the Auto-Negotiation algorithm, if present, issues the message PMA_LINK.request (SCAN_FOR_CARRIER).

23.3.6.4 Effect of receipt

Whenever link_control=SCAN_FOR_CARRIER, the PHY shall enable the Link Integrity state diagram, but block passage into the state LINK_PASS, while holding rcv=DISABLE, and xmit=DISABLE. While link_control=SCAN_FOR_CARRIER, the PHY shall report link_status=READY if it recognizes 100BASE-T4 link integrity pulses coming from the far end, otherwise it reports link_status=FAIL.

Whenever link_control=DISABLE, the PHY shall report link_status=FAIL and hold the Link Integrity state diagram in the RESET state, while holding rcv=disable and xmit=DISABLE.

While link_control=ENABLE, the PHY shall allow the Link Integrity function to determine if the link is available and, if so, set rcv=ENABLE and xmit=ENABLE.

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23.3.7 PMA_RXERROR.indicate

The primitive is generated in the PMA by the PMA Align function to indicate the status of the signal being received from the MDI. The purpose of this primitive is to give the PCS or repeater client an indication of a PMA detectable receive error.

23.3.7.1 Semantics of the service primitive

PMA_RXERROR.indicate (rxerror_status)

The rxerror_status parameter can take on one of two values: ERROR or NO_ERROR, indicating whether the incoming signal contains a detectable error (ERROR) or not (NO_ERROR).

23.3.7.2 When generated

The PMA shall generate this primitive to indicate whether or not each incoming packet contains a PMA detectable error (23.2.1.4).

23.3.7.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

23.4 PMA functional specifications

The PMA couples messages from a PMA service interface (23.3) to the 100BASE-T4 baseband medium (23.6).

The interface between PCS and the baseband medium is the Medium Dependent Interface (MDI), specified in 23.7.

23.4.1 PMA functions

The PMA sublayer comprises one PMA Reset function and six simultaneous and asynchronous operating functions. The PMA operating functions are PMA Transmit, PMA Receive, PMA Carrier Sense, Link Integrity, PMA Align, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function. When the PMA is used in conjunction with a PCS, the RESET function may be shared between layers.

The PMA reference diagram, Figure 23–11, shows how the operating functions relate to the messages of the PMA Service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive, and are not shown in Figure 23–11. The Management Interface and its functions are specified in Clause 22.

23.4.1.1 PMA Reset function

The PMA Reset function shall be executed any time either of two conditions occur. These two conditions are power-on and the receipt of a reset request from the management entity. The PMA Reset function initializes all PMA functions. The PMA Reset function sets pma_reset=ON for the duration of its reset function. All state diagrams take the open-ended pma_reset branch upon execution of the PMA Reset function. The reference diagrams do not explicitly show the PMA Reset function.

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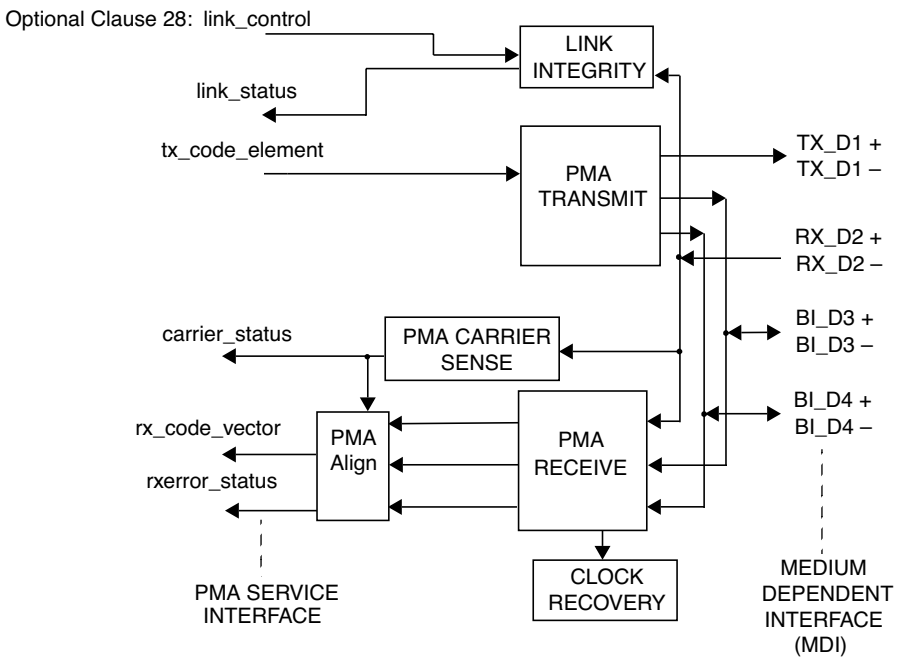


Figure 23–11—PMA reference diagram

23.4.1.2 PMA Transmit function

Except as provided for in the next paragraph, whenever (tx_code_vector=DATA)×(pma_carrier=OFF), the PMA shall transmit onto the MDI ternary symbols on pairs TX_D1, BI_D3, and BI_D4 equal to tx_code_vector[TX_D1], tx_code_vector[BI_D3], and tx_code_vector[BI_D4], respectively.

Whenever (tx_code_vector=DATA)×(pma_carrier=ON), the PMA shall transmit onto the MDI ternary symbols on pairs TX_D1, BI_D3, and BI_D4 equal to tx_code_vector[TX_D1], CS0, and CS0, respectively, and continue doing so until tx_code_vector=IDLE.

NOTE—This shuts off the transmitters on channels BI_D3 and BI_D4, and keeps them off, in the event of a collision. Shutting off the transmitters prevents overload and saturation of the transmitters, and also reduces the amount of near-end crosstalk present while monitoring for the end of carrier.

Whenever tx_code_vector=IDLE, an idle signal shall be transmitted on pair TX_D1 and silence on pairs BI_D3 and BI_D4. The idle signal consists of periods of silence (times where the differential output voltage remains at 0 mV ± 50 mV) broken by the transmission of link integrity test pulses.

The 100BASE-T4 idle signal is similar to the 10BASE-T idle signal, but with 100BASE-T4 ternary signal levels and a faster repetition rate. The 100BASE-T4 idle signal is called TP_IDL_100. The TP_IDL_100 signal shall be a repeating sequence formed from one 1.2 ms ± 0.6 ms period of silence (the time where the differential voltage remains at 0 mV ± 50 mV) and one link test pulse. Each link test pulse shall be a succession of two ternary symbols having logical values of –1 and 1 transmitted on pair TX_D1 using CS-1 and CS1 as defined in 23.4.3.1. Following a packet, the TP_IDL_100 shall start with a period of silence.

Transmission of TP_IDL_100 may be terminated at any time with respect to the link test pulse. It shall be terminated such that ternary symbols of the subsequent packet are not corrupted, and are not delayed any more than is specified in 23.11.

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For any link test pulse occurring within 20 ternary symbol times of the beginning of a preamble, the zero crossing jitter (as defined in 23.5.1.2.5) of the link test pulse when measured along with the zero crossings of the preamble shall be less than 4 ns p-p.

NOTE—The above condition allows clock recovery implementations that optionally begin fast-lock sequences on part of a link integrity pulse to properly acquire lock on a subsequent preamble sequence.

Regardless of other considerations, when the transmitter is disabled (xmit=DISABLE), the PMA Transmit function shall transmit the TP_IDL_100 signal.

23.4.1.3 PMA Receive function

PMA Receive contains the circuits necessary to convert physically encoded ternary symbols from the physical MDI receive pairs (RX_D2, BI_D3 and BI_D4) into a logical format suitable for the PMA Align function. Each receive pair has its own dedicated PMA Receive circuitry.

The PHY shall receive the signals on the receive pairs (RX_D2, BI_D3, and BI_D4) and translate them into one of the PMA_UNITDATA.indicate parameters IDLE, PREAMBLE, or DATA with a ternary symbol error rate of less than one part in 10^8.

If both pma_carrier=ON and tx_code_vector=DATA, the value of rx_code_vector is unspecified until pma_carrier=OFF.

23.4.1.4 PMA Carrier Sense function

The PMA Carrier Sense function shall set pma_carrier=ON upon reception of the following pattern on pair RX_D2 at the receiving MDI, as measured using a 100BASE-T4 transmit test filter (23.5.1.2.3):

> Any signal greater than 467 mV, followed by any signal less than –225 mV, followed by any signal greater than 467 mV, all three events occurring within 2 ternary symbol times.

The operation of carrier sense is undefined for signal amplitudes greater than 4.5 V.

See 23.5.1.3.2 for a list of signals defined *not* to set pma_carrier=ON.

After asserting pma_carrier=ON, PMA Carrier Sense shall set pma_carrier=OFF upon receiving either of these conditions:

a) Seven consecutive ternary symbols of value CS0 on pair RX_D2.
b) (tx_code_vector=DATA) has not been true at any time since pma_carrier was asserted, *and* the 6T code group eop1 has been received, properly framed, on any of the lines RX_D2, BI_D4, or BI_D3, *and* enough time has passed to assure passage of all ternary symbols of eop4 across the PMA service interface.

NOTE—Designers may wish to take advantage of the fact that the minimum received packet fragment will include at least 24 ternary symbols of data on pair RX_D2. Therefore, once carrier is activated, it is not necessary to begin searching for seven consecutive zeroes until after the 24th ternary symbol has been received. During the time that the first 24 ternary symbols are being received, the near-end crosstalk from pairs BI_D3 and BI_D4, which are switched off during collisions, decays substantially.

While rcv=ENABLE, the PMA CARRIER function shall set carrier_status = pma_carrier.

While rcv≠ENABLE, the PMA CARRIER function shall set carrier_status = OFF.

This function operates independently of the Link Integrity function.

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23.4.1.5 Link Integrity function

Link Integrity provides the ability to protect the network from the consequences of failure of the simplex link attached to RX_D2. While such a failure is present, transfer of data by the Transmit and Receive functions is disabled.

Link Integrity observes the incoming wire pair, RX_D2, to determine whether the device connected to the far end is of type 100BASE-T4. Based on its observations, Link Integrity sets two important internal variables:

a) pma_type variable is set to 100BASE-T4.
b) link_status variable is a parameter sent across the PMA Service interface.

The Link Integrity function shall comply with the state diagram of Figure 23–12.

Four conditions gate the progression of states toward LINK_PASS: (1) reception of at least 31 link integrity test pulses; (2) reception of at least 96 more link integrity test pulses, or reception of carrier; (3) cessation of carrier, if it was present; (4) detection of equals link_control ENABLE.

While the PMA is not in the LINK_PASS state, the Link Integrity function sets rcv=DISABLE and xmit=DISABLE, thus disabling the bit transfer of the Transmit and Receive functions.

If a visible indicator is provided on the PHY to indicate the link status, it is recommended that the color be green and that the indicator be labeled appropriately. It is further recommended that the indicator be on when the PHY is in the LINK_PASS state and off otherwise.

23.4.1.6 PMA Align function

The PMA Align function accepts received ternary symbols from the PMA Receive function, along with pma_carrier. PMA Align is responsible for realigning the received ternary symbols to eliminate the effects of unequal pair propagation time, commonly called pair skew. PMA Align also looks for the SSD pattern to determine the proper alignment of 6T code groups, and then forwards PMA_UNITDATA.indicate (DATA) messages to the PCS. The SSD pattern includes referencing patterns on each of the three receive lines that may be used to establish the proper relationship of received ternary symbols (see Figure 23–6).

NOTE—The skew between lines is not expected to change measurably from packet to packet.

At the beginning of each received frame, the PMA Carrier Sense function asserts pma_carrier=ON. During the preamble, the Clock Recovery function begins synchronizing its receive clock. Until clock is synchronized, data coming from the low-level PMA Receive function is meaningless. The PMA Align function is responsible for waiting for the receiver clock to stabilize and then properly recognizing the 100BASE-T4 coded SSD pattern. The PMA Align function shall send PMA_UNITDATA.indicate (PREAMBLE) messages to the PCS from the time pma_carrier=ON is asserted until the PMA is ready to transfer the first PMA_UNITDATA.indicate (DATA) message. Once the PMA Align function locates a SSD pattern, it begins forwarding PMA_UNITDATA.indicate (DATA) messages to the PCS, starting with the first ternary symbol of the first data word on pair BI_D3, as defined in Figure 23–6. This first PMA_UNITDATA.indicate (DATA) message shall transfer the following ternary symbols, as specified in the frame structure diagram, Figure 23–6:

rx_code_vector[BI_D3]first ternary symbol of first data code group

rx_code_vector[RX_D2]second ternary symbol prior to start of second data code group

rx_code_vector[BI_D4]fourth ternary symbol prior to start of third data code group

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PMA Align shall continue sending PMA_UNITDATA.indicate (DATA) messages until pma_carrier=OFF. While pma_carrier=OFF, PMA Align shall emit PMA_UNITDATA.indicate (IDLE) messages.

If no valid SSD pattern is recognized within 22 ternary symbol times of the assertion of pma_carrier=ON, the PMA Align function shall set rxerror_status=ERROR. The PMA Align function is permitted to begin sending PMA_UNITDATA.indicate (DATA) messages upon receipt of a partially recognized SSD pattern, but it is required to set rxerror_status=ERROR if the complete SSD does not match perfectly the expected ternary symbol sequence. Rxerror_status shall be reset to NO_ERROR when pma_carrier=OFF.

The PMA Align function is permitted to use the first received packet of at least minimum size after RESET or the transition to LINK_PASS to learn the nominal skew between pairs, adjust its equalizer, or perform any other initiation functions. During this first packet, the PMA Align function shall emit PMA_UNITDATA.indicate (PREAMBLE) messages, but may optionally choose to never begin sending PMA_UNITDATA.indicate (DATA) messages.

The PMA Align function shall tolerate a maximum skew between any two pairs of 60 ns in either direction without error.

To protect the network against the consequences of mistaken packet framing, the PMA Align function shall detect the following error and report it by setting rxerror_status=ERROR (optionally, those error patterns already detected by codeword_error, dc_balance_error, or eop_error do not also have to be detected by rxerror_status): *In a series of good packets, any one packet that has been corrupted with three or fewer ternary symbols in error causing its sosb 6T code groups on one or more pairs to appear in the wrong location*.

Several approaches are available for meeting this requirement, including, but not limited to, a) comparing the relative positions of sosb 6T code groups on successive packets; b) measuring the time between the first preamble pulse and reception of sosb on each pair; c) counting the number of zero crossings from the beginning of the preamble until sosb; and d) monitoring for exception strings like “11” and “–1–1–1” in conjunction with one or more of the above techniques.

Regardless of other considerations, when the receive function is disabled (rcv=DISABLE), the PMA Align function shall emit PMA_UNITDATA.indicate (IDLE) messages and no others.

23.4.1.7 Clock Recovery function

The Clock Recovery function couples to all three receive pairs. It provides a synchronous clock for sampling each pair. While it may not drive the MII directly, the Clock Recovery function is the underlying root source of RX_CLK.

The Clock Recovery function shall provide a clock suitable for synchronously decoding ternary symbols on each line within the bit error tolerance provided in 23.4.1.3. During each preamble, in order to properly recognize the frame delimiting pattern formed by code word sosb on each pair, the received clock signal must be stable and ready for use in time to decode the following ternary symbols: the 16th ternary symbol of pair RX_D2, the 18th ternary symbol of pair BI_D4, and the 14th ternary symbol of pair BI_D3.

23.4.2 PMA interface messages

The messages between the PMA and PCS are defined above in 23.3, PMA Service Interface. Communication between a repeater unit and PMA also uses the PMA Service Interface. Communication through the MDI is summarized in Tables 23–2 and 23–3.

TP_IDL_100 is defined in 23.4.1.2. The waveforms used to convey CS1, CS0, and CS-1 are defined in 23.5.1.2.

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Table 23–2—MDI signals transmitted by the PHY

Signal	Allowed pair	Meaning
CS1	TX_D1, BI_D3 BI_D4	A waveform that conveys the ternary symbol 1. Nominal voltage level +3.5 V.
CS0	TX_D1, BI_D3 BI_D4	A waveform that conveys the ternary symbol 0. Nominal voltage level 0 V.
CS-1	TX_D1, BI_D3 BI_D4	A waveform that conveys the ternary symbol –1. Nominal voltage level –3.5 V.
TP_IDL_100	TX_D1	Idle signal. Indicates transmitter is currently operating at 100 Mb/s.

Table 23–3—Signals received at the MDI

Signal	Allowed pair	Meaning
CS1	RX_D2, BI_D3 BI_D4	A waveform that conveys the ternary symbol 1. Nominal transmitted voltage level +3.5 V.
CS0	RX_D2, BI_D3 BI_D4	A waveform that conveys the ternary symbol 0. Nominal transmitted voltage level 0 V.
CS-1	RX_D2, BI_D3 BI_D4	A waveform that conveys the ternary symbol –1. Nominal transmitted voltage level –3.5 V.
TP_IDL_100	RX_D2	Idle signal. Indicates transmitter is currently operating at 100 Mb/s.

TP_IDL_100 is defined in 23.4.1.2. The encodings for CS1, CS0, and CS-1 are defined in 23.5.1.2.

Re-timing of CS1, CS0, and CS-1 signals within the PMA is required.

23.4.3 PMA state diagrams

The notation used in the state diagrams follows the conventions of 21.5. Transitions shown without source states are evaluated continuously and take immediate precedence over all other conditions.

23.4.3.1 PMA constants

CS0

A waveform that conveys the ternary symbol 0.

Value: CS0 has a nominal voltage of 0 V. See 23.5.1.2.

CS1

A waveform that conveys the ternary symbol 1.

Value: CS1 has a nominal peak voltage of +3.5 V. See 23.5.1.2.

CS-1

A waveform that conveys the ternary symbol –1.

Value: CS-1 has a nominal peak voltage of –3.5 V. See 23.5.1.2.

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link_100_max

A constant.

Value: Greater than 5.0 ms and less than 7.0 ms.

Used by link_max_timer to detect the absence of 100BASE-T4 link test pulses on pair RX_D2.

link_100_min

A constant.

Value: Greater than 0.15 ms and less than 0.45 ms.

Used by cnt_link to detect link test pulses on pair RX_D2 that are too close together to be valid 100BASE-T4 link test pulses.

23.4.3.2 State diagram variables

pma_reset

Causes reset of all PCS functions.

Values: ON and OFF

Set by: PMA Reset

pma_carrier

A version of carrier_status used internally by the PMA sublayer. The variable pma_carrier always functions regardless of the link status. The value of pma_carrier is passed on through the PMA service interface as carrier_status when rcv=ENABLE. At other times, the passage of pma_carrier information to the PMA service interface is blocked.

Values: ON, OFF

Set by: PMA CARRIER

rcv

Controls the flow of data from the PMA to PCS through the PMA_UNITDATA.indicate message.

Values: ENABLE (receive is enabled)
DISABLE (the PMA always sends PMA_UNITDATA.indicate (IDLE), and carrier_status is set to OFF)

xmit

Controls the flow of data from PCS to PMA through the PMA_UNITDATA.request message.

Values: ENABLE (transmit is enabled)
DISABLE (the PMA interprets all PMA_UNITDATA.request messages as PMA_UNITDATA.request (IDLE). The PMA transmits no data, but continues sending TP_IDL_100).

23.4.3.3 State diagram timers

link_max_timer

A re-triggerable timer.

Values: The condition link_max_timer_done goes true when the timer expires.

Restart when: Timer is restarted for its full duration by every occurrence of either a link test pulse on pair RX_D2 or the assertion of pma_carrier=ON (restarting the timer resets the condition link_max_timer_done).

Duration: link_100_max

Used by Link Integrity to detect the absence of 100BASE-T4 link test pulses on pair RX_D2.

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23.4.3.4 State diagram counters

cnt_link

Counts number of 100BASE-T4 link test pulses (see 23.5.1.3.1) received on pair RX_D2.

Values: nonnegative integers

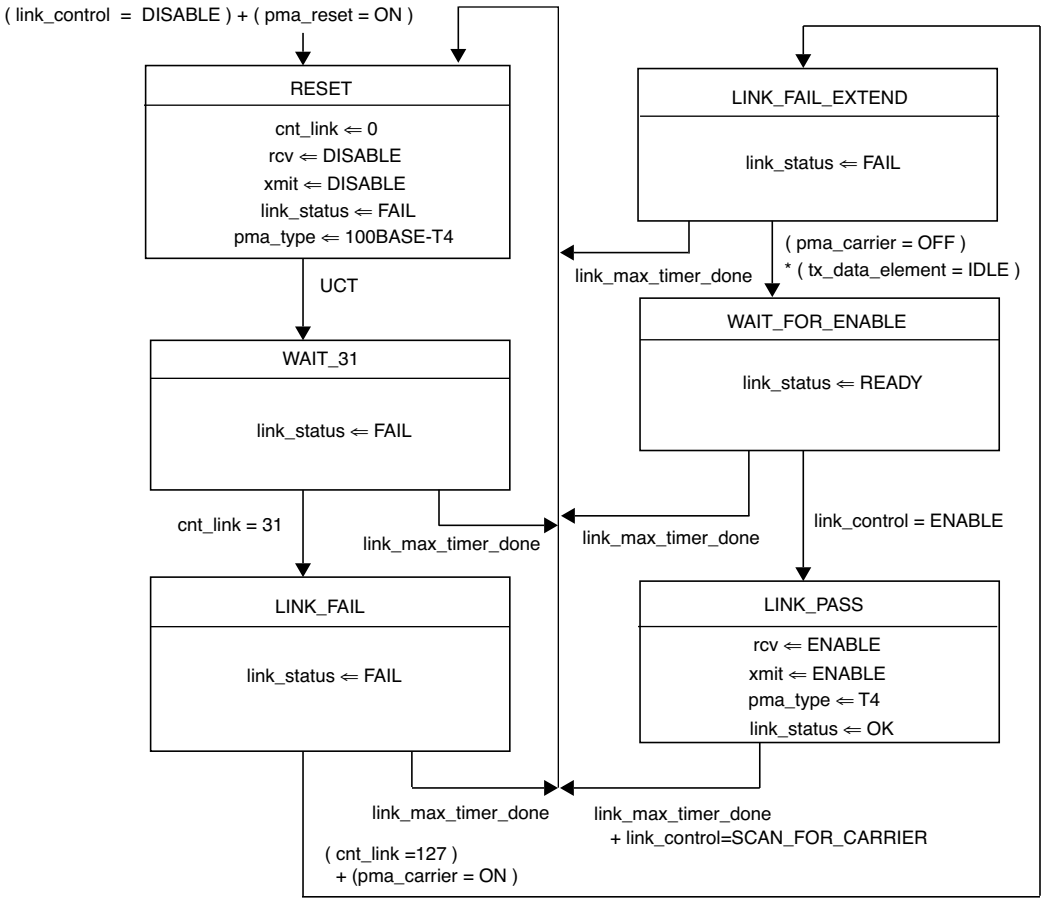
Reset to zero: On either of two conditions:

a) While in any state other than LINK_PASS, reset counter to zero if successive link test pulses are received within link_100_min.
b) While in any state, reset to zero if link_max_timer expires.

While in the LINK_PASS state, ignore pulses received within link_100_min (i.e., do not count them).

23.4.3.5 Link Integrity state diagram

The Link Integrity state diagram is shown in Figure 23–12.



NOTE—The variables link_control and link_status are designated as link_control_[T4] and link_status_[T4], respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–16).

Figure 23–12—Link Integrity state diagram

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23.5 PMA electrical specifications

This clause defines the electrical characteristics of the PHY at the MDI.

The ground reference point for all common-mode tests is the MII ground circuit. Implementations without an MII use the chassis ground. The values of all components in test circuits shall be accurate to within ±1% unless otherwise stated.

23.5.1 PMA-to-MDI interface characteristics

23.5.1.1 Isolation requirement

The PHY shall provide electrical isolation between the DTE, or repeater circuits including frame ground, and all MDI leads. This electrical separation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in subclause 5.3.2 of IEC 60950: 1991.
b) 2250 Vdc for 60 s, applied as specified in subclause 5.3.2 of IEC 60950: 1991.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time or half value), as defined in IEC 60060.

There shall be no insulation breakdown, as defined in subclause 5.3.2 of IEC 60950: 1991, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 Vdc.

23.5.1.2 Transmitter specifications

The PMA shall provide the Transmit function specified in 23.4.1.2 in accordance with the electrical specifications of this clause.

Where a load is not specified, the transmitter shall meet requirements of this clause when each transmit output is connected to a differentially connected 100 Ω resistive load.

23.5.1.2.1 Peak differential output voltage

While repetitively transmitting the ternary sequence [0 0 1 0 0 0 0 0 -1 0 0 0] (leftmost ternary symbol first), and while observing the differential transmitted output at the MDI, for any pair, with no intervening cable, the absolute value of both positive and negative peaks shall fall within the range of 3.15 V to 3.85 V (3.5 V ± 10%).

23.5.1.2.2 Differential output templates

While repetitively transmitting the ternary sequence [0 0 1 0 0 0 0 0 -1 0 0 0], and while observing the transmitted output at the MDI, the observed waveform shall fall within the normalized transmit template listed in Table 23–4. Portions of this table are represented graphically in Figure 23–13. The entire normalized transmit template shall be scaled by a single factor between 3.15 and 3.85. It is a functional requirement that linear interpolation be used between points. The template time axis may be shifted horizontally to attain the most favorable match. In addition to this simple test pattern, all other pulses, including link integrity pulses and also including the first pulse of each packet preamble, should meet this same normalized transmit template, with appropriate shifting and linear superposition of the CS1 and CS-1 template limits. Transmitters are allowed to insert additional delay in the transmit path in order to meet the first pulse requirement, subject to the overall timing limitations listed in 23.11, Timing summary.

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While transmitting the TP_IDL_100 signal, and while observing the transmitted output at the MDI, the observed waveform shall fall within the normalized link pulse template listed in Table 23–4. Portions of this table are represented graphically in Figure 23–14. The entire template shall be scaled by the same factor used for the normalized transmit template test. It is a functional requirement that linear interpolation be used between template points. The template time axis may be shifted horizontally to attain the most favorable match.

After transmitting seven or more consecutive CS0 waveforms during the TP_IDL_100 signal, each pair, as observed using the 100BASE-T4 Transmit Test Filter (23.5.1.2.3) connected to the MDI, shall attain a state within 50 mV of zero.

When the TX_D1, BI_D3, or BI_D4 pair is driven with a repeating pattern (`1 -1 1 -1` ...) any harmonic measured at the MDI output shall be at least 27 dB below the fundamental at 12.5 MHz.

NOTE 1—The specification on maximum spectral components is not intended to ensure compliance with regulations concerning RF emissions. The implementor should consider any applicable local, national, or international regulations. Additional filtering of spectral components may therefore be necessary.

NOTE 2—The repetitive pattern [`0 0 1 0 0 0 0 0 -1 0 0 0`] (leftmost ternary symbol first) may be synthesized using the 8B6T coding rules from a string of repeating data octets with value 73 hex. The repetitive pattern [`1 -1 1 -1 1 -1`] (leftmost ternary symbol first) may be synthesized using the 8B6T coding rules from a string of repeating data octets with value 92 hex.

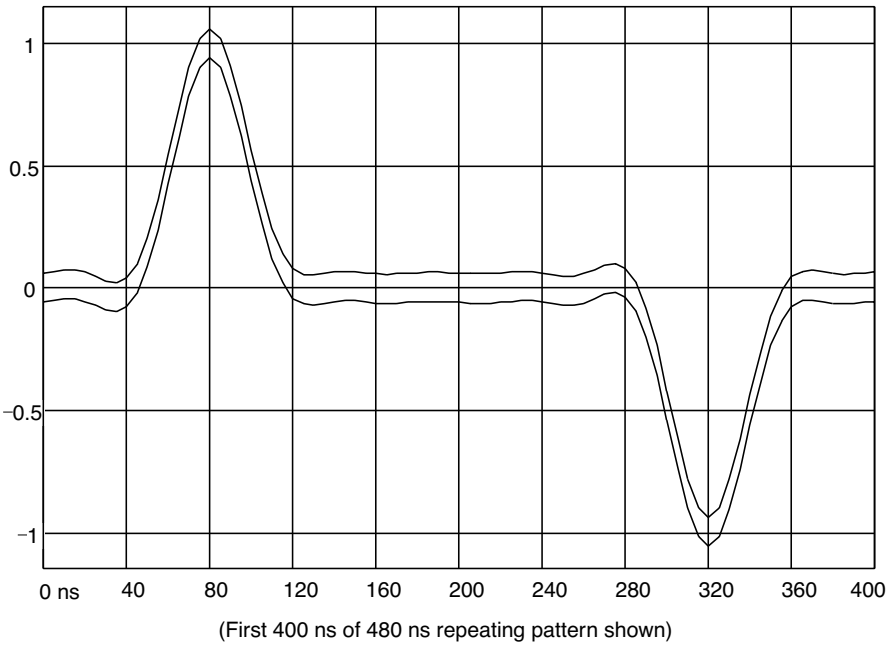


Figure 23–13—Normalized transmit template as measured at MD

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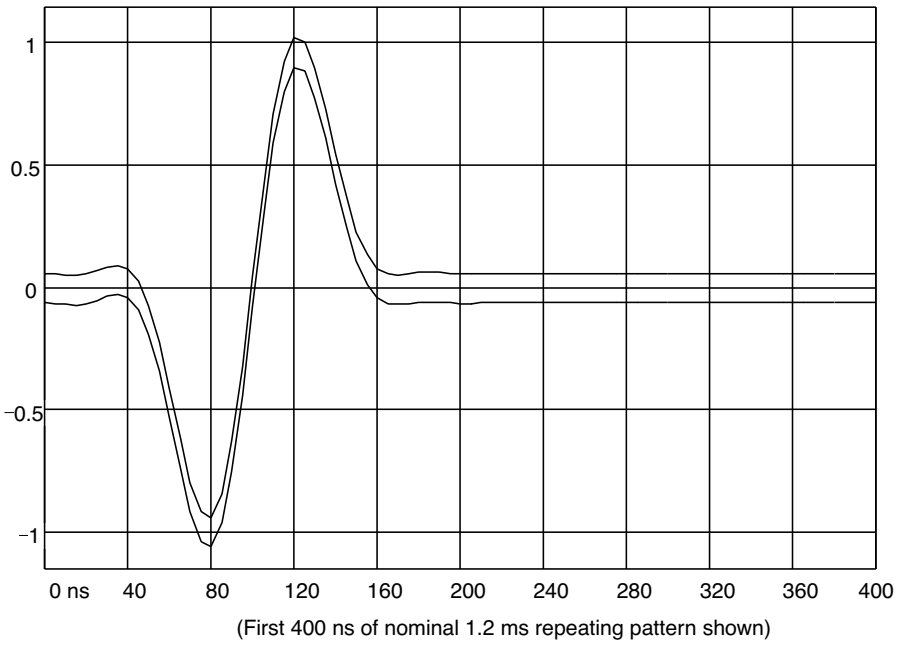


Figure 23–14—Normalized link pulse template as measured at MDI

The ideal template values may be automatically generated from the following equations:

Laplace transform of
Ideal transmit response $$IdealResponse(s) = \frac{Ideal(s)}{LPF(s)}$$

Where $Ideal(s)$ is a 100% raised cosine system response

Where $LPF(s)$ is a 3-pole Butterworth low pass filter response with –3 dB point at 25 MHz

Convert *IdealResponse(s)* from frequency domain to time domain

Use at least 8 samples per ternary symbol for the conversion

Superimpose alternating positive and negative copies of the ideal time response, seperated by 6 ternary symbol times, to form the ideal transmit voltage waveform.

The template limits are formed by offsetting the ideal transmit voltage waveform by plus and minus 6% of its peak.

23.5.1.2.3 Differential output ISI (intersymbol interference)

While observing a pseudo-random 8B6T coded data sequence (with every 6T code group represented at least once) preceded by at least 128 octets and followed by at least 128 octets of data, and while observing the transmitted output through a 100BASE-T4 Transmit Test Filter (one implementation of which is depicted in Figure 23–16), the ISI shall be less than 9%. The ISI for this test is defined by first finding the largest of the three peak-to-peak ISI error voltages marked in Figure 23–15 as TOP ISI, MIDDLE ISI, and BOTTOM ISI.

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Table 23–4—Normalized voltage templates as measured at the MDI

Time, ns	Normalized transmit template, pos. limit	Normalized transmit template, neg. limit	Normalized link template, pos. limit	Normalized link template, neg. limit
0	0.060	–0.061	0.061	–0.060
5	0.067	–0.054	0.056	–0.065
10	0.072	–0.049	0.052	–0.069
15	0.072	–0.049	0.052	–0.069
20	0.063	–0.058	0.058	–0.063
25	0.047	–0.074	0.071	–0.050
30	0.030	–0.091	0.086	–0.035
35	0.023	–0.098	0.094	–0.027
40	0.041	–0.080	0.080	–0.041
45	0.099	–0.022	0.027	–0.094
50	0.206	0.085	–0.076	–0.197
55	0.358	0.237	–0.231	–0.352
60	0.544	0.423	–0.428	–0.549
65	0.736	0.615	–0.640	–0.761
70	0.905	0.784	–0.829	–0.950
75	1.020	0.899	–0.954	–1.075
80	1.060	0.940	–0.977	–1.098
85	1.020	0.899	–0.876	–0.997
90	0.907	0.786	–0.653	–0.774
95	0.744	0.623	–0.332	–0.453
100	0.560	0.439	0.044	–0.077
105	0.384	0.263	0.419	0.298
110	0.239	0.118	0.738	0.617
115	0.137	0.016	0.959	0.838
120	0.077	–0.044	1.060	0.940
125	0.053	–0.068	1.044	0.923
130	0.050	–0.071	0.932	0.811
135	0.057	–0.064	0.759	0.638
140	0.064	–0.057	0.565	0.444
145	0.067	–0.054	0.383	0.262
150	0.065	–0.056	0.238	0.117
155	0.061	–0.060	0.138	0.017
160	0.057	–0.064	0.081	–0.040
165	0.055	–0.066	0.057	–0.064

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Table 23–4—Normalized voltage templates as measured at the MDI *(continued)*

Time, ns	Normalized transmit template, pos. limit	Normalized transmit template, neg. limit	Normalized link template, pos. limit	Normalized link template, neg. limit
170	0.056	–0.065	0.054	–0.067
175	0.059	–0.062	0.058	–0.063
180	0.062	–0.059	0.063	–0.058
185	0.064	–0.057	0.064	–0.057
190	0.064	–0.057	0.063	–0.058
195	0.062	–0.059	0.060	–0.061
200	0.060	–0.061	0.058	–0.063
205	0.057	–0.064	0.058	–0.063
210	0.056	–0.065	0.059	–0.062
215	0.058	–0.063	0.060	–0.061
220	0.061	–0.060	0.062	–0.059
225	0.064	–0.057	0.062	–0.059
230	0.066	–0.055	0.062	–0.059
235	0.065	–0.056	0.061	–0.060
240	0.061	–0.060	0.060	–0.061
245	0.054	–0.067	0.060	–0.061
250	0.049	–0.072	0.060	–0.061
255	0.049	–0.072	0.060	–0.061
260	0.058	–0.063	0.061	–0.060
265	0.074	–0.047	0.061	–0.060
270	0.091	–0.030	0.061	–0.060
275	0.099	–0.022	0.061	–0.060
280	0.080	–0.041	0.060	–0.061
285	0.022	–0.099	0.060	–0.061
290	–0.085	–0.206	0.060	–0.061
295	–0.238	–0.359	0.060	–0.061
300	–0.423	–0.544	0.061	–0.060
305	–0.615	–0.736	0.061	–0.060
310	–0.783	–0.904	0.061	–0.060
315	–0.899	-1.020	0.061	–0.060
320	–0.940	-1.061	0.060	–0.061
325	–0.899	-1.020	0.060	–0.061
330	–0.786	–0.907	0.060	–0.061
335	–0.623	–0.744	0.060	–0.061

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Table 23–4—Normalized voltage templates as measured at the MDI *(continued)*

Time, ns	Normalized transmit template, pos. limit	Normalized transmit template, neg. limit	Normalized link template, pos. limit	Normalized link template, neg. limit
340	–0.439	–0.560	0.061	–0.060
345	–0.263	–0.384	0.061	–0.060
350	–0.118	–0.239	0.061	–0.060
355	–0.016	–0.137	0.061	–0.060
360	0.044	–0.077	0.060	–0.061
365	0.068	–0.053	0.060	–0.061
370	0.070	–0.051	0.060	–0.061
375	0.064	–0.057	0.060	–0.061
380	0.057	–0.064	0.061	–0.060
385	0.054	–0.067	0.061	–0.060
390	0.056	–0.065	0.061	–0.060
395	0.060	–0.061	0.061	–0.060
400	0.064	–0.057	0.060	–0.061
405	0.065	–0.056	0.060	–0.061
410	0.064	–0.057	0.060	–0.061
415	0.061	–0.060	0.060	–0.061
420	0.059	–0.062	0.061	–0.060
425	0.058	–0.063	0.061	–0.060
430	0.059	–0.062	0.061	–0.060
435	0.060	–0.061	0.061	–0.060
440	0.061	–0.060	0.060	–0.061
445	0.062	–0.059	0.060	–0.061
450	0.062	–0.059	0.060	–0.061
455	0.061	–0.060	0.060	–0.061
460	0.060	–0.061	0.061	–0.060
465	0.059	–0.062	0.061	–0.060
470	0.060	–0.061	0.061	–0.060
475	0.060	–0.061	0.061	–0.060
480	0.061	–0.060	0.060	–0.061

The largest of these peak-to-peak ISI error voltages is then divided by the overall peak-to-peak signal voltage. (The technique of limiting the ratio of worst ISI to overall peak-to-peak voltage at 9% accomplishes the same end as limiting the ratio of worst ISI to nominal peak-to-peak at 10%.)

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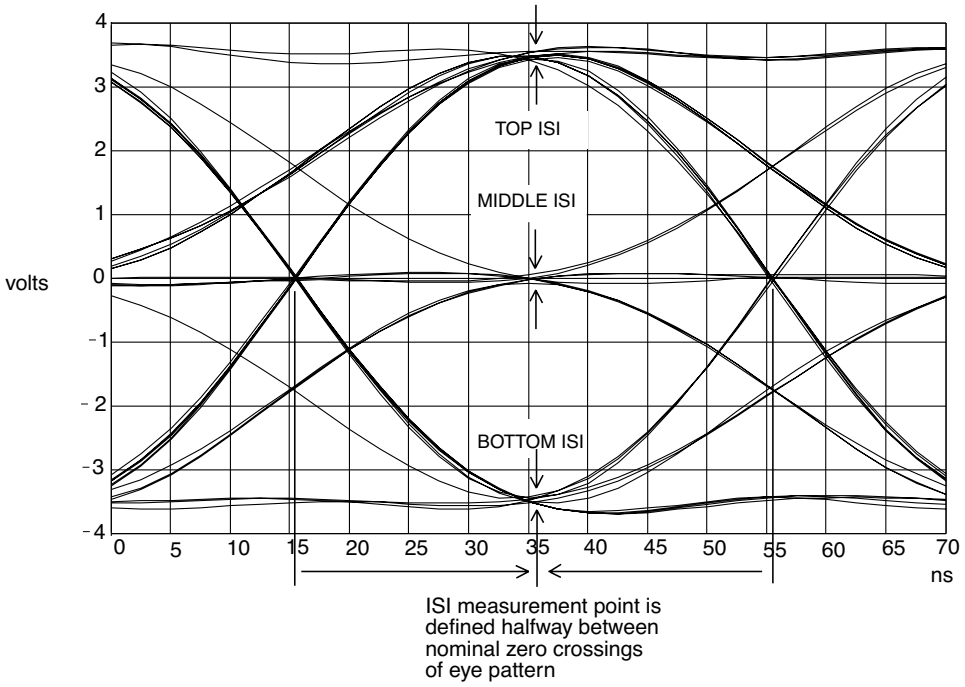


Figure 23–15—Definition of sampling points for ISI measurement

It is a mandatory requirement that the peak-to-peak ISI, and the overall peak-to-peak signal voltage, be measured at a point in time halfway between the nominal zero crossings of the observed eye pattern.

It is a mandatory requirement that the 100BASE-T4 Transmit Test Filter perform the function of a third-order Butterworth filter with its –3 dB point at 25.0 MHz.

One acceptable implementation of a 100BASE-T4 Transmit Test Filter appears in Figure 23–16. That implementation uses the 100BASE-T4 Transmit Test Filter as a line termination. The output of the filter is terminated in 100 Ω. It is a mandatory requirement that such implementations of the 100BASE-T4 Transmit Test Filter be designed such that the reflection loss of the filter, when driven by a 100 Ω source, exceeds 17 dB across the frequency range 2 to 12.5 MHz.

Equivalent circuits that implement the same overall transfer function are also acceptable. For example, the 100BASE-T4 Transmit Test Filter may be tapped onto a line in parallel with an existing termination. It is a mandatory requirement that such implementations of the 100BASE-T4 Transmit Test Filter be designed with an input impedance sufficiently high that the reflection loss of the parallel combination of filter and 100 Ω termination, when driven by 100 Ω, exceeds 17 dB across the frequency range 2 to 12.5 MHz.

23.5.1.2.4 Transmitter differential output impedance

The differential output impedance as measured at the MDI for each transmit pair shall be such that any reflection due to differential signals incident upon the MDI from a balanced cable having an impedance of 100 Ω is at least 17 dB below the incident signal, over the frequency range of 2.0 MHz to 12.5 MHz. This return loss shall be maintained at all times when the PHY is fully powered.

With every transmitter connected as in Figure 23–17, and while transmitting a repeating sequence of packets as specified in Table 23–5, the amount of droop on any transmit pair as defined in Figure 23–18 during the transmission of eop1 and eop4 shall not exceed 6.0%.

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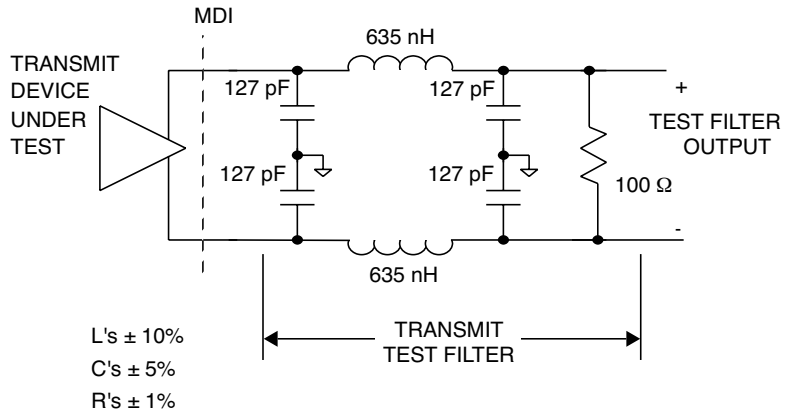


Figure 23–16—Acceptable implementation of transmit test filter

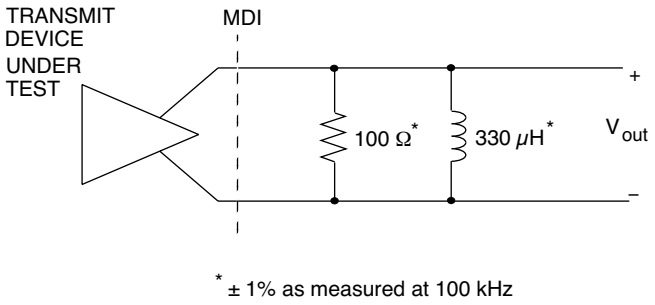


Figure 23–17—Output impedance test setup

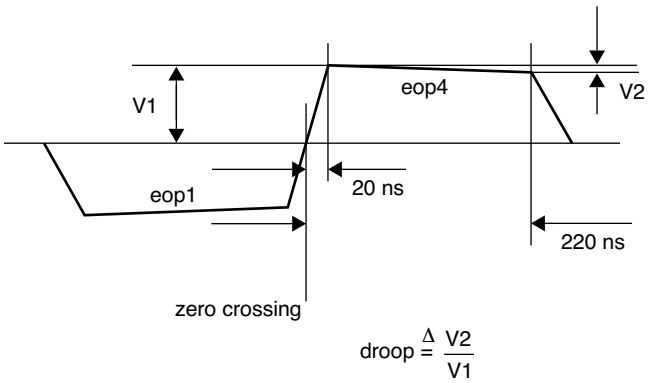


Figure 23–18—Measurement of output droop

Table 23–5—Sequence of packets for droop test

Packet sequence (Transmit this sequence of packets in a repetitive loop)	**Packet length** (Number of data octets)	**Data, hex** (All octets in each packet are the same)
first packet	64	AA
second packet	65	AA
third packet	66	AA

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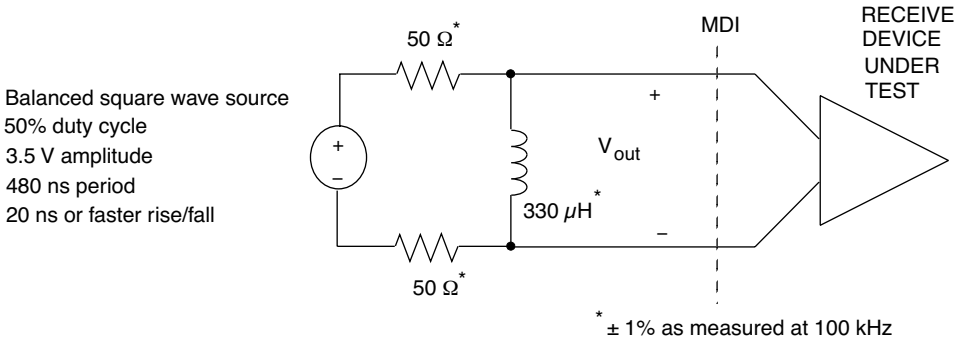


Figure 23–19—Input impedance test setup

23.5.1.2.5 Output timing jitter

While repetitively transmitting a random sequence of valid 8B6T code words, and while observing the output of a 100BASE-T4 Transmit Test Filter connected at the MDI to any of the transmit pairs as specified in 23.5.1.2.3, the measured jitter shall be no more than 4 ns p-p. For the duration of the test, each of the other transmit pairs shall be connected to either a 100BASE-T4 Transmit Test Filter or a 100 Ω resistive load.

NOTE 1—Jitter is the difference between the actual zero crossing point in time and the ideal time. For various ternary transitions, the zero crossing time is defined differently. For transitions between +1 and –1 or vice versa, the zero crossing point is defined as that point in time when the voltage waveform crosses zero. For transitions between zero and the other values, or from some other value to zero, the zero crossing time is defined as that point in time when the voltage waveform crosses the boundary between logical voltage levels, halfway between zero volts and the logical +1 or logical –1 ideal level.

NOTE 2—The ideal zero crossing times are contained in a set of points $\{t_n\}$ where $t_n = t_0 + n/f$, where n is an integer, and f is in the range 25.000 MHz ± 0.01%. A collection of zero crossing times satisfies the jitter requirement if there exists a pair (t_0, f) such that each zero crossing time is separated from some member of $\{t_n\}$ by no more than 4 ns.

23.5.1.2.6 Transmitter impedance balance

The common-mode to differential-mode impedance balance of each transmit output shall exceed

$$29 - 17\log\left(\frac{f}{10}\right)\text{dB}$$

where f is the frequency (in MHz) over the frequency range 2.0 MHz to 12.5 MHz. The balance is defined as

$$20\log\left(\frac{E_{\text{cm}}}{E_{\text{dif}}}\right)$$

where E_{cm} is an externally applied sine-wave voltage as shown in Figure 23-20.

NOTE—The balance of the test equipment (such as the matching of the test resistors) must be insignificant relative to the balance requirements.

23.5.1.2.7 Common-mode output voltage

The implementor should consider any applicable local, national, or international regulations. Driving unshielded twisted pairs with high-frequency, common-mode voltages may result in interference to other equipment. FCC conducted and radiated emissions tests may require that, while transmitting data, the magnitude of the total common-mode output voltage, $E_{\text{cm(out)}}$, on any transmit circuit, be less than a few millivolts when measured as shown in Figure 23–21.

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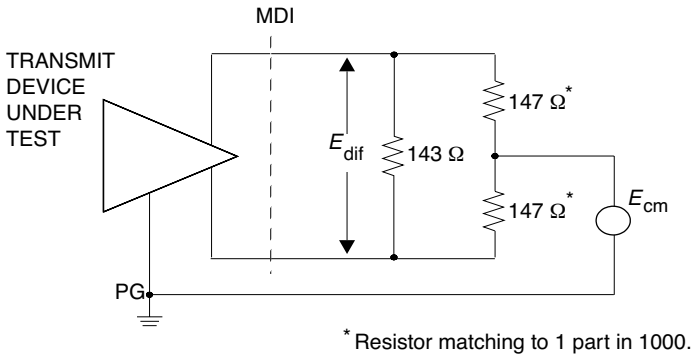


Figure 23-20—Transmitter impedance balance and common-mode rejection test circuit

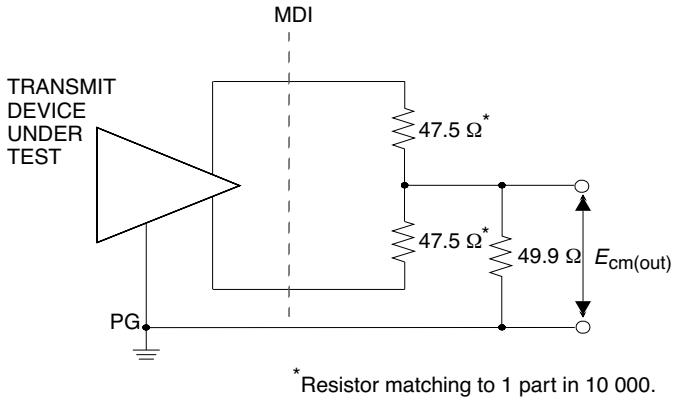


Figure 23–21—Common-mode output voltage test circuit

23.5.1.2.8 Transmitter common-mode rejection

The application of E_{cm} as shown in Figure 23-20 shall not change the differential voltage at any transmit output, E_{dif}, by more than 100 mV for all data sequences while the transmitter is sending data. Additionally, the edge jitter added by the application of E_{cm} shall be no more than 1.0 ns. E_{cm} shall be a 15 V peak 10.1 MHz sine wave.

23.5.1.2.9 Transmitter fault tolerance

Transmitters, when either idle or nonidle, shall withstand without damage the application of short circuits across any transmit output for an indefinite period of time and shall resume normal operation after such faults are removed. The magnitude of the current through such a short circuit shall not exceed 420 mA.

Transmitters, when either idle or nonidle, shall withstand without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity (as indicated in Figure 23–22). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

23.5.1.2.10 Transmit clock frequency

The ternary symbol transmission rate on each pair shall be 25.000 MHz ± 0.01%.

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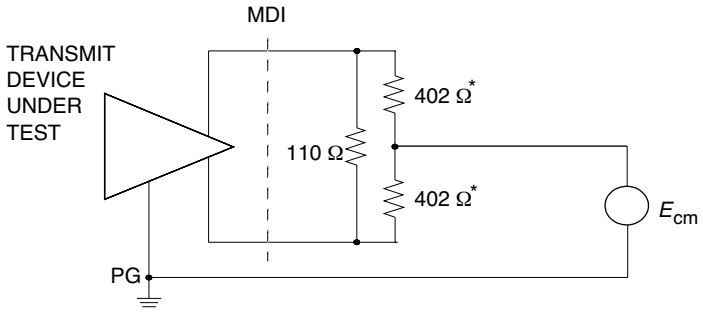


Figure 23–22—Transmitter fault tolerance test circuit

23.5.1.3 Receiver specifications

The PMA shall provide the Receive function specified in 23.4.1.3 in accordance with the electrical specifications of this clause. The patch cables and interconnecting hardware used in test configurations shall meet Category 5 specifications as in ISO/IEC 11801: 1995.

The term *worst-case UTP model*, as used in this clause, refers to lumped-element cable model shown in Figure 23–23 that has been developed to simulate the attenuation and group delay characteristics of 100 m of worst-case Category 3 PVC UTP cable.

This constant resistance filter structure has been optimized to best match the following amplitude and group delay characteristics, where the argument f is in hertz, and the argument x is the cable length in meters. For the worst-case UTP model, argument x was set to 100 m, and the component values determined for a best least mean squared fit of both real and imaginary parts of $H(f, x)$ over the frequency range 2 to 15 MHz.

NOTE—This group delay model is relative and does not includes the fixed delay associated with 100 m of Category 3 cable. An additional 570 ns of fixed delay should be added in order to obtain the absolute group delay.

$$PropagationImag(f, x) = j(-10)\sqrt{\frac{f}{10^7}}\left(\frac{x}{100}\right)$$

$$PropagationReal(f, x) = -\left(7.1\sqrt{\frac{f}{10^6} + 0.70\frac{f}{10^6}}\right)\left(\frac{x}{305}\right)$$

$$\frac{PropagationImag(f, x) + PropagationReal(f, x)}{20}$$

$$H(f, x) = 10$$

23.5.1.3.1 Receiver differential input signals

Differential signals received on the receive inputs that were transmitted within the constraints of 23.5.1.2, and have then passed through a worst-case UTP model, shall be correctly translated into one of the PMA_UNITDATA.indicate messages and sent to the PCS. In addition, the receiver, when presented with a link test pulse generated according to the requirements of 23.4.1.2 and followed by at least 3T of silence on pair RX_D2, shall accept it as a link test pulse.

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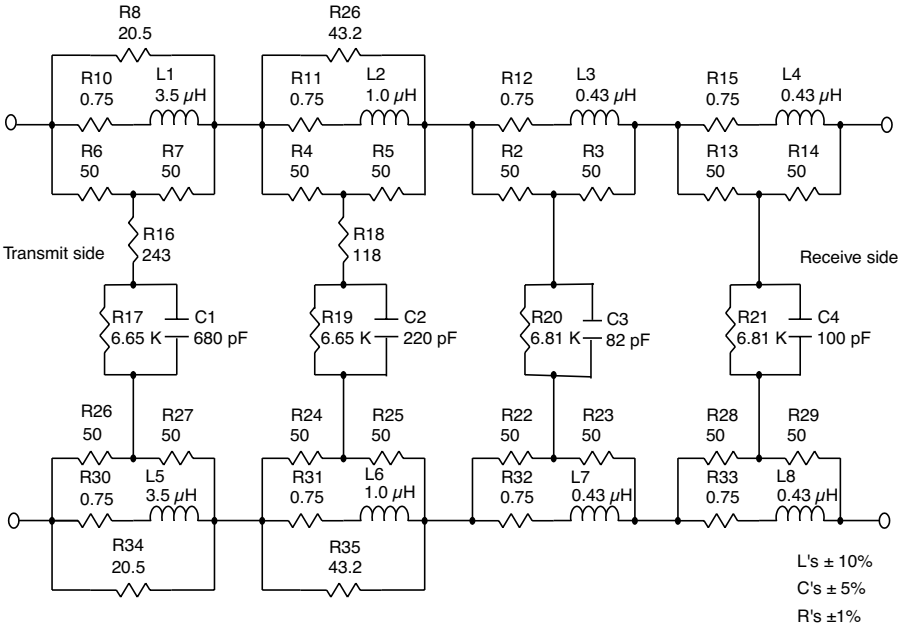


Figure 23–23—Worst-case UTP model

Both data and link test pulse receive features shall be tested in at least two configurations: using the worst-case UTP model, and with a connection less than one meter in length between transmitter and receiver.

A receiver is allowed to discard the first received packet after the transition into state LINK_PASS, using that packet for the purpose of fine-tuning its receiver equalization and clock recovery circuits.

NOTE—Implementors may find it practically impossible to meet the requirements of this subclause without using some form of adaptive equalization.

23.5.1.3.2 Receiver differential noise immunity

The PMA, when presented with 8B6T encoded data meeting the requirements of 23.5.1.3.1, shall translate this data into PMA_UNITDATA.indicate (DATA) messages with a bit loss of no more than that specified in 23.4.1.3.

The PMA Carrier Sense function shall *not* set pma_carrier=ON upon receiving any of the following signals on pair RX_D2 at the receiving MDI, as measured using a 100BASE-T4 transmit test filter (23.5.1.2.3):

a) All signals having a peak magnitude less than 325 mV.
b) All continuous sinusoidal signals of amplitude less than 8.7 V peak-to-peak and frequency less than 1.7 MHz.
c) All sine waves of single cycle or less duration, starting with phase 0° or 180°, and of amplitude less than 8.7 V peak-to-peak, where the frequency is between 1.7 MHz and 15 MHz. For a period of 7 BT before and after this single cycle, the signal shall be less than 325 mV.
d) Fast link pulse burst (FLP burst), as defined in Clause 28.
e) The link integrity test pulse signal TP_IDL_100.

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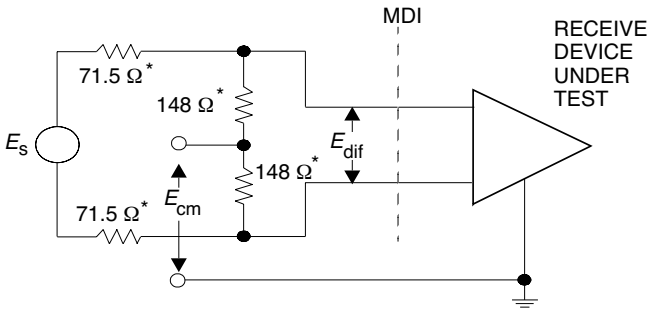
23.5.1.3.3 Receiver differential input impedance

The differential input impedance as measured at the MDI for each receive input shall be such that any reflection due to differential signals incident upon each receive input from a balanced cable having an impedance of 100 Ω is at least 17 dB below the incident signal, over the frequency range of 2.0 MHz to 12.5 MHz. This return loss shall be maintained at all times when the PHY is fully powered.

With each receiver connected as in Figure 23–19, and with the source adjusted to simulate eop1 and eop4 (50% duty cycle square wave with 3.5 V amplitude, period of 480 ns, and risetime of 20 ns or faster), the amount of droop on each receive pair as defined in Figure 23–18 shall not exceed 6.0%.

23.5.1.3.4 Common-mode rejection

While receiving packets from a compliant 100BASE-T4 transmitter connected to all MDI pins, a receiver shall send the proper PMA_UNITDATA.indicate messages to the PCS for any differential input signal E_s that results in a signal E_{dif} that meets 23.5.1.3.1 even in the presence of common-mode voltages E_{cm} (applied as shown in Figure 23–24). E_{cm} shall be a 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%–80%), connected to each of the receive pairs RX_D2, BI_D3, and BI_D4.



* Resistor matching to 1 part in 1000.

Figure 23–24—Receiver common-mode rejection test circuit

23.5.1.3.5 Receiver fault tolerance

The receiver shall tolerate the application of short circuits between the leads of any receive input for an indefinite period of time without damage and shall resume normal operation after such faults are removed. Receivers shall withstand without damage a 1000 V common-mode impulse of either polarity (E_{cm} as indicated in Figure 23–25). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

23.5.1.3.6 Receiver frequency tolerance

The receive feature shall properly receive incoming data with a ternary symbol rate within the range 25.000 MHz ± 0.01%.

23.5.2 Power consumption

After 100 ms following PowerOn, the current drawn by the PHY shall not exceed 0.75 A when powered through the MII.

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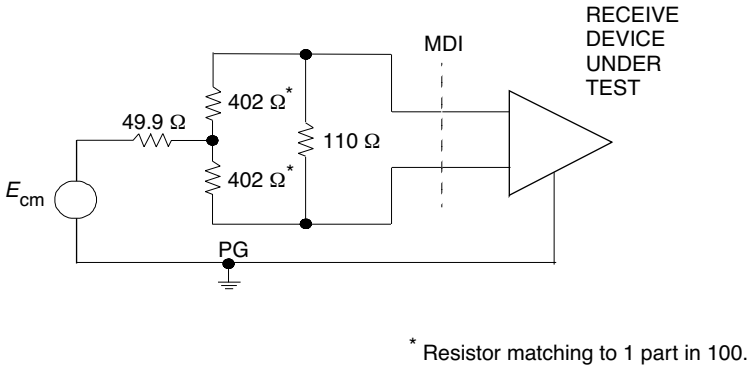


Figure 23–25—Common-mode impulse test circuit

The PHY shall be capable of operating from all voltage sources allowed by Clause 22, including those current limited to 0.75 A, as supplied by the DTE or repeater through the resistance of all permissible MII cables.

The PHY shall not introduce extraneous signals on the MII control circuits during normal power-up and power-down.

While in power-down mode the PHY is not required to meet any of the 100BASE-T4 performance requirements.

23.6 Link segment characteristics

23.6.1 Cabling

Cabling and installation practices generally suitable for use with this standard appear in ISO/IEC 11801: 1995. Exceptions, notes, and additional requirements are as listed below.

a) 100BASE-T4 uses a star topology. Horizontal cabling is used to connect PHY entities.
b) 100BASE-T4 is an ISO/IEC 11801: 1995 class C application, with additional installation requirements and transmission parameters specified in 23.6.2 through 23.6.4. The highest fundamental frequency transmitted by 8B6T coding is 12.5 MHz. The aggregate data rate for three pairs using 8B6T coding is 100 Mb/s.
c) 100BASE-T4 shall use four pairs of balanced cabling, Category 3 or better, with a nominal characteristic impedance of 100 Ω.
d) When using Category 3 cable for the link segment, Clause 23 recommends, but does not require, the use of Category 4 or better connecting hardware, patch cords and jumpers. The use of Category 4 or better connecting hardware increases the link segment composite NEXT loss, composite ELFEXT loss and reduces the link segment insertion loss. This lowers the link segment crosstalk noise, which in turn decreases the probability of errors.
e) The use of shielded cable is outside the scope of this standard.

23.6.2 Link transmission parameters

Unless otherwise specified, link segment testing shall be conducted using source and load impedances of 100 Ω.

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23.6.2.1 Insertion loss

The insertion loss of a simplex link segment shall be no more than 12 dB at all frequencies between 2 and 12.5 MHz. This consists of the attenuation of the twisted pairs, connector losses, and reflection losses due to impedance mismatches between the various components of the simplex link segment. The insertion loss specification shall be met when the simplex link segment is terminated in source and load impedances that satisfy 23.5.1.2.4 and 23.5.1.3.3.

NOTE—The loss of PVC-insulated cable exhibits significant temperature dependence. At temperatures greater than 40 °C, it may be necessary to use a less temperature-dependent cable, such as many Fluorinated Ethylene Propylene (FEP), Polytetrafluoroethylene (PTFE), or Perfluoroalkoxy (PFA) plenum-rated cables.

23.6.2.2 Differential characteristic impedance

The magnitude of the differential characteristic impedance of a 3 m length of twisted pair used in a simplex link shall be between 85 Ω and 115 Ω for all frequencies between 2 MHz and 12.5 MHz.

23.6.2.3 Coupling parameters

In order to limit the noise coupled into a simplex link segment from adjacent simplex link segments, Near-End Crosstalk (NEXT) loss and Equal Level Far-End Crosstalk (ELFEXT) loss are specified for each simplex link segment. In addition, since three simplex links (TX_D1, Bl_D3, and Bl_D4) are used to send data between PHYs and one simplex link (RX_D2) is used to carry collision information as specified in 23.1.4, Multiple-Disturber NEXT loss and Multiple-Disturber ELFEXT loss are also specified.

23.6.2.3.1 Differential Near-End Crosstalk (NEXT) loss

The differential Near-End Crosstalk (NEXT) loss between two simplex link segments is specified in order to ensure that collision information can be reliably received by the PHY receiver. The NEXT loss between each of the three data carrying simplex link segments and the collision sensing simplex link segment shall be at least $24.5 - 15\times\log_{10}(f/12.5)$ (where f is the frequency in MHz) over the frequency range 2.0 MHz to 12.5 MHz.

23.6.2.3.2 Multiple-disturber NEXT (MDNEXT) loss

Since three simplex links are used to send data between PHYs and one simplex link is used to carry collision information, the NEXT noise that is coupled into the collision, sensing simplex link segment is from multiple (three) signal sources, or disturbers. The MDNEXT loss between the three data carrying simplex link segments and the collision sensing simplex link segment shall be at least $21.4 - 15\times\log_{10}(f/12.5)$ dB (where f is the frequency in MHz) over the frequency range 2.0 to 12.5 MHz. Refer to 12.7.3.2 and Annex B.3 Example Crosstalk Computation for Multiple Disturbers, for a tutorial and method for estimating the MDNEXT loss for an n-pair cable.

23.6.2.3.3 Equal Level Far-End Crosstalk (ELFEXT) loss

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk noise at the far end of a simplex link segment to meet the BER objective specified in 23.1.2 and the noise specifications of 23.6.3. Far-End Crosstalk (FEXT) noise is the crosstalk noise that appears at the far end of a simplex link segment which is coupled from an adjacent simplex link segment with the noise source (transmitters) at the near end. ELFEXT loss is the ratio of the data signal to FEXT noise at the output of a simplex link segment (receiver input). To limit the FEXT noise from adjacent simplex link segments, the ELFEXT loss between two data carrying simplex link segments shall be greater than $23.1 - 20\times\log_{10}(f/12.5)$ dB (where f is the frequency in MHz) over the frequency range 2.0 MHz to 12.5 MHz. ELFEXT loss at frequency f and distance l is defined as

$$\text{ELFEXT\_Loss}\ (f,l) = 20 \times \log_{10}\left(\frac{V_{\text{pds}}}{V_{\text{pcn}}}\right) - \text{SLS\_Loss (dB)}$$

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where

V_{pds}	is the peak voltage of disturbing signal (near-end transmitter)
V_{pcn}	is the peak crosstalk noise at the far end of disturbed simplex link segment
SLS_Loss	is the insertion loss of the disturbing simplex link segment

23.6.2.3.4 Multiple-disturber ELFEXT (MDELFEXT) loss

Since three simplex links are used to transfer data between PHYs, the FEXT noise that is coupled into an data carrying simplex link segment is from multiple (two) signal sources, or disturbers. The MDELFEXT loss between a data carrying simplex link segment and the other two data carrying simplex link segments shall be greater than $20.9 - 20\times\log_{10}(f/12.5)$ (where f is the frequency in MHz) over the frequency range 2.0 MHz to 12.5 MHz. Refer to 12.7.3.2 and Appendix A3, Example Crosstalk Computation for Multiple Disturbers, for a tutorial and method for estimating the MDELFEXT loss for an n-pair cable.

23.6.2.4 Delay

Since T4 sends information over three simplex link segments in parallel, the absolute delay of each and the differential delay are specified to comply with network round-trip delay limits and ensure the proper decoding by receivers, respectively.

23.6.2.4.1 Maximum link delay

The propagation delay of a simplex link segment shall not exceed 570 ns at all frequencies between 2.0 MHz and 12.5 MHz.

23.6.2.4.2 Maximum link delay per meter

The propagation delay per meter of a simplex link segment shall not exceed 5.7 ns/m at all frequencies between 2.0 MHz and 12.5 MHz.

23.6.2.4.3 Difference in link delays

The difference in propagation delay, or skew, under all conditions, between the fastest and the slowest simplex link segment in a link segment shall not exceed 50 ns at all frequencies between 2.0 MHz and 12.5 MHz. It is a further functional requirement that, once installed, the skew between all pair combinations due to environmental conditions shall not vary more than ± 10 ns, within the above requirement.

23.6.3 Noise

The noise level on the link segments shall be such that the objective error rate is met. The noise environment consists generally of two primary contributors: self-induced near-end crosstalk, which affects the ability to detect collisions, and far-end crosstalk, which affects the signal-to-noise ratio during packet reception.

23.6.3.1 Near-End Crosstalk

The MDNEXT (Multiple-Disturber Near-End Crosstalk) noise on a link segment depends on the level of the disturbing signals on pairs TX_D1, BI_D3, and BI_D4, and the crosstalk loss between those pairs and the disturbed pair, RX_D2.

The MDNEXT noise on a link segment shall not exceed 325 mVp.

This standard is compatible with the following assumptions:

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a) Three disturbing pairs with 99th percentile pair-to-pair NEXT loss greater than 24.5 dB at 12.5 MHz (i.e., Category 3 cable).
b) Six additional disturbers (2 per simplex link) representing connectors at the near end of the link segment with 99th percentile NEXT loss greater than 40 dB at 12.5 MHz (i.e., Category 3 connectors installed in accordance with 23.6.4.1).
c) All disturbers combined according to the MDNEXT Monte Carlo procedure outlined in Appendix A3, Example Crosstalk Computation for Multiple Disturbers.

The MDNEXT noise is defined using three maximum level 100BASE-T4 transmitters sending uncorrellated continuous data sequences while attached to the simplex link segments TX_D1, BI_D3, and BI_D4 (disturbing links), and the noise measured at the output of a filter connected to the simplex link segment RX_D2. (disturbed link). Each continuous data sequence is a pseudo-random bit pattern having a length of at least 2047 bits that has been coded according to the 8B6T coding rules in 23.2.1.2. The filter is the 100BASE-T4 Transmit Test Filter specified in 23.5.1.2.3.

23.6.3.2 Far-End Crosstalk

The MDFEXT (Multiple-Disturber Far-End Crosstalk) noise on a link segment depends on the level of the disturbing signals on pairs TX_D1, BI_D3, and BI_D4, and the various crosstalk losses between those pairs.

The MDFEXT noise on a link segment shall not exceed 87 mVp.

This standard is compatible with the following assumptions:

a) Two disturbing pairs with 99th percentile ELFEXT (Equal Level Far-End Crosstalk) loss greater than 23 dB at 12.5 MHz.
b) Nine additional disturbers (three per simplex link) representing connectors in the link segment with 99th percentile NEXT loss greater than 40 dB at 12.5 MHz.
c) All disturbers combined according to the MDNEXT Monte Carlo procedure outlined in Appendix A3, Example Crosstalk Computation for Multiple Disturbers.

The MDFEXT noise is defined using two maximum level 100BASE-T4 transmitters sending uncorrellated continuous data sequences while attached to two simplex link segments (disturbing links) and the noise measured at the output of a filter connected to the far end of a third simplex link segment (disturbed link). Each continuous data sequence is a pseudo-random bit pattern having a length of at least 2047 bits that has been coded according to the 8B6T coding rules in 23.2.1.2. The filter is the 100BASE-T4 Transmit Test Filter specified in 23.5.1.2.3.

23.6.4 Installation practice

23.6.4.1 Connector installation practices

The amount of untwisting in a pair as a result of termination to connecting hardware should be no greater than 25 mm (1.0 in) for Category 3 cables. This is the same value recommended in ISO/IEC 11801: 1995 for Category 4 connectors.

23.6.4.2 Disallow use of Category 3 cable with more than four pairs

Jumper cables, or horizontal runs, made from more than four pairs of Category 3 cable are not allowed.

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23.6.4.3 Allow use of Category 5 jumpers with up to 25 pairs

Jumper cables made from up to 25 pairs of Category 5 cable, for the purpose of mass-terminating port connections at a hub, are allowed. Such jumper cables, if used, shall be limited in length to no more than 10 m total.

23.7 MDI specification

This clause defines the MDI. The link topology requires a crossover function between PMAs. Implementation and location of this crossover are also defined in this clause.

23.7.1 MDI connectors

Eight-pin connectors meeting the requirements of section 3 and figures 1 through 5 of IEC 60603-7: 1990 shall be used as the mechanical interface to the balanced cabling. The plug connector shall be used on the balanced cabling and the jack on the PHY. These connectors are depicted (for informational use only) in Figures 23–26 and 23–27. Table 23-6 shows the assignment of PMA signals to connector contacts for PHYs with and without an internal crossover.

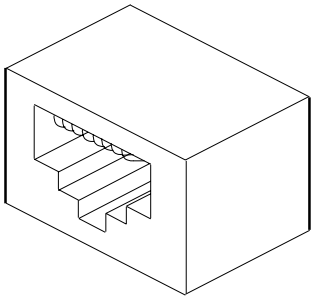


Figure 23–26—MDI connector

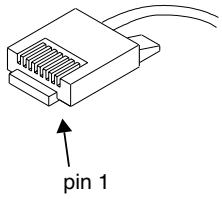


Figure 23–27—Balanced cabling connector

Table 23-6—MDI connection and labeling requirements

Contact	PHY without internal crossover (recommended for DTE) internal PMA signals	PHY with internal crossover (recommended for repeater) internal PMA signals	MDI labeling requirement
1	TX_D1+	RX_D2+	TX_D1+
2	TX_D1–	RX_D2–	TX_D1–
3	RX_D2+	TX_D1+	RX_D2+
4	BI_D3+	BI_D4+	BI_D3+
5	BI_D3–	BI_D4–	BI_D3–
6	RX_D2–	TX_D1–	RX_D2–
7	BI_D4+	BI_D3+	BI_D4+
8	BI_D4–	BI_D3–	BI_D4–

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23.7.2 Crossover function

It is a functional requirement that a crossover function be implemented in every link segment. The crossover function connects the transmitters of one PHY to the receivers of the PHY at the other end of the link segment. Crossover functions may be implemented internally to a PHY or elsewhere in the link segment. For a PHY that does not implement the crossover function, the MDI labels in the last column of Table 23–4 refer to its own internal circuits (second column). For PHYs that do implement the internal crossover, the MDI labels in the last column of Table 23–4 refer to the internal circuits of the remote PHY of the link segment. Additionally, the MDI connector for a PHY that implements the crossover function shall be marked with the graphical symbol “X”. Internal and external crossover functions are shown in Figure 23–28. The crossover function specified here for pairs TX_D1 and RX_D2 is compatible with the crossover function specified in 14.5.2 for pairs TD and RD.

When a link segment connects a DTE to a repeater, it is recommended the crossover be implemented in the PHY local to the repeater. If both PHYs of a link segment contain internal crossover functions, an additional external crossover is necessary. It is recommended that the crossover be visible to an installer from one of the PHYs. When both PHYs contain internal crossovers, it is further recommended in networks in which the topology identifies either a central backbone segment or a central repeater that the PHY furthest from the central element be assigned the external crossover to maintain consistency.

Implicit implementation of the crossover function within a twisted-pair cable, or at a wiring panel, while not expressly forbidden, is beyond the scope of this standard.

23.8 System considerations

The repeater unit specified in Clause 27 forms the central unit for interconnecting 100BASE-T4 twisted-pair links in networks of more than two nodes. It also provides the means for connecting 100BASE-T4 twisted-pair links to other 100 Mb/s baseband segments. The proper operation of a CSMA/CD network requires that network size be limited to control round-trip propagation delay as specified in Clause 29.

23.9 Environmental specifications

23.9.1 General safety

All equipment meeting this standard shall conform to IEC 60950: 1991.

23.9.2 Network safety

This clause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cable systems described in this clause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

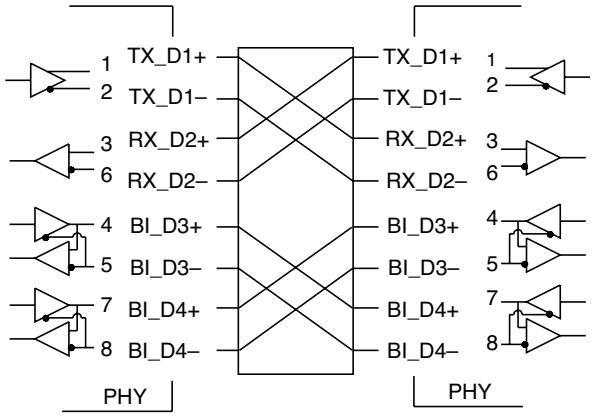
a) Direct contact between LAN components and power, lighting, or communications circuits
b) Static charge buildup on LAN cables and components
c) High-energy transients coupled onto the LAN cable system
d) Voltage potential differences between safety grounds to which various LAN components are connected

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational

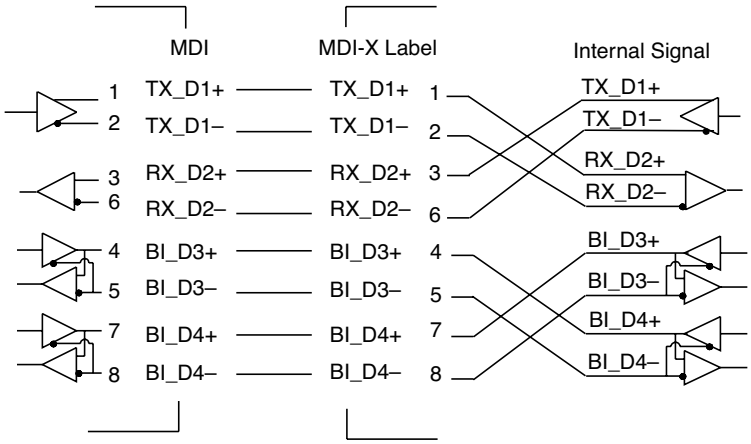
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a) Two PHYs with external crossover function



b) PHY with internal crossover function

Figure 23–28—Crossover function

system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network.

23.9.2.1 Installation

It is a mandatory functional requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

23.9.2.2 Grounding

Any safety grounding path for an externally connected PHY shall be provided through the circuit ground of the MII connection.

WARNING

It is assumed that the equipment to which the PHY is attached is properly grounded, and not left floating nor serviced by a "doubly insulated, ac power distribution system." The use of floating or insulated equipment, and the consequent implications for safety, are beyond the scope of this standard.

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23.9.2.3 Installation and maintenance guidelines

It is a mandatory functional requirement that, during installation and maintenance of the cable plant, care be taken to ensure that noninsulated network cable conductors do not make electrical contact with unintended conductors or ground.

23.9.2.4 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 100BASE-T4 equipment. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply.

Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400 Ω source impedance.

Ringing voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 Ω source resistance. The dc component is 56 Vdc with a 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 100BASE-T4 equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE—Wiring errors may impose telephony voltages differentially across 100BASE-T4 transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, receivers will generally appear to the telephone system as off-hook telephones. Therefore, full-ring voltages will be applied for only short periods. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to the low resistance of the transformer coil.

23.9.3 Environment

23.9.3.1 Electromagnetic emission

The twisted-pair link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

23.9.3.2 Temperature and humidity

The twisted-pair link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

23.10 PHY labeling

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Data rate capability in Mb/s
b) Power level in terms of maximum current drain (for external PHYs)
c) Any applicable safety warnings

See also 23.7.2.

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23.11 Timing summary

23.11.1 Timing references

All MII signals are defined (or corrected to) the DTE end of a zero length MII cable.

NOTE—With a finite length MII cable, TX_CLK appears in the PHY one cable propagation delay *earlier* than at the MII. This advances the transmit timing. Receive timing is retarded by the same amount.

The phrase *adjusted for pair skew*, when applied to a timing reference on a particular pair, means that the designated timing reference has been adjusted by adding to it the difference between the time of arrival of preamble on the latest of the three receive pairs and the time of arrival of preamble on that particular pair.

PMA_UNITDATA.request

Figures 23–29, 23–30, 23–31, and 23–32. The implementation of this abstract message is not specified. Conceptually, this is the time at which the PMA has been given full knowledge and use of the ternary symbols to be transmitted.

PMA_UNITDATA.indicate

Figure 23–33. The implementation of this abstract message is not specified. Conceptually, this is the time at which the PCS has been given full knowledge and use of the ternary symbols received.

WAVEFORM

Figure 23–29. Point in time at which output waveform has moved 1/2 way from previous nominal output level to present nominal output level.

TX_EN

Figure 23–30. First rising edge of TX_CLK following the rising edge of TX_EN.

NOT_TX_EN

Figures 23–31 and 23–32. First rising edge of TX_CLK following the falling edge of TX_EN.

CRS

Figure 23–33. Rising edge of CRS.

CARRIER_STATUS

Figure 23–33. Rising edge of carrier_status.

NOT_CARRIER_STATUS

Figure 23–34. Falling edge of carrier_status.

RX_DV

No figure. First rising edge of RX_CLK following rising edge of RX_DV.

COL

No figure. Rising edge of COL signal at MII.

NOT_COL

No figure. Falling edge of COL signal at MII.

PMA_ERROR

No figure. Time at which rxerror_status changes to ERROR.

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23.11.2 Definitions of controlled parameters

PMA_OUT

Figure 23–29. Time between PMA_UNITDATA.request (tx_code_vector) and the WAVEFORM timing reference for each of the three transmit channels TX_D1, BI_D3, or BI_D4.

TEN_PMA

Figures 23–30, 23–31, and 23–32. Time between TX_EN timing reference and MA_UNITDATA.request (tx_code_vector).

TEN_CRS

Figure 23–30. Time between TX_EN timing reference and the loopback of TX_EN to CRS as measured at the CRS timing reference point.

NOT_TEN_CRS

Figures 23–31 and 23–32. Time between NOT_TX_EN timing reference and the loopback of TX_EN to CRS as measured at the NOT_CRS timing reference point. In the event of a collision (COL is raised at any point during a packet) the minimum time for NOT_TEN_CRS may optionally be as short as 0.

RX_PMA_CARRIER

Figure 23–33. Time between the WAVEFORM timing reference, adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse) and the CARRIER_STATUS timing reference.

RX_CRS

Figure 23–33. Time between the WAVEFORM timing reference, adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse) and the CRS timing reference.

NOTE—The input waveform used for this test is an ordinary T4 preamble, generated by a compliant T4 transmitter. As such, the delay between the first and third pulses of the preamble (which are used by the carrier sense logic) is very nearly 80 ns.

RX_NOT_CRS

For a data packet, the time between the WAVEFORM timing reference, adjusted for pair skew, of the first pulse of eop1, and the de-assertion of CRS. For a collision fragment, the time between the WAVEFORM timing reference, adjusted for pair skew, of the ternary symbol on pair TX_D2, which follows the last ternary data symbol received on pair RX_D2, and the de-assertion of CRS.

Both are limited to the same value. For a data packet, detection of the six ternary symbols of eopo1 is accomplished in the PCS layer. For a collision fragment, detection of the concluding seven ternary zeroes is accomplished in the PMA layer, and passed to the PCS in the form of the carrier_status indication.

FAIRNESS

The difference between RX_NOT_CRS at the conclusion of one packet and RX_CRS on a subsequent packet. The packets used in this test may arrive with an IPG anywhere in the range of 80 to 160.

RX_PMA_DATA

Figure 23–33. Time between the WAVEFORM timing reference, adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse) and the particular PMA_UNITDATA.indicate that transfers to the PCS the first ternary symbol of the first 6T code group from receive pair BI_D3.

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EOP_CARRIER_STATUS

Figure 23–34. For a data packet, the time between the WAVEFORM timing reference, adjusted for pair skew, of first pulse of eop1 and the NOT_CARRIER_STATUS timing reference.

EOC_CARRIER_STATUS

Figure 23–35. In the case of a colliding packet, the time between the WAVEFORM timing reference, adjusted for pair skew, of the ternary symbol on pair RX_D2, which follows the last ternary data symbol received on pair RX_D2 and the NOT_CARRIER_STATUS timing reference.

RX_RXDV

No figure. Time between WAVEFORM timing reference, adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse) and the RX_DV timing reference.

RX_PMA_ERROR

No figure. In the event of a preamble in error, the time between the WAVEFORM timing reference adjusted for pair skew, of first pulse of that preamble (or first pulse of the preamble preceded by a link test pulse or a partial link test pulse), and the PMA_ERROR timing reference.

RX_COL

No figure. In the event of a collision, the time between the WAVEFORM timing reference adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse), and the COL timing reference.

RX_NOT_COL

No figure. In the event of a collision in which the receive signal stops before the locally transmitted signal, the time between the WAVEFORM timing reference adjusted for pair skew, of the ternary symbol on pair RX_D2, which follows the last ternary data symbol received on pair RX_D2 and the NOT_COL timing reference point.

TX_NOT_COL

No figure. In the event of a collision in which the locally transmitted signal stops before the received signal, the time between the NOT_TX_EN timing reference and the loopback of TX_EN to COL as measured at the NOT_COL timing reference point.

TX_SKEW

Greatest absolute difference between a) the waveform timing reference of the first pulse of a preamble as measured on output pair TX_D1; b) the waveform timing reference of the first pulse of a preamble as measured on output pair BI_D3; and c) the waveform timing reference of the first pulse of a preamble as measured on output pair BI_D4. Link test pulses, if present during the measurement, must be separated from the preamble by at least 100 ternary symbols.

CRS_PMA_DATA

Time between the timing reference for CARRIER STATUS and the transferral, via PMA_UNITDATA.indicate, of the first ternary symbol of the 6T code group marked DATA1 in Figure 23–6.

COL_to_BI_D3/D4_OFF

No figure. In the case of a colliding packet, the time between the WAVE FORM timing reference, adjusted for pair skew, of the first pulse of preamble (or the first pulse of the preamble preceded by a link test pulse or a partial link test pulse) on RX_D2, and the first ternary zero transmitted on BI_D3 and on BI_D4.

NOTE—Subclause 23.4.1.2 mandates that transmission on pairs BI_D3 and BI_D4 be halted in the event of a collision.

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23.11.3 Table of required timing values

While in the LINK_PASS state, each PHY timing parameter shall fall within the Low and High limits listed in Table 23–7. All units are in bit times. A bit time equals 10 ns.

Table 23–7—Required timing values

Controlled parameter	Low limit (bits)	High limit (bits)	Comment
PMA_OUT	1	9.5	
TEN_PMA + PMA_OUT	7	17.5	
TEN_CRS	0	+4	
NOT_TEN_CRS	0	36	
RX_PMA_CARRIER	0	15.5	
RX_CRS	0	27.5	
RX_NOT_CRS	0	51.5	
FAIRNESS	0	28	
RX_PMA_DATA	67	90.5	
EOP_CARRIER_STATUS	51	74.5	
EOC_CARRIER_STATUS	3	50.5	
RX_RXDV	81	114.5	
RX_PMA_ERROR	RX_PMA_DATA	RX_PMA_DATA + 20	Allowed limits equal the actual RX_PMA_DATA time for the device under test plus from 0 to 20 BT
RX_COL	0	27.5	SAME AS RX_CRS
RX_NOT_COL	0	51.5	SAME AS RX_NOT_CRS
TX_NOT_COL	0	36	
TX_SKEW	0	0.5	
CRS_PMA_DATA	0	78.5	
COL_to_BI_D3/D4_OFF	0	40	

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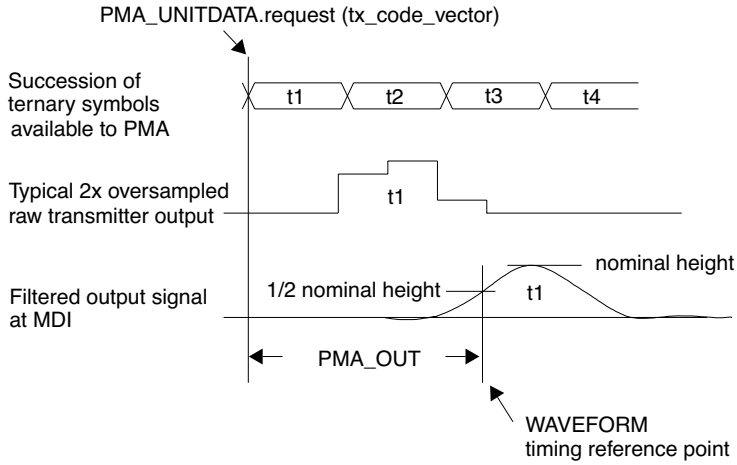


Figure 23–29—PMA TRANSMIT timing while tx_code_vector = DATA

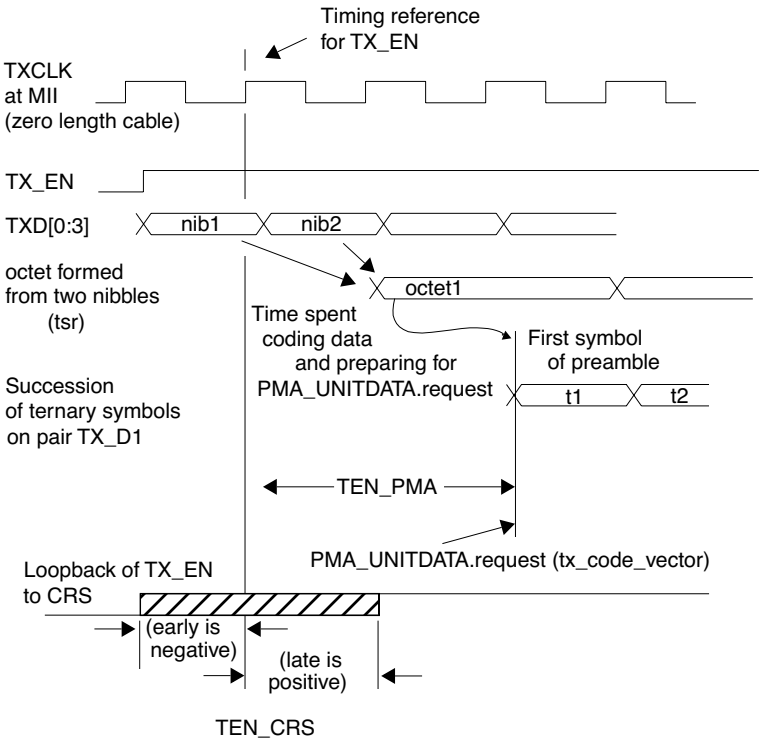


Figure 23–30—PCS TRANSMIT timing at start of packet

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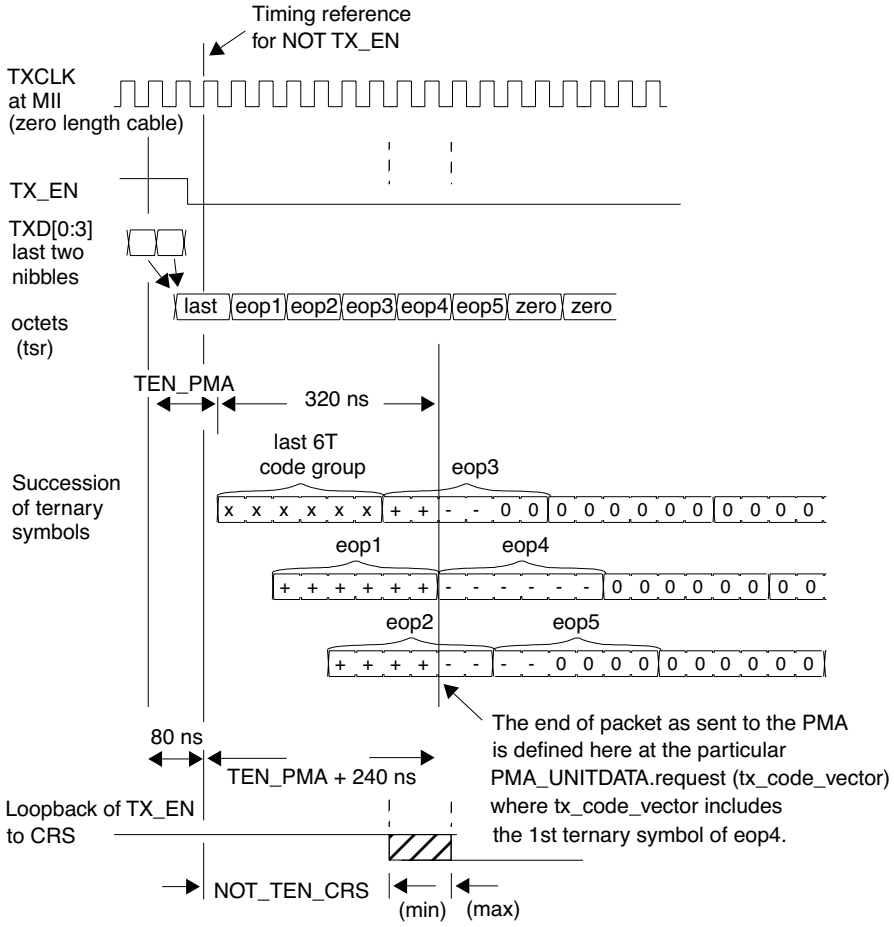


Figure 23–31—PCS TRANSMIT timing end of normal packet

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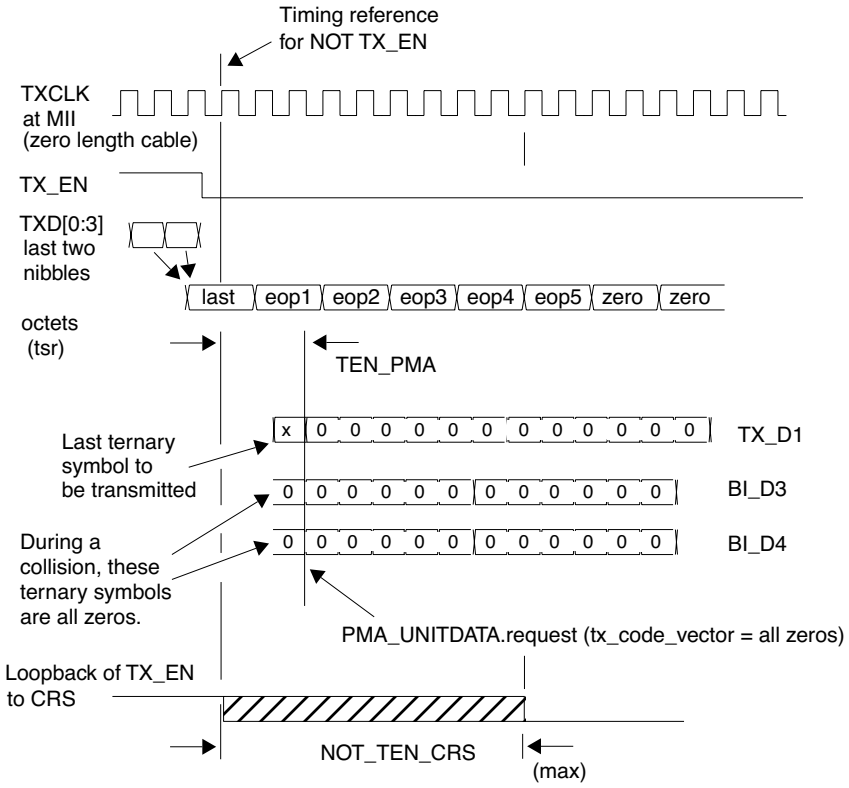


Figure 23–32—PCS TRANSMIT timing end of colliding packet

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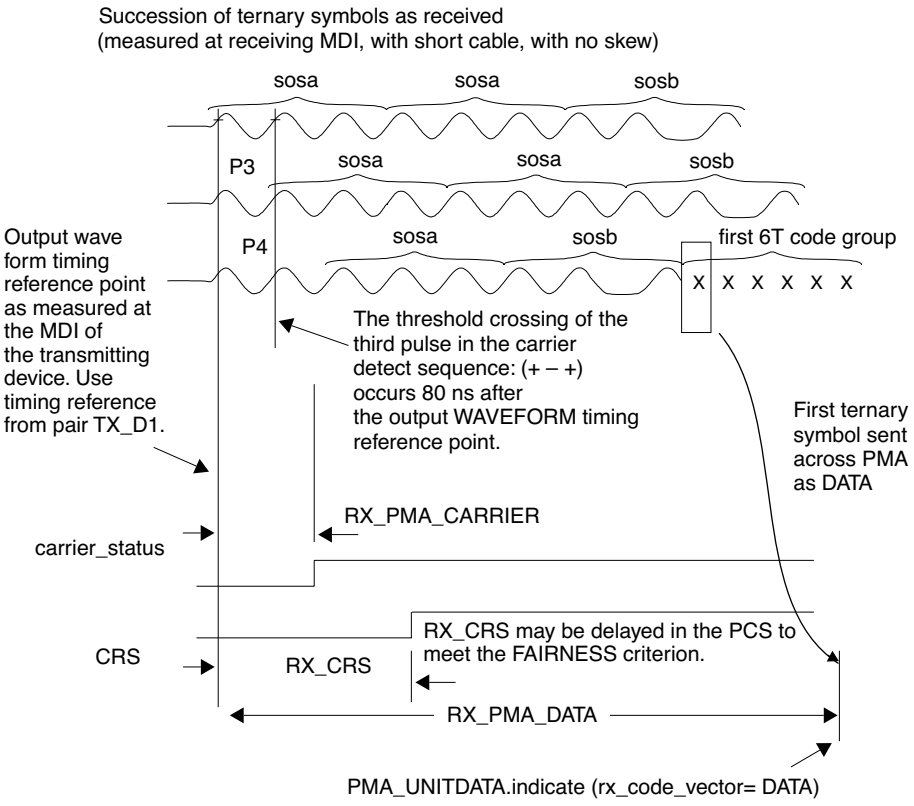


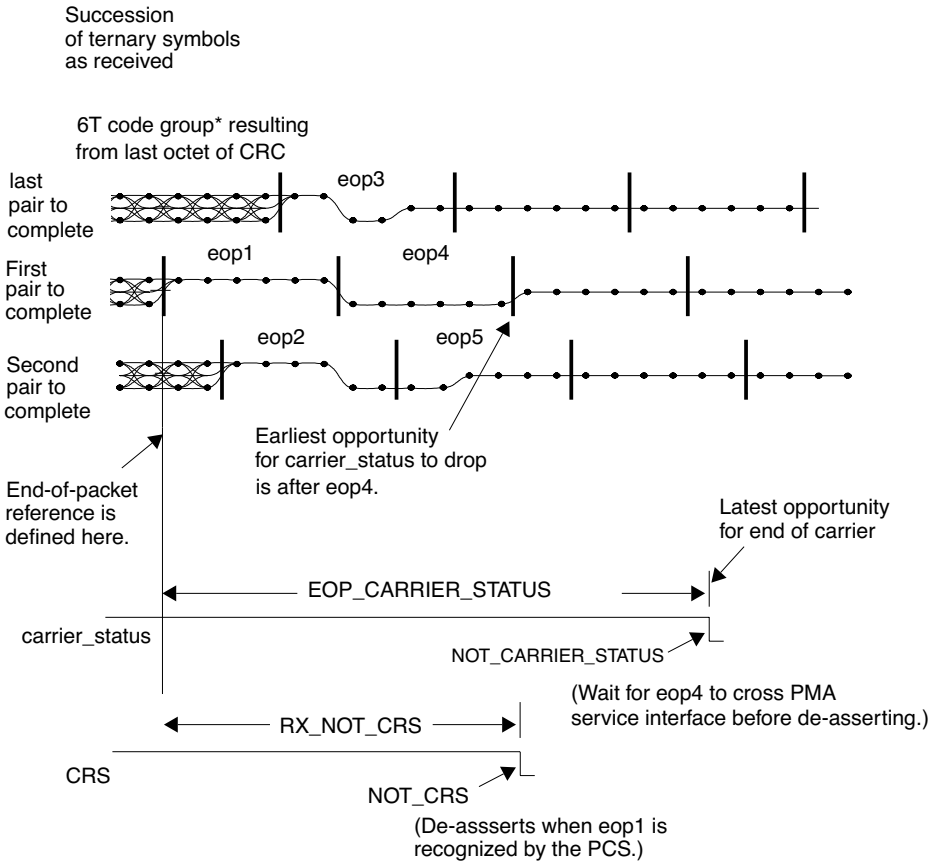
Figure 23–33—PMA RECEIVE timing start of packet

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*RX_DV de-asserts after sending the last nibble of this decoded octet across the MII. CRS may de-assert prior to that time.

Figure 23–34—PMA RECEIVE timing end of normal packet

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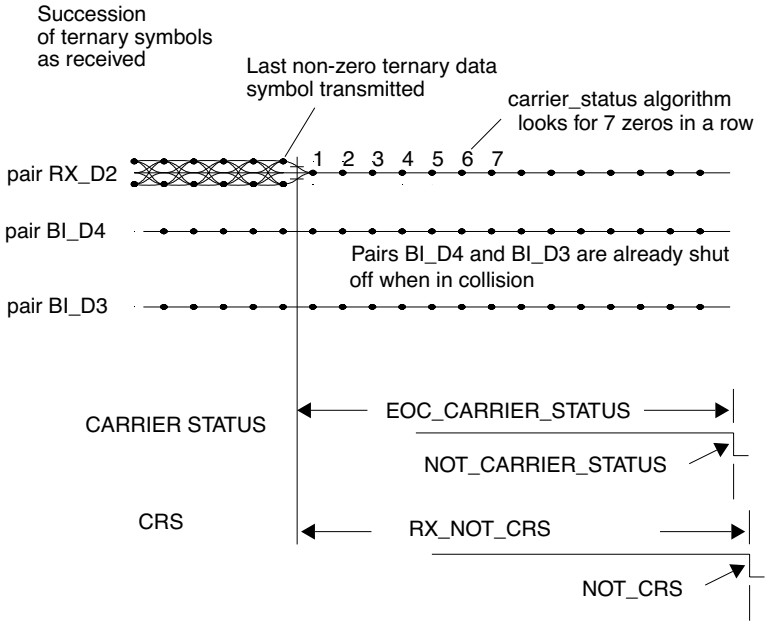


Figure 23–35—PMA RECEIVE timing end of colliding packet

23.12 Protocol Implementation Conformance Statement (PICS) proforma for Clause 23, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100BASE-T4[4]

23.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 23, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100BASE-T4, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

[4]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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23.12.2 Identification

23.12.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTES 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

23.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2002, Clause 23, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100BASE-T4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

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23.12.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*MII	Exposed MII interface	23.1.5.3	O		Devices supporting this option must also support the PCS option
*PCS	PCS functions	23.1.5.2	O		Required for integration with DTE or MII
*PMA	Exposed PMA service interface	23.1.5.2	O		Required for integration into symbol level repeater core
*XVR	Internal wiring crossover	23.7.2	O		Usually implemented in repeater, usually not in DTE
*NWY	Support for optional Auto-Negotiation (Clause 28)	23.1.5.4	O		Required if Auto-Negotiation is implemented
*INS	Installation / cable		O		Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer

23.12.4 PICS proforma tables for the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T4

23.12.4.1 Compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
CCO-1	Compatibility at the MDI	23.1.5.1	M		

23.12.4.2 PCS Transmit functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCT-1	PCS Transmit function	23.2.1.2	PCS:M		Complies with state diagram Figure 23–8
PCT-2	Data encoding	23.2.1.2	PCS:M		8B6T with DC balance encoding rules
PCT-3	Order of ternary symbol transmission	Annex 23A	PCS:M		Leftmost symbol of each 6T code group first

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23.12.4.3 PCS Receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCR1	PCS Receive function	23.2.1.3	PCS:M		Complies with state diagram Figure 23–9
PCR2	Value of RXD<3:0> while RXDV is de-asserted	23.2.1.3	PCS:M		All zeroes
PCR3	Data decoding	23.2.1.3	PCS:M		8B6T with error detecting rules
PCR4	Value of dc_balance_error, eop_error and codeword_error at times other than those specified in the error detecting rules.	23.2.1.3	PCS:M		OFF
PCR5	Codeword_error indication sets RX_ER when	23.2.1.3	PCS:M		During transfer of both affected data nibbles across the MII
PCR6	Dc_balance_error sets RX_ER when	23.2.1.3	PCS:M		During transfer of both affected nibbles across the MII
PCR7	Eop_error sets RX_ER when	23.2.1.3	PCS:M		During transfer of last decoded data nibble across the MII
PCR8	Action taken if carrier_status is truncated dur to early de-assertion of carrier_status	23.2.1.3	PCS:M		Assert RX_ER, and then de-assert RX_DV

23.12.4.4 Other PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCO1	PCS Reset function executed when	23.2.1.1	PCS:M		Power-on, or the receipt of a reset request from the management entity
PCO2	PCS Error Sense function	23.2.1.4	PCS:M		Complies with state diagram Figure 23–10
PCO3	Signaling of RX_ER to MII	23.2.1.4	PCS:M		Before last nibble of Clause 4 MAC frame has passed across MII
PCO4	Timing of rxerror_status	23.2.1.4	PCS:M		Causes RX_ER to appear on the MII no later than last nibble of first data octet
PCO5	PCS Carrier Sense function	23.2.1.5	PCS:M		Controls MII signal CRS according to rules in 23.2.1.5
PCO6	MII signal COL is asserted when	23.2.1.6	PCS:M		Upon detection of a PCS collision
PCO7	At other times COL remains	23.2.1.6	PCS:M		De-asserted
PCO8	Loopback implemented in accordance with 22.4.1.2	23.2.2.2	PCS:M		Redundantly specified in 22.2.4.1.2

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23.12.4.4 Other PCS functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PCO9	No spurious signals emitted on the MDI during or after power down	23.2.2.2	M		
PCO10	PMA frame structure	23.2.3	M		Conformance to Figure 23–6
PCO11	PMA_UNITDATA messages	23.2.3	PMA:M		Must have a clock for both directions

23.12.4.5 PCS state diagram variables

Item	Feature	Subclause	Status	Support	Value/Comment
PCS1	Timing of eop adjusted such that the last nibble sent across the MII with RX_DV asserted is	23.2.4.2	PCS:M		Last nibble of last decoded data octet in a packet
PCS2	Transmission of octets on the three transmit pairs	23.2.4.2	PCS:M		Transmission order is: TX_D1, then BI_D3, and then BI_D4
PCS3	Value of tsr during first 16 TX_CLK cycles after TX_EN is asserted	23.2.4.2	PCS:M		sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosb, sosb, sosb, sosb, sosb, sosb
PCS4	Value of tsr during first 10 TX_CLK cycles after TX_EN is de-asserted	23.2.4.2	PCS:M		eop1, eop1, eop2, eop2, eop3, eop3, eop4, eop4, eop5, eop5
PCS5	TX_ER causes transmission of	23.2.4.2	PCS:M		bad_code
PCS6	TX_ER received during the first 16 TX_CLK cycles causes	23.2.4.2	PCS:M		Transmission of **bad_code** during 17th and 18th clock cycles
PCS7	Action taken in event TX_EN falls on an odd nibble boundary	23.2.4.2	PCS:M		Extension of TX_EN by one TX_CLK cycle, and transmission of bad_code
PCS8	Transmission when TX_EN is not asserted	23.2.4.2	PCS:M		zero_code
PCS9	TX_CLK generated synchronous to	23.2.4.2	PCS:M		tw1_timer

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23.12.4.6 PMA service interface

Item	Feature	Subclause	Status	Support	Value/Comment
PMS1	Continuous generation of PMA_TYPE	23.3.1.2	M		
PMS2	Generation of PMA_UNITDATA.indicate (DATA) messages	23.3.3.2	M		synchronous with data received at the MDI
PMS3	Generation of PMA_CARRIER.indicate message	23.3.4.2	M		ON/OFF
PMS4	Generation of PMA_LINK.indicate message	23.3.5.2	M		FAIL/READY/OK
PMS5	Link_control defaults on power-on or reset to	23.3.6.2	M		ENABLE
PMS6	Action taken in SCAN_FOR_CARRIER mode	23.3.6.4	NWY:M		Enables link integrity state diagram, but blocks passage into LINK_PASS
PMS7	Reporting of link_status while in SCAN_FOR_CARRRIER mode	23.3.6.4	NWY:M		FAIL / READY
PMS8	Reporting of link_status while in DISABLE mode	23.3.6.4	NWY:M		FAIL
PMS9	Action taken in ENABLE mode	23.3.6.4	NWY:M		enables data processing functions
PMS10	Generation of PMA_RXERROR	23.3.7.2	M		ERROR / NO_ERROR

23.12.4.7 PMA Transmit functions

Item	Feature	Subclause	Status	Support	Value/Comment
PMT1	Transmission while (tx_code_vector=DATA) * (pma_carrier=OFF)	23.4.1.2	M		tx_code_vector[TX_D1] tx_code_vector[BI_D3] tx_code_vector[BI_D4]
PMT2	Transmission from time (tx_code_vector=DATA) * (pma_carrier=ON), until (tx_code_vector=IDLE	23.4.1.2	M		tx_code_vector[TX_D1] CS0 CS0
PMT3	Transmission while tx_code_vector=IDLE	23.4.1.2	M		Idle signal TP_DIL_100
PMT4	Duration of silence between link test pulses	23.4.1.2	M		1.2 ms ± 0.6 ms
PMT5	Link test pulse composed of	23.4.1.2	M		CS-1, CS1 transmitted on TX_D1

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23.12.4.7 PMA Transmit functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PMT6	Following a packet, TP_IDL_100 signal starts with	23.4.1.2	M		Period of silence
PMT7	Effect of termination of TP_IDL_100	23.4.1.2	M		No delay or corruption of subsequent packet
PMT8	Zero crossing jitter of link test pulse	23.4.1.2	M		Less than 4 ns p-p
PMT9	Action taken when xmit=disable	23.4.1.2	M		Transmitter behaves as if tx_code_vector=IDLE

23.12.4.8 PMA Receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PMR1	Reception and translation of data with ternary symbol error rate less than	23.4.1.3	M		One part in 10^8
PMR2	Assertion of pma_carrier=ON upon reception of test signal	23.4.1.4	M		Test signal is a succession of three data values, produced synchronously with a 25 MHz clock, both preceded and followed by 100 symbols of silence. The three values are: 467 mV, –225 mV, and then 467 mV again
PMR3	condition required to turn off pma_carrier	23.4.1.4	M		Either of a) Seven consecutive zeroes b) Reception of eop1 per 23.4.1.4
PMR4	Value of carrier_status while rcv=ENABLE	23.4.1.4	M		pma_carrier
PMR5	Value of carrier_status while rcv=DISABLE	23.4.1.4	M		OFF

23.12.4.9 Link Integrity functions

Item	Feature	Subclause	Status	Support	Value/Comment
LIF1	Link Integrity function complies with	23.4.1.5	M		State diagram Figure 23–12

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23.12.4.10 PMA Align functions

Item	Feature	Subclause	Status	Support	Value/Comment
ALN1	Generation of PMA_UNITDATA.indicate (PREAMBLE) messages	23.4.1.6	M		
ALN2	Ternary symbols transferred by first PMA_UNITADATA.indicate (DATA) message	23.4.1.6	M		rx_code_vector[BI_D3]: first ternary symbol of first data code group rx_code_vector[BI_D2]: two ternary symbols prior to start of second data code group rx_code_vector[BI_D4]: four ternary symbols prior to start of third data code group
ALN3	PMA_UNITDATA.indicate (DATA) messages continue until carrier_status=OFF	23.4.1.6	M		
ALN4	While carrier_status=OFF, PMA emits message	23.4.1.6	M		PMA_UNITDATA.indicate (IDLE)
ALN5	Failure to recognize SSD generates rxerror_status=ERROR	23.4.1.6	M		
ALN6	Action taken when carrier_status=OFF	23.4.1.6	M		Clear rxerror_status
ALN7	Action taken if first packet is used for alignment	23.4.1.6	M		PMA emits PMA_UNITDATA..indicate (PREAMBLE)
ALN8	Tolerance of line skew	23.4.1.6	M		60 ns
ALN9	Detection of misplaced **sosb** 6T code group caused by 3 or fewer ternary symbols in error	23.4.1.6	M		
ALN10	Action taken if **rcv**=disable	23.4.1.6	M		PMA emits PMA_UNITDATA..indicate (IDLE)

23.12.4.11 Other PMA functions

Item	Feature	Subclause	Status	Support	Value/Comment
PMO1	PMA Reset function	23.4.1.1	M		
PMO2	Suitable clock recovery	23.4.1.7	M		

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23.12.4.12 Isolation requirements

Item	Feature	Subclause	Status	Support	Value/Comment
ISO1	Values of all components used in test circuits	23.5	M		Accurate to within ±1% unless required otherwise
ISO2	Electrical isolation meets	23.5.1.1	M		1500 V at 50–60 Hz for 60 s per IEC 60950: 1991 *or* 2250 Vdc for 60 s per IEC 60950: 1991 *or* Ten 2400 V pulses per IEC 60060
ISO3	Insulation breakdown during isolation test	23.5.1.1	M		None per IEC 60950: 1991
ISO4	Resistance after isolation test	23.5.1.1	M		At least 2 M Ω

23.12.4.13 PMA electrical requirements

Item	Feature	Subclause	Status	Support	Value/Comment
PME1	Conformance to all transmitter specifications in 23.5.1.2	23.5.1.2	M		
PME2	Transmitter load unless otherwise specified	23.5.1.2	M		100 Ω
PME3	Peak differential output voltage	23.5.1.2.1	M		3.15–3.85 V
PME4	Differential transmit template at MDI	23.5.1.2.2	M		Table 23–2
PME5	Differential MDI output template voltage scaling	23.5.1.2.2	M		3.15– 3.85 V
PME6	Interpolation between points on transmit template	23.5.1.2.2	M		Linear
PME7	Differential link pulse template at MDI	23.5.1.2.2	M		Table 23–2
PME8	Differential link pulse template scaling	23.5.1.2.2	M		Same value as used for differential transmit template scaling
PME9	Interpolation between point on link pulse template	23.5.1.2.2	M		Linear
PME10	State when transmitting seven or more consecutive CS0 during TP_IDL-100 signal	23.5.1.2.2	M		–50 mV to 50 mV
PME11	Limit on magnitude of harmonics measured at MDI	23.5.1.2.2	M		27 dB below fundamental
PME12	Differential output ISI	23.5.1.2.3	M		Less than 9%

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23.12.4.13 PMA electrical requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME13	Measurement of ISI and peak-to-peak signal voltage	23.5.1.2.3	M		Halfway between nominal zero crossing of the observed eye pattern
PME14	Transfer function of 100BASE-T4 transmit test filter	23.5.1.2.3	M		Third-order Butterworth filter with –3 dB point at 25.0 MHz
PME15	Reflection loss of 100BASE-T4 transmit test filter and 100 W load across the frequency range 2–12.5 MHz	23.5.1.2.3	M		Exceeds 17 dB
PME16	Differential output impedance	23.5.1.2.4	M		Provide return loss into 100 Ω of 17 dB from 2.0 to 12.5 MHz
PME17	Maintenance of return loss	23.5.1.2.4	M		At all times PHY is fully powered
PME18	Droop as defined in Figure 23–18 during transmission of eop1 and eop4	23.5.1.2.4	M		Less than 6%
PME19	Output timing jitter	23.5.1.2.5	M		No more than 4 ns peak-to-peak
PME20	Measurement of output timing jitter	23.5.1.2.5	M		Other transmit outputs connected to 100BASE-T4 ISI test filter or 100 Ω load
PME21	Minimum transmitter impedance balance	23.5.1.2.6	M		$29 - 17\log\left(\frac{f}{10}\right)$ dB
PME22	Transmitter common-mode rejection; effect of E_{cm} as shown in Figure 23-20 upon E_{dif}	23.5.1.2.8	M		Less than 100 mV
PME23	Transmitter common-mode rejection; effect of E_{cm} as shown in Figure 23-20 upon edge jitter	23.5.1.2.8	M		Less than 1.0 ns
PME24	E_{cm} used for common-mode rejection tests	23.5.1.2.8	M		15 V peak, 10.1 MHz sine wave
PME25	Transmitter faults; response to indefinite application of short circuits	23.5.1.2.9	M		Withstand without damage and resume operation after fault is removed
PME26	Transmitter faults; response to 1000 V common-mode impulse per IEC 60060	23.5.1.2.9	M		Withstand without damage
PME27	Shape of impulse used for common-mode impulse test	23.5.1.2.9	M		0.3/50 μs as defined in IEC 60060
PME28	Ternary symbol transmission rate	23.5.1.2.10	M		25.000 MHz ± 0.01%

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23.12.4.13 PMA electrical requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME29	Conformance to all receiver specifications in 23.5.1.3	23.5.1.3	M		
PME30	Action taken upon receipt of differential signals that were transmitted within the constraints of 23.5.1.2 and have passed through worst-case UTP model	23.5.1.3.1	M		Correctly translated into PMA_UNITDATA messages
PME31	Action taken upon receipt of link test pulse	23.5.1.3.1	M		Accept as a link test pulse
PME32	Test configuration for data reception and link test pulse tests	23.5.1.3.1	M		Using worst-case UTP model, and with a connection less than one meter in length
PME33	Bit loss	23.5.1.3.2	M		No more than that specified in 23.5.1.3.1
PME34	Reaction of pma_carrier to signal less than 325 mV peak	23.5.1.3.2	M		Must not set pma_carrier=ON
PME35	Reaction of pma_carrier to continuous sinusoid less than 1.7 MHz	23.5.1.3.2	M		Must not set pma_carrier=ON
PME36	Reaction of pma_carrier to single cycle or less	23.5.1.3.2	M		Must not set pma_carrier=ON
PME37	Reaction of pma_carrier to fast link pulse as defined in Clause 28	23.5.1.3.2	M		Must not set pma_carrier=ON
PME38	Reaction of pma_carrier to link integrity test pulse signal TP_IDL_100	23.5.1.3.2	M		Must not set pma_carrier=ON
PME39	Differential input impedance	23.5.1.3.3	M		Provide return loss into 100 Ω of 17 dB from 2.0 to 12.5 MHz
PME40	Maintenance of return loss	23.5.1.3.3	M		At all times PHY is fully powered
PME41	Droop as defined in Figure 23–18 during reception of test signal defined in Figure 23–19	23.5.1.3.3	M		Less than 6%
PME42	Receiver common-mode rejection; effect of E_{cm} as shown in Figure 23–24	23.5.1.3.4	M		Receiver meets 23.5.1.3.1
PME43	E_{cm} used for common-mode rejection tests	23.5.1.3.4	M		25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns
PME44	Receiver faults; response to indefinite application of short circuits	23.5.1.3.5	M		Withstand without damage and resume operation after fault is removed

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23.12.4.13 PMA electrical requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME45	Receiver faults; response to 1000 V common mode impulse per IEC 60060	23.5.1.3.5	M		Withstand without damage
PME46	Shape of impulse used for common mode impulse test	23.5.1.3.5	M		0.3/50 μs as defined in IEC 60060
PME47	Receiver properly receives data have a worst-case ternary symbol range	23.5.1.3.6	M		25.00 MHz ± 0.01%
PME48	Steady-state current consumption	23.5.2	MII:M		0.75 A maximum
PME49	PHY operating voltage range	23.5.2	MII:M		Includes worst voltage available from MII
PME50	Extraneous signals induced on the MII control circuits during normal power-up and power-down	23.5.2	M		None

23.12.4.14 Characteristics of the link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LNK1	Cable used	23.6.1	INS:M		Four pairs of balanced cabling, Category 3 or better, with a nominal characteristic impedance of 100 Ω
LNK2	Source and load impedance used for cable testing (unless otherwise specified)	23.6.2	INS:M		100 Ω
LNK3	Insertion loss of simplex link segment	23.6.2.1	INS:M		Less than 12 dB
LNK4	Source and load impedances used to measure cable insertion loss	23.6.2.1	INS:M		Meet 23.5.1.2.4 and 23.5.1.3.3
LNK5	Characteristic impedance over the range 2–12.5 MHz	23.6.2.2	INS:M		85–115 Ω
LNK6	NEXT loss between 2 and 12.5 MHz	23.6.2.3.1	INS:M		Greater than $24.5 - 15\log\left(\frac{f}{12.5}\right)$ dB
LNK7	MDNEXT loss between 2 and 12.5 MHz	23.6.2.3.2	INS:M		Greater than $21.4 - 15\log\left(\frac{f}{12.5}\right)$ dB

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23.12.4.14 Characteristics of the link segment *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
LNK8	ELFEXT loss between 2 and 12.5 MHz	23.6.2.3.3	INS:M		Greater than $23.1 - 15\log\left(\frac{f}{12.5}\right)$ dB
LNK9	MDELFEXT loss between 2 and 12.5 MHz	23.6.2.3.4	INS:M		Greater than $20.9 - 15\log\left(\frac{f}{12.5}\right)$ dB
LNK10	Propagation delay	23.6.2.4.1	INS:M		Less than 570 ns
LNK11	Propagation delay per meter	23.6.2.4.2	INS:M		Less than 5.7 ns/m
LNK12	Skew	23.6.2.4.3	INS:M		Less than 50 ns
LNK13	Variation in skew once installed	23.6.2.4.3	INS:M		Less than ± 10 ns, within constraint of LNK8
LNK14	Noise level	23.6.3	INS:M		Such that objective error rate is met
LNK15	MDNEXT noise	23.6.3.1	INS:M		Less than 325 mVp
LNK16	MDFEXT noise	23.6.3.2	INS:M		Less than 87 mVp
LNK17	Maximum length of Category 5, 25-pair jumper cables	23.6.3.2	INS:M		10 m

23.12.4.15 MDI requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MDI1	MDI connector	23.7.1	M		IEC 60603-7: 1990
MDI2	Connector used on PHY	23.7.1	M		Jack (as opposed to plug)
MDI3	Crossover in every twisted-pair link	23.7.2	INS:M		
MDI4	MDI connector that implements the crossover function	23.7.2	XVR:M		Marked with “X”

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23.12.4.16 General safety and environmental requirements

Item	Feature	Subclause	Status	Support	Value/Comment
SAF1	Conformance to safety specifications	23.9.1	M		IEC 60950: 1991
SAF2	Installation practice	23.9.2.1	INS:M		Sound practice, as defined by applicable local codes
SAF3	Any safety grounding path for an externally connected PHY shall be provided through the circuit ground of the MII connection	23.9.2.2	M		
SAF4	Care taken during installation to ensure that noninsulated network cable conductors do not make electrical contact with unintended conductors or ground	23.9.2.3	INS:M		
SAF5	Application of voltages specified in 23.9.2.4 does not result in any safety hazard	23.9.2.4	M		
SAF6	Conformance with local and national codes for the limitation of electromagnetic interference	23.9.3.1	INS:M		

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23.12.4.17 Timing requirements

Item	Feature	Subclause	Status	Support	Value/Comment
TIM1	PMA_OUT	23.11.3	PMA:M		1 to 9.5 BT
TIM2	TEN_PMA + PMA_OUT	23.11.3	PCS:M		7 to 17.5 BT
TIM3	TEN_CRS	23.11.3	PCS:M		0 to +4 BT
TIM4	NOT_TEN_CRS	23.11.3	PCS:M		28 to 36 BT
TIM5	RX_PMA_CARRIER	23.11.3	PMA:M		Less than 15.5 BT
TIM6	RX_CRS	23.11.3	PCS:M		Less than 27.5 BT
TIM7	RX_NOT_CRS	23.11.3	PCS:M		0 to 51.5 BT
TIM8	FAIRNESS	23.11.3	PCS:M		0 to 28 BT
TIM9	RX_PMA_DATA	23.11.3	PMA:M		67 to 90.5 BT
TIM10	EOP_CARRIER_STATUS	23.11.3	M		51 to 74.5 BT
TIM11	EOC_CARRIER_STATUS	23.11.3	M		3 to 50.5 BT
TIM12	RX_RXDV	23.11.3	PCS:M		81 to 114.5 BT
TIM13	RX_PMA_ERROR	23.11.3	M		Allowed limits equal the actual RX_PMA_DATA time for the device under test plus from 0 to 20 BT
TIM14	RX_COL	23.11.3	PCS:M		Less than 27.5 BT
TIM15	RX_NOT_COL	23.11.3	PCS:M		Less than 51.5 BT
TIM16	TX_NOT_COL	23.11.3	PCS:M		Less than 36 BT
TIM17	TX_SKEW	23.11.3	M		Less than 0.5 BT
TIM18	CRS_PMA_DATA	23.11.3	PMA:M		Less than 78.5 BT
TIM19	COL_to_BI_D3/4_OFF	23.11.3	PMA:M		Less than 40 BT

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24. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X

24.1 Overview

24.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) sublayer that are common to a family of 100 Mb/s Physical Layer implementations, collectively known as 100BASE-X. There are currently two embodiments within this family: 100BASE-TX and 100BASE-FX. 100BASE-TX specifies operation over two copper media: two pairs of shielded twisted-pair cable (STP) and two pairs of unshielded twisted-pair cable (Category 5 UTP).[5] 100BASE-FX specifies operation over two optical fibers. The term 100BASE-X is used when referring to issues common to both 100BASE-TX and 100BASE-FX.

100BASE-X leverages the Physical Layer standards of ISO/IEC 9314 and ANSI X3T12 (FDDI) through the use of their Physical Medium Dependent (PMD) sublayers, including their Medium Dependent Interfaces (MDI). For example, ANSI X3.263-1995 (TP-PMD) defines a 125 Mb/s, full duplex signaling system for twisted-pair wiring that forms the basis for 100BASE-TX as defined in Clause 25. Similarly, ISO/IEC 9314-3: 1990 defines a system for transmission on optical fiber that forms the basis for 100BASE-FX as defined in Clause 26.

100BASE-X maps the interface characteristics of the FDDI PMD sublayer (including MDI) to the services expected by the CSMA/CD MAC. 100BASE-X can be extended to support any other full duplex medium requiring only that the medium be PMD compliant.

24.1.2 Objectives

The following are the objectives of 100BASE-X:

a) Support the CSMA/CD MAC in the half duplex and the full duplex modes of operation.
b) Support the 100BASE-T MII, repeater, and optional Auto-Negotiation.
c) Provide 100 Mb/s data rate at the MII.
d) Support cable plants using Category 5 UTP, 150 Ω STP or optical fiber, compliant with ISO/IEC 11801.
e) Allow for a nominal network extent of 200–400 m, including
   1) Unshielded twisted-pair links of 100 m;
   2) Two repeater networks of approximately 200 m span;
   3) One repeater network of approximately 300 m span (using fiber); and
   4) DTE/DTE links of approximately 400 m (half duplex mode using fiber) and 2 km (full duplex mode using multimode fiber).
f) Preserve full duplex behavior of underlying PMD channels.

24.1.3 Relationship of 100BASE-X to other standards

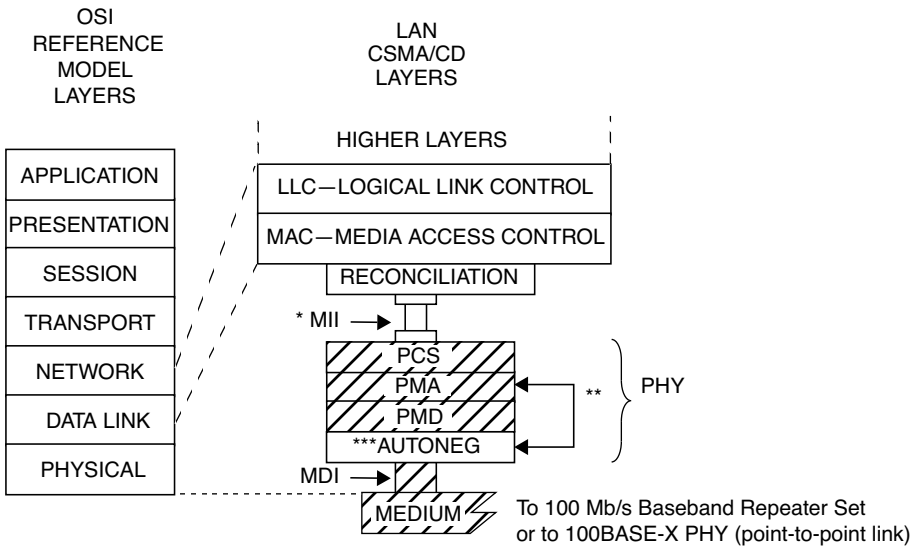
Figure 24–1 depicts the relationships among the 100BASE-X sublayers (shown shaded), other 100BASE-T sublayers, the CSMA/CD MAC, and the IEEE 802.2 LLC.

[5]ISO/IEC 11801 makes no distinction between shielded or unshielded twisted-pair cables, referring to both as balanced cables.

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MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* MII is optional.
** AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indicate.
*** AUTONEG is optional.

Figure 24–1—Type 100BASE-X PHY relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

24.1.4 Summary of 100BASE-X sublayers

The following provides an overview of the 100BASE-X sublayers that are embodied in the 100BASE-X Physical sublayer (PHY).[6]

24.1.4.1 Physical Coding Sublayer (PCS)

The PCS interface is the Media Independent Interface (MII) that provides a uniform interface to the Reconciliation sublayer for all 100BASE-T PHY implementations (e.g., 100BASE-X and 100BASE-T4). 100BASE-X, as other 100BASE-T PHYs, is modeled as providing services to the MII. This is similar to the use of an AUI interface.

The 100BASE-X PCS realizes all services required by the MII, including:

a) Encoding (decoding) of MII data nibbles to (from) five-bit code-groups (4B/5B);
b) Generating Carrier Sense and Collision Detect indications;
c) Serialization (deserialization) of code-groups for transmission (reception) on the underlying serial PMA, and
d) Mapping of Transmit, Receive, Carrier Sense and Collision Detection between the MII and the underlying PMA.

[6] The 100BASE-X PHY should not be confused with the FDDI PHY, which is a sublayer functionally aligned to the 100BASE-T PCS.

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24.1.4.2 Physical Medium Attachment (PMA) sublayer

The PMA provides a medium-independent means for the PCS and other bit-oriented clients (e.g., repeaters) to support the use of a range of physical media. The 100BASE-X PMA performs the following functions:

a) Mapping of transmit and receive code-bits between the PMA's client and the underlying PMD;
b) Generating a control signal indicating the availability of the PMD to a PCS or other client, also synchronizing with Auto-Negotiation when implemented;
c) Optionally, generating indications of activity (carrier) and carrier errors from the underlying PMD;
d) Optionally, sensing receive channel failures and transmitting the Far-End Fault Indication; and detecting the Far-End Fault Indication; and
e) Recovery of clock from the NRZI data supplied by the PMD.

24.1.4.3 Physical Medium Dependent (PMD) sublayer

100BASE-X uses the FDDI signaling standards ISO/IEC 9314-3: 1990 and ANSI X3.263-1995 (TP-PMD). These signaling standards, called PMD sublayers, define 125 Mb/s, full duplex signaling systems that accommodate multi-mode optical fiber, STP and UTP wiring. 100BASE-X uses the PMDs specified in these standards with the PMD Service Interface specified in 24.4.1.

The MDI, logically subsumed within the PMD, provides the actual medium attachment, including connectors, for the various supported media.

100BASE-X does not specify the PMD and MDI other than including the appropriate standard by reference along with the minor adaptations necessary for 100BASE-X. Figure 24–2 depicts the relationship between 100BASE-X and the PMDs of ISO/IEC 9314-3: 1990 (for 100BASE-FX) and ANSI X3.263-1995 (for 100BASE-TX). The PMDs (and MDIs) for 100BASE-TX and 100BASE-FX are specified in subsequent clauses of this standard.

24.1.5 Inter-sublayer interfaces

There are a number of interfaces employed by 100BASE-X. Some (such as the PMA and PMD interfaces) use an abstract service model to define the operation of the interface. The PCS Interface is defined as a set of physical signals, in a medium-independent manner (MII). Figure 24–3 depicts the relationship and mapping of the services provided by all of the interfaces relevant to 100BASE-X.

It is important to note that, while this specification defines interfaces in terms of bits, nibbles, and code-groups, implementations may choose other data path widths for implementation convenience. The only exceptions are: a) the MII, which, when implemented, uses a nibble-wide data path as specified in Clause 22, and b) the MDI, which uses a serial, physical interface.

24.1.6 Functional block diagram

Figure 24–4 provides a functional block diagram of the 100BASE-X PHY.

24.1.7 State diagram conventions

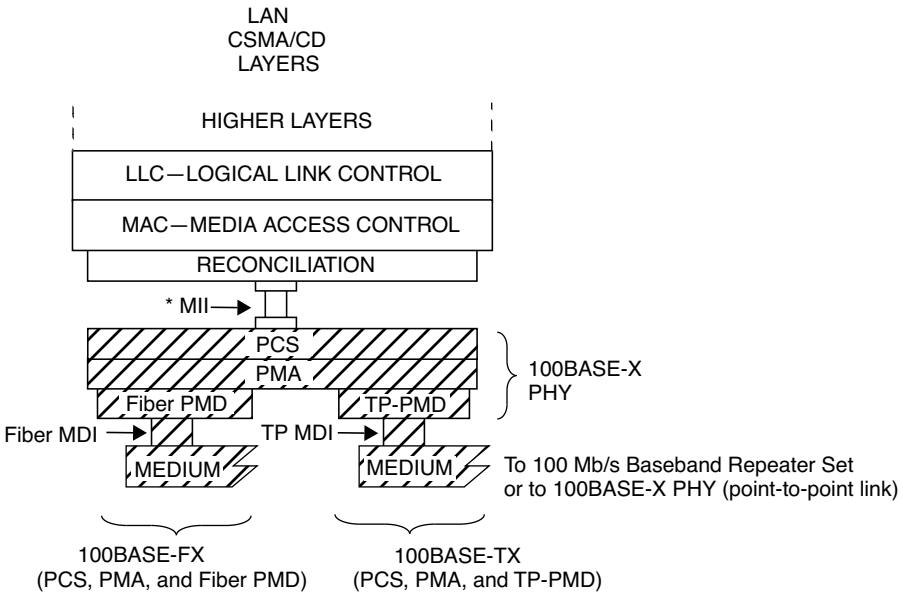
The body of this standard is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5; state diagram timers follow the conventions of 14.2.3.2.

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MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
Fiber PMD = PHYSICAL MEDIUM DEPENDENT SUBLAYER FOR FIBER
TP-PMD = PHYSICAL MEDIUM DEPENDENT SUBLAYER FOR TWISTED PAIRS

NOTE—The PMD sublayers are mutually independent.
* MII is optional.

Figure 24–2—Relationship of 100BASE-X and the PMDs

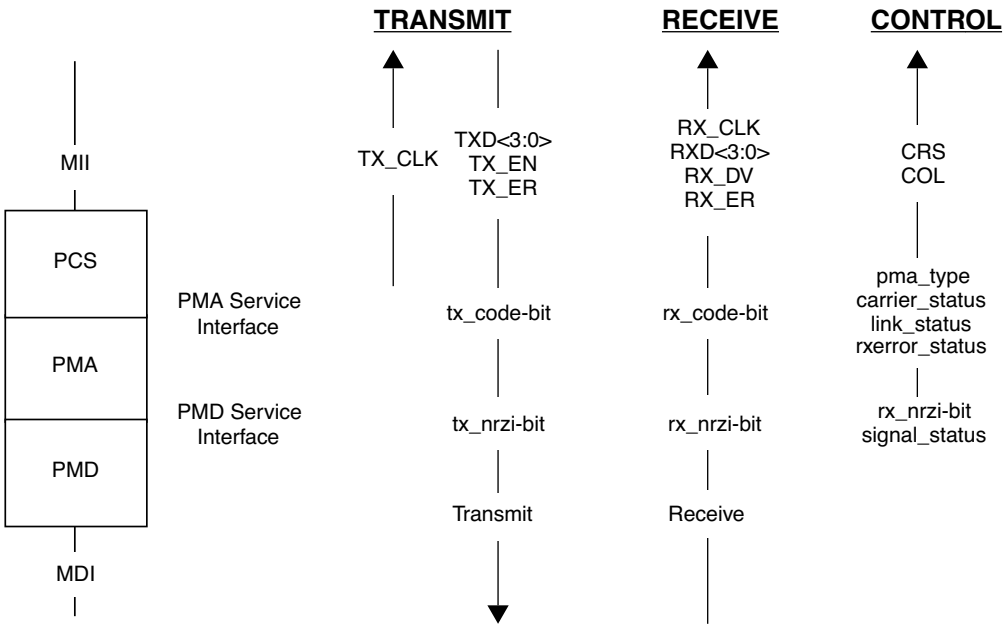


Figure 24–3—Interface mapping

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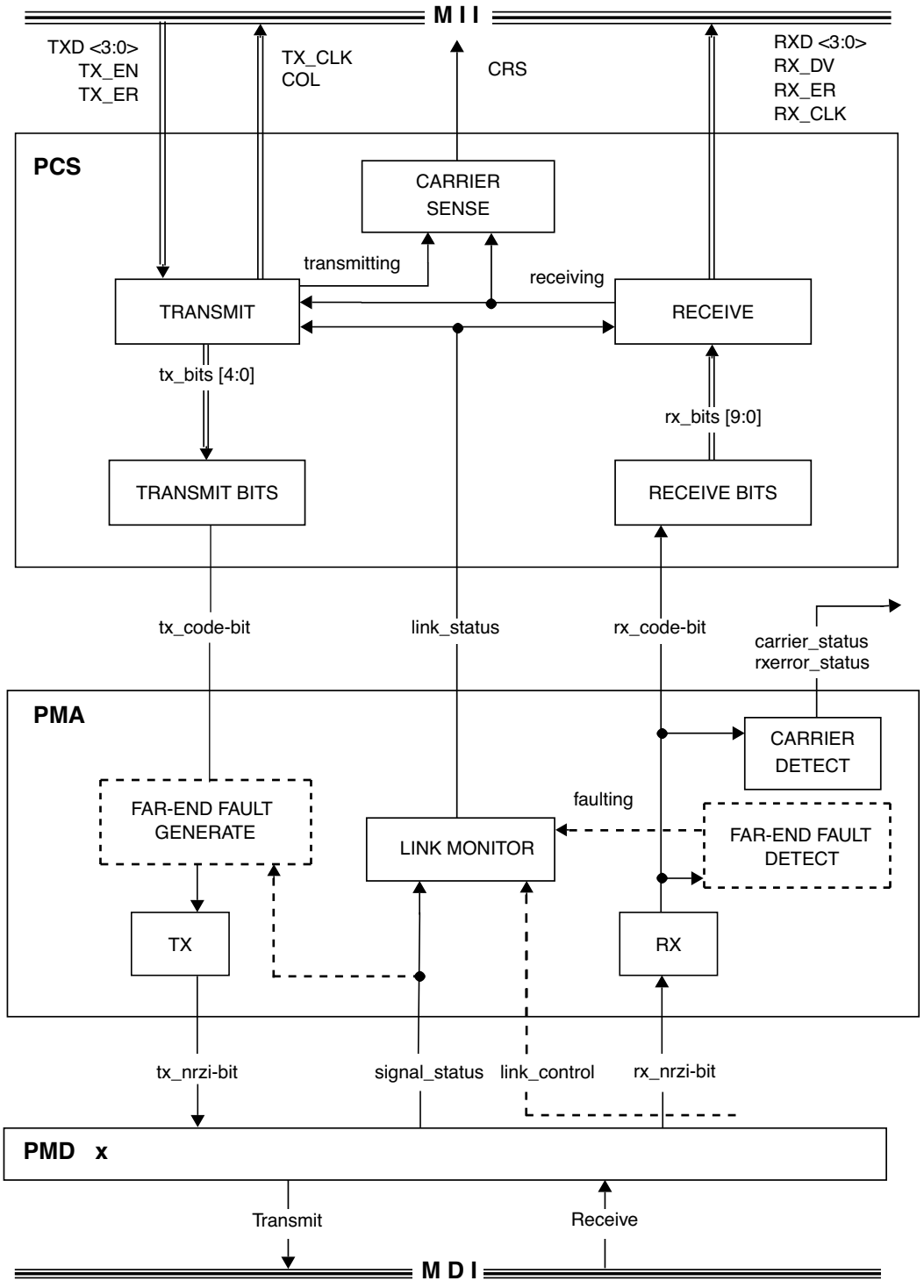


Figure 24–4—Functional block diagram

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24.2 Physical Coding Sublayer (PCS)

24.2.1 Service Interface (MII)

The PCS Service Interface allows the 100BASE-X PCS to transfer information to and from the MAC (via the Reconciliation sublayer) or other PCS client, such as a repeater. The PCS Service Interface is precisely defined as the Media Independent Interface (MII) in Clause 22.

In this clause, the setting of MII variables to TRUE or FALSE is equivalent, respectively, to “asserting” or “de-asserting” them as specified in Clause 22.

24.2.2 Functional requirements

The PCS comprises the Transmit, Receive, and Carrier Sense functions for 100BASE-T. In addition, the collisionDetect signal required by the MAC (COL on the MII) is derived from the PMA code-bit stream. The PCS shields the Reconciliation sublayer (and MAC) from the specific nature of the underlying channel. Specifically for receiving, the 100BASE-X PCS passes to the MII a sequence of data nibbles derived from incoming code-groups, each comprised of five code-bits, received from the medium. Code-group alignment and MAC packet delimiting is performed by embedding special non-data code-groups. The MII uses a nibble-wide, synchronous data path, with packet delimiting being provided by separate TX_EN and RX_DV signals. The PCS provides the functions necessary to map these two views of the exchanged data. The process is reversed for transmit.

The following provides a detailed specification of the functions performed by the PCS, which comprise five parallel processes (Transmit, Transmit Bits, Receive, Receive Bits, and Carrier Sense). Figure 24–4 includes a functional block diagram of the PCS.

The Receive Bits process accepts continuous code-bits via the PMA_UNITDATA.indicate primitive. Receive monitors these bits and generates RXD <3:0>, RX_DV and RX_ER on the MII, and the internal flag, receiving, used by the Carrier Sense and Transmit processes.

The Transmit process generates continuous code-groups based upon the TXD <3:0>, TX_EN, and TX_ER signals on the MII. These code-groups are transmitted by Transmit Bits via the PMA_UNITDATA.request primitive. The Transmit process generates the MII signal COL based on whether a reception is occurring simultaneously with transmission. Additionally, it generates the internal flag, transmitting, for use by the Carrier Sense process.

The Carrier Sense process asserts the MII signal CRS when either transmitting or receiving is TRUE. Both the Transmit and Receive processes monitor link_status via the PMA_LINK.indicate primitive, to account for potential link failure conditions.

24.2.2.1 Code-groups

The PCS maps four-bit nibbles from the MII into five-bit code-groups, and vice versa, using a 4B/5B block coding scheme. A code-group is a consecutive sequence of five code-bits interpreted and mapped by the PCS. Implicit in the definition of a code-group is an establishment of code-group boundaries by an alignment function within the PCS Receive process. It is important to note that, with the sole exception of the SSD, which is used to achieve alignment, code-groups are undetectable and have no meaning outside the 100BASE-X physical protocol data unit, called a “stream.”

The coding method used, derived from ISO/IEC 9314-1, provides

a) Adequate codes (32) to provide for all Data code-groups (16) plus necessary control code-groups;

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b) Appropriate coding efficiency (4 data bits per 5 code-bits; 80%) to effect a 100 Mb/s Physical Layer interface on a 125 Mb/s physical channel as provided by FDDI PMDs; and
c) Sufficient transition density to facilitate clock recovery (when not scrambled).

Table 24–1 specifies the interpretation assigned to each five bit code-group, including the mapping to the nibble-wide (TXD or RXD) Data signals on the MII. The 32 code-groups are divided into four categories, as shown.

For clarity in the remainder of this clause, code-group names are shown between /slashes/. Code-group sequences are shown in succession, e.g.: /1/2/....

The indicated code-group mapping is identical to ISO/IEC 9314-1: 1989, with four exceptions:

a) The FDDI term *symbol* is avoided in order to prevent confusion with other 100BASE-T terminology. In general, the term *code-group* is used in its place.
b) The /S/ and /Q/ code-groups are not used by 100BASE-X and are interpreted as INVALID.
c) The /R/ code-group is used in 100BASE-X as the second code-group of the End-of-Stream delimiter rather than to indicate a Reset condition.
d) The /H/ code-group is used to propagate receive errors rather than to indicate the Halt Line State.

24.2.2.1.1 Data code-groups

A Data code-group conveys one nibble of arbitrary data between the MII and the PCS. The sequence of Data code-groups is arbitrary, where any Data code-group can be followed by any other Data code-group. Data code-groups are coded and decoded but not interpreted by the PCS. Successful decoding of Data code-groups depends on proper receipt of the Start-of-Stream delimiter sequence, as defined in Table 24–1.

24.2.2.1.2 Idle code-groups

The Idle code-group (/I/) is transferred between streams. It provides a continuous fill pattern to establish and maintain clock synchronization. Idle code-groups are emitted from, and interpreted by, the PCS.

24.2.2.1.3 Control code-groups

The Control code-groups are used in pairs (/J/K/, /T/R/) to delimit MAC packets. Control code-groups are emitted from, and interpreted by, the PCS.

24.2.2.1.4 Start-of-Stream Delimiter (/J/K/)

A Start-of-Stream Delimiter (SSD) is used to delineate the boundary of a data transmission sequence and to authenticate carrier events. The SSD is unique in that it may be recognized independently of previously established code-group boundaries. The Receive function within the PCS uses the SSD to establish code-group boundaries. A SSD consists of the sequence /J/K/.

On transmission, the first 8 bits of the MAC preamble are replaced by the SSD, a replacement that is reversed on reception.

24.2.2.1.5 End-of-Stream delimiter (/T/R/)

An End-of-Stream delimiter (ESD) terminates all normal data transmissions. Unlike the SSD, an ESD cannot be recognized independent of previously established code-group boundaries. An ESD consists of the sequence /T/R/.

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Table 24–1—4B/5B code-groups

	PCS code-group [4:0] 4 3 2 1 0	Name	MII (TXD/RXD) <3:0> 3 2 1 0	Interpretation
DATA	1 1 1 1 0	0	0 0 0 0	Data 0
	0 1 0 0 1	1	0 0 0 1	Data 1
	1 0 1 0 0	2	0 0 1 0	Data 2
	1 0 1 0 1	3	0 0 1 1	Data 3
	0 1 0 1 0	4	0 1 0 0	Data 4
	0 1 0 1 1	5	0 1 0 1	Data 5
	0 1 1 1 0	6	0 1 1 0	Data 6
	0 1 1 1 1	7	0 1 1 1	Data 7
	1 0 0 1 0	8	1 0 0 0	Data 8
	1 0 0 1 1	9	1 0 0 1	Data 9
	1 0 1 1 0	A	1 0 1 0	Data A
	1 0 1 1 1	B	1 0 1 1	Data B
	1 1 0 1 0	C	1 1 0 0	Data C
	1 1 0 1 1	D	1 1 0 1	Data D
	1 1 1 0 0	E	1 1 1 0	Data E
	1 1 1 0 1	F	1 1 1 1	Data F
	1 1 1 1 1	I	undefined	IDLE; used as inter-stream fill code
CONTROL	1 1 0 0 0	J	0 1 0 1	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
	1 0 0 0 1	K	0 1 0 1	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
	0 1 1 0 1	T	undefined	End-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
	0 0 1 1 1	R	undefined	End-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
INVALID	0 0 1 0 0	H	Undefined	Transmit Error; used to force signaling errors
	0 0 0 0 0	V	Undefined	Invalid code
	0 0 0 0 1	V	Undefined	Invalid code
	0 0 0 1 0	V	Undefined	Invalid code
	0 0 0 1 1	V	Undefined	Invalid code
	0 0 1 0 1	V	Undefined	Invalid code
	0 0 1 1 0	V	Undefined	Invalid code
	0 1 0 0 0	V	Undefined	Invalid code
	0 1 1 0 0	V	Undefined	Invalid code
	1 0 0 0 0	V	Undefined	Invalid code
	1 1 0 0 1	V	Undefined	Invalid code

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24.2.2.1.6 Invalid code-groups

The /H/ code-group indicates that the PCS's client wishes to indicate a Transmit Error to its peer entity. The normal use of this indicator is for repeaters to propagate received errors. Transmit Error code-groups are emitted from the PCS, at the request of the PCS's client through the use of the TX_ER signal, as described in 24.2.4.2.

The presence of any invalid code-group on the medium, including /H/, denotes a collision artifact or an error condition. Invalid code-groups are not intentionally transmitted onto the medium by DTE's. The PCS indicates the reception of an Invalid code-group on the MII through the use of the RX_ER signal, as described in 24.2.4.4.

24.2.2.2 Encapsulation

The 100BASE-X PCS accepts frames from the MAC through the Reconciliation sublayer and MII. Due to the continuously signaled nature of the underlying PMA, and the encoding performed by the PCS, the 100BASE-X PCS encapsulates the MAC frame (100BASE-X Service Data Unit, SDU) into a Physical Layer stream (100BASE-X Protocol Data Unit, PDU).

Except for the two code-group SSD, data nibbles within the SDU (including the non-SSD portions of the MAC preamble and SFD) are not interpreted by the 100BASE-X PHY. The conversion from a MAC frame to a Physical Layer stream and back to a MAC frame is transparent to the MAC.

Figure 24–5 depicts the mapping between MAC frames and Physical Layer streams.

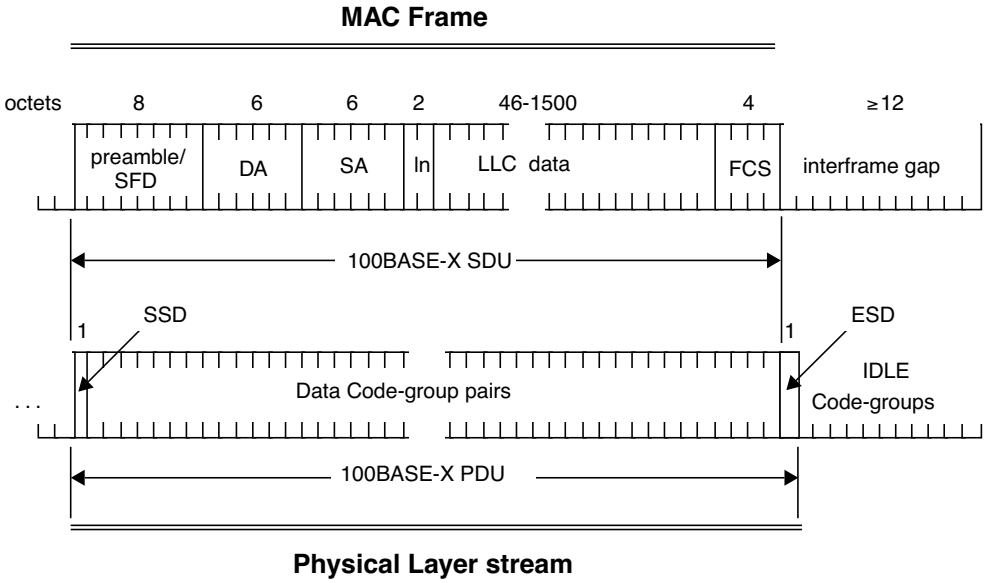


Figure 24–5—PCS encapsulation

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A properly formed stream can be viewed as comprising three elements:

a) *Start-of-Stream Delimiter.* The start of a Physical Layer stream is indicated by a SSD, as defined in 24.2.2.1. The SSD replaces the first octet of the preamble from the MAC frame and vice versa.
b) *Data Code-groups*. Between delimiters (SSD and ESD), the PCS conveys Data code-groups corresponding to the data nibbles of the MII. These Data code-groups comprise the 100BASE-X Service Data Unit (SDU). Data nibbles within the SDU (including those corresponding to the MAC preamble and SFD) are not interpreted by the 100BASE-X PCS.
c) *End-of-Stream Delimiter.* The end of a properly formed stream is indicated by an ESD, as defined in 24.2.2.1. The ESD is transmitted by the PCS following the de-assertion of TX_EN on the MII, which corresponds to the last data nibble composing the FCS from the MAC. It is transmitted during the period considered by the MAC to be the interframe gap (IFG). On reception, ESD is interpreted by the PCS as terminating the SDU.

Between streams, IDLE code-groups are conveyed between the PCS and PMA.

24.2.2.3 Data delay

The PCS maps a non-aligned code-bit data path from the PMA to an aligned, nibble-wide data path on the MII, both for Transmit and Receive. Logically, received bits must be buffered to facilitate SSD detection and alignment, coding translation, and ESD detection. These functions necessitate an internal PCS delay of at least two code-groups. In practice, alignment may necessitate even longer delays of the incoming code-bit stream.

When the MII is present as an exposed interface, the MII signals TX_CLK and RX_CLK, not depicted in the following state diagrams, shall be generated by the PCS in accordance with Clause 22.

24.2.2.4 Mapping between MII and PMA

Figure 24–6 depicts the mapping of the nibble-wide data path of the MII to the five-bit-wide code-groups (internal to the PCS) and the code-bit path of the PMA interface.

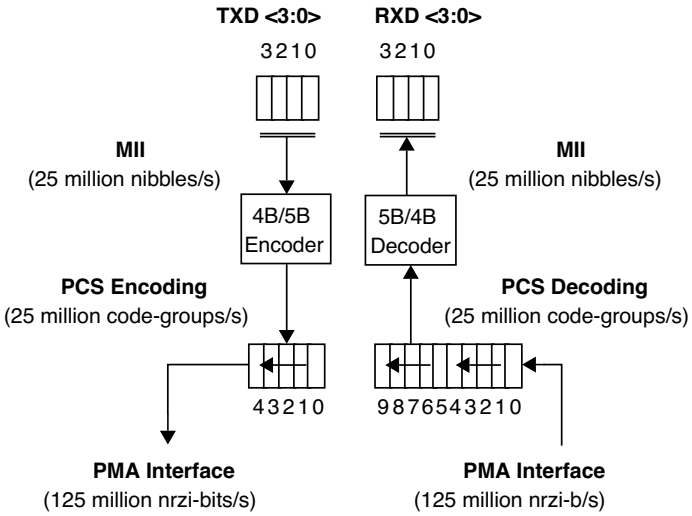


Figure 24–6—PCS reference diagram

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Upon receipt of a nibble from the MII, the PCS encodes it into a five-bit code-group, according to 24.2.2.1. Code-groups are serialized into code-bits and passed to the PMA for transmission on the underlying medium, according to Figure 24–6. The first transmitted code-bit of a code-group is bit 4, and the last code-bit transmitted is bit 0. There is no numerical significance ascribed to the bits within a code-group; that is, the code-group is simply a five-bit pattern that has some predefined interpretation.

Similarly, the PCS deserializes code-bits received from the PMA, according to Figure 24–6. After alignment is achieved, based on SSD detection, the PCS converts code-groups into MII data nibbles, according to 24.2.2.1.

24.2.3 State variables

24.2.3.1 Constants

DATA
: The set of 16 code-groups corresponding to valid DATA, as specified in 24.2.2.1. (In the Receive state diagram, the set operators $\in$ and $\notin$ are used to represent set membership and non-membership, respectively.)

ESD
: The code-group pair corresponding to the End-of-Stream delimiter, as specified in 24.2.2.1.

ESD1
: The code-group pair corresponding to the End-of-Stream delimiter, Part 1 (/T/), as specified in 24.2.2.1.

ESD2
: The code-group pair corresponding to the End-of-Stream delimiter, Part 2 (/R/), as specified in 24.2.2.1.

HALT
: The Transmit Error code-group (/H/), as specified in 24.2.2.1.

IDLE
: The IDLE code-group, as specified in 24.2.2.1.

IDLES
: A code-group pair comprised of /I/I/; /I/ as specified in 24.2.2.1.

SSD
: The code-group pair corresponding to the Start-of-Stream delimiter, as specified in 24.2.2.1.

SSD1
: The code-group corresponding to the Start-of-Stream delimiter, Part 1 (/J/), as specified in 24.2.2.1.

SSD2
: The code-group corresponding to the Start-of-Stream delimiter, Part 2 (/K/), as specified in 24.2.2.1.

24.2.3.2 Variables

In the following, values for the MII parameters are definitively specified in Clause 22.

COL
: The COL signal of the MII as specified in Clause 22.

CRS
: The CRS signal of the MII as specified in Clause 22.

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link_status
: The link_status parameter as communicated by the PMA_LINK.indicate primitive.

  Values: FAIL; the receive channel is not intact
  READY; the receive channel is intact and ready to be enabled by Auto-Negotiation
  OK; the receive channel is intact and enabled for reception

receiving
: A boolean set by the Receive process to indicate non-IDLE activity (after squelch). Used by the Carrier Sense process, and also interpreted by the Transmit process for indicating a collision.

  Values: TRUE; unsquelched carrier being received
  FALSE; carrier not being received

rx_bits [9:0]
: A vector of the 10 most recently received code-bits from the PMA as assembled by Receive Bits and processed by Receive. rx_bits [0] is the most recently received (newest) code-bit; rx_bits [9] is the least recently received code-bit (oldest). When alignment has been achieved, it contains the last two code-groups.

rx_code-bit
: The rx_code-bit parameter as communicated by the most recent PMA_UNITDATA.indicate primitive (that is, the value of the most recently received code-bit from the PMA).

RX_DV
: The RX_DV signal of the MII as specified in Clause 22. Set by the Receive process, RX_DV is also interpreted by the Receive Bits process as an indication that rx_bits is code-group aligned.

RX_ER
: The RX_ER signal of the MII as specified in Clause 22.

RXD <3:0>
: The RXD <3:0> signal of the MII as specified in Clause 22.

transmitting
: A boolean set by the Transmit Process to indicate a transmission in progress. Used by the Carrier Sense process.

  Values: TRUE; the PCS's client is transmitting
  FALSE; the PCS's client is not transmitting

tx_bits [4:0]
: A vector of code-bits representing a code-group prepared for transmission by the Transmit Process and transmitted to the PMA by the Transmit Bits process.

TX_EN
: The TX_EN signal of the MII as specified in Clause 22.

TX_ER
: The TX_ER signal of the MII as specified in Clause 22.

TXD <3:0>
: The TXD <3:0> signal of the MII as specified in Clause 22.

24.2.3.3 Functions

nibble DECODE (code-group)
: In Receive, this function takes as its argument a five-bit code-group and returns the corresponding MII RXD <3:0> nibble, per Table 24–1.

code-group ENCODE (nibble)
: In the Transmit process, this function takes as its argument an MII TXD <3:0> nibble, and returns the corresponding five-bit code-group per Table 24–1.

SHIFTLEFT (rx_bits)
: In Receive Bits, this function shifts rx_bits left one bit placing rx_bits [8] in rx_bits [9], rx_bits [7] in rx_bits [8] and so on until rx_bits [1] gets rx_bits [0].

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24.2.3.4 Timers

code-bit_timer

In the Transmit Bits process, the timer governing the output of code-bits from the PCS to the PMA and thereby to the medium with a nominal 8 ns period. This timer shall be derived from a fixed frequency oscillator with a base frequency of 125 MHz ± 0.005% and phase jitter above 20 kHz less than ± 8°.

24.2.3.5 Messages

gotCodeGroup.indicate

A signal sent to the Receive process by the Receive Bits process after alignment has been achieved signifying completion of reception of the next code-group in rx_bits(4:0), with the preceding code-group moved to rx_bits [9:5]. rx_bits [9:5] may be considered as the "current" code-group.

PMA_UNITDATA.indicate (rx_code-bit)

A signal sent by the PMA signifying that the next code-bit from the medium is available in rx_code-bit.

sentCodeGroup.indicate

A signal sent to the Transmit process from the Transmit Bits process signifying the completion of transmission of the code-group in tx_bits [4:0].

24.2.4 State diagrams

24.2.4.1 Transmit Bits

Transmit Bits is responsible for taking code-groups prepared by the Transmit process and transmitting them to the PMA using PMA_UNITDATA.request, the frequency of which determines the transmit clock. Transmit deposits these code-groups in tx_bits with Transmit Bits signaling completion of a code-group transmission with sentCodeGroup.indicate.

The PCS shall implement the Transmit Bits process as depicted in Figure 24–7 including compliance with the associated state variables as specified in 24.2.3.

24.2.4.2 Transmit

The Transmit process sends code-groups to the PMA via tx_bits and the Transmit Bits process. When initially invoked, and between streams (delimited by TX_EN on the MII), the Transmit process sources continuous Idle code-groups (/I/) to the PMA. Upon the assertion of TX_EN by the MII, the Transmit process passes an SSD (/J/K/) to the PMA, ignoring the TXD <3:0> nibbles during these two code-group times. Following the SSD, each TXD <3:0> nibble is encoded into a five-bit code-group until TX_EN is deasserted. If, while TX_EN is asserted, the TX_ER signal is asserted, the Transmit process passes Transmit Error code-groups (/H/) to the PMA. Following the de-assertion of TX_EN, an ESD (/T/R/) is generated, after which the transmission of Idle code-groups is resumed by the IDLE state.

Collision detection is implemented by noting the occurrence of carrier receptions during transmissions, following the model of 10BASE-T. The indication of link_status ≠ OK by the PMA at any time causes an immediate transition to the IDLE state and supersedes any other Transmit process operations.

The PCS shall implement the Transmit process as depicted in Figure 24–8 including compliance with the associated state variables as specified in 24.2.3.

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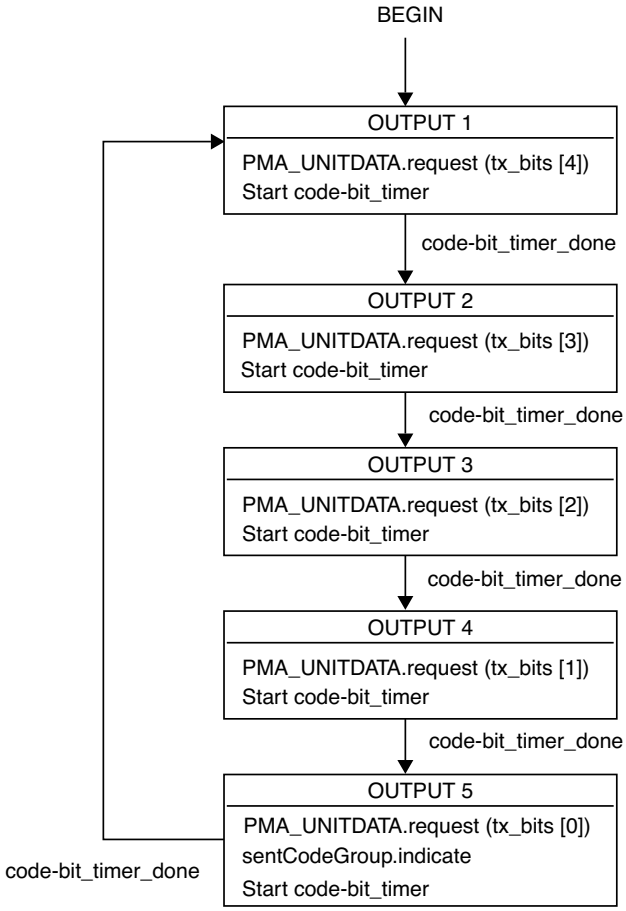


Figure 24–7—Transmit Bits state diagram

24.2.4.3 Receive Bits

The Receive Bits process collects code-bits from the PMA interface passing them to the Receive process via rx_bits. rx_bits [9:0] represents a sliding, 10-bit window on the PMA code-bits, with newly received code-bits from the PMA (rx_code-bit) being shifted into rx_bits [0]. This is depicted in Figure 24–9. Bits are collected serially until Receive indicates alignment by asserting RX_DV, after which Receive Bits signals Receive for every five code-bits accumulated. Serial processing resumes with the de-assertion of RX_DV.

The PCS shall implement the Receive Bits process as depicted in Figure 24–10 including compliance with the associated state variables as specified in 24.2.3.

24.2.4.4 Receive

The Receive process state machine can be viewed as comprising two sections: prealigned and aligned. In the prealigned states, IDLE, CARRIER DETECT, and CONFIRM K, the Receive process is waiting for an indication of channel activity followed by a SSD. After successful alignment, the incoming code-groups are decoded while waiting for stream termination.

24.2.4.4.1 Detecting channel activity

In a DTE operating in half duplex mode, the detection of activity on the underlying channel is used both by the MAC (via the MII CRS signal and the Reconciliation sublayer) for deferral purposes, and by the

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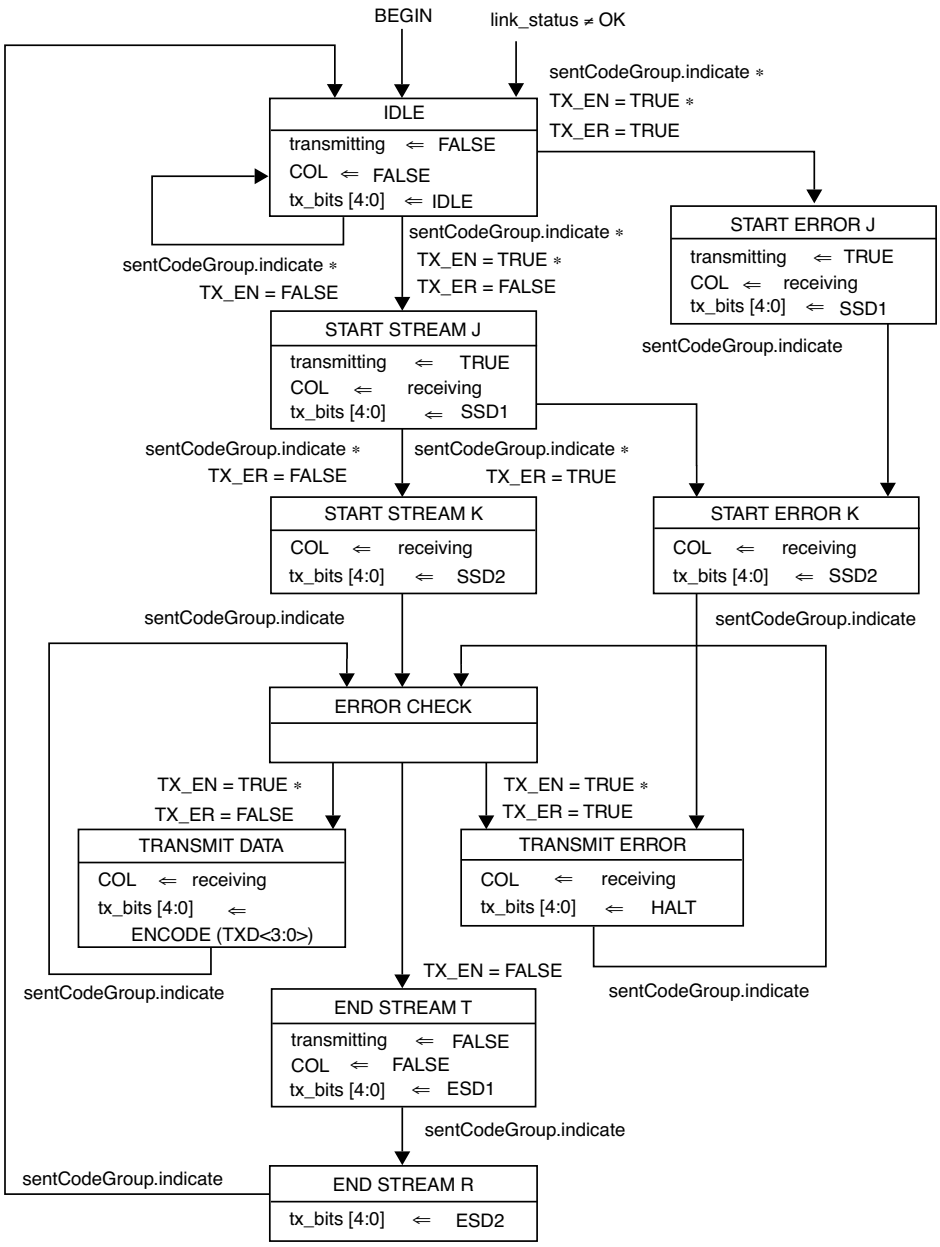


Figure 24–8—Transmit state diagram

Transmit process for collision detection. Activity, signaled by the assertion of receiving, is indicated by the receipt of two non-contiguous ZEROS within any 10 code-bits of the incoming code-bit stream.

24.2.4.4.2 Code-group alignment

After channel activity is detected, the Receive process first aligns the incoming code-bits on code-group boundaries for subsequent data decoding. This is achieved by scanning the rx_bits vector for a SSD (/J/K/). The MII RX_DV signal remains deasserted during this time, which ensures that the Reconciliation sublayer will ignore any signals on RXD <3:0>. Detection of the SSD causes the Receive process to enter the START OF STREAM J state.

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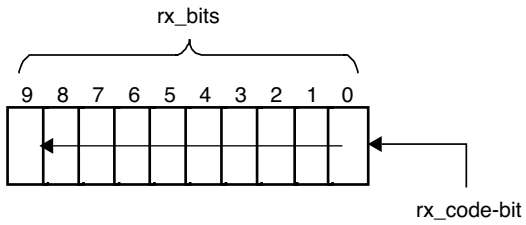


Figure 24–9—Receive Bits reference diagram

Well-formed streams contain SSD (/J/K/) in place of the first eight preamble bits. In the event that something else is sensed immediately following detection of carrier, a False Carrier Indication is signaled to the MII by asserting RX_ER and setting RXD to 1110 while RX_DV remains de-asserted. The associated carrier event, as terminated by 10 ONEs, is otherwise ignored.

24.2.4.4.3 Stream decoding

The Receive process substitutes a sequence of alternating ONE and ZERO data-bits for the SSD, which is consistent with the preamble pattern expected by the MAC.

The Receive process then performs the DECODE function on the incoming code-groups, passing decoded data to the MII, including those corresponding to the remainder of the MAC preamble and SFD. The MII signal RX_ER is asserted upon decoding any code-group following the SSD that is neither a valid Data code-group nor a valid stream termination sequence.

24.2.4.4.4 Stream termination

There are two means of effecting stream termination in the Receive process (Figure 24–11).

A normal stream termination is caused by detection of an ESD (/T/R/) in the rx_bits vector. In order to preserve the ability of the MAC to properly delimit the FCS at the end of the frame (that is, to avoid incorrect AlignmentErrors in the MAC) the internal signal receiving (and through it, the MII CRS signal, per Clause 22) is de-asserted immediately following the last code-bit in the stream that maps to the FCS. Note that the condition link_status ≠ OK during stream reception (that is, when receiving = TRUE) causes an immediate transition to the LINK FAILED state and supersedes any other Receive process operations.

A premature stream termination is caused by the detection of two Idle code-groups (/I/I) in the rx_bits vector prior to an ESD. Note that RX_DV remains asserted during the nibble corresponding to the first five contiguous ONEs while RX_ER is signaled on the MII. RX_ER is also asserted in the LINK FAILED state, which ensures that RX_ER remains asserted for sufficient time to be detected.

Stream termination causes a transition to the IDLE state.

The PCS shall implement the Receive process as depicted in Figure 24–11 including compliance with the associated state variables as specified in 24.2.3.

24.2.4.5 Carrier Sense

The Carrier Sense process generates the signal CRS on the MII, which (via the Reconciliation sublayer) a MAC operating in half duplex mode uses for deferral. The process operates by performing a logical OR operation on the internal messages receiving and transmitting, generated by the Receive and Transmit processes, respectively.

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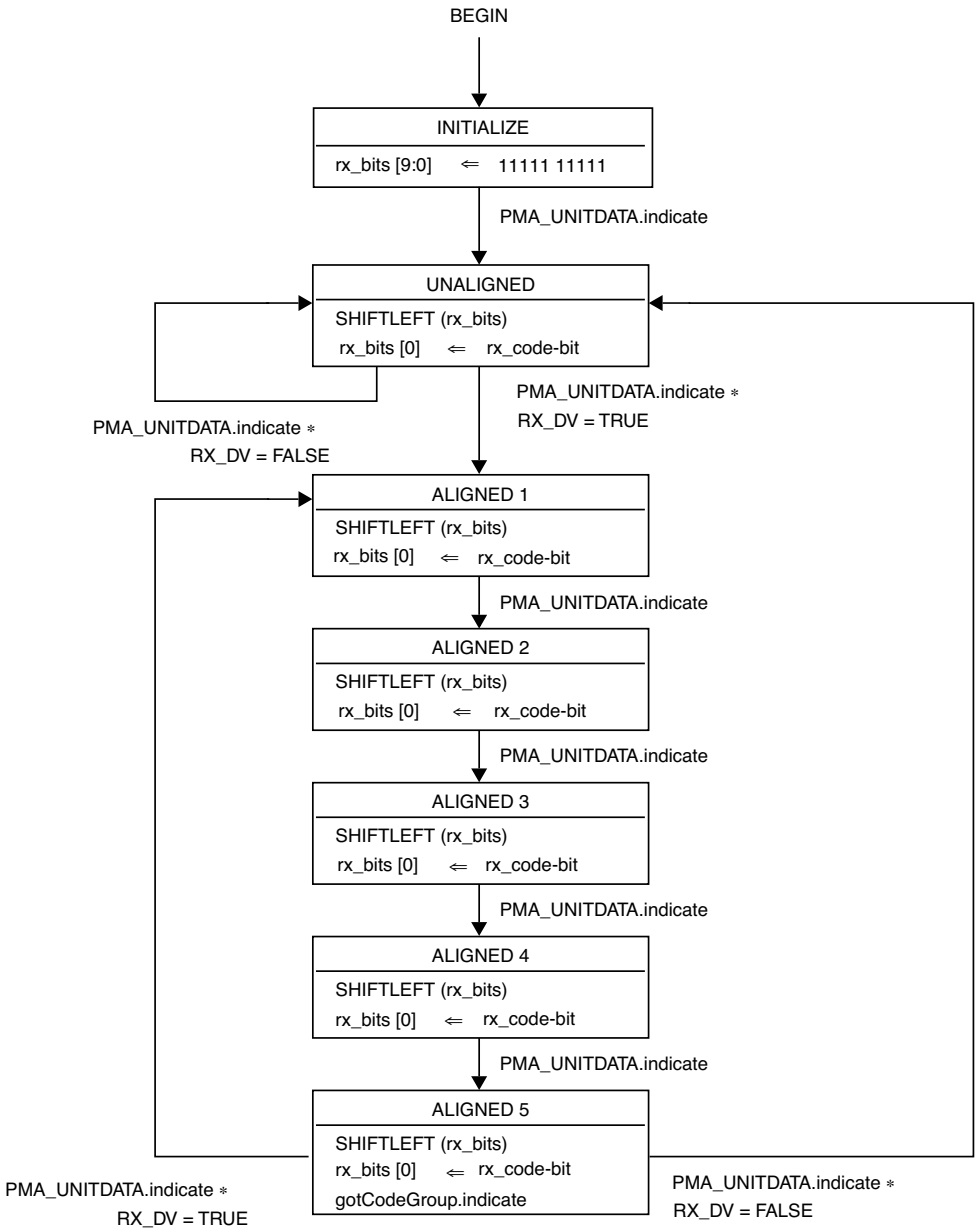


Figure 24–10—Receive Bits state diagram

The PCS shall implement the Carrier Sense process as depicted in Figure 24–12 including compliance with the associated state variables as specified in 24.2.3.

24.3 Physical Medium Attachment (PMA) sublayer

24.3.1 Service interface

The following specifies the service interface provided by the PMA to the PCS or another client, such as a repeater. These services are described in an abstract manner and do not imply any particular implementation.

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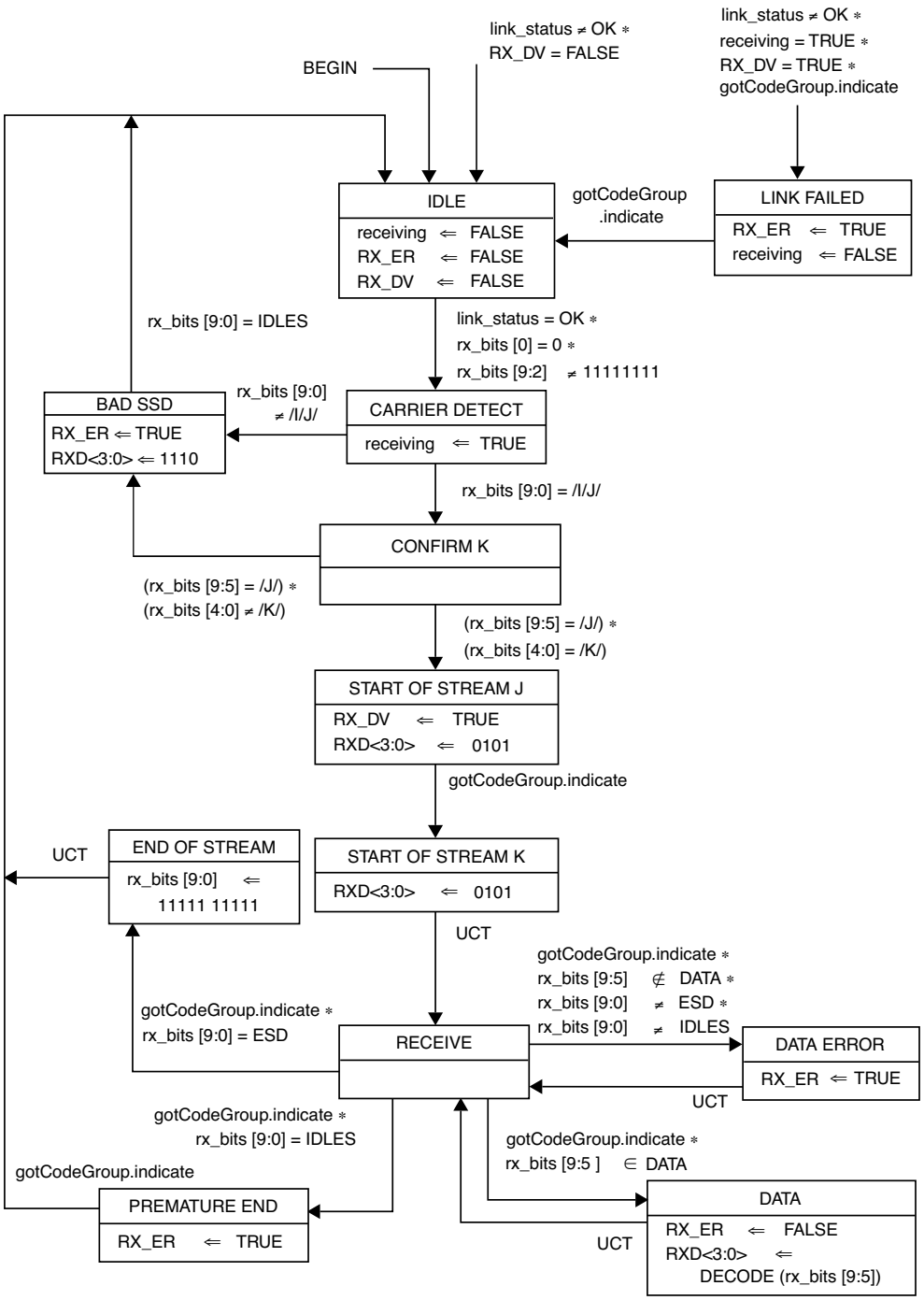


Figure 24–11—Receive state diagram

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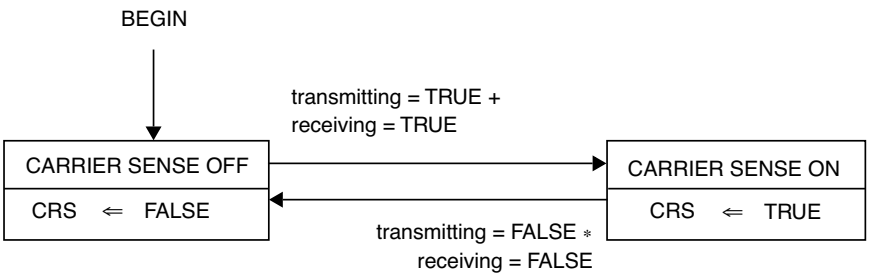


Figure 24–12—Carrier Sense state diagram

The PMA Service Interface supports the exchange of code-bits between the PCS and/or Repeater entities. The PMA converts code-bits into NRZI format and passes these to the PMD, and vice versa. It also generates additional status indications for use by its client.

The following primitives are defined:

PMA_TYPE.indicate
PMA_UNITDATA.request
PMA_UNITDATA.indicate
PMA_CARRIER.indicate
PMA_LINK.indicate
PMA_LINK.request
PMA_RXERROR.indicate

24.3.1.1 PMA_TYPE.indicate

This primitive is generated by the PMA to indicate the nature of the PMA instantiation. The purpose of this primitive is to allow clients to support connections to the various types of 100BASE-T PMA entities in a generalized manner.

24.3.1.1.1 Semantics of the service primitive

PMA_TYPE.indicate (pma_type)

The pma_type parameter for use with a 100BASE-X PMA is “X”.

24.3.1.1.2 When generated

The PMA continuously generates this primitive to indicate the value of pma_type.

24.3.1.1.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.1.2 PMA_UNITDATA.request

This primitive defines the transfer of data (in the form of code-bits) from the PMA’s client to the PMA.

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24.3.1.2.1 Semantics of the service primitive

PMA_UNITDATA.request (tx_code-bit)

This primitive defines the transfer of data (in the form of code-bits) from the PCS or other client to the PMA. The tx_code-bit parameter can take one of two values: ONE or ZERO.

24.3.1.2.2 When generated

The PCS or other client continuously sends, at a nominal 125 Mb/s rate, the appropriate code-bit for transmission on the medium.

24.3.1.2.3 Effect of receipt

Upon receipt of this primitive, the PMA generates a PMD_UNITDATA.request primitive, requesting transmission of the indicated code-bit, in NRZI format (tx_nrzi-bit), on the MDI.

24.3.1.3 PMA_UNITDATA.indicate

This primitive defines the transfer of data (in the form of code-bits) from the PMA to the PCS or other client.

24.3.1.3.1 Semantics of the service primitive

PMA_UNITDATA.indicate (rx_code-bit)

The data conveyed by PMA_UNITDATA.indicate is a continuous code-bit sequence at a nominal 125 Mb/s rate. The rx_code-bit parameter can take one of two values: ONE or ZERO.

24.3.1.3.2 When generated

The PMA continuously sends code-bits to the PCS or other client corresponding to the PMD_UNITDATA.indicate primitives received from the PMD.

24.3.1.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.1.4 PMA_CARRIER.indicate

This primitive is generated by the PMA to indicate that a non-squelched, non-IDLE code-bit sequence is being received from the PMD. The purpose of this primitive is to give clients the earliest reliable indication of activity on the underlying continuous-signaling channel.

24.3.1.4.1 Semantics of the service primitive

PMA_CARRIER.indicate (carrier_status)

The carrier_status parameter can take on one of two values, ON or OFF, indicating whether a non-squelched, non-IDLE code-bit sequence (that is, carrier) is being received (ON) or not (OFF).

24.3.1.4.2 When generated

The PMA generates this primitive to indicate a change in the value of carrier_status.

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24.3.1.4.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.1.5 PMA_LINK.indicate

This primitive is generated by the PMA to indicate the status of the underlying PMD receive link.

24.3.1.5.1 Semantics of the service primitive

PMA_LINK.indicate (link_status)

The link_status parameter can take on one of three values: READY, OK, or FAIL, indicating whether the underlying receive channel is intact and ready to be enabled by Auto-Negotiation (READY), intact and enabled (OK), or not intact (FAIL). Link_status is set to FAIL when the PMD sets signal_status to OFF; when Auto-Negotiation (optional) sets link_control to DISABLE; or when Far-End Fault Detect (optional) sets faulting to TRUE. When link_status ≠ OK, then rx_code-bit and carrier_status are undefined.

24.3.1.5.2 When generated

The PMA generates this primitive to indicate a change in the value of link_status.

24.3.1.5.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.1.6 PMA_LINK.request

This primitive is generated by the Auto-Negotiation algorithm, when implemented, to allow it to enable and disable operation of the PMA. See Clause 28. When Auto-Negotiation is not implemented, the primitive is never invoked and the PMA behaves as if link_control = ENABLE.

24.3.1.6.1 Semantics of the service primitive

PMA_LINK.request (link_control)

The link_control parameter takes on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE. Auto-Negotiation sets link_control to SCAN_FOR_CARRIER prior to receiving any fast link pulses, permitting the PMA to sense a 100BASE-X signal. Auto-Negotiation sets link_control to DISABLE when it senses an Auto-Negotiation partner (fast link pulses) and must temporarily disable the 100BASE-X PHY while negotiation ensues. Auto-Negotiation sets link_control to ENABLE when full control is passed to the 100BASE-X PHY.

24.3.1.6.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in Clause 28.

24.3.1.6.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as described in 24.3.4.4.

24.3.1.7 PMA_RXERROR.indicate

This primitive is generated by the PMA to indicate that an error has been detected during a carrier event.

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24.3.1.7.1 Semantics of the service primitive

PMA_RXERROR.indicate (rxerror_status)

The rxerror_status parameter can take on one of two values: ERROR or NO_ERROR, indicating whether the received carrier event contains a detectable error (ERROR) or not (NO_ERROR). A carrier event is considered to be in error when it is not started by a Start-of-Stream Delimiter.

24.3.1.7.2 When generated

The PMA generates this primitive whenever a new, non-squelched carrier event is not started by a Start-of-Stream Delimiter.

24.3.1.7.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.2 Functional requirements

The 100BASE-X PMA comprises the following functions:

a) Mapping of transmit and receive code-bits between the PMA Service Interface and the PMD Service Interface;
b) Link Monitor, which maps the PMD_SIGNAL.indicate primitive to the PMA_LINK.indicate primitive, indicating the availability of the underlying PMD;
c) Carrier Detection, which generates the PMA_CARRIER.indicate and PMA_RXERROR.indicate primitives from inspection of received PMD signals; and
d) Far-End Fault (optional), comprised of the Far-End Fault Generate and Far-End Fault Detect processes, which sense receive channel failures and send the Far-End Fault Indication, and sense the Far-End Fault Indication.

Figure 24–4 includes a functional block diagram of the PMA.

24.3.2.1 Far-End fault

Auto-Negotiation provides a Remote Fault capability useful for detection of asymmetric link failures; i.e., channel error conditions detected by the far-end station but not the near-end station. Since Auto-Negotiation is specified only for media supporting eight-pin modular connectors, such as used by 100BASE-TX over unshielded twisted pair, Auto-Negotiation's Remote Fault capability is unavailable to other media for which it may be functionally beneficial, such as 100BASE-TX over shielded twisted pair or 100BASE-FX. A remote fault capability for 100BASE-FX is particularly useful due to this medium's applicability over longer distances (making end-station checking inconvenient) and for backbones (in which detection of link failures can trigger redundant systems).

For these reasons, 100BASE-X provides an optional Far-End Fault facility when Auto-Negotiation cannot be used. Far-End Fault shall not be implemented for media capable of supporting Auto-Negotiation.

When no signal is being received, as indicated by the PMD's signal detect function, the Far-End Fault feature permits the station to transmit a special Far-End Fault Indication to its far-end peer. The Far-End Fault Indication is sent only when a physical error condition is sensed on the receive channel. In all other situations, including reception of the Far-End Fault Indication itself, the PMA passes through tx_code-bit. (Note that the Far-End Fault architecture is such that IDLEs are automatically transmitted when the Far-End Fault Indication is detected. This is necessary to re-establish communication when the link is repaired.)

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The Far-End Fault Indication is comprised of three or more repeating cycles, each of 84 ONEs followed by a single ZERO. This signal is sent in-band and is readily detectable but is constructed so as to not satisfy the 100BASE-X carrier sense criterion. It is therefore transparent to the PMA's client and to stations not implementing Far-End Fault.

As shown in Figure 24–4, Far-End Fault is implemented through the Far-End Fault Generate, Far-End Fault Detect, and the Link Monitor processes.

The Far-End Fault Generate process, which is interposed between the incoming tx_code-bit stream and the TX process, is responsible for sensing a receive channel failure (signal_status=OFF) and transmitting the Far-End Fault Indication in response. The transmission of the Far-End Fault Indication may start or stop at any time depending only on signal_status.

The Far-End Fault Detect process continuously monitors rx_code-bits from the RX process for the Far-End Fault Indication. Detection of the Far-End Fault Indication disables the station by causing the Link Monitor process to deassert link_status, which in turn causes the station to source IDLEs. Far-End Fault detection can also be used by management functions not specified in this clause.

24.3.2.2 Comparison to previous IEEE 802.3 PMAs

Previous 802.3 PMAs perform the additional functions of SQE Test and Jabber. Neither of these functions is implemented in the 100BASE-X PMA.

SQE Test is provided in other Physical Layers to check the integrity of the Collision Detection mechanism independently of the Transmit and Receive capabilities of the Physical Layer. Since 100BASE-X effects collision detection by sensing receptions that occur during transmissions, collision detection is dependent on the health of the receive channel. By checking the ability to properly receive signals from the PMD, the Link Monitor function therefore functionally subsumes the functions previously implemented by SQE Test.

The Jabber function prevents a DTE from causing total network failure under certain classes of faults. When using mixing media (e.g., coaxial cables or passive optical star couplers), this function must naturally be implemented in the DTE. 100BASE-X requires the use of an active repeater, with one DTE or repeater attached to each port. As an implementation optimization, the Jabber function has therefore been moved to the repeater in 100BASE-X.

24.3.3 State variables

24.3.3.1 Constants

FEF_CYCLES

The number of consecutive cycles (of FEF_ONES ONEs and a single ZERO) necessary to indicate the Far-End Fault Indication. This value is 3.

FEF_ONES

The number of consecutive ONEs to be transmitted for each cycle of the Far-End Fault Indication. This value is 84.

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24.3.3.2 Variables

carrier_status

The carrier_status parameter to be communicated by the Carrier Detect process through the PMA_CARRIER.indicate primitive. Carrier is defined as receipt of 2 noncontiguous ZEROes in 10 code-bits.

Values: ON; carrier is being received
OFF; carrier is not being received

faulting

The faulting variable set by the Far-End Fault Detect process, when implemented, indicating whether or not a Far-End Fault Indication is being sensed. This variable is used by the Link Monitor process to force link_status to FAIL.When Far-End Fault is not implemented, this variable is always FALSE.

Values: TRUE; Far-End Fault Indication is being sensed
FALSE; Far-End Fault Indication is not being sensed

link_control

The link_control parameter as communicated by the PMA_LINK.request primitive. When Auto-Negotiation is not implemented, the value of link_control is always ENABLE. See Clause 28 for a complete definition.

link_status

The link_status parameter as communicated by the Link Monitor process through the PMA_LINK.indicate primitive.

Values: FAIL; the receive channel is not intact
READY; the receive channel is intact and ready to be enabled by Auto-Negotiation
OK; the receive channel is intact and enabled for reception

r_bits [9:0]

In Carrier Detect, a vector of the 10 most recently received code-bits from the PMD RX process. r_bits [0] is the most recently received (newest) code-bit; r_bits [9] is the least recently received code-bit (oldest). r_bits is an internal variable used exclusively by the Carrier Detect process.

rx_code-bit

The rx_code-bit parameter as delivered by the RX process, which operates in synchronism with the PMD_UNITDATA.indicate primitive. rx_code-bit is the most recently received code-bit from the PMD after conversion from NRZI.

rxerror_status

The rxerror_status parameter to be communicated by the Carrier Detect process through the PMA_RXERROR.indicate primitive.

Values: NO_ERROR; no error detected in the carrier event being received
ERROR; the carrier event being received is in error

signal_status

The signal_status parameter as communicated by the PMD_SIGNAL.indicate primitive.

Values: ON; the quality and level of the received signal is satisfactory
OFF; the quality and level of the received signal is not satisfactory

tx_code-bit_in

In Link Fault Generate, the tx_code-bit parameter as conveyed to the PMA from the PMA client by the PMA_UNITDATA.request.

tx_code-bit_out

In Link Fault Generate, the tx_code-bit parameter to be passed to the TX process. Note that this is called tx_code-bit by the TX process.

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24.3.3.3 Functions

SHIFTLEFT (rx_bits)

In Carrier Detect, this function shifts rx_bits left one bit placing rx_bits [8] in rx_bits [9], rx_bits [7] in rx_bits [8] and so on until rx_bits [1] gets rx_bits [0].

24.3.3.4 Timers

stabilize_timer

An implementation-dependent delay timer between 330 μs and 1000 μs, inclusive, to ensure that the link is stable.

24.3.3.5 Counters

num_cycles

In Link Fault Detect, a counter containing the number of consecutive Far-End Fault cycles currently sensed. This counter gets reset on intialization or when the bit stream fails to qualify as a potential Far-End Fault Indication. It never exceeds FEF_CYCLES.

num_ones

This represents two separate and independent counters: In Link Fault Generate, a counter containing the number of consecutive ONEs already sent during this cycle of the Far-End Fault Indication. In Link Fault Detect, a counter containing the number of consecutive ONEs currently sensed; it gets reset whenever a ZERO is detected or when the bit stream fails to qualify as a potential Far-End Fault Indication. These counters never exceed FEF_ONES.

24.3.3.6 Messages

PMD_UNITDATA.indicate (rx_nrzi-bit)

A signal sent by the PMD signifying that the next nrzi-bit is available from the medium. nrzi-bit is converted (instantaneously) to code-bit by the RX process and used by the Carrier Detect process.

5xPMD_UNITDATA.indicates

In Carrier Detect, this shorthand notation represents repetition of the preceding state five times synchronized with five successive PMD_UNITDATA.indicates.

PMA_UNITDATA.request (tx_code-bit)

A signal sent by the PMA's client signifying that the next nrzi-bit is available for transmission. For this process, the tx_code-bit parameter is interpreted as tx_code-bit_in.

24.3.4 Process specifications and state diagrams

24.3.4.1 TX

The TX process passes data from the PMA's client directly to the PMD. The PMA shall implement the TX process as follows: Upon receipt of a PMA_UNITDATA.request (tx_code-bit), the PMA performs a conversion to NRZI format and generates a PMD_UNITDATA.request (tx_nrzi-bit) primitive with the same logical value for the tx_nrzi-bit parameter. Note that tx_code-bit is equivalent to tx_code-bit_out of the Link Fault Generate process when implemented.

24.3.4.2 RX

The RX process passes data from the PMD directly to the PMA's client and to the Carrier Detect process. The PMA shall implement the RX process as follows: Upon receipt of a PMD_UNITDATA.indicate (rx_nrzi-bit),

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the PMA performs a conversion from NRZI format and generates a PMA_UNITDATA.indicate (rx_code-bit) primitive with the same logical value for the rx_code-bit parameter.

24.3.4.3 Carrier detect

The PMA Carrier Detect process provides repeater clients an indication that a carrier event has been sensed and an indication if it is deemed in error. A carrier event is defined as receipt of two non-contiguous ZEROS within any 10 rx_code-bits. A carrier event is in error if it does not start with an SSD. The Carrier Detect process performs this function by continuously monitoring the code-bits being delivered by the RX process, and checks for specific patterns which indicate non-IDLE activity and SSD bit patterns.

The Carrier Detect process collects code-bits from the PMD RX process. r_bits [9:0] represents a sliding, 10-bit window on the code-bit sequence, with newly received code-bits from the RX process being shifted into r_bits [0]. The process shifts the r_bits vector to the left, inserts the newly received code-bit into position 0, and waits for the next PMD.UNITDATA.indicate before repeating the operation. This is depicted in Figure 24–13. The Carrier Detect process monitors the r_bits vector until it detects two noncontiguous ZEROS in the incoming code-bit sequence. This signals a transition of carrier_status from OFF to ON. Each new carrier is further examined for a leading SSD (1100010001) with rxerror_status set to ERROR if it is not confirmed. A pattern of 10 contiguous ONEs in the stream indicates a return to carrier_status = OFF. Code-bit patterns of contiguous ONEs correspond to IDLE code-groups in the PCS, per the encoding specified in 24.2.2.1.

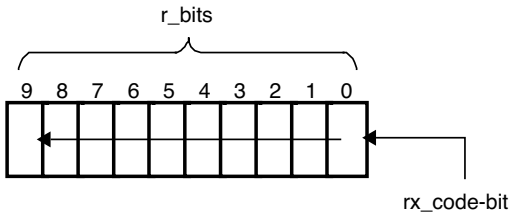


Figure 24–13—Carrier Detect reference diagram

The PMA shall, if it is supporting a repeater, implement the Carrier Detect process as depicted in Figure 24–14 including compliance with the associated state variables as specified in 24.3.3.

24.3.4.4 Link Monitor

The Link Monitor process is responsible for determining whether the underlying receive channel is providing reliable data. Failure of the underlying channel typically causes the PMA's client to suspend normal actions. The Link Monitor process takes advantage of the PMD sublayer's continuously signaled transmission scheme, which provides the PMA with a continuous indication of signal detection on the channel through signal_status as communicated by the PMD_SIGNAL.indicate primitive. It responds to control by Auto-Negotiation, when implemented, which is effected through the link_control parameter of PMA_SIGNAL.request.

The Link Monitor process monitors signal_status, setting link_status to FAIL whenever signal_status is OFF or when Auto-Negotiation sets link_control to DISABLE. The link is deemed to be reliably operating when signal_status has been continuously ON for a period of time. This period is implementation dependent but not less than 330 μs or greater than 1000 μs. If so qualified, Link Monitor sets link_status to READY in order to synchronize with Auto-Negotiation, when implemented. Auto-Negotiation permits full operation by setting link_control to ENABLE. When Auto-Negotiation is not implemented, Link Monitor operates with link_control always set to ENABLE.

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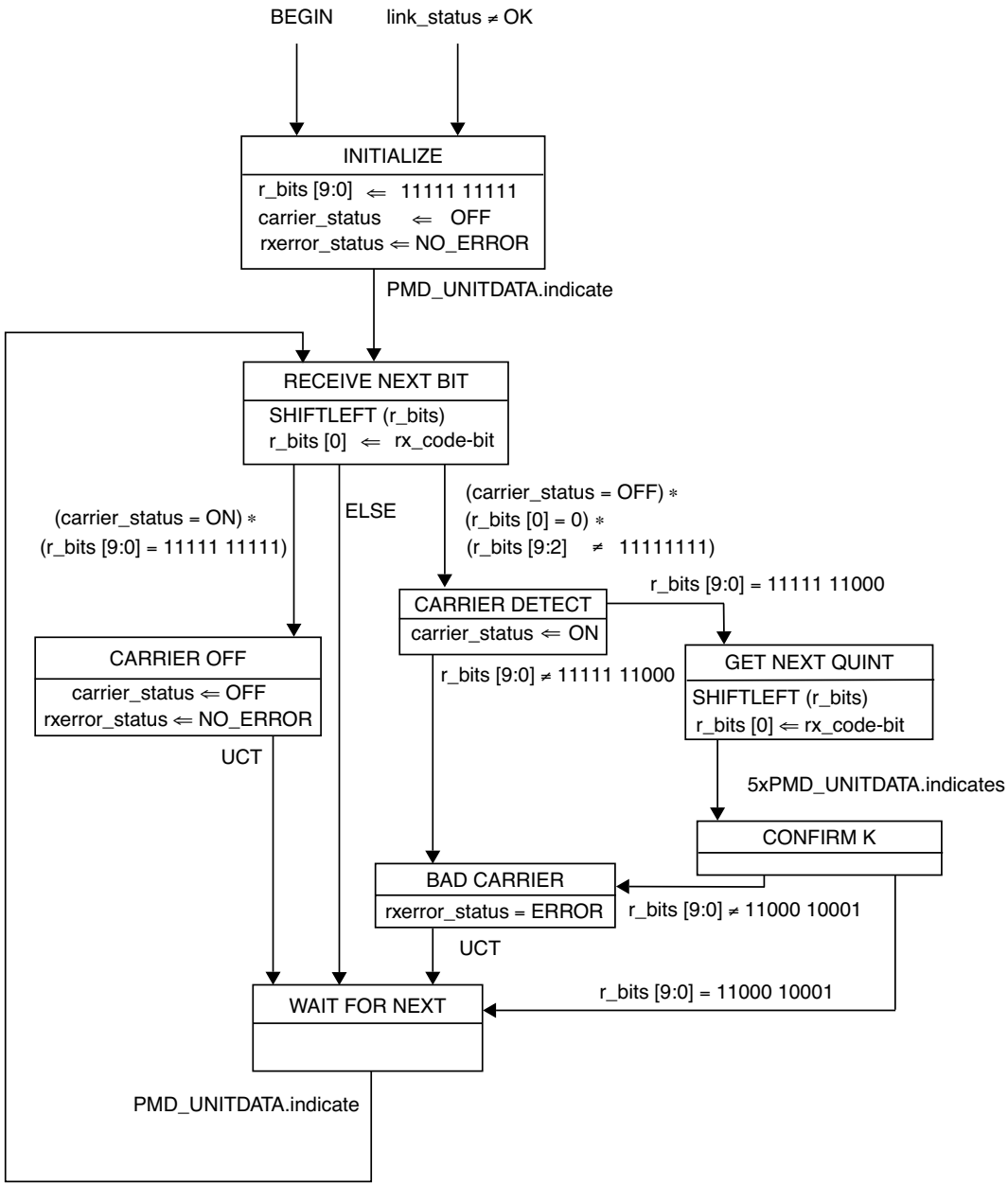


Figure 24–14—Carrier Detect state diagram

The PMA shall implement the Link Monitor process as depicted in Figure 24–15 including compliance with the associated state variables as specified in 24.3.3.

24.3.4.5 Far-End Fault Generate

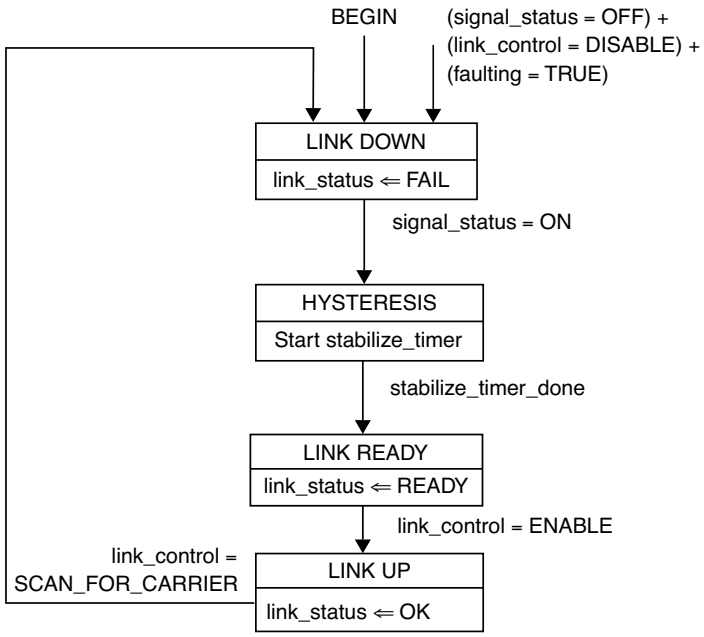
Far-End Fault Generate simply passes tx_code-bits to the TX process when signal_status=ON. When signal_status=OFF, it repetitively generates each cycle of the Far-End Fault Indication until signal_status is reasserted.

If Far-End Fault is implemented, the PMA shall implement the Far-End Fault Generate process as depicted in Figure 24–16 including compliance with the associated state variables as specified in 24.3.3.

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NOTE—The variables link_control and link_status are designated as link_control_[TX] and link_status_[TX], respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–16).

Figure 24–15—Link Monitor state diagram

24.3.4.6 Far-End Fault Detect

Far-End Fault Detect passively monitors the rx_code-bit stream from the RX process for the Far-End Fault Indication. It does so by maintaining counters for the number of consecutive ONEs seen since the last ZERO (num_ones) and the number of cycles of 84 ONEs and a single ZERO (num_cycles). The Far-End Fault Indication is denoted by three or more cycles, each of 84 ONEs and a single ZERO. Note that the number of consecutive ONEs may exceed 84 on the first cycle.

If Far-End Fault is implemented, the PMA shall implement the Far-End Fault Detect process as depicted in Figure 24–17 including compliance with the associated state variables as specified in 24.3.3.

24.4 Physical Medium Dependent (PMD) sublayer service interface

24.4.1 PMD service interface

The following specifies the services provided by the PMD. The PMD is a sublayer within 100BASE-X and may not be present in other 100BASE-T PHY specifications. PMD services are described in an abstract manner and do not imply any particular implementation. It should be noted that these services are functionally identical to those defined in the FDDI standards, such as ISO/IEC 9314-3: 1990 and ANSI X3.263-1995, with two exceptions:

a) 100BASE-X does not include a Station Management (SMT) function; therefore the PMD-to-SMT interface defined in ISO/IEC 9314-3: 1990 and ANSI X3.263-1995.
b) 100BASE-X does not support multiple instances of a PMD in service to a single PMA; therefore, no qualifiers are needed to identify the unique PMD being referenced.

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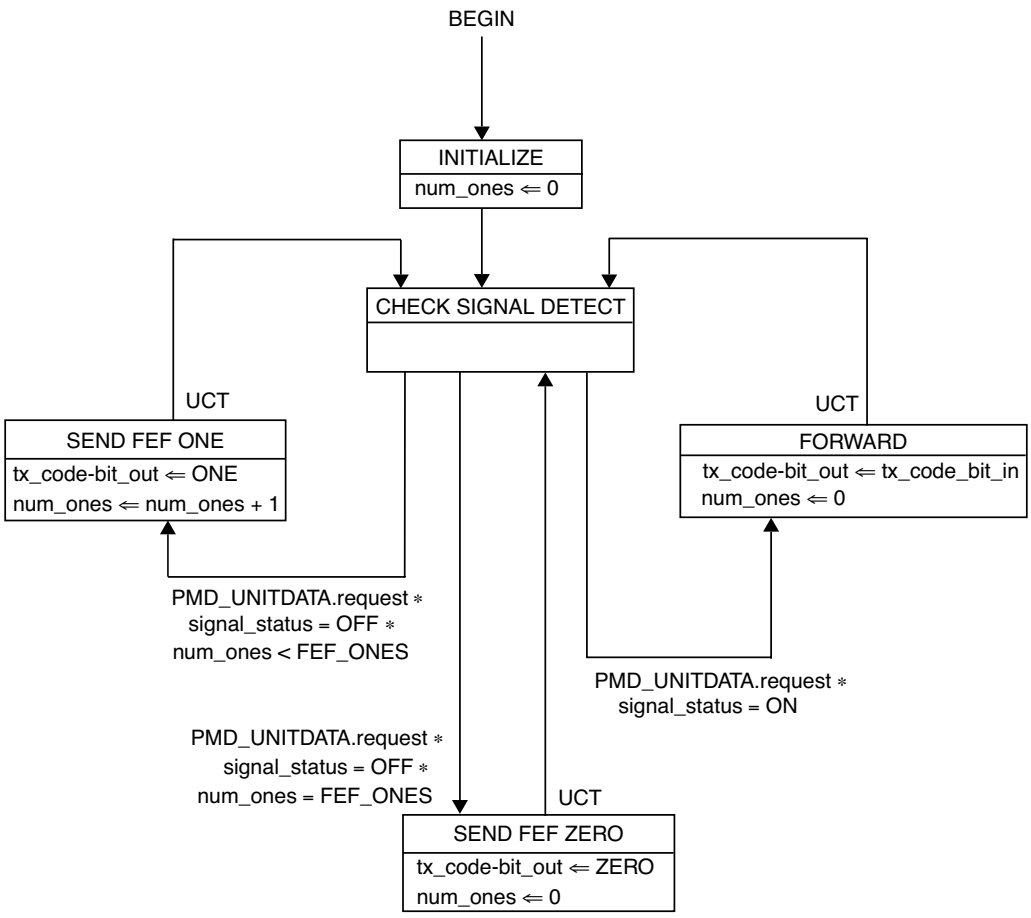


Figure 24–16—Far-End Fault Generate state diagram

There are also *editorial* differences between the interfaces specified here and in the referenced standards, as required by the context of 100BASE-X.

The PMD Service Interface supports the exchange of nrzi-bits between PMA entities. The PMD translates the nrzi-bits to and from signals suitable for the specified medium.

The following primitives are defined:

PMD_UNITDATA.request
PMD_UNITDATA.indicate
PMD_SIGNAL.indicate

24.4.1.1 PMD_UNITDATA.request

This primitive defines the transfer of data (in the form of nrzi-bits) from the PMA to the PMD.

24.4.1.1.1 Semantics of the service primitive

PMD_UNITDATA.request (tx_nrzi-bit)

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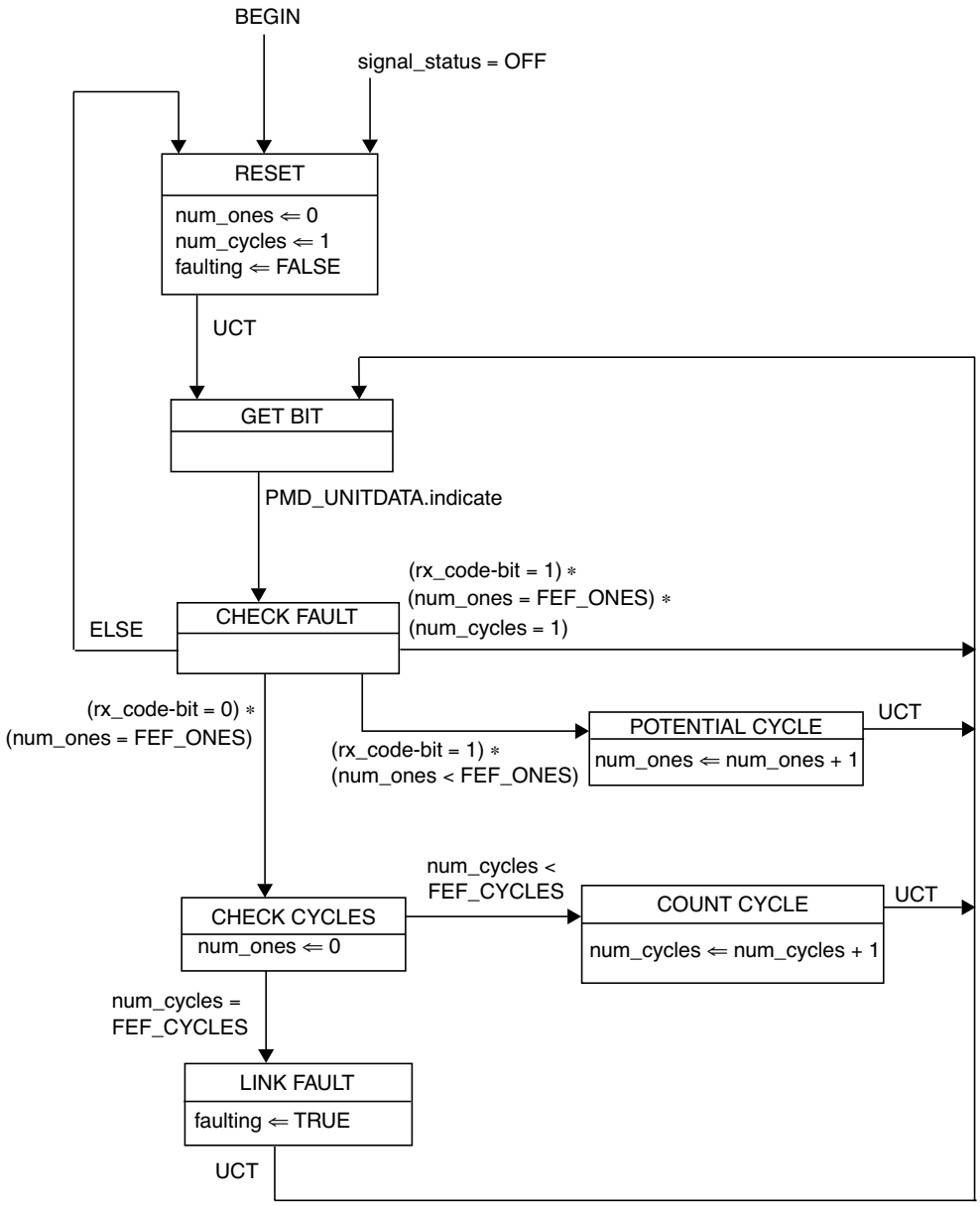


Figure 24–17—Far-End Fault Detect state diagram

The data conveyed by PMD_UNITDATA.request is a continuous sequence of nrzi-bits. The tx_nrzi-bit parameter can take one of two values: ONE or ZERO.

24.4.1.1.2 When generated

The PMA continuously sends, at a nominal 125 Mb/s rate, the PMD the appropriate nrzi-bits for transmission on the medium.

24.4.1.1.3 Effect of receipt

Upon receipt of this primitive, the PMD converts the specified nrzi-bit into the appropriate signals on the MDI.

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24.4.1.2 PMD_UNITDATA.indicate

This primitive defines the transfer of data (in the form of nrzi-bits) from the PMD to the PMA.

24.4.1.2.1 Semantics of the service primitive

PMD_UNITDATA.indicate (rx_nrzi-bit)

The data conveyed by PMD_UNITDATA.indicate is a continuous nrzi-bit sequence. The rx_nrzi-bit parameter can take one of two values: ONE or ZERO.

24.4.1.2.2 When generated

The PMD continuously sends nrzi-bits to the PMA corresponding to the signals received from the MDI.

24.4.1.2.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

24.4.1.3 PMD_SIGNAL.indicate

This primitive is generated by the PMD to indicate the status of the signal being received from the MDI.

24.4.1.3.1 Semantics of the service primitive

PMD_SIGNAL.indicate (signal_status)

The signal_status parameter can take on one of two values: ON or OFF, indicating whether the quality and level of the received signal is satisfactory (ON) or unsatisfactory (OFF). When signal_status = OFF, then rx_nrzi-bit is undefined, but consequent actions based on PMD_SIGNAL.indicate, where necessary, interpret rx_nrzi-bit as logic ZERO.

24.4.1.3.2 When generated

The PMD generates this primitive to indicate a change in the value of signal_status.

24.4.1.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

24.4.2 Medium Dependent Interface (MDI)

The MDI, a physical interface associated with a PMD, is comprised of an electrical or optical medium connector. The 100BASE-X MDIs, defined in subsequent clauses, are specified by reference to the appropriate FDDI PMD, such as in ISO/IEC 9314-3: 1990 and ANSI X3.263-1995, together with minor modifications (such as connectors and pin-outs) necessary for 100BASE-X.

24.5 Compatibility considerations

There is no requirement for a compliant device to implement or expose any of the interfaces specified for the PCS, PMA, or PMD. However, if an exposed interface is provided to the PCS, it shall comply with the requirements for the MII, as specified in Clause 22.

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24.6 Delay constraints

In half duplex mode, proper operation of a CSMA/CD LAN demands that there be an upper bound on the propagation delays through the network. This implies that MAC, PHY, and repeater implementors must conform to certain delay minima and maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

In full duplex mode, predictable operation of the (optional) MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementors must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

MAC constraints are contained in Clause 21. Topological constraints are contained in Clause 29. MAC Control sublayer constraints are contained in Clause 31.

The reference point for all MDI measurements is the 50% point of the mid-cell transition corresponding to the reference code-bit, as measured at the MDI. Although 100BASE-TX output is scrambled, it is assumed that these measurements are made via apparatuses that appropriately account for this.

24.6.1 PHY delay constraints (exposed MII)

Every 100BASE-X PHY with an exposed MII shall comply with the bit delay constraints specified in Table 24–2. These figures apply for all 100BASE-X PMDs.

Table 24–2—Bit delay constraints

a) MDI to MII delay constraints (exposed MII, half duplex mode)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MII ⇔ MDI	TX_EN sampled to MDI output	6	14	TX_CLK rising	1st bit of /J/
	MDI input to CRS assert		20	1st bit of /J/	
	MDI input to CRS de-assert (aligned)	13	24	1st bit of /T/	
	MDI input to CRS de-assert (unaligned)	13	24	1st ONE	
	MDI input to COL assert		20	1st bit of /J/	
	MDI input to COL de-assert (aligned)	13	24	1st bit of /T/	
	MDI input to COL de-assert (unaligned)	13	24	1st ONE	
	TX_EN sampled to CRS assert	0	4	TX_CLK rising	
	TX_EN sampled to CRS de-assert	0	16	TX_CLK rising	

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Table 24–3—Bit delay constraints *(Continued)*

b) PHY delay constraints (exposed MII, full duplex mode)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MII ⇔ MDI	TX_EN sampled to MDI output		14	TX_CLK rising	1st bit of /J/
	MDI Input to RX_DV de-assert		32	first bit of /T/	RX_CLK rising

24.6.2 DTE delay constraints (unexposed MII)

Every 100BASE-X DTE with no exposed MII shall comply with the bit delay constraints specified in Table 24–3. These figures apply for all 100BASE-X PMDs.

Table 24–4—DTE delay constraints (unexposed MII, half duplex mode)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MAC ⇔ MDI	MAC transmit start to MDI output		18		1st bit of /J/
	MDI input to MDI output (worst-case nondeferred transmit)		54	1st bit of /J/	1st bit of /J/
	MDI input to collision detect		28	1st bit of /J/	
	MDI input to MDI output = Jam (worst case collision response)		54	1st bit of /J/	1st bit of jam

24.6.3 Carrier de-assertion/assertion constraint (half duplex mode only)

To ensure fair access to the network, each DTE shall, additionally, satisfy the following:

(MAX MDI to MAC Carrier De-assert Detect) – (MIN MDI to MAC Carrier Assert Detect) < 13

24.7 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801.

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24.8 Protocol Implementation Conformance Statement (PICS) proforma for Clause 24, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X[7]

24.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 24, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

24.8.2 Identification

24.8.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

24.8.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2002, Clause 24, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

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24.8.2.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*DTE	Supports DTE without MII	24.4	O/1		
*REP	Supports Repeater without MII	24.4	O/1		
*MII	Supports exposed MII interface	24.4	O/1		
*PCS	Implements PCS functions	24.2	REP: O DTE: M MII: M		
PMA	Implements PMA RX, TX and Link Monitor functions	24.3	M		
*NWC	Medium capable of supporting Auto-Negotiation		O		See Clause 28
*FEF	Implements Far-End Fault	24.3.2.1	NWC: X		
NWY	Supports Auto-Negotiation (Clause 28)		NWC: O		See Clause 28

24.8.3 PICS proforma tables for the Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X

24.8.3.1 General compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
GN1	Compliance with MII requirements	24.4	MII:M		See Clause 22
GN2	Environmental specifications	24.7	M		

24.8.3.2 PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PS1	Transmit Bits process	24.2.3	PCS:M		
PS2	Transmit process	24.2.4.2	PCS:M		
PS3	Receive Bits process	24.2.4.3	PCS:M		
PS4	Receive process	24.2.4.4	PCS:M		
PS5	Carrier Sense process	24.2.4.5	PCS:M		

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24.8.3.3 PMA functions

Item	Feature	Subclause	Status	Support	Value/Comment
PA1	TX process	24.3.4.1	M		
PA2	RX process	24.3.4.2	M		
PA3	Carrier Detect process	24.3.2.1	REP: M		
PA4	Link Monitor process	24.3.4.4	M		
PA5	Far-End Fault Generate process	24.3.4.5	FEF: M		
PA6	Far-End Fault Detect process	24.3.4.6	FEF: M		

24.8.3.4 Timing

Item	Feature	Subclause	Status	Support	Value/Comment
TM1	Support for MII signals TX_CLK and RX_CLK	24.2.2.3	MII:M		See Clause 22
TM2	Accuracy of code-bit_timer	24.2.3	M		
TM3	Compliance with PHY bit delay constraints	24.6.1	MII:M REP: O		
TM4	Compliance with DTE bit delay constraints	24.6.2	DTE:M		
TM5	Compliance with Carrier De-assert/Assert Constraint	24.6.3	DTE:M		

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25. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX

25.1 Overview

This clause specifies the 100BASE-X PMD (including MDI) and baseband medium for twisted-pair wiring, 100BASE-TX. In order to form a complete 100BASE-TX Physical Layer, the 100BASE-X PMD (including MDI) shall be integrated with the 100BASE-X PCS and PMA of Clause 24, which are assumed incorporated by reference. As such, the 100BASE-TX PMD shall comply with the PMD service interface specified in 24.4.1.

25.2 Functional specifications

The 100BASE-TX PMD (and MDI) is specified by incorporating the FDDI TP-PMD standard, ANSI X3.263: 1995 (TP-PMD), by reference, with the modifications noted below. This standard provides support for Category 5 unshielded twisted pair (UTP) and shielded twisted pair (STP). For improved legibility in this clause, ANSI X3.263: 1995 (TP-PMD), will henceforth be referred to as TP-PMD.

25.3 General exceptions

The 100BASE-TX PMD is precisely the PMD specified as TP-PMD, with the following general modifications:

a) The Scope and General description discussed in TP-PMD 1 and 5 relate to the use of those standards with an FDDI PHY, ISO/IEC 9314-1: 1989, and MAC, ISO/IEC 9314-2: 1989. These sections are not relevant to the use of the PMD with 100BASE-X.
b) The Normative references, Definitions and Conventions of TP-PMD 2, 3, and 4 are used only as necessary to interpret the applicable sections of TP-PMD referenced in this clause.
c) The PMD Service Specifications of TP-PMD 6 are replaced by those specified in 24.4.1. The 100BASE-TX PMD Service specification is a proper subset of the PMD Service Specification in TP-PMD.
d) The cable plant specifications for untwisted shielded pair (UTP) of TP-PMD 11.1 are replaced by those specified in 25.4.6.
e) There are minor terminology differences between this standard and TP-PMD that do not cause ambiguity. The terminology used in 100BASE-X was chosen to be consistent with other IEEE 802 standards, rather than with FDDI. Terminology is both defined and consistent within each standard. Special note should be made of the interpretations shown in Table 25–1.

Table 25–1—Interpretation of general FDDI terms and concepts

FDDI term or concept	Interpretation for 100BASE-TX
bypass	<unused>
Connection Management (CMT)	<no comparable entity>
frame	stream
Halt Line State (HLS)	<unused>
hybrid mode	<no comparable entity>
MAC (or MAC-2)	MAC

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Table 25–1—Interpretation of general FDDI terms and concepts *(continued)*

FDDI term or concept	Interpretation for 100BASE-TX
Master Line State (MLS)	<unused>
maximum frame size = 9000 symbols	maximum stream size = 3062 code-groups
PHY (or PHY-2)	PMA; i.e., PMD client
PHY Service Data Unit (SDU)	stream
PM_SIGNAL.indication (Signal_Detect)	PMD_SIGNAL.indicate (signal_status)
PM_UNITDATA.indication (PM_Indication)	PMD_UNITDATA.indicate (nrzi-bit)
PM_UNITDATA.request (PM_Request)	PMD_UNITDATA.request (nrzi-bit)
preamble	inter-packet IDLEs
Quiet Line State (QLS)	<unused>
SM_PM_BYPASS.request (Control_Action)	Assume: SM_PM_BYPASS.request(Control_Action = Insert)
SM_PM_CONTROL.request (Control_Action)	Assume: SM_PM_CONTROL.request (Control_Action = Transmit_Enable)
SM_PM_SIGNAL.indication (Signal_Detect)	<unused>
Station Management (SMT)	<no comparable entity>
symbol	code-group

25.4 Specific requirements and exceptions

The 100BASE-TX PMD (including MDI) shall comply to the requirements of TP-PMD, 7, 8, 9, 10, and 11, and normative Annex A with the exceptions listed below. In TP-PMD, informative annexes B, C, E, G, I, and J, with exceptions listed below, provide additional information useful to PMD sublayer implementors. Where there is conflict between specifications in TP-PMD and those in this standard, those of this standard shall prevail.

25.4.1 Change to 7.2.3.1.1, “Line state patterns”

Descrambler synchronization on the Quiet Line State (QLS), Halt Line State (HLS), and Master Line State (MLS) Line State Patterns cited in TP-PMD 7.2.3.1.1 is optional.

25.4.2 Change to 7.2.3.3, “Loss of synchronization”

The synchronization error triggered by PH_Invalid as defined in TP-PMD 7.2.3.3a is not applicable.

25.4.3 Change to Table 8-1, “Contact assignments for unshielded twisted pair”

100BASE-TX for unshielded twisted pair adopts the contact assignments of 10BASE-T. Therefore, the contact assignments shown in TP-PMD Table 8-1 shall instead be as depicted in Table 25–2.

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Table 25–2—UTP MDI contact assignments

Contact	PHY without internal crossover MDI SIGNAL	PHY with internal crossover MDI SIGNAL
1	Transmit +	Receive +
2	Transmit –	Receive –
3	Receive +	Transmit +
4		
5		
6	Receive –	Transmit –
7		
8		

25.4.4 Deletion of 8.3, "Station labelling"

Clause 8.3 of TP-PMD shall not be applied to 100BASE-TX.

25.4.5 Change to 9.1.9, "Jitter"

The jitter measurement specified in 9.1.9 of TP-PMD may be performed using scrambled IDLEs.

25.4.6 UTP cable plant

The cable plant specification for unshielded twisted pair (UTP) of TP-PMD 11.1 is replaced by that specified in this subclause. The term "link segment" used in this subclause refers to a duplex channel of two pairs. Specifications for a link segment apply equally to each of the two pairs of a duplex channel. All implementations of the balanced cabling link shall be compatible at the MDI.

25.4.6.1 Cabling system characteristics

The cabling system used to support a 100BASE-TX duplex channel requires two pairs of Category 5 balanced cabling with a nominal impedance of 100 Ω. The cabling system components (cables, cords, and connectors) used to provide the link segment shall consist of Category 5 components as specified in ANSI/TIA/EIA-568-A:1995 and ISO/IEC 11801:1995 (Class D).

25.4.6.2 Link transmission parameters

The transmission parameters contained in this subclause are specified to ensure that a Category 5 link segment of up to 100 m, will provide a reliable medium. The transmission parameters of the link segment include insertion loss, characteristics impedance, return loss, NEXT loss, and external coupled noise.

25.4.6.2.1 Insertion loss

The insertion loss of the link segment shall be less than,

$$\text{Insertion\_Loss}(f) < 2.1f^{0.529} + 0.4/f \qquad \text{(dB)}$$

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at all frequencies from 1 MHz to 100 MHz. This includes the attenuation of the balanced cabling pairs, including work area and equipment cables plus connector losses within the link segment.

The insertion loss specification shall be met when the link segment is terminated in 100 Ω.

NOTE—The above equation approximates the insertion loss specification at 20°C for discrete frquencies of Category 5 100-meter links specified in ANSI/TIA/EIA-568-A Annex E and in TIA/EIA TSB-67.

25.4.6.2.2 Differential characteristic impedance

The nominal differential characteristic impedance of each link segment, which includes cable cords and connecting hardware, is 100 Ω for all frequenceis between 1 MHz and 100 MHz.

25.4.6.2.3 Return loss

Each link segment shall meet or exceed the return loss specified in the following equation at all frequencies from 1 MHz to 100 MHz.

$$\text{Return\_Loss}(f) \begin{cases} 15 & (1 - 20\ \text{MHz}) \\ 15 - 10\log_{10}(f/20) & (20 - 100\ \text{MHz}) \end{cases} \text{(dB)}$$

where f is the frequency in MHz. The reference impedance shall be 100 Ω.

25.4.6.2.4 Differential Near-End Crosstalk (NEXT)

In order to limit the crosstalk at the near end of a duplex channel, the differential pair-to-pair Near-End Crosstalk (NEXT) loss between the two pairs of a duplex channel shall be at least,

$$27.1 - 16.8\log_{10}(f/100)\ \text{(dB)}$$

where f is the frequency over the range of 1 MHz to 100 MHz.

NOTE—The above equation approximates the NEXT loss specification at discrete frequencies for Category 5 100-meter links specified in ANSI/TIA/EIA-568-A Annex E and in TIA/EIA TSB-67.

25.4.6.3 Noise environment

The 100BASE-TX noise environment consists of noise from external sources and could impact the objective BER. This noise may consist of sources outside the cabling that couple into the link segment via electric and magnetic fields. In addition noise from adjacent cables, referred to as alien crosstalk, may couple into the link segment. This alien crosstalk is generally present when cables are bound tightly together. To ensure robust operation a 100BASE-TX PHY should operate in the presence of an external noise as specified in 25.4.6.3.1.

25.4.6.3.1 External coupled noise

The differential noise coupled from external sources that is measured at the output of a filter connected to the output of the near end of a disturbed link segment should not exceed 40 mV peak-to-peak. The filter for this measurement is a fifth order Butterworth filter with a 3 dB cutoff at 100 MHz.

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25.4.7 Replacement of 11.2, "Crossover function"

Clause 11.2 of TP-PMD is replaced with the following:

A crossover function compliant with 14.5.2 shall be implemented except that a) the signal names are those used in TP-PMD, and b) the contact assignments for STP are those shown in Table 8-2 of TP-PMD. Note that compliance with 14.5.2 implies a recommendation that crossover (for both UTP and STP) be performed within repeater PHYs.

25.4.8 Change to A.2, "DDJ test pattern for baseline wander measurements"

The length of the test pattern specified in TP-PMD annex A.2 may be shortened to accommodate feasible 100BASE-X measurements, but shall not be shorter than 3000 code-groups.

NOTE—This pattern is to be applied to the MII. (When applied to the MAC, the nibbles within each byte are to be swapped. E.g., as delivered to the MAC, the test pattern would start, "60 c9 16 ...".)

25.4.9 Change to annex G, "Stream cipher scrambling function"

An example of a stream cipher scrambling implementation is shown in TP-PMD annex G. This may be modified to allow synchronization solely on the IDLE sequences between packets.

25.4.10 Change to annex I, "Common mode cable termination"

The contact assignments shown in TP-PMD figures I-1 and I-2 shall instead comply with those specified in Table 25–2.

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25.5 Protocol Implementation Conformance Statement (PICS) proforma for Clause 25, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX[8]

25.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 25, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

25.5.2 Identification

25.5.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

25.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2002, Clause 25, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

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25.5.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*TXU	Supports unshielded twisted pair	25.2	O/1		
TXS	Supports shielded twisted pair	25.2	O/1		

25.5.4 PICS proforma tables for the Physical Medium Dependent (PMD) sublayer and base-band medium, type 100BASE-TX

25.5.4.1 General compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
GN1	Integrates 100BASE-X PMA and PCS	25.1	M		See Clause 24

25.5.4.2 PMD compliance

Item	Feature	Subclause	Status	Support	Value/Comment
PD1	Compliance with 100BASE-X PMD Service Interface	25.1	M		See 24.2.3
PD2	Compliance with ANSI X3.263-1995, 7, 8 (excluding 8.3), 9, 10, 11 and normative annex A, with listed exceptions	25.4 25.4.5	M		
PD3	Precedence over ANSI X3.263-1995	25.4	M		
PD4	MDI contact assignments for unshielded twisted pair	25.4.4 25.4.3	TXU: M		
PD5	Compliance with crossover function of 14.5.2 with listed adaptations	25.4.8	M		
PD6	Minimum jitter test pattern length	25.4.9	M		3000 code-groups

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25.5.4.3 Characteristics of link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LKS1	Implementations of balanced cabling link	25.4.6	M		Compatible at the MDI.
LKS2	100BASE-T links	25.4.6.1	M		Category 5 components as specified in ANSI/TIA/EIA-568-A:1995 and ISO/IEC 11801:1995 (Class D).
LKS3	Insertion loss	25.4.6.2.1	M		As specified in 25.4.6.2.1 at all frequencies from 1 MHz to 100 MHz when link segment is terminated in 100 Ω.
LKS4	Return loss	25.4.6.2.3	M		As specified in 25.4.6.2.3 at all frequencies from 1 MHz to 100 MHz when link segment is terminated in 100 Ω.
LKS5	Differential Near-End Crosstalk (NEXT)	25.4.6.2.4	M		As specified in 25.4.6.2.4 at all frequencies from 1 MHz to 100 MHz.

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26. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-FX

26.1 Overview

This clause specifies the 100BASE-X PMD (including MDI) and fiber optic medium for multi-mode fiber, 100BASE-FX. In order to form a complete 100BASE-FX Physical Layer it shall be integrated with the 100BASE-X PCS and PMA of Clause 24, which are assumed incorporated by reference. As such, the 100BASE-FX PMD shall comply with the PMD service interface specified in 24.4.1.

26.2 Functional specifications

The 100BASE-FX PMD (and MDI) is specified by incorporating the FDDI PMD standard, ISO/IEC 9314-3: 1990, by reference, with the modifications noted below. This standard provides support for two optical fibers. For improved legibility in this clause, ISO/IEC 9314-3: 1990 will henceforth be referred to as fiber-PMD.

26.3 General exceptions

The 100BASE-FX PMD is precisely the PMD specified as fiber-PMD, with the following general modifications:

a) The Scope and General description discussed in fiber-PMD 1 and 5 relate to the use of those standards with an FDDI PHY, ISO/IEC 9314-1: 1989, and MAC, ISO/IEC 9314-2: 1989. These clauses are not relevant to the use of the PMD with 100BASE-X.
b) The Normative references, Definitions and Conventions of fiber-PMD 2, 3, and 4 are used only as necessary to interpret the applicable sections of fiber-PMD referenced in this clause.
c) The PMD Service Specifications of fiber-PMD 6 are replaced by those specified in 24.4.1. The 100BASE-FX PMD Service specification is a proper subset of the PMD service specification in fiber-PMD.
d) There are minor terminology differences between this standard and fiber-PMD that do not cause ambiguity. The terminology used in 100BASE-X was chosen to be consistent with other IEEE 802 standards, rather than with FDDI. Terminology is both defined and consistent within each standard. Special note should be made of the interpretations shown in Table 26–1.

Table 26–1—Interpretation of general FDDI terms and concepts

FDDI term or concept	Interpretation for 100BASE-X
bypass	<unused>
Connection Management (CMT)	<no comparable entity>
frame	stream
Halt Line State (HLS)	<unused>
hybrid mode	<no comparable entity>
MAC (or MAC-2)	MAC
Master Line State (MLS)	<unused>
maximum frame size = 9000 symbols	maximum stream size = 3062 code-groups

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Table 26–1—Interpretation of general FDDI terms and concepts *(continued)*

FDDI term or concept	Interpretation for 100BASE-X
PHY (or PHY-2)	PMA; i.e., PMD client
PHY Service Data Unit (SDU)	stream
PM_SIGNAL.indication (Signal_Detect)	PMD_SIGNAL.indicate (signal_status)
PM_UNITDATA.indication (PM_Indication)	PMD_UNITDATA.indicate (nrzi-bit)
PM_UNITDATA.request (PM_Request)	PMD_UNITDATA.request (nrzi-bit)
preamble	inter-packet IDLEs
Quiet Line State (QLS)	<unused>
SM_PM_BYPASS.request (Control_Action)	Assume: SM_PM_BYPASS.request (Control_Action = Insert)
SM_PM_CONTROL.request (Control_Action)	Assume: SM_PM_CONTROL.request (Control_Action = Transmit_Enable)
SM_PM_SIGNAL.indication (Signal_Detect)	<unused>
Station Management (SMT)	<no comparable entity>
symbol	code-group

26.4 Specific requirements and exceptions

The 100BASE-FX PMD (including MDI) and baseband medium shall conform to the requirements of fiber-PMD Clauses 8, 9, and 10. In the referenced standard, fiber-PMD, informative Annexes A through G provide additional information useful to PMD sublayer implementors. Where there is conflict between specifications in fiber-PMD and those in this standard, those of this standard shall prevail.

26.4.1 Medium Dependent Interface (MDI)

The 100BASE-FX medium dependent interface (MDI) shall conform to one of the following connectors. The recommended alternative is the Low Cost Fibre Optical Interface Connector.

a) Low Cost Fibre Optical Interface Connector (commonly called the duplex SC connector) as specified in ANSI X3.237-1995, 7.1.1 through 7.3.1, inclusive.
b) Media Interface Connector (MIC) as specified in fiber-PMD 7 and Annex F. When the MIC is used, the receptacle shall be keyed as “M”.
c) Optical Medium Connector Plug and Socket (commonly called ST connector) as specified in 15.3.2.

26.4.2 Crossover function

A crossover function shall be implemented in every cable-pair link. The crossover function connects the transmitter of one PHY to the receiver of the PHY at the other end of the cable-pair link. For 100BASE-FX, the crossover function is realized in the cable plant.

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26.5 Protocol Implementation Conformance Statement (PICS) proforma for Clause 26, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-FX[9]

26.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 26, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-FX, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

26.5.2 Identification

26.5.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

26.5.3 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2002, Clause 26, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-FX
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

[9]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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26.5.4 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
FSC	Supports Low Cost Fibre Optical Interface Connector (duplex SC)	26.4.1	O/1		Recommended. See ANSI X3.237-1995, 7.1.1 through 7.3.1
*FMC	Supports Media Interface Connector (MIC)	26.4.1	O/1		See ISO/IEC 9314-3: 1990, 7 and Annex F
FST	Supports Optical Medium Connector Plug and Socket (ST)	26.4.1	O/1		See 15.3.2

26.5.5 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-FX

26.5.5.1 General compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
GN1	Integrates 100BASE-X PMA and PCS	26.1	M		See Clause 24

26.5.5.2 PMD compliance

Item	Feature	Subclause	Status	Support	Value/Comment
PD1	Compliance with 100BASE-X PMD Service Interface	26.1	M		See 24.4.1
PD2	Compliance with ISO/IEC 9314-3: 1990 8, 9, and 10	26.4	M		
PD3	Precedence over ISO/IEC 9314-3: 1990	26.4	M		
PD4	MIC receptacle keying	26.4.1	FMC: M		“M”
PD5	Crossover function in cable	26.4.2	M		

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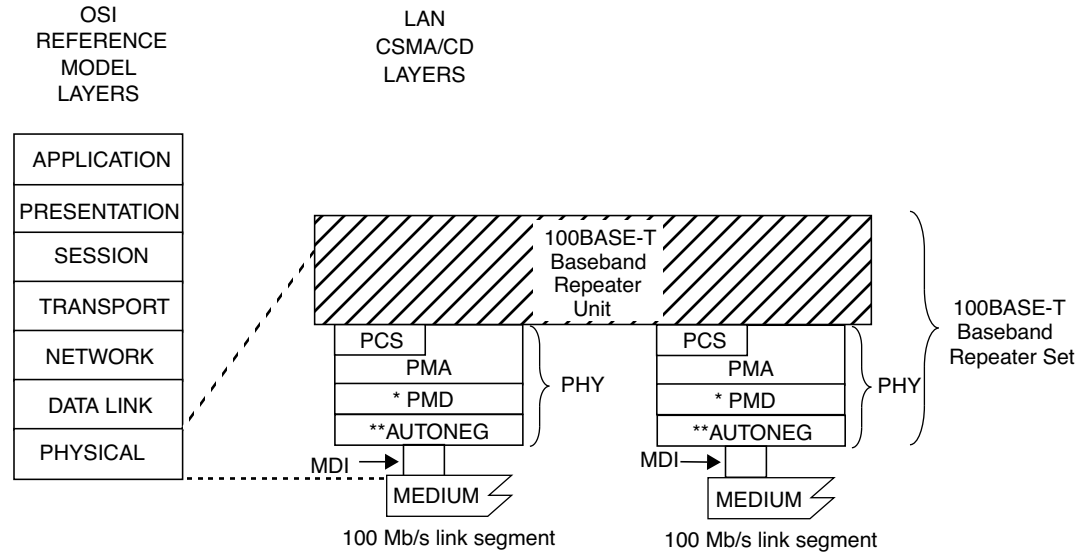
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27. Repeater for 100 Mb/s baseband networks

27.1 Overview

27.1.1 Scope

Clause 27 defines the functional and electrical characteristics of a repeater for use with 100BASE-T 100 Mb/s baseband networks. A repeater for any other IEEE 802.3 network type is beyond the scope of this clause. The relationship of this standard to the entire ISO/IEC 8802-3 CSMA/CD LAN standard is shown in Figure 27–1. The purpose of the repeater is to provide a simple, inexpensive, and flexible means of coupling two or more segments.



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* PMD is specified for 100BASE-TX and -FX only; 100BASE-T4 does not use this layer.
Use of MII between PCS and baseband repeater unit is optional.
** AUTONEG is optional.

Figure 27–1—100BASE-T repeater set relationship to the ISO/IEC OSI reference model

27.1.1.1 Repeater set

Repeater sets are an integral part of all 100 Mb/s baseband networks with more than two DTEs and are used to extend the physical system topology by providing a means of coupling two or more segments. Multiple repeater sets are permitted within a single collision domain to provide the maximum connection path length. Segments may be connected directly by a repeater or a pair of repeaters that are, in turn, connected by a inter-repeater link (IRL). Allowable topologies shall contain only one operative signal path between any two

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points on the network. A repeater set is not a station and does not count toward the overall limit of 1024 stations on a network.

A repeater set can receive, and if necessary decode, data from any segment under worst-case noise, timing, and signal amplitude conditions. It retransmits the data to all other segments attached to it with timing, amplitude, and, if necessary, coding restored. The retransmission of data occurs simultaneously with reception. If a collision occurs, the repeater set propagates the collision event throughout the network by transmitting a Jam signal. A repeater set also provides a degree of protection to a network by isolating a faulty segment's carrier activity from propagating through the network.

27.1.1.2 Repeater unit

A repeater unit is a subset of a repeater set containing all the repeater-specific components and functions, exclusive of PHY components and functions. A repeater unit connects to the PMA and, if necessary, the PCS sublayers of its PHYs.

27.1.1.3 Repeater classes

Two classes of repeater sets are defined—Class I and Class II.

Class I:
: A type of repeater set specified such that in a maximum length segment topology, only one such repeater set may exist between any two DTEs within a single collision domain.

Class II:
: A type of repeater set specified such that in a maximum length segment topology, only two such repeater sets may exist between any two DTEs within a single collision domain.

More complex topologies are possible in systems that do not use worst-case cable. See Clause 29 for requirements.

27.1.2 Application perspective

This subclause states the broad objectives and assumptions underlying the specification defined through Clause 27.

27.1.2.1 Objectives

a) Provide physical means for coupling two or more LAN segments at the Physical Layer.
b) Support interoperability of independently developed physical, electrical, and optical interfaces.
c) Provide a communication channel with a mean bit error rate, at the physical service interface equivalent to that for the attached PHY.
d) Provide for ease of installation and service.
e) Ensure that fairness of DTE access is not compromised.
f) Provide for low-cost networks, as related to both equipment and cabling.
g) Make use of building wiring appropriate for the supported PHYs and telephony wiring practices.

27.1.2.2 Compatibility considerations

All implementations of the repeater set shall be compatible at the MDI. The repeater set is defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the repeater set in an application-dependent manner provided the appropriate PHY specifications are met.

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27.1.2.2.1 Internal segment compatibility

Implementations of the repeater set that contain a MAC layer for network management or other purposes, irrespective of whether they are connected through an exposed repeater port or are internally ported, shall conform to the requirements of Clause 30 on that port if repeater management is implemented.

27.1.3 Relationship to PHY

A close relationship exists between Clause 27 and the PHY clauses, Clause 23 for the 100BASE-T4 PHY and Clauses 24 to 26 for the 100BASE-X PHYs, and Clause 32 for the 100BASE-T2 PHY. The PHY's PMA, PCS, and MDI specifications provide the actual medium attachment, including drivers, receivers, and Medium Interface Connectors for the various supported media. The repeater clause does not define a new PHY; it utilizes the existing PHYs complete and without modification.

27.2 PMA interface messages

The messages between the repeater unit and the PMA in the PHY utilizes the PMA service interface defined in 23.3, 24.3, and 32.4.2. The PMA service interface primitives are summarized below:

PMA_TYPE.indicate
PMA_UNITDATA.request
PMA_UNITDATA.indicate
PMA_CARRIER.indicate
PMA_LINK.indicate
PMA_RXERROR.indicate

27.3 Repeater functional specifications

A repeater set provides the means whereby data from any segment can be received under worst case noise, timing, and amplitude conditions and then retransmitted with timing and amplitude restored to all other attached segments. Retransmission of data occurs simultaneously with reception. If a collision occurs, the repeater set propagates the collision event throughout the network by transmitting a Jam signal. If an error is received by the repeater set, no attempt is made to correct it and it is propagated throughout the network by transmitting an invalid signal.

The repeater set provides the following functional capability to handle data flow between ports:

a) *Signal restoration*. Provides the ability to restore the timing and amplitude of the received signal prior to retransmission.
b) *Transmit function*. Provides the ability to output signals on the appropriate port and encoded appropriately for that port. Details of signal processing are described in the specifications for the PHYs.
c) *Receive function*. Provides the ability to receive input signals presented to the ports. Details of signal processing are described in the specifications for the PHYs.
d) *Data Handling function*. Provides the ability to transfer code-elements between ports in the absence of a collision.
e) *Received Event Handling requirement*. Provides the ability to derive a carrier signal from the input signals presented to the ports.
f) *Collision Handling function*. Provides the ability to detect the simultaneous reception of frames at two or more ports and then to propagate a Jam message to all connected ports.
g) *Error Handling function*. Provides the ability to prevent substandard links from generating streams of false carrier and interfering with other links.
h) *Partition function*. Provides the ability to prevent a malfunctioning port from generating an excessive number of consecutive collisions and indefinitely disrupting data transmission on the network.

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i) *Receive Jabber function*. Provides the ability to interrupt the reception of abnormally long streams of input data.

27.3.1 Repeater functions

The repeater set shall provide the Signal Restoration, Transmit, Receive, Data Handling, Received Event Handling, Collision Handling, Error Handling, Partition, and Receive Jabber functions. The repeater is transparent to all network acquisition activity and to all DTEs. The repeater will not alter the basic fairness criterion for all DTEs to access the network or weigh it toward any DTE or group of DTEs regardless of network location.

The Transmit and Receive functional requirements are specified by the PHY clauses, Clause 23 for 100BASE-T4, Clauses 24 to 26 for 100BASE-X, and Clause 32 for 100BASE-T2.

27.3.1.1 Signal restoration functional requirements

27.3.1.1.1 Signal amplification

The repeater set (including its integral PHYs) shall ensure that the amplitude characteristics of the signals at the MDI outputs of the repeater set are within the tolerances of the specification for the appropriate PHY type. Therefore, any loss of signal-to-noise ratio due to cable loss and noise pickup is regained at the output of the repeater set as long as the incoming data is within system specification.

27.3.1.1.2 Signal wave-shape restoration

The repeater set (including its integral PHYs) shall ensure that the wave-shape characteristics of the signals at the MDI outputs of a repeater set are within the specified tolerance for the appropriate PHY type. Therefore, any loss of wave-shape due to PHYs and media distortion is restored at the output of the repeater set.

27.3.1.1.3 Signal retiming

The repeater set (including its integral PHYs) shall ensure that the timing of the encoded data output at the MDI outputs of a repeater set are within the specified tolerance for the appropriate PHY type. Therefore, any receive jitter from the media is removed at the output of the repeater set.

27.3.1.2 Data handling functional requirements

27.3.1.2.1 Data frame forwarding

The repeater set shall ensure that the data frame received on a single input port is distributed to all other output ports in a manner appropriate for the PHY type of that port. The data frame is that portion of the packet after the SFD and before the end-of-frame delimiter. The only exceptions to this rule are when contention exists among any of the ports, when the receive port is partitioned as defined in 27.3.1.6, when the receive port is in the Jabber state as defined in 27.3.1.7, or when the receive port is in the Link Unstable state as defined in 27.3.1.5.1. Between unpartitioned ports, the rules for collision handling (see 27.3.1.4) take precedence.

27.3.1.2.2 Received code violations

The repeater set shall ensure that any code violations received while forwarding a packet are propagated to all outgoing segments. These code violations shall be forwarded as received or replaced by bad_code (see 23.2.1.2), /H/ (see 24.2.2.1), or (ESC/0, 0/ESC) (see Figure 32–9) code-groups, as appropriate for the outgoing PHY type. Once a received code violation has been replaced by the bad_code, /H/, or (ESC/0, 0/ESC) code-groups, this substitution shall continue for the remainder of the packet regardless of its content. The only exception to this rule is when contention exists among any of the ports, where the rules for collision handling (see 27.3.1.4) then take precedence.

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27.3.1.3 Received event handling functional requirements

27.3.1.3.1 Received event handling

For all its ports, the repeater set shall implement a function (scarrier_present) that represents a received event. Received events include both the Data Frame and any encapsulation of the Data Frame such as Preamble, SFD, and the code-groups /H/, /J/, /K/, bad_code, eop, /T/, /R/, SSD, ESD, etc. A received event is exclusive of the IDLE pattern. Upon detection of scarrier_present from one port, the repeater set repeats all received signals in the Data Frame from that port to the other port (or ports) as described in Figure 27–2.

27.3.1.3.2 Preamble regeneration

The repeater set shall output preamble as appropriate for the outgoing PHY type followed by the SFD.

27.3.1.3.3 Start-of-packet propagation delay

The start-of-packet propagation delay for a repeater set is the time delay between the start of the packet (see 24.6, 23.11.3, and 32.12.1) on its repeated-from (input) port to the start of the packet on its repeated-to (output) port (or ports). This parameter is referred to as the SOP delay. The maximum value of this delay is constrained by Table 27–2.

27.3.1.3.4 Start-of-packet variability

The start-of-packet variability for a repeater set is defined as the total worst-case difference between start-of-packet propagation delays for successive packets separated by 104 bit times (BT) or less at the same input port. The variability shall be less than or equal to those specified in Table 27–1.

Table 27–1—Start-of-packet variability

Input port type	Variability (BT)
100BASE-FX	7.0
100BASE-TX	7.0
100BASE-T4	8.0
100BASE-T2	8.0

27.3.1.4 Collision handling functional requirements

27.3.1.4.1 Collision detection

The repeater performs collision detection by monitoring all its enabled input ports for received events. When the repeater detects received events on more than one input port, it shall enter a collision state and transmit the Jam message to all of its output ports.

27.3.1.4.2 Jam generation

While a collision is occurring between any of its ports, the repeater unit shall transmit the Jam message to all of the PMAs to which it is connected. The Jam message shall be transmitted in accordance with the repeater state diagram in Figure 27–4 and Figure 27–5.

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27.3.1.4.3 Collision-jam propagation delay

The start-of-collision Jam propagation delay for a repeater set is the time delay between the start of the second packet input signals to arrive at its port and the start of Jam (see 24.6, 23.11, and 32.12.1) out on all ports. This parameter is referred to as the SOJ delay. The delay shall be constrained by Table 27–2. Note that a device defined by two columns in Table 27–2 must meet the performance requirements specified in both columns.

Table 27–2—Start-of-packet propagation and start-of-collision jam propagation delays

Class I repeater	Class II repeater with all ports TX/FX	Class II repeater with any port T4	Class II repeater with any port T2
SOP + SOJ ≤ 140 BT	SOP ≤ 46 BT, SOJ ≤ 46 BT	SOP+SOJ ≤ 67 BT	SOP+SOJ ≤ 90 BT

27.3.1.4.4 Cessation-of-collision Jam propagation delay

The cessation-of-collision Jam propagation delay for a repeater set is the time delay between the end of the packet (see 24.6 and 23.11.3) that creates a state such that Jam should end at a port and the end of Jam (see 24.6 and 23.11.3) at that port. The states of the input signals that should cause Jam to end are covered in detail in the repeater state diagrams. This parameter is referred to as the EOJ delay. The delay shall be constrained by Table 27–3.

Table 27–3—Cessation-of-collision Jam propagation delay

Class I repeater	Class II repeater
EOJ ≤ SOP	EOJ ≤ SOP

27.3.1.5 Error handling functional requirements

27.3.1.5.1 100BASE-X and 100BASE-T2 carrier integrity functional requirements

In 100BASE-TX, 100BASE-FX, and 100BASE-T2 systems, it is desirable that the repeater set protect the network from some transient fault conditions that would disrupt network communications. Potential likely causes of such conditions are DTE and repeater power-up and power-down transients, cabling disconnects, and faulty wiring.

Each 100BASE-TX, 100BASE-FX, and 100BASE-T2 repeater PMA interface shall contain a self-interrupt capability, as described in Figure 27–9, to prevent a segment's spurious carrier activity from reaching the repeater unit and hence propagating through the network.

The repeater PMA interface shall count consecutive false carrier events. A false carrier event is defined as a carrier event that does not begin with a valid start of stream delimiter (see 24.2.2.1.4 and 32.3.1.2.3). The count shall be incremented on each false carrier event and shall be reset on reception of a valid carrier event. In addition, each PMA interface shall contain a false carrier timer, which is enabled at the beginning of a false carrier event and reset at the conclusion of such an event. A repeater unit shall transmit the JAM message to all of the PMAs to which it is connected for the duration of the false carrier event or until the duration of the event exceeds the time specified by the false_carrier_timer (see 27.3.2.1.4), whichever is shorter. The JAM message shall be transmitted in accordance with the Repeater state diagram in Figure 27–4 and Figure 27–5. The LINK UNSTABLE condition shall be detected when the False Carrier Count exceeds

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the value FCCLimit (see 27.3.2.1.1) or the duration of a false carrier event exceeds the time specified by the false_carrier_timer. In addition, the LINK UNSTABLE condition shall be detected upon power-up reset.

Upon detection of LINK UNSTABLE, the port shall perform the following:

a) Inhibit sending further messages to the repeater unit.
b) Inhibit sending further output messages from the repeater unit.
c) Continue to monitor activity on that PMA interface.

The repeater shall exit the LINK UNSTABLE condition when one of the following is met:

a) The repeater has detected no activity (Idle) for more than the time specified by ipg_timer plus idle_timer (see 27.3.2.1.4) on Port X.
b) A valid carrier event with a duration greater than the time specified by valid_carrier_timer (see 27.3.2.1.4) has been received, preceded by no activity (Idle) for more than the time specified by ipg_timer (see 27.3.2.1.4) on Port X.

27.3.1.5.2 Speed handling

If the PHY has the capability of detecting speeds other than 100 Mb/s, then the repeater set shall have the capability of blocking the flow of non-100 Mb/s signals. The incorporation of 100 Mb/s and 10 Mb/s repeater functionality within a single repeater set is beyond the scope of this standard.

27.3.1.6 Partition functional requirements

In large multisegment networks it may be desirable that the repeater set protect the network from some fault conditions that would disrupt network communications. A potentially likely cause of this condition could be due to a cable fault.

Each repeater PMA interface shall contain a self-interrupt capability, as described in Figure 27–8, to prevent a faulty segment's carrier activity from reaching the repeater unit and hence propagating through the network. The repeater PMA interface shall count collisions. The count shall be incremented on each transmission that suffers a collision. The count shall be reset on a carrier event of duration in excess of no_collision_timer (see 27.3.2.1.4) without incurring a collision. If this count reaches the value CCLimit (see 27.3.2.1.1), the Partition condition shall be detected.

Upon detection of Partition, the port shall perform the following:

a) Inhibit sending further input messages to the repeater unit.
b) Continue to output messages from the repeater unit.
c) Continue to monitor activity on that PMA interface.

The repeater shall reset the Partition function when one of the following conditions is met:

a) On power-up reset.
b) The repeater has transmitted on the port for a duration in excess of no_collision_timer (see 27.3.2.1.4) without incurring a collision.

NOTE—It is possible that under some network conditions the partition state machine will partition a port due to normal network collisions rather than a fault condition. It is also possible that some double fault conditions will remain undetected. To reduce the likelihood of these events occurring, the following optional measures, as described in Figure 27–8, are recommended:

a) The collision count is additionally reset when the repeater has transmitted on the port for a duration in excess of no_collision_timer without detecting a collision.

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b) The Partition function is additionally reset when the repeater has received activity on the port for a duration in excess of no_collision_timer without detecting a collision.
c) The Partition condition is additionally detected due to a carrier event of duration in excess of jabber_timer (see 27.3.1.7) in which a collision has occurred.

27.3.1.7 Receive jabber functional requirements

Each repeater PMA interface shall contain a self-interrupt capability, as described in Figure 27–7, to prevent an illegally long reception of data from reaching the repeater unit. The repeater PMA interface shall provide a window of duration jabber_timer bit times (see 27.3.2.1.4) during which the input messages may be passed on to other repeater unit functions. If a reception exceeds this duration, the jabber condition shall be detected.

Upon detection of jabber, the port shall perform the following:

a) Inhibit sending further input messages to the repeater unit.
b) Inhibit sending further output messages from the repeater unit.

The repeater PMA interface shall reset the Jabber function and re-enable data transmission and reception when either one of the following conditions is met:

a) On power-up reset.
b) When carrier is no longer detected.

27.3.2 Detailed repeater functions and state diagrams

A precise algorithmic definition is given in this subclause, providing a complete procedural model for the operation of a repeater, in the form of state diagrams. Note that whenever there is any apparent ambiguity concerning the definition of repeater operation, the state diagrams should be consulted for the definitive statement.

The model presented in this subclause is intended as a primary specification of the functions to be provided by any repeater unit. It is important to distinguish, however, between the model and a real implementation. The model is optimized for simplicity and clarity of presentation, while any realistic implementation should place heavier emphasis on such constraints as efficiency and suitability to a particular implementation technology.

It is the functional behavior of any repeater unit implementation that shall match the standard, not the internal structure. The internal details of the procedural model are useful only to the extent that they help specify the external behavior clearly and precisely. For example, the model uses a separate Receive Port Jabber state diagram for each port. However, in actual implementation, the hardware may be shared.

The notation used in the state diagram follows the conventions of 1.2.1. Note that transitions shown without source states are evaluated at the completion of every state and take precedence over other transition conditions.

27.3.2.1 State diagram variables

27.3.2.1.1 Constants

CCLimit

The number of consecutive collisions that must occur before a segment is partitioned.

Values: Positive integer greater than 60.

FCCLimit

The number of consecutive False Carrier events that must occur before a segment is isolated.

Value: 2.

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27.3.2.1.2 Variables

activity(Port designation)

Indicates port activity status. The repeater core effects a summation of this variable received from all its attached ports and responds accordingly.

Values: 0; no frame or packet activity at any port.
1; exactly 1 port of the repeater set has frame or packet activity input.
>1; more than 1 port of the repeater set has frame or packet activity input. Alternately, one or more ports has detected a carrier that is not valid.

all_data_sent

Indicates if all received data frame bits or code-groups from the current frame have been sent. During or after collision the all_data_sent variable follows the inverse of the carrier of port N.

Values: true; all received data frame bits or code-groups have been sent.
false; all received data frame bits or code-groups have not been sent.

begin

The Interprocess flag controlling state diagram initialization values.

Values: true
false

carrier_status(X)

Signal received from PMA; indicates the status of sourced Carrier input at Port X.

Values: ON; the carrier_status parameter of the PMA_CARRIER.indicate primitive for Port X is ON.
OFF; the carrier_status parameter of the PMA_CARRIER.indicate primitive for Port X is OFF.

data_ready

Indicates if the repeater has detected and/or decoded the MAC SFD and is ready to send the received data.

Values: true; the MAC SFD has been detected and/or decoded.
false; the MAC SFD has not been detected nor decoded.

force_jam(X)

Flag from Carrier Integrity state diagram for Port X, which determines whether all ports should transmit Jam.

Values: true; the Carrier Integrity Monitor has determined that it requires all ports be forced to transmit Jam.
false; the Carrier Integrity Monitor has determined that it does not require all ports be forced to transmit Jam.

Default: for T4 ports: false

isolate(X)

Flag from Carrier Integrity state diagram for Port X, which determines whether a port should be enabled or disabled.

Values: true; the Carrier Integrity Monitor has determined the port should be disabled.
false; the Carrier Integrity Monitor has determined the port should be enabled.

jabber(X)

Flag from Receive Timer state diagram for Port X, which indicates that the port has received excessive length activity.

Values: true; port has exceeded the continuous activity limit.

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false; port has not exceeded the continuous activity limit.

link_status(X)

Signal received from PMA; indicates link status for Port X (see 23.3.5, 24.3.1.5, and 32.4.1.3.1).

Values: OK; the link_status parameter of the PMA_LINK.indicate primitive for Port X is OK.
READY; the link_status parameter of the PMA_LINK.indicate primitive for Port X is READY (for 100BASE-TX and 100BASE-T4).
FAIL; the link_status parameter of the PMA_LINK.indicate primitive for Port X is FAIL.

opt(X)

Implementation option. Either value may be chosen for repeater implementation.

Values: true; port will emit the JamT4 pattern in response to collision conditions.
false; port will append Jam pattern after preamble and SFD in response to collision conditions.

OUT(X)

Type of output repeater is sourcing at Port X.

Values: Idle; repeater is transmitting an IDLE pattern as described by 23.4.1.2, 24.2.2.1.2, or 32.3.1.2.3.
In(N); repeater is transmitting rx_code_bit(s) as received from Port (N) except /J/K/ (see 24.3.4.2), or recoded rx_symbol_vector as received from Port (N) except SSD (see 32.3.5.2).
Pream; repeater is sourcing preamble pattern as defined by the PMA or PCS of the port type (see 23.2.1.2, 24.2.2.2, 32.3.1.2, Figure 23–6 and Figure 24–5.)
Data; repeater is transmitting data frame on Port X. This data represents the original MAC source data field, properly encoded for the PHY type (see 23.2.1.2, 24.2.2.2, and 32.3.1.2.3).
Jam; repeater is sourcing well formed arbitrary data encodings, excluding SFD, to the port PMA.
JamX; repeater is sourcing a pattern representing 010101... repetitively on Port X.
JamT4; repeater is sourcing the pattern +-+-... repetitively on Port X.

JamT2; repeater is sending a pattern representing 010101... repetitively on Port X.
SFD; repeater is sourcing the Start Frame Delimiter on Port X encoded as defined by the appropriate PHY (see 23.2.3, Figure 24–5 and 32.3.1.2).
/J/K/; repeater is sourcing the code-groups /J/K/ as defined by the PMA on Port X (see 24.2.2.1.4).
/T/R/; repeater is sourcing the code-groups /T/R/ as defined by the PMA on Port X (see 24.2.2.1.5).

SSD; repeater is sourcing the code-groups SSD as defined by the PMA on Port X (see 32.4.2.5).

ESD; repeater is sourcing the code-groups ESD as defined by the PMA on Port X (see 32.3.1.2.3).
DF; repeater is sourcing the Data Frame of the packet on Port X. These are code elements originating on Port N exclusive of EOP1-5, SOSA and SOSB (see 23.2.3 and 23.2.4).
EOP; repeater is sourcing end of packet delimiter (EOP1-5) as defined by the appropriate PMA on Port X (see 23.2.1.2 and 23.2.4.1).
bad_code; repeater is sourcing bad_code as defined by the PMA of the transmit port (see 23.2.4.1).
tx_err; repeater is sourcing a transmit error code element, either bad_code (see 23.2.4.1) or the code-group /H/ (see 24.2.2.1), or (ESC/0, 0/ESC) (see Figure 32–12) as appropriate to the outgoing PHY type.

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partition(X)

Flag from Partition state diagram for Port X, which determines whether a port receive path should be enabled or disabled.

Values: true; port has exceeded the consecutive collision limit.
false; port has not exceeded the consecutive collision limit.

part_opt(X)

Implementation option. Either value may be chosen for repeater implementation (see 27.3.1.6).

Values: true; port supports the recommended optional measures in the partition state machine.
false; port does not support the recommended optional measures in the partition state machine.

rxerror_status(X)

Signal received from PMA; indicates if Port X has detected an error condition from the PMA (see 23.3.7.1, Figure 24–14, and Figure 32–14).The repeater need not propagate this error condition during collision events.

Values: ERROR; the rxerror_status parameter of the PMA_RXERROR.indicate primitive for Port X is ERROR.
NO_ERROR; the rxerror_status parameter of the PMA_RXERROR.indicate primitive for Port X is NO_ERROR.

RX_ER(X)

Signal received from PCS; indicates if Port X has detected an error condition from the PCS (see 23.2.1.4, 24.2.3.2, 32.3.4.1, Figure 23–10, Figure 24–11, and Figure 32–13). The repeater need not propagate this error condition during collision events.

Values: true; the PCS RX_ER signal for Port X is asserted.
false; the PCS RX_ER signal for Port X is negated.

scarrier_present(X)

Signal received from PMA; indicates the status of sourced Carrier input at Port X.

Values: true; the carrier_status parameter of the PMA_CARRIER.indicate primitive for Port X is ON.
false; the carrier_status parameter of the PMA_CARRIER.indicate primitive for Port X is OFF.

source_type(X)

Signal received from PMA; indicates PMA type for Port X. The first port to assert activity maintains the source type status for all transmitting port(s) until activity is deasserted. Repeaters may optionally force nonequality on comparisons using this variable. It must then follow the behavior of the state diagrams accordingly and meet all the delay parameters as applicable for the real implemented port type(s).

Values: FXTX; the pma_type parameter of the PMA_TYPE.indicate primitive for Port X is X.
T4; the pma_type parameter of the PMA_TYPE.indicate primitive for Port X is T4.
T2; the pma_type parameter of the PMA_TYPE.indicate primitive for Port X is T2.

27.3.2.1.3 Functions

command(X)

A function that passes an inter-process flag to all ports specified by X.

Values: copy; indicates that the repeater core has summed the activity levels of its active ports and is in the ACTIVE state.
collision; indicates that the repeater core has summed the activity levels of its active ports and is in the JAM state.

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quiet; indicates that the repeater core has summed the activity levels of its active ports and is in the IDLE state.

port(Test)

A function that returns the designation of a port passing the test condition. For example, port(activity = scarrier_present) returns the designation: X for a port for which scarrier_present = true. If multiple ports meet the test condition, the Port function will be assigned one and only one of the acceptable values.

27.3.2.1.4 Timers

All timers operate in the same fashion. A timer is reset and starts timing upon entering a state where "start x_timer" is asserted. At time "x" after the timer has been started, "x_timer_done" is asserted and remains asserted until the timer is reset. At all other times, "x_timer_not_done" is asserted.

When entering a state where "start x_timer" is asserted, the timer is reset and restarted even if the entered state is the same as the exited state.

The timers used in the repeater state diagrams are defined as follows:

false_carrier_timer

Timer for length of false carrier (27.3.1.5.1) that must be present before the ISOLATION state is entered. The timer is done when it reaches 450 – 500 BT.

idle_timer

Timer for length of time without carrier activity that must be present before the ISOLATION state is exited (27.3.1.5.1). The timer is done when it reaches 33 000 ± 25% BT.

ipg_timer

Timer for length of time without carrier activity that must be present before carrier integrity tests (27.3.1.5.1) are re-enabled. The timer is done when it reaches 64 – 86 BT.

jabber_timer

Timer for length of carrier that must be present before the Jabber state (27.3.1.7), and optionally during a collision the Partition state (27.3.1.6), is entered. The timer is done when it reaches 40 000 – 75 000 BT.

no_collision_timer

Timer for length of packet without collision before the Partition state is exited (27.3.1.6). The timer is done when it reaches 450 – 560 BT.

valid_carrier_timer

Timer for length of valid carrier that must be present before the Isolation state is exited (27.3.1.5.1). The timer is done when it reaches 450 – 500 BT.

27.3.2.1.5 Counters

CC(X)

Consecutive port collision count for Port X. Partitioning occurs on a terminal count of CCLimit being reached.

Values: Non-negative integers up to a terminal count of CCLimit.

FCC(X)

False Carrier Counter for Port X. Isolation occurs on a terminal count of FCCLimit being reached.

Values: Non-negative integers up to a terminal count of FCCLimit.

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27.3.2.1.6 Port designation

Ports are referred to by number. Port information is obtained by replacing the X in the desired function with the number of the port of interest. Ports are referred to in general as follows:

X

Generic port designator. When X is used in a state diagram, its value is local to that diagram and not global to the set of state diagrams.

N

Is defined by the Port function on exiting the IDLE or JAM states of Figure 27–2. It indicates a port that caused the exit from these states.

ALL

Indicates all repeater ports are to be considered. All ports shall meet test conditions in order for the test to pass.

ALLXN

Indicates all ports except N should be considered. All ports considered shall meet the test conditions in order for the test to pass.

ANY

Indicates all ports are to be considered. One or more ports shall meet the test conditions in order for the test to pass.

ANYXN

Indicates any port other than N meeting the test conditions shall cause the test to pass.

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27.3.2.2 State diagrams

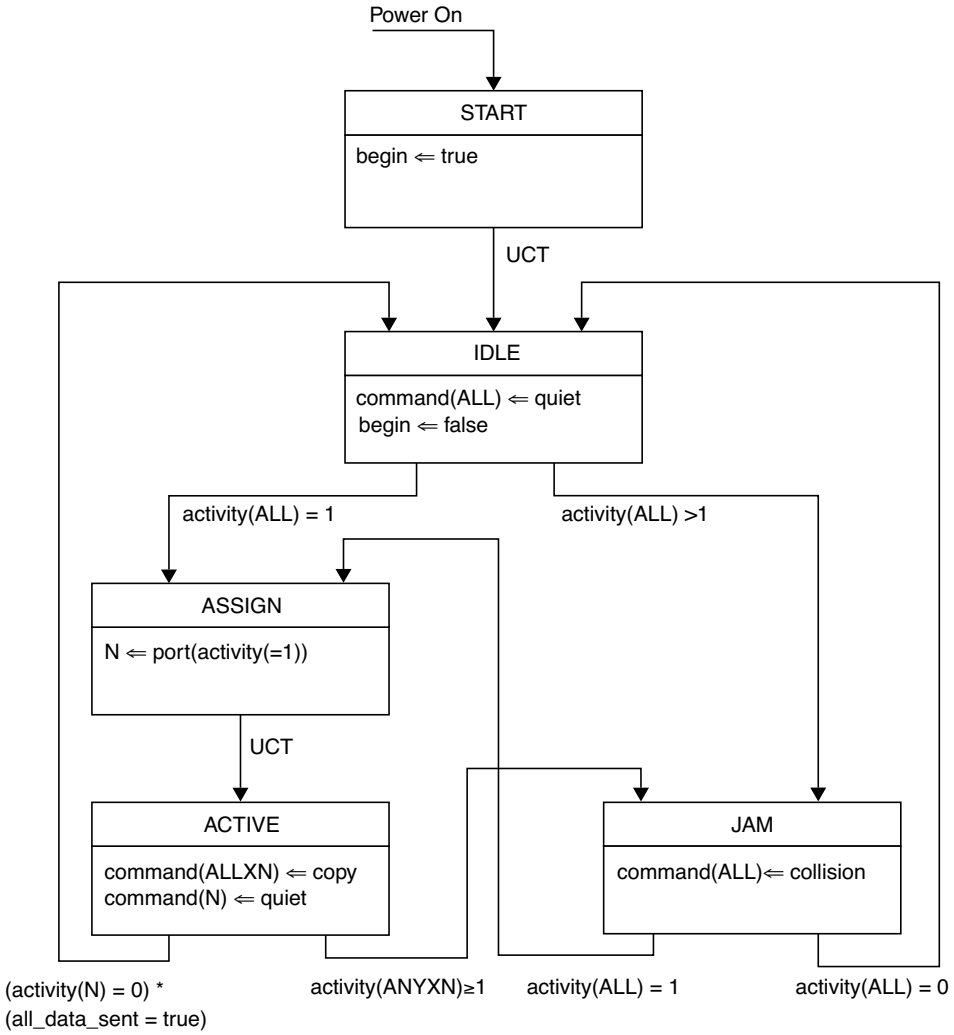


Figure 27–2—Repeater Core state diagram

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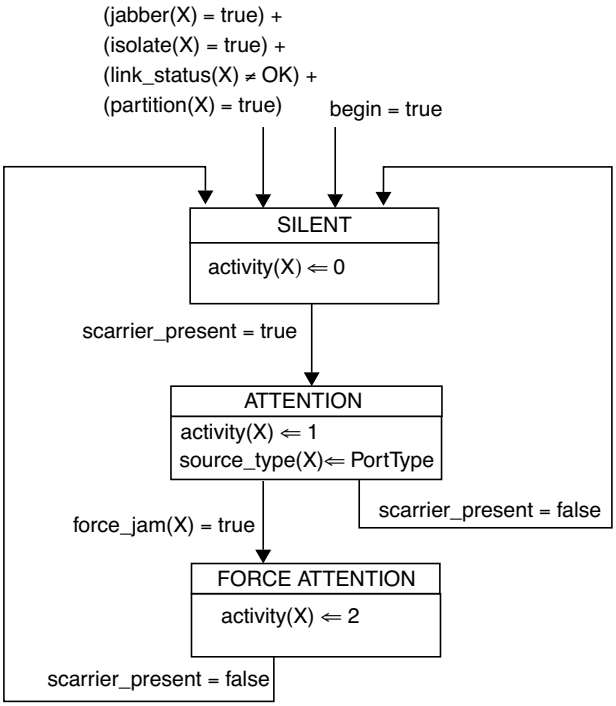


Figure 27–3—Receive state diagram for Port X

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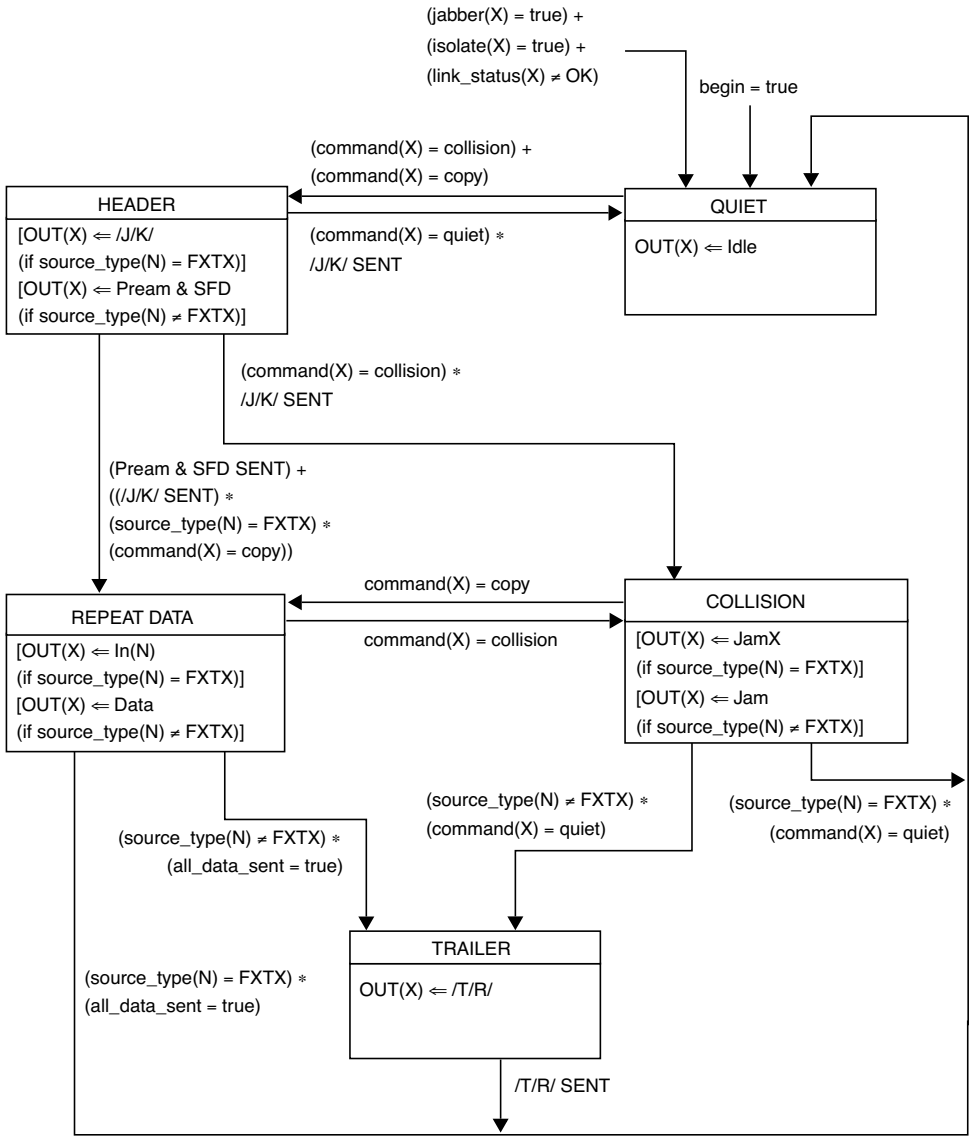


Figure 27–4—100BASE-TX and 100BASE-FX Transmit state diagram for Port X

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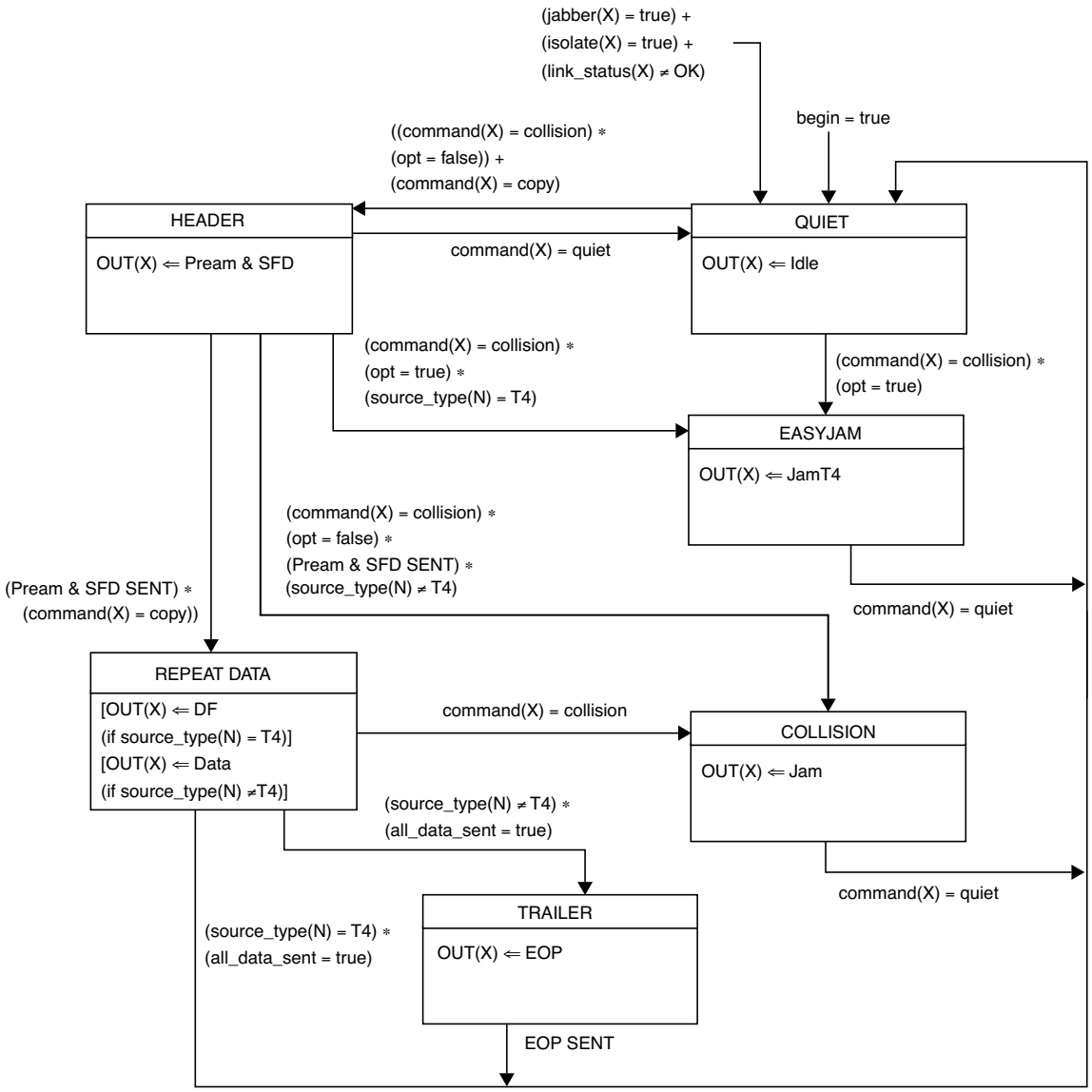


Figure 27–5—100BASE-T4 Transmit state diagram for Port X

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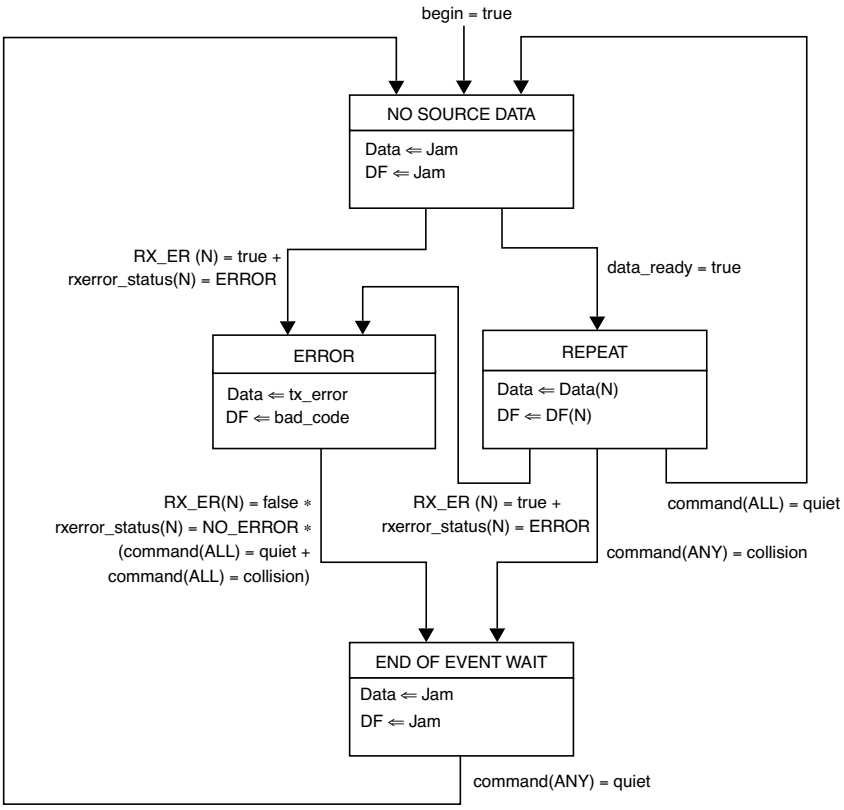


Figure 27–6—Repeater Data Handler state diagram

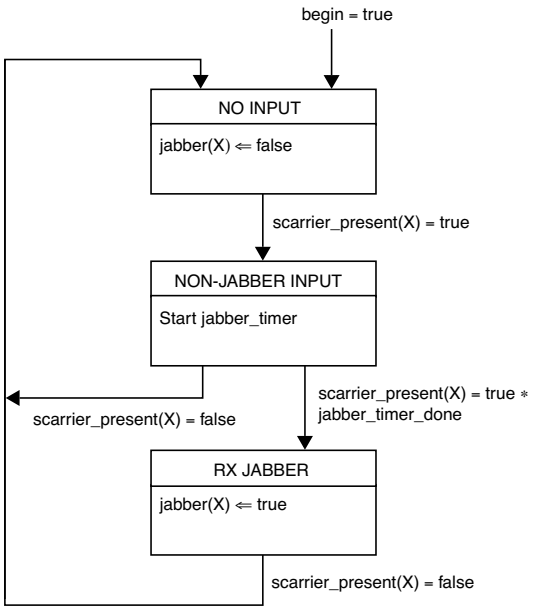


Figure 27–7—Receive Timer state diagram for Port X

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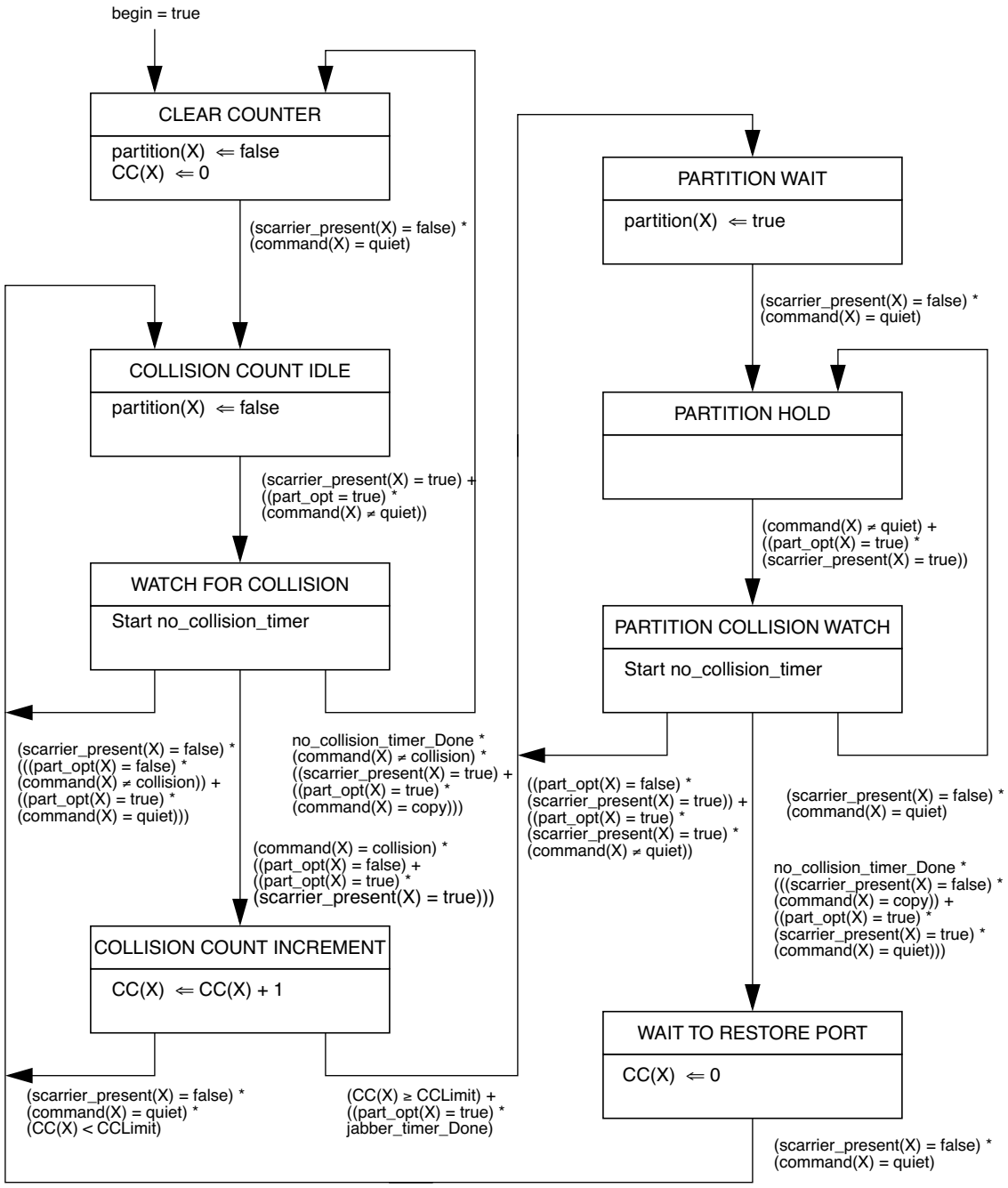


Figure 27–8—Partition state diagram for Port X

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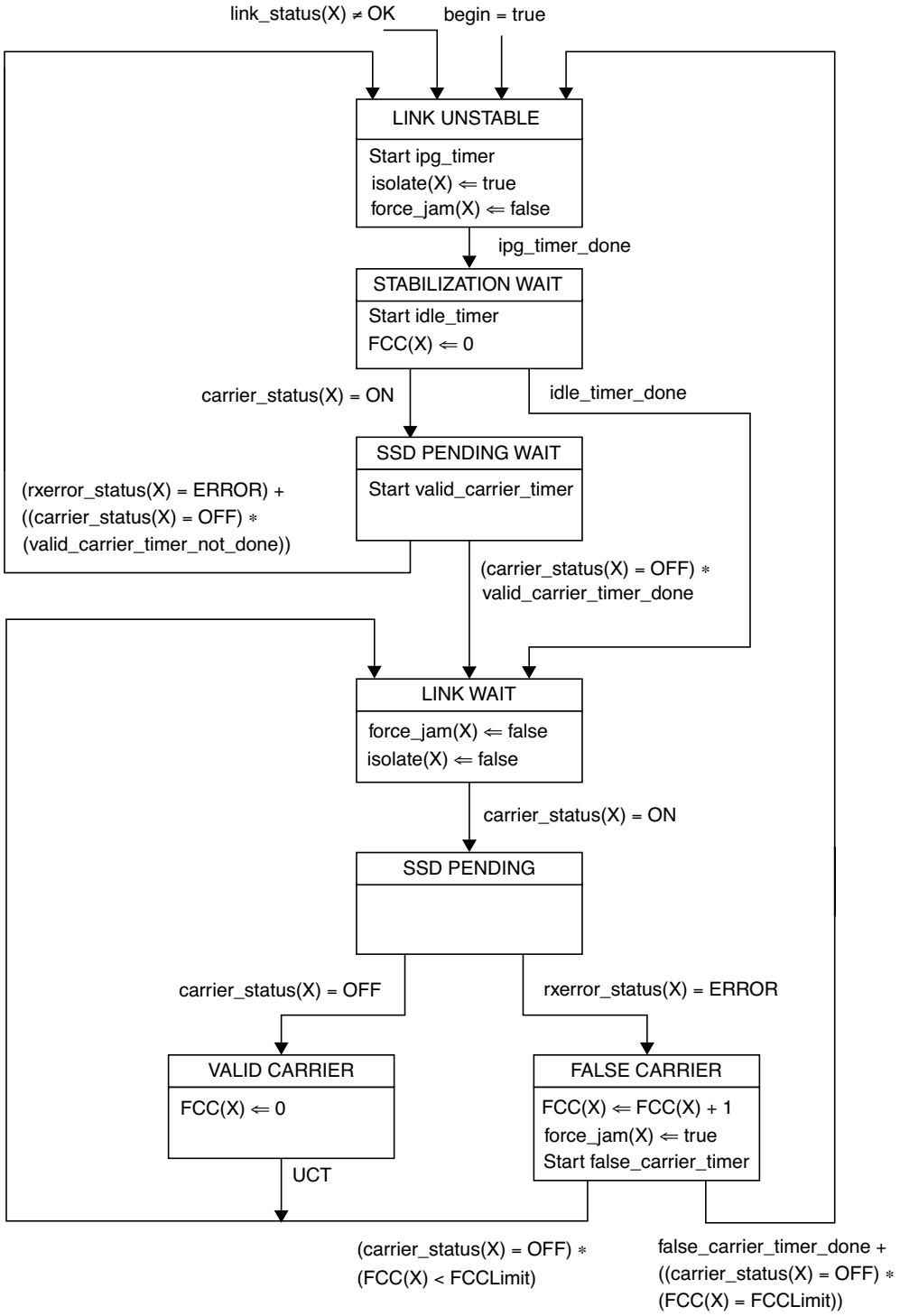


Figure 27–9—100BASE-X/T2 Carrier Integrity Monitor state diagram for Port X

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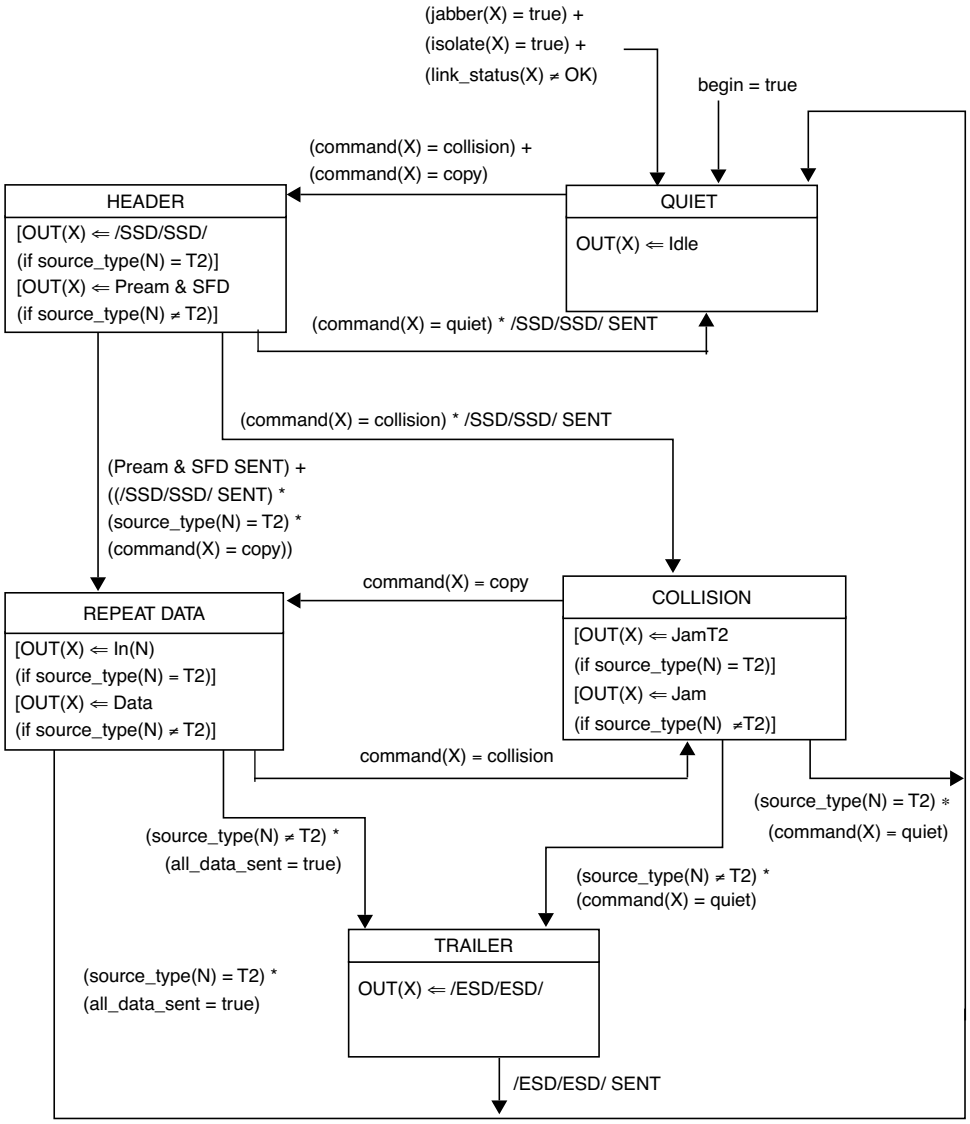


Figure 27–10—100BASE-T2 Transmit state diagram for Port X

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27.4 Repeater electrical specifications

27.4.1 Electrical isolation

Network segments that have different isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of the repeater set.

27.5 Environmental specifications

27.5.1 General safety

All equipment meeting this standard shall conform to IEC 60950: 1991.

27.5.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cable systems described in this subclause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cables and components.
c) High-energy transients coupled onto the LAN cable system.
d) Voltage potential differences between safety grounds to which the various LAN components are connected.

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network. Isolation requirements are defined in 27.5.3.

27.5.2.1 Installation

Sound installation practice, as defined by applicable local codes and regulations, shall be followed in every instance in which such practice is applicable.

27.5.2.2 Grounding

The safety ground, or chassis ground for the repeater set, shall be provided through the main ac power cord via the third wire ground as defined by applicable local codes and regulations. It is recommended that an external PHY to the repeater should also be mechanically grounded to the repeater unit through the power and ground signals in the MII connection and via the metal shell and shield of the MII connector if available.

If the MDI connector should provide a shield connection, the shield may be connected to the repeater safety ground. A network segment connected to the repeater set through the MDI may use a shield. If both ends of the network segment have a shielded MDI connector available, then the shield may be grounded at both ends according to local regulations and ISO/IEC 11801: 1995, and as long as the ground potential difference between both ends of the network segment is less than 1 V rms. The same rules apply towards an inter-repeater link between two repeaters. Multiple repeaters should reside on the same power main; if not, then it is highly recommended that the repeaters be connected via fiber.

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WARNING

It is assumed that the equipment to which the repeater is attached is properly grounded and not left floating nor serviced by a "doubly insulated ac power distribution system." The use of floating or insulated equipment, and the consequent implications for safety, are beyond the scope of this standard.

27.5.2.3 Installation and maintenance guidelines

During installation and maintenance of the cable plant, care should be taken to ensure that uninsulated network cable connectors do not make electrical contact with unintended conductors or ground.

27.5.3 Electrical isolation

There are two electrical power distribution environments to be considered that require different electrical isolation properties:

a) *Environment A*. When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.
b) *Environment B*. When a LAN crosses the boundary between separate power distribution systems or the boundary of a single building.

27.5.3.1 Environment A requirements

Attachment of network segments via repeater sets requires electrical isolation of 500 V rms, one-minute withstand, between the segment and the protective ground of the repeater unit.

27.5.3.2 Environment B requirements

The attachment of network segments that cross Environment B boundaries requires electrical isolation of 1500 V rms, one-minute withstand, between each segment and all other attached segments and also the protective ground of the repeater unit.

The requirements for interconnected electrically conducting LAN segments that are partially or fully external to a single building environment may require additional protection against lightning strike hazards. Such requirements are beyond the scope of this standard. It is recommended that the above situation be handled by the use of nonelectrically conducting segments (e.g., fiber optic).

It is assumed that any nonelectrically conducting segments will provide sufficient isolation within that media to satisfy the isolation requirements of Environment B.

27.5.4 Reliability

A two-port repeater set shall be designed to provide a mean time between failure (MTBF) of at least 50 000 hours of continuous operation without causing a communications failure among stations attached to the network medium. Repeater sets with more than two ports shall add no more than 3.46×10^{-6} failures per hour for each additional port.

The repeater set electronics should be designed to minimize the probability of component failures within the repeater electronics that prevent communications among other PHYs on the individual segments. Connectors and other passive components comprising the means of connecting the repeater to the cable should be designed to minimize the probability of total network failure.

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27.5.5 Environment

27.5.5.1 Electromagnetic emission

The repeater shall comply with applicable local and national codes for the limitation of electromagnetic interference.

27.5.5.2 Temperature and humidity

The repeater is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the repeater the operating environmental conditions to facilitate selection, installation, and maintenance.

27.6 Repeater labeling

It is required that each repeater (and supporting documentation) shall be labeled in a manner visible to the user with these parameters:

a) Crossover ports appropriate to the respective PHY should be marked with an X.
b) The repeater set class type should be labeled in the following manner:
    1) Class I: a Roman numeral “I” centered within a circle.
    2) Class II: a Roman numeral “II” centered within a circle.

Additionally, it is recommended that each repeater (and supporting documentation) also be labeled in a manner visible to the user with at least these parameters:

a) Data rate capability in Mb/s
b) Any applicable safety warnings
c) Port type, i.e., 100BASE-TX, 100BASE-T4, or 100BASE-T2
d) Worst-case bit time delays between any two ports appropriate for
    1) Start-of-packet propagation delay
    2) Start-of-collision Jam propagation delay
    3) Cessation-of-collision Jam propagation delay

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27.7 Protocol Implementation Conformance Statement (PICS) proforma for Clause 27, Repeater for 100 Mb/s baseband networks[10]

27.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 27, Repeater for 100 Mb/s baseband networks, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

27.7.2 Identification

27.7.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

27.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2002, Clause 27, Repeater for 100 Mb/s baseband networks
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

[10]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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27.7.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*FXP	Repeater supports 100BASE-FX connections	27.1.2.2	O		
*TXP	Repeater supports 100BASE-TX connections	27.1.2.2	O		
*T4P	Repeater supports 100BASE-T4 connections	27.1.2.2	O		
*T2P	Repeater supports 100BASE-T2 connections	27.1.2.2	O		
*CLI	Repeater meets Class I delays	27.1.1.3	O		
*CLII	Repeater meets Class II delays	27.1.1.3	O		
*PHYS	PHYs capable of detecting non 100BASE-T signals	27.3.1.5.2	O		
*OPF	Partition function supports the recommended optional measures as described	27.3.1.6	O		

In addition, the following predicate name is defined for use when different implementations from the set above have common parameters:

*XP:FXP or TXP

27.7.4 PICS proforma tables for the repeater for 100 Mb/s baseband networks

27.7.4.1 Compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
CC1	100BASE-FX port compatible at the MDI	27.1.2.2	FXP:M		
CC2	100BASE-TX port compatible at the MDI	27.1.2.2	TXP:M		
CC3	100BASE-T4 port compatible at the MDI	27.1.2.2	T4P:M		
CC4	Internal segment compatibility	27.1.2.2.1	M		Internal port meets Clause 30 when repeater management implemented
CC5	100BASE-T2 port compatible at the MDI	27.1.2.2	T2P:M		

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27.7.4.2 Repeater functions

Item	Feature	Subclause	Status	Support	Value/Comment
RF1	Signal Restoration	27.3.1	M		
RF2	Data Handling	27.3.1	M		
RF3	Received Event Handling	27.3.1	M		
RF4	Collision Handling	27.3.1	M		
RF5	Error Handling	27.3.1	M		
RF6	Partition	27.3.1	M		
RF7	Received Jabber	27.3.1	M		

27.7.4.3 Signal Restoration function

Item	Feature	Subclause	Status	Support	Value/Comment
SR1	Output amplitude as required by 100BASE-FX	27.3.1.1.1	FXP:M		
SR2	Output amplitude as required by 100BASE-TX	27.3.1.1.1	TXP:M		
SR3	Output amplitude as required by 100BASE-T4	27.3.1.1.1	T4P:M		
SR4	Output signal wave-shape as required by 100BASE-FX	27.3.1.1.2	FXP:M		
SR5	Output signal wave-shape as required by 100BASE-TX	27.3.1.1.2	TXP:M		
SR6	Output signal wave-shape as required by 100BASE-T4	27.3.1.1.2	T4P:M		
SR7	Output data timing as required by 100BASE-FX	27.3.1.1.3	FXP:M		
SR8	Output data timing as required by 100BASE-TX	27.3.1.1.3	TXP:M		
SR9	Output data timing as required by 100BASE-T4	27.3.1.1.3	T4P:M		
SR10	Output amplitude as required by 100BASE-T2	27.3.1.1.1	T2P:M		
SR11	Output signal wave-shape as required by 100BASE-T2	27.3.1.1.2	T2P:M		
SR12	Output data timing as required by 100BASE-T2	27.3.1.1.3	T2P:M		

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27.7.4.4 Data Handling function

Item	Feature	Subclause	Status	Support	Value/Comment
DH1	Data frames forwarded to all ports except receiving port	27.3.1.2.1	M		
DH2	Data frames transmitted as appropriate for 100BASE-FX	27.3.1.2.1	FXP:M		
DH3	Data frames transmitted as appropriate for 100BASE-TX	27.3.1.2.1	TXP:M		
DH4	Data frames transmitted as appropriate for 100BASE-T4	27.3.1.2.1	T4P:M		
DH5	Code Violations forwarded to all transmitting ports	27.3.1.2.2	M		
DH6	Code Violations forwarded as received	27.3.1.2.2	O.1		
DH7	Received Code Violation forwarded as /H/ or as received	27.3.1.2.2	XP:O.1		
DH8	Received Code Violation forwarded as bad_code or as received	27.3.1.2.2	T4P:O.1		
DH9	Code element substitution for remainder of packet after received Code Violation	27.3.1.2.2	M		
DH10	Data frames transmitted as appropriate for 100BASE-T2	27.3.1.2.1	T2P:M		

27.7.4.5 Receive Event Handling function

Item	Feature	Subclause	Status	Support	Value/Comment
RE1	scarrier_present detect implemented	27.3.1.3.1	M		
RE2	Repeat all received signals	27.3.1.3.1	M		
RE3	Preamble encoded as required by 100BASE-FX	27.3.1.3.2	FXP:M		
RE4	Preamble encoded as required by 100BASE-TX	27.3.1.3.2	TXP:M		
RE5	Preamble encoded as required by 100BASE-T4	27.3.1.3.2	T4P:M		
RE6	Start-of-packet propagation delay, Class I repeater	27.3.1.3.3	CLI:M		
RE7	Start-of-packet propagation delay, Class II repeater	27.3.1.3.3	CLII:M		
RE8	Start-of-packet variability for 100BASE-FX input port	27.3.1.3.4	FXP:M		7.0 BT

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27.7.4.5 Receive Event Handling function *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
RE8	Start-of-packet variability for 100BASE-TX input port	27.3.1.3.4	TXP:M		7.0 BT
RE9	Start-of-packet variability for 100BASE-T4 input port	27.3.1.3.4	T4P:M		8.0 BT
RE10	Preamble encoded as required by 100BASE-T2	27.3.1.3.2	T2P:M		
RE11	Start of packet variability for 100BASE-T2 input port	27.3.1.3.4	T2P:M		8.0 BT

27.7.4.6 Collision Handling function

Item	Feature	Subclause	Status	Support	Value/Comment
CO1	Collision Detection	27.3.1.4.1	M		Receive event on more than one port
CO2	Jam Generation	27.3.1.4.2	M		Transmit Jam message while collision is detected
CO3	Collision-jam propagation delay, Class I repeater	27.3.1.4.3	CLI:M		SOP + SOJ ≤ 140 BT
CO4	Collision-jam propagation delay, Class II repeater with any port T4	27.3.1.4.3	CLII:M		SOP + SOJ ≤ 67 BT
CO5	Collision-jam propagation delay, Class II repeater, all TX/FX ports	27.3.1.4.3	CLII:M		SOP ≤ 46, SOJ ≤ 46 BT
CO6	Cessation of collision propagation delay, Class I repeater	27.3.1.4.4	CLI:M		EOJ ≤ SOP
CO7	Cessation of collision propagation delay, Class II repeater	27.3.1.4.4	CLII:M		EOJ ≤ SOP
CO8	Collision-jam propagation delay, Class II repeater with any port T2	27.3.1.4.3	CLII * T2P:M		SOP + SOJ ≤ 90 BT

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27.7.4.7 Error Handling function

Item	Feature	Subclause	Status	Support	Value/Comment
EH1	Carrier Integrity function implementation	27.3.1.5.1	XP:M		Self-interrupt of data reception
EH2	False carrier count for Link Unstable detection	27.3.1.5.1	XP:M		False carrier count in excess of FCCLimit
EH3	False carrier count reset	27.3.1.5.1	XP:M		Count reset on valid carrier
EH4	False carrier timer for Link Unstable detection	27.3.1.5.1	XP:M		False carrier of length in excess of false_carrier_timer
EH5	Jam message duration	27.3.1.5.1	XP:M		Equals duration of false carrier event, but not greater than duration of false_carrier_timer
EH6	Link Unstable detection	27.3.1.5.1	XP:M		False Carrier count exceed FCCLimit or False carrier exceeds the false_carrier_timer or power-up reset
EH7	Messages sent to repeater unit in Link Unstable state	27.3.1.5.1	XP:M		Inhibited sending messages to repeater unit
EH8	Messages sent from repeater unit in Link Unstable state	27.3.1.5.1	XP:M		Inhibited sending output messages
EH9	Monitoring activity on PMA interface in Link Unstable state	27.3.1.5.1	XP:M		Continue monitoring activity at PMA interface
EH10	Reset of Link Unstable state	27.3.1.5.1	XP:M		No activity for more than ipg_timer plus idle_timer or Valid carrier event of duration greater than valid_carrier_timer preceded by Idle of duration greater than ipg_timer
EH11	Block flow of non-100 Mb/s signals	27.3.1.5.2	PHYS:M		

27.7.4.8 Partition functions

Item	Feature	Subclause	Status	Support	Value/Comment
PA1	Partition function implementation	27.3.1.6	M		Self-interrupt of data reception
PA2	Collision count for entry into partition state	27.3.1.6	M		Collision count greater than or equal to CCLimit
PA3	Collision counter incrementing	27.3.1.6	M		Count incremented on a collision
PA4	Collision counter reset	27.3.1.6	M		Count reset on receive activity in excess of no_collision_timer without collision

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27.7.4.8 Partition functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PA5			OPF:M		Count reset on transmission in excess of no_collision_timer without collision
PA6	Messages sent to repeater unit in Partition state	27.3.1.6	M		Inhibited sending messages to repeater unit
PA7	Messages sent from repeater unit in Partition state	27.3.1.6	M		Continue sending output messages
PA8	Monitoring activity on PMA interface in Partition state	27.3.1.6	M		Continue monitoring activity at PMA interface
PA9	Reset of Partition state	27.3.1.6	M		Power-up reset or transmission in excess of no_collision_timer without collision
PA10			OPF:M		Receive activity in excess of no_collision_timer without collision
PA11	Excessive carrier entry into Partition state	27.3.1.6	OPF:M		Carrier duration in excess of jabber_timer in which a collision occurs

27.7.4.9 Receive Jabber function

Item	Feature	Subclause	Status	Support	Value/Comment
RJ1	Receive Jabber function implementation	27.3.1.7	M		Self-interrupt of data reception
RJ2	Excessive receive duration timer for Receive Jabber detection	27.3.1.7	M		Reception duration in excess of jabber_timer
RJ3	Messages sent to repeater unit in Receive Jabber state	27.3.1.7	M		Inhibit sending input messages to repeater unit
RJ4	Messages sent from repeater unit in Receive Jabber state	27.3.1.7	M		Inhibit sending output messages
RJ5	Reset of Receive Jabber state	27.3.1.7	M		Power-up reset or Carrier no longer detected

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27.7.4.10 Repeater state diagrams

Item	Feature	Subclause	Status	Support	Value/Comment
SD1	Repeater Core state diagram	27.3.2.2	M		Meets the requirements of Figure 27–2
SD2	Receive state diagram for Port X	27.3.2.2	M		Meets the requirements of Figure 27–3
SD3	100BASE-TX and 100BASE-FX Transmit state diagram for Port X	27.3.2.2	XP:M		Meets the requirements of Figure 27–4
SD4	100BASE-T4 Transmit state diagram for Port X	27.3.2.2	T4P:M		Meets the requirements of Figure 27–5
SD5	Repeater Data Handler state diagram	27.3.2.2	M		Meets the requirements of Figure 27–6
SD6	Receive Timer for Port X state diagram	27.3.2.2	M		Meets the requirements of Figure 27–7
SD7	Repeater Partition state diagram for Port X	27.3.2.2	M		Meets the requirements of Figure 27–8
SD8	Carrier Integrity Monitor for Port X state diagram	27.3.2.2	M		Meets the requirements of Figure 27–9
SD9	100BASE-T2 Transmit state diagram for Port X	27.3.2.2	T2P:M		Meets the requirements of Figure 27–10

27.7.4.11 Repeater electrical

Item	Feature	Subclause	Status	Support	Value/Comment
EL1	Port-to-port isolation	27.4.1	M		Satisfies isolation and grounding requirements for attached network segments
EL2	Safety	27.5.1	M		IEC 60950: 1991
EL3	Installation practices	27.5.2.1	M		Sound, as defined by local code and regulations
EL4	Grounding	27.5.2.2	M		Chassis ground provided through ac mains cord
EL5	2-port repeater set MTBF	27.5.4	M		At least 50 000 hours
EL6	Additional port effect on MTBF	27.5.4	M		No more than 3.46×10^{-6} increase in failures per hour
EL7	Electromagnetic interference	27.5.5.1	M		Comply with local or national codes

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27.7.4.12 Repeater labeling

Item	Feature	Subclause	Status	Support	Value/Comment
LB1	Crossover ports	27.6	M		Marked with an X
LB2	Class I repeater	27.6	CLI:M		Marked with a Roman numeral I centered within a circle
LB3	Class II repeater	27.6	CLII:M		Marked with Roman numerals II centered within a circle
LB4	Data Rate	27.6	O		100 Mb/s
LB5	Safety warnings	27.6	O		Any applicable
LB6	Port Types	27.6	O		100BASE-FX or 100BASE-TX or 100BASE-T4 or 100BASE-T2
LB7	Worse-case start-of-packet propagation delay	27.6	O		Value in Bit Times
LB8	Worse-case start-of-collision-Jam propagation delay	27.6	O		Value in Bit Times
LB9	Worse-case cessation-of-collision Jam propagation delay	27.6	O		Value in Bit Times

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28. Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Auto-Negotiation on twisted pair

28.1 Overview

28.1.1 Scope

Clause 28 describes the Auto-Negotiation function that allows a device to advertise enhanced modes of operation it possesses to a device at the remote end of a link segment and to detect corresponding enhanced operational modes that the other device may be advertising. The normative definitions for all extensions to Auto-Negotiation and all related register assignments for this standard are documented in Annex 28D.

The objective of the Auto-Negotiation function is to provide the means to exchange information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities. Auto-Negotiation is performed using a modified 10BASE-T link integrity test pulse sequence, such that no packet or upper layer protocol overhead is added to the network devices (see Figure 28–1). Auto-Negotiation does not test the link segment characteristics (see 28.1.4).

The function allows the devices at both ends of a link segment to advertise abilities, acknowledge receipt and understanding of the common mode(s) of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function. The Auto-Negotiation function allows the devices to switch between the various operational modes in an ordered fashion, permits management to disable or enable the Auto-Negotiation function, and allows management to select a specific operational mode. The Auto-Negotiation function also provides a Parallel Detection function to allow 10BASE-T, 100BASE-TX, and 100BASE-T4 compatible devices to be recognized, even though they may not provide Auto-Negotiation.

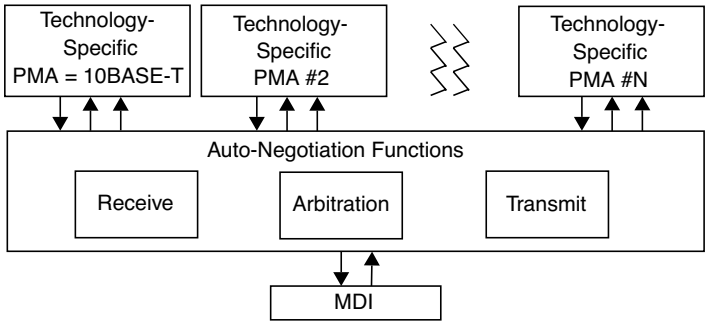


Figure 28–1—High-level model

The basic mechanism to achieve Auto-Negotiation is to pass information encapsulated within a burst of closely spaced link integrity test pulses that individually meet the 10BASE-T Transmitter Waveform for Link Test Pulse (Figure 14–12). This burst of pulses is referred to as a Fast Link Pulse (FLP) Burst. Each device capable of Auto-Negotiation issues FLP Bursts at power up, on command from management, or due to user interaction. The FLP Burst consists of a series of link integrity test pulses that form an alternating clock/data sequence. Extraction of the data bits from the FLP Burst yields a Link Code Word that identifies the operational modes supported by the remote device, as well as some information used for the Auto-Negotiation function's handshake mechanism.

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To maintain interoperability with existing 10BASE-T devices, the function also supports the reception of 10BASE-T compliant link integrity test pulses. 10BASE-T link pulse activity is referred to as the Normal Link Pulse (NLP) sequence and is defined in 14.2.1.1. A device that fails to respond to the FLP Burst sequence by returning only the NLP sequence is treated as a 10BASE-T compatible device.

28.1.2 Application perspective/objectives

The Auto-Negotiation function is designed to be expandable and allow IEEE 802.3 compatible devices using an eight-pin modular connector to self-configure a jointly compatible operating mode. Implementation of the Auto-Negotiation function is optional. However, it is highly recommended that this method alone be utilized to perform the negotiation of the link operation.

The following are the objectives of Auto-Negotiation:

a) Must interoperate with the IEEE 802.3 10BASE-T installed base.
b) Must allow automatic upgrade from the 10BASE-T mode to the desired “High-Performance Mode.”
c) Requires that the 10BASE-T data service is the Lowest Common Denominator (LCD) that can be resolved. A 10BASE-T PMA is not required to be implemented, however. Only the NLP Receive Link Integrity Test function is required.
d) Reasonable and cost-effective to implement.
e) Must provide a sufficiently extensible code space to
    1) Meet existing and future requirements.
    2) Allow simple extension without impacting the installed base.
    3) Accommodate remote fault signals.
    4) Accommodate link partner ability detection.
f) Must allow manual or Network Management configuration to override the Auto-Negotiation.
g) Must be capable of operation in the absence of Network Management.
h) Must not preclude the ability to negotiate “back” to the 10BASE-T operational mode.
i) Must operate when
    1) The link is initially electrically connected.
    2) A device at either end of the link is powered up, reset, or a renegotiation request is made.
j) The Auto-Negotiation function may be enabled by automatic, manual, or Network Management intervention.
k) Completes the base page Auto-Negotiation function in a bounded time period.
l) Will provide the basis for the link establishment process in future CSMA/CD compatible LAN standards that use an eight-pin modular connector.
m) Must not cause corruption of IEEE 802.3 Layer Management statistics.
n) Operates using a peer-to-peer exchange of information with no requirement for a master device (not master-slave).
o) Must be robust in the UTP cable noise environment.
p) Must not significantly impact EMI/RFI emissions.

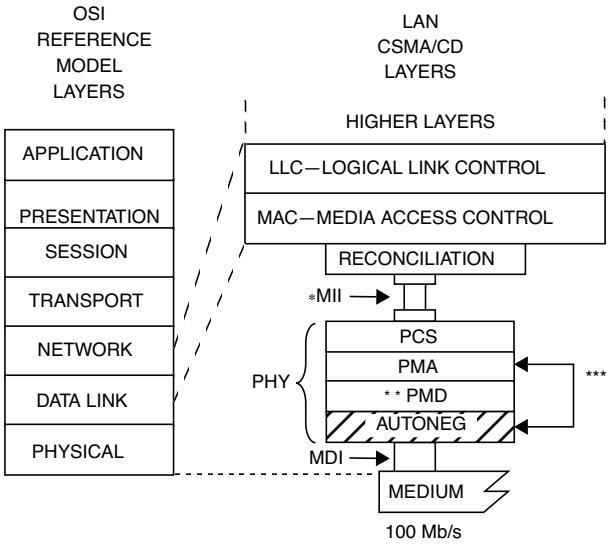
28.1.3 Relationship to ISO/IEC 8802-3

The Auto-Negotiation function is provided at the Physical Layer of the OSI reference model as shown in Figure 28–2. Devices that support multiple modes of operation may advertise this fact using this function. The actual transfer of information of ability is observable only at the MDI or on the medium. Auto-Negotiation signaling does not occur across either the AUI or MII. Control of the Auto-Negotiation function may be supported through the Management Interface of the MII or equivalent. If an explicit embodiment of the MII is supported, the control and status registers to support the Auto-Negotiation function shall be implemented in accordance with the definitions in Clause 22 and 28.2.4. If a physical embodiment of the MII management is not present, then it is strongly recommended that the implementation provide control and status mechanisms equivalent to those described in Clause 22 and 28.2.4 for manual and/or management interaction.

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MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
AUTONEG = AUTO-NEGOTIATION
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* MII is optional for 10 Mb/s DTEs and for 100 Mb/s systems and is not specified for 1 Mb/s systems.
** PMD is specified for 100BASE-X only; 100BASE-T4 does not use this layer.
*** AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indicate.

Figure 28–2—Location of Auto-Negotiation function within the ISO/IEC OSI reference model

28.1.4 Compatibility considerations

The Auto-Negotiation function is designed to be completely backwards compatible and interoperable with 10BASE-T compliant devices. In order to achieve this, a device supporting the Auto-Negotiation function must provide the NLP Receive Link Integrity Test function as defined in Figure 28–17. The Auto-Negotiation function also supports connection to 100BASE-TX and 100BASE-T4 devices without Auto-Negotiation through the Parallel Detection function. Connection to technologies other than 10BASE-T, 100BASE-TX, or 100BASE-T4 that do not incorporate Auto-Negotiation is not supported.

Implementation of the Auto-Negotiation function is optional. For CSMA/CD compatible devices that use the eight-pin modular connector of ISO/IEC 8877: 1992 and that also encompass multiple operational modes, if a signaling method is used to automatically configure the preferred mode of operation, then the Auto-Negotiation function shall be used in compliance with Clause 28. If the device uses 10BASE-T compatible link signaling to advertise non-CSMA/CD abilities, the device shall implement the Auto-Negotiation function as administered by this specification. All future CSMA/CD implementations that use an eight-pin modular connector shall be interoperable with devices supporting Clause 28. If the implementor of a non-CSMA/CD eight-pin modular device wishes to assure that its operation does not conflict with CSMA/CD devices, then adherence to Clause 28 is recommended.

While this Auto-Negotiation function must be implemented in CSMA/CD compatible devices that utilize the eight-pin modular connector, encompass multiple operational modes, and offer an Auto-Negotiation mechanism, the use of this function does not mandate that the 10BASE-T packet data communication service must exist. A device that employs this function must support the 10BASE-T Link Integrity Test function through

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the NLP Receive Link Integrity Test state diagram. The device may also need to support other technology-dependent link test functions depending on the modes supported. Auto-Negotiation does not perform cable tests, such as detect number of conductor pairs (if more than two pairs are required) or cable performance measurements. Some PHYs that explicitly require use of high-performance cables, may require knowledge of the cable type, or additional robustness tests (such as monitoring CRC or framing errors) to determine if the link segment is adequate.

28.1.4.1 Interoperability with existing 10BASE-T devices

During Auto-Negotiation, FLP Bursts separated by 16 ± 8 ms are transmitted. The FLP Burst itself is a series of pulses separated by 62.5 ± 7 μs. The timing of FLP Bursts will cause a 10BASE-T device that is in the LINK TEST PASS state to remain in the LINK TEST PASS state while receiving FLP Bursts. An Auto-Negotiation able device must recognize the NLP sequence from a 10BASE-T Link Partner, cease transmission of FLP Bursts, and enable the 10BASE-T PMA, if present. If the NLP sequence is detected and if the Auto-Negotiation able device does not have a 10BASE-T PMA, it will cease transmission of FLP Bursts, forcing the 10BASE-T Link Partner into the LINK TEST FAIL state(s) as indicated in Figure 14–6.

NOTE—Auto-Negotiation does not support the transmission of the NLP sequence. The 10BASE-T PMA provides this function if it is connected to the MDI. In the case where an Auto-Negotiation able device without a 10BASE-T PMA is connected to a 10BASE-T device without Auto-Negotiation, the NLP sequence is not transmitted because the Auto-Negotiation function has no 10BASE-T PMA to enable that can transmit the NLP sequence.

28.1.4.2 Interoperability with Auto-Negotiation compatible devices

An Auto-Negotiation compatible device decodes the base Link Code Word from the FLP Burst, and examines the contents for the highest common ability that both devices share. Both devices acknowledge correct receipt of each other's base Link Code Words by responding with FLP Bursts containing the Acknowledge Bit set. After both devices complete acknowledgment, and optionally, Next Page exchange, both devices enable the highest common mode negotiated. The highest common mode is resolved using the priority resolution hierarchy specified in Annex 28B. It may subsequently be the responsibility of a technology-dependent link integrity test function to verify operation of the link prior to enabling the data service.

28.1.4.3 Cabling compatibility with Auto-Negotiation

Provision has been made within Auto-Negotiation to limit the resulting link configuration in situations where the cabling may not support the highest common capability of the two end points. The system administrator/installer must take the cabling capability into consideration when configuring a hub port's advertised capability. That is, the advertised capability of a hub port should not result in an operational mode that is not compatible with the cabling.

28.2 Functional specifications

The Auto-Negotiation function provides a mechanism to control connection of a single MDI to a single PMA type, where more than one PMA type may exist. Management may provide additional control of Auto-Negotiation through the Management function, but the presence of a management agent is not required.

The Auto-Negotiation function shall provide the Auto-Negotiation Transmit, Receive, Arbitration, and NLP Receive Link Integrity Test functions and comply with the state diagrams of Figures 28–14 to 28–17. The Auto-Negotiation functions shall interact with the technology-dependent PMAs through the Technology-Dependent Interface. Technology-dependent PMAs include, but are not limited to, 100BASE-TX and 100BASE-T4. Technology-dependent link integrity test functions shall be implemented and interfaced to only if the device supports the given technology. For example, a 10BASE-T and 100BASE-TX Auto-Negotiation able device must implement and interface to the 100BASE-TX PMA/link integrity test function, but

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does not need to include the 100BASE-T4 PMA/Link Integrity Test function. The Auto-Negotiation function shall provide an optional Management function that provides a control and status mechanism.

28.2.1 Transmit function requirements

The Transmit function provides the ability to transmit FLP Bursts. The first FLP Bursts exchanged by the Local Device and its Link Partner after Power-On, link restart, or renegotiation contain the base Link Code Word defined in 28.2.1.2. The Local Device may modify the Link Code Word to disable an ability it possesses, but will not transmit an ability it does not possess. This makes possible the distinction between local abilities and advertised abilities so that multimode devices may Auto-Negotiate to a mode lower in priority than the highest common local ability.

28.2.1.1 Link pulse transmission

Auto-Negotiation's method of communication builds upon the link pulse mechanism employed by 10BASE-T MAUs to detect the status of the link. Compliant 10BASE-T MAUs transmit link integrity test pulses as a mechanism to determine if the link segment is operational in the absence of packet data. The 10BASE-T NLP sequence is a pulse (Figure 14–12) transmitted every 16 ± 8 ms while the data transmitter is idle.

Auto-Negotiation substitutes the FLP Burst in place of the single 10BASE-T link integrity test pulse within the NLP sequence (Figure 28–3). The FLP Burst encodes the data that is used to control the Auto-Negotiation function. FLP Bursts shall not be transmitted when Auto-Negotiation is complete and the highest common denominator PMA has been enabled.

FLP Bursts were designed to allow use beyond initial link Auto-Negotiation, such as for a link monitor type function. However, use of FLP Bursts beyond the current definition for link startup shall be prohibited. Definition of the use of FLP Bursts while in the FLP LINK GOOD state is reserved.

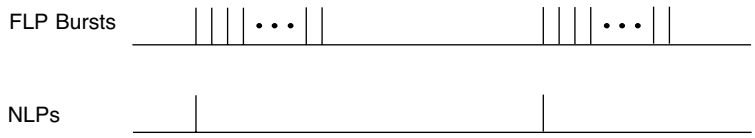


Figure 28–3—FLP Burst sequence to NLP sequence mapping

28.2.1.1.1 FLP burst encoding

FLP Bursts shall be composed of link pulses meeting the requirements of Figure 14–12. A Fast Link Pulse Burst consists of 33 pulse positions. The 17 odd-numbered pulse positions shall contain a link pulse and represent clock information. The 16 even-numbered pulse positions shall represent data information as follows: a link pulse present in an even-numbered pulse position represents a logic one, and a link pulse absent from an even-numbered pulse position represents a logic zero. Clock pulses are differentiated from data pulses by the spacing between pulses as shown in Figure 28–5 and enumerated in Table 28–1.

The encoding of data using pulses in an FLP Burst is illustrated in Figure 28–4.

28.2.1.1.2 Transmit timing

The first pulse in an FLP Burst shall be defined as a clock pulse. Clock pulses within an FLP Burst shall be spaced at 125 ± 14 μs. If the data bit representation of logic one is to be transmitted, a pulse shall occur 62.5 ± 7 μs after the preceding clock pulse. If a data bit representing logic zero is to be transmitted, there shall be no link integrity test pulses within 111 μs of the preceding clock pulse.

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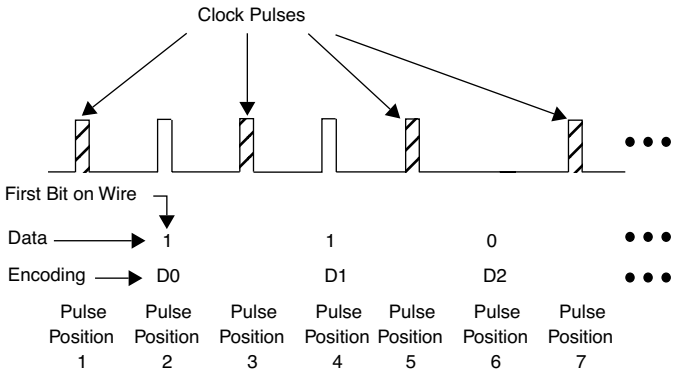


Figure 28–4—Data bit encoding within FLP Bursts

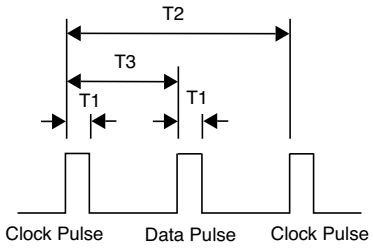


Figure 28–5—FLP Burst pulse-to-pulse timing

The first link pulse in consecutive FLP Bursts shall occur at a 16 ± 8 ms interval (Figure 28–6).



Figure 28–6—FLP Burst to FLP Burst timing

Table 28–1—FLP Burst timing summary

#	Parameter	Min.	Typ.	Max.	Units
T1	Clock/Data Pulse Width (Figure 14–12)		100		ns
T2	Clock Pulse to Clock Pulse	111	125	139	µs
T3	Clock Pulse to Data Pulse (Data = 1)	55.5	62.5	69.5	µs
T4	Pulses in a Burst	17		33	#
T5	Burst Width		2		ms
T6	FLP Burst to FLP Burst	8	16	24	ms

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28.2.1.2 Link Code Word encoding

The base Link Code Word (base page) transmitted within an FLP Burst shall convey the encoding shown in Figure 28–7. The Auto-Negotiation function may support additional pages using the Next Page function. Encodings for the Link Code Word(s) used in Next Page exchange are defined in 28.2.3.4. In an FLP Burst, D0 shall be the first bit transmitted.

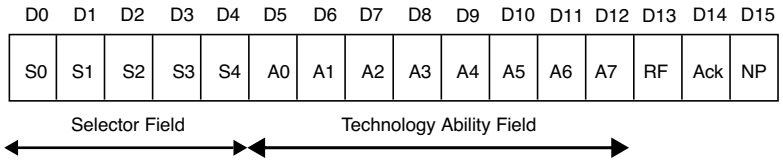


Figure 28–7—Base page encoding

28.2.1.2.1 Selector Field

Selector Field (S[4:0]) is a five bit wide field, encoding 32 possible messages. Selector Field encoding definitions are shown in Annex 28A. Combinations not specified are reserved for future use. Reserved combinations of the Selector Field shall not be transmitted.

28.2.1.2.2 Technology Ability Field

Technology Ability Field (A[7:0]) is an eight bit wide field containing information indicating supported technologies specific to the selector field value. These bits are mapped to individual technologies such that abilities are advertised in parallel for a single selector field value. The Technology Ability Field encoding for the IEEE 802.3 selector is described in Annex 28B.2 and in Annex 28D. Multiple technologies may be advertised in the Link Code Word. A device shall support the data service ability for a technology it advertises. It is the responsibility of the Arbitration function to determine the common mode of operation shared by a Link Partner and to resolve multiple common modes.

NOTE—While devices using a Selector Field value other than the IEEE 802.3 Selector Field value are free to define the Technology Ability Field bits, it is recommended that the 10BASE-T bit be encoded in the same bit position as in the IEEE 802.3 selector. A common bit position can be important if the technology using the other selector will ever coexist on a device that also offers a 10BASE-T mode.

28.2.1.2.3 Remote Fault

Remote Fault (RF) is encoded in bit D13 of the base Link Code Word. The default value is logic zero. The Remote Fault bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the Auto-Negotiation advertisement register (Register 4) is set to logic one, the RF bit in the transmitted base Link Code Word is set to logic one. When the RF bit in the received base Link Code Word is set to logic one, the Remote Fault bit in the MII status register (Register 1) will be set to logic one, if the MII management function is present.

The Remote Fault bit shall be used in accordance with the Remote Fault function specifications (28.2.3.5).

28.2.1.2.4 Acknowledge

Acknowledge (Ack) is used by the Auto-Negotiation function to indicate that a device has successfully received its Link Partner's Link Code Word. The Acknowledge Bit is encoded in bit D14 regardless of the value of the Selector Field or Link Code Word encoding. If no Next Page information is to be sent, this bit

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shall be set to logic one in the Link Code Word after the reception of at least three consecutive and consistent FLP Bursts (ignoring the Acknowledge bit value). If Next Page information is to be sent, this bit shall be set to logic one after the device has successfully received at least three consecutive and matching FLP Bursts (ignoring the Acknowledge bit value), and will remain set until the Next Page information has been loaded into the Auto-Negotiation Next Page transmit register (Register 7). In order to save the current received Link Code Word, it must be read from the Auto-Negotiation link partner ability register (Register 6) before the Next Page of transmit information is loaded into the Auto-Negotiation Next Page transmit register. After the COMPLETE ACKNOWLEDGE state has been entered, the Link Code Word shall be transmitted six to eight (inclusive) times.

28.2.1.2.5 Next Page

Next Page (NP) is encoded in bit D15 regardless of the Selector Field value or Link Code Word encoding. Support for transmission and reception of additional Link Code Word encodings is optional. If Next Page ability is not supported, the NP bit shall always be set to logic zero. If a device implements Next Page ability and wishes to engage in Next Page exchange, it shall set the NP bit to logic one. A device may implement Next Page ability and choose not to engage in Next Page exchange by setting the NP bit to a logic zero. The Next Page function is defined in 28.2.3.4.

28.2.1.3 Transmit Switch function

The Transmit Switch function shall enable the transmit path from a single technology-dependent PMA to the MDI once a highest common denominator choice has been made and Auto-Negotiation has completed.

During Auto-Negotiation, the Transmit Switch function shall connect only the FLP Burst generator controlled by the Transmit State Diagram, Figure 28–14, to the MDI.

When a PMA is connected to the MDI through the Transmit Switch function, the signals at the MDI shall conform to all of the PHY's specifications.

28.2.2 Receive function requirements

The Receive function detects the NLP sequence using the NLP Receive Link Integrity Test function of Figure 28–17. The NLP Receive Link Integrity Test function will not detect link pass based on carrier sense.

The Receive function detects the FLP Burst sequence, decodes the information contained within, and stores the data in rx_link_code_word[16:1]. The Receive function incorporates a receive switch to control connection to the 100BASE-TX or 100BASE-T4 PMAs in addition to the NLP Receive Link Integrity Test function, excluding the 10BASE-T Link Integrity Test function present in a 10BASE-T PMA. If Auto-Negotiation detects link_status=READY from any of the technology-dependent PMAs prior to FLP Burst detection, the autoneg_wait_timer (28.3.2) is started. If any other technology-dependent PMA indicates link_status=READY when the autoneg_wait_timer expires, Auto-Negotiation will not allow any data service to be enabled and may signal this as a remote fault to the Link Partner using the base page and will flag this in the Local Device by setting the Parallel Detection Fault bit (6.4) in the Auto-Negotiation expansion register. If a 10BASE-T PMA exists above the Auto-Negotiation function, it is not permitted to receive MDI activity in parallel with the NLP Receive Link Integrity Test function or any other technology-dependent function.

28.2.2.1 FLP Burst ability detection and decoding

In Figures 28–8 to 28–10, the symbol "t_0=0" indicates the event that caused the timers described to start, and all subsequent times given are referenced from that point. All timers referenced shall expire within the range specified in Table 28–9 in 28.3.2.

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The Receive function shall identify the Link Partner as Auto-Negotiation able if it receives 6 to 17 (inclusive) consecutive link pulses that are separated by at least flp_test_min_timer time (5–25 μs) but less than flp_test_max_timer time (165–185 μs) as shown in Figure 28–8. The information contained in the FLP Burst that identifies the Link Partner as Auto-Negotiation able shall not be passed to the Arbitration function if the FLP Burst is not complete. The Receive function may use the FLP Burst that identifies the Link Partner as Auto-Negotiation able for ability matching if the FLP Burst is complete. However, it is not required to use this FLP Burst for any purpose other than identification of the Link Partner as Auto-Negotiation able. Implementations may ignore multiple FLP Bursts before identifying the Link Partner as Auto-Negotiation able to allow for potential receive equalization time.

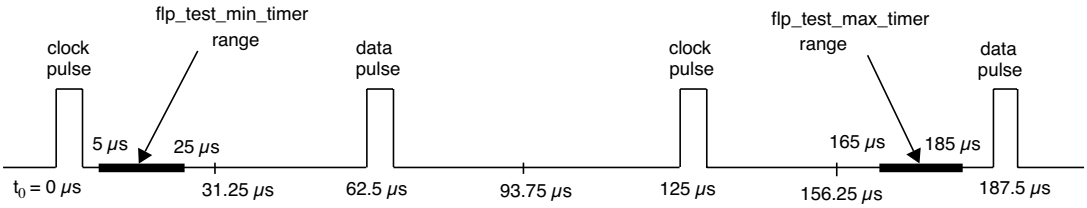


Figure 28–8—FLP detect timers (flp_test_min/max_timers)

The Receive function captures and decodes link pulses received in FLP Bursts. The first link pulse in an FLP Burst shall be interpreted as a clock link pulse. Detection of a clock link pulse shall restart the data_detect_min_timer and data_detect_max timer. The data_detect_min/max_timers enable the receiver to distinguish data pulses from clock pulses and logic one data from logic zero data, as follows:

a) If, during an FLP Burst, a link pulse is received when the data_detect_min_timer has expired while the data_detect_max_timer has not expired, the data bit shall be interpreted as a logic one (Figure 28–9).
b) If, during an FLP Burst, a link pulse is received after the data_detect_max_timer has expired, the data bit shall be interpreted as a logic zero (Figure 28–9) and that link pulse shall be interpreted as a clock link pulse.

As each data bit is identified it is stored in the appropriate rx_link_code_word[16:1] element.

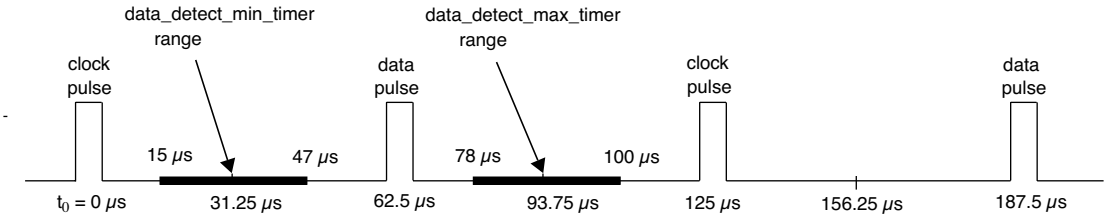


Figure 28–9—FLP data detect timers (data_detect_min/max_timers)

FLP Bursts conforming to the nlp_test_min_timer and nlp_test_max_timer timing as shown in Figure 28–10 shall be considered to have valid separation.

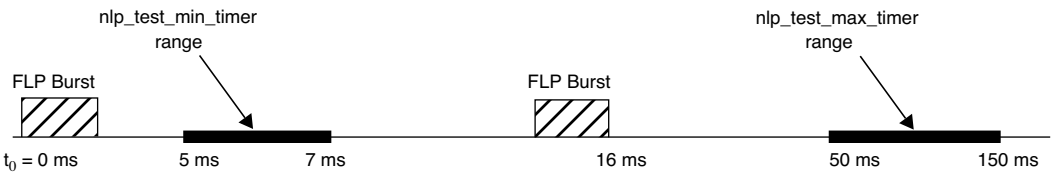
28.2.2.2 NLP detection

NLP detection is accomplished via the NLP Receive Link Integrity Test function in Figure 28–17. The NLP Receive Link Integrity Test function is a modification of the original 10BASE-T Link Integrity Test function (Figure 14–6), where the detection of receive activity will not cause a transition to the LINK TEST

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NOTE—The reference for the starting of the nlp_test_min_timer is from the beginning of the FLP Burst, as shown by t_0, while the reference for the starting of the nlp_test_max_timer is from the expiration of the nlp_test_min_timer.

Figure 28–10—FLP Burst timer (nlp_test_min/max_timers)

PASS state during Auto-Negotiation. The NLP Receive Link Integrity Test function also incorporates the Technology-Dependent Interface requirements.

28.2.2.3 Receive Switch function

The Receive Switch function shall enable the receive path from the MDI to a single technology-dependent PMA once a highest common denominator choice has been made and Auto-Negotiation has completed.

During Auto-Negotiation, the Receive Switch function shall connect both the FLP Burst receiver controlled by the Receive state diagram, Figure 28–15, and the NLP Receive Link Integrity Test state diagram, Figure 28–17, to the MDI. During Auto-Negotiation, the Receive Switch function shall also connect the 100BASE-TX and 100BASE-T4 PMA receivers to the MDI if the 100BASE-TX and/or 100BASE-T4 PMAs are present.

When a PMA is connected to the MDI through the Receive Switch function, the signals at the PMA shall conform to all of the PHY's specifications.

28.2.2.4 Link Code Word matching

The Receive function shall generate ability_match, acknowledge_match, and consistency_match variables as defined in 28.3.1.

28.2.3 Arbitration function requirements

The Arbitration function ensures proper sequencing of the Auto-Negotiation function using the Transmit function and Receive function. The Arbitration function enables the Transmit function to advertise and acknowledge abilities. Upon indication of acknowledgment, the Arbitration function determines the highest common denominator using the priority resolution function and enables the appropriate technology-dependent PMA via the Technology-Dependent Interface (28.2.6).

28.2.3.1 Parallel detection function

The Local Device detects a Link Partner that supports Auto-Negotiation by FLP Burst detection. The Parallel Detection function allows detection of Link Partners that support 100BASE-TX, 100BASE-T4, and/or 10BASE-T, but do not support Auto-Negotiation. Prior to detection of FLP Bursts, the Receive Switch shall direct MDI receive activity to the NLP Receive Link Integrity Test state diagram, 100BASE-TX and 100BASE-T4 PMAs, if present, but shall not direct MDI receive activity to the 10BASE-T or any other PMA. If at least one of the 100BASE-TX, 100BASE-T4, or NLP Receive Link Integrity Test functions establishes link_status=READY, the LINK STATUS CHECK state is entered and the autoneg_wait_timer is started. If exactly one link_status=READY indication is present when the autoneg_wait_timer expires, then Auto-Negotiation shall set link_control=ENABLE for the PMA indicating link_status=READY. If a PMA is enabled, the Arbitration function shall set link_control=DISABLE to all other PMAs and indicate that

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Auto-Negotiation has completed. On transition to the FLP LINK GOOD CHECK state from the LINK STATUS CHECK state the Parallel Detection function shall set the bit in the link partner ability register (Register 5) corresponding to the technology detected by the Parallel Detection function.

NOTE 1—Native 10BASE-T devices will be detected by the NLP Receive Link Integrity Test function, an integrated part of the Auto-Negotiation function. Hence, Parallel Detection for the 10BASE-T PMA is not required or allowed.

NOTE 2—When selecting the highest common denominator through the Parallel Detection function, only the half-duplex mode corresponding to the selected PMA may automatically be detected.

28.2.3.2 Renegotiation function

A renegotiation request from any entity, such as a management agent, shall cause the Arbitration function to disable all technology-dependent PMAs and halt any transmit data and link pulse activity until the break_link_timer expires (28.3.2). Consequently, the Link Partner will go into link fail and normal Auto-Negotiation resumes. The Local Device shall resume Auto-Negotiation after the break_link_timer has expired by issuing FLP Bursts with the base page valid in tx_link_code_word[16:1].

Once Auto-Negotiation has completed, renegotiation will take place if the Highest Common Denominator technology that receives link_control=ENABLE returns link_status=FAIL. To allow the PMA an opportunity to determine link integrity using its own link integrity test function, the link_fail_inhibit_timer qualifies the link_status=FAIL indication such that renegotiation takes place if the link_fail_inhibit_timer has expired and the PMA still indicates link_status=FAIL or link_status=READY.

28.2.3.3 Priority Resolution function

Since a Local Device and a Link Partner may have multiple common abilities, a mechanism to resolve which mode to configure is required. The mechanism used by Auto-Negotiation is a Priority Resolution function that predefines the hierarchy of supported technologies. The single PMA enabled to connect to the MDI by Auto-Negotiation shall be the technology corresponding to the bit in the Technology Ability Field common to the Local Device and Link Partner that has the highest priority as defined in Annex 28B. This technology is referred to as the Highest Common Denominator, or HCD, technology. If the Local Device receives a Technology Ability Field with a bit set that is reserved, the Local Device shall ignore that bit for priority resolution. Determination of the HCD technology occurs on entrance to the FLP LINK GOOD CHECK state. In the event that a technology is chosen through the Parallel Detection function, that technology shall be considered the highest common denominator (HCD) technology. In the event that there is no common technology, HCD shall have a value of “NULL,” indicating that no PMA receives link_control=ENABLE, and link_status_[HCD]=FAIL.

28.2.3.4 Next Page function

The Next Page function uses the standard Auto-Negotiation arbitration mechanisms to allow exchange of arbitrary pieces of data. Data is carried by optional Next Pages of information, which follow the transmission and acknowledgment procedures used for the base Link Code Word. Two types of Next Page encodings are defined: Message Pages and Unformatted Pages.

A dual acknowledgment system is used. Acknowledge (Ack) is used to acknowledge receipt of the information; Acknowledge 2 (Ack2) is used to indicate that the receiver is able to act on the information (or perform the task) defined in the message.

Next Page operation is controlled by the same two mandatory control bits, Next Page and Acknowledge, used in the Base Link Code Word. Setting the NP bit in the Base Link Code Word to logic one indicates that the device is Next Page Able. If both a device and its Link Partner are Next Page Able, then Next Page exchange may occur. If one or both devices are not Next Page Able, then Next Page exchange will not occur

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and, after the base Link Code Words have been exchanged, the FLP LINK GOOD CHECK state will be entered. The Toggle bit is used to ensure proper synchronization between the Local Device and the Link Partner.

Next Page exchange occurs after the base Link Code Words have been exchanged. Next Page exchange consists of using the normal Auto-Negotiation arbitration process to send Next Page messages. Two message encodings are defined: Message Pages, which contain predefined 11 bit codes, and Unformatted Pages. Unformatted Pages can be combined to send extended messages. If the Selector Field values do not match, then each series of Unformatted Pages shall be preceded by a Message Page containing a message code that defines how the following Unformatted Pages will be interpreted. If the Selector Field values match, then the convention governing the use of Message Pages shall be as defined by the Selector Field value definition. Any number of Next Pages may be sent in any order; however, it is recommended that the total number of Next Pages sent be kept small to minimize the link startup time.

Next Page transmission ends when both ends of a link segment set their Next Page bits to logic zero, indicating that neither has anything additional to transmit. It is possible for one device to have more pages to transmit than the other device. Once a device has completed transmission of its Next Page information, it shall transmit Message Pages with Null message codes and the NP bit set to logic zero while its Link Partner continues to transmit valid Next Pages. An Auto-Negotiation able device shall recognize reception of Message Pages with Null message codes as the end of its Link Partner's Next Page information.

28.2.3.4.1 Next Page encodings

The Next Page shall use the encoding shown in Figure 28–11 and Figure 28–12 for the NP, Ack, MP, Ack2, and T bits. The 11-bit field D10–D0 shall be encoded as a Message Code Field if the MP bit is logic one and an Unformatted Code Field if MP is set to logic zero.

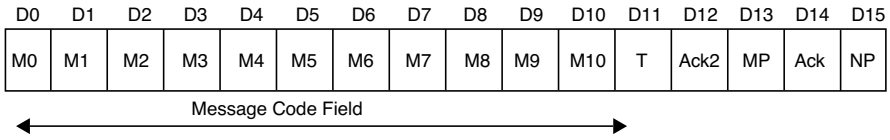


Figure 28–11—Message Page encoding

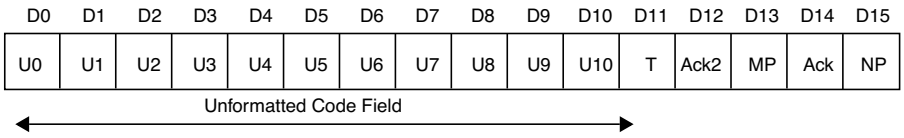


Figure 28–12—Unformatted Page encoding

28.2.3.4.2 Next Page

Next Page (NP) is used by the Next Page function to indicate whether or not this is the last Next Page to be transmitted. NP shall be set as follows:

logic zero = last page.
logic one = additional Next Page(s) will follow.

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28.2.3.4.3 Acknowledge

As defined in 28.2.1.2.4.

28.2.3.4.4 Message Page

Message Page (MP) is used by the Next Page function to differentiate a Message Page from an Unformatted Page. MP shall be set as follows:

logic zero = Unformatted Page.
logic one = Message Page.

28.2.3.4.5 Acknowledge 2

Acknowledge 2 (Ack2) is used by the Next Page function to indicate that a device has the ability to comply with the message. Ack2 shall be set as follows:

logic zero = cannot comply with message.
logic one = will comply with message.

28.2.3.4.6 Toggle

Toggle (T) is used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged Link Code Word. The initial value of the Toggle bit in the first Next Page transmitted is the inverse of bit 11 in the base Link Code Word and, therefore, may assume a value of logic one or zero. The Toggle bit shall be set as follows:

logic zero = previous value of the transmitted Link Code Word equalled logic one.
logic one = previous value of the transmitted Link Code Word equalled logic zero.

28.2.3.4.7 Message Page encoding

Message Pages are formatted pages that carry a single predefined Message Code, which is enumerated in Annex 28C. Two-thousand and forty-eight Message Codes are available. The allocation of these codes will be controlled by the contents of Annex 28C. If the Message Page bit is set to logic one, then the bit encoding of the Link Code Word shall be interpreted as a Message Page.

28.2.3.4.8 Message Code Field

Message Code Field (M[10:0]) is an eleven bit wide field, encoding 2048 possible messages. Message Code Field definitions are shown in Annex 28C. Combinations not specified are reserved for future use. Reserved combinations of the Message Code Field shall not be transmitted.

28.2.3.4.9 Unformatted Page encoding

Unformatted Pages carry the messages indicated by Message Pages. Five control bits are predefined, the remaining 11 bits may take on an arbitrary value. If the Message Page bit is set to logic zero, then the bit encoding of the Link Code Word shall be interpreted as an Unformatted Page.

28.2.3.4.10 Unformatted Code Field

Unformatted Code Field (U[10:0]) is an eleven bit wide field, which may contain an arbitrary value.

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28.2.3.4.11 Use of Next Pages

a) Both devices must indicate Next Page ability for either to commence exchange of Next Pages.
b) If both devices are Next Page able, then both devices shall send at least one Next Page.
c) Next Page exchange shall continue until neither device on a link has more pages to transmit as indicated by the NP bit. A Message Page with a Null Message Code Field value shall be sent if the device has no other information to transmit.
d) A Message Code can carry either a specific message or information that defines how following Unformatted Page(s) should be interpreted.
e) If a Message Code references Unformatted Pages, the Unformatted Pages shall immediately follow the referencing Message Code in the order specified by the Message Code.
f) Unformatted Page users are responsible for controlling the format and sequencing for their Unformatted Pages.

28.2.3.4.12 MII register requirements

The Next Page Transmit register defined in 28.2.4.1.6 shall hold the Next Page to be sent by Auto-Negotiation. Received Next Pages may be stored in the Auto-Negotiation link partner ability register.

28.2.3.5 Remote fault sensing function

The Remote Fault function may indicate to the Link Partner that a fault condition has occurred using the Remote Fault bit and, optionally, the Next Page function.

Sensing of faults in a device as well as subsequent association of faults with the Remote Fault bit shall be optional. If the Local Device has no mechanism to detect a fault or associate a fault condition with the received Remote Fault bit indication, then it shall transmit the Remote Fault bit with the value contained in the Auto-Negotiation advertisement register bit (4.13).

A Local Device may indicate it has sensed a fault to its Link Partner by setting the Remote Fault bit in the Auto-Negotiation advertisement register and renegotiating.

If the Local Device sets the Remote Fault bit to logic one, it may also use the Next Page function to specify information about the fault that has occurred. Remote Fault Message Page Codes have been specified for this purpose.

The Remote Fault bit shall remain set until after successful negotiation with the base Link Code Word, at which time the Remote Fault bit shall be reset to a logic zero. On receipt of a base Link Code Word with the Remote Fault bit set to logic one, the device shall set the Remote Fault bit in the MII status register (1.4) to logic one if the MII management function is present.

28.2.4 Management function requirements

The management interface is used to communicate Auto-Negotiation information to the management entity. If an MII is physically implemented, then management access is via the MII Management interface. Where no physical embodiment of the MII exists, an equivalent to MII Registers 0, 1, 4, 5, 6, and 7 (Clause 22) are recommended to be provided.

28.2.4.1 Media Independent Interface

The Auto-Negotiation function shall have five dedicated registers:

a) MII control register (Register 0).
b) MII status register (Register 1).

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c) Auto-Negotiation advertisement register (Register 4).
d) Auto-Negotiation link partner ability register (Register 5).
e) Auto-Negotiation expansion register (Register 6).

If the Next Page function is implemented, the Auto-Negotiation next page transmit register (Register 7) shall be implemented.

28.2.4.1.1 MII control register

MII control register (Register 0) provides the mechanism to disable/enable and/or restart Auto-Negotiation. The definition for this register is provided in 28.2.4.1.

The Auto-Negotiation function shall be enabled by setting bit 0.12 to a logic one. If bit 0.12 is set to a logic one, then bits 0.13 and 0.8 shall have no effect on the link configuration, and the Auto-Negotiation process will determine the link configuration. If bit 0.12 is cleared to logic zero, then bits 0.13 and 0.8 will determine the link configuration regardless of the prior state of the link configuration and the Auto-Negotiation process.

A PHY shall return a value of one in bit 0.9 until the Auto-Negotiation process has been initiated. The Auto-Negotiation process shall be initiated by setting bit 0.9 to a logic one. If Auto-Negotiation was completed prior to this bit being set, the process shall be reinitiated. If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, then this bit will have no meaning, and should be written as zero. This bit is self-clearing. The Auto-Negotiation process shall not be affected by clearing this bit to logic zero.

28.2.4.1.2 MII status register

The MII status register (Register 1) includes information about all modes of operations supported by the Local Device's PHY, the status of Auto-Negotiation, and whether the Auto-Negotiation function is supported by the PHY or not. The definition for this register is provided in 28.2.4.2.

When read as a logic one, bit 1.5 indicates that the Auto-Negotiation process has been completed, and that the contents of Registers 4, 5, and 6 are valid. When read as a logic zero, bit 1.5 indicates that the Auto-Negotiation process has not been completed, and that the contents of Registers 4, 5, and 6 are meaningless. A PHY shall return a value of zero in bit 1.5 if Auto-Negotiation is disabled by clearing bit 0.12. A PHY shall also return a value of zero in bit 1.5 if it lacks the ability to perform Auto-Negotiation.

When read as logic one, bit 1.4 indicates that a remote fault condition has been detected. The type of fault as well as the criteria and method of fault detection is PHY specific. The Remote Fault bit shall be implemented with a latching function, such that the occurrence of a remote fault will cause the Remote Fault bit to become set and remain set until it is cleared. The Remote Fault bit shall be cleared each time Register 1 is read via the management interface, and shall also be cleared by a PHY reset.

When read as a one, bit 1.3 indicates that the PHY has the ability to perform Auto-Negotiation. When read as a logic zero, bit 1.3 indicates that the PHY lacks the ability to perform Auto-Negotiation.

28.2.4.1.3 Auto-Negotiation advertisement register (Register 4) (R/W)

This register contains the Advertised Ability of the PHY. (See Table 28–2). The bit definition for the base page is defined in 28.2.1.2. On power-up, before Auto-Negotiation starts, this register shall have the following configuration: The Selector Field (4.4:0) is set to an appropriate code as specified in Annex 28A. The Acknowledge bit (4.14) is set to logic zero. The Technology Ability Field (4.12:5) is set based on the values set in the MII status register (Register 1) (1.15:11) or equivalent. See also Annex 28D.

Only the bits in the Technology Ability Field that represent the technologies supported by the Local Device may be set. Any of the Technology Ability Field bits that may be set can also be cleared by management

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Table 28–2—Advertisement register bit definitions

Bit(s)	Name	Description	R/W
4.15	Next Page	See 28.2.1.2	R/W
4.14	Reserved	Write as zero, ignore on read	RO
4.13	Remote Fault	See 28.2.1.2	R/W
4.12:5	Technology Ability Field	See 28.2.1.2	R/W
4.4:0	Selector Field	See 28.2.1.2	R/W

before a renegotiation. This can be used to enable management to Auto-Negotiate to an alternate common mode.

The management entity may initiate renegotiation with the Link Partner using alternate abilities by setting the Selector Field (4.4:0) and Technology Ability Field (4.12:5) to indicate the preferred mode of operation and setting the Restart Auto-Negotiation bit (0.9) in the control register (Register 0) to logic one.

Any writes to this register prior to completion of Auto-Negotiation as indicated by bit 1.5 should be followed by a renegotiation for the new values to be properly used for Auto-Negotiation. Once Auto-Negotiation has completed, this register value may be examined by software to determine the highest common denominator technology.

28.2.4.1.4 Auto-Negotiation link partner ability register (Register 5) (RO)

All of the bits in the Auto-Negotiation link partner ability register are read only. A write to the Auto-Negotiation link partner ability register shall have no effect.

This register contains the Advertised Ability of the Link Partner's PHY. (See Tables 28–3 and 28–4.) The bit definitions shall be a direct representation of the received Link Code Word (Figure 28–7). Upon successful completion of Auto-Negotiation, status register (Register 1) Auto-Negotiation Complete bit (1.5) shall be set to logic one. If the Next Page function is supported, the Auto-Negotiation link partner ability register may be used to store Link Partner Next Pages.

Table 28–3—Link partner ability register bit definitions (Base Page)

Bit(s)	Name	Description	R/W
5.15	Next Page	See 28.2.1.2	RO
5.14	Acknowledge	See 28.2.1.2	RO
5.13	Remote Fault	See 28.2.1.2	RO
5.12:5	Technology Ability Field	See 28.2.1.2	RO
5.4:0	Selector Field	See 28.2.1.2	RO

The values contained in this register are only guaranteed to be valid once Auto-Negotiation has successfully completed, as indicated by bit 1.5 or, if used with Next Page exchange, after the Page Received bit (6.1) has been set to logic one.

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Table 28–4—Link partner ability register bit definitions (Next Page)

Bit(s)	Name	Description	R/W
5.15	Next Page	See 28.2.3.4	RO
5.14	Acknowledge	See 28.2.3.4	RO
5.13	Message Page	See 28.2.3.4	RO
5.12	Acknowledge 2	See 28.2.3.4	RO
5.11	Toggle	See 28.2.3.4	RO
5.10:0	Message/Unformatted Code Field	See 28.2.3.4	RO

NOTE—If this register is used to store Link Partner Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent Link Partner Next Pages.

28.2.4.1.5 Auto-Negotiation expansion register (Register 6) (RO)

All of the bits in the Auto-Negotiation expansion register are read only; a write to the Auto-Negotiation expansion register shall have no effect. (See Table 28–5.)

Table 28–5—Expansion register bit definitions

Bit(s)	Name	Description	R/W	Default
6.15:5	Reserved	Write as zero, ignore on read	RO	0
6.4	Parallel Detection Fault	1 = A fault has been detected via the Parallel Detection function. 0 = A fault has not been detected via the Parallel Detection function.	RO/ LH	0
6.3	Link Partner Next Page Able	1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able	RO	0
6.2	Next Page Able	1 = Local Device is Next Page able 0 = Local Device is not Next Page able	RO	0
6.1	Page Received	1 = A New Page has been received 0 = A New Page has not been received	RO/ LH	0
6.0	Link Partner Auto-Negotiation Able	1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able	RO	0

Bits 6.15:5 are reserved for future Auto-Negotiation expansion.

The Parallel Detection Fault bit (6.4) shall be set to logic one to indicate that zero or more than one of the NLP Receive Link Integrity Test function, 100BASE-TX, or 100BASE-T4 PMAs have indicated link_status=READY when the autoneg_wait_timer expires. The Parallel Detection Fault bit shall be reset to logic zero on a read of the Auto-Negotiation expansion register (Register 6).

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The Link Partner Next Page Able bit (6.3) shall be set to logic one to indicate that the Link Partner supports the Next Page function. This bit shall be reset to logic zero to indicate that the Link Partner does not support the Next Page function.

The Next Page Able bit (6.2) shall be set to logic one to indicate that the Local Device supports the Next Page function. The Next Page Able bit (6.2) shall be set to logic zero if the Next Page function is not supported.

The Page Received bit (6.1) shall be set to logic one to indicate that a new Link Code Word has been received and stored in the Auto-Negotiation link partner ability register. The Page Received bit shall be reset to logic zero on a read of the Auto-Negotiation expansion register (Register 6).

The Link Partner Auto-Negotiation Able bit (6.0) shall be set to logic one to indicate that the Link Partner is able to participate in the Auto-Negotiation function. This bit shall be reset to logic zero if the Link Partner is not Auto-Negotiation able.

28.2.4.1.6 Auto-Negotiation Next Page transmit register (Register 7) (R/W)

The Auto-Negotiation Next Page Transmit register contains the Next Page Link Code Word to be transmitted when Next Page ability is supported. (See Table 28–6.) The contents are defined in 28.2.3.4. On power-up, this register shall contain the default value of 2001H, which represents a Message Page with the Message Code set to Null Message. This value may be replaced by any valid Next Page Message Code that the device wishes to transmit. Writing to this register shall set mr_next_page_loaded to true.

Table 28–6—Next Page transmit register bit definitions

Bit(s)	Name	Description	R/W
7.15	Next Page	See 28.2.3.4	R/W
7.14	Reserved	Write as 0, ignore on read	RO
7.13	Message Page	See 28.2.3.4	R/W
7.12	Acknowledge 2	See 28.2.3.4	R/W
7.11	Toggle	See 28.2.3.4	RO
7.10:0	Message/Unformatted Code field	See 28.2.3.4	R/W

28.2.4.1.7 Auto-Negotiation Link Partner Ability register (Register 8) (RO)

Support for 100BASE-T2 and 1000BASE-T requires support for Next Page and the provision of an Auto-Negotiation Link Partner Next Page Ability register (register 8) to store Link Partner Next Pages as shown in Table 28–7. All of the bits in the Auto-Negotiation Link Partner Next Page Ability register are read only. A write to the Auto-Negotiation Link Partner Next Page Ability register shall have no effect.

The values contained in this register are only guaranteed to be valid after the Page Received bit (6.1) has been set to logical one or once Auto-Negotiation has successfully completed, as indicated by bit 1.5.

NOTE—If this register is used to store multiple Link Partner Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent Link Partner Next Pages.

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Table 28–7—Link Partner Next Page Ability register bit definitions

Bit(s)	Name	Description	R/W
8.15	Next Page	see 28.2.3.4	RO
8.14	Acknowledge	see 28.2.3.4	RO
8.13	Message Page	see 28.2.3.4	RO
8.12	Acknowledge 2	see 28.2.3.4	RO
8.11	Toggle	see 28.2.3.4	RO
8.10:0	Message/Unformatted Code Field	see 28.2.3.4	RO

28.2.4.1.8 State diagram variable to MII register mapping

The state diagrams of Figures 28–14 to 28–17 generate and accept variables of the form “mr_x,” where x is an individual signal name. These variables comprise a management interface that may be connected to the MII management function or other equivalent function. Table 28–8 describes how the MII registers map to the management function interface signals.

Table 28–8—State diagram variable to MII register mapping

State diagram variable	MII register
mr_adv_ability[16:1]	4.15:0 Auto-Negotiation advertisement register
mr_autoneg_complete	1.5 Auto-Negotiation Complete
mr_autoneg_enable	0.12 Auto-Negotiation Enable
mr_lp_adv_ability[16:1]	5.15:0 Auto-Negotiation link partner ability register
mr_lp_autoneg_able	6.0 Link Partner Auto-Negotiation Able
mr_lp_np_able	6.3 Link Partner Next Page Able
mr_main_reset	0.15 Reset
mr_next_page_loaded	Set on write to Auto-Negotiation Next Page Transmit register; cleared by Arbitration state diagram
mr_np_able	6.2 Next Page Able
mr_np_tx[16:1]	7.15:0 Auto-Negotiation Next Page Transmit Register
mr_page_rx	6.1 Page Received
mr_parallel_detection_fault	6.4 Parallel Detection Fault
mr_restart_negotiation	0.9 Auto-Negotiation Restart
set if Auto-Negotiation is available	1.3 Auto-Negotiation Ability

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28.2.4.2 Auto-Negotiation managed object class

The Auto-Negotiation Managed Object Class is defined in Clause 30.

28.2.5 Absence of management function

In the absence of any management function, the advertised abilities shall be provided through a logical equivalent of mr_adv_ability[16:1]. A device shall comply with all Next Page function requirements, including the provision of the mr_np_able, mr_lp_np_able, and mr_next_page_loaded variables (or their logical equivalents), in order to permit the NP bit to be set to logic one in the transmitted Link Code Word.

NOTE—Storage of a valid base Link Code Word is required to prevent a deadlock situation where negotiation must start again while Next Pages are being transmitted. If a shared transmit register were used, then renegotiation could not occur when Next Pages were being transmitted because the base Link Code Word would not be available. This requirement can be met using a number of different implementations, including use of temporary registers or register stacks.

28.2.6 Technology-Dependent Interface

The Technology-Dependent Interface is the communication mechanism between each technology's PMA and the Auto-Negotiation function. Auto-Negotiation can support multiple technologies, all of which need not be implemented in a given device. Each of these technologies may utilize its own technology-dependent link integrity test function.

28.2.6.1 PMA_LINK.indicate

This primitive is generated by the PMA to indicate the status of the underlying medium. The purpose of this primitive is to give the PCS, repeater client, or Auto-Negotiation function a means of determining the validity of received code elements.

28.2.6.1.1 Semantics of the service primitive

PMA_LINK.indicate(link_status)

The link_status parameter shall assume one of three values: READY, OK, or FAIL, indicating whether the underlying receive channel is intact and ready to be enabled (READY), intact and enabled (OK), or not intact (FAIL). When link_status=FAIL or link_status=READY, the PMA_CARRIER.indicate and PMA_UNITDATA.indicate primitives are undefined.

28.2.6.1.2 When generated

A technology-dependent PMA and the NLP Receive Link Integrity Test state diagram (Figure 28–17) shall generate this primitive to indicate the value of link_status.

28.2.6.1.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the state diagrams of Figure 28–16.

28.2.6.2 PMA_LINK.request

This primitive is generated by Auto-Negotiation to allow it to enable and disable operation of the PMA.

28.2.6.2.1 Semantics of the service primitive

PMA_LINK.request(link_control)

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The link_control parameter shall assume one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

The link_control=SCAN_FOR_CARRIER mode is used by the Auto-Negotiation function prior to receiving any FLP Bursts or link_status=READY indications. During this mode, the PMA shall search for carrier and report link_status=READY when carrier is received, but no other actions shall be enabled.

The link_control=DISABLE mode shall be used by the Auto-Negotiation function to disable PMA processing.

The link_control=ENABLE mode shall be used by Auto-Negotiation to turn control over to a single PMA for all normal processing functions.

28.2.6.2.2 When generated

The Auto-Negotiation function shall generate this primitive to indicate to the PHY how to respond, in accordance with the state diagrams of Figure 28–15 and Figure 28–16.

Upon power-on or reset, if the Auto-Negotiation function is enabled (mr_autoneg_enable=true) the PMA_LINK.request(DISABLE) message shall be issued to all technology-dependent PMAs. If Auto-Negotiation is disabled at any time including at power-on or reset, the state of PMA_LINK.request(link_control) is implementation dependent.

28.2.6.2.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the NLP Receive Link Integrity Test state diagram (Figure 28–17) and the receiving technology-dependent link integrity test function, based on the intent specified in the primitive semantics.

28.2.6.3 PMA_LINKPULSE.request

This primitive is generated by Auto-Negotiation to indicate that a valid Link Pulse, as transmitted in compliance with Figure 14–12, has been received.

28.2.6.3.1 Semantics of the service primitive

PMA_LINKPULSE.request (linkpulse)

The linkpulse parameter shall assume one of two values: TRUE or FALSE.

The linkpulse=FALSE mode shall be used by the Auto-Negotiation function to indicate that the Receive State Diagram has performed a state transition.

The linkpulse=TRUE mode shall be used by the Auto-Negotiation function to indicate that a valid Link Pulse has been received.

28.2.6.3.2 When generated

The Auto-Negotiation function shall generate this primitive to indicate to the PHY how to respond, in accordance with the state diagram of Figure 28–15.

Upon power-on or reset, if the Auto-Negotiation function is enabled (mr_autoneg_enable=true) the PMA_LINKPULSE.request (FALSE) message shall be issued to all technology-dependent PMAs. If Auto-

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Negotiation is disabled at any time including at power-on or reset, the state of PMA_LINKPULSE.request (linkpulse) is implementation dependent.

28.2.6.3.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the receiving technology-dependent PMA function, based on the intent specified in the primitive semantics.

28.3 State diagrams and variable definitions

The notation used in the state diagrams (Figures 28–14 to 28–17) follows the conventions in 21.5. State diagram variables follow the conventions of 21.5.2 except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set. Variables using the "mr_x" notation do not have state diagram defaults; however, their appropriate initialization conditions when mapped to the MII interface are covered in 28.2.4 and 22.2.4. The variables, timers, and counters used in the state diagrams are defined in 28.3, 14.2.3, and 28.2.6.

Auto-Negotiation shall implement the Transmit state diagram, Receive state diagram, Arbitration state diagram, and NLP Receive Link Integrity Test state diagram as depicted in 28.3. Additional requirements to these state diagrams are made in the respective functional requirements sections. Options to these state diagrams clearly stated as such in the functional requirements sections or state diagrams shall be allowed. In the case of any ambiguity between stated requirements and the state diagrams, the state diagrams shall take precedence.

The functional reference diagram (Figure 28–13) provides a generic example, illustrated with initial PMA implementations and showing the mechanism for expansion. New PMAs are documented in Annex 28D.

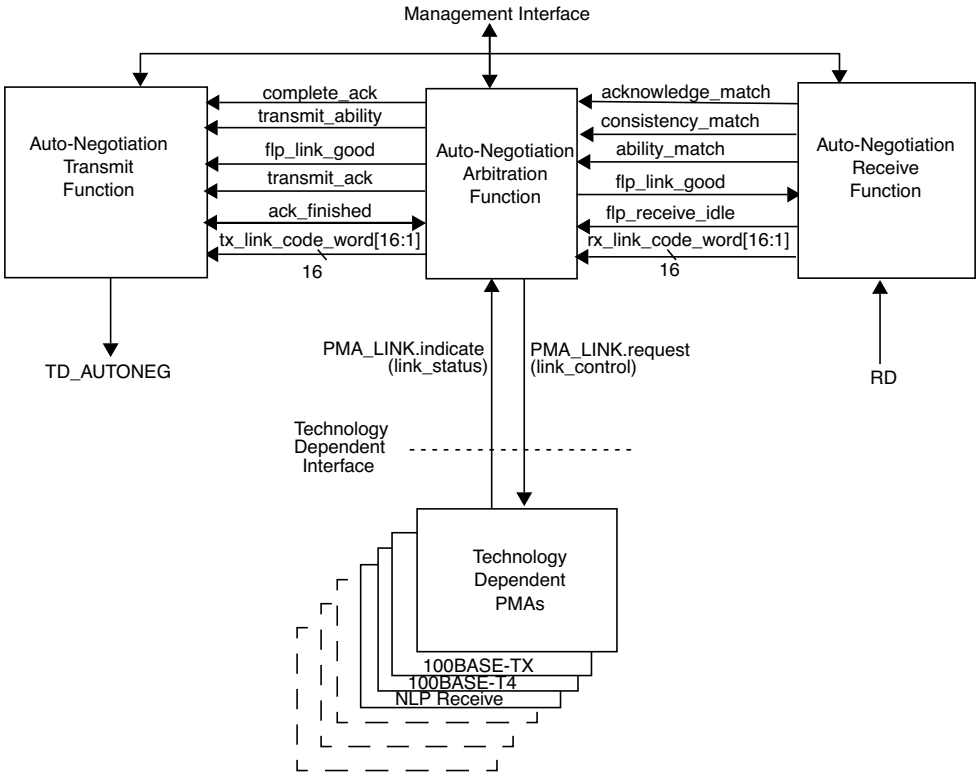


Figure 28–13—Functional reference diagram

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28.3.1 State diagram variables

A variable with "_[x]" appended to the end of the variable name indicates a variable or set of variables as defined by "x". "x" may be as follows:

all;	represents all specific technology-dependent PMAs supported in the Local Device and the NLP Receive Link Integrity Test state diagram.
1GigT;	represents that the 1000BASE-T PMA is the signal source.
HCD;	represents the single technology-dependent PMA chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or Parallel Detection function. To select 10BASE-T, LIT is used instead of NLP to enable the full 10BASE-T Link Integrity Test function state diagram.
notHCD;	represents all technology-dependent PMAs not chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or Parallel Detection function.
TX;	represents that the 100BASE-TX PMA is the signal source.
T4;	represents that the 100BASE-T4 PMA is the signal source.
NLP;	represents that the NLP Receive Link Integrity Test function is the signal source.
PD;	represents all of the following that are present: 100BASE-TX PMA, 100BASE-T4 PMA, and the NLP Receive Link Integrity Test state diagram.
LIT;	represents the 10BASE-T Link Integrity Test function state diagram is the signal source or destination.

Variables with [16:1] appended to the end of the variable name indicate arrays that can be directly mapped to 16-bit registers. For these variables, "[x]" indexes an element or set of elements in the array, where "[x]" may be as follows:

— Any integer.
— Any variable that takes on integer values.
— NP; represents the index of the Next Page bit.
— ACK; represents the index of the Acknowledge bit.
— RF; represents the index of the Remote Fault bit.

Variables of the form "mr_x", where x is a label, comprise a management interface that is intended to be connected to the MII Management function. However, an implementation-specific management interface may provide the control and status function of these bits.

ability_match

Indicates that three consecutive Link Code Words match, ignoring the Acknowledge bit. Three consecutive words are any three words received one after the other, regardless of whether the word has already been used in a word-match comparison or not.

Values: false; three matching consecutive Link Code Words have not been received, ignoring the Acknowledge bit (default).
true; three matching consecutive Link Code Words have been received, ignoring the Acknowledge bit.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

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ability_match_word [16:1]

A 16-bit array that contains the last Link Code Word that caused ability_match = true. For each element in the array:

Values: zero; data bit is logicial zero.
one; data bit is logical one.

ack_finished

Status indicating that the final remaining_ack_cnt Link Code Words with the Ack bit set have been transmitted.

Values: false; more Link Code Words with the Ack bit set to logic one must be transmitted.
true; all remaining Link Code Words with the Ack bit set to logic one have been transmitted.

acknowledge_match

Indicates that three consecutive Link Code Words match and have the Acknowledge bit set. Three consecutive words are any three words received one after the other, regardless of whether the word has already been used in a word match comparison or not.

Values: false; three matching and consecutive Link Code Words have not been received with the Acknowledge bit set (default).
true; three matching and consecutive Link Code Words have been received with the Acknowledge bit set.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

base_page

Status indicating that the page currently being transmitted by Auto-Negotiation is the initial Link Code Word encoding used to communicate the device's abilities.

Values: false; a page other than base Link Code Word is being transmitted.
true; the base Link Code Word is being transmitted.

complete_ack

Controls the counting of transmitted Link Code Words that have their Acknowledge bit set.

Values: false; transmitted Link Code Words with the Acknowledge bit set are not counted (default).
true; transmitted Link Code Words with the Acknowledge bit set are counted.

consistency_match

Indicates that the Link Code Word that caused ability_match to be set is the same as the Link Code Word that caused acknowledge_match to be set.

Values: false; the Link Code Word that caused ability_match to be set is not the same as the Link Code Word that caused acknowledge_match to be set, ignoring the Acknowledge bit value.
true; the Link Code Word that caused ability_match to be set is the same as the Link Code Word that caused acknowledge_match to be set, independent of the Acknowledge bit value.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

desire_np

Status indicating that the Local Device desires to engage in Next Page exchange. This information comes from the setting of the NP bit in the base Link Code Word stored in the Auto-Negotiation advertisement register (Register 4).

Values: false; Next Page exchange is not desired.
true; Next Page exchange is desired.

flp_link_good

Indicates that Auto-Negotiation has completed.

Values: false; negotiation is in progress (default).

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true; negotiation is complete, forcing the Transmit and Receive functions to IDLE.

flp_receive_idle
Indicates that the Receive state diagram is in the IDLE, LINK PULSE DETECT, or LINK PULSE COUNT state.

Values: false; the Receive state diagram is not in the IDLE, LINK PULSE DETECT, or LINK PULSE COUNT state (default).
true; the Receive state diagram is in the IDLE, LINK PULSE DETECT, or LINK PULSE COUNT state.

incompatible_link
Parameter used following Priority Resolution to indicate the resolved link is incompatible with the Local Device settings. A device's ability to set this variable to true is optional.

Values: false; A compatible link exists between the Local Device and Link Partner (default).
true; Optional indication that Priority Resolution has determined no highest common denominator exists following the most recent negotiation.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

link_control
This variable is defined in 28.2.6.2.1.

link_status
This variable is defined in 28.2.6.1.1.

linkpulse
This variable is defined in 28.2.6.3.1.

Values: false; linkpulse is set to false after any Receive State Diagram state transition (default).
true; linkpulse is set to true when a valid Link Pulse is received.

mr_autoneg_complete
Status indicating whether Auto-Negotiation has completed or not.

Values: false; Auto-Negotiation has not completed.
true; Auto-Negotiation has completed.

mr_autoneg_enable
Controls the enabling and disabling of the Auto-Negotiation function.

Values: false; Auto-Negotiation is disabled.
true; Auto-Negotiation is enabled.

mr_adv_ability[16:1]
A 16-bit array that contains the Advertised Abilities Link Code Word.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_lp_adv_ability[16:1]
A 16-bit array that contains the Link Partner's Advertised Abilities Link Code Word.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_lp_np_able
Status indicating whether the Link Partner supports Next Page exchange.

Values: false; the Link Partner does not support Next Page exchange.
true; the Link Partner supports Next Page exchange.

mr_np_able
Status indicating whether the Local Device supports Next Page exchange.

Values: false; the Local Device does not support Next Page exchange.

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true; the Local Device supports Next Page exchange.

mr_lp_autoneg_able
Status indicating whether the Link Partner supports Auto-Negotiation.

Values: false; the Link Partner does not support Auto-Negotiation.
true; the Link Partner supports Auto-Negotiation.

mr_main_reset
Controls the resetting of the Auto-Negotiation state diagrams.

Values: false; do not reset the Auto-Negotiation state diagrams.
true; reset the Auto-Negotiation state diagrams.

mr_next_page_loaded
Status indicating whether a new page has been loaded into the Auto-Negotiation Next Page Transmit register (Register 7).

Values: false; a New Page has not been loaded.
true; a New Page has been loaded.

mr_np_tx[16:1]
A 16-bit array that contains the new Next Page to transmit.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_page_rx
Status indicating whether a New Page has been received. A New Page has been successfully received when acknowledge_match=true and consistency_match=true and the Link Code Word has been written to mr_lp_adv_ability[16:1].

Values: false; a New Page has not been received.
true; a New Page has been received.

mr_parallel_detection_fault
Error condition indicating that while performing Parallel Detection, either flp_receive_idle = false, or zero or more than one of the following indications were present when the autoneg_wait_timer expired. This signal is cleared on read of the Auto-Negotiaion expansion register.

1) link_status_ [NLP] = READY
2) link_status_[TX] = READY
3) link_status_[T4] = READY

Values: false; Exactly one of the above three indications was true when the autoneg_wait_timer expired, and flp_receive_idle = true.
true; either zero or more than one of the above three indications was true when the autoneg_wait_timer expired, or flp_receive_idle = false.

mr_restart_negotiation
Controls the entrance to the TRANSMIT DISABLE state to break the link before Auto-Negotiation is allowed to renegotiate via management control.

Values: false; renegotiation is not taking place.
true; renegotiation is started.

np_rx
Flag to hold the value of rx_link_code_word[NP] upon entry to the COMPLETE ACKNOWLEDGE state. This value is associated with the value of rx_link_code_word[NP] when acknowledge_match was last set.

Values zero; local device np_rx bit equals a logical zero.
one; local device np_rx bit equals a logical one.

power_on
Condition that is true until such time as the power supply for the device that contains the Auto-

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Negotiation state diagrams has reached the operating region or the device has low power mode set via MII control register bit 0.11.

Values: false; the device is completely powered (default).
true; the device has not been completely powered.

rx_link_code_word[16:1]

A 16-bit array that contains the data bits to be received from an FLP Burst.
For each element within the array:

Values: zero; data bit is a logical zero.
one; data bit is a logical one.

single_link_ready

Status indicating that flp_receive_idle = true and only one the of the following indications is being received:

1) link_status_[NLP] = READY
2) link_status_[TX] = READY
3) link_status_[T4] = READY

Values: false; either zero or more than one of the above three indications are true or flp_receive_idle = false.
true; Exactly one of the above three indications is true and flp_receive_idle = true.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

TD_AUTONEG

Controls the signal sent by Auto-Negotiation on the TD_AUTONEG circuit.

Values: idle; Auto-Negotiation prevents transmission of all link pulses on the MDI.
link_test_pulse; Auto-Negotiation causes a single link pulse as defined by Figure 14–12 to be transmitted on the MDI.

toggle_rx

Flag to keep track of the state of the Link Partner's Toggle bit.

Values: 0; Link Partner's Toggle bit equals logic zero.
1; Link Partner's Toggle bit equals logic one.

toggle_tx

Flag to keep track of the state of the Local Device's Toggle bit.

Values: 0; Local Device's Toggle bit equals logic zero.
1; Local Device's Toggle bit equals logic one.

transmit_ability

Controls the transmission of the Link Code Word containing tx_link_code_word[16:1].

Values: false; any transmission of tx_link_code_word[16:1] is halted (default).
true; the transmit state diagram begins sending tx_link_code_word[16:1].

transmit_ack

Controls the setting of the Acknowledge bit in the tx_link_code_word[16:1] to be transmitted.

Values: false; sets the Acknowledge bit in the transmitted tx_link_code_word[16:1] to a logic zero (default).
true; sets the Acknowledge bit in the transmitted tx_link_code_word[16:1] to a logic one.

transmit_disable

Controls the transmission of tx_link_code_word[16:1].

Values: false; tx_link_code_word[16:1] transmission is allowed (default).
true; tx_link_code_word[16:1] transmission is halted.

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tx_link_code_word[16:1]
: A 16-bit array that contains the data bits to be transmitted in an FLP Burst. This array may be loaded from mr_adv_ability or mr_np_tx.
For each element within the array:

Values: Zero; data bit is logical zero.
One; data bit is logical one.

28.3.2 State diagram timers

All timers operate in the manner described in 14.2.3.2.

autoneg_wait_timer
: Timer for the amount of time to wait before evaluating the number of link integrity test functions with link_status=READY asserted. The autoneg_wait_timer shall expire 500–1000 ms from the assertion of link_status=READY from the 100BASE-TX PMA, 100BASE-T4 PMA, or the NLP Receive State diagram.

break_link_timer
: Timer for the amount of time to wait in order to assure that the Link Partner enters a Link Fail state. The timer shall expire 1200–1500 ms after being started.

data_detect_max_timer
: Timer for the maximum time between a clock pulse and the next link pulse. This timer is used in conjunction with the data_detect_min_timer to detect whether the data bit between two clock pulses is a logic zero or a logic one. The data_detect_max_timer shall expire 78–100 μs from the last clock pulse.

data_detect_min_timer
: Timer for the minimum time between a clock pulse and the next link pulse. This timer is used in conjunction with the data_detect_max_timer to detect whether the data bit between two clock pulses is a logic zero or a logic one. The data_detect_min_timer shall expire 15–47 μs from the last clock pulse.

flp_test_max_timer
: Timer for the maximum time between two link pulses within an FLP Burst. This timer is used in conjunction with the flp_test_min_timer to detect whether the Link Partner is transmitting FLP Bursts. The flp_test_max_timer shall expire 165–185 μs from the last link pulse.

flp_test_min_timer
: Timer for the minimum time between two link pulses within an FLP Burst. This timer is used in conjunction with the flp_test_max_timer to detect whether the Link Partner is transmitting FLP Bursts. The flp_test_min_timer shall expire 5–25 μs from the last link pulse.

interval_timer
: Timer for the separation of a transmitted clock pulse from a data bit. The interval_timer shall expire 55.5–-69.5 μs from each clock pulse and data bit.

link_fail_inhibit_timer
: Timer for qualifying a link_status=FAIL indication or a link_status=READY indication when a specific technology link is first being established. A link will only be considered “failed” if the link_fail_inhibit_timer has expired and the link has still not gone into the link_status=OK state. The link_fail_inhibit_timer shall expire 750–1000 ms after entering the FLP LINK GOOD CHECK state.

NOTE—The link_fail_inhibit_timer expiration value must be greater than the time required for the Link Partner to complete Auto-Negotiation after the Local Device has completed Auto-Negotiation plus the time required for the specific technology to enter the link_status=OK state. The maximum time difference between a Local Device and its Link Partner completing Auto-Negotiation is

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(Maximum FLP Burst to FLP Burst separation) × (Maximum number of FLP Bursts needed to complete acknowledgment) = (24 ms) × (8 bursts) = 192 ms.

For example, 100BASE-T4 requires approximately 460 ms to enter link_status=OK for a total minimum link_fail_inhibit_timer time of 652 ms. The lower bound for the link_fail_inhibit_timer was chosen to provide adequate margin for the current technologies and any future PMAs.

nlp_test_max_timer
: Timer for the maximum time that no FLP Burst may be seen before forcing the receive state diagram to the IDLE state. The nlp_test_max_timer shall expire 50–150 ms after being started or restarted.

nlp_test_min_timer
: Timer for the minimum time between two consecutive FLP Bursts. The nlp_test_min_timer shall expire 5–7 ms after being started or restarted.

transmit_link_burst_timer
: Timer for the separation of a transmitted FLP Burst from the next FLP Burst. The transmit_link_burst_timer shall expire 5.7-22.3 ms after the last transmitted link pulse in an FLP Burst.

Table 28–9—Timer min./max. value summary

Parameter	Min.	Typ.	Max.	Units
autoneg_wait_timer	500		1000	ms
break_link_timer	1200		1500	ms
data_detect_min_timer	15		47	μs
data_detect_max_timer	78		100	μs
flp_test_min_timer	5		25	μs
flp_test_max_timer	165		185	μs
interval_timer	55.5	62.5	69.5	μs
link_fail_inhibit_timer	750		1000	ms
nlp_test_max_timer	50		150	ms
nlp_test_min_timer	5		7	ms
transmit_link_burst_timer	5.7	14	22.3	ms

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28.3.3 State diagram counters

flp_cnt

A counter that may take on integer values from 0 to 17. This counter is used to keep a count of the number of FLPs detected to enable the determination of whether the Link Partner supports Auto-Negotiation.

Values: not_done; 0 to 5 inclusive.
done; 6 to 17 inclusive.
init; counter is reset to zero.

remaining_ack_cnt

A counter that may take on integer values from 0 to 8. The number of additional Link Code Words with the Acknowledge Bit set to logic one to be sent to ensure that the Link Partner receives the acknowledgment.

Values: not_done; positive integers between 0 and 5 inclusive.
done; positive integers 6 to 8 inclusive (default).
init; counter is reset to zero.

rx_bit_cnt

A counter that may take on integer values from 0 to 17. This counter is used to keep a count of data bits received from an FLP Burst and to ensure that when erroneous extra pulses are received, the first 16 bits are kept while the rest are ignored. When this variable reaches 16 or 17, enough data bits have been received. This counter does not increment beyond 17 and does not return to 0 until it is reinitialized.

Values: not_done; 1 to 15 inclusive.
done; 16 or 17
init; counter is reset to zero.
rx_bit_cnt_check; 10 to 17 inclusive.

tx_bit_cnt

A counter that may take on integer values from 1 to 17. This counter is used to keep a count of data bits sent within an FLP Burst. When this variable reaches 17, all data bits have been sent.

Values: not_done; 1 to 16 inclusive.
done; 17.
init; counter is initialized to 1.

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28.3.4 State diagrams

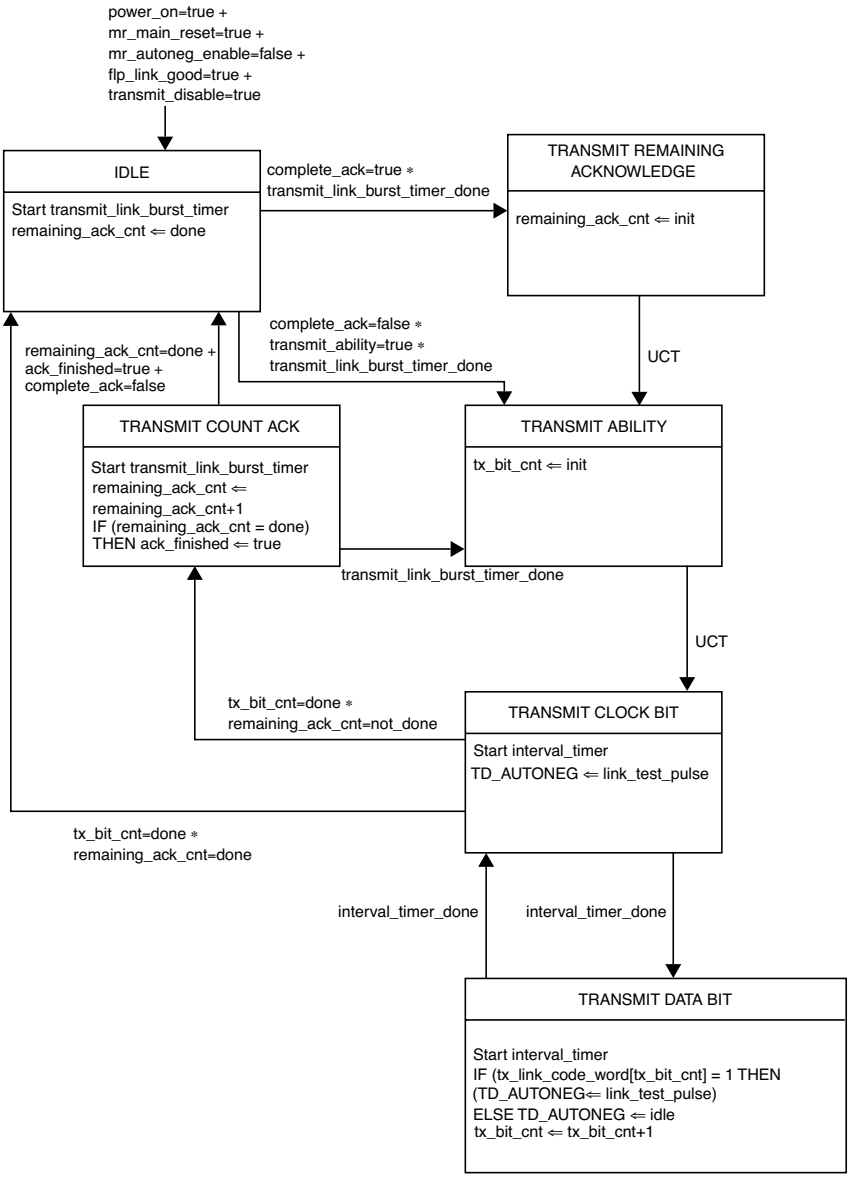


Figure 28–14—Transmit state diagram

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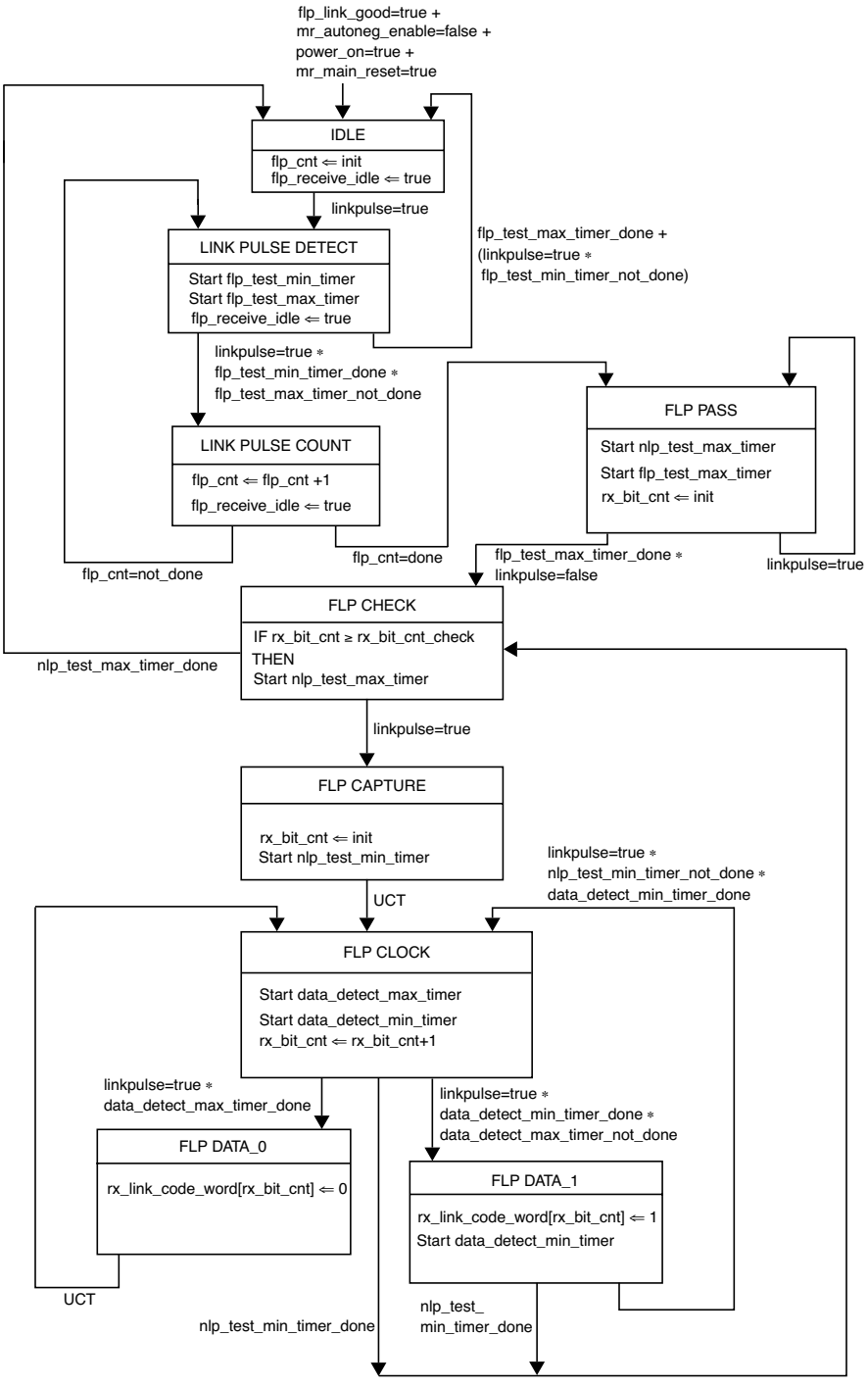
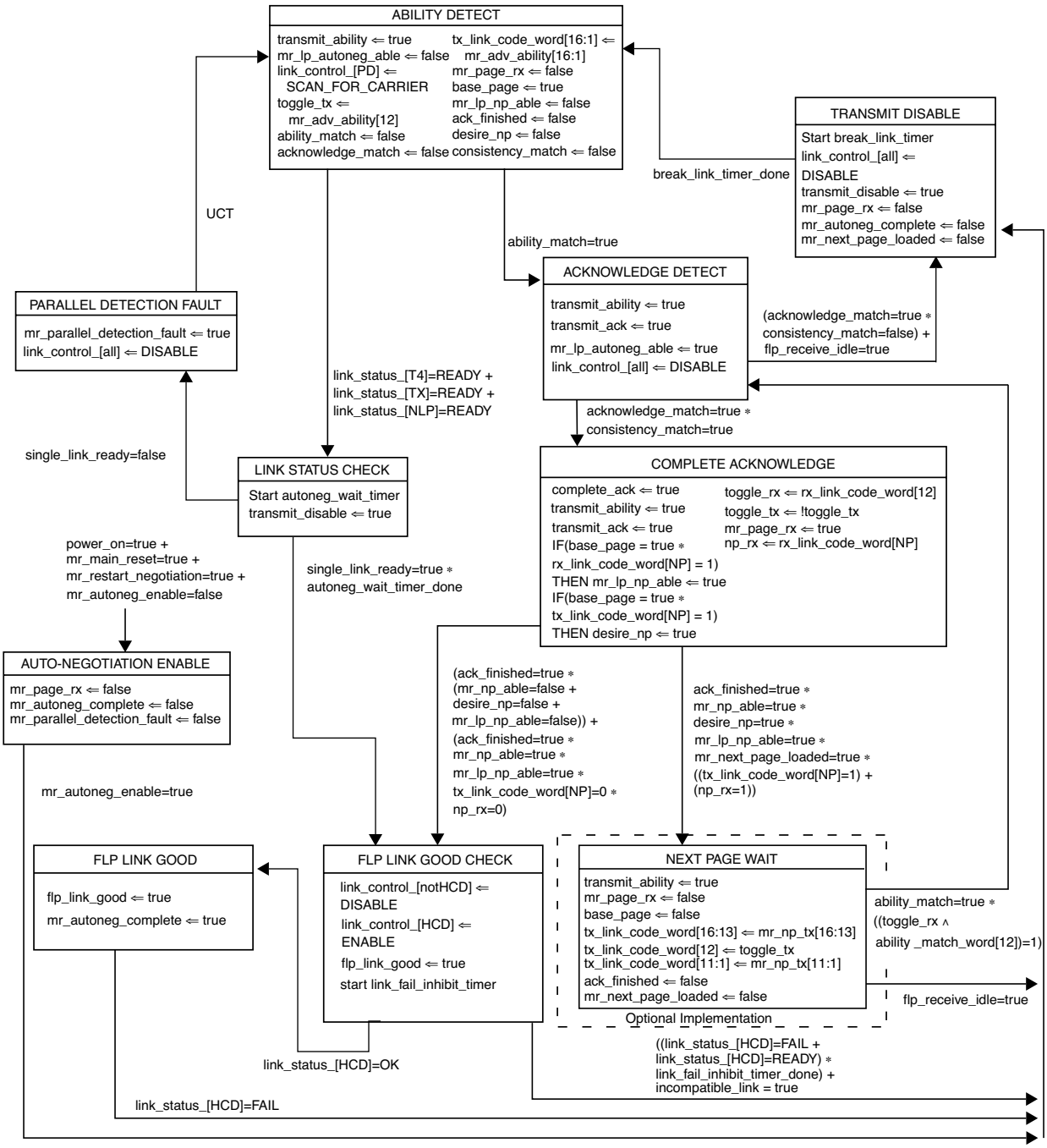


Figure 28–15—Receive state diagram

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NOTE—The transition from COMPLETE ACKNOWLEDGE to FLP LINK GOOD CHECK can be simplified to "ack_finished=true" if the optional Next Page function is not supported.

NOTE—ability_match, acknowledge_match, single_link_ready, consistency_match, and incompatible_link are set according to the variable definitions and are not set explicitly in the state diagrams.

Figure 28–16—Arbitration state diagram

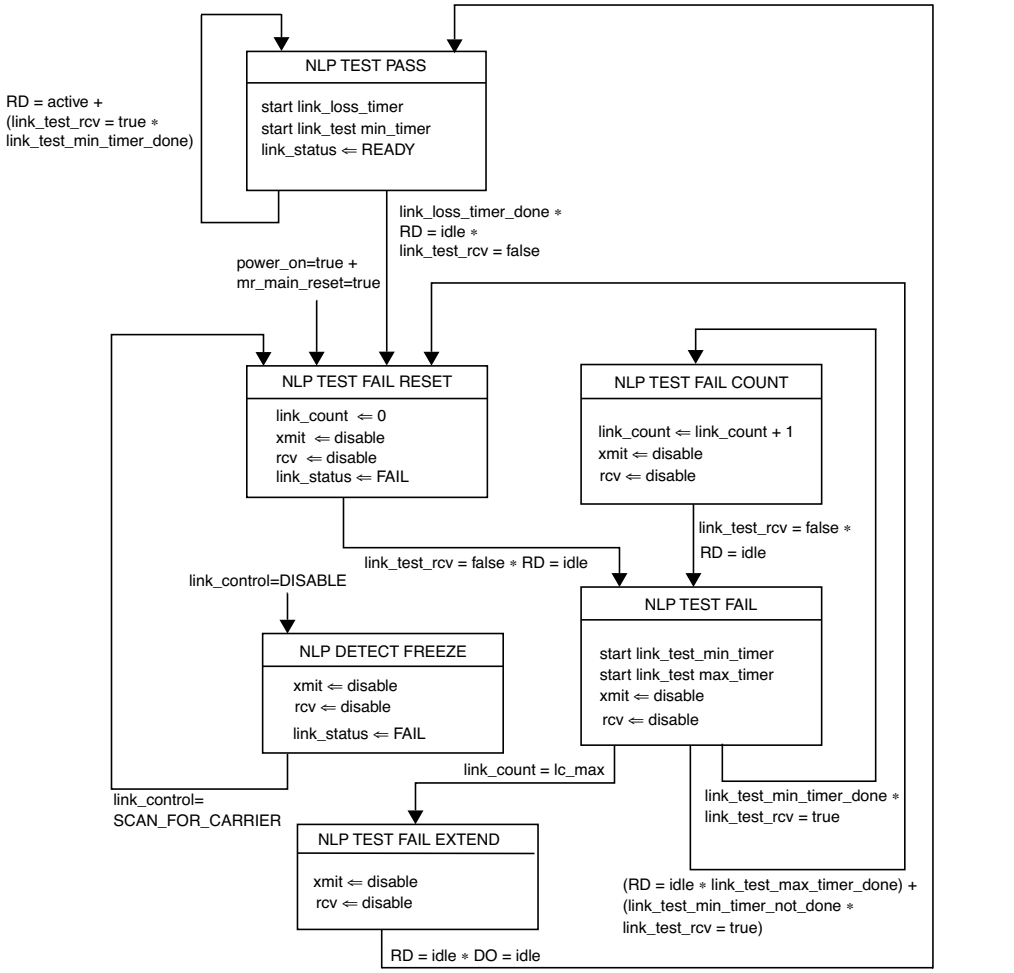
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NOTE—The variables link_control and link_status are viewed as dedicated signals by the NLP Receive Link integrity Test state diagram, but are viewed as link_control_[NLP] and link_status_[NLP] by the Auto-Negotiation Arbitration state diagram, Figure 28–16.

Figure 28–17—NLP Receive Link Integrity Test state diagram

28.4 Electrical specifications

The electrical characteristics of pulses within FLP Bursts shall be identical to the characteristics of NLPs and shall meet the requirements of Figure 14–12.

It is the responsibility of the technology-specific Transmit and Receive functions to interface to the MDI correctly.

NOTE—The requirements relative to the interface to the MDI are specified via the Transmit Switch and Receive Switch functions.

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28.5 Protocol Implementation Conformance Statement (PICS) proforma for Clause 28, Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Auto-Negotiation on twisted pair[11]

28.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 28, Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Auto-Negotiation on twisted pair, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

28.5.2 Identification

28.5.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

28.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2002, Clause 28, Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Auto-Negotiation on twisted pair
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required?No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

[11] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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28.5.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/comment
10BT	Implementation supports a 10BASE-T data service	28.1.2	O		N/A
*NP	Implementation supports Next Page function	28.1.2	O		N/A
*MII	Implementation supports the MII Management Interface	28.1.2	O/1		N/A
MGMT	Implementation supports a non-MII Management Interface	28.1.2	O/1		N/A
*NOM	Implementation does not support management	28.1.2	O/1		N/A
*RF	Implementation supports Remote Fault Sensing	28.2.3.5	O		N/A

28.5.4 PICS proforma tables for Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Auto-Negotiation on twisted pair

28.5.4.1 Scope

Item	Feature	Subclause	Status	Support	Value/comment
1	MII Management Interface control and status registers	28.1.3	MII:M		Implemented in accordance with the definitions in Clause 22 and 28.2.4
2	CSMA/CD compatible devices using an eight-pin modular connector and using a signaling method to automatically configure the preferred mode of operation	28.1.4	M		Auto-Negotiation function implemented in compliance with Clause 28
3	Device uses 10BASE-T compatible link signaling to advertise non-CSMA/CD abilities	28.1.4	M		Auto-Negotiation function implemented in compliance with Clause 28
4	Future CSMA/CD implementations that use an eight-pin modular connector	28.1.4	M		Interoperable with devices compliant with Clause 28

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28.5.4.2 Auto-Negotiation functions

Item	Feature	Subclause	Status	Support	Value/comment
1	Transmit	28.2	M		Complies with Figure 28–14
2	Receive	28.2	M		Complies with Figure 28–15
3	Arbitration	28.2	M		Complies with Figure 28–16
4	NLP Receive Link Integrity Test	28.2	M		Complies with Figure 28–17
5	Technology-Dependent Interface	28.2	M		Complies with 28.2.6
6	Technology-dependent link integrity test	28.2	M		Implemented and interfaced to for those technologies supported by device
7	Management	28.2	O		MII based or alternate management

28.5.4.3 Transmit function requirements

Item	Feature	Subclause	Status	Support	Value/comment
1	FLP Burst transmission	28.2.1.1	M		Not transmitted once Auto-Negotiation is complete and highest common denominator PMA has been enabled. Prohibited other than for link start-up
2	FLP Burst composition	28.2.1.1.1	M		Pulses in FLP Bursts meet the requirements of Figure 14–12
3	FLP Burst pulse definition	28.2.1.1.1	M		17 odd-numbered pulse positions represent clock information; 16 even-numbered pulse positions represent data information
4	The first pulse in an FLP Burst	28.2.1.1.2	M		Defined as a clock pulse for timing purposes
5	FLP Burst clock pulse spacing	28.2.1.1.2	M		Within an FLP Burst, spacing is 125 ± 14 μs
6	Logic one data bit representation	28.2.1.1.2	M		Pulse transmitted 62.5 ± 7 µs after the preceding clock pulse
7	Logic zero data bit representation	28.2.1.1.2	M		No link integrity test pulses within 111 μs of the preceding clock pulse
8	Consecutive FLP Bursts	28.2.1.1.2	M		The first link pulse in each FLP Burst is separated by 16 ± 8 ms
9	FLP Burst base page	28.2.1.2	M		Conforms to Figure 28–7
10	FLP Burst bit transmission order	28.2.1.2	M		Transmission is D0 first to D15 last

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28.5.4.3 Transmit function requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
11	Selector Field values	28.2.1.2.1	M		Only defined values transmitted
12	Technology Ability Field values	28.2.1.2.2	M		Implementation supports a data service for each ability set in the Technology Ability Field
13	Remote Fault bit	28.2.1.2.3	M		Used in accordance with the Remote Fault function specifications
14	Acknowledge bit set, no Next Page to be sent	28.2.1.2.4	M		Set to logic one in the Link Code Word after the reception of at least three consecutive and consistent FLP Bursts
15	Acknowledge bit set, Next Page to be sent	28.2.1.2.4	NP:M		Set to logic one in the transmitted Link Code Word after the reception of at least three consecutive and consistent FLP Bursts and the current receive Link Code Word is saved
16	Number of Link Code Words sent with Acknowledge bit set	28.2.1.2.4	M		6 to 8 inclusive after COMPLETE ACKNOWLEDGE state entered
17	Device does not implement optional Next Page ability	28.2.1.2.5	M		NP=0 in base Link Code Word
18	Device implements optional Next Page ability and wishes to engage in Next Page exchange	28.2.1.2.5	NP:M		NP=1 in base Link Code Word
19	Transmit Switch function on completion of Auto-Negotiation	28.2.1.3	M		Enables the transmit path from a single technology-dependent PMA to the MDI once the highest common denominator has been selected
20	Transmit Switch function during Auto-Negotiation	28.2.1.3	M		Connects FLP Burst generator governed by Figure 28–14 to the MDI
21	Signals presented at MDI after connection through Transmit Switch from PMA	28.2.1.3	M		Conform to appropriate PHY specifications

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28.5.4.4 Receive function requirements

Item	Feature	Subclause	Status	Support	Value/comment
1	Timer expiration	28.2.2.1	M		Timer definition in 28.3.2, values shown in Table 28–9
2	Identification of Link Partner as Auto-Negotiation able	28.2.2.1	M		Reception of 6 to 17 (inclusive) consecutive link pulses separated by at least flp_test_min_timer time but less than flp_test_max_timer time
3	First FLP Burst identifying Link Partner as Auto-Negotiation able	28.2.2.1	M		Data recovered is discarded if FLP Burst is incomplete
4	First link pulse in an FLP Burst	28.2.2.1	M		Interpreted as a clock link pulse
5	Restart of the data_detect_min_timer and data_detect_max_timer	28.2.2.1	M		Detection of a clock link pulse (Figure 28–9)
6	Reception of logic one	28.2.2.1	M		Link pulse received between greater than data_detect_min_timer time and less than data_detect_max_timer time after a clock pulse (Figure 28–9)
7	Reception of logic zero	28.2.2.1	M		Link pulse received after greater than data_detect_max_timer time after clock pulse, is treated as clock pulse (Figure 28–9)
8	FLP Bursts separation	28.2.2.1	M		Conforms to the nlp_test_min_timer and nlp_test_max_timer timing (Figure 28–10)
9	Receive Switch function on completion of Auto-Negotiation	28.2.2.3	M		Enables the receive path from the MDI to a single technology-dependent PMA once the highest common denominator has been selected
10	Receive Switch function during Auto-Negotiation	28.2.2.3	M		Connects the MDI to the FLP and NLP receivers governed by Figures 28–15 and 28–17, and to the 100BASE-TX and 100BASE-T4 receivers if present
11	Signals presented to PMA after connection through Receive Switch from MDI	28.2.2.3	M		Conform to appropriate PHY specifications
12	Generation of ability_match, acknowledge_match, and consistency_match	28.2.2.4	M		Responsibility of Receive function in accordance with 28.3.1

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28.5.4.5 Arbitration functions

Item	Feature	Subclause	Status	Support	Value/comment
1	MDI receive connection during Auto-Negotiation, prior to FLP detection	28.2.3.1	M		Connected to the NLP Receive Link Integrity Test state diagram, and the link integrity test functions of 100BASE-TX and/or 100BASE-T4. Not connected to the 10BASE-T or any other PMA
2	Parallel detection operational mode selection	28.2.3.1	M		Set link_control=ENABLE for the single PMA indicating link_status=READY when the autoneg_wait_timer expires
3	Parallel detection PMA control	28.2.3.1	M		Set link_control=DISABLE to all PMAs except the selected operational PMA and indicate Auto-Negotiation has completed
4	Parallel detection setting of link partner ability register	28.2.3.1	M		On transition to the FLP LINK GOOD CHECK state from the LINK STATUS CHECK state the Parallel Detection function shall set the bit in the link partner ability register (Register 5) corresponding to the technology detected by the Parallel Detection function
5	Response to renegotiation request	28.2.3.2	M		Disable all technology-dependent link integrity test functions and halt transmit activity until break_link_timer expires
6	Auto-Negotiation resumption	28.2.3.2	M		Issue FLP Bursts with base page valid in tx_link_code_word[16:1] after break_link_timer expires
7	Priority resolution	28.2.3.3	M		Single PMA connected to MDI is enabled corresponding to Technology Ability Field bit common to both Local/Link Partner Device and that has highest priority as defined by Annex 28B
8	Effect of receipt of reserved Technology Ability Field bit on priority resolution	28.2.3.3	M		Local Device ignores during priority resolution
9	Effect of parallel detection on priority resolution	28.2.3.3	M		Local Device considers technology identified by parallel detection as HCD
10	Values for HCD and link_status_[HCD] in the event there is no common technology	28.2.3.3	M		HCD=NULL link_status_[HCD]=FAIL

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28.5.4.5 Arbitration functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
11	Message Page to Unformatted Page relationship for non-matching Selector Fields	28.2.3.4	NP:M		Each series of Unformatted Pages is preceded by an Message Page containing a message code that defines how the following Unformatted Page(s) will be interpreted
12	Message Page to Unformatted Page relationship for matching Selector Fields	28.2.3.4	NP:M		Use of Message Pages is specified by the Selector Field value
13	Transmission of Null message codes	28.2.3.4	NP:M		Sent with NP=0 on completion of all Next Pages while Link Partner continues to transmit valid Next Page information
14	Reception of Null message codes	28.2.3.4	NP:M		Recognized as indicating end of Link Partner's Next Page information
15	Next Page encoding	28.2.3.4.1	NP:M		Comply with Figures 28–11 and 28–12 for the NP, Ack, MP, Ack2, and T bits
16	Message/Unformatted Code Field	28.2.3.4.1	NP:M		D10-D0 encoded as Message Code Field if MP=1 or Unformatted Code Field if MP=0
17	NP bit encoding	28.2.3.4.2	NP:M		Logic 0=last page, logic 1=additional Next Page(s) follow
18	Message Page bit encoding	28.2.3.4.4	NP:M		Logic 0=Unformatted Page, logic 1=Message Page
19	Ack2 bit encoding	28.2.3.4.5	NP:M		Logic 0=cannot comply with message; logic 1= will comply with message
20	Toggle	28.2.3.4.6	NP:M		Takes the opposite value of the Toggle bit in the previously exchanged Link Code Word
21	Toggle encoding	28.2.3.4.6	NP:M		Logic zero = previous value of the transmitted Link Code Word equalled logic one Logic one = previous value of the transmitted Link Code Word equalled logic zero
22	Message Page encoding	28.2.3.4.7	NP:M		If MP=1, Link Code Word interpreted as Message Page
23	Message Code Field	28.2.3.4.8	NP:M		Combinations not shown in Annex 28B are reserved and may not be transmitted
24	Unformatted Page encoding	28.2.3.4.9	NP:M		If MP=0, Link Code Word interpreted as Unformatted Page

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28.5.4.5 Arbitration functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
25	Minimum Next Page exchange	28.2.3.4.11	NP:M		If both devices indicate Next Page able, both send a minimum of one Next Page
26	Multiple Next Page exchange	28.2.3.4.11	NP:M		If both devices indicate Next Page able, exchange continues until neither Local/Remote Device has additional information; device sends Next Page with Null Message Code if it has no information to transmit
27	Unformatted Page ordering	28.2.3.4.11	NP:M		Unformatted Pages immediately follow the referencing Message Code in the order specified by the Message Code
28	Next Page Transmit register	28.2.3.4.12	NP:M		Defined in 28.2.4.1.6
29	Next Page receive data	28.2.3.4.12	NP:O		May be stored in Auto-Negotiation link partner ability register
30	Remote Fault sensing	28.2.3.5	RF:M		Optional
31	Transmission of RF bit by Local Device	28.2.3.5	M		If Local Device has no method to set RF bit, it must transmit RF bit with value of RF bit in Auto-Negotiation advertisement register (4.13)
32	RF bit reset	28.2.3.5	M		Once set, the RF bit remains set until successful renegotiation with the base Link Code Word
33	Receipt of Remote Fault indication in Base Link Code Word	28.2.3.5	MII:M		Device sets the Remote Fault bit in the MII status register (1.4) to logic one if MII is present

28.5.4.6 Management function requirements

Item	Feature	Subclause	Status	Support	Value/comment
1	Mandatory MII registers for Auto-Negotiation	28.2.4.1	MII:M		Registers 0, 1, 4, 5, 6
2	Optional MII register for Auto-Negotiation	28.2.4.1	MII* NP:M		Register 7
3	Auto-Negotiation enable	28.2.4.1.1	MII:M		Set control register Auto-Negotiation Enable bit (0.12)

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28.5.4.6 Management function requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
4	Manual Speed/Duplex settings	28.2.4.1.1	MII:M		When bit 0.12 set, control register Speed Detection (0.13) and Duplex Mode (0.8) are ignored, and the Auto-Negotiation function determines link configuration
5	Control register (Register 0) Restart Auto-Negotiation (0.9) default	28.2.4.1.1	MII:M		PHY returns value of one in 0.9 until Auto-Negotiation has been initiated
6	Control register (Register 0) Restart Auto-Negotiation (0.9) set	28.2.4.1.1	MII:M		When 0.9 set, Auto-Negotiation will (re)initiate. On completion, 0.9 will be reset by the PHY device. Writing a zero to 0.9 at any time has no effect
7	Control register (Register 0) Restart Auto-Negotiation (0.9) reset	28.2.4.1.1	MII:M		0.9 is self-clearing; writing a zero to 0.9 at any time has no effect
8	Status register (Register 1) Auto-Negotiation Complete (1.5) reset	28.2.4.1.2	MII:M		If bit 0.12 reset, or a PHY lacks the ability to perform Auto-Negotiation, (1.5) is reset
9	Status register (Register 1) Remote Fault (1.4)	28.2.4.1.2	MII:M		Set by the PHY and remains set until either the status register is read or the PHY is reset
10	Advertisement register power on default	28.2.4.1.3	MII:M		Selector field as defined in Annex 28A; Ack=0; Technology Ability Field based on MII status register (1.15:11) or logical equivalent
11	Link partner ability register read/write	28.2.4.1.4	MII:M		Read only; write has no effect
12	Link partner ability register bit definitions	28.2.4.1.4	MII:M		Direct representation of the received Link Code Word (Figure 28–7)
13	Status register (Register 1) Auto-Negotiation Complete (1.5) set	28.2.4.1.4	MII:M		Set to logic one upon successful completion of Auto-Negotiation
14	Auto-Negotiation expansion register (Register 6)	28.2.4.1.5	MII:M		Read only; write has no effect
15	Link Partner Auto-Negotiation Able bit (6.0)	28.2.4.1.5	MII:M		Set to indicate that the Link Partner is able to participate in the Auto-Negotiation function
16	Page Received bit (6.1) set	28.2.4.1.5	MII:M		Set to indicate that a new Link Code Word has been received and stored in the Auto-Negotiation link partner ability register
17	Page Received bit (6.1) reset	28.2.4.1.5	MII:M		Reset on a read of the Auto-Negotiation expansion register (Register 6)

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28.5.4.6 Management function requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
18	The Next Page Able bit (6.2) set	28.2.4.1.5	NP* MII:M		Set to indicate that the Local Device supports the Next Page function
19	The Link Partner Next Page Able bit (6.3) set	28.2.4.1.5	MII:M		Set to indicate that the Link Partner supports the Next Page function
20	Parallel Detection Fault bit (6.4) set	28.2.4.1.5	MII:M		Set to indicate that zero or more than one of the NLP Receive Link Integrity Test function, 100BASE-TX, or 100BASE-T4 PMAs have indicated link_status=READY when the autoneg_wait_timer expires
21	Parallel Detection Fault bit (6.4) reset	28.2.4.1.5	MII:M		Reset on a read of the Auto-Negotiation expansion register (Register 6)
22	Next Page Transmit register default	28.2.4.1.6	NP* MII:M		On power-up, contains value of 2001 H
23	Write to Next Page Transmit register	28.2.4.1.6	NP* MII:M		mr_next_page_loaded set to true
24	Absence of management function	28.2.5	NOM:M		Advertised abilities provided through a logical equivalent of mr_adv_ability[16:1]
25	Next Page support in absence of MII management	28.2.5	NOM:M		Device must provide logical equivalent of mr_np_able, mr_lp_np_able, or mr_next_page_loaded variables in order to set NP bit in transmitted Link Code Word

28.5.4.7 Technology-dependent interface

Item	Feature	Subclause	Status	Support	Value/comment
1	PMA_LINK.indicate(link_status) values	28.2.6.1.1	M		link_status set to READY, OK or FAIL
2	PMA_LINK.indicate(link_status) generation	28.2.6.1.2	M		Technology-dependent PMA and NLP Receive Link Integrity Test state diagram (Figure 28–17) responsibility
3	PMA_LINK.indicate(link_status), effect of receipt	28.2.6.1.3	M		Governed by the state diagram of Figure 28–16
4	PMA_LINK.request(link_control) values	28.2.6.1.3	M		link_control set to SCAN_FOR_CARRIER, DISABLE, or ENABLE

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28.5.4.7 Technology-dependent interface *(continued)*

Item	Feature	Subclause	Status	Support	Value/comment
5	Effect of link_control=SCAN_FOR_CARRIER	28.2.6.2.1	M		PMA to search for carrier and report link_status=READY when carrier is received, but no other actions are enabled
6	Effect of link_control=DISABLE	28.2.6.2.1	M		Disables PMA processing
7	Effect of link_control=ENABLE	28.2.6.2.1	M		Control passed to a single PMA for normal processing functions
8	PMA_LINK.request(link_control) generation	28.2.6.2.2	M		Auto-Negotiation function responsibility in accordance with Figures 28–15 and 28–16
9	PMA_LINK.request(link_control) default upon power-on, reset, or release from power-down	28.2.6.2.2	M		link_control = DISABLE state to all technology-dependent PMAs
10	PMA_LINK.request(link_control) effect of receipt	28.2.6.2.3	M		Governed by Figure 28–17 and the receiving technology-dependent link integrity test function
11	The linkpulse parameter shall	28.2.6.3.1	M	Yes [ ]	TRUE or FALSE.
12	The linkpulse=FALSE shall be used	28.2.6.3.1	M	Yes [ ]	By the Auto-Negotiation function to indicate that the Receive State Diagram has performed a state transition.
13	The linkpulse=TRUE shall be used	28.2.6.3.1	M	Yes [ ]	By the Auto-Negotiation function to indicate that a valid Link Pulse has been received.
14	The Auto-Negotiation function shall generate linkpulse	28.2.6.3.2	M	Yes [ ]	To indicate to the PHY how to respond, in accordance with the state diagram of Figure 28–15.
15	Upon power-on or reset, if Auto-Negotiation is enabled (mr_autoneg_enable=true) the PMA_LINKPULSE.request(FALSE) message shall be	28.2.6.3.2	M	Yes [ ]	Issued to all technology-dependent PMAs.
16	The effect of the receipt of linkpulse shall be governed	28.2.6.3.3	M	Yes [ ]	By the receiving technology-dependent PMA function, based on the intent specified in the primitive semantics.

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28.5.4.8 State diagrams

Item	Feature	Subclause	Status	Support	Value/comment
1	Adherence to state diagrams	28.3	M		Implement all features of Figures 28–14 to 28–17. Identified options to Figures 28–14 to 28–17 are permitted
3	Ambiguous requirements	28.3	M		State diagrams take precedence in defining functional operation
4	autoneg_wait_timer	28.3.1	M		Expires between 500–1000 ms after being started
5	break_link_timer	28.3.2	M		Expires between 1200–1500 ms after being started
6	data_detect_min_timer	28.3.2	M		Expires between 15–47 μs from the last clock pulse
7	data_detect_max_timer	28.3.2	M		Expire between 78–100 μs from the last clock pulse
8	flp_test_max_timer	28.3.2	M		Expires between 165–185 μs from the last link pulse
9	flp_test_min_timer	28.3.2	M		Expires between 5–25 μs from the last link pulse
10	interval_timer	28.3.2	M		Expires 55.5–69.5 μs from each clock pulse and data bit
11	link_fail_inhibit_timer	28.3.2	M		Expires 750–1000 ms after entering the FLP LINK GOOD CHECK state
12	nlp_test_max_timer	28.3.2	M		Expires between 50–150 ms after being started if not restarted
13	nlp_test_min_timer	28.3.2	M		Expires between 5–7 ms after being started if not restarted
14	transmit_link_burst_timer	28.3.1	M		Expires 5.7–22.3 ms after the last transmitted link pulse in an FLP Burst

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28.5.4.9 Electrical characteristics

Item	Feature	Subclause	Status	Support	Value/comment
1	Pulses within FLP Bursts	28.4	M		Identical to the characteristics of NLPs and meet the requirements of Figure 14–12

28.5.4.10 Auto-Negotiation annexes

Item	Feature	Annex	Status	Support	Value/comment
1	Selector field, S[4:0] values in the Link Code Word	Annex 28A	M		Identifies base message type as defined by Table 28A–1
2	Selector field reserved combinations	Annex 28A	M		Transmission not permitted
3	Relative priorities of the technologies supported by the IEEE 802.3 Selector Field value	28B.3	M		Defined in Annex 28B.3
4	Relative order of the technologies supported by IEEE 802.3 Selector Field	28B.3	M		Remain unchanged
5	Addition of new technology	28B.3	M		Inserted into its appropriate place in the priority resolution hierarchy, shifting technologies of lesser priority lower in priority
6	Addition of vendor-specific technology	28B.3	M		Priority of IEEE 802.3 standard topologies maintained, vendor-specific technologies to be inserted into an appropriate location
7	Message Code Field	Annex 28C	NP:M		Defines how following Unformatted Pages (if applicable) are interpreted
8	Message Code Field reserved combinations	Annex 28C	NP:M		Transmission not permitted
9	Auto-Negotiation reserved code 1	28C.1	NP:M		Transmission of M10 to M0 equals 0, not permitted
10	Null Message Code	28C.2	NP:M		Transmitted during Next Page exchange when the Local Device has no information to transmit and Link Partner has additional pages to transmit
11	Remote Fault Identifier Message Code	28C.5	NP:M		Followed by single Unformatted Page to identify fault type with types defined in 28C.5

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28.5.4.10 Auto-Negotiation annexes *(continued)*

Item	Feature	Annex	Status	Support	Value/comment
12	Organizationally Unique Identifier Message Code	28C.6	NP:M		Followed by 4 Unformatted Pages. First Unformatted Page contains most significant 11 bits of OUI (bits 23:13) with MSB in U10; Second Unformatted Page contains next most significant 11 bits of OUI (bits 12:2), with MSB in U10; Third Unformatted Page contains the least significant 2 bits of OUI (bits 1:0) with MSB in U10, bits U8:0 contains user-defined code specific to OUI; Fourth Unformatted Page contains user-defined code specific to OUI
13	PHY Identifier Message Code	28C.7	NP:M		Followed by 4 Unformatted Pages. First Unformatted Page contains most significant 11 bits of PHY ID (2.15:5) with MSB in U10; Second Unformatted Page contains PHY ID bits 2.4:0 to 3.15:10, with MSB in U10; Third Unformatted Page contains PHY ID bits 3.9:0, with MSB in U10, and U0 contains user-defined code specific to PHY ID; Fourth Unformatted Page contains user-defined code specific to PHY ID
14	Auto-Negotiation reserved code 2	28C.8	NP:M		Transmission of M10 to M0 equals 1, not permitted

28.6 Auto-Negotiation expansion

Auto-Negotiation is designed in a way that allows it to be easily expanded as new technologies are developed. When a new technology is developed, the following things must be done to allow Auto-Negotiation to support it:

a) The appropriate Selector Field value to contain the new technology must be selected and allocated.
b) A Technology bit must be allocated for the new technology within the chosen Selector Field value.
c) The new technology's relative priority within the technologies supported within a Selector Field value must be established.

Code space allocations are enumerated in Annex 28A, Annex 28B, and Annex 28C. Additions and insertions to the annexes are allowed. No changes to existing bits already defined are allowed.

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29. System considerations for multisegment 100BASE-T networks

29.1 Overview

This clause provides information on building 100BASE-T networks. The 100BASE-T technology is designed to be deployed in both homogenous 100 Mb/s networks and heterogeneous 10/100 Mb/s mixed CSMA/CD networks. Network topologies can be developed within a single 100BASE-T collision domain, but maximum flexibility is achieved by designing multiple collision domain networks that are joined by bridges and/or routers configured to provide a range of service levels to DTEs. For example, a combined 100BASE-T/10BASE-T system built with repeaters and bridges can deliver dedicated 100 Mb/s, shared 100 Mb/s, dedicated 10 Mb/s, and shared 10 Mb/s service to DTEs. The effective bandwidth of shared services is controlled by the number of DTEs that share the service.

Linking multiple 100BASE-T collision domains with bridges maximizes flexibility. Bridged topology designs can provide single bandwidth (Figure 29–1) or multiple bandwidth (Figure 29–2) services.

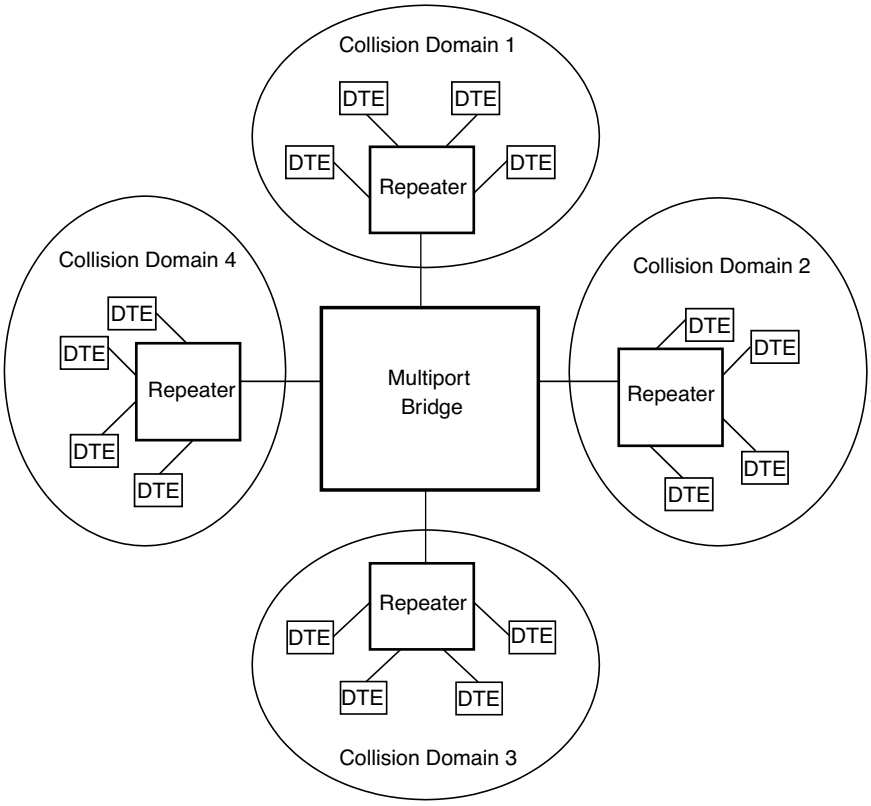


Figure 29–1—100 Mb/s multiple collision domain topology using multiport bridge

Individual collision domains can be linked by single devices (as shown in Figure 29–1 and Figure 29–2) or by multiple devices from any of several transmission systems. The design of multiple-collision-domain networks is governed by the rules defining each of the transmission systems incorporated into the design.

The design of shared bandwidth 10 Mb/s collision domains is defined in 13.1through 13.4; the design of shared bandwidth 100 Mb/s CSMA/CD collision domains is defined in 29.1.1 through 29.3.1.2. The design of 10BASE full duplex LANs is defined in 13.5; the design of full duplex 100BASE-X LANs is defined in 29.4.

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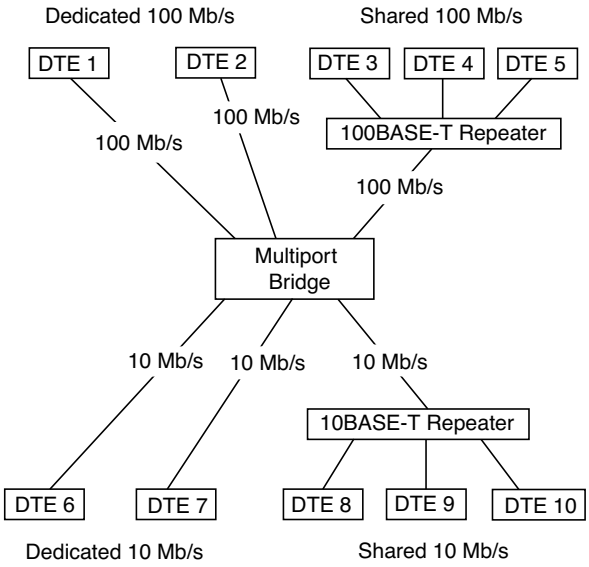


Figure 29–2—Multiple bandwidth, multiple collision domain topology using multiport bridge

29.1.1 Single collision domain multisegment networks

This clause provides information on building 100 Mb/s CSMA/CD multisegment networks within a single collision domain. The proper operation of a CSMA/CD network requires the physical size and number of repeaters to be limited in order to meet the round-trip propagation delay requirements of 4.2.3.2.3 and 4.4.2.1 and IPG requirements specified in 4.4.2.1.

This clause provides two network models. Transmission System Model 1 is a set of configurations that have been validated under conservative rules and have been qualified as meeting the requirements set forth above. Transmission System Model 2 is a set of calculation aids that allow those configuring a network to test a proposed configuration against a simple set of criteria that allows it to be qualified. Transmission System Model 2 validates an additional broad set of topologies that are fully functional and do not fit within the simpler, but more restrictive rules of Model 1.

The physical size of a CSMA/CD network is limited by the characteristics of individual network components. These characteristics include the following:

a) Media lengths and their associated propagation time delay
b) Delay of repeater units (start-up, steady-state, and end of event)
c) Delay of MAUs and PHYs (start-up, steady-state, and end of event)
d) Interpacket gap shrinkage due to repeater units
e) Delays within the DTE associated with the CSMA/CD access method
f) Collision detect and deassertion times associated with the MAUs and PHYs

Table 29–1 summarizes the delays for 100BASE-T media segments. For more detailed information on the delays associated with individual 100BASE-T components, see

MII: Annex 22A
100BASE-T2: 32.12
100BASE-T4: 23.11

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100BASE-TX: 24.6
100BASE-FX: ISO/IEC 9314-3: 1990
Repeater: 27.3

Table 29–1—Delays for network media segments Model 1

Media type	Maximum number of PHYs per segment	Maximum segment length (m)	Maximum medium round-trip delay per segment (BT)
Balanced cable Link Segment 100BASE-T	2	100	114
Fiber Link Segment	2	412	412

29.1.2 Repeater usage

Repeaters are the means used to connect segments of a network medium together into a single collision domain. Different signaling systems (i.e., 100BASE-T2, 100BASE-T4, 100BASE-TX, 100BASE-FX) can be joined into a common collision domain using repeaters. Bridges can also be used to connect different signaling systems; however, if a bridge is so used, each system connected to the bridge will be a separate collision domain.

Two types of repeaters are defined for 100BASE-T (see Clause 27). Class I repeaters are principally used to connect unlike physical signaling systems and have internal delays such that only one Class I repeater can reside within a single collision domain when maximum cable lengths are used (see Figure 29–4). Class II repeaters typically provide ports for only one physical signaling system type (e.g., 100BASE-TX but not 100BASE-T4) and have smaller internal delays so that two such repeaters may reside within a given collision domain when maximum cable lengths are used (see Figure 29–6). Cable length can be sacrificed to add additional repeaters in a collision domain (see 29.3).

29.2 Transmission System Model 1

The following network topology constraints apply to networks using Transmission System Model 1.

a) All balanced cable (copper) segments less than or equal to 100 m each.
b) Fiber segments less than or equal to 412 m each.
c) MII cables for 100BASE-T shall not exceed 0.5 m each. When evaluating system topology, MII cable delays need not be accounted for separately. Delays attributable to the MII are incorporated into DTE and repeater component delays.

29.3 Transmission System Model 2

The physical size and number of topological elements in a 100BASE-T network is limited primarily by round-trip collision delay. A network configuration must be validated against collision delay using a network model. Since there are a limited number of topology models for any 100BASE-T collision domain, the modeling process is quite straightforward and can easily be done either manually or with a spreadsheet.

The model proposed here is derived from the one presented in 13.4. Modifications have been made to accommodate adjustments for DTE, repeater, and cable speeds.

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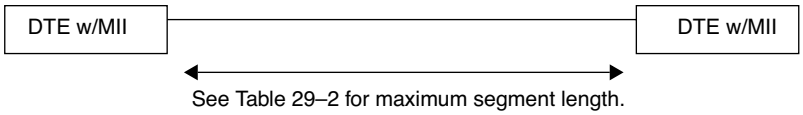


Figure 29–3—Model 1: Two DTEs, no repeater

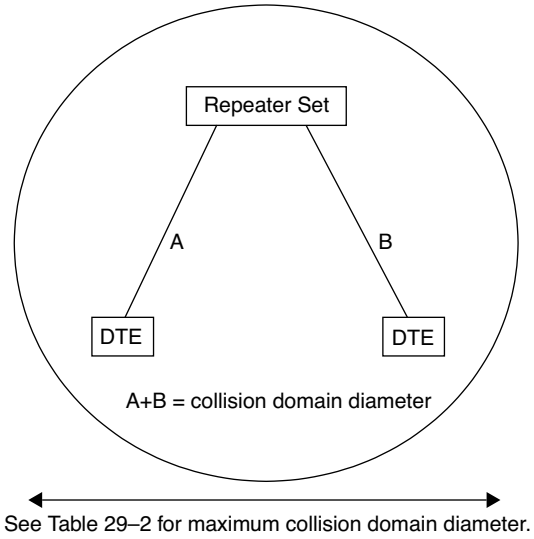


Figure 29–4—Model 1: Single repeater

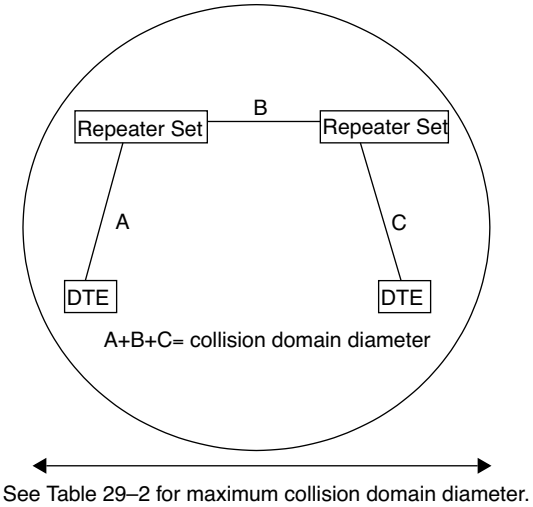


Figure 29–5—System Model 1: Two Class II repeaters

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Table 29–2—Maximum Model 1 collision domain diameter[a]

Model	Balanced cabling (copper)	Fiber	Balanced cabling & fiber (T2 or T4 and FX)	Balanced cabling & fiber (TX and FX)
DTE-DTE (see Figure 29–3)	100	412	NA	NA
One Class I repeater (see Figure 29–4)	200	272	231[a]	260.8[a]
One Class II repeater (see Figure 29–4)	200	320	304[b]	308.8[b]
Two Class II repeaters (see Figure 29–5)	205	228	236.3[c]	216.2[c]

[a]Assumes 100 m of balanced cabling and one fiber link.
[b]This entry included for completeness. It may be impractical to construct a T4 to FX class II repeater.
[c] Assumes 105 m of balanced cabling and one fiber link.

29.3.1 Round-trip collision delay

For a network to be valid, it must be possible for any two DTEs on the network to contend for the network at the same time. Each station attempting to transmit must be notified of the contention by the returned "collision" signal within the "collision window" (see 4.1.2.2 and 5.2.2.1.2). Additionally, the maximum length fragment created must contain less than 512 bits after the start-of-frame delimiter (SFD). These requirements limit the physical diameter (maximum distance between DTEs) of a network. The maximum round-trip delay must be qualified between all pairs of DTEs in the network. In practice this means that the qualification must be done between those that, by inspection of the topology, are candidates for the longest delay. The following network modeling methodology is provided to assist that calculation.

29.3.1.1 Worst-case path delay value (PDV) selection

The worst-case path through a network to be validated shall be identified by examination of aggregate DTE delays, cable delays, and repeater delays. The worst case consists of the path between the two DTEs at opposite ends of the network that have the longest round-trip time. Figure 29–6 and Figure 29–7 show schematic representatins of one-repeater and two-repeater paths.

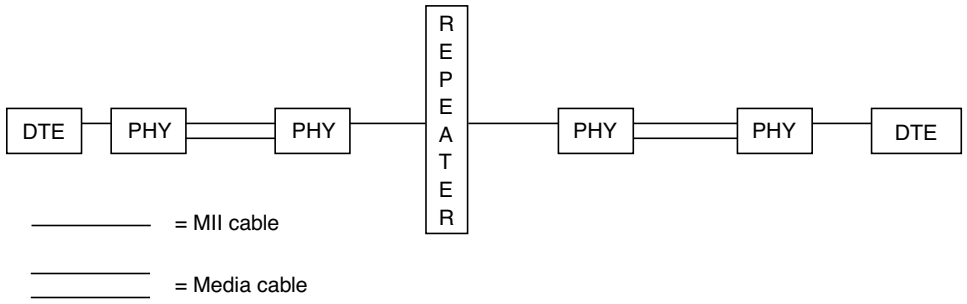


Figure 29–6—System Model 2: Single repeater

29.3.1.2 Worst-case PDV calculation

Once a set of paths is chosen for calculation, each shall be checked for validity against the following formula:

$$PDV = \sum \text{link delays (LSDV)} + \sum \text{repeater delays} + \text{DTE delays} + \text{safety margin}$$

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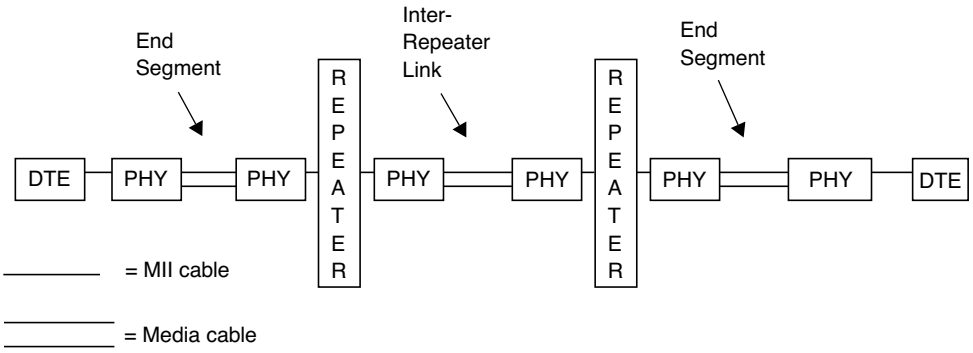


Figure 29–7—System Model 2-2: Two repeaters

Values for the formula variables are determined by the following method:

a) Determine the delay for each link segment (Link Segment Delay Value, or LSDV), including inter-repeater links, using the formula

LSDV=2 (for round-trip delay) × segment length × cable delay for this segment

NOTE 1—Length is the sum of the cable lengths between the PHY interfaces at the repeater and the farthest DTE for End Segments plus the sum of the cable lengths between the repeater PHY interfaces for Inter-Repeater Links. All measurements are in meters.

NOTE 2—Cable delay is the delay specified by the manufacturer or the maximum value for the type of cable used as shown in Table 29–3. For this calculation, cable delay must be specified in bit times per meter (BT/m). Table 29–4 can be used to convert values specified relative to the speed of light (%c) or nanoseconds per meter (ns/m).

NOTE 3—When actual cable lengths or propagation delays are not known, use the Max delay in bit times as specified in Table 29–3 for copper cables. Delays for fiber should be calculated, as the value found in Table 29–3 will be too large for most applications.

b) Sum together the LSDVs for all segments in the path.

c) Determine the delay for each repeater in the path. If model-specific data are not available from the manufacturer, determine the class of each repeater (I or II) and enter the appropriate default value from Table 29–3.

d) MII cables for 100BASE-T shall not exceed 0.5 m each. When evaluating system topology, MII cable delays need not be accounted for separately. Delays attributable to the MII are incorporated into DTE and repeater component delays.

e) Use the DTE delay value shown in Table 29–3 unless your equipment manufacturer defines a different value.

f) Decide on appropriate safety margin—0 to 5 bit times—for the PDV calculation. Safety margin is used to provide additional margin to accommodate unanticipated delay elements, such as extra-long connecting cable runs between wall jacks and DTEs. (A safety margin of 4 BT is recommended.)

g) Insert the values obtained through the calculations above into the following formula to calculate the PDV. (Some configurations may not use all the elements of the formula.)

PDV = ∑link delays (LSDV) + ∑repeater delays + DTE delay + safety margin

h) If the PDV is less than 512, the path is qualified in terms of worst-case delay.

i) Late collisions and/or CRC errors are indicators that path delays exceed 512 BT.

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Table 29–3—Network component delays, Transmission System Model 2

Component	Round trip delay in bit times per meter	Maximum round trip delay in bit times
Two TX/FX DTEs		100
Two T4 DTEs		138
Two T2 DTEs		96
One T2 or T4 and one TX/FX DTE[a]		127
Cat 3 cabling segment	1.14	114 (100 m)
Cat 4 cabling segment	1.14	114 (100 m)
Cat 5 cabling segment	1.112	111.2 (100 m)
STP cabling segment	1.112	111.2 (100 m)
Fiber optic cabling segment	1.0	412 (412 m)
Class I repeater		140
Class II repeater with all ports TX/FX		92
Class II repeater with any port T4		67
Class II repeater with any port T2		90

[a] Worst-case values are used (TX/FX values for MAC transmit start and MDI input to collision detect; T4 value for MDI input to MDI output).

Table 29–4—Conversion table for cable delays

Speed relative to c	ns/m	BT/m
0.4	8.34	0.834
0.5	6.67	0.667
0.51	6.54	0.654
0.52	6.41	0.641
0.53	6.29	0.629
0.54	6.18	0.618
0.55	6.06	0.606
0.56	5.96	0.596
0.57	5.85	0.585
0.58	5.75	0.575
0.5852	5.70	0.570
0.59	5.65	0.565
0.6	5.56	0.556
0.61	5.47	0.547
0.62	5.38	0.538

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Table 29–4—Conversion table for cable delays *(continued)*

Speed relative to c	ns/m	BT/m
0.63	5.29	0.529
0.64	5.21	0.521
0.65	5.13	0.513
0.654	5.10	0.510
0.66	5.05	0.505
0.666	5.01	0.501
0.67	4.98	0.498
0.68	4.91	0.491
0.69	4.83	0.483
0.7	4.77	0.477
0.8	4.17	0.417
0.9	3.71	0.371

29.4 Full duplex 100 Mb/s topology limitations

Unlike half duplex CSMA/CD networks, the physical size of full duplex 100 Mb/s CSMA/CD networks is not limited by the round-trip collision propagation delay. Instead, the maximum link length between DTEs is limited only by the signal transmission characteristics of the specific cable, as specified in Table 29–5.

Table 29–5—Link segment length limits; 100 Mb/s full duplex segments

Cable Type	Maximum link segment length
100BASE-TX (UTP, STP per Clause 25)	**100 m**
100BASE-FX (multimode fiber per Clause 26)	**2000 m**
100BASE-T2 (UTP per Clause 32)	**100 m**

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30. 10 Mb/s, 100 Mb/s, 1000 Mb/s, MAC Control, and Link Aggregation Management

30.1 Overview

This clause provides the Layer Management specification for DTEs, repeaters, and MAUs based on the CSMA/CD access method. The clause is produced from the ISO framework additions to Clause 5, Layer Management; Clause 19, Repeater Management; and Clause 20, MAU Management. It incorporates additions to the objects, attributes, and behaviors to support 100 and 1000 Mb/s CSMA/CD, full duplex operation, MAC Control, and Link Aggregation.

The layout of this clause takes the same form as 5.1, 5.2, and Clauses 19 and 20, although with equivalent subclauses grouped together. It identifies a common management model and framework applicable to IEEE 802.3 managed elements, identifies those elements and defines their managed objects, attributes, and behaviours in a protocol-independent language. It also includes a formal GDMO definition of the protocol encodings for CMIP and ISO/IEC 15802-2: 1995 [ANSI/IEEE Std 802.1B and 802.1k, 1995 Edition].

NOTE—The arcs (that is, object identifier values) defined in Annex 30A, the formal GDMO definitions, deprecate the arcs previously defined in Annexes H.1 (Layer Management), H.2 (Repeater Management), and H.3 (MAU Management). See IEEE Std 802.1F-1993, Annex C.4.

This clause provides the Layer Management specification for DTEs, repeaters, and MAUs based on the CSMA/CD access method. It defines facilities comprised of a set of statistics and actions needed to provide IEEE 802.3 Management services. The information in this clause should be used in conjunction with the Procedural Model defined in 4.2.7 through 4.2.10. The Procedural Model provides a formal description of the relationship between the CSMA/CD Layer Entities and the Layer Management facilities.

This management specification has been developed in accordance with the OSI management architecture as specified in the ISO Management Framework document, ISO/IEC 7498-4: 1989. It is independent of any particular management application or management protocol.

The management facilities defined in this standard may be accessed both locally and remotely. Thus, the Layer Management specification provides facilities that can be accessed from within a station or can be accessed remotely by means of a peer-management protocol operating between application entities.

In CSMA/CD no peer management facilities are necessary for initiating or terminating normal protocol operations or for handling abnormal protocol conditions. Since these activities are subsumed by the normal operation of the protocol, they are not considered to be a function of Layer Management and are, therefore, not discussed in this clause.

Implementation of part or all of 10 Mb/s, 100 Mb/s and 1000 Mb/s Management is not a requirement for conformance to Clauses 4, 7, 9, 22, 23, 24, 25, 26, 27, 28, 31,32, 35, 36, 37, 38, 39, 40, and 41.

The intent of this standard is to furnish a management specification that can be used by the wide variety of different devices that may be attached to a network specified by ISO/IEC 8802-3. Thus, a comprehensive list of management facilities is provided.

The improper use of some of the facilities described in this clause may cause serious disruption of the network. In accordance with ISO management architecture, any necessary security provisions should be provided by the Agent in the Local System Environment. This can be in the form of specific security features or in the form of security features provided by the peer communication facilities.

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30.1.1 Scope

This clause includes selections from Clauses 5, 19, and 20. It is intended to be an entirely equivalent specification for the management of 10 Mb/s DTEs, 10 Mb/s baseband repeater units, and 10 Mb/s integrated MAUs. It also includes the additions for management of full duplex operation, MAC Control, 100 Mb/s and 1000 Mb/s DTEs and repeater units, embedded MAUs, and external PHYs connected with the MII or GMII. Implementations of management for 10 Mb/s DTEs, repeater units, and embedded MAUs should follow the requirements of this clause (e.g., a 10 Mb/s implementation should incorporate the attributes to indicate that it is not capable of 100 or 1000 Mb/s operation, a half duplex DTE should incorporate the attributes to indicate that it is not capable of full duplex operation, etc.).

This clause defines a set of mechanisms that enable management of ISO/IEC 8802-3 10 Mb/s, 100 Mb/s and 1000 Mb/s DTEs, baseband repeater units, and integrated Medium Attachment Units (MAUs). In addition, for ports without integral MAUs, attributes are provided for characteristics observable from the AUI of the connected DTE or repeater. Direct management of AUI MAUs that are external to their respective DTEs or repeaters is beyond the scope of this standard. The managed objects within this standard are defined in terms of their behaviour, attributes, actions, notifications, and packages in accordance with IEEE 802.1 and ISO standards for network management. Managed objects are grouped into mandatory and optional packages.

This specification is defined to be independent of any particular management application or management protocol. The means by which the managed objects defined in this standard are accessed is beyond the scope of this standard.

30.1.2 Relationship to objects in IEEE 802.1F

The following managed object classes, if supported by an implementation, shall be as specified in IEEE Std 802.1F-1993: ResourceTypeID, EWMAMetricMonitor.

oResourceTypeID

This object class is mandatory and shall be implemented as defined in IEEE 802.1F. This object is bound to oMAC-Entity, oRepeater, and oMAU as defined by the NAMEBINDINGs in 30A.8.1. Note that the binding to oMAU is mandatory only when MII is present. The Entity Relationship Diagram, Figure 30–3, shows these bindings pictorially.

oEWMAMetricMonitor

This object class is optional. When implemented, it shall be implemented as defined in IEEE 802.1F, subject to the specific requirements described below. This object is bound to system as defined by the NAMEBINDINGs in 30A.1.1, 30A.3.1, and 30A.2.1.

Implementations of IEEE 802.3 Management that support the oEWMAMetricMonitor managed object class are required to support values of granularity period as small as one second. Implementations are required to support at least one sequence of low and high thresholds. The granularity period may be set to equal to the moving time period as a minimal conformant implementation.

30.1.3 Systems management overview

Within the ISO Open Systems Interconnection (OSI) architecture, the need to handle the special problems of initializing, terminating, and monitoring ongoing activities and assisting in their operations, as well as handling abnormal conditions, is recognized. These needs are collectively addressed by the systems management component of the OSI architecture.

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A management protocol is required for the exchange of information between systems on a network. This management standard is independent of any particular management protocol.

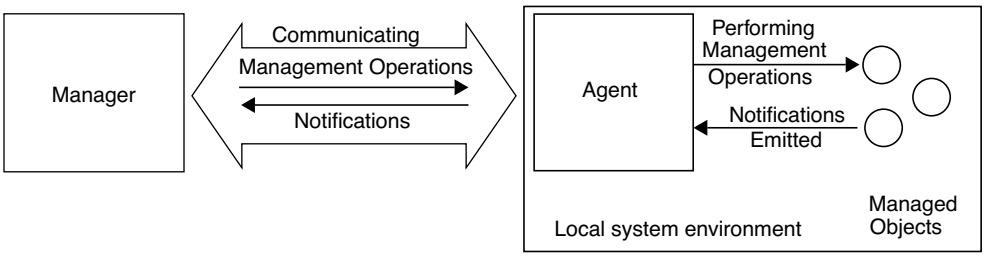
This management standard, in conjunction with the management standards of other layers, provides the means to perform various management functions. IEEE 802.3 Management collects information needed from the MAC and Physical Layers and the devices defined in IEEE 802.3. It also provides a means to exercise control over those elements.

The relationship between the various management entities and the layer entities according to the ISO model is shown in Figure 30–1.

30.1.4 Management model

This standard describes management of DTEs, repeaters, and integrated MAUs in terms of a general model of management of resources within the open systems environment. The model, which is described in ISO/IEC 10040: 1992, is briefly summarized here.

Management is viewed as a distributed application modeled as a set of interacting management processes. These processes are executed by systems within the open environment. A managing system executes a managing process that invokes management operations. A managed system executes a process that is receptive to these management operations and provides an interface to the resources to be managed. A managed object is the abstraction of a resource that represents its properties as seen by (and for the purpose of) management. Managed objects respond to a defined set of management operations. Managed objects are also capable of emitting a defined set of notifications. This interaction of processes is shown in Figure 30–1.



NOTE—This figure is drawn from Figure 1 of ISO/IEC 10040: 1992, Information technology—Open Systems Interconnection—Systems management overview. In the event of any conflict, the depiction in ISO/IEC 10040: 1992 takes precedence.

Figure 30–1—Interaction between manager, agent, and objects

A managed object is a management view of a resource. The resource may be a logical construct, function, physical device, or anything subject to management. Managed objects are defined in terms of four types of elements:

a) *Attributes*. Data-like properties (as seen by management) of a managed object.
b) *Actions*. Operations that a managing process may perform on an object or its attributes.
c) *Notifications*. Unsolicited reports of events that may be generated by an object.
d) *Behaviour*. The way in which managed objects, attributes, and actions interact with the actual resources they model and with each other.

The above items are defined in 30.3, 30.4, 30.5, and 30.6 of this clause in terms of the template requirements of ISO/IEC 10165-4: 1991.

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Some of the functions and resources within 802.3 devices are appropriate targets for management. They have been identified by specifying managed objects that provide a management view of the functions or resources. Within this general model, the 802.3 device is viewed as a managed device. It performs functions as defined by the applicable standard for such a device. Managed objects providing a view of those functions and resources appropriate to the management of the device are specified. The purpose of this standard is to define the object classes associated with the devices in terms of their attributes, operations, notifications, and behaviour.

30.2 Managed objects

30.2.1 Introduction

This clause identifies the Managed Object classes for IEEE 802.3 components within a managed system. It also identifies which managed objects and packages are applicable to which components.

All counters defined in this specification are assumed to be wrap-around counters. Wrap-around counters are those that automatically go from their maximum value (or final value) to zero and continue to operate. These unsigned counters do not provide for any explicit means to return them to their minimum (zero), i.e., reset. Because of their nature, wrap-around counters should be read frequently enough to avoid loss of information. Counters in 30.3, 30.4, 30.5, and 30.6 that have maximum increment rates specified for 10 Mb/s operation, and are appropriate to 100 Mb/s operation, have ten times the stated maximum increment rate for 100 Mb/s operation unless otherwise indicated. Counters that are appropriate to 1000 Mb/s operation have one hundred times the stated maximum increment rate for 1000 Mb/s operation unless otherwise indicated.

30.2.2 Overview of managed objects

Managed objects provide a means to

— Identify a resource
— Control a resource
— Monitor a resource

30.2.2.1 Text description of managed objects

In case of conflict, the formal behavior definitions in 30.3, 30.4, 30.5, 30.6, and 30.7 take precedence over the text descriptions in this subclause.

oAggregator — If implemented, oAggregator is the top-most managed object class of the DTE portion of the containment tree shown in Figure 30–3. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this International Standard. The oAggregator managed object class provides the management controls necessary to allow an instance of an Aggregator to be managed.

oAggregationPort — If oAggregator is implemented, oAggregationPort is contained within oAggregator. An instance of this managed object class is present for each Aggregation Port that is part of the aggregation represented by the oAggregator instance. This managed object class provides the basic management controls necessary to allow an instance of an Aggregation Port to be managed, for the purposes of Link Aggregation.

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oAggPortStats If oAggregator is implemented, a single instance of oAggPortStats may be contained within oAggregationPort. This managed object class provides optional additional statistics related to LACP and Marker protocol activity on an instance of an Aggregation Port that is involved in Link Aggregation.

oAggPortDebugInformation
If oAggregator is implemented, a single instance of oAggPortDebugInformation may be contained within oAggregationPort. This managed object class provides optional additional information that can assist with debugging and fault finding in Systems that support Link Aggregation.

oMACControlEntity If implemented, and if oAggregator is implemented, oMACControlEntity is contained within oAggregator. Otherwise, if implemented, oMACControlEntity becomes the top-most managed object class of the DTE portion of the containment tree shown in Figure 30–3. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this International Standard.

oMACControlFunctionEntity
Contained within oMACControlEntity. Each function defined and implemented within the MAC Control sublayer has an associated oMACControlFunctionEntity for the purpose of managing that function.

oMACEntity If oMACControlEntity is implemented, oMACEntity is contained within oMACControlEntity. Otherwise, if oAggregator is implemented, oMACEntity is contained within oAggregator. Otherwise, oMACEntity becomes the top-most managed object class of the DTE portion of the containment tree shown in Figure 30–3. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this International Standard.

oPHYEntity
Contained within oMACEntity. Many instances of oPHYEntity may coexist within one instance of oMACEntity; however, only one PHY may be active for data transfer to and from the MAC at any one time. oPHYEntity is the managed object that contains the MAU managed object in a DTE.

oRepeater
The top-most managed object class of the repeater portion of the containment tree shown in Figure 30–3. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this standard.

oRepeaterMonitor
A managed object class called out by IEEE Std 802.1F-1993. See 30.1.2, oEWMAMetricMonitor.

oGroup
The group managed object class is a view of a collection of repeater ports.

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oRepeaterPort

The repeater port managed object class provides a view of the functional link between the data transfer service and a single PMA. The attributes associated with repeater port deal with the monitoring of traffic being handled by the repeater from the port and control of the operation of the port. The Port Enable/Disable function as reported by portAdminState is preserved across events involving loss of power. The oRepeaterPort managed object contains the MAU managed object in a repeater set.

NOTE—Attachment to nonstandard PMAs is outside the scope of this standard.

oMAU

The managed object of that portion of the containment tree shown in Figure 30–3. The attributes, notifications, and actions defined in this subclause are contained within the MAU managed object. Neither counter values nor the value of MAUAdminState is required to be preserved across events involving the loss of power.

oAutoNegotiation

The managed object of that portion of the containment tree shown in Figure 30–3. The attributes, notifications, and actions defined in this subclause are contained within the MAU managed object.

oResourceTypeID

A managed object class called out by IEEE Std 802.1F-1993. It is used within this clause to identify manufacturer, product, and revision of managed components that implement functions and interfaces defined within IEEE 802.3. The Clause 22 MII or Clause 35 GMII specifies two registers to carry PHY Identifier (22.2.4.3.1), which provides succinct information sufficient to support oResourceTypeID.

30.2.2.2 Functions to support management

Functions are defined in Clauses 5, 7, 22, 23, 24, 25, 26, 27, 28, 31, 32, 35, 36, 37, 38, 39, 40, and 41 both to facilitate unmanaged operation and managed operation. The functions in these clauses that facilitate managed operation are referenced from the text of this management clause.

30.2.2.2.1 DTE MAC sublayer functions

For DTE MACs, with regard to reception-related error statistics a hierarchical order has been established such that when multiple error statuses can be associated with one frame, only one status is returned to the LLC. This hierarchy in descending order is as follows:

— frameTooLong
— alignmentError
— frameCheckError
— lengthError

The counters are primarily incremented based on the status returned to the MAC client; therefore, the hierarchical order of the counters is determined by the order of the status. Frame fragments are not included in any of the statistics unless otherwise stated. In implementing any of the specified actions, receptions and transmissions that are in progress are completed before the action takes effect.

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30.2.2.2.2 Repeater functions

The Repeater Port Object class contains seven functions which are defined in this clause and are used to collect statistics on the activity received by the port. The relationship of the functions to the repeater port and to the port attributes is shown in Figure 30–2.

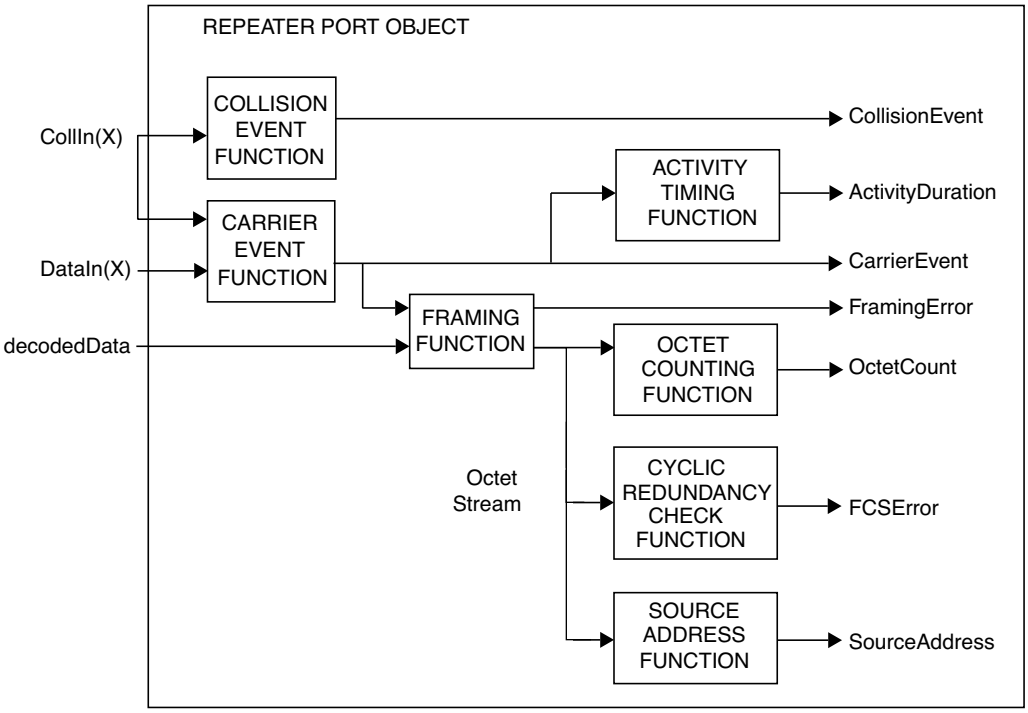


Figure 30–2—Functions relationship

Activity Timing function

The Activity Timing function measures the duration of the assertion of the CarrierEvent signal. For 10 Mb/s repeaters, this duration value must be adjusted by removing the value of Carrier Recovery Time (see 9.5.6.5) to obtain the true duration of activity on the network. The output of the Activity Timing function is the ActivityDuration value, which represents the duration of the CarrierEvent signal as expressed in units of bit times.

Carrier Event function

For 10 Mb/s repeaters theCarrier Event function for port N asserts the CarrierEvent signal when the repeater exits the IDLE state (see Figure 9–2) and the port has been determined to be port N. It de-asserts the CarrierEvent signal when, for a duration of at least Carrier Recovery Time (see 9.5.6.5), both the DataIn(N) variable has the value II and the CollIn(N) variable has the value –SQE. The value N is the port assigned at the time of transition from the IDLE state. For 100 and 1000 Mb/s repeaters the Carrier Event function for port N asserts the CarrierEvent signal when the repeater exits the IDLE state of the repeater state diagram (Figure 27–2 and Figure 41–2) and the port has been determined to be port N. The Carrier Event function for Port N de-asserts the CarrierEvent signal when the repeater enters the IDLE state of the

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repeater state diagram (Figure 27–2 and Figure 41–2).

Collision Event function

The Collision Event function asserts the CollisionEvent signal when a collision is detected at a repeater port. For a 10 Mb/s repeater port this is indicated by the CollIn(X) variable having the value SQE. For a 100 and 1000 Mb/s repeater port this is indicated by entering the COLLISION COUNT INCREMENT state of the partition state diagram (Figure 27–8 and Figure 41–4). The CollisionEvent signal remains asserted until the assertion of any CarrierEvent signal due to the reception of the following event.

Cyclic Redundancy Check function

The Cyclic Redundancy Check function verifies that the sequence of octets output by the Framing function contains a valid Frame Check Sequence Field. The Frame Check Sequence Field is the last four octets received from the output of the Framing function. The algorithm for generating an FCS from the octet stream is specified in 3.2.8. If the FCS generated according to this algorithm is not the same as the last four octets received from the Framing function, then the FCSError signal is asserted. The FCSError signal is cleared and the Cyclic Redundancy Check function is reinitialized upon the assertion of the CarrierEvent signal due to the reception of the following event and, additionally in the case of a frame burst on a 1000 Mb/s network, upon the recognition of a valid Start of Packet delimiter (see 35.2.3.6), once the duration of the CarrierEvent is greater than or equal to slotTime.

Framing function

The Framing function recognizes the boundaries of an incoming frame by monitoring the CarrierEvent signal and the decoded data stream. Data bits are accepted while the CarrierEvent signal is asserted. The framing function delineates frames by stripping the Start of Packet delimiter (see 35.2.3.6), preamble, Start of frame delimiter, End of Packet delimiter (see 35.2.3.6), and any Carrier Extend from the received data stream. The remaining bits of each frame are aligned along octet boundaries. If there is not an integral number of octets, then FramingError shall be asserted. The FramingError signal is cleared upon the assertion of the CarrierEvent signal due to the reception of the following event. For 1000 Mb/s repeaters, the data stream shall continue until the end of the CarrierEvent signal or upon the recognition of a valid Start of Packet delimiter once the duration of the CarrierEvent is greater than or equal to slotTime. Such a Start of Packet delimiter will begin a new data stream.

Octet Counting function

The Octet Counting function counts the number of complete octets received from the output of the framing function. The output of the octet counting function is the OctetCount value. The OctetCount value is reset to zero upon the assertion of the CarrierEvent signal due to the reception of the following event and, additionally in the case of a frame burst on a 1000 Mb/s network, upon the recognition of a valid Start of Packet delimiter (see 35.2.3.6), once the duration of the CarrierEvent is greater than or equal to slotTime.

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Source Address function

The Source Address function extracts octets from the stream output by the framing function. The seventh through twelfth octets shall be extracted from the octet stream and output as the SourceAddress variable. The SourceAddress variable is set to an invalid state upon the assertion of the CarrierEvent signal due to the reception of the following event and, additionally in the case of a frame burst on a 1000 Mb/s network, upon the recognition of a valid Start of Packet delimiter (see 35.2.3.6), once the duration of the CarrierEvent is greater than or equal to slotTime.

30.2.3 Containment

A containment relationship is a structuring relationship for managed objects in which the existence of a managed object is dependent on the existence of a containing managed object. The contained managed object is said to be the subordinate managed object, and the containing managed object the superior managed object. The containment relationship is used for naming managed objects. The local containment relationships among object classes are depicted in the entity relationship diagram, Figure 30–3. This figure shows the names of the object classes and whether a particular containment relationship is one-to-one or one-to-many. For further requirements on this topic, see IEEE Std 802.1F-1993.

MAU management is only valid in a system that provides management at the next higher containment level, that is, either a DTE or repeater with management.

30.2.4 Naming

The name of an individual managed object is hierarchically defined within a managed system. For example, in the context of repeater management, a repeater port might be identified as “repeater 3, group 01, port 13,” that is, port 13 of group 01 of a repeater with repeaterID 3 within the managed system.

In the case of MAU management, this will present itself in one of the two forms that are appropriate for a MAU’s use, that is, as associated with a CSMA/CD interface of a DTE or with a particular port of a managed repeater. For example, a MAU could be identified as “repeater 3, group 01, port 13, MAU 1” or, that is, the MAU associated with port 13 of group 01 of a repeater with repeaterID 3 within the managed system. Examples of this are represented in the relationship of the naming attributes in the entity relationship diagram, Figure 30–3.

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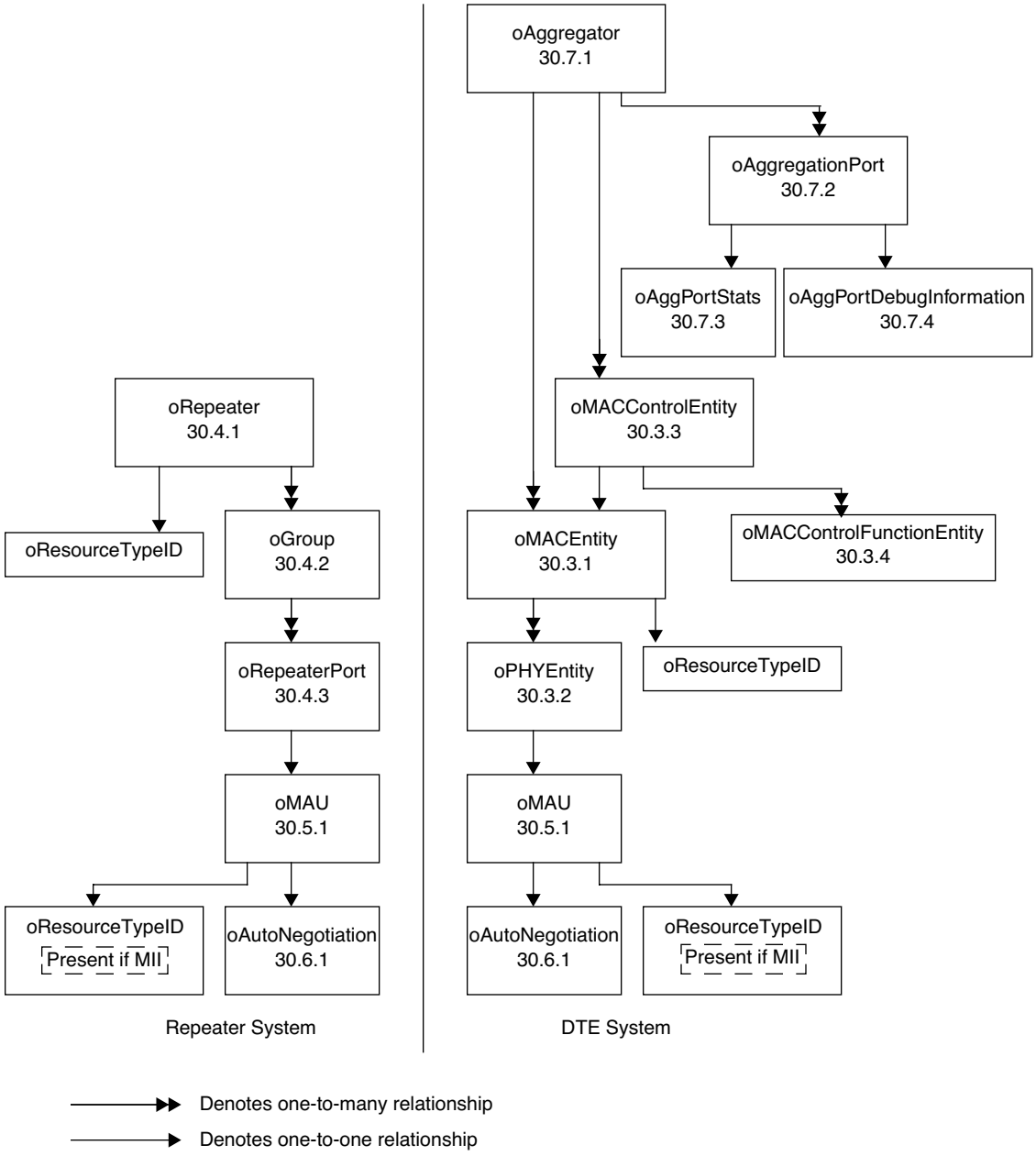


Figure 30–3—10/100/1000 Mb/s MAC, Control, and Link Aggregation entity relationship diagram

30.2.5 Capabilities

This standard makes use of the concept of *packages,* as defined in ISO/IEC 10165-4: 1992, as a means of grouping behavior, attributes, actions, and notifications within a managed object class definition. Packages may be either mandatory or conditional, that is to say, present if a given condition is true. Within this standard *capabilities* are defined, each of which corresponds to a set of packages that are components of a number of managed object class definitions and that share the same condition for presence. Implementation of the appropriate basic and mandatory packages is the minimum requirement for claiming conformance to

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IEEE 802.3 10 Mb/s, 100 Mb/s, 1000 Mb/s, MAC Control, and Link Aggregation Management. Implementation of an entire optional capability is required in order to claim conformance to that capability. The capabilities and packages for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Management are specified in Table 30–1a, Table 30–1b, Table 30–1c, Table 30–1d, and Table 30–1e. The capabilities and packages for Link Aggregation Management are specified in Table 30–2.

DTE Management has two packages that are required for management at the minimum conformance configuration—the Basic Package and the Mandatory Package. Systems that implement the optional MAC Control sublayer shall also implement the Basic and Mandatory Packages for the MAC Control Entity managed object class to claim DTE minimum conformance. For systems that include multiple PHY entities per MAC entity and implement the Multiple PHY Package to manage the selection of the active PHY, the optional Recommended Package shall be implemented. Systems that implement the optional Link Aggregation sublayer shall also implement the Basic and Mandatory Packages for the Aggregator and Aggregation Port managed object class to claim minimum DTE conformance.

For managed MAUs, the Basic Package is mandatory; all other packages are optional. For a managed MAU to be conformant to this standard, it shall fully implement the Basic Package. For a MAU to be conformant to an optional package it shall implement that entire package. While nonconformant (reference aMAUType = “other”) MAUs may utilize some or all of this clause to specify their management, conformance to this clause requires both a conformant MAU and conformant management. MAU Management is optional with respect to all other CSMA/CD Management. If an MII is present then the conditional MII Capability must be implemented. This provides the means to identify the vendor and type of the externally connected device.

There are two distinct aspects of Repeater Management.

The first aspect provides the means to monitor and control the functions of a repeater. These functions include, but are not limited to: identifying a repeater, testing and initializing a repeater, and enabling/disabling a port. This is encompassed by the mandatory Basic Control Capability.

The second aspect provides the means to monitor traffic from attached segments, and to measure traffic sourced by DTEs connected to these segments. This is done by gathering statistics on packets that enter a repeater and maintaining those statistics on a per port basis. This is encompassed by the optional Performance Monitor Capability. The optional Address Tracking Capability provides the means to identify existence and movement of attached DTEs by their MAC addresses. While nonconformant (reference aRepeaterType = “other”) repeaters may utilize some or all of this clause to specify their management, conformance to this clause requires both a conformant repeater and conformant management.

If link Auto-Negotiation is present and managed, the Auto-Negotiation managed object class shall be implemented in its entirety. All attributes and actions are mandatory.

The 1000 Mb/s Burst Monitor Capability provides additional attributes that relate only to 1000 Mb/s operation, while the 100 Mb/s Monitor Capability has attributes that apply to a mixed 100 and 1000 Mb/s operation. These attributes are provided to complement the counter attributes of the optional packages and capabilities that apply to 10 Mb/s and mixed 10, 100, and 1000 Mb/s implementations. It is recommended that when the 100/1000 Mb/s Monitor Capability or 1000 Mb/s Burst Monitor Capability is implemented, the appropriate complementary counter packages and capabilities are also implemented.

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Table 30–1a—Capabilities

				DTE								Repeater					MAU						
				Basic Package (Mandatory)	Mandatory Package (Mandatory)	Recommended Package (Optional)	Optional Package (Optional)	Array Package (Optional)	Excessive Deferral Package (Optional)	Multiple PHY Package (Optional)	100/1000 Mb/s Monitor Capability (Optional)	Basic Control Capability (Mandatory)	Performance Monitor Capability (Optional)	Address Tracking Capability (Optional)	100/1000 Mb/s Monitor Capability (Optional)	1000 Mb/s Burst Monitor Capability (Optional)	Basic Package (Mandatory)	MAU Control Package (Optional)	Media Loss Tracking Package (Conditional)	Broadband DTE MAU Package (Conditional)	MII Capability (Conditional)	100/1000 Mb/s Monitor Capability (Optional)	Auto-Negotiation Package (Mandatory)
oResourceTypeID managed object																							
	aResourceTypeIDName	ATTRIBUTE	GET	X								X									X		
	aResourceInfo	ATTRIBUTE	GET	X								X									X		
oMACEntity managed object class (30.3.1)																							
	aMACID	ATTRIBUTE	GET	X																			
	aFramesTransmittedOK	ATTRIBUTE	GET		X																		
	aSingleCollisionFrames	ATTRIBUTE	GET		X																		
	aMultipleCollisionFrames	ATTRIBUTE	GET		X																		
	aFramesReceivedOK	ATTRIBUTE	GET		X																		
	aFrameCheckSequenceErrors	ATTRIBUTE	GET		X																		
	aAlignmentErrors	ATTRIBUTE	GET		X																		
	aOctetsTransmittedOK	ATTRIBUTE	GET			X																	
	aFramesWithDeferredXmissions	ATTRIBUTE	GET			X																	
	aLateCollisions	ATTRIBUTE	GET			X																	
	aFramesAbortedDueToXSColls	ATTRIBUTE	GET			X																	
	aFramesLostDueToIntMACXmitError	ATTRIBUTE	GET			X																	
	aCarrierSenseErrors	ATTRIBUTE	GET			X																	
	aOctetsReceivedOK	ATTRIBUTE	GET			X																	
	aFramesLostDueToIntMACRcvError	ATTRIBUTE	GET			X																	
	aPromiscuousStatus	ATTRIBUTE	GET-SET			X																	
	aReadMulticastAddressList	ATTRIBUTE	GET			X																	
	aMulticastFramesXmittedOK	ATTRIBUTE	GET				X																
	aBroadcastFramesXmittedOK	ATTRIBUTE	GET				X																
	aFramesWithExcessiveDeferral	ATTRIBUTE	GET						X														
	aMulticastFramesReceivedOK	ATTRIBUTE	GET				X																
	aBroadcastFramesReceivedOK	ATTRIBUTE	GET				X																
	aInRangeLengthErrors	ATTRIBUTE	GET				X																
	aOutOfRangeLengthField	ATTRIBUTE	GET				X																
	aFrameTooLongErrors	ATTRIBUTE	GET				X																
	aMACEnableStatus	ATTRIBUTE	GET-SET				X																

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Table 30–1b—Capabilities

				DTE								Repeater				MAU					
				Basic Package (Mandatory)	Mandatory Package (Mandatory)	Recommended Package (Optional)	Optional Package (Optional)	Array Package (Optional)	Excessive Deferral Package (Optional)	Multiple PHY Package (Optional)	100/1000 Mb/s Monitor Capability (Optional)	Basic Control Capability (Mandatory)	Performance Monitor Capability (Optional)	Address Tracking Capability (Optional)	T00/1000 Mb/s Monitor Capability (Optional)	1000 Mb/s Burst Monitor Capability (Optional)	Basic Package (Mandatory)	MAU Control Package (Optional)	Media Loss Tracking Package (Conditional)	Broadband DTE MAU Package (Conditional)	MII Capability (Conditional)	100/1000 Mb/s Monitor Capability (Optional)	Auto-Negotiation Package (Mandatory)
oMACEntity managed object class (con'd.)																						
	aTransmitEnableStatus	ATTRIBUTE	GET-SET				X															
	aMulticastReceiveStatus	ATTRIBUTE	GET-SET				X															
	aReadWriteMACAddress	ATTRIBUTE	GET-SET				X															
	aCollisionFrames	ATTRIBUTE	GET					X														
	aMACCapabilities	ATTRIBUTE	GET		X[1]	X																
	aDuplexStatus	ATTRIBUTE	GET-SET		X[1]	X																
	acInitializeMAC	ACTION		X																		
	acAddGroupAddress	ACTION				X																
	acDeleteGroupAddress	ACTION				X																
	acExecuteSelfTest	ACTION					X															
oPHYEntity managed object class (30.3.2)																						
	aPHYID	ATTRIBUTE	GET	X																		
	aPHYType	ATTRIBUTE	GET	X																		
	aPHYTypeList	ATTRIBUTE	GET	X																		
	aSQETestErrors	ATTRIBUTE	GET			X																
	aSymbolErrorDuringCarrier	ATTRIBUTE	GET								X											
	aMIIDetect	ATTRIBUTE	GET	X																		
	aPHYAdminState	ATTRIBUTE	GET	X																		
	acPHYAdminControl	ACTION								X												
oMACControlEntity managed object class (30.3.3)																						
	aMACControlID	ATTRIBUTE	GET		X																	
	aMACControlFunctionsSupported	ATTRIBUTE	GET-SET		X																	
	aMACControlFramesTransmitted	ATTRIBUTE	GET			X																
	aMACControlFramesReceived	ATTRIBUTE	GET			X																
	aUnsupportedOpcodesReceived	ATTRIBUTE	GET			X																

NOTE 1: The aMACCapailities and aDuplexStatus attributes are Mandatory in systems that can operate in full duplex mode. They are Recommended in systems that can operate only in half duplex mode.

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Table 30–1c—Capabilities

			DTE								Repeater					MAU					
			Basic Package (Mandatory)	Mandatory Package (Mandatory)	Recommended Package (Optional)	Optional Package (Optional)	Array Package (Optional)	Excessive Deferral Package (Optional)	Multiple PHY Package (Optional)	100/1000 Mb/s Monitor Capability (Optional)	Basic Control Capability (Mandatory)	Performance Monitor Capability (Optional)	Address Tracking Capability (Optional)	100/1000 Mb/s Monitor Capability (Optional)	1000 Mb/s Burst Monitor Capability (Optional)	Basic Package (Mandatory)	MAU Control Package (Optional)	Media Loss Tracking Package (Conditional)	Broadband DTE MAU Package (Conditional)	MII Capability (Conditional)	100/1000 Mb/s Monitor Capability (Optional)	Auto-Negotiation Package (Mandatory)
oPAUSEEntity managed object class (instance of oMACControlFunctionEntity) (30.3.4)																					
aPAUSELinkDelayAllowance	ATTRIBUTE	GET-SET		X																	
aPAUSEMACCtrlFramesTransmitted	ATTRIBUTE	GET			X																
aPAUSEMACCtrlFramesReceived	ATTRIBUTE	GET			X																
oRepeater managed object class (30.4.1)																					
aRepeaterID	ATTRIBUTE	GET									X										
aRepeaterType	ATTRIBUTE	GET									X										
aRepeaterGroupCapacity	ATTRIBUTE	GET									X										
aGroupMap	ATTRIBUTE	GET									X										
aRepeaterHealthState	ATTRIBUTE	GET									X										
aRepeaterHealthText	ATTRIBUTE	GET									X										
aRepeaterHealthData	ATTRIBUTE	GET									X										
aTransmitCollisions	ATTRIBUTE	GET										X									
acResetRepeater	ACTION										X										
acExecuteNonDisruptiveSelfTest	ACTION										X										
nRepeaterHealth	NOTIFICATION										X										
nRepeaterReset	NOTIFICATION										X										
nGroupMapChange	NOTIFICATION										X										
oGroup managed object class (30.4.2)																					
aGroupID	ATTRIBUTE	GET									X										
aGroupPortCapacity	ATTRIBUTE	GET									X										
aPortMap	ATTRIBUTE	GET									X										
nPortMapChange	NOTIFICATION										X										

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Table 30–1d—Capabilities

				DTE							Repeater					MAU						
				Basic Package (Mandatory)	Mandatory Package (Mandatory)	Recommended Package (Optional)	Optional Package (Optional)	Array Package (Optional)	Excessive Deferral Package (Optional)	Multiple PHY Package (Optional)	100/1000 Mb/s Monitor Capability (Optional)	Basic Control Capability (Mandatory)	Performance Monitor Capability (Optional)	Address Tracking Capability (Optional)	100/1000 Mb/s Monitor Capability (Optional)	1000 Mb/s Burst Monitor Capability (Optional)	Basic Package (Mandatory)	MAU Control Package (Optional)	Media Loss Tracking Package (Conditional)	Broadband DTE MAU Package (Conditional)	MII Capability (Conditional)	100/1000 Mb/s Monitor Capability (Optional)	Auto-Negotiation Package (Mandatory)
oRepeaterPort managed object class (30.4.3)																							
	aPortID	ATTRIBUTE	GET									X											
	aPortAdminState	ATTRIBUTE	GET									X											
	aAutoPartitionState	ATTRIBUTE	GET									X											
	aReadableFrames	ATTRIBUTE	GET										X										
	aReadableOctets	ATTRIBUTE	GET										X										
	aFrameCheckSequenceErrors	ATTRIBUTE	GET										X										
	aAlignmentErrors	ATTRIBUTE	GET										X										
	aFramesTooLong	ATTRIBUTE	GET										X										
	aShortEvents	ATTRIBUTE	GET										X										
	aRunts	ATTRIBUTE	GET										X										
	aCollisions	ATTRIBUTE	GET										X										
	aLateEvents	ATTRIBUTE	GET										X										
	aVeryLongEvents	ATTRIBUTE	GET										X										
	aDataRateMismatches	ATTRIBUTE	GET										X										
	aAutoPartitions	ATTRIBUTE	GET										X										
	aIsolates	ATTRIBUTE	GET												X								
	aSymbolErrorDuringPacket	ATTRIBUTE	GET												X								
	aLastSourceAddress	ATTRIBUTE	GET											X									
	aSourceAddressChanges	ATTRIBUTE	GET											X									
	aBursts	ATTRIBUTE	GET													X							
	acPortAdminControl	ACTION										X											

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Table 30–1e—Capabilities

			DTE								Repeater					MAU							
			Basic Package (Mandatory)	Mandatory Package (Mandatory)	Recommended Package (Optional)	Optional Package (Optional)	Array Package (Optional)	Excessive Deferral Package (Optional)	Multiple PHY Package (Optional)	100/1000 Mb/s Monitor Capability (Optional)	Basic Control Capability (Mandatory)	Performance Monitor Capability (Optional)	Address Tracking Capability (Optional)	100/1000 Mb/s Monitor Capability (Optional)	1000 Mb/s Burst Monitor Capability (Optional)	Basic Package (Mandatory)	MAU Control Package (Optional)	Media Loss Tracking Package (Conditional)	Broadband DTE MAU Package (Conditional)	MII Capability (Conditional)	100/1000 Mb/s Monitor Capability (Optional)	Auto-Negotiation Package (Mandatory)
oMAU managed object class (30.5.1)																							
aMAUID	ATTRIBUTE	GET														X							
aMAUType	ATTRIBUTE	GET-SET														X							
aMAUTypeList	ATTRIBUTE	GET														X							
aMediaAvailable	ATTRIBUTE	GET														X							
aLoseMediaCounter	ATTRIBUTE	GET																X					
aJabber	ATTRIBUTE	GET														X							
aMAUAdminState	ATTRIBUTE	GET														X							
aBbMAUXmitRcvSplitType	ATTRIBUTE	GET																	X				
aBroadbandFrequencies	ATTRIBUTE	GET																	X				
aFalseCarriers	ATTRIBUTE	GET																			X		
aIdleErrorCount	ATTRIBUTE	GET																			X		
acResetMAU	ACTION																X						
acMAUAdminControl	ACTION																X						
nJabber	NOTIFICATION															X							
oAuto-Negotiation managed object class (30.6.1)																							
aAutoNegID	ATTRIBUTE	GET																					X
aAutoNegAdminState	ATTRIBUTE	GET																					X
aAutoNegRemoteSignaling	ATTRIBUTE	GET																					X
aAutoNegAutoConfig	ATTRIBUTE	GET-SET																					X
aAutoNegLocalTechnologyAbility	ATTRIBUTE	GET																					X
aAutoNegAdvertisedTechnologyAbility	ATTRIBUTE	GET-SET																					X
aAutoNegReceivedTechnologyAbility	ATTRIBUTE	GET																					X
aAutoNegLocalSelectorAbility	ATTRIBUTE	GET																					X
aAutoNegAdvertisedSelectorAbility	ATTRIBUTE	GET-SET																					X
aAutoNegReceivedSelectorAbility	ATTRIBUTE	GET																					X
acAutoNegRestartAutoConfig	ACTION																						X
acAutoNegAdminControl	ACTION																						X
Common Attributes Template																							
aCMCounter	ATTRIBUTE	GET		X	X	X		X		X		X	X	X			X	X			X		

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Table 30–2—Link Aggregation Capabilities

				DTE					
	Object Name	**Object Type**	**Operations Supported**	**Basic Package (Mandatory)**	**Mandatory Package (Mandatory)**	**Recommended Package (Optional)**	**Optional Package (Optional)**	**Aggregation Port Statistics (Optional)**	**Aggregation Port Debug Information (Optional)**
oAggregator (30.7.1)									
	aAggID	ATTRIBUTE	GET	X					
	aAggDescription	ATTRIBUTE	GET		X				
	aAggName	ATTRIBUTE	GET-SET		X				
	aAggActorSystemID	ATTRIBUTE	GET-SET		X				
	aAggActorSystemPriority	ATTRIBUTE	GET-SET		X				
	aAggAggregateOrIndividual	ATTRIBUTE	GET		X				
	aAggActorAdminKey	ATTRIBUTE	GET-SET		X				
	aAggActorOperKey	ATTRIBUTE	GET		X				
	aAggMACAddress	ATTRIBUTE	GET		X				
	aAggPartnerSystemID	ATTRIBUTE	GET		X				
	aAggPartnerSystemPriority	ATTRIBUTE	GET		X				
	aAggPartnerOperKey	ATTRIBUTE	GET		X				
	aAggAdminState	ATTRIBUTE	GET-SET		X				
	aAggOperState	ATTRIBUTE	GET		X				
	aAggTimeOfLastOperChange	ATTRIBUTE	GET		X				
	aAggDataRate	ATTRIBUTE	GET		X				
	aAggOctetsTxOK	ATTRIBUTE	GET			X			
	aAggOctetsRxOK	ATTRIBUTE	GET			X			
	aAggFramesTxOK	ATTRIBUTE	GET		X				
	aAggFramesRxOK	ATTRIBUTE	GET		X				
	aAggMulticastFramesTxOK	ATTRIBUTE	GET				X		
	aAggMulticastFramesRxOK	ATTRIBUTE	GET				X		
	aAggBroadcastFramesTxOK	ATTRIBUTE	GET				X		
	aAggBroadcastFramesRxOK	ATTRIBUTE	GET				X		
	aAggFramesDiscardedOnTx	ATTRIBUTE	GET			X			

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Table 30–2—Link Aggregation Capabilities *(continued)*

				DTE					
	Object Name	**Object Type**	**Operations Supported**	**Basic Package (Mandatory)**	**Mandatory Package (Mandatory)**	**Recommended Package (Optional)**	**Optional Package (Optional)**	**Aggregation Port Statistics (Optional)**	**Aggregation Port Debug Information (Optional)**
	aAggFramesDiscardedOnRx	ATTRIBUTE	GET			X			
	aAggFramesWithTxErrors	ATTRIBUTE	GET			X			
	aAggFramesWithRxErrors	ATTRIBUTE	GET			X			
	aAggUnknownProtocolFrames	ATTRIBUTE	GET			X			
	aAggLinkUpDownNotificationEnable	ATTRIBUTE	GET-SET		X				
	nAggLinkUpNotification	NOTIFICATION			X				
	nAggLinkDownNotification	NOTIFICATION			X				
	aAggPortList	ATTRIBUTE	GET			X			
	aAggCollectorMaxDelay	ATTRIBUTE	GET-SET		X				
oAggregationPort (30.7.2)									
	aAggPortID	ATTRIBUTE	GET	X					
	aAggPortActorSystemPriority	ATTRIBUTE	GET-SET		X				
	aAggPortActorSystemID	ATTRIBUTE	GET		X				
	aAggPortActorAdminKey	ATTRIBUTE	GET-SET		X				
	aAggPortActorOperKey	ATTRIBUTE	GET		X				
	aAggPortPartnerAdminSystemPriority	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerOperSystemPriority	ATTRIBUTE	GET		X				
	aAggPortPartnerAdminSystemID	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerOperSystemID	ATTRIBUTE	GET		X				
	aAggPortPartnerAdminKey	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerOperKey	ATTRIBUTE	GET		X				
	aAggPortSelectedAggID	ATTRIBUTE	GET		X				
	aAggPortAttachedAggID	ATTRIBUTE	GET		X				
	aAggPortActorPort	ATTRIBUTE	GET		X				
	aAggPortActorPortPriority	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerAdminPort	ATTRIBUTE	GET-SET		X				

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Table 30–2—Link Aggregation Capabilities *(continued)*

				DTE					
	Object Name	**Object Type**	**Operations Supported**	**Basic Package (Mandatory)**	**Mandatory Package (Mandatory)**	**Recommended Package (Optional)**	**Optional Package (Optional)**	**Aggregation Port Statistics (Optional)**	**Aggregation Port Debug Information (Optional)**
	aAggPortPartnerOperPort	ATTRIBUTE	GET		X				
	aAggPortPartnerAdminPortPriority	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerOperPortPriority	ATTRIBUTE	GET		X				
	aAggPortActorAdminState	ATTRIBUTE	GET-SET		X				
	aAggPortActorOperState	ATTRIBUTE	GET		X				
	aAggPortPartnerAdminState	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerOperState	ATTRIBUTE	GET		X				
	aAggPortAggregateOrIndividual	ATTRIBUTE	GET		X				
oAggPortStats (30.7.3)									
	aAggPortStatsID	ATTRIBUTE	GET					X	
	aAggPortStatsLACPDUsRx	ATTRIBUTE	GET					X	
	aAggPortStatsMarkerPDUsRx	ATTRIBUTE	GET					X	
	aAggPortStatsMarkerResponsePDUsRx	ATTRIBUTE	GET					X	
	aAggPortStatsUnknownRx	ATTRIBUTE	GET					X	
	aAggPortStatsIllegalRx	ATTRIBUTE	GET					X	
	aAggPortStatsLACPDUsTx	ATTRIBUTE	GET					X	
	aAggPortStatsMarkerPDUsTx	ATTRIBUTE	GET					X	
	aAggPortStatsMarkerResponsePDUsTx	ATTRIBUTE	GET					X	
oAggPortDebugInformation (30.7.4)									
	aAggPortDebugInformationID	ATTRIBUTE	GET						X
	aAggPortDebugRxState	ATTRIBUTE	GET						X
	aAggPortDebugLastRxTime	ATTRIBUTE	GET						X
	aAggPortDebugMuxState	ATTRIBUTE	GET						X
	aAggPortDebugMuxReason	ATTRIBUTE	GET						X
	aAggPortDebugActorChurnState	ATTRIBUTE	GET						X
	aAggPortDebugPartnerChurnState	ATTRIBUTE	GET						X

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Table 30–2—Link Aggregation Capabilities *(continued)*

				DTE					
	Object Name	**Object Type**	**Operations Supported**	**Basic Package (Mandatory)**	**Mandatory Package (Mandatory)**	**Recommended Package (Optional)**	**Optional Package (Optional)**	**Aggregation Port Statistics (Optional)**	**Aggregation Port Debug Information (Optional)**
	aAggPortDebugActorChurnCount	ATTRIBUTE	GET						X
	aAggPortDebugPartnerChurnCount	ATTRIBUTE	GET						X
	aAggPortDebugActorSyncTransitionCount	ATTRIBUTE	GET						X
	aAggPortDebugPartnerSyncTransitionCount	ATTRIBUTE	GET						X
	aAggPortDebugActorChangeCount	ATTRIBUTE	GET						X
	aAggPortDebugPartnerChangeCount	ATTRIBUTE	GET						X
Common Attributes Template									
	aCMCounter	ATTRIBUTE	GET		X	X	X	X	X

30.3 Layer management for DTEs

30.3.1 MAC entity managed object class

This subclause formally defines the behaviours for the oMACEntity managed object class attributes, actions, and notifications.

30.3.1.1 MAC entity attributes

30.3.1.1.1 aMACID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aMACID is assigned so as to uniquely identify a MAC among the subordinate managed objects of the containing object.;

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30.3.1.1.2 aFramesTransmittedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that are successfully transmitted. This counter is incremented when the TransmitStatus is reported as transmitOK. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).;

30.3.1.1.3 aSingleCollisionFrames

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 13 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that are involved in a single collision, and are subsequently transmitted successfully. This counter is incremented when the result of a transmission is reported as transmitOK and the attempt value is 2. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.4 aMultipleCollisionFrames

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 11 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that are involved in more than one collision and are subsequently transmitted successfully. This counter is incremented when the TransmitStatus is reported as transmitOK and the value of the attempts variable is greater than 2 and less or equal to attemptLimit. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.5 aFramesReceivedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that are successfully received (receiveOK). This does not include frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented when the ReceiveStatus is reported as receiveOK. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.6 aFrameCheckSequenceErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

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Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of receive frames that are an integral number of octets in length and do not pass the FCS check. This does not include frames received with frame-too-long, or frame-too-short (frame fragment) error. This counter is incremented when the ReceiveStatus is reported as frameCheckError. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

NOTE—Coding errors detected by the physical layer for speeds above 10 Mb/s will cause the frame to fail the FCS check.;

30.3.1.1.7 aAlignmentErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that are not an integral number of octets in length and do not pass the FCS check. This counter is incremented when the ReceiveStatus is reported as alignmentError. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3). This counter will not increment for 8 bit wide group encoding schemes.;

30.3.1.1.8 aOctetsTransmittedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 230 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of data and padding octets of frames that are successfully transmitted. This counter is incremented when the TransmitStatus is reported as transmitOK. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).;

30.3.1.1.9 aFramesWithDeferredXmissions

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 13 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames whose transmission was delayed on its first attempt because the medium was busy. This counter is incremented when the Boolean variable deferred has been asserted by the TransmitLinkMgmt function (4.2.8). Frames involved in any collisions are not counted. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.10 aLateCollisions

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

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BEHAVIOUR DEFINED AS:

A count of the times that a collision has been detected later than one slotTime from the start of the packet transmission. A late collision is counted twice, i.e., both as a collision and as a lateCollision. This counter is incremented when the lateCollisionCount variable is nonzero. The actual update is incremented in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.11 aFramesAbortedDueToXSColls

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 3255 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of the frames that, due to excessive collisions, are not transmitted successfully. This counter is incremented when the value of the attempts variable equals attemptLimit during a transmission. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2.). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.12 aFramesLostDueToIntMACXmitError

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that would otherwise be transmitted by the station, but could not be sent due to an internal MAC sublayer transmit error. If this counter is incremented, then none of the other counters in this section are incremented. The exact meaning and mechanism for incrementing this counter is implementation dependent.;

30.3.1.1.13 aCarrierSenseErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of times that the carrierSense variable was not asserted or was deasserted during the transmission of a frame without collision. This counter is incremented when the carrierSenseFailure flag is true at the end of transmission. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.14 aOctetsReceivedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 230 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of data and padding octets in frames that are successfully received. This does not include octets in frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented when the result of a reception is

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reported as a receiveOK status. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.15 aFramesLostDueToIntMACRcvError

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A count of frames that would otherwise be received by the station, but could not be accepted due to an internal MAC sublayer receive error. If this counter is incremented, then none of the other counters in this section are incremented. The exact meaning and mechanism for incrementing this counter is implementation dependent.;

30.3.1.1.16 aPromiscuousStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET operation returns the value “true” for promiscuous mode enabled, and “false” otherwise.

Frames without errors received solely because this attribute has the value “true” are counted as frames received correctly; frames received in this mode that do contain errors update the appropriate error counters.

A SET operation to the value “true” provides a means to cause the LayerMgmtRecognizeAddress function to accept frames regardless of their destination address.

A SET operation to the value “false” causes the MAC sublayer to return to the normal operation of carrying out address recognition procedures for station, broadcast, and multicast group addresses (LayerMgmtRecognizeAddress function).;

30.3.1.1.17 aReadMulticastAddressList

ATTRIBUTE

APPROPRIATE SYNTAX:
SEQUENCE OF MAC addresses

BEHAVIOUR DEFINED AS:
The current multicast address list.;

30.3.1.1.18 aMulticastFramesXmittedOK

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A count of frames that are successfully transmitted, as indicated by the status value transmitOK, to a group destination address other than broadcast. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).;

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30.3.1.1.19 aBroadcastFramesXmittedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of the frames that were successfully transmitted as indicated by the TransmitStatus transmitOK, to the broadcast address. Frames transmitted to multicast addresses are not broadcast frames and are excluded. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).;

30.3.1.1.20 aFramesWithExcessiveDeferral

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 412 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that deferred for an excessive period of time. This counter may only be incremented once per LLC transmission. This counter is incremented when the excessDefer flag is set. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.21 aMulticastFramesReceivedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that are successfully received and are directed to an active nonbroadcast group address. This does not include frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented as indicated by the receiveOK status, and the value in the destinationField. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.22 aBroadcastFramesReceivedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that are successfully received and are directed to the broadcast group address. This does not include frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented as indicated by the receiveOK status, and the value in the destinationField. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.23 aInRangeLengthErrors

ATTRIBUTE

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APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames with a length/type field (see 3.2.6[12]) value between the minimum unpadded MAC client data size and the maximum allowed MAC client data size, inclusive, that does not match the number of MAC client data octets received. The counter also increments for frames whose length/type field value is less than the minimum allowed unpadded MAC client data size and the number of MAC client data octets received is greater than the minimum unpadded MAC client data size. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.24 aOutOfRangeLengthField

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames with a length field value greater than the maximum allowed LLC data size. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

NOTE—In the past, this counter was incremented by frames containing "Type" fields. Due to the modification to legitimize "Type" fields, such frames will now increment aFramesReceivedOK and this counter will not increment.;

30.3.1.1.25 aFrameTooLongErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 815 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames received that exceed the maximum permitted frame size. This counter is incremented when the status of a frame reception is frameTooLong. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

NOTE—Implementations may use either maxUntaggedFrameSize or (maxUntaggedFrameSize + qTagPrefixSize) (see 4.2.7.1 and 4.4.2) for the maximum permitted frame size, either as a constant or as a function of whether the frame received is a basic or tagged frame (see 3.2 and 3.5). In implementations that treat this as a constant it is recommended that the larger value be used. The use of any value other than the larger value in this case may result in the counter being incremented by valid tagged frames.;

30.3.1.1.26 aMACEnableStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

True if MAC sublayer is enabled and false if disabled. This is accomplished by setting or checking the values of the receiveEnabled and transmitEnabled variables. Setting to true provides a means to cause the MAC sublayer to enter the normal operational state at idle. The PLS is reset by this operation (see 7.2.2.2.1). This is accomplished by setting receiveEnabled and transmitEnabled to true.
Setting to false causes the MAC sublayer to end all transmit and receive operations, leaving it in a

[12]The"Type" interpretation of this field was added to the standard by IEEE Std 802.3x-1997.

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disabled state. This is accomplished by setting receiveEnabled and transmitEnabled to false.;

30.3.1.1.27 aTransmitEnableStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
True if transmission is enabled and false otherwise. This is accomplished by setting or checking the value of the transmitEnabled variable.
Setting this to true provides a means to enable MAC sublayer frame transmission (TransmitFrame function). This is accomplished by setting transmitEnabled to true.
Setting this to false will inhibit the transmission of further frames by the MAC sublayer (TransmitFrame function). This is accomplished by setting transmitEnabled to false.;

30.3.1.1.28 aMulticastReceiveStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
True if multicast receive is enabled, and false otherwise. Setting this to true provides a means to cause the MAC sublayer to return to the normal operation of multicast frame reception. Setting this to false will inhibit the reception of further multicast frames by the MAC sublayer.;

30.3.1.1.29 aReadWriteMACAddress

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
Read the MAC station address or change the MAC station address to the one supplied (RecognizeAddress function). Note that the supplied station address shall not have the group bit set and shall not be the null address.;

30.3.1.1.30 aCollisionFrames

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of 32 generalized nonresettable counters. Each counter has a maximum increment rate of 13 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A histogram of collision activity. The indices of this array (1 to attemptLimit – 1) denote the number of collisions experienced in transmitting a frame. Each element of this array contains a counter that denotes the number of frames that have experienced a specific number of collisions. When the TransmitStatus is reported as transmitOK and the value of the attempts variable equals n, then collisionFrames[n–1] counter is incremented. The elements of this array are incremented in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.31 aMACCapabilities

ATTRIBUTE

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APPROPRIATE SYNTAX:

A SEQUENCE that meets the requirements of the description below:

half duplex	Capable of operating in half duplex mode
full duplex	Capable of operating in full duplex mode

BEHAVIOUR DEFINED AS:

This indicates the capabilities of the MAC.;

30.3.1.1.32 aDuplexStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

half duplex	Half duplex mode
full duplex	Full duplex mode
unknown	Duplex status unknown

BEHAVIOUR DEFINED AS:

A GET operation returns the current mode of operation of the MAC entity, either half duplex, full duplex, or unknown.

A SET operation changes the mode of operation of the MAC entity to the indicated value. A SET operation shall have no effect on a device whose mode cannot be changed through management or that can only operate in a single mode.;

30.3.1.2 MAC entity actions

30.3.1.2.1 acInitializeMAC

ACTION

APPROPRIATE SYNTAX:

None required

BEHAVIOUR DEFINED AS:

This action provides a means to call the Initialize procedure (4.2.7.5). This action also results in the initialization of the PLS.;

30.3.1.2.2 acAddGroupAddress

ACTION

APPROPRIATE SYNTAX:

MACAddress

BEHAVIOUR DEFINED AS:

Add the supplied multicast group address to the address recognition filter (RecognizeAddress function).;

30.3.1.2.3 acDeleteGroupAddress

ACTION

APPROPRIATE SYNTAX:

MACAddress

BEHAVIOUR DEFINED AS:

Delete the supplied multicast group address from the address recognition filter (RecognizeAddress function).;

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30.3.1.2.4 acExecuteSelfTest

ACTION

APPROPRIATE SYNTAX:
None required

BEHAVIOUR DEFINED AS:
Execute a self-test and report the results (success or failure). The actual mechanism employed to carry out the self-test is not defined in this standard. If a Clause 22 MII or Clause 35 GMII is present then this action shall also invoke a data integrity test using MII or GMII loopback, returning to normal operation on completion of the test.;

30.3.2 PHY devicePHY device managed object class

This subclause formally defines the behaviours for the oPHYEntity managed object class attributes, actions and notifications. Management of that portion of the physical sublayer whose physical containment within the DTE is optional is outside the scope of this clause.

30.3.2.1 PHY device attributes

30.3.2.1.1 aPHYID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aPHYID is assigned so as to uniquely identify a PHY, i.e., Physical Layer among the subordinate managed objects of system (systemID and system are defined in ISO/IEC 10165-2: 1992 [SMI], Definition of management information).;

30.3.2.1.2 aPhyType

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

other	Undefined
unknown	Initializing, true state or type not yet known
none	MII present and nothing connected
10 Mb/s	Clause 7 10 Mb/s Manchester
100BASE-T4	Clause 23 100 Mb/s 8B/6T
100BASE-X	Clause 24 100 Mb/s 4B/5B
100BASE-T2	Clause 32 100 Mb/s PAM5X5
1000BASE-X	Clause 36 1000 Mb/s 8B/10B
1000BASE-T	Clause 40 1000 Mb/s 4D-PAM5

BEHAVIOUR DEFINED AS:
A read-only value that identifies the PHY type. The enumeration of the type is such that the value matches the clause number of this International Standard that specifies the particular PHY. The value of this attribute maps to the value of aMAUType. The enumeration “none” can only occur in a standard implementation where an MII exists and there is nothing connected. However, the attribute aMIIDetect should be used to determine whether an MII exists or not.;

30.3.2.1.3 aPhyTypeList

ATTRIBUTE

APPROPRIATE SYNTAX:

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A SEQUENCE that meets the requirements of the description below:

other	Undefined
unknown	Initializing, true state or type not yet known
none	MII present and nothing connected
10 Mb/s	Clause 7 10 Mb/s Manchester
100BASE-T4	Clause 23 100 Mb/s 8B/6T
100BASE-X	Clause 24 100 Mb/s 4B/5B
100BASE-T2	Clause 32 100 Mb/s PAM5X5
1000BASE-X	Clause 36 1000 Mb/s 8B/10B
1000BASE-T	Clause 40 1000 Mb/s 4D-PAM5

BEHAVIOUR DEFINED AS:

A read-only list of the possible types that the PHY could be, identifying the ability of the PHY. If Clause 28 or Clause 37, Auto-Negotiation, is present, then this attribute will map to the local technology ability or advertised ability of the local device.;

30.3.2.1.4 aSQETestErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of times that the SQE_TEST_ERROR was received. The SQE_TEST_ERROR is set in accordance with the rules for verification of the SQE detection mechanism in the PLS Carrier Sense function (see 7.2.4.6). The SQE test function is not a part of 100 or 1000 Mb/s PHY operation, and so SQETestErrors will not occur in 100 or 1000 Mb/s PHYs. The contents of this attribute are undefined for full duplex operation.;

30.3.2.1.5 aSymbolErrorDuringCarrier

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 160 000 counts per second for 100 Mb/s implementations

BEHAVIOUR DEFINED AS:

For 100 Mb/s operation it is a count of the number of times when valid carrier was present and there was at least one occurrence of an invalid data symbol (see 23.2.1.4, 24.2.2.1.6, and 32.3.4.1).
For half duplex operation at 1000 Mb/s, it is a count of the number of times the receiving media is non-idle (a carrier event) for a period of time equal to or greater than slotTime (see 4.2.4), and during which there was at least one occurrence of an event that causes the PHY to indicate “Data reception error” or “Carrier Extend Error” on the GMII (see Table 35–2).
For full duplex operation at 1000 Mb/s, it is a count of the number of times the receiving media is non-idle (a carrier event) for a period of time equal to or greater than minFrameSize, and during which there was at least one occurrence of an event that causes the PHY to indicate “Data reception error” on the GMII (see Table 35–2). At all speeds this counter shall be incremented only once per valid CarrierEvent and if a collision is present this counter shall not increment.;

30.3.2.1.6 aMIIDetect

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
unknown
present, nothing connected

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present, connected
absent

BEHAVIOUR DEFINED AS:

An attribute of the PhyEntity managed object class indicating whether an MII connector is physically present, and if so whether it is detectably connected as specified in 22.2.2.12.;

30.3.2.1.7 aPhyAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries:
disabled
enabled

BEHAVIOUR DEFINED AS:

A disabled PHY neither transmits nor receives. The PHY shall be explicitly enabled to restore operation. The acPhyAdminControl action provides this ability. The port enable/disable function as reported by this attribute is preserved across DTE reset including loss of power. Only one PHY per MAC can be enabled at any one time. Setting a PHY to the enabled state using the action acPhyAdminControl will result in all other instances of PHY (indicated by PhyID) instantiated within the same MAC to be disabled. If a Clause 22 MII or Clause 35 GMII is present then setting this attribute to "disabled" will result in electrical isolation as defined in 22.2.4.1.6, Isolate; and setting this attribute to "enabled" will result in normal operation as defined in 22.2.4.1.5, Power down; and 22.2.4.1.6, Isolate.;

30.3.2.2 PHY device actions

30.3.2.2.1 acPhyAdminControl

ACTION

APPROPRIATE SYNTAX:

Same as aPortAdminState

BEHAVIOUR DEFINED AS:

This action provides a means to alter aPhyAdminState. Setting a PHY to the enabled state will result in all other instances of PHY being disabled.;

30.3.3 MAC control entity object class

This subclause formally defines the behaviours for the oMACControlEntity managed object class attributes.

30.3.3.1 aMACControlID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aMACControlID is assigned so as to uniquely identify a MAC Control entity among the subordinate managed objects of the containing object.;

30.3.3.2 aMACControlFunctionsSupported

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE that meets the requirements of the description below:

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PAUSE PAUSE command implemented

BEHAVIOUR DEFINED AS:

A read-write list of the possible MAC Control functions implemented within the device. Each function implemented will have an associated MAC Control Function Entity object class. Currently, the only function defined is the PAUSE command.;

30.3.3.3 aMACControlFramesTransmitted

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC Control frames passed to the MAC sublayer for transmission. This counter is incremented when a MA_CONTROL.request primitive is generated within the MAC Control sublayer.;

30.3.3.4 aMACControlFramesReceived

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC Control frames passed by the MAC sublayer to the MAC Control sublayer. This counter is incremented when a ReceiveFrame function call returns a valid frame with a lengthOrType field value equal to the reserved Type for 802.3_MAC_Control as specified in 31.4.1.3.;

30.3.3.5 aUnsupportedOpcodesReceived

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC Control frames received that contain an opcode from Table 31A–1 that is not supported by the device. This counter is incremented when a ReceiveFrame function call returns a valid frame with a lengthOrType field value equal to the reserved Type for 802.3_MAC_Control as specified in 31.4.1.3, and with an opcode for a function that is not supported by the device.;

30.3.4 PAUSE entity managed object class

This subclause formally defines the behaviours for the oPAUSEEntity managed object class attributes.

30.3.4.1 aPAUSELinkDelayAllowance

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

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A GET operation returns the value, in bits, of the allowance made by the PAUSE MAC Control entity for round-trip propagation delay of the full duplex link.
A SET operation changes the value of the allowance made by the PAUSE MAC Control entity for round-trip propagation delay of the full duplex link to the indicated value, in bits.;

30.3.4.2 aPAUSEMACCtrlFramesTransmitted

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A count of PAUSE frames passed to the MAC sublayer for transmission. This counter is incremented when a MA_CONTROL.request primitive is generated within the MAC Control sublayer with an opcode indicating the PAUSE operation.;

30.3.4.3 aPAUSEMACCtrlFramesReceived

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC Control frames passed by the MAC sublayer to the MAC Control sublayer. This counter is incremented when a ReceiveFrame function call returns a valid frame with: (1) a lengthOrType field value equal to the reserved Type for 802.3_MAC_Control as specified in 31.4.1.3, and (2) an opcode indicating the PAUSE operation.;

30.4 Layer management for 10, 100, and 1000 Mb/s baseband repeaters

30.4.1 Repeater managed object class

This subclause formally defines the behaviours for the oRepeater managed object class, attributes, actions, and notifications.

30.4.1.1 Repeater attributes

30.4.1.1.1 aRepeaterID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aRepeaterID is assigned so as to uniquely identify a repeater among the subordinate managed objects of system (systemID and system are defined in ISO/IEC 10165-2: 1992 [SMI], Definition of management information).;

30.4.1.1.2 aRepeaterType

ATTRIBUTE

APPROPRIATE SYNTAX:
An INTEGER that meets the requirements of the following description:

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9	10 Mb/s Baseband
271	100 Mb/s Baseband, Class I
272	100 Mb/s Baseband, Class II
41	1000 Mb/s Baseband
other	See 30.2.5
unknown	Initializing, true state or type not yet known

BEHAVIOUR DEFINED AS:

Returns a value that identifies the CSMA/CD repeater type. The enumeration of the type is such that the value matches the clause number of the standard that specifies the particular repeater, with further numerical identification for the repeater classes within the same clause.;

30.4.1.1.3 aRepeaterGroupCapacity

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The aRepeaterGroupCapacity is the number of groups that can be contained within the repeater. Within each managed repeater, the groups are uniquely numbered in the range from 1 to aRepeaterGroupCapacity.

Some groups may not be present in a given repeater instance, in which case the actual number of groups present is less than aRepeaterGroupCapacity. The number of groups present is never greater than aRepeaterGroupCapacity.;

30.4.1.1.4 aGroupMap

ATTRIBUTE

APPROPRIATE SYNTAX:

BITSTRING

BEHAVIOUR DEFINED AS:

A string of bits which reflects the current configuration of units that are viewed by group managed objects. The length of the bitstring is “aRepeaterGroupCapacity” bits. The first bit relates to group 1. A “1” in the bitstring indicates presence of the group, “0” represents absence of the group.;

30.4.1.1.5 aRepeaterHealthState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE LIST that has the following entries:

other	undefined or unknown
ok	no known failures
repeaterFailure	known to have a repeater related failure
groupFailure	known to have a group related failure
portFailure	known to have a port related failure
generalFailure	has a failure condition, unspecified type

BEHAVIOUR DEFINED AS:

The aRepeaterHealthState attribute indicates the operational state of the repeater. The aRepeaterHealthData and aRepeaterHealthText attributes may be consulted for more specific information about the state of the repeater’s health. In case of multiple kinds of failures (e.g., repeater failure and port failure), the value of this attribute shall reflect the highest priority in the following order:
repeater failure
group failure
port failure
general failure;

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30.4.1.1.6 aRepeaterHealthText

ATTRIBUTE

APPROPRIATE SYNTAX:
A PrintableString, 255 characters max

BEHAVIOUR DEFINED AS:
The aRepeaterHealthText attribute is a text string that provides information relevant to the operational state of the repeater. Repeater vendors may use this mechanism to provide detailed failure information or instructions for problem resolution.

The contents are vendor specific.;

30.4.1.1.7 aRepeaterHealthData

ATTRIBUTE

APPROPRIATE SYNTAX:
OCTET STRING, 0–255

BEHAVIOUR DEFINED AS:
The aRepeaterHealthData attribute is a block of data octets that provides information relevant to the operational state of the repeater. The encoding of this data block is vendor dependent. Repeater vendors may use this mechanism to provide detailed failure information or instructions for problem resolution.;

30.4.1.1.8 aTransmitCollisions

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
For a Clause 9 repeater, the counter increments every time the repeater state diagram enters the TRANSMIT COLLISION state from any state other than ONE PORT LEFT (Figure 9–2). For a Clause 27 repeater, the counter increments every time the Repeater Core state diagram enters the JAM state as a result of Activity(ALL) > 1 (Figure 27–2). For a Clause 41 repeater, the counter increments every time the Repeater Unit state diagram enters the JAM state (Figure 41–2).

NOTE—Some non-collision events such as false carriers will cause the repeater unit to enter the JAM state and increment this counter.;

30.4.1.2 Repeater actions

30.4.1.2.1 acResetRepeater

ACTION

APPROPRIATE SYNTAX:
None required

BEHAVIOUR DEFINED AS:
This causes a transition to the START state of Figure 9–2 for a Clause 9 repeater, to the START state of Figure 27–2 for a Clause 27 repeater, or to the START state of Figure 41–2 for a Clause 41 repeater. The repeater performs a disruptive self-test that has the following characteristics:

1. The components are not specified
2. The test resets the repeater but without affecting management information about the repeater
3. The test does not inject packets onto any segment
4. Packets received during the test may or may not be transferred

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5. The test does not interfere with management functions
This causes a nRepeaterReset notification to be sent.;

30.4.1.2.2 acExecuteNonDisruptiveSelfTest

ACTION

APPROPRIATE SYNTAX:
None required

BEHAVIOUR DEFINED AS:
The repeater performs a vendor-specific, non-disruptive self-test that has the following characteristics:
1. The components are not specified
2. The test does not change the state of the repeater or management information about the repeater
3. The test does not inject packets onto any segment
4. The test does not prevent the transfer of any packets
5. Completion of the test causes a nRepeaterHealth to be sent.;

30.4.1.3 Repeater notifications

30.4.1.3.1 nRepeaterHealth

NOTIFICATION

APPROPRIATE SYNTAX:
A SEQUENCE of three data types. The first is mandatory, the following two are optional. The first is the value of the attribute aRepeaterHealthState. The second is the value of the attribute aRepeaterHealthText. The third is the value of the attribute aRepeaterHealthData

BEHAVIOUR DEFINED AS:
This notification conveys information related to the operational state of the repeater. See the aRepeaterHealthState, aRepeaterHealthText, and aRepeaterHealthData attributes for descriptions of the information that is sent.

The nRepeaterHealth notification is sent only when the health state of the repeater changes. The nRepeaterHealth notification shall contain repeaterHealthState. repeaterHealthData and repeaterHealthText may or may not be included. The nRepeaterHealth notification is not sent as a result of powering up a repeater.;

30.4.1.3.2 nRepeaterReset

NOTIFICATION

APPROPRIATE SYNTAX:
A SEQUENCE of three data types. The first is mandatory, the following two are optional. The first is the value of the attribute aRepeaterHealthState. The second is the value of the attribute aRepeaterHealthText. The third is the value of the attribute aRepeaterHealthData

BEHAVIOUR DEFINED AS:
This notification conveys information related to the operational state of the repeater. The nRepeaterReset notification is sent when the repeater is reset as the result of a power-on condition or upon completion of the acResetRepeater action. The nRepeaterReset notification shall contain repeaterHealthState. repeaterHealthData and repeaterHealthText may or may not be included.;

30.4.1.3.3 nGroupMapChange

NOTIFICATION

APPROPRIATE SYNTAX:
BITSTRING

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BEHAVIOUR DEFINED AS:

This notification is sent when a change occurs in the group structure of a repeater. This occurs only when a group is logically removed from or added to a repeater. The nGroupMapChange notification is not sent when powering up a repeater. The value of the notification is the updated value of the aGroupMap attribute.;

30.4.2 Group managed object class

This subclause formally defines the behaviours for the oGroup managed object class, attributes, actions, and notifications.

30.4.2.1 Group attributes

30.4.2.1.1 aGroupID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A value unique within the repeater. The value of aGroupID is assigned so as to uniquely identify a group among the subordinate managed objects of the containing object (oRepeater). This value is never greater than aRepeaterGroupCapacity.;

30.4.2.1.2 aGroupPortCapacity

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The aGroupPortCapacity is the number of ports contained within the group. Valid range is 1–1024. Within each group, the ports are uniquely numbered in the range from 1 to aGroupPortCapacity. Some ports may not be present in a given group instance, in which case the actual number of ports present is less than aGroupPortCapacity. The number of ports present is never greater than aGroupPortCapacity.;

30.4.2.1.3 aPortMap

ATTRIBUTE

APPROPRIATE SYNTAX:

BitString

BEHAVIOUR DEFINED AS:

A string of bits that reflects the current configuration of port managed objects within this group. The length of the bitstring is “aGroupPortCapacity” bits. The first bit relates to group 1. A “1” in the bitstring indicates presence of the port, “0” represents absence of the port.;

30.4.2.2 Group notifications

30.4.2.2.1 nPortMapChange

NOTIFICATION

APPROPRIATE SYNTAX:

BitString

BEHAVIOUR DEFINED AS:

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This notification is sent when a change occurs in the port structure of a group. This occurs only when a port is logically removed from or added to a group. The nPortMapChange notification is not sent when powering up a repeater. The value of the notification is the updated value of the aPortMap attribute.;

30.4.3 Repeater port managed object class

This subclause formally defines the behaviours for the oRepeaterPort managed object class, attributes, actions, and notifications.

30.4.3.1 Port attributes

30.4.3.1.1 aPortID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A value unique in the group. It is assumed that ports are partitioned into groups that also have IDs. The value of aPortID is assigned so as to uniquely identify a repeater port among the subordinate managed objects of the containing object (oGroup). This value can never be greater than aGroupPortCapacity.;

30.4.3.1.2 aPortAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE LIST that has the following entries:
disabled
enabled

BEHAVIOUR DEFINED AS:
A disabled port neither transmits nor receives. The port shall be explicitly enabled to restore operation. The acPortAdminControl action provides this ability. The port enable/disable function as reported by this attribute is preserved across repeater reset including loss of power. aPortAdminState takes precedence over auto-partition and functionally operates between the auto-partition mechanism and the AUI/PMA, PCS/PMA, or GMII/PCS as applicable. For a Clause 9 and 27 repeater, the port auto-partition is reinitialized upon acPortAdminControl taking the value "enabled." For a Clause 41 repeater, the port auto-partition, receive jabber and carrier integrity functions are reinitialized upon acPortAdminControl taking the value "enabled.";

30.4.3.1.3 aAutoPartitionState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE LIST that has the following entries:
autoPartitioned
notAutoPartitioned

BEHAVIOUR DEFINED AS:
The aAutoPartitionState flag indicates whether the port is currently partitioned by the repeater's auto-partition protection. The conditions that cause port partitioning are specified in partition state diagram in Clauses 9, 27, and 41. They are not differentiated here. A Clause 27 and 41 repeater port partitions on entry to the PARTITION WAIT state of the partition state diagram (Figure 27–8 and Figure 41–4).;

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30.4.3.1.4 aReadableFrames

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 15 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A representation of the total frames of valid frame length. Increment counter by one for each frame whose OctetCount is greater than or equal to minFrameSize and for which the FCSError and CollisionEvent signals are not asserted, and for which the attribute aFramesTooLong has not been incremented. Additionally, for 1000 Mb/s repeaters, this count shall only be incremented for frames which are received within a CarrierEvent which has a ActivityDuration of greater than or equal to (slotTime + JamSize) BT (see 4.4.2).

NOTE—This statistic provides one of the parameters necessary for obtaining the packet error rate.;

30.4.3.1.5 aReadableOctets

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 240 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by OctetCount for each frame which has been determined to be a readable frame.

NOTE—This statistic provides an indicator of the total data transferred.;

30.4.3.1.6 aFrameCheckSequenceErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 15 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by one for each frame with the FCSError signal asserted and the FramingError and CollisionEvent signals deasserted and whose OctetCount is greater than or equal to minFrameSize and for which the attribute aFramesTooLong has not been incremented.;

30.4.3.1.7 aAlignmentErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 15 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by one for each frame with the FCSError and FramingError signals asserted and CollisionEvent signal deasserted and whose OctetCount is greater than or equal to minFrameSize and for which the attribute aFramesTooLong has not been incremented. If aAlignmentErrors is incremented then the aFrameCheckSequenceErrors attribute shall not be incremented for the same frame. This counter will not increment for 8 bit wide group encoding schemes.;

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30.4.3.1.8 aFramesTooLong

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 815 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by one for each frame whose OctetCount is greater than maxUntaggedFrameSize or (maxUntaggedFrameSize + qTagPrefixSize) (see 4.2.7.1 and 4.4.2). A repeater may use either value in a constant manner, in which case the larger value is recommended. Alternatively, a repeater may use the appropriate value as a function of whether the frame in question is a basic or tagged MAC frame (see 3.2 and 3.5). If aFrameTooLong is counted then neither the aAlignmentErrors nor the aFrameCheckSequenceErrors attribute shall be incremented for the frame.

30.4.3.1.9 aShortEvents

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by one for each CarrierEvent with ActivityDuration less than ShortEventMaxTime. In the 10 Mb/s case ShortEventMaxTime is greater than 74 BT and less than 82 BT. ShortEventMaxTime has tolerances included to provide for circuit losses between a conformance test point at the AUI and the measurement point within the state diagram. In the 100 Mb/s case ShortEventMaxTime is 84 bits (21 nibbles), and for the 1000 Mb/s case ShortEventMaxTime is 72 bits (9 octets).

NOTE 1—shortEvents may indicate externally generated noise hits which will cause the repeater to transmit Runts to its other ports, or propagate a collision (which may be late) back to the transmitting DTE and damaged frames to the rest of the network.

NOTE 2—implementors may wish to consider selecting the ShortEventMaxTime towards the lower end of the allowed tolerance range to accommodate bit losses suffered through physical channel devices not budgeted for within this standard.

NOTE 3—Note also that the significance of this attribute is different in 10, 100, and 1000 Mb/s collision domains. Clause 9 repeaters perform fragment extension of short events which would be counted as runts on the interconnect ports of other repeaters. Clause 27 repeaters do not perform fragment extension. Clause 41 repeaters support one repeater per collision domain and do not perform fragment extension.;

30.4.3.1.10 aRunts

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by one for each CarrierEvent that meets one of the following two conditions. Only one test need be made. a) The ActivityDuration is greater than ShortEventMaxTime and less than ValidPacketMinTime and the CollisionEvent signal is deasserted. b) The OctetCount is less than 64, the ActivityDuration is greater than ShortEventMaxTime, and the CollisionEvent signal is deasserted. For 10 and 100 Mb/s repeaters, ValidPacketMinTime is greater than or equal to 552 BT and less than 565 BT. A CarrierEvent greater than or equal to 552 BT but less than 565 BT may or may not be counted as a runt. At 10 Mb/s an event whose length is greater than 74 BT but

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less than 82 BT shall increment either the aShortEvents attribute or the aRunts attribute, but not both. ValidPacketMinTime has tolerances included to provide for circuit losses between a conformance test point at the AUI and the measurement point within the state diagram.
For 1000 Mb/s repeaters, ValidPacketMinTime is 4136 BT.

NOTE—Runts usually indicate collision fragments, a normal network event.
In certain situations associated with large diameter networks a percentage of runts may exceed ValidPacket-MinTime.;

30.4.3.1.11 aCollisions

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

This counter increments for any CarrierEvent signal on any port in which the CollisionEvent signal on this port is asserted.;

30.4.3.1.12 aLateEvents

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

For a Clause 9 repeater port this counter increments for each CarrierEvent in which the CollIn(X) variable transitions to the value SQE (see 9.6.6.2) while the ActivityDuration is greater than the LateEventThreshold. For a Clause 27 and Clause 41 repeater port this counter increments for each CarrierEvent in which the CollisionEvent signal assertion occurs while the ActivityDuration is greater than the LateEventThreshold. In both cases such a CarrierEvent is counted twice, as both an aCollision and as an aLateEvent.
For 10 and 100 Mb/s repeaters, the LateEventThreshold is greater than 480 BT and less than 565 BT. LateEventThreshold has tolerances included to permit an implementation to build a single threshold to serve as both the LateEventThreshold and ValidPacketMinTime threshold. For 1000 Mb/s repeaters, the LateEventThreshold is equal to ValidPacketMinTime.;

30.4.3.1.13 aVeryLongEvents

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 250 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

For a Clause 9 repeater port this counter increments for each CarrierEvent whose ActivityDuration is greater than the MAU Jabber Lockup Protection timer TW3 (see 9.6.1, 9.6.5). For a Clause 27 and Clause 41 repeater port this counter increments on entry to the RX JABBER state of the receive timer state diagram (Figure 27–7 and Figure 41–3). Other counters may be incremented as appropriate.;

30.4.3.1.14 aDataRateMismatches

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter

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BEHAVIOUR DEFINED AS:

Increment counter by one for each frame received by this port that meets all of the conditions required by only one of the following three measurement methods:

Measurement method A, which is valid for 10 and 100 Mb/s operation only: a) The CollisionEvent signal is not asserted. b) The ActivityDuration is greater than ValidPacketMinTime. c) The received frequency (data rate) is detectably mismatched from the local transmit frequency.

Measurement method B, which is valid for 10 and 100 Mb/s operation only: a) The CollisionEvent signal is not asserted. b) The OctetCount is greater than 63. c) The received frequency (data rate) is detectably mismatched from the local transmit frequency.

Measurement method C, which is valid for 1000 Mb/s operation only: The received frequency (data rate) is detectably mismatched from the local transmit frequency.

The exact degree of mismatch is vendor specific and is to be defined by the vendor for conformance testing. When this event occurs, other counters whose increment conditions were satisfied may or may not also be incremented, at the implementor's discretion.

NOTE—Whether or not the repeater was able to maintain data integrity is beyond the scope of this standard.;

30.4.3.1.15 aAutoPartitions

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter

BEHAVIOUR DEFINED AS:

Increment counter by one for each time that the repeater has automatically partitioned this port. The conditions that cause a Clause 9 repeater port to partition are specified in the partition state diagram in Clause 9. They are not differentiated here. A Clause 27 and Clause 41 repeater port partitions on entry to the PARTITION WAIT state of the partition state diagram (Figure 27–8 and Figure 41–4).;

30.4.3.1.16 aIsolates

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 400 counts per second at 100 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by one each time that the repeater port automatically isolates as a consequence of false carrier events. The conditions that cause a port to automatically isolate are as defined by the transition from the FALSE CARRIER state to the LINK UNSTABLE state of the carrier integrity state diagram (Figure 27–9 and Figure 41–5).

NOTE—Isolates do not affect the value of aPortAdminState.;

30.4.3.1.17 aSymbolErrorDuringPacket

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 160 000 counts per second for 100 Mb/s implementations

BEHAVIOUR DEFINED AS:

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A count of the number of times when valid length packet was received at the port and there was at least one occurrence of an invalid data symbol. This can increment only once per valid CarrierEvent. A collision presence at any port of the repeater containing port N, will not cause this attribute to increment.;

30.4.3.1.18 aLastSourceAddress

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
The Source Address of the last readable Frame received by this port.;

30.4.3.1.19 aSourceAddressChanges

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 15 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
Increment counter by one each time that the aLastSourceAddress attribute has changed.

NOTE—This may indicate whether a link is connected to a single DTE or another multi-user segment.;

30.4.3.1.20 aBursts

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 235 000 counts per second at 1000 Mb/s

BEHAVIOUR DEFINED AS:
This counter is valid for 1000 Mb/s operation only. This counter increments by one for each CarrierEvent with ActivityDuration greater than or equal to slotTime during which the CollisionEvent signal has not been asserted. Note that this counter will not increment for a 10 or 100 Mb/s port as packet bursting is not supported at these speeds.;

30.4.3.2 Port actions

30.4.3.2.1 acPortAdminControl

ACTION

APPROPRIATE SYNTAX:
Same as aPortAdminStateBEHAVIOUR DEFINED AS:
This action provides a means to alter aPortAdminState. For a Clause 9 and 27 repeater it should exert a BEGIN on the Partitioning state diagram (Figures 9–6 and 27–8) upon taking the value “enabled.” For a Clause 41 repeater it shall exert a BEGIN on the receive timer, partition, and carrier integrity state diagrams (Figure 41–3, Figure 41–4, and Figure 41–5) upon taking the value “enabled.”;

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30.5 Layer management for 10, 100, and 1000 Mb/s medium attachment units (MAUs)

30.5.1 MAU managed object class

This subclause formally defines the behaviours for the oMAU managed object class, attributes, actions, and notifications.

30.5.1.1 MAU attributes

30.5.1.1.1 aMAUID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aMAUID is assigned so as to uniquely identify a MAU among the subordinate managed objects of the containing object.;

30.5.1.1.2 aMAUType

ATTRIBUTE

APPROPRIATE SYNTAX:
A GET-SET ENUMERATION that meets the requirements of the description below:

global	undefined
other	See 30.2.5
unknown	Initializing, true state or type not yet known
AUI	no internal MAU, view from AUI
10BASE5	Thick coax MAU as specified in Clause 8
FOIRL	FOIRL MAU as specified in 9.9
10BASE2	Thin coax MAU as specified in Clause 10
10BROAD36	Broadband DTE MAU as specified in Clause 11
10BASE-T	UTP MAU as specified in \Clause 14, duplex mode unknown
10BASE-THD	UTP MAU as specified in Clause 14, half duplex mode
10BASE-TFD	UTP MAU as specified in Clause 14, full duplex mode
10BASE-FP	Passive fiber MAU as specified in Clause 16
10BASE-FB	Synchronous fiber MAU as specified in Clause 17
10BASE-FL	Asynchronous fiber MAU as specified in Clause 18, duplex mode unknown
10BASE-FLHD	Asynchronous fiber MAU as specified in Clause 18, half duplex mode
10BASE-FLFD	Asynchronous fiber MAU as specified in Clause 18, full duplex mode
100BASE-T4	Four-pair Category 3 UTP as specified in Clause 23
100BASE-TX	Two-pair Category 5 UTP as specified in Clause 25, duplex mode unknown
100BASE-TXHD	Two-pair Category 5 UTP as specified in Clause 25, half duplex mode
100BASE-TXFD	Two-pair Category 5 UTP as specified in Clause 25, full duplex mode
100BASE-FX	X fiber over PMD as specified in Clause 26, duplex mode unknown
100BASE-FXHD	X fiber over PMD as specified in Clause 26, half duplex mode
100BASE-FXFD	X fiber over PMD as specified in Clause 26, full duplex mode
100BASE-T2	Two-pair Category 3 UTP as specified in Clause 32, duplex mode unknown
100BASE-T2HD	Two-pair Category 3 UTP as specified in Clause 32, half duplex mode
100BASE-T2FD	Two-pair Category 3 UTP as specified in Clause 32, full duplex mode
1000BASE-X	X PCS/PMA as specified in Clause 36 over undefined PMD, duplex mode unknown
1000BASE-XHD	X PCS/PMA as specified in Clause 36 over undefined PMD , half duplex mode

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1000BASE-XFD X PCS/PMA as specified in Clause 36 over undefined PMD, full duplex mode
1000BASE-LX X fiber over long-wavelength laser PMD as specified in Clause 38, duplex mode unknown
1000BASE-LXHD X fiber over long-wavelength laser PMD as specified in Clause 38, half duplex mode
1000BASE-LXFDX fiber over long-wavelength laser PMD as specified in Clause 38, full duplex mode
1000BASE-SX X fiber over short-wavelength laser PMD as specified in Clause 38, duplex mode unknown
1000BASE-SXHD X fiber over short-wavelength laser PMD as specified in Clause 38, half duplex mode
1000BASE-SXFD X fiber over short-wavelength laser PMD as specified in Clause 38, full duplex mode
1000BASE-CX X copper over 150-Ohm balanced cable PMD as specified in Clause 39, duplex mode unknown
1000BASE-CXHDX copper over 150-Ohm balanced cable PMD as specified in Clause 39, half duplex mode
1000BASE-CXFD X copper over 150-Ohm balanced cable PMD as specified in Clause 39, full duplex mode
1000BASE-T Four-pair Category 5 UTP PHY to be specified in Clause 40, duplex mode unknown
1000BASE-THD Four-pair Category 5 UTP PHY to be specified in Clause 40, half duplex mode
1000BASE-TFD Four-pair Category 5 UTP PHY to be specified in Clause 40, full duplex mode
802.9a Integrated services MAU as specified in IEEE Std 802.9 ISLAN-16T

BEHAVIOUR DEFINED AS:

Returns a value that identifies the 10 Mb/s, 100 Mb/s, or 1000 Mb/s internal MAU type. If an AUI is to be identified to access an external MAU, the type “AUI” is returned. A SET operation to one of the possible enumerations indicated by aMAUTypeList will force the MAU into the new operating mode. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the mode force bits specified in 22.2.4.1. If Clause 28 or Clause 37 Auto-Negotiation is operational, then this will change the advertised ability to the single enumeration specified in the SET operation, and cause an immediate link renegotiation. A change in the MAU type will also be reflected in aPHYType.

The enumerations 1000BASE-X, 1000BASE-XHD and 1000BASE-XFD shall only be returned if the underlying PMD type is unknown.;

30.5.1.1.3 aMAUTypeList

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of ENUMERATIONS that match the syntax of aMAUType

BEHAVIOUR DEFINED AS:
A GET attribute that returns the possible types that the MAU could be, identifying the ability of the MAU. This attribute maps to aPHYTypeList.;

30.5.1.1.4 aMediaAvailable

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED value list that has the following entries:
other undefined
unknown initializing, true state not yet known

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available	link or light normal, loopback normal
not available	link loss or low light, no loopback
remote fault	remote fault with no detail
invalid signal	invalid signal, applies only to 10BASE-FB
remote jabber	remote fault, reason known to be jabber
remote link loss	remote fault, reason known to be far-end link loss
remote test	remote fault, reason known to be test
offline	offline, applies only to Clause 37 Auto-Negotiation
auto neg error	Auto-Negotiation Error, applies only to Clause 37 Auto-Negotiation

BEHAVIOUR DEFINED AS:

If the MAU is a link or fiber type (FOIRL, 10BASE-T, 10BASE-F), then this is equivalent to the link test fail state/low light function. For an AUI, 10BASE2, 10BASE5, or 10BROAD36 MAU, this indicates whether or not loopback is detected on the DI circuit. The value of this attribute persists between packets for MAU types AUI, 10BASE5, 10BASE2, 10BROAD36, and 10BASE-FP.

At power-up or following a reset, the value of this attribute will be "unknown" for AUI, 10BASE5, 10BASE2, 10BROAD36, and 10BASE-FP MAUs. For these MAUs loopback will be tested on each transmission during which no collision is detected. If DI is receiving *input* when DO returns to IDL after a transmission and there has been no collision during the transmission, then loopback will be detected. The value of this attribute will only change during noncollided transmissions for AUI, 10BASE2, 10BASE5, 10BROAD36, and 10BASE-FP MAUs.

For 100BASE-T2,100BASE-T4, 100BASE-TX, and 100BASE-FX the enumerations match the states within the respective link integrity state diagrams, Figures 32-16, 23–12 and 24–15. Any MAU that implements management of Clause 28 Auto-Negotiation will map remote fault indication to MediaAvailable "remote fault." Any MAU that implements management of Clause 37 Auto-Negotiation will map the received RF1 and RF2 bits as specified in Table 37–2, as follows. Offline maps to the enumeration "offline," Link_Failure maps to the enumeration "remote fault" and Auto-Negotiation Error maps to the enumeration "auto neg error."

The enumeration "remote fault" applies to 10BASE-FB remote fault indication, the 100BASE-X far-end fault indication and nonspecified remote faults from a system running Clause 28 Auto-Negotiation. The enumerations "remote jabber," "remote link loss," or "remote test" should be used instead of "remote fault" where the reason for remote fault is identified in the remote signaling protocol.

Where a Clause 22 MII or Clause 35 GMII is present, a logic one in the remote fault bit (22.2.4.2.11) maps to the enumeration "remote fault," a logic zero in the link status bit (22.2.4.2.13) maps to the enumeration "not available." The enumeration "not available" takes precedence over "remote fault.";

30.5.1.1.5 aLoseMediaCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 10 counts per second

BEHAVIOUR DEFINED AS:

Counts the number of times that the MediaAvailable attribute changes from the enumeration "available" to any other enumeration. Mandatory for MAU type "AUI," optional for all others.;

30.5.1.1.6 aJabber

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of two indications. The first, JabberFlag, consists of an ENUMERATED value list that has the following entries:

other	undefined
unknown	initializing, true state not yet known
normal	state is true or normal

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fault	state is false, fault, or abnormal

The second, jabberCounter, is a generalized nonresettable counter. This counter has a maximum increment rate of 40 counts per second

BEHAVIOUR DEFINED AS:

If the MAU is in the JABBER state, the jabberFlag portion of the attribute is set to the "fault" value. The jabberCounter portion of the attribute is incremented each time the flag is set to the "fault" value. This attribute returns the value "other" for type AUI. Note that this counter will not increment for a 100 or 1000 Mb/s PHY, as there is no defined JABBER state.;

30.5.1.1.7 aMAUAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

other	undefined
unknown	initializing, true state not yet known
operational	powered and connected
standby	inactive but on
shutdown	similar to power down

BEHAVIOUR DEFINED AS:

A MAU in management state "standby" forces DI and CI to idle and the media transmitter to idle or fault, if supported. The management state "standby" only applies to link type MAUs. The state of MediaAvailable is unaffected. A MAU or AUI in the management state "shutdown" assumes the same condition on DI, CI and the media transmitter as if it were powered down or not connected. For an AUI, this management state will remove power from the AUI. The MAU may return the value "undefined" for Jabber and MediaAvailable attributes when it is in this management state. A MAU in the management state "operational" is fully functional, and operates and passes signals to its attached DTE or repeater port in accordance with its specification.;

30.5.1.1.8 aBbMAUXmitRcvSplitType

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

other	undefined
single	single-cable system
dual	dual-cable system, offset normally zero

BEHAVIOUR DEFINED AS:

Returns a value that indicates the type of frequency multiplexing/cabling system used to separate the transmit and receive paths for the 10BROAD36 MAU. All other types return "undefined.";

30.5.1.1.9 aBroadbandFrequencies

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of two instances of the type INTEGER.

The first INTEGER represents the Transmitter Carrier Frequency. The value of its INTEGER represents the frequency of the carrier divided by 250 kHz.

The second INTEGER represents the Translation Offset Frequency. The value of its INTEGER represents the frequency of the offset divided by 250 kHz

BEHAVIOUR DEFINED AS:

Returns a value that indicates the transmit carrier frequency and translation offset frequency in MHz/4 for the 10BROAD36 MAU. This allows the frequencies to be defined to a resolution of 250 kHz.;

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30.5.1.1.10 aFalseCarriers

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 160 000 counts per second under maximum network load, and 10 counts per second under zero network load, for 100 Mb/s implementations. This counter has a maximum increment rate of 1 600 000 counts per second under maximum network load, and 100 000 counts per second under zero network load, for 1000 Mb/s implementations

BEHAVIOUR DEFINED AS:

A count of the number of false carrier events during IDLE in 100BASE-X and 1000BASE-X links. This counter does not increment at the symbol rate. For 100BASE-X, it can increment after a valid carrier completion at a maximum rate of once per 100 ms until the nextCarrierEvent. For 1000BASE-X, it can increment after a valid carrier completion at a maximum rate of once per 10 μs until the next CarrierEvent.

NOTE—The increased increment rate for this attribute at 1000 Mb/s relative to its increment rate at 100 Mb/s has been provided to improve its use as an indication of line quality.;

30.5.1.1.11 aIdleErrorCount

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

This attribute takes the eight-bit value from the 100BASE-T2 Status register (MII management register 10) bits 7:0 “Idle Error Count” as described in 100BASE-T2, 32.5.3.2.6 and 40.5.;

30.5.1.2 MAU actions

30.5.1.2.1 acResetMAU

ACTION

APPROPRIATE SYNTAX:

None required

BEHAVIOUR DEFINED AS:

Resets the MAU in the same manner as would a power-off, power-on cycle of at least 0.5 s duration. During the 0.5 s DO, DI, and CI should be idle.;

30.5.1.2.2 acMAUAdminControl

ACTION

APPROPRIATE SYNTAX:

The same as used for aMAUAdminState

BEHAVIOUR DEFINED AS:

Executing an acMAUAdminControl action causes the MAU to assume the aMAUAdminState attribute value of one of the defined valid management states for control input. The valid inputs are “standby,” “operational,” and “shutdown” state (see the behaviour definition bMAUAdminState for the description of each of these states) except that a “standby” action to a mixing type MAU or an AUI will cause the MAU to enter the “shutdown” management state.;

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30.5.1.3 MAU notifications

30.5.1.3.1 nJabber

NOTIFICATION

APPROPRIATE SYNTAX:
The same as used for aJabber

BEHAVIOUR DEFINED AS:
The notification is sent whenever a managed 10 Mb/s MAU enters the JABBER state.;

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

This subclause formally defines the behaviours for the oAuto-Negotiation managed object class, attributes, actions, and notifications.

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.1 aAutoNegID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aAutoNegID is assigned so as to uniquely identify an Auto-Negotiation managed object among the subordinate managed objects of the containing object.;

30.6.1.1.2 aAutoNegAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:
enabled
disabled

BEHAVIOUR DEFINED AS:
An interface which has Auto-Negotiation signaling ability will be enabled to do so when this attribute is in the enabled state. If disabled then the interface will act as it would if it had no Auto-Negotiation signaling.;

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30.6.1.1.3 aAutoNegRemoteSignaling

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
detected
notdetected

BEHAVIOUR DEFINED AS:

The value indicates whether the remote end of the link is operating Auto-Negotiation signaling or not. It shall take the value detected if, during the previous link negotiation, FLP Bursts or /C/ ordered_sets (see 36.2.4.10) were received from the remote end.;

30.6.1.1.4 aAutoNegAutoConfig

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
other
configuring
complete
disabled
parallel detect fail

BEHAVIOUR DEFINED AS:

Indicates whether Auto-Negotiation signaling is in progress or has completed. The enumeration "parallel detect fail" maps to a failure in parallel detection as defined in 28.2.3.1.;

30.6.1.1.5 aAutoNegLocalTechnologyAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE that meets the requirements of the description below:

global	Reserved for future use
other	See 30.2.5
unknown	Initializing, true state or type not yet known
10BASE-T	10BASE-T half duplex as defined in Clause 14
10BASE-TFD	Full duplex 10BASE-T as defined in Clauses 14 and 31
100BASE-T4	100BASE-T4 half duplex as defined in Clause 23
100BASE-TX	100BASE-TX half duplex as defined in Clause 25
100BASE-TXFD	Full duplex 100BASE-TX as defined in Clauses 25 and 31
FDX PAUSE	PAUSE operation for full duplex links as defined in Annex 31B
FDX APAUSE	Asymmetric PAUSE operation for full duplex links as defined in Clause 37 and Annex 31B
FDX SPAUSE	Symmetric PAUSE operation for full duplex links as defined in Clause 37 and Annex 31B
FDX BPAUSE	Asymmetric and Symmetric PAUSE operation for full duplex links as defined in Clause 37 and Annex 31B
100BASE-T2	100BASE-T2 half duplex as defined in Clause 32
100BASE-T2FD	Full duplex 100BASE-T2 as defined in Clauses 31 and 32
1000BASE-X	1000BASE-X half duplex as specified in Clause 36
1000BASE-XFD	Full duplex 1000BASE-X as specified in Clauses 31 and 36
1000BASE-T	1000BASE-T half duplex UTP PHY as specified in Clause 40
1000BASE-TFD	Full duplex 1000BASE-T UTP PHY as specified in Clause 31 and as specified in Clause 40

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Rem Fault1	Remote fault bit 1 (RF1) as specified in Clause 37
Rem Fault2	Remote fault bit 2 (RF2) as specified in Clause 37
isoethernet	IEEE Std 802.9 ISLAN-16T

BEHAVIOUR DEFINED AS:

This indicates the technology ability of the local device, as defined in Clause 28 and Clause 37.

30.6.1.1.6 aAutoNegAdvertisedTechnologyAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

Same as aAutoNegLocalTechnologyAbility

BEHAVIOUR DEFINED AS:

For Clause 28 Auto-Negotiation this GET-SET attribute maps to the Technology Ability Field of the Auto-Negotiation Link Code Word. For Clause 37 Auto-Negotiation, this GET-SET attribute maps to bits D0-D13 of Config_Reg base page (see 37.2.1).

A SET operation to a value not available in aAutoNegLocalTechnologyAbility will be rejected. A successful SET operation will result in immediate link renegotiation if aAutoNegAdminState is enabled.

NOTE—This will in every case cause temporary link loss during link renegotiation. If set to a value incompatible with aAutoNegReceivedTechnologyAbility, link negotiation will not be successful and will cause permanent link loss.;

30.6.1.1.7 aAutoNegReceivedTechnologyAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

Same as aAutoNegLocalTechnologyAbility

BEHAVIOUR DEFINED AS:

Indicates the advertised technology ability of the remote hardware. For Clause 28 Auto-Negotiation, this attribute maps to the Technology Ability Field of the last received Auto-Negotiation Link Code Word(s). For Clause 37 Auto-Negotiation, this attribute maps to bits D0-D13 of the received Config_Reg base page (see 37.2.1).;

30.6.1.1.8 aAutoNegLocalSelectorAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE that meets the requirements of the description below:

other	Undefined
ethernet	IEEE Std 802.3
isoethernet	IEEE Std 802.9a-1995
tokenring	IEEE Std 802.5

BEHAVIOUR DEFINED AS:

This indicates the value of the selector field of the local hardware. Selector field is defined in 28.2.1.2.1. The enumeration of the Selector Field indicates the standard that defines the remaining encodings for Auto-Negotiation using that value of enumeration. For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the value ethernet.;

30.6.1.1.9 aAutoNegAdvertisedSelectorAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

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Same as aAutoNegLocalSelectorAbility

BEHAVIOUR DEFINED AS:

In the case of Clause 28 Auto-Negotiation, this GET-SET attribute maps to the Message Selector Field of the Auto-Negotiation Link Code Word. A SET operation to a value not available in aAutoNegLocalSelectorAbility will be rejected. A successful SET operation will result in immediate link renegotiation if aAutoNegAdminState is enabled. For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the value ethernet.

NOTE—This will in every case cause temporary link loss during link renegotiation. If set to a value incompatible with aAutoNegReceivedSelectorAbility, link negotiation will not be successful and will cause permanent link loss.;

30.6.1.1.10 aAutoNegReceivedSelectorAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

Same as aAutoNegLocalSelectorAbility

BEHAVIOUR DEFINED AS:

In the case of Clause 28 Auto-Negotiation, this attribute indicates the advertised message transmission ability of the remote hardware. Maps to the Message Selector Field of the last received Auto-Negotiation Link Code Word.For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the value ethernet.;

30.6.1.2 Auto-Negotiation actions

30.6.1.2.1 acAutoNegRestartAutoConfig

ATTRIBUTE

APPROPRIATE SYNTAX:

None required

BEHAVIOUR DEFINED AS:

Forces Auto-Negotiation to begin link renegotiation. Has no effect if Auto-Negotiation signaling is disabled.;

30.6.1.2.2 acAutoNegAdminControl

ATTRIBUTE

APPROPRIATE SYNTAX:

Same as aAutoNegAdminState

BEHAVIOUR DEFINED AS:

This action provides a means to turn Auto-Negotiation signaling on or off.;

30.7 Management for Link Aggregation

30.7.1 Aggregator managed object class

This subclause formally defines the behaviors for the oAggregator managed object class, attributes, and notifications.

Some of the attributes that are part of the definition of the oAggregator managed object class are derived by summing counter values from attributes of other objects; e.g., to generate a count of received frames for the Aggregator, the individual value for each Aggregation Port contributes to the sum. Where calculations of this form are used, the values that contribute to the Aggregator's attributes are *increments* in the values of the

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component attributes, not their absolute values. As any individual Aggregation Port is potentially only temporarily attached to its current Aggregator, the count values it contributes to the Aggregator's counters are the increments in its values that it has experienced during the period of time that it has been attached to that Aggregator.

The counter values defined for the Aggregator have been formulated as far as possible to make the Aggregator behave like an individual IEEE 802.3 MAC. The counts of frames received and transmitted are formulated to reflect the counts that would be expected by the MAC Client; they do not include frames transmitted and received as part of the operation of LACP or the Marker protocol, only frames that pass through the interface between the MAC Client and the Aggregator. However, as LACP and the Marker protocol are, as far as the individual MACs are concerned, part of their MAC Client, the RX/TX counters for the individual MACs will reflect both control and data traffic. As counts of errors at the port level cannot always be cleanly delineated between those that occurred as a result of aggregation activity and those that did not, no attempt has been made to separate these aspects of the port error counts. Therefore, there is not necessarily a direct correspondence between the individual MAC counters and the corresponding derived counters at the Aggregator level.

It should also be noted that the counters defined for the Aggregator include values that can only apply to half duplex links. This is consistent with the approach taken in Link Aggregation that a link that can only operate as an individual link is nonetheless considered as being attached to an Aggregator. This simplifies the modelling of managed objects for links that can operate in either half or full duplex, and ensures a consistent presentation of the attributes regardless of the type of links attached to the Aggregator.

NOTE—The operation of autonegotiation may mean that a given link can operate in full duplex or half duplex, depending upon the capabilities of the device(s) connected to it. Keeping the management view the same regardless of a link's current mode of operation allows a consistent management approach to be taken across all types of links.

30.7.1.1 Aggregator attributes

30.7.1.1.1 aAggID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The unique identifier allocated to this Aggregator by the local System. This attribute identifies an Aggregator instance among the subordinate managed objects of the containing object. This value is read-only.

NOTE—The aAggID is represented in the SNMP MIB as an ifIndex—see 30C.4.2.;

30.7.1.1.2 aAggDescription

ATTRIBUTE

APPROPRIATE SYNTAX:

A PrintableString, 255 characters max.

BEHAVIOUR DEFINED AS:

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A human-readable text string containing information about the Aggregator. This string could include information about the distribution algorithm in use on this Aggregator; for example, "Aggregator 1, Dist Alg=Dest MAC address." This string is read-only. The contents are vendor specific.;

30.7.1.1.3 aAggName

ATTRIBUTE

APPROPRIATE SYNTAX:

A PrintableString, 255 characters max.

BEHAVIOUR DEFINED AS:

A human-readable text string containing a locally significant name for the Aggregator. This string is read-write.;

30.7.1.1.4 aAggActorSystemID

ATTRIBUTE

APPROPRIATE SYNTAX:

MACAddress

BEHAVIOUR DEFINED AS:

A 6-octet read-write MAC address value used as a unique identifier for the System that contains this Aggregator.

NOTE—From the perspective of the Link Aggregation mechanisms described in Clause 43, only a single combination of Actor's System ID and System Priority are considered, and no distinction is made between the values of these parameters for an Aggregator and the port(s) that are associated with it (i.e., the protocol is described in terms of the operation of aggregation within a single System). However, the managed objects provided for the Aggregator and the port both allow management of these parameters. The result of this is to permit a single piece of equipment to be configured by management to contain more than one System from the point of view of the operation of Link Aggregation. This may be of particular use in the configuration of equipment that has limited aggregation capability (see 43.6).;

30.7.1.1.5 aAggActorSystemPriority

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A 2-octet read-write value indicating the priority value associated with the Actor's System ID.;

30.7.1.1.6 aAggAggregateOrIndividual

ATTRIBUTE

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APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean value indicating whether the Aggregator represents an Aggregate (“TRUE”) or an Individual link (“FALSE”).;

30.7.1.1.7 aAggActorAdminKey

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current administrative value of the Key for the Aggregator. The administrative Key value may differ from the operational Key value for the reasons discussed in 43.6.2. This is a 16-bit read-write value. The meaning of particular Key values is of local significance.;

30.7.1.1.8 aAggActorOperKey

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current operational value of the Key for the Aggregator. The administrative Key value may differ from the operational Key value for the reasons discussed in 43.6.2. This is a 16-bit read-only value. The meaning of particular Key values is of local significance.;

30.7.1.1.9 aAggMACAddress

ATTRIBUTE

APPROPRIATE SYNTAX:

MACAddress

BEHAVIOUR DEFINED AS:

A 6-octet read-only value carrying the individual MAC address assigned to the Aggregator.;

30.7.1.1.10 aAggPartnerSystemID

ATTRIBUTE

APPROPRIATE SYNTAX:

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MACAddress

BEHAVIOUR DEFINED AS:

A 6-octet read-only MAC address value consisting of the unique identifier for the current protocol Partner of this Aggregator. A value of zero indicates that there is no known Partner. If the aggregation is manually configured, this System ID value will be a value assigned by the local System.;

30.7.1.1.11 aAggPartnerSystemPriority

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A 2-octet read-only value that indicates the priority value associated with the Partner's System ID. If the aggregation is manually configured, this System Priority value will be a value assigned by the local System.;

30.7.1.1.12 aAggPartnerOperKey

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current operational value of the Key for the Aggregator's current protocol Partner. This is a 16-bit read-only value. If the aggregation is manually configured, this Key value will be a value assigned by the local System.;

30.7.1.1.13 aAggAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
up
down

BEHAVIOUR DEFINED AS:

This read-write value defines the administrative state of the Aggregator. A value of "up" indicates that the operational state of the Aggregator (aAggOperState) is permitted to be either up or down. A value of "down" forces the operational state of the Aggregator to be down. Changes to the administrative state affect the operational state of the Aggregator only, not the operational state of the Aggregation Ports that are attached to the Aggregator. A GET opera-

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tion returns the current administrative state. A SET operation changes the administrative state to a new value.;

30.7.1.1.14 aAggOperState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
up
down

BEHAVIOUR DEFINED AS:

This read-only value defines the operational state of the Aggregator. The operational state is "up" if one or more of the Aggregation Ports that are attached to the Aggregator are collecting, or both collecting and distributing, and if the value of aAggAdminState for the Aggregator is also "up." If none of the Aggregation Ports that are attached to the Aggregator are collecting and/or distributing, or if there are no Aggregation Ports attached to this Aggregator, then the operational state is "down." An operational state of "up" indicates that the Aggregator is available for use by the MAC Client; a value of "down" indicates that the Aggregator is not available for use by the MAC Client.;

30.7.1.1.15 aAggTimeOfLastOperChange

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aTimeSinceSystemReset (Annex F.2.1) at the time the interface entered its current operational state. If the current state was entered prior to the last re-initialization of the local network management subsystem, then this object contains a value of zero. This value is read-only.;

30.7.1.1.16 aAggDataRate

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current data rate, in bits per second, of the aggregate link. The value is calculated as N times the data rate of a single link in the aggregation, where N is the number of active links. This attribute is read-only.;

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30.7.1.1.17 aAggOctetsTxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 230 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data and padding octets transmitted by this Aggregator on all Aggregation Ports that are (or have been) members of the aggregation. The count does not include octets transmitted by the Aggregator in frames that carry LACPDUs or Marker PDUs (30.7.3.1.7, 30.7.3.1.8, 30.7.3.1.9). However, it includes frames discarded by the Distribution function of the Aggregator (30.7.1.1.25). This value is read-only.;

30.7.1.1.18 aAggOctetsRxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 230 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data and padding octets received by this Aggregator, from the Aggregation Ports that are (or have been) members of the aggregation. The count does not include octets received in frames that carry LACP or Marker PDUs (30.7.3.1.2, 30.7.3.1.3, 30.7.3.1.4), or frames discarded by the Collection function of the Aggregator (30.7.1.1.26). This value is read-only.;

30.7.1.1.19 aAggFramesTxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data frames transmitted by this Aggregator on all Aggregation Ports that are (or have been) members of the aggregation. The count does not include frames transmitted by the Aggregator that carry LACP or Marker PDUs (30.7.3.1.7, 30.7.3.1.8, 30.7.3.1.9). However, it includes frames discarded by the Distribution function of the Aggregator (30.7.1.1.25). This value is read-only.;

30.7.1.1.20 aAggFramesRxOK

ATTRIBUTE

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APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data frames received by this Aggregator, from the Aggregation Ports that are (or have been) members of the aggregation. The count does not include frames that carry LACP or Marker PDUs (30.7.3.1.2, 30.7.3.1.3, 30.7.3.1.4), or frames discarded by the Collection function of the Aggregator (30.7.1.1.26). This value is read-only.;

30.7.1.1.21 aAggMulticastFramesTxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data frames transmitted by this Aggregator on all Aggregation Ports that are (or have been) members of the aggregation, to a group destination address other than the broadcast address. The count does not include frames transmitted by the Aggregator that carry LACP or Marker PDUs (30.7.3.1.7, 30.7.3.1.8, 30.7.3.1.9). However, it includes frames discarded by the Distribution function of the Aggregator (30.7.1.1.25). This value is read-only.;

30.7.1.1.22 aAggMulticastFramesRxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data frames received by this Aggregator, from the Aggregation Ports that are (or have been) members of the aggregation, that were addressed to an active group address other than the broadcast address. The count does not include frames that carry LACP or Marker PDUs (30.7.3.1.2, 30.7.3.1.3, 30.7.3.1.4), or frames discarded by the Collection function of the Aggregator (30.7.1.1.26). This value is read-only.;

30.7.1.1.23 aAggBroadcastFramesTxOK

ATTRIBUTE

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APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the broadcast data frames transmitted by this Aggregator on all Aggregation Ports that are (or have been) members of the aggregation. The count does not include frames transmitted by the Aggregator that carry LACP or Marker PDUs (30.7.3.1.7, 30.7.3.1.8, 30.7.3.1.9). However, it includes frames discarded by the Distribution function of the Aggregator (30.7.1.1.25). This value is read-only.;

30.7.1.1.24 aAggBroadcastFramesRxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the broadcast data frames received by this Aggregator, from the Aggregation Ports that are (or have been) members of the aggregation. The count does not include frames that carry LACP or Marker PDUs (30.7.3.1.2, 30.7.3.1.3, 30.7.3.1.4), illegal or unknown protocol frames (30.7.3.1.5, 30.7.3.1.6), or frames discarded by the Collection function of the Aggregator (30.7.1.1.26). This value is read-only.;

30.7.1.1.25 aAggFramesDiscardedOnTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of data frames requested to be transmitted by this Aggregator that were discarded by the Distribution function of the Aggregator when conversations are re-allocated to different ports, due to the requirement to ensure that the conversations are flushed on the old ports in order to maintain proper frame ordering (43A.3), or discarded as a result of excessive collisions by ports that are (or have been) members of the aggregation. This value is read-only.;

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30.7.1.1.26 aAggFramesDiscardedOnRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of data frames, received on all ports that are (or have been) members of the aggregation, that were discarded by the Collection function of the Aggregator as they were received on ports whose Collection function was disabled. This value is read-only.;

30.7.1.1.27 aAggFramesWithTxErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of data frames requested to be transmitted by this Aggregator that experienced transmission errors on ports that are (or have been) members of the aggregation. This count does not include frames discarded due to excess collisions. This value is read-only.;

30.7.1.1.28 aAggFramesWithRxErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of data frames discarded on reception by all ports that are (or have been) members of the aggregation, or that were discarded by the Collection function of the Aggregator, or that were discarded by the Aggregator due to the detection of an illegal Slow Protocols PDU (30.7.3.1.6). This value is read-only.;

30.7.1.1.29 aAggUnknownProtocolFrames

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

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BEHAVIOUR DEFINED AS:

A count of data frames discarded on reception by all ports that are (or have been) members of the aggregation, due to the detection of an unknown Slow Protocols PDU (30.7.3.1.5). This value is read-only.;

30.7.1.1.30 aAggPortList

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE OF INTEGERs that match the syntax of aAggPortID.

BEHAVIOUR DEFINED AS:

The value of this read-only attribute contains the list of Aggregation Ports that are currently attached to the Aggregator. An empty list indicates that there are no Aggregation Ports attached. Each integer value in the list carries an aAggPortID attribute value (30.7.2.1.1).;

30.7.1.1.31 aAggLinkUpDownNotificationEnable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
enabled
disabled

BEHAVIOUR DEFINED AS:

When set to “enabled,” Link Up and Link Down notifications are enabled for this Aggregator. When set to “disabled,” Link Up and Link Down notifications are disabled for this Aggregator. This value is read-write.;

30.7.1.1.32 aAggCollectorMaxDelay

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of this 16-bit read-write attribute defines the maximum delay, in tens of microseconds, that may be imposed by the Frame Collector between receiving a frame from an Aggregator Parser, and either delivering the frame to its MAC Client or discarding the frame (see 43.2.3.1.1).;

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30.7.1.2 Aggregator Notifications

30.7.1.2.1 nAggLinkUpNotification

NOTIFICATION

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

When aAggLinkUpDownNotificationEnable is set to “enabled,” a Link Up notification is generated when the Operational State of the aggregator changes from “down” to “up.” When aAggLinkUpDownNotificationEnable is set to “disabled,” no Link Up notifications are generated. The notification carries the identifier of the Aggregator whose state has changed.;

30.7.1.2.2 nAggLinkDownNotification

NOTIFICATION

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

When aAggLinkUpDownNotificationEnable is set to “enabled,” a Link Down notification is generated when the Operational State of the aggregator changes from “up” to “down.” When aAggLinkUpDownNotificationEnable is set to “disabled,” no Link Down notifications are generated. The notification carries the identifier of the Aggregator whose state has changed.;

30.7.2 Aggregation Port managed object class

This subclause formally defines the behaviors for the oAggregationPort managed object class attributes.

30.7.2.1 Aggregation Port Attributes

30.7.2.1.1 aAggPortID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The unique identifier allocated to this Aggregation Port by the local System. This attribute identifies an Aggregation Port instance among the subordinate managed objects of the containing object. This value is read-only.

NOTE—The aAggPortID is represented in the SNMP MIB as an ifIndex—see 30C.4.4.;

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30.7.2.1.2 aAggPortActorSystemPriority

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A 2-octet read-write value used to define the priority value associated with the Actor's System ID.;

30.7.2.1.3 aAggPortActorSystemID

ATTRIBUTE

APPROPRIATE SYNTAX:

MACAddress

BEHAVIOUR DEFINED AS:

A 6-octet read-only MAC address value that defines the value of the System ID for the System that contains this Aggregation Port.;

30.7.2.1.4 aAggPortActorAdminKey

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current administrative value of the Key for the Aggregation Port. This is a 16-bit read-write value. The meaning of particular Key values is of local significance.;

30.7.2.1.5 aAggPortActorOperKey

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current operational value of the Key for the Aggregation Port. This is a 16-bit read-only value. The meaning of particular Key values is of local significance.;

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30.7.2.1.6 aAggPortPartnerAdminSystemPriority

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A 2-octet read-write value used to define the administrative value of priority associated with the Partner's System ID. The assigned value is used, along with the value of aAggPortPartnerAdminSystemID, aAggPortPartnerAdminKey, aAggPortPartnerAdminPort, and aAggPortPartnerAdminPortPriority, in order to achieve manually configured aggregation.;

30.7.2.1.7 aAggPortPartnerOperSystemPriority

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A 2-octet read-only value indicating the operational value of priority associated with the Partner's System ID. The value of this attribute may contain the manually configured value carried in aAggPortPartnerAdminSystemPriority if there is no protocol Partner.;

30.7.2.1.8 aAggPortPartnerAdminSystemID

ATTRIBUTE

APPROPRIATE SYNTAX:

MACAddress

BEHAVIOUR DEFINED AS:

A 6-octet read-write MACAddress value representing the administrative value of the Aggregation Port's protocol Partner's System ID. The assigned value is used, along with the value of aAggPortPartnerAdminSystemPriority, aAggPortPartnerAdminKey, aAggPortPartnerAdminPort, and aAggPortPartnerAdminPortPriority, in order to achieve manually configured aggregation.;

30.7.2.1.9 aAggPortPartnerOperSystemID

ATTRIBUTE

APPROPRIATE SYNTAX:

MACAddress

BEHAVIOUR DEFINED AS:

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A 6-octet read-only MACAddress value representing the current value of the Aggregation Port's protocol Partner's System ID. A value of zero indicates that there is no known protocol Partner. The value of this attribute may contain the manually configured value carried in aAggPortPartnerAdminSystemID if there is no protocol Partner.;

30.7.2.1.10 aAggPortPartnerAdminKey

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current administrative value of the Key for the protocol Partner. This is a 16-bit read-write value. The assigned value is used, along with the value of aAggPortPartnerAdminSystemPriority, aAggPortPartnerAdminSystemID, aAggPortPartnerAdminPort, and aAggPortPartnerAdminPortPriority, in order to achieve manually configured aggregation.;

30.7.2.1.11 aAggPortPartnerOperKey

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current operational value of the Key for the protocol Partner. The value of this attribute may contain the manually configured value carried in aAggPortPartnerAdminKey if there is no protocol Partner. This is a 16-bit read-only value.;

30.7.2.1.12 aAggPortSelectedAggID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The identifier value of the Aggregator that this Aggregation Port has currently selected. Zero indicates that the Aggregation Port has not selected an Aggregator, either because it is in the process of detaching from an Aggregator or because there is no suitable Aggregator available for it to select. This value is read-only.;

30.7.2.1.13 aAggPortAttachedAggID

ATTRIBUTE

APPROPRIATE SYNTAX:

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INTEGER

BEHAVIOUR DEFINED AS:

The identifier value of the Aggregator that this Aggregation Port is currently attached to. Zero indicates that the Aggregation Port is not currently attached to an Aggregator. This value is read-only.;

30.7.2.1.14 aAggPortActorPort

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The port number locally assigned to the Aggregation Port. The port number is communicated in LACPDUs as the Actor_Port. This value is read-only.;

30.7.2.1.15 aAggPortActorPortPriority

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The priority value assigned to this Aggregation Port. This 16-bit value is read-write.;

30.7.2.1.16 aAggPortPartnerAdminPort

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current administrative value of the port number for the protocol Partner. This is a 16-bit read-write value. The assigned value is used, along with the value of aAggPortPartnerAdminSystemPriority, aAggPortPartnerAdminSystemID, aAggPortPartnerAdminKey, and aAggPortPartnerAdminPortPriority, in order to achieve manually configured aggregation.;

30.7.2.1.17 aAggPortPartnerOperPort

ATTRIBUTE

APPROPRIATE SYNTAX:

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INTEGER

BEHAVIOUR DEFINED AS:

The operational port number assigned to this Aggregation Port by the Aggregation Port's protocol Partner. The value of this attribute may contain the manually configured value carried in aAggPortPartnerAdminPort if there is no protocol Partner. This 16-bit value is read-only.;

30.7.2.1.18 aAggPortPartnerAdminPortPriority

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current administrative value of the port priority for the protocol Partner. This is a 16-bit read-write value. The assigned value is used, along with the value of aAggPortPartnerAdminSystemPriority, aAggPortPartnerAdminSystemID, aAggPortPartnerAdminKey, and aAggPortPartnerAdminPort, in order to achieve manually configured aggregation.;

30.7.2.1.19 aAggPortPartnerOperPortPriority

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The priority value assigned to this Aggregation Port by the Partner. The value of this attribute may contain the manually configured value carried in aAggPortPartnerAdminPortPriority if there is no protocol Partner. This 16-bit value is read-only.;

30.7.2.1.20 aAggPortActorAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (1..8)]

BEHAVIOUR DEFINED AS:

A string of 8 bits, corresponding to the administrative values of Actor_State (43.4.2) as transmitted by the Actor in LACPDUs. The first bit corresponds to bit 0 of Actor_State (LACP_Activity), the second bit corresponds to bit 1 (LACP_Timeout), the third bit corresponds to bit 2 (Aggregation), the fourth bit corresponds to bit 3 (Synchronization), the fifth bit corresponds to bit 4 (Collecting), the sixth bit corresponds to bit 5 (Distributing), the seventh bit corresponds to bit 6 (Defaulted), and the eighth bit corresponds to bit 7 (Expired).

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These values allow administrative control over the values of LACP_Activity, LACP_Timeout, and Aggregation. This attribute value is read-write.;

30.7.2.1.21 aAggPortActorOperState

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (1..8)]

BEHAVIOUR DEFINED AS:

A string of 8 bits, corresponding to the current operational values of Actor_State (40.4.2) as transmitted by the Actor in LACPDUs. The bit allocations are as defined in 30.7.2.1.20. This attribute value is read-only.;

30.7.2.1.22 aAggPortPartnerAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (1..8)]

BEHAVIOUR DEFINED AS:

A string of 8 bits, corresponding to the current administrative value of Actor_State for the protocol Partner. The bit allocations are as defined in 30.7.2.1.20. This attribute value is read-write. The assigned value is used in order to achieve manually configured aggregation.;

30.7.2.1.23 aAggPortPartnerOperState

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (1..8)]

BEHAVIOUR DEFINED AS:

A string of 8 bits, corresponding to the current values of Actor_State in the most recently received LACPDU transmitted by the protocol Partner. The bit allocations are as defined in 30.7.2.1.20. In the absence of an active protocol Partner, this value may reflect the manually configured value aAggPortPartnerAdminState. This attribute value is read-only.;

30.7.2.1.24 aAggPortAggregateOrIndividual

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

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BEHAVIOUR DEFINED AS:

A read-only Boolean value indicating whether the Aggregation Port is able to Aggregate (“TRUE”) or is only able to operate as an Individual link (“FALSE”).;

30.7.3 Aggregation Port Statistics managed object class

This subclause formally defines the behaviors for the oAggPortStats managed object class attributes.

30.7.3.1 Aggregation Port Statistics attributes

30.7.3.1.1 aAggPortStatsID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

This read-only attribute identifies an Aggregation Port Statistics object instance among the subordinate managed objects of the containing object. The value allocated to this attribute shall be the same as the containing oAggregationPort managed object.;

30.7.3.1.2 aAggPortStatsLACPDUsRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

The number of valid LACPDUs received on this Aggregation Port. This value is read-only.;

30.7.3.1.3 aAggPortStatsMarkerPDUsRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

The number of valid Marker PDUs received on this Aggregation Port. This value is read-only.;

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30.7.3.1.4 aAggPortStatsMarkerResponsePDUsRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

The number of valid Marker Response PDUs received on this Aggregation Port. This value is read-only.;

30.7.3.1.5 aAggPortStatsUnknownRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 50 counts per second.

BEHAVIOUR DEFINED AS:

The number of frames received that either

— Carry the Slow Protocols Ethernet Type value (43B.4), but contain an unknown PDU, or

— Are addressed to the Slow Protocols group MAC Address (43B.3), but do not carry the Slow Protocols Ethernet Type. This value is read-only.;

30.7.3.1.6 aAggPortStatsIllegalRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 50 counts per second.

BEHAVIOUR DEFINED AS:

The number of frames received that carry the Slow Protocols Ethernet Type value (43B.4), but contain a badly formed PDU or an illegal value of Protocol Subtype (43B.4). This value is read-only.;

30.7.3.1.7 aAggPortStatsLACPDUsTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

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BEHAVIOUR DEFINED AS:

The number of LACPDUs transmitted on this Aggregation Port. This value is read-only.;

30.7.3.1.8 aAggPortStatsMarkerPDUsTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

The number of Marker PDUs transmitted on this Aggregation Port. This value is read-only.;

30.7.3.1.9 aAggPortStatsMarkerResponsePDUsTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

The number of Marker Response PDUs transmitted on this Aggregation Port. This value is read-only.;

30.7.4 Aggregation Port Debug Information managed object class

This subclause formally defines the behaviors for the oAggPortDebugInformation managed object class attributes.

30.7.4.1 Aggregation Port Debug Information attributes

30.7.4.1.1 aAggPortDebugInformationID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

This read-only attribute identifies an LACP Debug Information object instance among the subordinate managed objects of the containing object. The value allocated to this attribute shall be the same as the containing oAggregationPort managed object.;

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30.7.4.1.2 aAggPortDebugRxState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

current
expired
defaulted
initialize
lacpDisabled
portDisabled

BEHAVIOUR DEFINED AS:

This attribute holds the value “current” if the Receive state machine for the Aggregation Port is in the CURRENT state, “expired” if the Receive state machine is in the EXPIRED state, “defaulted” if the Receive state machine is in the DEFAULTED state, “initialize” if the Receive state machine is in the INITIALIZE state, “lacpDisabled” if the Receive state machine is in the LACP_DISABLED state, or “portDisabled” if the Receive state machine is in the PORT_DISABLED state. This value is read-only.;

30.7.4.1.3 aAggPortDebugLastRxTime

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aTimeSinceSystemReset (F.2.1) when the last LACPDU was received by this Aggregation Port. This value is read-only.;

30.7.4.1.4 aAggPortDebugMuxState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

detached
waiting
attached
collecting
distributing
collecting_distributing

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BEHAVIOUR DEFINED AS:

This attribute holds the value “detached” if the Mux state machine (43.4.15) for the Aggregation Port is in the DETACHED state, “waiting” if the Mux state machine for the Aggregation Port is in the WAITING state, “attached” if the Mux state machine for the Aggregation Port is in the ATTACHED state, “collecting” if the Mux state machine for the Aggregation Port is in the COLLECTING state, “distributing” if the Mux state machine for the Aggregation Port is in the DISTRIBUTING state, and “collecting_distributing” if the Mux state machine for the Aggregation Port is in the COLLECTING_DISTRIBUTING state. This value is read-only.;

30.7.4.1.5 aAggPortDebugMuxReason

ATTRIBUTE

APPROPRIATE SYNTAX:

A PrintableString, 255 characters max.

BEHAVIOUR DEFINED AS:

A human-readable text string indicating the reason for the most recent change of Mux machine state. This value is read-only.;

30.7.4.1.6 aAggPortDebugActorChurnState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

noChurn
churn

BEHAVIOUR DEFINED AS:

The state of the Actor Churn Detection machine (43.4.17) for the Aggregation Port. A value of “noChurn” indicates that the state machine is in either the NO_ACTOR_CHURN or the ACTOR_CHURN_MONITOR state, and “churn” indicates that the state machine is in the ACTOR_CHURN state. This value is read-only.;

30.7.4.1.7 aAggPortDebugPartnerChurnState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

noChurn
churn

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BEHAVIOUR DEFINED AS:

The state of the Partner Churn Detection machine (43.4.17) for the Aggregation Port. A value of "noChurn" indicates that the state machine is in either the NO_PARTNER_CHURN or the PARTNER_CHURN_MONITOR state, and "churn" indicates that the state machine is in the PARTNER_CHURN state. This value is read-only.;

30.7.4.1.8 aAggPortDebugActorChurnCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

Count of the number of times the Actor Churn state machine has entered the ACTOR_CHURN state. This value is read-only.;

30.7.4.1.9 aAggPortDebugPartnerChurnCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

Count of the number of times the Partner Churn state machine has entered the PARTNER_CHURN state. This value is read-only.;

30.7.4.1.10 aAggPortDebugActorSyncTransitionCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

Count of the number of times the Actor's Mux state machine (43.4.15) has entered the IN_SYNC state. This value is read-only.;

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30.7.4.1.11 aAggPortDebugPartnerSyncTransitionCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

Count of the number of times the Partner's Mux state machine (43.4.15) has entered the IN_SYNC state. This value is read-only.;

30.7.4.1.12 aAggPortDebugActorChangeCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

Count of the number of times the Actor's perception of the LAG ID for this Aggregation Port has changed. This value is read-only.;

30.7.4.1.13 aAggPortDebugPartnerChangeCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

Count of the number of times the Partner's perception of the LAG ID (43.3.6.1) for this Aggregation Port has changed. This value is read-only.;

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31. MAC Control

31.1 Overview

This clause specifies an optional MAC Control Sublayer (MAC Control) for use with the CSMA/CD MAC. MAC Control provides for real-time control and manipulation of MAC sublayer operation. This clause specifies a generalized architecture and protocol for MAC Control. Specific implementations of control functions using this protocol are specified in the normative annexes to this clause. The MAC Control protocol is specified such that it can support new functions to be implemented and added to this standard in the future.

Non-realtime, or quasistatic control (e.g., configuration of MAC operational parameters) is provided by Layer Management.

Operation of the MAC Control sublayer is transparent to the CSMA/CD MAC.

The body of this clause and its associated annexes contain state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram shall prevail. The notation used in the state diagrams follows the conventions of 21.5.

31.2 Layer architecture

The MAC Control sublayer is a client of the CSMA/CD MAC. Figure 31–1 depicts the architectural positioning of the MAC Control sublayer with respect to the CSMA/CD MAC and the MAC Control client. MAC Control clients may include the Bridge Relay Entity, LLC, or other applications.

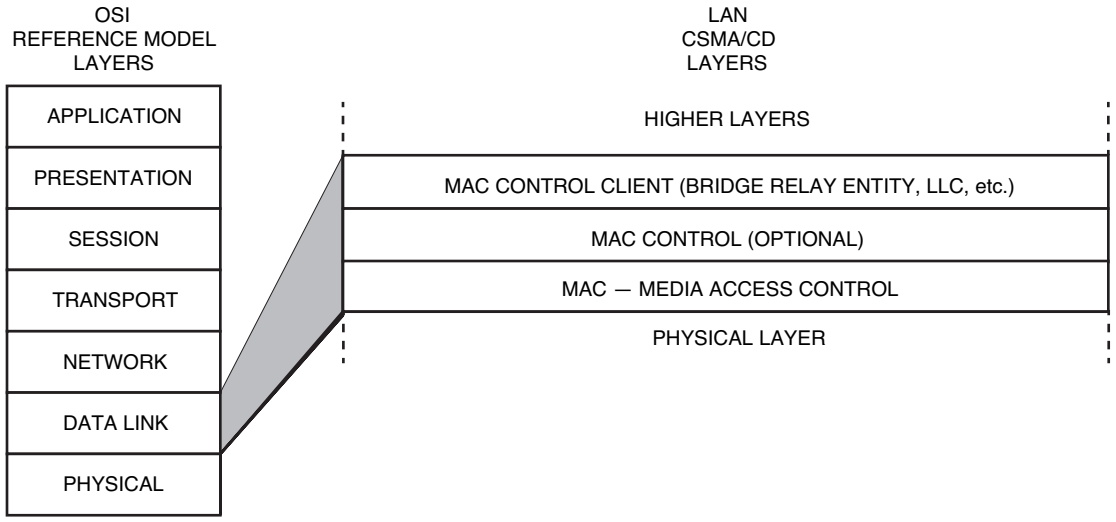


Figure 31–1—Architectural positioning of MAC Control sublayer

31.3 Support by interlayer interfaces

This subclause describes how the MAC Control sublayer uses the service interfaces specified in clauses 2 and 4. In the absence of the optional MAC Control sublayer, the MAC sublayer provides services to its client directly, through the interface specified in 4.3.2.

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The optional MAC Control sublayer is inserted between the MAC sublayer and its normal client (i.e., its client in the absence of the MAC Control sublayer). The MAC Control sublayer provides a client service interface to the MAC client as specified in Clause 2, and maps these service primitives to those specified in 4.3.2.

NOTE—In the absence of the MAC Control sublayer, Clause 31 makes no attempt to reconcile the long-standing inconsistencies between the interface definitions in subclauses 4.3.2 and 2.3. These existing inconsistencies have not historically hampered the construction of interoperable networking equipments, and are not sufficiently important to merit further attention.

Figure 31–2 depicts the usage of interlayer interfaces by the MAC Control sublayer. Devices that implement the MAC Control sublayer shall support the optional MAC service primitives, MA_CONTROL.request and MA_CONTROL.indication, as specified in 2.3.3 and 2.3.4.

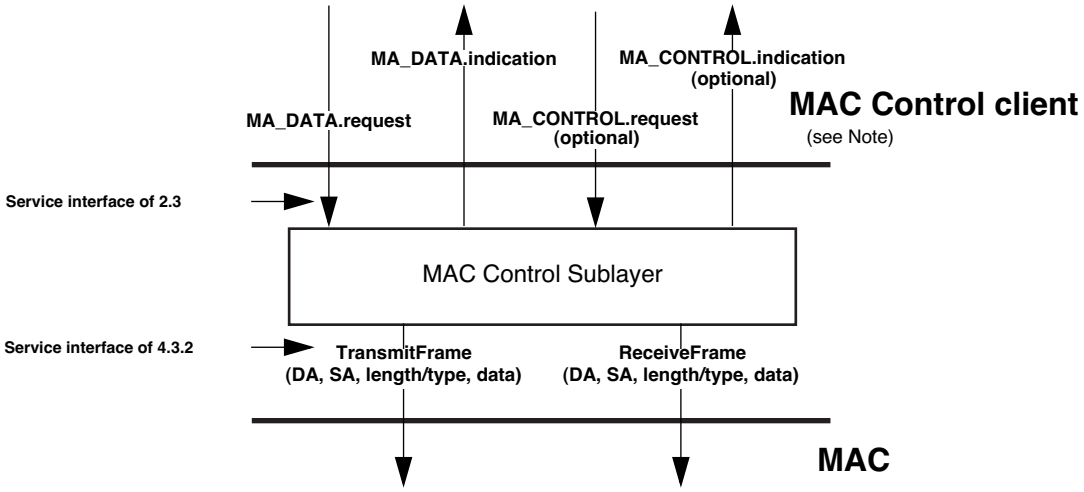


Figure 31–2—MAC Control sublayer support of interlayer service interfaces

Clients of the MAC Control sublayer may generate either MA_CONTROL.request or MA_DATA.request primitives. MA_CONTROL.request primitives generated by MAC Control clients are interpreted by the MAC Control sublayer, and may result in the generation of TransmitFrame function calls to the MAC sublayer, or other actions as necessary to support the requested MAC Control sublayer function. Based upon the state of the MAC Control sublayer, MA_DATA.request primitives may cause the immediate generation of a TransmitFrame function call to the MAC sublayer, or be delayed, discarded, or modified in order to perform the requested MAC Control function.

All frames validly received by the CSMA/CD MAC are passed to the MAC Control sublayer for interpretation. If the frame is destined for the MAC Control client, the MAC Control sublayer generates an MA_DATA.indication primitive, providing complete transparency for normal data exchange between MAC Control clients. If the frame is destined for the MAC Control sublayer entity, it is interpreted and acted on internal to the MAC Control sublayer. This may result in state changes within the MAC Control sublayer, the generation of MA_CONTROL.indication primitives, or other actions as necessary to support the MAC Control sublayer function. MAC Control sublayer functions shall always sink MAC Control frames.

Frames destined for the MAC Control sublayer (MAC Control frames) are distinguished from frames destined for MAC Control clients by a unique Length/Type field identifier.

The MAC Control sublayer generates MA_CONTROL.indication primitives to its client, signaling the current value of internal state variables. Each MAC Control function implemented may have its own function-specific state indications.

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31.4 MAC Control frames

MAC Control frames comprise MAC client data for the CSMA/CD MAC, as specified in Clause 3. They are encapsulated by the CSMA/CD MAC; that is, they are prepended by a Preamble and Start-of-Frame delimiter and appended by an FCS.

MAC Control frames are distinguished from other MAC frames only by their Length/Type field identifier.

31.4.1 MAC Control frame format

For any particular implementation of this standard, MAC Control frames are fixed length, containing minFrameSize–32 bits. The underlying MAC prepends the Preamble and Start-of-Frame delimiter fields, and appends the FCS. Figure 31–3 depicts the MAC Control frame format.

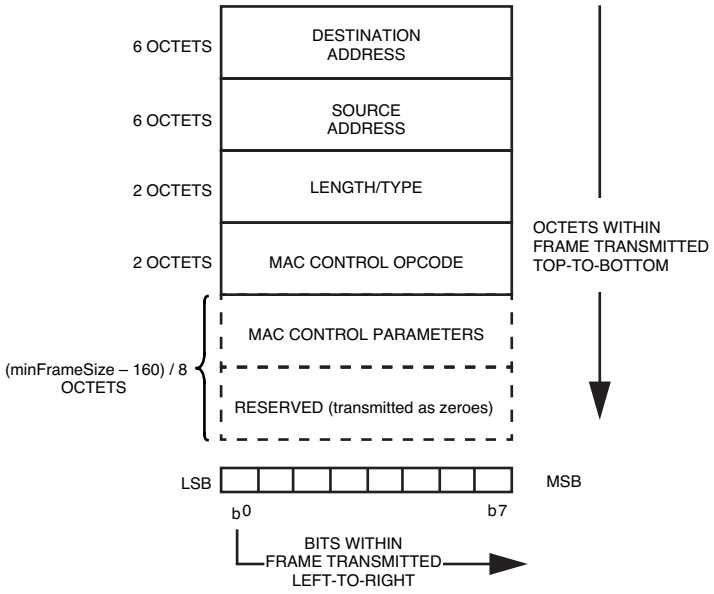


Figure 31–3—MAC Control frame format

31.4.1.1 Destination Address field

The Destination Address field of a MAC Control frame contains the 48-bit address of the station(s) for which the frame is intended. It may be an individual or multicast (including broadcast) address. Permitted values for the Destination Address field may be specified separately for each MAC Control opcode in the annexes to Clause 31.

31.4.1.2 Source Address field

The Source Address field of a MAC Control frame contains the 48-bit individual address of the station sending the frame.

31.4.1.3 Length/Type field

The Length/Type field of a MAC Control frame is a 2-octet field that shall contain the hexadecimal value: 88-08. This value carries the Type interpretation (see 3.2.6), and has been universally assigned for MAC Control of CSMA/CD LANs.

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31.4.1.4 MAC Control Opcode field

The MAC Control Opcode field shall contain a 2-octet operation code indicating the MAC Control function. It defines the semantics of the MAC Control Parameters field specified in 31.4.1.5. Annex 31A contains the list of defined MAC Control opcodes and interpretations.

A MAC Control frame shall contain exactly one MAC Control opcode.

31.4.1.5 MAC Control Parameters field

The MAC Control Parameters field shall contain MAC Control opcode-specific parameters. This field may contain none, one, or more parameters as defined by the MAC Control Opcode. The opcode-specific semantics of the MAC Control Parameters field are defined in the normative annex specifying each MAC Control function.

The MAC Control Parameters field shall contain an integral number of octets. The length of the MAC Control Parameters field varies from a minimum of zero, to a maximum of minFrameSize –160 bits. See 4.2.3.3 for a discussion of minFrameSize.

31.4.1.6 Reserved field

The Reserved field is used when the MAC Control parameters do not fill the fixed length MAC Control frame. The size of the Reserved field, if any, is determined by the size of the MAC Control Parameters field supplied by MAC Control and the minimum frame size parameter of the particular implementation.

The length of Reserved field required for a MAC Control Parameters field that is n octets long is [minFrameSize – (8 × n + 160)] bits. See 4.2.3.3 for a discussion of minFrameSize. The Reserved field is transmitted as all zeroes.

31.5 Opcode-independent MAC Control sublayer operation

The MAC Control sublayer generates ReceiveFrame function calls continuously to the underlying MAC. The MAC passes to the MAC Control sublayer all valid frames. Invalid frames, as specified in 3.4, are not passed to the MAC Control sublayer in response to a ReceiveFrame function call.

31.5.1 Frame parsing and data frame reception

Upon receipt, the MAC Control sublayer parses the incoming frame to determine whether it is destined for the MAC client (Data frame) or for a specific function within the MAC Control sublayer entity itself (MAC Control frame). MAC Control frames with a length of minFrameSize and a supported opcode field are interpreted and acted upon by the MAC Control sublayer.

A frame that does not contain the unique Length/Type field specified in 31.4.1.3 is a Data frame. The receipt of a Data frame results in the generation of a MA_DATA.indication primitive by the MAC Control sublayer, with the following parameters:

a) The destination_address parameter is set equal to the destinationParam from the ReceiveFrame function.
b) The source_address parameter is set equal to the sourceParam from the ReceiveFrame function.
c) The m_sdu parameter is set equal to the concatenation of the lengthOrTypeParam and the dataParam from the ReceiveFrame function.
d) The reception_status parameter is set equal to the ReceiveStatus from the ReceiveFrame function.

NOTE—For Length/Type field values in the range between maxValidLength and minTypeValue, the behavior of the RemovePad function in the underlying MAC sublayer is unspecified. Frames with Length/Type field values in this range may or may not be passed up by the MAC sublayer.

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MAC Control frames with a length greater than minFrameSize and a supported opcode field may be discarded, or truncated to minFrameSize, interpreted, and acted upon. Unsupported MAC Control frames are discarded. Discarded frames are neither passed to the MAC client nor interpreted nor acted upon by the MAC Control sublayer.

31.5.2 Control frame reception

Validly received MAC Control frames are further parsed to determine the opcode. The opcode is contained in the first two octets of the dataParam from the ReceiveFrame function. If the MAC Control sublayer entity supports the function requested by the specified opcode, it interprets and acts upon the MAC Control frame in an opcode- and request_operand-specific manner. (See annexes.) This action may change the state of the MAC Control sublayer, affecting its behavior with respect to data transmission requests by the MAC client, future control frame receptions, or control indications to the MAC client.

If the MAC Control sublayer entity does not support the function requested by the specified opcode, it discards the MAC Control frame. The discard of a frame in this manner may be reported to network management.

31.5.3 Opcode-independent MAC Control receive state diagram

The MAC Control sublayer shall implement the receive state machine specified in this subclause.

31.5.3.1 Constants

802.3_MAC_Control
: The 16-bit Length/Type field value reserved for CSMA/CD MAC Control usage, specified in 31.4.1.3.

31.5.3.2 Variables

receiveEnabled
: A boolean set by Network Management to indicate that the station is permitted to receive from the network.

Values: true; Receiver is enabled by management
false; Receiver is disabled by management

31.5.3.3 Functions

ReceiveFrame
: The MAC Sublayer primitive called to receive a frame with the specified parameters.

31.5.3.4 Messages

MA_CONTROL.indication
: A signal sent by the MAC Control sublayer signifying a change in the internal sublayer state.

MA_DATA.indication
: The service primitive used by the MAC Control sublayer to pass a received data frame to the MAC Control client with the specified parameters.

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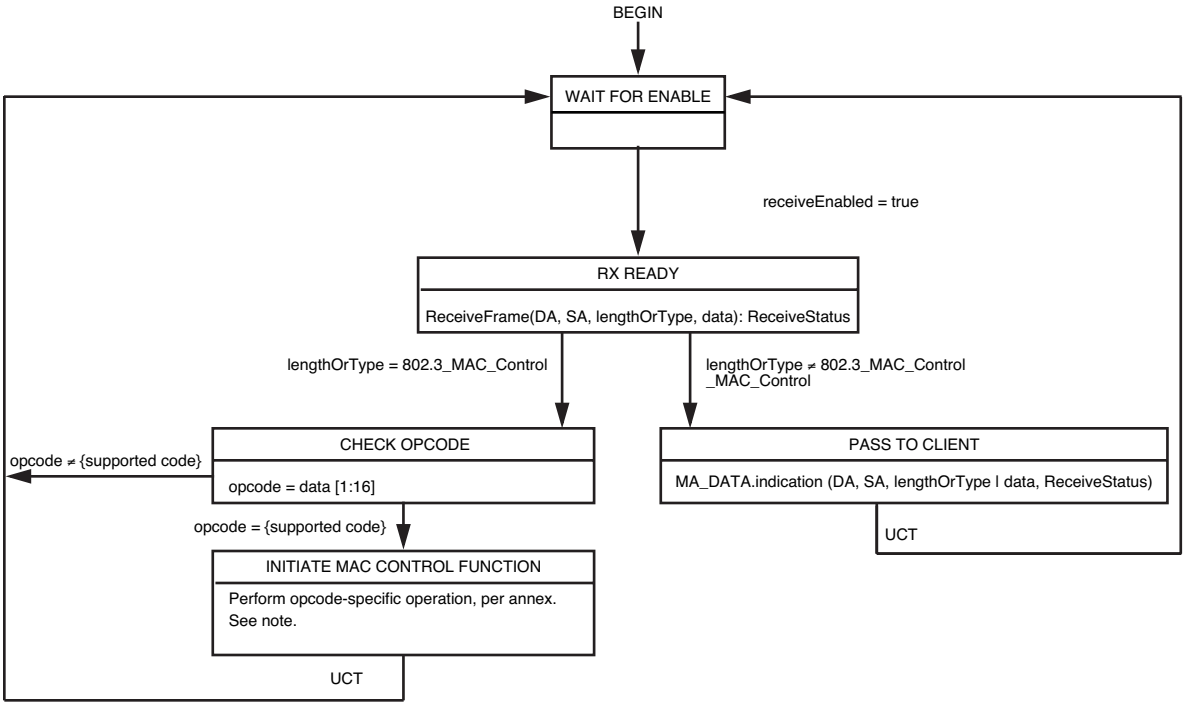
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31.5.3.5 Opcode-independent MAC Control Receive state diagram



NOTE—The opcode-specific operation is launched as a parallel process by the MAC Control sublayer, and not as a synchronous function. Progress of the generic MAC Control Receive state machine (as shown in this figure) is not implicitly impeded by the launching of the opcode-specific function.

Figure 31–4—Generic MAC Control Receive state diagram

The functions performed in the INITIATE MAC CONTROL FUNCTION state are opcode-specific, and are provided in the annexes to Clause 31.

31.6 Compatibility requirements

An instantiation of the MAC Control sublayer is not required to implement all valid control functions specified in Annex 31A.

31.7 MAC Control client behavior

The MAC Control sublayer uses the services of the underlying connectionless-mode MAC sublayer to exchange both Data and Control frames. The MAC Control sublayer does not provide any mechanism for recovery from lost, discarded, damaged, or delayed frames. It is the responsibility of the MAC Control client to implement mechanisms for dealing with lost, discarded, damaged, and delayed frames, if necessary.

Since implementation of the MAC Control sublayer is optional, a MAC Control client cannot assume the existence of a MAC Control sublayer entity in a peer DTE.

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31.8 Protocol Implementation Conformance Statement (PICS) proforma for Clause 31, MAC Control[13]

31.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 31, the optional MAC Control sublayer, shall complete the following PICS proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

31.8.2 Identification

31.8.2.1 Implementation identification

Supplier	
Contact point for queries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations, other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

31.8.2.2 Protocol summary

Identification of protocol specification	IEEE Std 802.3-2002, Clause 31, MAC Control
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; The answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

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31.8.3 PICS proforma for MAC Control frames

31.8.3.1 Support by interlayer interfaces

Item	Feature	Subclause	Value/comment	Status	Support
SI1	Support for optional MAC service primitives, MA_CONTROL.request and MA_CONTROL.indication	31.3	Required	M	Yes [ ]

31.8.3.2 MAC Control frame format

Item	Feature	Subclause	Value/comment	Status	Support
FF1	Length/Type field	31.4.1.3	2-octet field containing 88-08	M	Yes [ ]
FF2	MAC Control opcode	31.4.1.4	2-octet operation code	M	Yes [ ]
FF3	Number of opcodes	31.4.1.4	1	M	Yes [ ]
FF4	MAC Control parameters	31.4.1.5	MAC Control Parameter field as described	M	Yes [ ]

31.8.3.3 Opcode-independent MAC Control sublayer operation

Item	Feature	Subclause	Value/comment	Status	Support
SD1	Generic MAC Control receive state diagram	31.5.3	Meets requirements of Figure 31–4	M	Yes [ ]
SD2	MAC Control frame action	31.3	Sink MAC Control frames	M	Yes [ ]

31.8.3.4 Control opcode assignments

Item	Feature	Subclause	Value/comment	Status	Support
COA1	Opcode values and interpretations	31A	Reserved opcodes not used	M	Yes [ ]

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32. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T2

NOTE—This PHY is not recommended for new installations.

32.1 Overview

The 100BASE-T2 PHY is one of the 100BASE-T family of high-speed CSMA/CD network specifications. The 100BASE-T2 Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and baseband medium specifications are aimed at users who want 100 Mb/s performance over basic data grade Category 3 twisted-pair cabling systems. 100BASE-T2 signaling requires two pairs of Category 3 cabling, or cabling with better transfer characteristics than Category 3, installed according to ISO/IEC 11801, as specified in 32.7. This type of cabling, and the connectors used with it, are simple to install and reconfigure.

This clause defines the type 100BASE-T2 PCS, type 100BASE-T2 PMA sublayer, and type 100BASE-T2 Medium Dependent Interface (MDI). Together, the PCS and the PMA sublayer comprise a 100BASE-T2 Physical Layer (PHY). Control actions needed for correct PHY operations are specified by the 100BASE-T2 PHY Control function. Provided in this document are full functional, electrical, and mechanical specifications for the type 100BASE-T2 PHY Control function, PCS, PMA, and MDI. This clause also specifies the baseband medium used with 100BASE-T2.

The objectives of 100BASE-T2 are as follows:

a) To support the CSMA/CD MAC;

b) To support the 100BASE-T Media Independent Interface (MII), repeater, and Auto-Negotiation;

c) To support full duplex operations (Clause 31);

d) To provide 100 Mb/s data rate at the MII;

e) To provide for operating over two pairs of Category 3, 4, or 5 balanced twisted-pair cabling systems installed in accordance with ISO/IEC 11801, as specified in 32.7, at distances up to 100 m;

f) To support operation of other applications on adjacent pairs;

g) To allow for a nominal network extent of 200 m including

   1) Balanced cabling links of 100 m to support both half duplex and full duplex operation and

   2) Two-repeater networks of approximately 200 m span;

h) To provide a communication channel with a symbol error rate of less than one part in 10^{10} at the PMA service interface.

32.1.1 Relation of 100BASE-T2 to other standards

Relations between the 100BASE-T2 PHY and the ISO/IEC Open Systems Interconnection (OSI) Reference Model and the IEEE 802.3 CSMA/CD LAN Model are shown in Figure 32–1. The PHY layers shown in Figure 32–1 connect one Clause 4 Media Access Control (MAC) layer to a Clause 27 repeater. This clause also discusses other variations of the basic configuration shown in Figure 32–1. This whole clause builds on Clauses 1, 2, 3, 4, 21, 22, 27, 28, 29, and 30 of this standard.

32.1.2 Operation of 100BASE-T2

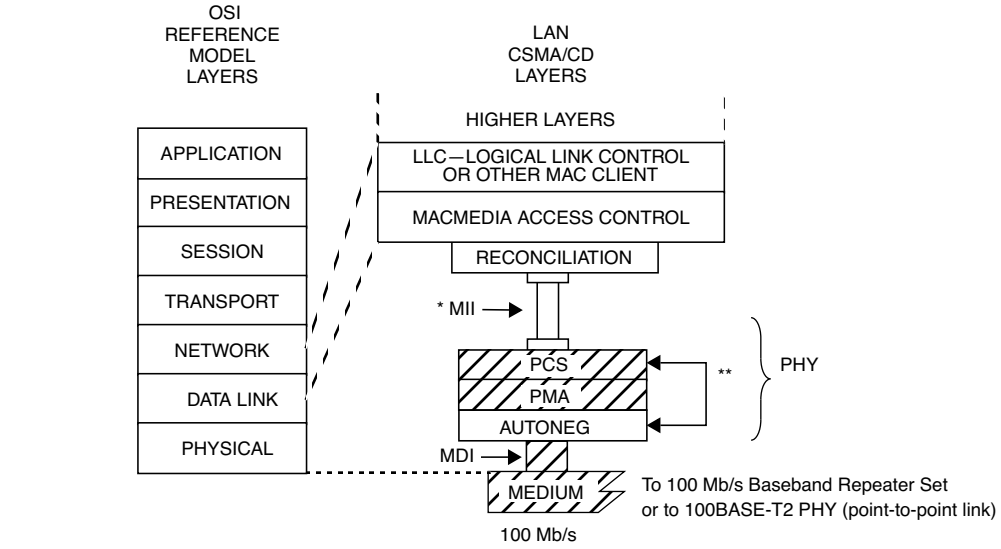
The 100BASE-T2 PHY employs dual-duplex baseband transmission over two wire pairs BI_DA and BI_DB, whereby the aggregate data rate of 100 Mb/s is achieved by transmission at a modulation rate of 25

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NOTE 1—* MII is optional.

NOTE 2—** AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indicate.

Figure 32–1—Type 100BASE-T2 PHY relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

MBd over each wire pair in each direction simultaneously (full duplex transmission), as shown in Figure 32–2. Transmitted symbols are selected from the two-dimensional 5 × 5 symbol constellation illustrated in Figure 32–3. Redundancy in the 5 × 5 constellation allows specific encoding rules to be employed to represent MII data streams, an idle mode or control signals as sequences of two-dimensional symbols. Each two-dimensional symbol can be viewed as a pair (A_n, B_n) of one-dimensional quinary symbols taken from the set {–2, –1, 0, +1, +2}. Five-level Pulse Amplitude Modulation is employed for transmission over each wire pair (PAM 5 × 5). The modulation rate of 25 MBd matches the MII clock rate of 25 MHz. The corresponding symbol period is 40 ns. This specification permits the use of Category 3, 4, or 5 balanced cabling, installed according to ISO/IEC 11801, as defined in 32.7.

A 100BASE-T2 PHY can be configured either as a *master* PHY or as a *slave* PHY. The master-slave relationship between two stations sharing a link segment is established during Auto-Negotiation (see Clause 28, 32.5, Annex 28C, and 32.5.2). The master PHY uses an external clock to determine the timing of transmitter and receiver operations. The slave PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations, i.e., it performs loop timing, as illustrated in Figure 32–2. In a DTE to repeater connection, the repeater is typically set to be master and the DTE is typically set to be slave.

The following subclauses summarize the PCS, PMA, and PHY Control sections of this document. Figure 32–4 shows the division of responsibilities between the PCS, the PMA sublayer, and the PHY Control function.

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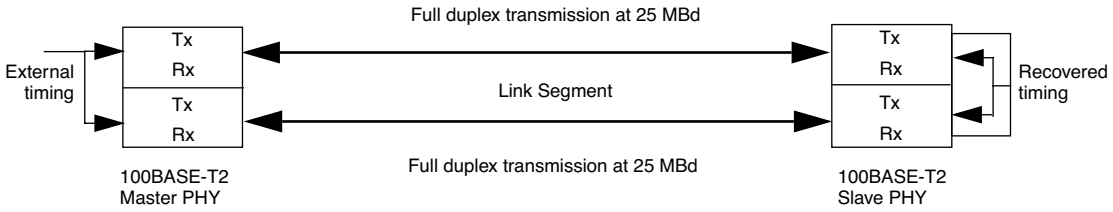


Figure 32–2—100BASE-T2 topology

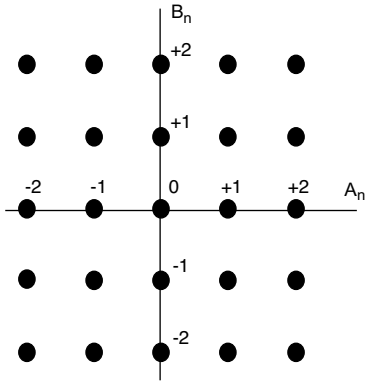


Figure 32–3—PAM5×5 symbol constellation

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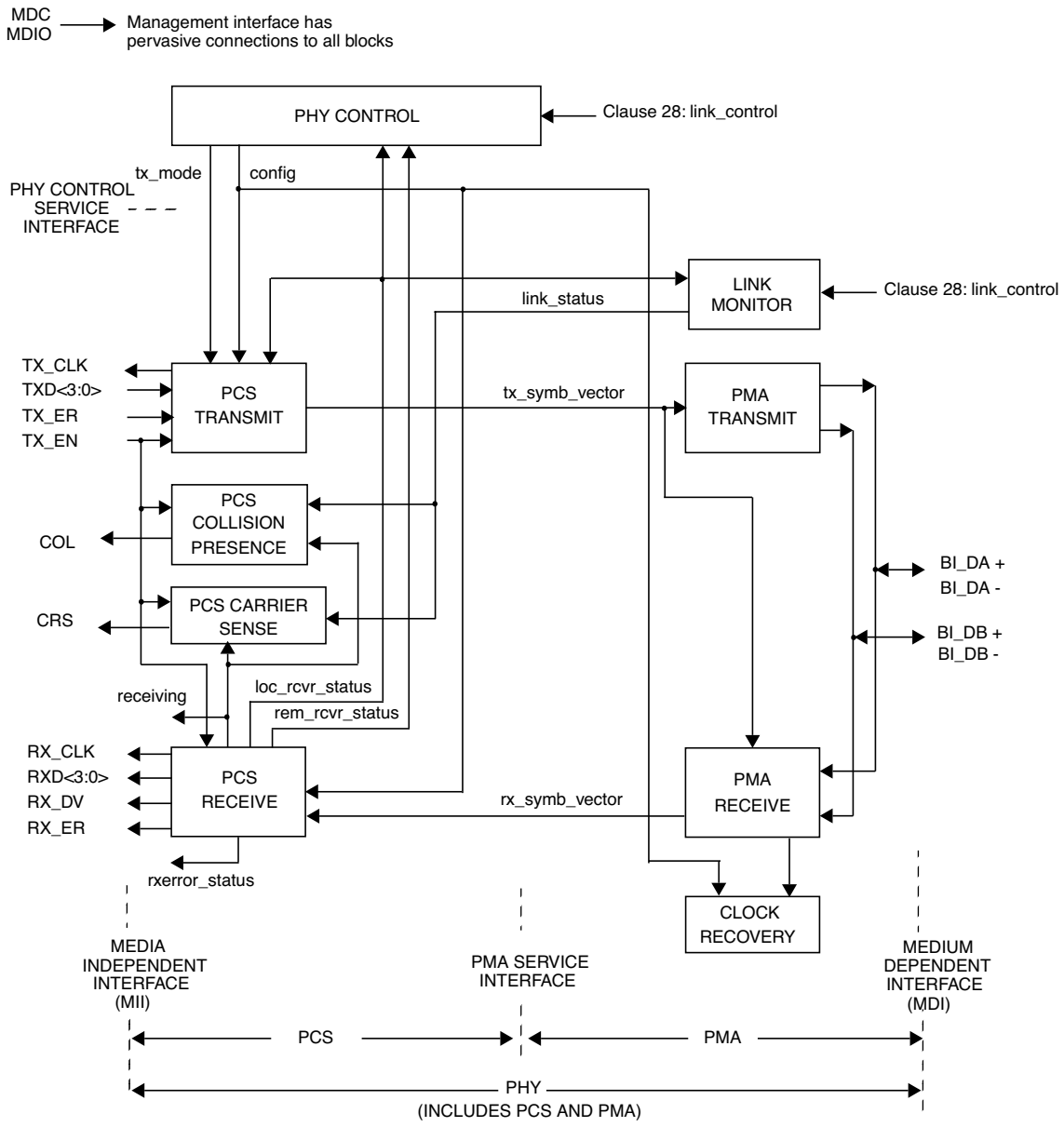


Figure 32–4—Division of responsibilities between 100BASE-T2 PCS, PMA, and PHY Control

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32.1.2.1 Physical coding sublayer (PCS)

The 100BASE-T2 PCS couples an MII, as described in Clause 22, to a PMA sublayer.

The functions performed by the PCS comprise the generation of continuous quinary symbol sequences to be transmitted over each wire pair. During *data mode*, i.e., when a data stream from the MII is transmitted, the four bits representing the TXD<3:0> data nibble are scrambled by a side-stream scrambler and encoded into a pair of quinary symbols. During *idle mode*, i.e., between transmission of consecutive data streams, the sequences of quinary symbols are generated with an encoding rule that differs from the encoding rule used in data mode. Through this technique, sequences of arbitrary quinary symbols that represent data can easily be distinguished from sequences that represent the idle mode. Furthermore, idle mode encoding takes into account the information of whether the local PHY is operating reliably or not and allows conveying this information to the remote station. A transition from the idle to the data mode is signaled by inserting a Start-of-Stream delimiter that consists of a pattern of two consecutive pairs of quinary symbols. Similarly, the end of a data stream transmission is signaled by inserting an End-of-Stream delimiter that also consists of a pattern of two consecutive pairs of quinary symbols. Further patterns are reserved for signaling a transmit error during transmission of a data stream.

PCS Receive processes pairs of quinary symbols provided by the PMA. It detects the beginning and the end of streams of data and, during the reception of a data stream, descrambles and decodes the received quinary symbol pairs into nibbles RXD<3:0> that are passed to the MII. PCS Receive also detects errors in the received sequences and signals them to the MII. Furthermore, the PCS contains a PCS Carrier Sense function, a PCS Collision Presence function, and a management interface.

The PCS functions and state diagrams are specified in 32.3. The signals provided by the PCS at the MII conform to the interface requirements of Clause 22. The PCS interfaces to PHY Control and to the PMA are abstract message-passing interfaces specified in 32.2 and 32.4, respectively.

32.1.2.2 PMA sublayer

The PMA couples messages from the PMA service interface onto the balanced cabling physical medium. The PMA provides dual-duplex communications at 25 MBd over two pairs of balanced cabling up to 100 m in length.

The PMA Transmit function comprises two independent transmitters to generate five-level pulse-amplitude modulated signals on each of the two pairs BI_DA and BI_DB, as described in 32.4.1.1.2.

The PMA Receive function comprises two independent receivers for five-level pulse-amplitude modulated signals on each of the two pairs BI_DA and BI_DB, as described in 32.4.1.1.3. The receivers are responsible for acquiring clock, and providing quinary symbol pairs to the PCS as defined by the PMA_UNITDATA.indicate message. The PMA also contains functions for Link Monitor.

PMA functions and state diagrams are specified in 32.4. PMA electrical specifications are given in 32.6.

32.1.2.3 PHY Control function

PCS and PMA sublayer operations are controlled via signals generated by the PHY Control function. PHY Control does not itself represent a sublayer but rather a logical grouping of the control functions necessary for proper operations of a 100BASE-T2 transceiver.

PHY Control determines whether the PHY should operate in a normal state, where packets can be exchanged over the link segment, or whether the PHY should be forced to send quinary symbol sequences that represent the idle mode. The latter occurs when either one of the PHYs, or both PHYs, that share a link segment are not operating reliably.

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The PHY Control function and state diagram are specified in 32.2, prior to introducing the PCS and PMA functional specifications. The PHY Control interface to the PCS and PMA sublayer is an abstract message-passing interface also specified in 32.2.

32.1.3 Application of 100BASE-T2

32.1.3.1 Compatibility considerations

All implementations of the balanced cabling link shall be compatible at the MDI. The PCS, PMA, and the medium are defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided the MDI and MII specifications are met.

32.1.3.2 Incorporating the 100BASE-T2 PHY into a DTE

When the PHY is incorporated within the physical bounds of a DTE, conformance to the MII is optional, provided that the observable behavior of the resulting system is identical to that of a system with a full MII implementation. For example, an integrated PHY may incorporate an interface between PCS and MAC that is logically equivalent to the MII, but does not have the full output current drive capability called for in the MII specification.

32.1.3.3 Use of 100BASE-T2 PHY for point-to-point communication

The 100BASE-T2 PHY, in conjunction with the MAC specified in Clauses 1 through 4 (including parameterized values in 4.4.2.3 to support 100 Mb/s operation) may be used at both ends of a link for point-to-point applications between two DTEs. Such a configuration does not require a repeater. In this case each PHY may connect through an MII to its respective DTE. Optionally, either PHY (or both PHYs) may be incorporated into the DTEs without an exposed MII.

32.1.3.4 Auto-Negotiation requirement

Full Auto-Negotiation, as specified in Clause 28, shall be included in all compliant implementations.

32.1.4 State diagram conventions

The body of this clause and its associated annexes contain state diagrams, including definitions of variables, constants and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram shall prevail. The notation used in the state diagrams follows the conventions of 21.5.

32.2 PHY Control functional specifications and service interface

32.2.1 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY in a mode of operation during which packets can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 32–5.

During Auto-Negotiation, PHY Control ensures that the transmitter is disabled. When the Auto-Negotiation process asserts link_control=ENABLE, PHY Control enters the TRAINING state. During training, PHY Control enforces transmission in the idle mode by setting tx_mode=SEND_I and the PHY transmits sequences of quinary symbols encoded with the parameter loc_rcvr_status=NOT_OK. When the PHY achieves successful training and establishes proper receiver operations, PCS Receive asserts the parameter loc_rcvr_status=OK, and PCS Transmit conveys this information to the link partner via idle transmission.

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The criterion for assertion of the parameter loc_rcvr_status is left to the implementor. It can be based, for example, on observing the mean-square error at the decision point of the receiver or detecting errors during reception of symbol streams that represent the idle mode. Upon observation that the remote PHY also operates reliably (rem_rcvr_status=OK), the normal mode of operation is entered where transmission of packets over the link segment can take place.

The normal mode of operation corresponds to the SEND IDLE OR DATA state, where PHY Control asserts tx_mode=SEND_N. In this state, when no packets have to be sent, idle mode transmission takes place. Encoding of quinary symbols is realized with the parameter loc_rcvr_status = OK.

If during the normal mode of operation unsatisfactory receiver operations is detected (loc_rcvr_status=NOT_OK), transmission of the current packet, if any, is completed and PHY Control enters the TRAINING state.

Whenever a PHY that operates reliably detects unsatisfactory operation of the remote PHY (rem_rcvr_status=NOT_OK), it enters the SEND IDLE state where tx_mode=SEND_I is asserted and idle transmission takes place. In this state, encoding is performed with the parameter loc_rcvr_status=OK. As soon as the remote PHY signals satisfactory receiver operation (rem_rcvr_status=OK), the SEND IDLE OR DATA state is entered. Note that if in the SEND IDLE state loc_rcvr_status takes the value NOT_OK transition to the TRAINING state occurs.

PHY Control may force the transmit scrambler state to be initialized to a random value by requesting the execution of the PCS Reset function defined in 32.3.1.1.

32.2.2 PHY Control Service interface

The following specifies the services provided by PHY Control. These services are described in an abstract manner and do not imply any particular implementation.

The following primitives are defined:

PHYC_CONFIG.indicate
PHYC_TXMODE.indicate
PHYC_RXSTATUS.request
PHYC_REMRXSTATUS.request

The parameter link_control is identical to the link_control parameter defined for the PMA Service interface in 32.4.2.4.

32.2.2.1 PHYC_CONFIG.indicate

Each PHY in a 100BASE-T2 link is configured as a master PHY or as a slave PHY. Master/slave configuration is determined during Auto-Negotiation (see 32.5). The result of this negotiation is provided to PHY Control.

32.2.2.1.1 Semantics of the primitive

PHYC_CONFIG.indicate (config)

PHYC_CONFIG.indicate specifies to PCS and PMA Clock Recovery via the parameter config whether the PHY must operate as a master PHY or as a slave PHY. The parameter config can take on one of two values of the form:

MASTER This value is continuously asserted when the PHY must operate as a master PHY.

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SLAVE — This value is continuously asserted when the PHY must operate as a slave PHY.

32.2.2.1.2 When generated

PHY Control shall generate PHYC_CONFIG.indicate messages synchronously with every MII TX_CLK cycle.

32.2.2.1.3 Effect of receipt

Upon reception of this primitive, PCS and PMA Clock Recovery shall perform their functions in master or slave configuration according to the value assumed by the parameter config.

32.2.2.2 PHYC_TXMODE.indicate

The transmitter in a 100BASE-T2 link normally sends over the two pairs quinary symbols that can represent an MII data stream or the idle mode.

32.2.2.2.1 Semantics of the primitive

PHYC_TXMODE.indicate (tx_mode)

PHYC_TXMODE.indicate specifies to PCS Transmit via the parameter tx_mode what sequence of quinary symbols the PCS should be transmitting. The parameter tx_mode can take on one of two values of the form:

SEND_N — This value is continuously asserted when transmission of sequences of quinary symbols representing an MII data stream or the idle mode is to take place.

SEND_I — This value is continuously asserted in case transmission of sequences of quinary symbols representing the idle mode is to take place.

32.2.2.2.2 When generated

PHY Control shall generate PHYC_TXMODE.indicate messages synchronously with every MII TX_CLK cycle.

32.2.2.2.3 Effect of receipt

Upon receipt of this primitive, the PCS shall perform its Transmit function as described in 32.3.1.2.

32.2.2.3 PHYC_RXSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the receive link for the local PHY. The parameter loc_rcvr_status conveys to PHY Control and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by PCS Transmit encoding functions.

32.2.2.3.1 Semantics of the primitive

PHYC_RXSTATUS.request (loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the form:

OK — This value is asserted and remains true during reliable operation of the receive link for the local PHY.

NOT_OK — This value is asserted whenever operation of the receive link for the local PHY is unreliable.

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32.2.2.3.2 When generated

PCS Receive shall generate PHYC_RXSTATUS.request messages synchronously with signals received at the MDI. It shall prevent that the value of the parameter loc_rcvr_status is modified while TX_EN=1 in order to avoid that a transition from data to idle mode or from idle to data mode occurs while a packet is being presented to the PCS at the MII.

32.2.2.3.3 Effect of receipt

The effect of receipt of this primitive is specified in 32.2.5 and 32.4.1.3.3.

32.2.2.4 PHYC_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link as communicated by the remote PHY. The parameter rem_rcvr_status conveys to PHY Control the information on whether reliable operation of the remote PHY is detected or not.

32.2.2.4.1 Semantics of the primitive

PHYC_REMRXSTATUS.request (rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK	The receive link for the remote PHY is operating reliably.
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected.

32.2.2.4.2 When generated

The PCS shall generate PHYC_REMRXSTATUS.request messages synchronously with signals received at the MDI.

32.2.2.4.3 Effect of receipt

The effect of receipt of this primitive is specified in 32.2.5.

32.2.3 State diagram variables

link_control
: See 32.4.1.3.1.

link_status
: See 32.4.1.3.1.

loc_rcvr_status
: Variable set by the PCS Receive function to indicate correct or incorrect operation of the receive link for the local PHY.

  Values: OK: the receive link for the local PHY is operating reliably,
  NOT_OK: operation of the receive link for the local PHY is not reliable.

pma_reset
: Allows reset of all PMA functions.

  Values: ON and OFF

  Set by: PMA Reset

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rem_rcvr_status
: Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not.

  Values: OK: the receive link for the remote PHY is operating reliably,
  NOT_OK: reliable operation of the receive link for the remote PHY is not detected.

tx_mode
: PCS Transmit shall send quinary symbols according to the value assumed by this variable.

  Values: SEND_N: transmission of sequences of quinary symbols representing an MII data stream, the idle mode, or control signals shall take place,
  SEND_I: transmission of sequences of quinary symbols representing the idle mode shall take place.

32.2.4 State diagram timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

maxwait_timer
: A timer used to measure the amount of time during which a receiver dwells in the TRAINING state. The timer shall expire 2500–3000 ms after entering the TRAINING state.

minwait_timer
: A timer used to measure the amount of time during which a receiver waits in the SEND IDLE OR DATA, the TRAINING, or the SEND IDLE state before being allowed to leave the current state. The timer shall expire 128T = 5.12 μs after being started.

32.2.5 PHY Control state diagram

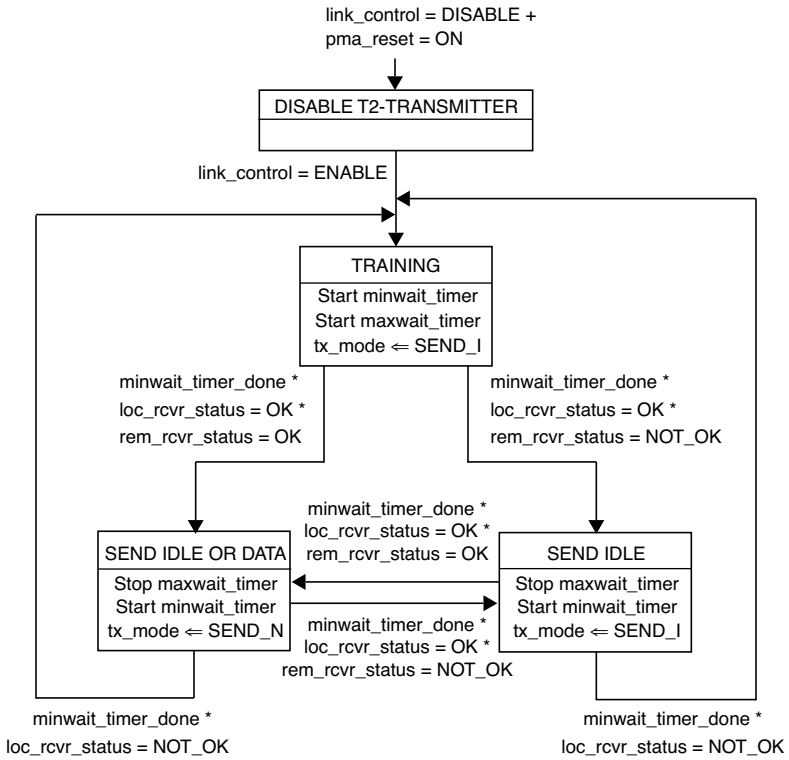


Figure 32–5—PHY Control state diagram

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32.3 PCS functional specifications

The PCS comprises one PCS Reset function and four simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit, PCS Receive, PCS Carrier Sense, and PCS Collision Presence. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 32–5, shows how the four operating functions relate to the messages of the PCS-PMA and the PCS-PHY Control interfaces. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive, and are not shown in Figure 32–5. The management functions are specified in Clause 30. See also Figure 32–7, which presents a block diagram helpful for understanding the definitions of PCS Transmit function variables, and Figure 32–11, which defines the structure of frames passed from PCS to PMA.

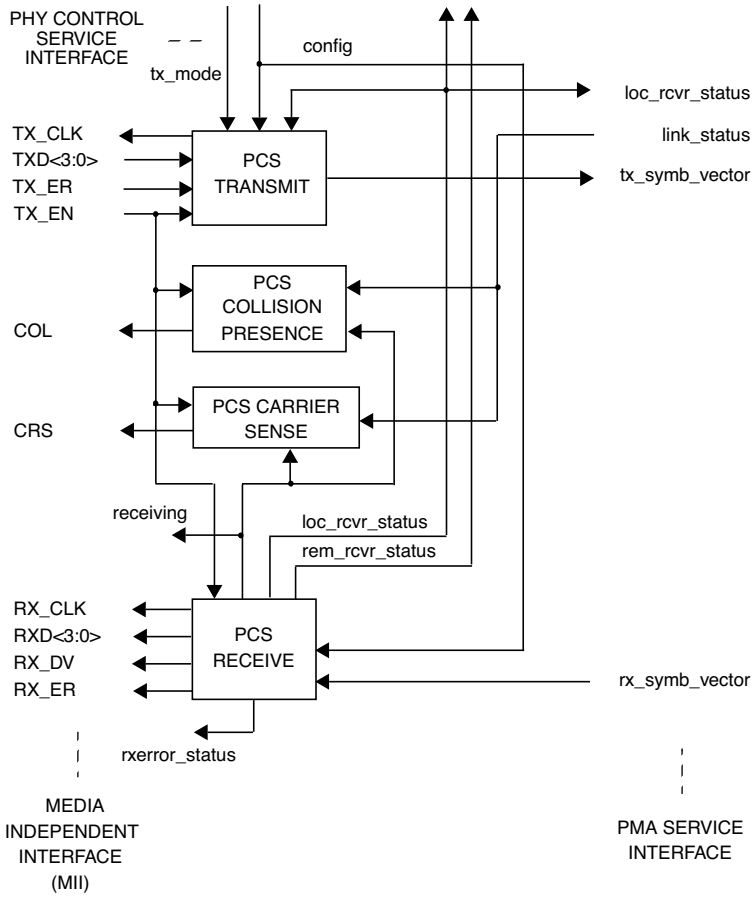


Figure 32-6—PCS reference diagram

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32.3.1 PCS functions

32.3.1.1 PCS Reset function

The PCS Reset function shall be executed any time one of three conditions occurs. These three conditions are "power on," the receipt of a request for reset from the management entity, and the receipt of a request for reset from PHY Control. PCS Reset initializes all PCS functions. PCS Reset sets pcs_reset = ON for the duration of its Reset function. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

32.3.1.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 32–12.

In normal mode of operation, the tx_mode parameter, which is transferred from PHY Control to the PCS via the PHYC_TXMODE.indicate message, assumes the value tx_mode=SEND_N, and the PCS Transmit function generates at each symbol period pairs of quinary symbols that represent data or the idle mode. A symbol period T is equal to 40 ns. A time index n, where n is an integer, is introduced to establish a temporal relationship between different symbol periods. The tx_symb_vector parameter at time n is a two-element vector of quinary symbols (A_n, B_n) that is transferred to the PMA via PMA_UNITDATA.request. The PMA shall transmit symbols A_n and B_n over wire pairs BI_DA and BI_DB, respectively. During transmission of data, the four bits representing the TXD<3:0> data nibble are scrambled by the OCS using a side-stream scrambler then encoded into a pair of quinary symbols and transferred to the PMA. The idle mode is signaled by a sequence of pairs of quinary symbols that are also generated using the side-stream transmit scrambler. However, the encoding rules by which the quinary symbols are obtained are different for the data and the idle modes. This allows, at the receiver, sequences of quinary symbol pairs that represent data to be distinguished from sequences of quinary symbol pairs that represent the idle mode. A transition from the idle mode to the data mode is signalled by inserting a Start-of-Stream delimiter that consists of a pattern of two consecutive pairs of quinary symbols. Similarly, the end of transmission of data is signalled by an End-of-Stream delimiter that also consists of a pattern of two consecutive pairs of quinary symbols. Further patterns are reserved for signaling the assertion of TX_ER within a stream of data.

If tx_mode = SEND_I is asserted, PCS Transmit generates sequences of symbol pairs (A_n, B_n) according to the encoding rule in idle mode. Idle mode encoding takes into account the value of the parameter loc_rcvr_status. By this mechanism, a PHY indicates during idle transmission the status of its own receiver to the link partner.

The PCS Transmit reference diagram is shown in Figure 32–7. PCS encoding involves the generation of the three-bit words Sa_n[2:0], Sb_n[2:0], Ta_n[2:0], and Tb_n[2:0], from which the pairs of quinary symbols (A_n, B_n) are obtained. The three-bit words Sa_n[2:0] and Sb_n[2:0] are determined first, as explained in 32.3.1.2.2, from sequences of random binary symbols derived from the transmit side-stream scrambler. The generation of Ta_n[2:0] and Tb_n[2:0] and the quinary symbols A_n and B_n is given in 32.3.1.2.3. The physical structure represented in Figure 32–7 is not required. Implementors are free to construct any logical devices having functionality identical to that described by the following specifications and the PCS Transmit state diagram.

32.3.1.2.1 Side-stream scrambler polynomials

The PCS Transmit function employs side-stream scrambling. If the parameter config provided to the PCS by the PHY Control function via the PHYC_CONFIG.indicate message assumes the value MASTER, PCS Transmit shall employ

$$g_M(x) = 1 + x^{13} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. If config = SLAVE, PCS Transmit shall employ

$$g_S(x) = 1 + x^{20} + x^{33}$$

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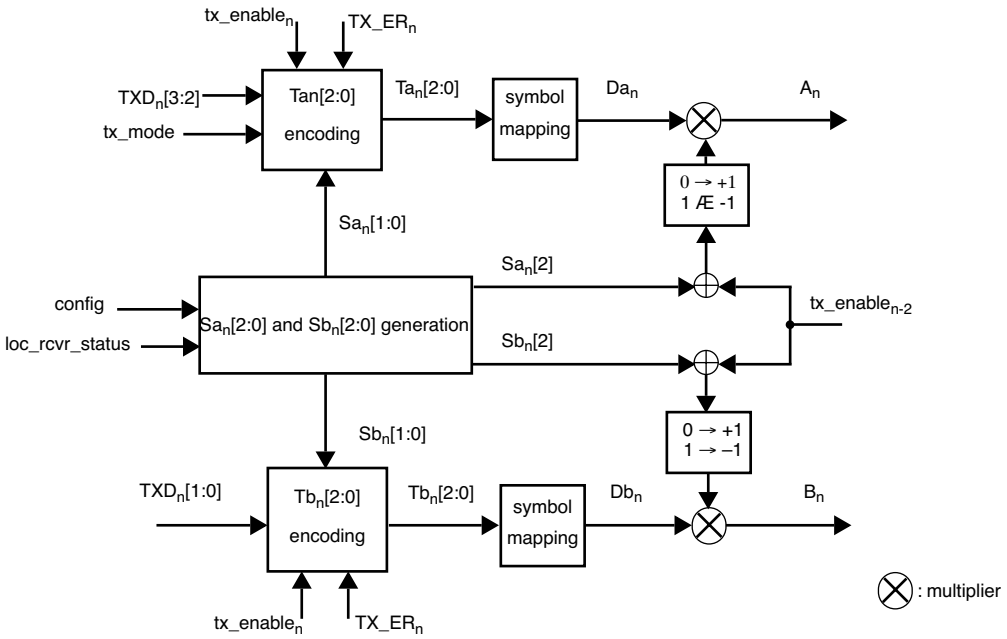
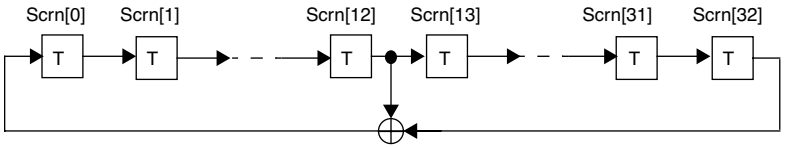
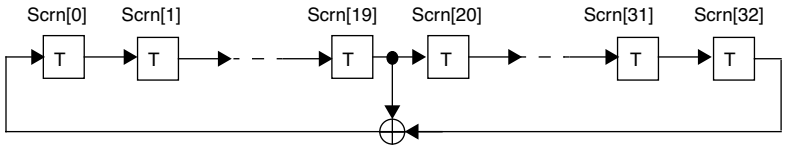


Figure 32–7—PCS Transmit reference diagram

as transmitter side-stream scrambler generator polynomial. The implementation of master and slave PHY side-stream scramblers by linear-feedback shift registers is shown in Figure 32–8. The bits stored in the shift register delay line at time n are denoted by Scr$_n$[32:0]. At each symbol period, the shift register is advanced by one bit and one new bit represented by Scr$_n$[0] is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are randomly set. The generation of the random bits is left to the implementor.



a) Side-stream scrambler employed by the master PHY



b) Side-stream scrambler employed by the slave PHY

Figure 32–8—Realization of side-stream scramblers by linear feedback shift registers

32.3.1.2.2 Generation of bits Sa$_n$[2:0] and Sb$_n$[2:0]

PCS Transmit encoding rules are based on the generation, at time n, of the four bits Sx$_n$, Sy$_n$, Sa$_n$[2], and Sb$_n$[2]. These four bits are mutually uncorrelated and also uncorrelated with the bit Scr$_n$[0] in data and idle

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modes. For both master and slave PHYs, they are obtained by the same linear combinations of bits stored in the transmit scrambler shift register delay line. The four bits are elements of the same maximum-length shift register sequence of length $2^{33} - 1$ as $Scr_n[0]$, but shifted in time. The associated delays are all large and different, such that there is no apparent correlation among the five bits $Scr_n[0]$, Sx_n, Sy_n, $Sa_n[2]$, and $Sb_n[2]$. The bits Sx_n and Sy_n are given by

$$Sx_n = Scr_n[3] \oplus Scr_n[8]$$

$$Sy_n = Scr_n[4] \oplus Scr_n[6]$$

where $\oplus$ denotes the XOR logic operator. Four bits $X_n[1:0]$ and $Y_n[1:0]$ are obtained by

$$X_n[0] = \begin{cases} Sx_n & \text{if } \{n - n_0 = 0 \pmod 2 \text{ or loc\_rcvr\_status = OK }\} \\ Sx_n \oplus 1 & \text{else} \end{cases}$$

$$X_n[1] = X_n[0] \oplus 1$$

$$Y_n[0] = \begin{cases} Sy_n & \text{if } n - n_0 = 0 \pmod 2 \\ Sy_{n-1} \oplus 1 & \text{else} \end{cases}$$

$$Y_n[1] = Y_n[0]$$

where n_0 denotes the time index of the last transmitter side-stream scrambler reset.

The bits San[2:0] and Sbn[2:0] are given by

$$Sa_n[2] = Scr_n[1] \oplus Scr_n[5]$$

$$Sa_n[1:0] = \begin{cases} X_n[1:0] & \text{if } Scr_n[0] = 1 \\ Y_n[1:0] & \text{else} \end{cases}$$

$$Sb_n[2] = Scr_n[2] \oplus Scr_n[12]$$

$$Sb_n[1:0] = \begin{cases} Y_n[1:0] & \text{if } Scr_n[0] = 1 \\ X_n[1:0] & \text{else} \end{cases}$$

32.3.1.2.3 Generation of sequences A_n and B_n

If tx_mode = SEND_N, the PCS Transmit function generates sequences A_n and B_n that represent either a stream of data or an idle mode. If tx_mode = SEND_I, idle transmission is enforced. The encoding rule is determined by the value of the signal tx_enable_n, given by

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$$\text{tx\_enable}_n = \begin{cases} TX\_EN_n & \text{if tx\_mode = SEND\_N} \\ 0 & \text{else} \end{cases}$$

where TX_EN_n represents the MII signal TX_EN at time n. If $\text{tx\_enable}_n = 1$, transmission of a stream of data takes place. As illustrated in Figure 32–11, the definition of a Start-of-Stream Delimiter ("SSD") is related to the condition $SSD_n = (\text{tx\_enable}_n) * (!\ \text{tx\_enable}_{n-2}) = 1$, where "*" and "!" denote the logic AND and NOT operators, respectively. For the generation of "SSD", PCS Transmit replaces the first two nibbles of the preamble in a data stream with the symbols defined below. Similarly, the definition of an End-of-Stream Delimiter (ESD) is related to the condition $ESD_n = (!\ \text{tx\_enable}) * (\text{tn\_enable}_{n-2}) = 1$. This occurs during the first two symbol periods after transmission of the last nibble of a data stream.

The symbols A_n and B_n are obtained from the three-bit words $Ta_n[2:0]$ and $Tb_n[2:0]$ whose definitions in the data and the idle modes are given below.

Data mode (tx_enable_n=1):

Definition of "SSD":

$Ta_n[2:0] = [1, 0, 0]$

$Tb_n[2:0] = [!\text{tx\_enable}_{n-1}, \text{tx\_enable}_{n-2}, \text{tx\_enable}_{n-2}]$

A most significant bit $Ta_n[2]$=1 or $Tb_n[2]$=1 results in the transmission of a symbol that can be interpreted as an ESC symbol.

Encoding of data nibbles:

$$Ta_n[2:0] = [0, (Sa_n[1] \oplus TXD_n[3]), (Sa_n[0] \oplus TXD_n[2] \oplus 1)]$$

$$Tb_n[2:0] = [0, (Sb_n[1] \oplus TXD_n[1]), (Sb_n[0] \oplus TXD_n[0] \oplus 1)]$$

where $TXD_n[3:0]$ denotes the data nibble TXD[3:0] at time n.

Encoding of error indication:

If TX_ER_n=1 is asserted, where TX_ER_n denotes the value of the signal TX_ER at time n, error indication is signaled by means of the ESC and 0 symbols. The encoding rule is given by

$$Ta_n[2:0] = [(Sa_n[1] \oplus Sa_n[0]), 0, 0]$$

$$Tb_n[2:0] = [(Sb_n[1] \oplus Sb_n[0]), 0, 0]$$

Idle mode (tx_enable_n=0):

Definition of "ESD":

$Ta_n[2:0] = [1, 0, 0]$

$Tb_n[2:0] = [\text{tx\_enable}_{n-1}, !\text{tx\_enable}_{n-2}, !\text{tx\_enable}_{n-2}]$

Encoding in the idle mode:

$$Ta_n[2:0] = [0, Sa_n[1], Sa_n[0]]$$

$$Tb_n[2:0] = [0, Sb_n[1], Sb_n[0]]$$

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The mapping of $Ta_n[2:0]$ and $Tb_n[2:0]$ into quinary symbols Da_n and Db_n is given in Figure 32–9. This mapping ensures that the symbols representing data are Gray coded. The quinary symbols A_n and B_n are obtained from Da_n and Db_n by

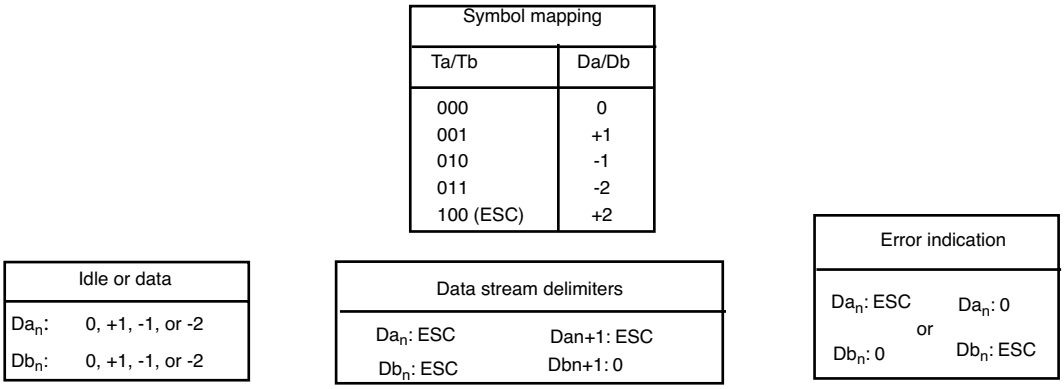


Figure 32–9—Symbol mapping and encoding rule summary

$$A_n = \begin{cases} Da_n & \text{if } \mathrm{Sa}_n[2] \oplus \mathrm{tx\_enable}_{n-2} = 0 \\ -Da_n & \text{else} \end{cases}$$

$$B_n = \begin{cases} Db_n & \text{if } \mathrm{Sb}_n[2] \oplus \mathrm{tx\_enable}_{n-2} = 0 \\ -Db_n & \text{else} \end{cases}$$

With the rules defined in this subclause, if in idle mode a transmitted symbol on one wire pair belongs to the set {–2,0,+2}, the symbol on the other wire pair belongs to the set {–1,+1}. Moreover, one of the quinary symbols that are transmitted at time $2(n–n_0)$ and $2(n–n_0)+1$ is guaranteed to be either +2 or –2. Both in data and idle modes, the symbol sequences on each wire pair can be modeled as sequences of independent and identically distributed quinary symbols. The symbol constellations and symbol probabilities for these two modes are shown in Figure 32–10. The average symbol energy is the same in data and idle modes.

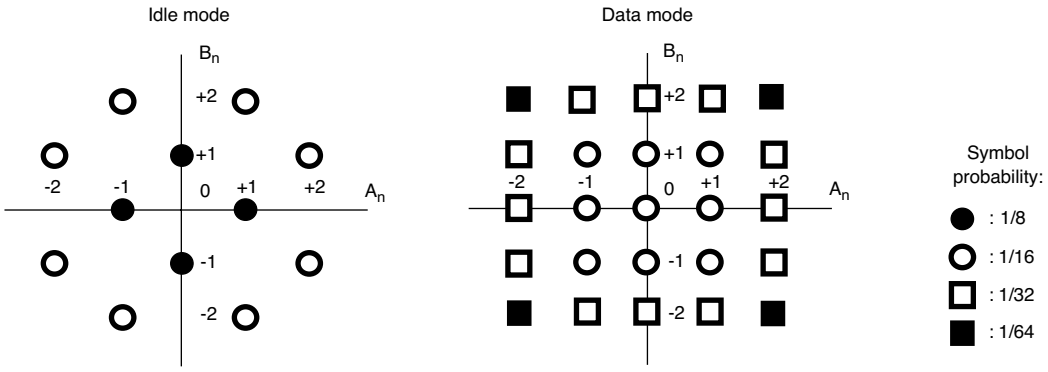


Figure 32–10—Symbol constellations in idle and data modes

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32.3.1.3 PCS Receive function

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 32–13.

The PCS Receive function accepts pairs of detected quinary symbols provided by the PMA Receive function via the parameter rx_symb_vector. To achieve correct operation, PCS Receive uses the knowledge of the encoding rules that are employed in the idle mode. For example, the property that in the idle mode if A_n belongs to the set {–2,0,+2} then B_n belongs to the set {–1,+1}, and vice versa, can be used to acquire the correct state for the receiver side-stream descrambler, and to determine which detected quinary symbol was transmitted on wire pair BI_DA and which on wire pair BI_DB. Also, correct polarity of the detected quinary symbols can reliably be obtained by ensuring in the idle mode that the encoding rule holds whenever a –2 symbol is received. PCS Receive generates the sequence of vectors of two quinary symbols (RA_n, RB_n) and indicates the reliability of receiver operations by setting the parameter loc_rcvr_status to OK (logic high) or NOT_OK (logic low). The sequence (RA_n, RB_n) is processed to generate the signals RXD<3:0>, RX_DV, and RX_ER, which are presented to the MII. PCS Receive detects the transmission of a stream of data from the remote station and conveys this information to the PCS Carrier Sense and PCS Collision Presence functions via the parameter receiving.

32.3.1.3.1 Receiver descrambler polynomials

For side-stream descrambling, the master PHY shall employ the receiver descrambler generator polynomial $g'_M(x) = 1 + x^{20} + x^{33}$, and the slave PHY shall employ the receiver descrambler generator polynomial $g'_S(x) = 1 + x^{13} + x^{33}$.

32.3.1.3.2 Decoding of quinary symbols

At the beginning of a stream of data, PCS Receive detects “SSD” and asserts the signal RX_DV. Detection of “SSD” is achieved by processing two consecutive vectors (RA_{n-1}, RB_{n-1}) and (RA_n, RB_n) at each time n. Upon detection of “SSD,” PCS Receive also assigns the value TRUE to the parameter receiving that is provided to the PCS Carrier Sense and Collision Presence functions.

Table 32–1 shows the mapping of symbols RA_n and RB_n into two-bit words Qa_n[1:0] and Qb_n[1:0] that are descrambled and decoded to generate nibbles of data RXD[3:0].

Table 32–1—Inverse quinary symbol mapping

RA_n/RB_n	$Qa_n[1:0]/Qb_n[1:0]$
0	00
+1	01 or 10
–1	01 or 10
± 2	11

The mapping shown in Table 32–1 corresponds to the inverse of the encoding function employed by PCS Transmit. For example, a symbol $A_n = +1$ is generated by Ta_n[1:0] being equal to “01” or “10.” Hence, in the above table the value of Qa_n[1:0] for $RA_n = +1$ is specified as being equal to “01 or 10.” Similarly for other entries in the table.

During reception of a stream of data, PCS Receive checks that the symbols RA_n and RB_n follow the encoding rule defined in 32.3.1.2 whenever they assume values ± 2. PCS Receive processes two consecutive vectors at each time n to detect “ESD.” Upon detection of “ESD,” PCS Receive de-asserts the signal RX_DV, and assigns the value FALSE to the parameter receiving. If a violation of the encoding rules is detected, PCS

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Receive asserts the signal RX_ER for at least one symbol period. During reception of an idle sequence, PCS Receive checks that the symbols RA_n and RB_n follow the encoding rule defined in 32.3.1.2.

32.3.1.4 PCS Carrier Sense function

The PCS Carrier Sense function shall conform to the PCS Carrier Sense state diagram in Figure 32–14.

The PCS Carrier Sense function controls the MII signal CRS according to the rules presented in this clause. While link_status = OK, CRS is asserted whenever receiving=TRUE or TX_EN=1.

32.3.1.5 PCS Collision Presence function

A PCS collision is defined as the simultaneous occurrence of TX_EN=1 and the assertion of the parameter receiving=TRUE while link_status=OK. While a PCS collision is detected, the MII signal COL shall be asserted. At other times COL shall remain de-asserted.

32.3.2 PCS interfaces

32.3.2.1 PCS–MII interface signals

The signals in Table 32–2 are formally defined in 22.2.2. Jabber detection as specified in 22.2.4.2.12 is not required by this standard.

Table 32–2—MII interface signals

Signal name	Meaning	Subclause
TX_CLK	Transmit clock	22.2.2.1
RX_CLK	Receive clock	22.2.2.2
TX_EN	Frames transmit data	22.2.2.3
TXD<3:0>	Transmit data	22.2.2.4
TX_ER	Forces transmission of illegal code	22.2.2.5
RX_DV	Frames receive SFD and DATA	22.2.2.6
RXD<3:0>	Receive data	22.2.2.7
RX_ER	Receive error indication	22.2.2.8
CRS	Non-idle medium indication	22.2.2.9
COL	Collision indication	22.2.2.10
MDC	Management data clock	22.2.2.11
MDIO	Management data	22.2.2.12

32.3.2.2 PCS–management entity signals

The management interface has pervasive connections to all functions. Operation of the management control lines MDC and MDIO, and requirements for managed objects inside the PCS and PMA, are specified in Clauses 22 and 30, respectively.

No spurious signals shall be emitted onto the MDI when the PHY is held in power down mode as defined in 22.2.4.1.5, independently of the value of TX_EN, or when released from power down mode, or when external power is first applied to the PHY.

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32.3.3 Frame structure

Frames passed from the PCS to the PMA sublayer shall have the structure shown in Figure 32–11. This figure shows the temporal relationship between the signals tx_enable$_n$, and TXD[3:0] and the sequences of quinary symbol pairs (A_n, B_n) in correspondence of transitions from the idle mode to transmission of data and vice versa. Time proceeds from left to right in the figure.

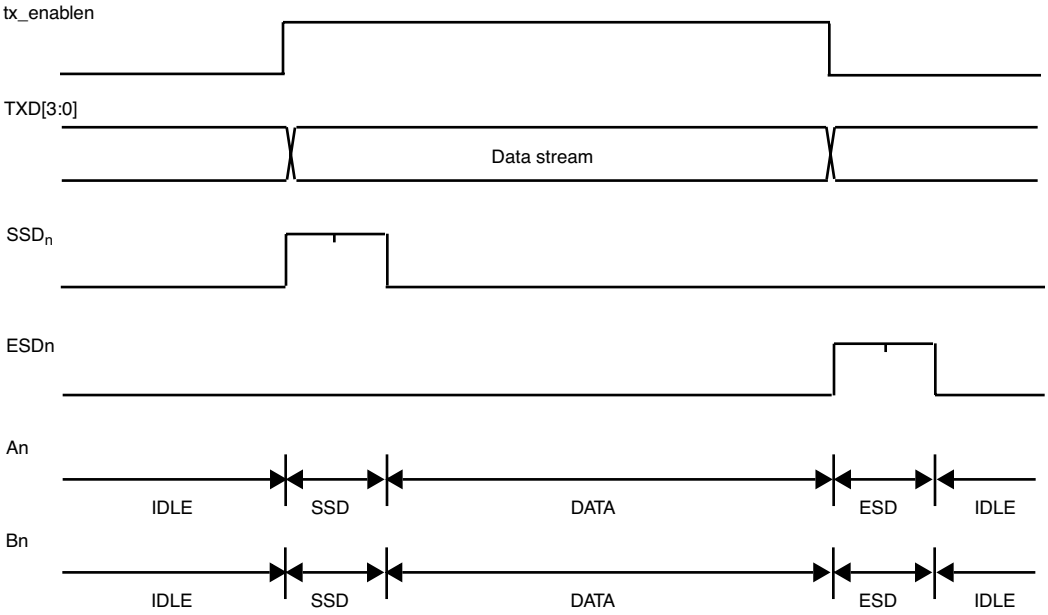


Figure 32–11—PCS sublayer to PMA sublayer frame structure

32.3.4 State variables

32.3.4.1 Variables

COL

The COL signal of the MII as specified in Clause 22.

config

The config parameter set by PHY Control and passed to the PCS via the PHYC_CONFIG.indicate primitive.
Values: MASTER and SLAVE.

CRS

The CRS signal of the MII as specified in Clause 22.

DATA

A sequence of vectors of two quinary symbols corresponding to valid data, as specified in 32.3.1.2.

ESD

Two consecutive vectors of two quinary symbols corresponding to the End-of-Stream delimiter, as specified in 32.3.1.2.

IDLE

A sequence of vectors of two quinary symbols generated in idle mode, as specified in 32.3.1.2.

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link_status

The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indicate primitive.
Values: OK, READY, and FAIL

loc_rcvr_status

The loc_rcvr_status parameter generated by PCS Receive.
Values: OK and NOT_OK

pcs_reset

The pcs_reset parameter set by the PCS Reset function.
Values: ON and OFF

(RA_n, RB_n)

The vector of the two correctly aligned most recently received quinary symbols generated by PCS Receive.

receiving

The receiving parameter generated by the PCS Receive function.
Values: TRUE and FALSE

rxerror_status

The rxerror_status parameter set by the PCS Receive function. Although this variable is set by PCS Receive, it achieves the same function as the variable rxerror_status of Clause 24 that is set by PMA and communicated through the PMA_RXERROR.indicate primitive.
Values: ERROR and NO_ERROR

RX_DV

The RX_DV signal of the MII as specified in Clause 22.

RX_ER

The RX_ER signal of the MII as specified in Clause 22.

rx_symb_vector

A vector of two quinary symbols received by the PMA and passed to the PCS via the PMA_UNITDATA.indicate primitive.
Value: SYMB_PAIR

RXD[3:0]

The RXD<3:0> signal of the MII as specified in Clause 22.

SSD

Two consecutive vectors of two quinary symbols corresponding to the Start-of-Stream delimiter, as specified in 32.3.1.2.

tx_enable

The tx_enable parameter generated by PCS Transmit as specified in 32.3.1.2.3.

TX_ER

The TX_ER signal of the MII as specified in Clause 22.

tx_mode

The tx_mode parameter set by PHY Control and passed to the PCS via the

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PHYC_TXMODE.indicate primitive.
Values: SEND_N and SEND_I

tx_symb_vector

A vector of two quinary symbols generated by the PCS Transmit function and passed to the PMA via the PMA_UNITDATA.request primitive.
Value: SYMB_PAIR

32.3.4.2 Timer

symb_timer

A continuous free-running timer. The condition symb_timer_done becomes true upon timer expiration.

Restart time: Immediately after expiration; timer restart resets the condition symb_timer_done.

Duration: 40 ns nominal.

TX_CLK shall be generated synchronously with symb_timer (see tolerance required for TX_CLK in 32.6.1.2.6). In the PCS Transmit state diagram, the message PMA_UNITDATA.request is issued concurrently with symb_timer_done.

32.3.4.3 Messages

PMA_UNITDATA.indicate (rx_symb_vector)
A signal sent by PMA Receive indicating that a vector of two quinary symbols is available in rx_symb_vector.

PMA_UNITDATA.request (tx_symb_vector)
A signal sent to PMA Transmit indicating that a vector of two quinary symbols is available in tx_symb_vector.

32.3.5 State diagrams

32.3.5.1 PCS Transmit

PCS Transmit sends vectors of two quinary symbols to the PMA via the tx_symb_vector parameter. In normal mode of operation, between streams indicated by the parameter tx_enable, PCS Transmit generates sequences of vectors using the encoding rules defined for the idle mode. Upon assertion of tx_enable, PCS Transmit passes an "SSD" of two consecutive vectors of two quinary symbols to the PMA replacing the preamble bits of a stream of data during these two symbol periods. Following the "SSD," each TXD<3:0> nibble is encoded into a vector of two quinary symbols until tx_enable is de-asserted. If, while tx_enable is asserted, the TX_ER signal is also asserted, PCS Transmit passes to the PMA vectors indicating a transmit error. Note that if the signal TX_ER is asserted while "SSD" is being sent, the transmission of the error condition is delayed until transmission of "SSD" has been completed. Following the de-assertion of tx_enable, an "ESD" of two consecutive vectors of two quinary symbols is generated, after which the transmission of a sequence indicating the idle mode is resumed.

Collision detection is implemented by noting the occurrence of carrier receptions during transmissions, following the model of 10BASE-T. The PCS shall implement the Transmit process as depicted in Figure 32–12 including compliance with the associated state variables as specified in 32.3.4.

32.3.5.2 PCS Receive

PCS Receive accepts vectors of two quinary symbols from the PMA via the rx_symb_vector parameter. After correct receiver operation has been achieved, the loc_rcvr_status parameter assumes the value OK, and PCS

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Receive continuously checks that the received sequence satisfies the encoding rule used in idle mode. As soon as a violation is detected, PCS Receive asserts the parameter receiving and determines whether the violation is due to reception of "SSD" or to a receiver error by examining the last two received vectors (RA_{n-1}, RB_{n-1}) and (RA_n, RB_n). In the first case, during the two symbol periods corresponding to "SSD," PCS Receive replaces "SSD" by preamble bits. Following "SSD," the signal RX_DV is asserted and each received vector is decoded into a data nibble RXD<3:0> until "ESD" is detected. De-assertion of RX_DV and transition to the IDLE state take place upon detection of "ESD". The signal RX_ER is asserted if a receiver error occurs before proper stream termination. In the second case, the signal RX_ER is asserted and the parameter rxerror_status assumes the value ERROR. De-assertion of RX_DV and transition to the IDLE state (rxerror_status=NO_ERROR) takes place upon detection of a sequence generated in idle mode.

A premature stream termination is caused by the detection of four consecutive vectors satisfying the encoding rule used in idle mode prior to the detection of "ESD", provided that the first vector is not a valid data vector. Note that RX_DV remains asserted during the symbol periods corresponding to the first three idle vectors, while RX_ER=TRUE is signaled on the MII. The signal RX_ER is also asserted in the LINK FAILED state, which ensures that RX_ER remains asserted for at least one symbol period. The PCS shall implement the Receive process as depicted in Figure 32–13 including compliance with the associated state variables as specified in 32.3.4.

The parameters receiving and rxerror_status are communicated to the PCS's clients by the following primitives:

PCS_CARRIER.indicate (carrier_status)
: A signal generated by PCS Receive to indicate reception of non-idle quinary symbols. The purpose of this primitive is to give clients indication of activity on the underlying continuous-signaling channel.

PCS_RXERROR.indicate (rxerror_status)
: A signal generated by PCS Receive to indicate a reception of non-idle symbols that does not start with "SSD."

32.3.5.3 PCS Carrier Sense

The PCS Carrier Sense process generates the signal CRS on the MII, which the MAC uses via the Reconciliation sublayer for frame receptions and for deferral. The process operates by performing logical operations on TX_EN and receiving. The PCS shall implement the Carrier Sense process as depicted in Figure 32–14 including compliance with the associated state variables as specified in 32.3.4.

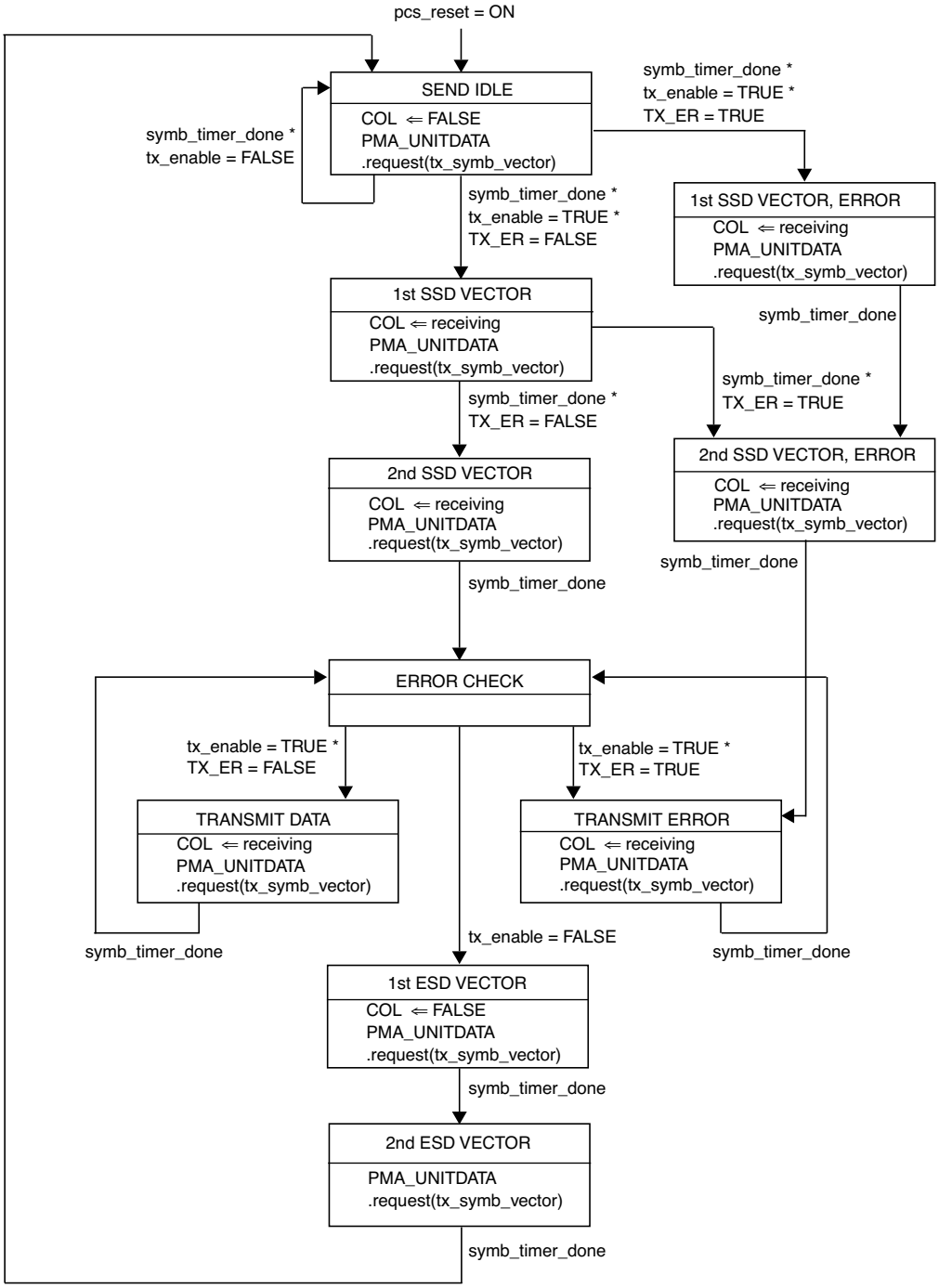
32.3.6 PCS electrical specifications

The interface between PCS, PMA and PHY Control is an abstract message-passing interface, having no specified electrical properties. Electrical characteristics of the signals passing between the PCS and MII may be found in Clause 22.

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NOTE—The generation of PMA_UNITDATA.request(tx_symb_vector) depends on the parameters config, tx_mode, and loc_rcvr_status as defined in 32.3.1.2 and is not shown explicitly in the state diagram.

Figure 32–12—PCS Transmit state diagram

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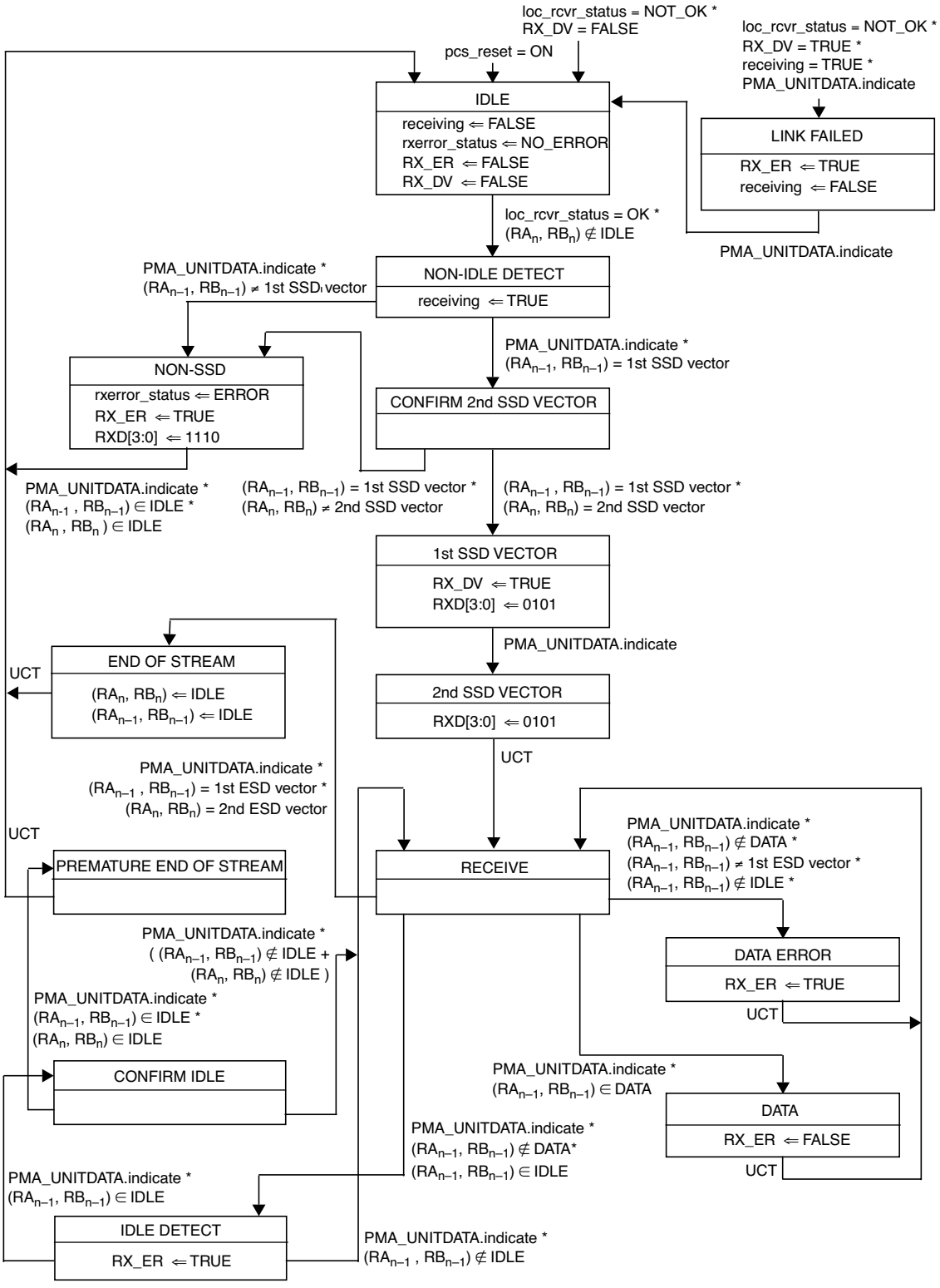


Figure 32–13—PCS Receive state diagram

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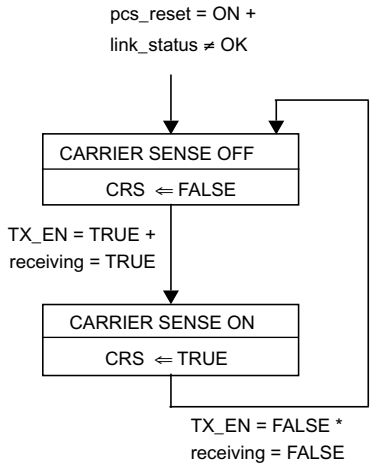


Figure 32–14—PCS Carrier Sense state diagram

32.4 PMA functional specifications and service interface

32.4.1 PMA functional specifications

The PMA couples messages from a PMA service interface specified in 32.4.2 to the 100BASE-T2 baseband medium, specified in 32.7. The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), specified in 32.8.

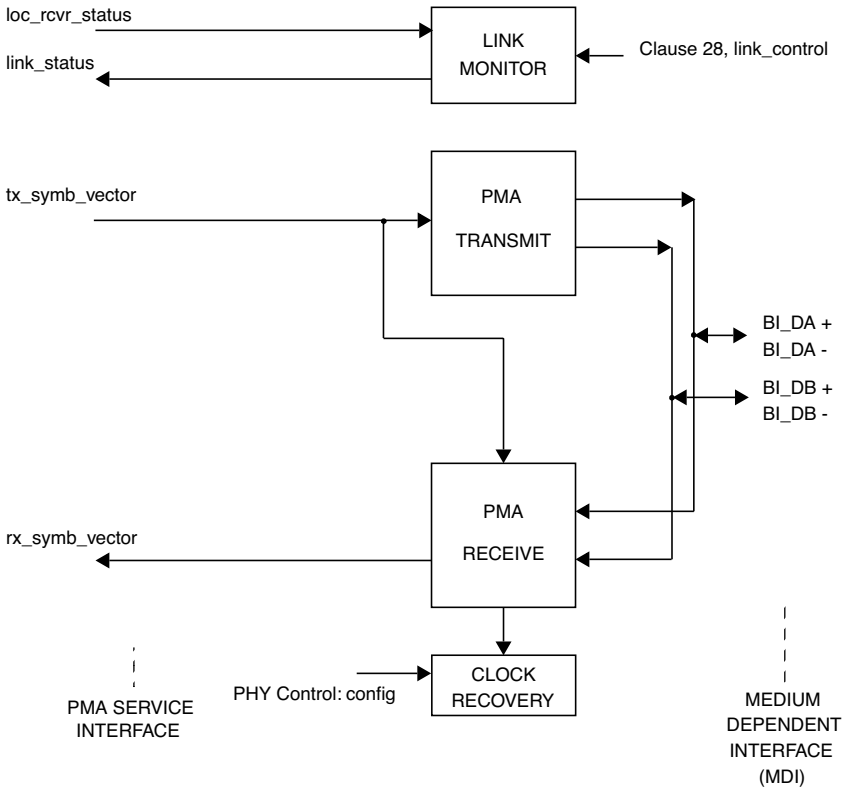


Figure 32–15—PMA reference diagram

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32.4.1.1 PMA functions

The PMA sublayer comprises one PMA Reset function and four simultaneous and asynchronous operating functions. The PMA operating functions are PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function. The Reset function may be shared between PMA and PCS sublayers.

The PMA reference diagram, Figure 32–15, shows how the operating functions relate to the messages of the PMA Service interface, PHY Control Service interface, and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive, and are not shown in Figure 32–15. The management interface and its functions are specified in Clause 22.

32.4.1.1.1 PMA Reset function

The PMA Reset function shall be executed any time either of two conditions occurs. These two conditions are "power on" and the receipt of a reset request from the management entity. The PMA Reset function initializes all PMA functions and forces Auto-Negotiation to be executed. The PMA Reset function sets pma_reset = ON for the duration of its reset function. All state diagrams take the open ended pma_reset branch upon execution of the PMA Reset function. The reference diagrams do not explicitly show the PMA Reset function.

32.4.1.1.2 PMA Transmit function

The PMA Transmit function comprises two independent transmitters to generate five-level pulse-amplitude modulated signals on each of the two pairs BI_DA and BI_DB. PMA Transmit shall continuously transmit onto the MDI pulses modulated by the quinary symbols given by tx_symb_vector[BI_DA] and tx_symb_vector[BI_DB], respectively. The two transmitters shall be driven by the same transmit clock. The signals generated by PMA Transmit will follow the mathematical description given in 32.4.1.2.1, and shall comply with the electrical specifications given in 32.6.

32.4.1.1.3 PMA Receive function

The PMA Receive function comprises two independent receivers for quinary pulse-amplitude modulated signals on each of the two pairs BI_DA and BI_DB. PMA Receive contains the circuits necessary to detect quinary symbol sequences from the signals received at the MDI over receive pairs BI_DA and BI_DB and present these sequences to the PCS Receive function. The signals received at the MDI are described mathematically in 32.4.1.2.2. The PHY shall translate the signals received on pairs BI_DA and BI_DB into the PMA_UNITDATA.indicate parameter rx_symb_vector with a symbol error rate of less than one part in 10^{10}.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization, suppression of cyclo-stationary interference signals created by alien near-end crosstalk sources, and echo and self near-end crosstalk cancellation. The sequence of quinary transmitted symbols tx_symb_vector is needed to perform echo and self near-end crosstalk cancellation.

32.4.1.1.4 Link Monitor function

Link Monitor determines the status of the underlying receive channel. Failure of the underlying receive channel typically causes the PMA's clients to suspend normal operation.

The Auto-Negotiation process notifies Link Monitor whether the device connected to the far end is of type 100BASE-T2. Based on this and other information, Link Monitor sets two important internal variables:

a) The pma_type variable that indicates whether the remote station is of type 100BASE-T2 or not,
b) The link_status variable that is sent across the PMA Service interface.

The Link Monitor function shall comply with the state diagram of Figure 32-16.

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Upon power-on, reset, or release from power-down, the Auto-Negotiation algorithm sets link_control=SCAN_FOR_CARRIER and sends during this period fast link pulses to signal its presence to a remote station. If the presence of a remote station is sensed through reception of fast link pulses, the Auto-Negotiation algorithm sets link_control=DISABLE and exchanges Auto-Negotiation information with the remote station. During this period, link_status=FAIL is asserted. If the presence of a remote 100BASE-T2 station is established, the Auto-Negotiation algorithm permits full operation by setting link_control=ENABLE. As soon as reliable transmission is achieved, the variable link_status=OK is asserted, upon which further PHY operations can take place.

32.4.1.1.5 Clock Recovery function

The Clock Recovery function couples to both receive pairs. It provides a synchronous clock for sampling the signals on the two pairs.

The Clock Recovery function shall provide a clock suitable for synchronous signal sampling on each line so that the symbol-error rate indicated in 32.4.1.1.3 is achieved. The received clock signal must be stable and ready for use when training has been completed (loc_rcvr_status=OK).

32.4.1.2 PMA interface messages

The messages between the PMA, PCS, and PHY Control are defined in 32.4.2, PMA Service Interface. Communication through the MDI is summarized below.

32.4.1.2.1 MDI signals transmitted by the PHY

The quinary symbols to be transmitted by the PMA on the two pairs BI_DA and BI_DB are denoted by tx_symb_vector[BI_DA] and tx_symb_vector[BI_DB], respectively. Five-level Pulse Amplitude Modulation over each pair (PAM5×5) is the modulation scheme employed in 100BASE-T2. It is the function of PMA Transmit to generate on each pair a pulse-amplitude modulated signal of the form

$$s(t) = \sum_k a_k h_1(t - kT)$$

where a_k represents the quinary symbol from the set $\{-2, -1, 0, +1, +2\}$ to be transmitted at time kT, and $h_1(t)$ denotes the system symbol response at the MDI. This symbol response shall comply with the electrical specifications given in 32.6.

32.4.1.2.2 Signals received at the MDI

Signals received at the MDI can be expressed for each pair as pulse-amplitude modulated signals that are corrupted by noise:

$$r(t) = \sum_k a_k h_2(t - kT) + w(t)$$

In this equation, $h_2(t)$ denotes the impulse response of the overall channel from the transmit side up to the MDI at the receive side, and $w(t)$ is a term that includes the contribution of various noise sources. The two signals received on pair BI_DA and BI_DB shall be processed within the PMA Receive function to yield the quinary received symbols rx_symb_vector[BI_DA] and rx_symb_vector[BI_DB].

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32.4.1.3 PMA state diagram

32.4.1.3.1 State diagram variables

link_control
: The link_control parameter as communicated by the PMA_LINK.request primitive.
Values: See 32.4.2.4.

link_status
: The link_status parameter as communicated by the Link Monitor function through the PMA_LINK.indicate primitive.
Values: See 32.4.2.5.

loc_rcvr_status
: The loc_rcvr_status parameter as communicated by the PMA_RXSTATUS.request primitive.
Values: See 32.2.2.3.1.

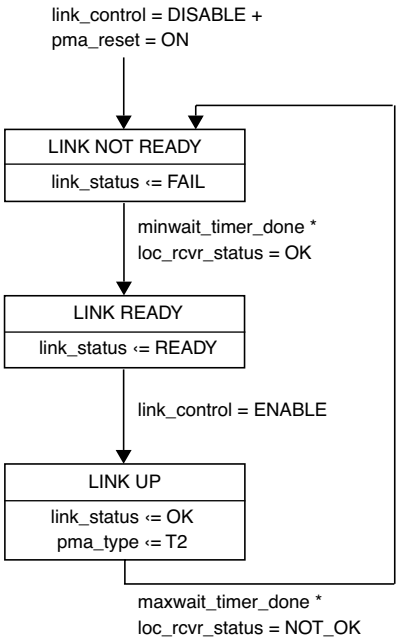
pma_reset
: Allows reset of all PMA functions.
Values: ON and OFF
Set by: PMA Reset

32.4.1.3.2 Timers

maxwait_timer
: Values: See 32.2.4.

minwait_timer
: Values: See 32.2.4.

32.4.1.3.3 Link Monitor state diagram



NOTE—The variables link_control and link_status are designated as link_control_[T2] and link_status_[T2], respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–16).

Figure 32-16—Link Monitor state diagram

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32.4.2 PMA service interface

This subclause specifies the services provided by the PMA. These services are described in an abstract manner and do not imply any particular implementation. The PMA Service Interface supports the exchange of symbol vectors, status indications, and control signals between the PMA, the PCS, and PHY Control. The following primitives are defined:

PMA_TYPE.indicate
PMA_UNITDATA.request
PMA_UNITDATA.indicate
PMA_LINK.request
PMA_LINK.indicate
PMA_CARRIER.indicate
PMA_RXERROR.indicate

The parameter config is passed from PHY Control to the PMA via the primitive PHYC_CONFIG.indicate. The definition of this parameter is given for the PHY Control Service interface in 32.2.2.1 and is not repeated here for the PMA Service interface.

32.4.2.1 PMA_TYPE.indicate

This primitive is generated by the PMA to indicate the nature of the PMA instantiation. Its purpose is to allow clients to support connections to the various types of 100BASE-T PMA entities in a generalized manner.

32.4.2.1.1 Semantics of the service primitive

PMA_TYPE.indicate (pma_type)

The pma_type parameter for use with the 100BASE-T2 PMA is T2.

32.4.2.1.2 When generated

The PMA shall continuously generate this primitive to indicate the value of pma_type.

32.4.2.1.3 Effect of receipt

The client uses the value of pma_type to define the semantics of the primitives defined at the PMA service interface.

32.4.2.2 PMA_UNITDATA.request

This primitive defines the transfer of pairs of quinary symbols in the form of the tx_symb_vector parameter from the PCS to the PMA. The quinary symbols are obtained in the PCS Transmit function using the encoding rules defined in 32.3.1.2 to represent MII data streams, an idle mode, or other sequences.

32.4.2.2.1 Semantics of the service primitive

PMA_UNITDATA.request (tx_symb_vector)

During transmission using 100BASE-T2 signaling, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over each of the two transmit pairs BI_DA and BI_DB. The tx_symb_vector parameter takes on the form:

SYMB_PAIR	A vector of two quinary symbols, one for each of the two transmit pairs BI_DA and BI_DB. Each quinary symbol may take on one of the values –2, –1, 0, +1 or +2.

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The quinary symbols that are elements of tx_symb_vector are called, according to the pair on which each will be transmitted, tx_symb_vector[BI_DA] and tx_symb_vector[BI_DB].

32.4.2.2.2 When generated

The PCS generates PMA_UNITDATA.request (SYMB_PAIR) synchronously with every MII TX_CLK cycle.

32.4.2.2.3 Effect of receipt

Upon receipt of this primitive, the PMA transmits on the MDI the signals corresponding to the indicated quinary symbols. The parameter tx_symb_vector is also used by the PMA Receive function to process the signals received on pairs BI_DA and BI_DB.

32.4.2.3 PMA_UNITDATA.indicate

This primitive defines the transfer of pairs of quinary symbols in the form of the rx_symb_vector parameter from the PMA to the PCS.

32.4.2.3.1 Semantics of the service primitive

PMA_UNITDATA.indicate (rx_symb_vector)

During reception of PAM5×5 signals using 100BASE-T2 signaling, the PMA_UNITDATA.indicate simultaneously conveys to the PCS via the parameter rx_symb_vector the values of the symbols detected on each of the two receive pairs BI_DA and BI_DB. The rx_symbol_vector parameter takes on the form:

SYMB_PAIR — A vector of two quinary symbols, one for each of the two receive pairs BI_DA and BI_DB. Each quinary symbol may take on one of the values –2, –1, 0, +1 or +2.

The quinary symbols that are elements of rx_symb_vector are called, according to the pair upon which each symbol was received, rx_symbol_vector[BI_DA] and rx_symb_vector[BI_DB].

32.4.2.3.2 When generated

The PMA shall generate PMA_UNITDATA.indicate (SYMB_PAIR) messages synchronously with signals received at the MDI.

32.4.2.3.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

32.4.2.4 PMA_LINK.request

This primitive allows the Auto-Negotiation algorithm to enable and disable operation of the PMA.

32.4.2.4.1 Semantics of the service primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

SCAN_FOR_CARRIER — Used by the Auto-Negotiation algorithm prior to receiving any fast link pulses. During this mode the PMA reports link_status=FAIL. PHY processes are disabled.

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DISABLE	Set by the Auto-Negotiation algorithm in the event fast link pulses are detected. *PHY processes are disabled*. This allows the Auto-Negotiation algorithm to determine how to configure the link.
ENABLE	Used by Auto-Negotiation to turn control over to the PHY for data processing functions.

32.4.2.4.2 When generated

Upon power on, reset, or release from power down, the Auto-Negotiation algorithm issues the message PMA_LINK.request (SCAN_FOR_CARRIER).

32.4.2.4.3 Effect of receipt

While link_control=SCAN_FOR_CARRIER or link_control=DISABLE, the PMA shall report link_status=FAIL. While link_control=ENABLE, PHY Control determines the operations to be performed by the PHY.

32.4.2.5 PMA_LINK.indicate

This primitive is generated by the PMA to indicate the status of the underlying medium. This primitive informs the PCS, PHY Control and the Auto-Negotiation algorithm about the status of the underlying link.

32.4.2.5.1 Semantics of the service primitive

PMA_LINK.indicate (link_status)

The link_status parameter can take on one of three values: FAIL, READY, or OK.

FAIL	No valid link established.
READY	Training completed after Auto-Negotiation.
OK	The Link Monitor function indicates that a valid 100BASE-T2 link is established. Reliable reception of signals transmitted from the remote PHY is possible.

32.4.2.5.2 When generated

The PMA shall generate this primitive to indicate the value of link_status in compliance with the state diagrams given in Figure 32-16.

32.4.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 32.2 and 32.3.

32.4.2.6 PMA_CARRIER.indicate

This primitive is identical to PCS_CARRIER.indicate defined in 32.3.5.2. It is not explicitly shown in the PMA reference diagram.

32.4.2.7 PMA_RXERROR.indicate

This primitive is identical to PCS_RXERROR.indicate defined in 32.3.5.2. It is not explicitly shown in the PMA reference diagram.

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32.4.2.8 PMA_RXSTATUS.request

This primitive allows the Link Monitor to determine via the parameter loc_rcvr_status generated by the PCS Receive function whether reliable receiver operations are established. The parameter loc_rcvr_status is also passed from the PCS Receive function to the PHY Control Service interface via the primitive PHYC_RXSTATUS.request. The definition of this parameter is given for the PHY Control Service interface in 32.2.2.3 and is not repeated here for the PMA Service interface.

32.5 Management functions

100BASE-T2 makes extensive use of the management functions provided by the Media Independent Interface (Clause 22) and the communication and self-configuration functions provided by Auto-Negotiation (Clause 28.)

In addition to the provision of MII Registers 0, 1, 4, 5, 6, and 7, it is required that implementations that support 100BASE-T2 also provide equivalents to MII Registers 8, 9, and 10 (Clause 22). Register 8 is used to provide the Auto-Negotiation Link Partner NEXT Page Register, Register 9 is used to provide the MASTER-SLAVE Control Register, and Register 10 is used to provide the MASTER-SLAVE Status Register. These registers are used to configure PHYs for testing, to manually configure PHYs for MASTER-SLAVE negotiation, to store the contents of next pages during the Auto-Negotiation process, and to store information reporting the results of the master/slave configuration process as described in the next subclause.

32.5.1 100BASE-T2 Use of Auto-Negotiation and MII Registers 8, 9, and 10

On power-up, before Auto-Negotiation starts, the Auto-Negotiaton Advertisement register shall have the following configuration: The Selector Field (4.4:0) is set to an appropriate code as specified in Annex 28A. The Acknowledge bit (4.14) is set to logic zero. The Technology Ability Field (4:9:5) is set based on the values set in the MII Status Register (Register 1) (1.15:11) or equivalent and (4.11:10) is set based on the values set in the MII Status Register (Register 1) (1.10:9) or equivalent.

When Auto-Negotiation begins, 100BASE-T2 implementations send an Auto-Negotiation base page with bit D15 set to logical one to indicate that a next page follows (see 28.2.1.2.)

The base page is followed by a formatted next page containing the 100BASE-T2 Technology Ability Message Code (7), which indicates that two unformatted next pages containing the 100BASE-T2 Technology Ability fields follow (see Table 28C–1.)

Two unformatted next pages are sent using the 100BASE-T2 Technology Ability fields shown in Table 32–6 Register 8 will be used to store the transmitted information while it is being processed as described below.

Bit U0 of page 1 shall be copied from MII Register 4.10 to indicate 100BASE-T2FD advertised ability.

Bit U1 of page 1 shall be copied from MII Register 4.11 to indicate 100BASE-T2HD advertised ability.

Bit U2 of page 1 shall be copied from MASTER-SLAVE control register 9.10 to indicate that the PHY device is a repeater port or DTE for 100BASE-T2.

Bits U3 and U4 shall be copied from MASTER-SLAVE control register (bits 9.12 and 9.11) for use by the MASTER-SLAVE negotiation process as described below.

Bits U5-U10 of page 1 and U0-U9 of page 2 shall be used to define the seed used for the MASTER-SLAVE negotiation process described as follows.

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Using the information described above, the PHY performs a MASTER-SLAVE configuration process as defined in 32.5.4.3. This process is conducted at the entrance to the FLP LINK GOOD CHECK state shown Auto-Negotiation Arbitration State Diagram (Figure 28–16.)

If the local device detects that both the local device and the remote device are of the same type (either repeater or DTE) and that both have generated the same random seed, it sets the Ack2 bit of Register 8 to logical zero and generates and transmits a new random seed for MASTER-SLAVE negotiation.

The MASTER-SLAVE configuration process returns one of the three following outcomes.

Successful: Bit 10:15 of the MASTER-SLAVE Status Register is set to logical zero and bit 10.14 is set to logical one. 100BASE-T2 returns control to Auto-Negotiation (at the entrance to the FLP LINK GOOD CHECK state in Figure 28–16) and passes the value of MASTER or SLAVE to PHYC_CONFIG.indicate (see 32.2.2.)

Unsuccessful: link_status_T2 is set to FAIL and Auto-Negotiation restarts (see Figure 28–16.)

Fault detected: (This happens when both end stations are set for manual configuration and both are set to MASTER or both are set to SLAVE.) Bit 10.15 of the MASTER-SLAVE Status Register is set to logical one to indicate that a manual configuration fault has been detected and bit 10.14 is set to logical one to indicate that MASTER-SLAVE resolution completed with a fault. Because the MASTER-SLAVE relationship was not established, link_status_T2 is set to FAIL, causing Auto-Negotiation to restart.

32.5.2 Management functions

The management interface specified in Clause 22 provides a simple, two-wire, serial interface to connect a management entity and a managed PHY for the purposes of controlling the PHY and gathering status from the PHY. This interface is referred to as the MII Management Interface. The register definition specifies a basic register set with an extension mechanism.

100BASE-T2 requires the basic register set that consists of two registers referred to as the Control Register (Register 0) and the Status Register (Register 1) and of some PHY-specific registers. The detailed definitions of these registers are given in 22.2.4.

The full set of management registers is listed in Table 22–6 and 100BASE-T2 PHY specific registers are given in Table 32-3.

Table 32-3—100BASE-T2 Control and Status registers

Register address	Register name	Basic/Extended
9	MASTER-SLAVE Control register	E
10	MASTER-SLAVE Status register	E

32.5.3 PHY specific registers for 100BASE-T2

Some of the extended registers (registers with addresses 2 to 15) are used as PHY specific registers as described in 22.2.4.3. A 100BASE-T2 PHY shall use register addresses 9 and 10 for its control and status functions. The bits in the 100BASE-T2 Control register are used to place the PHY into several possible test modes and to determine the MASTER-SLAVE relationship during Auto-Negotiation. The bits in the

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100BASE-T2 Status register are used to report the MASTER-SLAVE relationship determined during Auto-Negotiation, the local and remote receiver status, and provide an idle error counter.

32.5.3.1 100BASE-T2 Control register (Register 9)

Register 9 shall provide the following values for 100BASE-T2. The assignment of bits in the register is shown in Table 32–4. The default value for each bit of the register should be chosen so that the initial state of the PHY upon power up or reset is a normal operational state without management intervention.

Table 32–4—100BASE-T2 Control register (MII management Register 9) bit definition

Bit(s)	Name	Description	R/W
9.15:14	Transmitter test mode	Default bit values are “00”	R/W
9.13	Receiver test mode	Default bit value is “0”	R/W
9.12	MASTER-SLAVE Manual Configuration Enable	1 = Enable MASTER-SLAVE Manual Configuration value 0 = Disable MASTER-SLAVE Manual Configuration value (default)	R/W
9.11	MASTER-SLAVE Manual Configuration Value	1 = Configure PHY as MASTER during MASTER-SLAVE negotiation, only when 9.12 is set to logical one. 0 = Configure PHY as SLAVE during MASTER-SLAVE negotiation, only when 9.12 is set to logical one.	R/W
9.10	T2_Repeater/DTE bit	1 = Repeater device port 0 = DTE device	R/W
9.9:0	Reserved		

32.5.3.1.1 Transmitter test mode

For a PHY with 100BASE-T2 capability, the PHY shall be placed in transmitter test mode 1 operation (described in 32.6.1.2.1) when bit 9.15 is set to logical zero and bit 9.14 is set to logical one. When bit 9.15 is set to logical one and bit 9.14 is set to logical zero, the PHY shall be placed in transmitter test mode 2 operation as described in 32.6.1.2.1. When bit 9.15 is set to logical one and bit 9.14 is set to logical one, the PHY shall be placed in the transmitter test mode 3 operation as described in 32.6.1.2.1.

The default value for bits 9.15:14 are all zero.

32.5.3.1.2 Receive test mode

The PHY shall be placed in the receiver test mode as described in 32.6.1.3.2 when the bit 9.13 is set to logical one.

The default value for bit 9.13 is zero.

32.5.3.1.3 MASTER-SLAVE Manual Configuration Enable

The MASTER-SLAVE relationship is established during Auto-Negotiation via either automatic MASTER-SLAVE configuration or manual configuration. If bit 9.12 is set to logical zero, then the MASTER-SLAVE configuration negotiation function will determine the PHY configuration. If bit 9.12 is set to logical one, then manual MASTER-SLAVE configuration is enabled, using 9.11 to specify the value. (Usage of this bit is further described in 32.5.3.1.)

The default value of bit 9.12 is zero.

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32.5.3.1.4 MASTER-SLAVE Manual Configuration Value

MASTER-SLAVE Manual configuration is enabled by setting bit 9.12 to logical one. When manual configuration mode is enabled, setting bit 9.11 to logical one configures the PHY as MASTER, and setting bit 9.11 to logic zero configures the PHY as SLAVE during MASTER-SLAVE negotiation process and shall be used to report the result of the MASTER-SLAVE configuration resolution for that PHY. Detailed description of the use of this bit in MASTER-SLAVE configuration resolution is provided in 32.5.3.1.

The default value of bit 9.11 is zero.

32.5.3.1.5 T2_Repeater/DTE Bit

Bit 9.10 shall be set to logical zero if the PHY is a DTE device and shall be set to a logical one if the PHY is a repeater device port (usage of this bit is described in 32.5.2.)

32.5.3.1.6 Reserved bits

Bits 9.9:0 are reserved for future standardization. They shall be written as zero and shall be ignored when read; however, a PHY shall return the value zero in these bits.

32.5.3.2 100BASE-T2 Status register (Register 10)

Register 10 shall provide the following values for 100BASE-T2. The assignment of bits in the register is shown in Table 32–5. The default value for each bit of the register should be chosen so that the initial state of the PHY upon power up or reset is a normal operational state without management intervention.

Table 32–5—100BASE-T2 Status register (MII management Register 10) bit definition

Bit(s)	Name	Description	R/W[a]
10.15	MASTER-SLAVE manual configuration fault	1 = MASTER-SLAVE manual configuration fault detected 0 = No MASTER-SLAVE manual configuration fault detected	RO/SC
10.14	MASTER-SLAVE configuration resolution complete	1 = MASTER-SLAVE configuration resolution has completed 0 = MASTER-SLAVE configuration resolution has not completed	RO
10.13	Local Receiver Status	1 = Local Receiver OK 0 = Local Receiver not OK	RO
10.12	Remote Receiver Status	1 = Remote Receiver OK 0 = Remote Receiver not OK	RO
10.11:8	Reserved		
10.7:0	Idle Error Count	Idle Error count	RO/SC

[a]R/W = Read/Write, SC = Self Clearing, RO = Read Only

32.5.3.2.1 MASTER-SLAVE Manual Configuration Fault

When read as a logical one, bit 10.15 indicates that a MASTER-SLAVE Manual Configuration Fault condition has been detected. The type of fault as well as the criteria and method of fault detection is PHY specific. The MASTER-SLAVE Manual Configuration Fault bit shall be implemented with a latching function, such that the occurrence of a MASTER-SLAVE Manual Configuration Fault will cause the MASTER-SLAVE Manual Configuration Fault bit to be set and remain set until it is cleared. The MASTER-SLAVE Manual Configuration Fault bit shall be cleared each time Register 10 is read via the management interface and shall also be cleared by a 100BASE-T2 PMA reset.

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For 100BASE-T2, this fault condition will occur when both PHYs are forced to be MASTER or SLAVE at the same time using bits 9.12 and 9.11. Bit 10.15 should be set via the MASTER-SLAVE Configuration Resolution function described in 32.5.4.

32.5.3.2.2 MASTER-SLAVE Configuration Resolution Complete

When read as a logical one, bit 10.14 indicates that the MASTER-SLAVE Resolution process has been completed and that the contents of Registers 9 and 10 related to MASTER-SLAVE are valid. When read as a logic zero, bit 10.14 indicates that the MASTER-SLAVE Configuration Resolution process has not been completed and that the contents of Registers 9 and 10 which are related to MASTER-SLAVE resolution are invalid. Bit 10.14 should be set via the MASTER-SLAVE Configuration Resolution function described in 32.5.4.

32.5.3.2.3 Local Receiver Status

Bit 10.13 indicates the status of the local receiver. Local receiver status is defined by the value of the loc_rcvr_status variable described in 32.2.3.

32.5.3.2.4 Remote Receiver Status

Bit 10.12 indicates the status of the remote receiver. Remote receiver status is defined by the value of the rem_rcvr_status variable described in 32.2.3.

32.5.3.2.5 Reserved bits

Bit 10.11:8 are reserved for future standardization. They shall be written as zero and shall be ignored when read; however, a PHY shall return the value zero in these bits.

32.5.3.2.6 Idle Error count

Bits 10.7:0 indicate the Idle Error count, where 10.7 is the most significant bit. During normal operation these bits contain a cumulative count of the errors detected when the receiver is receiving idles and the PHY Control parameter tx_mode is equal to SEND_N (indicating that both local and remote receiver status have been detected to be OK). When the PHY has receiver test mode (bit 9.13) enabled, these bits contain a cumulative count of the errors detected at all times when the local receiver status is OK. These bits are reset to all zeroes when the error count is read by the management function or upon execution of the PCS Reset function and they are held at all ones in case of overflow (see 30.5.1.1.11).

32.5.4 Changes and additions to Auto-Negotiation (Clause 28)

32.5.4.1 Change to 28.2.4.1.3 (Auto-Negotiation Advertisement register)

For implementations which support 100BASE-T2, the Technology Ability Field (4:9:5) is set based on the values set in the MII Status Register (Register 1) (1.15:11) or equivalent and (4.11:10) is set based on the values set in the MII Status Register (Register 1) (1.10:9) or equivalent. Use of Register 4 is defined in 28.2.4.1.3.

32.5.4.2 Use of Auto-Negotiation Next Page codes for 100BASE-T2 PHYs

For a PHY capable of 100BASE-T2 transmission, during Auto-Negotiation the Base Page will be followed by a Next Page with a message code containing the 100BASE-T2 Technology Ability Message Code (7) as shown in Table 28C–1. This Message Next Page indicates that two Unformatted Message Next Pages will follow which contain the 100BASE-T2 Technology Ability Fields as described in Table 32–6.

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Table 32–6—Bit assignments for Unformatted Next Pages containing 100BASE-T2 Technology Ability Field

Bit	Technology	MII register bit/source
PAGE 1		
U0	100BASE-T2 Half Duplex (1 = Half Duplex and 0 = no Half Duplex)	MII Register 4.10
U1	100BASE-T2 Full Duplex (1=Full Duplex and 0 = no Full Duplex)	MII Register 4.11
U2	100BASE-T2 Repeater/DTE bit (1 = Repeater and 0 = DTE)	MII Register 9.10 (MASTER-SLAVE Control register)
U3	100BASE-T2 MASTER-SLAVE Manual Configuration Enable (1 = Manual Configuration Enable); intended to be used for manual selection in a particular MASTER-SLAVE mode. To be used in conjunction with bit U4	MII Register 9.12 (MASTER-SLAVE Control register)
U4	100BASE-T2 MASTER-SLAVE Manual Configuration value 1 = MASTER and 0 = SLAVE. This bit is ignored if U3 = 0.	MII Register 9.11 (MASTER-SLAVE Control register)
U5	100BASE-T2 MASTER-SLAVE Seed Bit 0 (SB0) (LSB)	MASTER-SLAVE seed value (15.0)
U6	100BASE-T2 MASTER-SLAVE Seed Bit 1 (SB1)	
U7	100BASE-T2 MASTER-SLAVE Seed Bit 2 (SB2)	
U8	100BASE-T2 MASTER-SLAVE Seed Bit 3 (SB3)	
U9	100BASE-T2 MASTER-SLAVE Seed Bit 4 (SB4)	
U10	100BASE-T2 MASTER-SLAVE Seed Bit 5 (SB5)	
PAGE 2		
U0	100BASE-T2 MASTER-SLAVE Seed Bit 6 (SB6)	
U1	100BASE-T2 MASTER-SLAVE Seed Bit 7 (SB7)	
U2	100BASE-T2 MASTER-SLAVE Seed Bit 8 (SB8)	
U3	100BASE-T2 MASTER-SLAVE Seed Bit 9 (SB9)	
U4	100BASE-T2 MASTER-SLAVE Seed Bit 10 (SB10)	
U5	100BASE-T2 MASTER-SLAVE Seed Bit 11 (SB11)	
U6	100BASE-T2 MASTER-SLAVE Seed Bit 12 (SB12)	
U7	100BASE-T2 MASTER-SLAVE Seed Bit 13 (SB13)	
U8	100BASE-T2 MASTER-SLAVE Seed Bit 14 (SB14)	
U9	100BASE-T2 MASTER-SLAVE Seed Bit 15 (SB15)	
U10	unused	

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32.5.4.3 MASTER-SLAVE Configuration Resolution

Since both PHYs that share a link segment are capable of being MASTER or SLAVE, a prioritization scheme exists to ensure that the correct mode is chosen. The MASTER-SLAVE relationship shall be determined during Auto-Negotiation using Table 32–7 with the 100BASE-T2 Technology Ability Next Page bit values specified in Table 32–7 and information received from the link partner.

Table 32–7—100BASE-T2 MASTER-SLAVE Configuration Resolution table

Local Device Type	Remote Link Partner Type	Resolution Function result	
		Local Device	Remote Link Partner
DTE (U2=0 & U3=0) or Manual SLAVE (U3=1 & U4=0)	Repeater (U2=1 & U3=0) or Manual MASTER (U3=1 & U4=1)	SLAVE	MASTER
Repeater (U2=1 & U3=0)	Manual MASTER (U3=1 & U4=1)		
Manual SLAVE (U3=1 & U4=0)	DTE (U2=0 & U3=0)		
Repeater (U2=1 & U3=0) or Manual MASTER (U3=1 & U4=1)	DTE (U2=0 & U3=0) or Manual SLAVE (U3=1 & U4=0)	MASTER	SLAVE
DTE (U2=0 & U3=0)	Manual Slave (U3=1 & U4=0)		
Manual Master (U3=1 & U4=1)	Repeater (U2=1 & U3=0)		
Repeater (U2=1 & U3=0)	Repeater (U2=1 & U3=0)	PHY with higher seed value is the MASTER. If the seeds are equal, the MASTER-SLAVE resolution is unsuccessful, set link_status_T2=FAIL, causing Auto-Negotiation to restart.	
DTE (U2=0 & U3=0)	DTE (U2=0 & U3=0)		
Manual SLAVE (U3=1 & U4=0)	Manual SLAVE (U3=1 & U4=0)	Fault detected Set link_status_T2=FAIL, forcing Auto-Negotiation to restart.	
Manual MASTER (U3=1 & U4=1)	Manual MASTER (U3=1 & U4=1)		

The rationale for this hierarchy is straightforward. A 100BASE-T2 repeater has higher priority than a DTE to become the MASTER. In the case where both devices are of the same type, e.g., both devices are Repeaters, the device with the higher MASTER-SLAVE seed bits (SB0..SB15), where SB15 is the MSB, becomes the MASTER and the device with the lower seed value becomes the SLAVE. In case both devices have the same seed value, both should assert link_status_T2=FAIL (as defined in 28.3.1) and restart Auto-Negotiation. Successful completion of the MASTER-SLAVE resolution shall be treated as MASTER-SLAVE configuration resolution complete and the 100BASE-T2 Status Register bit 10.14 shall be set to logical one.

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The method of generating a random seed is left to the implementor. The generated random seeds should belong to a sequence of independent, identically distributed integer numbers with a uniform distribution in the range of 0 to 65535. The algorithm used to generate the integer should be designed to minimize the correlation between the number generated by any two devices at any given time. A seed counter shall be provided to track the number of seed attempts. The seed counter shall be set to zero at start-up and shall be incremented each time a seed is generated. A MASTER-SLAVE resolution fault shall be declared if resolution is not reached after the generation of seven seeds.

The MASTER-SLAVE Manual Configuration Enable bit (control register bit 9.12) is used to manually set a device to become the MASTER or the SLAVE. In case both devices are manually set to become the MASTER or the SLAVE, this condition shall be flagged as a MASTER-SLAVE Manual Configuration fault condition, thus the MASTER-SLAVE Manual Configuration fault bit (status register bit 10.15) shall be set to logical one. The MASTER-SLAVE Manual Configuration fault condition shall be treated as MASTER-SLAVE configuration resolution complete and status register bit 10.14 shall be set to logical one. In this case, link_status_T2 will be set to FAIL, because the MASTER-SLAVE relationship was not resolved. This will force Auto-Negotiation to restart after the link_fail_inhibit_timer has expired. Determination of MASTER-SLAVE values occur on the entrance to the FLP LINK GOOD CHECK state (Figure 28–16) when the highest common denominator (HCD) technology is 100BASE-T2. The resulting MASTER-SLAVE value is used by the 100BASE-T2 PHY control (32.2.2.1).

32.6 PMA electrical specifications

This clause defines the electrical characteristics of the PHY at the MDI.

The ground reference point for all common-mode tests is the MII ground circuit. Implementations without an MII use the chassis ground. The values of all components in test circuits shall be accurate to within ±1% unless otherwise stated.

32.6.1 PMA-to-MDI interface characteristics

32.6.1.1 Isolation requirement

The PHY shall provide electrical isolation between the DTE or repeater circuits, including frame ground and all MDI leads. This electrical separation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50–60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC 60950
b) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC 60950
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time or half value), as defined in IEC 60060.

There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC 60950, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 Vdc.

32.6.1.2 Transmitter electrical specifications

The PMA shall provide the Transmit function specified in 32.4.1.1.2 in accordance with the electrical specifications of this clause.

Where a load is not specified, the transmitter shall meet requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output.

The tolerance on the poles of the test filters used in this clause shall be ±1%.

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32.6.1.2.1 Transmitter test modes

Since the 100BASE-T2 PCS employs scrambling, synchronization of data at the MII to the scrambled state is virtually impossible. Therefore a special transmit test mode shall be required to allow for testing of the transmitter waveform. Additionally, a test mode for measuring transmitter output jitter is also required.

For a PHY with a MII interface, these modes shall be enabled by setting bits 9.14 and 9.15 (MASTER-SLAVE Control Register) of the MII Management register set as shown in Table 32–8. These test modes shall only change the data symbols provided to the transmitter circuitry and may not alter the electrical characteristics of the transmitter. A PHY without an MII shall provide a means to provide these functions. The vendor shall provide a means to enable these modes for conformance testing.

Table 32–8—MII management register set

Bit 9.15	Bit 9.14	Mode
0	0	Normal operation
0	1	TX Test mode 1—waveform test
1	0	TX Test mode 2—jitter test
1	1	TX Test mode 3—

When transmit test mode 1 is enabled, the PHY shall transmit the following sequence of data symbols (A_n and B_n of 32.3.1.2.3) continually from both transmitters:

{{+2 followed by 127 0 symbols}, {-2 followed by 127 0 symbols},{+1 followed by 127 0 symbols}, {–1 followed by 127 0 symbols}, {16 +2 symbols, 16 –2 symbols followed by 224 0 symbols}}

This sequence is repeated continually without breaks between the repetitions when the transmit test mode is enabled. A typical transmitter output is shown below in Figure 32–17. The transmitter shall time the transmitted symbols from a 25.000 MHz ± 0.01% clock.

When transmit test mode 2 is enabled, the PHY shall transmit the data symbol sequence {+2,–2} repeatedly on both channels. The transmitter shall time the transmitted symbols from a 25.000 MHz ± 0.01% clock.

When transmit test mode 3 is enabled, the PHY shall transmit idle data compliant with the idle signaling specified in 32.3 with loc_rcvr_status=OK.

32.6.1.2.2 Peak differential output voltage and level distortion

When in transmit test mode 1 and observing the differential signal output at the MDI terminated in 100 Ω, preprocessed by the high pass filter defined below, for each pair, with no intervening cable, the absolute value of the peak of the waveform at points A and B as defined in Figure 32–17 shall fall within 1.71–1.91V (1.81 V ± 0.5 dB).

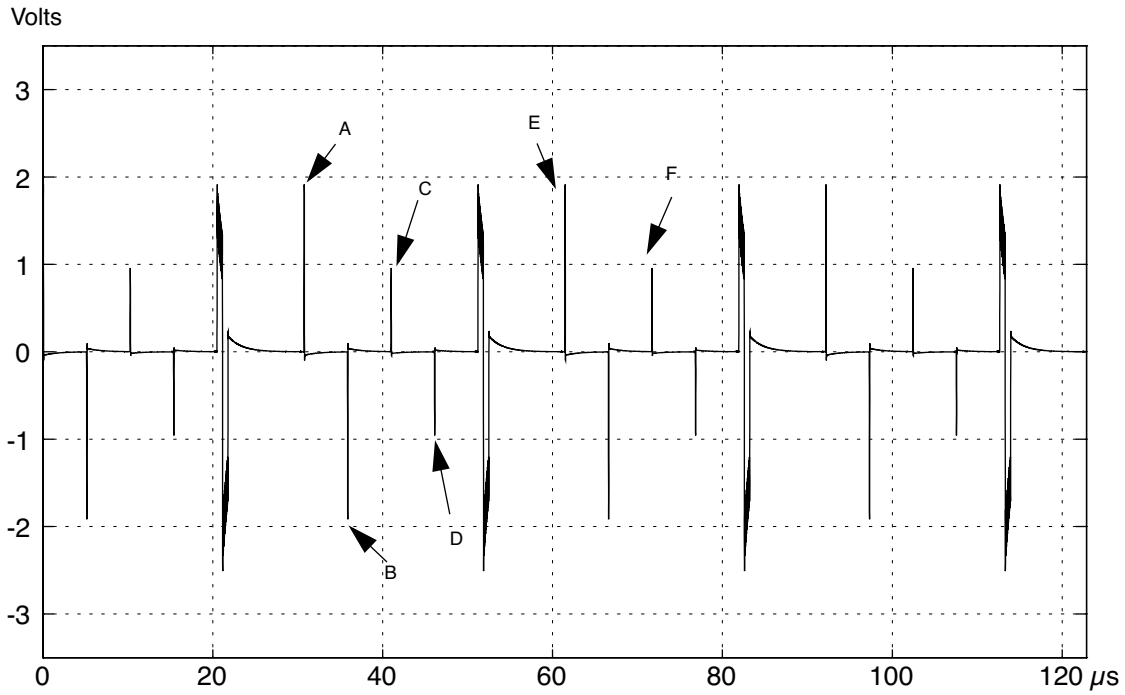
The absolute value of the peak of the waveforms at points A and B shall differ by less than 1%.

The absolute value of the peak of the waveform at points C and D as defined in Figure 32–17 shall differ from 0.5 times the average of the absolute values of the peaks of the waveform at points A and B by less than 2%.

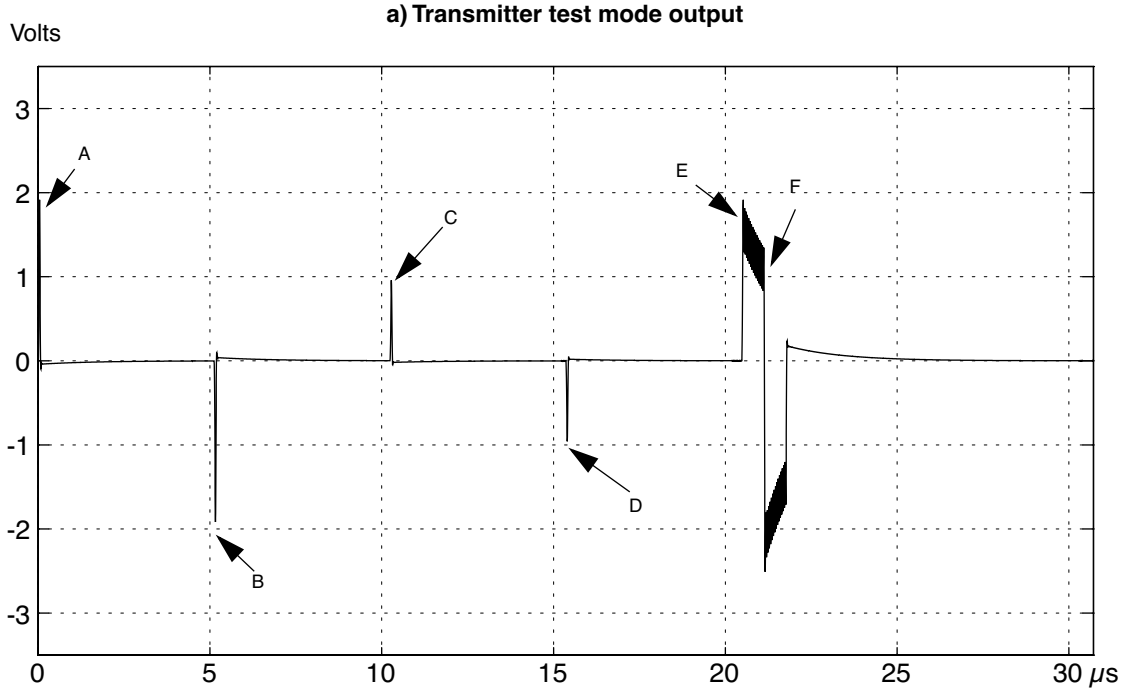
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a) Transmitter test mode output



b) Expanded view of partial cycle of transmitter test mode output

Figure 32–17—Example transmitter test mode transmitter

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The preprocessing filter shall have the following transfer function[14]:

$$H_{\text{preprocess}}(f) = \frac{jf}{jf + 200 \times 10^3} \quad f \text{ in Hz}$$

32.6.1.2.3 Maximum output droop

When in transmit test mode 1 and observing the differential signal output at the MDI, for either pair, with no intervening cable, the peak value of the waveform at point F as defined in Figure 32–17 shall be greater than 70.5% of the peak value of the waveform at point E. A preprocessing filter is not used for this measurement.

32.6.1.2.4 Differential output templates

The transmitter differential output voltage shall be measured at the output of the high pass preprocessing filter defined in 32.6.1.2.2, with no intervening cables. The voltage waveforms A, B, C and D defined in Figure 32–17, after normalization by their respective peak values, shall lie within the time domain template defined in Figure 32–18 and the piecewise linear interpolation between the points in Table 32–9. The waveforms may be shifted in time as appropriate to fit within the template.

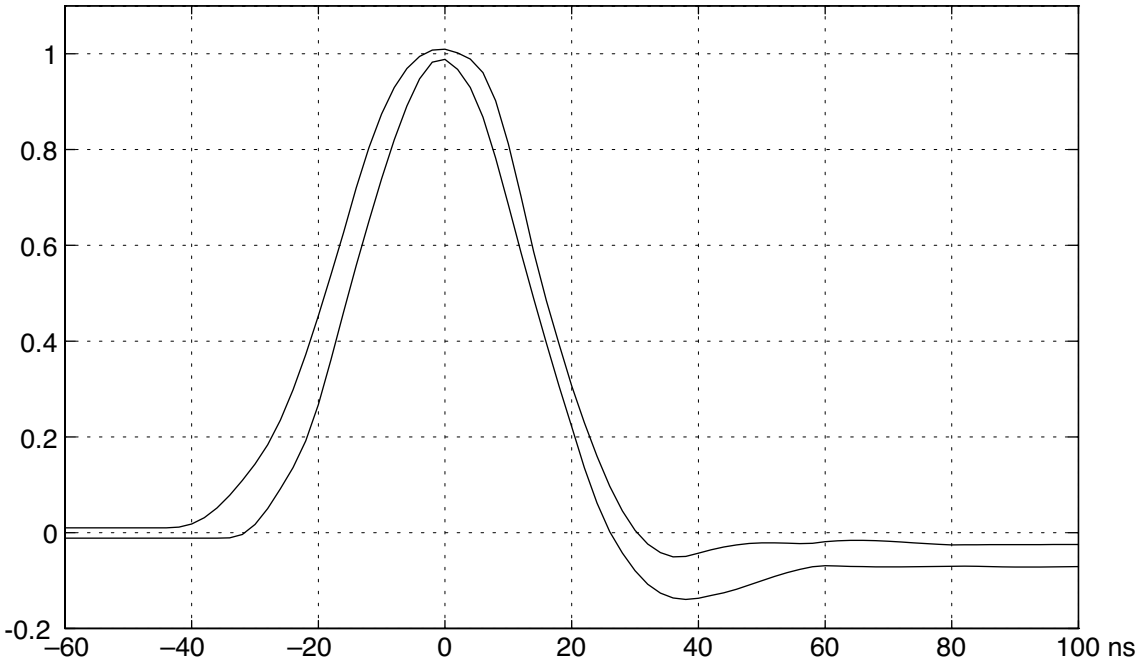
Additionally, the magnitude in dB of the Fourier transform of the preprocessed waveforms A, B, C and D shall lie within the frequency domain template defined in Figure 32–18 and the piecewise linear interpolation between the points in Table 32–9. The time span of the waveforms so processed shall be –80 ns to +2000 ns with the 0 ns point of the waveform aligned as for the time domain mask shown in Figure 32–18 and the magnitude of the Fourier transform should be normalized so that the maximum value is at 0 dB.[15]

[14]"j" denotes the positive square root of –1.

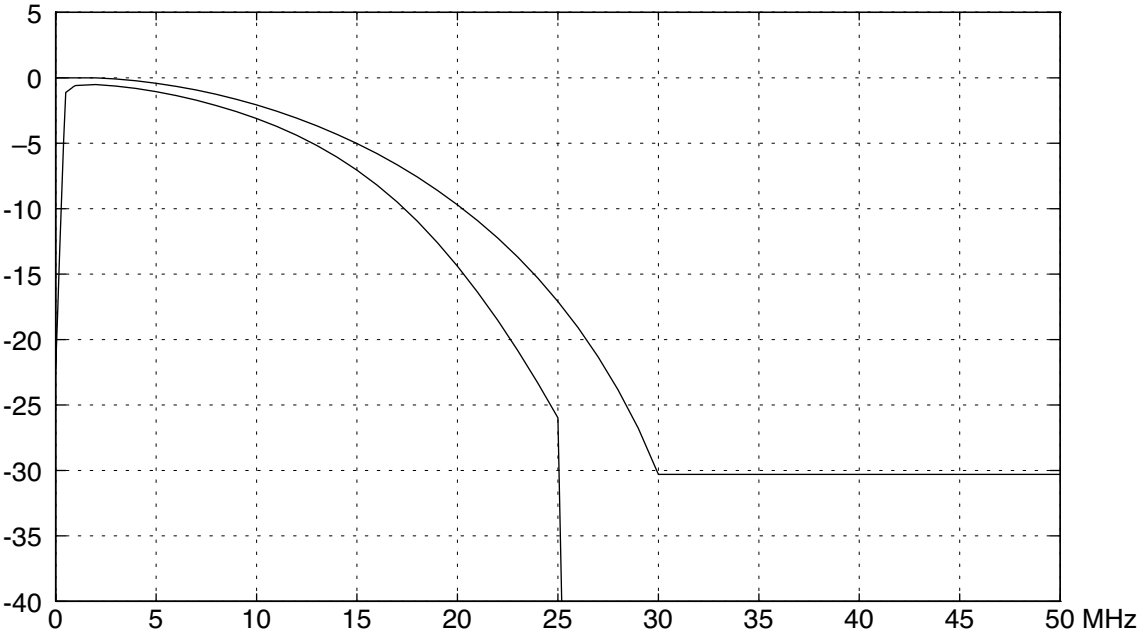
[15]A sampling rate of 100 MHz is adequate to generate the frequency domain mask.

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a) Normalized time domain transmit template



b) Normalized frequency domain transmit template

NOTE—The frequency domain transmit template is not intended to address electromagnetic radiation limits.

Figure 32–18—Normalized transmit templates as measured at MDI through preprocessing filter

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Table 32–9—Normalized time domain voltage template

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
–60	0.010	–0.011	22	0.230	0.136
–58	0.010	–0.011	24	0.160	0.062
–56	0.010	–0.011	26	0.097	0.002
–54	0.010	–0.011	28	0.045	–0.042
–52	0.010	–0.011	30	0.005	–0.079
–50	0.010	–0.011	32	–0.024	–0.108
–48	0.010	–0.011	34	–0.042	–0.126
–46	0.010	–0.011	36	–0.051	–0.136
–44	0.010	–0.011	38	–0.050	–0.139
–42	0.012	–0.011	40	–0.043	–0.137
–40	0.018	–0.011	42	–0.036	–0.131
–38	0.031	–0.011	44	–0.030	–0.126
–36	0.052	–0.011	46	–0.025	–0.118
–34	0.078	–0.011	48	–0.023	–0.109
–32	0.109	–0.004	50	–0.021	–0.100
–30	0.143	0.017	52	–0.021	–0.091
–28	0.184	0.050	54	–0.022	–0.084
–26	0.235	0.092	56	–0.023	–0.077
–24	0.298	0.136	58	–0.022	–0.071
–22	0.372	0.192	60	–0.019	–0.069
–20	0.453	0.268	62	–0.017	–0.070
–18	0.538	0.360	64	–0.016	–0.070
–16	0.627	0.461	66	–0.016	–0.071
–14	0.720	0.558	68	–0.017	–0.071
–12	0.804	0.650	70	–0.018	–0.071
–10	0.874	0.739	72	–0.020	–0.071
–8	0.930	0.820	74	–0.021	–0.071
–6	0.969	0.891	76	–0.023	–0.071
–4	0.995	0.948	78	–0.024	–0.070
–2	1.008	0.982	80	–0.026	–0.070
0	1.009	0.988	82	–0.025	–0.070

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Table 32–9—Normalized time domain voltage template *(continued)*

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
2	1.002	0.967	84	–0.025	–0.070
4	0.989	0.930	86	–0.025	–0.071
6	0.961	0.868	88	–0.025	–0.071
8	0.902	0.782	90	–0.025	–0.072
10	0.812	0.685	92	–0.025	–0.072
12	0.703	0.585	94	–0.025	–0.072
14	0.587	0.489	96	–0.025	–0.071
16	0.485	0.396	98	–0.025	–0.071
18	0.394	0.306	100	–0.025	–0.071
20	0.307	0.221			

Table 32–10—Normalized frequency domain amplitude spectrum template

Frequency, MHz	Normalized transmit frequency domain template, upper limit, dB	Normalized transmit frequency domain template,lower limit, dB	Frequency, MHz	Normalized transmit frequency domain template, upper limit, dB	Normalized transmit frequency domain template,lower limit, dB
0.1	0.00	–17.88	22	–12.24	–18.52
0.2	0.00	–13.49	23	–13.70	–20.84
0.3	0.00	–9.09	24	–15.31	–23.32
0.4	0.00	–4.70	25	–17.09	–25.97
0.5	0.00	–1.13	26	–19.08	
0.6	0.00	–1.01	27	–21.31	
0.7	0.00	–0.90	28	–23.84	
0.8	0.00	–0.78	29	–26.78	
0.9	0.00	–0.66	30	–30.29	
1	0.00	–0.59	31	–30.29	
2	–0.00	–0.52	32	–30.29	
3	–0.08	–0.63	33	–30.29	
4	–0.23	–0.82	34	–30.29	

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Table 32–10—Normalized frequency domain amplitude spectrum template *(continued)*

Frequency, MHz	Normalized transmit frequency domain template, upper limit, dB	Normalized transmit frequency domain template,lower limit, dB	Frequency, MHz	Normalized transmit frequency domain template, upper limit, dB	Normalized transmit frequency domain template,lower limit, dB
5	–0.42	–1.06	35	–30.29	
6	–0.65	–1.36	36	–30.29	
7	–0.93	–1.71	37	–30.29	
8	–1.26	–2.12	38	–30.29	
9	–1.64	–2.59	39	–30.29	
10	–2.07	–3.12	40	–30.29	
11	–2.55	–3.72	41	–30.29	
12	–3.08	–4.40	42	–30.29	
13	–3.67	–5.17	43	–30.29	
14	–4.31	–6.05	44	–30.29	
15	–5.03	–7.06	45	–30.29	
16	–5.80	–8.20	46	–30.29	
17	–6.65	–9.50	47	–30.29	
18	–7.58	–10.96	48	–30.29	
19	–8.59	–12.59	49	–30.29	
20	–9.70	–14.39	50	–30.29	
21	–10.91	–16.37			

32.6.1.2.5 Transmitter timing jitter

When in transmit test mode 2, the peak-to-peak jitter of the zero crossings of the differential signal output at the MDI shall be less than 0.5 ns.

32.6.1.2.6 Transmit clock frequency

The quinary symbol transmission rate on each pair shall be 25.000 MHz ± 0.01%.

32.6.1.3 Receiver electrical specifications

The PMA shall provide the Receive function specified in 32.4.1.1.3 in accordance with the electrical specifications of this clause. The patch cabling and interconnecting hardware used in test configurations shall meet or exceed ISO/IEC 11801, Category 3 specifications.

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32.6.1.3.1 Test channel

To perform the Receiver Alien NEXT Tolerance test and Receiver timing jitter test described in this clause, a test channel including transmitter, cabling and NEXT models is required. This test channel is shown conceptually in Figure 32–19.

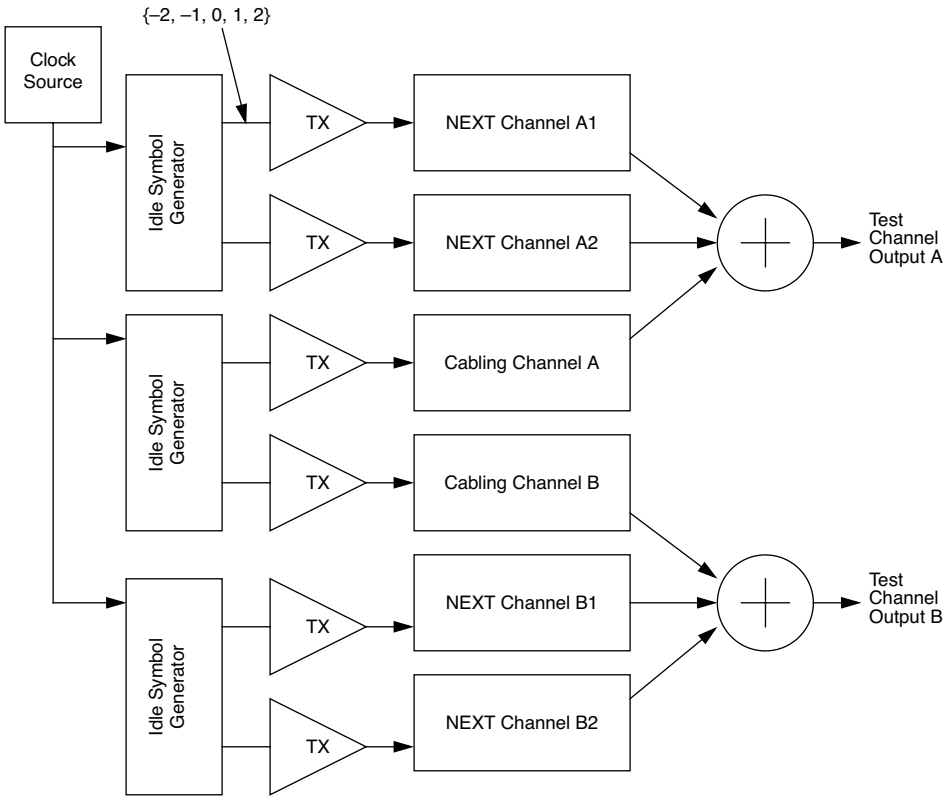


Figure 32–19—Conceptual diagram of test channel

The combined responses of the TX block and NEXT or cabling channel blocks shall be those defined in Table 32–8. The responses of Table 32–10 are shown in Figure 32–20. The responses represent the response of the test channel to isolated "1" symbols in a stream of "0" symbols at the input to the transmitter blocks. The test channel may also include a first order high pass filter with 3 dB cutoff frequency of less than 100 kHz in addition to the tabulated responses. The output impedance of the test channel shall be consistent with 32.6.1.4.1. The idle symbol generator outputs shall be conformant with the idle signaling specified in 32.3 with loc_rcvr_status=OK. The clock source shall result in a quinary symbol transmission rate conformant with 32.6.1.2.6. The peak-to-peak jitter on the clock source shall be less than 0.2 ns.

The test channel may be implemented in any fashion consistent with the above specifications and with the further constraint that the ratio of the squared error between the implemented NEXT channel symbol responses and the specified NEXT channel symbol responses to the energy in the specified NEXT channel symbol responses shall be less than 5% and the energy of the implemented NEXT channel symbol responses and the energy of the specified NEXT channel symbol responses shall differ by less than ± 0.25 dB. If digital filters are used to generate the channel characteristics, care must be taken to ensure that the signal to quantization noise at the channel output is greater than 35 dB.

The NEXT channel impulse responses defined in Table 32–11 have been developed to simulate the attenuation and phase characteristics of worst case 100BASE-T2 alien NEXT.

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The cabling attenuation and group delay characteristics used to derive the cable symbol responses specified in Table 32–8 at 0 m and 100 m are obtained from the following worst-case model of the cabling attenuation. The model includes 1.2 dB of flat loss simulating three worst-case Category 3 connectors. The group delay of the model is relative and does not include the fixed delay associated with 100 m of Category 3 cabling. An additional 570 ns of fixed delay should be added in order to obtain the absolute group delay; however, it is not necessary to add this fixed delay to the test channel.

$$\gamma(f) = -(1.537\times10^{-6}\sqrt{\pi f} + j1.537\times10^{-6}\sqrt{\pi f} + 44.5\times10^{-12}2\pi f)$$

$$H(f,l) = e^{\gamma(f)l}10^{-1.2/20}$$

f in Hz

l in meters

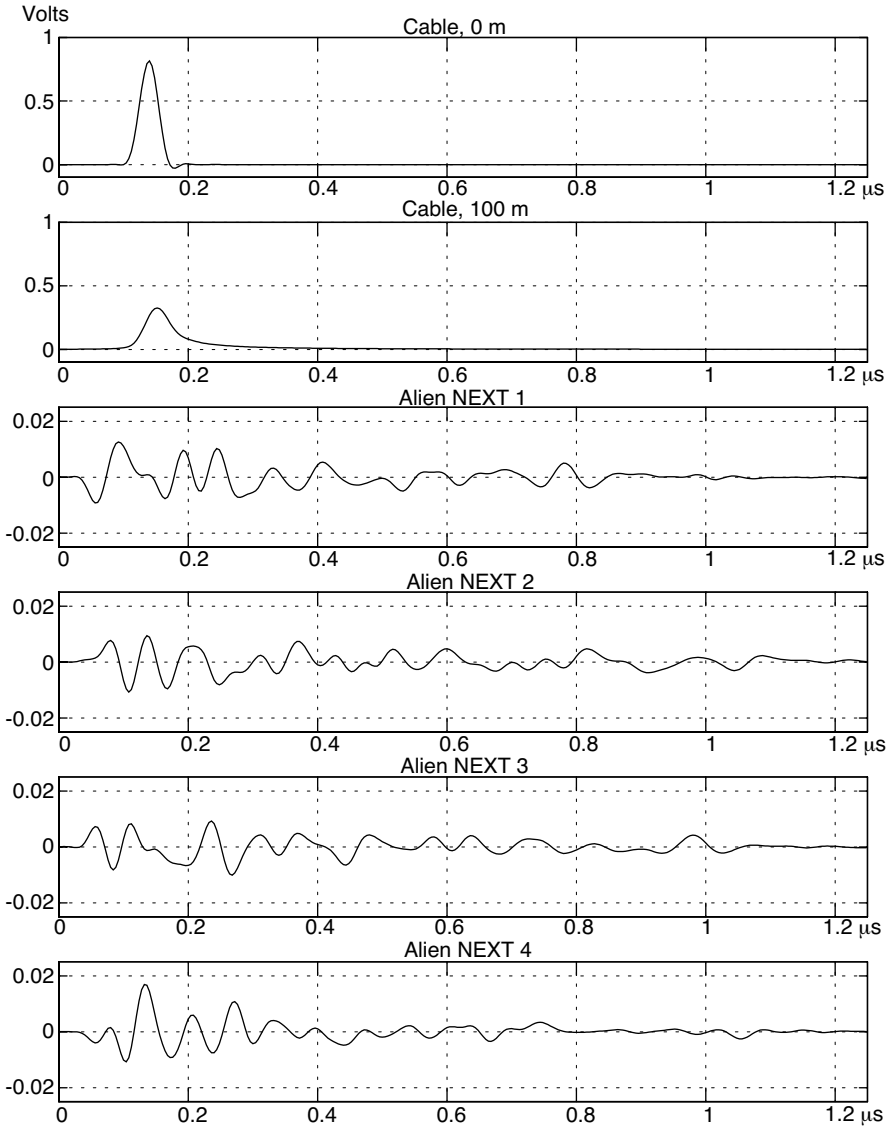


Figure 32–20—Test channel responses

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.000	4.23e-06	1.48e-03	1.62e-05	1.19e-05	–5.05e-06	3.70e-05
0.004	–4.87e-06	1.55e-03	–5.97e-05	1.67e-05	6.71e-05	2.02e-05
0.008	–6.84e-06	1.62e-03	–8.19e-05	1.15e-05	9.78e-05	1.20e-05
0.012	–1.28e-05	1.69e-03	–3.79e-05	7.58e-06	6.43e-05	1.50e-05
0.016	3.56e-06	1.77e-03	4.53e-05	–1.47e-05	1.52e-06	6.51e-06
0.020	6.97e-06	1.86e-03	1.40e-04	–1.73e-05	–9.59e-05	–8.16e-06
0.024	1.68e-05	1.96e-03	1.86e-04	3.46e-05	–2.01e-04	–3.64e-05
0.028	8.73e-06	2.07e-03	1.07e-04	1.67e-04	–2.67e-04	–8.81e-05
0.032	–1.98e-05	2.19e-03	–2.56e-04	3.80e-04	–1.52e-04	–2.18e-04
0.036	–2.24e-05	2.33e-03	–1.10e-03	5.84e-04	3.94e-04	–5.53e-04
0.040	–2.95e-05	2.48e-03	–2.53e-03	7.54e-04	1.49e-03	–1.14e-03
0.044	3.65e-05	2.64e-03	–4.46e-03	8.74e-04	3.09e-03	–1.95e-03
0.048	7.11e-05	2.83e-03	–6.54e-03	9.73e-04	4.89e-03	–2.83e-03
0.052	6.30e-05	3.04e-03	–8.29e-03	1.13e-03	6.41e-03	–3.56e-03
0.056	–1.42e-04	3.27e-03	–9.25e-03	1.38e-03	7.24e-03	–3.97e-03
0.060	–4.49e-04	3.53e-03	–9.04e-03	1.93e-03	6.96e-03	–3.84e-03
0.064	–2.89e-04	3.87e-03	–7.53e-03	2.90e-03	5.37e-03	–3.06e-03
0.068	–2.72e-04	4.22e-03	–4.73e-03	4.32e-03	2.51e-03	–1.69e-03
0.072	–3.87e-04	4.55e-03	–9.82e-04	5.95e-03	–1.15e-03	–5.29e-05
0.076	–1.39e-04	5.09e-03	3.14e-03	7.23e-03	–4.72e-03	1.19e-03
0.080	4.92e-04	5.83e-03	6.98e-03	7.68e-03	–7.33e-03	1.50e-03
0.084	1.50e-03	6.70e-03	9.98e-03	6.90e-03	–8.27e-03	5.20e-04
0.088	9.97e-04	7.69e-03	1.19e-02	4.74e-03	–7.36e-03	–1.68e-03
0.092	–1.45e-03	8.81e-03	1.26e-02	1.43e-03	–4.82e-03	–4.65e-03
0.096	–3.84e-03	1.04e-02	1.22e-02	–2.63e-03	–1.17e-03	–7.77e-03
0.100	–1.58e-03	1.27e-02	1.10e-02	–6.60e-03	2.75e-03	–1.01e-02
0.104	1.30e-02	1.64e-02	9.20e-03	–9.57e-03	6.05e-03	–1.08e-02
0.108	4.64e-02	2.27e-02	7.06e-03	–1.08e-02	7.97e-03	–9.32e-03
0.112	1.05e-01	3.30e-02	4.91e-03	–9.84e-03	8.20e-03	–5.54e-03
0.116	1.95e-01	4.93e-02	3.07e-03	–7.06e-03	7.00e-03	–2.20e-04
0.120	3.14e-01	7.28e-02	1.72e-03	–3.05e-03	4.92e-03	5.68e-03
0.124	4.54e-01	1.04e-01	9.15e-04	1.34e-03	2.63e-03	1.10e-02
0.128	5.95e-01	1.42e-01	6.23e-04	5.31e-03	6.32e-04	1.50e-02

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.132	7.15e-01	1.84e-01	6.67e-04	8.16e-03	–7.36e-04	1.69e-02
0.136	7.93e-01	2.28e-01	8.34e-04	9.39e-03	–1.30e-03	1.66e-02
0.140	8.15e-01	2.68e-01	7.62e-04	8.84e-03	–1.25e-03	1.44e-02
0.144	7.77e-01	3.01e-01	1.20e-04	6.66e-03	–9.31e-04	1.08e-02
0.148	6.83e-01	3.21e-01	–1.23e-03	3.32e-03	–8.01e-04	6.60e-03
0.152	5.49e-01	3.27e-01	–3.18e-03	–5.48e-04	–1.13e-03	2.50e-03
0.156	3.96e-01	3.20e-01	–5.26e-03	–4.29e-03	–1.86e-03	–1.22e-03
0.160	2.50e-01	3.01e-01	–6.94e-03	–7.31e-03	–2.84e-03	–4.34e-03
0.164	1.30e-01	2.73e-01	–7.68e-03	–9.17e-03	–3.84e-03	–6.80e-03
0.168	4.47e-02	2.40e-01	–7.12e-03	–9.59e-03	–4.72e-03	–8.47e-03
0.172	–5.75e-03	2.06e-01	–5.15e-03	–8.55e-03	–5.39e-03	–9.25e-03
0.176	–2.72e-02	1.75e-01	–1.95e-03	–6.26e-03	–5.80e-03	–9.17e-03
0.180	–2.85e-02	1.49e-01	1.90e-03	–3.26e-03	–6.01e-03	–8.19e-03
0.184	–1.82e-02	1.28e-01	5.60e-03	–1.83e-04	–6.13e-03	–6.35e-03
0.188	–5.94e-03	1.11e-01	8.37e-03	2.37e-03	–6.29e-03	–3.77e-03
0.192	2.81e-03	9.82e-02	9.58e-03	4.08e-03	–6.50e-03	–7.34e-04
0.196	6.25e-03	8.84e-02	9.06e-03	5.05e-03	–6.67e-03	2.21e-03
0.200	5.54e-03	8.06e-02	6.92e-03	5.49e-03	–6.65e-03	4.54e-03
0.204	3.70e-03	7.39e-02	3.66e-03	5.66e-03	–6.24e-03	5.81e-03
0.208	1.64e-03	6.80e-02	6.86e-05	5.68e-03	–5.26e-03	5.91e-03
0.212	5.59e-05	6.26e-02	–3.01e-03	5.52e-03	–3.62e-03	4.88e-03
0.216	–1.02e-03	5.77e-02	–4.83e-03	5.16e-03	–1.33e-03	2.95e-03
0.220	–1.53e-03	5.34e-02	–4.97e-03	4.40e-03	1.42e-03	4.48e-04
0.224	–9.73e-04	4.96e-02	–3.46e-03	3.07e-03	4.28e-03	–2.25e-03
0.228	–3.20e-04	4.63e-02	–6.22e-04	1.04e-03	6.85e-03	–4.71e-03
0.232	2.89e-05	4.33e-02	2.90e-03	–1.55e-03	8.65e-03	–6.56e-03
0.236	1.73e-04	4.06e-02	6.35e-03	–4.20e-03	9.24e-03	–7.53e-03
0.240	1.33e-04	3.83e-02	8.95e-03	–6.40e-03	8.35e-03	–7.48e-03
0.244	1.39e-04	3.62e-02	1.02e-02	–7.73e-03	5.99e-03	–6.40e-03
0.248	9.80e-05	3.42e-02	9.77e-03	–8.11e-03	2.56e-03	–4.30e-03
0.252	4.22e-05	3.25e-02	7.90e-03	–7.70e-03	–1.34e-03	–1.35e-03
0.256	–2.56e-06	3.08e-02	4.95e-03	–6.76e-03	–5.02e-03	2.14e-03
0.260	–3.84e-05	2.93e-02	1.50e-03	–5.62e-03	–7.91e-03	5.67e-03

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.264	–2.83e-05	2.80e-02	–1.85e-03	–4.58e-03	–9.67e-03	8.59e-03
0.268	–2.41e-05	2.67e-02	–4.54e-03	-3.89e-03	–1.01e-02	1.04e-02
0.272	–8.46e-06	2.55e-02	–6.29e-03	–3.61e-03	–9.30e-03	1.08e-02
0.276	4.04e-07	2.44e-02	–7.13e-03	–3.62e-03	–7.62e-03	9.78e-03
0.280	4.91e-06	2.34e-02	–7.25e-03	–3.70e-03	–5.51e-03	7.51e-03
0.284	1.01e-05	2.24e-02	–6.97e-03	–3.61e-03	–3.40e-03	4.44e-03
0.288	3.79e-06	2.15e-02	–6.54e-03	–3.18e-03	–1.47e-03	1.18e-03
0.292	2.18e-06	2.07e-02	–6.11e-03	–2.37e-03	2.01e-04	–1.65e-03
0.296	–2.23e-06	1.99e-02	–5.78e-03	–1.23e-03	1.62e-03	–3.54e-03
0.300	–1.74e-06	1.92e-02	–5.43e-03	6.10e-05	2.78e-03	–4.28e-03
0.304	4.33e-07	1.85e-02	–4.87e-03	1.26e-03	3.62e-03	–3.93e-03
0.308	2.19e-07	1.79e-02	–3.88e-03	2.10e-03	4.14e-03	–2.74e-03
0.312	1.40e-06	1.73e-02	–2.42e-03	2.37e-03	4.25e-03	–1.08e-03
0.316	–5.61e-07	1.67e-02	–7.17e-04	1.97e-03	3.87e-03	6.99e-04
0.320	–4.40e-07	1.62e-02	9.57e-04	9.16e-04	2.95e-03	2.25e-03
0.324	–4.37e-07	1.56e-02	2.28e-03	–5.89e-04	1.53e-03	3.34e-03
0.328	–3.68e-08	1.51e-02	3.07e-03	–2.20e-03	–8.99e-05	3.92e-03
0.332	9.92e-07	1.47e-02	3.23e-03	–3.52e-03	–1.59e-03	4.04e-03
0.336	5.29e-07	1.43e-02	2.74e-03	–4.19e-03	–2.63e-03	3.85e-03
0.340	5.69e-07	1.38e-02	1.73e-03	–4.00e-03	–3.00e-03	3.44e-03
0.344	–1.87e-07	1.34e-02	4.38e-04	–2.97e-03	–2.62e-03	2.85e-03
0.348	–3.47e-07	1.31e-02	–8.80e-04	–1.22e-03	–1.53e-03	2.11e-03
0.352	–9.04e-08	1.27e-02	–2.04e-03	9.56e-04	5.06e-05	1.27e-03
0.356	8.10e-08	1.24e-02	–3.01e-03	3.22e-03	1.79e-03	3.65e-04
0.360	5.29e-07	1.20e-02	–3.78e-03	5.22e-03	3.32e-03	–5.53e-04
0.364	3.23e-07	1.17e-02	–4.36e-03	6.64e-03	4.36e-03	–1.41e-03
0.368	1.82e-07	1.14e-02	–4.67e-03	7.34e-03	4.82e-03	–2.03e-03
0.372	–6.93e-08	1.11e-02	–4.60e-03	7.31e-03	4.75e-03	–2.26e-03
0.376	–1.46e-07	1.09e-02	–4.11e-03	6.65e-03	4.31e-03	–1.98e-03
0.380	6.66e-08	1.06e-02	–3.17e-03	5.50e-03	3.64e-03	–1.29e-03
0.384	1.71e-07	1.03e-02	–1.84e-03	4.02e-03	2.88e-03	–3.97e-04
0.388	3.12e-07	1.01e-02	–2.24e-04	2.44e-03	2.18e-03	4.68e-04
0.392	1.95e-07	9.86e-03	1.51e-03	9.58e-04	1.59e-03	1.07e-03

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.396	5.86e-08	9.64e-03	3.13e-03	–2.37e-04	1.17e-03	1.30e-03
0.400	–2.48e-08	9.43e-03	4.40e-03	–1.02e-03	8.60e-04	1.08e-03
0.404	–3.03e-08	9.22e-03	5.16e-03	–1.34e-03	5.83e-04	4.43e-04
0.408	1.02e-07	9.02e-03	5.37e-03	–1.16e-03	2.87e-04	–4.57e-04
0.412	1.68e-07	8.83e-03	5.08e-03	–5.37e-04	-8.75e-05	–1.43e-03
0.416	1.93e-07	8.64e-03	4.41e-03	4.06e-04	–5.80e-04	–2.27e-03
0.420	1.20e-07	8.46e-03	3.49e-03	1.39e-03	–1.26e-03	–2.94e-03
0.424	3.01e-08	8.29e-03	2.45e-03	2.10e-03	–2.18e-03	–3.47e-03
0.428	5.52e-09	8.12e-03	1.40e-03	2.28e-03	–3.31e-03	–3.92e-03
0.432	2.95e-08	7.96e-03	4.39e-04	1.83e-03	–4.53e-03	–4.33e-03
0.436	1.05e-07	7.80e-03	–4.02e-04	8.46e-04	–5.62e-03	–4.64e-03
0.440	1.40e-07	7.65e-03	–1.11e-03	–4.79e-04	–6.34e-03	–4.79e-03
0.444	1.27e-07	7.51e-03	–1.71e-03	–1.86e-03	–6.51e-03	–4.72e-03
0.448	7.69e-08	7.37e-03	–2.18e-03	–2.95e-03	–6.01e-03	–4.34e-03
0.452	2.73e-08	7.23e-03	–2.53e-03	–3.49e-03	–4.88e-03	–3.66e-03
0.456	2.59e-08	7.10e-03	–2.75e-03	–3.31e-03	–3.20e-03	–2.68e-03
0.460	5.54e-08	6.97e-03	–2.83e-03	–2.57e-03	–1.24e-03	–1.56e-03
0.464	9.74e-08	6.85e-03	–2.80e-03	–1.60e-03	7.13e-04	–5.10e-04
0.468	1.11e-07	6.73e-03	–2.65e-03	–7.72e-04	2.36e-03	2.70e-04
0.472	8.93e-08	6.61e-03	–2.40e-03	–3.48e-04	3.50e-03	6.40e-04
0.476	5.48e-08	6.49e-03	–2.08e-03	–3.49e-04	4.12e-03	6.10e-04
0.480	3.08e-08	6.39e-03	–1.72e-03	–6.97e-04	4.26e-03	2.42e-04
0.484	3.87e-08	6.28e-03	–1.36e-03	–1.18e-03	4.05e-03	–3.37e-04
0.488	6.37e-08	6.17e-03	–1.02e-03	–1.52e-03	3.61e-03	–9.74e-04
0.492	8.60e-08	6.07e-03	–7.22e-04	–1.45e-03	3.03e-03	–1.52e-03
0.496	8.68e-08	5.98e-03	–5.08e-04	–7.85e-04	2.45e-03	–1.85e-03
0.500	6.64e-08	5.88e-03	–4.43e-04	4.01e-04	1.89e-03	–1.94e-03
0.504	4.41e-08	5.79e-03	–6.03e-04	1.84e-03	1.38e-03	–1.81e-03
0.508	3.47e-08	5.70e-03	–1.02e-03	3.19e-03	9.06e-04	–1.54e-03
0.512	4.54e-08	5.61e-03	–1.69e-03	4.14e-03	4.56e-04	–1.20e-03
0.516	6.35e-08	5.52e-03	–2.55e-03	4.57e-03	6.45e-05	–7.70e-04
0.520	7.41e-08	5.44e-03	–3.47e-03	4.40e-03	–2.43e-04	–2.64e-04
0.524	6.88e-08	5.36e-03	–4.30e-03	3.69e-03	–4.49e-04	3.11e-04

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.528	5.25e-08	5.28e-03	–4.86e-03	2.59e-03	–5.97e-04	9.07e-04
0.532	3.91e-08	5.20e-03	–4.98e-03	1.30e-03	–7.31e-04	1.46e-03
0.536	3.76e-08	5.13e-03	–4.57e-03	4.15e-05	–8.65e-04	1.90e-03
0.540	4.78e-08	5.05e-03	–3.67e-03	–1.04e-03	–9.88e-04	2.14e-03
0.544	5.97e-08	4.98e-03	–2.47e-03	–1.87e-03	–1.04e-03	2.11e-03
0.548	6.32e-08	4.91e-03	–1.16e-03	–2.42e-03	–9.79e-04	1.74e-03
0.552	5.59e-08	4.84e-03	4.24e-05	–2.70e-03	–7.35e-04	1.07e-03
0.556	4.40e-08	4.78e-03	9.93e-04	–2.70e-03	–2.60e-04	2.15e-04
0.560	3.68e-08	4.71e-03	1.60e-03	–2.43e-03	4.47e-04	–6.81e-04
0.564	3.90e-08	4.65e-03	1.85e-03	–1.93e-03	1.33e-03	–1.46e-03
0.568	4.74e-08	4.59e-03	1.86e-03	–1.22e-03	2.25e-03	–2.02e-03
0.572	5.44e-08	4.53e-03	1.78e-03	–3.47e-04	3.03e-03	–2.28e-03
0.576	5.40e-08	4.47e-03	1.74e-03	6.36e-04	3.49e-03	–2.22e-03
0.580	4.68e-08	4.41e-03	1.79e-03	1.66e-03	3.55e-03	–1.86e-03
0.584	3.86e-08	4.36e-03	1.86e-03	2.66e-03	3.17e-03	–1.27e-03
0.588	3.55e-08	4.30e-03	1.85e-03	3.54e-03	2.41e-03	–5.17e-04
0.592	3.92e-08	4.25e-03	1.67e-03	4.23e-03	1.41e-03	2.65e-04
0.596	4.55e-08	4.19e-03	1.23e-03	4.64e-03	3.37e-04	9.51e-04
0.600	4.89e-08	4.14e-03	5.18e-04	4.74e-03	-6.03e-04	1.45e-03
0.604	4.65e-08	4.09e-03	–4.25e-04	4.50e-03	–1.23e-03	1.72e-03
0.608	4.03e-08	4.04e-03	–1.43e-03	3.96e-03	–1.42e-03	1.79e-03
0.612	3.52e-08	3.99e-03	–2.30e-03	3.21e-03	–1.13e-03	1.73e-03
0.616	3.46e-08	3.95e-03	–2.85e-03	2.33e-03	–4.11e-04	1.62e-03
0.620	3.84e-08	3.90e-03	–2.96e-03	1.44e-03	6.15e-04	1.56e-03
0.624	4.26e-08	3.86e-03	–2.66e-03	6.40e-04	1.76e-03	1.61e-03
0.628	4.37e-08	3.81e-03	–2.01e-03	1.25e-05	2.81e-03	1.78e-03
0.632	4.06e-08	3.77e-03	–1.16e-03	–4.14e-04	3.60e-03	2.01e-03
0.636	3.58e-08	3.72e-03	–2.62e-04	–6.60e-04	4.00e-03	2.11e-03
0.640	3.29e-08	3.68e-03	5.11e-04	–7.79e-04	3.95e-03	1.94e-03
0.644	3.37e-08	3.64e-03	1.04e-03	–8.48e-04	3.47e-03	1.38e-03
0.648	3.69e-08	3.60e-03	1.32e-03	–9.56e-04	2.68e-03	4.76e-04
0.652	3.95e-08	3.56e-03	1.38e-03	–1.17e-03	1.71e-03	–6.44e-04
0.656	3.91e-08	3.52e-03	1.32e-03	–1.52e-03	7.06e-04	–1.80e-03

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.660	3.60e-08	3.48e-03	1.24e-03	–1.97e-03	–2.19e-04	–2.78e-03
0.664	3.25e-08	3.45e-03	1.22e-03	–2.47e-03	–1.02e-03	–3.39e-03
0.668	3.12e-08	3.41e-03	1.34e-03	–2.93e-03	–1.66e-03	–3.51e-03
0.672	3.26e-08	3.38e-03	1.58e-03	–3.22e-03	–2.14e-03	–3.12e-03
0.676	3.51e-08	3.34e-03	1.92e-03	–3.27e-03	–2.45e-03	–2.36e-03
0.680	3.64e-08	3.31e-03	2.26e-03	–3.01e-03	–2.58e-03	–1.40e-03
0.684	3.52e-08	3.27e-03	2.53e-03	–2.48e-03	–2.54e-03	–4.72e-04
0.688	3.24e-08	3.24e-03	2.67e-03	–1.77e-03	–2.30e-03	2.96e-04
0.692	3.01e-08	3.21e-03	2.66e-03	–1.04e-03	–1.85e-03	8.20e-04
0.696	2.98e-08	3.17e-03	2.47e-03	–4.69e-04	–1.20e-03	1.07e-03
0.700	3.13e-08	3.14e-03	2.17e-03	–1.76e-04	–4.09e-04	1.10e-03
0.704	3.31e-08	3.11e-03	1.78e-03	–2.25e-04	4.27e-04	9.85e-04
0.708	3.34e-08	3.08e-03	1.38e-03	–6.12e-04	1.21e-03	8.49e-04
0.712	3.19e-08	3.05e-03	9.74e-04	–1.24e-03	1.87e-03	7.97e-04
0.716	2.96e-08	3.02e-03	5.40e-04	–1.94e-03	2.35e-03	8.91e-04
0.720	2.83e-08	2.99e-03	4.50e-05	–2.52e-03	2.66e-03	1.15e-03
0.724	2.86e-08	2.96e-03	–5.39e-04	–2.82e-03	2.80e-03	1.56e-03
0.728	2.99e-08	2.94e-03	–1.21e-03	–2.76e-03	2.82e-03	2.06e-03
0.732	3.10e-08	2.91e-03	–1.93e-03	–2.34e-03	2.78e-03	2.56e-03
0.736	3.07e-08	2.88e-03	–2.63e-03	–1.64e-03	2.70e-03	2.99e-03
0.740	2.91e-08	2.86e-03	–3.19e-03	–8.03e-04	2.59e-03	3.27e-03
0.744	2.75e-08	2.83e-03	–3.49e-03	2.08e-05	2.40e-03	3.36e-03
0.748	2.68e-08	2.80e-03	–3.41e-03	6.61e-04	2.08e-03	3.25e-03
0.752	2.74e-08	2.78e-03	–2.90e-03	9.96e-04	1.62e-03	2.96e-03
0.756	2.85e-08	2.75e-03	–1.98e-03	9.72e-04	1.01e-03	2.54e-03
0.760	2.89e-08	2.73e-03	–7.19e-04	6.06e-04	3.03e-04	2.04e-03
0.764	2.83e-08	2.71e-03	7.27e-04	–1.29e-05	–4.51e-04	1.55e-03
0.768	2.69e-08	2.68e-03	2.19e-03	–7.52e-04	–1.17e-03	1.09e-03
0.772	2.57e-08	2.66e-03	3.49e-03	–1.45e-03	–1.76e-03	6.97e-04
0.776	2.55e-08	2.64e-03	4.45e-03	–1.95e-03	–2.16e-03	3.84e-04
0.780	2.62e-08	2.61e-03	4.96e-03	–2.13e-03	–2.35e-03	1.50e-04
0.784	2.70e-08	2.59e-03	4.94e-03	–1.91e-03	–2.33e-03	–9.21e-06
0.788	2.70e-08	2.57e-03	4.41e-03	–1.30e-03	–2.16e-03	–1.09e-04

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.792	2.62e-08	2.55e-03	3.43e-03	–3.53e-04	–1.88e-03	–1.67e-04
0.796	2.50e-08	2.53e-03	2.14e-03	7.94e-04	–1.52e-03	–1.97e-04
0.800	2.43e-08	2.51e-03	6.97e-04	1.99e-03	–1.11e-03	–2.12e-04
0.804	2.44e-08	2.48e-03	–7.29e-04	3.07e-03	–6.76e-04	–2.16e-04
0.808	2.50e-08	2.46e-03	–1.98e-03	3.92e-03	–2.42e-04	–2.11e-04
0.812	2.55e-08	2.44e-03	–2.95e-03	4.47e-03	1.71e-04	–1.93e-04
0.816	2.52e-08	2.43e-03	–3.56e-03	4.69e-03	5.47e-04	–1.58e-04
0.820	2.44e-08	2.41e-03	–3.79e-03	4.59e-03	8.49e-04	–1.06e-04
0.824	2.35e-08	2.39e-03	–3.68e-03	4.24e-03	1.04e-03	–4.15e-05
0.828	2.31e-08	2.37e-03	–3.29e-03	3.71e-03	1.09e-03	3.17e-05
0.832	2.34e-08	2.35e-03	–2.72e-03	3.10e-03	9.78e-04	1.09e-04
0.836	2.38e-08	2.33e-03	–2.02e-03	2.46e-03	7.26e-04	1.89e-04
0.840	2.40e-08	2.31e-03	–1.28e-03	1.85e-03	3.61e-04	2.70e-04
0.844	2.36e-08	2.29e-03	–5.54e-04	1.30e-03	–7.48e-05	3.50e-04
0.848	2.29e-08	2.28e-03	9.66e-05	8.67e-04	–5.29e-04	4.35e-04
0.852	2.22e-08	2.26e-03	6.28e-04	5.63e-04	–9.51e-04	5.28e-04
0.856	2.21e-08	2.24e-03	1.02e-03	3.91e-04	–1.30e-03	6.25e-04
0.860	2.24e-08	2.23e-03	1.26e-03	3.27e-04	–1.54e-03	7.05e-04
0.864	2.27e-08	2.21e-03	1.35e-03	3.18e-04	–1.67e-03	7.38e-04
0.868	2.27e-08	2.19e-03	1.32e-03	3.13e-04	–1.71e-03	7.00e-04
0.872	2.22e-08	2.18e-03	1.20e-03	2.49e-04	–1.65e-03	5.79e-04
0.876	2.15e-08	2.16e-03	1.06e-03	6.50e-05	–1.54e-03	3.86e-04
0.880	2.11e-08	2.15e-03	9.49e-04	–2.75e-04	–1.39e-03	1.42e-04
0.884	2.11e-08	2.13e-03	9.05e-04	–7.77e-04	–1.23e-03	–1.19e-04
0.888	2.14e-08	2.11e-03	9.32e-04	–1.40e-03	–1.08e-03	–3.50e-04
0.892	2.16e-08	2.10e-03	1.01e-03	–2.06e-03	–9.51e-04	–5.12e-04
0.896	2.14e-08	2.08e-03	1.10e-03	–2.69e-03	–8.58e-04	–5.74e-04
0.900	2.09e-08	2.07e-03	1.17e-03	–3.22e-03	–8.19e-04	–5.37e-04
0.904	2.04e-08	2.06e-03	1.17e-03	–3.60e-03	–8.53e-04	–4.30e-04
0.908	2.02e-08	2.04e-03	1.07e-03	–3.81e-03	–9.70e-04	–2.86e-04
0.912	2.02e-08	2.03e-03	8.84e-04	–3.86e-03	–1.17e-03	–1.38e-04
0.916	2.05e-08	2.01e-03	6.43e-04	–3.76e-03	–1.43e-03	–3.73e-06
0.920	2.05e-08	2.00e-03	4.00e-04	–3.57e-03	–1.72e-03	1.07e-04

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.924	2.03e-08	1.99e-03	2.04e-04	–3.32e-03	–2.00e-03	1.97e-04
0.928	1.98e-08	1.97e-03	8.04e-05	–3.05e-03	–2.21e-03	2.83e-04
0.932	1.94e-08	1.96e-03	3.54e-05	–2.77e-03	–2.31e-03	3.84e-04
0.936	1.93e-08	1.95e-03	6.11e-05	–2.49e-03	–2.25e-03	5.12e-04
0.940	1.94e-08	1.93e-03	1.19e-04	–2.19e-03	–2.02e-03	6.60e-04
0.944	1.96e-08	1.92e-03	1.68e-04	–1.87e-03	–1.61e-03	7.99e-04
0.948	1.95e-08	1.91e-03	1.69e-04	–1.51e-03	–1.04e-03	8.98e-04
0.952	1.92e-08	1.90e-03	1.12e-04	–1.11e-03	–3.35e-04	9.23e-04
0.956	1.88e-08	1.88e-03	3.20e-05	–6.75e-04	4.63e-04	8.56e-04
0.960	1.86e-08	1.87e-03	–3.29e-05	–2.21e-04	1.31e-03	6.88e-04
0.964	1.85e-08	1.86e-03	–3.97e-05	2.28e-04	2.16e-03	4.27e-04
0.968	1.86e-08	1.85e-03	3.82e-05	6.47e-04	2.94e-03	1.05e-04
0.972	1.87e-08	1.84e-03	2.03e-04	1.01e-03	3.58e-03	–2.35e-04
0.976	1.86e-08	1.82e-03	4.37e-04	1.30e-03	4.03e-03	–5.42e-04
0.980	1.83e-08	1.81e-03	6.79e-04	1.50e-03	4.23e-03	–7.76e-04
0.984	1.80e-08	1.80e-03	8.54e-04	1.61e-03	4.14e-03	–9.10e-04
0.988	1.78e-08	1.79e-03	8.92e-04	1.65e-03	3.77e-03	–9.27e-04
0.992	1.78e-08	1.78e-03	7.59e-04	1.61e-03	3.13e-03	–8.27e-04
0.996	1.79e-08	1.77e-03	4.78e-04	1.51e-03	2.31e-03	–6.23e-04
1.000	1.79e-08	1.76e-03	9.92e-05	1.35e-03	1.38e-03	–3.43e-04
1.004	1.77e-08	1.75e-03	–3.03e-04	1.14e-03	4.42e-04	–2.81e-05
1.008	1.74e-08	1.74e-03	–6.46e-04	8.71e-04	–4.26e-04	2.80e-04
1.012	1.72e-08	1.73e-03	–8.64e-04	5.31e-04	–1.16e-03	5.35e-04
1.016	1.71e-08	1.71e-03	–9.09e-04	1.17e-04	–1.71e-03	6.95e-04
1.020	1.71e-08	1.70e-03	–7.85e-04	–3.71e-04	–2.06e-03	7.20e-04
1.024	1.72e-08	1.69e-03	–5.39e-04	–9.22e-04	–2.21e-03	5.83e-04
1.028	1.71e-08	1.68e-03	–2.39e-04	–1.51e-03	–2.20e-03	2.80e-04
1.032	1.69e-08	1.67e-03	4.62e-05	–2.08e-03	–2.04e-03	–1.70e-04
1.036	1.67e-08	1.66e-03	2.68e-04	–2.58e-03	–1.78e-03	–7.21e-04
1.040	1.65e-08	1.66e-03	3.93e-04	–2.92e-03	–1.45e-03	–1.31e-03
1.044	1.65e-08	1.65e-03	4.08e-04	–3.07e-03	–1.08e-03	–1.86e-03
1.048	1.65e-08	1.64e-03	3.24e-04	–2.97e-03	–6.97e-04	–2.29e-03
1.052	1.65e-08	1.63e-03	1.64e-04	-2.62e-03	-3.38e-04	-2.53e-03

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
1.056	1.64e-08	1.62e-03	–2.93e-05	–2.04e-03	–2.07e-05	–2.54e-03
1.060	1.62e-08	1.61e-03	–2.24e-04	–1.30e-03	2.39e-04	–2.32e-03
1.064	1.60e-08	1.60e-03	–3.91e-04	–4.72e-04	4.34e-04	–1.91e-03
1.068	1.59e-08	1.59e-03	–5.13e-04	3.49e-04	5.60e-04	–1.37e-03
1.072	1.59e-08	1.58e-03	–5.79e-04	1.08e-03	6.21e-04	–7.75e-04
1.076	1.59e-08	1.57e-03	–5.84e-04	1.66e-03	6.27e-04	–2.13e-04
1.080	1.59e-08	1.56e-03	–5.35e-04	2.04e-03	5.90e-04	2.42e-04
1.084	1.57e-08	1.56e-03	–4.46e-04	2.24e-03	5.24e-04	5.43e-04
1.088	1.55e-08	1.55e-03	–3.40e-04	2.26e-03	4.42e-04	6.80e-04
1.092	1.54e-08	1.54e-03	–2.40e-04	2.14e-03	3.58e-04	6.70e-04
1.096	1.53e-08	1.53e-03	–1.64e-04	1.95e-03	2.82e-04	5.53e-04
1.100	1.53e-08	1.52e-03	–1.21e-04	1.72e-03	2.23e-04	3.73e-04
1.104	1.53e-08	1.51e-03	–1.09e-04	1.48e-03	1.90e-04	1.72e-04
1.108	1.53e-08	1.51e-03	–1.19e-04	1.27e-03	1.85e-04	–1.10e-05
1.112	1.51e-08	1.50e-03	–1.38e-04	1.09e-03	2.03e-04	–1.51e-04
1.116	1.49e-08	1.49e-03	–1.54e-04	9.49e-04	2.33e-04	–2.31e-04
1.120	1.48e-08	1.48e-03	–1.57e-04	8.36e-04	2.60e-04	–2.52e-04
1.124	1.48e-08	1.47e-03	–1.42e-04	7.46e-04	2.72e-04	–2.18e-04
1.128	1.48e-08	1.47e-03	–1.14e-04	6.77e-04	2.53e-04	–1.33e-04
1.132	1.48e-08	1.46e-03	–8.40e-05	6.30e-04	1.95e-04	–6.35e-06
1.136	1.47e-08	1.45e-03	–6.31e-05	6.05e-04	9.72e-05	1.50e-04
1.140	1.45e-08	1.44e-03	–5.84e-05	5.99e-04	–2.78e-05	3.12e-04
1.144	1.44e-08	1.44e-03	–7.04e-05	6.01e-04	–1.58e-04	4.51e-04
1.148	1.43e-08	1.43e-03	–9.63e-05	6.02e-04	–.69e-04	5.45e-04
1.152	1.43e-08	1.42e-03	–1.29e-04	5.87e-04	–3.41e-04	5.76e-04
1.156	1.43e-08	1.42e-03	–1.60e-04	5.43e-04	–3.62e-04	5.36e-04
1.160	1.42e-08	1.41e-03	–1.81e-04	4.58e-04	–3.29e-04	4.30e-04
1.164	1.41e-08	1.40e-03	–1.83e-04	3.30e-04	–2.48e-04	2.72e-04
1.168	1.40e-08	1.39e-03	–1.65e-04	1.72e-04	–1.35e-04	9.19e-05
1.172	1.39e-08	1.39e-03	–1.28e-04	4.95e-06	–1.13e-05	–7.86e-05
1.176	1.38e-08	1.38e-03	–7.75e-05	–1.48e-04	1.02e-04	–2.10e-04
1.180	1.38e-08	1.37e-03	–1.90e-05	–2.62e-04	1.90e-04	–2.83e-04
1.184	1.38e-08	1.37e-03	4.03e-05	-3.19e-04	2.48e-04	-2.93e-04

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
1.188	1.37e-08	1.36e-03	9.40e-05	–3.07e-04	2.73e-04	–2.43e-04
1.192	1.36e-08	1.35e-03	1.37e-04	–2.28e-04	2.68e-04	–1.50e-04
1.196	1.35e-08	1.35e-03	1.66e-04	–9.21e-05	2.37e-04	–3.64e-05
1.200	1.34e-08	1.34e-03	1.80e-04	7.95e-05	1.86e-04	7.45e-05
1.204	1.34e-08	1.34e-03	1.79e-04	2.63e-04	1.22e-04	1.62e-04
1.208	1.34e-08	1.33e-03	1.62e-04	4.36e-04	5.03e-05	2.17e-04
1.212	1.33e-08	1.32e-03	1.27e-04	5.81e-04	–2.48e-05	2.37e-04
1.216	1.33e-08	1.32e-03	7.69e-05	6.83e-04	–9.88e-05	2.28e-04
1.220	1.32e-08	1.31e-03	1.24e-05	7.35e-04	–1.66e-04	2.01e-04
1.224	1.31e-08	1.30e-03	–6.03e-05	7.34e-04	–2.22e-04	1.66e-04
1.228	1.30e-08	1.30e-03	–1.36e-04	6.87e-04	–2.61e-04	1.35e-04
1.232	1.29e-08	1.29e-03	–2.14e-04	6.00e-04	–2.84e-04	1.13e-04
1.236	1.29e-08	1.29e-03	–2.89e-04	4.86e-04	–2.93e-04	1.02e-04
1.240	1.29e-08	1.28e-03	–3.66e-04	3.57e-04	–2.97e-04	9.58e-05
1.244	1.29e-08	1.27e-03	–4.41e-04	2.30e-04	–3.00e-04	9.07e-05
1.248	1.29e-08	1.27e-03	–5.17e-04	1.15e-04	–3.10e-04	7.92e-05

32.6.1.3.2 Receiver test mode

To facilitate the testing of the receiver in the presence of synchronous 100BASE-T2 alien NEXT, a special receiver test mode shall be required to allow for receiver alien NEXT tolerance and jitter testing. For a PHY with an MII, this mode shall be enabled by setting bit 9.13 (MASTER-SLAVE Control register) of the MII management register set to a 1. A PHY without an MII shall provide a means to enable this test mode. This mode shall not be overridden except by clearing bit 9.13 or resetting the PHY.

When the receive test mode is enabled, the receiver shall configure itself in SLAVE mode, continually attempt to bring its receiver up until successful receiver operation is achieved and transmit symbols in idle mode. For a PHY with an MII, when the receiver is properly detecting the received data (loc_rcvr_status=OK), it shall set bit 10.13 of the MII management register to 1 and reset the error count in bits 10.0 through 10.7 (MSB) to zero. The error count shall be incremented for every symbol error detected in the received idle sequence (where rem_rcvr_status is assumed to be OK). Upon loss of proper data reception, the receiver shall clear bit 10.13. A PHY without an MII shall provide a means to realize this function. The vendor shall provide a means to enable this mode for conformance testing.

32.6.1.3.3 Receiver differential input signals

Differential signals received on the receive inputs that were transmitted within the specifications given in 32.6.1.2, and have then passed through a link as defined in 32.7, shall be translated into one of the

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PMA_UNITDATA.indicate messages with an symbol error rate less than 10^{-10} and sent to the PCS after link bring-up.

Performance shall be tested in at least two configurations: using a 100 m link segment conformant to 32.7 and with a link segment less than 1 m in length between transmitter and receiver.

32.6.1.3.4 Receiver Alien NEXT tolerance

Differential signals received from the test channel defined in 32.6.1.3.1 shall be detected with a symbol error rate less than 10^{-8} when the PHY is in receiver test mode for the following combinations of channel and worst-case alien NEXT responses, as shown in Table 32-13.

Table 32-13—Receiver Alien NEXT test cases

Case	Cable channels	NEXT Channels			
		A1	A2	B1	B2
1	0 m	Alien NEXT 1	Alien NEXT 3	Alien NEXT 4	Alien NEXT 2
2	0 m	Alien NEXT 1	Alien NEXT 4	Alien NEXT 3	Alien NEXT 2
3	100 m	Alien NEXT 1	Alien NEXT 3	Alien NEXT 4	Alien NEXT 2
4	100 m	Alien NEXT 1	Alien NEXT 4	Alien NEXT 3	Alien NEXT 2

NOTE—Implementors will find it practically impossible to meet the requirements of this subclause without using some form of adaptive equalization and cyclostationary interference suppression.

32.6.1.3.5 Receiver timing jitter

For the test channels described below, the peak-to-peak value of RX_CLK zero-crossing jitter shall be less than 1.3 ns after the receiver is properly receiving the data and has set bit 9.13 of the MII management register set to 1. When the jitter waveform on RX_CLK is filtered by a high pass filter having the transfer function below,[16] the peak-to-peak value of the resulting filtered timing jitter shall be less than 0.8 ns.

Test channels:

Channels 1–4 are the test channels described in 32.6.1.3.1 with the four combinations of worst-case channel and alien NEXT responses tabulated in 32.6.1.3.4.

Channels 5–6 are the test channels described in 32.6.1.3.1 with the combinations of worst-case channel and alien NEXT responses tabulated in cases 1 and 2 of 32.6.1.3.4 plus the addition of 100 m of Category 3 compliant cable between the test channel fixture and the PHY under test.

$$H_{\text{jitterfilter}}(f) = \frac{jf}{jf + 1000} \qquad f \text{ in Hz}$$

The RX_CLK of the MII shall be made available for this test. A PHY without an MII shall provide an equivalent clock.

32.6.1.3.6 Common-mode noise rejection

While receiving packets from a compliant 100BASE-T2 transmitter, connected to all MDI pins, a receiver shall send the proper PMA_UNITDATA.indicate messages to the PCS for any differential input signal E_s that results in a signal E_{dif} that meets 32.6.1.3.3 even in the presence of common mode voltages E_{cm} (applied

[16] "j" denotes the positive square root of –1.

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as shown in Figure 32–21). E_{cm} shall be a 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%-80%), connected to each of the pairs (BI_DA+, BI_DA-) and (BI_DB+, BI_DB-).

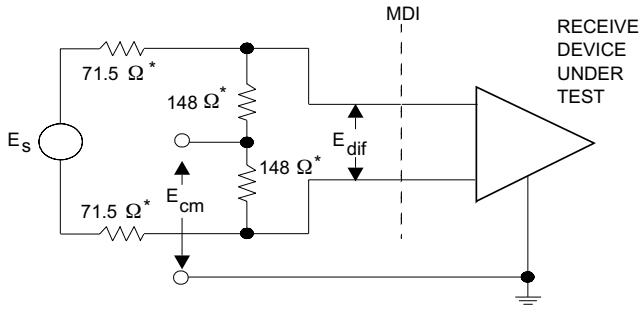


Figure 32–21—Receiver common-mode noise rejection test circuit

32.6.1.3.7 Receiver frequency tolerance

The receive feature shall properly receive incoming data with a 5-level symbol rate within the range 25.000 MHz ± 0.01%.

32.6.1.4 MDI Specifications

32.6.1.4.1 MDI differential impedance

The differential impedance as measured at the MDI for each transmit/receive channel shall be such that any reflection due to differential signals incident upon the MDI from a balanced cabling having an impedance of 100 Ω is at least 17 dB below the incident signal over the frequency range 2.0–6.5 MHz and at least 12.9–20 $\log_{10}(f/10)$ dB over the frequency range 6.5–25 MHz (f in MHz). This return loss shall be maintained at all times when the PHY is transmitting data.

32.6.1.4.2 MDI impedance balance

Over the frequency range 2.0–25.0 MHz, the common-mode to differential-mode impedance balance of each channel of the MDI shall exceed

$$29 - 17\log\left(\frac{f}{10}\right) \text{ dB}$$

where f is the frequency in MHz when the transmitter is transmitting idle mode data (transmit test mode 3).

The balance is defined as

$$20\log\left(\frac{E_{cm}}{E_{dif}}\right)$$

where E_{cm} is an externally applied sine wave voltage as shown in Figure 32–22 and E_{dif} is the resulting waveform due only to the applied sine wave and not the transmitted data.[17]

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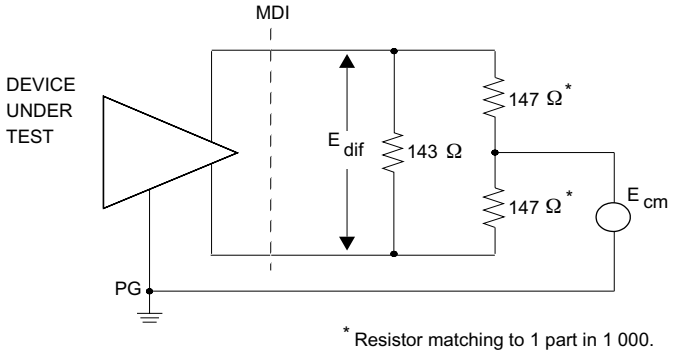


Figure 32–22—MDI impedance balance test circuit

NOTE—The balance of the test equipment (such as the matching of the test resistors) must be insignificant relative to the balance requirements.

32.6.1.4.3 MDI common-mode output voltage

The implementor should consider any applicable local, national, or international regulations. Driving balanced cable pairs with high-frequency common mode voltages may cause radiated emissions which may result in interference to other equipment. FCC conducted and radiated emissions tests may require that the magnitude of the total common mode output voltage, E_{cm_out}, on any transmit circuit, when measured as shown in Figure 32–23, be less than a few millivolts when transmitting data.

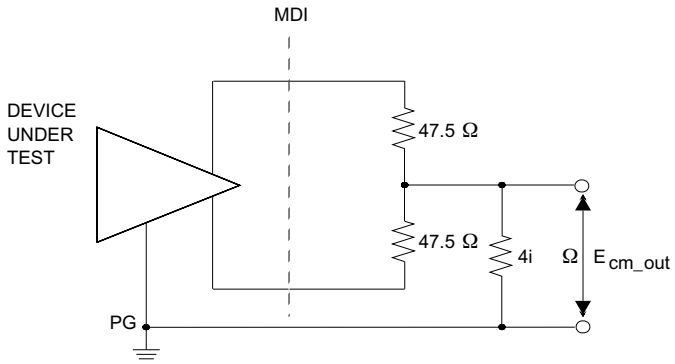


Figure 32–23—Common-mode output voltage test circuit

NOTE—The balance of the test equipment (such as the matching of the test resistors) must be insignificant relative to the balance requirements.

32.6.1.4.4 MDI fault tolerance

Transmitters and receivers shall withstand without damage the application of short circuits across any MDI port for an indefinite period of time and shall resume normal operation after such faults are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

Transmitters shall withstand without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity (as indicated in Figure 32–24). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

[17]Triggered averaging can be used to separate the component due to the applied common-mode sine wave from the transmitted data component.

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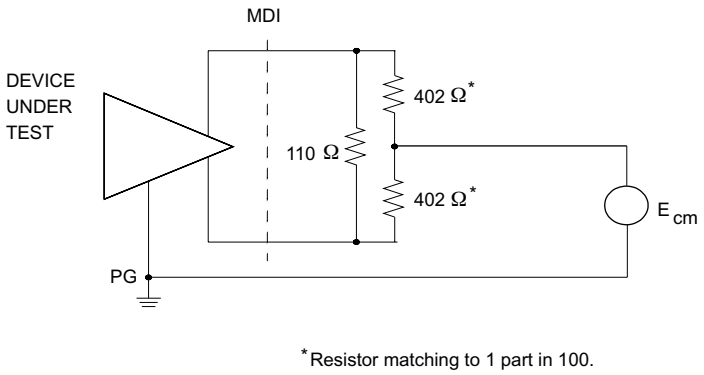


Figure 32–24—MDI fault tolerance test circuit

32.6.2 Power consumption

After 100 ms following PowerOn, the current drawn by the PHY shall not exceed 1.0 A when powered through the MII.

The PHY shall be capable of operating from all voltage sources allowed by Clause 22, including those current limited to 1.0 A, as supplied by the DTE or repeater through the resistance of all permissible MII cabling.

The PHY shall not introduce extraneous signals on the MII control circuits during normal power-up and power-down.

While in power-down mode, the PHY is not required to meet any of the 100BASE-T2 performance requirements.

32.7 Link segment characteristics

100BASE-T2 employs a dual duplex transmission system, i.e., two full duplex channels are used simultaneously to transmit data. The use of the term *link segment* in this clause refers to two duplex channels and the specifications for a link segment apply individually to each of the two duplex channels. Furthermore, the term duplex channel will be used to refer a single channel of the dual duplex link segment.

100BASE-T2 is designed to allow use of the pairs of the cabling other than the two used for the full duplex channels of the 100BASE-T2 service. Services supported for use in the other pairs are as follows:

a) 100BASE-T2
b) 10BASE-T
c) Digital phone services compliant with the ITU-T Recommendation I.430 and ANSI T1.605 and T1.601

32.7.1 Cabling

Cabling and installation practices generally suitable for use with this standard appear in ISO/IEC 11801. Exceptions, notes, and additional requirements are as listed below.

a) 100BASE-T2 uses a star topology. Balanced cabling is used to connect PHY entities.
b) 100BASE-T2 is an ISO 11801 class C application, with additional installation requirements and transmission parameters specified in 32.7.2–32.7.4. The width of the PAM5 × 5 transmit spectrum is

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approximately 25 MHz (as shown in Figure 32–19). The aggregate data rate for two pairs using PAM5 × 5 coding is 100 Mb/s.

c) 100BASE-T2 shall use 2 pairs of balanced cabling, Category 3 or better, with a nominal characteristic impedance of 100 Ω.
d) When using Category 3 cabling for the link segment, Clause 32 recommends, but does not require, the use of Category 4 or better connecting hardware, patch cords and jumpers. The use of Category 4 or better connecting hardware increases the link segment composite NEXT loss, composite ELFEXT loss and reduces the link segment insertion loss. This lowers the link segment crosstalk noise which in turn decreases the probability of errors.
e) The use of shielding is outside the scope of this standard.
f) The use of other cabling systems is discussed in Annex 32A.

32.7.2 Link transmission parameters

Unless otherwise specified, link segment testing shall be conducted using source and load impedances of 100 Ω.

The tolerance on the poles of the test filter used in this clause shall be ± 1%.

32.7.2.1 Insertion loss

The insertion loss of a link segment shall be no more than 14.6 dB at all frequencies between 2 and 16 MHz. This consists of the attenuation of the balanced cabling pairs, connector losses, and reflection losses due to impedance mismatches between the various components of the link segment. The insertion loss specification shall be met when the link segment is terminated in source and load impedances that satisfy 32.6.1.4.1.

NOTE—The loss of PVC-insulated cabling exhibits significant temperature dependence. At temperatures greater than 40 ^{o}C, it may be necessary to use a less temperature-dependent cabling, such as many Fluorinated Ethylene Propylene (FEP), Polytetrafluoroethylene (PTFE), or Perfluoroalkoxy (PFA) plenum-rated cabling.

32.7.2.2 Differential characteristic impedance

The cable used in the links shall meet the requirements for characteristic impedance specified in ISO/IEC 11801. Connecting hardware shall meet the return loss requirements for connecting hardware specified in ISO/IEC 11801.

32.7.2.3 Coupling parameters

In order to limit the noise coupled into a duplex channel from an adjacent duplex channel, Near-End Crosstalk (NEXT) loss and Equal Level Far-End Crosstalk (ELFEXT) loss are specified for each link segment. In addition, since two dual-duplex connections may co-exist in a 4-pair cabling and a receiver on a duplex channel will be disturbed by crosstalk from one to three other duplex (or simplex) channels, Multiple-Disturber NEXT loss and Multiple-Disturber ELFEXT loss are also specified. When a 10BASE-T service is used within the same cabling, a restriction on the allowable NEXT loss to Insertion Loss (NIR) of the cabling is required and is specified in 32.7.2.3.5.

32.7.2.3.1 Differential near-end crosstalk (NEXT) loss

The differential Near-End Crosstalk (NEXT) loss between the two duplex channels of a link segment is specified in order to limit the crosstalk noise at the near end of a link segment to meet the symbol error rate objective specified in 32.1 and the noise specifications of 32.7.3. The NEXT loss between the two duplex channels of a link segment shall be at least $19.3 - 16.6\log_{10}(f/16)$ (where f is the frequency in MHz) over the frequency range 2–16 MHz.

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32.7.2.3.2 Multiple-disturber NEXT (MDNEXT) loss

Since two dual duplex applications (connections) may exist in a 4-pair cabling system, a received signal may be disturbed by multiple alien NEXT signals. The MDNEXT loss between each link segment duplex channel and the two alien data carrying duplex channels shall be at least $19.0–16.6\log_{10}(f/16)$ dB (where f is the frequency in MHz) over the frequency range 2.0–16 MHz. MDNEXT is computed as the power sum of the individual NEXT losses. This specification is consistent with two disturbers, each with a NEXT loss of at least $22.0–16.6\log_{10}(f/16)$.

NOTE—Since the self NEXT noise from the other duplex channel of a connection can be cancelled using digital signal processing techniques whereas the alien NEXT noise from an alien connection can not be cancelled in the same fashion, the self NEXT noise is treated differently than the alien NEXT noise and is not included in the MDNEXT calculation.

32.7.2.3.3 Equal level far-end crosstalk loss (ELFEXT)

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk noise at the far end of a link segment to meet the symbol error rate objective specified in 32.1 and the noise specifications of 32.7.3. Far-End Crosstalk (FEXT) noise is the crosstalk noise that appears at the far end of one of the duplex channels which is coupled from one of the duplex channels with the noise source (transmitters) at the near end. ELFEXT loss is the ratio of the data signal to FEXT noise at the far end output of a duplex channel. To limit the FEXT noise from an adjacent duplex channel, the ELFEXT loss between each duplex channel shall be greater than $20.9–20\log_{10}(f/16)$ dB (where f is the frequency in MHz) over the frequency range 2–16 MHz. ELFEXT loss at frequency f and distance l is defined as

$$\text{ELFEXT\_Loss}(f,l) = 20\log_{10}(\text{Vpds/Vpcn}) - \text{SLS\_Loss(dB)}$$

where Vpds = peak voltage of disturbing signal (near-end transmitter), Vpcn = peak crosstalk noise at far-end of disturbed channel, and SLS_Loss = insertion loss of the disturbing channel.

32.7.2.3.4 Multiple-disturber ELFEXT (MDELFEXT) loss

Since two duplex channels are used to transfer data between PHYs and two connections can exist in a 4-pair cabling, the FEXT noise that is coupled into a data carrying duplex channel is from one to three disturbers. The MDELFEXT loss between a duplex channel and the other data carrying duplex channels shall be greater than $19.9–20\log_{10}(f/16)$ (where f is the frequency in MHz) over the frequency range 2–16 MHz.This specification is consistent with three disturbers, one with a FEXT loss of at least $20.9–20\log_{10}(f/16)$ and two with a FEXT loss of at least $27.0–20\log_{10}(f/16)$.

MDELNEXT is computed as the power sum of the individual FEXT losses.

32.7.2.3.5 10BASE-T NEXT loss to insertion loss ratio requirement

The objective of this specification is to support the coexistence of a 100BASE-T2 link segment and a 10BASE-T link segment in a 4-pair cable. When a 100BASE-T2 link segment operates in the same 4-pair cable with a 10BASE-T link segment, each 100BASE-T2 duplex channel will receive alien NEXT noise signals from the 10BASE-T link segment. To ensure reliable operation, a minimum signal to noise ratio must be maintained. This minimum signal to noise ratio is assured by meeting the following NEXT loss to insertion loss ratio (NIR).

NIR is defined by the following equation:

$$NIR\ (\text{dB}) = (AdjustedNEXTLoss - InsertionLoss_{6\ \text{MHz}})$$

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where $InsertionLoss_{6\ MHz}$ is the maximum of the insertion loss at 6 MHz of the two duplex channels of the 100BASE-T2 link segment and *AdjustedNEXTLoss* is determined by the following algorithm:

AdjustedNEXTLoss Algorithm

Step 1. Measure the NEXT loss as a function of frequency over the range 1–16 MHz for each of the six pair combinations between the four pairs of the cabling. The maximum spacing in frequency of the samples shall be 250 kHz.

Step 2. Add $16.6\log_{10}(f/16)$ to the NEXT loss measurements (where f is frequency in MHz) to normalize the NEXT loss as a function of frequency.

Step 3. Determine the minimum value of the normalized NEXT loss across the frequency range over all pair combinations. The minimum value is the AdjustedNEXTLoss.

The NIR shall be greater than 19.4 dB.

32.7.2.4 Delay

Since 100BASE-T2 sends information over two duplex channels in parallel, the propagation delay of each channel and the difference in delay are specified to comply with network round-trip delay of the two channels and ensure proper decoding by receivers, respectively.

32.7.2.4.1 Maximum link delay

The propagation delay of a link segment shall not exceed 5.7 ns/m at all frequencies between 2 and 25 MHz.

32.7.2.4.2 Difference in link delays

The difference in propagation delay, or skew, under all conditions, between the two duplex channels of a link segment shall not exceed 90 ns at all frequencies between 2 and 25 MHz. It is a further functional requirement that, once installed, the skew between the duplex links due to environmental conditions shall not vary more than ± 20 ns, within the above requirement.

32.7.3 Noise

The noise level on the link segments shall be such that the cabling noise requirements which follow are met. The noise environment consists generally of a main contributor, self-induced and alien near-end crosstalk noise, and a lessor contributor, far-end crosstalk noise.

The noise environment for 100BASE-T2 can consist of the following elements:

a) Echo from the local transmitter on the same pair (duplex channel). Echo is caused by the hybrid used to achieve simultaneous bidirectional transmission of data in the T2 system and by impedance mismatches in the link segment. It is practically impossible to achieve robust performance without using echo cancellation to reduce this noise to a small residual. Echo cancellation is possible since the symbols transmitted from the disturbing local transmitter are available to the cancellation processor.

b) Near-end crosstalk (NEXT) noise from the local transmitter on the other pair (duplex channel) of the link segment. This is often referred to as self NEXT noise since the source is from the same link segment. NEXT noise cancellation is typically used to reduce this noise to a small residual. NEXT noise cancellation is possible since the symbols transmitted from the disturbing local transmitter are available to the cancellation processor.

c) Far-end crosstalk (FEXT) noise from the remote transmitters on the other pair (duplex channel) of the link segment. This is often referred to as self FEXT noise since the source is from the same link segment. Self FEXT noise can not be cancelled in the same way as echo and self NEXT noise since

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the symbols from the remote transmitter are not immediately available; however, in the link configurations used for 100BASE-T2, self FEXT noise is much smaller than self NEXT noise and can generally be neglected.[18]

d) Noise from non-idealities in the duplex channels, transmitters and receivers; for example, DAC/ADC non-linearity, electrical noise (shot and thermal) and non-linear channel characteristics.

e) Noise from sources outside the cabling which couple into the link segment via electric and magnetic fields.

f) Noise from services in adjacent wire pairs in the same cable sheath. These services generate near- and far-end crosstalk and are often referred to as alien NEXT noise and alien FEXT noise since the sources are not from the link segment of the disturbed duplex channel. Since the transmitted symbols from an alien NEXT noise source are not available to the PHY of the disturbed duplex channel, it is not possible to cancel the alien NEXT noise as can be done for self NEXT noise. If the alien NEXT noise is from a 100BASE-T2 transceiver, a technique termed cyclostationary interference suppression can be used to suppress the alien NEXT noise. It will be practically impossible achieve reliable operation in the presence of alien NEXT noise meeting the limits of the specifications in subclause 32.6 without using some form of cyclostationary interference suppression. 10BASE-T can not be suppressed and therefore an additional constraint has been placed on the link (see subclause 32.7.2.3.5) to ensure adequate signal to noise levels for reliable performance. Digital phone services compliant with the ITU-T Recommendation I.430 and ANSI T1.605 and T1.601 also can not be suppressed but produce substantially smaller crosstalk than 10BASE-T and thus do not require any additional constraints on the link.

100BASE-T2 supports three types of service in adjacent pairs of the same cable: 100BASE-T2, 10BASE-T, and digital phone service compliant with the ISDN-BR U and S/T interfaces. Analog phone service is not supported since the noise generated during off-hook transitions and ringing source from older PBX equipment can cause bit errors to occur.

NOTE—Due to the use of noise cancellation, cyclostationary interference suppression and the use of adaptive equalization, there is no meaningful way to add up the noises at the input to the receiver into an overall noise level and simulation of a design is required to determine the contribution of each source to the final error at the symbol decision point.

32.7.3.1 Near-end crosstalk noise

The MDNEXT (Multiple-Disturber Near-End Crosstalk) noise on a duplex channel from an alien connection depends on the signal spectrum on the alien channels and the crosstalk between the alien channels and the disturbed channel.

The MDNEXT noise on each duplex link of a link segment shall not exceed 182 mVp.

This specification is compatible with the following assumptions:

a) Two disturbing alien pairs with a NEXT loss greater than 22.0 dB at 16 MHz
b) All disturbers combined on a power sum basis

The MDNEXT noise is the noise measured at the output of a filter connected to the output of the near end of a disturbed link segment using maximum level 100BASE-T2 transmitters attached to the near end of an alien disturbing link segment. Each continuous transmit signal is generated by a transceiver in idle mode meeting the data scrambling and encoding rules in 32.3, e.g., a transmitter in transmit test mode 3.

[18]Additionally, FEXT noise may be suppressed to some degree via cyclostationary interference suppression; however, in the presence of alien NEXT noise, the equalizer will be primarily suppressing the alien NEXT noise.

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32.7.3.2 Far-end crosstalk noise

The MDFEXT (Multiple-Disturber Far-End Crosstalk) noise on a duplex channel depends on the signal spectrum on the disturbing channels and the various crosstalk losses between those channels and the disturbed channel.

The MDFEXT noise on a link segment shall not exceed 54.4 mVp.

This specification is compatible with the following assumptions:

a) One disturbing pair with ELFEXT (Equal Level Far-End Crosstalk) loss greater than 20.9 dB at 16 MHz
b) Two additional disturbers with ELFEXT (Equal Level Far-End Crosstalk) loss greater than 27.0 dB at 16 MHz
c) All disturbers combined on a power sum basis

The MDFEXT noise is the noise measured at the output of a filter connected to the output of the far end of a disturbed link segment using maximum level 100BASE-T2 transmitters attached to the near end of the other duplex channel of the link segment and both duplex channels of an alien disturbing link segment. Each continuous transmit signal is generated by a transceiver in idle mode meeting the data scrambling and encoding rules in 32.3, e.g., a transmitter in transmit test mode 3.

The filter is a 5th order Butterworth filter with a 3 dB cutoff at 23 MHz.

32.7.3.3 External coupled noise

Noise coupled from external sources, measured at the output of a filter connected to the output of the near end of a disturbed link segment shall not exceed 25 mV peak.[19]

The filter is a 5th order Butterworth filter with a 3 dB cutoff at 23 MHz.

32.7.4 Installation practice

32.7.4.1 Connector installation practices

The amount of untwisting in a pair as a result of termination to connecting hardware should be no greater than 25 mm (1.0 in.) for Category 3 cabling. This is the same value recommended in ISO/IEC 11801 for Category 4 connectors.

32.7.4.2 Restrictions on use of Category 3 cabling with more than four pairs

Jumper cabling, or horizontal runs, made from more than four pairs of Category 3 cabling shall not be used.

32.7.4.3 Restrictions on use of Category 5 cabling with up to 25 pairs

Cables made from up to 25 pairs of Category 5 cable are allowed. Such cables, if used, shall be limited in length to no more than 90 m total. The services in the cable shall be limited to any combination 100BASE-T2, 10BASE-T and digital phone services compliant with the ITU-T Recommendation I.430 and ANSI T1.605 and T1.601 interfaces up to a total of 12 services in the cable.

[19]This assumes the link has worst-case attenuation and alien NEXT and that the noise has the worst possible properties. In the absence of alien NEXT the tolerance to external noise sources is substantially increased. Tolerance to stationary noise such as continuous wave interference from AM radio can be substantially higher since the equalizer can notch out frequencies with poor signal to noise ratios. Tolerance to isolated impulse noise events is also typically much higher and dependent on the shape of the impulse.

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32.8 MDI specification

This subclause defines the MDI. The link topology requires a crossover function between PMAs. Implementation and location of this crossover are also defined in this subclause.

32.8.1 MDI connectors

Eight-pin connectors meeting the requirements of section 3 and Figures 1–4 of IEC 60603-7, Detail Specification for Connectors, 8-Way shall be used as the mechanical interface to the balanced cabling. The plug connector shall be used on the balanced cabling and the jack on the PHY. These connectors are depicted (for informational use only) in Figures 32–25 and 32–26. Table 32–14 shows the assignment of PMA signals to connector contacts for PHYs.

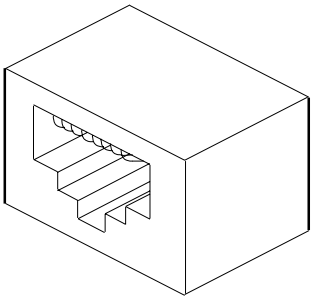


Figure 32–25—MDI connector

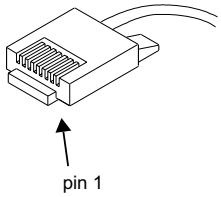


Figure 32–26—Balanced cabling connector

Table 32–14—Assignment of PMA signals to MDI pin-outs

Contact	PHY without internal crossover (100BASE-T2 operation)	PHY with internal crossover (Auto-Negotiation operation)	MDI labeling requirement
1	BI_DA+	BI_DB+	BI_DA+
2	BI_DA-	BI_DB-	BI_DA-
3	BI_DB+	BI_DA+	BI_DB+
4	Not used	Not used	
5	Not used	Not used	
6	BI_DB-	BI_DA-	BI_DB-
7	Not used	Not used	
8	Not used	Not used	

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32.8.2 Crossover function

Although the crossover function is not required for successful operation of 100BASE-T2, it is a functional requirement that a crossover function be implemented in every link segment to support the operation of Auto-Negotiation. The crossover function connects the transmitters of one PHY to the receivers of the PHY at the other end of the link segment. Crossover functions may be implemented internally to a PHY or elsewhere in the link segment. For a PHY that does not implement the crossover function, the MDI labels in the last column of Table 32–14 refer to its own internal circuits (second column). For PHYs that do implement the internal crossover, the MDI labels in the last column of Table 32–14 refer to the internal circuits of the remote PHY of the link segment. Additionally, the MDI connector for a PHY that implements the crossover function shall be marked with the graphical symbol X. The crossover function specified here is compatible with the crossover function specified in 14.5.2 for pairs TD and RD.

When a link segment connects a DTE to a repeater, it is recommended the crossover be implemented in the PHY local to the repeater. If both PHYs of a link segment contain internal crossover functions, an additional external crossover is necessary. It is recommended that the crossover be visible to an installer from one of the PHYs. When both PHYs contain internal crossovers, it is further recommended in networks in which the topology identifies either a central backbone segment or a central repeater that the PHY furthest from the central element be assigned the external crossover to maintain consistency.

Implicit implementation of the crossover function within a twisted-pair cable, or at a wiring panel, while not expressly forbidden, is beyond the scope of this standard.

32.9 System considerations

The repeater unit specified in Clause 27 forms the central unit for interconnecting 100BASE-T2 twisted-pair links in networks of more than two nodes. It also provides the means for connecting 100BASE-T2 balanced cabling links to other 100 Mb/s baseband segments. The proper operation of a CSMA/CD network requires that network size be limited to control round-trip propagation delay as specified in Clause 29.

When operated in Full Duplex mode where CSMA/CD requirements do not apply, 100BASE-T2 balanced cabling links are limited to 100 m as per ISO/IEC 11801.

32.10 Environmental specifications

32.10.1 General safety

All equipment meeting this standard shall conform to IEC 60950.

32.10.2 Network safety

This clause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cabling systems described in this clause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits
b) Static charge buildup on LAN cabling and components
c) High-energy transients coupled onto the LAN cabling system
d) Voltage potential differences between safety grounds to which various LAN components are connected

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Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network.

32.10.2.1 Installation

It is a mandatory functional requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

32.10.2.2 Grounding

Any safety grounding path for an externally connected PHY shall be provided through the circuit ground of the MII connection.

WARNING

It is assumed that the equipment to which the PHY is attached is properly grounded, and not left floating nor serviced by a "doubly insulated, ac power distribution system." The use of floating or insulated equipment, and the consequent implications for safety, are beyond the scope of this standard.

32.10.2.3 Installation and maintenance guidelines

It is a mandatory functional requirement that, during installation and maintenance of the cabling plant, care be taken to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

32.10.2.4 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 100BASE-T2 equipment. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply.

Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400 Ω source impedance.

Ringing voltage is a composite signal consisting of an AC component and a DC component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 Ω source resistance. The DC component is 56 Vdc with 300–600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 100BASE-T2 equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE—Wiring errors may impose telephony voltages differentially across 100BASE-T2 transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, receivers will generally appear to the telephone system as off-hook telephones. Therefore, full-ring voltages will be applied for only short periods. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to the low resistance of the transformer coil.

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32.10.3 Environment

32.10.3.1 Electromagnetic emission

The twisted-pair link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

32.10.3.2 Temperature and humidity

The twisted-pair link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

32.10.4 Cabling specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801.

32.11 PHY labeling

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Data rate capability in Mb/s
b) Power level in terms of maximum current drain (for external PHYs)
c) Port type (i.e., 100BASE-T2)
d) Any applicable safety warnings

See also 32.8.2.

32.12 Delay constraints

Proper operation of a CSMA/CD LAN, operating in half duplex mode, demands that there be an upper bound on the propagation delays through the network. This implies that MAC, PHY and repeater implementors must conform to certain delay minima and maxima, and that network planners and administrators conform to constraints regarding the cabling topology and concatenation of devices. MAC constraints are contained in Clause 21. Topological constraints are contained in Clause 29. In the full duplex mode of operation, DTEs are not required to conform to the constraints specified in this clause.

The reference point for all MDI measurements is the peak point of the mid-cell transition corresponding to the reference code-bit, as measured at the MDI. Although 100BASE-T2 output is scrambled, it is assumed that these measurements are made via apparatuses that appropriately account for this.

32.12.1 PHY delay constraints (exposed MII)

Every 100BASE-T2 PHY with an exposed MII shall comply with the bit delay constraints specified in Table 32–15. These figures apply for all 100BASE-T2 PMDs.

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Table 32–15—MDI to MII delay constraints (exposed MII)

Sublayer Measurement Points	Event	Min (bits)	Max (bits)	Input Timing Reference	Output Timing Reference
MII ⇔ MDI	TX_EN Sampled to MDI Output	7	9	TX_CLK rising	1st symbol of SSD
	MDI input to CRS assert		25	1st symbol of SSD	
	MDI input to CRS de-assert		29	1st ONE	
	MDI input to COL assert		25	1st symbol of SSD	
	MDI input to COL de-assert		29	1st symbol of SSD	
	TX_EN sampled to CRS assert	0	4	TX_CLK rising	
	TX_EN sampled to CRS de-assert	0	16	TX_CLK rising	

32.12.2 DTE delay constraints (unexposed MII)

Every 100BASE-T2 DTE with no exposed MII shall comply with the bit delay constraints specified in Table 32–16. These figures apply for all 100BASE-T2 PMDs.

Table 32–16—DTE delay constraints (unexposed MII)

Sublayer Measurement Points	Event	Min (bits)	Max (bits)	Input Timing Reference	Output Timing Reference
MAC ⇔ MDI	MAC transmit start to MDI output		13		1st symbol of SSD
	MDI input to MDI output (worst-case non-deferred transmit)		50	1st symbol of SSD	1st symbol of SSD
	MDI input to collision detect		33	1st symbol of SSD	
	MDI input to MDI output = Jam (worst-case collision response)		50	1st symbol of SSD	1st symbol of SSD

32.13 Protocol Implementation Conformance Statement (PICS) proforma for Clause 32, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T2[20]

The supplier of a protocol implementation that is claimed to conform to Clause 32, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T2, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

Instructions for interpreting and filling out the PICS proforma may be found in Clause 21.

[20] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may futher publish the completed PICS.

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32.13.1 Identification

32.13.1.1 Implementation identification

Supplier	
Contact point for queries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1— Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

32.13.1.2 Protocol summary

Identification of protocol specification	IEEE Std 802.3-2002, Clause 32, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T2
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exceptions items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

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32.13.2 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*MII	Exposed MII interface	32.1.3.2	O	Yes [ ] No [ ]	Devices supporting this option must also support the PCS option.
PC	PHY Control functions	32.2	M	Yes [ ]	Required for proper operation of the PHY.
*PCS	PCS functions	32.3	O	Yes [ ] No [ ]	Required for integration with DTE or MII.
*PMA	Exposed PMA service interface	32.4.2	O	Yes [ ] No [ ]	Required for integration into symbol level repeater core.
NWY	Support for Auto-Negotiation (Clause 28)	32.1.3.4	M	Yes [ ]	Required
*INS	Installation/cabling	32.7.4	O	Yes [ ] No [ ]	Items marked with INS include installation practices and cabling specifications not applicable to a PHY manufacturer.

32.13.3 Compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
CCO1	Compatibility at the MDI	32.1.3.1	M	Yes [ ]	
CCO2	Auto-Negotiation required	32.1.3.4	M	Yes [ ]	
CCO3	State diagrams prevail	32.1.4	M	Yes [ ]	In discrepancy between text and state diagram.

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32.13.4 PHY control function

Item	Feature	Subclause	Status	Support	Value/Comment
PC01	PHY Control shall	32.2.1	M	Yes [ ]	Comply with the state diagram descriptions given in Figure 32–5.
PC02	PHY Control shall	32.2.2.1.2	M	Yes [ ]	Generate PHYC_CONFIG.indicate messages synchronously with every MII TX_CLK cycle.
PC03	Upon receipt of the PHYC_CONFIG primitive, PCS Transmit and PMA Clock Recovery shall	32.2.2.1.3	M	Yes [ ]	Perform their functions in master or slave configuration according to the value of the parameter config.
PC04	PHY Control shall	32.2.2.2.2	M	Yes [ ]	Generate PHYC_LOCRXSTATUS.indicate messages synchronously with every MII TX_CLK cycle.
PC05	Upon reception of the PHYC_LOCRXSTATUS.indicate primitive, PCS Transmit shall	32.2.2.2.3	M	Yes [ ]	Perform its function according to the value assumed by the parameter loc_cvr_status.
PC06	PHY Control shall	32.2.2.3.2	M	Yes [ ]	Generate PHYC_TXMODE.indicate messages synchronously with every MII TX_CLK cycle.
PC07	Upon receipt of the PHYC_TXMODE.indicate primitive, the PCS shall	32.2.2.3.3	M	Yes [ ]	Perform its Transmit function as described in 32.3.1.2.
PC8	The PCS shall	32.2.2.3.2	M	Yes [ ]	Generate PHYC_RXSTATUS.request messages synchronously with signals received at the MDI.
PC9	The PCS shall	32.2.2.4.2	M	Yes [ ]	Generate PHYC_REMRXSTATUS.request messages synchronously with signals received at the MDI.
PC10	PCS Transmit shall	32.2.3	M	Yes [ ]	Send quinary symbols according to the value assumed by tx_mode.
PC11	When tx_mode assumes the value of SEND_N	32.2.3	M	Yes [ ]	Transmission of sequences of quinary symbols representing an MII data stream, the idle mode, or control sequences shall take place.
PC12	When tx_mode assumes the value of SEND_I	32.2.3	M	Yes [ ]	Transmission of sequences of quinary symbols representing the idle mode shall take place.

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32.13.5 Physical Coding Sublayer (PCS) or Physical Medium Attachment (PMA) sublayer

32.13.5.1 PCS transmit functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCT01	The PCS shall	32.3.5.1	M	Yes [ ]	Implement the Transmit process as depicted in Figure 32–12 including compliance with the associated state variables specified in 32.3.4.
PCT02	PCS Transmit function shall	32.3.1.2	M	Yes [ ]	Conform to the PCS Transmit state diagram in Figure 32–12.
PCT03	If the parameter config provided to the PCS by the PHY Control function via the PHYC_CONFIG.indicate message assumes the value MASTER, PCS Transmit shall	32.3.1.2.1	M	Yes [ ]	Employ the transmitter side-stream scrambler generator polynomial specified for use with MASTER in 32.3.1.2.1.
PCT04	If the parameter config provided to the PCS by the PHY Control function via the PHYC_CONFIG.indicate message assumes the value SLAVE, PCS Transmit shall	32.3.1.2.1	M	Yes [ ]	Employ the transmitter side-stream scrambler generator polynomial specified for use with SLAVE in 32.3.1.2.1.
PCT05	Transmission of quinary symbol pairs over wire pairs	32.3.1.2	M	Yes [ ]	Symbols A_n and B_n are transmitted over BI_DA and BI_DB respectively.

32.13.5.2 PCS receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCR01	The PCS shall	32.3.5.2	M	Yes [ ]	Implement the Receive process as depicted in Figure 32–13 including compliance with the associated state variables as specified in 32.3.4.
PCR02	PCS Receive function shall	32.3.1.3	M	Yes [ ]	Conform to the PCS Receive state diagram shown in Figure 32–13.
PCR03	For side-stream descrambling, the MASTER PHY shall employ	32.3.1.3.1	M	Yes [ ]	The receiver scramber generator polynomial specified for MASTER operation in 32.3.1.3.1.
PCR04	For side-stream descrambling, the SLAVE PHY shall employ	32.3.1.3.1	M	Yes [ ]	The receiver scrambler generator polynomial specified for SLAVE operation in 32.3.1.3.1.

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32.13.5.3 Other PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCO1	The PCS Reset function shall	32.3.1.1	M	Yes [ ]	Be executed any time “power on,” receipt of a request for reset from the management entity, or receipt of a request for reset from the PHY Control occur.
PCO2	THE PCS shall	32.3.1.4	M	Yes [ ]	Implement the PCS Carrier Sense function shown in Figure 32–14.
PCO3	PCS Carrier Sense function shall	32.3.5.3	M	Yes [ ]	Comply with the PCS Carrier Sense state diagram shown in Figure 32–14 including compliance with the associated state variables specified in 32.3.4.
PCO4	MII COL signal shall be asserted while	32.3.1.5	M	Yes [ ]	A PCS collision is being detected.
PCO5	The MII signal COL shall remain de-asserted.	32.3.1.5	M	Yes [ ]	A PCS collision is not being detected.
PCO6	No spurious PCS management entity signals shall be emitted onto the MDI while the PHY is held in power down mode as defined in 22.2.4.1.5, independently of the value of TX_EN, or when released from power down mode, or when power is first applied to the PHY.	32.3.2.2	M	Yes [ ]	
PCO7	Frames passed from the PCS to the PMA sublayer shall	32.3.3	M	Yes [ ]	Have the structure shown in Figure 32–11.
PCO8	TX_CLK shall be generated	32.3.4.2	M	Yes [ ]	Synchronously with symb_timer with tolerance as specified in 32.6.1.2.6.

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32.13.5.4 PMA functions

Item	Feature	Subclause	Status	Support	Value/Comment
PMF1	PMA Reset function shall be executed	32.4.1.1.1	M	Yes [ ]	At power on and upon receipt of a reset request from the management entity.
PMF2	PMA transmit shall continuously transmit	32.3.1.2	M	Yes [ ]	Onto the MDI pulses modulated by the quinary symbols given by tx_symb_vector[BI_DA] and tx_symb_vector[BI_DB] respectively.
PMF3	The two transmitters shall be driven by the same transmit clock.	32.4.1.1.2	M	Yes [ ]	
PMF4	PMA Transmit function will follow	32.4.1.1.2	M	Yes [ ]	The mathematical description given in 32.4.1.2.1.
PMF5	PMA Transmit shall comply with	32.4.1.1.2	M	Yes [ ]	The electrical specifications given in 32.6.
PMF6	PMA Receive function shall	32.4.1.1.3	M	Yes [ ]	Translate the signals received on pairs BI_DA and BI_DB into the PMA_UNITDATA.indicate parameter rx_symb_vector with a symbol error rate of less than one part in 10^{10}.
PMF7	The Link Monitor function shall	32.4.1.1.4	M	Yes [ ]	Comply with the state diagram shown in Figure 32–17.
PMF8	Clock Recovery function shall provide	32.4.1.1.5	M	Yes [ ]	A clock suitable for synchronous signal sampling on each line so that the symbol-error rate indicated in 32.4.1.1.3 is achieved.
PMF9	The waveform obtained at the MDI shall comply with	32.4.1.2.1	M	Yes [ ]	The electrical specifications given in 32.6.
PMF10	The two signals received on pair BI_DA and BI_DB shall be processed within the PMA Receive function to yield	32.4.1.2.2	M	Yes [ ]	The quinary received symbols rx_symb_vector[BI_DA] and rx_symb_vector[BI_DB].

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32.13.5.5 PMA service interface

Item	Feature	Subclause	Status	Support	Value/Comment
PMS1	Continuous generation of PMA_TYPE	32.4.1.2.2	M	Yes [ ]	
PMS2	Generation of PMA_UNITDATA.indicate (SYMB_PAIR) messages	32.4.2.3.2	M	Yes [ ]	Synchronous with data received at the MDI.
PMS3	The PMA shall generate	32.4.2.5.2	M	Yes [ ]	PMA_LINK.indicate to indicate the value of link_status.
PMS4	Effect of receipt of PMA_LINK.request messages	32.4.2.4.3	M	Yes [ ]	While link_control=SCAN_FOR_CARRIER or link_control=DISABLE, the PMA shall report link_status=fail; while link_control=ENABLE, PHY determines operations to be performed by the PHY.

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32.13.5.6 Management functions

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	A 100BASE-T2 PHY shall	32.5	M	Yes [ ]	Use register addresses 9 and 10 for its control and status functions.
MF2	Register 9 shall	32.5.3.1	M	Yes [ ]	Provide values as specified in Table 32–4.
MF3	A PHY with 100BASE-T2 capability shall	32.5.3.1.1	M	Yes [ ]	Be placed in transmitter test mode 1 when bit 9.15 is set to logic zero and bit 9.14 is set to logic one.
MF4	A PHY with 100BASE-T2 capability shall	32.5.3.1.1	M	Yes [ ]	Be placed in transmitter test mode 2 when bit 9.15 is set to logic one and bit 9.14 is set to logic zero.
MF5	A PHY with 100BASE-T2 capability shall	32.5.3.1.1	M	Yes [ ]	Be placed in transmitter test mode 3 when bit 9.15 is set to logic one and bit 9.14 is set to logic one.
MF6	A PHY with 100BASE-T2 capability shall	32.5.3.1.2	M	Yes [ ]	Be placed in receiver test mode when bit 9.13 is set to logic one.
MF7	MASTER-SLAVE configuration negotiation will determine PHY configuration if	32.5.3.1.3	M	Yes [ ]	Bit 9.12 is set to logic zero.
MF8	Manual MASTER-SLAVE configuration will be set manually using bit 9.11 to set the value if	32.5.3.1.3	M	Yes [ ]	Bit 9.12 is set to logic one.
MF9	Bit 9.11 shall be used to report the results of manual MASTER-SLAVE configuration.	32.5.3.1.4	M	Yes [ ]	
MF10	Bit 9.10 shall	32.5.3.1.5	M	Yes [ ]	Be set to logic zero if the PHY is a DTE device and be set to logic one if the PHY is a repeater device port.
MF11	Bits 9.9:0 shall	32.5.3.1.6	M	Yes [ ]	Be set to logic zero.
MF12	Bits 9.9:0 shall be ignored when read	32.5.3.1.6	M	Yes [ ]	
MF13	A PHY shall return a value of zero for bits 9.9:0.	32.5.3.1.6	M	Yes [ ]	
MF14	Register 10 shall	32.5.3.1.2	M	Yes [ ]	Be used as shown in Table 32–5.
MF15	Bits 10.11:8 shall	32.5.3.2.5	M	Yes [ ]	Be set to logic zeros by default.
MF16	The MASTER-SLAVE Manual Configuration Fault bit shall be implemented	32.5.3.2.1	M	Yes [ ]	With a latching function, such that the occurrence of a MASTER-SLAVE Manual Configuration Fault will cause the MASTER-SLAVE Manual Configuration Fault bit to be set and remain set until cleared.
MF17	The MASTER-SLAVE Manual Configuration Fault bit shall be cleared	32.5.3.2.1	M	Yes [ ]	Each time register 10 is read by the management interface.

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32.13.5.6 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF18	The MASTER-SLAVE Management Configuration Fault bit shall also be cleared by	32.5.3.2.1	M	Yes [ ]	A 100BASE-T2 PMA reset.
MF19	Bits 10:11:8 shall	32.5.3.2.5	M	Yes [ ]	Be ignored when read.
MF20	A PHY shall return a value of zero for bits10.11:8.	32.5.3.2.5	M	Yes [ ]	

32.13.5.7 100BASE-T2 specific Auto-Negotiation requirements

Item	Feature	Subclause	Status	Support	Value/Comment
AN1	Base Page will be followed with	32.5.4.2	M	Yes [ ]	A Next Page with a message code containing the 100BASE-T2 Technology Ability Message Code (7).
AN2	Message Next Page shall be followed with	32.5.4.2	M	Yes [ ]	Unformatted Message Next Page containing the 100BASE-T2 Technology Ability Fields as described in Table 32–6.
AN3	MASTER-SLAVE relationship shall be determined by	32.5.4.3	M	Yes [ ]	Using Table 32–7with the 100BASE-T2 Technology Ability Next Page bit values specified in Table 32–6.
AN4	A seed counter shall be provided to	32.5.4.3	M	Yes [ ]	Track the generation of seeds.
AN5	At start-up, the seed counter shall be set to	32.5.4.3	M	Yes [ ]	Zero.
AN6	The seed counter shall be incremented	32.5.4.3	M	Yes [ ]	Every time a new random seed is sent.
AN7	Maximum seed attempts before declaring a MASTER_SLAVE configuration Resolution Fault	32.5.4.3	M	Yes [ ]	Seven.
AN8	During MASTER_SLAVE configuration, the device with the lower seed value shall	32.5.4.3	M	Yes [ ]	Become the SLAVE.
AN9	Both PHYs set in manual mode to be either MASTER or SLAVE shall be treated as	32.5.4.3	M	Yes [ ]	MASTER-SLAVE resolution fault (Failure) condition
AN10	MASTER-SLAVE resolution fault (failure) condition shall result in	32.5.4.3	M	Yes [ ]	MASTER-SLAVE Configuration Resolution Fault bit (10.15) to be set
AN11	MASTER-SLAVE Configuration resolution fault condition shall be treated as	32.5.4.3	M	Yes [ ]	MASTER-SLAVE Configuration Resolution complete

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32.13.5.8 PMA electrical specifications

Item	Feature	Subclause	Status	Support	Value/Comment
PME1	The value of all components in test circuits shall be accurate to within	32.6	M	Yes [ ]	±1%.
PME2	The PHY shall provide electrical isolation between	32.6.1.1	M	Yes [ ]	The DTE or repeater circuits including frame ground, and all MDI leads.
PME3	PHY-provided electrical separation shall withstand at least one of three electrical strength tests	32.6.1.1	M	Yes [ ]	a) 1500 V rms at 50–60Hz for 60 s, applied as specified in section 5.3.2 of IEC 60950. b) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC 60950. c) a sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs. (1.2 μs virtual front time, 50 μs virtual time or half value), as defined in IEC 60950.
PME4	There shall be no insulation breakdown as defined in Section 5.3.2 of IEC 60950, during the test.	32.6.1.1	M	Yes [ ]	
PME5	The resistance after the test shall be at least	32.6.1.1	M	Yes [ ]	2 MΩ, measured at 500 Vdc.
PME6	The PMA shall provide the Transmit function specified in 32.4.1.1.2 in accordance with the electrical specifications of this clause.	32.6.1.2	M	Yes [ ]	
PME7	Where a load is not specified, the transmitter shall meet all the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output.	32.6.1.2	M	Yes [ ]	
PME8	The tolerance on the poles of the test filters used in 32.6 shall be	32.6.1.2	M	Yes [ ]	±1%
PME9	A special transmit test mode shall be required to allow for testing of the transmitter waveform	32.6.1.2.1	M	Yes [ ]	
PME10	A test mode for measuring transmitter output jitter is required.	32.6.1.2.1	M	Yes [ ]	
PME11	For a PHY with a MII interface, the transmit test mode shall be enabled by	32.6.1.2.1	M	Yes [ ]	Setting bit 9.15 and 9.14 (MASTER-SLAVE Control register) of the MII management register set as shown in Table 32–6.

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME12	These test modes shall only change the data symbols provided to the transmitter circuitry and may not alter the electrical characteristics of the transmitter	32.6.1.2.1	M	Yes [ ]	
PME13	When transmit test mode 1 is enabled, the PHY shall transmit	32.6.1.2.1	M	Yes [ ]	The sequence of data symbols specified in 32.6.1.2.1 continuously from both transmitters.
PME14	When in test mode 1, the transmitter shall time the transmitted symbols	32.6.1.2.1	M	Yes [ ]	From a 25.000 MHz ± 0.01% clock.
PME15	When test mode 2 is enabled, the PHY shall transmit	32.6.1.2.1	M	Yes [ ]	The data symbol sequence {+2,–2} repeatedly on both channels.
PME16	When in test mode 2, the transmitter shall time the transmitted symbols	32.6.1.2.1	M	Yes [ ]	From a 25.000 MHz ± 0.01% clock.
PME17	A PHY without a MII shall provide a means to enter this test mode.	32.6.1.2.1	M	Yes [ ]	
PME18	The vendor shall	32.6.1.2.1	M	Yes [ ]	Provide a means to enable these modes for testing.
PME19	When in transmit test mode 1 and observing the differential signal output at the MDI, terminated in 100 Ω, preprocessed by the high pass filter defined below, for either pair, with no intervening cable, the absolute value of the peak of the waveform at points A and B as defined in Figure 32–18 shall fall within	32.6.1.2.2	M	Yes [ ]	The range of 1.71V to 1.91 V (1.81 V ± 0.5 dB).
PME20	The absolute value of the peak of the waveforms at points A and B shall	32.6.1.2.2	M	Yes [ ]	Differ by less than 2%.
PME21	The absolute value of the peak of the waveform at points C and D as defined in Figure 32–18 shall differ	32.6.1.2.2	M	Yes [ ]	From 0.5 times the average of the absolute values of the peaks of the waveform at points A and B by less than 2%.
PME22	The preprocessing filter shall have	32.6.1.2.2	M	Yes [ ]	The transfer function specified in 32.6.1.2.2.
PME23	When in transmit test mode 1 and observing the differential transmitted output at the MDI, for either pair, with no intervening cabling, the peak value of the waveform at point F as defined in Figure 32–17 shall be	32.6.1.2.3	M	Yes [ ]	Greater than 70.5% of the peak value of the waveform at point E. A preprocessing filter is not used for this measurement.

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME24	The transmitter differential output voltage shall be measured at the output of the high pass filter defined in 32.6.1.2.2 with no intervening cables.	32.6.1.2.4	M	Yes [ ]	
PME25	The voltage waveforms at points A, B, C and D as defined in Figure 32–17,when normalized by their respective peak values, shall	32.6.1.2.4	M	Yes [ ]	Lie within the time domain template defined in Figure 32–18 and the piecewise linear interpolation between the points in Table 32–6
PME26	The magnitude in dB of the Fourier transform of the waveforms at points A, B, C and D shall	32.6.1.2.4	M	Yes [ ]	Lie within the transmit frequency domain template defined in Figure 32–18 and the piecewise linear interpolation between the points in Table 32–7.
PME27	The time span of the waveforms so processed shall be	32.6.1.2.4	M	Yes [ ]	–80 ns to +2000 ns with the 0 ns point of the waveform aligned as for the time domain mask shown in Figure 32–18 and the magnitude of the Fourier transform should be normalized so that the maximum value is at 0 dB.
PME28	When in transmit mode 2, the peak-to-peak jitter of the zero crossings of the differential signal output at the MDI shall	32.6.1.2.5	M	Yes [ ]	Be less than 0.5 ns.
PME29	The quinary symbol transmission rate on each pair shall be	32.6.1.2.6	M	Yes [ ]	25.000 MHz ± 0.01%.
PME30	The PMA shall provide	32.6.1.3	M	Yes [ ]	The Receive function specified in 32.4.1.3 in accordance with the electrical specifications of this clause.
PME31	The patch cabling and interconnecting hardware used in test configurations shall	32.6.1.3	M	Yes [ ]	Meet or exceed ISO/IEC 11801 Category 3 specifications.
PME32	The combined responses of the test fixture TX block and NEXT or cabling channel blocks shall be	32.6.1.3.1	M	Yes [ ]	Those defined in Table 32–8.
PME33	The output impedance of the test channel shall be	32.6.1.3	M	Yes [ ]	Consistent with 32.6.1.4.1.
PME34	The idle symbol generator outputs shall be	32.6.1.3	M	Yes [ ]	Conformant with the idle signaling specified in 32.3 with loc_rcvr_status=OK.
PME35	The clock source shall	32.6.1.3	M	Yes [ ]	Result in a quinary symbol transmission rate conformant with 32.6.1.2.6.
PME36	The jitter on the clock source shall be	32.6.1.3	M	Yes [ ]	Less than 0.2 ns.

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME37	The test channel implementation shall ensure that the ratio of the squared error between the implemented NEXT channel symbol responses and the specified NEXT channel symbol responses to the energy in the specified NEXT channel symbol responses shall be	32.6.1.3	M	Yes [ ]	Less than 5%.
PME38	The test channel implementation shall ensure that the energy of the implemented NEXT channel impulse responses and the energy of the specified NEXT channel impulse responses shall	32.6.1.3	M	Yes [ ]	Differ by less than ±0.25 dB.
PME39	A special receiver test mode shall be required to allow for receiver alien NEXT tolerance and jitter testing.	32.6.1.3.2	M	Yes [ ]	
PME40	For a PHY with a MII interface, this mode shall be enabled by	32.6.1.3.2	M	Yes [ ]	Setting bit 9.13 (MASTER-SLAVE Control Register) of the MII management register set to a 1.
PME41	A PHY without an MII shall provide	32.6.1.3.2	M	Yes [ ]	A means to enable this test mode.
PME42	This mode shall not be overridden except by	32.6.1.3.2	M	Yes [ ]	Clearing bit 9.13 or resetting the PHY.
PME43	When the receive test mode is enabled, the receiver shall	32.6.1.3.2	M	Yes [ ]	Configure itself in SLAVE mode, continually attempt to bring its receiver up until successful receiver operation is achieved and transmit symbols in idle mode.
PME44	For a PHY with a MII interface, when the receiver is properly detecting the received data, it shall set	32.6.1.3.2	M	Yes [ ]	Bit 10.13 of the MII management register set to 1 and reset the error count in bit 10.0–10.7 (MSB) to zero.
PME45	The error count shall be incremented	32.6.1.3.2	M	Yes [ ]	For every symbol error detected in the received idle sequence.
PME46	Upon loss of proper data reception, the receiver shall	32.6.1.3.2	M	Yes [ ]	Clear bit 10.13.
PME47	A PHY without an MII shall provide	32.6.1.3.2	M	Yes [ ]	A means to provide the functions defined in PME43 through PME46.
PME48	The vendor shall provide a means to enable this mode for conformance testing.	32.6.1.3.2	M	Yes [ ]	

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME49	Differential signals received on the receive inputs that were transmitted within the constraints of 32.6.1.2, and have then passed through a link as defined in 32.7, shall be translated into	32.6.1.3.3	M	Yes [ ]	One of the PMA_UNITDATA.indicate messages with an bit error rate less than 10^{-10} and sent to the PCS after link bring-up.
PME50	Performance shall be tested	32.6.1.3.3	M	Yes [ ]	In at least two configurations: using a 100 m link segment conformant to 32.7 and with a link segment less than one meter in length between transmitter and receiver.
PME51	Differential signals received from the test channel defined in 32.6.1.3.1 shall be detected	32.6.1.3.4	M	Yes [ ]	With a symbol error rate less than 10^{-10} when the PHY is in receiver test mode for the combinations of channel and worst-case alien NEXT responses specified in 32.6.1.2.
PME52	In the test configuration described in 32.6.1.3.1 and for all combinations of worst-case channel and alien NEXT coefficients tabulated in 32.6.1.3.4, the peak-to-peak value of the RX_CLK zero-crossing jitter shall be less than	32.6.1.3.5	M	Yes [ ]	1.3 ns after the receiver is properly receiving the data and has set bit 9.13 of the MII management register set to 1.
PME53	When the jitter waveform is filtered by a high pass filter having the transfer function specified in 32.6.1.3.4, the peak-to-peak value of the jitter waveform shall be less than	32.6.1.3.5	M	Yes [ ]	0.8 ns.
PME54	The RX_CLK of the MII shall be made available for the receiver jitter test specified in 32.6.1.3.5.	32.6.1.3.5	M	Yes [ ]	
PME55	A PHY without an MII shall provide an equivalent to the MII RX-CLK clock for the receiver jitter test specified in 32.6.1.3.5.	32.6.1.3.5	M	Yes [ ]	
PME56	While receiving packets from a compliant 100BASE-T2 transmitter connected to all MDI pins, a receiver shall send the	32.6.1.3.6	M	Yes [ ]	Proper PMA_UNITDATA.indicate messages to the PCS for any differential input signal E_s that results in a signal E_{dif} that meets 32.6.1.3.3 even in the presence of common mode voltages E_{cm} (applied as shown in Figure 32–21).

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME57	E_{cm} shall be	32.6.1.3.6	M	Yes [ ]	A 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%–80%), connected to each of the pairs BI_DA+, BI_DA-, BI_DB+ and BI_DB-.
PME58	The receive feature shall properly receive	32.6.1.3.7	M	Yes [ ]	Incoming data with a 5-level symbol rate within the range 25.000 MHz ± 0.01%.
PME59	The differential impedance as measured at the MDI for each transmit/receive channel shall be such that	32.6.1.4.1	M	Yes [ ]	Any reflection due to differential signals incident upon the MDI from a balanced cabling having an impedance of 100 Ω is at least 17 dB below the incident signal, over the frequency range of 2.0 MHz to 25.0 MHz and at least $12.9–20\log_{10}(f/10)$ dB over the frequency range 6.5 MHz to 25 MHz (f in MHz).
PME60	This return loss shall be maintained	32.6.1.4.1	M	Yes [ ]	At all times when the PHY is transmitting data.
PME61	The common-mode to differential-mode impedance balance of each transmit output shall exceed	32.6.1.4.2	M	Yes [ ]	The value specified by the equations specified in 32.6.1.2.6 over the range 2.0–25.0 MHz.
PME62	Transmitters and receivers shall tolerate	32.6.1.4.4	M	Yes [ ]	The application of short circuits between the leads of any receive input for an indefinite period of time without damage.
PME63	Transmitters and receivers shall resume	32.6.1.4.4	M	Yes [ ]	Normal operation after such faults are removed.
PME64	The magnitude of the current through the short circuit specified in PME62 shall not exceed	32.6.1.4.4	M	Yes [ ]	300 mA.
PME65	Transmitters shall withstand without damage	32.6.1.4.4	M	Yes [ ]	A 1000 V common mode impulse of either polarity (E_{cm} as indicated in Figure 32–24).
PME66	The shape of the impulse shall be	32.6.1.4.4	M	Yes [ ]	0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.
PME67	After 100 ms following PowerOn, the current drawn by the PHY shall not exceed	32.6.2	M	Yes [ ]	1.0 A when powered through the MII.

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME68	The PHY shall	32.6.2	M	Yes [ ]	Be capable of operating from all voltage sources allowed by Clause 22, including those current limited to1.0 A, as supplied by the DTE or repeater through the resistance of all permissible MII cabling.
PME69	The PHY shall not introduce	32.6.2	M	Yes [ ]	Extraneous signals on the MII control circuits during normal power-up and power-down.

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32.13.5.9 Characteristics of the link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LKS1	100BASE-T2 links shall use	32.7.1	M	Yes [ ]	2 pair of balanced cabling, CAT 3 or better, with a nominal impedance of 100 Ω.
LKS2	Unless otherwise specified, link segment testing shall be conducted using	32.7.2	M	Yes [ ]	Source and load impedances of 100 Ω.
LKS3	The tolerance on the poles of the test filter used in this section shall be	32.7.2	M	Yes [ ]	± 1%.
LKS4	The insertion loss of a link segment shall be no more than	32.7.2.1	M	Yes [ ]	14.6 dB at all frequencies between 2 and 16 MHz.
LKS5	The insertion loss specification shall be met when	32.7.2.1	M	Yes [ ]	The link segment is terminated in source and load impedances that satisfy 32.6.1.4.1.
LKS6	The magnitude of the differential characteristic impedance of a 3 m segment of balanced cabling pair used in a link shall be	32.7.2.2	M	Yes [ ]	Between 85 and 115 Ω for all frequencies between 2 and 16 MHz.
LKS7	The NEXT loss between each of the two duplex channels of a link segment shall be	32.7.2.3.1	M	Yes [ ]	At least $19.3–16.6\log_{10}(f/16)$ (where f is the frequency in MHz) over the frequency range 2.0 to 16 MHz.
LKS8	The NEXT loss between link segments of two different connections shall be	32.7.2.3.1	M	Yes [ ]	At least $22.0 –16.6\log_{10}(f/16)$ (where f is the frequency in MHz) over the frequency range 2.0 to 16 MHz.
LKS9	The MDNEXT loss between a link segment and the two alien data carrying channels shall be	32.7.2.3.2	M	Yes [ ]	At least $19.0–16.6\log_{10}(f/16)$ dB (where f is the frequency in MHz) over the frequency range 2.0 to 16 MHz.
LKS10	To limit the FEXT noise from an adjacent channel, the ELFEXT loss between channels shall be	32.7.2.3.3	M	Yes [ ]	Greater than $20.9–20\log_{10}(f/16)$ dB as defined in 32.7.2.3.3
LKS11	The MDELFEXT loss between a duplex channel and the other data carrying duplex channels shall be	32.7.2.3.4	M	Yes [ ]	Greater than $19.9–20\log10(f/16)$ (where f is the frequency in MHz) over the frequency range 2.0 to 16 MHz.
LKS12	The maximum spacing of the frequency in the sample shall be	32.7.2.3.5	M	Yes [ ]	250 kHz.

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32.13.5.9 Characteristics of the link segment *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
LKS13	When 10BASE-T service is used in adjacent pairs, the channel shall provide	32.7.2.3.5	M	Yes [ ]	A NEXT loss to Insertion loss Ratio (NIR) greater than 19.4 dB.
LKS14	The propagation delay of a link segment shall not exceed	32.7.2.4.1	M	Yes [ ]	5.7 ns/meter at all frequencies between 2.0–25.0 MHz.
LKS15	The difference in propagation delay, or skew, under all conditions, between the fastest and the slowest channel in a link segment shall not exceed	32.7.2.4.2	M	Yes [ ]	50 ns at all frequencies between 2.0–25.0 MHz.
LKS16	Once installed, the skew between pairs due to environmental conditions shall not vary	32.7.2.4.2	M	Yes [ ]	More than ± 10 ns.
LKS17	The noise level on the link segments shall be such that	32.7.3	M	Yes [ ]	The objective error rate is met.
LKS18	The MDNEXT noise on a link segment shall not exceed	32.7.3.1	M	Yes [ ]	182 mVp.
LKS19	The MDFEXT noise on a link segment shall not exceed	32.7.3.2	M	Yes [ ]	54.4 mVp.
LKS20	Cables made from up to 25 pairs of Category 5 cabling, if used, shall be limited in length to no more than	32.7.4.3	O	Yes [ ]	90 m total.
LKS21	The services in 25 pair Category 5 cabling shall be limited to any combination of 100BASE-T2, 10BASE-T and digital phone service compliant with the ISDN-BR U and S/T interfaces up to a total of 12 services in the cable.	32.7.4.3	M	Yes [ ]	
LKS22	Jumper cabling, or horizontal runs, made from more than 4 pairs of Category 3 cabling shall not be used	32.7.4.3	M	Yes [ ]	

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32.13.5.10 MDI requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MDI1	MDI connector	32.8.1	M	Yes [ ]	8-Way connector as per IEC 60603-7.
MDI2	Connector used on cabling	32.8.1	M	Yes [ ]	Plug.
MDI3	Connector used on PHY	32.8.1	M	Yes [ ]	Jack (as opposed to plug).
MDI4	AN MDI connector for the PHY that implements the crossover function shall be marked	32.8.2	M	Yes [ ]	With the graphical symbol “X”.

32.13.5.11 General safety and environmental requirements

Item	Feature	Subclause	Status	Support	Value/Comment
ENV1	Conformance to safety specifications	32.10.1	M	Yes [ ]	IEC 60950.
ENV2	Installation practice	32.10.2.1	M	Yes [ ]	Sound practice, as defined by applicable local codes.
ENV3	Any safety grounding path for an externally connected PHY shall be provided through the circuit ground of the MII connection.	32.10.2.2	M	Yes [ ]	
ENV4	Care taken during installation to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.	32.10.2.3	M	Yes [ ]	
ENV5	Application of voltages specified in 32.10.2.4 does not result in any safety hazard.	32.10.2.4	M	Yes [ ]	
ENV6	Conformance with local and national codes for the limitation of electromagnetic interference.	32.10.3.1	M	Yes [ ]	
ENV7	All equipment subject to this clause shall conform to	32.10.4	M	Yes [ ]	The requirements of 14.7 and the applicable sections of ISO/IEC 11801.

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32.13.5.12 Timing requirements exposed MII

Item	Feature	Subclause	Status	Support	Value/Comment
TME1	TX-EN (sampled to MDI output)	32.12.1	M	Yes [ ]	7–9 bit times
TME2	MDI input to CRS assert	32.12.1	M	Yes [ ]	25 bit times
TME3	MDI input to CRS de-assert	32.12.1	M	Yes [ ]	29 bit times
TME4	MDI input to COL assert	32.12.1	M	Yes [ ]	25 bit times
TME5	MDI input to COL de-assert	32.12.1	M	Yes [ ]	29 bit times
TME6	TX_EN sampled to CRS assert	32.12.1	M	Yes [ ]	0–4 bit times
TME7	TX_EN sampled to CRS de-assert	32.12.1	M	Yes [ ]	0–16 bit times

32.13.5.13 Timing requirements unexposed MII

Item	Feature	Subclause	Status	Support	Value/Comment
TMU1	MAC transmit start to MDI output	32.12.2	M	Yes [ ]	13 bit times
TMU2	MDI input to MDI output (worst-case non-deferred transmit)	32.12.2	M	Yes [ ]	50 bit times
TMU3	MDI input to collision detect	32.12.2	M	Yes [ ]	33 bit times
TMU4	MDI input to MDI output = Jam (worst-case collision response)	32.12.2	M	Yes [ ]	50 bit times

32.13.5.14 Timing requirements: carrier assertion/deassertion constraint

Item	Feature	Subclause	Status	Support	Value/Comment
TMC1	Each DTE shall satisfy the relationship	36.5.3	M	Yes [ ]	(MAX MDI to MAC Carrier De-assert Detect)–(MIN MDI to MAC Carrier Assert Detect).

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NOTE—The remaining annexes in the standard are numbered in correspondence to their associated clauses; e.g., Annexes 22A, 22B, and 22C correspond to Clause 22.

Annex 22A

(informative)

MII output delay, setup, and hold time budget

22A.1 System model

The discussion of signal timing characteristics that follows will refer to the system model depicted in Figure 22A–1, Figure 22A–2, and Figure 22A–3. This system model can be applied to each of the three application environments defined in 22.2.1.

Figure 22A–1 depicts a simple system model in which the MII is used to interconnect two integrated circuits on the same circuit assembly. In this model the Reconciliation sublayer comprises one integrated circuit, and the PHY comprises the other. A Reconciliation sublayer or a PHY may actually be composed of several separate integrated circuits. The system model in Figure 22A–1 includes two unidirectional signal transmission paths, one from the Reconciliation sublayer to the PHY and one from the PHY to the Reconciliation sublayer. The path from the Reconciliation sublayer to the PHY is separated into two sections, labeled A1 and B1. The path from the PHY to the Reconciliation sublayer is separated into two sections, labeled C1 and D1.

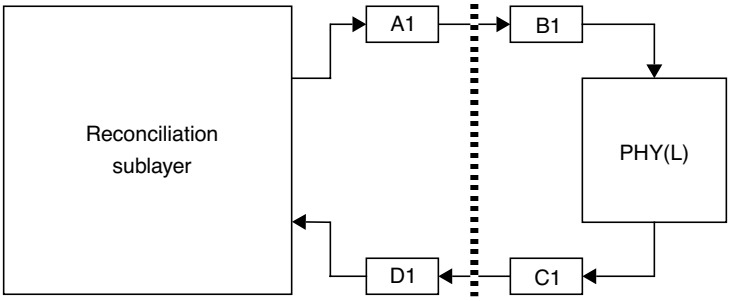


Figure 22A–1—Model for integrated circuit to integrated circuit connection

Figure 22A–2 depicts a system model for the case where the MII is used to interconnect two circuit assemblies. The circuit assemblies may be physically connected in a motherboard/daughterboard arrangement, or they may be physically connected with the cable defined in 22.4.5 and the line interface connector defined in 22.6. The system model in Figure 22A–2 includes two unidirectional signal transmission paths, one from the Reconciliation sublayer to the PHY and one from the PHY to the Reconciliation sublayer. The path from the Reconciliation sublayer to the PHY is separated into two sections, labeled A2 and B2. The path from the PHY to the Reconciliation sublayer is separated into two sections, labeled C2 and D2.

Figure 22A–3 depicts a system model in which the MII is used to interconnect both integrated circuits and circuit assemblies. This system model allows for separate signal transmission paths to exist between the Reconciliation sublayer and a local PHY(L), and between the Reconciliation sublayer and a remote PHY(R). The unidirectional paths between the Reconciliation sublayer and the PHY(L) are composed of sections A1, B1, C1, and D1. The unidirectional paths between the Reconciliation sublayer and the remote PHY(R) are composed of sections A2, B2, C2, and D2.

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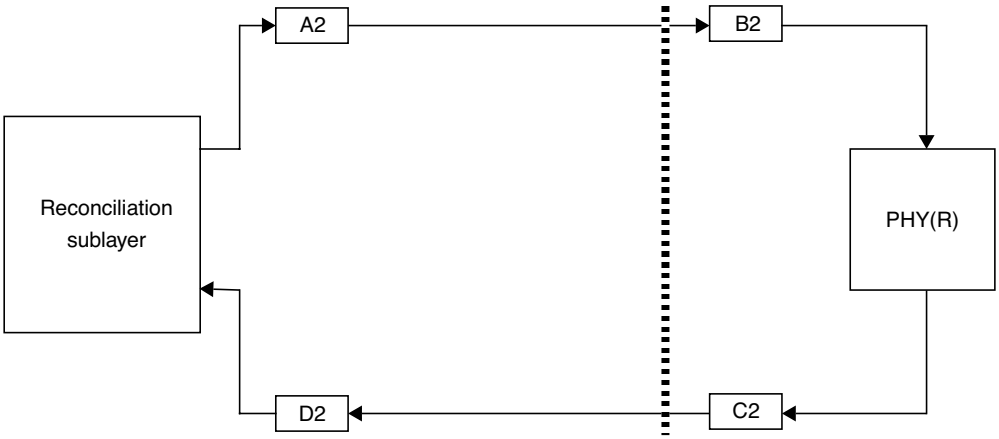


Figure 22A–2—Model for circuit assembly to circuit assembly connection

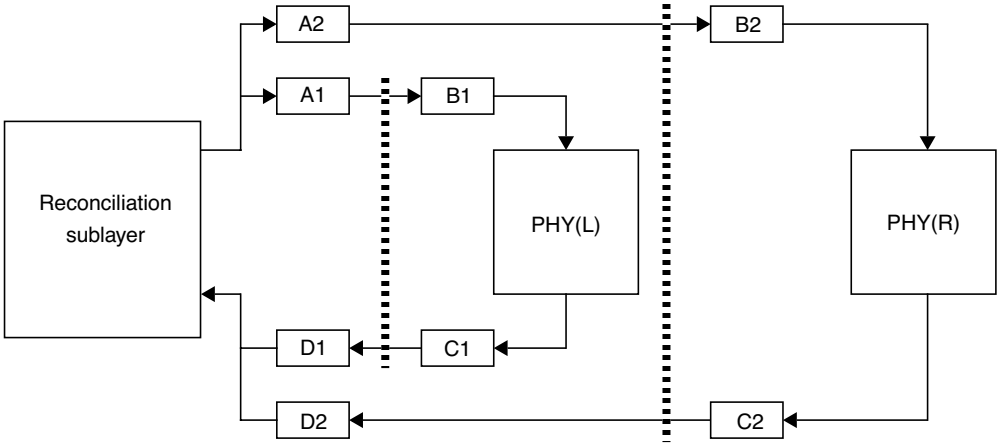


Figure 22A–3—Combined model

Each of these system models assumes a set of common timing and electrical characteristics that shall be met at the input and output ports of the Reconciliation sublayer and PHY devices. The characteristics of the signal transmission paths are identified for each of the sections A1, B1, C1, D1, A2, B2, C2, and D2.

22A.2 Signal transmission path characteristics

The signal transmission path characteristics are specified for each of the path sections defined in 22A.1. The characteristics for these sections are specified so as to allow sections A1, B1, C1, and D1 to be implemented in the form of printed circuit board traces, while sections A2, B2, C2, and D2 may be implemented with a combination of printed circuit board traces and wire conductors in a cable assembly.

The signal transmission path characteristics are stated in terms of their maximum delay and their characteristic impedance. These values are summarized in Table 22A–1.

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Table 22A–1—Signal transmission path characteristics

Section	Maximum delay (ns)	Impedance (Ω)
A1, D1	5	68 ± 15%
B1, C1	2.5	68 ± 15%
A2, D2	5	68 ± 10%
B2, C2	2.5	68 ± 10%

The driver characteristics specified in 22.4.3, the receiver characteristics specified in 22.4.4, and the signal transmission path characteristics specified in Table 22A–1 can be applied to the system models shown in Figure 22A–1 or Figure 22A–2. The combination of loads presented in Figure 22A–3 cannot be adequately driven by an output buffer that meets the driver characteristics specified in 22.4.3 while being sampled by an input buffer that meets the receiver characteristics specified in 22.4.4.

To address the system model depicted in Figure 22A–3, it is permissible to incorporate an additional stage of buffering into path sections A1, A2, D1, and D2, provided that the resulting maximum delay characteristic for those path sections does not exceed the value stated in Table 22A–1. The delay characteristic for transmission path sections A2 and D2 includes an allowance for the delay that results from the presence of a lumped capacitive load at the end of the path. For a transmission path section with a characteristic impedance Z_o, with a lumped capacitive load C_L, this delay is nominally Z_oC_L. In the case of a maximum transmission path section impedance of 78 Ω with a lumped load of 8 pF, the nominal delay is 0.6 ns. Thus the allowable delay for a buffer inserted into transmission path section A2 or D2 is 4.4 ns.

22A.3 Budget calculation

A recommended timing budget is shown in Table 22A–2. This budget assumes that the combined system model shown in Figure 22A–3 represents a worst case.

Table 22A–2—Round-trip delay budget

Description	Incremental delay (ns)	Cumulative delay (ns)
TX_CLK output at PHY(R)	0.0	0.0
Transmission path section C2	2.5	2.5
Transmission path section D2	5.0	7.5
clock to output in Reconciliation sublayer	15.0	22.5
Transmission path section A2	5.0	27.5
Transmission path section B2	2.5	30.0
Setup time at PHY(R)	10.0	40.0

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Annex 22B

(informative)

MII driver ac characteristics

22B.1 Implications of CMOS ASIC processes

For MII drivers that drive rail to rail, such as those commonly used in CMOS ASICs (complimentary metal oxide semiconductor application-specific integrated circuits), the ac characteristic performance requirements of 22.4.3.2 can be met if the V_{oh} vs. I_{oh} and V_{ol} vs. I_{ol} dc characteristics of the driver stay within the unshaded areas of Figure 22B–1.

The variation in output resistance of a field effect transistor (FET) due to variations in supply voltage, temperature, and process may require that a resistance be placed in series with the output of the FETs to meet this specification. The series resistance can be part of the driver circuit, or external to the driver. If the series resistance is not part of the driver circuit, the driver vendor shall specify the value of series resistance required to meet the specification. A series resistor used to meet this specification is conceptually part of the driver regardless of whether it is physically internal or external to the driver.

The propagation delay of the path between the driver and an external series resistor used to meet the specification shall not exceed 10% of the 10–90% rise/fall time of the driver.

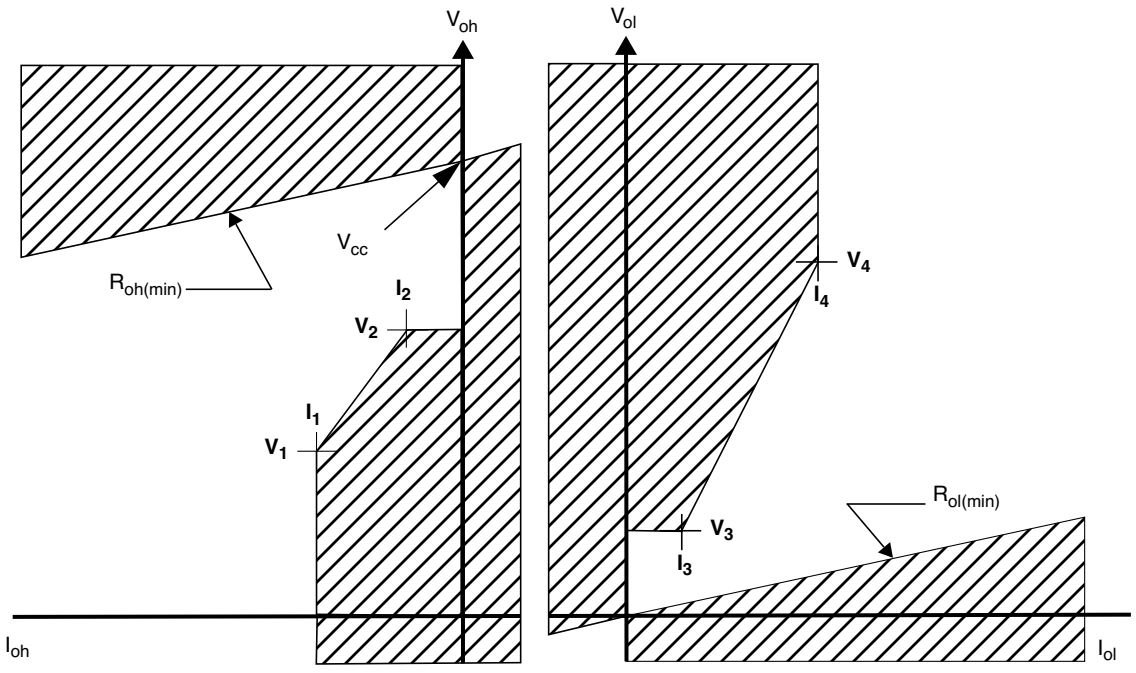


Figure 22B–1—Driver output V–I curve

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22B.2 $R_{o(min)}$ and V, I values for operation from 5 V ± 10% supply

Referring to Figure 22B–1, $R_{oh(min)}$ and $R_{ol(min)}$ both equal 40 Ω, and the values for the V-I points on the curve are given in Table 22B–1 for MII drivers that drive rail to rail from a +5 V ± 10% power supply.

Table 22B–1—Values for driver output V-I curve (5 V supply)

V–I point	I (mA)	V (V)
I_1, V_1	–20	1.10
I_2, V_2	–4	2.4
I_3, V_3	4	0.40
I_4, V_4	43	3.05

22B.3 $R_{o(min)}$ and V, I values for operation from 3.3 ± 0.3 V supply

Referring to Figure 22B–1, $R_{oh(min)}$ and $R_{ol(min)}$ both equal 33 Ω, and the values for the V–I points on the curve are given in Table 22B–2 for MII drivers that drive rail to rail from a +3.3 ± 0.3 V power supply.

Table 22B–2—Values for driver output V-I curve (3.3 V supply)

V-I point	I (mA)	V (V)
I_1,V_1	–20	1.10
I_2,V_2	–4	2.4
I_3,V_3	4	0.40
I_4,V_4	26	2.10

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Annex 22C

(informative)

Measurement techniques for MII signal timing characteristics

22C.1 Measuring timing characteristics of source terminated signals

The measurement of timing relationships between MII signals at the MII connector is complicated by the use of driver output impedance to control transmission line reflections on point-to-point transmission paths passing through the connector. The voltage waveforms on point-to-point transmission paths can be different at the MII connector and at the end of the paths. A clean transition (or step) from one logic state to the other at the end of a point to point path can appear as two half-steps at the MII connector.

To eliminate ambiguity as to where on a two half-step state transition to measure timing, all timing measurements on point-to-point transmission paths will be at the end of the path. In some cases, an end of path must be artificially created.

22C.2 Measuring timing characteristics of transmit signals at the MII

The timing of TX_EN, TX_ER, and TXD<3:0> relative to TX_CLK at the MII connector is measured as follows.

Use the time base for TX_CLK as a timing reference. Break the TX_CLK path at the MII connector, forcing the TX_CLK point-to-point transmission path to end at the connector. Measure when the rising edge of TX_CLK passes through $V_{ih(min)}$ at the MII connector. Call this time T_{clk}. Reconnect the TX_CLK path at the MII connector and break the paths of TX_EN, TX_ER, and TXD<3:0> at the MII connector, forcing the paths to end at the connector. Measure when TX_EN, TX_ER, and TXD<3:0> exit the switching region at the MII connector. Call these times T_{en}, T_{er}, and $T_{<3:0>}$, respectively.

The timing relationships at the MII connector for TX_EN, TX_ER, and TXD<3:0> relative to TX_CLK are met if $(T_{en} - T_{clk})$, $(T_{er} - T_{clk})$, $(T_3 - T_{clk})$, $(T_2 - T_{clk})$, $(T_1 - T_{clk})$, and $(T_0 - T_{clk})$, respectively, meet the timing relationships specified in 22.3.1.

22C.3 Measuring timing characteristics of receive signals at the MII

The timing of RX_DV, RX_ER, and RXD<3:0> relative to RX_CLK at the MII connector is measured as follows.

Break the paths of RX_CLK, RX_DV, RX_ER, and RXD<3:0> at the MII connector, forcing the paths to end at the connector. Measure when RX_DV, RX_ER, and RXD<3:0> exit the switching region at the MII connector relative to when the rising edge of RX_CLK passes through $V_{il(max)}$. Also measure when RX_DV, RX_ER, and RXD<3:0> reenter the switching region relative to when the rising edge of RX_CLK passes through $V_{ih(min)}$.

The timing relationships at the MII connector for RX_DV, RX_ER, and RXD<3:0> relative to RX_CLK are met if the times measured in the previous step meet the timing relationships specified in 22.3.2.

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22C.4 Measuring timing characteristics of MDIO

The MDIO and MDC signal timing characteristics cannot be measured using the techniques defined for the transmit and receive signals since MDIO and MDC may connect a single station management entity to multiple PHY devices. The MDIO and MDC timing characteristics are measured with a PHY connected to the MII connector. The signal timing characteristics for MDC and MDIO must be met over the range of conditions which occur when from one to 32 PHYs are connected to an STA. When 32 PHYs are connected to an STA, the total capacitance can be as large as 390 pF on MDC, and as large as 470 pF on MDIO.

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Annex 23A

(normative)

6T code words

The *leftmost* ternary symbol of each 6T Code group shown in Table 23A–1 (broken into 23A–1a and 23A–1b for pagination) shall be transmitted *first*. The *leftmost* nibble of each data octet is the *most significant*.

Table 23A–1a—100BASE-T4 8B6T code table

Data octet	6T code group	Data octet	6T code group	Data octet	6T code group	Data octet	6T code group
00	+ - 0 0 + -	20	0 0 - + + -	40	+ 0 + 0 0 -	60	0 - 0 + + 0
01	0 + - + - 0	21	- - + 0 0 +	41	+ + 0 0 - 0	61	0 0 - + 0 +
02	+ - 0 + - 0	22	+ + - 0 + -	42	+ 0 + 0 - 0	62	0 - 0 + 0 +
03	- 0 + + - 0	23	+ + - 0 - +	43	0 + + 0 - 0	63	- 0 0 + 0 +
04	- 0 + 0 + -	24	0 0 + 0 - +	44	0 + + 0 0 -	64	- 0 0 + + 0
05	0 + - - 0 +	25	0 0 + 0 + -	45	+ + 0 - 0 0	65	0 0 - 0 + +
06	+ - 0 - 0 +	26	0 0 - 0 0 +	46	+ 0 + - 0 0	66	0 - 0 0 + +
07	- 0 + - 0 +	27	- - + + + -	47	0 + + - 0 0	67	- 0 0 0 + +
08	- + 0 0 + -	28	- 0 - + + 0	48	0 0 0 + 0 0	68	- + - + + 0
09	0 - + + - 0	29	- - 0 + 0 +	49	0 0 0 - + +	69	- - + + 0 +
0A	- + 0 + - 0	2A	- 0 - + 0 +	4A	0 0 0 + - +	6A	- + - + 0 +
0B	+ 0 - + - 0	2B	0 - - + 0 +	4B	0 0 0 + + -	6B	+ - - + 0 +
0C	+ 0 - 0 + -	2C	0 - - + + 0	4C	0 0 0 - + 0	6C	+ - - + + 0
0D	0 - + - 0 +	2D	- - 0 0 + +	4D	0 0 0 - 0 +	6D	- - + 0 + +
0E	- + 0 - 0 +	2E	- 0 - 0 + +	4E	0 0 0 + - 0	6E	- + - 0 + +
0F	+ 0 - - 0 +	2F	0 - - 0 + +	4F	0 0 0 + 0 -	6F	+ - - 0 + +
10	+ 0 + - - 0	30	+ - 0 0 - +	50	+ 0 + - - +	70	- + + 0 0 0
11	+ + 0 - 0 -	31	0 + - - + 0	51	+ + 0 - + -	71	+ - + 0 0 0
12	+ 0 + - 0 -	32	+ - 0 - + 0	52	+ 0 + - + -	72	+ + - 0 0 0
13	0 + + - 0 -	33	- 0 + - + 0	53	0 + + - + -	73	0 0 + 0 0 0
14	0 + + - - 0	34	- 0 + 0 - +	54	0 + + - - +	74	- 0 + 0 0 0
15	+ + 0 0 - -	35	0 + - + 0 -	55	+ + 0 + - -	75	0 - + 0 0 0
16	+ 0 + 0 - -	36	+ - 0 + 0 -	56	+ 0 + + - -	76	+ 0 - 0 0 0
17	0 + + 0 - -	37	- 0 + + 0 -	57	0 + + + - -	77	0 + - 0 0 0
18	0 + - 0 + -	38	- + 0 0 - +	58	+ + + 0 - -	78	0 - - + + +
19	0 + - 0 - +	39	0 - + - + 0	59	+ + + - 0 -	79	- 0 - + + +
1A	0 + - + + -	3A	- + 0 - + 0	5A	+ + + - - 0	7A	- - 0 + + +
1B	0 + - 0 0 +	3B	+ 0 - - + 0	5B	+ + 0 - - 0	7B	- - 0 + + 0
1C	0 - + 0 0 +	3C	+ 0 - 0 - +	5C	+ + 0 - - +	7C	+ + - 0 0 -
1D	0 - + + + -	3D	0 - + + 0 -	5D	+ + 0 0 0 -	7D	0 0 + 0 0 -
1E	0 - + 0 - +	3E	- + 0 + 0 -	5E	- - + + + 0	7E	+ + - - - +
1F	0 - + 0 + -	3F	+ 0 - + 0 -	5F	0 0 - + + 0	7F	0 0 + - - +

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Table 23A–1b—100BASE-T4 8B6T code table

Data octet	6T code group	Data octet	6T code group	Data octet	6T code group	Data octet	6T code group
80	+ - + 0 0 -	A0	0 - 0 + + -	C0	+ - + 0 + -	E0	+ - 0 + + -
81	+ + - 0 - 0	A1	0 0 - + - +	C1	+ + - + - 0	E1	0 + - + - +
82	+ - + 0 - 0	A2	0 - 0 + - +	C2	+ - + + - 0	E2	+ - 0 + - +
83	- + + 0 - 0	A3	- 0 0 + - +	C3	- + + + - 0	E3	- 0 + + - +
84	- + + 0 0 -	A4	- 0 0 + + -	C4	- + + 0 + -	E4	- 0 + + + -
85	+ + - - 0 0	A5	0 0 - - + +	C5	+ + - - 0 +	E5	0 + - - + +
86	+ - + - 0 0	A6	0 - 0 - + +	C6	+ - + - 0 +	E6	+ - 0 - + +
87	- + + - 0 0	A7	- 0 0 - + +	C7	- + + - 0 +	E7	- 0 + - + +
88	0 + 0 0 0 -	A8	- + - + + -	C8	0 + 0 0 + -	E8	- + 0 + + -
89	0 0 + 0 - 0	A9	- - + + - +	C9	0 0 + + - 0	E9	0 - + + - +
8A	0 + 0 0 - 0	AA	- + - + - +	CA	0 + 0 + - 0	EA	- + 0 + - +
8B	+ 0 0 0 - 0	AB	+ - - + - +	CB	+ 0 0 + - 0	EB	+ 0 - + - +
8C	+ 0 0 0 0 -	AC	+ - - + + -	CC	+ 0 0 0 + -	EC	+ 0 - + + -
8D	0 0 + - 0 0	AD	- - + - + +	CD	0 0 + - 0 +	ED	0 - + - + +
8E	0 + 0 - 0 0	AE	- + - - + +	CE	0 + 0 - 0 +	EE	- + 0 - + +
8F	+ 0 0 - 0 0	AF	+ - - - + +	CF	+ 0 0 - 0 +	EF	+ 0 - - + +
90	+ - + - - +	B0	0 - 0 0 0 +	D0	+ - + 0 - +	F0	+ - 0 0 0 +
91	+ + - - + -	B1	0 0 - 0 + 0	D1	+ + - - + 0	F1	0 + - 0 + 0
92	+ - + - + -	B2	0 - 0 0 + 0	D2	+ - + - + 0	F2	+ - 0 0 + 0
93	- + + - + -	B3	- 0 0 0 + 0	D3	- + + - + 0	F3	- 0 + 0 + 0
94	- + + - - +	B4	- 0 0 0 0 +	D4	- + + 0 - +	F4	- 0 + 0 0 +
95	+ + - + - -	B5	0 0 - + 0 0	D5	+ + - + 0 -	F5	0 + - + 0 0
96	+ - + + - -	B6	0 - 0 + 0 0	D6	+ - + + 0 -	F6	+ - 0 + 0 0
97	- + + + - -	B7	- 0 0 + 0 0	D7	- + + + 0 -	F7	- 0 + + 0 0
98	0 + 0 - - +	B8	- + - 0 0 +	D8	0 + 0 0 - +	F8	- + 0 0 0 +
99	0 0 + - + -	B9	- - + 0 + 0	D9	0 0 + - + 0	F9	0 - + 0 + 0
9A	0 + 0 - + -	BA	- + - 0 + 0	DA	0 + 0 - + 0	FA	- + 0 0 + 0
9B	+ 0 0 - + -	BB	+ - - 0 + 0	DB	+ 0 0 - + 0	FB	+ 0 - 0 + 0
9C	+ 0 0 - - +	BC	+ - - 0 0 +	DC	+ 0 0 0 - +	FC	+ 0 - 0 0 +
9D	0 0 + + - -	BD	- - + + 0 0	DD	0 0 + + 0 -	FD	0 - + + 0 0
9E	0 + 0 + - -	BE	- + - + 0 0	DE	0 + 0 + 0 -	FE	- + 0 + 0 0
9F	+ 0 0 + - -	BF	+ - - + 0 0	DF	+ 0 0 + 0 -	FF	+ 0 - + 0 0

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Annex 23B

(informative)

Noise budget

Worst-case values for noise effects in the 100BASE-T4 system are as shown in Tables 23B–1 and 23B–2.

Table 23B–1—Carrier presence analysis

Received signal peak amplitude (min.)	792 mVp
NEXT noise	325 mVp

Table 23B–2—Far-end signal analysis

Received signal peak amplitude (min.)	796 mVp
Baseline wander	14 mVp
ISI	80 mVp
Reflections	60 mVp
FEXT noise	87 mVp

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Annex 23C

(informative)

Use of cabling systems with a nominal differential characteristic impedance of 120 Ω

The 100BASE-T4 standard specifies only the use of 100 Ω link segments for conformance. Since ISO/IEC 11801: 1995 also recognizes 120 Ω cabling, this informative annex specifies the conditions for using cabling systems with a nominal characteristic impedance of 120 Ω by 100BASE-T4 conformant stations.

The use of cables with a characteristic impedance outside the range specified in 23.6 will generally increase the mismatching effects in the link components, inducing additional noise in the received signals.

In particular, the use of a homogeneous link segment having a characteristic impedance of 120 Ω ±15 Ω over the frequency band 1 to 16 MHz may add up to 1.4% of additional noise to the signals at the input of the receivers (worst-case short-length link segment).

Therefore, in order to keep the overall noise (MDFEXT + reflections) at the same value as for a 100 Ω link segment when using a 120 Ω link segment, the minimum ELFEXT loss requirement for the cable must be increased by 2 dB (i.e., from 23 dB to 25 dB at 12.5 MHz, see 23.6.3.2). Accordingly, the MDFEXT noise requirement shall be decreased from 87 mV peak to 69 mV peak. In practice, this means that cables rated category 4 or higher, as specified in ISO/IEC 11801: 1995, are required when 120 Ω cables are used with 100BASE-T4 compliant PMDs.

NOTE 1—The use of 100 Ω cords at end points in conjunction with 120 Ω premises cabling may be tolerated provided that all the components of the link are of Category 5, as defined in ISO/IEC 11801: 1995.

NOTE 2—The use of 100 Ω cords at any intermediate cross-connect points on 120 Ω links as well as the use of 120 Ω cords in conjunction with 100 Ω premises cabling is not allowed since it would result in worst-case jitter greater than that allowed in this standard.

CAUTION—Users of this annex are further advised to check with the manufacturer of the particular 100BASE-T4 couplers they intend to use with a 120 Ω link to see whether those couplers can operate correctly on cables with Z_c as high as 120 Ω ± 15 Ω.

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Annex 27A

(normative)

Repeater delay consistency requirements

Proper operation of the network requires that repeaters do not cause the Inter-Packet Gap (IPG) to disappear by propagating the end of any carrier event to different output ports with greatly different delay times. Maximum port-to-port delays have been assigned as absolute delays to meet requirements for detection of collision within a slot time and limiting the length of collision fragments to less than minimum frame size. To avoid specification of minimum input-to-output propagation time as absolute values that reduce implementation flexibility, these delays are instead implied by imposing a triangular delay inequality relationship.

Consider three ports {A, B, C}. Using the notation SOP(xy) to mean the start-of-packet delay for an input at port x to resulting output on port y, repeaters shall achieve this relationship for all groups of three ports within a repeater set:

SOP(AC) < SOP(AB) + SOP(BC)

Following a frame transmitted by node A that propagates to nodes B and C, this constraint ensures that node B cannot complete an IPG timer and initiate a transmission that arrives at node C before node C has also advanced its own IPG timer sufficiently that a pending frame can contend for access to the network.

There is a second delay consistency requirement, one that relates to jam propagation by repeaters. Using a notation similar to that above, SOJ(xy) stands for the start-of-jam propagation delay from port x to port y and EOJ(xy) for the end-of-jam delay between same two ports.

To ensure proper detection of collisions and avoid generation of fragments that exceed minimum frame size, maximum values have been imposed on SOJ and EOJ delays through repeaters. No specific minima have been specified as all delays less than the maxima meet the collision detection and fragment length criteria. To prevent the jam pattern from shrinking excessively as it propagates through repeaters, repeaters shall meet this relationship between all pairs of ports:

EOJ(AB) >= SOJ(AB) – 4 bit times

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Annex 28A

(normative)

Selector Field definitions

The Selector Field, S[4:0] in the Link Code Word, shall be used to identify the type of message being sent by Auto-Negotiation. The following table identifies the types of messages that may be sent. As new messages are developed, this table will be updated accordingly.

The Selector Field uses a 5-bit binary encoding, which allows 32 messages to be defined. All unspecified combinations are reserved. Reserved combinations shall not be transmitted.

Table 28A–1—Selector Field value mappings

S4	S3	S2	S1	S0	Selector description
0	0	0	0	0	Reserved for future Auto-Negotiation development
0	0	0	0	1	IEEE Std 802.3
0	0	0	1	0	IEEE Std 802.9 ISLAN-16T
0	0	0	1	1	IEEE Std 802.5
1	1	1	1	1	Reserved for future Auto-Negotiation development[a]

[a]For up-to-date information on the allocation of Auto-Negotiation Selector fields see http://www.ieee802.org/3/selectors/selectors.html

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Annex 28B

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IEEE 802.3 Selector Base Page definition

This annex provides the Technology Ability Field bit assignments, Priority Resolution table, and Message Page transmission conventions relative to the IEEE 802.3 Selector Field value within the base page encoding.

As new IEEE 802.3 LAN technologies are developed, a reserved bit in the Technology Ability field may be assigned to each technology by the standards body.

The new technology will then be inserted into the Priority Resolution hierarchy and made a part of the Auto-Negotiation standard. The relative hierarchy of the existing technologies will not change, thus providing backward compatibility with existing Auto-Negotiation implementations.

It is important to note that the reserved bits are required to be transmitted as logic zeros. This guarantees that devices implemented using the current priority table will be forward compatible with future devices using an updated priority table.

28B.1 Selector field value

The value of the IEEE 802.3 Selector Field is S[4:0] = 00001.

28B.2 Technology Ability Field bit assignments

The Technology bit field consists of bits D5 through D12 (A0–A7, respectively) in the IEEE 802.3 Selector Base Page. Table 28B–1 summarizes the bit assignments.

Note that the order of the bits within the Technology Ability Field has no relationship to the relative priority of the technologies.

Setting Bit A5 or Bit A6 indicates that the DTE has implemented both the optional MAC control sublayer and the PAUSE function as specified in Clause 31 and Annex 31B. This capability is significant only when the link is configured for full duplex operation, regardless of data rate and medium. The encoding of Bits A5 and A6 is specified in Table 28B–2.

Table 28B–1—Technology Ability Field bit assignments

Bit	Technology	Minimum cabling requirement
A0	10BASE-T	Two-pair category 3
A1	10BASE-T full duplex	Two-pair category 3
A2	100BASE-TX	Two-pair category 5
A3	100BASE-TX full duplex	Two-pair category 5
A4	100BASE-T4	Four-pair category 3
A5	PAUSE operation for full duplex links	Not applicable
A6	Asymmetric PAUSE operation for full duplex Links	Not applicable
A7	Reserved for future technology	

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Table 28B–2—Pause encoding

PAUSE (A5)	ASM_DIR (A6)	Capability
0	0	No PAUSE
0	1	Asymmetric PAUSE toward link partner
1	0	Symmetric PAUSE
1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device

The PAUSE bit indicates that the device is capable of providing the symmetric PAUSE functions as defined in Annex 31B. The ASM_DIR bit indicates that asymmetric PAUSE is supported. The value of the PAUSE bit when the ASM_DIR bit is set indicates the direction the PAUSE frames are supported for flow across the link. Asymmetric PAUSE configuration results in independent enabling of the PAUSE receive and PAUSE transmit functions as defined by Annex 31B. See 28B.3 regarding PAUSE configuration resolution.

28B.3 Priority resolution

Since two devices may have multiple abilities in common, a prioritization scheme exists to ensure that the highest common denominator ability is chosen. The following list shall represent the relative priorities of the technologies supported by the IEEE 802.3 Selector Field value, where priorities are listed from highest to lowest.

a) 1000BASE-T full duplex
b) 1000BASE-T
c) 100BASE-T2 full duplex
d) 100BASE-TX full duplex
e) 100BASE-T2
f) 100BASE-T4
g) 100BASE-TX
h) 10BASE-T full duplex
i) 10BASE-T

The rationale for this hierarchy is straightforward. 10BASE-T is the lowest common denominator and therefore has the lowest priority. Full duplex solutions are always higher in priority than their half duplex counterparts. 1000BASE-T has a higher priority than 100 Mb/s technologies. 100BASE-T2 is ahead of 100BASE-TX and 100BASE-T4 because 100BASE-T2 runs across a broader spectrum of copper cabling and can support a wider base of configurations. 100BASE-T4 is ahead of 100BASE-TX because 100BASE-T4 runs across a broader spectrum of copper cabling. The relative order of the technologies specified herein shall not be changed. As each new technology is added, it shall be inserted into its appropriate place in the list, shifting technologies of lesser priority lower in priority. If a vendor-specific technology is implemented, the priority of all IEEE 802.3 standard technologies shall be maintained, with the vendor specific technology inserted at any appropriate priority location.

The use of the PAUSE operation for full duplex links (as indicated by bits A5 and A6) is orthogonal to the negotiated data rate, medium, or link technology. The setting of these bits indicates the availability of additional DTE capability when full duplex operation is in use. The PAUSE function shall be enabled according to Table 28B–3 only if the Highest Common Denominator is a full duplex technology. There is no priority resolution associated with the PAUSE operation.

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Table 28B–3—Pause resolution

Local device		Link partner		Local device resolution	Link partner resolution
PAUSE	**ASM_DIR**	**PAUSE**	**ASM_DIR**		
0	0	Don't care	Don't care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	0	Don't care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	1	Enable PAUSE transmit Disable PAUSE receive	Enable PAUSE receive Disable PAUSE transmit
1	0	0	Don't care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	Don't care	1	Don't care	Enable PAUSE Transmit and Receive	Enable PAUSE Transmit and Receive
1	1	0	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	1	0	1	Enable PAUSE receive Disable PAUSE transmit	Enable PAUSE transmit Disable PAUSE receive

28B.4 Message Page transmission convention

Each series of Unformatted Pages shall be preceded by a Message Page containing a Message Code that defines how the following Unformatted Pages will be used.

Next Page message codes should be allocated globally across Selector Field values so that meaningful communication is possible between technologies using different Selector Field values.

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Annex 28C

(normative)

Next Page Message Code Field definitions

The Message Code Field of a message page used in Next Page exchange shall be used to identify the meaning of a message. The following table identifies the types of messages that may be sent. As new messages are developed, this table will be updated accordingly.

The Message Code Field uses an 11-bit binary encoding that allows 2048 messages to be defined. All Message Codes not specified shall be reserved for IEEE use or allocation.

Table 28C–1—Message code field values

Message Code #	M 10	M 9	M 8	M 7	M 6	M 5	M 4	M 3	M 2	M 1	M 0	Message Code Description
0	0	0	0	0	0	0	0	0	0	0	0	Reserved for future Auto-Negotiation use
1	0	0	0	0	0	0	0	0	0	0	1	Null Message
2	0	0	0	0	0	0	0	0	0	1	0	One UP with Technology Ability Field follows
3	0	0	0	0	0	0	0	0	0	1	1	Two UPs with Technology Ability Field follow
4	0	0	0	0	0	0	0	0	1	0	0	One UP with Binary coded Remote fault follows
5	0	0	0	0	0	0	0	0	1	0	1	Organizationally Unique Identifier Tagged Message
6	0	0	0	0	0	0	0	0	1	1	0	PHY Identifier Tag Code
7	0	0	0	0	0	0	0	0	1	1	1	100BASE-T2 Technology Message Code. 100BASE-T2 Ability Page to follow using Unformatted Next Page
8	0	0	0	0	0	0	0	1	0	0	0	1000BASE-T Technology Message Code. Two 1000BASE-T Ability Pages to follow using Unformatted Next Pages.
9.....	0	0	0	0	0	0	0	1	0	0	1	Reserved for future Auto-Negotiation use
.....2047	1	1	1	1	1	1	1	1	1	1	1	Reserved for future Auto-Negotiation use

28C.1 Message code #0—Auto-Negotiation reserved code 1

This code is reserved for future Auto-Negotiation function enhancements. Devices shall not transmit this code.

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28C.2 Message code #1—Null Message code

The Null Message code shall be transmitted during Next Page exchange when the Local Device has no further messages to transmit and the Link Partner is still transmitting valid Next Pages. See 28.2.3.4 for more details.

28C.3 Message code #2—Technology Ability extension code 1

This Message Code is reserved for future expansion of the Technology Ability Field and indicates that a defined user code with a specific Technology Ability Field encoding follows.

28C.4 Message code #3—Technology Ability extension code 2

This Message Code is reserved for future expansion of the Technology Ability Field and indicates that two defined user codes with specific Technology Ability Field encodings follow.

28C.5 Message code #4—Remote fault number code

This Message Code shall be followed by a single user code whose encoding specifies the type of fault that has occurred. The following user codes are defined:

0: RF Test
    This code can be used to test Remote Fault operation.
1: Link Loss
2: Jabber
3: Parallel Detection Fault
    This code may be sent to identify when bit 6.4 is set.

28C.6 Message code #5—Organizationally Unique Identifier (OUI) tag code

The OUI Tagged Message shall consist of a single message code of 0000 0000 0101 followed by four user codes defined as follows. The first user code shall contain the most significant 11 bits of the OUI (bits 23:13) with the most significant bit in bit 10 of the user code. The second user code shall contain the next most significant 11 bits of the OUI (bits 12:2) with the most significant bit in bit 10 of the user code. The third user code shall contain the remaining least significant 2 bits of the OUI (bits 1:0) with the most significant bit in bit 10 of the user code. Bits 8:0 of the fourth user contain a user-defined user code value that is specific to the OUI transmitted. The fourth and final user code shall contain a user-defined user code value that is specific to the OUI transmitted.

28C.7 Message code #6—PHY identifier tag code

The PHY ID tag code message shall consist of a single message code of 0000 0000 0110 followed by four user codes defined as follows. The first user code shall contain the most significant 11 bits of the PHY ID (2.15:5) with the most significant bit in bit 10 of the user code. The second user code shall contain bits 2.4:0 to 3.15:10 of the PHY ID with the most significant bit in bit 10 of the user code. The third user code shall contain bits 3.9:0 of the PHY ID with the most significant bit in bit 10 of the user code. Bit 0 in the third user code shall contain a user-defined user code value that is specific to the PHY ID transmitted. The fourth and final user code shall contain a user-defined user code value that is specific to the PHY ID transmitted.

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28C.8 Message code #2047—Auto-Negotiation reserved code 2

This code is reserved for future Auto-Negotiation function enhancements. Devices shall not transmit this code.

28C.9 Message code #7—100BASE-T2 technology message code

Clause 32 (100BASE-T2) uses Next Page Message Code 7 to indicate that T2 implementations will follow the transmission of this page [the initial, Message (formatted) Next Page] with two unformatted Next Pages which contain information defined in 32.5.4.2.

28C.10 Message Code #8 - 1000BASE-T technology message code

Clause 40 (1000BASE-T) uses Next Page Message Code 8 to indicate that 1000BASE-T implementations will follow the transmission of this page [the initial, Message (formatted) Next Page] with two unformatted Next Pages that contain information defined in 40.5.1.2.

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Annex 28D

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Description of extensions to Clause 28 and associated annexes

28D.1 Introduction

This annex is to be used to document extensions and modifications to Clause 28 required by IEEE 802.3 clauses and other standards that use Auto-Negotiation and that were approved after June 1995. It provides a single location to define such extensions and modifications without changing the basic contents of Clause 28.

Subclause 28D.2 lists those clauses and standards that require extensions to Clause 28 and provides pointers to the subclauses where those extensions are listed.

28D.2 Extensions to Clause 28

28D.2.1 Extensions required for Clause 31 (full duplex)

Clause 31 (full duplex) requires the use of Auto-Negotiation. Extensions to Clause 28 and associated annexes required for the correct operation of full duplex are shown in 28D.3.

28D.2.2 Extensions required for Clause 32 (100BASE-T2)

Clause 32 (100BASE-T2) requires the use of Auto-Negotiation. Extensions to Clause 28 required for correct operation of 100BASE-T2 are shown in 28D.4.

28D.3 Extensions for Clause 31

Full duplex requires the use of bit A5 in the Technology Ability Field of the IEEE 802.3 Selector Base Page. (This bit is also defined as MII bit 4.10.) This bit was previously defined as “reserved for future technology.”

Bit	Technology	Minimum cabling requirement
A5	PAUSE operation for full duplex links	Not applicable

Bit A5 (PAUSE operation for full duplex links) signifies that the DTE has implemented both the optional MAC Control sublayer and the PAUSE function as specified in Clause 31 and Annex 31B. This capability is significant only when the link is configured for full duplex operation, regardless of data rate and medium.

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28D.4 Extensions for Clause 32 (100BASE-T2)

Clause 32 (100BASE-T2) makes special use of Auto-Negotiation and requires additional MII registers. This use is summarized below. Details are provided in 32.5.

Auto-Negotiation is mandatory for 100BASE-T2 (32.1.3.4).

100BASE-T2 introduces the concept of MASTER and SLAVE to define DTEs and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER/SLAVE status (32.5.4.3).

100BASE-T2 uses unique next page transmit and receive registers (MII Registers 8, 9 and 10) in conjunctions with Auto-Negotiation. These registers are in addition to Registers 0–7 as defined in 28.2.4 (32.5.2).

100BASE-T2 use of Auto-Negotiation generates information which is stored in configuration and status bits defined for the MASTER-SLAVE Control register (MII Register 9) and the MASTER-SLAVE Status register (MII Register 10).

100BASE-T2 requires an ordered exchange of next page messages (32.5.1).

100BASE-T2 parameters are configured based on information provided by the ordered exchange of next page messages.

100BASE-T2 adds new message codes to be transmitted during Auto-Negotiation (32.5.4.2).

100BASE-T2 adds 100BASE-T2 full duplex and half duplex capabilities to the priority resolution table (28B.3) and MII Status Register (22.2.4.2).

T2 is defined as a valid value for “x” in 28.3.1 (e.g., link_status_T2). T2 represents that the 100BASE-T2 PMA is the signal source.

28D.5 Extensions required for Clause 40 (1000BASE-T)

Clause 40 (1000BASE-T) makes special use of Auto-Negotiation and requires additional MII registers. This use is summarized below. Details are provided in 40.5.

a) Auto-Negotiation is mandatory for 1000BASE-T. (40.5.1)
b) 1000BASE-T requires an ordered exchange of Next Page messages. (40.5.1.2)
c) 1000BASE-T parameters are configured based on information provided by the ordered exchange of NEXT Page messages.
d) 1000BASE-T uses MASTER and SLAVE to define PHY operations and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER-SLAVE status.(40.5.2)
e) 1000BASE-T transmits and receives Next Pages for exchange of information related to MASTER-SLAVE operation. The information is specified in MII registers 9 and 10 (see 32.5.2 and 40.5.1.1), which are required in addition to registers 0-8 as defined in 28.2.4.
f) 1000BASE-T adds new message codes to be transmitted during Auto-Negotiation. (40.5.1.3)
g) 1000BASE-T adds 1000BASE-T full duplex and half duplex capabilities to the priority resolution table. (28B.3) and MII Extended Status Register (22.2.2.4)
h) 1000BASE-T is defined as a valid value for “x” in 28.3.1 (e.g., link_status_1GigT.) 1GigT represents that the 1000BASE-T PMA is the signal source.
i) 1000BASE-T supports Asymmetric Pause as defined in Annex 28B.

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Annex 29A

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DTE and repeater delay components

29A.1 DTE delay

Round-trip DTE delay = MAC transmit start to MDI output
+ MDI input to MDI output (worst case, nondeferred)
+ MDI input to collision detect

NOTE 1—Refer to Clauses 23, 24, 25, and 26.

NOTE 2—Worst-case values are used for the one T4 and one TX/FX value shown in Table 29–3. (TX/FX values for MAC transmit start and MDI input to collision detect; T4 value for MDI input to MDI output.)

29A.2 Repeater delay

Repeater delay= SOP (start-of-packet propagation delay)
+ SOJ (start-of-jam propagation delay)

NOTE—Refer to Clause 27.

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Annex 29B

(informative)

Recommended topology documentation

It is strongly recommended that detailed records documenting the topology components of 100BASE-T networks be prepared and maintained to facilitate subsequent modification. Proper 100BASE-T topology design requires an accurate knowledge of link segment and hub parameters to ensure proper operation of single and multi-segment, single collision domain networks. Link segment documentation is site-specific and requires careful documentation. It is recommended that the information shown in Table 29B–1 be collected for each link segment and archived for future reference. Hub performance parameters may be obtained from manufacturer documentation.

Table 29B–1—Recommended link segment documentation

	Horizontal wiring (wiring closet, from punch-down block to end station wall plate)	MII cable(s)	Wiring closet patch cord	End station connecting cable
Length				
Type (e.g., Category 3)				
Cable manufacturer				
Cable code/id (from manufacturer)				
Cable delay (in bit times per meter)				

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Annex 30A

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GDMO specification for 802.3 managed object classes

This annex formally defines the protocol encodings for CMIP and ISO/IEC 15802-2: 1995 [ANSI/IEEE Std 802.1B and 802.1k, 1995 Edition] for the IEEE 802.3 Managed Objects using the templates specified in ISO/IEC 10165-4: 1992. The application of a GDMO template compiler against 30A.1 to 30A.8 will produce the proper protocol encodings.

NOTE 1—The arcs (that is, object identifier values) defined in Annex 30A deprecate the arcs previously defined in Annexes H.1 (Layer Management), H.2 (Repeater Management), and H.3 (MAU Management). See IEEE Std 802.1F-1993, Annex C.4.

NOTE 2—During the update for 1000 Mb/s operation differences between objects in the root of the registration arcs were harmonized. All instances of *{iso(1) std(0) iso8802(8802) csma(3)...* were changed to *{iso(1) member-body(2) us(840) 802dot3(10006)...* in order to harmonize with the rest of this GDMO specification. For maximum compatibility with previous implementations it is recommended that all implementations respond equally to requests for communication based on either registration arc.

Each attribute definition in this clause references directly by means of the WITH ATTRIBUTE SYNTAX construct or indirectly by means of the DERIVED FROM construct an ASN.1 type or subtype that defines the attribute's type and range. Those ASN.1 types and subtypes defined exclusively for CSMA/CD Management appear in a single ASN.1 module in 30B.1.

Counters for these protocol encodings are specified as either 32 or 64 bits wide. Thirty-two bit counters are used for the protocol encoding of counter attributes, providing the minimum rollover time is 58 min or more. Sixty-four bit counters are used for the protocol encoding of counter attributes that could roll over in less than 58 min with a 32-bit counter. Approximate counter rollover times are provided as notes below each counter BEHAVIOUR definition. 1000 Mb/s counters are 10 times faster than 100 Mb/s counters, similarly 100 Mb/s counters are 10 times faster than 10 Mb/s counters. For formal definition of the counter, refer to the BEHAVIOUR bCMCounter in 30B.1.

30A.1 DTE MAC entity managed object class

30A.1.1 DTE MAC entity formal definition

```
oMACEntity                          MANAGED OBJECT CLASS

    DERIVED FROM                    "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 :
                                    1992":top;

    CHARACTERIZED BY
        pBasic                      PACKAGE
            ATTRIBUTES              aMACID                  GET;
            ACTIONS                 acInitializeMAC;
        ;
    ;
    CONDITIONAL PACKAGES
        pMandatory                  PACKAGE
            ATTRIBUTES              aFramesTransmittedOK    GET,
                                    aSingleCollisionFrames  GET,
```

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```
                    aMultipleCollisionFrames        GET,
                    aFramesReceivedOK               GET,
                    aFrameCheckSequenceErrors       GET,
                    aAlignmentErrors                GET,
                    aMACCapabilities                GET,
                    aDuplexStatus                   GET-SET;
        REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006)
                    csmacdmgt(30) package(4) macMandatoryPkg(1)};
        PRESENT IF  Conformance to DTE Management is desired.
                    Attributes aMACCapabilities and aDuplexStatus are
                    mandatory in systems that can operate in full duplex
                    mode and are recommended in systems that can only
                    operate in half duplex mode.;
pRecommended        PACKAGE
        ATTRIBUTES  aOctetsTransmittedOK            GET,
                    aFramesWithDeferredXmissions    GET,
                    aLateCollisions                 GET,
                    aFramesAbortedDueToXSColls      GET,
                    aFramesLostDueToIntMACXmitError GET,
                    aCarrierSenseErrors             GET,
                    aOctetsReceivedOK               GET,
                    aFramesLostDueToIntMACRcvError  GET,
                    aPromiscuousStatus              GET-SET,
                    aReadMulticastAddressList       GET;
        ACTIONS     acAddGroupAddress,
                    acDeleteGroupAddress;
        REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006)
                    csmacdmgt(30) package(4)
                    macRecommendedPkg(2)};
        PRESENT IF  The Recommended Package is implemented.;
pOptional           PACKAGE
        ATTRIBUTES  aMulticastFramesXmittedOK       GET,
                    aBroadcastFramesXmittedOK       GET,
                    aMulticastFramesReceivedOK      GET,
                    aBroadcastFramesReceivedOK      GET,
                    aInRangeLengthErrors            GET,
                    aOutOfRangeLengthField          GET,
                    aFrameTooLongErrors             GET,
                    aMACEnableStatus                GET-SET,
                    aTransmitEnableStatus           GET-SET,
                    aMulticastReceiveStatus         GET-SET,
                    aReadWriteMACAddress            GET-SET;
        ACTIONS     acExecuteSelfTest;
        REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006)
                    csmacdmgt(30) package(4) optionalPkg(3)};
        PRESENT IF  The Optional Package and the Recommended Package
                    are implemented.;
pArray              PACKAGE
        ATTRIBUTES  aCollisionFrames                GET;
        REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006)
                    csmacdmgt(30) package(4) arrayPkg(4)};
        PRESENT IF  The Array Package and the Recommended Package
                    are implemented.;
pExcessiveDeferral  PACKAGE
        ATTRIBUTES  aFramesWithExcessiveDeferral    GET;
```


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REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) excessiveDeferralPkg(5)};
PRESENT IF The ExcessiveDeferral Package and the Recommended Package are implemented.;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) macObjectClass(1)};

nbMACName **NAME BINDING**

SUBORDINATE OBJECT CLASS oMACEntity;
NAMED BY SUPERIOR OBJECT CLASS "ISO/IEC 10165-2":system;
WITH ATTRIBUTE aMACID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) macName(1)};

nbMACMonitor **NAME BINDING**

SUBORDINATE OBJECT CLASS "IEEE802.1F":ewmaMetricMonitor;
NAMED BY SUPERIOR OBJECT CLASS "ISO/IEC 10165-2":system;
WITH ATTRIBUTE aScannerId;
CREATE WITH-AUTOMATIC-INSTANCE-NAMING;
DELETE ONLY-IF-NO-CONTAINED-OBJECTS;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) macMonitor(2)};

nbMAC-MACControl **NAME BINDING**

SUBORDINATE OBJECT CLASS oMACEntity;
NAMED BY SUPERIOR OBJECT CLASS oMACControlEntity;
WITH ATTRIBUTE aMACID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) nbMAC-MACControl(16)};

nbMAC-Aggregator **NAME BINDING**

SUBORDINATE OBJECT CLASS oMACEntity;
NAMED BY SUPERIOR OBJECT CLASS oAggregator;
WITH ATTRIBUTE aMACID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) nbMAC-Aggregator(17)};

30A.1.2 DTE MAC entity attributes

aMACID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY;
BEHAVIOUR bMACID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)

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attribute(7) macID(1)};

bMACID **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.1;

aFramesTransmittedOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFramesTransmittedOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) framesTransmittedOK(2)};

bFramesTransmittedOK **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.2;

The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

NOTE 2—This maps to framesSent (of the mandatory macPackage) in ISO/IEC 10742: 1994.;

aSingleCollisionFrames **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bSingleCollisionFrames;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) singleCollisionFrames(3)};

bSingleCollisionFrames **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.3;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 103 h.;

aMultipleCollisionFrames **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bMultipleCollisionFrames;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) multipleCollisionFrames(4)};

bMultipleCollisionFrames **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.4;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 125 h.;

aFramesReceivedOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFramesReceivedOK;

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REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) framesReceivedOK(5)};

bFramesReceivedOK **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.5;

The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

NOTE 2—This maps to framesReceived (of the mandatory macPackage) in ISO/IEC 10742: 1994.;

aFrameCheckSequenceErrors **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFrameCheckSequenceErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) frameCheckSequenceErrors(6)};

bFrameCheckSequenceErrors **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.6;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aAlignmentErrors **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bAlignmentErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) alignmentErrors(7)};

bAlignmentErrors **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.7;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aOctetsTransmittedOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bOctetsTransmittedOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) octetsTransmittedOK(8)};

bOctetsTransmittedOK **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.8;

The approximate minimum time between counter rollovers for 10 Mb/s operation is 58 min.

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NOTE 2—This maps to octetsSent (of the mandatory macPackage) in ISO/IEC 10742: 1994.;

aFramesWithDeferredXmissions **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFramesWithDeferredXmissions;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) framesWithDeferredXmissions(9)};

bFramesWithDeferredXmissions **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.9;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 103 h.;

aLateCollisions **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bLateCollisions;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) lateCollisions(10)};

bLateCollisions **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.10;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aFramesAbortedDueToXSColls **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFramesAbortedDueToXSColls;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) framesAbortedDueToXSColls(11)};

bFramesAbortedDueToXSColls **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.11;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 53 days.;

aFramesLostDueToIntMACXmitError **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFramesLostDueToIntMACXmitError;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) framesLostDueToIntMACXmitError(12)};

bFramesLostDueToIntMACXmitError **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.12;

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NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 16 h.;

aCarrierSenseErrors **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bCarrierSenseErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) carrierSenseErrors(13)};

bCarrierSenseErrors **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.13;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aOctetsReceivedOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bOctetsReceivedOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) octetsReceivedOK(14)};

bOctetsReceivedOK **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.14;

The approximate minimum time between counter rollovers for 10 Mb/s operation is 58 min.

This maps to octetsReceived (of the mandatory macPackage) in ISO/IEC 10742: 1994.;

aFramesLostDueToIntMACRcvError **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFramesLostDueToIntMACRcvError;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) framesLostDueToIntMACRcvError(15)};

bFramesLostDueToIntMACRcvError **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.15;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aPromiscuousStatus **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.TrueFalse;
BEHAVIOUR bPromiscuousStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) promiscuousStatus(16)};

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bPromiscuousStatus **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.1.16;

aReadMulticastAddressList **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MulticastAddressList
BEHAVIOUR bReadMulticastAddressList;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) readMulticastAddressList(17)};

bReadMulticastAddressList **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.1.17;

aMulticastFramesXmittedOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bMulticastFramesXmittedOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) multicastFramesXmittedOK(18)};

bMulticastFramesXmittedOK **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.1.18;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aBroadcastFramesXmittedOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bBroadcastFramesXmittedOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) broadcastFramesXmittedOK(19)};

bBroadcastFramesXmittedOK **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.1.19;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aFramesWithExcessiveDeferral **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFramesWithExcessiveDeferral;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) framesWithExcessiveDeferral(20)};

bFramesWithExcessiveDeferral **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.1.20;

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NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 58 days.;

aMulticastFramesReceivedOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bMulticastFramesReceivedOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) multicastFramesReceivedOK(21)};

bMulticastFramesReceivedOK **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.21;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aBroadcastFramesReceivedOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bBroadcastFramesReceivedOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) broadcastFramesReceivedOK(22)};

bBroadcastFramesReceivedOK **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.22;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aInRangeLengthErrors **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bInRangeLengthErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) inRangeLengthErrors(23)};

bInRangeLengthErrors **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.23;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aOutOfRangeLengthField **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bOutOfRangeLengthField;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) outOfRangeLengthField(24)};

bOutOfRangeLengthField **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.24;

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NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aFrameTooLongErrors **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFrameTooLongErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) frameTooLongErrors(25)};

bFrameTooLongErrors **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.25;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 61 days.;

aMACEnableStatus **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.TrueFalse;
BEHAVIOUR bMACEnableStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) mACEnableStatus(26)};

bMACEnableStatus **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.26;

aTransmitEnableStatus **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.TrueFalse;
BEHAVIOUR bTransmitEnableStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) transmitEnableStatus(27)};

bTransmitEnableStatus **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.27;

aMulticastReceiveStatus **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.TrueFalse;
BEHAVIOUR bMulticastReceiveStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) multicastReceiveStatus(28)};

bMulticastReceiveStatus **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.28;

aReadWriteMACAddress **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802CommonDefinitions.MACAddress;
BEHAVIOUR bReadWriteMACAddress;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)

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attribute(7) modifyMACAddress(29)};

bReadWriteMACAddress **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.29;

NOTE—This maps to localMACAddress (of the mandatory macPackage) in ISO/IEC 10742: 1994.;

aCollisionFrames **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AttemptArray;
BEHAVIOUR bCollisionFrames;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) collisionFrames(30)};

bCollisionFrames **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.30;

NOTE—The approximate minimum time for any single counter rollover for 10 Mb/s operation is 103 h.;

aMACCapabilities **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MACCapabilitiesList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bMACCapabilities;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aMACCapabilities(89)};

bMACCapabilities **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.31;

aDuplexStatus **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.DuplexValues;
MATCHES FOR EQUALITY;
BEHAVIOUR bDuplexStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aDuplexStatus(90)};

bDuplexStatus **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.32;

30A.1.3 DTE MAC entity actions

acInitializeMAC **ACTION**

BEHAVIOUR bInitializeMAC;
MODE CONFIRMED;

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REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) initializeMAC(1)};

bInitializeMAC **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.2.1;

acAddGroupAddress **ACTION**

BEHAVIOUR bAddGroupAddress;
MODE CONFIRMED;
WITH INFORMATION SYNTAX IEEE802CommonDefinitions.MACAddress;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) addGroupAddress(2)};

bAddGroupAddress **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.2.2;

acDeleteGroupAddress **ACTION**

BEHAVIOUR bDeleteGroupAddress;
MODE CONFIRMED;
WITH INFORMATION SYNTAX IEEE802CommonDefinitions.MACAddress;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) deleteGroupAddress(3)};

bDeleteGroupAddress **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.2.3;

acExecuteSelfTest **ACTION**

BEHAVIOUR bExecuteSelfTestMAC;
MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) executeSelfTestMAC(4)};

bExecuteSelfTestMAC **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.2.4;

30A.2 DTE physical entity managed object class

30A.2.1 DTE physical entity formal definition

oPHYEntity MANAGED OBJECT CLASS

DERIVED FROM “CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992”:top;

CHARACTERIZED BY
pBasic PACKAGE
ATTRIBUTES aPHYID GET,

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```
                                        aPHYType                GET,
                                        aPHYTypeList            GET,
                                        aMIIDetect              GET,
                                        aPHYAdminState          GET;
            ;
        ;
        CONDITIONAL PACKAGES
            pRecommended                PACKAGE
                ATTRIBUTES              aSQETestErrors          GET;
                REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                        csmacdmgt(30) package(4)
                                        phyRecommendedPkg(6)};
                PRESENT IF              The Recommended Package is implemented.;
            pMultiplePhy                PACKAGE
                ACTIONS                 acPHYAdminControl;
                REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                        csmacdmgt(30) package(4)
                                        phyMultiplePhyPkg(7)};
                PRESENT IF              There is more than one PHY per MAC.;

            p100MbpsMonitor             PACKAGE
                ATTRIBUTES              aSymbolErrorDuringCarrier   GET;
                REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                        csmacdmgt(30) package(4)
                                        phy100MbpsMonitor(8)};
                PRESENT IF              The 100/1000 Mb/s Monitor capability is
                                        implemented.;
        REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                            managedObjectClass(3) phyObjectClass(2)};
```

nbPHYName **NAME BINDING**

```
        SUBORDINATE OBJECT CLASS    oPHYEntity;
        NAMED BY SUPERIOR OBJECT CLASS
                                    oMACEntity;
        WITH ATTRIBUTE              aPHYID;
        REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                            nameBinding(6) phyName(3)};
```

nbPHYMonitor **NAME BINDING**

```
        SUBORDINATE OBJECT CLASS    "IEEE802.1F":ewmaMetricMonitor;
        NAMED BY SUPERIOR OBJECT CLASS
                                    "ISO/IEC 10165-2":system;
        WITH ATTRIBUTE              aScannerId;
            CREATE                  WITH-AUTOMATIC-INSTANCE-NAMING;
            DELETE                  ONLY-IF-NO-CONTAINED-OBJECTS;
        REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                            nameBinding(6) phyMonitor(4)};
```

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30A.2.2 DTE physical entity attributes

aPHYID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR	EQUALITY;
BEHAVIOUR	bPHYID;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) phyID(31)};

bPHYID **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.2.1.1;

aPHYType **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.PhyTypeValue;
MATCHES FOR	EQUALITY;
BEHAVIOUR	bPHYType;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) phyType(32)};

bPHYType **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.2.1.2;

aPHYTypeList **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.PhyTypeList;
MATCHES FOR	EQUALITY, ORDERING;
BEHAVIOUR	bPHYTypeList;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) phyTypeList(33)};

bPHYTypeList **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.2.1.3;

aSQETestErrors **ATTRIBUTE**

DERIVED FROM	aCMCounter;
BEHAVIOUR	bSQETestErrors;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) sqeTestErrors(34)};

bSQETestErrors **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.2.1.4;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

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aSymbolErrorDuringCarrier **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bSymbolErrorDuringCarrier;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) symbolErrorDuringCarrier(35)};

bSymbolErrorDuringCarrier **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.2.1.5;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aMIIDetect ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MIIDetect;
MATCHES FOR EQUALITY;
BEHAVIOUR bMIIDetect;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) mIIDetect(36)};

bMIIDetect **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.2.1.6;

aPHYAdminState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.
PortAdminState;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bPHYAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) phyAdminState(37)};

bPHYAdminState **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.2.1.7;

30A.2.3 DTE physical entity actions

acPHYAdminControl **ACTION**

BEHAVIOUR bPHYAdminControl;
MODE CONFIRMED;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.
PortAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) phyAdminControl(5)};

bPHYAdminControl **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.2.2.1;

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30A.3 DTE MAC control entity managed object class

30A.3.1 DTE MAC control entity formal definition

oMACControlEntity **MANAGED OBJECT CLASS**

DERIVED FROM "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992":top;
CHARACTERIZED BY
pMandatory PACKAGE
ATTRIBUTES aMACControlFunctionsSupported GET-SET;
;
;
CONDITIONAL PACKAGES
pRecommended PACKAGE
ATTRIBUTES aMACControlFramesTransmitted GET,
aMACControlFramesReceived GET,
aUnsupportedOpcodesReceived GET;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) macControlRecommendedPkg(17)};
PRESENT IF The Recommended Package is implemented.;
REGISTERED AS{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) macControlObjectClass(8)};

nbMACControl-System **NAME BINDING**

SUBORDINATE OBJECT CLASS oMACControlEntity;
NAMED BY SUPERIOR OBJECT CLASS “ISO/IEC 10165-2”:system;
WITH ATTRIBUTE aMACControlID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) nbMACControl-System(18)};

nbMACControl-Aggregator **NAME BINDING**

SUBORDINATE OBJECT CLASS oMACControlEntity;
NAMED BY SUPERIOR OBJECT CLASS oAggregator;
WITH ATTRIBUTE aMACControlID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) nbMACControl-Aggregator(19)};

nbMACControlMonitor **NAME BINDING**

SUBORDINATE OBJECT CLASS"IEEE802.1F":ewmaMetricMonitor;
NAMED BY SUPERIOR OBJECT CLASS
"ISO/IEC 10165-2":system;
WITH ATTRIBUTEaScannerId;
CREATE WITH-AUTOMATIC-INSTANCE-NAMING;
DELETE ONLY-IF-NO-CONTAINED-OBJECTS;
REGISTERED AS{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) macControlMonitor(15)};

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30A.3.2 DTE MAC Control entity attributes

aMACControlID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY;
BEHAVIOR bMACControlID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aMACControlID(92)};

bMACControlID **BEHAVIOR**

DEFINED AS See "BEHAVIOR DEFINED AS" in 30.3.3.1;

aMACControlFunctionsSupported **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MACControlFunctionsList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOR bMACControlFunctionsSupported;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aMACControlFunctionsSupported(93)};

bMACControlFunctionsSupported **BEHAVIOR**

DEFINED AS See "BEHAVIOR DEFINED AS" in 30.3.3.2;

aMACControlFramesTransmitted **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX aCMCounter;
BEHAVIOR bMACControlFramesTransmitted;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aMACControlFramesTransmitted(94)};

bMACControlFramesTransmitted **BEHAVIOR**

DEFINED AS See "BEHAVIOR DEFINED AS" in 30.3.3.3;

aMACControlFramesReceived **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX aCMCounter;
BEHAVIOR bMACControlFramesReceived;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aMACControlFramesReceived(95)};

bMACControlFramesReceived **BEHAVIOR**

DEFINED AS See "BEHAVIOR DEFINED AS" in 30.3.3.4;

aUnsupportedOpcodesReceived **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX aCMCounter;
BEHAVIOR bUnsupportedOpcodesReceived;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aUnsupportedOpcodesReceived(96)};

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bUnsupportedOpcodesReceived BEHAVIOR

DEFINED AS See "BEHAVIOR DEFINED AS" in 30.3.3.5;

30A.4 DTE MAC Control function entity managed object class

30A.4.1 DTE MAC Control function entity formal definition

oMACControlFunctionEntityMANAGED OBJECT CLASS

DERIVED FROM"CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992":top;
CHARACTERIZED BY
pMandatory PACKAGE
ATTRIBUTES aPAUSELinkDelayAllowance GET-SET;
;
;
CONDITIONAL PACKAGES
pRecommended PACKAGE
ATTRIBUTES aPAUSEMACCtrlFramesTransmitted GET,
aPAUSEMACCtrlFramesReceived GET;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006)
csmacdmgt(30)
package(4) macControlFunctionRecomendedPkg(17)};
PRESENT IF The Recommended Package is implemented.;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006)
csmacdmgt(30)
managedObjectClass(3)macControlFunctionObjectClass(9)};

30A.4.2 DTE MAC Control function entity attributes

aPAUSELinkDelayAllowance ATTRIBUTE

WITH ATTRIBUTE SYNTAX LinkDelayAllowance;
BEHAVIOR bPAUSELinkDelayAllowance;
REGISTERED AS {iso(1) memberbody(2) us(840) ieee802dot3(10006)
csmacdmgt(30) attribute(7) aPAUSELinkDelayAllowance(97)};

bPAUSELinkDelayAllowance BEHAVIOR

DEFINED AS See “BEHAVIOR DEFINED AS” in 30.3.4.1;

aPAUSEMACCtrlFramesTransmitted ATTRIBUTE

WITH ATTRIBUTE SYNTAX aCMCounter;
BEHAVIOR bPAUSEMACCtrlFramesTransmitted;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006)
csmacdmgt(30) attribute(7) aPAUSEMACCtrlFramesTransmitted(98)};

bPAUSEMACCtrlFramesTransmitted BEHAVIOR

DEFINED AS See "BEHAVIOR DEFINED AS" in 30.3.4.2;

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aPAUSEMACCtrlFramesReceived **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX aCMCounter;
BEHAVIOR bPAUSEMACCtrlFramesReceived;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aPAUSEMACCtrlFramesReceived(99)};

bPAUSEMACCtrlFramesReceived **BEHAVIOR**

DEFINED AS See "BEHAVIOR DEFINED AS" in 30.3.4.3;

30A.5 Repeater managed object class

30A.5.1 Repeater, formal definition

oRepeater MANAGED OBJECT CLASS

DERIVED FROM "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 1992":top;

CHARACTERIZED BY
pRepeaterBasicControl PACKAGE
ATTRIBUTES aRepeaterID GET,
aRepeaterType GET,
aRepeaterGroupCapacity GET,
aGroupMap GET,
aRepeaterHealthState GET,
aRepeaterHealthText GET,
aRepeaterHealthData GET;
ACTIONS acResetRepeater,
acExecuteNonDisruptiveSelfTest;
NOTIFICATIONS nRepeaterHealth,
nRepeaterReset,
nGroupMapChange;
;
;
CONDITIONAL PACKAGES
pRepeaterPerfMonitor PACKAGE
ATTRIBUTES aTransmitCollisions GET;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) repeaterPerfMonitorPkg(9)};
PRESENT IF The Performance Monitor Capability is implemented.;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) repeaterObjectClass(3)};

nbRepeaterName **NAME BINDING**

SUBORDINATE OBJECT CLASS repeater;
NAMED BY SUPERIOR OBJECT CLASS
"ISO/IEC 10165-2":system AND SUBCLASSES;
WITH ATTRIBUTE aRepeaterID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) repeaterName(5)};

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nbRepeaterMonitor **NAME BINDING**

SUBORDINATE OBJECT CLASS	"IEEE802.1F":oEWMAMetricMonitor;
NAMED BY SUPERIOR OBJECT CLASS	"ISO/IEC 10165-2":system AND SUBCLASSES;
WITH ATTRIBUTE	aScannerId;
CREATE	WITH-AUTOMATIC-INSTANCE-NAMING;
DELETE	ONLY-IF-NO-CONTAINED-OBJECTS;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) repeaterMonitor(6)};

30A.5.2 Repeater attributes

aRepeaterID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR	EQUALITY;
BEHAVIOUR	bRepeaterID;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) repeaterID(38)};

bRepeaterID **BEHAVIOUR**

DEFINED AS	See "BEHAVIOUR DEFINED AS" in 30.4.1.1.1.

aRepeaterType **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.RepeaterType;
MATCHES FOR	EQUALITY;
BEHAVIOUR	bRepeaterType;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) repeaterType (39)};

bRepeaterType **BEHAVIOUR**

DEFINED AS	See "BEHAVIOUR DEFINED AS" in 30.4.1.1.2.

a**RepeaterGroupCapacity** **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR	EQUALITY, ORDERING;
BEHAVIOUR	bRepeaterGroupCapacity;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) repeaterGroupCapacity(40)};

bRepeaterGroupCapacity **BEHAVIOUR**

DEFINED AS	See "BEHAVIOUR DEFINED AS" in 30.4.1.1.3.

aGroupMap **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.BitString;

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MATCHES FOR EQUALITY;
BEHAVIOUR bGroupMap;

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) groupMap(41)};

bGroupMap BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.1.1.4.

aRepeaterHealthState ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.RepeaterHealthState;
MATCHES FOR EQUALITY;
BEHAVIOUR bRepeaterHealthState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) repeaterHealthState(42)};

bRepeaterHealthState BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.1.1.5.

aRepeaterHealthText ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.RepeaterHealthText;
MATCHES FOR EQUALITY;
BEHAVIOUR bRepeaterHealthText;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) repeaterHealthText(43)};

bRepeaterHealthText BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.1.1.6.

aRepeaterHealthData ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.RepeaterHealthData;
MATCHES FOR EQUALITY;
BEHAVIOUR bRepeaterHealthData;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) repeaterHealthData(44)};

bRepeaterHealthData BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.1.1.7.

aTransmitCollisions ATTRIBUTE

DERIVED FROM aCMCounter;
BEHAVIOUR bTransmitCollisions;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)

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attribute(7) transmitCollisions (45)};

bTransmitCollisions **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.1.1.8.

NOTE—The approximate minimum time for counter rollover for 10 Mb/s operation is 16 h.

30A.5.3 Repeater actions

acResetRepeater **ACTION**

BEHAVIOUR bResetRepeater;
MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) resetRepeater(6)};

bResetRepeater **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.1.2.1.

acExecuteNonDisruptiveSelfTest **ACTION**

BEHAVIOUR bExecuteNonDisruptiveSelfTest;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) executeNonDisruptiveSelfTestAction(7)};

bExecuteNonDisruptiveSelfTest **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.1.2.2.

30A.5.4 Repeater notifications

nRepeaterHealth **NOTIFICATION**

BEHAVIOUR bRepeaterHealth;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.RepeaterHealthInfo
AND ATTRIBUTE IDS repeaterHealthState aRepeaterHealthState, repeaterHealthText aRepeaterHealthText, repeaterHealthData aRepeaterHealthData
;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10) repeaterHealth(1)};

bRepeaterHealth **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.1.3.1.

nRepeaterReset **NOTIFICATION**

BEHAVIOUR bRepeaterReset;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.

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RepeaterHealthInfo
AND ATTRIBUTE IDS repeaterHealthState aRepeaterHealthState,
repeaterHealthText aRepeaterHealthText,
repeaterHealthData aRepeaterHealthData
;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10) repeaterReset(2)};

bRepeaterReset BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.1.3.2.

nGroupMapChange NOTIFICATION

BEHAVIOUR bGroupMapChange;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.BitString;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10) groupMapChange(3)};

bGroupMapChange BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.1.3.3.

30A.6 Group managed object class

30A.6.1 Group, formal definition

oGroup MANAGED OBJECT CLASS

DERIVED FROM "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 1992":top;
CHARACTERIZED BY
pGroupBasicControl PACKAGE
ATTRIBUTES aGroupID GET,
aGroupPortCapacity GET,
aPortMap GET;
NOTIFICATIONS nPortMapChange;
;
;

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) groupObjectClass(4)};

nbGroupName NAME BINDING

SUBORDINATE OBJECT CLASS oGroup;
NAMED BY SUPERIOR OBJECT CLASS
oRepeater AND SUBCLASSES;
WITH ATTRIBUTE aGroupID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) groupName(7)};

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30A.6.2 Group attributes

aGroupID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR	EQUALITY;
BEHAVIOUR	bGroupID;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) groupID(46)};

bGroupID **BEHAVIOUR**

DEFINED AS	See “BEHAVIOUR DEFINED AS” in 30.4.2.1.1;

aGroupPortCapacity **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR	EQUALITY, ORDERING;
BEHAVIOUR	bGroupPortCapacity;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) groupPortCapacity(47)};

bGroupPortCapacity **BEHAVIOUR**

DEFINED AS	See “BEHAVIOUR DEFINED AS” in 30.4.2.1.2;

aPortMap **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.BitString;
MATCHES FOR	EQUALITY;
BEHAVIOUR	bPortMap;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) portMap(48)};

bPortMap **BEHAVIOUR**

DEFINED AS	See “BEHAVIOUR DEFINED AS” in 30.4.2.1.3;

30A.6.3 Group notifications

nPortMapChange **NOTIFICATION**

BEHAVIOUR	bPortMapChange;
WITH INFORMATION SYNTAX	IEEE802Dot3-MgmtAttributeModule.BitString;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10) portMapChange(4)};

bPortMapChange **BEHAVIOUR**

DEFINED AS	See “BEHAVIOUR DEFINED AS” in 30.4.2.2.1;

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30A.7 Repeater port managed object class

30A.7.1 Port, formal definition

```
oRepeaterPort                       MANAGED OBJECT CLASS

    DERIVED FROM                    "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2
                                    1992":top;

    CHARACTERIZED BY
        pPortBasicControl           PACKAGE
            ATTRIBUTES              aPortID                 GET,
                                    aPortAdminState         GET,
                                    aAutoPartitionState     GET;
            ACTIONS                 acPortAdminControl;
        ;
    ;
    CONDITIONAL PACKAGES
        pPortPerfMonitor            PACKAGE
            ATTRIBUTES              aReadableFrames         GET,
                                    aReadableOctets         GET,
                                    aFrameCheckSequenceErrors GET,
                                    aAlignmentErrors        GET,
                                    aFramesTooLong          GET,
                                    aShortEvents            GET,
                                    aRunts                  GET,
                                    aCollisions             GET,
                                    aLateEvents             GET,
                                    aVeryLongEvents         GET,
                                    aDataRateMismatches     GET,
                                    aAutoPartitions         GET;
            REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                    csmacdmgt(30) package(4)
                                    portPerfMonitorPkg(10)};
            PRESENT IF              The Performance Monitor Capability is implemented.;
        pPortAddrTracking           PACKAGE
            ATTRIBUTES              aLastSourceAddress      GET,
                                    aSourceAddressChanges   GET;
            REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                    csmacdmgt(30) package(4) portAddrTrackPkg(11)};
            PRESENT IF              The Address Tracking and Performance Monitor
                                    capabilities are implemented.;
        p100MbpsMonitor             PACKAGE
            ATTRIBUTES              aIsolates               GET,
                                    aSymbolErrorDuringPacket GET;
            REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                    csmacdmgt(30) package(4)
                                    port100MbpsMonitor(12)};
            PRESENT IF              The 100/1000 Mb/s Monitor capability is
                                    implemented;
        pBurst                      PACKAGE
            ATTRIBUTES              aBursts                 GET;
            REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                    csmacdmgt(30) package(4)
```

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portBurst(18)};
PRESENT IF The 1000 Mb/s Burst Monitor capability is implemented;

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) repeaterPortObjectClass(5)};

nbPortName NAME BINDING

SUBORDINATE OBJECT CLASS oRepeaterPort;
NAMED BY SUPERIOR OBJECT CLASS
oGroup AND SUBCLASSES;
WITH ATTRIBUTE aPortID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) portName(8)};

30A.7.2 Port attributes

aPortID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
BEHAVIOUR bPortID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) portID(49)};

bPortID **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.3.1.1;

aPortAdminState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.
PortAdminState;
MATCHES FOR EQUALITY;
BEHAVIOUR bPortAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) portAdminState(50)};

bPortAdminState **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.3.1.2;

aAutoPartitionState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.
AutoPartitionState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAutoPartition;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) autoPartitionState(51)};

bAutoPartition **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.3.1.3;

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aReadableFrames **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bReadableFrames;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) readableFrames(52)};

bReadableFrames **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.4;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aReadableOctets **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bReadableOctets;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) readableOctets(53)};

bReadableOctets **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.5;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 58 min.;

aFrameCheckSequenceErrors **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFCSErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) frameCheckSequenceErrors(54)};

bFCSErrors **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.6;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aAlignmentErrors **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bAlignmentErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) alignmentErrors(55)};

bAlignmentErrors **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.7;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

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aFramesTooLong **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFramesTooLong;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) framesTooLong(56)};

bFramesTooLong **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.8;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 61 days.;

aShortEvents **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bShortEvents;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) shortEvents(57)};

bShortEvents **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.9;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 16 hours;

aRunts **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bRunts;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) runts(58)};

bRunts **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.10;

NOTE—The approximate minimum time for counter rollover for 10 Mb/s operation is 16 h.;

aCollisions **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bCollisions;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) collisions(59)};

bCollisions **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.11;

NOTE—The approximate minimum time for counter rollover for 10 Mb/s operation is 16 h.;

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aLateEvents **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bLateEvents;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) lateEvents(60)};

bLateEvents **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.12;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 81 h.;

aVeryLongEvents **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bVeryLongEvents;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) veryLongEvents(61)};

bVeryLongEvents **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.13;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 198 days.;

aDataRateMismatches **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bDataRateMismatches;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) dataRateMismatches(62)};

bDataRateMismatches **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.14;

aAutoPartitions **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bAutoPartitions;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) autoPartitions(63)};

bAutoPartitions **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.15;

aIsolates **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bIsolates;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)

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attribute(7) isolates(64)};

bIsolates **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.3.1.16;

aSymbolErrorDuringPacket **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bSymbolErrorDuringPacket;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) symbolErrorDuringPacket(65)};

bSymbolErrorDuringPacket **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.3.1.17;

aLastSourceAddress **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802CommonDefinitions.MACAddress;
MATCHES FOR EQUALITY;
BEHAVIOUR bLastSourceAddress;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) lastSourceAddress(66)};

bLastSourceAddress **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.3.1.18;

aSourceAddressChanges **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bSourceAddressChanges;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) sourceAddressChanges(67)};

bSourceAddressChanges **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.3.1.19;

NOTE—The approximate minimum time for counter rollover for 10 Mb/s operation is 81 h.;

aBursts **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bBursts;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) bursts(100)};

bBursts **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.3.1.20;

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30A.7.3 Port actions

acPortAdminControl **ACTION**

BEHAVIOUR bPortAdminControl;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.PortAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) portAdminControl(8)};

bPortAdminControl **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.2.1;

30A.8 MAU managed object class

30A.8.1 MAU, formal definition

```
oMAU                                MANAGED OBJECT CLASS

    DERIVED FROM                    "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 :
                                    1992":top;

    CHARACTERIZED BY
        pMAUBasic                   PACKAGE
            ATTRIBUTES              aMAUID                  GET,
                                    aMAUType                GET-SET,
                                    aMAUTypeList            GET,
                                    aMediaAvailable         GET,
                                    aJabber                 GET,
                                    aMAUAdminState          GET;
            NOTIFICATIONS           nJabber;
        ;
    ;
    CONDITIONAL PACKAGES
        pMAUControl                 PACKAGE
            ACTIONS                 acResetMAU,
                                    acMAUAdminControl;
            REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                    csmacdmgt(30)
                                    package(4) mauControlPkg(13)};
            PRESENT IF              The pMAUControl package is implemented.;

        pMediaLossTracking          PACKAGE
            ATTRIBUTES              aLoseMediaCounter       GET;
            REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                    csmacdmgt(30)
                                    package(4) mediaLossTrackingPkg(14)};
            PRESENT IF              MAU TypeValue = AUI or if the
                                    pMediaLossTracking package is implemented.;

        pBroadbandDTEMAU            PACKAGE
            ATTRIBUTES              aBbMAUXmitRcvSplitType  GET,
```

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```
                                aBroadbandFrequencies          GET;
            REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                csmacdmgt(30)
                                package(4) broadbandMAUPkg(15)};
            PRESENT IF          The MAU is of type 10BROAD36.;

        p100MbpsMonitor         PACKAGE
            ATTRIBUTES          aFalseCarriers                 GET;
            REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                csmacdmgt(30)
                                package(4) mau100MbpsMonitor(16)};
            PRESENT IF          The MAU is capable of 100 Mb/s operation.;
    REGISTERED AS               {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                csmacdmgt(30)
                                managedObjectClass(3) mauObjectClass(6)};
```

nbMAU-repeaterName **NAME BINDING**

```
    SUBORDINATE OBJECT CLASS    oMAU;
    NAMED BY SUPERIOR OBJECT CLASS
                                            --(of oRepeaterPort)
                                oRepeaterPort   AND SUBCLASSES;
                                            --{1.2.840.10006.30.3.5}
    WITH ATTRIBUTE              aMAUID;
    REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                        nameBinding(6) mau-repeaterName(9)};
```

nbMAU-dteName **NAME BINDING**

```
    SUBORDINATE OBJECT CLASS    oMAU;
    NAMED BY SUPERIOR OBJECT CLASS
                                            --(of oPHYEntity)
                                oPHYEntity  AND SUBCLASSES
                                            --{1.2.840.10006.30.3.2};
    WITH ATTRIBUTE              aMAUID;
    REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                        nameBinding(6) mau-dteName(10)};
```

30A.8.2 MAU attributes

aMAUID **ATTRIBUTE**

```
    WITH ATTRIBUTE SYNTAX       IEEE802Dot3-MgmtAttributeModule.OneOfName;
    MATCHES FOR                 EQUALITY;
    BEHAVIOUR                   bMAUID;
    REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                        attribute(7) mauID(68)};
```

bMAUID **BEHAVIOUR**

```
    DEFINED AS          See “BEHAVIOUR DEFINED AS” in 30.5.1.1.1;
```


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aMAUType **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.TypeValue;
MATCHES FOR	EQUALITY, ORDERING;
BEHAVIOUR	bMAUType;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) mauType(69)};

bMAUType **BEHAVIOUR**

DEFINED AS	See “BEHAVIOUR DEFINED AS” in 30.5.1.1.2;

aMAUTypeList **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.TypeList;
MATCHES FOR	EQUALITY, ORDERING;
BEHAVIOUR	bMAUTypeList;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) mauTypeList(70)};

bMAUTypeList **BEHAVIOUR**

DEFINED AS	See “BEHAVIOUR DEFINED AS” in 30.5.1.1.3;

aMediaAvailable **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule. MediaAvailState;
MATCHES FOR	EQUALITY, ORDERING;
BEHAVIOUR	bMediaAvailable;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) mauMediaAvailable(71)};

bMediaAvailable **BEHAVIOUR**

DEFINED AS	See “BEHAVIOUR DEFINED AS” in 30.5.1.1.4;

aLoseMediaCounter **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.aCMCounter;
MATCHES FOR	EQUALITY, ORDERING;
BEHAVIOUR	bLoseMediaCounter;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) mauLoseMediaCounter(72)};

bLoseMediaCounter **BEHAVIOUR**

DEFINED AS	See “BEHAVIOUR DEFINED AS” in 30.5.1.1.5;

aJabber **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.Jabber;
MATCHES FOR	EQUALITY, ORDERING;
BEHAVIOUR	bJabberAttribute;

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REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) jabber(73)};

bJabberAttribute **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.5.1.1.6;

aMAUAdminState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AdminState;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bMAUAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) mauAdminState(74)};

bMAUAdminState **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.5.1.1.7;

aBbMAUXmitRcvSplitType **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.
BbandXmitRcvSplitType;
MATCHES FOR EQUALITY;
BEHAVIOUR bBbMAUXmitRcvSplitType;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) bBandSplitType(75)};

bBbMAUXmitRcvSplitType **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.5.1.1.8;

aBroadbandFrequencies **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.
BbandFrequency;
MATCHES FOR EQUALITY;
BEHAVIOUR bBroadbandFrequencies;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) bBandFrequencies(76)};

bBroadbandFrequencies **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.5.1.1.9;

aFalseCarriers **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bFalseCarriers;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) falseCarriers(77)};

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bFalseCarriers **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.5.1.1.10;

aIdleErrorCount **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.RegisterEight;
BEHAVIOUR bIdleErrorCount;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) idleErrorCount(91)};

bIdleErrorCount **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.5.1.1.11;

30A.8.3 MAU actions

acResetMAU **ACTION**

BEHAVIOUR bResetMAU;
MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) resetMAU(9)};

bResetMAU **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.5.1.2.1;

acMAUAdminControl **ACTION**

BEHAVIOUR bMAUAdminControl;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.AdminState;
MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) mauAdminCtrl(10)};

bMAUAdminControl **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.5.1.2.2;

30A.8.4 MAU notifications

nJabber **NOTIFICATION**

BEHAVIOUR bJabberNotification;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.Jabber;
;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10) jabber(5)};

bJabberNotification **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.5.1.3.1;

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30A.9 AutoNegotiation managed object class

30A.9.1 AutoNegotiation, formal definition

```
oAutoNegotiation                    MANAGED OBJECT CLASS

    DERIVED FROM                    "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 :
                                    1992":top;

    CHARACTERIZED BY
        pAutoNeg                    PACKAGE
            ATTRIBUTES              aAutoNegID                      GET,
                                    aAutoNegAdminState              GET,
                                    aAutoNegRemoteSignaling         GET,
                                    aAutoNegAutoConfig              GET-SET,
                                    aAutoNegLocalTechnologyAbility  GET,
                                    aAutoNegAdvertisedTechnologyAbility GET-SET,
                                    aAutoNegReceivedTechnologyAbility GET,
                                    aAutoNegLocalSelectorAbility    GET,
                                    aAutoNegAdvertisedSelectorAbility GET-SET,
                                    aAutoNegReceivedSelectorAbility GET;
            ACTIONS
                                    acAutoNegRestartAutoConfig,
                                    acAutoNegAdminControl;
        ;
    ;
    REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                        managedObjectClass(3) autoNegObjectClass(7)};

nbAutoNeg-mauName                   NAME BINDING

    SUBORDINATE OBJECT CLASS        oMAU;
    NAMED BY SUPERIOR OBJECT CLASS
                                            --(of oMAU)
                                    oMAU   AND SUBCLASSES;
                                            --{1.2.840.10006.30.3.6}
    WITH ATTRIBUTE                  aMAUID;
    REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                        nameBinding(6) autoNeg-mauName(11)};
```

30A.9.2 Auto-Negotiation attributes

```
aAutoNegID                          ATTRIBUTE

    WITH ATTRIBUTE SYNTAX           IEEE802Dot3-MgmtAttributeModule.OneOfName;
    MATCHES FOR                     EQUALITY;
    BEHAVIOUR                       bAutoNegID;
    REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                        attribute(7) autoNegID(78)};

bAutoNegID                          BEHAVIOUR

    DEFINED AS          See "BEHAVIOUR DEFINED AS" in 30.6.1.1.1;
```


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aAutoNegAdminState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AutoNegAdminState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAutoNegAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) autoNegAdminState(79)};

bAutoNegAdminState **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.1.2;

aAutoNegRemoteSignaling **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AutoNegRemoteSignalingDetect;
MATCHES FOR EQUALITY;
BEHAVIOUR bAutoNegRemoteSignaling;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) autoNegRemoteSignaling(80)};

bAutoNegRemoteSignaling **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.1.3;

aAutoNegAutoConfig **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AutoNegAutoConfig;
MATCHES FOR EQUALITY;
BEHAVIOUR bAutoNegAutoConfig;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) autoNegAutoConfig(81)};

bAutoNegAutoConfig **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.1.4;

aAutoNegLocalTechnologyAbility **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AutoNegTechnologyList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAutoNegLocalTechnologyAbility;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) autoNegLocalTechnologyAbility(82)};

bAutoNegLocalTechnologyAbility **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.1.5;

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aAutoNegAdvertisedTechnologyAbility ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AutoNegTechnologyList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAutoNegAdvertisedTechnologyAbility;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) autoNegAdvertisedTechnologyAbility(83)};

bAutoNegAdvertisedTechnologyAbility BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.6.1.1.6;

aAutoNegReceivedTechnologyAbility ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AutoNegTechnologyList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAutoNegReceivedTechnologyAbility;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) autoNegReceivedTechnologyAbility(84)};

bAutoNegReceivedTechnologyAbility BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.6.1.1.7;

aAutoNegLocalSelectorAbility ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AutoNegSelectorList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAutoNegLocalSelectorAbility;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) autoNegLocalSelectorAbility(85)};

bAutoNegLocalSelectorAbility BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.6.1.1.8;

aAutoNegAdvertisedSelectorAbility ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AutoNegSelectorList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAutoNegAdvertisedSelectorAbility;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) autoNegAdvertisedSelectorAbility(86)};

bAutoNegAdvertisedSelectorAbility BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.6.1.1.9;

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aAutoNegReceivedSelectorAbility **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.
AutoNegSelectorList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAutoNegReceivedSelectorAbility;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) autoNegReceivedSelectorAbility(87)};

bAutoNegReceivedSelectorAbility BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.1.10;

30A.9.3 AutoNegotiation actions

acAutoNegRestartAutoConfig **ACTION**

BEHAVIOUR bAutoNegRestartAutoConfig;
MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) autoNegRestartAutoConfig(11)};

bAutoNegRestartAutoConfig **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.2.1;

acAutoNegAdminControl **ACTION**

BEHAVIOUR bAutoNegAdminControl;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.
AutoNegAdminState;
MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) autoNegAdminCtrl(12)};

bAutoNegAdminControl **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.2.2;

30A.10 ResourceTypeID managed object class

30A.10.1 ResourceTypeID, formal definition

— Implementation of this managed object in accordance with the definition contained in IEEE Std
— 802.1F-1993 is a conformance requirement of this standard.
— NOTE—A single instance of the Resource Type ID managed object exists within the oMACEntity
— managed object class, a single instance of the Resource Type ID managed object exists within
— the oRepeater managed object class, and a single instance of the Resource Type ID managed
— object exists within the oMAU managed object class conditional on the presence of an MII.
— The managed object itself is contained in IEEE Std 802.1F-1993, therefore only name bindings
— appear in this standard;

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nbResourceTypeID-mac **NAME BINDING**

SUBORDINATE OBJECT CLASS "IEEE802.1F":oResourceTypeID;
NAMED BY SUPERIOR OBJECT CLASS
oMACEntity;
WITH ATTRIBUTE "IEEE802.1F":aResourceTypeIDName;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) resourceTypeID-mac(12)};

nbResourceTypeID-repeater **NAME BINDING**

SUBORDINATE OBJECT CLASS "IEEE802.1F":oResourceTypeID;
NAMED BY SUPERIOR OBJECT CLASS
oRepeater AND SUBCLASSES;
WITH ATTRIBUTE "IEEE802.1F":aResourceTypeIDName;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) resourceTypeID-repeater(13)};

nbResourceTypeID-mau **NAME BINDING**

SUBORDINATE OBJECT CLASS "IEEE802.1F":oResourceTypeID;
NAMED BY SUPERIOR OBJECT CLASS
oMAU AND SUBCLASSES;
WITH ATTRIBUTE "IEEE802.1F":aResourceTypeIDName;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) resourceTypeID-mau(14)};

30A.11 Aggregator managed object class

30A.11.1 Aggregator, formal definition

oAggregator **MANAGED OBJECT CLASS**

DERIVED FROM "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992":top;
CHARACTERIZED BY
pAggregatorBasic PACKAGE
ATTRIBUTES aAggID GET;
;
;
CONDITIONAL PACKAGES
pAggregatorMandatory PACKAGE
ATTRIBUTES aAggDescription GET,
aAggName GET-REPLACE,
aAggActorSystemID GET-REPLACE,
aAggActorSystemPriority GET-REPLACE,
aAggAggregateOrIndividual GET,
aAggActorAdminKey GET-REPLACE,
aAggActorOperKey GET,
aAggMACAddress GET,
aAggPartnerSystemID GET,
aAggPartnerSystemPriority GET,
aAggPartnerOperKey GET,
aAggAdminState GET-REPLACE,

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aAggOperState GET,
aAggTimeOfLastOperChange GET,
aAggDataRate GET,
aAggFramesTxOK GET,
aAggFramesRxOK GET,
aAggLinkUpDownNotificationEnable GET-REPLACE,
aAggCollectorMaxDelay GET-REPLACE;

NOTIFICATIONS
nAggLinkUpNotification,
nAggLinkDownNotification;

REGISTERED AS
{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) pAggregatorMandatory(19)};

PRESENT IF Conformance to Link Aggregation management is desired;

pAggregatorRecommendedPACKAGE

ATTRIBUTES aAggOctetsTxOK GET,
aAggOctetsRxOK GET,
aAggFramesDiscardedOnTx GET,
aAggFramesDiscardedOnRx GET,
aAggFramesWithTxErrors GET,
aAggFramesWithRxErrors GET,
aAggUnknownProtocolFrames GET,
aAggPortList GET;

REGISTERED AS
{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) pAggregatorRecommended(20)};

PRESENT IF The recommended package is implemented;

pAggregatorOptional PACKAGE

ATTRIBUTES aAggMulticastFramesTxOK GET,
aAggMulticastFramesRxOK GET,
aAggBroadcastFramesTxOK GET,
aAggBroadcastFramesRxOK GET;

REGISTERED AS
{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) pAggregatorOptional(21)};

PRESENT IF The optional package is implemented;

;

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) oAggregator(10)};

nbAggregatorName NAME BINDING

SUBORDINATE OBJECT CLASS oAggregator;
NAMED BY SUPERIOR OBJECT CLASS "ISO/IEC 10165-2":system;
WITH ATTRIBUTE aAggID
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) nbAggregatorName(20)};

30A.11.2 Aggregator attributes

aAggID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggID;

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MATCHES FOR EQUALITY;
BEHAVIOUR bAggID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggID(101)};

bAggID **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.1;

aAggDescription **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.DescriptionString;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggDescription;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggDescription(102)};

bAggDescription **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.2;

aAggName **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.DescriptionString;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggName;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggName(103)};

bAggName **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.3;

aAggActorSystemID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MACAddress;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggActorSystemID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggActorSystemID(104)};

bAggActorSystemID **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.4;

aAggActorSystemPriority **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PriorityValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggActorSystemPriority;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggActorSystemPriority(105)};

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bAggActorSystemPriority BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.5;

aAggAggregateOrIndividual ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggOrInd;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggAggregateOrIndividual;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggAggregateOrIndividual(106)};

bAggAggregateOrIndividual BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.6;

aAggActorAdminKey ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.KeyValue;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggActorAdminKey;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggActorAdminKey(107)};

bAggActorAdminKey BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.7;

aAggActorOperKey ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.KeyValue;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggActorOperKey;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggActorOperKey(108)};

bAggActorOperKey BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.8;

aAggMACAddress ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MACAddress;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggMACAddress;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggMACAddress(109)};

bAggMACAddress BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.9;

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aAggPartnerSystemID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MACAddress;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPartnerSystemID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPartnerSystemID(110)};

bAggPartnerSystemID **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.10;

aAggPartnerSystemPriority **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PriorityValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPartnerSystemPriority;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPartnerSystemPriority(111)};

bAggPartnerSystemPriority **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.11;

aAggPartnerOperKey **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.KeyValue;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPartnerOperKey;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPartnerOperKey(112)};

bAggPartnerOperKey **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.12;

aAggAdminState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggAdminState(113)};

bAggAdminState **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.13;

aAggOperState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggOperState ;

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REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggOperState(114)};

bAggOperState **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.14;

aAggTimeOfLastOperChange **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.Integer32;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggTimeOfLastOperChange;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggTimeOfLastOperChange(115)};

bAggTimeOfLastOperChange **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.15;

aAggDataRate **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggDataRate;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggDataRate;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggDataRate(116)};

bAggDataRate **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.16;

aAggOctetsTxOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggOctetsTxOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggOctetsTxOK(117)};

bAggOctetsTxOK **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.17.

NOTE—This counter has a maximum increment rate of 1 230 000 counts per second at 10 Mb/s.;

aAggOctetsRxOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggOctetsRxOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggOctetsRxOK(118)};

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bAggOctetsRxOK **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.18.

NOTE—This counter has a maximum increment rate of 1 230 000 counts per second at 10 Mb/s.;

aAggFramesTxOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggFramesTxOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggFramesTxOK(119)};

bAggFramesTxOK **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.19.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggFramesRxOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggFramesRxOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggFramesRxOK(120)};

bAggFramesRxOK **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.20.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggMulticastFramesTxOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggMulticastFramesTxOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggMulticastFramesTxOK(121)};

bAggMulticastFramesTxOK **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.21.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggMulticastFramesRxOK **ATTRIBUTE**

DERIVED FROM aCMCounter;

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MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggMulticastFramesRxOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggMulticastFramesRxOK(122)};

bAggMulticastFramesRxOK BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.22.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggBroadcastFramesTxOK ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggBroadcastFramesTxOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggBroadcastFramesTxOK(123)};

bAggBroadcastFramesTxOK BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.23.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggBroadcastFramesRxOK ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggBroadcastFramesRxOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggBroadcastFramesRxOK(124)};

bAggBroadcastFramesRxOK BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.24.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggFramesDiscardedOnTx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggFramesDiscardedOnTx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggFramesDiscardedOnTx(125)};

bAggFramesDiscardedOnTx BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.25.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

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aAggFramesDiscardedOnRx **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggFramesDiscardedOnRx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggFramesDiscardedOnRx(126)};

bAggFramesDiscardedOnRx **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.26.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggFramesWithTxErrors **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggFramesWithTxErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggFramesWithTxErrors(127)};

bAggFramesWithTxErrors **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.27.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggFramesWithRxErrors **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggFramesWithRxErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggFramesWithRxErrors(128)};

bAggFramesWithRxErrors **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.28.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggUnknownProtocolFrames **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggUnknownProtocolFrames;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggUnknownProtocolFrames(129)};

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bAggUnknownProtocolFrames BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.29.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggLinkUpDownNotificationEnable ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.NotificationEnable;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggLinkUpDownNotificationEnable;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggLinkUpDownNotificationEnable(130)};

bAggLinkUpDownNotificationEnable BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.31;

aAggPortList ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggPortList;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortList;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortList(131)};

bAggPortList BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.30;

aAggCollectorMaxDelay ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.CollectorMaxDelay;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggCollectorMaxDelay;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggCollectorMaxDelay(132)};

bAggCollectorMaxDelay BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.32;

30A.11.3 Aggregator notifications

nAggLinkUpNotification NOTIFICATION

BEHAVIOUR bAggLinkUpNotification;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.AggID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10) nAggLinkUpNotification(6)};

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bAggLinkUpNotification **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.2.1;

nAggLinkDownNotification **NOTIFICATION**

BEHAVIOUR bAggLinkDownNotification;
WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10) nAggLinkDownNotification(7)};

bAggLinkDownNotification **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.2.2;

30A.12 Aggregation Port managed object class

30A.12.1 Aggregation Port, formal definition

oAggregationPort **MANAGED OBJECT CLASS**

DERIVED FROM “CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992”:top;
CHARACTERIZED BY
pAggregationPortBasic PACKAGE
ATTRIBUTES aAggPortID GET;
;
;
CONDITIONAL PACKAGES
pAggregationPortMandatory PACKAGE
ATTRIBUTES aAggPortActorSystemPriority GET-REPLACE,
aAggPortActorSystemID GET,
aAggPortActorAdminKey GET-REPLACE,
aAggPortActorOperKey GET,
aAggPortPartnerAdminSystemPriority GET-REPLACE,
aAggPortPartnerOperSystemPriority GET,
aAggPortPartnerAdminSystemID GET-REPLACE,
aAggPortPartnerOperSystemID GET,
aAggPortPartnerAdminKey GET-REPLACE,
aAggPortPartnerOperKey GET,
aAggPortSelectedAggID GET,
aAggPortAttachedAggID GET,
aAggPortActorPort GET,
aAggPortActorPortPriority GET-REPLACE,
aAggPortPartnerAdminPort GET-REPLACE,
aAggPortPartnerOperPort GET,
aAggPortPartnerAdminPortPriority GET-REPLACE,
aAggPortPartnerOperPortPriority GET,
aAggPortActorAdminState GET-REPLACE,
aAggPortActorOperState GET,
aAggPortPartnerAdminState GET-REPLACE,
aAggPortPartnerOperState GET,
aAggPortAggregateOrIndividual GET;

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REGISTERED AS
{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacd-mgt(30) package(4) pAggregationPortMandatory(22)};
PRESENT IF Conformance to Link Aggregation management is desired;
;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) oAggregationPort(11)};

nbAggregationPort **NAME BINDING**

SUBORDINATE OBJECT CLASS oAggregationPort;
NAMED BY SUPERIOR OBJECT CLASS oAggregator;
WITH ATTRIBUTE aAggPortID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) nbAggregationPortName(21)};

30A.12.2 Aggregation Port attributes

aAggPortID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggPortID;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortID(133)};

bAggPortID **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.2.1.1;

aAggPortActorSystemPriority **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PriorityValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortActorSystemPriority;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortActorSystemPriority(134)};

bAggPortActorSystemPriority **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.2.1.2;

aAggPortActorSystemID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MACAddress;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortActorSystemID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortActorSystemID(135)};

bAggPortActorSystemID **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.2.1.3;

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aAggPortActorAdminKey ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.KeyValue;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortActorAdminKey;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortActorAdminKey(136)};

bAggPortActorAdminKey BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.4;

aAggPortActorOperKey ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.KeyValue;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortActorOperKey;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortActorOperKey(137)};

bAggPortActorOperKey BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.5;

aAggPortPartnerAdminSystemPriority ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PriorityValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerAdminSystemPriority;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerAdminSystemPriority(138)};

bAggPortPartnerAdminSystemPriority BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.6;

aAggPortPartnerOperSystemPriority ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PriorityValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerOperSystemPriority;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerOperSystemPriority(139)};

bAggPortPartnerOperSystemPriority BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.7;

aAggPortPartnerAdminSystemID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MACAddress;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerAdminSystemID;

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REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerAdminSystemID(140)};

bAggPortPartnerAdminSystemID BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.8;

aAggPortPartnerOperSystemID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MACAddress;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR baAggPortPartnerOperSystemID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerOperSystemID(141)};

bAggPortPartnerOperSystemID BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.9;

aAggPortPartnerAdminKey ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.KeyValue;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortPartnerAdminKey;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerAdminKey(142)};

bAggPortPartnerAdminKey BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.10;

aAggPortPartnerOperKey ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.KeyValue;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortPartnerOperKey;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerOperKey(143)};

bAggPortPartnerOperKey BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.11;

aAggPortSelectedAggID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggID;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortSelectedAggID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortSelectedAggID(144)};

bAggPortSelectedAggID BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.12;

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aAggPortAttachedAggID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggID;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortAttachedAggID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortAttachedAggID(145)};

bAggPortAttachedAggID **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.13;

aAggPortActorPort **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PortNumber;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortActorPort;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortActorPort(146)};

bAggPortActorPort **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.14;

aAggPortActorPortPriority **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PriorityValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortActorPortPriority;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortActorPortPriority(147)};

bAggPortActorPortPriority **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.15;

aAggPortPartnerAdminPort **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PortNumber;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerAdminPort;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerAdminPort(148)};

bAggPortPartnerAdminPort **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.16;

aAggPortPartnerOperPort **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PortNumber;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerOperPort;

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REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerOperPort(149)};

bAggPortPartnerOperPort BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.17;

aAggPortPartnerAdminPortPriority ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PriorityValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerAdminPortPriority;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerAdminPortPriority(150)};

bAggPortPartnerAdminPortPriority BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.18;

aAggPortPartnerOperPortPriority ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PriorityValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerOperPortPriority;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerOperPortPriority(151)};

bAggPortPartnerOperPortPriority BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.19;

aAggPortActorAdminState ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggPortState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortActorAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortActorAdminState(152)};

bAggPortActorAdminState BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.20;

aAggPortActorOperState ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggPortState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortActorOperState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortActorOperState(153)};

bAggPortActorOperState BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.21;

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aAggPortPartnerAdminState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggPortState;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerAdminState(154)};

bAggPortPartnerAdminState **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.22;

aAggPortPartnerOperState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggPortState;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerOperState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerOperState(155)};

bAggPortPartnerOperState **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.23;

aAggPortAggregateOrIndividual **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggOrInd;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortAggregateOrIndividual;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortAggregateOrIndividual(156)};

bAggPortAggregateOrIndividual **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.24;

30A.13 Aggregation Port Statistics managed object class

30A.13.1 Aggregation Port Statistics, formal definition

oAggPortStats **MANAGED OBJECT CLASS**

DERIVED FROM "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992":top;
CONDITIONAL PACKAGES
pAggPortStats PACKAGE
ATTRIBUTES aAggPortStatsID GET,
aAggPortStatsLACPDUsRx GET,
aAggPortStatsMarkerPDUsRx GET,
aAggPortStatsMarkerResponsePDUsRx GET,
aAggPortStatsUnknownRx GET,
aAggPortStatsIllegalRx GET,
aAggPortStatsLACPDUsTx GET,

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aAggPortStatsMarkerPDUsTx GET,
aAggPortStatsMarkerResponsePDUsTx GET;
REGISTERED AS
{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) pAggPortStats(23)};
PRESENT IF The Aggregation Port Statistics package is supported;
;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) oAggPortStats(12)};

nbAggPortStats NAME BINDING

SUBORDINATE OBJECT CLASS oAggPortStats;
NAMED BY SUPERIOR OBJECT CLASS oAggregationPort;
WITH ATTRIBUTE aAggPortStatsID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) nbAggPortStats(22)};

30A.13.2 Aggregation Port Statistics attributes

aAggPortStatsID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggPortID;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortStatsID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsID(157)};

bAggPortStatsID BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.3.1.1;

aAggPortStatsLACPDUsRx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortStatsLACPDUsRx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsLACPDUsRx(158)};

bAggPortStatsLACPDUsRx BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.3.1.2.

NOTE—This counter has a maximum increment rate of 5 counts per second at 10 Mb/s.;

aAggPortStatsMarkerPDUsRx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortStatsMarkerPDUsRx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsMarkerPDUsRx(159)};

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bAggPortStatsMarkerPDUsRx BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.3.1.3.

NOTE—This counter has a maximum increment rate of 5 counts per second at 10 Mb/s.;

aAggPortStatsMarkerResponsePDUsRx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortStatsMarkerResponsePDUsRx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsMarkerResponsePDUsRx(160)};

bAggPortStatsMarkerResponsePDUsRx BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.3.1.4.

NOTE—This counter has a maximum increment rate of 5 counts per second at 10 Mb/s.;

aAggPortStatsUnknownRx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortStatsUnknownRx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsUnknownRx(161)};

bAggPortStatsUnknownRx BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.3.1.5.

NOTE—This counter has a maximum increment rate of 50 counts per second at 10 Mb/s.;

aAggPortStatsIllegalRx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortStatsIllegalRx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsIllegalRx(162)};

bAggPortStatsIllegalRx BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.3.1.6.

NOTE—This counter has a maximum increment rate of 50 counts per second at 10 Mb/s.;

aAggPortStatsLACPDUsTx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortStatsLACPDUsTx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsLACPDUsTx(163)};

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bAggPortStatsLACPDUsTx BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.3.1.7.

NOTE—This counter has a maximum increment rate of 5 counts per second at 10 Mb/s.;

aAggPortStatsMarkerPDUsTx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortStatsMarkerPDUsTx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsMarkerPDUsTx(164)};

bAggPortStatsMarkerPDUsTx BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.3.1.8.

NOTE—This counter has a maximum increment rate of 5 counts per second at 10 Mb/s.;

aAggPortStatsMarkerResponsePDUsTx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortStatsMarkerResponsePDUsTx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsMarkerResponsePDUsTx(165)};

bAggPortStatsMarkerResponsePDUsTx BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.3.1.9.

NOTE—This counter has a maximum increment rate of 5 counts per second at 10 Mb/s.;

30A.14 Aggregation Port Debug Information managed object class

30A.14.1 Aggregation Port Debug Information, formal definition

oAggPortDebugInformation MANAGED OBJECT CLASS

DERIVED FROM "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992":top;
CONDITIONAL PACKAGES
pLACPDebug PACKAGE
ATTRIBUTES
aAggPortDebugInformationID GET,
aAggPortDebugRxState GET,
aAggPortDebugLastRxTime GET,
aAggPortDebugMuxState GET,
aAggPortDebugMuxReason GET,
aAggPortDebugActorChurnState GET,
aAggPortDebugPartnerChurnState GET,
aAggPortDebugActorChurnCount GET,
aAggPortDebugPartnerChurnCount GET,
aAggPortDebugActorSyncTransitionCount GET,
aAggPortDebugPartnerSyncTransitionCount GET,

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aAggPortDebugActorChangeCount GET,
aAggPortDebugPartnerChangeCount GET;
REGISTERED AS
{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) pAggPortDebugInformation(24)};
PRESENT IF The Aggregation Port Debug Information package is supported;
;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) oAggPortDebugInformation(13)};

nbAggPortDebugInformation NAME BINDING

SUBORDINATE OBJECT CLASS oAggPortDebugInformation;
NAMED BY SUPERIOR OBJECT CLASS oAggregationPort;
WITH ATTRIBUTE aAggPortDebugInformationID
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) nbAggPortDebugInformation(23)};

30A.14.2 Aggregation Port Debug Information attributes

aAggPortDebugInformationID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggPortID;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortDebugInformationID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugInformationID(166)};

bAggPortDebugInformationID BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.4.1.1;

aAggPortDebugRxState ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.RxState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortDebugRxState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugRxState(167)};

bAggPortDebugRxState BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.4.1.2;

aAggPortDebugLastRxTime ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.Integer32;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortDebugLastRxTime;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugLastRxTime(168)};

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bAggPortDebugLastRxTime BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.4.1.3;

aAggPortDebugMuxState ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MuxState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortDebugMuxState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugMuxState(169)};

bAggPortDebugMuxState BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.4.1.4;

aAggPortDebugMuxReason ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.DescriptionString;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortDebugMuxReason;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugMuxReason(170)};

bAggPortDebugMuxReason BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.4.1.5;

aAggPortDebugActorChurnState ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.ChurnState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortDebugActorChurnState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugActorChurnState(171)};

bAggPortDebugActorChurnState BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.4.1.6;

aAggPortDebugPartnerChurnState ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.ChurnState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortDebugPartnerChurnState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugPartnerChurnState(172)};

bAggPortDebugPartnerChurnState BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.4.1.7;

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aAggPortDebugActorChurnCount ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortDebugActorChurnCount;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugActorChurnCount(173)};

bAggPortDebugActorChurnCount BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.8.

NOTE—This counter has a maximum increment rate of 5 counts per second.;

aAggPortDebugPartnerChurnCount ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortDebugPartnerChurnCount;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugPartnerChurnCount(174)};

bAggPortDebugPartnerChurnCount BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.9.

NOTE—This counter has a maximum increment rate of 5 counts per second.;

aAggPortDebugActorSyncTransitionCount ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortDebugActorSyncTransitionCount;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugActorSyncTransitionCount(175)};

bAggPortDebugActorSyncTransitionCount BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.10.

NOTE—This counter has a maximum increment rate of 5 counts per second.;

aAggPortDebugPartnerSyncTransitionCount ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortDebugPartnerSyncTransitionCount;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugPartnerSyncTransitionCount(176)};

bAggPortDebugPartnerSyncTransitionCount BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.11.

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NOTE—This counter has a maximum increment rate of 5 counts per second.;

aAggPortDebugActorChangeCount ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortDebugActorChangeCount;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugActorChangeCount(177)};

bAggPortDebugActorChangeCount BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.12.

NOTE—This counter has a maximum increment rate of 5 counts per second.;

aAggPortDebugPartnerChangeCount ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortDebugPartnerChangeCount;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugPartnerChangeCount(178)};

bAggPortDebugPartnerChangeCount BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.13.

NOTE—This counter has a maximum increment rate of 5 counts per second.;

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Annex 30B

(normative)

GDMO and ASN.1 definitions for management

30B.1 Common attributes template

This template defines generic facilities that are used in the standard.

aCMCounter ATTRIBUTE

DERIVED FROM "ISO/IEC 10165-5":genericWrappingCounter;
BEHAVIOUR bCMCounter;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) cmCounter(88)};

bCMCounter BEHAVIOUR

DEFINED AS Wraps at one of two sizes. Size is conditional.
Wraps at 32 bits, that is this counter reaches its maximum value at $2^{32}-1$ (i.e., approximately 4.294×10^{9}) and then rolls over to zero on the next increment, if maximum increment rate from zero causes a rollover in 58 min or more.
Wraps at 64 bits, that is this counter reaches its maximum value at $2^{64}-1$ (i.e., approximately $1.844\ldots \times 10^{19}$) and then rolls over to zero on the next increment, if maximum increment rate from zero would cause a 32 bit counter to roll over in less than 58 min.
The counter that this is derived from initializes to zero. Initialization to zero is not a requirement of this standard;

30B.2 ASN.1 module for CSMA/CD managed objects

This ASN.1 module defines the ASN.1 types and subtypes that are referred to immediately after the WITH ATTRIBUTE SYNTAX construct in this clause's uses of the attribute template defined in ISO/IEC 10165-4: 1992, Guidelines for the definition of managed objects (GDMO).

IEEE802Dot3-MgmtAttributeModule {iso(1) member-body(2) us(840) ieee802dot3(10006) global(1) asn1Module(2) commonDefinitions(0) version(2)} DEFINITIONS IMPLICIT TAGS::= BEGIN

EXPORTS--*everything*

IMPORTS--*implicitly imports ISO 8824: 1990*

```
MACAddress
    FROM IEEE802CommonDefinitions
    {iso(1) member-body(2) us(840) ieee802dot1partF(10011)
    asn1Module(2) commonDefinitions(0) version1(0)};
AdminState::= ENUMERATED {
    other                   (1),    --undefined
```


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```
        unknown             (2),    --initializing, true state not yet known
        operational         (3),    --powered and connected
        standby             (4),    --inactive but on
        shutdown            (5)     --similar to power down
        }
AggDataRate ::= INTEGER (0..2^32-1)--The data rate of an Aggregation

AggID ::= INTEGER (0..2^32-1)

AggOrInd ::= BOOLEAN

AggPortID ::= INTEGER (0..2^32-1)

AggPortList ::= SEQUENCE OF AggPortID

AggPortState ::= BIT STRING (SIZE (1..8))

AggState ::= ENUMERATED {
        up                  (0),    --operational
        down                (1)     --disabled
        }

AttemptArray::= SEQUENCE OF aCMCounter--array [1..attempt limit - 1]

AutoNegAdminState::= ENUMERATED {
        disabled            (1),
        enabled             (2)
        }

AutoNegAutoConfig::= ENUMERATED {
        other               (1),
        configuring         (2),
        complete            (3),
        disabled            (4),
        parallel detect fail (5)
        }

AutoNegRemoteSignalingDetect::= ENUMERATED {
        detected            (1),
        notdetected         (2)
        }

AutoNegSelector::= ENUMERATED {
        other               (1),    --undefined
        ethernet            (2),    --802.3
        isoethernet         (3),    --802.9
        tokenring           (4)     --802.5
        }

AutoNegSelectorList::= SEQUENCE OF AutoNegSelector
```

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```
AutoNegTechnology::= ENUMERATED {
    global              (0),    --reserved for future use.
    other               (1),    --undefined
    unknown             (2),    --initializing, true ability not yet known.
    10BASE-T            (14),   --10BASE-T as defined in Clause 14
    10BASE-TFD          (142),  --Full duplex 10BASE-T as defined in Clauses 14 and 31
    100BASE-T4          (23),   --100BASE-T4 as defined in Clause 23
    100BASE-TX          (25),   --100BASE-TX as defined in Clause 25
    100BASE-TXFD        (252),  --Full duplex 100BASE-TX as defined in Clauses 25 and 31
    FDX PAUSE           (312),  --PAUSE operation for full duplex links as defined in
    Annex 31B
    FDX APAUSE          (313),  --Asymmetric PAUSE operation for full duplex links as defined
                                 in Clause 37 and Annex 31B
    FDX SPAUSE          (314),  --Symmetric PAUSE operation for full duplex links as defined
                                 in Clause 37 and Annex 31B
    FDX BPAUSE          (315),  --Asymmetric and Symmetric PAUSE operation for full duplex
                                 links as defined in Clause 37 and Annex 31B
    100BASE-T2          (32),   --100BASE-T2 as defined in Clause 32
    100BASE-T2FD        (322),  --Full duplex 100BASE-T2 as defined in Clauses 31 and 32
    1000BASE-X          (36),   --1000BASE-X as defined in Clause 36
    1000BASE-XFD        (362),  --Full duplex 1000BASE-X as defined in Clause 36
    1000BASE-T          (40),   --1000BASE-T UTP PHY as defined in Clause 36
    1000BASE-TFD        (402),  --Full duplex 1000BASE-T UTP PHY to be defined in
    Clause 36
    Rem Fault1          (37),   --Remote fault bit 1 (RF1) as specified in Clause 37
    Rem Fault2          (372),  --Remote fault bit 2 (RF1) as specified in Clause 37
    isoethernet         (8029)  --802.9 ISLAN-16T
    }

AutoNegTechnologyList::= SEQUENCE OF AutoNegTechnology

AutoPartitionState::= ENUMERATED {
    autoPartitioned     (1),
    notAutoPartitioned  (2)
    }


BbandFrequency::= SEQUENCE {
    xmitCarrierFrequency    [1]     INTEGER , --Frequency in MHz times 4 (250 kHz resolution)
    translationFrequency    [2]     INTEGER   --Frequency in MHz times 4 (250 kHz resolution)
    }


BbandXmitRcvSplitType::= ENUMERATED {
    other               (1),    --undefined
    single              (2),    --single-cable system
    dual                (3)     --dual-cable system, offset normally zero
    }


BitString::= BIT STRING (SIZE (1..1024))


ChurnState ::= ENUMERATED {
    noChurn             (0),    --NO_ACTOR/PARTNER_CHURN
                                --or ACTOR/PARTNER_CHURN_MONITOR
    churn               (1)     --ACTOR/PARTNER_CHURN
                        }


CollectorMaxDelay ::= INTEGER   --16 bit value, tens of microseconds
                                --(max = 0.65535 seconds)


DescriptionString ::= PrintableString (SIZE 0..255))
```


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```
DuplexValues::= ENUMERATED {
    half duplex         (1),    --capable of operating in half duplex mode
    full duplex         (2),    --capable of operating in full duplex mode
    unknown             (3)     --unknown duplex capability
    }

Integer32 ::= INTEGER (0..2^32-1)    --32 bit value

Jabber::= SEQUENCE {
    jabberFlag          [1]     JabberFlag,
    jabberCounter       [2]     JabberCounter
    }

JabberFlag::= ENUMERATED {
    other               (1),    --undefined
    unknown             (2),    --initializing, true state not yet known
    normal              (3),    --state is true or normal
    fault               (4)     --state is false, fault or abnormal
    }

JabberCounter::= INTEGER (0..2^32 –1)

KeyValue ::= INTEGER (0..2^16-1)    --16 bit value; range 0-65535

LACPActivity ::= ENUMERATED {
    active              (0),    --Port is Active LACP
    passive             (1)     --Port is Passive LACP
    }

LACPTimeout ::= ENUMERATED {
    short               (0),    --Timeouts are Short
    long                (1)     --Timeouts are Long
    }

LinkDelayAllowance::= INTEGER (0..2^32–1)

MACControlFunctions::= ENUMERATED {
    PAUSE               (312)   --PAUSE command implemented
    }

MACControlFunctionsList::= SEQUENCE OF MACControlFunctions

MACCapabilitiesList::= SEQUENCE OF DuplexValues

MauTypeList::= SEQUENCE OF TypeValue

MediaAvailState::= ENUMERATED {
    other               (1),    --undefined
    unknown             (2),    --initializing, true state not yet known
    available           (3),    --link or light normal, loopback normal
    not available       (4),    --link loss or low light, no loopback
```

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```
        remote fault            (5),    --remote fault with no detail
        invalid signal          (6),    --invalid signal, applies only to 10BASE-FB
        remote jabber           (7),    --remote fault, reason known to be jabber
        remote link loss        (8),    --remote fault, reason known to be far-end link loss
        remote test             (9),    --remote fault, reason known to be test
        offline                 (10),   --offline, applies only to Clause 37 Auto-Negotiation
        auto neg error          (11)    --Auto-Negotiation error, applies only to Clause 37
                                        Auto- Negotiation
        }

MIIDetect::= ENUMERATED {
        unknown                 (1),
        presentNothingConnected(2),
        presentConnected        (3),
        absent                  (4)
        }

MulticastAddressList::= SEQUENCE OF MACAddress

MuxState ::= ENUMERATED {
        detached                (0),    --DETACHED
        waiting                 (1),    --WAITING
        attached                (2),    --ATTACHED
        collecting              (3),    --COLLECTING
        distributing            (4),    --DISTRIBUTING
        collecting_distributing (5)     --COLLECTING_DISTRIBUTING
        }

NotificationEnable ::= ENUMERATED {
        enabled                 (0),    --Notifications enabled
        disabled                (1)     --Notifications disabled

OneOfName::= INTEGER (1..1024)

PhyTypeList::= SEQUENCE OF PhyTypeValue

PhyTypeValue::= ENUMERATED {
        other                   (1),    --undefined
        unknown                 (2),    --initializing, true state or type not yet known
        none                    (3),    --MII present and nothing connected
        10 Mb/s                 (7),    --Clause 7 10 Mb/s Manchester
        100BASE-T4              (23),   --Clause 23 100 Mb/s 8B/6T
        100BASE-X               (24),   --Clause 24 100 Mb/s 4B/5B
        100BASE-T2              (32),   --Clause 32 100 Mb/s PAM5x5
        1000BASE-X              (36),   --Clause 36 1000 Mb/s 8B/10B
        1000BASE-T              (40)    --Clause 40 1000 Mb/s 4D-PAM5
        }

PortAdminState::= ENUMERATED {
        disabled                (1),
        enabled                 (2)
        }

PortNumber ::= INTEGER (0..2^16-1)
```


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```
PriorityValue ::= INTEGER (0..2^16-1) --16 bits

RegisterEight::= INTEGER (0..255)

RepeaterHealthData::= OCTET STRING (SIZE (0..255))

RepeaterHealthInfo::= SEQUENCE {
    repeaterHealthState     [1]     RepeaterHealthState,
    repeaterHealthText      [2]     RepeaterHealthText  OPTIONAL,
    repeaterHealthData      [3]     RepeaterHealthData  OPTIONAL
    }

RepeaterHealthState::= ENUMERATED {
    other                   (1),    --undefined or unknown
    ok                      (2),    --no known failures
    repeaterFailure         (3),    --known to have a repeater-related failure
    groupFailure            (4),    --known to have a group-related failure
    portFailure             (5),    --known to have a port-related failure
    generalFailure          (6)     --has a failure condition, unspecified type
    }

RepeaterType::= ENUMERATED {
    other                   (1),    --See 30.2.5:
    unknown                 (2),    --initializing, true state or type not yet known
    10 Mb/s                 (9),    --Clause 9 10 Mb/s Baseband repeater
    100 Mb/sClassI          (271),  --Clause 27 class I 100 Mb/s Baseband repeater
    100 Mb/sClassII         (272),  --Clause 27 class II 100 Mb/s Baseband repeater
    1000 Mb/s               (41),   --Clause 41 1000 Mb/s Baseband repeater
    802.9a                  (99)    --Integrated services repeater
    }

RepeaterHealthText::= PrintableString (SIZE (0..255))

RxState ::= ENUMERATED {
    current                 (0),
    expired                 (1),
    defaulted               (2),
    initialize              (3),
    lacpDisabled            (4),
    portDisabled            (5)
    }

TrueFalse::= BOOLEAN

TypeList::= SEQUENCE OF TypeValue

TypeValue::= ENUMERATED {
    global                  (0),    --undefined
    other                   (1),    --undefined
    unknown                 (2),    --initializing, true state not yet known
    AUI                     (7),    --no internal MAU, view from AUI
    10BASE5                 (8),    --Thick coax MAU as specified in Clause 8
    FOIRL                   (9),    --FOIRL MAU as specified in 9.9
    10BASE2                 (10),   --Thin coax MAU as specified in Clause 10
```

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```
        10BROAD36       (11),   --Broadband DTE MAU as specified in Clause 11
        10BASE-T        (14),   --UTP MAU as specified in Clause 14, duplex mode
                                  unknown
        10BASE-THD      (141),  --UTP MAU as specified in Clause 14, half duplex mode
        10BASE-TFD      (142),  --UTP MAU as specified in Clause 14 , full duplex mode
        10BASE-FP       (16),   --Passive fiber MAU as specified in Clause 16
        10BASE-FB       (17),   --Synchronous fiber MAU as specified in Clause 17
        10BASE-FL       (18),   --Asynchronous fiber MAU as specified in Clause 18,
                                  duplex mode unknown
        10BASE-FLHD     (181),  --Asynchronous fiber MAU as specified in Clause 18,
                                  half duplex mode
        10BASE-FLFD     (182),  --Asynchronous fiber MAU as specified in Clause 18,
                                  full duplex mode
        100BASE-T4      (23),   --Four-pair Category 3 UTP as specified in Clause 23
        100BASE-TX      (25),   --Two-pair Category 5 UTP as specified in Clause 25, duplex
                                  mode unknown
        100BASE-TXHD    (251),  --Two-pair Category 5 UTP as specified in Clause 25, half
                                  duplex mode
        100BASE-TXFD    (252),  --Two-pair Category 5 UTP as specified in Clause 25, full
                                  duplex mode
        100BASE-FX      (26),   --X fiber over PMD as specified in Clause 26, duplex mode
                                  unknown
        100BASE-FXHD    (261),  --X fiber over PMD as specified in Clause 26, half duplex mode
        100BASE-FXFD    (262),  --X fiber over PMD as specified in Clause 26, full duplex mode
        100BASE-T2      (32),   --Two-pair Category 3 UTP as specified in Clause 32, duplex
                                  mode unknown
        100BASE-T2HD    (321),  --Two-pair Category 3 UTP as specified in Clause 32, half
                                  duplex mode
        100BASE-T2FD    (322),  --Two-pair Category 3 UTP as specified in Clause 32, full
                                  duplex mode
        1000BASE-X      (36),   --X PCS/PMA as specified in Clause 36 over unknown
                                  PMD, duplex mode unknown
        1000BASE-XHD    (361),  --X  PCS/PMA as specified in Clause 36 over unknown
                                  PMD, half duplex mode
        1000BASE-XFD    (362),  --X PCS/PMA as specified in Clause 36 over unknown
                                   PMD, full duplex mode
        1000BASE-LX     (381),  --X fiber over long-wavelength laser PMD as specified in
                                  Clause 38, duplex mode unknown
        1000BASE-LXHD   (382),  --X fiber over long-wavelength laser PMD as specified in
                                  Clause 38, half duplex mode
        1000BASE-LXFD   (383),  --X fiber over long-wavelength laser PMD as specified in
                                  Clause 38, full duplex mode
        1000BASE-SX     (384),  --X fiber over short-wavelength laser PMD as specified in
                                  Clause 38, duplex mode unknown
        1000BASE-SXHD   (385),  --X fiber over short-wavelength laser PMD as specified in
                                  Clause 38, half duplex mode
        1000BASE-SXFD   (386),  --X fiber over short-wavelength laser PMD as specified in
                                  Clause 38, full duplex mode
        1000BASE-CX     (39),   --X copper over 150-Ohm balanced cable PMD as specified in
                                  Clause 39, duplex mode unknown
        1000BASE-CXHD   (391),  --X copper over 150-Ohm balanced cable PMD as specified in
                                  Clause 39, half duplex mode
        1000BASE-CXFD   (392),  --X copper over 150-Ohm balanced cable PMD as specified in
                                  Clause 39, full duplex mode
        1000BASE-T      (40),   --Four-pair Category 5 UTP PHY as specified in
                                  Clause 40, duplex mode unknown
        1000BASE-THD    (401),  --Four-pair Category 5 UTP PHY as specified in
                                  Clause 40, half duplex mode
        1000BASE-TFD    (402),  --Four-pair Category 5 UTP PHY as specified in
                                  Clause 40, full duplex mode
        802.9a          (99)    --Integrated services MAU as specified in IEEE Std 802.9
                                  ISLAN-16T
        }
END
```


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Annex 30C

(normative)

SNMP MIB definitions for Link Aggregation

30C.1 Introduction

This annex defines a portion of the Management Information Base (MIB) for use with network management protocols in TCP/IP based internets. In particular it defines objects for managing the operation of the Link Aggregation sublayer, based on the specification of Link Aggregation contained in Clause 43. This annex includes an MIB module that is SNMPv2 SMI compliant.

30C.2 The SNMP Management Framework

The SNMP Management Framework presently consists of five major components

a) An overall architecture, described in RFC 2271.
b) Mechanisms for describing and naming objects and events for the purpose of management. The first version of this Structure of Management Information (SMI) is called SMIv1 and is described in RFC 1155, RFC 1212, and RFC 1215. The second version, called SMIv2, is described in RFC 1902, RFC 1903, and RFC 1904.
c) Message protocols for transferring management information. The first version of the SNMP message protocol is called SNMPv1 and is described in RFC 1157. A second version of the SNMP message protocol, which is not an Internet standards track protocol, is called SNMPv2c and is described in RFC 1901 and RFC 1906. The third version of the message protocol is called SNMPv3 and is described in RFC 1906, RFC 2272, and RFC 2274.
d) Protocol operations for accessing management information. The first set of protocol operations and associated PDU formats is described in RFC 1157. A second set of protocol operations and associated PDU formats is described in RFC 1905.
e) A set of fundamental applications described in RFC 2273 and the view-based access control mechanism described in RFC 2275.

Managed objects are accessed via a virtual information store, termed the Management Information Base or MIB. Objects in the MIB are defined using the mechanisms defined in the SMI.

This annex specifies an MIB module that is compliant to the SMIv2. An MIB conforming to the SMIv1 can be produced through the appropriate translations. The resulting translated MIB must be semantically equivalent, except where objects or events are omitted because no translation is possible (use of Counter64). Some machine-readable information in SMIv2 will be converted into textual descriptions in SMIv1 during the translation process. However, this loss of machine-readable information is not considered to change the semantics of the MIB.

30C.3 Security considerations

There are a number of management objects defined in this MIB that have a MAX-ACCESS clause of readwrite and/or read-create. Such objects may be considered sensitive or vulnerable in some network environments. The support for SET operations in a non-secure environment can have a negative effect on network operations.

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SNMPv1 by itself is not a secure environment. Even if the network itself is secure (e.g., by using IPSec), there is no control as to who on the secure network is allowed to access (read/change/create/delete) the objects in this MIB.

It is recommended that the implementors consider the security features as provided by the SNMPv3 framework. Specifically, the use of the User-based Security Model RFC 2274 and the View-based Access Control Model RFC 2275 is recommended. It then becomes a user responsibility to ensure that the SNMP entity giving access to an instance of this MIB is properly configured to give access only to those principals (users) that have legitimate rights to access(read/change/create/delete) them, as appropriate.

30C.4 Structure of the MIB

A single MIB module is defined in this annex. Objects in the MIB are arranged into groups. Each group is organized as a set of related objects. The overall structure and assignment of objects to their groups is shown in the following subclauses.

30C.4.1 Relationship to the managed objects defined in Clause 30

This subclause contains cross-references to the objects defined in Clause 30. Table 30C–1 contains cross references for the MIB objects defined in this annex. Table 30C–2 contains definitions of ifTable elements, as defined in RFC 2233, for an Aggregator. These table elements are cross referenced to the corresponding definitions in Clause 30.

Table 30C–1—Managed object cross reference table

Definition in Clause 30	MIB object
30.7.1.1.1 aAggID	ifIndex value (see RFC 2233)
30.7.1.1.4 aAggActorSystemID	dot3adAggActorSystemID
30.7.1.1.5 aAggActorSystemPriority	dot3adAggActorSystemPriority
30.7.1.1.6 aAggAggregateOrIndividual	dot3adAggAggregateOrIndividual
30.7.1.1.7 aAggActorAdminKey	dot3adAggActorAdminKey
30.7.1.1.8 aAggActorOperKey	dot3adAggActorOperKey
30.7.1.1.10 aAggPartnerSystemID	dot3adAggPartnerSystemID
30.7.1.1.11 aAggPartnerSystemPriority	dot3adAggPartnerSystemPriority
30.7.1.1.12 aAggPartnerOperKey	dot3adAggPartnerOperKey
30.7.1.1.30 aAggPortList	dot3adAggPortListTable
30.7.1.1.32 aAggCollectorMaxDelay	dot3adAggCollectorMaxDelay
30.7.2.1.1 aAggPortID	ifIndex value (see RFC 2233)
30.7.2.1.2 aAggPortActorSystemPriority	dot3adAggPortActorSystemPriority

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Table 30C–1—Managed object cross reference table *(continued)*

Definition in Clause 30	MIB object
30.7.2.1.3 aAggPortActorSystemID	dot3adAggPortActorSystemID
30.7.2.1.4 aAggPortActorAdminKey	dot3adAggPortActorAdminKey
30.7.2.1.5 aAggPortActorOperKey	dot3adAggPortActorOperKey
30.7.2.1.6 aAggPortPartnerAdminSystemPriority	dot3adAggPortPartnerAdminSystemPriority
30.7.2.1.7 aAggPortPartnerOperSystemPriority	dot3adAggPortPartnerOperSystemPriority
30.7.2.1.8 aAggPortPartnerAdminSystemID	dot3adAggPortPartnerAdminSystemID
30.7.2.1.9 aAggPortPartnerOperSystemID	dot3adAggPortPartnerOperSystemID
30.7.2.1.10 aAggPortPartnerAdminKey	dot3adAggPortPartnerAdminKey
30.7.2.1.11 aAggPortPartnerOperKey	dot3adAggPortPartnerOperKey
30.7.2.1.12 aAggPortSelectedAggID	dot3adAggPortSelectedAggID
30.7.2.1.13 aAggPortAttachedAggID	dot3adAggPortAttachedAggID
30.7.2.1.14 aAggPortActorPort	dot3adAggPortActorPort
30.7.2.1.15 aAggPortActorPortPriority	dot3adAggPortActorPortPriority
30.7.2.1.16 aAggPortPartnerAdminPort	dot3adAggPortPartnerAdminPort
30.7.2.1.17 aAggPortPartnerOperPort	dot3adAggPortPartnerOperPort
30.7.2.1.18 aAggPortPartnerAdminPortPriority	dot3adAggPortPartnerAdminPortPriority
30.7.2.1.19 aAggPortPartnerOperPortPriority	dot3adAggPortPartnerOperPortPriority
30.7.2.1.20 aAggPortActorAdminState	dot3adAggPortActorAdminState
30.7.2.1.21 aAggPortActorOperState	dot3adAggPortActorOperState
30.7.2.1.22 aAggPortPartnerAdminState	dot3adAggPortPartnerAdminState
30.7.2.1.23 aAggPortPartnerOperState	dot3adAggPortPartnerOperState
30.7.2.1.24 aAggPortAggregateOrIndividual	dot3adAggPortAggregateOrIndividual
30.7.3.1.1 aAggPortStatsID	ifIndex value (see RFC 2233) of the port
30.7.3.1.2 aAggPortStatsLACPDUsRx	dot3adAggPortStatsLACPDUsRx
30.7.3.1.3 aAggPortStatsMarkerPDUsRx	dot3adAggPortStatsMarkerPDUsRx
30.7.3.1.4 aAggPortStatsMarkerResponsePDUsRx	dot3adAggPortStatsMarkerResponsePDUsRx
30.7.3.1.5 aAggPortStatsUnknownRx	dot3adAggPortStatsUnknownRx

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Table 30C–1—Managed object cross reference table *(continued)*

Definition in Clause 30	MIB object
30.7.3.1.6 aAggPortStatsIllegalRx	dot3adAggPortStatsIllegalRx
30.7.3.1.7 aAggPortStatsLACPDUsTx	dot3adAggPortStatsLACPDUsTx
30.7.3.1.8 aAggPortStatsMarkerPDUsTx	dot3adAggPortStatsMarkerPDUsTx
30.7.3.1.9 aAggPortStatsMarkerResponsePDUsTx	dot3adAggPortStatsMarkerResponsePDUsTx
30.7.4.1.1 aAggPortDebugInformationID	ifIndex value (see RFC 2233) of the port
30.7.4.1.2 aAggPortDebugRxState	dot3adAggPortDebugRxState
30.7.4.1.3 aAggPortDebugLastRxTime	dot3adAggPortDebugLastRxTime
30.7.4.1.4 aAggPortDebugMuxState	dot3adAggPortDebugMuxState
30.7.4.1.5 aAggPortDebugMuxReason	dot3adAggPortDebugMuxReason
30.7.4.1.6 aAggPortDebugActorChurnState	dot3adAggPortDebugActorChurnState
30.7.4.1.7 aAggPortDebugPartnerChurnState	dot3adAggPortDebugPartnerChurnState
30.7.4.1.8 aAggPortDebugActorChurnCount	dot3adAggPortDebugActorChurnCount
30.7.4.1.9 aAggPortDebugPartnerChurnCount	dot3adAggPortDebugPartnerChurnCount
30.7.4.1.10 aAggPortDebugActorSyncTransitionCount	dot3adAggPortDebugActorSyncTransitionCount
30.7.4.1.11 aAggPortDebugPartnerSyncTransitionCount	dot3adAggPortDebugPartnerSyncTransitionCount
30.7.4.1.12 aAggPortDebugActorChangeCount	dot3adAggPortDebugActorChangeCount
30.7.4.1.13 aAggPortDebugPartnerChangeCount	dot3adAggPortDebugPartnerChangeCount

30C.4.2 The Aggregator Group

This group of objects, in combination with the ifTable entry for an Aggregator and the Aggregator Port List, provides the functionality of the Aggregator managed object class (30.7.1). The Aggregator Group provides the control elements necessary to configure an Aggregator, plus the statistical information necessary to monitor the behaviour of an Aggregator.

30C.4.3 The Aggregator Port List Group

This group of objects implements the functionality defined for the Aggregator Port List attribute (30.7.1.1.30).

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Table 30C–2—ifTable element definitions for an Aggregator

Object	Definition
ifIndex	A unique integer value is allocated to each Aggregator by the local System. Interpreted as defined in RFC 2233.
ifDescr	Interpreted as defined in RFC 2233 and as further refined in the definition of aAggDescription (30.7.1.1.2).
ifType	ieee8023adLag(161)[a].
ifMTU	The largest MAC Client SDU that can be carried by this Aggregator—1500 octets.
ifSpeed	The data rate of the Aggregation as defined for aAggDataRate (30.7.1.1.16).
ifPhysAddress	The individual MAC Address of the Aggregator as defined for aAggMACAddress (30.7.1.1.9).
ifAdminStatus	The administrative state of the Aggregator as defined for aAggAdminState (30.7.1.1.13).
ifOperStatus	The operational state of the Aggregator as defined for aAggOperState (30.7.1.1.14).
ifLastChange	Interpreted as defined in RFC 2233; see also the definition of aAggTimeOfLastOperChange (30.7.1.1.15).
ifInOctets	The total number of user data octets received by the aggregation, as defined for aAggOctetsRxOK (30.7.1.1.18).
ifInUcastPkts	The total number of unicast user data frames received by the aggregation. This value is calculated as the value of aAggFramesRxOK (30.7.1.1.20), less the values of aAggMulticastFramesRxOK (30.7.1.1.22) and aAggBroadcastFramesRxOK (30.7.1.1.24).
ifInNUcastPkts	Deprecated in RFC 2233.
ifInDiscards	The number of frames discarded on reception, as defined for aAggFramesDiscardedOnRx (30.7.1.1.26).
ifInErrors	The number of frames with reception errors, as defined for aAggFramesWithRxErrors (30.7.1.1.28).
ifInUnknownProtos	The number of unknown protocol frames discarded on reception, as defined for aAggUnknownProtocolFrames (30.7.1.1.29).
ifOutOctets	The total number of user data octets transmitted by the aggregation, as defined for aAggOctetsTxOK (30.7.1.1.17).
ifOutUcastPkts	The total number of unicast user data frames transmitted by the aggregation. This value is calculated as the value of aAggFramesTxOK (30.7.1.1.19), less the values of aAggMulticastFramesTxOK (30.7.1.1.21) and aAggBroadcastFramesTxOK (30.7.1.1.23).
ifOutNUcastPkts	Deprecated in RFC 2233.

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Table 30C–2—ifTable element definitions for an Aggregator *(continued)*

Object	Definition
ifOutDiscards	The number of frames discarded on transmission, as defined for aAggFrames-DiscardedOnTx (30.7.1.1.25).
ifOutErrors	The number of frames discarded due to transmission errors, as defined for aAggFramesWithTxErrors (30.7.1.1.27).
ifOutQLen	Deprecated in RFC 2233. Set to zero if present.
ifSpecific	Deprecated in RFC 2233. Set to { 0.0 } if present.
ifLinkUpDownTrapEnable	See the definition of aAggLinkUpDownNotificationEnable (30.7.1.1.31).
ifConnectorPresent	"FALSE."
ifHighSpeed	Set to zero.
ifName	The locally assigned textual name of the Aggregator, as defined for aAggName (30.7.1.1.3). Interpreted as defined in RFC 2233.
linkUp TRAP	See the definition of nAggLinkUpNotification (30.7.1.2.1).
linkDown TRAP	See the definition of nAggLinkDownNotification (30.7.1.2.2).

[a]Values of ifType are assigned by the Internet Assigned Numbers Authority (IANA). A directory of number assignments is maintained on their website, at URL: http://www.iana.org/numbers.html. The currently assigned ifType values can be found in the SMI Numbers (Network Management Parameters) section of that directory.

30C.4.4 The Aggregation Port Group

This group of objects provides the functionality of the Aggregation Port managed object class (30.7.2). The Aggregation Port Group provides the control elements necessary to configure a Port for Link Aggregation, plus the statistical information necessary to monitor the behavior of the port.

30C.4.5 The Aggregation Port Statistics Group

This group of objects provides the functionality of the Aggregation Port Statistics managed object class (30.7.3). The Aggregation Port Statistics Group provides additional statistical information related to LACP and Marker protocol activity on the port.

30C.4.6 The Aggregation Port Debug Group

This group of objects provides the functionality of the Aggregation Port Debug managed object class (30.7.4). The Aggregation Port Debug Group provides additional information related to the operation of LACP on the port; this information is primarily aimed at debugging the operation of the protocol and detecting fault conditions.

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30C.5 Relationship to other MIBs

It is assumed that a system implementing this MIB will also implement (at least) the "system" group defined in MIB-II defined in RFC 1213 and the "interfaces" group defined in RFC 2233.

30C.5.1 Relationship to the Interfaces MIB

RFC 2233, the Interface MIB Evolution, requires that any MIB that is an adjunct of the Interface MIB, clarify specific areas within the Interface MIB. These areas were intentionally left vague in RFC 2233 to avoid over constraining the MIB, thereby precluding management of certain media types.

Section 3.3 of RFC 2233 enumerates several areas that a media-specific MIB must clarify. Each of these areas is addressed in 30C.5.2 and 30C.5.3. The implementor is referred to RFC 2233 in order to understand the general intent of these areas.

In RFC 2233, the "interfaces" group is defined as being mandatory for all systems and contains information on an entity's interfaces, where each interface is thought of as being attached to a *subnetwork*. (Note that this term is not to be confused with *subnet,* which refers to an addressing partitioning scheme used in the Internet suite of protocols.) The term *segment* is sometimes used to refer to such a subnetwork.

Implicit in this MIB is the notion of Aggregators and Aggregation ports. Each of these Aggregators and Aggregation ports is associated with one interface of the "interfaces" group (one row in the ifTable) and each port is associated with a different interface.

Each Aggregator and Aggregation port is uniquely identified by an interface number (ifIndex). The ifIndex value assigned to a given Aggregation port is the same as the ifIndex value assigned to the MAC interface with which that Aggregation port is associated.

30C.5.2 Layering model

This annex assumes the interpretation of the Interfaces Group to be in accordance with RFC 2233, which states that the ifTable contains information on the managed resource's interfaces and that each sublayer below the internetwork layer of a network interface is considered an interface.

This annex recommends that, within an entity, aggregations that are instantiated as an entry in dot3adAggTable are also represented by an entry in ifTable.

Where an entity contains Link Aggregation entities that transmit and receive traffic to/from an aggregation, these should be represented in the ifTable as interfaces of type ieee8023adLag(161).

30C.5.3 ifStackTable

If the ifStackTable defined in RFC1573 is implemented, then

a) The relationship shown in the table has the property that an Aggregation is a higher interface relative to an Aggregation Port.
b) This relationship is read-only.

NOTE—The restriction stated here is intended to enforce a strict hierarchical relationship between Aggregations and Aggregation Ports, and to prevent those relationships from being modified. The read-only restriction does not apply to any other relationships that may be expressed in the ifStackTable.

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30C.5.4 ifRcvAddressTable

The ifRcvAddressTable contains all MAC Addresses, unicast, multicast, and broadcast, for which an interface can receive packets and forward them up to a higher layer entity for local consumption. An Aggregator has at least one such address.

30C.6 Definitions for Link Aggregation MIB

In the MIB definition[21] below, should there be any discrepancy between the DESCRIPTION text and the BEHAVIOUR DEFINED AS in the corresponding definition in Clause 30, the definition in Clause 30 shall take precedence.

NOTES

1—The ASCII for 30C.6 is available from http://www.ieee802.org/3/publication/index.html.[22]

```
IEEE8023-LAG-MIB DEFINITIONS ::= BEGIN


-- ------------------------------------------------------------
-- IEEE 802.3ad MIB
-- ------------------------------------------------------------


IMPORTS
    MODULE-IDENTITY, OBJECT-TYPE, Counter32, TimeTicks, BITS
        FROM SNMPv2-SMI
    DisplayString, MacAddress, TEXTUAL-CONVENTION, TruthValue
        FROM SNMPv2-TC
    MODULE-COMPLIANCE, OBJECT-GROUP
        FROM SNMPv2-CONF
    InterfaceIndex
        FROM IF-MIB
    PortList
        FROM Q-BRIDGE-MIB
    ;


lagMIB MODULE-IDENTITY
    LAST-UPDATED "9911220000Z"
    ORGANIZATION "IEEE 802.3ad Working Group"
    CONTACT-INFO
        " stds-802-3-trunking@majordomo.ieee.org"
    DESCRIPTION
        "The Link Aggregation module for managing IEEE 802.3ad."
    ::= { iso(1) member-body(2) us(840) ieee802dot3(10006) snmpmibs(300) linkagg(43)
      }


lagMIBObjects OBJECT IDENTIFIER ::= { lagMIB 1 }


-- ------------------------------------------------------------
```

[21]MIB definitions are available at http://www.ietf.org/.

[22]*Copyright release for SNMP MIB:* Users of this standard may freely reproduce the SNMP MIB in this annex so it can be used for its intended purpose.

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```
-- Textual Conventions
-- ----------------------------------------------------------


LacpKey ::= TEXTUAL-CONVENTION
    STATUS       current
    DESCRIPTION
        "The Actor or Partner Key value."
    SYNTAX      INTEGER (0..65535)


LacpState ::= TEXTUAL-CONVENTION
    STATUS      current
    DESCRIPTION
        "The Actor and Partner State values from the LACPDU."
    SYNTAX      BITS {
         lacpActivity(0),
         lacpTimeout(1),
         aggregation(2),
         synchronization(3),
         collecting(4),
         distributing(5),
         defaulted(6),
         expired(7)
                }


ChurnState ::= TEXTUAL-CONVENTION
    STATUS       current
    DESCRIPTION
        "The state of the Churn Detection machine."
    SYNTAX      INTEGER {
                    noChurn(1),
                    churn(2),
                    churnMonitor(3)
                }


-- ----------------------------------------------------------


-- ----------------------------------------------------------
-- groups in the LAG MIB
-- ----------------------------------------------------------


dot3adAgg OBJECT IDENTIFIER ::= { lagMIBObjects 1 }
dot3adAggPort OBJECT IDENTIFIER ::= { lagMIBObjects 2 }


-- ----------------------------------------------------------

-- ----------------------------------------------------------
-- The Tables Last Changed Object
-- ----------------------------------------------------------

dot3adTablesLastChanged OBJECT-TYPE
    SYNTAX      TimeTicks
    MAX-ACCESS read-only
```

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```
        STATUS      current
        DESCRIPTION
            "This object indicates the time of the
            most recent change to the dot3adAggTable,
            dot3adAggPortListTable, or
            dot3adAggPortTable."
    ::= { lagMIBObjects 3 }

    -- ----------------------------------------------------------
    -- The Aggregator Configuration Table
    -- ----------------------------------------------------------


    dot3adAggTable OBJECT-TYPE
        SYNTAX      SEQUENCE OF Dot3adAggEntry
        MAX-ACCESS  not-accessible
        STATUS      current
        DESCRIPTION
            "A table that contains information about every
            Aggregator that is associated with this System."
        REFERENCE
            "IEEE 802.3 Subclause 30.7.1"
        ::= { dot3adAgg 1 }


    dot3adAggEntry OBJECT-TYPE
        SYNTAX      Dot3adAggEntry
        MAX-ACCESS  not-accessible
        STATUS      current
        DESCRIPTION
            "A list of the Aggregator parameters. This is indexed
            by the ifIndex of the Aggregator."
        INDEX { dot3adAggIndex }
        ::= { dot3adAggTable 1 }


    Dot3adAggEntry ::=
        SEQUENCE {
            dot3adAggIndex
                InterfaceIndex,
            dot3adAggMACAddress
                MacAddress,
            dot3adAggActorSystemPriority
                INTEGER,
            dot3adAggActorSystemID
                MacAddress,
            dot3adAggAggregateOrIndividual
                TruthValue,
            dot3adAggActorAdminKey
                LacpKey,
            dot3adAggActorOperKey
                LacpKey,
            dot3adAggPartnerSystemID
                MacAddress,
            dot3adAggPartnerSystemPriority
                INTEGER,
            dot3adAggPartnerOperKey
                LacpKey,
            dot3adAggCollectorMaxDelay
```


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```
            INTEGER
    }


dot3adAggIndex OBJECT-TYPE
    SYNTAX       InterfaceIndex
    MAX-ACCESS   not-accessible
    STATUS       current
    DESCRIPTION
        "The unique identifier allocated to this Aggregator by the local System.
        This attribute identifies an Aggregator instance among the subordinate
        managed objects of the containing object. This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.1.1.1"
    ::= { dot3adAggEntry 1 }


dot3adAggMACAddress OBJECT-TYPE
    SYNTAX       MacAddress
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "A 6-octet read-only value carrying the individual
       MAC address assigned to the Aggregator."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.1.1.9"
    ::= { dot3adAggEntry 2 }


dot3adAggActorSystemPriority OBJECT-TYPE
    SYNTAX       INTEGER (0..65535)
    MAX-ACCESS   read-write
    STATUS       current
    DESCRIPTION
        "A 2-octet read-write value indicating the priority value
        associated with the Actor's System ID."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.1.1.5"
    ::= { dot3adAggEntry 3 }


dot3adAggActorSystemID OBJECT-TYPE
    SYNTAX       MacAddress
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "A 6-octet read-write MAC address value used as a unique
        identifier for the System that contains this Aggregator.
        NOTE-From the perspective of the Link Aggregation
        mechanisms described in Clause 43, only a single
        combination of Actor's System ID and System Priority are
        considered, and no distinction is made between the
        values of these parameters for an Aggregator and the
        port(s) that are associated with it; i.e., the protocol
        is described in terms of the operation of aggregation
        within a single System. However, the managed objects
        provided for the Aggregator and the port both allow
        management of these parameters. The result of this is to
        permit a single piece of equipment to be configured by
```

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```
        management to contain more than one System from the
        point of view of the operation of Link Aggregation. This
        may be of particular use in the configuration of
        equipment that has limited aggregation capability (see 43.6).”
    REFERENCE
        “IEEE 802.3 Subclause 30.7.1.1.4”
    ::= { dot3adAggEntry 4 }


    dot3adAggAggregateOrIndividual OBJECT-TYPE
        SYNTAX       TruthValue
        MAX-ACCESS   read-only
        STATUS       current
        DESCRIPTION
            “A read-only Boolean value indicating whether the
            Aggregator represents an Aggregate (‘TRUE’) or
            an Individual link (‘FALSE’).”
        REFERENCE
            “IEEE 802.3 Subclause 30.7.1.1.6”
        ::= { dot3adAggEntry 5 }


    dot3adAggActorAdminKey OBJECT-TYPE
        SYNTAX       LacpKey
        MAX-ACCESS   read-write
        STATUS       current
        DESCRIPTION
            “The current administrative value of the Key for the Aggregator.
            The administrative Key value may differ from the operational
            Key value for the reasons discussed in 43.6.2. This is a 16-bit,
            read-write value. The meaning of particular Key values
            is of local significance.”
        REFERENCE
            “IEEE 802.3 Subclause 30.7.1.1.7”
        ::= { dot3adAggEntry 6 }


    dot3adAggActorOperKey OBJECT-TYPE
        SYNTAX       LacpKey
        MAX-ACCESS   read-only
        STATUS       current
        DESCRIPTION
            “The current operational value of the Key for the Aggregator.
            The administrative Key value may differ from the operational
            Key value for the reasons discussed in 43.6.2.
            This is a 16-bit read-only value. The meaning of particular Key
            values is of local significance.
        REFERENCE
            “IEEE 802.3 Subclause 30.7.1.1.8”
        ::= { dot3adAggEntry 7 }


    dot3adAggPartnerSystemID OBJECT-TYPE
        SYNTAX       MacAddress
        MAX-ACCESS   read-only
        STATUS       current
        DESCRIPTION
            “A 6-octet read-only MAC address value consisting
            of the unique identifier for the current protocol Partner of
```


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```
        this Aggregator. A value of zero indicates that there is no
        known Partner. If the aggregation is manually configured, this
        System ID value will be a value assigned by the local System.”
    REFERENCE
        “IEEE 802.3 Subclause 30.7.1.1.10”
    ::= { dot3adAggEntry 8 }


dot3adAggPartnerSystemPriority OBJECT-TYPE
    SYNTAX       INTEGER (0..65535)
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        “A 2-octet read-only value that indicates the priority
        value associated with the Partner’s System ID. If the
        aggregation is manually configured, this System Priority value
        will be a value assigned by the local System.”
    REFERENCE
        “IEEE 802.3 Subclause 30.7.1.1.11”
    ::= { dot3adAggEntry 9 }


dot3adAggPartnerOperKey OBJECT-TYPE
    SYNTAX       LacpKey
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        “The current operational value of the Key for the
        Aggregator’s current protocol Partner. This is
        a 16-bit read-only value. If the aggregation is manually
        configured, this Key value will be a value assigned by the
        local System.”
    REFERENCE
        “IEEE 802.3 Subclause 30.7.1.1.12”
    ::= { dot3adAggEntry 10 }


dot3adAggCollectorMaxDelay OBJECT-TYPE
    SYNTAX       INTEGER (0..65535)
    MAX-ACCESS   read-write
    STATUS       current
    DESCRIPTION
        “The value of this 16-bit read-write attribute defines
        the maximum delay, in tens of microseconds, that
        may be imposed by the Frame Collector between
        receiving a frame from an Aggregator Parser, and
        either delivering the frame to its MAC Client or discarding
        the frame (see 43.2.3.1.1).”
    REFERENCE
        “IEEE 802.3 Subclause 30.7.1.1.32”
    ::= { dot3adAggEntry 11 }


-- ----------------------------------------------------------------
-- The Aggregation Port List Table
-- ----------------------------------------------------------------


dot3adAggPortListTable OBJECT-TYPE
```

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```
    SYNTAX      SEQUENCE OF Dot3adAggPortListEntry
    MAX-ACCESS  not-accessible
    STATUS      current
    DESCRIPTION
        "A table that contains a list of all the ports
        associated with each Aggregator."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.1.1.30"
    ::= { dot3adAgg 2 }


dot3adAggPortListEntry OBJECT-TYPE
    SYNTAX      Dot3adAggPortListEntry
    MAX-ACCESS  not-accessible
    STATUS      current
    DESCRIPTION
        "A list of the ports associated with a given Aggregator.
        This is indexed by the ifIndex of the Aggregator."
    INDEX { dot3adAggIndex }
    ::= { dot3adAggPortListTable 1 }


Dot3adAggPortListEntry ::=
    SEQUENCE {
        dot3adAggPortListPorts
            PortList
    }


dot3adAggPortListPorts OBJECT-TYPE
    SYNTAX      PortList
    MAX-ACCESS  read-only
    STATUS      current
    DESCRIPTION
        "The complete set of ports currently associated with
        this Aggregator.  Each bit set in this list represents
        an Actor Port member of this Link Aggregation."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.1.1.30"
    ::= { dot3adAggPortListEntry 1 }


-- ----------------------------------------------------------------
-- The Aggregation Port Table
-- ----------------------------------------------------------------


dot3adAggPortTable OBJECT-TYPE
    SYNTAX      SEQUENCE OF Dot3adAggPortEntry
    MAX-ACCESS  not-accessible
    STATUS      current
    DESCRIPTION
        "A table that contains Link Aggregation Control
        configuration information about every
        Aggregation Port associated with this device.
        A row appears in this table for each physical port."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.2"
    ::= { dot3adAggPort 1 }
```


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```
dot3adAggPortEntry OBJECT-TYPE
    SYNTAX      Dot3adAggPortEntry
    MAX-ACCESS  not-accessible
    STATUS      current
    DESCRIPTION
        “A list of Link Aggregation Control configuration
        parameters for each Aggregation Port on this device.”
    INDEX      { dot3adAggPortIndex }
    ::= { dot3adAggPortTable 1 }


Dot3adAggPortEntry ::=
    SEQUENCE {
        dot3adAggPortIndex
            InterfaceIndex,
        dot3adAggPortActorSystemPriority
            INTEGER,
        dot3adAggPortActorSystemID
            MacAddress,
        dot3adAggPortActorAdminKey
            LacpKey,
        dot3adAggPortActorOperKey
            LacpKey,
        dot3adAggPortPartnerAdminSystemPriority
            INTEGER,
        dot3adAggPortPartnerOperSystemPriority
            INTEGER,
        dot3adAggPortPartnerAdminSystemID
            MacAddress,
        dot3adAggPortPartnerOperSystemID
            MacAddress,
        dot3adAggPortPartnerAdminKey
            LacpKey,
        dot3adAggPortPartnerOperKey
            LacpKey,
        dot3adAggPortSelectedAggID
            InterfaceIndex,
        dot3adAggPortAttachedAggID
            InterfaceIndex,
        dot3adAggPortActorPort
            INTEGER,
        dot3adAggPortActorPortPriority
            INTEGER,
        dot3adAggPortPartnerAdminPort
            INTEGER,
        dot3adAggPortPartnerOperPort
            INTEGER,
        dot3adAggPortPartnerAdminPortPriority
            INTEGER,
        dot3adAggPortPartnerOperPortPriority
            INTEGER,
        dot3adAggPortActorAdminState
            LacpState,
        dot3adAggPortActorOperState
            LacpState,
        dot3adAggPortPartnerAdminState
            LacpState,
```

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```
        dot3adAggPortPartnerOperState
            LacpState,
        dot3adAggPortAggregateOrIndividual
            TruthValue
    }


dot3adAggPortIndex OBJECT-TYPE
    SYNTAX       InterfaceIndex
    MAX-ACCESS   not-accessible
    STATUS       current
    DESCRIPTION
        "The ifIndex of the port"
    REFERENCE
        "IEEE 802.3 Subclause 30.7.2.1.1"
    ::= { dot3adAggPortEntry 1 }


dot3adAggPortActorSystemPriority OBJECT-TYPE
    SYNTAX       INTEGER (0..65535)
    MAX-ACCESS   read-write
    STATUS       current
    DESCRIPTION
        "A 2-octet read-write value used to define the priority
        value associated with the Actor's System ID."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.2.1.2"
    ::= { dot3adAggPortEntry 2 }


dot3adAggPortActorSystemID OBJECT-TYPE
    SYNTAX       MacAddress
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "A 6-octet read-only MAC address value that defines
        the value of the System ID for the System that contains this
        Aggregation Port."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.2.1.3"
    ::= { dot3adAggPortEntry 3 }


dot3adAggPortActorAdminKey OBJECT-TYPE
    SYNTAX       LacpKey
    MAX-ACCESS   read-write
    STATUS       current
    DESCRIPTION
        "The current administrative value of the Key for the
        Aggregation Port. This is a 16-bit read-write value.
        The meaning of particular Key values is of local significance."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.2.1.4"
    ::= { dot3adAggPortEntry 4 }


dot3adAggPortActorOperKey OBJECT-TYPE
    SYNTAX       LacpKey
    MAX-ACCESS   read-write
```


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```
        STATUS       current
        DESCRIPTION
            "The current operational value of the Key for the
            Aggregation Port. This is a 16-bit read-only value.
            The meaning of particular Key values is of local significance."
        REFERENCE
            "IEEE 802.3 Subclause 30.7.2.1.5"
        ::= { dot3adAggPortEntry 5 }


    dot3adAggPortPartnerAdminSystemPriority OBJECT-TYPE
        SYNTAX       INTEGER (0..65535)
        MAX-ACCESS   read-write
        STATUS       current
        DESCRIPTION
            "A 2-octet read-write value used to define the administrative
            value of priority associated with the Partner's System ID. The
            assigned value is used, along with the value of
            aAggPortPartnerAdminSystemID, aAggPortPartnerAdminKey,
            aAggPortPartnerAdminPort, and aAggPortPartnerAdminPortPriority,
            in order to achieve manually configured aggregation."
        REFERENCE
            "IEEE 802.3 Subclause 30.7.2.1.7"
        ::= { dot3adAggPortEntry 6 }


    dot3adAggPortPartnerOperSystemPriority OBJECT-TYPE
        SYNTAX       INTEGER (0..65535)
        MAX-ACCESS   read-only
        STATUS       current
        DESCRIPTION
            "A 2-octet read-only value indicating the operational value
            of priority associated with the Partner's System ID. The
            value of this attribute may contain the manually configured value
            carried in aAggPortPartnerAdminSystemPriority
            if there is no protocol Partner."
        REFERENCE
            "IEEE 802.3 Subclause 30.7.2.1.7"
        ::= { dot3adAggPortEntry 7 }


    dot3adAggPortPartnerAdminSystemID OBJECT-TYPE
        SYNTAX       MacAddress
        MAX-ACCESS   read-write
        STATUS       current
        DESCRIPTION
            "A 6-octet read-write MACAddress value representing
            the administrative value of the Aggregation Port's protocol
            Partner's System ID. The assigned value is used, along with
            the value of aAggPortPartnerAdminSystemPriority,
            aAggPortPartnerAdminKey, aAggPortPartnerAdminPort,
            and aAggPortPartnerAdminPortPriority, in order to
            achieve manually configured aggregation."
        REFERENCE
            "IEEE 802.3 Subclause 30.7.2.1.8"
        ::= { dot3adAggPortEntry 8 }


    dot3adAggPortPartnerOperSystemID OBJECT-TYPE
```

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```
        SYNTAX       MacAddress
        MAX-ACCESS   read-only
        STATUS       current
        DESCRIPTION
            "A 6-octet read-only MACAddress value representing
            the current value of the Aggregation Port's protocol Partner's
            System ID. A value of zero indicates that there is no known
            protocol Partner. The value of this attribute may contain the
            manually configured value carried in
            aAggPortPartnerAdminSystemID if there is no protocol Partner."
        REFERENCE
            "IEEE 802.3 Subclause 30.7.2.1.9"
        ::= { dot3adAggPortEntry 9 }


    dot3adAggPortPartnerAdminKey OBJECT-TYPE
        SYNTAX       LacpKey
        MAX-ACCESS   read-write
        STATUS       current
        DESCRIPTION
            "The current administrative value of the Key for the
            protocol Partner. This is a 16-bit read-write value.
            The assigned value is used, along with the value of
            aAggPortPartnerAdminSystemPriority, aAggPortPartnerAdminSystemID,
            aAggPortPartnerAdminPort, and aAggPortPartnerAdminPortPriority,
            in order to achieve manually configured aggregation.
        REFERENCE
            "IEEE 802.3 Subclause 30.7.2.1.10"
        ::= { dot3adAggPortEntry 10 }


    dot3adAggPortPartnerOperKey OBJECT-TYPE
        SYNTAX       LacpKey
        MAX-ACCESS   read-only
        STATUS       current
        DESCRIPTION
            "The current operational value of the Key for the
            protocol Partner. The value of this attribute may contain
            the manually configured value carried in
            aAggPortPartnerAdminKey if there is no protocol Partner.
            This is a 16-bit read-only value."
        REFERENCE
            "IEEE 802.3 Subclause 30.7.2.1.11"
        ::= { dot3adAggPortEntry 11 }


    dot3adAggPortSelectedAggID OBJECT-TYPE
        SYNTAX       InterfaceIndex
        MAX-ACCESS   read-only
        STATUS       current
        DESCRIPTION
            "The identifier value of the Aggregator that this Aggregation
            Port has currently selected. Zero indicates that the Aggregation
            Port has not selected an Aggregator, either because it is in the
            process of detaching from an Aggregator or because there is no
            suitable Aggregator available for it to select. This value is read-only."
        REFERENCE
            "IEEE 802.3 Subclause 30.7.2.1.12"
        ::= { dot3adAggPortEntry 12 }
```


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```
dot3adAggPortAttachedAggID OBJECT-TYPE
    SYNTAX       InterfaceIndex
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "The identifier value of the Aggregator that this Aggregation
        Port is currently attached to. Zero indicates that the Aggregation
        Port is not currently attached to an Aggregator. This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.2.1.13"
    ::= { dot3adAggPortEntry 13 }


dot3adAggPortActorPort OBJECT-TYPE
    SYNTAX       INTEGER (0..65535)
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "The port number locally assigned to the Aggregation Port.
        The port number is communicated in LACPDUs as the
        Actor_Port. This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.2.1.14"
    ::= { dot3adAggPortEntry 14 }


dot3adAggPortActorPortPriority OBJECT-TYPE
    SYNTAX       INTEGER (0..65535)
    MAX-ACCESS   read-write
    STATUS       current
    DESCRIPTION
        "The priority value assigned to this Aggregation Port.
        This 16-bit value is read-write."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.2.1.15"
    ::= { dot3adAggPortEntry 15 }


dot3adAggPortPartnerAdminPort OBJECT-TYPE
    SYNTAX       INTEGER (0..65535)
    MAX-ACCESS   read-write
    STATUS       current
    DESCRIPTION
        "The current administrative value of the port number
        for the protocol Partner. This is a 16-bit read-write value.
        The assigned value is used, along with the value of
        aAggPortPartnerAdminSystemPriority,
        aAggPortPartnerAdminSystemID, aAggPortPartnerAdminKey,
        and aAggPortPartnerAdminPortPriority,
        in order to achieve manually configured aggregation."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.2.1.16"
    ::= { dot3adAggPortEntry 16 }


dot3adAggPortPartnerOperPort OBJECT-TYPE
    SYNTAX       INTEGER (0..65535)
```

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```
        MAX-ACCESS   read-only
        STATUS       current
        DESCRIPTION
            "The operational port number assigned to this Aggregation
            Port by the Aggregation Port's protocol Partner. The value
            of this attribute may contain the manually configured value
            carried in aAggPortPartnerAdminPort if there is no protocol
            Partner. This 16-bit value is read-only."
      REFERENCE
            "IEEE 802.3 Subclause 30.7.2.1.17"
        ::= { dot3adAggPortEntry 17 }


    dot3adAggPortPartnerAdminPortPriority OBJECT-TYPE
        SYNTAX       INTEGER (0..65535)
        MAX-ACCESS   read-write
        STATUS       current
        DESCRIPTION
            "The current administrative value of the port priority
            for the protocol Partner. This is a 16-bit read-write value.
            The assigned value is used, along with the value of
            aAggPortPartnerAdminSystemPriority, aAggPortPartnerAdminSystemID,
            aAggPortPartnerAdminKey, and aAggPortPartnerAdminPort,
            in order to achieve manually configured aggregation."
        REFERENCE
            "IEEE 802.3 Subclause 30.7.2.1.18"
        ::= { dot3adAggPortEntry 18 }


    dot3adAggPortPartnerOperPortPriority OBJECT-TYPE
        SYNTAX       INTEGER (0..65535)
        MAX-ACCESS   read-only
        STATUS       current
        DESCRIPTION
            "The priority value assigned to this Aggregation Port
            by the Partner. The value of this attribute may contain the
            manually configured value carried in
            aAggPortPartnerAdminPortPriority if there is no
            protocol Partner. This 16-bit value is read-only."
        REFERENCE
            "IEEE 802.3 Subclause 30.7.2.1.19"
        ::= { dot3adAggPortEntry 19 }


    dot3adAggPortActorAdminState OBJECT-TYPE
        SYNTAX       LacpState
        MAX-ACCESS   read-write
        STATUS       current
        DESCRIPTION
            "A string of 8 bits, corresponding to the administrative values
            of Actor_State (43.4.2) as transmitted by the Actor in LACPDUs.
            The first bit corresponds to bit 0 of Actor_State (LACP_Activity),
            the second bit corresponds to bit 1 (LACP_Timeout), the third bit
            corresponds to bit 2 (Aggregation), the fourth bit corresponds to
            bit 3 (Synchronization), the fifth bit corresponds to bit 4
            (Collecting), the sixth bit corresponds to bit 5 (Distributing),
            the seventh bit corresponds to bit 6 (Defaulted), and the eighth
            bit corresponds to bit 7 (Expired). These values allow
            administrative control over the values of LACP_Activity,
```


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```
        LACP_Timeout and Aggregation. This attribute value is read-write."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.2.1.20"
    ::= { dot3adAggPortEntry 20 }


dot3adAggPortActorOperState OBJECT-TYPE
    SYNTAX       LacpState
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "A string of 8 bits, corresponding to the current
        operational values of Actor_State as transmitted by the
        Actor in LACPDUs. The bit allocations are as defined in
        30.7.2.1.20. This attribute value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.2.1.21"
    ::= { dot3adAggPortEntry 21 }


dot3adAggPortPartnerAdminState OBJECT-TYPE
    SYNTAX       LacpState
    MAX-ACCESS   read-write
    STATUS       current
    DESCRIPTION
        "A string of 8 bits, corresponding to the current administrative
        value of Actor_State for the protocol Partner. The bit
        allocations are as defined in 30.7.2.1.20. This attribute value is
        read-write. The assigned value is used in order to achieve
        manually configured aggregation."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.2.1.22"
    ::= { dot3adAggPortEntry 22 }


dot3adAggPortPartnerOperState OBJECT-TYPE
    SYNTAX       LacpState
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "A string of 8 bits, corresponding to the current values of
        Actor_State in the most recently received LACPDU transmitted
        by the protocol Partner. The bit allocations are as defined in
        30.7.2.1.20. In the absence of an active protocol Partner, this
        value may reflect the manually configured value
        aAggPortPartnerAdminState. This attribute value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.2.1.23"
    ::= { dot3adAggPortEntry 23 }


dot3adAggPortAggregateOrIndividual OBJECT-TYPE
    SYNTAX       TruthValue
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "A read-only Boolean value indicating whether the
        Aggregation Port is able to Aggregate ('TRUE') or is
        only able to operate as an Individual link ('FALSE')."
```

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```
        REFERENCE
            "IEEE 802.3 Subclause 30.7.1.1.24"
        ::= { dot3adAggPortEntry 24 }


    -- ----------------------------------------------------------------
    -- LACP Statistics Table
    -- ----------------------------------------------------------------


    dot3adAggPortStatsTable OBJECT-TYPE
        SYNTAX      SEQUENCE OF Dot3adAggPortStatsEntry
        MAX-ACCESS  not-accessible
        STATUS      current
        DESCRIPTION
            "A table that contains Link Aggregation information
            about every port that is associated with this device.
            A row appears in this table for each physical port."
        REFERENCE
            "IEEE 802.3 Subclause 30.7.3"
        ::= { dot3adAggPort 2 }


    dot3adAggPortStatsEntry OBJECT-TYPE
        SYNTAX      Dot3adAggPortStatsEntry
        MAX-ACCESS  not-accessible
        STATUS      current
        DESCRIPTION
            "A list of Link Aggregation Control Protocol statistics
            for each port on this device."
        INDEX { dot3adAggPortIndex }
        ::= { dot3adAggPortStatsTable 1 }


    Dot3adAggPortStatsEntry ::=
        SEQUENCE {
            dot3adAggPortStatsLACPDUsRx
                Counter32,
            dot3adAggPortStatsMarkerPDUsRx
                Counter32,
            dot3adAggPortStatsMarkerResponsePDUsRx
                Counter32,
            dot3adAggPortStatsUnknownRx
                Counter32,
            dot3adAggPortStatsIllegalRx
                Counter32,
            dot3adAggPortStatsLACPDUsTx
                Counter32,
            dot3adAggPortStatsMarkerPDUsTx
                Counter32,
            dot3adAggPortStatsMarkerResponsePDUsTx
                Counter32
        }


    dot3adAggPortStatsLACPDUsRx OBJECT-TYPE
        SYNTAX       Counter32
        MAX-ACCESS   read-only
        STATUS       current
```


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```
        DESCRIPTION
            "The number of valid LACPDUs received on this
            Aggregation Port. This value is read-only."
        REFERENCE
            "IEEE 802.3 Subclause 30.7.3.1.2"
        ::= { dot3adAggPortStatsEntry 1 }


    dot3adAggPortStatsMarkerPDUsRx OBJECT-TYPE
        SYNTAX       Counter32
        MAX-ACCESS   read-only
        STATUS       current
        DESCRIPTION
            "The number of valid Marker PDUs received on this
            Aggregation Port. This value is read-only."
        REFERENCE
            "IEEE 802.3 Subclause 30.7.3.1.3"
        ::= { dot3adAggPortStatsEntry 2 }


    dot3adAggPortStatsMarkerResponsePDUsRx OBJECT-TYPE
        SYNTAX       Counter32
        MAX-ACCESS   read-only
        STATUS       current
        DESCRIPTION
            "The number of valid Marker Response PDUs received on this
            Aggregation Port. This value is read-only."
        REFERENCE
            "IEEE 802.3 Subclause 30.7.3.1.4"
        ::= { dot3adAggPortStatsEntry 3 }


    dot3adAggPortStatsUnknownRx OBJECT-TYPE
        SYNTAX       Counter32
        MAX-ACCESS   read-only
        STATUS       current
        DESCRIPTION
            "The number of frames received that either:
            - carry the Slow Protocols Ethernet Type value (43B.4),
              but contain an unknown PDU,  or:
            - are addressed to the Slow Protocols group MAC
              Address (43B.4), but do not carry the Slow Protocols Ethernet Type.
            This value is read-only."
        REFERENCE
            "IEEE 802.3 Subclause 30.7.3.1.5"
        ::= { dot3adAggPortStatsEntry 4 }


    dot3adAggPortStatsIllegalRx OBJECT-TYPE
        SYNTAX       Counter32
        MAX-ACCESS   read-only
        STATUS       current
        DESCRIPTION
            "The number of frames received that carry the Slow
            Protocols Ethernet Type value (43B.4), but contain a badly formed
            PDU or an illegal value of Protocol Subtype (43B.4).
            This value is read-only."
        REFERENCE
            "IEEE 802.3 Subclause 30.7.3.1.6"
```

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```
    ::= { dot3adAggPortStatsEntry 5 }


dot3adAggPortStatsLACPDUsTx OBJECT-TYPE
    SYNTAX       Counter32
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "The number of LACPDUs transmitted on this
        Aggregation Port. This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.3.1.7"
    ::= { dot3adAggPortStatsEntry 6 }


dot3adAggPortStatsMarkerPDUsTx OBJECT-TYPE
    SYNTAX       Counter32
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "The number of Marker PDUs transmitted on this
        Aggregation Port. This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.3.1.8"
    ::= { dot3adAggPortStatsEntry 7 }


dot3adAggPortStatsMarkerResponsePDUsTx OBJECT-TYPE
    SYNTAX       Counter32
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "The number of Marker Response PDUs transmitted
        on this Aggregation Port. This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.3.1.9"
    ::= { dot3adAggPortStatsEntry 8 }


-- ----------------------------------------------------------------
-- LACP Debug Table
-- ----------------------------------------------------------------
dot3adAggPortDebugTable OBJECT-TYPE
    SYNTAX      SEQUENCE OF Dot3adAggPortDebugEntry
    MAX-ACCESS  not-accessible
    STATUS      current
    DESCRIPTION
        "A table that contains Link Aggregation debug
        information about every port that is associated with
        this device.  A row appears in this table for each
        physical port."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.4"
    ::= { dot3adAggPort 3 }


dot3adAggPortDebugEntry OBJECT-TYPE
    SYNTAX      Dot3adAggPortDebugEntry
    MAX-ACCESS  not-accessible
```


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```
        STATUS      current
        DESCRIPTION
            "A list of the debug parameters for a port."
        INDEX { dot3adAggPortIndex }
        ::= { dot3adAggPortDebugTable 1 }


    Dot3adAggPortDebugEntry ::=
        SEQUENCE {
            dot3adAggPortDebugRxState
                INTEGER,
            dot3adAggPortDebugLastRxTime
                TimeTicks,
            dot3adAggPortDebugMuxState
                INTEGER,
            dot3adAggPortDebugMuxReason
                DisplayString,
            dot3adAggPortDebugActorChurnState
                ChurnState,
            dot3adAggPortDebugPartnerChurnState
                ChurnState,
            dot3adAggPortDebugActorChurnCount
                Counter32,
            dot3adAggPortDebugPartnerChurnCount
                Counter32,
            dot3adAggPortDebugActorSyncTransitionCount
                Counter32,
            dot3adAggPortDebugPartnerSyncTransitionCount
                Counter32,
            dot3adAggPortDebugActorChangeCount
                Counter32,
            dot3adAggPortDebugPartnerChangeCount
                Counter32
        }


    dot3adAggPortDebugRxState OBJECT-TYPE
        SYNTAX       INTEGER {
                        current(1),
                        expired(2),
                        defaulted(3),
                        initialize(4),
                        lacpDisabled(5),
                        portDisabled(6)
                     }
        MAX-ACCESS   read-only
        STATUS       current
        DESCRIPTION
            "This attribute holds the value 'current' if the Receive
            state machine for the Aggregation Port is in the
            CURRENT state, 'expired' if the Receive state machine
            is in the EXPIRED state, 'defaulted' if the Receive state
            machine is in the DEFAULTED state, 'initialize' if the
            Receive state machine is in the INITIALIZE state,
            'lacpDisabled' if the Receive state machine is in the
            LACP_DISABLED state, or 'portDisabled' if the Receive
            state machine is in the PORT_DISABLED state.
            This value is read-only."
        REFERENCE
```

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```
        "IEEE 802.3 Subclause 30.7.4.1.2"
    ::= { dot3adAggPortDebugEntry 1 }


dot3adAggPortDebugLastRxTime OBJECT-TYPE
    SYNTAX      TimeTicks
    MAX-ACCESS  read-only
    STATUS      current
    DESCRIPTION
        "The value of aTimeSinceSystemReset (F.2.1) when
        the last LACPDU was received by this Aggregation Port.
        This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.4.1.3"
    ::= { dot3adAggPortDebugEntry 2 }


dot3adAggPortDebugMuxState OBJECT-TYPE
    SYNTAX      INTEGER {
                   detached(1),
                   waiting(2),
                   attached(3),
                   collecting(4),
                   distributing(5),
                   collecting_distributing(6)
                }
    MAX-ACCESS  read-only
    STATUS      current
    DESCRIPTION
        "This attribute holds the value 'detached' if the Mux
        state machine (43.4.14) for the Aggregation Port is
        in the DETACHED state, 'waiting' if the Mux state machine
        is in the WAITING state, 'attached' if the Mux state
        machine for the Aggregation Port is in the ATTACHED
        state, 'collecting' if the Mux state machine for the
        Aggregation Port is in the COLLECTING state, 'distributing'
        if the Mux state machine for the Aggregation Port is
        in the DISTRIBUTING state, and 'collecting_distributing'
        if the Mux state machine for the Aggregation Port is in
        the COLLECTING_DISTRIBUTING state.
        This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.4.1.4"
    ::= { dot3adAggPortDebugEntry 3 }


dot3adAggPortDebugMuxReason OBJECT-TYPE
    SYNTAX      DisplayString
    MAX-ACCESS  read-only
    STATUS      current
    DESCRIPTION
        "A human-readable text string indicating the reason
        for the most recent change of Mux machine state.
        This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.4.1.5"
    ::= { dot3adAggPortDebugEntry 4 }
```


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```
dot3adAggPortDebugActorChurnState OBJECT-TYPE
    SYNTAX       ChurnState
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "The state of the Actor Churn Detection machine
        (43.4.17) for the Aggregation Port. A value of 'noChurn'
        indicates that the state machine is in either the
        NO_ACTOR_CHURN or the ACTOR_CHURN_MONITOR
        state, and 'churn' indicates that the state machine is in the
        ACTOR_CHURN state. This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.4.1.6"
    ::= { dot3adAggPortDebugEntry 5 }


dot3adAggPortDebugPartnerChurnState OBJECT-TYPE
    SYNTAX       ChurnState
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "The state of the Partner Churn Detection machine
        (43.4.17) for the Aggregation Port. A value of 'noChurn'
        indicates that the state machine is in either the
        NO_PARTNER_CHURN or the PARTNER_CHURN_MONITOR
        state, and 'churn' indicates that the state machine is
        in the PARTNER_CHURN state.
        This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.4.1.7"
    ::= { dot3adAggPortDebugEntry 6 }


dot3adAggPortDebugActorChurnCount OBJECT-TYPE
    SYNTAX       Counter32
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "Count of the number of times the Actor Churn state
        machine has entered the ACTOR_CHURN state.
        This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.4.1.8"
    ::= { dot3adAggPortDebugEntry 7 }


dot3adAggPortDebugPartnerChurnCount OBJECT-TYPE
    SYNTAX       Counter32
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "Count of the number of times the Partner Churn
        state machine has entered the PARTNER_CHURN state.
        This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.4.1.9"
    ::= { dot3adAggPortDebugEntry 8 }
```

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```
dot3adAggPortDebugActorSyncTransitionCount OBJECT-TYPE
    SYNTAX       Counter32
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "Count of the number of times the Actor's Mux state
        machine (43.4.15) has entered the IN_SYNC state.
        This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.4.1.10"
    ::= { dot3adAggPortDebugEntry 9 }


dot3adAggPortDebugPartnerSyncTransitionCount OBJECT-TYPE
    SYNTAX       Counter32
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "Count of the number of times the Partner's Mux
        state machine (43.4.15) has entered the IN_SYNC state.
        This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.4.1.11"
    ::= { dot3adAggPortDebugEntry 10 }


dot3adAggPortDebugActorChangeCount OBJECT-TYPE
    SYNTAX       Counter32
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "Count of the number of times the Actor's perception of
        the LAG ID for this Aggregation Port has changed.
        This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.4.1.12"
    ::= { dot3adAggPortDebugEntry 11 }


dot3adAggPortDebugPartnerChangeCount OBJECT-TYPE
    SYNTAX       Counter32
    MAX-ACCESS   read-only
    STATUS       current
    DESCRIPTION
        "Count of the number of times the Partner's perception of
        the LAG ID (see 43.3.6.1) for this Aggregation Port has changed.
        This value is read-only."
    REFERENCE
        "IEEE 802.3 Subclause 30.7.4.1.13"
    ::= { dot3adAggPortDebugEntry 12 }

-- ----------------------------------------------------------
-- IEEE 802.3ad MIB - Conformance Information
-- ----------------------------------------------------------

dot3adAggConformance OBJECT IDENTIFIER ::= { lagMIB 2 }


dot3adAggGroups OBJECT IDENTIFIER ::= { dot3adAggConformance 1 }
```


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```
dot3adAggCompliances OBJECT IDENTIFIER
    ::= { dot3adAggConformance 2 }

-- ----------------------------------------------------------
-- units of conformance
-- ----------------------------------------------------------

dot3adAggGroup OBJECT-GROUP
    OBJECTS {
        dot3adAggActorSystemID,
        dot3adAggActorSystemPriority,
        dot3adAggAggregateOrIndividual,
        dot3adAggActorAdminKey,
        dot3adAggMACAddress,
        dot3adAggActorOperKey,
        dot3adAggPartnerSystemID,
        dot3adAggPartnerSystemPriority,
        dot3adAggPartnerOperKey,
        dot3adAggCollectorMaxDelay
    }
    STATUS      current
    DESCRIPTION
        "A collection of objects providing information about an
        aggregation."
    ::= { dot3adAggGroups 1 }


dot3adAggPortListGroup OBJECT-GROUP
    OBJECTS {
        dot3adAggPortListPorts
    }
    STATUS      current
    DESCRIPTION
        "A collection of objects providing information about every
        port in an aggregation."
    ::= { dot3adAggGroups 2 }


dot3adAggPortGroup OBJECT-GROUP
    OBJECTS {
        dot3adAggPortActorSystemPriority,
        dot3adAggPortActorSystemID,
        dot3adAggPortActorAdminKey,
        dot3adAggPortActorOperKey,
        dot3adAggPortPartnerAdminSystemPriority,
        dot3adAggPortPartnerOperSystemPriority,
        dot3adAggPortPartnerAdminSystemID,
        dot3adAggPortPartnerOperSystemID,
        dot3adAggPortPartnerAdminKey,
        dot3adAggPortPartnerOperKey,
        dot3adAggPortSelectedAggID,
        dot3adAggPortAttachedAggID,
        dot3adAggPortActorPort,
        dot3adAggPortActorPortPriority,
        dot3adAggPortPartnerAdminPort,
        dot3adAggPortPartnerOperPort,
        dot3adAggPortPartnerAdminPortPriority,
```

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```
            dot3adAggPortPartnerOperPortPriority,
            dot3adAggPortActorAdminState,
            dot3adAggPortActorOperState,
            dot3adAggPortPartnerAdminState,
            dot3adAggPortPartnerOperState,
            dot3adAggPortAggregateOrIndividual
        }
        STATUS      current
        DESCRIPTION
            "A collection of objects providing information about every
            port in an aggregation."
        ::= { dot3adAggGroups 3 }


    dot3adAggPortStatsGroup OBJECT-GROUP
        OBJECTS {
            dot3adAggPortStatsLACPDUsRx,
            dot3adAggPortStatsMarkerPDUsRx,
            dot3adAggPortStatsMarkerResponsePDUsRx,
            dot3adAggPortStatsUnknownRx,
            dot3adAggPortStatsIllegalRx,
            dot3adAggPortStatsLACPDUsTx,
            dot3adAggPortStatsMarkerPDUsTx,
            dot3adAggPortStatsMarkerResponsePDUsTx
        }
        STATUS      current
        DESCRIPTION
            "A collection of objects providing information about every
            port in an aggregation."
        ::= { dot3adAggGroups 4 }


    dot3adAggPortDebugGroup OBJECT-GROUP
        OBJECTS {
            dot3adAggPortDebugRxState,
            dot3adAggPortDebugLastRxTime,
            dot3adAggPortDebugMuxState,
            dot3adAggPortDebugMuxReason,
            dot3adAggPortDebugActorChurnState,
            dot3adAggPortDebugPartnerChurnState,
            dot3adAggPortDebugActorChurnCount,
            dot3adAggPortDebugPartnerChurnCount,
            dot3adAggPortDebugActorSyncTransitionCount,
            dot3adAggPortDebugPartnerSyncTransitionCount,
            dot3adAggPortDebugActorChangeCount,
            dot3adAggPortDebugPartnerChangeCount
        }
        STATUS      current
        DESCRIPTION
            "A collection of objects providing debug information about
            every aggregated port."
        ::= { dot3adAggGroups 5 }

    dot3adTablesLastChangedGroup OBJECT-GROUP
        OBJECTS {
            dot3adTablesLastChanged
        }
        STATUS current
        DESCRIPTION
```


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```
        "A collection of objects providing information about the time
        of changes to the configuration of aggregations and their ports."
  ::= { dot3adAggGroup 6 }

  -- ----------------------------------------------------------------
  -- compliance statements
  -- ----------------------------------------------------------------


  dot3adAggCompliance MODULE-COMPLIANCE
      STATUS  current
      DESCRIPTION
          "The compliance statement for device support of
          Link Aggregation."


      MODULE
          MANDATORY-GROUPS {
              dot3adAggGroup,
              dot3adAggPortGroup,
             dot3adTablesLastChangedGroup
          }


          GROUP       dot3adAggPortListGroup
          DESCRIPTION
              "This group is optional."


          GROUP       dot3adAggPortStatsGroup
          DESCRIPTION
              "This group is optional."


          GROUP       dot3adAggPortDebugGroup
          DESCRIPTION
              "This group is optional."


      ::= { dot3adAggCompliances 1 }


  END
```

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Annex 31A

(normative)

MAC Control opcode assignments

Table 31A–1 shows the currently defined opcode values and interpretations:

Table 31A–1—MAC Control opcodes

Opcode (Hexadecimal)	MAC Control function	Specified in annex	Value/comment
00-00	Reserved		
00-01	PAUSE	31B	Requests that the recipient stop transmitting non-control frames for a period of time indicated by the parameters of this function.
00-02 through FF-FF	Reserved		

Opcodes are transmitted high-order octet first. Within each octet, bits are transmitted least-significant bit first. Reserved opcodes shall not be used by MAC Control sublayer entities.

Table 31A–2 shows the elements and semantics of the indication_operand_list for MA_CONTROL.indication primitives for each currently defined opcode value in Table 31A–1:

Table 31A–2—MAC Control indications

PAUSE (opcode 0x0001)		
indication_operand_list element	**Value**	**Interpretation**
pause_status	paused	Indicates that the PAUSE function is inhibiting transmission of data frames by the MAC client.
	not_paused	Indicates that the PAUSE function is not inhibiting transmission of data frames by the MAC client.

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Annex 31B

(normative)

MAC Control PAUSE operation

31B.1 PAUSE description

The PAUSE operation is used to inhibit transmission of data frames for a specified period of time. A MAC Control client wishing to inhibit transmission of data frames from another station on the network generates a MA_CONTROL.request primitive specifying:

a) The globally assigned 48-bit multicast address 01-80-C2-00-00-01,
b) The PAUSE opcode,
c) A request_operand indicating the length of time for which it wishes to inhibit data frame transmission. (See 31B.2.)

The PAUSE operation cannot be used to inhibit transmission of MAC Control frames.

PAUSE frames shall only be sent by DTEs configured to the full duplex mode of operation.

The globally assigned 48-bit multicast address 01-80-C2-00-00-01 has been reserved for use in MAC Control PAUSE frames for inhibiting transmission of data frames from a DTE in a full duplex mode IEEE 802.3 LAN. IEEE 802.1D-conformant bridges will not forward frames sent to this multicast destination address, regardless of the state of the bridge's ports, or whether or not the bridge implements the MAC Control sublayer. To allow generic full duplex flow control, stations implementing the PAUSE operation shall instruct the MAC (e.g., through layer management) to enable reception of frames with destination address equal to this multicast address.

NOTE—By definition, an IEEE 802.3 LAN operating in full duplex mode comprises exactly two stations, thus there is no ambiguity regarding the destination DTE's identity. The use of a well-known multicast address relieves the MAC Control sublayer and its client from having to know, and maintain knowledge of the individual 48-bit address of the other DTE in a full duplex environment

31B.2 Parameter semantics

The PAUSE opcode takes the following request_operand:

pause_time
: A 2-octet, unsigned integer containing the length of time for which the receiving station is requested to inhibit data frame transmission. The field is transmitted most-significant octet first, and least-significant octet second. The pause_time is measured in units of pause_quanta, equal to 512 bit times of the particular implementation (See 4.4). The range of possible pause_time is 0 to 65535 pause_quanta.

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31B.3 Detailed specification of PAUSE operation

31B.3.1 Transmit operation

Upon receipt of a MA_CONTROL.request primitive containing the PAUSE opcode from a MAC Control client, the MAC Control sublayer calls the MAC sublayer TransmitFrame function with the following parameters:

a) The destinationParam is set equal to the destination_address parameter of the MA_DATA.request primitive. This is currently restricted to the value specified in 31B.1.
b) The sourceParam is set equal to the 48-bit individual address of the station.
c) The lengthOrTypeParam is set to the reserved 802.3_MAC_Control value specified in 31.4.1.3.
d) The dataParam is set equal to the concatenation of the PAUSE opcode encoding (see Annex 31A), the pause_time request_operand specified in the MA_CONTROL.request primitive (see 2.3.3.2), and a field containing zeroes of the length specified in 31.4.1.6.

Upon receipt of a data transmission request from the MAC Control client through the MA_DATA.request primitive, if the transmission of data frames has not been inhibited due to reception of a valid MAC Control frame specifying the PAUSE operation and a non-zero pause_time, the MAC Control sublayer calls the MAC sublayer TransmitFrame function with the following parameters:

a) The destinationParam is set equal to the destination_address parameter of the MA_CONTROL.request primitive.
b) The sourceParam is set equal to the 48-bit individual address of the station.
c) The lengthOrTypeParam and dataParam are set from the m_sdu field of the MA_DATA.request primitive.

31B.3.2 Transmit state diagram for PAUSE operation

It is not required that an implementation be able to transmit PAUSE frames. MAC Control sublayer entities that transmit PAUSE frames shall implement the Transmit State machine specified in this subclause.

31B.3.2.1 Constants

pause_command
: The 2-octet encoding of the PAUSE command, as specified in Annex 31A.

reserved_multicast_address
: The 48-bit address specified in 31B.1 (a).

802.3_MAC_Control
: The 16 bit type field assignment for 802.3 MAC Control specified in 31.4.1.3.

phys_Address
: A 48-bit value, equal to the unicast address of the station implementing the MAC Control sublayer.

31B.3.2.2 Variables

transmitEnabled
: A boolean set by Network Management to indicate that the station is permitted to transmit on the network.
: Values: true; Transmitter is enabled by management
false; Transmitter is disabled by management

transmission_in_progress
: A boolean used to indicate to the Receive State Machine that a TransmitFrame function call is pending.

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Values: true; transmission is in progress
false; transmission is not in progress

n_quanta_tx
An integer indicating the number of pause_quanta that the transmitter of a PAUSE frame is requesting that the receiver pause.

pause_timer_Done
A boolean set by the MAC Control PAUSE Operation Receive State Machine to indicate the expiration of a pause_timer initiated by reception of a MAC Control frame with a PAUSE opcode.

Values: true; The pause_timer has expired.
false; The pause_timer has not expired.

31B.3.2.3 Functions

TransmitFrame
The MAC Sublayer primitive called to transmit a frame with the specified parameters.

31B.3.2.4 Timers

pause_timer
The timer governing the inhibition of transmission of data frames from a MAC Client by the PAUSE function.

31B.3.2.5 Messages

MA_CONTROL.request
The service primitive used by a client to request a MAC Control sublayer function with the specified request_operands.

MA_DATA.request
The service primitive used by a client to request MAC data transmission with the specified parameters.

31B.3.2.6 Transmit state diagram for PAUSE operation

Figure 31B–1 depicts the Transmit State Diagram for a MAC Control sublayer entity implementing the PAUSE operation.

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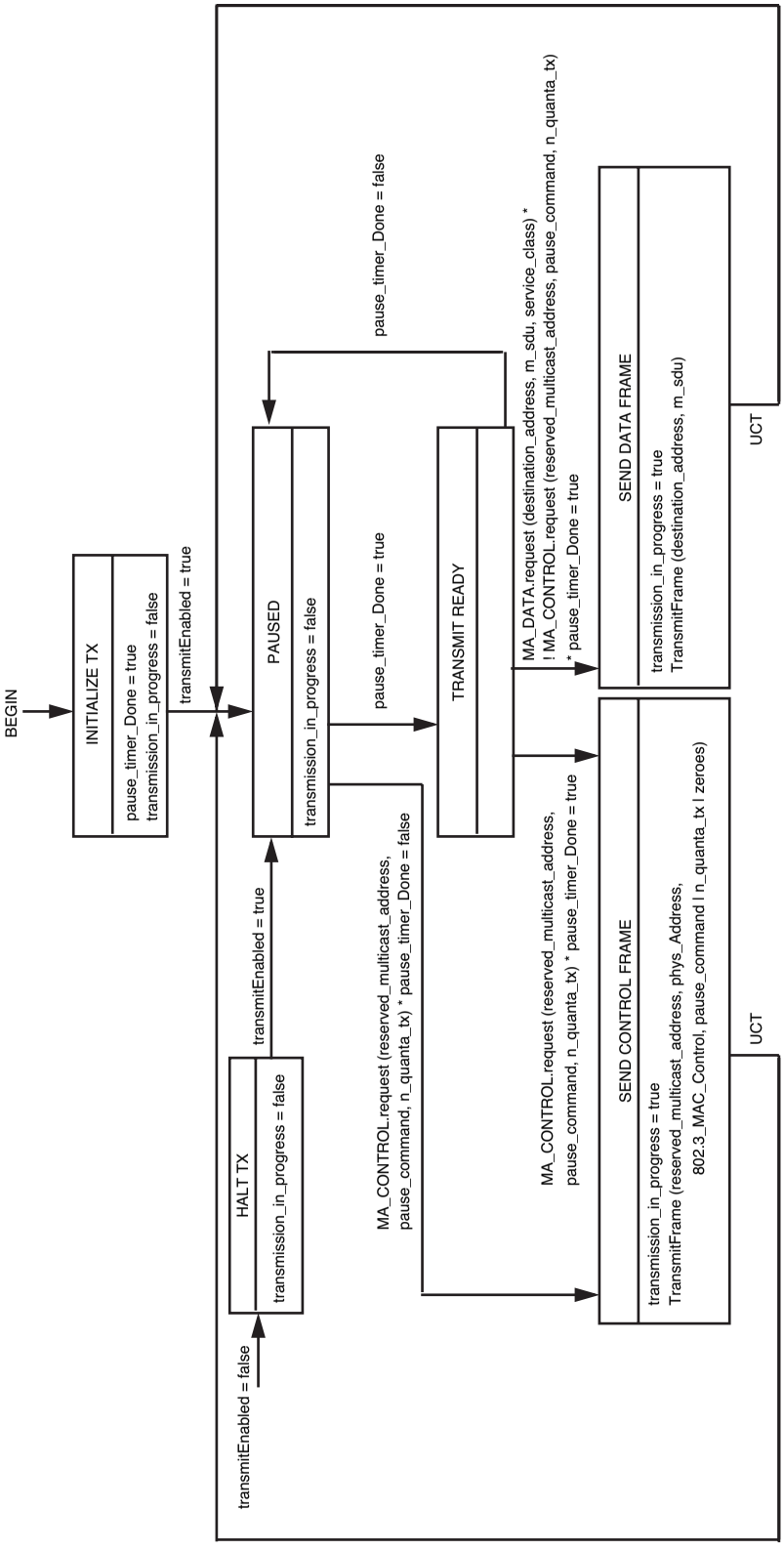


Figure 31B–1—PAUSE Operation Transmit state diagram

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31B.3.3 Receive operation

The opcode-independent MAC Control sublayer Receive State Machine accepts and parses valid frames received from the MAC sublayer. MAC Control sublayer entities that implement the PAUSE operation shall implement the Receive State machine specified in this subclause. The functions specified in this subclause are performed upon receipt of a valid Control frame containing the PAUSE opcode, and define the function called by the INITIATE MAC CONTROL FUNCTION state of Figure 31–4. (See 31.5.3.)

Upon receipt of a valid MAC Control frame with the opcode indicating PAUSE and the destination address indicating either: (1) the reserved multicast address specified in 31B.1, or (2) the unique physical address associated with this station, the MAC Control sublayer starts a timer for the length of time specified by the pause_time request_operand in the Control frame (see 31B.2). The value of the variable pause_timer_Done is set to false upon the setting of the pause_timer to a non-zero value by the MAC Control PAUSE Operation Receive State Machine. The value of the variable pause_timer_Done is set to true when the timer value reaches zero (i.e., the timer expires). If the received PAUSE operation indicates a pause_timer value of zero, the value of pause_timer_Done is set to true immediately.

The receipt of a valid MAC Control frame with the opcode indicating PAUSE and the destination address indicating the reserved multicast address specified in 31B.1 or the unique physical address associated with this station will cause the pause_timer to be set according to the pause_time request_operand in the newly received frame, regardless of the current setting of the pause_timer, i.e., new PAUSE operations override earlier PAUSE operations.

31B.3.4 Receive state diagram for PAUSE operation

31B.3.4.1 Constants

pause_quantum
: The unit of measurement for pause time specified in 31B.2

pause_command
: The 2-octet encoding of the PAUSE command, as specified in Annex 31A.

reserved_multicast_address
: The 48-bit address specified in 31B.1 (a).

phys_Address
: A 48-bit value, equal to the unicast address of the station implementing the MAC Control sublayer.

31B.3.4.2 Variables

n_quanta_rx
: An integer used to extract the number of pause quanta to set the pause_timer from the dataParam of the received frame.

opcode
: The opcode parsed from the received frame.

DA
: The destination address from the ReceiveFrame function.

transmission_in_progress
: A boolean used by the Transmit State Machine to indicate that a TransmitFrame function call is pending.

  Values: true; transmission is in progress
  false; transmission is not in progress

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31B.3.4.3 Timers

pause_timer
: The timer governing the inhibition of transmission of data frames.

31B.3.4.4 Receive state diagram (INITIATE_MAC CONTROL FUNCTION) for PAUSE operation

Figure 31B–2 depicts the INITIATE MAC CONTROL FUNCTION for the PAUSE operation. (See 31.5.3.)

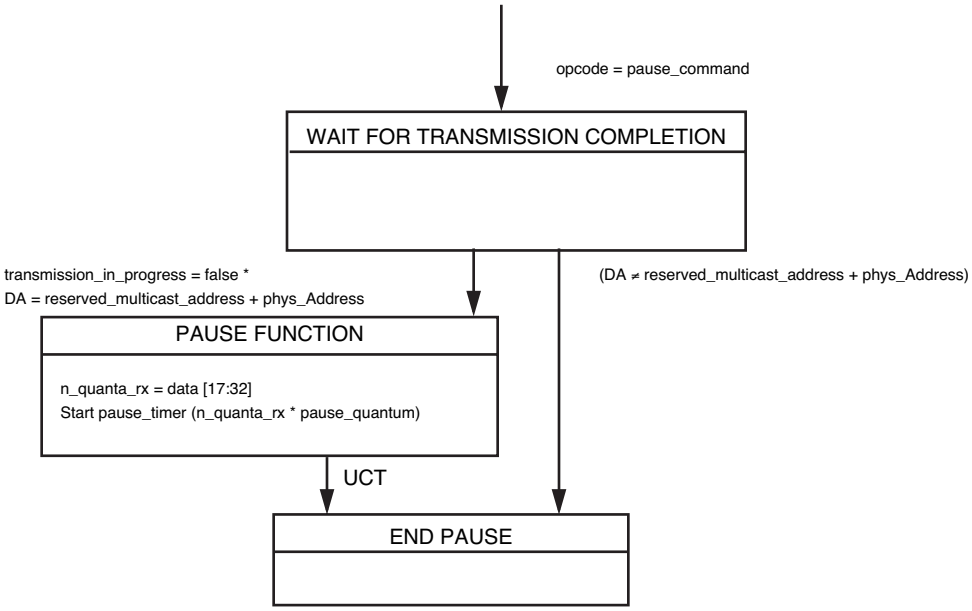


Figure 31B–2—PAUSE Operation Receive state diagram

31B.3.5 Status indication operation

MAC Control sublayer entities that implement the PAUSE operation shall implement the Indication State machine specified in this subclause.

The PAUSE function sets the pause_status variable to one of two values: paused or not_paused, and indicates this to its client through the MA_CONTROL.indication primitive.

31B.3.6 Indication state diagram for pause operation

31B.3.6.1 Constants

pause_command
: The 2-octet encoding of the PAUSE command, as specified in Annex 31A.

31B.3.6.2 Variables

pause_status
: Used to indicate the state of the MAC Control sublayer for the PAUSE operation. It takes one of two values: paused or not_paused.

pause_timer_Done
: A boolean set by the MAC Control PAUSE Operation Receive State Machine to indicate the expiration of a pause_timer initiated by reception of a MAC Control frame with a PAUSE opcode.

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Values: true; The pause_timer has expired.
false; The pause_timer has not expired.

31B.3.6.3 Messages

MA_CONTROL.indication
The service primitive used indicate the state of the MAC Control sublayer to its client.

31B.3.6.4 Indication state diagram for PAUSE operation

Figure 31B–3 depicts the Indication State Diagram for a MAC Control sublayer implementing the PAUSE operation.

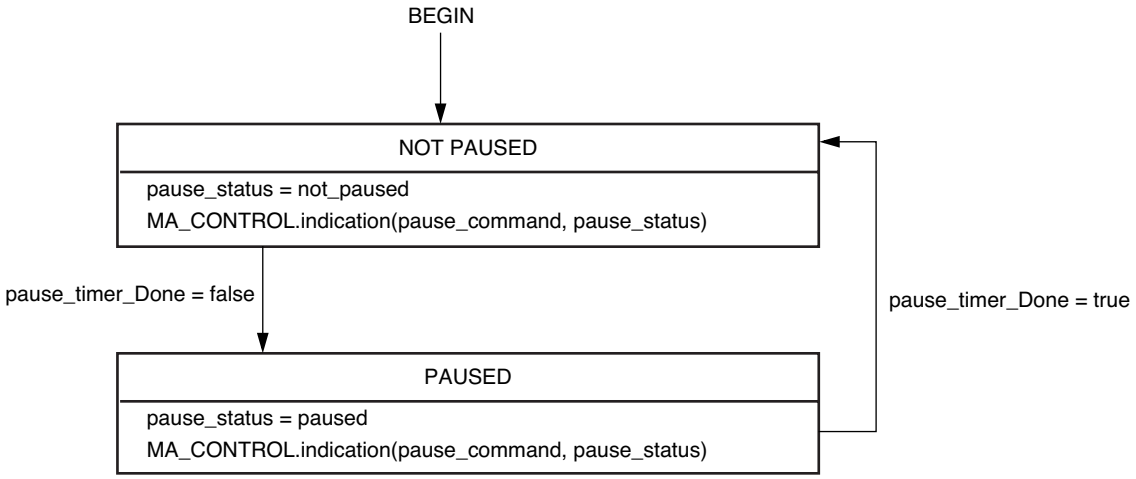


Figure 31B–3—PAUSE Operation Indication state diagram

31B.3.7 Timing considerations for PAUSE operation

In a full duplex mode DTE, it is possible to receive PAUSE frames asynchronously with respect to the transmission of Data frames. For effective flow control, it is necessary to place an upper bound on the length of time that a DTE can transmit Data frames after receiving a valid PAUSE frame with a non-zero pause_time request_operand.

Reception of a PAUSE frame shall not affect the transmission of a frame that has been submitted by the MAC Control sublayer to the underlying MAC (i.e., the TransmitFrame function is synchronous, and is never interrupted).

At operating speeds of 100 Mb/s or less, a station that implements an exposed MII, shall not begin to transmit a (new) frame (assertion of TX_EN at the MII, see 22.2.2.3) more than pause_quantum bit times after the reception of a valid PAUSE frame (de-assertion of RX_DV at the MII, see 22.2.2.6) that contains a non-zero value of pause_time. Stations that do not implement an exposed MII, shall measure this time at the MDI, with the timing specification increased to (pause_quantum + 64) bit times.

At operating speeds above 100 Mb/s, a station shall not begin to transmit a (new) frame more than two pause_quantum bit times after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

In addition to DTE and MAC Control delays, system designers should take into account the delay of the link segment when designing devices that implement the PAUSE operation (see Clause 29).

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31B.4 Protocol Conformance Statement (PICS) proforma for MAC Control PAUSE operation[23]

31B.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 31B, MAC Control PAUSE operation, shall complete the following PICS proforma in addition to the PICS of Clause 31.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

31B.4.2 Identification

31B.4.2.1 Implementation identification

Supplier	
Contact point for queries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations, other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

31B.4.2.2 Protocol summary

Identification of protocol specification	IEEE Std 802.3-2002, Annex 31B, MAC Control PAUSE operation
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; The answer Yes means that the implementation does not conform to IEEE Std 802.3-2002)	

Date of Statement	

[23] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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31B.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PST	Support for transmit of PAUSE frames	31B.3.2	N/A	O	Yes [ ] No [ ]
*MIIa	At operating speeds of 100 Mb/s or less, MII connection exists and is accessible for test.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIb	At operating speeds of 100 Mb/s or less, MII connection does not exist or is not accessible for test.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIc	At operating speeds above 100 Mb/s	31B.3.7	N/A	O	Yes [ ] No [ ]

31B.4.4 PAUSE command requirements

Item	Feature	Subclause	Value/comment	Status	Support
PCR1	Duplex mode of DTE	31B.1	Full duplex	M	Yes [ ]
PCR2	Reception of frames with destination address equal to the multicast address 01-80-C2-00-00-01	31B.1	Enabled	M	Yes [ ]

31B.4.5 PAUSE command state diagram requirements

Item	Feature	Subclause	Value/comment	Status	Support
PSD1	Transmit state diagram for PAUSE operation	31B.3.2	Meets requirements of Figure 31B–1	PST: M	N/A [ ] M:Yes [ ]
PSD2	Receive state diagram for PAUSE operation	31B.3.4	Meets requirements of Figure 31B–2	M	Yes [ ]
PSD3	Indication state diagram for PAUSE operation	31B.3.6	Meets requirements of Figure 31B–3	M	Yes [ ]

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31B.4.6 PAUSE command MAC timing considerations

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	Effect of PAUSE frame on a frame already submitted to underlying MAC	31B.3.7	Has no effect	M	Yes [ ]
	Delay from receiving valid PAUSE command, with non-zero value for pause_time, to cessation of transmission	31B.3.7	Measured as described		
TIM2	Measurement point for station with MII		Delay at MDI ≤ pause_quantum bits	MIIa: M	N/A [ ] M: Yes [ ]
TIM3	Measurement point for station without MII		Delay at MDI ≤ (pause_quantum + 64) bits	MIIb: M	N/A [ ] M: Yes [ ]
TIM4	Measurement point for station at greater than 100 Mb/s		Delay at MDI ≤ (2 × pause-quantum) bits	MIIc: M	N/A [ ] M: Yes [ ]

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Annex 32A

(informative)

Use of cabling systems with nominal differential characteristic impedance of 120 Ω or 150 Ω

The 100BASE-T2 standard specifies only the use of 100 Ω link segments for conformance. Since ISO/IEC 11801: 1995 also recognizes 120 Ω and 150 Ω cabling, this informative annex specifies the conditions for using cabling systems with nominal characteristic impedances of 120 Ω and 150 Ω by 100BASE-T2 conformant stations.

The use of cabling with a characteristic impedance outside the range specified in 32.7.2.2 will generally increase the mismatching effects in the link components if directly coupled to the PHY without a impedance transforming balun and results in the following consequences:

a) Increased echo due primarily to poorer hybrid performance
b) Increased cabling attenuation roughness due to increased reflections
c) Increased transmitter launch amplitude
d) Possible non-linearities in transmitter

The effect of increased echo and reflection is more than compensated by use of Category 4 or higher 120 Ω cabling or 150 Ω cabling consistent with ISO/IEC 11801 specifications. The increased transmitter launch level will not be an additional noise or EMC problem on these quality cabling. Manufacturers intending to support a direct connection of 120 Ω or 150 Ω cabling to the 100BASE-T2 PHY must ensure that the transmitters can tolerate the impedance without additional non-linearity.

If baluns are used instead of a direct connection, care must be taken to ensure that the corner frequencies of the baluns do not substantially interfere with the 100BASE-T2 signals. In practice, a lower corner frequency less than 100 kHz and an upper corner frequency greater than 30 MHz should be adequate for use with Category 4 or higher 120 Ω cabling or 150 Ω cabling consistent with ISO/IEC 11801 specifications.

CAUTION—Users of the present annex are further advised to check with the manufacturer of the particular 100BASE-T2 devices they intend to use with a 120 Ω or 150 Ω link whether those devices can operate correctly on cabling with Zc as high as 120 Ω ± 15 Ω and 150 Ω ± 15 Ω.

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Information technology—
Telecommunications and information exchange between systems—
Local and metropolitan area networks—Specific requirements—

Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) access method and physical layer specifications

SECTION THREE: This section includes Clauses 34 through 43 and Annexes 36A through 43C.

34. Introduction to 1000 Mb/s baseband network

34.1 Overview

Gigabit Ethernet couples an extended version of the ISO/IEC 8802-3 (CSMA/CD MAC) to a family of 1000 Mb/s Physical Layers. The relationships among Gigabit Ethernet, the extended ISO/IEC 8802-3 (CSMA/CD MAC), and the ISO/IEC Open System Interconnection (OSI) reference model are shown in Figure 34–1.

Gigabit Ethernet uses the extended ISO/IEC 8802-3 MAC layer interface, connected through a Gigabit Media Independent Interface layer to Physical Layer entities (PHY sublayers) such as 1000BASE-LX, 1000BASE-SX, and 1000BASE-CX, and 1000BASE-T.

Gigabit Ethernet extends the ISO/IEC 8802-3 MAC beyond 100 Mb/s to 1000 Mb/s. The bit rate is faster, and the bit times are shorter—both in proportion to the change in bandwidth. In full duplex mode, the minimum packet transmission time has been reduced by a factor of ten. Achievable topologies for 1000 Mb/s full duplex operation are comparable to those found in 100BASE-T full duplex mode. In half duplex mode, the minimum packet transmission time has been reduced, but not by a factor of ten. Cable delay budgets are similar to those in 100BASE-T. The resulting achievable topologies for the half duplex 1000 Mb/s CSMA/CD MAC are similar to those found in half duplex 100BASE-T.

34.1.1 Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII)

The Gigabit Media Independent Interface (Clause 35) provides an interconnection between the Media Access Control (MAC) sublayer and Physical Layer entities (PHY) and between PHY Layer and Station Management (STA) entities. This GMII supports 1000 Mb/s operation through its eight bit wide (octet wide) transmit and receive paths. The Reconciliation sublayer provides a mapping between the signals provided at the GMII and the MAC/PLS service definition.

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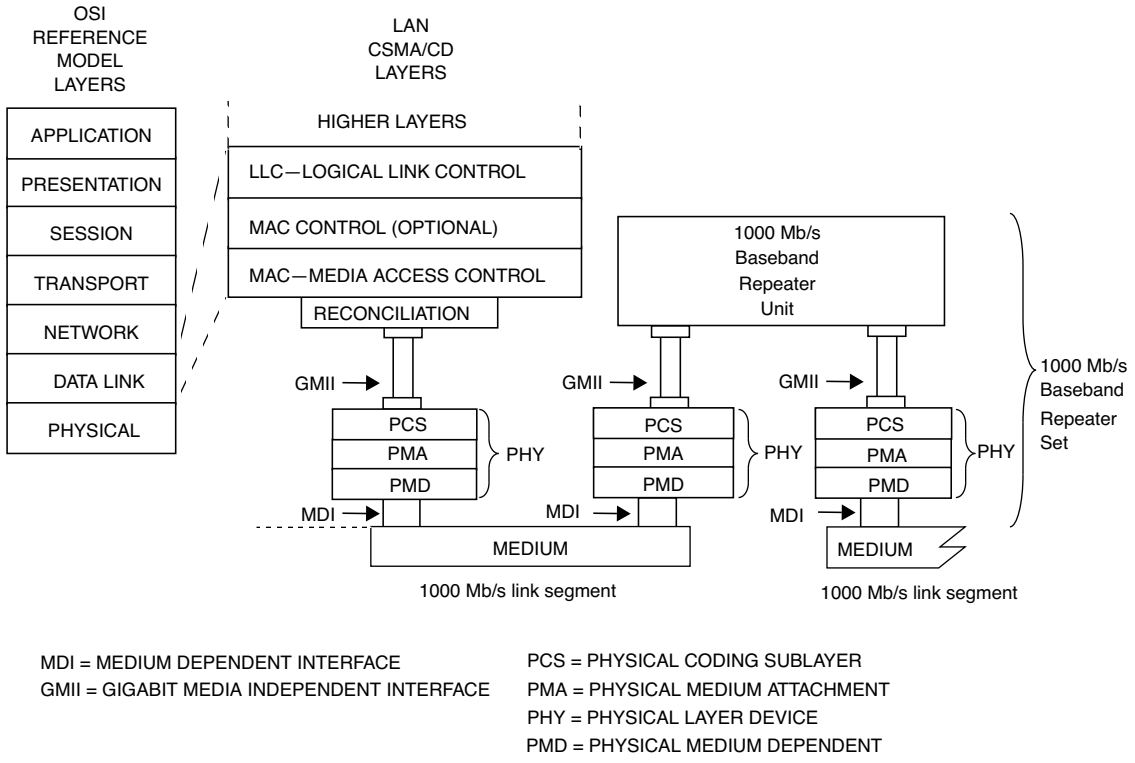


Figure 34–1—Architectural positioning of Gigabit Ethernet (1000 Mb/s operation)

34.1.2 Physical Layer signaling systems

This standard specifies a family of Physical Layer implementations. The generic term 1000 Mb/s MAC refers to any use of the 1000 Mb/s ISO/IEC 8802-3 CSMA/CD MAC (the Gigabit Ethernet MAC) coupled with any physical layer implementation.

The term 1000BASE-X refers to a specific family of physical layer implementations specified in Clauses 36–39. The 1000BASE-X family of physical layer standards has been adapted from the ANSI X3.230-1994 [B20] (Fibre Channel) FC-0 and FC-1 physical layer specifications and the associated 8B/10B data coding method. The 1000BASE-X family of physical layer implementations is composed of 1000BASE-SX, 1000BASE-LX, and 1000BASE-CX.

All 1000BASE-X PHY devices share the use of common PCS, PMA, and Auto-Negotiation specifications (see Clauses 36 and 37). The 1000BASE-T PHY (Clause 40) uses four pairs of Category 5 balanced copper cabling. Clause 40 defines its own PCS, which does not use 8B/10B coding.

Specifications unique to the physical operation of each physical layer device are shown in the following table:

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1000BASE-SX Short Wave Length Optical	Duplex multimode fibers	Clause 38
1000BASE-LX Long Wave Length Optical	Duplex single-mode fibers or Duplex multimode fibers	Clause 38
1000BASE-CX Shielded Jumper Cable	Two pairs of specialized balanced cabling	Clause 39
1000BASE-T Category 5 UTP	Advanced multilevel signaling over four pairs of Category 5 balanced copper cabling.	Clause 40

34.1.3 Repeater

A repeater set (Clause 41) is an integral part of any Gigabit Ethernet network with more than two DTEs in a collision domain. A repeater set extends the physical system topology by coupling two or more segments. Only one repeater is permitted within a single collision domain.

34.1.4 Auto-Negotiation, type 1000BASE-X

Auto-Negotiation (Clause 37) provides a 1000BASE-X device with the capability to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for joint operation. Auto-Negotiation is performed upon link startup through the use of a special sequence of reserved link code words. Clause 37 adopts the basic architecture and algorithms from Clause 28, but not the use of fast link pulses.

34.1.5 Physical Layer line signaling for 10 Mb/s and 100 Mb/s Auto-Negotiation on twisted pair

Auto-Negotiation (Clause 28) is used by 1000BASE-T devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for joint operation. Auto-Negotiation is performed upon link startup through the use of a special sequence of fast link pulses.

34.1.6 Management

Managed objects, attributes, and actions are defined for all Gigabit Ethernet components (Clause 30). That clause consolidates all IEEE 802.3 management specifications so that 10/100/1000 Mb/s agents can be managed by existing network management stations with little or no modification to the agent code.

34.2 State diagrams

State machine diagrams take precedence over text.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

34.3 Protocol Implementation Conformance Statement (PICS) proforma

The supplier of a protocol implementation that is claimed to conform to any part of IEEE 802.3, Clauses 35 through 41, shall complete a Protocol Implementation Conformance Statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. Each of the Gigabit Ethernet PICS conforms to the same notation and conventions used in 100BASE-T (see 21.6).

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34.4 Relation of Gigabit Ethernet to other standards

Suitable entries for Table G1 of ISO/IEC 11801: 1995, annex G, would be as follows:

a) Within the section Optical Link:
CSMA/CD 1000BASE-SX ISO/IEC 8802-3/ PDAM 26
b) Within the section Optical Link:
CSMA/CD 1000BASE-LX ISO/IEC 8802-3/PDAM 26
c) Within the section Balanced Cabling Link Class D (defined up to 100MHz):
CSMA/CD 1000BASE-T* ISO/IEC8802-3/DAD 1995

*To support 1000BASE-T applications, Class D links shall meet the requirements for return loss, ELFEXT and MDELFEXT specified in 40.7.

A suitable entry for Table G5 of ISO/IEC 11801: 1995, Annex G, would be as follows:

Table 34–1—Table G5 of ISO/IEC 11801

	Fibre per Clauses 5, 7, and 8			**Optical link per 6**								
				Horizontal			**Building backbone**			**Campus backbone**		
	62.5/125 μm MMF	**50/125 μm MMF**	**10/125 μm SMF**	**62.5/125 μm MMF**	**50/125 μm MMF**	**10/125 μm SMF**	**62.5/125 μm MMF**	**50/125 μm MMF**	**10/125 μm SMF**	**62.5/125 μm MMF**	**50/125 μm MMF**	**10/125 μm SMF**
8802-3: 1000BASE-SX	I	I		N	N		I	N		I	I	
8802-3: 1000BASE-LX	I	I	I	N	N	N	N	N	N	I	I	N
NOTE—"N" denotes normative support of the media in the standard. "I" denotes that there is information in the International Standard regarding operation on this media.												

Suitable entries for table G4 of ISO/IEC 11801:1995 Annex G would be:

Table 34–2—Table G4 of ISO/IEC 11801:1995

	Balanced cabling per Clauses 5, 7, and 8							**Performance based cabling per 6**												
								Class A			**Class B**			**Class C**			**Class D**		
	Cat 3 100 Ω	**Cat 4 100 Ω**	**Cat 5 100 Ω**	**Cat 3 120 Ω**	**Cat 4 120 Ω**	**Cat 5 120 Ω**	**150 Ω**	**100 Ω**	**120 Ω**	**150 Ω**	**100 Ω**	**120 Ω**	**150 Ω**	**100 Ω**	**120 Ω**	**150 Ω**	**100 Ω**	**120 Ω**	**150 Ω**
8802-3: 1000BASE-T			I[a]														I[a]		
NOTE—"I" denotes that there is information in the International Standard regarding operation on this media.																				

[a]8802-3 imposes additional requirements on return loss, ELFEXT and MDELFEXT.

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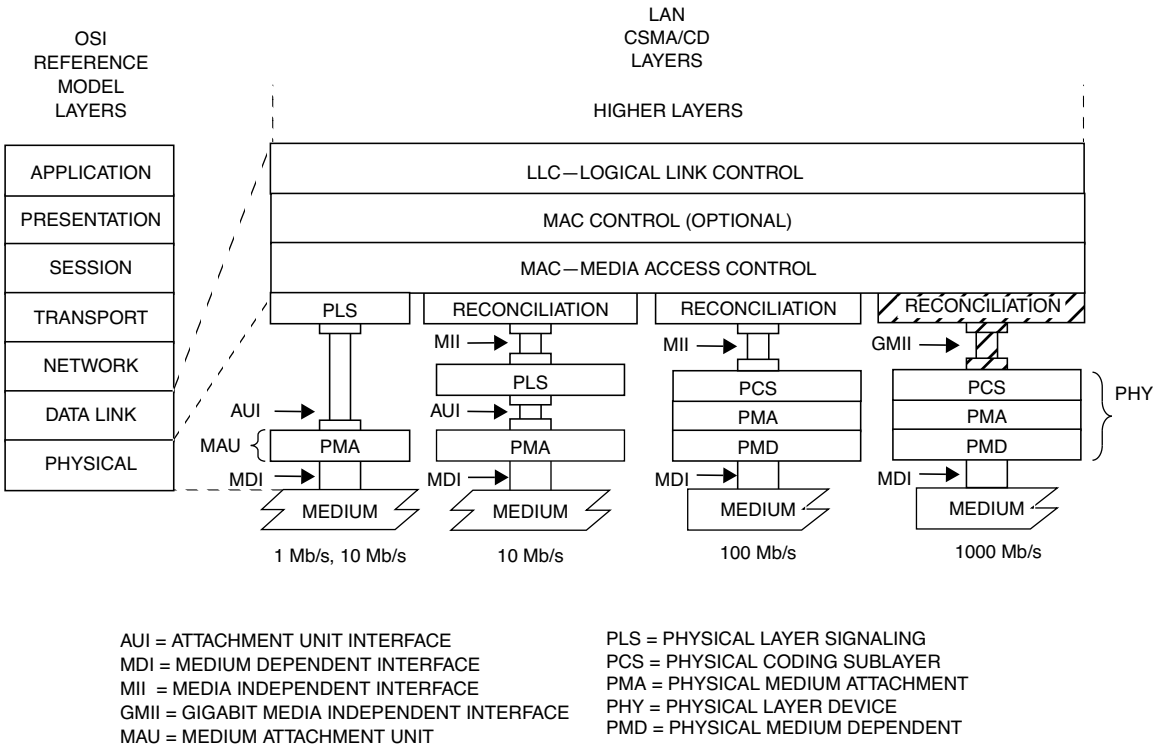
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35. Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII)

35.1 Overview

This clause defines the logical and electrical characteristics for the Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII) between CSMA/CD media access controllers and various PHYs. Figure 35–1 shows the relationship of the Reconciliation sublayer and GMII to the ISO/IEC OSI reference model.



AUI = ATTACHMENT UNIT INTERFACE
MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MAU = MEDIUM ATTACHMENT UNIT

PLS = PHYSICAL LAYER SIGNALING
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 35–1—GMII location in the OSI protocol stack

The purpose of this interface is to provide a simple, inexpensive, and easy-to-implement interconnection between Media Access Control (MAC) sublayer and PHYs, and between PHYs and Station Management (STA) entities.

This interface has the following characteristics:

a) It is capable of supporting 1000 Mb/s operation.
b) Data and delimiters are synchronous to clock references.
c) It provides independent eight-bit-wide transmit and receive data paths.
d) It provides a simple management interface.
e) It uses signal levels, compatible with common CMOS digital ASIC processes and some bipolar processes.
f) It provides for full duplex operation.

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35.1.1 Summary of major concepts

a) The GMII is based on the MII defined in Clause 22.
b) Each direction of data transfer is serviced by Data (an eight-bit bundle), Delimiter, Error, and Clock signals.
c) Two media status signals are provided. One indicates the presence of carrier, and the other indicates the occurrence of a collision.
d) The GMII uses the MII management interface composed of two signals that provide access to management parameters and services as specified in Clause 22.
e) MII signal names have been retained and the functions of most signals are the same, but additional valid combinations of signals have been defined for 1000 Mb/s operation.
f) The Reconciliation sublayer maps the signal set provided at the GMII to the PLS service primitives provided to the MAC.
g) GMII signals are defined such that an implementation may multiplex most GMII signals with the similar PMA service interface defined in Clause 36.

35.1.2 Application

This clause applies to the interface between the MAC and PHYs, and between PHYs and Station Management entities. The implementation of the interface is primarily intended as a chip-to-chip (integrated circuit to integrated circuit) interface implemented with traces on a printed circuit board. A motherboard-to-daughterboard interface between two or more printed circuit boards is not precluded.

This interface is used to provide media independence so that an identical media access controller may be used with any of the copper and optical PHY types.

35.1.3 Rate of operation

The GMII supports only 1000 Mb/s operation and is defined within this clause. Operation at 10 Mb/s and 100 Mb/s is supported by the MII defined in Clause 22.

PHYs that provide a GMII shall support 1000 Mb/s operation, and may support additional rates using other interfaces (e.g., MII). PHYs must report the rates at which they are capable of operating via the management interface, as described in 22.2.4. Reconciliation sublayers that provide a GMII shall support 1000 Mb/s and may support additional rates using other interfaces.

35.1.4 Allocation of functions

The allocation of functions at the GMII balances the need for media independence with the need for a simple and cost-effective interface.

While the Attachment Unit Interface (AUI) was defined to exist between the Physical Signaling (PLS) and Physical Medium Attachment (PMA) sublayers for 10 Mb/s DTEs, the GMII (like the Clause 22 MII) maximizes media independence by cleanly separating the Data Link and Physical Layers of the ISO/IEC seven-layer reference model. This allocation also recognizes that implementations can benefit from a close coupling between the PLS or PCS sublayer and the PMA sublayer.

35.2 Functional specifications

The GMII is designed to make the differences among the various media transparent to the MAC sublayer. The selection of logical control signals and the functional procedures are all designed to this end.

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35.2.1 Mapping of GMII signals to PLS service primitives and Station Management

The Reconciliation sublayer maps the signals provided at the GMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the Reconciliation sublayer, and described here, behave in exactly the same manner as defined in Clause 6.

Figure 35–2 depicts a schematic view of the Reconciliation sublayer inputs and outputs, and demonstrates that the GMII management interface is controlled by the Station Management entity (STA).

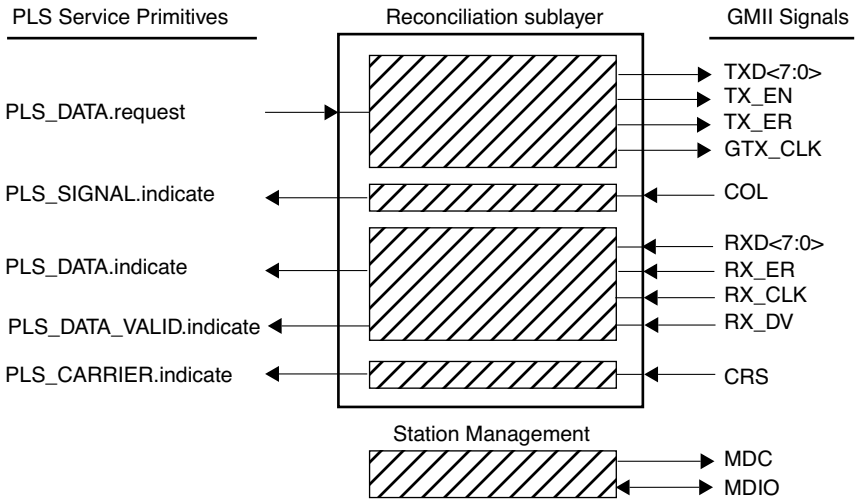


Figure 35–2—Reconciliation Sublayer (RS) inputs and outputs and STA connections to GMII

35.2.1.1 Mapping of PLS_DATA.request

35.2.1.1.1 Function

Map the primitive PLS_DATA.request to the GMII signals TXD<7:0>, TX_EN, TX_ER and GTX_CLK.

35.2.1.1.2 Semantics of the service primitive

PLS_DATA.request (OUTPUT_UNIT)

The OUTPUT_UNIT parameter can take one of five values: ONE, ZERO, TRANSMIT_COMPLETE, EXTEND or EXTEND_ERROR. It represents or is equivalent to a single data bit. These values are conveyed by the signals TX_EN, TX_ER, TXD<7>, TXD<6>, TXD<5>, TXD<4>, TXD<3>, TXD<2>, TXD<1> and TXD<0>.

Each of the eight TXD signals conveys either a ONE or ZERO of data while TX_EN is asserted. Eight data bit equivalents of EXTEND or EXTEND_ERROR are conveyed by a specific encoding of the TXD<7:0> signals when TX_EN is not asserted, and TX_ER is asserted, see Table 35–1. Synchronization between the Reconciliation sublayer and the PHY is achieved by way of the GTX_CLK signal. The value TRANSMIT_COMPLETE is conveyed by the de-assertion of either TX_EN or TX_ER at the end of a MAC's transmission.

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35.2.1.1.3 When generated

The GTX_CLK signal is generated by the Reconciliation sublayer. The TXD<7:0>, TX_EN and TX_ER signals are generated by the Reconciliation sublayer after every group of eight PLS_DATA.request transactions from the MAC sublayer to request the transmission of eight data bits on the physical medium, to extend the carrier event the equivalent of eight bits, or to stop transmission.

35.2.1.2 Mapping of PLS_DATA.indicate

35.2.1.2.1 Function

Map the primitive PLS_DATA.indicate to the GMII signals RXD<7:0>, RX_DV, RX_ER, and RX_CLK.

35.2.1.2.2 Semantics of the service primitive

PLS_DATA.indicate (INPUT_UNIT)

The INPUT_UNIT parameter can take one of three values: ONE, ZERO or EXTEND. It represents or is equivalent to a single data bit. These values are derived from the signals RX_DV, RX_ER, RXD<7>, RXD<6>, RXD<5>, RXD<4>, RXD<3>, RXD<2>, RXD<1>, and RXD<0>. The value of the data transferred to the MAC is controlled by GMII error indications, see 35.2.1.5.

Each of the eight RXD signals conveys either a ONE or ZERO of data while RX_DV is asserted. Eight data bit equivalents of EXTEND are conveyed by a specific encoding of the RXD<7:0> signals when RX_DV is not asserted, and RX_ER is asserted; see Table 35–2. Synchronization between the Reconciliation sublayer and the PHY is achieved by way of the RX_CLK signal.

35.2.1.2.3 When generated

This primitive is generated to all MAC sublayer entities in the network after a PLS_DATA.request is issued. Each octet transferred on RXD<7:0> will result in the generation of eight PLS_DATA.indicate transactions.

35.2.1.3 Mapping of PLS_CARRIER.indicate

35.2.1.3.1 Function

Map the primitive PLS_CARRIER.indicate to the GMII signal CRS.

35.2.1.3.2 Semantics of the service primitive

PLS_CARRIER.indicate (CARRIER_STATUS)

The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF. CARRIER_STATUS assumes the value CARRIER_ON when the GMII signal CRS is asserted and assumes the value CARRIER_OFF when CRS is de-asserted.

35.2.1.3.3 When generated

The PLS_CARRIER.indicate service primitive is generated by the Reconciliation sublayer whenever the CARRIER_STATUS parameter changes from CARRIER_ON to CARRIER_OFF or vice versa.

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35.2.1.4 Mapping of PLS_SIGNAL.indicate

35.2.1.4.1 Function

Map the primitive PLS_SIGNAL.indicate to the GMII signal COL.

35.2.1.4.2 Semantics of the service primitive

PLS_SIGNAL.indicate (SIGNAL_STATUS)

The SIGNAL_STATUS parameter can take one of two values: SIGNAL_ERROR or NO_SIGNAL_ERROR. SIGNAL_STATUS assumes the value SIGNAL_ERROR when the GMII signal COL is asserted, and assumes the value NO_SIGNAL_ERROR when COL is de-asserted.

35.2.1.4.3 When generated

The PLS_SIGNAL.indicate service primitive is generated whenever SIGNAL_STATUS makes a transition from SIGNAL_ERROR to NO_SIGNAL_ERROR or vice versa.

35.2.1.5 Response to error indications from GMII

If, during frame reception, both RX_DV and RX_ER are asserted, the Reconciliation sublayer shall ensure that the MAC will detect a FrameCheckError in that frame.

Carrier is extended when RX_DV is not asserted and RX_ER is asserted with a proper encoding of RXD<7:0>. When a Carrier Extend Error is received during the extension, the Reconciliation sublayer shall send PLS_DATA.indicate values of ONE or ZERO and ensure that the MAC will detect a FrameCheckError in the sequence.

These requirements may be met by incorporating a function in the Reconciliation sublayer that produces a received frame data sequence delivered to the MAC sublayer that is guaranteed to not yield a valid CRC result, as specified by the algorithm in 3.2.8. This data sequence may be produced by substituting data delivered to the MAC.

Other techniques may be employed to respond to Data Reception Error or Carrier Extend Error provided that the result is that the MAC sublayer behaves as though a FrameCheckError occurred in the received frame.

35.2.1.6 Conditions for generation of TX_ER

If, during the process of transmitting a frame, it is necessary to request that the PHY deliberately corrupt the contents of the frame in such a manner that a receiver will detect the corruption with the highest degree of probability, then Transmit Error Propagation shall be asserted by the appropriate encoding of TX_ER, and TX_EN. Similarly, if during the process of transmitting carrier extension to a frame, it is necessary to request that the PHY deliberately corrupt the contents of the carrier extension in such a manner that a receiver will detect the corruption with the highest degree of probability, then Carrier Extend Error shall be signalled by the appropriate encoding of TXD<7:0>.

This capability has additional use within a repeater. For example, a repeater that detects an RX_ER during frame reception on an input port may propagate that error indication to its output ports by asserting TX_ER during the process of transmitting that frame.

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35.2.1.7 Mapping of PLS_DATA_VALID.indicate

35.2.1.7.1 Function

Map the primitive PLS_DATA_VALID.indicate to the GMII signals RX_DV, RX_ER and RXD<7:0>.

35.2.1.7.2 Semantics of the service primitive

PLS_DATA_VALID.indicate (DATA_VALID_STATUS)

The DATA_VALID_STATUS parameter can take one of two values: DATA_VALID or DATA_NOT_VALID. DATA_VALID_STATUS assumes the value DATA_VALID when the GMII signal RX_DV is asserted, or when RX_DV is not asserted, RX_ER is asserted and the values of RXD<7:0> indicate Carrier Extend or Carrier Extend Error. DATA_VALID_STATUS assumes the value DATA_NOT_VALID at all other times.

35.2.1.7.3 When generated

The PLS_DATA_VALID.indicate service primitive is generated by the Reconciliation sublayer whenever DATA_VALID_STATUS parameter changes from DATA_VALID to DATA_NOT_VALID or vice versa.

35.2.2 GMII signal functional specifications

35.2.2.1 GTX_CLK (1000 Mb/s transmit clock)

GTX_CLK is a continuous clock used for operation at 1000 Mb/s. GTX_CLK provides the timing reference for the transfer of the TX_EN, TX_ER, and TXD signals from the Reconciliation sublayer to the PHY. The values of TX_EN, TX_ER, and TXD are sampled by the PHY on the rising edge of GTX_CLK. GTX_CLK is sourced by the Reconciliation sublayer.

The GTX_CLK frequency is nominally 125 MHz, one-eighth of the transmit data rate.

35.2.2.2 RX_CLK (receive clock)

RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV, RX_ER and RXD signals from the PHY to the Reconciliation sublayer. RX_DV, RX_ER and RXD are sampled by the Reconciliation sublayer on the rising edge of RX_CLK. RX_CLK is sourced by the PHY.

The PHY may recover the RX_CLK from the received data or it may derive the RX_CLK reference from a local clock (e.g., GTX_CLK). When derived from the received data, RX_CLK shall have a frequency equal to one-eighth of the data rate of the received signal, and when derived from a local clock a nominal frequency of 125 MHz.

When the signal received from the medium is continuous and the PHY can recover the RX_CLK reference and supply the RX_CLK on a continuous basis, there is no need to transition between the recovered clock reference and a local clock reference on a frame-by-frame basis. If loss of received signal from the medium causes a PHY to lose the recovered RX_CLK reference, the PHY shall source the RX_CLK from a local clock reference.

Transitions from local clock to recovered clock or from recovered clock to local clock shall be made only while RX_DV and RX_ER are de-asserted. During the interval between the assertion of CRS and the assertion of RX_DV at the beginning of a frame, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition until the PHY has successfully locked onto the recovered clock. Following the de-assertion of RX_DV at the end of a frame, or the de-assertion of RX_ER at the end of carrier extension, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition for an interval that shall not exceed twice the nominal clock period.

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NOTE—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and GTX_CLK signals. See additional information in 35.4.

35.2.2.3 TX_EN (transmit enable)

TX_EN in combination with TX_ER indicates the Reconciliation sublayer is presenting data on the GMII for transmission. It shall be asserted by the Reconciliation sublayer synchronously with the first octet of the preamble and shall remain asserted while all octets to be transmitted are presented to the GMII. TX_EN shall be negated prior to the first rising edge of GTX_CLK following the final data octet of a frame. TX_EN is driven by the Reconciliation sublayer and shall transition synchronously with respect to the GTX_CLK.

Figure 35–3 depicts TX_EN behavior during a frame transmission with no collisions and without carrier extension or errors.

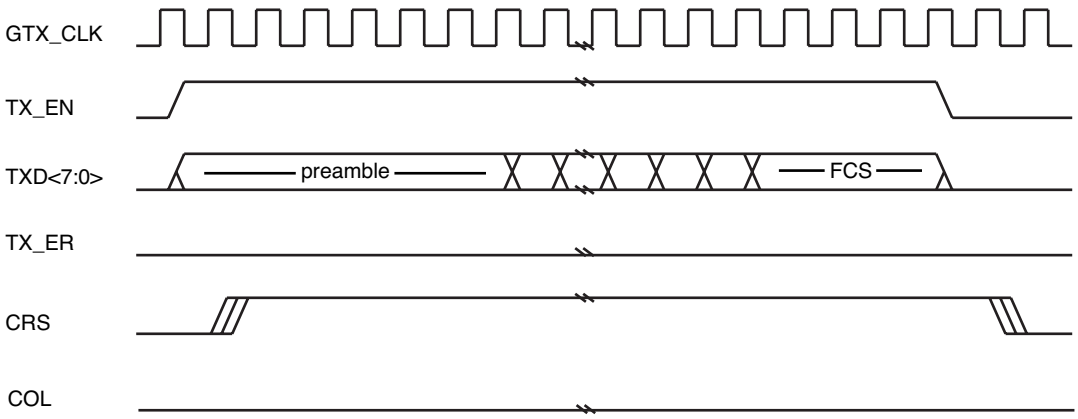


Figure 35–3—Basic frame transmission

35.2.2.4 TXD (transmit data)

TXD is a bundle of eight data signals (TXD<7:0>) that are driven by the Reconciliation sublayer. TXD<7:0> shall transition synchronously with respect to the GTX_CLK. For each GTX_CLK period in which TX_EN is asserted and TX_ER is de-asserted, data are presented on TXD<7:0> to the PHY for transmission. TXD<0> is the least significant bit. While TX_EN and TX_ER are both de-asserted, TXD<7:0> shall have no effect upon the PHY.

While TX_EN is de-asserted and TX_ER is asserted, TXD<7:0> are used to request the PHY to generate Carrier Extend or Carrier Extend Error code-groups. The use of TXD<7:0> during the transmission of a frame with carrier extension is described in 35.2.2.5. Carrier extension shall only be signalled immediately following the data portion of a frame.

Table 35–1 specifies the permissible encodings of TXD<7:0>, TX_EN, and TX_ER.

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Table 35–1—Permissible encodings of TXD<7:0>, TX_EN, and TX_ER

TX_EN	TX_ER	TXD<7:0>	Description	PLS_DATA.request parameter
0	0	00 through FF	Normal inter-frame	TRANSMIT_COMPLETE
0	1	00 through 0E	Reserved	—
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved	—
0	1	1F	Carrier Extend Error	EXTEND_ERROR (eight bits)
0	1	20 through FF	Reserved	—
1	0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1	1	00 through FF	Transmit error propagation	No applicable parameter
NOTE—Values in TXD<7:0> column are in hexadecimal.				

35.2.2.5 TX_ER (transmit coding error)

TX_ER is driven by the Reconciliation Sublayer and shall transition synchronously with respect to the GTX_CLK. When TX_ER is asserted for one or more TX_CLK periods while TX_EN is also asserted, the PHY shall emit one or more code-groups that are not part of the valid data or delimiter set somewhere in the frame being transmitted. The relative position of the error within the frame need not be preserved. Figure 35–4 shows the behavior of TX_ER during the transmission of a frame propagating an error.

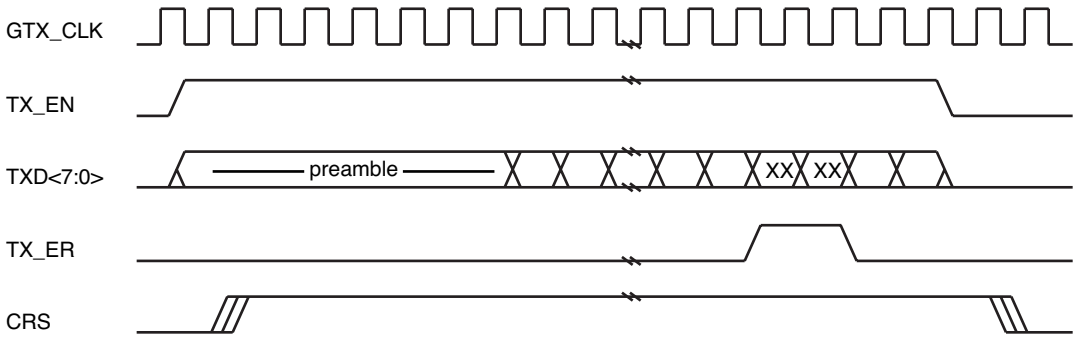


Figure 35–4—Propagating an error within a frame

Assertion of appropriate TXD values when TX_EN is de-asserted and TX_ER is asserted will cause the PHY to generate either Carrier Extend or Carrier Extend Error code-groups. The transition from TX_EN asserted and TX_ER de-asserted to TX_EN de-asserted and TX_ER asserted with TXD specifying Carrier Extend shall result in the PHY transmitting an end-of-packet delimiter as the initial code-groups of the carrier extension. Figures 35–5 and 35–6 show the behavior of TX_ER during the transmission of carrier extension. The propagation of an error in carrier extension is requested by holding TX_EN de-asserted and TX_ER asserted along with the appropriate value of TXD<7:0>.

Burst transmission of frames also uses carrier extension between frames of the burst. Figure 35–7 shows the behavior of TX_ER and TX_EN during burst transmission.

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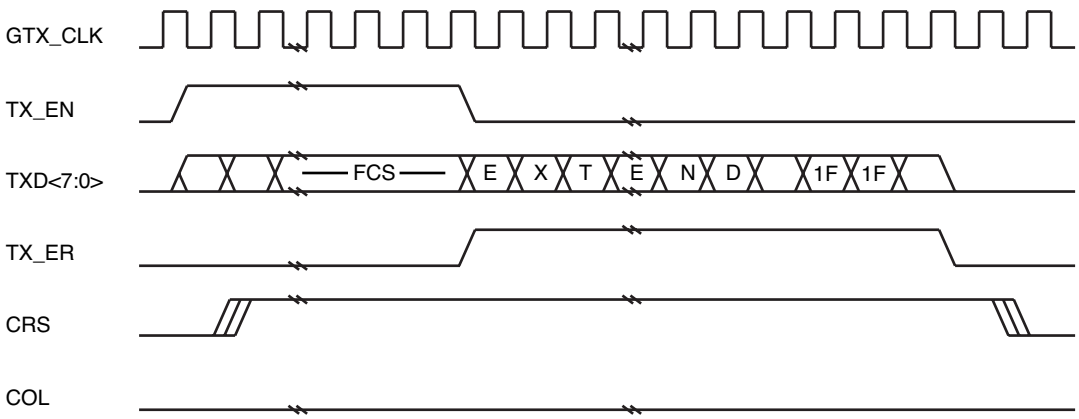


Figure 35–5—Propagating an error within carrier extension

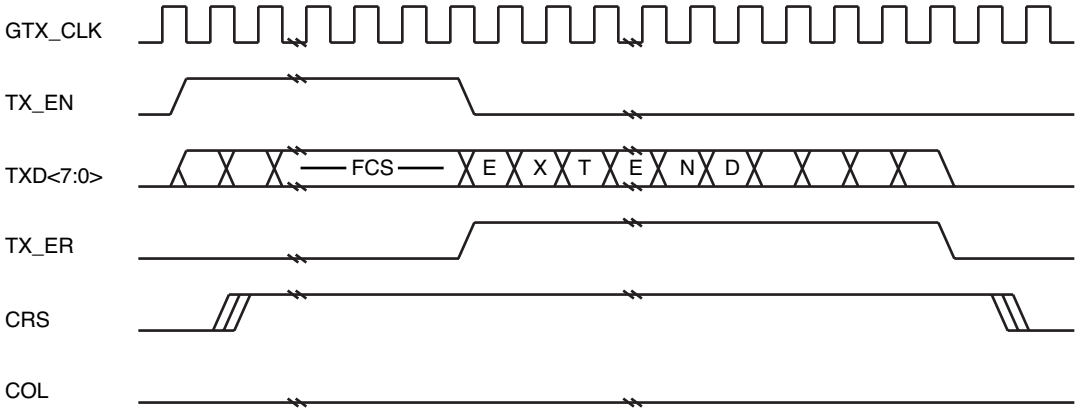


Figure 35–6—Transmission with carrier extension

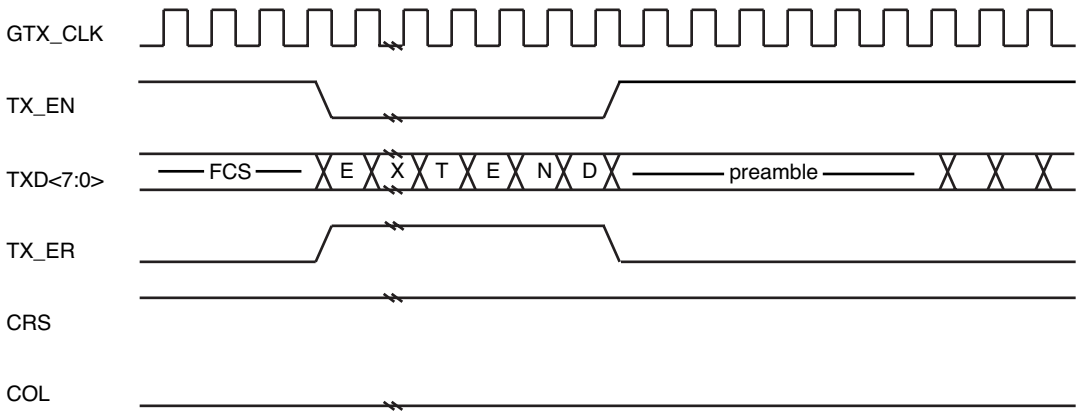


Figure 35–7—Burst transmission

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35.2.2.6 RX_DV (receive data valid)

RX_DV is driven by the PHY to indicate that the PHY is presenting recovered and decoded data on the RXD<7:0> bundle. RX_DV shall transition synchronously with respect to the RX_CLK. RX_DV shall be asserted continuously from the first recovered octet of the frame through the final recovered octet and shall be negated prior to the first rising edge of RX_CLK that follows the final octet. In order for a received frame to be correctly interpreted by the Reconciliation sublayer and the MAC sublayer, RX_DV must encompass the frame, starting no later than the Start Frame Delimiter (SFD) and excluding any End-of-Frame delimiter.

Figure 35–8 shows the behavior of RX_DV during frame reception with no errors or carrier extension.

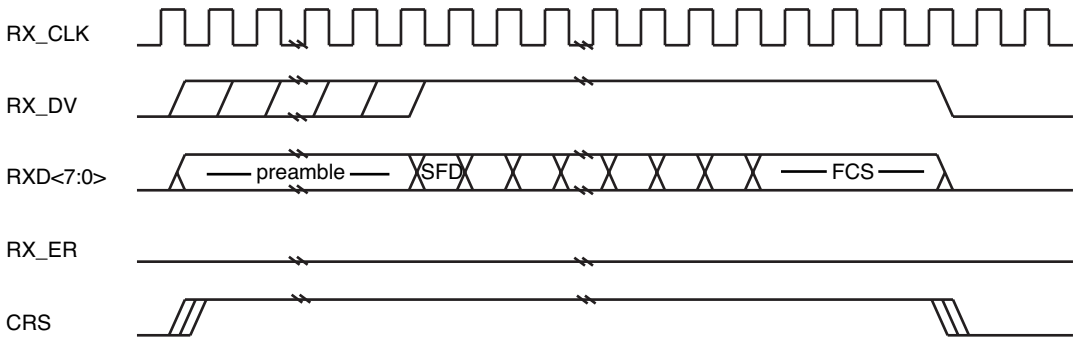


Figure 35–8—Basic frame reception

35.2.2.7 RXD (receive data)

RXD is a bundle of eight data signals (RXD<7:0>) that are driven by the PHY. RXD<7:0> shall transition synchronously with respect to RX_CLK. For each RX_CLK period in which RX_DV is asserted, RXD<7:0> transfer eight bits of recovered data from the PHY to the Reconciliation sublayer. RXD<0> is the least significant bit. Figure 35–8 shows the behavior of RXD<7:0> during frame reception.

While RX_DV is de-asserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal while driving the specific value listed in Table 35–2 onto RXD<7:0>. See 36.2.5.2.3 for a description of the conditions under which a PHY will provide a False Carrier indication.

In order for a frame to be correctly interpreted by the MAC sublayer, a completely formed SFD must be passed across the GMII.

In a DTE operating in half duplex mode, a PHY is not required to loop data transmitted on TXD<7:0> back to RXD<7:0> unless the loopback mode of operation is selected as defined in 22.2.4.1.2. In a DTE operating in full duplex mode, data transmitted on TXD <7:0> shall not be looped back to RXD <7:0> unless the loopback mode of operation is selected.

While RX_DV is de-asserted and RX_ER is asserted, a specific RXD<7:0> value is used to transfer recovered Carrier Extend from the PHY to the Reconciliation sublayer. A Carrier Extend Error is indicated by another specific value of RXD<7:0>. Figure 35–9 shows the behavior of RX_DV during frame reception with carrier extension. Carrier extension shall only be signalled immediately following frame reception.

Burst transmission of frames also uses carrier extension between frames of the burst. Figure 35–10 shows the behavior of RX_ER and RX_DV during burst reception.

Table 35–2 specifies the permissible encoding of RXD<7:0>, RX_ER, and RX_DV, along with the specific indication provided by each code.

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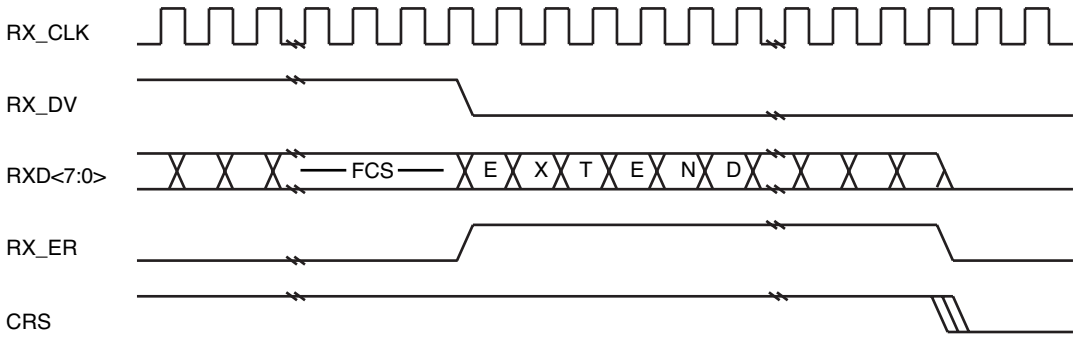


Figure 35–9—Frame reception with carrier extension

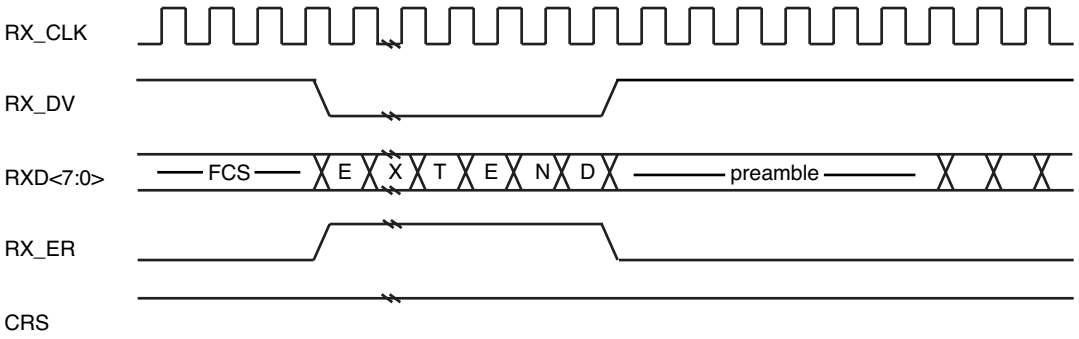


Figure 35–10—Burst reception

Table 35–2—Permissible encoding of RXD<7:0>, RX_ER, and RX_DV

RX_DV	RX_ER	RXD<7:0>	Description	PLS_DATA.indicate parameter
0	0	00 through FF	Normal inter-frame	No applicable parameter
0	1	00	Normal inter-frame	No applicable parameter
0	1	01 through 0D	Reserved	—
0	1	0E	False Carrier indication	No applicable parameter
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved	—
0	1	1F	Carrier Extend Error	ZERO, ONE (eight bits)
0	1	20 through FF	Reserved	—
1	0	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1	1	00 through FF	Data reception error	ZERO, ONE (eight bits)
NOTE—Values in RXD<7:0> column are in hexadecimal.				

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35.2.2.8 RX_ER (receive error)

RX_ER is driven by the PHY and shall transition synchronously with respect to RX_CLK. When RX_DV is asserted, RX_ER shall be asserted for one or more RX_CLK periods to indicate to the Reconciliation sublayer that an error (e.g., a coding error, or another error that the PHY is capable of detecting that may otherwise be undetectable at the MAC sublayer) was detected somewhere in the frame presently being transferred from the PHY to the Reconciliation sublayer.

The effect of RX_ER on the Reconciliation sublayer is defined in 35.2.1.5. Figure 35–11 shows the behavior of RX_ER during the reception of a frame with errors. Two independent error cases are illustrated. When RX_DV is asserted, assertion of RX_ER indicates an error within the data octets of a frame. An error within carrier extension is indicated by driving the appropriate value on RXD<7:0> while keeping RX_ER asserted.

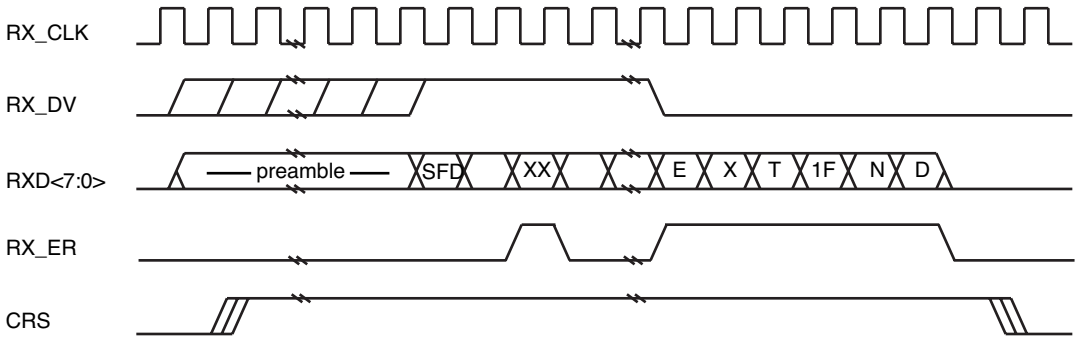


Figure 35–11—Two examples of reception with error

Assertion of RX_ER when RX_DV is de-asserted with specific RXD values indicates the decode of carrier extension by the PHY. The transition from RX_DV asserted and RX_ER de-asserted to RX_DV de-asserted and RX_ER asserted with RXD specifying Carrier Extend shall result in the Reconciliation sublayer indicating EXTEND INPUT_UNITs to the MAC. Figure 35–9 shows the behavior of RX_DV and RX_ER during frame reception with carrier extension.

While RX_DV is de-asserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal for at least one cycle of the RX_CLK while driving the appropriate value onto RXD<7:0>, as defined in Table 35–2. See 36.2.5.2.3 for a description of the conditions under which a PHY will provide a False Carrier indication. Figure 35–12 shows the behavior of RX_ER, RX_DV and RXD<7:0> during a False Carrier indication.

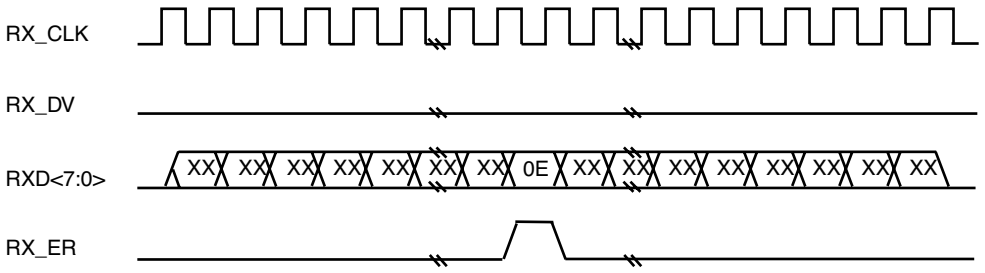


Figure 35–12—False Carrier indication

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35.2.2.9 CRS (carrier sense)

CRS is driven by the PHY. Except when used in a repeater, a PHY in half duplex mode shall assert CRS when either the transmit or receive medium is non-idle and shall de-assert CRS when both the transmit and receive media are idle. The PHY shall ensure that CRS remains asserted throughout the duration of a collision condition.

When used in a repeater, a PHY shall assert CRS when the receive medium is non-idle and shall de-assert CRS when the receive medium is idle.

CRS is not required to transition synchronously with respect to either the GTX_CLK or the RX_CLK.

The behavior of CRS is unspecified when the PHY is in full duplex mode.

Figure 35–3 and Figure 35–5 show the behavior of CRS during a frame transmission without a collision, while Figure 35–13 and Figure 35–14 show the behavior of CRS during a frame transmission with a collision.

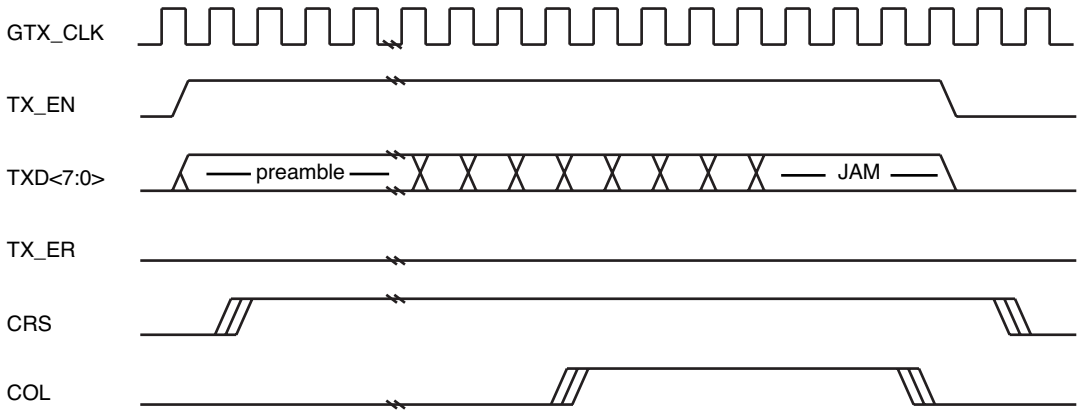


Figure 35–13—Transmission with collision

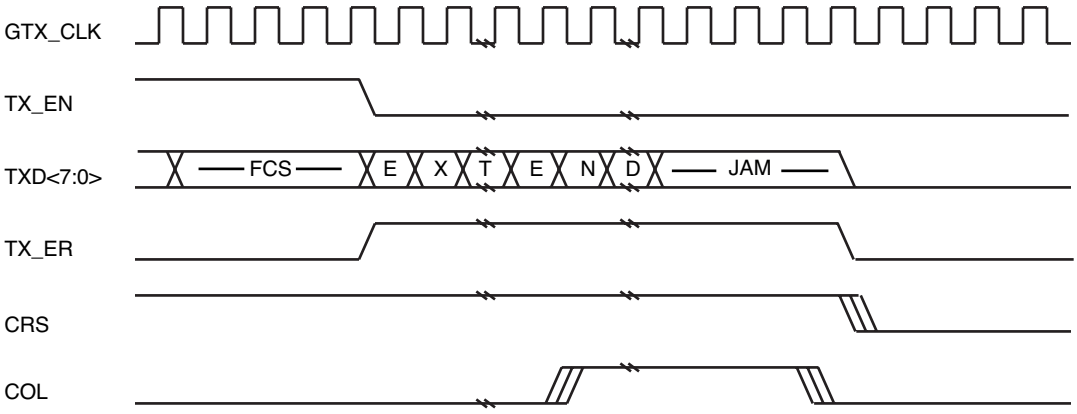


Figure 35–14—Transmission with collision in carrier extension

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35.2.2.10 COL (collision detected)

COL is driven by the PHY and shall be asserted upon detection of a collision on the medium, and shall remain asserted while the collision condition persists.

COL is not required to transition synchronously with respect to either the GTX_CLK or the RX_CLK.

The behavior of the COL signal is unspecified when the PHY is in full duplex mode.

Figure 35–13 and Figure 35–14 show the behavior of COL during a frame transmission with a collision.

35.2.2.11 MDC (management data clock)

MDC is specified in 22.2.2.11.

35.2.2.12 MDIO (management data input/output)

MDIO is specified in 22.2.2.12.

35.2.3 GMII data stream

Data frames transmitted through the GMII shall be transferred within the data stream shown in Figure 35–15.

<inter-frame><preamble><sfd><data><efd><extend>

Figure 35–15—GMII data stream

For the GMII, transmission and reception of each octet of data shall be as shown in Figure 35–16.

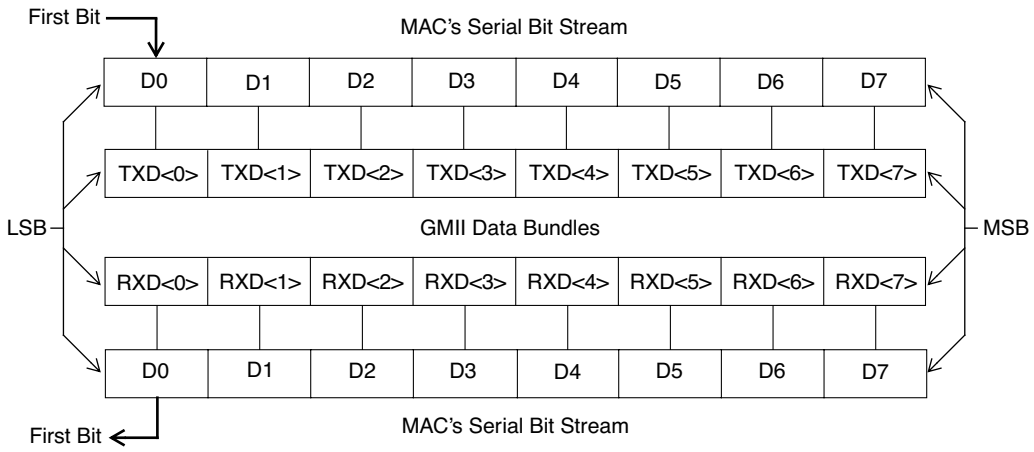


Figure 35–16—Relationship of data bundles to MAC serial bit stream

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35.2.3.1 Inter-frame <inter-frame>

The inter-frame <inter-frame> period on a GMII transmit or receive path is an interval during which no data activity occurs on the path. Between bursts or single frame transmissions, the absence of data activity on the receive path is indicated by the de-assertion of both RX_DV and RX_ER or the de-assertion of the RX_DV signal with an RXD<7:0> value of 00 hexadecimal. On the transmit path the absence of data activity is indicated by the de-assertion of both TX_EN and TX_ER.

Between frames within a burst, the inter-frame period is signalled as Carrier Extend on the GMII. As shown in Figure 35–7, this is done by asserting TX_ER with the appropriate encoding of TXD<7:0> simultaneous with the de-assertion of TX_EN on the transmit path; and, as shown in Figure 35–10, by asserting RX_ER with the appropriate encoding of RXD<7:0> simultaneous with the de-assertion of RX_DV on the receive path.

Within a burst, the MAC interFrameSpacing parameter defined in Clause 4, is measured from the de-assertion of the TX_EN signal to the assertion of the TX_EN signal, and between bursts measured from the de-assertion of the CRS signal to the assertion of the CRS signal.

35.2.3.2 Preamble <preamble> and start of frame delimiter <sfd>

35.2.3.2.1 Transmit case

The preamble <preamble> begins a frame transmission. The bit value of the preamble field at the GMII is unchanged from that specified in 4.2.5 and when generated by a MAC shall consist of 7 octets with the following bit values:

10101010 10101010 10101010 10101010 10101010 10101010 10101010

The SFD (Start Frame Delimiter) <sfd> indicates the start of a frame and immediately follows the preamble. The bit value of the SFD at the GMII is unchanged from that specified in 4.2.6, and is the following bit sequence:

10101011

The preamble and SFD are shown above with their bits ordered for serial transmission from left to right. As shown, the leftmost bit of each octet is the LSB of the octet and the rightmost bit of each octet is the MSB of the octet.

The preamble and SFD shall be transmitted through the GMII as octets starting from the assertion of TX_EN.

35.2.3.2.2 Receive case

The conditions for assertion of RX_DV are defined in 35.2.2.6. The operation of 1000 Mb/s PHYs can result in shrinkage of the preamble between transmission at the source GMII and reception at the destination GMII. Table 35–3 depicts the case where no preamble bytes are conveyed across the GMII. This case may not be possible with a specific PHY, but illustrates the minimum preamble with which MAC shall be able to operate. Table 35–4 depicts the case where the entire preamble is conveyed across the GMII.

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Table 35–3—Start of receive with no preamble preceding SFD

Signal	Bit values of octets received through GMII[a]			
RXD0	X	X	1[b]	D0[c]
RXD1	X	X	0	D1
RXD2	X	X	1	D2
RXD3	X	X	0	D3
RXD4	X	X	1	D4
RXD5	X	X	0	D5
RXD6	X	X	1	D6
RXD7	X	X	1	D7
RX_DV	0	0	1	1

[a]Leftmost octet is the first received.
[b]Start Frame Delimiter octet.
[c]D0 through D7 is the first octet of the PDU (first octet of the Destination Address).

Table 35–4—Start of receive with entire preamble preceding SFD

Signal	Bit values of octets received through GMII[a]									
RXD0	X	1	1	1	1	1	1	1	1[b]	D0[c]
RXD1	X	0	0	0	0	0	0	0	0	D1
RXD2	X	1	1	1	1	1	1	1	1	D2
RXD3	X	0	0	0	0	0	0	0	0	D3
RXD4	X	1	1	1	1	1	1	1	1	D4
RXD5	X	0	0	0	0	0	0	0	0	D5
RXD6	X	1	1	1	1	1	1	1	1	D6
RXD7	X	0	0	0	0	0	0	0	1	D7
RX_DV	0	1	1	1	1	1	1	1	1	1

[a]Leftmost octet is the first received.
[b]Start Frame Delimiter octet.
[c]D0 through D7 is the first octet of the PDU (first octet of the Destination Address).

35.2.3.3 Data <data>

The data <data> in a well-formed frame shall consist of a set of data octets.

35.2.3.4 End-of-Frame delimiter <efd>

De-assertion of the TX_EN signal constitutes an End-of-Frame delimiter <efd> for data conveyed on TXD<7:0>, and de-assertion of RX_DV constitutes an End-of-Frame delimiter for data conveyed on RXD<7:0>.

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35.2.3.5 Carrier extension <extend>

The Reconciliation sublayer signals carrier extension <extend> on the transmit path by the assertion of the TX_ER signal with the appropriate value of TXD<7:0> simultaneous with the de-assertion of the TX_EN signal. Carrier extension is signaled on the receive path by the assertion of the RX_ER signal with the appropriate encoding on RXD<7:0> simultaneous with the de-assertion of RX_DV. Carrier extension may not be present on all frames.

35.2.3.6 Definition of Start of Packet and End of Packet Delimiters

For the purposes of Clause 30 layer management, the Start of Packet delimiter is defined as the rising edge of RX_DV; and the End of Packet delimiter is defined as the falling edge of RX_DV. (See Clause 30.2.2.2.2.)

35.2.4 MAC delay constraints (with GMII)

A Gigabit Ethernet MAC with a GMII shall comply with the delay constraints in Table 35–5.

Table 35–5—MAC delay constraints (with GMII)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MAC ⇔ GMII	MAC transmit start to TX_EN = 1 sampled		48		GTX_CLK rising
	CRS assert to MAC detect[a]	0	48		
	CRS de-assert to MAC detect[a]	0	48		
	CRS assert to TX_EN = 1 sampled (worst-case nondeferred transmit)		112		GTX_CLK rising
	COL assert to MAC detect	0	48		
	COL de-assert to MAC detect	0	48		
	COL assert to TXD = Jam sampled (worst-case collision response)		112		GTX_CLK rising; first octet of jam

[a]For any given implementation: Max de-assert – Min. assert ≤ 16 bits.

35.2.5 Management functions

The GMII shall use the MII management register set specified in 22.2.4. The detailed description of some management registers are dependent on the PHY type and are specified in either 28.2.4 or 37.2.5.

35.3 Signal mapping

The GMII is specified such that implementors may share pins for implementation of the GMII, the MII specified in Clause 22 and the TBI specified in Clause 36. A recommended mapping of the signals for the GMII, MII, and TBI is shown in Table 35–6. Implementors using this recommended mapping are to comply with the GMII electrical characteristics in 35.4, MII electrical characteristics in 22.3, and the TBI electrical characteristics in 36.3 as appropriate for the implemented interfaces.

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In an implementation supporting the MII and GMII, some signal pins are not used in both interfaces. For example, the TXD and RXD data bundles are four bits wide for the MII and eight bits wide for the GMII. Also, the GTX_CLK is only used when operating as a GMII while TX_CLK is used when operating as an MII.

Similarly, an implementation supporting both the GMII and TBI interfaces will map TBI signals onto the GMII control signal pins of TX_ER, TX_EN, RX_ER, and RX_DV. The COL and CRS signals of the GMII have no corollary in the TBI.

It is recommended that unused signal pins be driven to a valid logic state.

Table 35–6—Signal mapping

GMII	MII	TBI
TX_ER	TX_ER	TX<9>
TX_EN	TX_EN	TX<8>
TXD<7>		TX<7>
TXD<6>		TX<6>
TXD<5>		TX<5>
TXD<4>		TX<4>
TXD<3>	TXD<3>	TX<3>
TXD<2>	TXD<2>	TX<2>
TXD<1>	TXD<1>	TX<1>
TXD<0>	TXD<0>	TX<0>
COL	COL	

GMII	MII	TBI
RX_ER	RX_ER	RX<9>
RX_DV	RX_DV	RX<8>
RXD<7>		RX<7>
RXD<6>		RX<6>
RXD<5>		RX<5>
RXD<4>		RX<4>
RXD<3>	RXD<3>	RX<3>
RXD<2>	RXD<2>	RX<2>
RXD<1>	RXD<1>	RX<1>
RXD<0>	RXD<0>	RX<0>
CRS	CRS	

35.4 Electrical characteristics

The electrical characteristics of the GMII are specified such that the GMII can be applied within a variety of 1000 Mb/s equipment types. The electrical specifications are optimized for an integrated circuit to integrated circuit application environment. This includes applications where a number of PHY integrated circuits may be connected to a single integrated circuit as may be found in a repeater. Though specified for use on a single circuit board, applications to a motherboard-to-daughterboard interconnection are not precluded.

The electrical characteristics specified in this clause apply to all GMII signals except MDIO and MDC. The electrical characteristics for MDIO and MDC are specified in 22.3.4.

35.4.1 DC characteristics

All GMII drivers and receivers shall comply with the dc parametric attributes specified in Table 35–7.

The potential applied to the input of a GMII receiver may exceed the potential of the receiver's power supply (i.e., a GMII driver powered from a 3.6 V supply driving V_{OH} into a GMII receiver powered from a 2.5 V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications.

35.4.2 AC characteristics

The GMII ac electrical characteristics are specified in a manner that allows the implementor flexibility in selecting the GMII topologies its devices support and the techniques used to achieve the specified characteristics.

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Table 35–7—DC specifications

Symbol	Parameter	Conditions		Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA	V_{CC} = Min	2.10	3.60	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0 mA	V_{CC} = Min	GND	0.50	V
V_{IH}	Input High Voltage			1.70	—	V
V_{IL}	Input Low Voltage			—	0.90	V
I_{IH}	Input High Current	V_{CC} = Max	V_{IN} = 2.1 V	—	40	µA
I_{IL}	Input Low Current	V_{CC} = Max	V_{IN} = 0.5 V	–600	—	µA

All GMII devices are required to support point-to-point links. The electrical length of the circuit board traces used to implement these links can be long enough to exhibit transmission line effects and require some form of termination. The implementor is allowed the flexibility to select the driver output characteristics and the termination technique and components to be used with its drivers for point-to-point links.

Implementors may elect to support other GMII topologies in addition to the point-to-point topology and may specify different termination techniques and components for each supported topology.

Since the output characteristics and output voltage waveforms of GMII drivers depend on the termination technique and the location of the termination components, the ac output characteristics of GMII drivers are not explicitly specified. Rather, the ac characteristics of the signal delivered to a GMII receiver are specified. These characteristics are independent of the topology and termination technique and apply uniformly to all GMII applications.

35.4.2.1 Signal Timing measurements

All GMII ac timing measurements are made at the GMII receiver input and are specified relative to the V_{IL_AC}(max) and V_{IH_AC}(min) thresholds.

The GTX_CLK and RX_CLK parameters t_{PERIOD}, t_{HIGH}, and t_{LOW} are defined in Figure 35–17. The GTX_CLK and RX_CLK parameters t_R and t_F and other transient performance specifications are defined in Figure 35–18. These parameters and the GTX_CLK and RX_CLK rising and falling slew rates are measured using the “GMII Point-to-Point Test Circuit” shown in Figure 35–20.

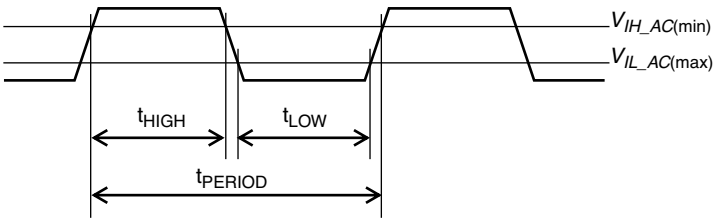


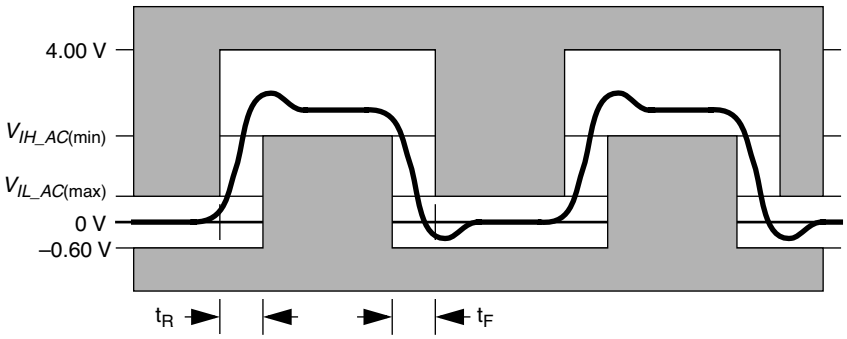
Figure 35–17—GTX_CLK and RX_CLK timing parameters at receiver input

The t_{SETUP} and t_{HOLD} parameters are defined in Figure 35–19. These parameters are measured using the “GMII Setup and Hold Time Test Circuit” shown in Figure 35–21.

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NOTE—As measured at input measurement point

Figure 35–18—GMII receiver input potential template

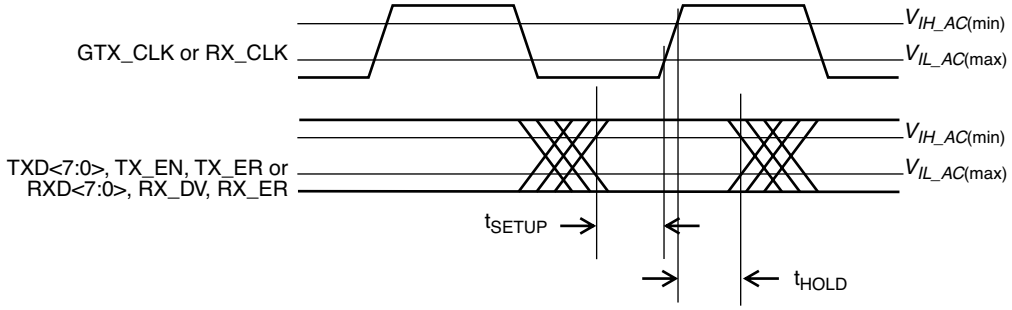


Figure 35–19—GMII signal timing at receiver input

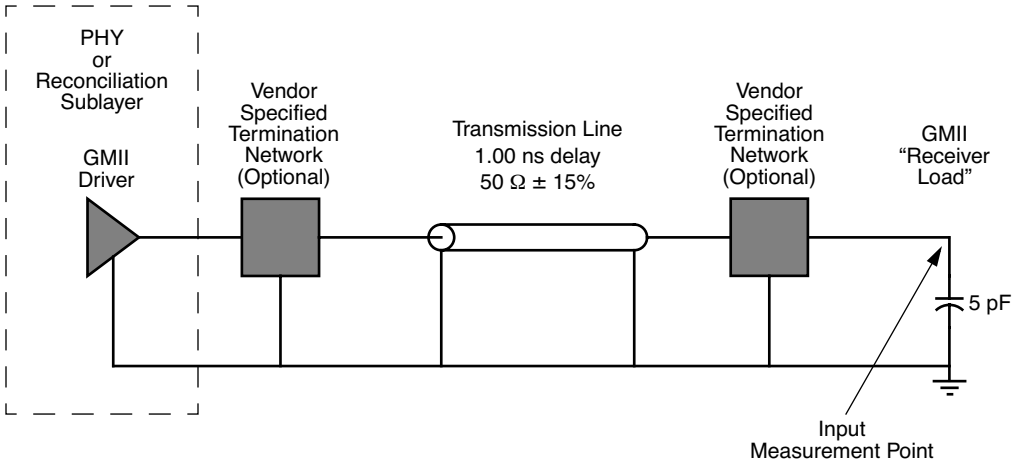


Figure 35–20—GMII point-to-point test circuit

35.4.2.2 GMII test circuit topology

The "GMII Point-to-Point Test Circuit" is defined in Figure 35–20. All parameter measurements made with this circuit are made at the "Input Measurement Point" defined in Figure 35–20. The 5 pF capacitor is included to approximate the input load of a GMII receiver. The termination networks used to implement the "GMII Point-to-Point Test Circuit" shall be those specified by the implementor of the GMII driver for 50 Ω ± 15%

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impedance transmission line point-to-point links. One or both of the termination networks specified by the implementor of the GMII driver may be straight-through connections if the networks are not needed to comply with the GMII ac and transient performance specifications.

The "GMII Point-to-Point Test Circuit" specifies a 1 ns transmission line. In a GMII implementation, the circuit board traces between the PHY and Reconciliation sublayer are not restricted to a delay of 1 ns.

The "GMII Setup and Hold Time Test Circuit" is defined in Figure 35–21. The circuit is comprised of the source of the synchronous GMII signal under test and its clock (the Reconciliation Layer or the PHY) and two "GMII Point-to-Point Test Circuits." One of the test circuits includes the GMII driver for the signal under test, the other test circuit includes the GMII driver for the clock that provides timing for the signal under test. The signal under test is measured at the "Signal Measurement Point" relative to its clock, which is measured at the "Clock Measurement Point" as defined in Figure 35–21.

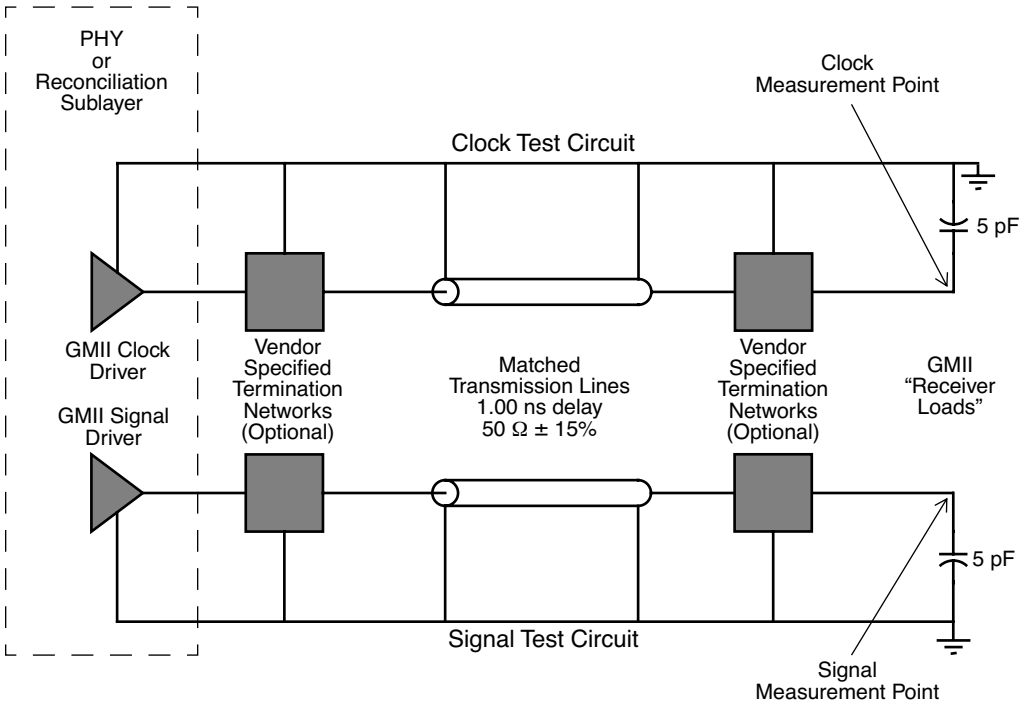


Figure 35–21—GMII setup and hold time test circuit

35.4.2.3 GMII ac specifications

A GMII driver, when used in combination with the termination networks specified by the implementor of the driver for a specific GMII topology, shall produce a potential at the input pin of any GMII receiver in that topology that complies with the input potential template shown in Figure 35–18. This requirement applies for all GMII signals and any GMII topology.

To ensure that all GMII devices support point-to-point links, a GMII driver, when driving the "GMII Point-to-Point Test Circuit" shown in Figure 35–20, shall produce a potential at the "Input Measurement Point" of the "GMII Point-to-Point Test Circuit" that complies with the input potential template shown in Figure 35–18.

All GMII signal sources, including the GMII drivers, GMII receivers and GMII signals shall comply with the ac specifications in Table 35–8.

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Table 35–8—AC specifications

Symbol	Parameter	Conditions	Min	Max	Units
V_{IL_AC}	Input Low Voltage ac	–	–	0.70	V
V_{IH_AC}	Input High Voltage ac	–	1.90	–	V
f_{FREQ}	GTX_CLK Frequency	–	125 – 100 ppm	125 + 100 ppm	MHz
t_{PERIOD}	GTX_CLK Period	–	7.50	8.50	ns
t_{PERIOD}	RX_CLK Period	–	7.50	–	ns
t_{HIGH}	GTX_CLK, RX_CLK Time High	–	2.50	–	ns
t_{LOW}	GTX_CLK, RX_CLK Time Low	–	2.50	–	ns
t_R	GTX_CLK, RX_CLK Rise Time	V_{IL_AC}(max) to V_{IH_AC}(min)	–	1.00	ns
t_F	GTX_CLK, RX_CLK Fall Time	V_{IH_AC}(min) to V_{IL_AC}(max)	–	1.00	ns
–	Magnitude of GTX_CLK, RX_CLK Slew Rate (rising)[a]	V_{IL_AC}(max) to V_{IH_AC}(min)	0.6	–	V/ns
–	Magnitude of GTX_CLK, RX_CLK Slew Rate (falling)[a]	V_{IH_AC}(min) to V_{IL_AC}(max)	0.6	–	V/ns
t_{SETUP}	TXD, TX_EN, TX_ER Setup to ↑ GTX_CLK and RXD, RX_DV, RX_ER Setup to ↑ RX_CLK	–	2.50	–	ns
t_{HOLD}	TXD, TX_EN, TX_ER Hold from ↑ GTX_CLK and RXD, RX_DV, RX_ER Hold from ↑ RX_CLK	–	0.50	–	ns
t_{SETUP} (RCVR)	TXD, TX_EN, TX_ER Setup to ↑ GTX_CLK and RXD, RX_DV, RX_ER Setup to ↑ RX_CLK	–	2.00	–	ns
t_{HOLD} (RCVR)	TXD, TX_EN, TX_ER Hold from ↑ GTX_CLK and RXD, RX_DV, RX_ER Hold from ↑ RX_CLK	–	0.00	–	ns

[a]Clock Skew rate is the instantaneous rate of change of the clock potential with respect to time (dV/dt), not an average value over the entire rise or fall time interval. Conformance with this specification guarantees that the clock signals will rise and fall monotonically through the switching region.

Two sets of setup and hold time parameters are specified in Table 35–8. The first set, t_{SETUP} and t_{HOLD}, applies to the source of a synchronous GMII signal and its clock and is measured using the "GMII Setup and Hold Time Test Circuit," which has transmission lines with matched propagation delays in the "clock" and "signal" paths. The second set, $t_{SETUP(RCVR)}$ and $t_{HOLD(RCVR)}$, applies to the GMII receiver and specifies the minimum setup and hold times available to the GMII receiver at its input pins. The difference between the two sets of setup and hold time parameters provides margin for a small amount of mismatch in the propagation delays of the "clock" path and the "signal" paths in GMII applications.

The GMII ac specifications in Table 35–8 and the transient performance specifications in Figure 35–18 shall be met under all combination of worst-case GMII driver process and supply potential variation, ambient temperature, transmission line impedance variation, and termination network component impedance variation.

Designers of components containing GMII receivers should note that there is no upper bound specified on the magnitude of the slew rate of signals that may be applied to the input of a GMII receiver. The high-

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frequency energy in a high slew rate (short rise time) signal can excite the parasitic reactances of the receiver package and input pad to such a degree that the signal at the receiver input pin and the signal at the input pad differ significantly. This is particularly true for GTX_CLK and RX_CLK, which transition at twice the rate of other signals in the interface.

35.5 Protocol Implementation Conformance Statement (PICS) proforma for Clause 35, Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII)[1]

35.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 35, Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII), shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

35.5.2 Identification

35.5.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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35.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2002, Clause 35, Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

35.5.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*EL	GMII electrical interface	35.4		O	Yes [ ] No [ ]
*G1	PHY support of GMII	35.1.3		O	Yes [ ] No [ ]
G2	Reconciliation sublayer support of GMII	35.1.3		O	Yes [ ] No [ ]
*HD	Half duplex capability	35.2.2.6		O	Yes [ ] No [ ]

35.5.3 PICS proforma tables for reconciliation sublayer and Gigabit Media Independent Interface

35.5.3.1 Mapping of PLS service primitives

Item	Feature	Subclause	Value/Comment	Status	Support
PL1	Response to error in frame	35.2.1.5	Must produce FrameCheckError when RX_DV and RX_ER are asserted	M	Yes [ ]
PL2	Response to error in extension	35.2.1.5	Must produce FrameCheckError on received Carrier Extend Error	M	Yes [ ]
PL2a	Propagation of errors in frame	35.2.1.6	Assert TX_ER while TX_EN asserted	O	Yes [ ]
PL3	Propagation of errors in extension	35.2.1.6	Must send ONE or ZERO and assert Carrier Extend Error to propagate error within carrier extension	O	Yes [ ] No [ ]

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35.5.3.2 GMII signal functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
SF1					
SF2	RX_CLK frequency	35.2.2.2	One eighth of received data rate or nominal 125 MHz.	M	Yes [ ]
SF3	RX_CLK source on loss of signal	35.2.2.2	Nominal clock reference (e.g., GTX_CLK)	M	Yes [ ]
SF4	RX_CLK transitions between recovered and nominal clock	35.2.2.2	While RX_DV de-asserted	M	Yes [ ]
SF5	RX_CLK max high/low time following de-assertion of RX_DV	35.2.2.2	Maximum 2 times the nominal period	M	Yes [ ]
SF6	TX_EN assertion	35.2.2.3	On first octet of preamble	M	Yes [ ]
SF7	TX_EN remains asserted	35.2.2.3	Stay asserted while all octets are transmitted over GMII	M	Yes [ ]
SF8	TX_EN negation	35.2.2.3	Before first GTX_CLK after final octet of frame	M	Yes [ ]
SF9	TX_EN transitions	35.2.2.3	Synchronous with GTX_CLK	M	Yes [ ]
SF10	TXD <7:0> transitions	35.2.2.4	Synchronous with GTX_CLK	M	Yes [ ]
SF11	TXD <7:0> effect on PHY while TX_EN and TX_ER are de-asserted	35.2.2.4	No effect	M	Yes [ ]
SF12	Signalling carrier extension	35.2.2.4	Only immediately following frame	M	Yes [ ]
SF13	TX_ER transitions	35.2.2.5	Synchronous with GTX_CLK	M	Yes [ ]
SF14	TX_ER effect on PHY while TX_EN is asserted	35.2.2.5	Cause PHY to emit invalid code-group	M	Yes [ ]
SF15	Transmission of end-of-packet delimiter	35.2.2.5	On de-assertion of TX_EN and simultaneous assertion of TX_ER	M	Yes [ ]
SF16	TX_ER implementation	35.2.2.5	At GMII of PHY	M	Yes [ ]
SF17	TX_ER implementation	35.2.2.5	Implemented if half duplex operation supported.	HD:M	Yes [ ] N/A [ ]
SF18	TX_ER driven	35.2.2.5	To valid state even if constant	M	Yes [ ]
SF19	RX_DV transitions	35.2.2.6	Synchronous with RX_CLK	M	Yes [ ]
SF20	RX_DV assertion	35.2.2.6	From first recovered octet to final octet of a frame	M	Yes [ ]
SF21	RX_DV negation	35.2.2.6	Before the first RX_CLK following the final octet of the frame	M	Yes [ ]
SF22	RXD <7:0> transitions	35.2.2.7	Synchronous with RX_CLK	M	Yes [ ]
SF22a	RXD loopback	35.2.2.7	No loopback unless loopback mode selected	M	Yes [ ]

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35.5.3.2 GMII signal functional specifications *(continued)*

Item	Feature	Subclause	Value/Comment	Status	Support
SF23	Signalling carrier extension	35.2.2.7	Only immediately following frame	M	Yes [ ]
SF24	RX_ER transitions	35.2.2.8	Synchronous with RX_CLK	M	Yes [ ]
SF25	RX_ER assertion	35.2.2.8	By PHY to indicate error	M	Yes [ ]
SF26	Generation of EXTEND	35.2.2.8	In response to simultaneous de-assertion of RX_DV and assertion of RX_ER by PHY	M	Yes [ ]
SF27	CRS assertion	35.2.2.9	By PHY when either transmit or receive is NON-IDLE	M	Yes [ ]
SF28	CRS de-assertion	35.2.2.9	By PHY when both transmit and receive are IDLE	M	Yes [ ]
SF29	CRS assertion during collision	35.2.2.9	Remain asserted throughout	M	Yes [ ]
SF30	CRS assertion—repeater	35.2.2.9	By repeater when receive is NON-IDLE	M	Yes [ ]
SF31	CRS de-assertion—repeater	35.2.2.9	By repeater when medium is IDLE	M	Yes [ ]
SF32	COL assertion	35.2.2.10	By PHY upon collision on medium	M	Yes [ ]
SF33	COL remains asserted while collision persists	35.2.2.10		M	Yes [ ]

35.5.3.3 Data stream structure

Item	Feature	Subclause	Value/Comment	Status	Support
DS1	Format of transmitted data stream	35.2.3	Per Figure 35–15	M	Yes [ ]
DS2	Transmission order	35.2.3	Per Figure 35–16	M	Yes [ ]
DS3	Preamble 7 octets long	35.2.3.2	10101010 10101010 10101010 10101010 10101010 10101010 10101010	M	Yes [ ]
DS4	Preamble and SFD transmission	35.2.3.2	Starting at assertion of TX_EN	M	Yes [ ]
DS5	Minimum preamble	35.2.3.2	MAC operates with minimum preamble	M	Yes [ ]
DS6	Data length	35.2.3.3	Set of octets	M	Yes [ ]

35.5.3.4 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
DC1	MAC delay	35.2.4	Comply with Table 35–5	M	Yes [ ]

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35.5.3.5 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Management registers	35.2.5	GMII base registers as defined in 22.4	M	Yes [ ]

35.5.3.6 Electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
EC1	DC specifications	35.4.1	All drivers and receivers per Table 35–7	EL:M	Yes [ ] N/A [ ]
EC3	AC and transient specifications	35.4.2.3	Under all combinations of worst case parameters	EL:M	Yes [ ] N/A [ ]
EC4	Topology input potential	35.4.2.3	Complies with Figure 35–18 at each receiver of topology	EL:M	Yes [ ] N/A [ ]
EC5	Tested driver input potential	35.4.2.3	Complies with Figure 35–18 as tested per Figure 35–20	EL:M	Yes [ ] N/A [ ]
EC6	Test circuit termination	35.4.2.2	As specified by GMII driver implementor	EL:M	Yes [ ] N/A [ ]
EC7	AC specifications	35.4.2.3	Per Table 35–8	EL:M	Yes [ ] N/A [ ]

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36. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X

36.1 Overview

36.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) sublayer that are common to a family of 1000 Mb/s Physical Layer implementations, collectively known as 1000BASE-X. There are currently three embodiments within this family: 1000BASE-CX, 1000BASE-LX, and 1000BASE-SX. The 1000BASE-CX embodiment specifies operation over a single copper media: two pairs of 150 Ω balanced copper cabling. 1000BASE-LX specifies operation over a pair of optical fibers using long-wavelength optical transmission. 1000BASE-SX specifies operation over a pair of optical fibers using short-wavelength optical transmission. The term 1000BASE-X is used when referring to issues common to any of the subvariants.

1000BASE-X is based on the Physical Layer standards developed by ANSI X3.230-1994 (Fibre Channel Physical and Signaling Interface). In particular, this standard uses the same 8B/10B coding as Fibre Channel, a PMA sublayer compatible with speed-enhanced versions of the ANSI 10-bit serializer chip, and similar optical and electrical specifications.

1000BASE-X PCS and PMA sublayers map the interface characteristics of the PMD sublayer (including MDI) to the services expected by the Reconciliation sublayer. 1000BASE-X can be extended to support any other full duplex medium requiring only that the medium be compliant at the PMD level.

36.1.2 Objectives

The following are the objectives of 1000BASE-X:

a) To support the CSMA/CD MAC;
b) To support the 1000 Mb/s repeater;
c) To provide for Auto-Negotiation among like 1000 Mb/s PMDs;
d) To provide 1000 Mb/s data rate at the GMII;
e) To support cable plants using 150 Ω balanced copper cabling, or optical fiber compliant with ISO/IEC 11801: 1995;
f) To allow for a nominal network extent of up to 3 km, including
    1) 150 Ω balanced links of 25 m span;
    2) one-repeater networks of 50 m span (using all 150 Ω balanced copper cabling);
    3) one-repeater networks of 200 m span (using fiber); and
    4) DTE/DTE links of 3000 m (using fiber);
g) To preserve full duplex behavior of underlying PMD channels;
h) To support a BER objective of 10^{-12}.

36.1.3 Relationship of 1000BASE-X to other standards

Figure 36–1 depicts the relationships among the 1000BASE-X sublayers (shown shaded), the CSMA/CD MAC and reconciliation layers, and the ISO/IEC 8802-2 LLC.

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36.1.4 Summary of 1000BASE-X sublayers

The following provides an overview of the 1000BASE-X sublayers.[2]

36.1.4.1 Physical Coding Sublayer (PCS)

The PCS interface is the Gigabit Media Independent Interface (GMII) that provides a uniform interface to the Reconciliation sublayer for all 1000 Mb/s PHY implementations (e.g., not only 1000BASE-X but also other possible types of gigabit PHY entities). 1000BASE-X provides services to the GMII in a manner analogous to how 100BASE-X provides services to the 100 Mb/s MII.

The 1000BASE-X PCS provides all services required by the GMII, including

a) Encoding (decoding) of GMII data octets to (from) ten-bit code-groups (8B/10B) for communication with the underlying PMA;
b) Generating Carrier Sense and Collision Detect indications for use by PHY's half duplex clients;
c) Managing the Auto-Negotiation process, and informing the management entity via the GMII when the PHY is ready for use.

36.1.4.2 Physical Medium Attachment (PMA) sublayer

The PMA provides a medium-independent means for the PCS to support the use of a range of serial-bit-oriented physical media. The 1000BASE-X PMA performs the following functions:

a) Mapping of transmit and receive code-groups between the PCS and PMA via the PMA Service Interface;
b) Serialization (deserialization) of code-groups for transmission (reception) on the underlying serial PMD;
c) Recovery of clock from the 8B/10B-coded data supplied by the PMD;
d) Mapping of transmit and receive bits between the PMA and PMD via the PMD Service Interface;
e) Data loopback at the PMD Service Interface.

36.1.4.3 Physical Medium Dependent (PMD) sublayer

1000BASE-X physical layer signaling for fiber and copper media is adapted from ANSI X3.230-1994 (FC-PH), Clauses 6 and 7 respectively. These clauses define 1062.5 Mb/s, full duplex signaling systems that accommodate single-mode optical fiber, multimode optical fiber, and 150 Ω balanced copper cabling. 1000BASE-X adapts these basic physical layer specifications for use with the PMD sublayer and mediums specified in Clause 38 and Clause 39.

The MDI, logically subsumed within each PMD subclause, is the actual medium attachment, including connectors, for the various supported media.

Figure 36–1 depicts the relationship between 1000BASE-X and its associated PMD sublayers.

36.1.5 Inter-sublayer interfaces

There are a number of interfaces employed by 1000BASE-X. Some (such as the PMA Service Interface) use an abstract service model to define the operation of the interface. An optional physical instantiation of the PCS Interface has been defined. It is called the GMII (Gigabit Media Independent Interface). An optional physical instantiation of the PMA Service Interface has also been defined (see 36.3.3). It is adapted from

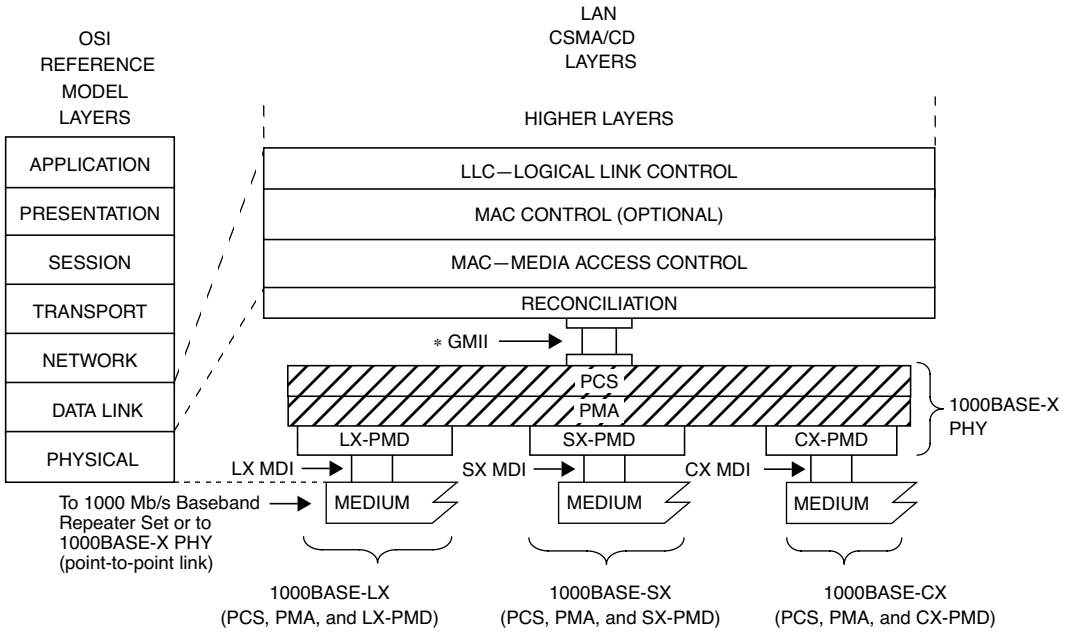
[2]The 1000BASE-X PHY consists of that portion of the Physical Layer between the MDI and GMII consisting of the PCS, PMA, and PMD sublayers. The 1000BASE-X PHY is roughly analogous to the 100BASE-X PHY.

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MDI=MEDIUM DEPENDENT INTERFACE
GMII=GIGABIT MEDIA INDEPENDENT INTERFACE
PCS=PHYSICAL CODING SUBLAYER
PMA=PHYSICAL MEDIUM ATTACHMENT
PHY=PHYSICAL LAYER DEVICE
PMD=PHYSICAL MEDIUM DEPENDENT
LX-PMD=PMD FOR FIBER—LONG WAVELENGTH, Clause 38
SX-PMD=PMD FOR FIBER—SHORT WAVELENGTH, Clause 38
CX-PMD=PMD FOR 150 Ω BALANCED COPPER CABLING, Clause 39

NOTE—The PMD sublayers are mutually independent.

* GMII is optional.

Figure 36–1—Relationship of 1000BASE-X and the PMDs

ANSI Technical Report TR/X3.18-1997 (Fibre Channel—10-bit Interface). Figure 36–2 depicts the relationship and mapping of the services provided by all of the interfaces relevant to 1000BASE-X.

It is important to note that, while this specification defines interfaces in terms of bits, octets, and code-groups, implementors may choose other data path widths for implementation convenience. The only exceptions are a) the GMII, which, when implemented at an observable interconnection port, uses an octet-wide data path as specified in Clause 35, b) the PMA Service Interface, which, when physically implemented as the TBI (Ten-Bit Interface) at an observable interconnection port, uses a 10-bit wide data path as specified in 36.3.3, and c) the MDI, which uses a serial, physical interface.

36.1.6 Functional block diagram

Figure 36–2 provides a functional block diagram of the 1000BASE-X PHY.

36.1.7 State diagram conventions

The body of this standard is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2.

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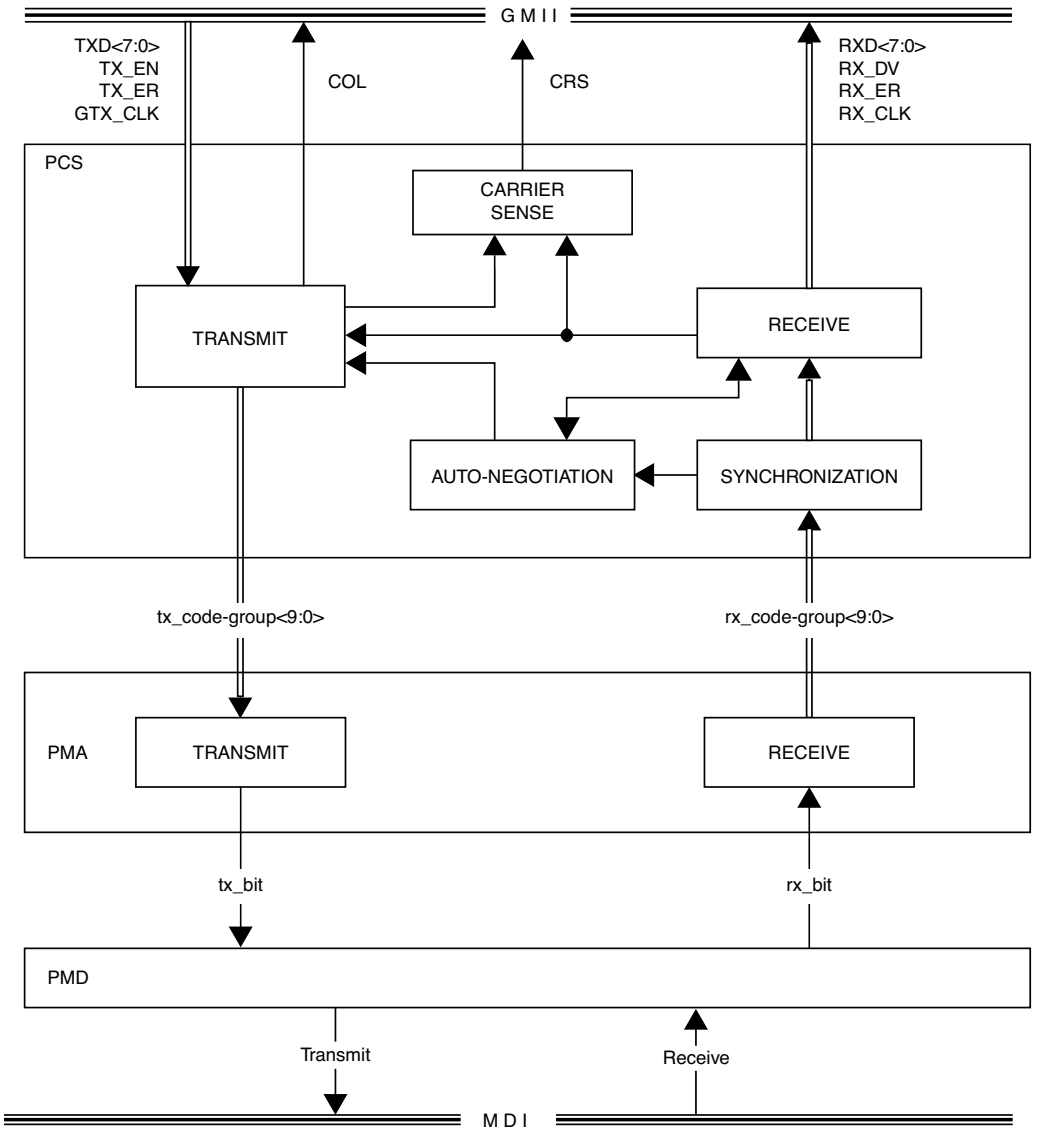


Figure 36–2—Functional block diagram

36.2 Physical Coding Sublayer (PCS)

36.2.1 PCS Interface (GMII)

The PCS Service Interface allows the 1000BASE-X PCS to transfer information to and from a PCS client. PCS clients include the MAC (via the Reconciliation sublayer) and repeater. The PCS Interface is precisely defined as the Gigabit Media Independent Interface (GMII) in Clause 35.

In this clause, the setting of GMII variables to TRUE or FALSE is equivalent, respectively, to “asserting” or “de-asserting” them as specified in Clause 35.

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36.2.2 Functions within the PCS

The PCS comprises the PCS Transmit, Carrier Sense, Synchronization, PCS Receive, and Auto-Negotiation processes for 1000BASE-X. The PCS shields the Reconciliation sublayer (and MAC) from the specific nature of the underlying channel. When communicating with the GMII, the PCS uses an octet-wide, synchronous data path, with packet delimiting being provided by separate transmit control signals (TX_EN and TX_ER) and receive control signals (RX_DV and RX_ER). When communicating with the PMA, the PCS uses a ten-bit wide, synchronous data path, which conveys ten-bit code-groups. At the PMA Service Interface, code-group alignment and MAC packet delimiting are made possible by embedding special non-data code-groups in the transmitted code-group stream. The PCS provides the functions necessary to map packets between the GMII format and the PMA Service Interface format.

The PCS Transmit process continuously generates code-groups based upon the TXD <7:0>, TX_EN, and TX_ER signals on the GMII, sending them immediately to the PMA Service Interface via the PMA_UNITDATA.request primitive. The PCS Transmit process generates the GMII signal COL based on whether a reception is occurring simultaneously with transmission. Additionally, it generates the internal flag, transmitting, for use by the Carrier Sense process. The PCS Transmit process monitors the Auto-Negotiation process xmit flag to determine whether to transmit data or reconfigure the link.

The Carrier Sense process controls the GMII signal CRS (see Figure 36–8).

The PCS Synchronization process continuously accepts code-groups via the PMA_UNITDATA.indicate primitive and conveys received code-groups to the PCS Receive process via the SYNC_UNITDATA.indicate primitive. The PCS Synchronization process sets the sync_status flag to indicate whether the PMA is functioning dependably (as well as can be determined without exhaustive error-rate analysis).

The PCS Receive process continuously accepts code-groups via the SYNC_UNITDATA.indicate primitive. The PCS Receive process monitors these code-groups and generates RXD <7:0>, RX_DV, and RX_ER on the GMII, and the internal flag, receiving, used by the Carrier Sense and Transmit processes.

The PCS Auto-Negotiation process sets the xmit flag to inform the PCS Transmit process to either transmit normal idles interspersed with packets as requested by the GMII or to reconfigure the link. The PCS Auto-Negotiation process is specified in Clause 37.

36.2.3 Use of code-groups

The PCS maps GMII signals into ten-bit code groups, and vice versa, using an 8B/10B block coding scheme. Implicit in the definition of a code-group is an establishment of code-group boundaries by a PMA code-group alignment function as specified in 36.3.2.4. Code-groups are unobservable and have no meaning outside the PCS. The PCS functions ENCODE and DECODE generate, manipulate, and interpret code-groups as provided by the rules in 36.2.4.

36.2.4 8B/10B transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link. The encodings defined by the transmission code ensure that sufficient transitions are present in the PHY bit stream to make clock recovery possible at the receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, some of the special code-groups of the transmission code contain a distinct and easily recognizable bit pattern that assists a receiver in achieving code-group alignment on the incoming PHY bit stream. The 8B/10B transmission code specified for use in this standard has a high transition density, is a run-length-limited code, and is dc-balanced. The transition density of the 8B/10B symbols ranges from 3 to 8 transitions per symbol.

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The definition of the 8B/10B transmission code in this standard is identical to that specified in ANSI X3.230-1994 (FC-PH), Clause 11. The relationship of code-group bit positions to PMA and other PCS constructs is illustrated in Figure 36–3.

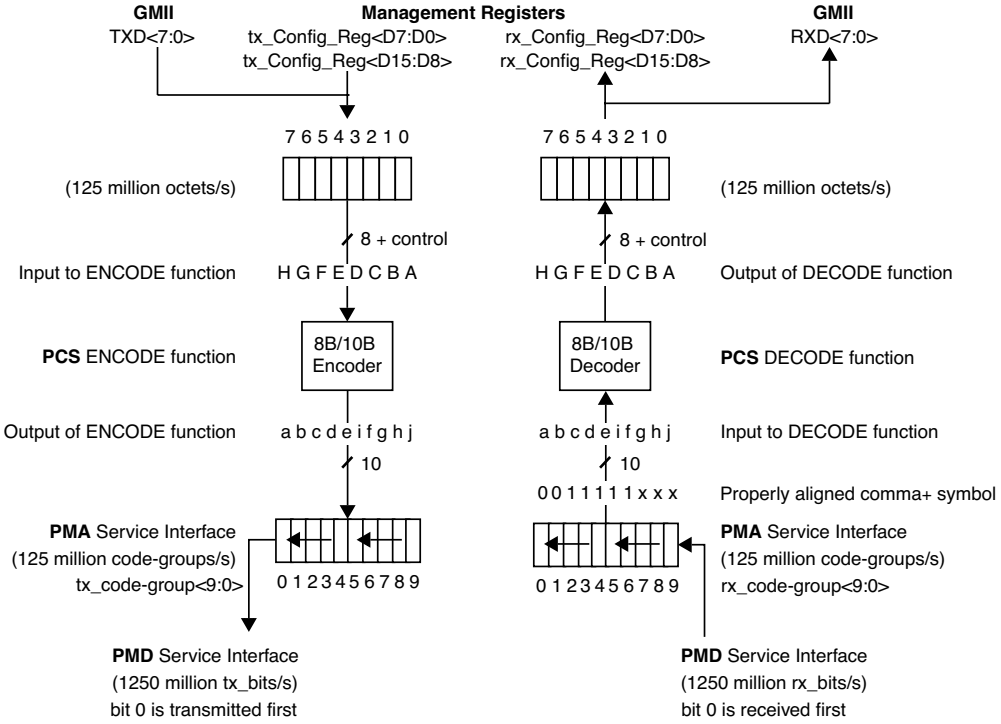


Figure 36–3—PCS reference diagram

36.2.4.1 Notation conventions

8B/10B transmission code uses letter notation for describing the bits of an unencoded information octet and a single control variable. Each bit of the unencoded information octet contains either a binary zero or a binary one. A control variable, Z, has either the value D or the value K. When the control variable associated with an unencoded information octet contains the value D, the associated encoded code-group is referred to as a data code-group. When the control variable associated with an unencoded information octet contains the value K, the associated encoded code-group is referred to as a special code-group.

The bit notation of A,B,C,D,E,F,G,H for an unencoded information octet is used in the description of the 8B/10B transmission code. The bits A,B,C,D,E,F,G,H are translated to bits a,b,c,d,e,i,f,g,h,j of 10-bit transmission code-groups. 8B/10B code-group bit assignments are illustrated in Figure 36–3. Each valid code-group has been given a name using the following convention: /Dx.y/ for the 256 valid data code-groups, and /Kx.y/ for special control code-groups, where x is the decimal value of bits EDCBA, and y is the decimal value of bits HGF.

36.2.4.2 Transmission order

Code-group bit transmission order is illustrated in Figure 36–3.

Code-groups within multi-code-group ordered_sets (as specified in Table 36–3) are transmitted sequentially beginning with the special code-group used to distinguish the ordered_set (e.g., /K28.5/) and proceeding code-group by code-group from left to right within the definition of the ordered_set until all code-groups of the ordered_set are transmitted.

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The first code-group of every multi-code-group ordered_set is transmitted in an even-numbered code-group position counting from the first code-group after a reset or power-on. Subsequent code-groups continuously alternate as odd and even-numbered code-groups.

The contents of a packet are transmitted sequentially beginning with the ordered_set used to denote the Start_of_Packet (the SPD delimiter) and proceeding code-group by code-group from left to right within the definition of the packet until the ordered_set used to denote the End_of_Packet (the EPD delimiter) is transmitted.

36.2.4.3 Valid and invalid code-groups

Table 36–1a defines the valid data code-groups (D code-groups) of the 8B/10B transmission code. Table 36–2 defines the valid special code-groups (K code-groups) of the code. The tables are used for both generating valid code-groups (encoding) and checking the validity of received code-groups (decoding). In the tables, each octet entry has two columns that represent two (not necessarily different) code-groups. The two columns correspond to the valid code-group based on the current value of the running disparity (Current RD – or Current RD +). Running disparity is a binary parameter with either the value negative (–) or the value positive (+). Annex 36B provides several 8B/10B transmission code running disparity calculation examples.

36.2.4.4 Running disparity rules

After powering on or exiting a test mode, the transmitter shall assume the negative value for its initial running disparity. Upon transmission of any code-group, the transmitter shall calculate a new value for its running disparity based on the contents of the transmitted code-group.

After powering on or exiting a test mode, the receiver should assume either the positive or negative value for its initial running disparity. Upon the reception of any code-group, the receiver determines whether the code-group is valid or invalid and calculates a new value for its running disparity based on the contents of the received code-group.

The following rules for running disparity shall be used to calculate the new running disparity value for code-groups that have been transmitted (transmitter's running disparity) and that have been received (receiver's running disparity).

Running disparity for a code-group is calculated on the basis of sub-blocks, where the first six bits (abcdei) form one sub-block (six-bit sub-block) and the second four bits (fghj) form the other sub-block (four-bit sub-block). Running disparity at the beginning of the six-bit sub-block is the running disparity at the end of the last code-group. Running disparity at the beginning of the four-bit sub-block is the running disparity at the end of the six-bit sub-block. Running disparity at the end of the code-group is the running disparity at the end of the four-bit sub-block.

Running disparity for the sub-blocks is calculated as follows:

a) Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the six-bit sub-block if the six-bit sub-block is 000111, and it is positive at the end of the four-bit sub-block if the four-bit sub-block is 0011;
b) Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at the end of the six-bit sub-block if the six-bit sub-block is 111000, and it is negative at the end of the four-bit sub-block if the four-bit sub-block is 1100;
c) Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

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NOTE—All sub-blocks with equal numbers of zeros and ones are disparity neutral. In order to limit the run length of 0's or 1's between sub-blocks, the 8B/10B transmission code rules specify that sub-blocks encoded as 000111 or 0011 are generated only when the running disparity at the beginning of the sub-block is positive; thus, running disparity at the end of these sub-blocks is also positive. Likewise, sub-blocks containing 111000 or 1100 are generated only when the running disparity at the beginning of the sub-block is negative; thus, running disparity at the end of these sub-blocks is also negative.

36.2.4.5 Generating code-groups

The appropriate entry in either Table 36–1a or Table 36–2 is found for each octet for which a code-group is to be generated (encoded). The current value of the transmitter's running disparity shall be used to select the code-group from its corresponding column. For each code-group transmitted, a new value of the running disparity is calculated. This new value is used as the transmitter's current running disparity for the next octet to be encoded and transmitted.

36.2.4.6 Checking the validity of received code-groups

The following rules shall be used to determine the validity of received code groups:

a) The column in Tables 36–1a and 36–2 corresponding to the current value of the receiver's running disparity is searched for the received code-group;
b) If the received code-group is found in the proper column, according to the current running disparity, then the code-group is considered valid and, for data code-groups, the associated data octet determined (decoded);
c) If the received code-group is not found in that column, then the code-group is considered invalid;
d) Independent of the code-group's validity, the received code-group is used to calculate a new value of running disparity. The new value is used as the receiver's current running disparity for the next received code-group.

Detection of an invalid code-group does not necessarily indicate that the code-group in which the invalid code-group was detected is in error. Invalid code-groups may result from a prior error which altered the running disparity of the PHY bit stream but which did not result in a detectable error at the code-group in which the error occurred.

The number of invalid code-groups detected is proportional to the bit-error-rate (BER) of the link. Link error monitoring may be performed by counting invalid code-groups.

36.2.4.7 Ordered_sets

Eight ordered_sets, consisting of a single special code-group or combinations of special and data code-groups are specifically defined. Ordered_sets which include /K28.5/ provide the ability to obtain bit and code-group synchronization and establish ordered_set alignment (see 36.2.4.9 and 36.3.2.4). Ordered_sets provide for the delineation of a packet and synchronization between the transmitter and receiver circuits at opposite ends of a link. Table 36–3 lists the defined ordered_sets.

36.2.4.7.1 Ordered_set rules

Ordered_sets are specified according to the following rules:

a) Ordered_sets consist of either one, two, or four code-groups;
b) The first code-group of all ordered_sets is always a special code-group;
c) The second code-group of all multi-code-group ordered_sets is always a data code-group. The second code-group is used to distinguish the ordered set from all other ordered sets. The second code-group provides a high bit transition density.

Table 36–3 lists the defined ordered_sets.

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Table 36–1a—Valid data code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD – abcdei fghj	Current RD + abcdei fghj
D0.0	00	000 00000	100111 0100	011000 1011
D1.0	01	000 00001	011101 0100	100010 1011
D2.0	02	000 00010	101101 0100	010010 1011
D3.0	03	000 00011	110001 1011	110001 0100
D4.0	04	000 00100	110101 0100	001010 1011
D5.0	05	000 00101	101001 1011	101001 0100
D6.0	06	000 00110	011001 1011	011001 0100
D7.0	07	000 00111	111000 1011	000111 0100
D8.0	08	000 01000	111001 0100	000110 1011
D9.0	09	000 01001	100101 1011	100101 0100
D10.0	0A	000 01010	010101 1011	010101 0100
D11.0	0B	000 01011	110100 1011	110100 0100
D12.0	0C	000 01100	001101 1011	001101 0100
D13.0	0D	000 01101	101100 1011	101100 0100
D14.0	0E	000 01110	011100 1011	011100 0100
D15.0	0F	000 01111	010111 0100	101000 1011
D16.0	10	000 10000	011011 0100	100100 1011
D17.0	11	000 10001	100011 1011	100011 0100
D18.0	12	000 10010	010011 1011	010011 0100
D19.0	13	000 10011	110010 1011	110010 0100
D20.0	14	000 10100	001011 1011	001011 0100
D21.0	15	000 10101	101010 1011	101010 0100
D22.0	16	000 10110	011010 1011	011010 0100
D23.0	17	000 10111	111010 0100	000101 1011
D24.0	18	000 11000	110011 0100	001100 1011
D25.0	19	000 11001	100110 1011	100110 0100
D26.0	1A	000 11010	010110 1011	010110 0100
D27.0	1B	000 11011	110110 0100	001001 1011
D28.0	1C	000 11100	001110 1011	001110 0100
D29.0	1D	000 11101	101110 0100	010001 1011
D30.0	1E	000 11110	011110 0100	100001 1011
D31.0	1F	000 11111	101011 0100	010100 1011
D0.1	20	001 00000	100111 1001	011000 1001
D1.1	21	001 00001	011101 1001	100010 1001
D2.1	22	001 00010	101101 1001	010010 1001
D3.1	23	001 00011	110001 1001	110001 1001
D4.1	24	001 00100	110101 1001	001010 1001
D5.1	25	001 00101	101001 1001	101001 1001
D6.1	26	001 00110	011001 1001	011001 1001
D7.1	27	001 00111	111000 1001	000111 1001
D8.1	28	001 01000	111001 1001	000110 1001
D9.1	29	001 01001	100101 1001	100101 1001
D10.1	2A	001 01010	010101 1001	010101 1001
D11.1	2B	001 01011	110100 1001	110100 1001
D12.1	2C	001 01100	001101 1001	001101 1001
D13.1	2D	001 01101	101100 1001	101100 1001
D14.1	2E	001 01110	011100 1001	011100 1001
D15.1	2F	001 01111	010111 1001	101000 1001
D16.1	30	001 10000	011011 1001	100100 1001
D17.1	31	001 10001	100011 1001	100011 1001
D18.1	32	001 10010	010011 1001	010011 1001
D19.1	33	001 10011	110010 1001	110010 1001
D20.1	34	001 10100	001011 1001	001011 1001
D21.1	35	001 10101	101010 1001	101010 1001
D22.1	36	001 10110	011010 1001	011010 1001
D23.1	37	001 10111	111010 1001	000101 1001
D24.1	38	001 11000	110011 1001	001100 1001
D25.1	39	001 11001	100110 1001	100110 1001
D26.1	3A	001 11010	010110 1001	010110 1001
D27.1	3B	001 11011	110110 1001	001001 1001

(continued)

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Table 36–1b—Valid data code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD –	Current RD +
			abcdei fghj	abcdei fghj
D28.1	3C	001 11100	001110 1001	001110 1001
D29.1	3D	001 11101	101110 1001	010001 1001
D30.1	3E	001 11110	011110 1001	100001 1001
D31.1	3F	001 11111	101011 1001	010100 1001
D0.2	40	010 00000	100111 0101	011000 0101
D1.2	41	010 00001	011101 0101	100010 0101
D2.2	42	010 00010	101101 0101	010010 0101
D3.2	43	010 00011	110001 0101	110001 0101
D4.2	44	010 00100	110101 0101	001010 0101
D5.2	45	010 00101	101001 0101	101001 0101
D6.2	46	010 00110	011001 0101	011001 0101
D7.2	47	010 00111	111000 0101	000111 0101
D8.2	48	010 01000	111001 0101	000110 0101
D9.2	49	010 01001	100101 0101	100101 0101
D10.2	4A	010 01010	010101 0101	010101 0101
D11.2	4B	010 01011	110100 0101	110100 0101
D12.2	4C	010 01100	001101 0101	001101 0101
D13.2	4D	010 01101	101100 0101	101100 0101
D14.2	4E	010 01110	011100 0101	011100 0101
D15.2	4F	010 01111	010111 0101	101000 0101
D16.2	50	010 10000	011011 0101	100100 0101
D17.2	51	010 10001	100011 0101	100011 0101
D18.2	52	010 10010	010011 0101	010011 0101
D19.2	53	010 10011	110010 0101	110010 0101
D20.2	54	010 10100	001011 0101	001011 0101
D21.2	55	010 10101	101010 0101	101010 0101
D22.2	56	010 10110	011010 0101	011010 0101
D23.2	57	010 10111	111010 0101	000101 0101
D24.2	58	010 11000	110011 0101	001100 0101
D25.2	59	010 11001	100110 0101	100110 0101
D26.2	5A	010 11010	010110 0101	010110 0101
D27.2	5B	010 11011	110110 0101	001001 0101
D28.2	5C	010 11100	001110 0101	001110 0101
D29.2	5D	010 11101	101110 0101	010001 0101
D30.2	5E	010 11110	011110 0101	100001 0101
D31.2	5F	010 11111	101011 0101	010100 0101
D0.3	60	011 00000	100111 0011	011000 1100
D1.3	61	011 00001	011101 0011	100010 1100
D2.3	62	011 00010	101101 0011	010010 1100
D3.3	63	011 00011	110001 1100	110001 0011
D4.3	64	011 00100	110101 0011	001010 1100
D5.3	65	011 00101	101001 1100	101001 0011
D6.3	66	011 00110	011001 1100	011001 0011
D7.3	67	011 00111	111000 1100	000111 0011
D8.3	68	011 01000	111001 0011	000110 1100
D9.3	69	011 01001	100101 1100	100101 0011
D10.3	6A	011 01010	010101 1100	010101 0011
D11.3	6B	011 01011	110100 1100	110100 0011
D12.3	6C	011 01100	001101 1100	001101 0011
D13.3	6D	011 01101	101100 1100	101100 0011
D14.3	6E	011 01110	011100 1100	011100 0011
D15.3	6F	011 01111	010111 0011	101000 1100
D16.3	70	011 10000	011011 0011	100100 1100
D17.3	71	011 10001	100011 1100	100011 0011
D18.3	72	011 10010	010011 1100	010011 0011
D19.3	73	011 10011	110010 1100	110010 0011
D20.3	74	011 10100	001011 1100	001011 0011
D21.3	75	011 10101	101010 1100	101010 0011
D22.3	76	011 10110	011010 1100	011010 0011
D23.3	77	011 10111	111010 0011	000101 1100

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Table 36–1c—Valid data code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD –	Current RD +
			abcdei fghj	abcdei fghj
D24.3	78	011 11000	110011 0011	001100 1100
D25.3	79	011 11001	100110 1100	100110 0011
D26.3	7A	011 11010	010110 1100	010110 0011
D27.3	7B	011 11011	110110 0011	001001 1100
D28.3	7C	011 11100	001110 1100	001110 0011
D29.3	7D	011 11101	101110 0011	010001 1100
D30.3	7E	011 11110	011110 0011	100001 1100
D31.3	7F	011 11111	101011 0011	010100 1100
D0.4	80	100 00000	100111 0010	011000 1101
D1.4	81	100 00001	011101 0010	100010 1101
D2.4	82	100 00010	101101 0010	010010 1101
D3.4	83	100 00011	110001 1101	110001 0010
D4.4	84	100 00100	110101 0010	001010 1101
D5.4	85	100 00101	101001 1101	101001 0010
D6.4	86	100 00110	011001 1101	011001 0010
D7.4	87	100 00111	111000 1101	000111 0010
D8.4	88	100 01000	111001 0010	000110 1101
D9.4	89	100 01001	100101 1101	100101 0010
D10.4	8A	100 01010	010101 1101	010101 0010
D11.4	8B	100 01011	110100 1101	110100 0010
D12.4	8C	100 01100	001101 1101	001101 0010
D13.4	8D	100 01101	101100 1101	101100 0010
D14.4	8E	100 01110	011100 1101	011100 0010
D15.4	8F	100 01111	010111 0010	101000 1101
D16.4	90	100 10000	011011 0010	100100 1101
D17.4	91	100 10001	100011 1101	100011 0010
D18.4	92	100 10010	010011 1101	010011 0010
D19.4	93	100 10011	110010 1101	110010 0010
D20.4	94	100 10100	001011 1101	001011 0010
D21.4	95	100 10101	101010 1101	101010 0010
D22.4	96	100 10110	011010 1101	011010 0010
D23.4	97	100 10111	111010 0010	000101 1101
D24.4	98	100 11000	110011 0010	001100 1101
D25.4	99	100 11001	100110 1101	100110 0010
D26.4	9A	100 11010	010110 1101	010110 0010
D27.4	9B	100 11011	110110 0010	001001 1101
D28.4	9C	100 11100	001110 1101	001110 0010
D29.4	9D	100 11101	101110 0010	010001 1101
D30.4	9E	100 11110	011110 0010	100001 1101
D31.4	9F	100 11111	101011 0010	010100 1101
D0.5	A0	101 00000	100111 1010	011000 1010
D1.5	A1	101 00001	011101 1010	100010 1010
D2.5	A2	101 00010	101101 1010	010010 1010
D3.5	A3	101 00011	110001 1010	110001 1010
D4.5	A4	101 00100	110101 1010	001010 1010
D5.5	A5	101 00101	101001 1010	101001 1010
D6.5	A6	101 00110	011001 1010	011001 1010
D7.5	A7	101 00111	111000 1010	000111 1010
D8.5	A8	101 01000	111001 1010	000110 1010
D9.5	A9	101 01001	100101 1010	100101 1010
D10.5	AA	101 01010	010101 1010	010101 1010
D11.5	AB	101 01011	110100 1010	110100 1010
D12.5	AC	101 01100	001101 1010	001101 1010
D13.5	AD	101 01101	101100 1010	101100 1010
D14.5	AE	101 01110	011100 1010	011100 1010
D15.5	AF	101 01111	010111 1010	101000 1010
D16.5	B0	101 10000	011011 1010	100100 1010
D17.5	B1	101 10001	100011 1010	100011 1010
D18.5	B2	101 10010	010011 1010	010011 1010
D19.5	B3	101 10011	110010 1010	110010 1010

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Table 36–1d—Valid data code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD –	Current RD +
			abcdei fghj	abcdei fghj
D20.5	B4	101 10100	001011 1010	001011 1010
D21.5	B5	101 10101	101010 1010	101010 1010
D22.5	B6	101 10110	011010 1010	011010 1010
D23.5	B7	101 10111	111010 1010	000101 1010
D24.5	B8	101 11000	110011 1010	001100 1010
D25.5	B9	101 11001	100110 1010	100110 1010
D26.5	BA	101 11010	010110 1010	010110 1010
D27.5	BB	101 11011	110110 1010	001001 1010
D28.5	BC	101 11100	001110 1010	001110 1010
D29.5	BD	101 11101	101110 1010	010001 1010
D30.5	BE	101 11110	011110 1010	100001 1010
D31.5	BF	101 11111	101011 1010	010100 1010
D0.6	C0	110 00000	100111 0110	011000 0110
D1.6	C1	110 00001	011101 0110	100010 0110
D2.6	C2	110 00010	101101 0110	010010 0110
D3.6	C3	110 00011	110001 0110	110001 0110
D4.6	C4	110 00100	110101 0110	001010 0110
D5.6	C5	110 00101	101001 0110	101001 0110
D6.6	C6	110 00110	011001 0110	011001 0110
D7.6	C7	110 00111	111000 0110	000111 0110
D8.6	C8	110 01000	111001 0110	000110 0110
D9.6	C9	110 01001	100101 0110	100101 0110
D10.6	CA	110 01010	010101 0110	010101 0110
D11.6	CB	110 01011	110100 0110	110100 0110
D12.6	CC	110 01100	001101 0110	001101 0110
D13.6	CD	110 01101	101100 0110	101100 0110
D14.6	CE	110 01110	011100 0110	011100 0110
D15.6	CF	110 01111	010111 0110	101000 0110
D16.6	D0	110 10000	011011 0110	100100 0110
D17.6	D1	110 10001	100011 0110	100011 0110
D18.6	D2	110 10010	010011 0110	010011 0110
D19.6	D3	110 10011	110010 0110	110010 0110
D20.6	D4	110 10100	001011 0110	001011 0110
D21.6	D5	110 10101	101010 0110	101010 0110
D22.6	D6	110 10110	011010 0110	011010 0110
D23.6	D7	110 10111	111010 0110	000101 0110
D24.6	D8	110 11000	110011 0110	001100 0110
D25.6	D9	110 11001	100110 0110	100110 0110
D26.6	DA	110 11010	010110 0110	010110 0110
D27.6	DB	110 11011	110110 0110	001001 0110
D28.6	DC	110 11100	001110 0110	001110 0110
D29.6	DD	110 11101	101110 0110	010001 0110
D30.6	DE	110 11110	011110 0110	100001 0110
D31.6	DF	110 11111	101011 0110	010100 0110
D0.7	E0	111 00000	100111 0001	011000 1110
D1.7	E1	111 00001	011101 0001	100010 1110
D2.7	E2	111 00010	101101 0001	010010 1110
D3.7	E3	111 00011	110001 1110	110001 0001
D4.7	E4	111 00100	110101 0001	001010 1110
D5.7	E5	111 00101	101001 1110	101001 0001
D6.7	E6	111 00110	011001 1110	011001 0001
D7.7	E7	111 00111	111000 1110	000111 0001
D8.7	E8	111 01000	111001 0001	000110 1110
D9.7	E9	111 01001	100101 1110	100101 0001
D10.7	EA	111 01010	010101 1110	010101 0001
D11.7	EB	111 01011	110100 1110	110100 1000
D12.7	EC	111 01100	001101 1110	001101 0001
D13.7	ED	111 01101	101100 1110	101100 1000
D14.7	EE	111 01110	011100 1110	011100 1000
D15.7	EF	111 01111	010111 0001	101000 1110

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Table 36–1e—Valid data code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD – abcdei fghj	Current RD + abcdei fghj
D16.7	F0	111 10000	011011 0001	100100 1110
D17.7	F1	111 10001	100011 0111	100011 0001
D18.7	F2	111 10010	010011 0111	010011 0001
D19.7	F3	111 10011	110010 1110	110010 0001
D20.7	F4	111 10100	001011 0111	001011 0001
D21.7	F5	111 10101	101010 1110	101010 0001
D22.7	F6	111 10110	011010 1110	011010 0001
D23.7	F7	111 10111	111010 0001	000101 1110
D24.7	F8	111 11000	110011 0001	001100 1110
D25.7	F9	111 11001	100110 1110	100110 0001
D26.7	FA	111 11010	010110 1110	010110 0001
D27.7	FB	111 11011	110110 0001	001001 1110
D28.7	FC	111 11100	001110 1110	001110 0001
D29.7	FD	111 11101	101110 0001	010001 1110
D30.7	FE	111 11110	011110 0001	100001 1110
D31.7	FF	111 11111	101011 0001	010100 1110

(concluded)

Table 36–2—Valid special code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD – abcdei fghj	Current RD + abcdei fghj	Notes
K28.0	1C	000 11100	001111 0100	110000 1011	1
K28.1	3C	001 11100	001111 1001	110000 0110	1,2
K28.2	5C	010 11100	001111 0101	110000 1010	1
K28.3	7C	011 11100	001111 0011	110000 1100	1
K28.4	9C	100 11100	001111 0010	110000 1101	1
K28.5	BC	101 11100	001111 1010	110000 0101	2
K28.6	DC	110 11100	001111 0110	110000 1001	1
K28.7	FC	111 11100	001111 1000	110000 0111	1,2
K23.7	F7	111 10111	111010 1000	000101 0111	
K27.7	FB	111 11011	110110 1000	001001 0111	
K29.7	FD	111 11101	101110 1000	010001 0111	
K30.7	FE	111 11110	011110 1000	100001 0111	

NOTE 1—Reserved.

NOTE 2—Contains a comma.

36.2.4.8 /K28.5/ code-group considerations

The /K28.5/ special code-group is chosen as the first code-group of all ordered_sets that are signaled repeatedly and for the purpose of allowing a receiver to synchronize to the incoming bit stream (i.e., /C/ and /I/), for the following reasons:

a) Bits abcdeif make up a comma. The comma can be used to easily find and verify code-group and ordered_set boundaries of the rx_bit stream.
b) Bits ghj of the encoded code-group present the maximum number of transitions, simplifying receiver acquisition of bit synchronization.

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Table 36–3—Defined ordered_sets

Code	Ordered_Set	Number of Code-Groups	Encoding
/C/	**Configuration**		Alternating /C1/ and /C2/
/C1/	Configuration 1	4	/K28.5/D21.5/Config_Reg[a]
/C2/	Configuration 2	4	/K28.5/D2.2/Config_Reg[a]
/I/	**IDLE**		Correcting /I1/, Preserving /I2/
/I1/	IDLE 1	2	/K28.5/D5.6/
/I2/	IDLE 2	2	/K28.5/D16.2/
	Encapsulation		
/R/	Carrier_Extend	1	/K23.7/
/S/	Start_of_Packet	1	/K27.7/
/T/	End_of_Packet	1	/K29.7/
/V/	Error_Propagation	1	/K30.7/

[a]Two data code-groups representing the Config_Reg value.

36.2.4.9 Comma considerations

The seven bit comma string is defined as either b'0011111' (comma+) or b'1100000' (comma-). The /I/ and /C/ ordered_sets and their associated protocols are specified to ensure that comma+ is transmitted with either equivalent or greater frequency than comma- for the duration of their transmission. This is done to ensure compatibility with common components.

The comma contained within the /K28.1/, /K28.5/, and /K28.7/ special code-groups is a singular bit pattern, which, in the absence of transmission errors, cannot appear in any other location of a code-group and cannot be generated across the boundaries of any two adjacent code-groups with the following exception:

The /K28.7/ special code-group is used by 1000BASE-X for diagnostic purposes only (see Annex 36A). This code-group, if followed by any of the following special or data code-groups: /K28.x/, /D3.x/, /D11.x/, /D12.x/, /D19.x/, /D20.x/, or /D28.x/, where x is a value in the range 0 to 7, inclusive, causes a comma to be generated across the boundaries of the two adjacent code-groups. A comma across the boundaries of any two adjacent code-groups may cause code-group realignment (see 36.3.2.4).

36.2.4.10 Configuration (/C/)

Configuration, defined as the continuous repetition of the ordered sets /C1/ and /C2/, is used to convey the 16-bit Configuration Register (Config_Reg) to the link partner. See Clause 37 for a description of the Config_Reg contents.

The ordered_sets, /C1/ and /C2/, are defined in Table 36–3. The /C1/ ordered_set is defined such that the running disparity at the end of the first two code-groups is opposite that of the beginning running disparity. The /C2/ ordered_set is defined such that the running disparity at the end of the first two code-groups is the same as the beginning running disparity. For a constant Config_Reg value, the running disparity after transmitting the sequence /C1/C2/ will be the opposite of what it was at the start of the sequence. This ensures that K28.5s containing comma+ will be sent during configuration.

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36.2.4.11 Data (/D/)

A data code-group, when not used to distinguish or convey information for a defined ordered_set, conveys one octet of arbitrary data between the GMII and the PCS. The sequence of data code-groups is arbitrary, where any data code-group can be followed by any other data code-group. Data code-groups are coded and decoded but not interpreted by the PCS. Successful decoding of the data code-groups depends on proper receipt of the Start_of_Packet delimiter, as defined in 36.2.4.13 and the checking of validity, as defined in 36.2.4.6.

36.2.4.12 IDLE (/I/)

IDLE ordered_sets (/I/) are transmitted continuously and repetitively whenever the GMII is idle (TX_EN and TX_ER are both inactive). /I/ provides a continuous fill pattern to establish and maintain clock synchronization. /I/ is emitted from, and interpreted by, the PCS. /I/ consists of one or more consecutively transmitted /I1/ or /I2/ ordered_sets, as defined in Table 36–3.

The /I1/ ordered_set is defined such that the running disparity at the end of the transmitted /I1/ is opposite that of the beginning running disparity. The /I2/ ordered_set is defined such that the running disparity at the end of the transmitted /I2/ is the same as the beginning running disparity. The first /I/ following a packet or Configuration ordered_set restores the current positive or negative running disparity to a negative value. All subsequent /I/s are /I2/ to ensure negative ending running disparity.

Distinct carrier events are separated by /I/s.

Implementations of this standard may benefit from the ability to add or remove /I2/ from the code-group stream one /I2/ at a time without altering the beginning running disparity associated with the code-group subsequent to the removed /I2/.

A received ordered set which consists of two code-groups, the first of which is /K28.5/ and the second of which is a data code-group other than /D21.5/ or /D2.2/ is treated as an /I/ ordered_set.

36.2.4.13 Start_of_Packet (SPD) delimiter

A Start_of_Packet delimiter (SPD) is used to delineate the starting boundary of a data transmission sequence and to authenticate carrier events. Upon each fresh assertion of TX_EN by the GMII, and subsequent to the completion of PCS transmission of the current ordered_set, the PCS replaces the current octet of the MAC preamble with SPD. Upon initiation of packet reception, the PCS replaces the received SPD delimiter with the data octet value associated with the first preamble octet. A SPD delimiter consists of the code-group /S/, as defined in Table 36–3.

SPD follows /I/ for a single packet or the first packet in a burst.

SPD follows /R/ for the second and subsequent packets of a burst.

36.2.4.14 End_of_Packet delimiter (EPD)

An End_of_Packet delimiter (EPD) is used to delineate the ending boundary of a packet. The EPD is transmitted by the PCS following each de-assertion of TX_EN on the GMII, which follows the last data octet comprising the FCS of the MAC packet. On reception, EPD is interpreted by the PCS as terminating a packet. A EPD delimiter consists of the code-groups /T/R/R/ or /T/R/K28.5/. The code-group /T/ is defined in Table 36–3. See 36.2.4.15 for the definition of code-groups used for /R/. /K28.5/ normally occurs as the first code-group of the /I/ ordered_set. See 36.2.4.12 for the definition of code-groups used for /I/.

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The receiver considers the MAC interpacket gap (IPG) to have begun two octets prior to the transmission of /I/. For example, when a packet is terminated by EPD, the /T/R/ portion of the EPD occupies part of the region considered by the MAC to be the IPG.

36.2.4.14.1 EPD rules

a) The PCS transmits a /T/R/ following the last data octet from the MAC;
b) If the MAC indicates carrier extension to the PCS, Carrier_Extend rules are in effect. See 36.2.4.15.1;
c) If the MAC does not indicate carrier extension to the PCS, perform the following:
   1) If /R/ is transmitted in an even-numbered code-group position, the PCS appends a single additional /R/ to the code-group stream to ensure that the subsequent /I/ is aligned on an even-numbered code-group boundary and EPD transmission is complete;
   2) The PCS transmits /I/.

36.2.4.15 Carrier_Extend (/R/)

Carrier_Extend (/R/) is used for the following purposes:

a) Carrier extension: Used by the MAC to extend the duration of the carrier event. When used for this purpose, carrier extension is emitted from and interpreted by the MAC and coded to and decoded from the corresponding code-group by the PCS. In order to extend carrier, the GMII must deassert TX_EN. The deassertion of TX_EN and simultaneous assertion of TX_ER causes the PCS to emit an /R/ with a two-octet delay, which gives the PCS time to complete its EPD before commencing transmissions. The number of /R/ code-groups emitted from the PCS equals the number of GMII GTX_CLK periods during which it extends carrier;
b) Packet separation: Carrier extension is used by the MAC to separate packets within a burst of packets. When used for this purpose, carrier extension is emitted from and interpreted by the MAC and coded to and decoded from the corresponding code-group by the PCS;
c) EPD2: The first /R/ following the /T/ in the End_of_Packet delimiters /T/R/I/ or /T/R/R/I/;
d) EPD3: The second /R/ following the /T/ in the End_of_Packet delimiter /T/R/R/I/. This /R/ is used, if necessary, to pad the only or last packet of a burst of packets so that the subsequent /I/ is aligned on an even-numbered code-group boundary. When used for this purpose, Carrier_Extend is emitted from, and interpreted by, the PCS. An EPD of /T/R/R/ results in one /R/ being delivered to the PCS client (see 36.2.4.14.1).

Carrier_Extend consists of one or more consecutively transmitted /R/ ordered_sets, as defined in Table 36–3.

36.2.4.15.1 Carrier_Extend rules

a) If the MAC indicates carrier extension to the PCS, the initial /T/R/ is followed by one /R/ for each octet of carrier extension received from the MAC;
b) If the last /R/ is transmitted in an even-numbered code-group position, the PCS appends a single additional /R/ to the code-group stream to ensure that the subsequent /I/ is aligned on an even-numbered code-group boundary.

36.2.4.16 Error_Propagation (/V/)

Error_Propagation (/V/) indicates that the PCS client wishes to indicate a transmission error to its peer entity. The normal use of Error_Propagation is for repeaters to propagate received errors. /V/ is emitted from the PCS, at the request of the PCS client through the use of the TX_ER signal, as described in Clause 35. Error_Propagation is emitted from, and interpreted by, the PCS. Error_Propagation consists of the ordered_set /V/, as defined in Table 36–3.

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The presence of Error_Propagation or any invalid code-group on the medium denotes a collision artifact or an error condition. Invalid code-groups are not intentionally transmitted onto the medium by DTEs. The PCS processes and conditionally indicates the reception of /V/ or an invalid code-group on the GMII as false carrier, data errors, or carrier extend errors, depending on its current context.

36.2.4.17 Encapsulation

The 1000BASE-X PCS accepts packets from the MAC through the Reconciliation sublayer and GMII. Due to the continuously signaled nature of the underlying PMA, and the encoding performed by the PCS, the 1000BASE-X PCS encapsulates MAC frames into a code-group stream. The PCS decodes the code-group stream received from the PMA, extracts packets from it, and passes the packets to the MAC via the Reconciliation sublayer and GMII.

Figure 36–4 depicts the PCS encapsulation of a MAC packet based on GMII signals.

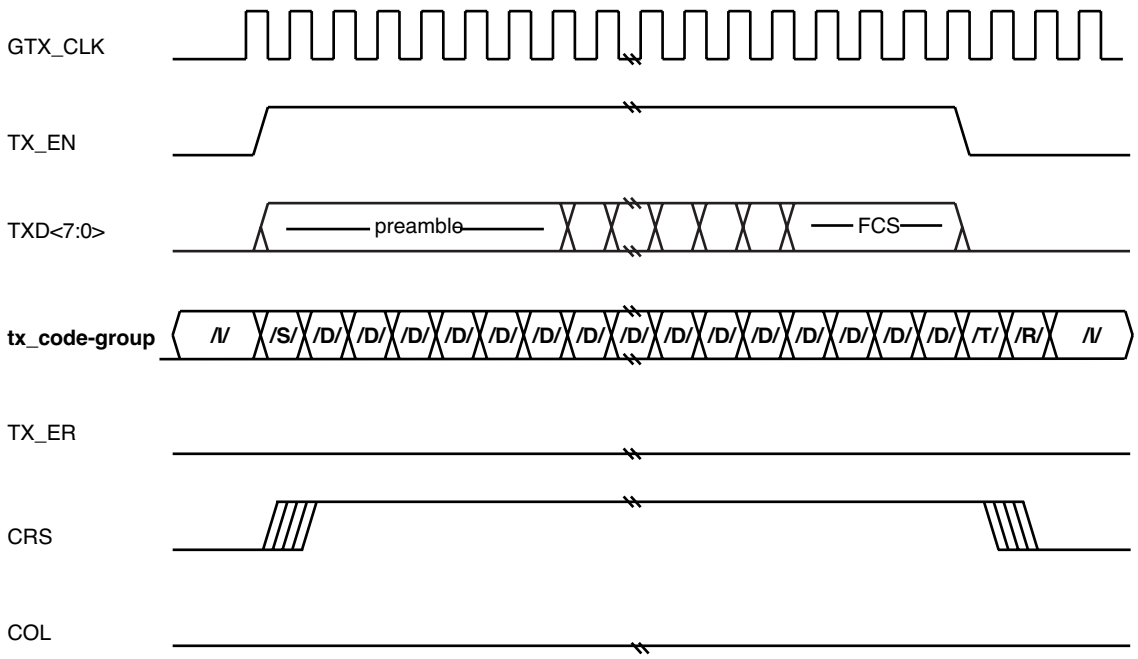


Figure 36–4—PCS encapsulation

36.2.4.18 Mapping between GMII, PCS and PMA

Figure 36–3 depicts the mapping of the octet-wide data path of the GMII to the ten-bit-wide code-groups of the PCS, and the one-bit paths of the PMA/PMD interface.

The PCS encodes an octet received from the GMII into a ten-bit code-group, according to Figure 36–3. Code-groups are serialized into a tx_bit stream by the PMA and passed to the PMD for transmission on the underlying medium, according to Figure 36–3. The first transmitted tx_bit is tx_code-group<0>, and the last tx_bit transmitted is tx_code-group<9>. There is no numerical significance ascribed to the bits within a code-group; that is, the code-group is simply a ten-bit pattern that has some predefined interpretation.

Similarly, the PMA deserializes rx_bits received from the PMD, according to Figure 36–3. The PCS Receive process converts rx_code-group<9:0>'s into GMII data octets, according to 36.2.5.2.2.

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36.2.5 Detailed functions and state diagrams

The notation used in the state diagrams in this clause follow the conventions in 21.5. State diagram variables follow the conventions of 21.5.2 except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set.

Timeless states are employed as an editorial convenience to facilitate the distribution of transition conditions from prior states. No actions are taken within these states. Exit conditions are evaluated for timeless states. Timeless states are as follows:

a) PCS transmit ordered_set state TX_PACKET;
b) PCS transmit code-group state GENERATE_CODE_GROUPS;
c) PCS transmit code-group state IDLE_DISPARITY_TEST;
d) PCS receive state RECEIVE;
e) PCS receive state EPD2_CHECK_END.

36.2.5.1 State variables

36.2.5.1.1 Notation conventions

/x/
: Denotes the constant code-group specified in 36.2.5.1.2 (valid code-groups must follow the rules of running disparity as per 36.2.4.5 and 36.2.4.6).

[/x/]
: Denotes the latched received value of the constant code-group (/x/) specified in 36.2.5.1.2 and conveyed by the SYNC_UNITDATA.indicate message described in 36.2.5.1.6.

36.2.5.1.2 Constants

/C/
: The Configuration ordered_set group, comprising either the /C1/ or /C2/ ordered_set, as specified in 36.2.4.10. Conveys the Config_Reg value as tx_Config_Reg<D15:D0> for the PCS Transmit process and rx_Config_Reg<D15:D0> for the PCS Receive process.

/COMMA/
: The set of special code-groups which include a comma as specified in 36.2.4.9 and listed in Table 36–2.

/D/
: The set of 256 code-groups corresponding to valid data, as specified in 36.2.4.11.

/Dx.y/
: One of the set of 256 code-groups corresponding to valid data, as specified in 36.2.4.11.

/I/
: The IDLE ordered_set group, comprising either the /I1/ or /I2/ ordered_sets, as specified in 36.2.4.12.

/INVALID/
: The set of invalid data or special code-groups, as specified in 36.2.4.6.

/Kx.y/
: One of the set of 12 code-groups corresponding to valid special code-groups, as specified in Table 36–2.

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/R/

The code-group used as either: End_of_Packet delimiter part 2; End_of_Packet delimiter part 3; Carrier_Extend; and /I/ alignment.

/S/

The code-group corresponding to the Start_of_Packet delimiter (SPD) as specified in 36.2.4.13.

/T/

The code-group used for the End_of_Packet delimiter part 1.

/V/

The Error_Propagation code-group, as specified in 36.2.4.16.

36.2.5.1.3 Variables

cgbad

Alias for the following terms: ((rx_code-groupŒ/INVALID/) + (rx_code-group=/COMMA/ *rx_even=TRUE)) * PMA_UNITDATA.indicate

cggood

Alias for the following terms: !((rx_code-groupŒ/INVALID/) + (rx_code-group=/COMMA/ *rx_even=TRUE)) * PMA_UNITDATA.indicate

COL

The COL signal of the GMII as specified in Clause 35.

CRS

The CRS signal of the GMII as specified in Clause 35.

EVEN

The latched state of the rx_even variable, when rx_even=TRUE, as conveyed by the SYNC_UNITDATA.indicate message described in 36.2.5.1.6.

mr_loopback

A boolean that indicates the enabling and disabling of data being looped back through the PHY. Loopback of data through the PHY is enabled when Control register bit 0.14 is set to one.

Values: FALSE; Loopback through the PHY is disabled.
TRUE; Loopback through the PHY is enabled.

mr_main_reset

Controls the resetting of the PCS via Control Register bit 0.15.

Values: FALSE; Do not reset the PCS.
TRUE; Reset the PCS.

ODD

The latched state of the rx_even variable, when rx_even=FALSE, as conveyed by the SYNC_UNITDATA.indicate message described in 36.2.5.1.6.

power_on

Condition that is true until such time as the power supply for the device that contains the PCS has reached the operating region. The condition is also true when the device has low power mode set via Control register bit 0.11.

Values: FALSE; The device is completely powered (default).
TRUE; The device has not been completely powered.

NOTE—Power_on evaluates to its default value in each state where it is not explicitly set.

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receiving

A boolean set by the PCS Receive process to indicate carrier activity. Used by the Carrier Sense process, and also interpreted by the PCS Transmit process for indicating a collision. (See also 36.2.5.1.4, carrier_detect(x).)

Values: TRUE; Carrier being received.
FALSE; Carrier not being received.

repeater_mode

A boolean used to make the assertion of Carrier Sense occur only in response to receive activity when the PCS is used in a CSMA/CD repeater. This variable is set to TRUE in a repeater application, and set to FALSE in all other applications.

Values: TRUE; Allows the assertion of CRS in response to receive activity only.
FALSE; Allows the assertion of CRS in response to either transmit or receive activity.

rx_bit

A binary parameter conveyed by the PMD_UNITDATA.indicate service primitive, as specified in 38.1.1.2, to the PMA.

Values: ZERO; Data bit is a logical zero.
ONE; Data bit is a logical one.

rx_code-group<9:0>

A 10-bit vector represented by the most recently received code-group from the PMA. The element rx_code-group<0> is the least recently received (oldest) rx_bit; rx_code-group<9> is the most recently received rx_bit (newest). When code-group alignment has been achieved, this vector contains precisely one code-group.

rx_Config_Reg<D15:D0>

A 16-bit array that contains the data bits received from a /C/ ordered_set as defined in 36.2.4.10. Conveyed by the PCS Receive process to the PCS Auto-Negotiation process. The format of the data bits is context dependent, relative to the state of the Auto-Negotiation function, and is presented in 37.2.1.1 and 37.2.4.3.1. For each element within the array:

Values: ZERO; Data bit is a logical zero.
ONE; Data bit is a logical one.

RX_DV

The RX_DV signal of the GMII as specified in Clause 35. Set by the PCS Receive process.

RX_ER

The RX_ER signal of the GMII as specified in Clause 35. Set by the PCS Receive process.

rx_even

A boolean set by the PCS Synchronization process to designate received code-groups as either even- or odd-numbered code-groups as specified in 36.2.4.2.

Values: TRUE; Even-numbered code-group being received.
FALSE; Odd-numbered code-group being received.

RXD<7:0>

The RXD<7:0> signal of the GMII as specified in Clause 35. Set by the PCS Receive process.

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signal_detect

A boolean set by the PMD continuously via the PMD_SIGNAL.indicate(signal_detect) message to indicate the status of the incoming link signal.

Values: FAIL; A signal is not present on the link.
OK; A signal is present on the link.

sync_status

A parameter set by the PCS Synchronization process to reflect the status of the link as viewed by the receiver.

Values: FAIL; The receiver is not synchronized to code-group boundaries.
OK; The receiver is synchronized to code-group boundaries.

transmitting

A boolean set by the PCS Transmit process to indicate that packet transmission is in progress. Used by the Carrier Sense process and internally by the PCS Transmit process for indicating a collision.

Values: TRUE; The PCS is transmitting a packet.
FALSE; The PCS is not transmitting a packet.

tx_bit

A binary parameter used to convey data from the PMA to the PMD via the PMD_UNITDATA.request service primitive as specified in 38.1.1.1.

Values: ZERO; Data bit is a logical zero.
ONE; Data bit is a logical one.

tx_code-group<9:0>

A vector of bits representing one code-group, as specified in Tables 36–1a or 36–2, which has been prepared for transmission by the PCS Transmit process. This vector is conveyed to the PMA as the parameter of a PMD_UNITDATA.request(tx_bit) service primitive. The element tx_code-group<0> is the first tx_bit transmitted; tx_code-group<9> is the last tx_bit transmitted.

tx_Config_Reg<D15:D0>

A 16-bit array that contains the data bits to be transmitted in a /C/ ordered_set as defined in 36.2.4.10. Conveyed by the PCS Auto-Negotiation process to the PCS Transmit process. The format of the data bits is context dependent, relative to the state of the Auto-Negotiation function, and is presented in 37.2.1.1 and 37.2.4.3.1. For each element within the array:

Values: ZERO; Data bit is a logical zero.
ONE; Data bit is a logical one.

tx_disparity

A boolean set by the PCS Transmit process to indicate the running disparity at the end of code-group transmission as a binary value. Running disparity is described in 36.2.4.3.

Values: POSITIVE
NEGATIVE

TX_EN

The TX_EN signal of the GMII as specified in Clause 35.

TX_ER

The TX_ER signal of the GMII as specified in Clause 35.

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tx_even

A boolean set by the PCS Transmit process to designate transmitted code-groups as either even- or odd-numbered code-groups as specified in 36.2.4.2.

Values: TRUE; Even-numbered code-group being transmitted.
FALSE; Odd-numbered code-group being transmitted.

tx_o_set

One of the following defined ordered_sets: /C/, /T/, /R/, /I/, /S/, /V/, or the code-group /D/.

TXD<7:0>

The TXD<7:0> signal of the GMII as specified in Clause 35.

xmit

Defined in 37.3.1.1.

36.2.5.1.4 Functions

carrier_detect

In the PCS Receive process, this function uses for input the latched code-group ([/x/]) and latched rx_even (EVEN/ODD) parameters of the SYNC_UNITDATA.indicate message from the PCS Synchronization process. When SYNC_UNITDATA.indicate message indicates EVEN, the carrier_detect function detects carrier when either:

a) A two or more bit difference between [/x/] and both /K28.5/ encodings exists (see Table 36–2); or

b) A two to nine bit difference between [/x/] and the expected /K28.5/ (based on current running disparity) exists.

Values: TRUE; Carrier is detected.
FALSE; Carrier is not detected.

check_end

Prescient End_of_Packet and Carrier_Extend function used by the PCS Receive process to set RX_ER and RXD<7:0> signals. The check_end function returns the current and next two code-groups in rx_code-group<9:0>.

DECODE ([/x]/)

In the PCS Receive process, this function takes as its argument the latched value of rx_code-group<9:0> ([/x/]) and the current running disparity, and returns the corresponding GMII RXD<7:0>, rx_Config_Reg<D7:D0>, or rx_Config_Reg<D15:D8> octet, per Table 36–1a–e. DECODE also updates the current running disparity per the running disparity rules outlined in 36.2.4.4.

ENCODE(x)

In the PCS Transmit process, this function takes as its argument (x), where x is a GMII TXD<7:0>, tx_Config_Reg<D7:D0>, or tx_Config_Reg<D15:D8> octet, and the current running disparity, and returns the corresponding ten-bit code-group per Table 36–1a. ENCODE also updates the current running disparity per Table 36–1a–e.

signal_detectCHANGE

In the PCS Synchronization process, this function monitors the signal_detect variable for a state change. The function is set upon state change detection.

Values: TRUE; A signal_detect variable state change has been detected.
FALSE; A signal_detect variable state change has not been detected (default).

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NOTE—Signal_detectCHANGE is set by this function definition; it is not set explicitly in the state diagrams. Signal_detectCHANGE evaluates to its default value upon state entry.

VOID(x)

x Œ /D/, /T/, /R/, /K28.5/. Substitutes /V/ on a per code-group basis as requested by the GMII.

If [TX_EN=FALSE * TX_ER=TRUE * TXD≠(0000 1111)],

then return /V/;

Else if [TX_EN=TRUE * TX_ER=TRUE],

then return /V/;

Else return x.

xmitCHANGE

In the PCS Transmit process, this function monitors the xmit variable for a state change. The function is set upon state change detection.

Values: TRUE; An xmit variable state change has been detected.
FALSE; An xmit variable state change has not been detected (default).

NOTE—XmitCHANGE is set by this function definition; it is not set explicitly in the state diagrams. XmitCHANGE evaluates to its default value upon entry to state TX_TEST_XMIT.

36.2.5.1.5 Counters

good_cgs

Count of consecutive valid code-groups received.

36.2.5.1.6 Message

PMA_UNITDATA.indicate(rx_code-group<9:0>)

A signal sent by the PMA Receive process conveying the next code-group received over the medium (see 36.3.1.2).

PMA_UNITDATA.request(tx_code-group<9:0>)

A signal sent to the PMA Transmit process conveying the next code-group ready for transmission over the medium (see 36.3.1.1).

PMD_SIGNAL.indicate(signal_detect)

A signal sent by the PMD to indicate the status of the signal being received on the MDI.

PUDI

Alias for PMA_UNITDATA.indicate(rx_code-group<9:0>).

PUDR

Alias for PMA_UNITDATA.request(tx_code-group<9:0>).

RUDI

Alias for RX_UNITDATA.indicate(parameter).

RX_UNITDATA.indicate(parameter)

A signal sent by the PCS Receive process to the PCS Auto_Negotiation process conveying the following parameters:

Parameters: INVALID; indicates that an error condition has been detected while receiving /C/ or /I/ ordered_sets;

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/C/; the /C/ ordered_set has been received;
/I/; the /I/ ordered_set has been received.

SUDI

Alias for SYNC_UNITDATA.indicate(parameters).

SYNC_UNITDATA.indicate(parameters)

A signal sent by the PCS Synchronization process to the PCS Receive process conveying the following parameters:

Parameters: [/x/]; the latched value of the indicated code-group (/x/);
EVEN/ODD; The latched state of the rx_even variable;

Value: EVEN; Passed when the latched state of rx_even=TRUE.
ODD; Passed when the latched state of rx_even=FALSE.

TX_OSET.indicate

A signal sent to the PCS Transmit ordered_set process from the PCS Transmit code-group process signifying the completion of transmission of one ordered_set.

36.2.5.1.7 Timer

cg_timer

A continuous free-running timer.

Values: The condition cg_timer_done becomes true upon timer expiration.

Restart when: immediately after expiration; restarting the timer resets the condition cg_timer_done.

Duration: 8 ns nominal.

If the GMII is implemented, cg_timer shall expire synchronously with the rising edge of GTX_CLK (see tolerance required for GTX_CLK in 35.4.2.3). In the absence of a GMII, cg_timer shall expire every 8 ns ± 0.01%. In the PCS transmit code-group state diagram, the message PMA_UNITDATA.request is issued concurrently with cg_timer_done.

36.2.5.2 State diagrams

36.2.5.2.1 Transmit

The PCS Transmit process is depicted in two state diagrams: PCS Transmit ordered_set and PCS Transmit code-group. The PCS shall implement its Transmit process as depicted in Figures 36–5 and 36–6, including compliance with the associated state variables as specified in 36.2.5.1.

The Transmit ordered_set process continuously sources ordered_sets to the Transmit code-group process. When initially invoked, and when the Auto-Negotiation process xmit flag indicates CONFIGURATION, the Auto-Negotiation process is invoked. When the Auto-Negotiation process xmit flag indicates IDLE, and between packets (as delimited by the GMII), /I/ is sourced. Upon the assertion of TX_EN by the GMII when the Auto-Negotiation process xmit flag indicates DATA, the SPD ordered_set is sourced. Following the SPD, /D/ code-groups are sourced until TX_EN is deasserted. Following the de-assertion of TX_EN, EPD ordered_sets are sourced. If TX_ER is asserted when TX_EN is deasserted and carrier extend error is not indicated by TXD, /R/ ordered_sets are sourced for as many GTX_CLK periods as TX_ER is asserted with a delay of two GTX_CLK periods to first source the /T/ and /R/ ordered sets. If carrier extend error is indicated by TXD during carrier extend, /V/ ordered_sets are sourced. If TX_EN and TX_ER are both de-asserted, the /R/ ordered_set may be sourced, after which the sourcing of /I/ is resumed. If, while TX_EN is

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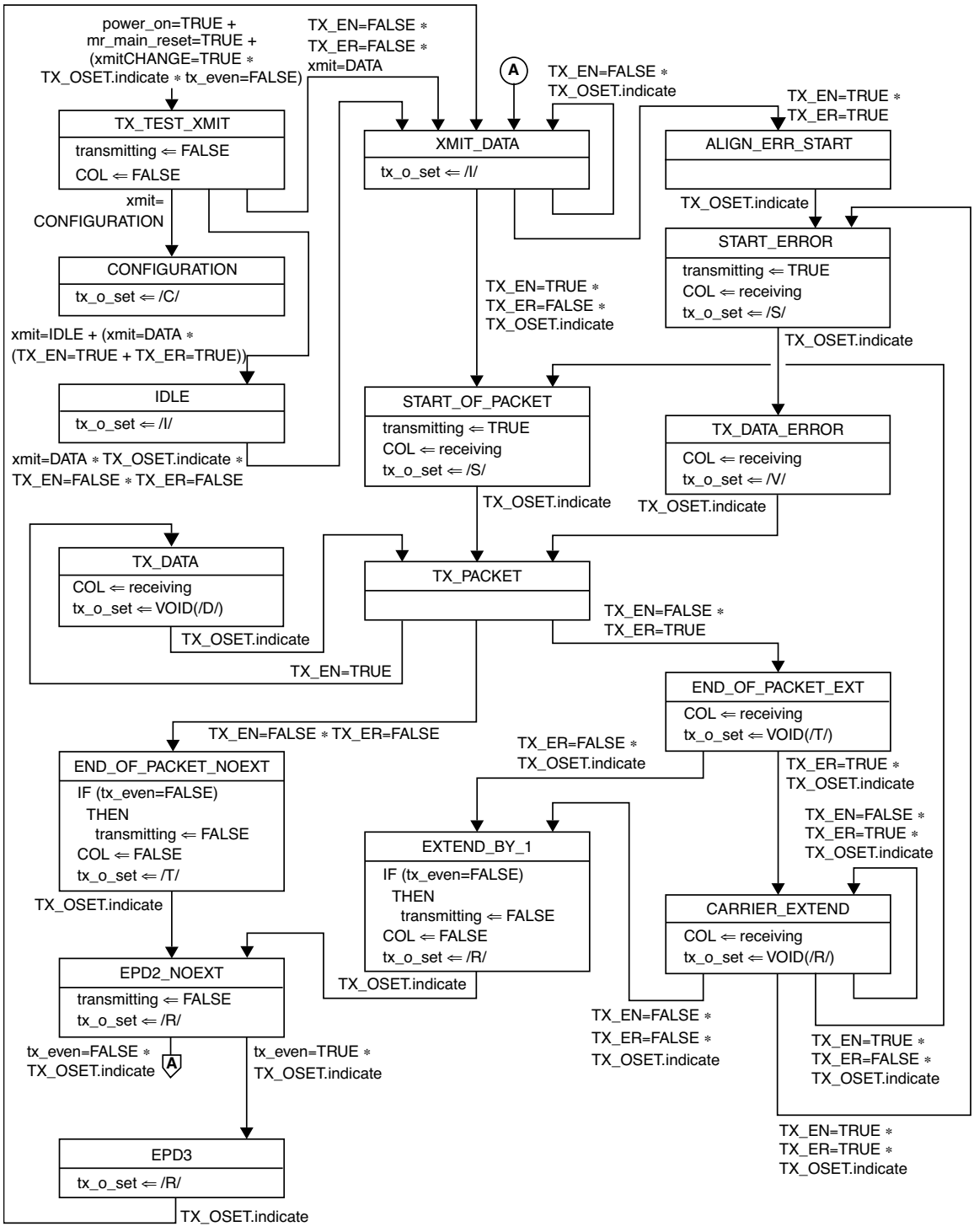


Figure 36–5—PCS transmit ordered_set state diagram

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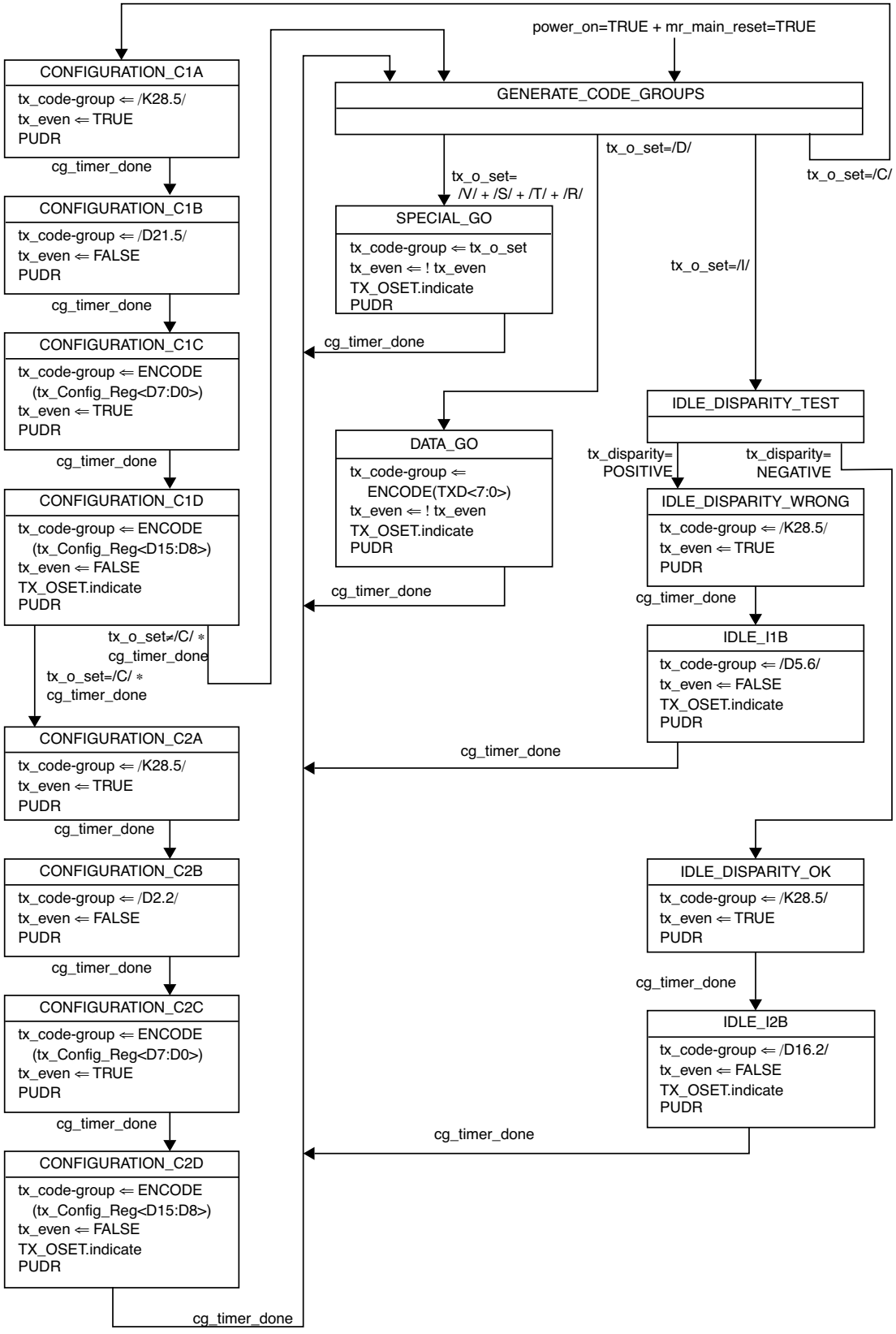
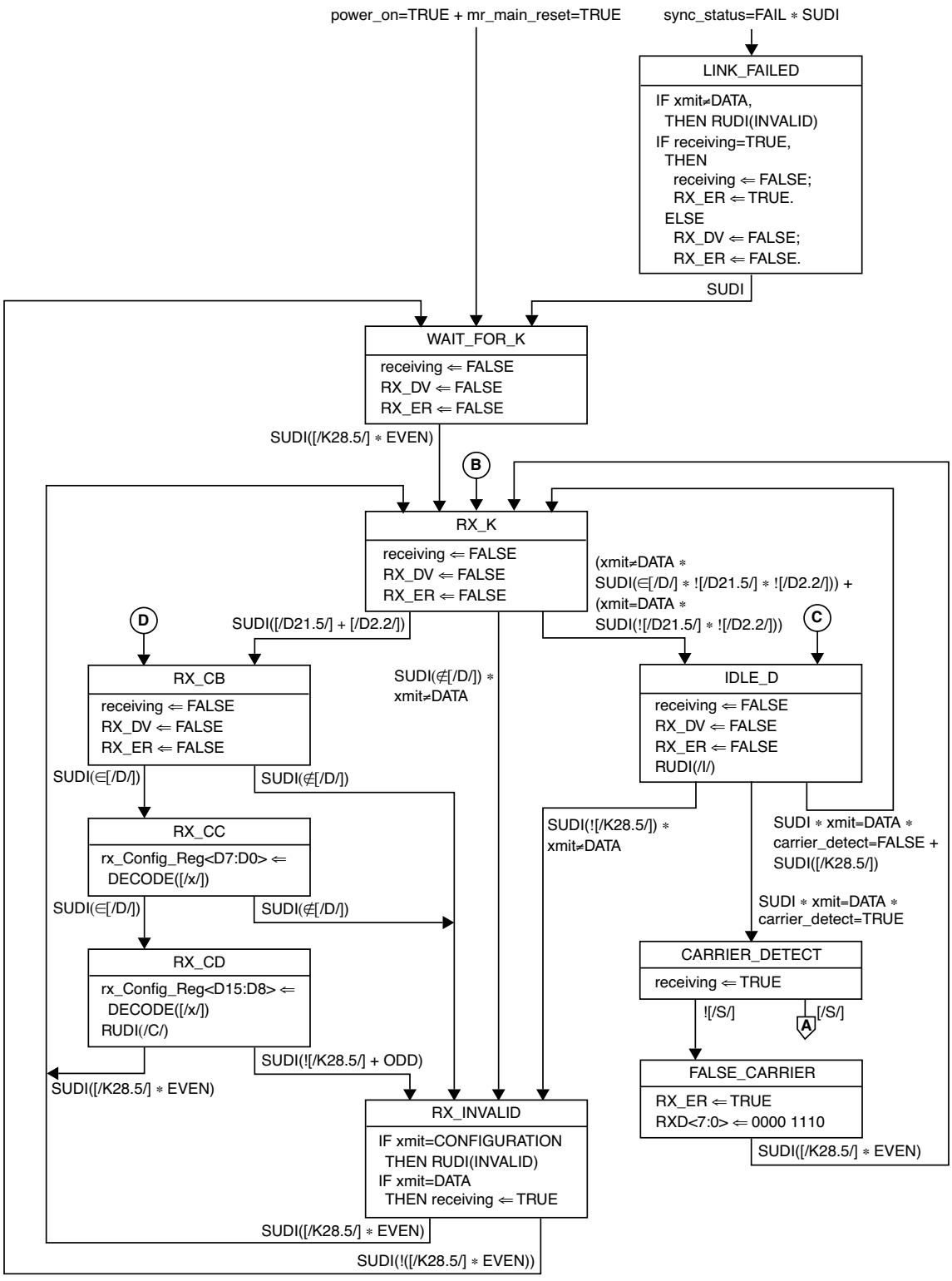


Figure 36–6—PCS transmit code-group state diagram

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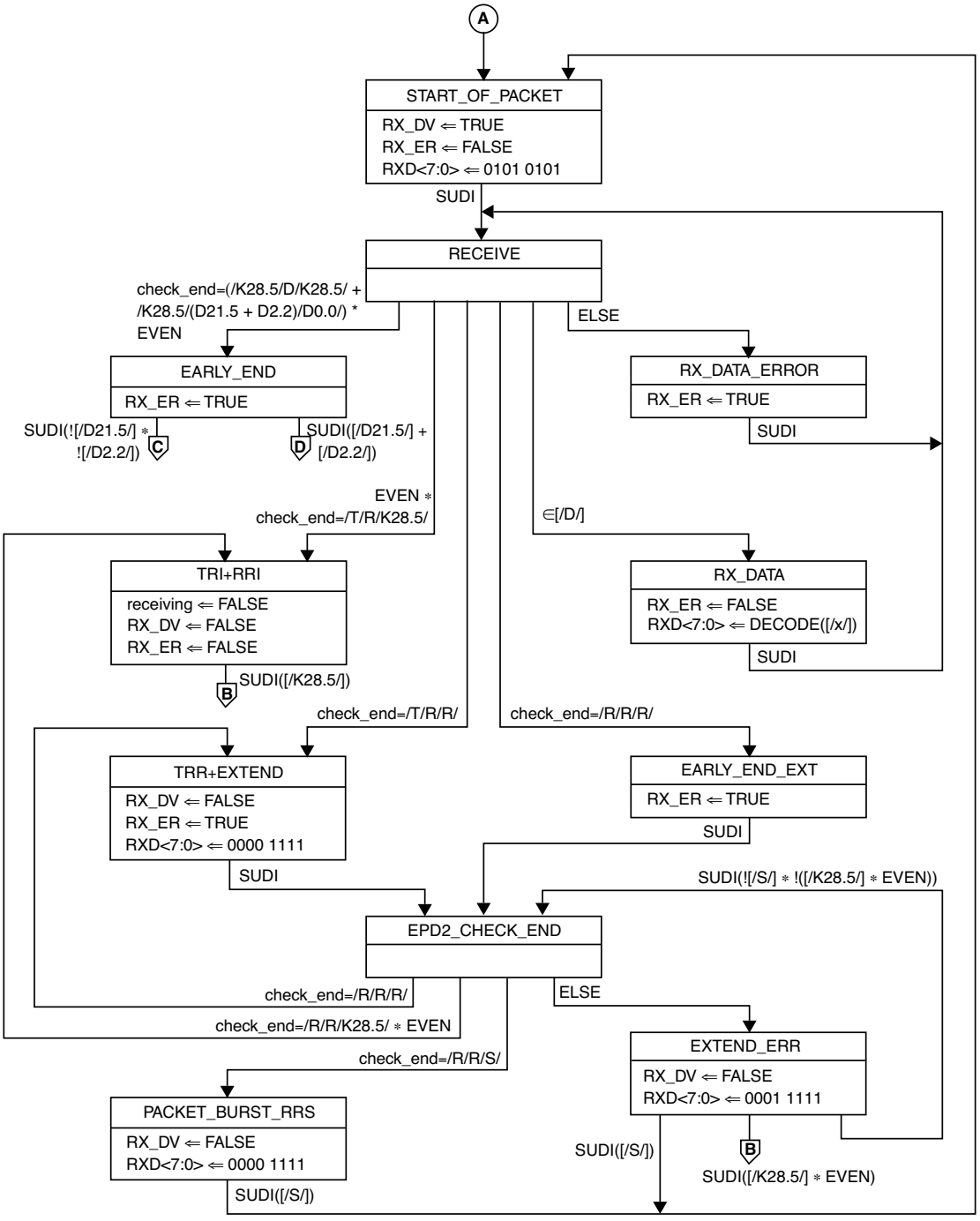
NOTE—Outgoing arcs leading to labeled polygons flow offpage to corresponding incoming arcs leading from labeled circles on Figure 36–7b, and vice versa.

Figure 36–7a—PCS receive state diagram, part a

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NOTE—Outgoing arcs leading to labeled polygons flow offpage to corresponding incoming arcs leading from labeled circles on Figure 36–7a, and vice versa.

Figure 36–7b—PCS receive state diagram, part b

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asserted, the TX_ER signal is asserted, the /V/ ordered_set is sourced except when the SPD ordered set is selected for sourcing.

Collision detection is implemented by noting the occurrence of carrier receptions during transmissions, following the models of 10BASE-T and 100BASE-X.

The Transmit code-group process continuously sources tx_code-group<9:0> to the PMA based on the ordered_sets sourced to it by the Transmit ordered_set process. The Transmit code-group process determines the proper code-group to source based on even/odd-numbered code-group alignment, running disparity requirements, and ordered_set format.

36.2.5.2.2 Receive

The PCS shall implement its Receive process as depicted in Figure 36–7a and Figure 36–7b, including compliance with the associated state variables as specified in 36.2.5.1.

The PCS Receive process continuously passes RXD<7:0> and sets the RX_DV and RX_ER signals to the GMII based on the received code-group from the PMA.

When the Auto-Negotiation process xmit flag indicates CONFIGURATION or IDLE, the PCS Receive process continuously passes /C/ and /I/ ordered sets and rx_Config_Reg<D15:D0> to the Auto-Negotiation process.

36.2.5.2.3 State variable function carrier_detect(x)

The detection of carrier on the underlying channel is used both by the MAC (via the GMII CRS signal and the Reconciliation sublayer) for deferral purposes, and by the PCS Transmit process for collision detection. A carrier event, signaled by the assertion of receiving, is indicated by the detection of a difference between the received code-group and /K28.5/ as specified in 36.2.5.1.4.

A carrier event is in error if it does not start with an SPD. The PCS Receive process performs this function by continuously monitoring incoming code-groups for specific patterns that indicate non-/I/ activity such as SPD. The detection of an SPD carrier event causes the PCS to substitute the value (01010101) for the SPD, set RXD<7:0> to this value, and assert RX_DV. The pattern substituted for the SPD is consistent with the preamble pattern expected by the MAC. The detection of a non-SPD carrier event (false carrier) causes the PCS to substitute the value (00001110) for the code-group received, set RXD<7:0> to this value, and assert RX_ER.

36.2.5.2.4 Code-group stream decoding

Subsequent to the detection of an SPD carrier event, the PCS Receive process performs the DECODE function on the incoming code-groups, passing decoded data to the GMII, including those corresponding to the remainder of the MAC preamble and SFD. The GMII signal RX_ER is asserted upon decoding any code-group following the SPD that neither is a valid /D/ code-group nor follows the EPD rules in 36.2.4.14.1.

Packets are terminated with an EPD as specified in 36.2.4.14. The PCS Receive process performs the check_end function to preserve the ability of the MAC to properly delimit the FCS at the end of a packet.

Detection of /T/R/R/ or /T/R/K28.5/ by the check_end function denotes normal (i.e. non-error) packet termination. Detection of /R/R/R/ by the check_end function denotes packet termination with error and Carrier_Extend processing. Detection of /K28.5/D/K28.5/ by the check_end function denotes packet termination with error. Detection of /K28.5/(D21.5 or D2.2)/D0.0 by the check_end function denotes packet termination with error.

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36.2.5.2.5 Carrier sense

The Carrier Sense process generates the signal CRS on the GMII, which (via the Reconciliation sublayer) the MAC uses for deferral.

The PCS shall implement the Carrier Sense process as depicted in Figure 36–8 including compliance with the associated state variables as specified in 36.2.5.1.

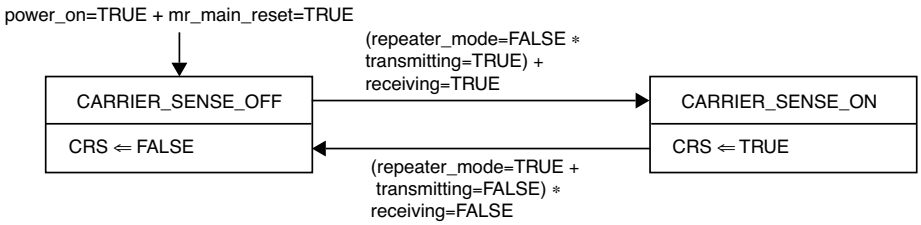


Figure 36–8—Carrier sense state diagram

36.2.5.2.6 Synchronization

The PCS shall implement the Synchronization process as depicted in Figure 36–9 including compliance with the associated state variables as specified in 36.2.5.1. The Synchronization process is responsible for determining whether the underlying receive channel is ready for operation. Failure of the underlying channel typically causes the PMA client to suspend normal actions.

A receiver that is in the LOSS_OF_SYNC state and that has acquired bit synchronization attempts to acquire code-group synchronization via the Synchronization process. Code-group synchronization is acquired by the detection of three ordered_sets containing commas in their leftmost bit positions without intervening invalid code-group errors. Upon acquisition of code-group synchronization, the receiver enters the SYNC_ACQUIRED_1 state. Acquisition of synchronization ensures the alignment of multi-code-group ordered_sets to even-numbered code-group boundaries.

Once synchronization is acquired, the Synchronization process tests received code-groups in sets of four code-groups and employs multiple sub-states, effecting hysteresis, to move between the SYNC_ACQUIRED_1 and LOSS_OF_SYNC states.

The condition sync_status=FAIL existing for ten ms or more causes the PCS Auto-Negotiation process to begin and the PCS Transmit process to begin transmission of /C/. Upon reception of three matching /C/s from the link partner, the PCS Auto-Negotiation process begins. The internal signal receiving is de-asserted in the PCS Receive process LINK_FAILED state when sync_status=FAIL and a code-group is received.

36.2.5.2.7 Auto-Negotiation process

The Auto-Negotiation process shall provide the means to exchange configuration information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities. See Clause 37 for a description of the Auto-Negotiation process and Config_Reg contents.

Upon successful completion of the Auto-Negotiation process, the xmit flag is set to DATA and normal link operation is enabled. The Auto-Negotiation process utilizes the PCS Transmit and Receive processes to convey Config_Reg contents.

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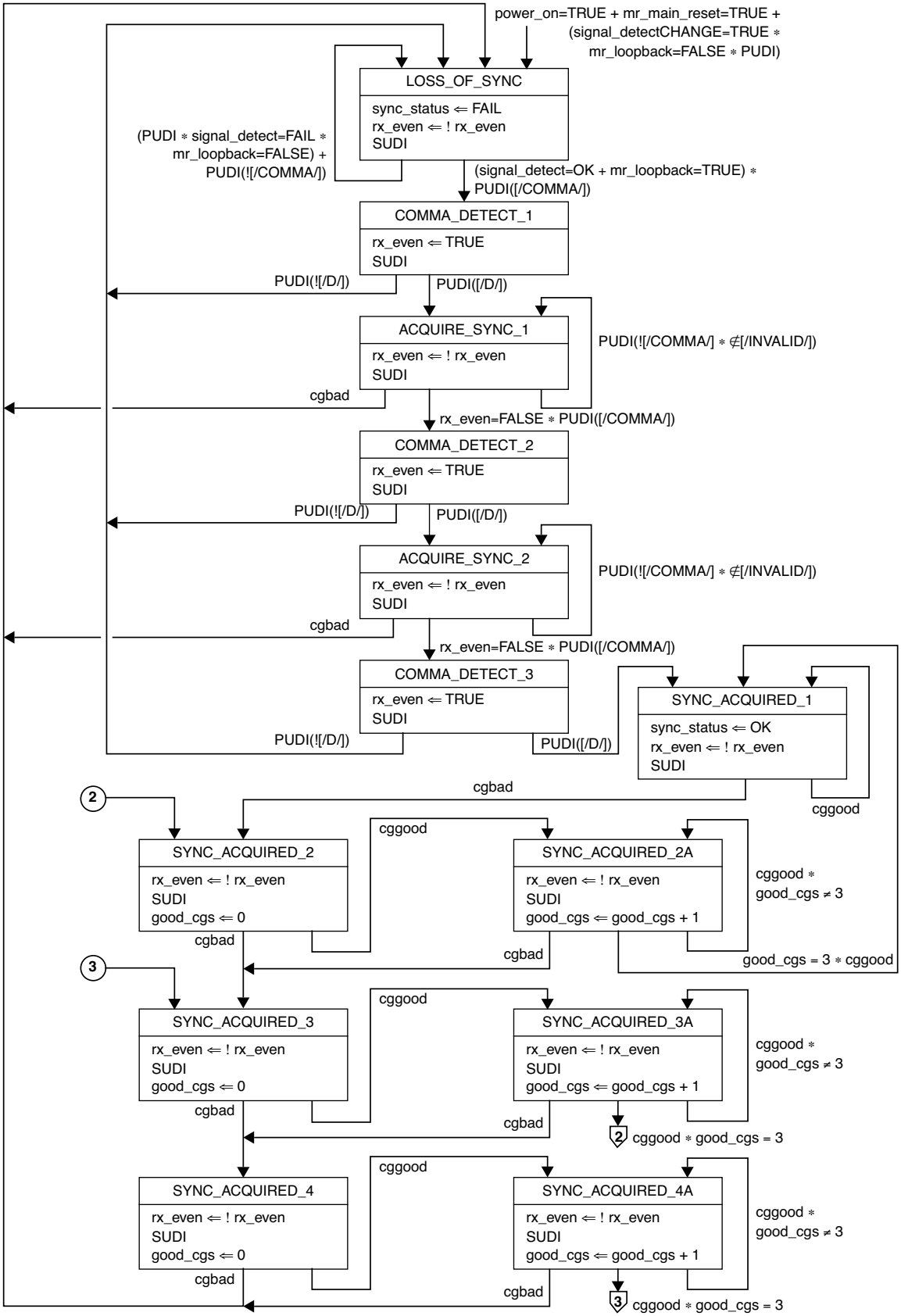


Figure 36–9—Synchronization state diagram

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36.3 Physical Medium Attachment (PMA) sublayer

36.3.1 Service Interface

The PMA provides a Service Interface to the PCS. These services are described in an abstract manner and do not imply any particular implementation. The PMA Service Interface supports the exchange of code-groups between PCS entities. The PMA converts code-groups into bits and passes these to the PMD, and vice versa. It also generates an additional status indication for use by its client.

The following primitives are defined:

PMA_UNITDATA.request(tx_code-group<9:0>)

PMA_UNITDATA.indicate(rx_code-group<9:0>)

36.3.1.1 PMA_UNITDATA.request

This primitive defines the transfer of data (in the form of code-groups) from the PCS to the PMA. PMA_UNITDATA.request is generated by the PCS Transmit process.

36.3.1.1.1 Semantics of the service primitive

PMA_UNITDATA.request(tx_code-group<9:0>)

The data conveyed by PMA_UNITDATA.request is the tx_code-group<9:0> parameter defined in 36.2.5.1.3.

36.3.1.1.2 When generated

The PCS continuously sends, at a nominal rate of 125 MHz, as governed by GTX_CLK, tx_code-group<9:0> to the PMA.

36.3.1.1.3 Effect of receipt

Upon receipt of this primitive, the PMA generates a series of ten PMD_UNITDATA.request primitives, requesting transmission of the indicated tx_bit to the PMD.

36.3.1.2 PMA_UNITDATA.indicate

This primitive defines the transfer of data (in the form of code-groups) from the PMA to the PCS. PMA_UNITDATA.indicate is used by the PCS Synchronization process.

36.3.1.2.1 Semantics of the service primitive

PMA_UNITDATA.indicate(rx_code-group<9:0>)

The data conveyed by PMA_UNITDATA.indicate is the rx_code-group<9:0> parameter defined in 36.2.5.1.3.

36.3.1.2.2 When generated

The PMA continuously sends one rx_code-group<9:0> to the PCS corresponding to the receipt of each code-group aligned set of ten PMD_UNITDATA.indicate primitives received from the PMD. The nominal rate of the PMA_UNITDATA.indicate primitive is 125 MHz, as governed by the recovered bit clock.

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36.3.1.2.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

36.3.2 Functions within the PMA

Figure 36–3 depicts the mapping of the octet-wide data path of the GMII to the ten-bit-wide code-groups of the PMA Service Interface, and on to the serial PMD Service Interface. The PMA comprises the PMA Transmit and PMA Receive processes for 1000BASE-X.

The PMA Transmit process serializes tx_code-groups into tx_bits and passes them to the PMD for transmission on the underlying medium, according to Figure 36–3. Similarly, the PMA Receive process deserializes rx_bits received from the PMD according to Figure 36–3. The PMA continuously conveys ten-bit code-groups to the PCS, independent of code-group alignment. After code-group alignment is achieved, based on comma detection, the PCS converts code-groups into GMII data octets, according to 36.2.5.2.2.

The proper alignment of a comma used for code-group synchronization is depicted in Figure 36–3.

NOTE—Strict adherence to manufacturer-supplied guidelines for the operation and use of PMA serializer components is required to meet the jitter specifications of Clauses 38 and 39. The supplied guidelines should address the quality of power supply filtering associated with the transmit clock generator, and also the purity of the reference clock fed to the transmit clock generator.

36.3.2.1 Data delay

The PMA maps a nonaligned one-bit data path from the PMD to an aligned, ten-bit-wide data path to the PCS, on the receive side. Logically, received bits must be buffered to facilitate proper code-group alignment. These functions necessitate an internal PMA delay of at least ten bit times. In practice, code-group alignment may necessitate even longer delays of the incoming rx_bit stream.

36.3.2.2 PMA transmit function

The PMA Transmit function passes data unaltered (except for serializing) from the PCS directly to the PMD. Upon receipt of a PMA_UNITDATA.request primitive, the PMA Transmit function shall serialize the ten bits of the tx_code-group<9:0> parameter and transmit them to the PMD in the form of ten successive PMD_UNITDATA.request primitives, with tx_code-group<0> transmitted first, and tx_code-group<9> transmitted last.

36.3.2.3 PMA receive function

The PMA Receive function passes data unaltered (except for deserializing and possible code-group slipping upon code-group alignment) from the PMD directly to the PCS. Upon receipt of ten successive PMD_UNITDATA.indicate primitives, the PMA shall assemble the ten received rx_bits into a single ten-bit value and pass that value to the PCS as the rx_code-group<9:0> parameter of the primitive PMA_UNITDATA.indicate, with the first received bit installed in rx_code-group<0> and the last received bit installed in rx_code-group<9>. An exception to this operation is specified in 36.3.2.4.

36.3.2.4 Code-group alignment

In the event the PMA sublayer detects a comma+ within the incoming rx_bit stream, it may realign its current code-group boundary, if necessary, to that of the received comma+ as shown in Figure 36–3. This process is referred to in this document as code-group alignment. The code-group alignment function shall be operational when the EN_CDET signal is active (see 36.3.3.1). During the code-group alignment process, the PMA sublayer may delete or modify up to four, but shall delete or modify no more than four, ten-bit

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code-groups in order to align the correct receive clock and code-group containing the comma+. This process is referred to as code-group slipping.

In addition, the PMA sublayer is permitted to realign the current code-group boundary upon receipt of a comma-pattern.

36.3.3 A physical instantiation of the PMA Service Interface

The ten-bit interface (TBI) is defined to provide compatibility among devices designed by different manufacturers. There is no requirement for a compliant device to implement or expose the TBI. A TBI implementation shall behave as described in 36.3.3 through 36.3.6.

Figure 36–10 illustrates the TBI functions and interfaces.

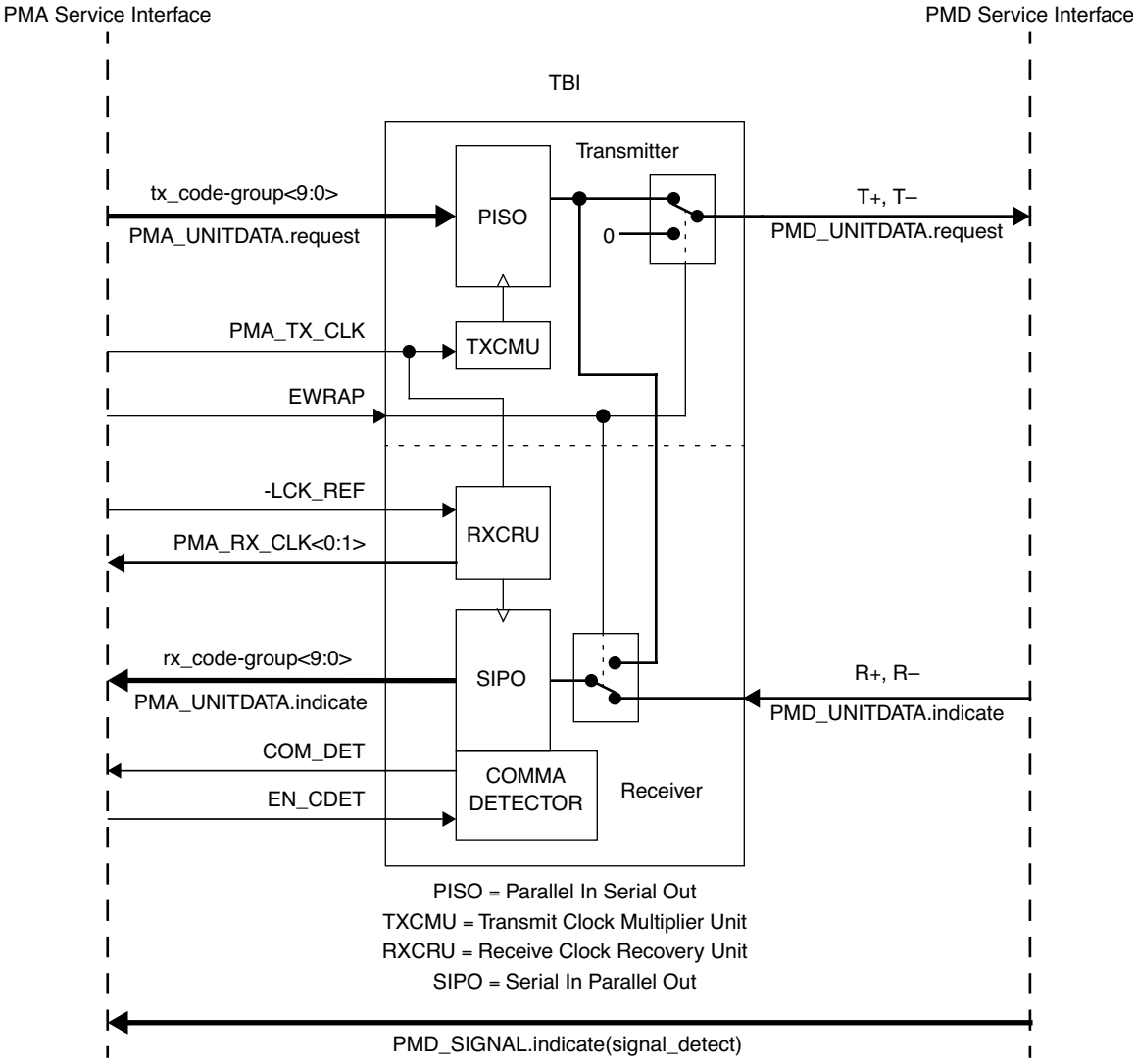


Figure 36–10—TBI reference diagram

As depicted in Figure 36–10, the TBI connects the PCS and PMD sublayers. It is equipped for full duplex transmission of code-groups at 125 MHz. The PCS provides code-groups on tx_code-group<9:0> to the

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PMA transmit function, which latches the data on the rising edge of the 125 MHz PMA_TX_CLK. An internal Clock Multiplier Unit uses PMA_TX_CLK to generate the internal 1250 MHz bit clock that is used to serialize the latched data out of the PMA outputs, if EWRAP is Low, or internally loop it back to the Receive function input, if EWRAP is High.

The PMA Receive function accepts 1250 Mb/s serial data from either the PMD, if EWRAP is Low, or the PMA transmit function, if EWRAP is High, and extracts a bit clock and recovered data from the serial inputs in a clock recovery unit. The recovered data is deserialized and conveyed to the PCS on rx_code-group<9:0>. Two recovered clocks, PMA_RX_CLK<0> and PMA_RX_CLK<1>, which are at 1/20th the baud (62.5 MHz), and 180˚ out-of-phase with one another, are used by the PMA to latch the received 10-bit code-groups. Even and odd-numbered code-groups are latched on successive rising edges of PMA_RX_CLK<1> and PMA_RX_CLK<0>, respectively.

Code-group alignment occurs in the PMA Receive function, if enabled by EN_CDET, when a comma pattern occurs in the PHY bit stream. Upon recognition of the comma pattern, the PMA Receive function outputs the ten-bit code-group containing the comma on rx_code-group<9:0> with the alignment specified in Figure 36–3, and clocked on the rising edge of PMA_RX_CLK<1>.

This TBI provides a Lock_to_Reference_Clock (LCK_REF) input, which may be used to lock the clock recovery unit to PMA_TX_CLK rather than incoming serial data. In the absence of serial data or invalid serial data, the PMA Receive function passes many 8B/10B invalid code-groups across to the PCS. A circuit may be constructed to detect those errors and, using LCK_REF, re-center the receiver clock recovery unit to PMA_TX_CLK in preparation for reacquiring lock on the incoming PHY bit stream.

36.3.3.1 Required signals

In the event this TBI is made accessible, the signals listed in Table 36–4 are provided, with the meanings described elsewhere in this section. Note that not all of these signals are used by the PCS.

Table 36–4—TBI required signals

Symbol	Signal Name	Signal Type	Active Level
tx_code-group<9:0>	Transmit Data	Input	H
PMA_TX_CLK	Transmit Clock	Input	↑
EWRAP	Enable Wrap	Input	H
rx_code-group<9:0>	Receive Data	Output	H
PMA_RX_CLK<0>	Receive Clock 0	Output	↑
PMA_RX_CLK<1>	Receive Clock 1	Output	↑
COM_DET	Comma Detect	Output	H
-LCK_REF	Lock to Reference	Input	L
EN_CDET	Enable Comma Detect	Input	H

tx_code-group<9:0>
: The 10-bit parallel transmit data presented to the PMA for serialization and transmission onto the media. The order of transmission is tx_bit<0> first, followed by tx_bit<1> through tx_bit<9>.

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PMA_TX_CLK

The 125 MHz transmit code-group clock. This code-group clock is used to latch data into the PMA for transmission. PMA_TX_CLK is also used by the transmitter clock multiplier unit to generate the 1250 MHz bit rate clock. PMA_TX_CLK is also used by the receiver when -LCK_REF is active. PMA_TX_CLK has a ±100 ppm tolerance. PMA_TX_CLK is derived from GMII GTX_CLK.

EWRAP

EWRAP enables the TBI to electrically loop transmit data to the receiver. The serial outputs on the transmitter are held in a static state during EWRAP operation. EWRAP may optionally be tied low (function disabled).

rx_code-group<9:0>

Presents the 10-bit parallel receive code-group data to the PCS for further processing. When code-groups are properly aligned, any received code-group containing a comma is clocked by PMA_RX_CLK<1>.

PMA_RX_CLK<0>

The 62.5 MHz receive clock that the protocol device uses to latch odd-numbered code-groups in the received PHY bit stream. This clock may be stretched during code-group alignment, and is not shortened.

PMA_RX_CLK<1>

The 62.5 MHz receive clock that the protocol device uses to latch even-numbered code-groups in the received PHY bit stream. PMA_RX_CLK<1> is 180˚ out-of-phase with PMA_RX_CLK<0>. This clock may be stretched during code-group alignment, and is not shortened.

COM_DET

An indication that the code-group associated with the current PMA_RX_CLK<1> contains a valid comma. When EN_CDET is asserted, the TBI is required to detect and code-group-align to the comma+ bit sequence. Optionally, the TBI may also detect and code-group-align to the comma- bit sequence. The TBI provides this signal as an output, but it may not be used by the PCS.

-LCK_REF

Causes the TBI clock recovery unit to lock to PMA_TX_CLK. The TBI attains frequency lock within 500 ms. This function is not used by the PCS.

NOTE—Implementors may find it necessary to use this signal in order to meet the clock recovery requirements of the PMA sublayer.

EN_CDET

Enables the TBI to perform the code-group alignment function on a comma (see 36.2.4.9, 36.3.2.4). When EN_CDET is asserted the code-group alignment function is operational. This signal is optionally generated by the PMA client. The PMA sublayer may leave this function always enabled.

36.3.3.2 Summary of control signal usage

Table 36–5 lists all possible combinations of control signals on this TBI, including the valid combinations as well as the undefined combinations.

36.3.4 General electrical characteristics of the TBI

In the event this TBI is made accessible, the following subclauses specify the general electrical characteristics of the TBI.

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Table 36–5—TBI combinations of control signals

EWRAP	-LCK_REF	EN_CDET	Interpretation
L	L	L	Undefined
L	L	H	Lock receiver clock recovery unit toPMA_TX_CLK
L	H	L	Normal operation; COM_DET disabled
L	H	H	Normal operation; COM_DET enabled
H	L	L	Undefined
H	L	H	Undefined
H	H	L	Loop transmit data to receiver; COM_DET disabled
H	H	H	Loop transmit data to receiver; COM_DET enabled

36.3.4.1 DC characteristics

Table 36–6 documents the required dc parametric attributes required of all inputs to the TBI and the dc parametric attributes associated with the outputs of the TBI. The inputs levels to the TBI may be greater than the power supply level (i.e., 5 V output driving V_{OH} into a 3.3 V input), tolerance to mismatched input levels is optional. TBI devices not tolerant of mismatched inputs levels that meet Table 36–6 requirements are still regarded as compliant.

Table 36–6—DC specifications

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	Output High Voltage	I_{OH} = –400 μA	V_{CC} = Min	2.2	3.0	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA	V_{CC} = Min	GND	0.25	0.6	V
V_{IH}	Input High Voltage			2.0	—	V_{CC}[a] + 10%	V
V_{IL}	Input Low Voltage			GND	—	0.8	V
I_{IH}	Input High Current	V_{CC} = Max	V_{IN} = 2.4 V	—	—	40	µA
I_{IL}	Input Low Current	V_{CC} = Max	V_{IN} = 0.4 V	—	—	600	µA
C_{IN}	Input Capacitance			—	—	4.0	pf
t_R	Clock Rise Time	0.8 V to 2.0 V		0.7	—	2.4	ns
t_F	Clock Fall Time	2.0 V to 0.8 V		0.7	—	2.4	ns
t_R	Data Rise Time	0.8 V to 2.0 V		0.7	—	—	ns
t_F	Data Fall Time	2.0 V to 0.8 V		0.7	—	—	ns

[a]Refers to the driving device power supply.

36.3.4.2 Valid signal levels

All ac measurements are made from the 1.4 V level of the clock to the valid input or output data levels as shown in Figure 36–11.

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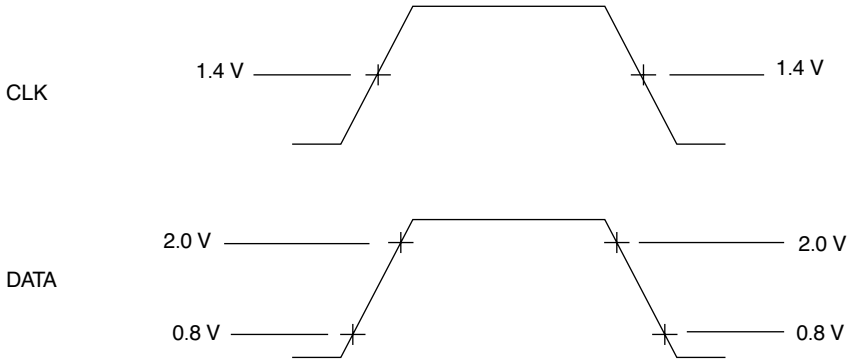


Figure 36–11—Input/output valid level for ac measurements

36.3.4.3 Rise and fall time definition

The rise and fall time definition for PMA_TX-CLK, PMA_RX_CLK<0>, PMA_RX_CLK<1>, and DATA is shown in Figure 36–12.

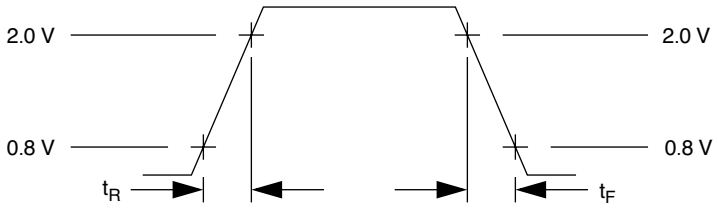


Figure 36–12—Rise and fall time definition

36.3.4.4 Output load

All ac measurements are assumed to have the output load of 10 pF.

36.3.5 TBI transmit interface electrical characteristics

In the event this TBI is made accessible, the electrical characteristics of the TBI transmit interface are specified in the following subclauses.

36.3.5.1 Transmit data (tx_code-group<9:0>)

The tx_code-group<9:0> signals carry data from the PCS to PMA to be serialized to the PMD in accordance with the transmission order shown in Figure 36–3. All tx_code-group<9:0> data conforms to valid code-groups.

36.3.5.2 TBI transmit interface timing

The TBI transmit interface timings in Table 36–7 defines the TBI input. All transitions in Figure 36–13 are specified from the PMA_TX_CLK reference level (1.4 V), to valid input signal levels.

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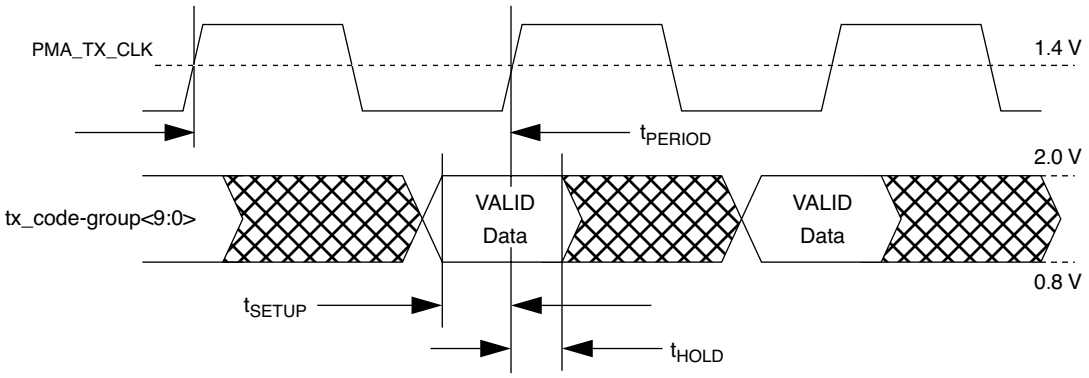


Figure 36–13—TBI transmit interface timing diagram

Table 36–7—Transmit ac specification

Parameter	Description	Min	Typ	Max	Units
t_{PERIOD}	PMA_TX_CLK Period[a]	—	8	—	ns
t_{SETUP}	Data Setup to ↑ PMA_TX_CLK	2.0	—	—	ns
t_{HOLD}	Data Hold from ↑ PMA_TX_CLK	1.0	—	—	ns
t_{DUTY}	PMA_TX_CLK Duty Cycle	40		60	%

[a] ±100 ppm tolerance on PMA_TX_CLK frequency.

36.3.6 TBI receive interface electrical characteristics

In the event this TBI is made accessible, the electrical characteristics of the TBI receive interface are specified in the following subclauses.

The TBI receive interface timings in Table 36–8 define the TBI output. All transitions in Figure 36–14 are specified from the Receive Clock reference level (1.4 V) to valid output signal levels.

36.3.6.1 Receive data (rx_code-group<9:0>)

The 10 receive data signals rx_code-group<9:0> carry parallel data from the PMA sublayer to the PCS sublayer during the rising edge of the receive clock (i.e., PMA_RX_CLK<1> transitions from Low to High). When properly locked and aligned, data transferred across this interface conforms to valid code-groups.

36.3.6.2 Receive clock (PMA_RX_CLK<0>, PMA_RX_CLK<1>)

The receive clocks supplied to the PCS and GMII are derived from the recovered bit clock. PMA_RX_CLK<0> is 180˚ out-of-phase with PMA_RX_CLK<1>.

Table 36–8 specifies a receive clock drift (t_{DRIFT}), which is applicable under all input conditions to the receiver (including invalid or absent input signals). However, the restriction does not apply when the receiver is realigning to a new code-group boundary and the receive clocks are being stretched to a new code-group boundary to avoid short pulses. During the code-group alignment process the receive clocks may slow a fixed amount, depending on the bit offset of the new comma and then return to the nominal frequency.

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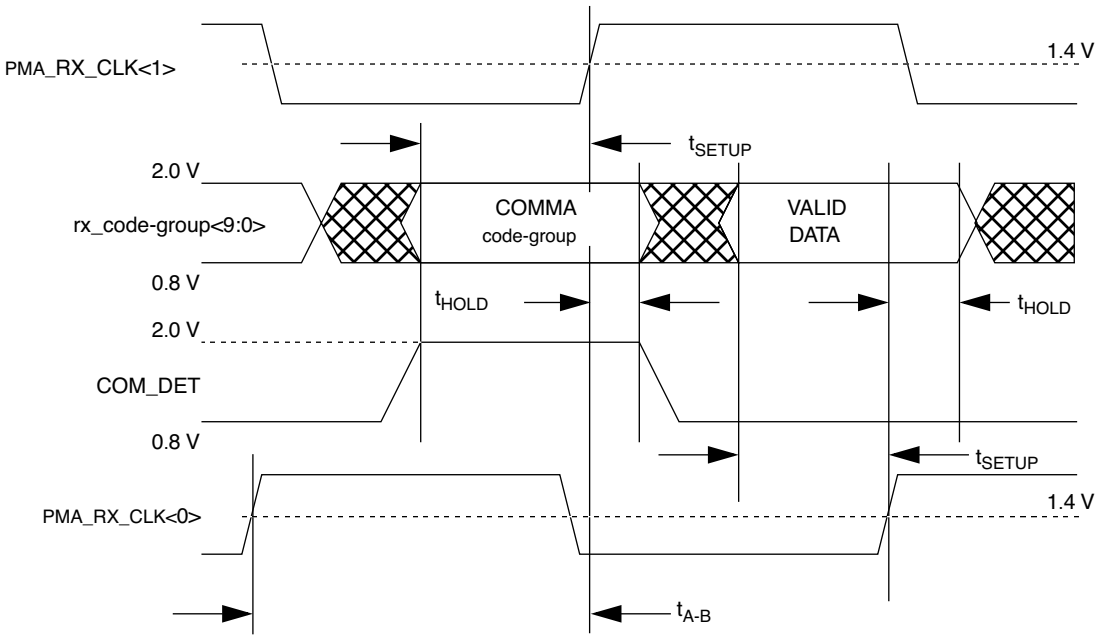


Figure 36–14—TBI receive interface timing diagram

Table 36–8—Receive bus ac specification

Parameter	Description	Min	Typ	Max	Units
t_{FREQ}	PMA_RX_CLK Frequency	—	62.5	—	MHz
t_{DRIFT}	PMA_RX_CLK Drift Rate[a]	0.2	—	—	μs/MHz
t_{SETUP}	Data Setup Before ↑PMA_RX_CLK	2.5	—	—	ns
t_{HOLD}	Data Hold After ↑PMA_RX_CLK	1.5	—	—	ns
t_{DUTY}	PMA_RX_CLK Duty Cycle	40	—	60	%
t_{A-B}	PMA_RX_CLK Skew	7.5	—	8.5	ns

[a]t_{DRIFT} is the (minimum) time for PMA_RX_CLK to drift from 63.5 MHz to 64.5 MHz or 60 MHz to 59 MHz from the PMA_RX_CLK lock value. It is applicable under all input signal conditions (except where noted in 36.3.2.4), including invalid or absent input signals, provided that the receiver clock recovery unit was previously locked to PMA_TX_CLK or to a valid input signal.

36.3.7 Loopback mode

Loopback mode shall be provided, as specified in this subclause, by the transmitter and receiver of a device as a test function to the device. When Loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. A device is explicitly placed in Loopback mode (i.e., Loopback mode is not the normal mode of operation of a device). The method of implementing Loopback mode is not defined by this standard.

NOTE—Loopback mode may be implemented either in the parallel or the serial circuitry of a device.

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36.3.7.1 Receiver considerations

A receiver may be placed in Loopback mode. Entry into or exit from Loopback mode may result in a temporary loss of synchronization.

36.3.7.2 Transmitter considerations

A transmitter may be placed in Loopback mode. The external behavior of a transmitter (i.e., the activity of a transmitter with respect to its attached link) in Loopback mode is specified in 22.2.4.1.2.

36.3.8 Test functions

A limited set of test functions may be provided as an implementation option for testing of the transmitter function.

Some test functions that are not defined by this standard may be provided by certain implementations. Compliance with the standard is not affected by the provision or exclusion of such functions by an implementation. Random jitter test patterns for 1000BASE-X are specified in Annex 36A.

A typical test function is the ability to transmit invalid code-groups within an otherwise valid PHY bit stream. Certain invalid PHY bit streams may cause a receiver to lose word and/or bit synchronization. See ANSI X3.230-1994 [B20] (FC-PH), subclause 5.4, for a more detailed discussion of receiver and transmitter behavior under various test conditions.

36.4 Compatibility considerations

There is no requirement for a compliant device to implement or expose any of the interfaces specified for the PCS or PMA. Implementations of a GMII shall comply with the requirements as specified in Clause 35. Implementations of a TBI shall comply with the requirements as specified in 36.3.3.

36.5 Delay constraints

In half duplex mode, proper operation of a CSMA/CD LAN demands that there be an upper bound on the propagation delays through the network. This implies that MAC, PHY, and repeater implementors must conform to certain delay minima and maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. MAC constraints are contained in 35.2.4 and Table 36–5. Topological constraints are contained in Clause 42.

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementors must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The reference point for all MDI measurements is the 50% point of the mid-cell transition corresponding to the reference bit, as measured at the MDI.

36.5.1 MDI to GMII delay constraints

Every 1000BASE-X PHY associated with a GMII shall comply with the bit time delay constraints specified in Table 36–9a for half duplex operation and Table 36–9b for full duplex operation. These figures apply for all 1000BASE-X PMDs. For any given implementation, the assertion and deassertion delays on CRS shall be equal.

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Table 36–9a—MDI to GMII delay constraints (half duplex mode)

Sublayer measurement points	Event	Min (bit time)	Max (bit time)	Input timing reference	Output timing reference
GMII ⇔ MDI	TX_EN=1 sampled to MDI output	—	136	PMA_TX_CLK rising	1st bit of /S/
	MDI input to CRS assert	—	192	1st bit of /S/	
	MDI input to CRS de-assert	—	192	1st bit of /K28.5/	
	MDI input to COL assert	—	192	1st bit of /S/	
	MDI input to COL de-assert	—	192	1st bit of /K28.5/	
	TX_EN=1 sampled to CRS assert	—	16	PMA_TX_CLK rising	
	TX_EN=0 sampled to CRS de-assert	—	16	PMA_TX_CLK rising	

Table 36–9b—MDI to GMII delay constraints (full duplex mode)

Sublayer measurement points	Event	Min (bit time)	Max (bit time)	Input timing reference	Output timing reference
GMII ⇔ MDI	TX_EN=1 sampled to MDI output	—	136	PMA_TX_CLK rising	1st bit of /S/
	MDI input to RX_DV de-assert	—	192	1st bit of /T/	RX_CLK rising

36.5.2 DTE delay constraints (half duplex mode)

Every DTE with a 1000BASE-X PHY shall comply with the bit time delay constraints specified in Table 36–10 for half duplex operation. These figures apply for all 1000BASE-X PMDs.

Table 36–10—DTE delay constraints (half duplex mode)

Sublayer measurement points	Event	Min (bit time)	Max (bit time)	Input timing reference	Output timing reference
MAC ⇔ MDI	MAC transmit start to MDI output	—	184		1st bit of /S/
	MDI input to MDI output (worst-case nondeferred transmit)	—	440	1st bit of /S/	1st bit of /S/
	MDI input to collision detect	—	240	1st bit of /S/	
	MDI input to MDI output = Jam (worst-case collision response)	—	440	1st bit of /S/	1st bit of jam

36.5.3 Carrier de-assertion/assertion constraint (half duplex mode)

To ensure fair access to the network, each DTE operating in half duplex mode shall, additionally, satisfy the following:

(MAX MDI to MAC Carrier De-assert Detect) – (MIN MDI to MAC Carrier Assert Detect) < 16 bits

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36.6 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801: 1995.

36.7 Protocol Implementation Conformance Statement (PICS) proforma for Clause 36, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X[3]

36.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 36, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

36.7.2 Identification

36.7.2.1 Implementation identification

Supplier (Note 1)	
Contact point for enquiries about the PICS (Note 1)	
Implementation Name(s) and Version(s) (Notes 1 and 3)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s) (Note 2)	

NOTE 1—Required for all implementations.

NOTE 2—May be completed as appropriate in meeting the requirements for the identification.

NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).

[3]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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36.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2002, Clause 36, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

36.7.3 Major Capabilities/Options

Item	Feature	Subclause	Value/Comment	Status	Support
*PMA	Ten-bit interface (TBI)	36.4		O	Yes [ ] No [ ]
*GMII	PHY associated with GMII	36.4		O	Yes [ ] No [ ]
*DTE	DTE with PHY not associated with GMII	36.5.2		O	Yes [ ] No [ ]
*FDX	PHY supports full duplex mode	36.5		O	Yes [ ] No [ ]
*HDX	PHY supports half duplex mode	36.5		O	Yes [ ] No [ ]
NOTE—The following abbreviations are used: *HDGM: HDX and GMII *FDGM: FDX and GMII *HDTE: HDX and DTE					

36.7.4 PICS proforma tables for the PCS and PMA sublayer, type 1000BASE-X

36.7.4.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Test functions Annex 36A support	36.3.8		O	Yes [ ] No [ ]
CC2	Environmental specifications	36.6		M	Yes [ ]

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36.7.4.2 Code-group functions

Item	Feature	Subclause	Value/Comment	Status	Support
CG1	Transmitter initial running disparity	36.2.4.4	Transmitter initial running disparity assumes negative value	M	Yes [ ]
CG2	Transmitter running disparity calculation	36.2.4.4	Running disparity is calculated after each code-group transmitted	M	Yes [ ]
CG3	Validating received code-groups	36.2.4.6		M	Yes [ ]
CG4	Running disparity rules	36.2.4.4	Running disparity is calculated after each code-group reception	M	Yes [ ]
CG5	Transmitted code-group is chosen from the corresponding running disparity	36.2.4.5		M	Yes [ ]

36.7.4.3 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	Transmit ordered_set	36.2.5.2.1	Meets the requirements of Figure 36–5	M	Yes [ ]
SD2	Transmit code-group	36.2.5.2.1	Meets the requirements of Figure 36–6	M	Yes [ ]
SD3	Receive	36.2.5.2.2	Meets the requirements of Figures 36–7a and 36–7b	M	Yes [ ]
SD4	Carrier sense	36.2.5.2.5	Meets the requirements of Figure 36–8	M	Yes [ ]
SD5	Synchronization	36.2.5.2.6	Meets the requirements of Figure 36–9	M	Yes [ ]
SD6	Auto-Negotiation	36.2.5.2.7	Described in Clause 37	M	Yes [ ]

36.7.4.4 PMA functions

Item	Feature	Subclause	Value/Comment	Status	Support
PMA1	Transmit function	36.3.2.2		M	Yes [ ]
PMA2	Receive function	36.3.2.3		M	Yes [ ]
PMA3	Code-group alignment	36.3.2.4	When EN_CDET is active	M	Yes [ ]
PMA4	Loopback mode	36.3.7		M	Yes [ ]

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36.7.4.5 PMA transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
PMT1	cg_timer expiration	36.2.5.1.7	See 35.4.2.3	GMII:M	Yes [ ] N/A [ ]
PMT2	cg_timer expiration	36.2.5.1.7	8 ns ± 0.01%	!GMII: M	Yes [ ] N/A [ ]

36.7.4.6 PMA code-group alignment function

Item	Feature	Subclause	Value/Comment	Status	Support
CDT1	Code-group alignment to comma-	36.3.2.4		O	Yes [ ] N/A [ ]
CDT2	Code-group slipping limit	36.3.2.4	Deletion or modification of no more than four code-groups	M	Yes [ ]
CDT3	Code-group alignment to comma+	36.3.2.4		O	Yes [ ] N/A [ ]

36.7.4.7 TBI

Item	Feature	Subclause	Value/Comment	Status	Support
TBI1	TBI requirements	36.3.3		PMA:M	Yes [ ] N/A [ ]

36.7.4.8 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	Equal carrier de-assertion and assertion delay on CRS	36.5.1		HDGM:M	Yes [ ] N/A [ ]
TIM2	MDI to GMII delay constraints for half duplex	36.5.1	Table 36–9a	HDGM:M	Yes [ ] N/A [ ]
TIM3	MDI to GMII delay constraints for full duplex	36.5.1	Table 36–9b	FDGM:M	Yes [ ] N/A [ ]
TIM4	DTE delay constraints for half duplex	36.5.2	Table 36–10	HDTE:M	Yes [ ] N/A [ ]
TIM5	Carrier de-assertion/assertion constraints	36.5.3		HDTE:M	Yes [ ] N/A [ ]

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37. Auto-Negotiation function, type 1000BASE-X

37.1 Overview

37.1.1 Scope

Clause 37 describes the 1000BASE-X Auto-Negotiation (AN) function that allows a device (local device) to advertise modes of operation it possesses to a device at the remote end of a link segment (link partner) and to detect corresponding operational modes that the link partner may be advertising.

The Auto-Negotiation function exchanges information between two devices that share a link segment and automatically configures both devices to take maximum advantage of their abilities. Auto-Negotiation is performed with /C/ and /I/ ordered_sets defined in Clause 36, such that no packet or upper layer protocol overhead is added to the network devices. Auto-Negotiation does not test the link segment characteristics (see 37.1.4).

The function allows the devices at both ends of a link segment to advertise abilities, acknowledge receipt and understanding of the common mode(s) of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function (see 37.2.4.2). The Auto-Negotiation function allows the devices to switch between the various operational modes in an ordered fashion, permits management to disable or enable the Auto-Negotiation function, and allows management to select a specific operational mode.

The basic mechanism to achieve Auto-Negotiation is to pass information encapsulated within /C/ ordered_sets. /C/ ordered_sets are directly analogous to FLP Bursts as defined in Clause 28 that accomplish the same function. Each device issues /C/ ordered_sets at power up, on command from management, upon detection of a PHY error, or due to user interaction.

37.1.2 Application perspective/objectives

This Auto-Negotiation function is designed to be expandable and allows 1000BASE-X devices to self-configure a jointly compatible operating mode.

The following are the objectives of Auto-Negotiation:

a) To be reasonable and cost-effective to implement;
b) Must provide a sufficiently extensible code space to
    3) Meet existing and future requirements;
    4) Allow simple extension without impacting the installed base;
    5) Accommodate remote fault signals; and
    6) Accommodate link partner ability detection.
c) Must allow manual or Network Management configuration to override the Auto-Negotiation;
d) Must be capable of operation in the absence of Network Management;
e) Must allow the ability to renegotiate;
f) Must operate when
    1) The link is initially connected;
    2) A device at either end of the link is powered up, reset, or a renegotiation request is made.
g) May be enabled by automatic, manual, or Network Management intervention;
h) To complete the base page Auto-Negotiation function in a bounded time period;
i) To operate using a peer-to-peer exchange of information with no requirement for a master device (not master-slave);
j) Must be robust in the 1000BASE-X MDI cable noise environment;
k) Must not significantly impact EMI/RFI emissions.

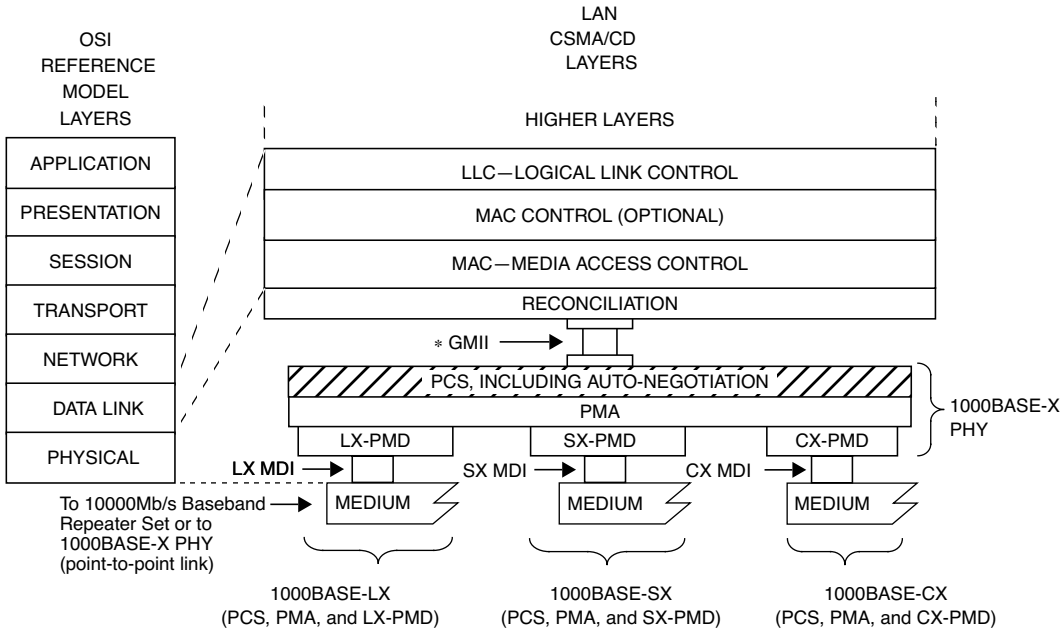
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37.1.3 Relationship to ISO/IEC 8802-3

The Auto-Negotiation function is provided at the PCS sublayer of the Physical Layer of the OSI reference model as shown in Figure 36–1. Devices that support multiple modes of operation may advertise this fact using this function. The transfer of information is observable only at the MDI or on the medium.



MDI=MEDIUM DEPENDENT INTERFACE
GMII=GIGABIT MEDIA INDEPENDENT INTERFACE
PCS=PHYSICAL CODING SUBLAYER
PMA=PHYSICAL MEDIUM ATTACHMENT
PHY=PHYSICAL LAYER DEVICE
PMD=PHYSICAL MEDIUM DEPENDENT
LX-PMD=PMD FOR FIBER—LONG WAVELENGTH, Clause 38
SX-PMD=PMD FOR FIBER—SHORT WAVELENGTH, Clause 38
CX-PMD=PMD FOR 150 Ω BALANCED COPPER CABLING, Clause 39

NOTE—The PMD sublayers are mutually independent.

* GMII is optional.

Figure 37–1—Location of the Auto-Negotiation function

37.1.4 Compatibility considerations

37.1.4.1 Auto-Negotiation

1000BASE-X devices provide the Auto-Negotiation function. Auto-Negotiation does not perform cable tests, such as cable performance measurements. Some PHYs that explicitly require use of high-performance cables, may require knowledge of the cable type, or additional robustness tests (such as monitoring invalid code-groups, CRC, or framing errors) to determine if the link segment is adequate.

37.1.4.2 Management interface

Manual or automatic invocation of Auto-Negotiation may result in frame loss. Exit from Auto-Negotiation to normal MAC frame processing may also result in frame loss as one link end may resume normal MAC frame processing ahead of its link partner.

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37.1.4.2.1 GMII management interface

Auto-Negotiation signaling does not occur across the GMII. Control of the Auto-Negotiation function may be supported through the Management Interface of the GMII or equivalent. If an explicit embodiment of the GMII is supported, the Control and Status registers to support the Auto-Negotiation function shall be implemented in accordance with the definitions in Clause 22 and 37.2.5.

37.1.4.3 Interoperability between Auto-Negotiation compatible devices

An Auto-Negotiation compatible device decodes the base page from the received /C/ ordered_sets and examines the contents for the highest common ability that both devices share. Both devices acknowledge correct receipt of each other's base page by responding with base pages containing the Acknowledge Bit set. After both devices complete acknowledgment, and any desired next page exchange, both devices enable the highest common mode negotiated. The highest common mode is resolved using the priority resolution hierarchy specified in 37.2.4.2.

37.1.4.4 User Configuration with Auto-Negotiation

Rather than disabling Auto-Negotiation, the following behavior is suggested in order to improve interoperability with other Auto-Negotiation devices. When a device is configured for one specific mode of operation (e.g. 1000BASE-X Full Duplex), it is recommended to continue using Auto-Negotiation but only advertise the specifically selected ability or abilities. This can be done by the Management agent only setting the bits in the advertisement registers that correspond to the selected abilities.

37.2 Functional specifications

The Auto-Negotiation function includes the Auto-Negotiation Transmit, Receive, and Arbitration functions specified in the state diagram of Figure 37–6 and utilizes the PCS Transmit and Receive state diagrams of Clause 36.

The Auto-Negotiation function provides an optional Management function that provides a control and status mechanism. Management may provide additional control of Auto-Negotiation through the Management function, but the presence of a management agent is not required.

37.2.1 Config_Reg encoding

The Config_Reg base page, transmitted by a local device or received from a link partner, is encapsulated within a /C/ ordered_set and shall convey the encoding shown in Figure 37–2. Auto-Negotiation supports additional pages using the Next Page function. Encodings for the Config_Reg(s) used in next page exchange are defined in 37.2.4.3.1. Config_Reg bits labeled as "rsvd" are reserved and shall be set to a logic zero.

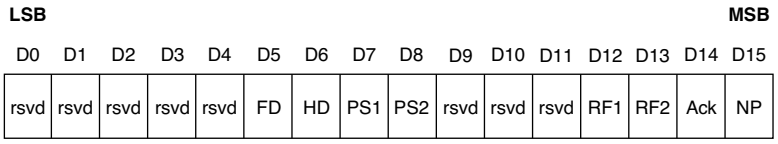


Figure 37–2—Config_Reg base page encoding

37.2.1.1 Base page to management register mapping

Several base page bits shown in Figure 37–2 indicate capabilities that are sourced from management registers. Table 37–1 describes how the management registers map to the management function interface signals.

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The bit format of the rx_Config_Reg<D15:D0> and tx_Config_Reg<D15:D0> variables is context dependent, relative to the state of the Auto-Negotiation function, and is presented here and in 37.2.4.3.1.

Table 37–1—Config_Reg base page to management register mapping

Config_Reg base page bits	Management register bit
Full Duplex (FD)	4.5 Full Duplex
Half Duplex (HD)	4.6 Half Duplex
PAUSE (PS1)	4.7 PAUSE
ASM_DIR (PS2)	4.8 ASM_DIR
Remote Fault (RF2, RF1)	4.13:12 Remote Fault

37.2.1.2 Full duplex

Full Duplex (FD) is encoded in bit D5 of the base Config_Reg.

37.2.1.3 Half duplex

Half Duplex (HD) is encoded in bit D6 of the base Config_Reg.

37.2.1.4 Pause

Pause (PS1, PS2) is encoded in bits D7 and D8 of the base Config_Reg. Pause provides a pause capability exchange mechanism. Pause encoding is specified in Table 37–2.

Table 37–2—Pause encoding

PAUSE (D7)	ASM_DIR(D8)	Capability
0	0	No PAUSE
0	1	Asymmetric PAUSE toward link partner
1	0	Symmetric PAUSE
1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device

The PAUSE bit indicates that the device is capable of providing the symmetric PAUSE functions as defined in Annex 31B. The ASM_DIR bit indicates that asymmetric PAUSE operation is supported. The value of the PAUSE bit when the ASM_DIR bit is set indicates the direction PAUSE frames are supported for flow across the link. Asymmetric PAUSE configuration results in independent enabling of the PAUSE receive and PAUSE transmit functions as defined by Annex 31B. See 37.2.4.2 for PAUSE configuration resolution.

37.2.1.5 Remote fault

Sensing of faults in a device as well as subsequent association of faults with the Remote Fault function encodings is optional. Remote Fault (RF) is encoded in bits D12 and D13 of the base page. The default value

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is 0b00. Remote Fault provides a standard transport mechanism for the transmission of simple fault and error information. The Remote Fault function may indicate to the link partner that a fault or error condition has occurred. The two Remote Fault bits, RF1 and RF2, shall be encoded as specified in Table 37–3.

Table 37–3—Remote Fault encoding

RF1	RF2	Description
0	0	No error, link OK (default)
0	1	Offline
1	0	Link_Failure
1	1	Auto-Negotiation_Error

If the local device has no mechanism to detect a fault or associate a fault condition with the received Remote Fault function encodings, then it shall transmit the default Remote Fault encoding of 0b00.

A local device may indicate it has sensed a fault to its link partner by setting a nonzero Remote Fault encoding in its base page and renegotiating.

If the local device sets the Remote Fault encoding to a nonzero value, it may also use the Next Page function to specify information about the fault that has occurred. Remote Fault Message Page Codes may be specified for this purpose (see Annex 28C).

The Remote Fault encoding shall remain set until after the Auto-Negotiation process transitions into IDLE_DETECT state with the base page, at which time the Remote Fault encoding is reset to 0b00. On receipt of a base page with a nonzero Remote Fault encoding, the device shall set the Remote Fault bit in the Status register (1.4) to logic one if the GMII management function is present.

37.2.1.5.1 No error, link OK

A Remote Fault encoding of 0b00 indicates that no remote fault or error condition has been detected by the local device.

37.2.1.5.2 Offline

A Remote Fault encoding of 0b01 indicates that the local device is going Offline. A local device may indicate Offline prior to powering off, running transmitter tests, or removing the local device from the active configuration. A local device need not successfully complete the Auto-Negotiation function from the receive perspective after completing the Auto-Negotiation function indicating Offline from its transmit perspective before further action is taken (e.g., powering off, running transmitter tests, removing the local device from the active configuration, etc.).

37.2.1.5.3 Link_Failure

A Remote Fault encoding of 0b10 indicates that the local device has detected a Link_Failure condition indicated by loss of synchronization. While sync_status = FAIL, remote fault information is not signaled. When sync_status becomes OK, stored remote fault information is signaled (see 36.2.5.1.3 and 36.2.5.2.6). Another indication of a link failure condition is provided by the reception of /C/ ordered_sets having rx_Config_Reg<D15:D0> = 0 for a duration exceeding link_timer.

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37.2.1.5.4 Auto-Negotiation_Error

A Remote Fault encoding of 0b11 indicates that the local device has detected a Auto-Negotiation_Error. Resolution which precludes operation between a local device and link partner shall be reflected to the link partner by the local device by indicating a Remote Fault code of Auto-Negotiation_Error.

37.2.1.6 Acknowledge

Acknowledge (Ack) is encoded in bit D14 of the base and next pages (see Figures 37–2, 37–3, and 37–4). The Ack bit is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner's base or next page.

This bit is set to logic one after the device has successfully received at least three consecutive and matching rx_Config_Reg<D15:D0> values (ignoring the Acknowledge bit value), and, for next page exchanges, remains set until the next page information has been loaded into the AN next page transmit register (register 7). After the Auto-Negotiation process COMPLETE_ACKNOWLEDGE state has been entered, the tx_Config_Reg<D15:D0> value is transmitted for the link_timer duration.

37.2.1.7 Next page

The base page and subsequent next pages may set the NP bit to a logic one to request next page transmission. Subsequent next pages may set the NP bit to a logic zero in order to communicate that there is no more next page information to be sent (see 37.2.4.3). A device may implement next page ability and choose not to engage in a Next Page exchange by setting the NP bit to a logic zero.

37.2.2 Transmit function requirements

The Transmit function provides the ability to transmit /C/ ordered_sets. After Power-On, link restart, or renegotiation, the Transmit function transmits /C/ ordered_sets containing zeroes indicating the restart condition. After sending sufficient zeroes, the /C/ ordered_sets contain the Config_Reg base page value defined in 37.2.1. The local device may modify the Config_Reg value to disable an ability it possesses, but shall not transmit an ability it does not possess. This makes possible the distinction between local abilities and advertised abilities so that devices capable of multiple modes may negotiate to a mode lower in priority than the highest common local ability.

The Transmit function shall utilize the PCS Transmit process specified in 36.2.5.2.1.

37.2.2.1 Transmit function to Auto-Negotiation process interface requirements

The variable tx_Config_Reg<D15:D0> is derived from mr_adv_abilities<16:1> or mr_np_tx<16:1>. This variable is the management representation of the AN advertisement register during base page exchange and the AN next page transmit register during next page exchange.

When the xmit variable is set to CONFIGURATION by the Auto-Negotiation process, the PCS Transmit function encodes the contents of the tx_Config_Reg<D15:D0> into the appropriate /C/ ordered_set for transmission onto the MDI. When the xmit variable is set to IDLE by the Auto-Negotiation process, the PCS Transmit function transmits /I/ ordered_sets onto the MDI. When the xmit variable is set to DATA by the Auto-Negotiation process, the PCS Transmit function transmits /I/ ordered_sets interspersed with packets onto the MDI.

37.2.3 Receive function requirements

The PCS Receive function detects /C/ and /I/ ordered_sets. For received /C/, the PCS Receive function decodes the information contained within, and stores the data in rx_Config_Reg<D15:D0>.

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The Receive function shall utilize the PCS Receive process specified in 36.2.5.2.2.

37.2.3.1 Receive function to Auto-Negotiation process interface requirements

The PCS Receive function provides the Auto-Negotiation process and management function with the results of rx_Config_Reg<D15:D0>. The PCS Auto-Negotiation function generates the ability_match, acknowledge_match, consistency_match, and idle_match signals.

The PCS Receive process sets the RX_UNITDATA.indicate(/C/) message when a /C/ ordered_set is received.

The PCS Receive process sets the RX_UNITDATA.indicate(/I/) message when a /I/ ordered_set is received.

The PCS Receive process sets the RX_UNITDATA.indicate(INVALID) message when an error condition is detected while not in normal receive processing (when the xmit variable is set to CONFIGURATION). The error conditions are specified in the PCS Receive state diagram of Figure 36–7a.

37.2.4 Arbitration process requirements

The Arbitration process ensures proper sequencing of the Auto-Negotiation function using the Transmit function and Receive function. The Arbitration process enables the Transmit function to advertise and acknowledge abilities. Upon completion of Auto-Negotiation information exchange, the Arbitration process determines the highest common mode using the priority resolution function and enables the appropriate functions.

37.2.4.1 Renegotiation function

A renegotiation request from any entity, such as a management agent, causes the Auto-Negotiation function to be restarted from Auto-Negotiation process state AN_ENABLE.

37.2.4.2 Priority resolution function

Since a local device and a link partner may have multiple common abilities, a mechanism to resolve which mode to configure is necessary. Auto-Negotiation shall provide the Priority Resolution function that defines the hierarchy of supported technologies.

Priority resolution is supported for pause and half/full duplex modes of operation. Full duplex shall have priority over half duplex mode. Priority resolution for pause capability shall be resolved as specified by Table 37–4. Resolution that precludes operation between a local device and link partner is reflected to the link partner by the local device by indicating a Remote Fault code of Auto-Negotiation_Error, if the remote fault function is supported (see 37.2.1.5).

37.2.4.3 Next Page function

Support for transmission and reception of additional page encodings beyond the base page (next pages) is optional. The Next Page function enables the exchange of user or application specific data. Data is carried by next pages of information, which follow the transmission and acknowledgment procedures used for the base pages. Two types of next page encodings are defined:

a) Message Pages (contain an eleven-bit formatted Message Code Field);

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Table 37–4—Pause priority resolution

Local Device		Link Partner		Local Resolution	Link Partner Resolution
PAUSE	ASM_DIR	PAUSE	ASM_DIR		
0	0	—	—	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	0	—	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	1	Enable PAUSE transmit, Disable PAUSE receive	Enable PAUSE receive, Disable PAUSE transmit
1	0	0	—	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	0	1	—	Enable PAUSE Transmit and Receive	Enable PAUSE Transmit and Receive
1	1	0	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	1	0	1	Enable PAUSE receive, Disable PAUSE transmit	Enable PAUSE transmit, Disable PAUSE receive
1	1	1	—	Enable PAUSE Transmit and Receive	Enable PAUSE Transmit and Receive

b) Unformatted Pages (contain an eleven-bit Unformatted Code Field).

A dual acknowledgment system is used. Acknowledge (Ack) is used to acknowledge receipt of the information (see 37.2.1.6). Acknowledge 2 (Ack2) is used to indicate that the receiver is able to act on the information (or perform the task) defined in the message (see 37.2.4.3.5).

Next page operation is controlled by the same two mandatory control bits, NP and Ack, used in the base page. The Toggle bit is used to ensure proper synchronization between the local device and the link partner.

Next page exchange occurs after the base page exchange has been completed. Next page exchange consists of using the Auto-Negotiation arbitration process to send Message or Unformatted next pages. Unformatted Pages can be combined to send extended messages. Any number of next pages may be sent in any order.

Subsequent to base page exchange, a next page exchange is invoked only if both the local device and its link partner have advertised next page ability during the base page exchange.

If the Next Page function is supported by both link ends and a next page exchange has been invoked by both link ends, the next page exchange ends when both ends of a link segment set their NP bits to logic zero, indicating that neither link end has further pages to transmit. It is possible for the link partner to have more next pages to transmit than the local device. Once a local device has completed transmission of its next page information, if any, it shall transmit Message Pages with a Null Message Code (see Annex 28C) and the NP bit set to logic zero while its link partner continues to transmit valid next pages. A device shall recognize reception of Message Pages with a Null Message Code and the NP bit set to logic zero as the end of its link partner's next page information. If both the local device and its link partner advertise Next Page ability in their base pages, then both devices shall send at least one Next Page. If a device advertises Next Page ability

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and has no next page information to send but is willing to receive next pages, and its link partner also advertises Next Page ability, it shall send a Message Page with a Null Message Code. The variable mr_np_loaded is set to TRUE to indicate that the local device has loaded its Auto-Negotiation next page transmit register with next page information for transmission.

A local device that requires or expects an Ack2 response from its link partner (to indicate a next page transaction has been received and can be acted upon), must terminate the next page sequence with a Null Message Code, in order to allow the link partner to transport the final Ack2 status.

37.2.4.3.1 Next page encodings

The next page shall use the encoding shown in Figure 37–3 and Figure 37–4 for the NP, Ack, MP, Ack2, and T bits. The eleven-bit field <D10:D0> is encoded as a Message Code Field if the MP bit is logic one and an Unformatted Code Field if MP is set to logic zero. The bit format of the rx_Config_Reg<D15:D0> and tx_Config_Reg<D15:D0> variables is context dependent, relative to the state of the Auto-Negotiation function, and is presented here and in 37.2.1.1.

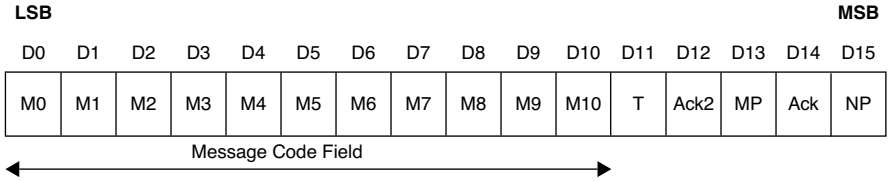


Figure 37–3—Message page encoding

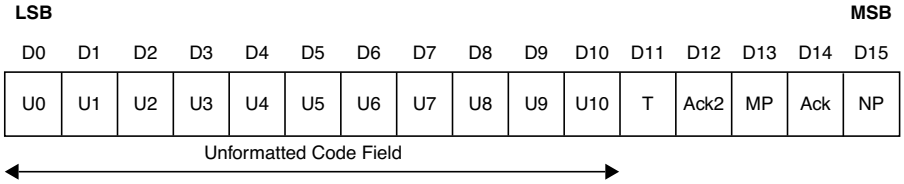


Figure 37–4—Unformatted page encoding

37.2.4.3.2 Next page

The Next Page (NP) bit is used by the Next Page function to indicate whether or not this is the last next page to be transmitted. NP shall be set as follows:

logic zero = Last page.
logic one = Additional next page(s) to follow.

37.2.4.3.3 Acknowledge

As defined in 37.2.1.6.

37.2.4.3.4 Message page

The Message Page (MP) bit is used by the Next Page function to differentiate a Message Page from an Unformatted Page. MP shall be set as follows:

logic zero = Unformatted Page.
logic one = Message Page.

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37.2.4.3.5 Acknowledge 2

The Acknowledge 2 (Ack2) bit is used by the Next Page function to indicate that a device has the ability to comply with the message. Ack2 shall be set as follows:

logic zero = Cannot comply with message.
logic one = Can comply with message.

37.2.4.3.6 Toggle

The Toggle (T) bit is used by the Arbitration function to ensure synchronization with the link partner during next page exchange. This bit takes the opposite value of the Toggle bit in the previously exchanged page. The initial value of the Toggle bit in the first next page transmitted is the inverse of tx_Config_Reg<D11> in the base page that preceded the next page exchange and, therefore, may assume a value of logic one or zero. The Toggle bit is set as follows:

logic zero = Previous value of tx_Config_Reg<D11> equalled logic one.
logic one = Previous value of tx_Config_Reg<D11> equalled logic zero.

37.2.4.3.7 Message page encoding

Message Pages are formatted pages that carry a single predefined Message Code, which is enumerated in Annex 28C. There are 2048 Message Codes available. The allocation of these codes is specified in Annex 28C. If the Message Page bit is set to logic one, the bit encoding of the Config_Reg value is interpreted as a Message Page.

37.2.4.3.8 Message Code Field

Message Code Field (M<10:0>) is an eleven-bit wide field, encoding 2048 possible messages. Message Code Field definitions are shown in Annex 28C. Combinations not specified are reserved for future use. Reserved combinations of the Message Code Field shall not be transmitted.

37.2.4.3.9 Unformatted page encoding

Unformatted Pages carry the messages indicated by Message Pages. Five control bits are predefined, the remaining eleven bits are interpreted based on the preceding message page. If the Message Page bit is set to logic zero, then the bit encoding of the Config_Reg value is interpreted as an Unformatted Page.

37.2.4.3.10 Unformatted Code Field

Unformatted Code Field (U<10:0>) is an eleven-bit wide field, which may contain an arbitrary value.

37.2.4.3.11 Use of next pages

The following rules for next page usage shall be observed:

a) A next page exchange is invoked when the local device and the link partner advertise (in their base pages) that they have next page information to transmit;
b) Next page exchange continues until neither device on a link has more pages to transmit as indicated by the NP bit. A Message Page with a Null Message Code Field value is sent if the device has no other information to transmit;
c) A Message Code can carry either a specific message or information that defines how following Unformatted Page(s) should be interpreted;

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d) If a Message Code references Unformatted Pages, the Unformatted Pages immediately follow the referencing Message Code in the order specified by the Message Code;
e) Unformatted Page users are responsible for controlling the format and sequencing for their Unformatted Pages.

37.2.4.3.12 Management register requirements

The AN next page transmit register defined in 37.2.5.1.6 holds the next page to be sent by Auto-Negotiation. Received next pages are stored in the AN link partner ability next page register defined in 37.2.5.1.7.

37.2.5 Management function requirements

The management interface is used to communicate Auto-Negotiation information to the management entity. Mandatory functions specified here reference bits in GMII registers 0, 1, 4, 5, 6, 7, 8, 15. Where an implementation does not use a GMII, equivalent functions to these bits must be included.

37.2.5.1 Management registers

The Auto-Negotiation function shall utilize six dedicated management registers:

a) Control register (Register 0);
b) Status register (Register 1);
c) AN advertisement register (Register 4);
d) AN link partner ability base page register (Register 5);
e) AN expansion register (Register 6);
f) Extended Status register (Register 15).

If Next Page is supported, the Auto-Negotiation function shall utilize an additional two management registers:

g) AN next page transmit register (Register 7);
h) AN link partner ability next page register (Register 8).

37.2.5.1.1 Control register (Register 0)

This register provides the mechanism to enable or disable Auto-Negotiation, restart Auto-Negotiation, and allow for manual configuration when Auto-Negotiation is not enabled. The definition for this register is provided in Clause 22.

When manual configuration is in effect at a local device, manual configuration should also be effected for the link partner to ensure predictable configuration. When manual configuration is in effect, values for the PAUSE bits (PS1, PS2) should result in a valid operational mode between the local device and the link partner.

37.2.5.1.2 Status register (Register 1)

This register includes information about all modes of operations supported by the local device and the status of Auto-Negotiation. The definition for this register is provided in Clause 22.

37.2.5.1.3 AN advertisement register (Register 4) (R/W)

This register contains the advertised ability of the local device (see Table 37–5). Before Auto-Negotiation starts, this register is configured to advertise the abilities of the local device.

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Table 37–5—AN advertisement register bit definitions

Bit(s)	Name	Description	R/W
4.15	Next Page	See 37.2.1.7	R/W
4.14	Reserved	Write as zero, ignore on read	RO
4.13:12	Remote Fault	See 37.2.1.5	R/W
4.11:9	Reserved	Write as zero, ignore on read	RO
4.8:7	Pause	See 37.2.1.4	R/W
4.6	Half Duplex	See 37.2.1.3	R/W
4.5	Full Duplex	See 37.2.1.2	R/W
4.4:0	Reserved	Write as zero, ignore on read	RO

37.2.5.1.4 AN link partner ability base page register (Register 5) (RO)

All of the bits in the AN link partner ability base page register are read only. A write to the AN link partner ability base page register has no effect.

This register contains the advertised ability of the link partner (see Table 37–6). The bit definitions are a direct representation of the link partner's base page. Upon successful completion of Auto-Negotiation, the Status register Auto-Negotiation Complete bit (1.5) is set to logic one.

The values contained in this register are guaranteed to be valid either once Auto-Negotiation has successfully completed, as indicated by bit 1.5 or when the Page Received bit (6.1) is set to logic one to indicate that a new base page has been received and stored in the Auto-Negotiation link partner ability base register.

Table 37–6—AN link partner ability base page register bit definitions

Bit(s)	Name	Description	R/W
5.15	Next Page	See 37.2.1.7	RO
5.14	Acknowledge	See 37.2.1.6	RO
5.13:12	Remote Fault	See 37.2.1.5	RO
5.11:9	Reserved	Ignore on read	RO
5.8:7	Pause	See 37.2.1.4	RO
5.6	Half Duplex	See 37.2.1.3	RO
5.5	Full Duplex	See 37.2.1.2	RO
5.4:0	Reserved	Ignore on read	RO

37.2.5.1.5 AN expansion register (Register 6) (RO)

All of the bits in the Auto-Negotiation expansion register are read only; a write to the Auto-Negotiation expansion register has no effect.

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Table 37–7—AN expansion register bit definitions

Bit(s)	Name	Description	R/W	Default
6.15:3	Reserved	Ignore on read	RO	0
6.2	Next Page Able	1 = Local device is next page able 0 = Local device is not next page able	RO	0
6.1	Page Received	1 = A new page has been received 0 = A new page has not been received	RO/ LH	0
6.0	Reserved	Ignore on read	RO	0

Bits 6.15:3 and 6.0 are reserved for future Auto-Negotiation expansion.

The Next Page Able bit (6.2) is set to logic one to indicate that the local device supports the Next Page function. The Next Page Able bit is set to logic zero if the Next Page function is not supported by the local device.

The Page Received bit (6.1) is set to logic one to indicate that a new page has been received and stored in the applicable AN link partner ability base or next page register.

The Page Received bit shall be reset to logic zero on a read of the AN expansion register (Register 6). Subsequent to the setting of the Page Received bit, and in order to prevent overlay of the AN link partner ability next page register, the AN link partner ability next page register should be read before the AN next page transmit register is written.

37.2.5.1.6 AN next page transmit register (Register 7)

This register contains the next page value to be transmitted, if required. The definition for this register is provided in 22.2.4.1.6.

37.2.5.1.7 AN link partner ability next page register (Register 8)

This register contains the advertised ability of the link partner's next page. The definition for this register is provided in 32.5.4.2 for changes to 28.2.4.1.4.

37.2.5.1.8 Extended status register (Register 15)

This register includes additional information about all modes of operations supported by the local device. The definition for this register is provided in Clause 22.

37.2.5.1.9 State diagram variable to management register mapping

The state diagram of Figure 37–6 generates and accepts variables of the form "mr_x," where x is an individual signal name. These variables comprise a management interface that may be connected to the GMII management function or other equivalent function. Table 37–8 describes how PCS state diagram variables in both Clauses 36 and 37 map to management register bits.

37.2.5.2 Auto-Negotiation managed object class

The Auto-Negotiation Managed Object Class is defined in Clause 30.

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Table 37–8—PCS state diagram variable to management register mapping

State diagram variable	Management register bit
mr_adv_ability<16:1>	4.15:0 Auto-Negotiation advertisement register
mr_an_complete	1.5 Auto-Negotiation complete
mr_an_enable	0.12 Auto-Negotiation enable
mr_loopback	0.14 Loopback (see 36.2.5.1.3)
mr_lp_adv_ability<16:1>	5.15:0 AN link partner ability register
mr_lp_np_rx<16:1>	8.15:0 AN link partner next page ability register
mr_main_reset	0.15 Reset
mr_np_able	6.2 Next page able
mr_np_loaded	Set on write to the AN next page transmit register; cleared by Auto-Negotiation state diagram
mr_np_tx<16:1>	7.15:0 AN next page transmit register
mr_page_rx	6.1 Page received
mr_restart_an	0.9 Auto-Negotiation restart
xmit=DATA	1.2 Link status

37.2.6 Absence of management function

In the absence of any management function, the advertised abilities shall be provided through a logical equivalent of mr_adv_ability<16:1>.

37.3 Detailed functions and state diagrams

The notation used in the state diagram in Figure 37–6 follows the conventions in 21.5. State diagram variables follow the conventions of 21.5.2 except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set. Variables using the “mr_x” notation do not have state diagram defaults; however, their appropriate initialization conditions when mapped to the management interface are covered in 22.2.4. The variables, timers, and counters used in the state diagrams are defined in 37.3.1.

Auto-Negotiation shall implement the Auto-Negotiation state diagram and meet the Auto-Negotiation state diagram interface requirements of the Receive and Transmit functions. Additional requirements to these state diagrams are made in the respective functional requirements sections. In the case of any ambiguity between stated requirements and the state diagrams, the state diagrams take precedence. A functional reference diagram of Auto-Negotiation is shown in Figure 37–5.

37.3.1 State diagram variables

Variables with <16:1> or <D15:D0> appended to the end of the variable name indicate arrays that can be mapped to 16-bit management registers. For these variables, “<x>” indexes an element or set of elements in the array, where “x” may be as follows:

— Any integer or set of integers.

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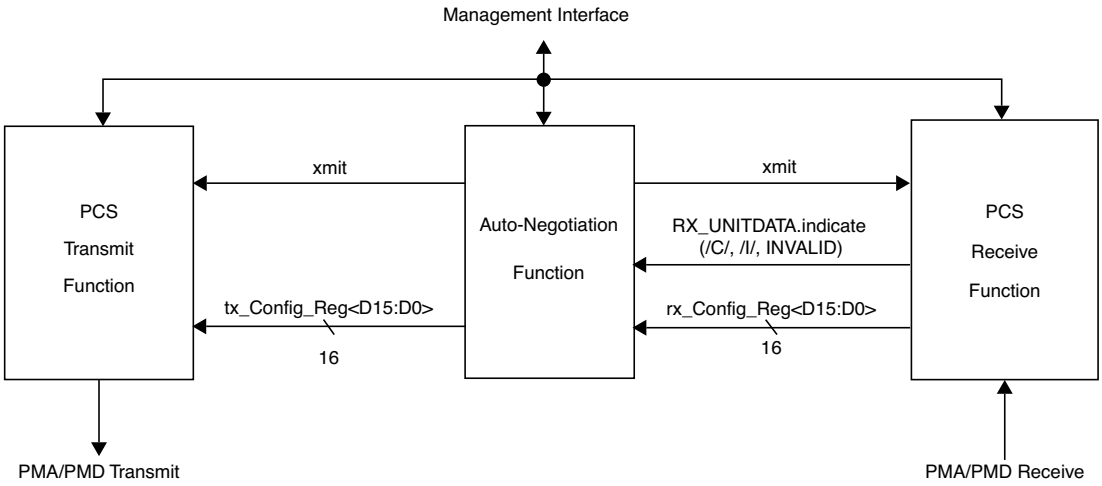


Figure 37–5—Functional reference diagram

— Any variable that takes on integer values.
— NP; represents the index of the Next Page bit.
— ACK; represents the index of the Acknowledge bit.
— RF; represents the index of the Remote Fault bits.

Variables of the form "mr_x," where x is a label, comprise a management interface that is intended to be connected to the GMII Management function. However, an implementation-specific management interface may provide the control and status function of these bits.

37.3.1.1 Variables

an_sync_status
: Qualified version of sync_status for use by Auto-Negotiation to detect a sync_status timeout condition.

  Values: OK; The variable sync_status defined in 36.2.5.1.3 is OK.
  FAIL; The variable sync_status defined in 36.2.5.1.3 is FAIL for a duration greater than or equal to the link timer.

mr_adv_ability<16:1>
: A 16-bit array that contains the advertised ability base page of the local device to be conveyed to tx_Config_Reg<D15:D0> for transmission to the link partner. For each element within the array:

  Values: ZERO; Data bit is logical zero.
  ONE; Data bit is logical one.

mr_an_complete
: Status indicating whether Auto-Negotiation has completed or not.

  Values: FALSE; Auto-Negotiation has not completed.
  TRUE; Auto-Negotiation has completed.

mr_an_enable
: Controls the enabling and disabling of the Auto-Negotiation function for 1000BASE-X. Auto-Negotiation function for 1000BASE-X is enabled when Control register bit 0.12 is set to one.

  Values: FALSE; Auto-Negotiation is disabled.
  TRUE; Auto-Negotiation is enabled.

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mr_lp_adv_ability<16:1>

A 16-bit array that contains the advertised ability base page of the link partner conveyed from rx_Config_Reg<D15:D0>. For each element within the array:

Values: ZERO; Data bit is logical zero.
ONE; Data bit is logical one.

mr_lp_np_rx<16:1>

A 16-bit array that contains the advertised ability of the link partner's next page conveyed from rx_Config_Reg<D15:D0>. For each element within the array:

Values: ZERO; Data bit is logical zero.
ONE; Data bit is logical one.

mr_main_reset

Controls the resetting of the Auto-Negotiation function.

Values: FALSE; Do not reset the Auto-Negotiation function.
TRUE; Reset the Auto-Negotiation function.

mr_np_able

Status indicating whether the local device supports next page exchange.

Values: FALSE; The local device does not support next page exchange.
TRUE; The local device supports next page exchange.

mr_np_loaded

Status indicating whether a new page has been loaded into the AN next page transmit register (register 7).

Values: FALSE; A new page has not been loaded.
TRUE; A new page has been loaded.

mr_np_tx<16:1>

A 16-bit array that contains the new next page to transmit. If a next page exchange is invoked, this array is conveyed to tx_Config_Reg<D15:D0> for transmission to the link partner. For each element within the array:

Values: ZERO; Data bit is logical zero.
ONE; Data bit is logical one.

mr_page_rx

Status indicating whether a new page has been received. A new page has been successfully received when acknowledge_match=TRUE and consistency_match=TRUE and the rx_Config_Reg<D15:D0> value has been written to mr_lp_adv_ability<16:1> or mr_lp_np_rx<16:1>, depending on whether the page received was a base or next page, respectively.

Values: FALSE; A new page has not been received.
TRUE; A new page has been received.

NOTE—For the first setting of mr_page_rx, mr_lp_adv_ability is valid but need not be read as it is preserved through a next page operation. On subsequent settings of mr_page_rx, mr_lp_np_rx must be read prior to loading mr_np_tx register in order to avoid the overlay of next page information.

mr_restart_an

Controls renegotiation via management control.

Values: FALSE; Do not restart Auto-Negotiation.
TRUE; Restart Auto-Negotiation.

np_rx

Flag to hold value of rx_Config_Reg<NP> upon entry to state COMPLETE ACKNOWLEDGE.

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This value is associated with the value of rx_Config_Reg<NP> when acknowledge_match was last set.

Values: ZERO; The local device np_rx bit equals logic zero.
ONE; The local device np_rx bit equals logic one.

power_on

Condition that is true until such time as the power supply for the device that contains the Auto-Negotiation function has reached the operating region. The condition is also true when the device has low power mode set via Control register bit 0.11.

Values: FALSE; The device is completely powered (default).
TRUE; The device has not been completely powered.

NOTE—Power_on evaluates to its default value in each state where it is not explicitly set.

resolve_priority

Controls the invocation of the priority resolution function specified in Table 37–4.

Values: OFF; The priority resolution function is not invoked (default).
ON; The priority resolution function is invoked.

NOTE—Resolve_priority evaluates to its default value in each state where it is not explicitly set.

rx_Config_Reg<D15:D0>

Defined in 36.2.5.1.3.

sync_status

Defined in 36.2.5.1.3.

toggle_rx

Flag to keep track of the state of the link partner Toggle bit.

Values: ZERO; The link partner Toggle bit equals logic zero.
ONE; The link partner Toggle bit equals logic one.

toggle_tx

Flag to keep track of the state of the local device Toggle bit.

Values: ZERO; The local device Toggle bit equals logic zero.
ONE; The local device Toggle bit equals logic one.

tx_Config_Reg<D15:D0>

Defined in 36.2.5.1.3. This array may be loaded from mr_adv_ability or mr_np_tx.

xmit

A parameter set by the PCS Auto-Negotiation process to reflect the source of information to the PCS Transmit process.

Values: CONFIGURATION: Tx_Config_Reg<D15:D0> information is being sourced from the PCS Auto-Negotiation process.
DATA: /I/, sourced from the PCS, is interspersed with packets sourced from the MAC.
IDLE: /I/ is being sourced from the PCS Auto-Negotiation process.

37.3.1.2 Functions

ability_match

For a stream of /C/ and /I/ ordered_sets, this function continuously indicates whether the last three consecutive rx_Config_Reg<D15,D13:D0> values match. Three consecutive rx_Config_Reg<D15,D13:D0> values are any three rx_Config_Reg<D15,D13:D0> values received one after the other, regardless of whether the rx_Config_Reg<D15,D13:D0> value has

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already been used in a rx_Config_Reg<D15,D13:D0> match comparison or not. The match count is reset upon receipt of /I/. The match count is reset upon receipt of a second or third consecutive rx_Config_Reg<D15,D13:D0> value which does not match the rx_Config_Reg<D15,D13:D0> values for which the match count was set to one.

Values: FALSE; Three matching consecutive rx_Config_Reg<D15,D13:D0> values have not been received (default).
TRUE; Three matching consecutive rx_Config_Reg<D15,D13:D0> values have been received.

NOTE—Ability_match is set by this function definition; it is not set explicitly in the state diagrams. Ability_match evaluates to its default value upon state entry.

acknowledge_match

For a stream of /C/ and /I/ ordered_sets, this function continuously indicates whether the last three consecutive rx_Config_Reg<D15:D0> values match and have the Acknowledge bit set. Three consecutive rx_Config_Reg<D15:D0> values are any three rx_Config_Reg<D15:D0> values contained within three /C/ ordered_sets received one after the other, regardless of whether the rx_Config_Reg<D15:D0> value has already been used in a rx_Config_Reg<D15:D0> match comparison or not. The match count is reset upon receipt of /I/. The match count is reset upon receipt of a second or third consecutive rx_Config_Reg<D15:D0> value which does not match the rx_Config_Reg<D15:D0> values for which the match count was set to one.

Values: FALSE; Three matching and consecutive rx_Config_Reg<D15:D0> values have not been received with the Acknowledge bit set (default).
TRUE; Three matching and consecutive rx_Config_Reg<D15:D0> values have been received with the Acknowledge bit set.

NOTE—Acknowledge_match is set by this function definition; it is not set explicitly in the state diagrams. Acknowledge_match evaluates to its default value upon state entry.

an_enableCHANGE

This function monitors the mr_an_enable variable for a state change. The function is set to TRUE on state change detection.

Values: TRUE; A mr_an_enable variable state change has been detected.
FALSE; A mr_an_enable variable state change has not been detected (default).

NOTE—An_enableCHANGE is set by this function definition; it is not set explicitly in the state diagrams. An_enableCHANGE evaluates to its default value upon state entry.

consistency_match

Indicates that the rx_Config_Reg<D15,D13:D0> value that caused ability_match to be set, for the transition from states ABILITY_DETECT or NEXT_PAGE_WAIT to state ACKNOWLEDGE_DETECT, is the same as the rx_Config_Reg<D15,D13:D0> value that caused acknowledge_match to be set.

Values: FALSE; The rx_Config_Reg<D15,D13:D0> value that caused ability_match to be set is not the same as the rx_Config_Reg<D15,D13:D0> value that caused acknowledge_match to be set, ignoring the Acknowledge bit value.
TRUE; The rx_Config_Reg<D15,D13:D0> value that caused ability_match to be set is the same as the rx_Config_Reg<D15,D13:D0> value that caused acknowledge_match to be set, independent of the Acknowledge bit value.

NOTE—Consistency_match is set by this function definition; it is not set explicitly in the state diagrams.

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idle_match
: For a stream of /C/ and /I/ ordered_sets, this function continuously indicates whether three consecutive /I/ ordered_sets have been received. The match count is reset upon receipt of /C/.

  Values: FALSE; Three consecutive /I/ ordered_sets have not been received (default).
  TRUE; Three consecutive /I/ ordered_sets have been received.

NOTE—Idle_match is set by this function definition; it is not set explicitly in the state diagrams. Idle_match evaluates to its default value upon state entry.

37.3.1.3 Messages

RUDI
: Alias for RX_UNITDATA.indicate(parameter). Defined in 36.2.5.1.6.

RX_UNITDATA.indicate
: Defined in 36.2.5.1.6.

37.3.1.4 Timers

All timers operate in the manner described in 14.2.3.2.

link_timer
: Timer used to ensure Auto-Negotiation protocol stability and register read/write by the management interface.

  Duration: 10 ms, tolerance +10 ms, –0 s.

37.3.1.5 State diagrams

The Auto-Negotiation state diagram is specified in Figure 37–6.

37.4 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801: 1995.

37.5 Protocol Implementation Conformance Statement (PICS) proforma for Clause 37, Auto-Negotiation function, type 1000BASE-X[4]

37.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 37, Auto-Negotiation function, type 1000BASE-X, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

37.5.2 Identification

[4]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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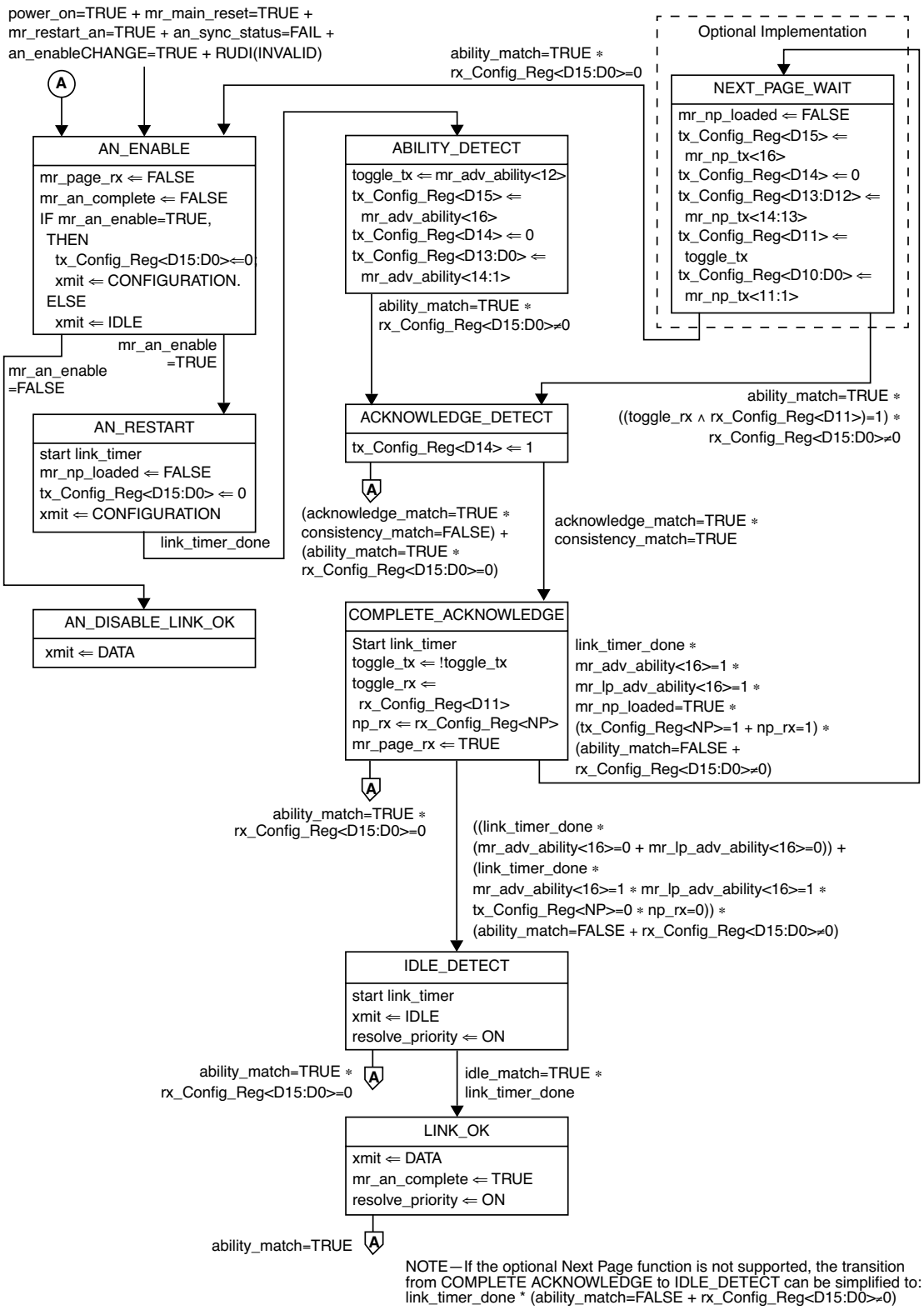


Figure 37–6—Auto-Negotiation state diagram

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37.5.2.1 Implementation identification

Supplier (Note 1)	
Contact point for enquiries about the PICS (Note 1)	
Implementation Name(s) and Version(s) (Notes 1 and 3)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s) (Note 2)	

NOTE 1—Required for all implementations.

NOTE 2—May be completed as appropriate in meeting the requirements for the identification.

NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).

37.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2002, Clause 37, Auto-Negotiation function, type 1000BASE-X
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	No [ ] Yes [ ]

Date of Statement	

37.5.3 Major Capabilities/Options

Item	Feature	Subclause	Value/Comment	Status	Support
*GMII	GMII Management Interface	37.1.4.2.1		O	Yes [ ] No [ ]
*RF	Remote Fault function	37.2.1.5		O	Yes [ ] No [ ]
*NP	Next Page function	37.2.4.3		O	Yes [ ] No [ ]

In addition, the following predicate name is defined for use when different implementations from the set above have common parameters:

*NPM: GMII and NP

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37.5.4 PICS proforma tables for the Auto-Negotiation function, type 1000BASE-X

37.5.4.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Provision of logical equivalent of mr_adv_ability<16:1>	37.2.6	In the absence of any management function	M	Yes [ ]
CC2	Environmental specifications	37.4		M	Yes [ ]

37.5.4.2 Auto-Negotiation functions

Item	Feature	Subclause	Value/Comment	Status	Support
AN1	Config_Reg encoding	37.2.1		M	Yes [ ]
AN2	Priority Resolution function	37.2.4.2		M	Yes [ ]
AN3	Auto-Negotiation state diagram	37.3		M	Yes [ ]

37.5.4.2.1 Config_Reg

Item	Feature	Subclause	Value/Comment	Status	Support
CR1	Reserved bits	37.2.1	Set to zero	M	Yes [ ]
CR2	Default encoding of Remote Fault bits	37.2.1.5	0b00	M	Yes [ ]

37.5.4.2.2 Remote Fault functions

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Remote Fault encoding	37.2.1.5		RF:M	Yes [ ] N/A [ ]
RF2	Use of Remote Fault Message Page code	37.2.1.5	To signal additional fault information	RF:O	Yes [ ] No [ ]
RF3	Notification duration	37.2.1.5	Remains set until transition to IDLE_DETECT state, then reset to 0b00	RF:M	Yes [ ] N/A [ ]
RF4	Status Register RF bit (1.4)	37.2.1.5	Upon detection of nonzero Remote Fault encoding	RF:M	Yes [ ] N/A [ ]
RF5	Offline indication	37.2.1.5.2	0b01	RF:O	Yes [ ] No [ ]
RF6	Link_Failure indication	37.2.1.5.3	0b10	RF:O	Yes [ ] No [ ]
RF7	Auto-Negotiation_Error	37.2.1.5.4	0b11	RF:M	Yes [ ] N/A [ ]

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37.5.4.2.3 AN transmit functions

Item	Feature	Subclause	Value/Comment	Status	Support
TX1	PCS Transmit function support	37.2.2		M	Yes [ ]
TX2	Transmission of non-possessive abilities	37.2.2	A device shall not transmit an ability it does not possess.	M	Yes [ ]

37.5.4.2.4 AN receive functions

Item	Feature	Subclause	Value/Comment	Status	Support
RX1	PCS Receive function support	37.2.3		M	Yes [ ]

37.5.4.2.5 Priority resolution functions

Item	Feature	Subclause	Value/Comment	Status	Support
PR1	Full duplex priority over half duplex	37.2.4.2		M	Yes [ ]
PR2	Priority resolution for pause capability	37.2.4.2	Specified in Table 37–4	M	Yes [ ]

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37.5.4.2.6 Next page functions

Item	Feature	Subclause	Value/Comment	Status	Support
	Transmission of Message Pages with a Null Message Code	37.2.4.3	Upon local device completion of next page requests	NP:M	Yes [ ] N/A [ ]
	Recognition of Message Pages with a Null Message Code	37.2.4.3	Signifies the end of link partner next page information	NP:M	Yes [ ] N/A [ ]
	Initial Next Page Exchange	37.2.4.3	Upon advertisement of NP ability by both devices	NP:M	Yes [ ] N/A [ ]
	Next Page Receipt Ability	37.2.4.3	Indicated by advertising NP ability via the NP bit	NP:M	Yes [ ] N/A [ ]
	Next page Config_Reg encoding	37.2.4.3.1		NP:M	Yes [ ] N/A [ ]
	Next Page (NP) bit setting	37.2.4.3.2	For link_timer after entry into COMPLETE_ACKNOWLEDGE state	NP:M	Yes [ ] N/A [ ]
	Message Page (MP) bit setting	37.2.4.3.4		NP:M	Yes [ ] N/A [ ]
	Acknowledge 2 (Ack2) bit setting	37.2.4.3.5		NP:M	Yes [ ] N/A [ ]
	Message Code Field combinations	37.2.4.3.8	Reserved combinations shall not be transmitted.	NP:M	Yes [ ] N/A [ ]
	Next Page usage rules	37.2.4.3.11		NP:M	Yes [ ] N/A [ ]

37.5.4.2.7 Management registers

Item	Feature	Subclause	Value/Comment	Status	Support
MR1	Control and Status registers	37.1.4.2.1		GMII:M	Yes [ ] N/A [ ]
MR2	Register usage	37.2.5.1	Logical equivalent of Registers 0, 1, 4, 5, 6 and 15	GMII:M	Yes [ ] N/A [ ]
MR3	Next Page Register usage	37.2.5.1	Logical equivalent of Registers 7 and 8	NPM:M	Yes [ ] N/A [ ]
MR4	Page Received resetting	37.2.5.1.5	Reset upon read to AN expansion register	M	Yes [ ]

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38. Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-LX (Long Wavelength Laser) and 1000BASE-SX (Short Wavelength Laser)

38.1 Overview

This clause specifies the 1000BASE-SX PMD and the 1000BASE-LX PMD (including MDI) and baseband medium for multimode and single-mode fiber. In order to form a complete Physical Layer, it shall be integrated with the 1000BASE-X PCS and PMA of Clause 36, and integrated with the management functions which are accessible through the Management Interface defined in Clause 35, which are hereby incorporated by reference.

38.1.1 Physical Medium Dependent (PMD) sublayer service interface

The following specifies the services provided by the 1000BASE-SX and 1000BASE-LX PMD. These PMD sublayers are described in an abstract manner and do not imply any particular implementation. It should be noted that these services are based on similar interfaces defined in ANSI X3.230-1994 [B20] (FC-PH).

The PMD Service Interface supports the exchange of encoded 8B/10B characters between PMA entities. The PMD translates the encoded 8B/10B characters to and from signals suitable for the specified medium.

The following primitives are defined:

PMD_UNITDATA.request
PMD_UNITDATA.indicate
PMD_SIGNAL.indicate

NOTE—Delay requirements from the MDI to GMII that include the PMD layer are specified in Clause 36. Of this budget, 4 ns is reserved for each of the transmit and receive functions of the PMD.

38.1.1.1 PMD_UNITDATA.request

This primitive defines the transfer of data (in the form of encoded 8B/10B characters) from the PMA to the PMD.

38.1.1.1.1 Semantics of the service primitive

PMD_UNITDATA.request (tx_bit)

The data conveyed by PMD_UNITDATA.request is a continuous sequence of encoded 8B/10B characters. The tx_bit parameter can take one of two values: ONE or ZERO.

38.1.1.1.2 When generated

The PMA continuously sends the appropriate encoded 8B/10B characters to the PMD for transmission on the medium, at a nominal 1.25 GBd signaling speed.

38.1.1.1.3 Effect of receipt

Upon receipt of this primitive, the PMD converts the specified encoded 8B/10B characters into the appropriate signals on the MDI.

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38.1.1.2 PMD_UNITDATA.indicate

This primitive defines the transfer of data (in the form of encoded 8B/10B characters) from the PMD to the PMA.

38.1.1.2.1 Semantics of the service primitive

PMD_UNITDATA.indicate (rx_bit)

The data conveyed by PMD_UNITDATA.indicate is a continuous sequence of encoded 8B/10B characters. The rx_bit parameter can take one of two values: ONE or ZERO.

38.1.1.2.2 When generated

The PMD continuously sends encoded 8B/10B characters to the PMA corresponding to the signals received from the MDI.

38.1.1.2.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

38.1.1.3 PMD_SIGNAL.indicate

This primitive is generated by the PMD to indicate the status of the signal being received from the MDI.

38.1.1.3.1 Semantics of the service primitive

PMD_SIGNAL.indicate(SIGNAL_DETECT)

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting light at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, then rx_bit is undefined, but consequent actions based on PMD_UNITDATA.indicate, where necessary, interpret rx_bit as a logic ZERO.

NOTE—SIGNAL_DETECT = OK does not guarantee that rx_bit is known good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the 10^{-12} BER objective.

38.1.1.3.2 When generated

The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT.

38.1.1.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

38.1.2 Medium Dependent Interface (MDI)

The MDI, a physical interface associated with a PMD, is comprised of an electrical or optical medium connection.

38.2 PMD functional specifications

The 1000BASE-X PMDs perform the Transmit and Receive functions that convey data between the PMD service interface and the MDI.

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38.2.1 PMD block diagram

For purposes of system conformance, the PMD sublayer is standardized at the following points. The optical transmit signal is defined at the output end of a patch cord (TP2), between 2 and 5 m in length, of a type consistent with the link type connected to the transmitter receptacle defined in 38.11.2. If a single-mode fiber offset-launch mode-conditioning patch cord is used, the optical transmit signal is defined at the end of this single-mode fiber offset-launch mode-conditioning patch cord at TP2. Unless specified otherwise, all transmitter measurements and tests defined in 38.6 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) connected to the receiver receptacle defined in 38.11.2. Unless specified otherwise, all receiver measurements and tests defined in 38.6 are made at TP3.

TP1 and TP4 are standardized reference points for use by implementers to certify component conformance. The electrical specifications of the PMD service interface (TP1 and TP4) are not system compliance points (these are not readily testable in a system implementation). It is expected that in many implementations, TP1 and TP4 will be common between 1000BASE-SX, 1000BASE-LX, and 1000BASE-CX (Clause 39).

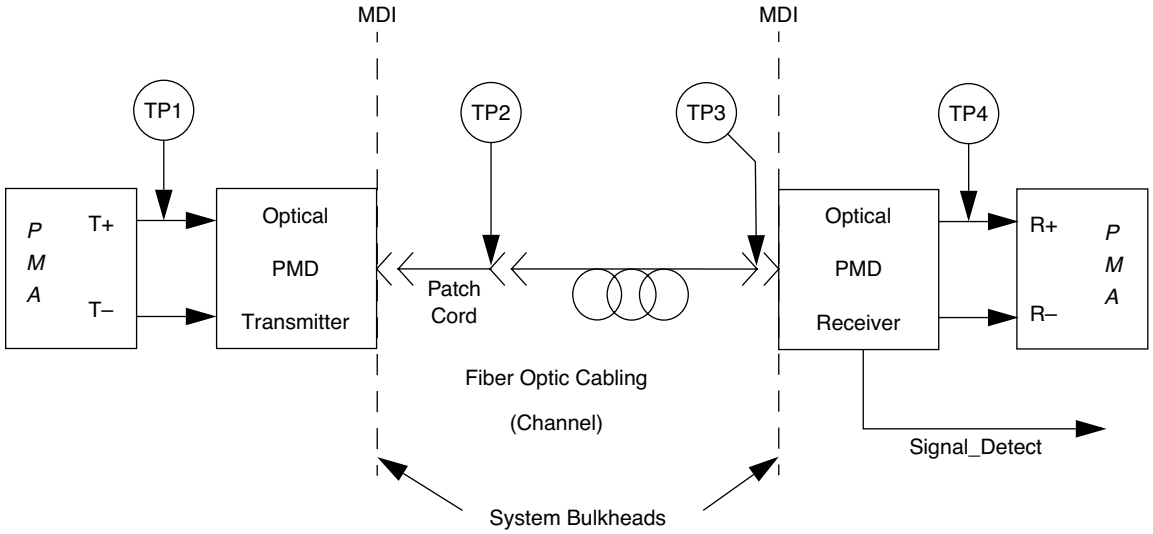


Figure 38–1—1000BASE-X block diagram

38.2.2 PMD transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according to the optical specifications in this clause. The higher optical power level shall correspond to tx_bit = ONE.

38.2.3 PMD receive function

The PMD Receive function shall convey the bits received from the MDI according to the optical specifications in this clause to the PMD service interface using the message PMD_UNITDATA.indicate(rx_bit). The higher optical power level shall correspond to rx_bit = ONE.

38.2.4 PMD signal detect function

The PMD Signal Detect function shall report to the PMD service interface, using the message PMD_SIGNAL.indicate(SIGNAL_DETECT), which is signaled continuously. PMD_SIGNAL.indicate is intended to be an indicator of optical signal presence.

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The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 38–1. The PMD receiver is not required to verify whether a compliant 1000BASE-X signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter..

Table 38–1—SIGNAL_DETECT value definition

Receive conditions	Signal detect value
Input_optical_power ≤ –30 dBm	FAIL
Input_optical_power ≥ Receive sensitivity AND compliant 1000BASE-X signal input	OK
All other conditions	Unspecified

As an unavoidable consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations must provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD due to cross talk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations which generate the SIGNAL_DETECT parameter values in response to the amplitude of the 8B/10B modulation of the optical signal and implementations that respond to the average optical power of the 8B/10B-modulated optical signal.

38.3 PMD to MDI optical specifications for 1000BASE-SX

The operating range for 1000BASE-SX is defined in Table 38–2. A 1000BASE-SX compliant transceiver supports both multimode fiber media types listed in Table 38–2 (i.e., both 50 μm and 62.5 μm multimode fiber) according to the specifications defined in 38.11. A transceiver that exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., a 50 μm solution operating at 600 m meets the minimum range requirement of 2 to 550 m).

Table 38–2—Operating range for 1000BASE-SX over each optical fiber type

Fiber type	Modal bandwidth @ 850 nm (min. overfilled launch) (MHz · km)	Minimum range (meters)
62.5 μm MMF	160	2 to 220
62.5 μm MMF	200	2 to 275
50 μm MMF	400	2 to 500
50 μm MMF	500	2 to 550
10 μm SMF	N/A	Not supported

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38.3.1 Transmitter optical specifications

The 1000BASE-SX transmitter shall meet the specifications defined in Table 38–3 per measurement techniques defined in 38.6. It shall also meet a transmit mask of the eye measurement as defined in 38.6.5.

Table 38–3—1000BASE-SX transmit characteristics

Description	62.5 μm MMF	50 μm MMF	Unit
Transmitter type	Shortwave Laser		
Signaling speed (range)	1.25 ± 100 ppm		GBd
Wavelength (λ, range)	770 to 860		nm
T_{rise}/T_{fall} (max; 20%-80%; λ > 830 nm)	0.26		ns
T_{rise}/T_{fall} (max; 20%-80%; λ ≤ 830 nm)	0.21		ns
RMS spectral width (max)	0.85		nm
Average launch power (max)	See footnote [a]		dBm
Average launch power (min)	–9.5		dBm
Average launch power of OFF transmitter (max)[b]	–30		dBm
Extinction ratio (min)	9		dB
RIN (max)	–117		dB/Hz
Coupled Power Ratio (CPR) (min)[c]	9 < CPR		dB

[a]The 1000BASE-SX launch power shall be the lesser of the class 1 safety limit as defined by 38.7.2 or the average receive power (max) defined by Table 38–4.
[b]Examples of an OFF transmitter are: no power supplied to the PMD, laser shutdown for safety conditions, activation of a "transmit disable" or other optional module laser shut down conditions. During all conditions when the PMA is powered, the ac signal (data) into the transmit port will be valid encoded 8B/10B patterns (this is a requirement of the PCS layers) except for short durations during system power-on-reset or diagnostics when the PMA is placed in a loopback mode.
[c]Radial overfilled launches as described in 38A.2, while they may meet CPR ranges, should be avoided.

The CPR specification provides sufficient mode volume so that individual multimode fiber (MMF) modes do not dominate fiber performance. This reduces the effect of peak-to-peak differential mode delay (DMD) between the launched mode groups and diminishes the resulting pulse-splitting-induced nulls in the frequency response.

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38.3.2 Receive optical specifications

The 1000BASE-SX receiver shall meet the specifications defined in Table 38–4 per measurement techniques defined in 38.6. The sampling instant is defined to occur at the eye center. The receive sensitivity includes the extinction ratio penalty.

Table 38–4—1000BASE-SX receive characteristics

Description	62.5 μm MMF	50 μm MMF	Unit
Signaling Speed (range)	1.25 ± 100 ppm		GBd
Wavelength (range)	770 to 860		nm
Average receive power (max)	0		dBm
Receive sensitivity	–17		dBm
Return loss (min)	12		dB
Stressed receive sensitivity[a, b]	–12.5	–13.5	dBm
Vertical eye-closure penalty[c]	2.60	2.20	dB
Receive electrical 3 dB upper cutoff frequency (max)	1500		MHz

[a]Measured with conformance test signal at TP3 (see 38.6.11) for BER = 10^{-12} at the eye center.
[b]Measured with a transmit signal having a 9 dB extinction ratio. If another extinction ratio is used, the stressed receive sensitivity should be corrected for the extinction ratio penalty.
[c]Vertical eye-closure penalty is a test condition for measuring stressed receive sensitivity. It is not a required characteristic of the receiver.

38.3.3 Worst-case 1000BASE-SX link power budget and penalties (informative)

The worst-case power budget and link penalties for a 1000BASE-SX channel are shown in Table 38–5.

Table 38–5—Worst-case 1000BASE-SX link power budget and penalties[a]

Parameter	62.5 μm MMF		50 μm MMF		Unit
Modal bandwidth as measured at 850 nm (minimum, overfilled launch)	160	200	400	500	MHz · km
Link power budget	7.5	7.5	7.5	7.5	dB
Operating distance	220	275	500	550	m
Channel insertion loss[b, c]	2.38	2.60	3.37	3.56	dB
Link power penalties[c]	4.27	4.29	4.07	3.57	dB
Unallocated margin in link power budget[c]	0.84	0.60	0.05	0.37	dB

[a]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.
[b]Operating distances used to calculate the channel insertion loss (see 1.4) are the maximum values specified in Table 38–2.
[c]A wavelength of 830 nm is used to calculate channel insertion loss, link power penalties, and unallocated margin.

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38.4 PMD to MDI optical specifications for 1000BASE-LX

The operating range for 1000BASE-LX is defined in Table 38–6. A 1000BASE-LX compliant transceiver supports all media types listed in Table 38–6 (i.e., 50 μm and 62.5 μm multimode fiber, and 10 μm single-mode fiber) according to the specifications defined in 38.11. A transceiver which exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., a single-mode solution operating at 5500 m meets the minimum range requirement of 2 to 5000 m).

Table 38–6—Operating range for 1000BASE-LX over each optical fiber type

Fiber type	Modal bandwidth @ 1300 nm (min. overfilled launch) (MHz · km)	Minimum range (meters)
62.5 μm MMF	500	2 to 550
50 μm MMF	400	2 to 550
50 μm MMF	500	2 to 550
10 μm SMF	N/A	2 to 5000

38.4.1 Transmitter optical specifications

The 1000BASE-LX transmitter shall meet the specifications defined in Table 38–7 per measurement techniques defined in 38.6. It shall also meet a transmit mask of the eye measurement as defined in 38.6.5. To ensure that the specifications of Table 38–7 are met with MMF links, the 1000BASE-LX transmitter output shall be coupled through a single-mode fiber offset-launch mode-conditioning patch cord, as defined in 38.11.4.

Table 38–7—1000BASE-LX transmit characteristics

Description	62.5 μm MMF	50 μm MMF	10 μm SMF	Unit
Transmitter type	Longwave Laser			
Signaling speed (range)	1.25 ± 100 ppm			GBd
Wavelength (range)	1270 to 1355			nm
T_{rise}/T_{fall} (max, 20-80% response time)	0.26			ns
RMS spectral width (max)	4			nm
Average launch power (max)	–3			dBm
Average launch power (min)	–11.5	–11.5	–11.0	dBm
Average launch power of OFF transmitter (max)	–30			dBm
Extinction ratio (min)	9			dB
RIN (max)	–120			dB/Hz
Coupled Power Ratio (CPR)[a]	28 < CPR< 40	12 < CPR < 20	N/A	dB

[a]Due to the dual media (single-mode and multimode) support of the LX transmitter, fulfillment of this specification requires a single-mode fiber offset-launch mode-conditioning patch cord described in 38.11.4 for MMF operation. This patch cord is not used for single-mode operation.

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Conditioned launch (CL) produces sufficient mode volume so that individual multimode fiber (MMF) modes do not dominate fiber performance. This reduces the effect of peak-to-peak differential mode delay (DMD) between the launched mode groups and diminishes the resulting pulse-splitting-induced nulls in the frequency response.

A CL is produced by using a single-mode fiber offset-launch mode-conditioning patch cord, inserted at both ends of a full duplex link, between the optical PMD MDI and the remainder of the link segment. The single-mode fiber offset-launch mode-conditioning patch cord contains a fiber of the same type as the cable (i.e., 62.5 μm or 50 μm fiber) connected to the optical PMD receiver input MDI and a specialized fiber/connector assembly connected to the optical PMD transmitter output.

38.4.2 Receive optical specifications

The 1000BASE-LX receiver shall meet the specifications defined in Table 38–8 per measurement techniques defined in 38.6. The sampling instant is defined to occur at the eye center. The receive sensitivity includes the extinction ratio penalty.

Table 38–8—1000BASE-LX receive characteristics

Description	Value	Unit
Signaling speed (range)	1.25 ± 100 ppm	GBd
Wavelength (range)	1270 to 1355	nm
Average receive power (max)	–3	dBm
Receive sensitivity	–19	dBm
Return loss (min)	12	dB
Stressed receive sensitivity[a, b]	–14.4	dBm
Vertical eye-closure penalty[c]	2.60	dB
Receive electrical 3 dB upper cutoff frequency (max)	1500	MHz

[a]Measured with conformance test signal at TP3 (see 38.6.11) for BER = 10^{-12} at the eye center.
[b]Measured with a transmit signal having a 9 dB extinction ratio. If another extinction ratio is used, the stressed receive sensitivity should be corrected for the extinction ratio penalty.
[c]Vertical eye-closure penalty is a test condition for measuring stressed receive sensitivity. It is not a required characteristic of the receiver.

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38.4.3 Worst-case 1000BASE-LX link power budget and penalties (informative)

The worst-case power budget and link penalties for a 1000BASE-LX channel are shown in Table 38–9.

Table 38–9—Worst-case 1000BASE-LX link power budget and penalties[a]

Parameter	62.5 μm MMF	50 μm MMF		10 μm SMF	Unit
Modal bandwidth as measured at 1300 nm (minimum, overfilled launch)	500	400	500	N/A	MHz · km
Link power budget	7.5	7.5	7.5	8.0	dB
Operating distance	550	550	550	5000	m
Channel insertion loss[b, c]	2.35	2.35	2.35	4.57	dB
Link power penalties[c]	3.48	5.08	3.96	3.27	dB
Unallocated margin in link power budget[c]	1.67	0.07	1.19	0.16	dB

[a]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.
[b]Operating distances used to calculate the channel insertion loss (see 1.4) are the maximum values specified in Table 38–6.
[c]A wavelength of 1270 nm is used to calculate channel insertion loss, link power penalties, and unallocated margin.

38.5 Jitter specifications for 1000BASE-SX and 1000BASE-LX

Numbers in the Table 38–10 represent high-frequency jitter (above 637 kHz) and do not include low-frequency jitter or wander. Implementations shall conform to the normative values highlighted **in bold** in Table 38–10 (see measurement procedure in 38.6.8). All other values are informative.

Table 38–10—1000BASE-SX and 1000BASE-LX jitter budget

Compliance point	Total jitter[a]		Deterministic jitter	
	UI	ps	UI	ps
TP1	**0.240**	**192**	0.100	80
TP1 to TP2	0.284	227	0.100	80
TP2	**0.431**	**345**	0.200	160
TP2 to TP3	0.170	136	0.050	40
TP3	**0.510**	**408**	0.250	200
TP3 to TP4	0.332	266	0.212	170
TP4[b]	**0.749**	**599**	0.462	370

[a] Total jitter is composed of both deterministic and random components. The allowed random jitter equals the allowed total jitter minus the actual deterministic jitter at that point.
[b]Measured with a conformance test signal at TP3 (see 38.6.11) set to an average optical power 0.5 dB greater than the stressed receive sensitivity from Table 38–4 for 1000BASE-SX and Table 38–8 for 1000BASE-LX.

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38.6 Optical measurement requirements

All optical measurements shall be made through a short patch cable, between 2 and 5 m in length. If a single-mode fiber offset-launch mode-conditioning patch cord is used, the optical transmit signal is defined at the output end (TP2) of the single-mode fiber offset-launch mode-conditioning patch cord.

38.6.1 Center wavelength and spectral width measurements

The center wavelength and spectral width (RMS) shall be measured using an optical spectrum analyzer per ANSI/EIA/TIA-455-127-1991 [B8]. Center wavelength and spectral width shall be measured under modulated conditions using a valid 1000BASE-X signal.

38.6.2 Optical power measurements

Optical power shall be measured using the methods specified in ANSI/EIA-455-95-1986 [B7]. This measurement may be made with the node transmitting any valid encoded 8B/10B data stream.

38.6.3 Extinction ratio measurements

Extinction ratio shall be measured using the methods specified in ANSI/TIA/EIA-526-4A-1997 [B13]. This measurement may be made with the node transmitting a data pattern defined in 36A.2. This is a repeating K28.7 data pattern. The extinction ratio is measured under fully modulated conditions with worst-case reflections.

NOTE—A repeating K28.7 data pattern generates a 125 MHz square wave.

38.6.4 Relative Intensity Noise (RIN)

RIN shall be measured according to ANSI X3.230-1994 [B20] (FC-PH), Annex A, A.5, *Relative intensity noise (RIN) measuring procedure*. Per this FC-PH annex, "This procedure describes a component test which may not be appropriate for a system level test depending on the implementation." RIN is referred to as RIN_{12} in the referenced standard. For multimode fiber measurements, the polarization rotator referenced in ANSI X3.230-1994 should be omitted, and the single-mode fiber should be replaced with a multimode fiber.

38.6.5 Transmitter optical waveform (transmit eye)

The required transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 38–2. The transmit mask is not used for response time and jitter specification.

Normalized amplitudes of 0.0 and 1.0 represent the amplitudes of logic ZERO and ONE, respectively.

The eye shall be measured with respect to the mask of the eye using a fourth-order Bessel-Thomson filter having a transfer function given by

$$H(p) = \frac{105}{105 + 105y + 45y^2 + 10y^3 + y^4}$$

where

$$y = 2.114p\,; \quad p = \frac{j\omega}{\omega_r}\,; \quad \omega_r = 2\pi f_r\,; \quad f_r = 0.9375\text{GHz}$$

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and where the filter response vs. frequency range for this fourth order Bessel-Thomson filter is defined in ITU-T G.957 , along with the allowed tolerances for its physical implementation.

NOTE 1—This Bessel-Thomson filter is not intended to represent the noise filter used within an optical receiver, but is intended to provide uniform measurement conditions at the transmitter.

NOTE 2—The fourth-order Bessel-Thomson filter is reactive. In order to suppress reflections, a 6 dB attenuator may be required at the filter input and/or output.

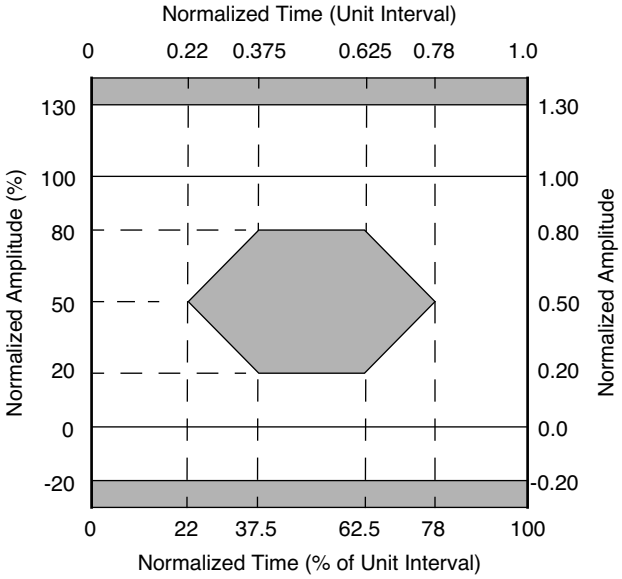


Figure 38–2—Transmitter eye mask definition

38.6.6 Transmit rise/fall characteristics

Optical response time specifications are based on unfiltered waveforms. Some lasers have overshoot and ringing on the optical waveforms which, if unfiltered, reduce the accuracy of the measured 20–80% response times. For the purpose of standardizing the measurement method, measured waveforms shall conform to the mask defined in Figure 38–2. If a filter is needed to conform to the mask, the filter response should be removed using the equation:

$$T_{rise,fall} = \sqrt{(T_{rise,fall\_measured})^2 - (T_{rise,fall\_filter})^2}$$

where the filter may be different for rise and fall. Any filter should have an impulse response equivalent to a fourth order Bessel-Thomson filter. The fourth-order Bessel-Thomson filter defined in 38.6.5 may be a convenient filter for this measurement; however, its low bandwidth adversely impacts the accuracy of the $T_{rise,fall}$ measurements.

38.6.7 Receive sensitivity measurements

The receive sensitivity shall be measured using a worst-case extinction ratio penalty while sampling at the eye center.

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The stressed receive sensitivity shall be measured using the conformance test signal at TP3, as specified in 38.6.11. After correcting for the extinction ratio of the source, the stressed receive sensitivity shall meet the conditions specified in Table 38–4 for 1000BASE-SX and in Table 38–8 for 1000BASE-LX.

38.6.8 Total jitter measurements

All total jitter measurements shall be made according to the method in ANSI X3.230-1994 [B20] (FC-PH), Annex A, A.4.2, *Active output interface eye opening measurement*. Total jitter at TP2 shall be measured utilizing a BERT (Bit Error Rate Test) test set. References to use of the Bessel-Thomson filter shall substitute use of the Bessel-Thomson filter defined in this clause (see 38.6.5). The test shall utilize the mixed frequency test pattern specified in 36A.3.

Total jitter at TP4 shall be measured using the conformance test signal at TP3, as specified in 38.6.11. The optical power shall be 0.5 dB greater than (to account for eye opening penalty) the stressed receive sensitivity level in Table 38–4 for 1000BASE-SX and in Table 38–8 for 1000BASE-LX. This power level shall be corrected if the extinction ratio differs from the specified extinction ratio (min) of 9 dB. Measurements shall be taken directly at TP4 without additional Bessel-Thomson filters.

Jitter measurement may use a clock recovery unit (commonly referred to in the industry as a “golden PLL”) to remove low-frequency jitter from the measurement as shown in Figure 38–3. The clock recovery unit has a low pass filter with 20 dB/decade rolloff with –3 dB point of 637 kHz. For this measurement, the recovered clock will run at the signaling speed. The golden PLL is used to approximate the PLL in the deserializer function of the PMA. The PMA deserializer is able to track a large amount of low-frequency jitter (such as drift or wander) below its bandwidth. This low-frequency jitter would create a large measurement penalty, but does not affect operation of the link.

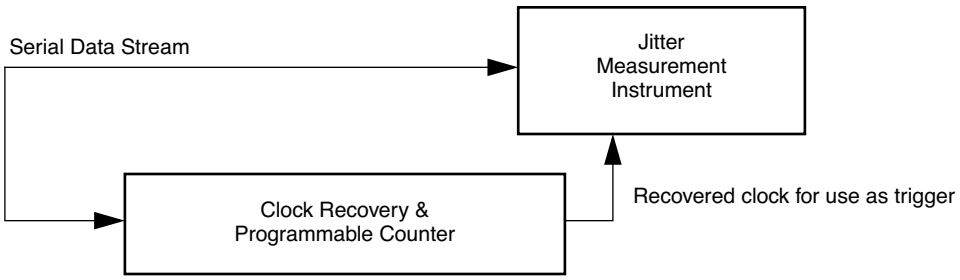


Figure 38–3—Utilization of clock recovery unit during measurement

38.6.9 Deterministic jitter measurement (informative)

Deterministic jitter should be measured according to ANSI X3.230-1994 [B20] (FC-PH), Annex A, A.4.3, *DJ Measurement*. The test utilizes the mixed frequency test pattern specified in 36A.3. This method utilizes a digital sampling scope to measure actual vs. predicted arrival of bit transitions of the 36A.3 data pattern (alternating K28.5 code-groups).

It is convenient to use the clock recovery unit described in 38.6.8 for purposes of generating a trigger for the test equipment. This recovered clock should have a frequency equivalent to 1/20th of the signaling speed.

38.6.10 Coupled Power Ratio (CPR) measurements

Coupled Power Ratio (CPR) is measured in accordance with ANSI/EIA/TIA-526-14A [B14]. Measured CPR values are time averaged to eliminate variation from speckle fluctuations. The coupled power ratio shall be measured for compliance with Table 38–3 and Table 38–7.

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38.6.11 Conformance test signal at TP3 for receiver testing

Receivers being tested for conformance to the stressed receive sensitivity requirements of 38.6.7 and the total jitter requirements of 38.6.8 shall be tested using a conformance test signal at TP3 conforming to the requirements described in Figure 38–4. The conformance test signal shall be generated using the short continuous random test pattern defined in 36A.5. The conformance test signal is conditioned by applying deterministic jitter (DJ) and intersymbol interference (ISI). The conditioned conformance test signal is shown schematically in Figure 38–4. The horizontal eye closure (reduction of pulse width) caused by the duty cycle distortion (DCD) component of DJ shall be no less than 65 ps. The vertical eye-closure penalty shall be greater than or equal to the value specified in Table 38–4 for 1000BASE-SX and Table 38–8 for 1000BASE-LX. The DJ cannot be added with a simple phase modulation, which does not account for the DCD component of DJ.

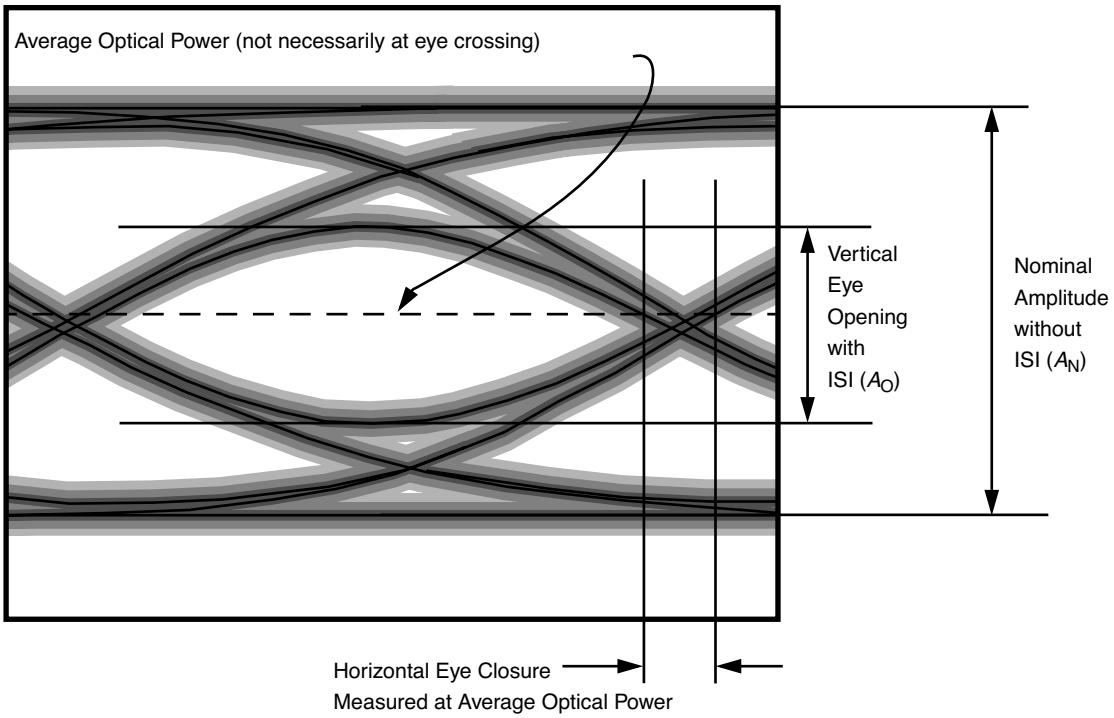


Figure 38–4—Required characteristics of the conformance test signal at TP3

The vertical eye-closure penalty is given by

$$\text{Vertical eye-closure penalty [dB]} = 10 \cdot \log \frac{A_O}{A_N}$$

where A_O is the amplitude of the eye opening, and A_N is the normal amplitude without ISI, as measured in Figure 38–4.

Figure 38–5 shows the recommended test set up for producing the conformance test signal at TP3. The coaxial cable is adjusted in length to produce the correct DCD component of DJ. Since the coaxial cable can produce the incorrect ISI, a limiting amplifier is used to restore fast rise and fall times. A Bessel-Thomson filter is selected to produce the minimum ISI induced eye closure as specified per Table 38–4 for 1000BASE-SX and Table 38–8 for 1000BASE-LX. This conditioned signal is used to drive a high bandwidth linearly modulated laser source.

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The vertical and horizontal eye closures to be used for receiver conformance testing are verified using a fast photodetector and amplifier. The bandwidth of the photodetector shall be at least 2.5 GHz and be coupled through a 1.875 GHz fourth-order Bessel-Thomson filter to the oscilloscope input. Special care should be taken to ensure that all the light from the fiber is collected by the fast photodetector and that there is negligible mode selective loss, especially in the optical attenuator.

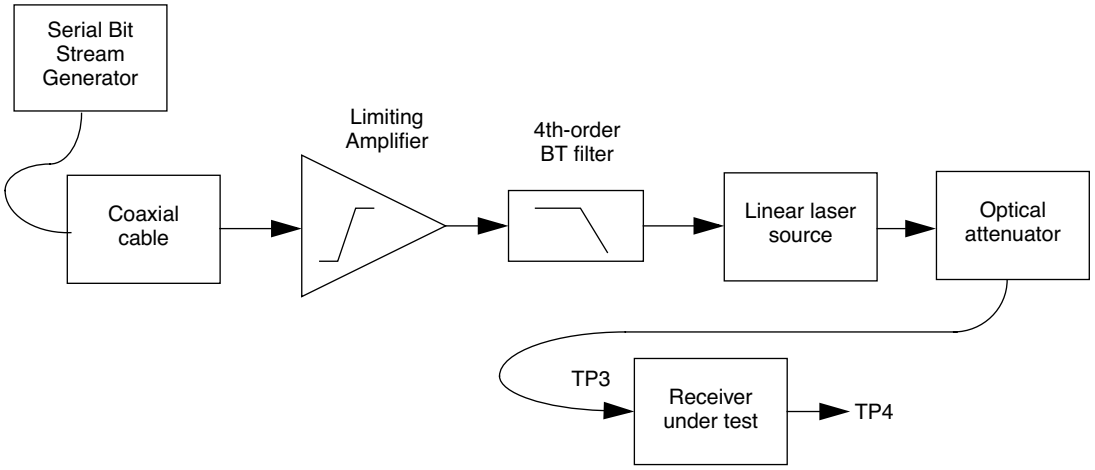


Figure 38–5—Apparatus for generating receiver conformance test signal at TP3

38.6.12 Measurement of the receiver 3 dB electrical upper cutoff frequency

The receiver 3 dB electrical upper cutoff frequency shall be measured as described below. The test setup is shown in Figure 38–6. The test is performed with a laser that is suitable for analog signal transmission. The laser is modulated by a digital data signal. In addition to the digital modulation, the laser is modulated with an analog signal. The analog and digital signals should be asynchronous. The data pattern to be used for this test is the short continuous random test pattern defined in 36A.5. The frequency response of the laser must be sufficient to allow it to respond to both the digital modulation and the analog modulation. The laser should be biased so that it remains linear when driven by the combined signals.

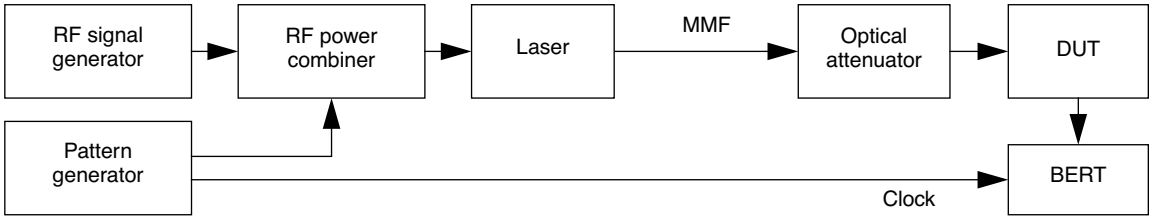


Figure 38–6—Test setup for receiver bandwidth measurement

The 3 dB upper cutoff frequency is measured using the following steps a) through e):

a) Calibrate the frequency response characteristics of the test equipment including the analog radio frequency (RF) signal generator, RF power combiner, and laser source. Measure the laser's extinction ratio according to 38.6.3. With the exception of extinction ratio, the optical source shall meet the requirements of Clause 38.
b) Configure the test equipment as shown in Figure 38–6. Take care to minimize changes to the signal path that could affect the system frequency response after the calibration in step a. Connect the laser

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output with no RF modulation applied to the receiver under test through an optical attenuator and taking into account the extinction ratio of the source, set the optical power to a level that approximates the stressed receive sensitivity level in Table 38–4 for 1000BASE-SX and in Table 38–8 for 1000BASE-LX.

c) Locate the center of the eye with the BERT. Turn on the RF modulation while maintaining the same average optical power established in step b.

d) Measure the necessary RF modulation amplitude (in dBm) required to achieve a constant BER (e.g., 10^{-8}) for a number of frequencies.

e) The receiver 3 dB electrical upper cutoff frequency is that frequency where the corrected RF modulation amplitude (the measured amplitude in "d" corrected with the calibration data in "a") increases by 3 dB (electrical). If necessary, interpolate between the measured response values.

38.7 Environmental specifications

38.7.1 General safety

All equipment meeting this standard shall conform to IEC-60950: 1991.

38.7.2 Laser safety

1000BASE-X optical transceivers shall be Class 1 laser certified under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore. Transceivers shall be certified to be in conformance with IEC 60825-1.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance and service. This documentation shall explicitly define requirements and usage restrictions on the host system necessary to meet these safety certifications.[5]

38.7.3 Installation

Sound installation practice, as defined by applicable local codes and regulations, shall be followed in every instance in which such practice is applicable.

38.8 Environment

Normative specifications in this clause shall be met by a system integrating a 1000BASE-X PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

[5]A host system that fails to meet the manufacturers requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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38.8.1 Electromagnetic emission

A system integrating a 1000BASE-X PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

38.8.2 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

38.9 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters, according to the PMD-MDI type.

PMD MDI type 1000BASE-SX:

a) 1000BASE-SX
b) Applicable safety warnings

PMD MDI type 1000BASE-LX:

a) 1000BASE-LX
b) Applicable safety warnings

Labeling requirements for Class 1 lasers are given in the laser safety standards referenced in 38.7.2.

38.10 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 38–7.

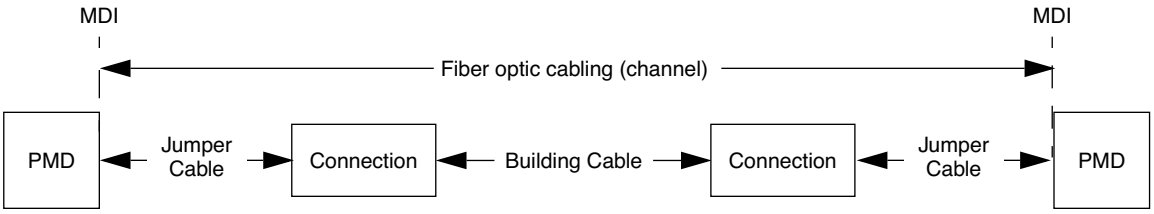


Figure 38–7—Fiber optic cabling model

The channel insertion loss is given in Table 38–11. Insertion loss measurements of installed fiber cables are made in accordance with ANSI/TIA/EIA-526-14A [B14], method B; and ANSI/TIA/EIA-526-7 [B15], method A-1. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

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Table 38–11—Channel insertion loss

Description	62.5 μm MMF			50 μm MMF			10 μm SMF	Unit
Wavelength	850	850	1300	850	850	1300	1310	nm
Modal bandwidth (min; overfilled launch)	160	200	500	400	500	400 or 500	N/A	MHz · km
Operating distance	220	275	550	500	550	550	5000	m
Channel insertion loss[a] [b]	2.33	2.53	2.32	3.25	3.43	2.32	4.5	dB

[a]These channel insertion loss numbers are based on the nominal operating wavelength.
[b]Operating distances used to calculate channel insertion loss are those listed in this table.

38.11 Characteristics of the fiber optic cabling

The 1000BASE-SX and 1000BASE-LX fiber optic cabling shall meet the specifications defined in Table 38–12. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together. It also includes a connector plug at each end to connect to the MDI. The fiber optic cabling spans from one MDI to another MDI, as shown in Figure 38–7.

38.11.1 Optical fiber and cable

The fiber optic cable requirements are satisfied by the fibers specified in IEC 60793-2:1992. Types A1a (50/125 μm multimode), A1b (62.5/125 μm multimode), and B1 (10/125 μm single-mode) with the exceptions noted in Table 38–12.

Table 38–12—Optical fiber and cable characteristics

Description	62.5 μm MMF		50 μm MMF		10 μm SMF	Unit
Nominal fiber specification wavelength	**850**	**1300**	**850**	**1300**	**1310**	**nm**
Fiber cable attenuation (max)	3.75[a]	1.5	3.5	1.5	0.5	dB/km
Modal Bandwidth (min; overfilled launch)	160	500	400	400	N/A	MHz · km
	200	500	500	500	N/A	MHz · km
Zero dispersion wavelength (λ_0)	$1320 \le \lambda_0 \le 1365$		$1295 \le \lambda_0 \le 1320$		$1300 \le \lambda_0 \le 1324$	nm
Dispersion slope (max) (S_0)	0.11 for $1320 \le \lambda_0 \le 1348$ and $0.001(1458 - \lambda_0)$ for $1348 \le \lambda_0 \le 1365$		0.11 for $1300 \le \lambda_0 \le 1320$ and $0.001(\lambda_0 - 1190)$ for $1295 \le \lambda_0 \le 1300$		0.093	ps / nm^2 · km

[a]This value of attenuation is a relaxation of the standard (IEC 60793-2, type A1b, category less than or equal to 3.5 dB/km).

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38.11.2 Optical fiber connection

An optical fiber connection as shown in Figure 38–7 consists of a mated pair of optical connectors. The 1000BASE-SX or 1000BASE-LX PMD is coupled to the fiber optic cabling through a connector plug into the MDI optical receptacle, as shown in 38.11.3.

38.11.2.1 Connection insertion loss

The insertion loss is specified for a connection, which consists of a mated pair of optical connectors.

The maximum link distances for multimode fiber are calculated based on an allocation of 1.5 dB total connection and splice loss. For example, this allocation supports three connections with an average insertion loss equal to 0.5 dB (or less) per connection, or two connections (as shown in Figure 38–7) with a maximum insertion loss of 0.75 dB. Connections with different loss characteristics may be used provided the requirements of Table 38–11 and Table 38–12 are met.

The maximum link distances for single-mode fiber are calculated based on an allocation of 2.0 dB total connection and splice loss. For example, this allocation supports four connections with an average insertion loss per connection of 0.5 dB. Connections with different loss characteristics may be used provided the requirements of Table 38–11 and Table 38–12 are met.

38.11.2.2 Connection return loss

The return loss for multimode connections shall be greater than 20 dB.

The return loss for single-mode connections shall be greater than 26 dB.

38.11.3 Medium Dependent Interface (MDI)

The 1000BASE-SX and 1000BASE-LX PMD is coupled to the fiber optic cabling through a connector plug into the MDI optical receptacle. The 1000BASE-SX and 1000BASE-LX MDI optical receptacles shall be the duplex SC, meeting the following requirements:

a) Meet the dimension and interface specifications of IEC 61754-4 [B25] and IEC 61754-4, Interface 4-2.
b) Meet the performance specifications as specified in ISO/IEC 11801.
c) Ensure that polarity is maintained.
d) The receive side of the receptacle is located on the left when viewed looking into the transceiver optical ports with the keys on the bottom surface.

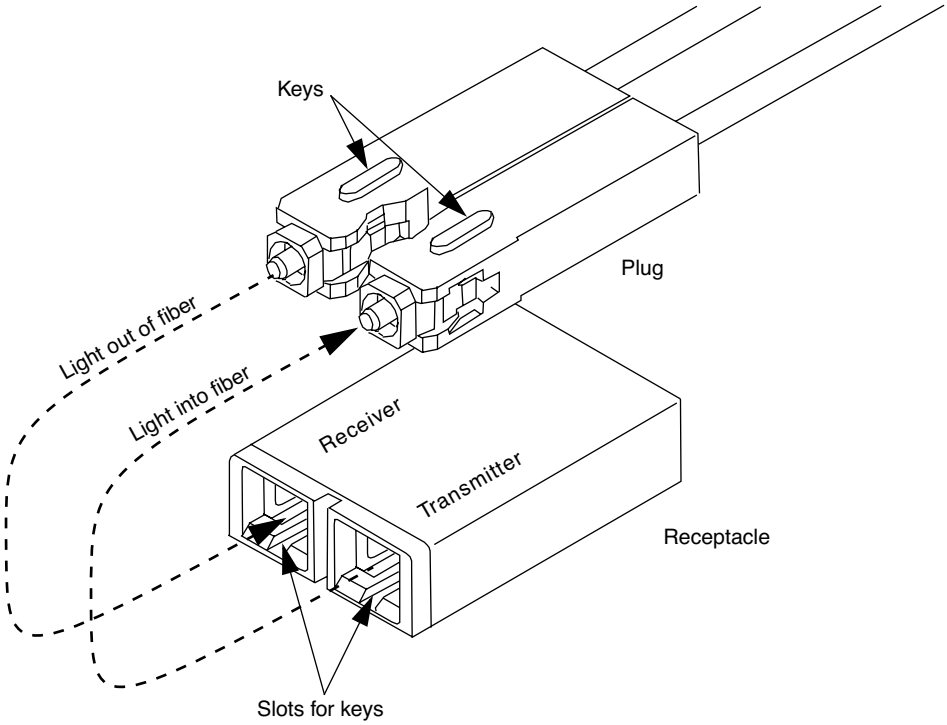
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A sample drawing of a duplex SC connector and receptacle is provided in Figure 38–8.



NOTE—Connector keys are used for transmit/receive polarity only. The connector keys do not differentiate between single-mode and multimode connectors.

Figure 38–8—Duplex SC connector and receptacle (informative)

38.11.4 single-mode fiber offset-launch mode-conditioning patch cord for MMF operation of 1000BASE-LX

This subclause specifies an example embodiment of a mode conditioner for 1000BASE-LX operation with MMF cabling. The MMF cabling should meet all of the specifications of 38.10. For 1000BASE-LX the mode conditioner consists of a single-mode fiber permanently coupled off-center to a graded index fiber. This example embodiment of a patch cord is not intended to exclude other physical implementations of offset-launch mode conditioners. However, any implementation of an offset-launch mode conditioner used for 1000BASE-LX shall meet the specifications of Table 38–13. The offset launch must be contained within the patch cord assembly and is not adjustable by the user.

Table 38–13—single-mode fiber offset-launch mode conditioner specifications

Description	62.5 μm MMF	50 μm MMF	Unit
Maximum insertion loss	0.5	0.5	dB
Coupled Power Ratio (CPR)	28 < CPR < 40	12 < CPR < 20	dB
Optical center offset between SMF and MMF	17 < Offset < 23	10 < Offset < 16	μm
Maximum angular offset	1	1	degree

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All patch cord connecting ferrules containing the single-mode-to-multimode offset launch shall have single-mode tolerances (IEC 61754-4 [B25] grade 1 ferrule).

The single-mode fiber used in the construction of the single-mode fiber offset-launch mode conditioner shall meet the requirements of 38.11.1. The multimode fiber used in the construction of the single-mode fiber offset-launch mode conditioner shall be of the same type as the cabling over which the 1000BASE-LX link is to be operated. If the cabling is 62.5 μm MMF then the MMF used in the construction of the mode conditioner should be of type 62.5 μm MMF. If the cabling is 50 μm MMF, then the MMF used in the construction of the mode conditioner should be of type 50 μm MMF.

Figure 38–9 shows the preferred embodiment of the single-mode fiber offset-launch mode-conditioning patch cord. This patch cord consists of duplex fibers including a single-mode-to-multimode offset launch fiber connected to the transmitter MDI and a second conventional graded index MMF connected to the receiver MDI. The preferred configuration is a plug-to-plug patch cord since it maximizes the power budget margin of the 1000BASE-LX link. The single-mode end of the patch cord shall be labeled “To Equipment.” The multimode end of the patch cord shall be labeled “To Cable.” The color identifier of the single-mode fiber connector shall be blue. The color identifier of all multimode fiber connector plugs shall be beige. The patch cord assembly is labeled “Offset-launch mode-conditioning patch cord assembly.” Labelling identifies which size multimode fiber is used in the construction of the patch cord. The keying of the SC duplex optical plug ensures that the single-mode fiber end is automatically aligned to the transmitter MDI.

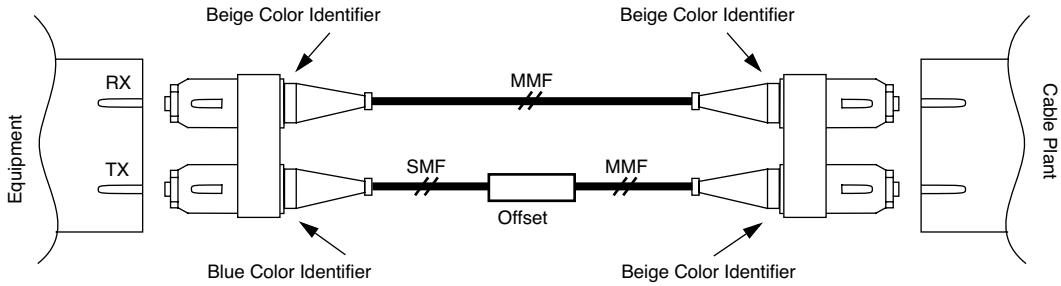


Figure 38–9—1000BASE-LX single-mode fiber offset-launch mode-conditioning patch cord assembly

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38.12 Protocol Implementation Conformance Statement (PICS) proforma for Clause 38, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-LX (Long Wavelength Laser) and 1000BASE-SX (Short Wavelength Laser)[6]

38.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 38, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-LX (Long Wavelength Laser) and 1000BASE-SX (Short Wavelength Laser), shall complete the following Protocol Implementation Conformance Statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

38.12.2 Identification

38.12.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

38.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2002, Clause 38, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-LX (Long Wavelength Laser) and 1000BASE-SX (Short Wavelength Laser)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

[6]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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38.12.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*LX	1000BASE-LX PMD	38.1	Device supports long wavelength operation (1270–1355 nm).	O/1	Yes [ ] No [ ]
*SX	1000BASE-SX PMD	38.1	Device supports short wavelength operation (770–860 nm). Either this option, or option LX, must be checked.	O/1	Yes [ ] No [ ]
*INS	Installation / cable	38.10	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer.	O	Yes [ ] No [ ]
*OFP	Single-mode offset-launch mode-conditioning patch cord	38.11.4	Items marked with OFP include installation practices and cable specifications not applicable to a PHY manufacturer.	O	Yes [ ] No [ ]
*TP1	Standardized reference point TP1 exposed and available for testing.	38.2.1	This point may be made available for use by implementors to certify component conformance.	O	Yes [ ] No [ ]
*TP4	Standardized reference point TP4 exposed and available for testing.	38.2.1	This point may be made available for use by implementors to certify component conformance.	O	Yes [ ] No [ ]

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38.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-LX (Long Wavelength Laser) and 1000BASE-SX (Short Wavelength Laser)

38.12.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FN1	Integration with 1000BASE-X PCS and PMA and management functions	38.1		M	Yes [ ]
FN2	Transmit function	38.2.2	Convey bits requested by PMD_UNITDATA.request() to the MDI	M	Yes [ ]
FN3	Mapping between optical signal and logical signal for transmitter	38.2.2	Higher optical power is a logical 1.	M	Yes [ ]
FN4	Receive function	38.2.3	Convey bits received from the MDI to PMD_UNITDATA.indicate()	M	Yes [ ]
FN5	Mapping between optical signal and logical signal for receiver	38.2.3	Higher optical power is a logical 1.	M	Yes [ ]
FN6	Signal detect function	38.2.4	Report to the PMD service interface the message PMD_SIGNAL.indicate(SIGNAL_DETECT)	M	Yes [ ]
FN7	Signal detect behavior	38.2.4	Meets requirements of Table 38–1	M	Yes [ ]

38.12.4.2 PMD to MDI optical specifications for 1000BASE-SX

Item	Feature	Subclause	Value/Comment	Status	Support
PMS1	Transmitter meets specifications in Table 38–3	38.3.1	Per measurement techniques in 38.6	SX:M	Yes [ ] N/A [ ]
PMS2	Transmitter eye measurement	38.3.1	Per 38.6.5	SX:M	Yes [ ] N/A [ ]
PMS3	Launch power	38.3.1	Lesser of class 1 safety limit per 38.7.2 or maximum receive power in Table 38–4	SX:M	Yes [ ] N/A [ ]
PMS4	Receiver meets specifications in Table 38–4	38.3.2	Per measurement techniques in 38.6	SX:M	Yes [ ] N/A [ ]

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38.12.4.3 PMD to MDI optical specifications for 1000BASE-LX

Item	Feature	Subclause	Value/Comment	Status	Support
PML1	Transmitter meets specifications in Table 38–7	38.4.1	Per measurement techniques in 38.6	LX:M	Yes [ ] N/A [ ]
PML2	Transmitter eye measurement	38.4.1	Per 38.6.5	LX:M	Yes [ ] N/A [ ]
PML3	Offset-launch mode-conditioning patch cord	38.4.1	Required for LX multimode operation	LX:M	Yes [ ] N/A [ ]
PML4	Receiver meets specifications in Table 38–8	38.4.2	Per measurement techniques in 38.6	LX:M	Yes [ ] N/A [ ]

38.12.4.4 Jitter specifications

Item	Feature	Subclause	Value/Comment	Status	Support
JT1	Total jitter specification at TP1	38.5	Meets specification of bold entries in Table 38–10	TP1:M	Yes [ ] N/A [ ]
JT2	Total jitter specification at TP2	38.5	Meets specification of bold entries in Table 38–10	M	Yes [ ]
JT3	Total jitter specification at TP3	38.5	Meets specification of bold entries in Table 38–10	INS:M	Yes [ ] N/A [ ]
JT4	Total jitter specification at TP4	38.5	Meets specification of bold entries in Table 38–10	TP4:M	Yes [ ] N/A [ ]

38.12.4.5 Optical measurement requirements

Item	Feature	Subclause	Value/Comment	Status	Support
OR1	Length of patch cord used for measurements	38.6	2 to 5 m	M	Yes [ ]
OR2	Center wavelength and spectral width measurement conditions	38.6.1	Using optical spectrum analyzer per ANSI/EIA/TIA-455-127-1991 [B8]	M	Yes [ ]
OR3	Center wavelength and spectral width measurement conditions	38.6.1	Under modulated conditions using a valid 1000BASE-X signal	M	Yes [ ]
OR4	Optical power measurement conditions	38.6.2	Per ANSI/EIA-455-95-1986 [B7]	M	Yes [ ]
OR5	Extinction ratio measurement conditions	38.6.3	Per ANSI/TIA/EIA-526-4A-1997 [B13] using patch cable per 38.6	M	Yes [ ]
OR6	RIN test methods	38.6.4	ANSI X3.230-1994 [B20] (FC-PH), Annex A, A.5 using patch cable per 38.6	M	Yes [ ]

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38.12.4.5 Optical measurement requirements *(continued)*

Item	Feature	Subclause	Value/Comment	Status	Support
OR7	Transmit eye mask measurement conditions	38.6.5	Using fourth-order Bessel-Thomson filter per 38.6.5, using patch cable per 38.6	M	Yes [ ]
OR8	Transmit rise/fall measurement conditions	38.6.6	Waveforms conform to mask in Figure 38–2, measure from 20% to 80%, using patch cable per 38.6	M	Yes [ ]
OR9	Receive sensitivity measurement conditions	38.6.7	Worst-case extinction ratio penalty while sampling at the eye center using patch cable per 38.6	M	Yes [ ]
OR10	Stressed receive sensitivity	38.6.7	Per 38.6.11, using patch cable per 38.6	M	Yes [ ]
OR11	Stressed receive sensitivity	38.6.7	Meet Table 38–4	SX:M	Yes [ ] N/A [ ]
OR12	Stressed receive sensitivity	38.6.7	Meet Table 38–8	LX:M	Yes [ ] N/A [ ]
OR13	Total jitter measurement conditions	38.6.8	ANSI X3.230-1994 [B20] (FC-PH), Annex A, Subclause A.4.2	M	Yes [ ]
OR14	Total jitter measurement conditions at TP2	38.6.8	Using BERT	M	Yes [ ]
OR15	Total jitter measurement conditions at TP2	38.6.8	Using Bessel-Thomson filter defined in 38.6.5	M	Yes [ ]
OR16	Total jitter measurement conditions	38.6.8	Using mixed frequency pattern specified in 36A.3	M	Yes [ ]
OR17	Total jitter measurement conditions at TP4	38.6.8	Using conformance test signal at TP3 (see 38.6.11)	M	Yes [ ]
OR18	Optical power used for total jitter measurement at TP4	38.6.8	0.5 dB greater than stressed receive sensitivity given in Table 38–4 (for SX) or (for LX)	M	Yes [ ]
OR19	Optical power used for total jitter measurement at TP4	38.6.8	Corrected for extinction ratio	M	Yes [ ]
OR20	Total jitter measurement conditions at TP4	38.6.8	Measured without Bessel-Thomson filters	M	Yes [ ]
OR21	Coupled power ratio	38.6.10	Measured using TIA/EIA-526-14A [B14], meets values in Table 38–3 (for SX) or (for LX)	M	Yes [ ]
OR22	Compliance test signal at TP3	38.6.11	Meets requirements of Figure 38–4	M	Yes [ ]
OR23	Compliance test signal at TP3	38.6.11	Pattern specified in 36A.5	M	Yes [ ]
OR24	Compliance test signal at TP3	38.6.11	DJ eye closure no less than 65 ps	M	Yes [ ]

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38.12.4.5 Optical measurement requirements *(continued)*

Item	Feature	Subclause	Value/Comment	Status	Support
OR25	Compliance test signal at TP3	38.6.11	Vertical eye-closure penalty meets requirements of Table 38–4	SX:M	Yes [ ] N/A [ ]
OR26	Compliance test signal at TP3	38.6.11	Vertical eye-closure penalty meets requirements of Table 38–8	LX:M	Yes [ ] N/A [ ]
OR27	Compliance test signal at TP3	38.6.11	Bandwidth of photodetector >2.5 GHz, and couple through 4th order Bessel-Thomson filter	M	Yes [ ]
OR28	Receiver electrical cutoff frequency measurement procedure	38.6.12	As described in 38.6.12	M	Yes [ ]
OR29	Optical source used for cutoff frequency measurement	38.6.12	With the exception of extinction ratio, meets requirements of Clause 38	M	Yes [ ]
OR30	Compliance with IEC 60950-1991	38.7.1		M	Yes [ ]
OR31	Laser safety compliance	38.7.2	Class 1	M	Yes [ ]
OR32	Laser safety compliance test conditions	38.7.2	IEC 60825-1	M	Yes [ ]
OR33	Documentation explicitly defines requirements and usage restrictions on the host system necessary to meet after certifications	38.7.2		M	Yes [ ]
OR34	Sound installation practices	38.7.3		INS:M	Yes [ ] N/A [ ]
OR35	Compliance with all requirements over the life of the product	38.8		M	Yes [ ]
OR36	Compliance with applicable local and national codes for the limitation of electromagnetic interference	38.8.1		M	Yes [ ]

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38.12.4.6 Characteristics of the fiber optic cabling

Item	Feature	Subclause	Value/Comment	Status	Support
LI1	Fiber optic cabling	38.11	Meets specifications in Table 38–11	INS:M	Yes [ ] N/A [ ]
LI2	Return loss for multimode connections	38.11.2.2	> 20 dB	INS:M	Yes [ ] N/A [ ]
LI3	Return loss for single-mode connections	38.11.2.2	> 26 dB	INS:M	Yes [ ] N/A [ ]
LI4	MDI optical plug	38.11.3	Duplex SC meeting IEC 61754-4, IEC 61754-4: 1997 [B25] Interface 4-2, and ISO/IEC 11801, maintains polarity and ensures orientation.	INS:M	Yes [ ]
LI5	MDI optical receptacle	38.11.3	Duplex SC meeting IEC 61754-4: 1997 [B25] Interface 4-2, and ISO/IEC 11801, maintains polarity and ensures orientation.	M	Yes [ ]
LI6	Offset-launch mode-conditioning patch cord	38.11.4	Meet conditions of Table 38–13	OFP:M	Yes [ ] N/A [ ]
LI7	Single-mode ferrules in offset-launch mode-conditioning patch cords	38.11.4	IEC 61754-4: 1997 [B25] grade 1 ferrule	OFP:M	Yes [ ] N/A [ ]
LI8	Single-mode fiber in offset-launch mode-conditioning patch cords	38.11.4	Per 38.11.1	OFP:M	Yes [ ] N/A [ ]
LI9	Multimode fiber in offset-launch mode-conditioning patch cords	38.11.4	Same type as used in LX cable plant	OFP:M	Yes [ ] N/A [ ]
LI10	Label on single-mode end of offset-launch mode-conditioning patch cords	38.11.4	Labeled “To Equipment”	OFP:M	Yes [ ] N/A [ ]
LI11	Label on multimode end of offset-launch mode-conditioning patch cords	38.11.4	Labeled “To Cable”	OFP:M	Yes [ ] N/A [ ]
LI12	Color identifier of single-mode fiber connector	38.11.4	Blue	OFP:M	Yes [ ] N/A [ ]
LI13	Color identifier of multimode fiber connector	38.11.4	Beige	OFP:M	Yes [ ] N/A [ ]

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39. Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-CX (short-haul copper)

39.1 Overview

This clause specifies the 1000BASE-CX PMD (including MDI) and baseband medium for short-haul copper. In order to form a complete 1000BASE-CX Physical Layer it shall be integrated with the 1000BASE-X PCS of Clause 36 and the PMD of Clause 38, which are hereby incorporated by reference. As such, the 1000BASE-CX PMD shall comply with the PMD service interface specified in 38.1.1.

1000BASE-CX has a minimum operating range of 0.1 to 25 m. Jumper cables, described in 39.4, are used to interconnect 1000BASE-CX PMDs. These cables shall not be concatenated to achieve longer distances. A 1000BASE-CX jumper cable assembly consists of a continuous shielded balanced cable terminated at each end with a polarized shielded plug described in 39.5.1. The jumper cable assembly provides an output signal on contacts R+/R– meeting the requirements shown in Figure 39–5 when a transmit signal compliant with Figures 39–3 and 39–4 is connected to the T+/T– contacts at the near-end MDI connector.

The links described in this clause are applied only to homogenous ground applications such as between devices within a cabinet or rack, or between cabinets interconnected by a common ground return or ground plane. This restriction minimizes safety and interference concerns caused by any voltage differences that could otherwise exist between equipment grounds.

39.2 Functional specifications

The 1000BASE-CX PMD performs three functions, Transmit, Receive, and Signal Status according to the service interface definition in 38.1.

39.2.1 PMD transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according electrical specifications in 39.3.1. The higher output voltage of T+ minus T– (differential voltage) shall correspond to tx_bit = ONE.

39.2.2 PMD receive function

The PMD Receive function shall convey the bits received at the MDI in accordance with the electrical specifications of 39.3.2 to the PMD service interface using the message PMD_UNITDATA.indicate(rx_bit). The higher output voltage of R+ minus R– (differential voltage) shall correspond to rx_bit = ONE.

39.2.3 PMD signal detect function

The PMD Signal Detect function shall report to the PMD service interface, using the message PMD_SIGNAL.indicate(SIGNAL_DETECT), which is signaled continuously. PMD_SIGNAL.indicate is intended to be an indicator of electrical signal presence.

The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 39–1. The PMD receiver is not required to verify whether a compliant 1000BASE-X signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

As an unavoidable consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations must provide adequate margin between the input signal level at which the

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Table 39–1—SIGNAL_DETECT value definition

Receive Conditions	Signal Detect Value
V_{input}, Receiver < (receiver sensitivity + worst-case local system noise)[a]	FAIL
Minimum differential sensitivity ≤ $V_{input,}$ Receiver ≤ Maximum differential input AND compliant 1000BASE-X signal input	OK
All other conditions	Unspecified

[a]Worst-case local system noise includes all receiver coupled noise sources (NEXT, power supply noise, and any reflected signals). Receive sensitivity is the actual sensitivity of the specific port (as opposed to the minimum differential sensitivity).

SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD due to cross talk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations which generate the SIGNAL_DETECT parameter values in response to the amplitude of the 8B/10B modulation of the electrical signal

39.3 PMD to MDI electrical specifications

All interface specifications are valid only at the point of entry and exit from the equipment. These points are identified as points TP2 and TP3 as shown in Figure 39–1. The specifications assume that all measurements are made after a mated connector pair, relative to the source or destination.

TP1 and TP4 are standardized reference points for use by implementers to certify component conformance. The electrical specifications of the PMD service interface (TP1 and TP4) are not system compliance points (these are not readily testable in a system implementation). It is expected that in many implementations TP1 and TP4 will be common between 1000BASE-SX (Clause 38), 1000BASE-LX (Clause 38), and 1000BASE-CX.

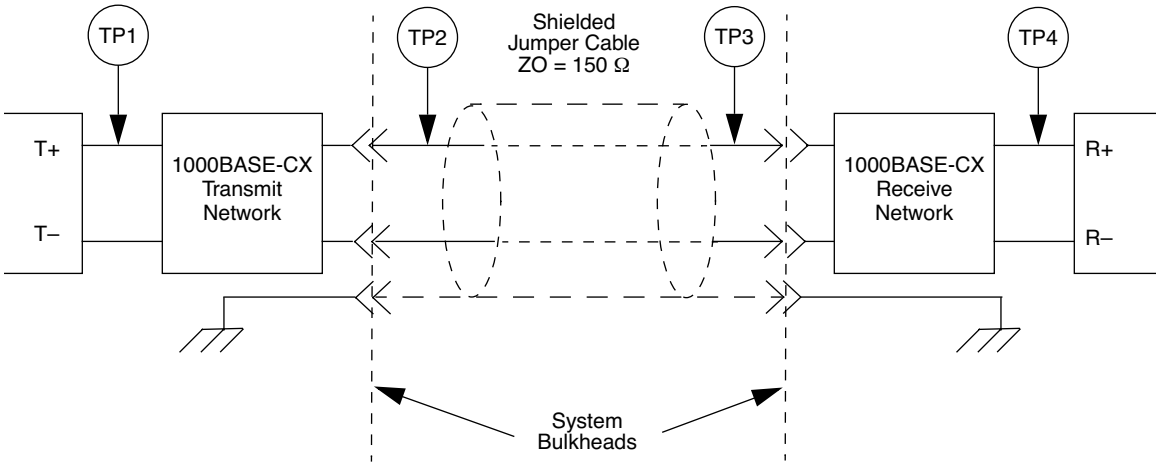
PMD specifications shall be measured using the measurement techniques defined in 39.6.

The reference points for all connections are those points TP2 and TP3 where the cabinet Faraday shield transitions between the cabinet and the jumper cable shield. If sections of transmission line exist within the Faraday shield, they are considered to be part of the associated transmit or receive network, and not part of the jumper cable assembly.

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NOTE—Jumper cable assembly shielding is attached to the system chassis via the connector shroud.

Figure 39–1—1000BASE-CX link (half link is shown)

Schematics in the diagrams in this clause are for illustration only and do not represent the only feasible implementation.

39.3.1 Transmitter electrical specifications

The output driver is assumed to have output levels approximating those of Emitter Coupled Logic (ECL), as measured at TP1. The transmitter shall meet the specifications in Table 39–2.

Table 39–2—Transmitter characteristics at TP2

Description	Value	Unit
Type	(P)ECL	
Data rate	1000	Mb/s
Clock tolerance	±100	ppm
Nominal signalling speed	1250	MBd
Differential amplitude (p-p)		
Max (worst case p-p)	2000	mV
Min (opening)	1100	mV
Max (OFF)[a]	170	mV
Rise/Fall time (20-80%)		
maximum	327	ps
minimum	85	ps
Differential skew (max)	25	ps

[a]Examples of an OFF transmitter are no power supplied to the PMD and PMA transmit output being driven to a static state during loopback.

For all links, the output driver shall be ac-coupled to the jumper cable assembly through a transmission network, and have output levels, measured at the input to the jumper cable assembly (TP2), meeting the eye diagram requirements of Figure 39–3 and Figure 39–4, when terminated as shown in Figure 39–2. The symbols X1 and X2 in Figure 39–3 and Figure 39–4 are defined in Table 39–3.

The normalized amplitude limits in Figure 39–3 are set to allow signal overshoot of 10% and undershoot of 20%, relative to the amplitudes determined to be a logic 1 and 0. The absolute transmitter output timing and

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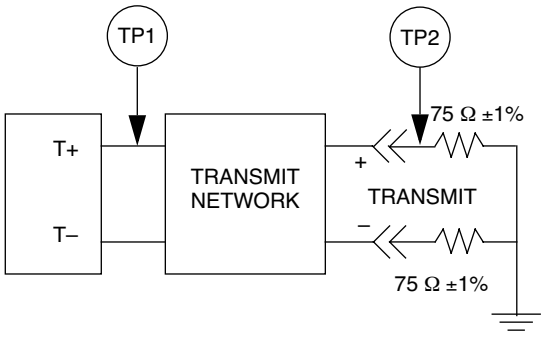


Figure 39–2—Balanced transmitter test load

amplitude requirements are specified in Table 39–2, Table 39–3, and Figure 39–4. The normalized transmitter output timing and amplitude requirements are specified in Table 39–2, Table 39–3, and Figure 39–3. The transmit masks of Figure 39–3 and Figure 39–4 are not used for response time and jitter specifications.

NOTE 1—The relationship between Figure 39–3 and Figure 39–4 can best be explained by a counter example. If a transmitter outputs a nominal 600 mV-ppd logic one level with overshoot to 900 mV-ppd, it will pass the absolute mask of Figure 39–4 but will not pass the normalized mask of Figure 39–3. Normalized, this signal would have 50% overshoot. This exceeds the 10% overshoot limit defined by the normalized eye mask.

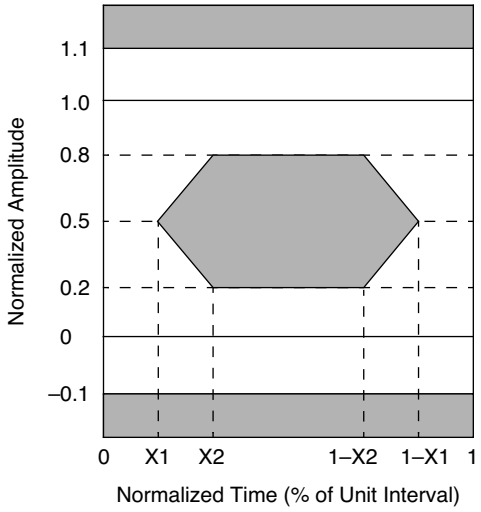


Figure 39–3—Normalized eye diagram mask at TP2

Table 39–3—Normalized time intervals for TP2

Symbol	Value	Units
X1	0.14	Unit Intervals (UI)
X2	0.34	Unit Intervals (UI)

The recommended interface to electrical transmission media is via transformer or capacitive coupling.

NOTE 2—All specifications, unless specifically listed otherwise, are based on differential measurements.

NOTE 3—All times indicated for TDR measurements are recorded times. Recorded times are twice the transit time of the TDR signal.

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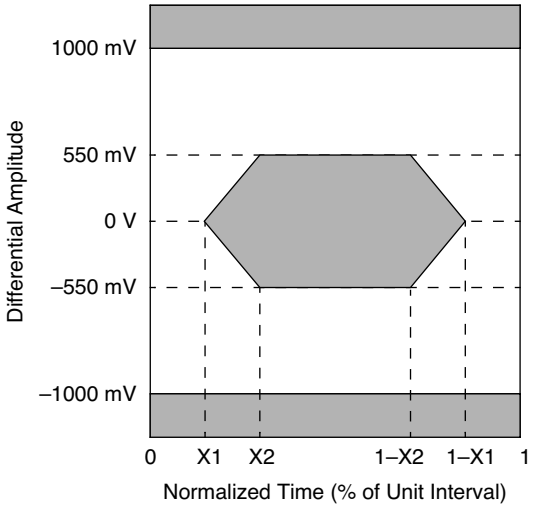


Figure 39–4—Absolute eye diagram mask at TP2

NOTE 4—The transmit differential skew is the maximum allowed time difference (on both low-to-high and high-to low transitions) as measured at TP2, between the true and complement signals. This time difference is measured at the mid-way point on the signal swing of the true and complement signals. These are single-ended measurements.

NOTE 5—The transmitter amplitude maximum specification identifies the maximum p-p signal that can be delivered into a resistive load matching that shown in Figure 39–2.

NOTE 6—The transmitter amplitude minimum specification identifies the minimum allowed p-p eye amplitude opening that can be delivered into a resistive load matching that shown in Figure 39–2.

NOTE 7—The normalized 1 is that amplitude determined to be the average amplitude when driving a logic 1. The normalized 0 is that amplitude determined to be the average amplitude when driving a logic 0.

NOTE 8—Eye diagram assumes the presence of only high-frequency jitter components that are not tracked by the clock recovery circuit. For this standard the lower cutoff frequency for jitter is 637 kHz.

39.3.2 Receiver electrical specifications

The receiver shall be ac-coupled to the media through a receive network located between TP3 and TP4 as shown in Figure 39–1. The receiver shall meet the signal requirements listed in Table 39–4.

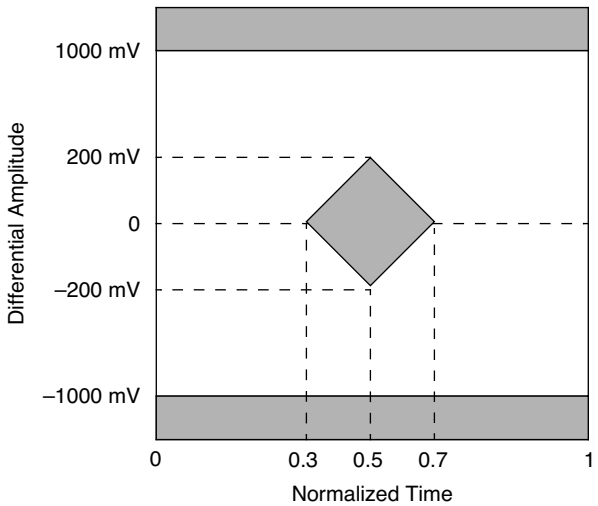


Figure 39–5—Eye diagram mask at point-TP3

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Table 39–4—Receiver characteristics (TP3)

Description	Value	Units
Data rate	1000	Mb/s
Nominal signalling speed	1250	MBd
Tolerance	±100	ppm
Minimum differential sensitivity (peak-peak)	400	mV
Maximum differential input (peak-peak)	2000	mV
Input Impedance @ TP3		
TDR Rise Time	85	ps
Exception_window[a]	700	ps
Through_connection	150 ± 30	Ω
At Termination[b]	150 ± 10	Ω
Differential Skew	175	ps

[a]Within the Exception_window no single impedance excursion shall exceed the Through_Connection-impedance tolerance for a period of twice the TDR rise time specification.

[b]The input impedance at TP3, for the termination, shall be recorded 4.0 ns following the reference location determined by an open connector between TP3 and TP4.

The minimum input amplitude to the receiver listed in Table 39–4 and Figure 39–5 is a worst case specification across all environmental conditions. Restricted environments may allow operation at lower minimum differential voltages, allowing significantly longer operating distances.

NOTE 1—All specifications, unless specifically listed otherwise, are based on differential measurements.

NOTE 2—The receiver minimum differential sensitivity identifies the minimum p-p eye amplitude at TP3 to meet the BER objective.

NOTE 3—Eye diagrams assume the presence of only high-frequency jitter components that are not tracked by the clock recovery circuit. For this standard the lower cutoff frequency for jitter is 637 kHz.

NOTE 4—All times indicated for TDR measurements are recorded times. Recorded times are twice the transit time of the TDR signal.

NOTE 5—Through_Connection impedance describes the impedance tolerance through a mated connector. This tolerance is greater than the termination or cable impedance due to limits in the technology of the connectors.

39.3.3 Jitter specifications for 1000BASE-CX

The 1000BASE-CX PMD shall meet the total jitter specifications defined in Table 38–10. Normative values are highlighted **in bold.** All other values are informative. Compliance points are defined in 39.3.

Jitter shall be measured as defined in 38.6.8 with the exception that no measurement will require the use of an optical to electrical converter (O/E).

Deterministic jitter budgetary specifications are included here to assist implementers in specifying components. Measurements for DJ are described in 38.6.9 with the exception that no measurement will require the use of an O/E.

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Table 39–5—1000BASE-CX jitter budget

Compliance point	Total jitter[a]		Deterministic jitter	
	UI	ps	UI	ps
TP1	**0.240**	**192**	0.120	96
TP1 to TP2	0.090	72	0.020	16
TP2	**0.279**	**223**	0.140	112
TP2 to TP3	0.480	384	0.260	208
TP3	**0.660**	**528**	0.400	320
TP3 to TP4	0.050	40	0.050	40
TP4	**0.710**	**568**	0.450	360

[a]Total jitter is composed of both deterministic and random components. The allowed random jitter equals the allowed total jitter minus the actual deterministic jitter at that point.

39.4 Jumper cable assembly characteristics

A 1000BASE-CX compliant jumper cable assembly shall consist of a continuous shielded balanced cable terminated at each end with a polarized shielded plug as described in 39.5.1. The jumper cable assembly shall provide an output signal on contacts R+/R– meeting the requirements shown in Figure 39–5 when a transmit signal compliant with Figures 39–3 and 39–4 is connected to the T+/T– contacts at the near-end MDI connector. This jumper cable assembly shall have electrical and performance characteristics as described in Table 39–6. Jumper cable assembly specifications shall be measured using the measurement techniques defined in 39.6. The jumper cable assembly may have integrated compensation networks.

NOTE 1—Jumper cable assemblies that meet the requirements for ANSI X3.230-1994 [B20] (FC-PH) may not meet the requirements of this clause.

NOTE 2—Through_Connection impedance describes the impedance tolerance through a mated connector. This tolerance is greater than the termination or cable impedance due to limits in the technology of the connectors.

To produce jumper cable assemblies capable of delivering signals compliant with the requirements of 39.4, the assemblies should generally have characteristics equal to or better than those in Table 39–7.

39.4.1 Compensation networks

A jumper cable assembly may include an equalizer network to meet the specifications and signal quality requirements (e.g., receiver eye mask at TP3) of this clause. The equalizer shall need no adjustment. All jumper cable assemblies containing such circuits shall be marked with information identifying the specific designed operational characteristics of the jumper cable assembly.

39.4.2 Shielding

The jumper cable assembly shall provide class 2 or better shielding in accordance with IEC 61196-1.

39.5 MDI specification

This clause defines the Media Dependent Interface (MDI). The 1000BASE-CX PMD of 39.3 is coupled to the jumper cable assembly by the media dependent interface (MDI).

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Table 39–6—Jumper cable assembly characteristics (normative)

Description	Value	Unit
Differential skew (max)	150	ps
Link Impedance @ TP2/TP3[a] Through_connection Cable	 150 ± 30 150 ± 10	 W W
TDR rise time Exception_window[b]	85 700	ps ps
Round-trip delay (max)[c]	253 253	bit times ns

[a]The link impedance measurement identifies the impedance mismatches present in the jumper cable assembly when terminated in its characteristic impedance. This measurement includes mated connectors at both ends of the Jumper cable assembly (points TP2 and TP3). The link impedance for the jumper cable assembly, shall be recorded 4.0 ns following the reference location determined by an open connector at TP2 and TP3.

[b]Within the Exception_window no single impedance excursion shall exceed the Through_Connection-impedance tolerance for a period of twice the TDR rise time specification. The Exception_window (used with specific impedance measurements) identifies the maximum time period during which the measured impedance is allowed to exceed the listed impedance tolerance. The maximum excursion within the Exception_window at TP3 shall not exceed ±33% of the nominal cable impedance.

[c]Used in Clause 42. This delay is a budgetary requirement of the upper layers. It is easily met by the jumper cable delay characteristics in this clause.

Table 39–7—Jumper cable assembly characteristics (informative)

Description	Value	Unit
Attenuation (max.) at 625 MHz	8.8	dB
Minimum NEXT loss @ 85 ps Tr (max)	6 24.5	% dB

39.5.1 MDI connectors

Connectors meeting the requirements of 39.5.1.1 (Style-1) and 39.5.1.2 (Style-2) shall be used as the mechanical interface between the PMD of 39.3 and the jumper cable assembly of 39.4. The plug connector shall be used on the jumper cable assembly and the receptacle on the PHY. Style-1 or style-2 connectors may be used as the MDI interface. To limit possible cross-plugging with non-1000BASE-CX interfaces that make use of the Style-1 connector, it is recommended that the Style-2 connector be used as the MDI connector.

39.5.1.1 Style-1 connector specification

The style-1 balanced connector for balanced jumper cable assemblies shall be the 9-pin shielded D-subminiature connector, with the mechanical mating interface defined by IEC 60807-3, having pinouts matching those in Figure 39–6, and the signal quality and electrical requirements of this clause. The style-1 connector pin assignments are shown in Figure 39–6 and Table 39–8.

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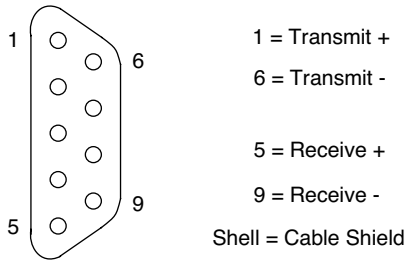


Figure 39–6—Style-1 balanced connector receptacle pin assignments

39.5.1.2 Style-2 connector specification

The style-2 balanced cable connector is the 8-pin shielded ANSI Fibre Channel style-2 connector with the mechanical mating interface defined by IEC 61076-3-103, having pinouts matching those shown in Figure 39–7, and conforming to the signal quality and electrical requirements of this clause.

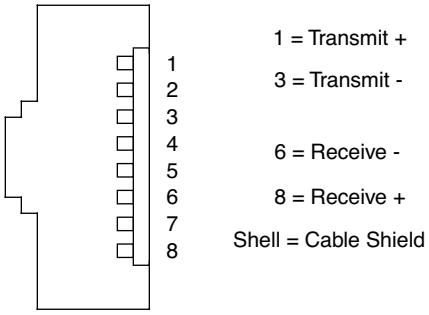


Figure 39–7—Style-2 balanced connector receptacle pin assignments

The style-1 or style-2 connector may be populated with optional contacts to support additional functions. The presence of such contacts in the connector assemblies does not imply support for these additional functions.

NOTE 1—Style-1 pins 2 and 8 (Style-2 pins 7 and 2) are reserved for applications that assign these pins to power and ground.

NOTE 2—Style-1 pin 3 (Style-2 pin 4) is reserved for applications that assign this pin to a Fault Detect function.

NOTE 3—Style-1 pin 7 (Style-2 pin 5) is reserved for applications that assign this pin to an Output Disable function.

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Table 39–8—MDI contact assignments

Contact		PMD MDI signal
Style-1	Style-2	
1	1	Transmit +
2	7	Reserved
3	4	Reserved
4		Mechanical key
5	8	Receive +
6	3	Transmit –
7	5	Reserved
8	2	Reserved
9	6	Receive –

39.5.1.3 Style-2 connector example drawing (informative)

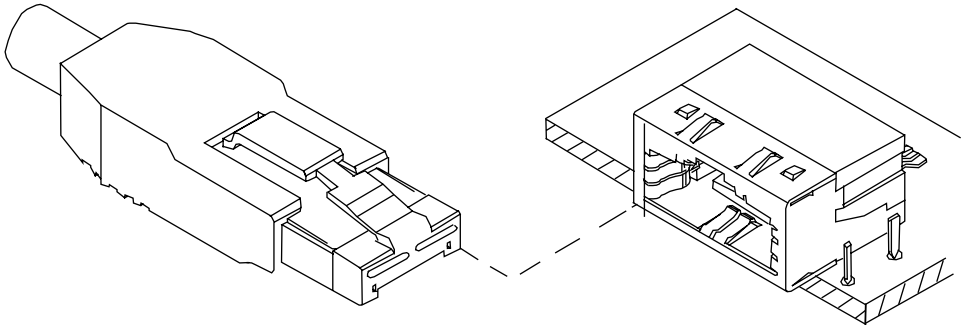


Figure 39–8—Style-2 connector, example drawing

39.5.2 Crossover function

The default jumper cable assembly shall be wired in a crossover fashion as shown in Figure 39–9, with each pair being attached to the transmitter contacts at one end and the receiver contacts at the other end.

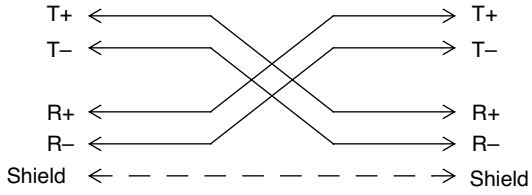


Figure 39–9—Balanced cable wiring

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39.6 Electrical measurement requirements

Electrical measurements shall be performed as described in this subclause.

39.6.1 Transmit rise/fall time

Rise time is a differential measurement across the T+ and T– outputs with a load present (including test equipment) equivalent to that shown in Figure 39–2. Both rising and falling edges are measured. The 100% and 0% levels are the normalized 1 and 0 levels present when sending an alternating K28.5 character stream.

Once the normalized amplitude is determined, the data pattern is changed to a continuous D21.5 character stream. The rise time specification is the time interval between the normalized 20% and 80% amplitude levels.

39.6.2 Transmit skew measurement

The transmitter skew is the time difference between the T+ and T– outputs measured at the normalized 50% crossover point with a load present (including test equipment) equivalent to that shown in Figure 39–2. This measurement is taken using two single ended probes. Skew in the test set-up must be calibrated out.

Normalized amplitudes can be determined using the method described in 39.6.1.

A continuous D21.5 or K28.7 data pattern is transmitted by the device under test. The data is averaged using an averaging scope. An easy method to view and measure the skew between these signals is to invert one.

39.6.3 Transmit eye (normalized and absolute)

This test is made as a differential measurement at the bulkhead connector. The scope trigger must either be a recovered clock as defined in 38.6.8 or a character clock internal to the equipment. The data pattern for this is the alternating K28.5.

If a character trigger is used, the overshoot/undershoot percentages must be measured at all ten bit positions. The load for this test is that shown in Figure 39–2.

39.6.4 Through_connection impedance

This is a differential TDR or equivalent measurement that must be made through a mated connector pair or pairs. Any lead-in trace or cable to the connector that is part of the test fixture should provide a reasonable impedance match so as to not effect the actual measurement. All TDR measurements must be filtered to the TDR rise time specification. Any test fixture used with these TDR tests must be calibrated to remove the effects of the test fixture, and verified to produce accurate results.

The impedance Through_connection interval starts at the first point where the measured impedance exceeds the limits for the termination and ends at the point that the impedance returns to within the termination impedance limits and remains there.

Within this Through_connection interval, an Exception_window exists where the impedance is allowed to exceed the Through_connection impedance limits up to a maximum deviation of ±33% of the nominal link impedance. The Exception_window begins at the point where the measured impedance first exceeds the impedance tolerance limits for Through_connection.

39.6.5 Jumper cable intra-pair differential skew

The jumper cable intra-pair differential skew measurement is conducted to determine the skew, or difference in velocity, of each wire in a cable pair when driven with a differential source. This measurement requires two

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mated connectors, one at the signal source and one at the opposite end of the cable. A pair of matched, complimentary signals (S+, S–) are driven into the T+ and T– contacts of the connector. These signals are time conditioned to start at the same point. This test shall be performed at both ends of the jumper cable assembly.

The jumper cable intra-pair skew is the time difference between the R+ and R– outputs of the excited pair within the jumper cable assembly measured at the normalized 50% crossover point with a load present (including test equipment) equivalent to that shown in Figure 39–2. This measurement is taken using two single ended probes. Skew in the test set-up must be calibrated out.

Normalized amplitudes can be determined using the method described in 39.6.1.

A continuous square wave is used for S+, S–. The data is averaged using an averaging scope. An easy method to view and measure the skew between these signals is to invert one. A differential TDR can provide a convenient method to time condition the input signals.

39.6.6 Receiver link signal

This differential measurement is made at the end of the jumper cable assembly, through mated connectors with a load present (including test equipment) equivalent to that shown in Figure 39–2. The signal is measured with an alternating K28.5 character stream and is tested to the mask requirements of Figure 39–5.

39.6.7 Near-End Cross Talk (NEXT)

NEXT Loss tests are conducted using a differential TDR (or equivalent) filtered to the rise time limit (near-end cross talk at a maximum T_r of 85 ps) in Table 39–6. The T+ and T– inputs of the jumper cable connector are excited to create a disturber pair while the R+ and R– contacts of the disturbed pair are measured within the same connector. The far-end R+/R– outputs of the disturber pair are terminated per Figure 39–2. The R+ and R– signals of the disturbed pair are terminated with a load (including test equipment) equivalent to that shown in Figure 39–2. The T+ and T– inputs of disturbed pair shall be terminated per Figure 39–2. This test shall be performed at both ends of the jumper cable assembly.

39.6.8 Differential time-domain reflectometry (TDR) measurement procedure

The differential TDR test setup measures the reflected waveform returned from a load when driven with a step input. It is obtained by driving the load under test with a step waveform using a driver with a specified source impedance and rise time. The reflected waveform is the difference between (a) the observed waveform at the device under test when driven with the specified test signal, and (b) the waveform that results when driving a standard test load with the same specified test signal. From this measured result we can infer the impedance of the device under test. The derivative of a time-domain reflectometry measurement is the time-domain equivalent of S_{11} parameter testing used in carrier-based systems.

For the measurement of 1000BASE-CX jumper cables, the following test conditions apply:

a) The driving waveform is sourced from a balanced, differential 150 Ω source with an 85 ps rise time (see 39.6.8.1).
b) The test setup is calibrated (see 39.6.8.2).

39.6.8.1 Driving waveform

If the natural differential output impedance of the driving waveform is not 75 Ω, it may be adjusted to within 75 ± 5 Ω by an attenuating resistive pad. When the driving point resistance is 100 Ω (as would be the case with a differential signal source having two independent, antipodal, 50 Ω sources), a good pad design is shown in Figure 39–10, where R1 = 173.2 Ω and R2 = 43.3 Ω. All resistors are surface-mount packages

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soldered directly to the test fixture with no intervening leads or traces, and the whole structure is mounted on a solid ground plane (used in three places).

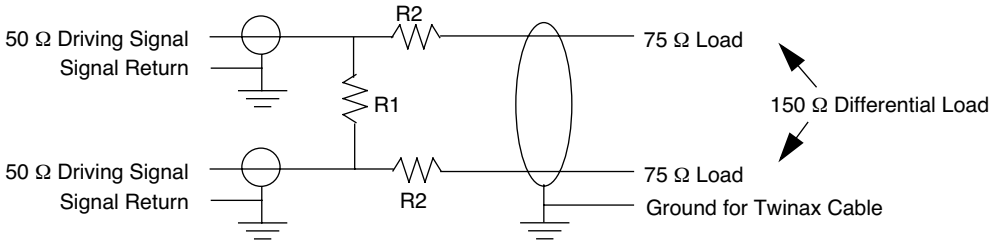


Figure 39–10—Differential TDR pad adapter

If the natural rise time of the driver is less than 85 ps, the resulting measured time-waveforms must be filtered to reduce the apparent rise time to 85 ± 10 ps.

39.6.8.2 Calibration of the test setup

Three measurements are made, with a short, and open, and a known test load. The value of the test resistance should be constant to within 1% over the frequency range dc to 6 GHz, and of known value. The value of the test resistance should be within the range 75 ± 5 Ω.

The differential voltages measured across the device-under-test terminals in these three cases are called V_{short}, V_{open}, and V_{test}, respectively. From these three measurements we will compute three intermediate quantities:

$$A = (V_{open} - V_{short}) /2$$

$$B = (V_{open} + V_{short}) /2$$

$$Z_0 = Z_{test} \cdot (V_{open} - V_{test})/(V_{test} - V_{short})$$

The value of Z_0 is the actual driving point impedance of the tester. It must be within 75 ± 5 Ω.

For any device under test, the conversion from measured voltage $V_{measured}$ to impedance is as follows:

$$\text{Measured impedance} = Z_0 \cdot (1 + V')/(1 - V')$$

where $V' = (V_{measured} - B)/A$.

39.7 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801: 1995. References to the MAU or AUI should be replaced with PHY or DTE and AUI to jumper cable assembly, as appropriate. Subclause 14.7.2.4, *Telephony voltage*, should be ignored. Should a case occur where, through a cabling error, two transmitters or receivers are directly connected, no damage shall occur to any transmitter, receiver, or other link component in the system. The link shall be able to withstand such an invalid connection without component failure or degradation for an indefinite period of time.

Systems connected with 1000BASE-CX links shall meet the bonding requirements (common ground connection) of ISO/IEC 11801: 1995, subclause 9.2, for shielded cable assemblies. Cable shield(s) shall be earthed (chassis ground) through the bulkhead connector shell(s) on both ends of the jumper cable assembly as shown in Figure 39–1.

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39.8 Protocol Implementation Conformance Statement (PICS) proforma for Clause 39, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-CX[7]

39.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 39, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-CX, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

39.8.2 Identification

39.8.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

39.8.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2002, Clause 39, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-CX
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

[7]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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39.8.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*INS	Installation / cable	39.4	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
*STY1	Style-1 MDI	39.5	Either the style-1 or the style-2 MDI must be provided	O/1	Yes [ ] No [ ]
*STY2	Style-2 MDI	39.5		O/1	Yes [ ] No [ ]
*TP1	Standardized reference point TP1 exposed and available for testing.	39.3	This point may be made available for use by implementors to certify component conformance.	O	Yes [ ] No [ ]
*TP4	Standardized reference point TP4 exposed and available for testing.	39.3	This point may be made available for use by implementors to certify component conformance.	O	Yes [ ] No [ ]

39.8.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-CX (short-haul copper)

39.8.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FN1	Integration with 1000BASE-X PCS and PMA	39.1		M	Yes [ ]
FN2	Complies with PMD service interface of 38.2	39.1		M	Yes [ ]
FN3	Jumper cables not concatenated	39.1		INS:M	Yes [ ] N/A [ ]
FN5	Transmit function	39.2.1	Convey bits requested by PMD_UNITDATA.request() to the MDI	M	Yes [ ]
FN6	Transmitter logical to electrical mapping	39.2.1;	Logical one equates to electrical high	M	Yes [ ]
FN7	Receive function	39.2.2	Convey bits received from the MDI to PMD_UNITDATA.indicate()	M	Yes [ ]
FN8	Receiver logical to electrical mapping	39.2.2	Logical one equates to electrical high.	M	Yes [ ]
FN9	Signal detect function	39.2.3	Report to the PMD service interface the message PMD_SIGNAL.indicate(SIGNAL_DETECT)	M	Yes [ ]
FN10	Signal detect behavior	39.2.3	Meets requirements of Table 39–1	M	Yes [ ]

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39.8.4.2 PMD to MDI electrical specifications

Item	Feature	Subclause	Value/Comment	Status	Support
PM1	Measurement requirements	39.3	Electrical measurements are made according to the tests specified in 39.6.	M	Yes [ ]
PM2	Transmitter characteristics	39.3.1	Transmitters meets requirements of Table 39–2	M	Yes [ ]
PM3	Transmitter coupling	39.3.1	AC-coupled	M	Yes [ ]
PM4	Transmitter eye diagram	39.3.1	Meets requirements of Figure 39–3 and Figure 39–4 when terminated as shown in Figure 39–2	M	Yes [ ]
PM5	Receiver coupling	39.3.2	AC-coupled	M	Yes [ ]
PM6	Receiver characteristics	39.3.2	Meet requirements of Table 39–4	M	Yes [ ]
PM7	Measurement conditions for input impedance at TP3	39.3.2	4 ns following reference location	M	Yes [ ]
PM8	Total jitter specification at TP1	39.3.3	Meets specification of bold entries in Table 38–10	TP1:M	Yes [ ] N/A [ ]
PM9	Total jitter specification at TP2	39.3.3	Meets specification of bold entries in Table 38–10	M	Yes [ ]
PM10	Total jitter specification at TP3	39.3.3	Meets specification of bold entries in Table 38–10	INS:M	Yes [ ] N/A [ ]
PM11	Total jitter specification at TP4	39.3.3	Meets specification of bold entries in Table 38–10	TP4:M	Yes [ ] N/A [ ]
PM12	Measurement conditions for jitter	39.3.3	Per 38.6.8 (with exceptions)	M	Yes [ ]

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39.8.4.3 Jumper cable assembly characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
LI1	Two polarized, shielded plug per 39.5.1 and shielded with electrical characteristics per Table 39–6	39.4	As defined in Table 39–6	INS:M	Yes [ ]
LI2	Delivers compliant signal when driven with worst case source signal	39.4	Transmit signal compliant with Figures 39–3 and 39–4, receive signal complaint with Figure 39–5, into a load compliant with Figure 39–2	INS:M	Yes [ ]
LI3	Measurement requirements	39.4	Electrical measurements are made according to the tests specified in 39.6.	INS:M	Yes [ ]
LI4	Maximum excursion during Exception_window of cable impedance measurement	39.4	± 33% of nominal cable impedance	INS:M	Yes [ ]
LI5	Measurement conditions for link impedance	39.4	4 ns following the reference location between TP3 and TP4	INS:M	Yes [ ]
LI6	Equalizer needs no adjustment	39.4.1		INS:M	Yes [ ] N/A [ ]
LI7	Cables containing equalizers shall be marked	39.4.1		INS:M	Yes [ ] N/A [ ]
LI8	Cable shielding	39.4.2	Class 2 or better per IEC 61196-1	INS:M	Yes [ ]

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39.8.4.4 Other requirements

Item	Feature	Subclause	Value/Comment	Status	Support
OR1	Style-1 connector	39.5.1.1	9-pin shielded D-subminiature with the mechanical mating interface defined by IEC 60807-3.	STY1:M	Yes [ ] N/A [ ]
OR2	Style-2 connector	39.5.1.2	8-pin ANSI Fibre Channel style-2 connector with mechanical mating interface defined by IEC 61076-3-103.	STY2:M	Yes [ ] N/A [ ]
OR3	Default cable assembly wired in a crossover assembly	39.5.2		INS:M	Yes [ ]
OR4	Transmit rise/fall time measurement	39.6.1	Meet requirements of Table 39–2 with load equivalent to Figure 39–2	M	Yes [ ]
OR5	Transmit skew measurement	39.6.2	Meet requirements of Table 39–2 with load equivalent to Figure 39–2	M	Yes [ ]
OR6	Transmit eye measurement	39.6.3	Meet requirements of Figure 39–3 and Figure 39–4 with load equivalent to Figure 39–2	M	Yes [ ]
OR7	Through_connection impedance measurement	39.6.4	Meet requirements of Table 39–4 with load equivalent to Figure 39–2	M	Yes [ ]
OR8	Jumper cable assembly differential skew measurement	39.6.5	Meet requirements of Table 39–6 with load equivalent to Figure 39–2	M	Yes [ ]
OR9	Receiver link signal	39.6.6	Meet requirements of Figure 39–5 with load equivalent to Figure 39–2	M	Yes [ ]
OR10	NEXT Loss measurement	39.6.7	Meet requirements of Table 39–6 with load equivalent to Figure 39–2	M	Yes [ ]
OR11	Conformance to 14.7 and applicable sections of ISO/IEC 11801:1995.	39.7		M	Yes [ ]
OR12	Cabling errors shall cause no damage to transmitter, receiver, or other link components	39.7		M	Yes [ ]
OR13	Withstand invalid connection for indefinite period	39.7		M	Yes [ ]
OR14	System meets common ground requirements of ISO/IEC 11801	39.7	Per ISO/IEC 11801, subclause 9.2	INS:M	Yes [ ]
OR15	Cable shields earthed on both ends of cable	39.7		INS:M	Yes [ ]

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40. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 1000BASE-T

40.1 Overview

The 1000BASE-T PHY is one of the Gigabit Ethernet family of high-speed CSMA/CD network specifications. The 1000BASE-T Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) and baseband medium specifications are intended for users who want 1000 Mb/s performance over Category 5 balanced twisted-pair cabling systems. 1000BASE-T signaling requires four pairs of Category 5 balanced cabling, as specified in ISO/IEC 11801:1995 and ANSI/EIA/TIA-568-A (1995) and tested for the additional performance parameters specified in 40.7 using testing procedures defined in proposed ANSI/TIA/EIA TSB95.

This clause defines the type 1000BASE-T PCS, type 1000BASE-T PMA sublayer, and type 1000BASE-T Medium Dependent Interface (MDI). Together, the PCS and the PMA sublayer comprise a 1000BASE-T Physical layer (PHY). Provided in this document are fully functional, electrical, and mechanical specifications for the type 1000BASE-T PCS, PMA, and MDI. This clause also specifies the baseband medium used with 1000BASE-T.

40.1.1 Objectives

The following are the objectives of 1000BASE-T:

a) Support the CSMA/CD MAC
b) Comply with the specifications for the GMII (Clause 35)
c) Support the 1000Mb/s repeater (Clause 41)
d) Provide line transmission that supports full and half duplex operation
e) Meet or exceed FCC Class A/CISPR or better operation
f) Support operation over 100 meters of Category 5 balanced cabling as defined in 40.7
g) Bit Error Rate of less than or equal to 10^{-10}
h) Support Auto-Negotiation (Clause 28)

40.1.2 Relationship of 1000BASE-T to other standards

Relations between the 1000BASE-T PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 CSMA/CD LAN Model are shown in Figure 40–1. The PHY sub-layers (shown shaded) in Figure 40–1 connect one Clause 4 Media Access Control (MAC) layer to the medium.

40.1.3 Operation of 1000BASE-T

The 1000BASE-T PHY employs full duplex baseband transmission over four pairs of Category 5 balanced cabling. The aggregate data rate of 1000 Mb/s is achieved by transmission at a data rate of 250 Mb/s over each wire pair, as shown in Figure 40–2. The use of hybrids and cancellers enables full duplex transmission by allowing symbols to be transmitted and received on the same wire pairs at the same time. Baseband signaling with a modulation rate of 125 Mbaud is used on each of the wire pairs. The transmitted symbols are selected from a four-dimensional 5-level symbol constellation. Each four-dimensional symbol can be viewed as a 4-tuple (A_n, B_n, C_n, D_n) of one-dimensional quinary symbols taken from the set {2, 1, 0, –1, –2}. 1000BASE-T uses a continuous signaling system; in the absence of data, Idle symbols are transmitted. Idle mode is a subset of code-groups in that each symbol is restricted to the set {2, 0, –2}to improve synchronization. Five-level Pulse Amplitude Modulation (PAM5) is employed for transmission over each wire pair. The modulation rate of 125 MBaud matches the GMII clock rate of 125 MHz and results in a symbol period of 8 ns.

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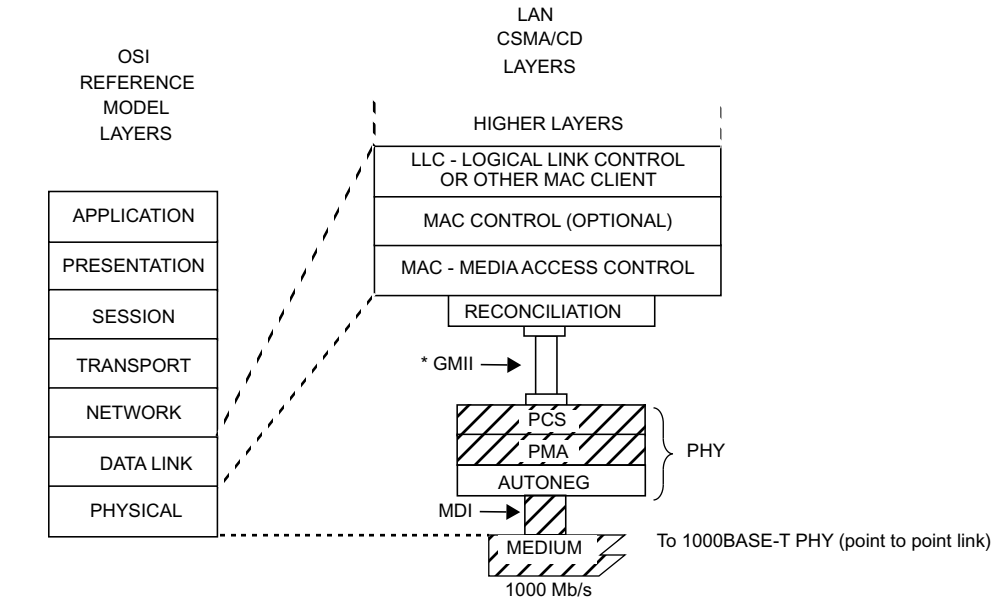


Figure 40–1—Type 1000BASE-T PHY relationship to the ISO Open Systems Interconnection (OSI) Reference Model and the IEEE 802.3 CSMA/CD LAN Model

A 1000BASE-T PHY can be configured either as a MASTER PHY or as a SLAVE PHY. The MASTER-SLAVE relationship between two stations sharing a link segment is established during Auto-Negotiation (see Clause 28, 40.5, and Annex 28C). The MASTER PHY uses a local clock to determine the timing of transmitter operations. The SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations, i.e., it performs loop timing, as illustrated in Figure 40–3. In a multiport to single-port connection, the multiport device is typically set to be MASTER and the single-port device is set to be SLAVE.

The PCS and PMA subclauses of this document are summarized in 40.1.3.1 and 40.1.3.2. Figure 40–3 shows the functional block diagram.

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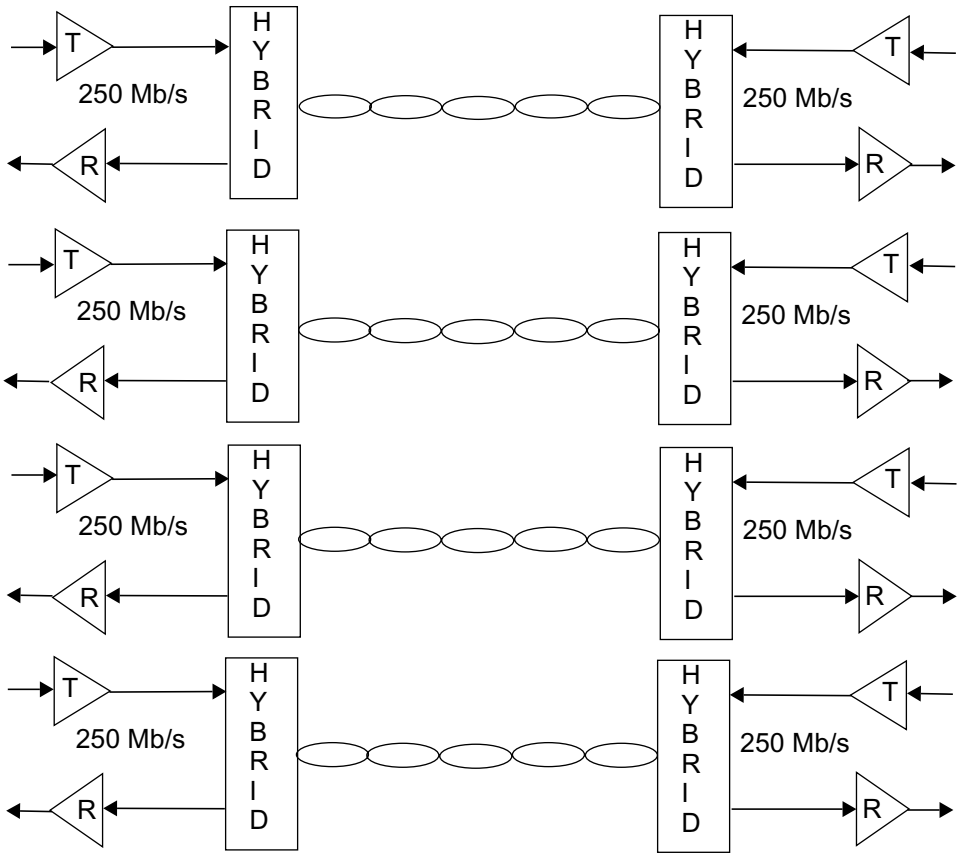
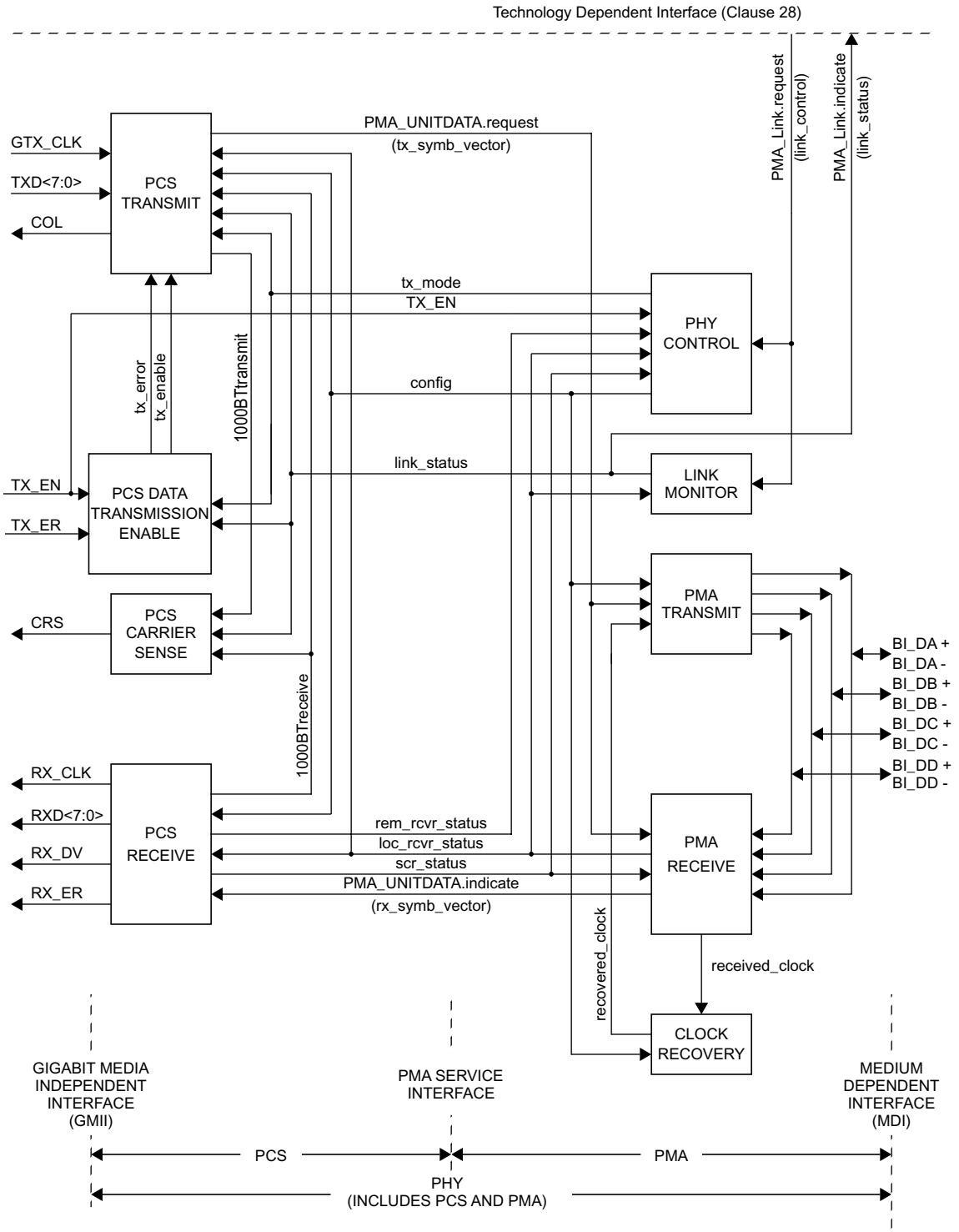


Figure 40–2—1000BASE-T topology

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NOTE The recovered_clock arc is shown to indicate delivery of the received clock signal back to PMA TRANSMIT for loop timing.

Figure 40–3—Functional block diagram

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40.1.3.1 Physical Coding Sublayer (PCS)

The 1000BASE-T PCS couples a Gigabit Media Independent Interface (GMII), as described in Clause 35, to a Physical Medium Attachment (PMA) sublayer.

The functions performed by the PCS comprise the generation of continuous code-groups to be transmitted over four channels and the processing of code-groups received from the remote PHY. The process of converting data bits to code-groups is called 4D-PAM5, which refers to the four-dimensional 5-level Pulse Amplitude Modulation coding technique used. Through this coding scheme, eight bits are converted to one transmission of four quinary symbols.

During the beginning of a frame's transmission, when TX_EN is asserted from the GMII, two code-groups representing the Start-of-Stream delimiter are transmitted followed by code-groups representing the octets coming from the GMII. Immediately following the data octets, the GMII sets TX_EN=FALSE, upon which the end of a frame is transmitted. The end of a frame consists of two convolutional state reset symbol periods and two End-of-Stream delimiter symbol periods. This is followed by an optional series of carrier extend symbol periods and, possibly, the start of a new frame during frame bursting. Otherwise, the end of a frame is followed by a series of symbols encoded in the idle mode. The nature of the encoding that follows the end of a frame is determined by the GMII signals TX_ER and TXD<7:0> as specified in Clause 35.

Between frames, a special subset of code-groups using only the symbols {2, 0, –2} is transmitted. This is called idle mode. Idle mode encoding takes into account the information of whether the local PHY is operating reliably or not (see 40.4.2.4) and allows this information to be conveyed to the remote station. During normal operation, idle mode is followed by a data mode that begins with a Start-of-Stream delimiter.

Further patterns are used for signaling a transmit error and other control functions during transmission of a data stream.

The PCS Receive processes code-groups provided by the PMA. The PCS Receive detects the beginning and the end of frames of data and, during the reception of data, descrambles and decodes the received code-groups into octets RXD<7:0> that are passed to the GMII. The conversion of code-groups to octets uses an 8B1Q4 data decoding technique. PCS Receive also detects errors in the received sequences and signals them to the GMII. Furthermore, the PCS contains a PCS Carrier Sense function, a PCS Collision Presence function, and a management interface.

The PCS functions and state diagrams are specified in 40.3. The signals provided by the PCS at the GMII conform to the interface requirements of Clause 35. The PCS Service Interfaces to the GMII and the PMA are abstract message-passing interfaces specified in 40.2.

40.1.3.2 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PMA service interface onto the balanced cabling physical medium and provides the link management and PHY Control functions. The PMA provides full duplex communications at 125 MBaud over four pairs of balanced cabling up to 100 m in length.

The PMA Transmit function comprises four independent transmitters to generate five-level, pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD, as described in 40.4.3.1.

The PMA Receive function comprises four independent receivers for five-level pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD, as described in 40.4.3.2. This signal encoding technique is referred to as 4D-PAM5. The receivers are responsible for acquiring clock and providing code-groups to the PCS as defined by the PMA_UNITDATA.indicate message. The PMA also contains functions for Link Monitor.

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The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control begins following the completion of Auto-Negotiation and provides the start-up functions required for successful 1000BASE-T operation. It determines whether the PHY operates in a normal state, enabling data transmission over the link segment, or whether the PHY sends special code-groups that represent the idle mode. The latter occurs when either one or both of the PHYs that share a link segment are not operating reliably.

PMA functions and state diagrams are specified in 40.4. PMA electrical specifications are given in 40.6.

40.1.4 Signaling

1000BASE-T signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over each wire pair. The signaling scheme achieves a number of objectives including

a) Forward Error Correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping and inverse mapping from octet data to a quartet of quinary symbols and back.
c) Uncorrelated symbols in the transmitted symbol stream.
d) No correlation between symbol streams traveling both directions on any pair combination.
e) No correlation between symbol streams on pairs BI_DA, BI_DB, BI_DC, and BI_DD.
f) Idle mode uses a subset of code-groups in that each symbol is restricted to the set {2, 0, –2}to ease synchronization, start-up, and retraining.
g) Ability to rapidly or immediately determine if a symbol stream represents data or idle or carrier extension.
h) Robust delimiters for Start-of-Stream delimiter (SSD), End-of-Stream delimiter (ESD), and other control signals.
i) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
j) Ability to automatically detect and correct for pair swapping and unexpected crossover connections.
k) Ability to automatically detect and correct for incorrect polarity in the connections.
l) Ability to automatically correct for differential delay variations across the wire-pairs.

The PHY operates in two basic modes, normal mode or training mode. In normal mode, PCS generates code-groups that represent data, control, or idles for transmission by the PMA. In training mode, the PCS is directed to generate only idle code-groups for transmission by the PMA, which enable the receiver at the other end to train until it is ready to operate in normal mode. (See the PCS reference diagram in 40.2.)

40.1.5 Inter-sublayer interfaces

All implementations of the balanced cabling link are compatible at the MDI. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and GMII (if the GMII is implemented) specifications are met. When the PHY is incorporated within the physical bounds of a single-port device or a multiport device, implementation of the GMII is optional. System operation from the perspective of signals at the MDI and management objects are identical whether the GMII is implemented or not.

40.1.6 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5.

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The values of all components in test circuits shall be accurate to within ±1% unless otherwise stated.

Default initializations, unless specifically specified, are left to the implementor.

40.2 1000BASE-T Service Primitives and Interfaces

1000BASE-T transfers data and control information across the following four service interfaces:

a) Gigabit Media Independent Interface (GMII)
b) PMA Service Interface
c) Medium Dependent Interface (MDI)
d) Technology-Dependent Interface

The GMII is specified in Clause 35; the Technology-Dependent Interface is specified in Clause 28. The PMA Service Interface is defined in 40.2.2 and the MDI is defined in 40.8.

40.2.1 Technology-Dependent Interface

1000BASE-T uses the following service primitives to exchange status indications and control signals across the Technology-Dependent Interface as specified in Clause 28:

PMA_LINK.request (link_control)

PMA_LINK.indicate (link_status)

40.2.1.1 PMA_LINK.request

This primitive allows the Auto-Negotiation algorithm to enable and disable operation of the PMA as specified in 28.2.6.2.

40.2.1.1.1 Semantics of the primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

SCAN_FOR_CARRIER	Used by the Auto-Negotiation algorithm prior to receiving any fast link pulses. During this mode the PMA reports link_status=FAIL.PHY processes are disabled.
DISABLE	Set by the Auto-Negotiation algorithm in the event fast link pulses are detected. PHY processes are disabled. This allows the Auto-Negotiation algorithm to determine how to configure the link.
ENABLE	Used by Auto-Negotiation to turn control over to the PHY for data processing functions.

40.2.1.1.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in Clause 28.

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40.2.1.1.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as defined in 40.4.2.5.

40.2.1.2 PMA_LINK.indicate

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 28.2.6.1. This primitive informs the PCS, PMA PHY Control function, and the Auto-Negotiation algorithm about the status of the underlying link.

40.2.1.2.1 Semantics of the primitive

PMA_LINK.indicate (link_status)

The link_status parameter can take on one of three values: FAIL, READY, or OK.

FAIL	No valid link established.
READY	The Link Monitor function indicates that a 1000BASE-T link is intact and ready to be established.
OK	The Link Monitor function indicates that a valid 1000BASE-T link is established. Reliable reception of signals transmitted from the remote PHY is possible.

40.2.1.2.2 When generated

The PMA generates this primitive continuously to indicate the value of link_status in compliance with the state diagram given in Figure 40–16.

40.2.1.2.3 Effect of receipt

The effect of receipt of this primitive is specified in 40.3.3.1.

40.2.2 PMA Service Interface

1000BASE-T uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indicate (tx_mode)

PMA_CONFIG.indicate (config)

PMA_UNITDATA.request (tx_symb_vector)

PMA_UNITDATA.indicate (rx_symb_vector)

PMA_SCRSTATUS.request (scr_status)

PMA_RXSTATUS.indicate (loc_rcvr_status)

PMA_REMRXSTATUS.request (rem_rcvr_status)

The use of these primitives is illustrated in Figure 40–4.

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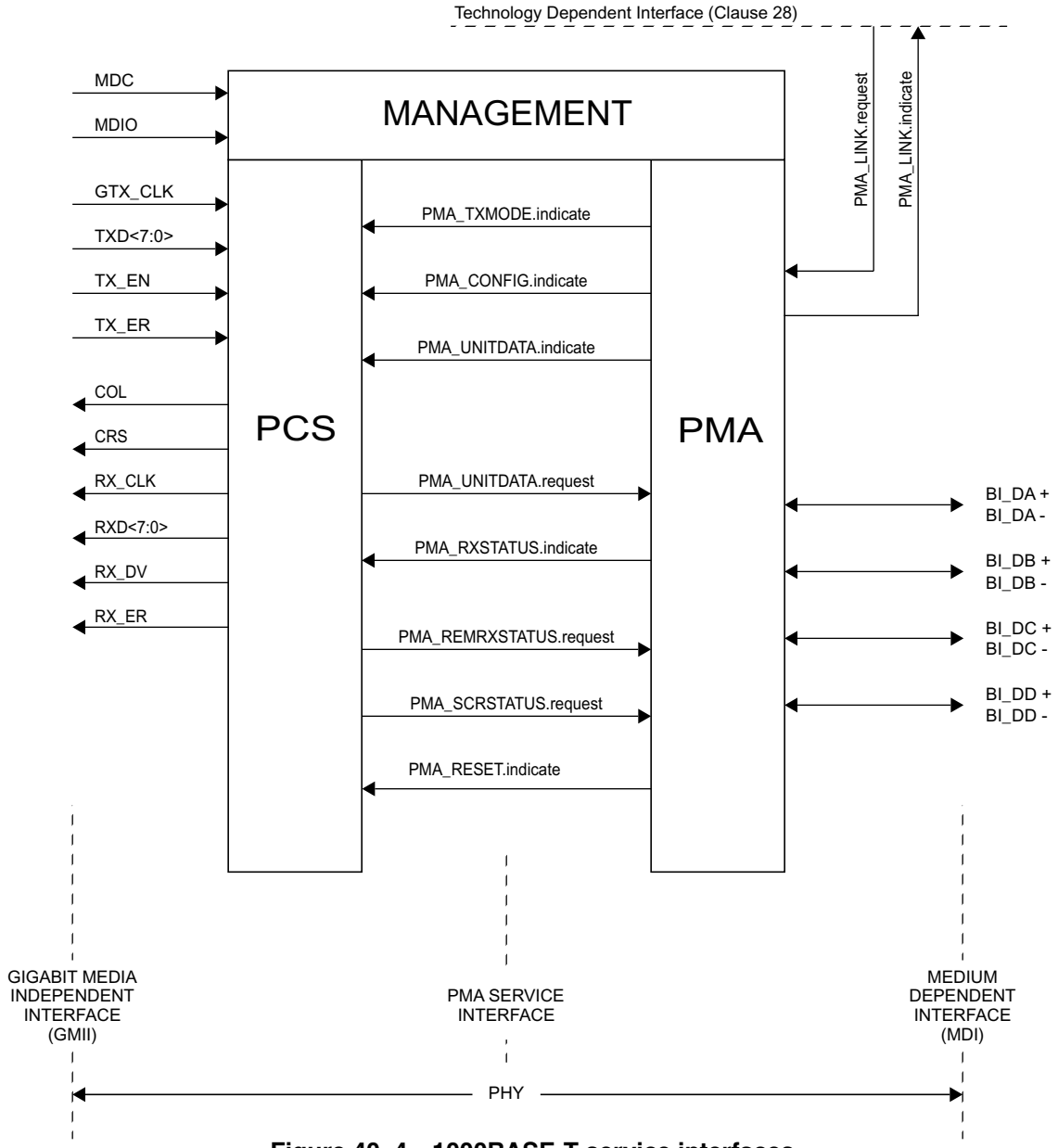


Figure 40–4—1000BASE-T service interfaces

40.2.3 PMA_TXMODE.indicate

The transmitter in a 1000BASE-T link normally sends over the four pairs, code-groups that can represent a GMII data stream, control information, or idles.

40.2.3.1 Semantics of the primitive

PMA_TXMODE.indicate (tx_mode)

PMA_TXMODE.indicate specifies to PCS Transmit via the parameter tx_mode what sequence of code-groups the PCS should be transmitting. The parameter tx_mode can take on one of the following three values of the form:

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SEND_N	This value is continuously asserted when transmission of sequences of code-groups representing a GMII data stream (data mode), control mode or idle mode is to take place.
SEND_I	This value is continuously asserted in case transmission of sequences of code-groups representing the idle mode is to take place.
SEND_Z	This value is continuously asserted in case transmission of zeros is required.

40.2.3.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indicate messages continuously.

40.2.3.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its Transmit function as described in 40.3.1.3.

40.2.4 PMA_CONFIG.indicate

Each PHY in a 1000BASE-T link is capable of operating as a MASTER PHY and as a SLAVE PHY. MASTER-SLAVE configuration is determined during Auto-Negotiation (40.5). The result of this negotiation is provided to the PMA.

40.2.4.1 Semantics of the primitive

PMA_CONFIG.indicate (config)

PMA_CONFIG.indicate specifies to PCS and PMA Transmit via the parameter config whether the PHY must operate as a MASTER PHY or as a SLAVE PHY. The parameter config can take on one of the following two values of the form:

MASTER	This value is continuously asserted when the PHY must operate as a MASTER PHY.
SLAVE	This value is continuously asserted when the PHY must operate as a SLAVE PHY.

40.2.4.2 When generated

PMA generates PMA_CONFIG.indicate messages continuously.

40.2.4.3 Effect of receipt

PCS and PMA Clock Recovery perform their functions in MASTER or SLAVE configuration according to the value assumed by the parameter config.

40.2.5 PMA_UNITDATA.request

This primitive defines the transfer of code-groups in the form of the tx_symb_vector parameter from the PCS to the PMA. The code-groups are obtained in the PCS Transmit function using the encoding rules defined in 40.3.1.3 to represent GMII data streams, an idle mode, or other sequences.

40.2.5.1 Semantics of the primitive

PMA_UNITDATA.request (tx_symb_vector)

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During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. The tx_symb_vector parameter takes on the form:

SYMB_4D	A vector of four quinary symbols, one for each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. Each quinary symbol may take on one of the values –2, –1, 0, +1, or +2.

The quinary symbols that are elements of tx_symb_vector are called, according to the pair on which each will be transmitted, tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD].

40.2.5.2 When generated

The PCS generates PMA_UNITDATA.request (SYMB_4D) synchronously with every transmit clock cycle.

40.2.5.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated quinary symbols. The parameter tx_symb_vector is also used by the PMA Receive function to process the signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD.

40.2.6 PMA_UNITDATA.indicate

This primitive defines the transfer of code-groups in the form of the rx_symb_vector parameter from the PMA to the PCS.

40.2.6.1 Semantics of the primitive

PMA_UNITDATA.indicate (rx_symb_vector)

During reception the PMA_UNITDATA.indicate simultaneously conveys to the PCS via the parameter rx_symb_vector the values of the symbols detected on each of the four receive pairs BI_DA, BI_DB, BI_DC, and BI_DD. The rx_symbol_vector parameter takes on the form:

SYMB_4D	A vector of four quinary symbols, one for each of the four receive pairs BI_DA, BI_DB, BI_DC, and BI_DD. Each quinary symbol may take on one of the values –2, –1, 0, +1, or +2.

The quinary symbols that are elements of rx_symb_vector are called, according to the pair upon which each symbol was received, rx_symbol_vector[BI_DA], rx_symbol_vector[BI_DB], rx_symbol_vector[BI_DC], and rx_symb_vector[BI_DD].

40.2.6.2 When generated

The PMA generates PMA_UNITDATA.indicate (SYMB_4D) messages synchronously with signals received at the MDI. The nominal rate of the PMA_UNITDATA.indicate primitive is 125 MHz, as governed by the recovered clock.

40.2.6.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

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40.2.7 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the descrambler has achieved synchronization.

40.2.7.1 Semantics of the primitive

PMA_SCRSTATUS.request (scr_status)

The scr_status parameter can take on one of two values of the form:

OK	The descrambler has achieved synchronization.
NOT_OK	The descrambler is not synchronized.

40.2.7.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages continuously.

40.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in 40.4.2.3, 40.4.2.4, and 40.4.6.1.

40.2.8 PMA_RXSTATUS.indicate

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criterion for setting the parameter loc_rcvr_status is left to the implementor. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol streams that represent the idle mode.

40.2.8.1 Semantics of the primitive

PMA_RXSTATUS.indicate (loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the form:

OK	This value is asserted and remains true during reliable operation of the receive link for the local PHY.
NOT_OK	This value is asserted whenever operation of the link for the local PHY is unreliable.

40.2.8.2 When generated

PMA Receive generates PMA_RXSTATUS.indicate messages continuously on the basis of signals received at the MDI.

40.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 40–15 and in subclauses 40.2 and 40.4.6.2.

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40.2.9 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The criterion for setting the parameter rem_rcvr_status is left to the implementor. It can be based, for example, on asserting rem_rcvr_status is NOT_OK until loc_rcvr_status is OK and then asserting the detected value of rem_rcvr_status after proper PCS receive decoding is achieved.

40.2.9.1 Semantics of the primitive

PMA_REMRXSTATUS.request (rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK	The receive link for the remote PHY is operating reliably.
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected.

40.2.9.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages continuously on the basis on signals received at the MDI.

40.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 40–15.

40.2.10 PMA_RESET.indicate

This primitive is used to pass the PMA Reset function to the PCS (pcs_reset=ON) when reset is enabled.

The PMA_RESET.indicate primitive can take on one of two values:

TRUE	Reset is enabled.
FALSE	Reset is not enabled.

40.2.10.1 When generated

The PMA Reset function is executed as described in 40.4.2.1.

40.2.10.2 Effect of receipt

The effect of receipt of this primitive is specified in 40.4.2.1.

40.3 Physical Coding Sublayer (PCS)

The PCS comprises one PCS Reset function and four simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit Enable, PCS Transmit, PCS Receive, and PCS Carrier Sense. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 40–5, shows how the four operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other

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layers are pervasive, and are not shown in Figure 40–5. Management is specified in Clause 30. See also Figure 40–7, which defines the structure of frames passed from PCS to PMA.

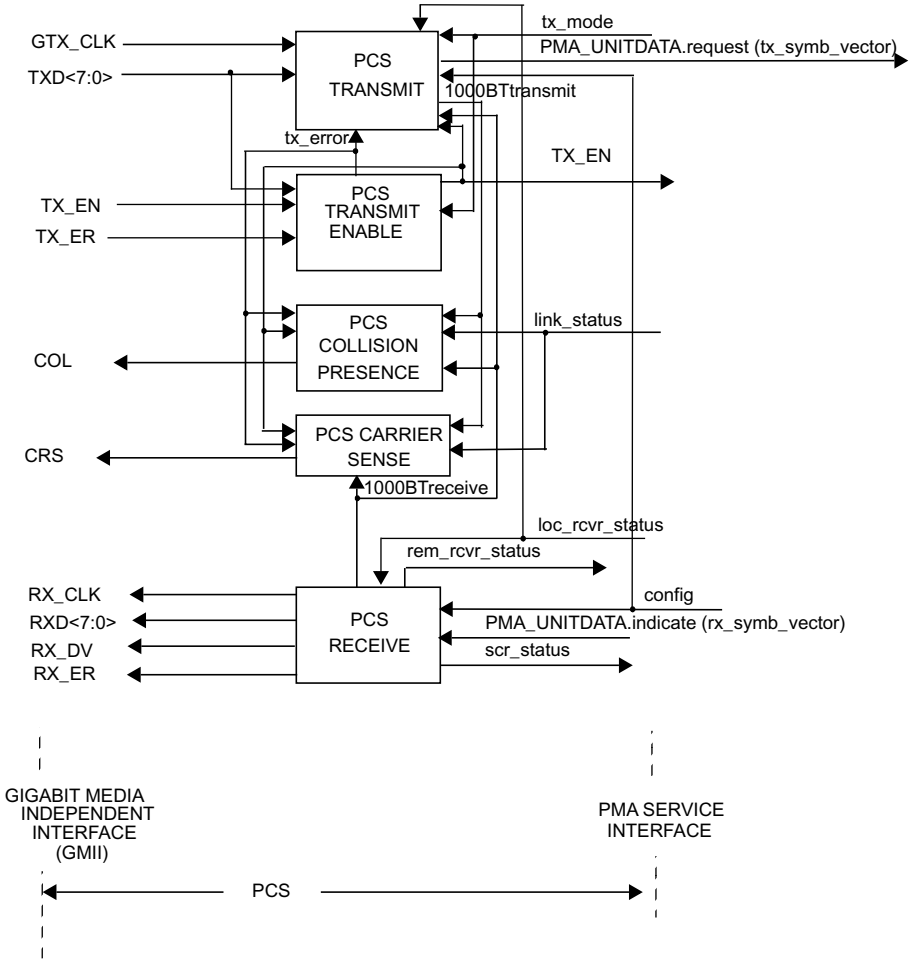


Figure 40–5—PCS reference diagram

40.3.1 PCS functions

40.3.1.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on (see 36.2.5.1.3).
b) The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset=ON while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

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40.3.1.2 PCS Data Transmission Enable

The PCS Data Transmission Enabling process generates the signals tx_enable and tx_error, which PCS Transmit uses for data and carrier extension encoding. The process uses logical operations on tx_mode, TX_ER, TX_EN, and TXD<7:0>. The PCS shall implement the Data Transmission Enabling process as depicted in Figure 40–8 including compliance with the associated state variables as specified in 40.3.3.

40.3.1.3 PCS Transmit function

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 40–9.

The PCS Transmit function generates the GMII signal COL based on whether a reception is occurring simultaneously with transmission. The PCS Transmit function is not required to generate the GMII signal COL in a 1000BASE-T PHY that does not support half duplex operation.

In each symbol period, PCS Transmit generates a code-group (A_n, B_n, C_n, D_n) that is transferred to the PMA via the PMA_UNITDATA.request primitive. The PMA transmits symbols A_n, B_n, C_n, D_n over wire-pairs BI_DA, BI_DB, BI_DC, and BI_DD respectively. The integer, n, is a time index that is introduced to establish a temporal relationship between different symbol periods. A symbol period, T, is nominally equal to 8 ns. In normal mode of operation, between streams of data indicated by the parameter tx_enable, PCS Transmit generates sequences of vectors using the encoding rules defined for the idle mode. Upon assertion of tx_enable, PCS Transmit passes a SSD of two consecutive vectors of four quinary symbols to the PMA, replacing the first two preamble octets. Following the SSD, each TXD<7:0> octet is encoded using an 4D-PAM5 technique into a vector of four quinary symbols until tx_enable is de-asserted. If TX_ER is asserted while tx_enable is also asserted, then PCS Transmit passes to the PMA vectors indicating a transmit error. Note that if the signal TX_ER is asserted while SSD is being sent, the transmission of the error condition is delayed until transmission of SSD has been completed. Following the de-assertion of tx_enable, a Convolutional State Reset (CSReset) of two consecutive code-groups, followed by an ESD of two consecutive code-groups, is generated, after which the transmission of idle or control mode is resumed.

If a PMA_TXMODE.indicate message has the value SEND_Z, PCS Transmit passes a vector of zeros at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indicate message has the value SEND_I, PCS Transmit generates sequences of code-groups according to the encoding rule in training mode. Special code-groups that use only the values {+2, 0, –2} are transmitted in this case. Training mode encoding also takes into account the value of the parameter loc_rcvr_status. By this mechanism, a PHY indicates the status of its own receiver to the link partner during idle transmission.

In the normal mode of operation, the PMA_TXMODE.indicate message has the value SEND_N, and the PCS Transmit function uses an 8B1Q4 coding technique to generate at each symbol period code-groups that represent data, control or idle based on the code-groups defined in Table 40–1 and Table 40–2. During transmission of data, the TXD<7:0> bits are scrambled by the PCS using a side-stream scrambler, then encoded into a code-group of quinary symbols and transferred to the PMA. During data encoding, PCS Transmit utilizes a three-state convolutional encoder.

The transition from idle or carrier extension to data is signalled by inserting a SSD, and the end of transmission of data is signalled by an ESD. Further code-groups are reserved for signaling the assertion of TX_ER within a stream of data, carrier extension, CSReset, and other control functions. During idle and carrier extension encoding, special code-groups with symbol values restricted to the set {2, 0, –2} are used. These code-groups are also generated using the transmit side-stream scrambler. However, the encoding rules for the idle, SSD, and carrier extend code-groups are different from the encoding rules for data, CSReset, CSExtend, and ESD code-groups. During idle, SSD, and carrier extension, the PCS Transmit function reverses the sign of the transmitted symbols. This allows, at the receiver, sequences of code-groups that represent data,

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CSReset, CSExtend, and ESD to be easily distinguished from sequences of code-groups that represent SSD, carrier extension, and idle.

PCS encoding involves the generation of the four-bit words $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$ from which the quinary symbols (A_n, B_n, C_n, D_n) are obtained. The four-bit words $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$ are determined (as explained in 40.3.1.3.2) from sequences of pseudorandom binary symbols derived from the transmit side-stream scrambler.

40.3.1.3.1 Side-stream scrambler polynomials

The PCS Transmit function employs side-stream scrambling. If the parameter config provided to the PCS by the PMA PHY Control function via the PMA_CONFIG.indicate message assumes the value MASTER, PCS Transmit shall employ

$$g_M(x) = 1 + x^{13} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. If the PMA_CONFIG.indicate message assumes the value of SLAVE, PCS Transmit shall employ

$$g_S(x) = 1 + x^{20} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. An implementation of master and slave PHY side-stream scramblers by linear-feedback shift registers is shown in Figure 40–6. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementor. In no case shall the scrambler state be initialized to all zeros.

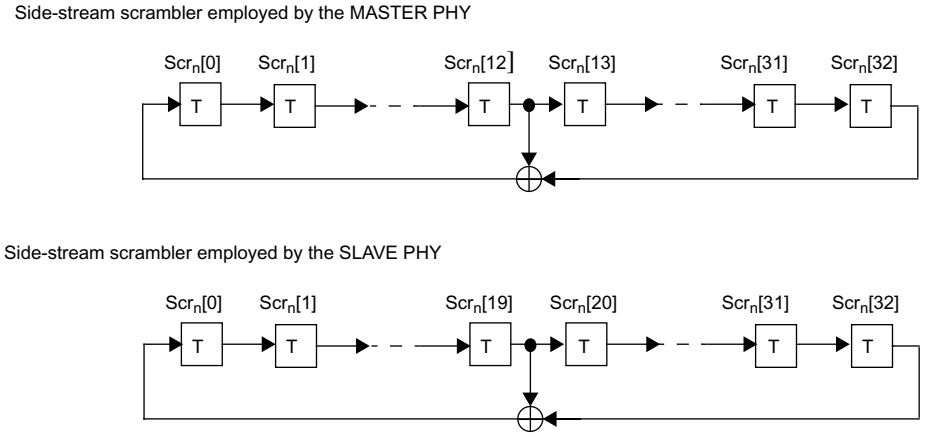


Figure 40–6—A realization of side-stream scramblers by linear feedback shift registers

40.3.1.3.2 Generation of bits $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$

PCS Transmit encoding rules are based on the generation, at time n, of the twelve bits $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$. The eight bits, $Sx_n[3:0]$ and $Sy_n[3:0]$, are used to generate the scrambler octet $Sc_n[7:0]$ for decorrelating the GMII data word TXD<7:0> during data transmission and for generating the idle and training symbols. The four bits, $Sg_n[3:0]$, are used to randomize the signs of the quinary symbols (A_n, B_n, C_n,

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D_n) so that each symbol stream has no dc bias. These twelve bits are generated in a systematic fashion using three bits, X_n, Y_n, and $Scr_n[0]$, and an auxiliary generating polynomial, g(x). The two bits, X_n and Y_n, are mutually uncorrelated and also uncorrelated with the bit $Scr_n[0]$. For both master and slave PHYs, they are obtained by the same linear combinations of bits stored in the transmit scrambler shift register delay line. These two bits are derived from elements of the same maximum-length shift register sequence of length $2^{33} - 1$ as $Scr_n[0]$, but shifted in time. The associated delays are all large and different so that there is no short-term correlation among the bits $Scr_n[0]$, X_n, and Y_n. The bits X_n and Y_n are generated as follows:

$$X_n = Scr_n[4] \wedge Scr_n[6]$$

$$Y_n = Scr_n[1] \wedge Scr_n[5]$$

where ^ denotes the XOR logic operator. From the three bits X_n, Y_n, and $Scr_n[0]$, further mutually uncorrelated bit streams are obtained systematically using the generating polynomial

$$g(x) = x^3 \wedge x^8$$

The four bits $Sy_n[3:0]$ are generated using the bit $Scr_n[0]$ and g(x) as in the following equations:

$$Sy_n[0] = Scr_n[0]$$

$$Sy_n[1] = g(Scr_n[0]) = Scr_n[3] \wedge Scr_n[8]$$

$$Sy_n[2] = g^2(Scr_n[0]) = Scr_n[6] \wedge Scr_n[16]$$

$$Sy_n[3] = g^3(Scr_n[0]) = Scr_n[9] \wedge Scr_n[14] \wedge Scr_n[19] \wedge Scr_n[24]$$

The four bits $Sx_n[3:0]$ are generated using the bit X_n and g(x) as in the following equations:

$$Sx_n[0] = X_n = Scr_n[4] \wedge Scr_n[6]$$

$$Sx_n[1] = g(X_n) = Scr_n[7] \wedge Scr_n[9] \wedge Scr_n[12] \wedge Scr_n[14]$$

$$Sx_n[2] = g^2(X_n) = Scr_n[10] \wedge Scr_n[12] \wedge Scr_n[20] \wedge Scr_n[22]$$

$$Sx_n[3] = g^3(X_n) = Scr_n[13] \wedge Scr_n[15] \wedge Scr_n[18] \wedge Scr_n[20] \wedge Scr_n[23] \wedge Scr_n[25] \wedge Scr_n[28] \wedge Scr_n[30]$$

The four bits $Sg_n[3:0]$ are generated using the bit Y_n and g(x) as in the following equations:

$$Sg_n[0] = Y_n = Scr_n[1] \wedge Scr_n[5]$$

$$Sg_n[1] = g(Y_n) = Scr_n[4] \wedge Scr_n[8] \wedge Scr_n[9] \wedge Scr_n[13]$$

$$Sg_n[2] = g^2(Y_n) = Scr_n[7] \wedge Scr_n[11] \wedge Scr_n[17] \wedge Scr_n[21]$$

$$Sg_n[3] = g^3(Y_n) = Scr_n[10] \wedge Scr_n[14] \wedge Scr_n[15] \wedge Scr_n[19] \wedge Scr_n[20] \wedge Scr_n[24] \wedge Scr_n[25] \wedge Scr_n[29]$$

By construction, the twelve bits $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$ are derived from elements of the same maximum-length shift register sequence of length $2^{33}-1$ as $Scr_n[0]$, but shifted in time by varying delays. The associated delays are all large and different so that there is no apparent correlation among the bits.

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40.3.1.3.3 Generation of bits $Sc_n[7:0]$

The bits $Sc_n[7:0]$ are used to scramble the GMII data octet TXD[7:0] and for control, idle, and training mode quartet generation. The definition of these bits is dependent upon the bits $Sx_n[3:0]$ and $Sy_n[3:0]$ that are specified in 40.3.1.3.2, the variable tx_mode that is obtained through the PMA Service Interface, the variable tx_enable_n that is defined in Figure 40–8, and the time index n.

The four bits $Sc_n[7:4]$ are defined as

$$Sc_n[7:4] = \begin{cases} Sx_n[3:0] & \text{if } (tx\_enable_{n-2} = 1) \\ [0\ 0\ 0\ 0] & \text{else} \end{cases}$$

The bits $Sc_n[3:1]$ are defined as

$$Sc_n[3:1] = \begin{cases} [0\ 0\ 0] & \text{if } (tx\_mode = SEND\_Z) \\ Sy_n[3:1] & \text{else if } (n\text{-}n_0) = 0 \pmod 2 \\ (Sy_{n-1}[3:1] \wedge [1\ 1\ 1]) & \text{else} \end{cases}$$

where n_0 denotes the time index of the last transmitter side-stream scrambler reset.

The bit $Sc_n[0]$ is defined as

$$Sc_n[0] = \begin{cases} 0 & \text{if } (tx\_mode = SEND\_Z) \\ Sy_n[0] & \text{else} \end{cases}$$

40.3.1.3.4 Generation of bits $Sd_n[8:0]$

The PCS Transmit function generates a nine-bit word $Sd_n[8:0]$ from Sc_n that represents either a convolutionally encoded stream of data, control, or idle mode code-groups. The convolutional encoder uses a three-bit word $cs_n[2:0]$, which is defined as

$$cs_n[1] = \begin{cases} Sd_n[6] \wedge cs_{n-1}[0] & \text{if } (tx\_enable_{n-2} = 1) \\ 0 & \text{else} \end{cases}$$

$$cs_n[2] = \begin{cases} Sd_n[7] \wedge cs_{n-1}[1] & \text{if } (tx\_enable_{n-2} = 1) \\ 0 & \text{else} \end{cases}$$

$$cs_n[0] = cs_{n-1}[2]$$

from which $Sd_n[8]$ is obtained as

$$Sd_n[8] = cs_n[0]$$

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The convolutional encoder bits are non-zero only during the transmission of data. Upon the completion of a data frame, the convolutional encoder bits are reset using the bit csreset$_n$. The bit csreset$_n$ is defined as

$$csreset_n = (tx\_enable_{n-2}) \text{ and } (\text{not } tx\_enable_n)$$

The bits Sd$_n$[7:6] are derived from the bits Sc$_n$[7:6], the GMII data bits TXD$_n$[7:6], and from the convolutional encoder bits as

$$Sd_n[7] = \begin{cases} Sc_n[7] \wedge TXD_n[7] & \text{if } (csreset_n = 0 \text{ and } tx\_enable_{n-2} = 1) \\ cs_{n-1}[1] & \text{else if } (csreset_n = 1) \\ Sc_n[7] & \text{else} \end{cases}$$

$$Sd_n[6] = \begin{cases} Sc_n[6] \wedge TXD_n[6] & \text{if } (csreset_n = 0 \text{ and } tx\_enable_{n-2} = 1) \\ cs_{n-1}[0] & \text{else if } (csreset_n = 1) \\ Sc_n[6] & \text{else} \end{cases}$$

The bits Sd$_n$[5:3] are derived from the bits Sc$_n$[5:3] and the GMII data bits TXD$_n$[5:3] as

$$Sd_n[5:3] = \begin{cases} Sc_n[5:3] \wedge TXD_n[5:3] & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[5:3] & \text{else} \end{cases}$$

The bit Sd$_n$[2] is used to scramble the GMII data bit TXD$_n$[2] during data mode and to encode loc_rcvr_status otherwise. It is defined as

$$Sd_n[2] = \begin{cases} Sc_n[2] \wedge TXD_n[2] & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[2] \wedge 1 & \text{else if } (loc\_rcvr\_status = \text{OK}) \\ Sc_n[2] & \text{else} \end{cases}$$

The bits Sd$_n$[1:0] are used to transmit carrier extension information during tx_mode=SEND_N and are thus dependent upon the bits cext$_n$ and cext_err$_n$. These bits are dependent on the variable tx_error$_n$, which is defined in Figure 40–8. These bits are defined as

$$cext_n = \begin{cases} tx\_error_n & \text{if } ((tx\_enable_n = 0) \text{ and } (TXD_n[7:0] = 0\text{x}0\text{F})) \\ 0 & \text{else} \end{cases}$$

$$cext\_err_n = \begin{cases} tx\_error_n & \text{if } ((tx\_enable_n = 0) \text{ and } (TXD_n[7:0] \neq 0\text{x}0\text{F})) \\ 0 & \text{else} \end{cases}$$

$$Sd_n[1] = \begin{cases} Sc_n[1] \wedge TXD_n[1] & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[1] \wedge cext\_err_n & \text{else} \end{cases}$$

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$$Sd_n[0] = \begin{cases} Sc_n[0] \wedge TXD_n[0] \text{ if } (tx\_enable_{n-2} = 1) \\ Sc_n[0] \wedge cext_n \text{ else} \end{cases}$$

40.3.1.3.5 Generation of quinary symbols TA_n, TB_n, TC_n, TD_n

The nine-bit word $Sd_n[8:0]$ is mapped to a quartet of quinary symbols (TA_n, TB_n, TC_n, TD_n) according to Table 40–1 and Table 40–2 shown as $Sd_n[6:8] + Sd_n[5:0]$.

Encoding of error indication:

If tx_error_n=1 when the condition (tx_enable_n * tx_enable_{n-2}) = 1, error indication is signaled by means of symbol substitution. In this condition, the values of $Sd_n[5:0]$ are ignored during mapping and the symbols corresponding to the row denoted as "xmt_err" in Table 40–1 and Table 40–2 shall be used.

Encoding of Convolutional Encoder Reset:

If tx_error_n=0 when the variable $csreset_n$ = 1, the convolutional encoder reset condition is normal. This condition is indicated by means of symbol substitution, where the values of $Sd_n[5:0]$ are ignored during mapping and the symbols corresponding to the row denoted as "CSReset" in Table 40–1 and Table 40–2 shall be used.

Encoding of Carrier Extension during Convolutional Encoder Reset:

If tx_error_n=1 when the variable $csreset_n$ = 1, the convolutional encoder reset condition indicates carrier extension. In this condition, the values of $Sd_n[5:0]$ are ignored during mapping and the symbols corresponding to the row denoted as "CSExtend" in Table 40–1 and Table 40–2 shall be used when TXD_n = 0x'0F, and the row denoted as "CSExtend_Err" in Table 40–1 and Table 40–2 shall be used when $TXD_n \neq$ 0x'0F. The latter condition denotes carrier extension with error. In case carrier extension with error is indicated during the first octet of CSReset, the error condition shall be encoded during the second octet of CSReset, and during the subsequent two octets of the End-of-Stream delimiter as well. Thus, the error condition is assumed to persist during the symbol substitutions at the End-of-Stream.

Encoding of Start-of-Stream delimiter:

The Start-of-Stream delimiter (SSD) is related to the condition SSD_n, which is defined as (tx_enable_n) * ($!tx\_enable_{n-2}$) = 1, where "*" and "!" denote the logic AND and NOT operators, respectively. For the generation of SSD, the first two octets of the preamble in a data stream are mapped to the symbols corresponding to the rows denoted as SSD1 and SSD2 respectively in Table 40–1. The symbols corresponding to the SSD1 row shall be used when the condition (tx_enable_n) * ($!tx\_enable_{n-1}$) = 1. The symbols corresponding to the SSD2 row shall be used when the condition (tx_enable_{n-1}) * ($!tx\_enable_{n-2}$) = 1.

Encoding of End-of-Stream delimiter:

The definition of an End-of-Stream delimiter (ESD) is related to the condition ESD_n, which is defined as ($!tx\_enable_{n-2}$) * (tn_enable_{n-4}) = 1. This occurs during the third and fourth symbol periods after transmission of the last octet of a data stream.

If carrier extend error is indicated during ESD, the symbols corresponding to the ESD_Ext_Err row shall be used. The two conditions upon which this may occur are

(tx_error_n) * (tx_error_{n-1}) * (tx_error_{n-2}) * ($TXD_n \neq$ 0x0F) = 1, and

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$(tx\_error_n) * (tx\_error_{n-1}) * (tx\_error_{n-2}) * (tx\_error_{n-3}) * (TXD_n \neq 0x0F) = 1$.

The symbols corresponding to the ESD1 row in Table 40–1 shall be used when the condition $(!tx\_enable_{n-2}) * (tx\_enable_{n-3}) = 1$, in the absence of carrier extend error indication at time n.

The symbols corresponding to the ESD2_Ext_0 row in Table 40–1 shall be used when the condition $(!tx\_enable_{n-3}) * (tx\_enable_{n-4}) * (!tx\_error_n) * (!tx\_error_{n-1}) = 1$.

The symbols corresponding to the ESD2_Ext_1 row in Table 40–1 shall be used when the condition $(!tx\_enable_{n-3}) * (tx\_enable_{n-4}) * (!tx\_error_n) * (tx\_error_{n-1}) * (tx\_error_{n-2}) * (tx\_error_{n-3}) = 1$.

The symbols corresponding to the ESD2_Ext_2 row in Table 40–1 shall be used when the condition $(!tx\_enable_{n-3}) * (tx\_enable_{n-4}) * (tx\_error_n) * (tx\_error_{n-1}) * (tx\_error_{n-2}) * (tx\_error_{n-3}) * (TXD_n = 0x0F) = 1$, in the absence of carrier extend error indication.

NOTE—The ASCII for Table 40–1 and Table 40–2 is available from http://www.ieee802.org/3/publication/index.html.[8]

Table 40–1—Bit-to-symbol mapping (even subsets)

		$Sd_n[6:8]$ = [000]	$Sd_n[6:8]$ = [010]	$Sd_n[6:8]$ = [100]	$Sd_n[6:8]$ = [110]
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**
Normal	000000	0, 0, 0, 0	0, 0,+1,+1	0,+1,+1, 0	0,+1, 0,+1
Normal	000001	–2, 0, 0, 0	–2, 0,+1,+1	–2,+1,+1, 0	–2,+1, 0,+1
Normal	000010	0,–2, 0, 0	0,–2,+1,+1	0,–1,+1, 0	0,–1, 0,+1
Normal	000011	–2,–2, 0, 0	–2,–2,+1,+1	–2,–1,+1, 0	–2,–1, 0,+1
Normal	000100	0, 0,–2, 0	0, 0,–1,+1	0,+1,–1, 0	0,+1,–2,+1
Normal	000101	–2, 0,–2, 0	–2, 0,–1,+1	–2,+1,–1, 0	–2,+1,–2,+1
Normal	000110	0,–2,–2, 0	0,–2,–1,+1	0,–1,–1, 0	0,–1,–2,+1
Normal	000111	–2,–2,–2, 0	–2,–2,–1,+1	–2,–1,–1, 0	–2,–1,–2,+1
Normal	001000	0, 0, 0,–2	0, 0,+1,–1	0,+1,+1,–2	0,+1, 0,–1
Normal	001001	–2, 0, 0,–2	–2, 0,+1,–1	–2,+1,+1,–2	–2,+1, 0,–1
Normal	001010	0,–2, 0,–2	0,–2,+1,–1	0,–1,+1,–2	0,–1, 0,–1
Normal	001011	–2,–2, 0,–2	–2,–2,+1,–1	–2,–1,+1,–2	–2,–1, 0,–1
Normal	001100	0, 0,–2,–2	0, 0,–1,–1	0,+1,–1,–2	0,+1,–2,–1
Normal	001101	–2, 0,–2,–2	–2, 0,–1,–1	–2,+1,–1,–2	–2,+1,–2,–1
Normal	001110	0,–2,–2,–2	0,–2,–1,–1	0,–1,–1,–2	0,–1,–2,–1
Normal	001111	–2,–2,–2,–2	–2,–2,–1,–1	–2,–1,–1,–2	–2,–1,–2,–1
Normal	010000	+1,+1,+1,+1	+1,+1, 0, 0	+1, 0, 0,+1	+1, 0,+1, 0
Normal	010001	–1,+1,+1,+1	–1,+1, 0, 0	–1, 0, 0,+1	–1, 0,+1, 0
Normal	010010	+1,–1,+1,+1	+1,–1, 0, 0	+1,–2, 0,+1	+1,–2,+1, 0

[8]*Copyright release for symbol codes:* Users of this standard may freely reproduce the symbol codes in this subclause so it can be used for its intended purpose.

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Table 40–1—Bit-to-symbol mapping (even subsets) *(continued)*

		$Sd_n[6:8]$ = [000]	$Sd_n[6:8]$ = [010]	$Sd_n[6:8]$ = [100]	$Sd_n[6:8]$ = [110]
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**
Normal	010011	–1,–1,+1,+1	–1,–1, 0, 0	–1,–2, 0,+1	–1,–2,+1, 0
Normal	010100	+1,+1,–1,+1	+1,+1,–2, 0	+1, 0,–2,+1	+1, 0,–1, 0
Normal	010101	–1,+1,–1,+1	–1,+1,–2, 0	–1, 0,–2,+1	–1, 0,–1, 0
Normal	010110	+1,–1,–1,+1	+1,–1,–2, 0	+1,–2,–2,+1	+1,–2,–1, 0
Normal	010111	–1,–1,–1,+1	–1,–1,–2, 0	–1,–2,–2,+1	–1,–2,–1, 0
Normal	011000	+1,+1,+1,–1	+1,+1, 0,–2	+1, 0, 0,–1	+1, 0,+1,–2
Normal	011001	–1,+1,+1,–1	–1,+1, 0,–2	–1, 0, 0,–1	–1, 0,+1,–2
Normal	011010	+1,–1,+1,–1	+1,–1, 0,–2	+1,–2, 0,–1	+1,–2,+1,–2
Normal	011011	–1,–1,+1,–1	–1,–1, 0,–2	–1,–2, 0,–1	–1,–2,+1,–2
Normal	011100	+1,+1,–1,–1	+1,+1,–2,–2	+1, 0,–2,–1	+1, 0,–1,–2
Normal	011101	–1,+1,–1,–1	–1,+1,–2,–2	–1, 0,–2,–1	–1, 0,–1,–2
Normal	011110	+1,–1,–1,–1	+1,–1,–2,–2	+1,–2,–2,–1	+1,–2,–1,–2
Normal	011111	–1,–1,–1,–1	–1,–1,–2,–2	–1,–2,–2,–1	–1,–2,–1,–2
Normal	100000	+2, 0, 0, 0	+2, 0,+1,+1	+2,+1,+1, 0	+2,+1, 0,+1
Normal	100001	+2,–2, 0, 0	+2,–2,+1,+1	+2,–1,+1, 0	+2,–1, 0,+1
Normal	100010	+2, 0,–2, 0	+2, 0,–1,+1	+2,+1,–1, 0	+2,+1,–2,+1
Normal	100011	+2,–2,–2, 0	+2,–2,–1,+1	+2,–1,–1, 0	+2,–1,–2,+1
Normal	100100	+2, 0, 0,–2	+2, 0,+1,–1	+2,+1,+1,–2	+2,+1, 0,–1
Normal	100101	+2,–2, 0,–2	+2,–2,+1,–1	+2,–1,+1,–2	+2,–1, 0,–1
Normal	100110	+2, 0,–2,–2	+2, 0,–1,–1	+2,+1,–1,–2	+2,+1,–2,–1
Normal	100111	+2,–2,–2,–2	+2,–2,–1,–1	+2,–1,–1,–2	+2,–1,–2,–1
Normal	101000	0, 0,+2, 0	+1,+1,+2, 0	+1, 0,+2,+1	0,+1,+2,+1
Normal	101001	–2, 0,+2, 0	–1,+1,+2, 0	–1, 0,+2,+1	–2,+1,+2,+1
Normal	101010	0,–2,+2, 0	+1,–1,+2, 0	+1,–2,+2,+1	0,–1,+2,+1
Normal	101011	–2,–2,+2, 0	–1,–1,+2, 0	–1,–2,+2,+1	–2,–1,+2,+1
Normal	101100	0, 0,+2,–2	+1,+1,+2,–2	+1, 0,+2,–1	0,+1,+2,–1
Normal	101101	–2, 0,+2,–2	–1,+1,+2,–2	–1, 0,+2,–1	–2,+1,+2,–1
Normal	101110	0,–2,+2,–2	+1,–1,+2,–2	+1,–2,+2,–1	0,–1,+2,–1
Normal	101111	–2,–2,+2,–2	–1,–1,+2,–2	–1,–2,+2,–1	–2,–1,+2,–1
Normal	110000	0,+2, 0, 0	0,+2,+1,+1	+1,+2, 0,+1	+1,+2,+1, 0
Normal	110001	–2,+2, 0, 0	–2,+2,+1,+1	–1,+2, 0,+1	–1,+2,+1, 0

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Table 40–1—Bit-to-symbol mapping (even subsets) *(continued)*

		$Sd_n[6:8]$ = [000]	$Sd_n[6:8]$ = [010]	$Sd_n[6:8]$ = [100]	$Sd_n[6:8]$ = [110]
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**
Normal	110010	0,+2,–2, 0	0,+2,–1,+1	+1,+2,–2,+1	+1,+2,–1, 0
Normal	110011	–2,+2,–2, 0	–2,+2,–1,+1	–1,+2,–2,+1	–1,+2,–1, 0
Normal	110100	0,+2, 0,–2	0,+2,+1,–1	+1,+2, 0,–1	+1,+2,+1,–2
Normal	110101	–2,+2, 0,–2	–2,+2,+1,–1	–1,+2, 0,–1	–1,+2,+1,–2
Normal	110110	0,+2,–2,–2	0,+2,–1,–1	+1,+2,–2,–1	+1,+2,–1,–2
Normal	110111	–2,+2,–2,–2	–2,+2,–1,–1	–1,+2,–2,–1	–1,+2,–1,–2
Normal	111000	0, 0, 0,+2	+1,+1, 0,+2	0,+1,+1,+2	+1, 0,+1,+2
Normal	111001	–2, 0, 0,+2	–1,+1, 0,+2	–2,+1,+1,+2	–1, 0,+1,+2
Normal	111010	0,–2, 0,+2	+1,–1, 0,+2	0,–1,+1,+2	+1,–2,+1,+2
Normal	111011	–2,–2, 0,+2	–1,–1, 0,+2	–2,–1,+1,+2	–1,–2,+1,+2
Normal	111100	0, 0,–2,+2	+1,+1,–2,+2	0,+1,–1,+2	+1, 0,–1,+2
Normal	111101	–2, 0,–2,+2	–1,+1,–2,+2	–2,+1,–1,+2	–1, 0,–1,+2
Normal	111110	0,–2,–2,+2	+1,–1,–2,+2	0,–1,–1,+2	+1,–2,–1,+2
Normal	111111	–2,–2,–2,+2	–1,–1,–2,+2	–2,–1,–1,+2	–1,–2,–1,+2
xmt_err	XXXXXX	0,+2,+2,0	+1,+1,+2,+2	+2,+1,+1,+2	+2,+1,+2,+1
CSExtend_Err	XXXXXX	–2,+2,+2,–2	–1,–1,+2,+2	+2,–1,–1,+2	+2,–1,+2,–1
CSExtend	XXXXXX	+2, 0, 0,+2	+2,+2,+1,+1	+1,+2,+2,+1	+1,+2,+1,+2
CSReset	XXXXXX	+2,–2,–2,+2	+2,+2,–1,–1	–1,+2,+2,–1	–1,+2,–1,+2
SSD1	XXXXXX	+2,+2,+2,+2	—	—	—
SSD2	XXXXXX	+2,+2,+2,–2	—	—	—
ESD1	XXXXXX	+2,+2,+2,+2	—	—	—
ESD2_Ext_0	XXXXXX	+2,+2,+2,–2	—	—	—
ESD2_Ext_1	XXXXXX	+2,+2, –2,+2	—	—	—
ESD2_Ext_2	XXXXXX	+2,–2,+2,+2	—	—	—
ESD_Ext_Err	XXXXXX	–2,+2,+2,+2	—	—	—
Idle/Carrier Extension	000000	0, 0, 0, 0	—	—	—
Idle/Carrier Extension	000001	–2, 0, 0, 0	—	—	—
Idle/Carrier Extension	000010	0,–2, 0, 0	—	—	—

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Table 40–1—Bit-to-symbol mapping (even subsets) *(continued)*

		$Sd_n[6:8]$ = [000]	$Sd_n[6:8]$ = [010]	$Sd_n[6:8]$ = [100]	$Sd_n[6:8]$ = [110]
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**
Idle/Carrier Extension	000011	–2,–2,0,0	—	—	—
Idle/Carrier Extension	000100	0,0,–2,0	—	—	—
Idle/Carrier Extension	000101	–2,0,–2,0	—	—	—
Idle/Carrier Extension	000110	0,–2,–2,0	—	—	—
Idle/Carrier Extension	000111	–2,–2,–2,0	—	—	—
Idle/Carrier Extension	001000	0,0,0,–2	—	—	—
Idle/Carrier Extension	001001	–2,0,0,–2	—	—	—
Idle/Carrier Extension	001010	0,–2,0,–2	—	—	—
Idle/Carrier Extension	001011	–2,–2,0,–2	—	—	—
Idle/Carrier Extension	001100	0,0,–2,–2	—	—	—
Idle/Carrier Extension	001101	–2,0,–2,–2	—	—	—
Idle/Carrier Extension	001110	0,–2,–2,–2	—	—	—
Idle/Carrier Extension	001111	–2,–2,–2,–2	—	—	—

Table 40–2—Bit-to-symbol mapping (odd subsets)

		$Sd_n[6:8]$ = [001]	$Sd_n[6:8]$ = [011]	$Sd_n[6:8]$ = [101]	$Sd_n[6:8]$ = [111]
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**	**TA_n,TB_n,TC_n,TD_n**
Normal	000000	0,0,0,+1	0,0,+1,0	0,+1,+1,+1	0,+1,0,0
Normal	000001	–2,0,0,+1	–2,0,+1,0	–2,+1,+1,+1	–2,+1,0,0
Normal	000010	0,–2,0,+1	0,–2,+1,0	0,–1,+1,+1	0,–1,0,0
Normal	000011	–2,–2,0,+1	–2,–2,+1,0	–2,–1,+1,+1	–2,–1,0,0
Normal	000100	0,0,–2,+1	0,0,–1,0	0,+1,–1,+1	0,+1,–2,0

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Table 40–2—Bit-to-symbol mapping (odd subsets) *(continued)*

		$Sd_n[6:8]$ = [001]	$Sd_n[6:8]$ = [011]	$Sd_n[6:8]$ = [101]	$Sd_n[6:8]$ = [111]
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**
Normal	000101	–2, 0,–2,+1	–2, 0,–1, 0	–2,+1,–1,+1	–2,+1,–2, 0
Normal	000110	0,–2,–2,+1	0,–2,–1, 0	0,–1,–1,+1	0,–1,–2, 0
Normal	000111	–2,–2,–2,+1	–2,–2,–1, 0	–2,–1,–1,+1	–2,–1,–2, 0
Normal	001000	0, 0, 0,–1	0, 0,+1,–2	0,+1,+1,–1	0,+1, 0,–2
Normal	001001	–2, 0, 0,–1	–2, 0,+1,–2	–2,+1,+1,–1	–2,+1, 0,–2
Normal	001010	0,–2, 0,–1	0,–2,+1,–2	0,–1,+1,–1	0,–1, 0,–2
Normal	001011	–2,–2, 0,–1	–2,–2,+1,–2	–2,–1,+1,–1	–2,–1, 0,–2
Normal	001100	0, 0,–2,–1	0, 0,–1,–2	0,+1,–1,–1	0,+1,–2,–2
Normal	001101	–2, 0,–2,–1	–2, 0,–1,–2	–2,+1,–1,–1	–2,+1,–2,–2
Normal	001110	0,–2,–2,–1	0,–2,–1,–2	0,–1,–1,–1	0,–1,–2,–2
Normal	001111	–2,–2,–2,–1	–2,–2,–1,–2	–2,–1,–1,–1	–2,–1,–2,–2
Normal	010000	+1,+1,+1, 0	+1,+1, 0,+1	+1, 0, 0, 0	+1, 0,+1,+1
Normal	010001	–1,+1,+1, 0	–1,+1, 0,+1	–1, 0, 0, 0	–1, 0,+1,+1
Normal	010010	+1,–1,+1, 0	+1,–1, 0,+1	+1,–2, 0, 0	+1,–2,+1,+1
Normal	010011	–1,–1,+1, 0	–1,–1, 0,+1	–1,–2, 0, 0	–1,–2,+1,+1
Normal	010100	+1,+1,–1, 0	+1,+1,–2,+1	+1, 0,–2, 0	+1, 0,–1,+1
Normal	010101	–1,+1,–1, 0	–1,+1,–2,+1	–1, 0,–2, 0	–1, 0,–1,+1
Normal	010110	+1,–1,–1, 0	+1,–1,–2,+1	+1,–2,–2, 0	+1,–2,–1,+1
Normal	010111	–1,–1,–1, 0	–1,–1,–2,+1	–1,–2,–2, 0	–1,–2,–1,+1
Normal	011000	+1,+1,+1,–2	+1,+1, 0,–1	+1, 0, 0,–2	+1, 0,+1,–1
Normal	011001	–1,+1,+1,–2	–1,+1, 0,–1	–1, 0, 0,–2	–1, 0,+1,–1
Normal	011010	+1,–1,+1,–2	+1,–1, 0,–1	+1,–2, 0,–2	+1,–2,+1,–1
Normal	011011	–1,–1,+1,–2	–1,–1, 0,–1	–1,–2, 0,–2	–1,–2,+1,–1
Normal	011100	+1,+1,–1,–2	+1,+1,–2,–1	+1, 0,–2,–2	+1, 0,–1,–1
Normal	011101	–1,+1,–1,–2	–1,+1,–2,–1	–1, 0,–2,–2	–1, 0,–1,–1
Normal	011110	+1,–1,–1,–2	+1,–1,–2,–1	+1,–2,–2,–2	+1,–2,–1,–1
Normal	011111	–1,–1,–1,–2	–1,–1,–2,–1	–1,–2,–2,–2	–1,–2,–1,–1
Normal	100000	+2, 0, 0,+1	+2, 0,+1, 0	+2,+1,+1,+1	+2,+1, 0, 0
Normal	100001	+2,–2, 0,+1	+2,–2,+1, 0	+2,–1,+1,+1	+2,–1, 0, 0
Normal	100010	+2, 0,–2,+1	+2, 0,–1, 0	+2,+1,–1,+1	+2,+1,–2, 0

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Table 40–2—Bit-to-symbol mapping (odd subsets) *(continued)*

		$Sd_n[6:8]$ = [001]	$Sd_n[6:8]$ = [011]	$Sd_n[6:8]$ = [101]	$Sd_n[6:8]$ = [111]
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**
Normal	100011	+2,–2,–2,+1	+2,–2,–1, 0	+2,–1,–1,+1	+2,–1,–2, 0
Normal	100100	+2, 0, 0,–1	+2, 0,+1,–2	+2,+1,+1,–1	+2,+1, 0,–2
Normal	100101	+2,–2, 0,–1	+2,–2,+1,–2	+2,–1,+1,–1	+2,–1, 0,–2
Normal	100110	+2, 0,–2,–1	+2, 0,–1,–2	+2,+1,–1,–1	+2,+1,–2,–2
Normal	100111	+2,–2,–2,–1	+2,–2,–1,–2	+2,–1,–1,–1	+2,–1,–2,–2
Normal	101000	0, 0,+2,+1	+1,+1,+2,+1	+1, 0,+2, 0	0,+1,+2, 0
Normal	101001	–2, 0,+2,+1	–1,+1,+2,+1	–1, 0,+2, 0	–2,+1,+2, 0
Normal	101010	0,–2,+2,+1	+1,–1,+2,+1	+1,–2,+2, 0	0,–1,+2, 0
Normal	101011	–2,–2,+2,+1	–1,–1,+2,+1	–1,–2,+2, 0	–2,–1,+2, 0
Normal	101100	0, 0,+2,–1	+1,+1,+2,–1	+1, 0,+2,–2	0,+1,+2,–2
Normal	101101	–2, 0,+2,–1	–1,+1,+2,–1	–1, 0,+2,–2	–2,+1,+2,–2
Normal	101110	0,–2,+2,–1	+1,–1,+2,–1	+1,–2,+2,–2	0,–1,+2,–2
Normal	101111	–2,–2,+2,–1	–1,–1,+2,–1	–1,–2,+2,–2	–2,–1,+2,–2
Normal	110000	0,+2, 0,+1	0,+2,+1, 0	+1,+2, 0, 0	+1,+2,+1,+1
Normal	110001	–2,+2, 0,+1	–2,+2,+1, 0	–1,+2, 0, 0	–1,+2,+1,+1
Normal	110010	0,+2,–2,+1	0,+2,–1, 0	+1,+2,–2, 0	+1,+2,–1,+1
Normal	110011	–2,+2,–2,+1	–2,+2,–1, 0	–1,+2,–2, 0	–1,+2,–1,+1
Normal	110100	0,+2, 0,–1	0,+2,+1,–2	+1,+2, 0,–2	+1,+2,+1,–1
Normal	110101	–2,+2, 0,–1	–2,+2,+1,–2	–1,+2, 0,–2	–1,+2,+1,–1
Normal	110110	0,+2,–2,–1	0,+2,–1,–2	+1,+2,–2,–2	+1,+2,–1,–1
Normal	110111	–2,+2,–2,–1	–2,+2,–1,–2	–1,+2,–2,–2	–1,+2,–1,–1
Normal	111000	+1,+1,+1,+2	0, 0,+1,+2	+1, 0, 0,+2	0,+1, 0,+2
Normal	111001	–1,+1,+1,+2	–2, 0,+1,+2	–1, 0, 0,+2	–2,+1, 0,+2
Normal	111010	+1,–1,+1,+2	0,–2,+1,+2	+1,–2, 0,+2	0,–1, 0,+2
Normal	111011	–1,–1,+1,+2	–2,–2,+1,+2	–1,–2, 0,+2	–2,–1, 0,+2
Normal	111100	+1,+1,–1,+2	0, 0,–1,+2	+1, 0,–2,+2	0,+1,–2,+2
Normal	111101	–1,+1,–1,+2	–2, 0,–1,+2	–1, 0,–2,+2	–2,+1,–2,+2
Normal	111110	+1,–1,–1,+2	0,–2,–1,+2	+1,–2,–2,+2	0,–1,–2,+2
Normal	111111	–1,–1,–1,+2	–2,–2,–1,+2	–1,–2,–2,+2	–2,–1,–2,+2
xmt_err	XXXXXX	+2,+2, 0,+1	0,+2,+1,+2	+1,+2,+2, 0	+2,+1,+2, 0

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Table 40–2—Bit-to-symbol mapping (odd subsets) *(continued)*

		$Sd_n[6:8]$ = [001]	$Sd_n[6:8]$ = [011]	$Sd_n[6:8]$ = [101]	$Sd_n[6:8]$ = [111]
Condition	**$Sd_n[5:0]$**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**	**TA_n,TB_n,TC_n, TD_n**
CSExtend_Err	XXXXXX	+2,+2, –2,–1	–2,+2,–1,+2	–1,+2,+2,–2	+2,–1,+2,–2
CSExtend	XXXXXX	+2, 0,+2,+1	+2, 0,+1,+2	+1, 0,+2,+2	+2,+1, 0,+2
CSReset	XXXXXX	+2,–2,+2,–1	+2,–2,–1,+2	–1,–2,+2,+2	+2,–1,–2,+2

40.3.1.3.6 Generation of A_n, B_n, C_n, D_n

The four bits $Sg_n[3:0]$ are used to randomize the signs of the quinary symbols (A_n, B_n, C_n, D_n) so that each symbol stream has no dc bias. The bits are used to generate binary symbols (SnA_n, SnB_n, SnC_n, SnD_n) that, when multiplied by the quinary symbols (TA_n, TB_n, TC_n, TD_n), result in (A_n, B_n, C_n, D_n).

PCS Transmit ensures a distinction between code-groups transmitted during idle mode plus SSD and those transmitted during other symbol periods. This distinction is accomplished by reversing the mapping of the sign bits when the condition (tx_enable_{n-2} + tx_enable_{n-4}) = 1. This sign reversal is controlled by the variable $Srev_n$ defined as

$$Srev_n = tx\_enable_{n-2} + tx\_enable_{n-4}$$

The binary symbols SnA_n, SnB_n, SnC_n, and SnD_n are defined using $Sg_n[3:0]$ as

$$SnA_n = \begin{cases} +1 \text{ if } [(Sg_n[0] \wedge Srev_n) = 0] \\ -1 \text{ else} \end{cases}$$

$$SnB_n = \begin{cases} +1 \text{ if } [(Sg_n[1] \wedge Srev_n) = 0] \\ -1 \text{ else} \end{cases}$$

$$SnC_n = \begin{cases} +1 \text{ if } [(Sg_n[2] \wedge Srev_n) = 0] \\ -1 \text{ else} \end{cases}$$

$$SnD_n = \begin{cases} +1 \text{ if } [(Sg_n[3] \wedge Srev_n) = 0] \\ -1 \text{ else} \end{cases}$$

The quinary symbols (A_n, B_n, C_n, D_n) are generated as the product of (SnA_n, SnB_n, SnC_n, SnD_n) and (TA_n, TB_n, TC_n, TD_n) respectively.

$$A_n = TA_n \times SnA_n$$

$$B_n = TB_n \times SnB_n$$

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$$C_n = TC_n \times SnC_n$$

$$D_n = TD_n \times SnD_n$$

40.3.1.4 PCS Receive function

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 40–10a including compliance with the associated state variables as specified in 40.3.3.

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb_vector. To achieve correct operation, PCS Receive uses the knowledge of the encoding rules that are employed in the idle mode. PCS Receive generates the sequence of vectors of four quinary symbols (RA_n, RB_n, RC_n, RD_n) and indicates the reliable acquisition of the descrambler state by setting the parameter scr_status to OK. The sequence (RA_n, RB_n, RC_n, RD_n) is processed to generate the signals RXD<7:0>, RX_DV, and RX_ER, which are presented to the GMII. PCS Receive detects the transmission of a stream of data from the remote station and conveys this information to the PCS Carrier Sense and PCS Transmit functions via the parameter 1000BTreceive.

40.3.1.4.1 Decoding of code-groups

When the PMA indicates that correct receiver operation has been achieved by setting the loc_rcvr_status parameter to the value OK, the PCS Receive continuously checks that the received sequence satisfies the encoding rule used in idle mode. When a violation is detected, PCS Receive assigns the value TRUE to the parameter 1000BTreceive and, by examining the last two received vectors (RA_{n-1}, RB_{n-1}, RC_{n-1}, RD_{n-1}) and (RA_n, RB_n, RC_n, RD_n), determines whether the violation is due to reception of SSD or to a receiver error.

Upon detection of SSD, PCS Receive also assigns the value TRUE to the parameter 1000BTreceive that is provided to the PCS Carrier Sense and Collision Presence functions. During the two symbol periods corresponding to SSD, PCS Receive replaces SSD by preamble bits. Upon the detection of SSD, the signal RX_DV is asserted and each received vector is decoded into a data octet RXD<7:0> until ESD is detected.

Upon detection of a receiver error, the signal RX_ER is asserted and the parameter rxerror_status assumes the value ERROR. De-assertion of RX_ER and transition to the IDLE state (rxerror_status=NO_ERROR) takes place upon detection of four consecutive vectors satisfying the encoding rule used in idle mode.

During reception of a stream of data, PCS Receive checks that the symbols RA_n, RB_n, RC_n, RD_n follow the encoding rule defined in 40.3.1.3.5 for ESD whenever they assume values ± 2. PCS Receive processes two consecutive vectors at each time n to detect ESD. Upon detection of ESD, PCS Receive de-asserts the signal RX_DV on the GMII. If the last symbol period of ESD indicates that a carrier extension is present, PCS Receive will assert the RX_ER signal on the GMII. If no extension is indicated in the ESD2 quartet, PCS Receive assigns the value FALSE to the parameter receiving. If an extension is present, the transition to the IDLE state occurs after detection of a valid idle symbol period and the parameter receiving remains TRUE until check_idle is TRUE. If a violation of the encoding rules is detected, PCS Receive asserts the signal RX_ER for at least one symbol period.

A premature stream termination is caused by the detection of invalid symbols during the reception of a data stream. Then, PCS Receive waits for the reception of four consecutive vectors satisfying the encoding rule used in idle mode prior to de-asserting the error indication. Note that RX_DV remains asserted during the symbol periods corresponding to the first three idle vectors, while RX_ER=TRUE is signaled on the GMII. The signal RX_ER is also asserted in the LINK FAILED state, which ensures that RX_ER remains asserted for at least one symbol period.

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40.3.1.4.2 Receiver descrambler polynomials

The PHY shall descramble the data stream and return the proper sequence of code-groups to the decoding process for generation of RXD<7:0> to the GMII. For side-stream descrambling, the MASTER PHY shall employ the receiver descrambler generator polynomial $g'_M(x) = 1 + x^{20} + x^{33}$ and the SLAVE PHY shall employ the receiver descrambler generator polynomial $g'_S(x) = 1 + x^{13} + x^{33}$.

40.3.1.5 PCS Carrier Sense function

The PCS Carrier Sense function generates the GMII signal CRS, which the MAC uses for deferral in half duplex mode. The PCS shall conform to the Carrier Sense state diagram as depicted in Figure 40–11 including compliance with the associated state variables as specified in 40.3.3. The PCS Carrier Sense function is not required in a 1000BASE-T PHY that does not support half duplex operation.

40.3.2 Stream structure

The tx_symb_vector and rx-symb_vector structure is shown in Figure 40–7.

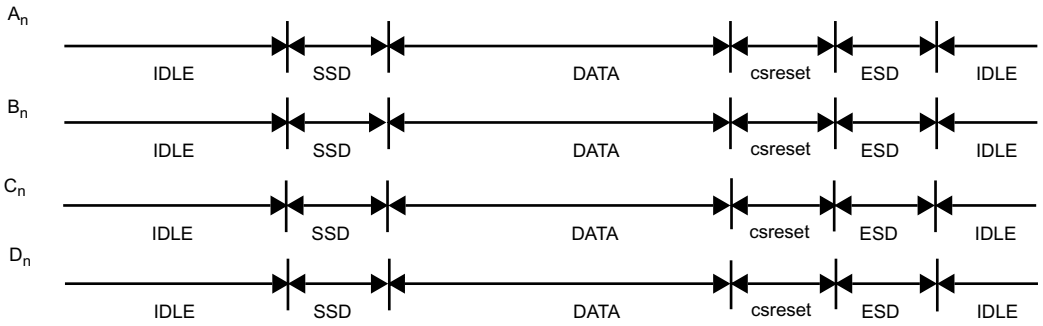


Figure 40–7—The tx_symb_vector and rx-symb_vector structure

40.3.3 State variables

40.3.3.1 Variables

CEXT

A vector of four quinary symbols corresponding to the code-group generated in idle mode to denote carrier extension, as specified in 40.3.1.3.

CEXT_Err

A vector of four quinary symbols corresponding to the code-group generated in idle mode to denote carrier extension with error indication, as specified in 40.3.1.3.

COL

The COL signal of the GMII as specified in 35.2.2.10.

config

The config parameter set by PMA and passed to the PCS via the PMA_CONFIG.indicate primitive.
Values: MASTER, SLAVE.

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CRS

The CRS signal of the GMII as specified in 35.2.2.9.

CSExtend

A vector of four quinary symbols corresponding to the code-group indicating convolutional encoder reset condition during carrier extension, as specified in 40.3.1.3.

CSExtend_Err

A vector of four quinary symbols corresponding to the code-group indicating convolutional encoder reset condition during carrier extension with error indication, as specified in 40.3.1.3.

CSReset

A vector of four quinary symbols corresponding to the code-group indicating convolutional encoder reset condition in the absence of carrier extension, as specified in 40.3.1.3.

DATA

A vector of four quinary symbols corresponding to the code-group indicating valid data, as specified in 40.3.1.3.

ESD1

A vector of four quinary symbols corresponding to the first code-group of End-of-Stream delimiter, as specified in 40.3.1.3.

ESD2_Ext_0

A vector of four quinary symbols corresponding to the second code-group of End-of-Stream delimiter in the absence of carrier extension over the two ESD symbol periods, as specified in 40.3.1.3.

ESD2_Ext_1

A vector of four quinary symbols corresponding to the second code-group of End-of-Stream delimiter when carrier extension is indicated during the first symbol period of the End-of-Stream delimiter, but not during the second symbol period, as specified in 40.3.1.3.

ESD2_Ext_2

A vector of four quinary symbols corresponding to the second code-group of End-of-Stream delimiter when carrier extension is indicated during the two symbol periods of the End-of-Stream delimiter, as specified in 40.3.1.3.

ESD_Ext_Err

A vector of four quinary symbols corresponding to either the first or second code-group of End-of-Stream delimiter when carrier extension with error is indicated during the End-of-Stream delimiter, as specified in 40.3.1.3.

IDLE

A sequence of vectors of four quinary symbols representing the special code-group generated in idle mode in the absence of carrier extension or carrier extension with error indication, as specified in 40.3.1.3.

link_status

The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indicate primitive.
Values: OK or FAIL

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loc_rcvr_status
: The loc_rcvr_status parameter set by the PMA Receive function and passed to the PCS via the PMA_RXSTATUS.indicate primitive.
Values: OK or NOT_OK

pcs_reset
: The pcs_reset parameter set by the PCS Reset function.
Values: ON or OFF

(RA_n, RB_n, RC_n, RD_n)
: The vector of the four correctly aligned most recently received quinary symbols generated by PCS Receive at time n.

1000BTreceive
: The receiving parameter generated by the PCS Receive function.
Values: TRUE or FALSE

rem_rcvr_status
: The rem_rcvr_status parameter generated by PCS Receive.
Values: OK or NOT_OK

repeater_mode
: See 36.2.5.1.3

Rx_n
: Alias for rx_symb_vector (a vector RA_n, RB_n, RC_n, RD_n) at time n.

rxerror_status
: The rxerror_status parameter set by the PCS Receive function.
Values: ERROR or NO_ERROR

RX_DV
: The RX_DV signal of the GMII as specified in 35.2.2.6.

RX_ER
: The RX_ER signal of the GMII as specified in 35.2.2.8.

rx_symb_vector
: A vector of four quinary symbols received by the PMA and passed to the PCS via the PMA_UNITDATA.indicate primitive.
Value: SYMB_4D

RXD[7:0]
: The RXD<7:0> signal of the GMII as specified in 35.2.2.7.

SSD1
: A vector of four quinary symbols corresponding to the first code-group of the Start-of-Stream delimiter, as specified in 40.3.1.3.5.

SSD2
: A vector of four quinary symbols corresponding to the second code-group of the Start-of-Stream delimiter, as specified in 40.3.1.3.5.

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1000BTtransmit
: A boolean used by the PCS Transmit Process to indicate whether a frame transmission is in progress. Used by Carrier Sense process.
Values: TRUE: The PCS is transmitting a stream
FALSE: The PCS is not transmitting a stream

TXD[7:0]
: The TXD<7:0> signal of the GMII as specified in 35.2.2.4.

tx_enable
: The tx_enable parameter generated by PCS Transmit as specified in Figure 40–8.
Values: TRUE or FALSE

tx_error
: The tx_error parameter generated by PCS Transmit as specified in Figure 40–8.
Values: TRUE or FALSE

TX_EN
: The TX_EN signal of the GMII as specified in 35.2.2.3.

TX_ER
: The TX_ER signal of the GMII as specified in 35.2.2.5.

tx_mode
: The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indicate primitive.
Values: SEND_Z, SEND_N, or SEND_I

Tx_n
: Alias for tx_symb_vector at time n.

tx_symb_vector
: A vector of four quinary symbols generated by the PCS Transmit function and passed to the PMA via the PMA_UNITDATA.request primitive.
Value: SYMB_4D

xmt_err
: A vector of four quinary symbols corresponding to a transmit error indication during normal data transmission or reception, as specified in 40.3.1.3.

40.3.3.2 Functions

check_end
: A function used by the PCS Receive process to detect the reception of valid ESD symbols. The check_end function operates on the next two rx_symb_vectors, (Rx_{n+1}) and (Rx_{n+2}), available via PMA_UNITDATA.indicate, and returns a boolean value indicating whether these two consecutive vectors contain symbols corresponding to a legal ESD encoding or not, as specified in 40.3.1.3.

check_idle
: A function used by the PCS Receive process to detect the reception of valid idle code-groups after an error condition during the process. The check_idle function operates on the current rx_symb_vector and the next three rx_symb_vectors available via PMA_UNITDATA.indicate and returns a boolean value indicating whether the four consecutive vectors contain symbols corresponding to the idle mode encoding or not, as specified in 40.3.1.3.

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DECODE

In the PCS Receive process, this function takes as its argument the value of rx_symb_vector and returns the corresponding GMII RXD<7:0> octet. DECODE follows the rules outlined in 40.2.6.1.

ENCODE

In the PCS Transmit process, this function takes as its argument GMII TXD <7:0> and returns the corresponding tx_symb_vector. ENCODE follows the rules outlined in 40.2.5.1.

40.3.3.3 Timer

symb_timer

Continuous timer: The condition symb_timer_done becomes true upon timer expiration.

Restart time: Immediately after expiration; timer restart resets the condition symb_timer_done.

Duration: 8 ns nominal. (See clock tolerance in 40.6.1.2.6.)

Symb-timer shall be generated synchronously with TX_TCLK. In the PCS Transmit state diagram, the message PMA_UNITDATA.request is issued concurrently with symb_timer_done.

40.3.3.4 Messages

PMA_UNITDATA.indicate (rx_symb_vector)

A signal sent by PMA Receive indicating that a vector of four quinary symbols is available in rx_symb_vector. (See 40.2.6.)

PMA_UNITDATA.request (tx_symb_vector)

A signal sent to PMA Transmit indicating that a vector of four quinary symbols is available in tx_symb_vector. (See 40.2.5.)

PUDI

Alias for PMA_UNITDATA.indicate (rx_symb_vector).

PUDR

Alias for PMA_UNITDATA.request (tx_symb_vector).

STD

Alias for symb_timer_done.

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40.3.4 State diagrams

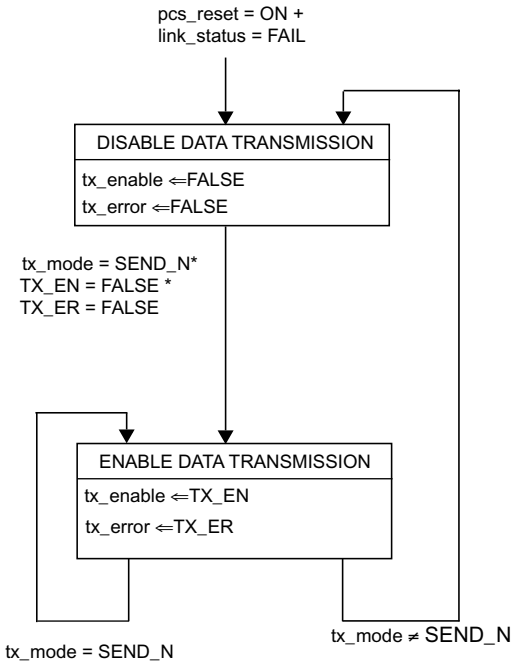


Figure 40–8—PCS Data Transmission Enabling state diagram

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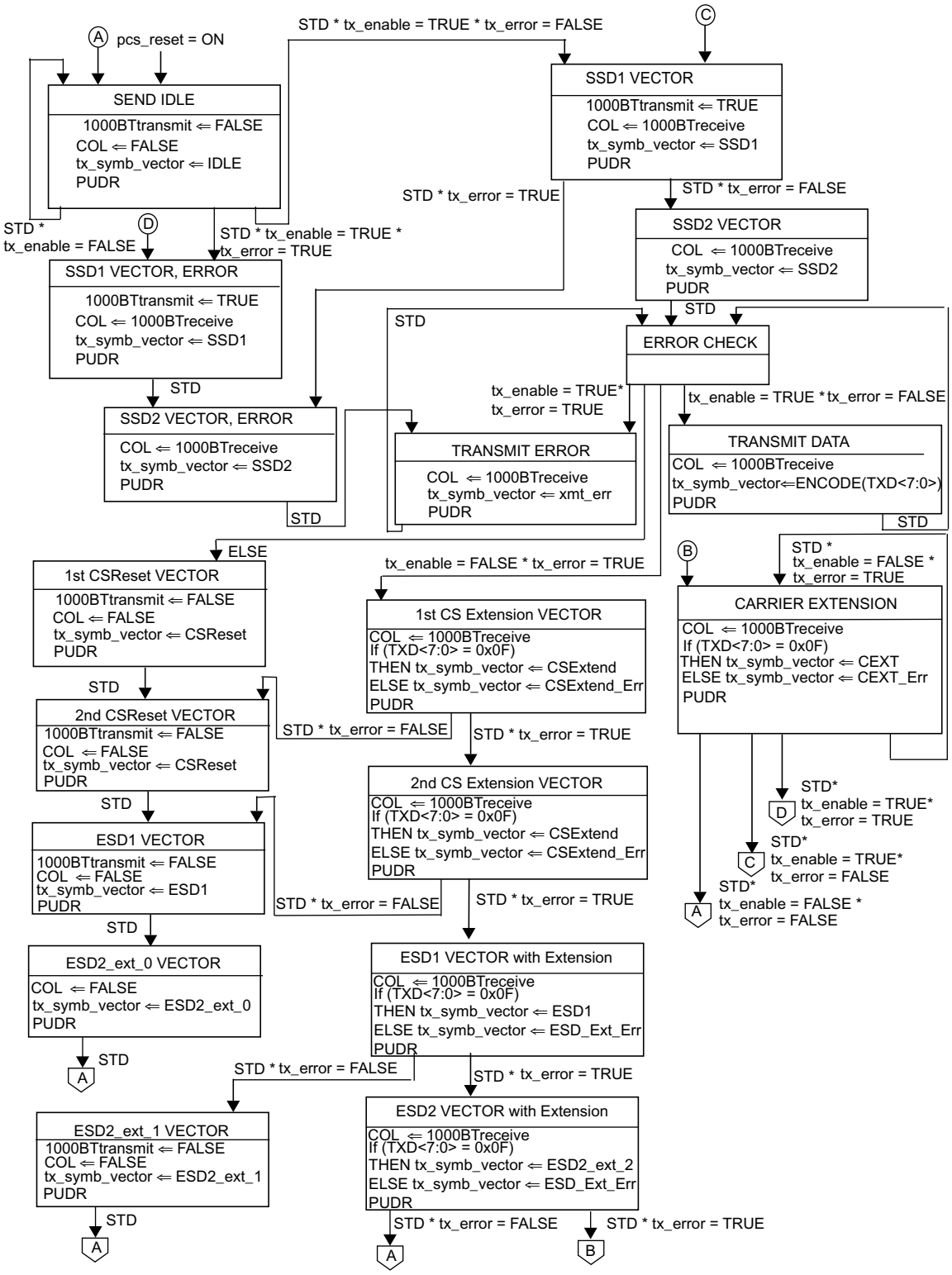


Figure 40–9—PCS Transmit state diagram

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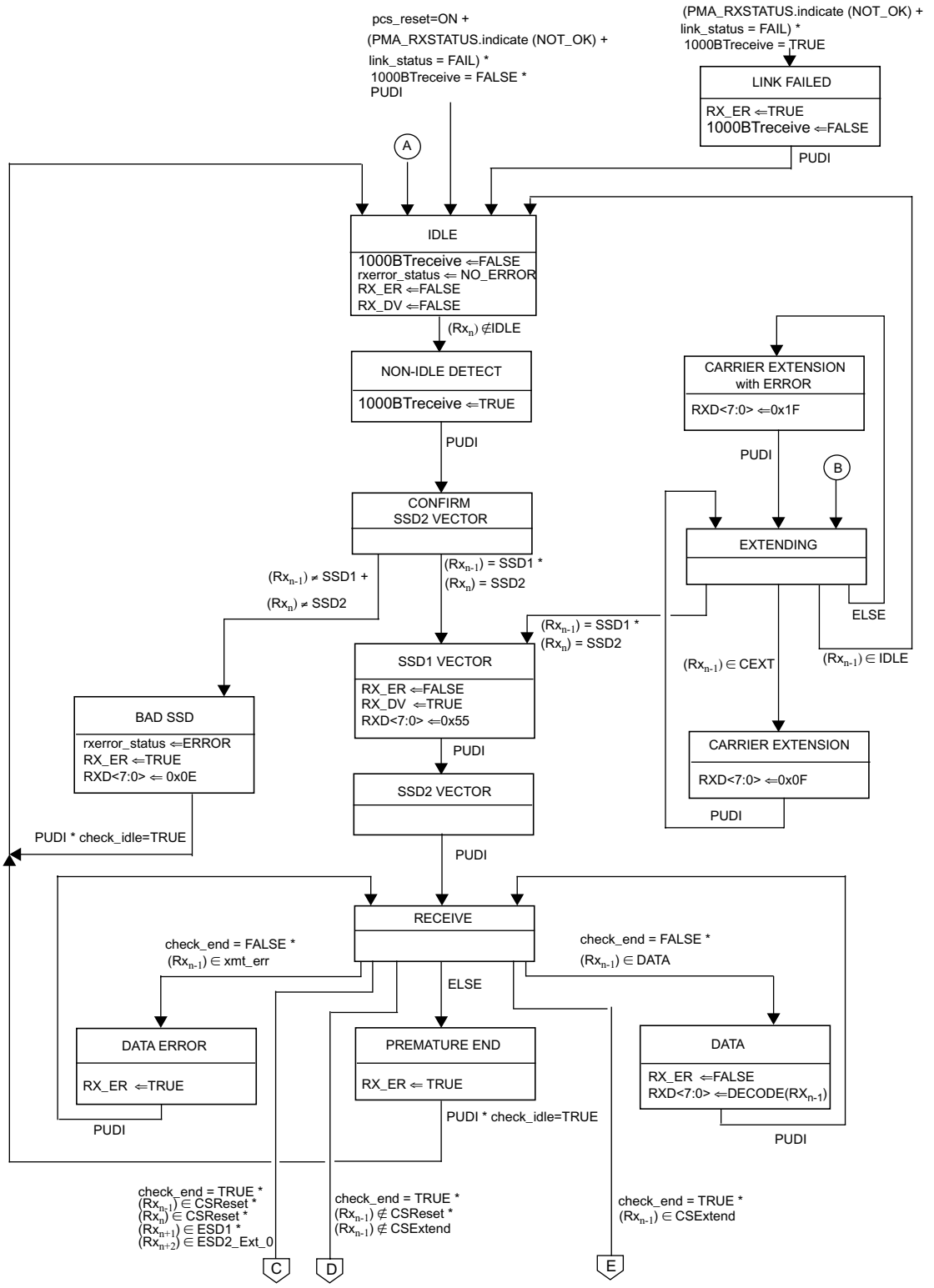


Figure 40–10a—PCS Receive state diagram, part a

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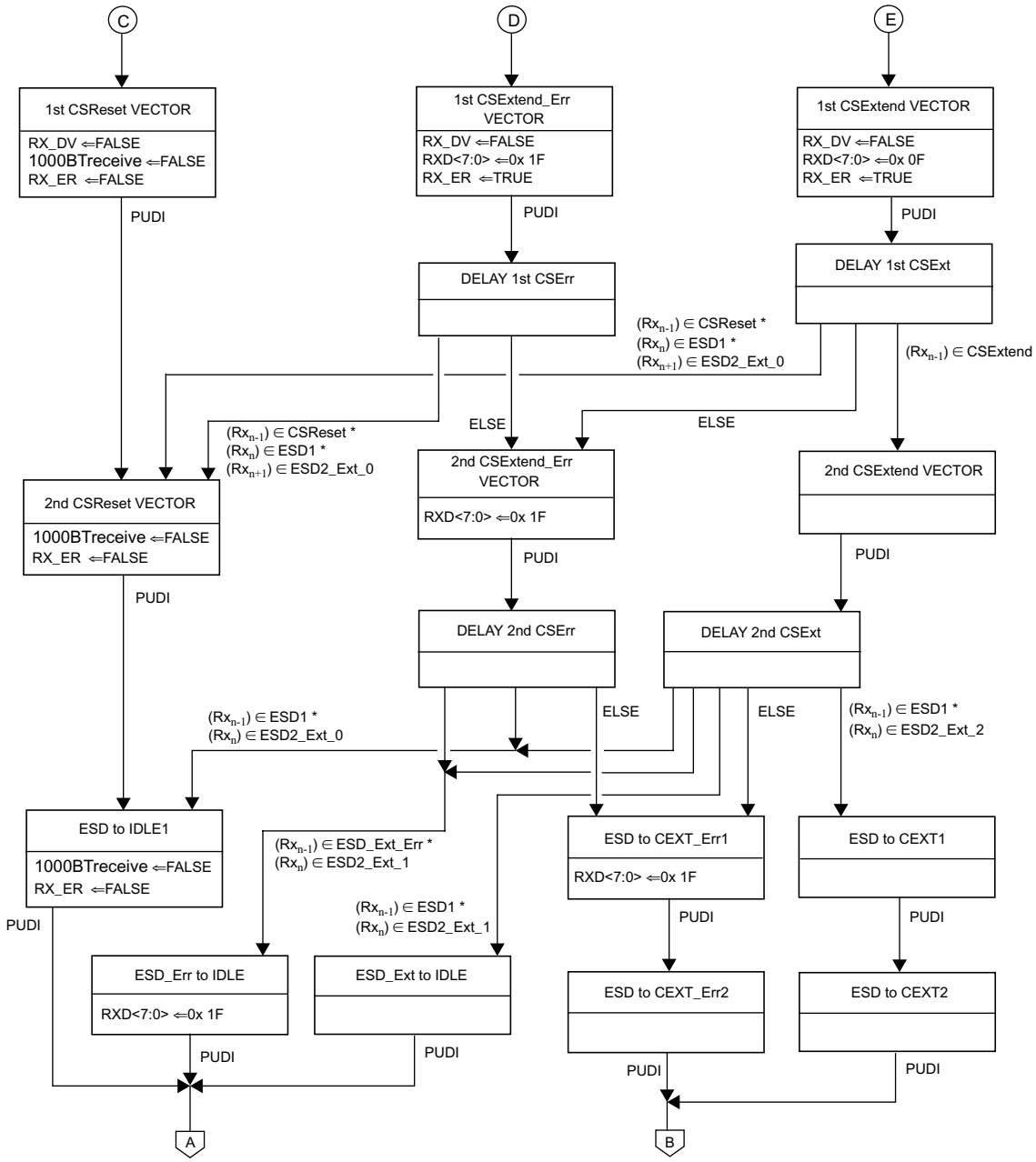


Figure 40–10b—PCS Receive state diagram, part b

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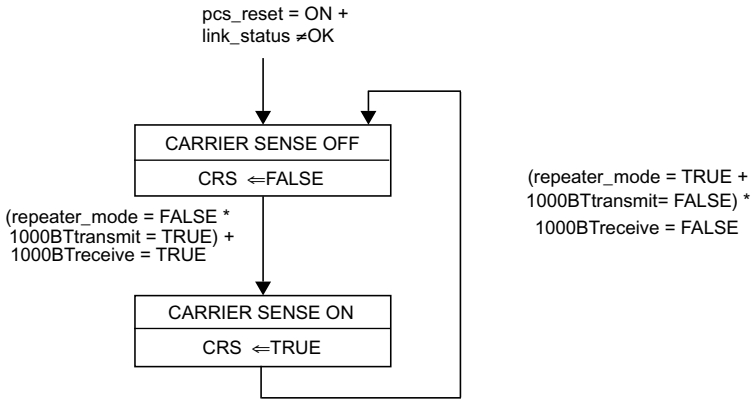


Figure 40–11—PCS Carrier Sense state diagram

40.3.4.1 Supplement to state diagram

Figure 40–12 reiterates the information shown in Figure 40–9 in timing diagram format. It is informative only. Time proceeds from left to right in the figure.

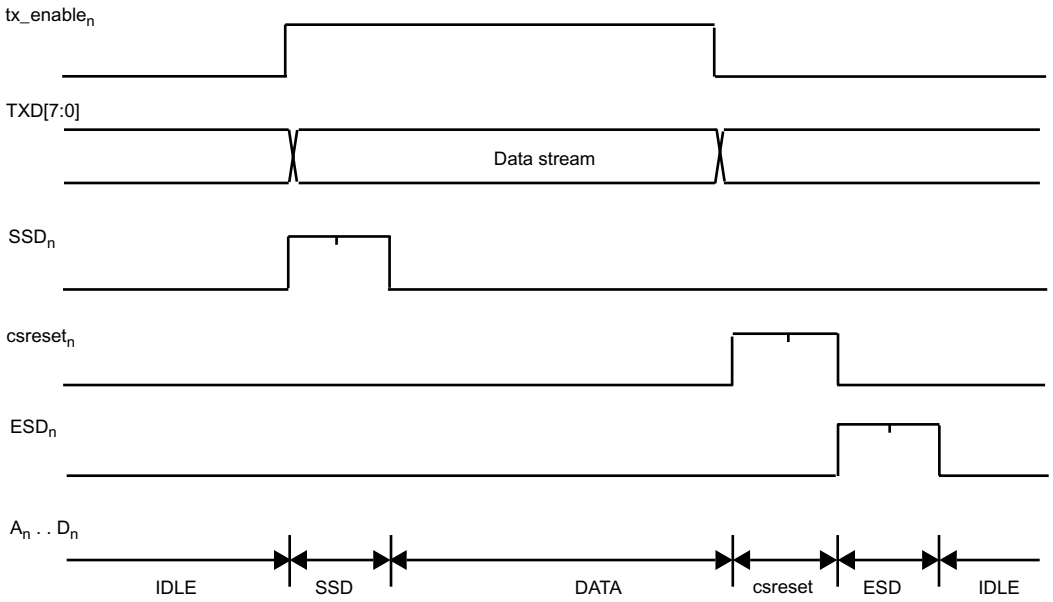


Figure 40–12—PCS sublayer to PMA timing

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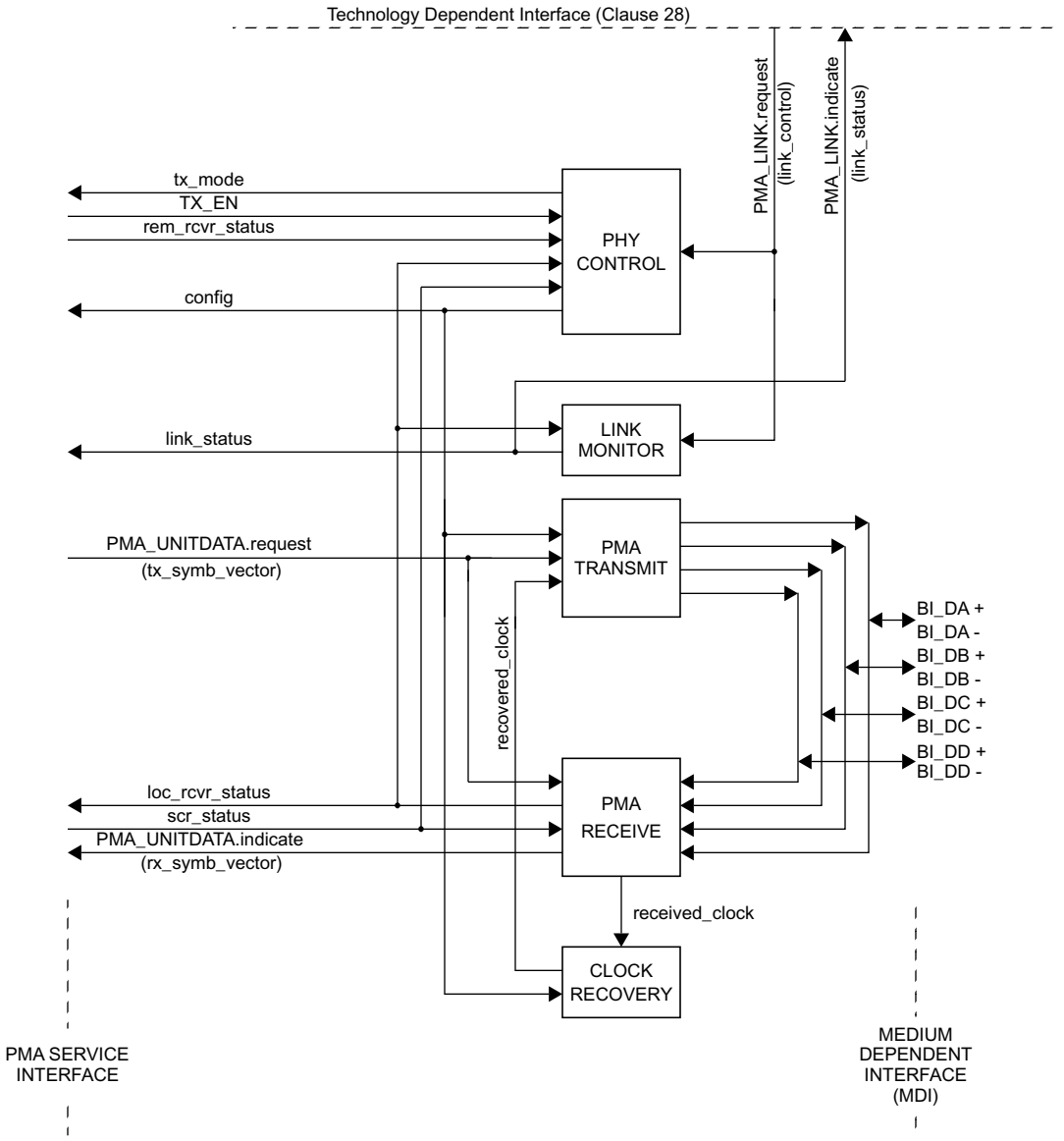
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40.4 Physical Medium Attachment (PMA) sublayer

40.4.1 PMA functional specifications

The PMA couples messages from a PMA service interface specified in 40.2.2 to the 1000BASE-T baseband medium, specified in 40.7.

The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 40.8.



NOTE The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

Figure 40–13—PMA reference diagram

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40.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure 40–13, shows how the operating functions relate to the messages of the PMA Service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 40–13. The management interface and its functions are specified in Clause 22.

40.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power on (see 36.2.5.1.3)
b) The receipt of a request for reset from the management entity

PMA Reset sets pcs_reset=ON while any of the above reset conditions hold true. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

40.4.2.2 PMA Transmit function

The PMA Transmit function comprises four synchronous transmitters to generate four 5-level pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. PMA Transmit shall continuously transmit onto the MDI pulses modulated by the quinary symbols given by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC] and tx_symb_vector[BI_DD], respectively. The four transmitters shall be driven by the same transmit clock, TX_TCLK. The signals generated by PMA Transmit shall follow the mathematical description given in 40.4.3.1, and shall comply with the electrical specifications given in 40.6.

When the PMA_CONFIG.indicate parameter config is MASTER, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 40.6.1.2.5. When the PMA_CONFIG.indicate parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 40.4.2.6 while meeting the jitter requirements of 40.6.1.2.5.

40.4.2.3 PMA Receive function

The PMA Receive function comprises four independent receivers for quinary pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. PMA Receive contains the circuits necessary to both detect quinary symbol sequences from the signals received at the MDI over receive pairs BI_DA, BI_DB, BI_DC, and BI_DD and to present these sequences to the PCS Receive function. The signals received at the MDI are described mathematically in 40.4.3.2. The PMA shall translate the signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DB into the PMA_UNITDATA.indicate parameter rx_symb_vector with a symbol error rate of less than 10^{-10} over a channel meeting the requirements of 40.7.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization, echo and crosstalk cancellation, and sequence estimation. The sequence of code-groups assigned to tx_symb_vector is needed to perform echo and self near-end crosstalk cancellation.

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The PMA Receive function uses the scr_status parameter and the state of the equalization, cancellation, and estimation functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The precise algorithm for generation of loc_rcvr_status is implementation dependent.

40.4.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 40–15.

During Auto-Negotiation PHY Control is in the DISABLE 1000BASE-T TRANSMITTER state and the transmitters are disabled. When the Auto-Negotiation process asserts link_control=ENABLE, PHY Control enters the SLAVE SILENT state. Upon entering this state, the maxwait timer is started and PHY Control forces transmission of zeros by setting tx_mode=SEND_Z. The transition out of the SLAVE SILENT state depends on whether the PHY is operating in MASTER or SLAVE mode. In MASTER mode, PHY Control transitions immediately to the TRAINING state. In SLAVE mode, PHY Control transitions to the TRAINING state only after the SLAVE PHY converges its decision feedback equilizer (DFE), acquires timing, and acquires its descrambler state, and sets scr_status=OK.

For the SLAVE PHY, the final convergence of the adaptive filter parameters is completed in the TRAINING state. The MASTER PHY performs all its receiver convergence functions in the TRAINING state. Upon entering the TRAINING state, the minwait_timer is started and PHY Control forces transmission into the idle mode by asserting tx_mode=SEND_I. After the PHY completes successful training and establishes proper receiver operations, PCS Transmit conveys this information to the link partner via transmission of the parameter loc_rcvr_status. (See Sd_n[2] in 40.3.1.3.4.) The link partner's value for loc_rcvr_status is stored in the local device parameter rem_rcvr status. When the minwait_timer expires and the condition loc_rcvr_status=OK is satisfied, PHY Control transitions into either the SEND IDLE OR DATA state if rem_rcvr_status=OK or the SEND IDLE state if rem_rcvr_status=NOT_OK. On entry into either the SEND IDLE or SEND IDLE OR DATA states, the maxwait_timer is stopped and the minwait_timer is started.

The normal mode of operation corresponds to the SEND IDLE OR DATA state, where PHY Control asserts tx_mode=SEND_N and transmission of data over the link can take place. In this state, when no frames have to be sent, idle transmission takes place.

If unsatisfactory receiver operation is detected in the SEND IDLE OR DATA or SEND IDLE states (loc_rcvr_status=NOT_OK) and the minwait_timer has expired, transmission of the current frame is completed and PHY Control enters the SLAVE SILENT state. In the SEND IDLE OR DATA state, whenever a PHY that operates reliably detects unsatisfactory operation of the remote PHY (rem_rcvr_status=NOT_OK) and the minwait_timer has expired, it enters the SEND IDLE state where tx_mode=SEND_I is asserted and idle transmission takes place. In this state, encoding is performed with the parameter loc_rcvr_status=OK. As soon as the remote PHY signals satisfactory receiver operation (rem_rcvr_status=OK) and the minwait_timer has expired, the SEND IDLE OR DATA state is entered.

PHY Control may force the transmit scrambler state to be initialized to an arbitrary value by requesting the execution of the PCS Reset function defined in 40.3.1.1.

40.4.2.5 Link Monitor function

Link Monitor determines the status of the underlying receive channel and communicates it via the variable link_status. Failure of the underlying receive channel typically causes the PMA's clients to suspend normal operation.

The Link Monitor function shall comply with the state diagram of Figure 40–16.

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Upon power on, reset, or release from power down, the Auto-Negotiation algorithm sets link_control=SCAN_FOR_CARRIER and, during this period, sends fast link pulses to signal its presence to a remote station. If the presence of a remote station is sensed through reception of fast link pulses, the Auto-Negotiation algorithm sets link_control=DISABLE and exchanges Auto-Negotiation information with the remote station. During this period, link_status=FAIL is asserted. If the presence of a remote 1000BASE-T station is established, the Auto-Negotiation algorithm permits full operation by setting link_control=ENABLE. As soon as reliable transmission is achieved, the variable link_status=OK is asserted, upon which further PHY operations can take place.

40.4.2.6 Clock Recovery function

The Clock Recovery function couples to all four receive pairs. It may provide independent clock phases for sampling the signals on each of the four pairs.

The Clock Recovery function shall provide clocks suitable for signal sampling on each line so that the symbol-error rate indicated in 40.4.2.3 is achieved. The received clock signal must be stable and ready for use when training has been completed (loc_rcvr_status=OK). The received clock signal is supplied to the PMA Transmit function by received_clock.

40.4.3 MDI

Communication through the MDI is summarized in 40.4.3.1 and 40.4.3.2.

40.4.3.1 MDI signals transmitted by the PHY

The quinary symbols to be transmitted by the PMA on the four pairs BI_DA, BI_DB, BI_DC, and BI_DD are denoted by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD], respectively. The modulation scheme used over each pair is 5-level Pulse Amplitude Modulation. PMA Transmit generates a pulse-amplitude modulated signal on each pair in the following form:

$$s(t) = \sum_k a_k h_1(t - kT)$$

In the above equation, a_k represents the quinary symbol from the set {2, 1, 0, –1, –2} to be transmitted at time kT, and $h_1(t)$ denotes the system symbol response at the MDI. This symbol response shall comply with the electrical specifications given in 40.6.

40.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed for each pair as pulse-amplitude modulated signals that are corrupted by noise as follows:

$$r(t) = \sum_k a_k h_2(t - kT) + w(t)$$

In this equation, $h_2(t)$ denotes the impulse response of the overall channel between the transmit symbol source and the receive MDI and $w(t)$ is a term that represents the contribution of various noise sources. The four signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD shall be processed within the PMA Receive function to yield the quinary received symbols rx_symb_vector[BI_DA], rx_symb_vector[BI_DB], rx_symb_vector[BI_DC], and rx_symb_vector[BI_DD].

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40.4.4 Automatic MDI/MDI-X Configuration

Automatic MDI/MDI-X Configuration is intended to eliminate the need for crossover cables between similar devices. Implementation of an automatic MDI/MDI-X configuration is optional for 1000BASE-T devices. If an automatic configuration method is used, it shall comply with the following specifications. The assignment of pin-outs for a 1000BASE-T crossover function cable is shown in Table 40–12 in 40.8.

40.4.4.1 Description of Automatic MDI/MDI-X state machine

The Automatic MDI/MDI-X state machine facilitates switching the BI_DA(C)+ and BI_DA(C)– with the BI_DB(D)+ and BI_DB(D)– signals respectively prior to the auto-negotiation mode of operation so that FLPs can be transmitted and received in compliance with Clause 28 Auto-Negotiation specifications. The correct polarization of the crossover circuit is determined by an algorithm that controls the switching function. This algorithm uses an 11-bit Linear Feedback Shift Register (LFSR) to create a pseudo-random sequence that each end of the link uses to determine its proposed configuration. Upon making the selection to either MDI or MDI-X, the node waits for a specified amount of time while evaluating its receive channel to determine whether the other end of the link is sending link pulses or PHY-dependent data. If link pulses or PHY-dependent data are detected, it remains in that configuration. If link pulses or PHY-dependent data are not detected, it increments its LFSR and makes a decision to switch based on the value of the next bit. The state machine does not move from one state to another while link pulses are being transmitted.

40.4.4.2 Pseudo-random sequence generator

One possible implementation of the pseudo-random sequence generator using a linear-feedback shift register is shown in Figure 40–14. The bits stored in the shift register delay line at time n are denoted by S[10:0]. At each sample period, the shift register is advanced by one bit and one new bit represented by S[0] is generated. Switch control is determined by S[10].

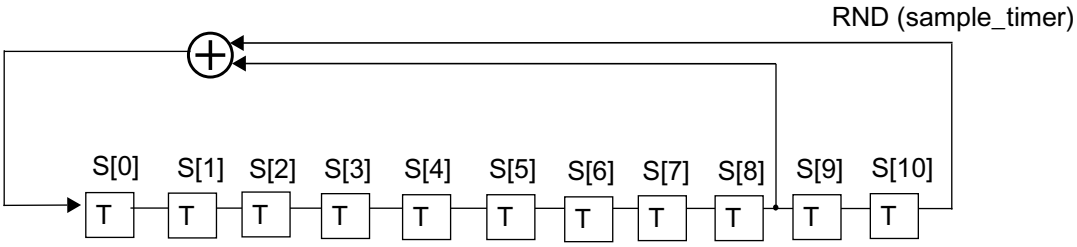


Figure 40–14—Automatic MDI/MDI-X linear-feedback shift register

40.4.5 State variables

40.4.5.1 State diagram variables

config

The PMA shall generate this variable continuously and pass it to the PCS via the PMA_CONFIG.indicate primitive.

Values: MASTER or SLAVE

link_control

This variable is defined in 28.2.6.2.

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Link_Det

This variable indicates linkpulse = true or link_status = READY has occurred at the receiver since the last time sample_timer has been started.

Values: TRUE: linkpulse = true or link_status = READY has occurred since the last time sample_timer has been started.

FALSE: otherwise

linkpulse

This variable is defined in 28.2.6.3.

link_status

This variable is defined in 28.2.6.1.

loc_rcvr_status

Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive link for the local PHY.

Values: OK: The receive link for the local PHY is operating reliably.
NOT_OK: Operation of the receive link for the local PHY is unreliable.

MDI_Status

This variable defines the condition of the Automatic MDI/MDI-X physical connection.

Values: MDI: The BI_DA, BI_DB, BI_DC, and BI_DD pairs follow the connections as described in the MDI column of Table 40–12.

MDI-X: The BI_DA, BI_DB, BI_DC, and BI_DD pairs follow the connections as described in the MDI-X column of Table 40–12.

pma_reset

Allows reset of all PMA functions.

Values: ON or OFF

Set by: PMA Reset

rem_rcvr_status

Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not.

Values: OK: The receive link for the remote PHY is operating reliably.

NOT_OK: Reliable operation of the receive link for the remote PHY is not detected.

RND (sample_timer)

This variable is defined as bit S[10] of the LSFR described in 40.4.4.2

scr_status

The scr_status parameter as communicated by the PMA_SCRSTATUS.request primitive.

Values: OK: The descrambler has achieved synchronization.

NOT_OK: The descrambler is not synchronized.

T_Pulse

This variable indicates that a linkpulse is being transmitted to the MDI.

Values: TRUE: Pulse being transmitted to the MDI

FALSE: Otherwise

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tx_enable
: The tx_enable parameter generated by PCS Transmit as specified in Figure 40–8.

  Values: TRUE or FALSE as per 40.3.3.1.

tx_mode
: PCS Transmit sends code-groups according to the value assumed by this variable.

  Values: SEND_N: This value is continuously asserted when transmission of sequences of code-groups representing a GMII data stream, control information, or idle mode is to take place.

  SEND_I: This value is continuously asserted when transmission of sequences of code-groups representing the idle mode is to take place.

  SEND_Z: This value is asserted when transmission of zero code-groups is to take place.

40.4.5.2 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where "stop timer" is asserted.

A_timer
: An asynchronous (to the Auto-Crossover State Machine) free-running timer that provides for a relatively arbitrary reset of the state machine to its initial state. This timer is used to reduce the probability of a lock-up condition where both nodes have the same identical seed initialization at the same point in time.

  Values: The condition A_timer_done becomes true upon timer expiration.

  Duration: This timer shall have a period of 1.3 s ± 25%.

  Initialization of A_timer is implementation specific.

maxwait_timer
: A timer used to limit the amount of time during which a receiver dwells in the SLAVE SILENT and TRAINING states. The timer shall expire 750 ± 10 ms if config = MASTER or 350 ± 5 ms if config = SLAVE. This timer is used jointly in the PHY Control and Link Monitor state diagrams. The maxwait_timer is tested by the Link Monitor to force link_status to be set to FAIL if the timer expires and loc_rcvr_status is NOT_OK. See Figure 40–15.

minwait_timer
: A timer used to determine the minimum amount of time the PHY Control stays in the TRAINING, SEND IDLE, or DATA states. The timer shall expire 1 ± 0.1μs after being started.

sample_timer
: This timer provides a long enough sampling window to ensure detection of Link Pulses or link_status, if they exist at the receiver.

  Values: The condition sample_timer_done becomes true upon timer expiration.

  Duration: This timer shall have a period of 62 ± 2 ms.

stabilize_timer
: A timer used to control the minimum time that loc_rcvr_status must be OK before a transition to Link Up can occur. The timer shall expire 1 ± 0.1 μs after being started.

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40.4.6 State Diagrams

40.4.6.1 PHY Control state diagram

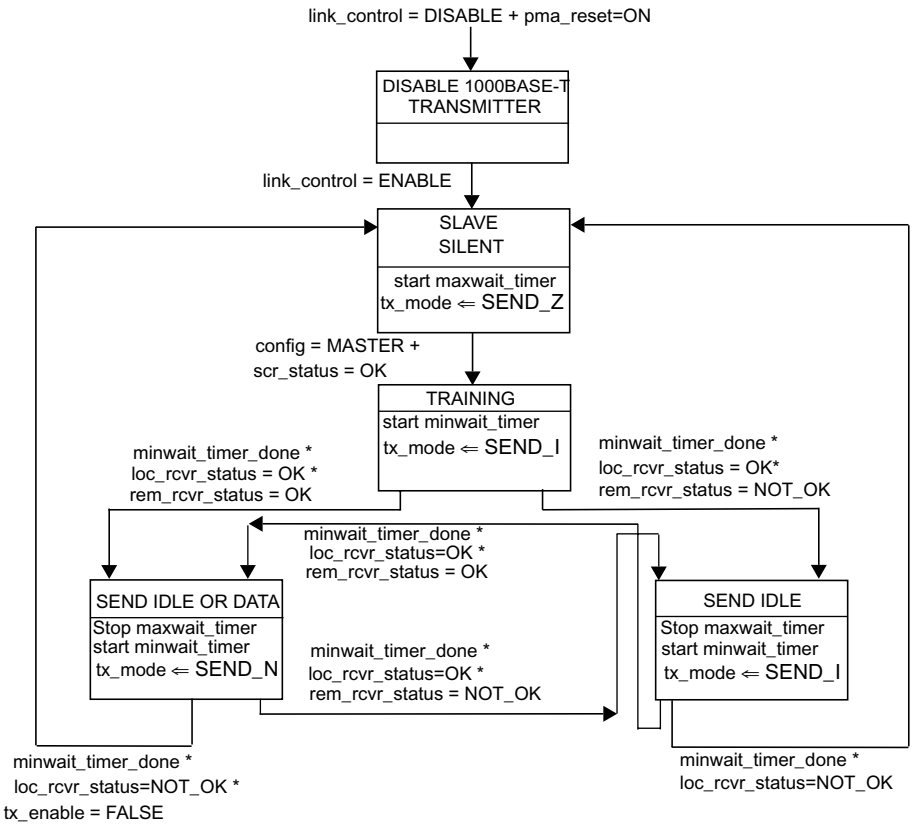


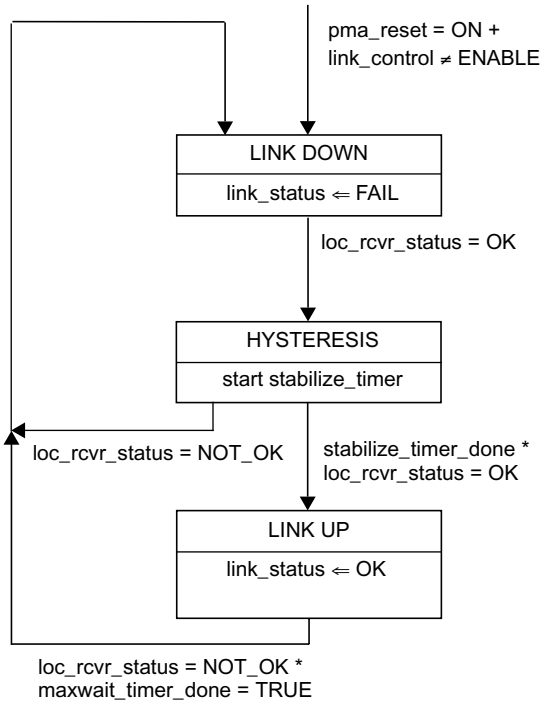
Figure 40–15—PHY Control state diagram

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40.4.6.2 Link Monitor state diagram



NOTES
1 maxwait_timer is started in PHY Control state diagram (see Figure 40—15).
2 The variables link_control and link_status are designated as link_control_(1GigT) and link_status_(1GigT), respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28—16).

Figure 40–16—Link Monitor state diagram

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40.4.6.2.1 Auto Crossover state diagram

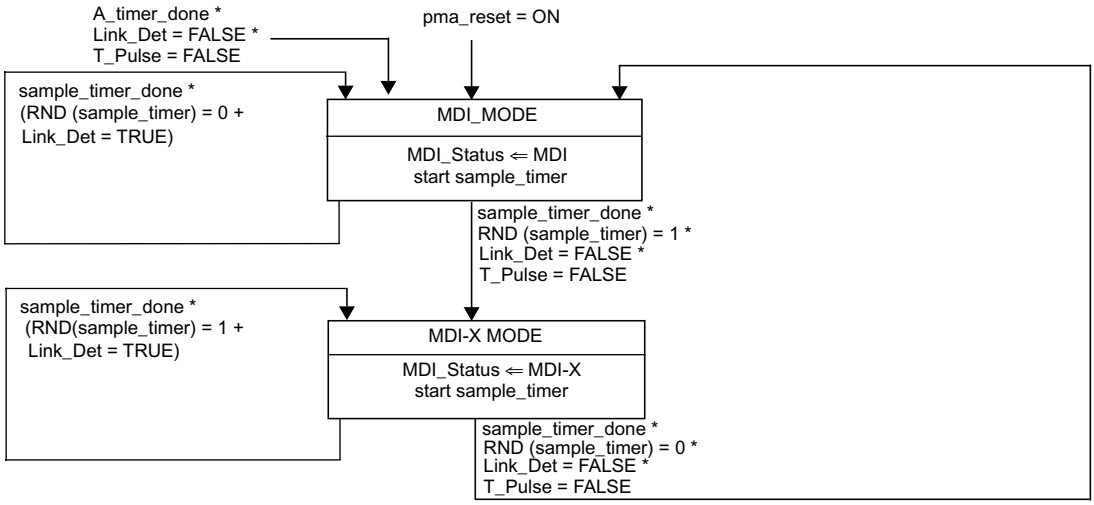


Figure 40–17—Auto Crossover state diagram

40.5 Management interface

1000BASE-T makes extensive use of the management functions provided by the MII Management Interface (see 22.2.4), and the communication and self-configuration functions provided by Auto-Negotiation (Clause 28.)

40.5.1 Support for Auto-Negotiation

All 1000BASE-T PHYs shall provide support for Auto-Negotiation (Clause 28) and shall be capable of operating as MASTER or SLAVE.

Auto-Negotiation is performed as part of the initial set-up of the link, and allows the PHYs at each end to advertise their capabilities (speed, PHY type, half or full duplex) and to automatically select the operating mode for communication on the link. Auto-negotiation signaling is used for the following two primary purposes for 1000BASE-T:

a) To negotiate that the PHY is capable of supporting 1000BASE-T half duplex or full duplex transmission.
b) To determine the MASTER-SLAVE relationship between the PHYs at each end of the link.

This relationship is necessary for establishing the timing control of each PHY. The 1000BASE-T MASTER PHY is clocked from a local source. The SLAVE PHY uses loop timing where the clock is recovered from the received data stream.

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40.5.1.1 1000BASE-T use of registers during Auto-Negotiation

A 1000BASE-T PHY shall use the management register definitions and values specified in Table 40–3.

Table 40–3—1000BASE-T Registers

Register	Bit	Name	Description	Type [a]
0	0.15:0	MII control register	Defined in 28.2.4.1.1	RO
1	1.15:0	MII status register	Defined in 28.2.4.1.2	RO
4	4.15:0	Auto-Negotiation advertisement register	The Selector Field (4.4:0) is set to the appropriate code as specified in Annex 28A. The Technology Ability Field bits 4.12:5 are set to the appropriate code as specified in Annexes 28B and 28D. Bit 4.15 is set to logical one to indicate the desired exchange of Next Pages describing the gigabit extended capabilities.	R/W
5	5.15:0	Auto-Negotiation link partner ability register	Defined in 28.2.4.1.4. 1000BASE-T implementations do not use this register to store Auto-Negotiation Link Partner Next Page data.	RO
6	6.15:0	Auto-Negotiation expansion register	Defined in 28.2.4.1.5	RO
7	7.15:0	Auto-Negotiation Next Page transmit register	Defined in 28.2.4.1.6	R/W
8	8.15:0	Auto-Negotiation link partner Next Page register	Defined in 28.2.4.1.8	RO
9	9.15:13	Test mode bits	Transmitter test mode operations are defined by bits 9.15:13 as described in 40.6.1.1.2 and Table 40–7. The default values for bits 9.15:13 are all zero.	R/W
9	9.12	MASTER-SLAVE Manual Config Enable	1=Enable MASTER-SLAVE Manual configuration value 0=Disable MASTER-SLAVE Manual configuration value Default bit value is 0.	R/W
9	9.11	MASTER-SLAVE Config Value	1=Configure PHY as MASTER during MASTER-SLAVE negotiation, only when 9.12 is set to logical one. 0=Configure PHY as SLAVE during MASTER-SLAVE negotiation, only when 9.12 is set to logical one. Default bit value is 0.	R/W
9	9.10	Port type	Bit 9.10 is to be used to indicate the preference to operate as MASTER (multiport device) or as SLAVE (single-port device) if the MASTER-SLAVE Manual Configuration Enable bit, 9.12, is not set. Usage of this bit is described in 40.5.2. 1=Multiport device 0=single-port device	R/W
9	9.9	1000BASE-T Full Duplex	1 = Advertise PHY is 1000BASE-T full duplex capable. 0 = Advertise PHY is not 1000BASE-T full duplex capable.	R/W
9	9.8	1000BASE-T Half Duplex	1 = Advertise PHY is 1000BASE-T half duplex capable. 0 = Advertise PHY is not 1000BASE-T half duplex capable.	R/W

[a] R/W = Read/Write, RO = Read Only, SC = Self Clearing, LH = Latch High

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Table 40–3—1000BASE-T Registers *(continued)*

Register	Bit	Name	Description	Type [a]
9	9.7:0	Reserved	Write as 0, ignore on read.	R/W
10	10.15	MASTER-SLAVE configuration fault	Configuration fault, as well as the criteria and method of fault detection, is PHY specific. The MASTER-SLAVE Configuration Fault bit will be cleared each time register 10 is read via the management interface and will be cleared by a 1000BASE-T PMA reset. This bit will self clear on Auto-Negotiation enable or Auto-Negotiation complete.This bit will be set if the number of failed MASTER-SLAVE resolutions reaches 7. For l000BASE-T, the fault condition will occur when both PHYs are forced to be MASTERs or SLAVEs at the same time using bits 9.12 and 9.11. Bit 10.15 should be set via the MASTER-SLAVE Configuration Resolution function described in 40.5.2. 1 = MASTER-SLAVE configuration fault detected 0 = No MASTER-SLAVE configuration fault detected	RO/LH/SC
10	10.14	MASTER-SLAVE configuration resolution	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE	RO
10	10.13	Local Receiver Status	1 = Local Receiver OK (loc_rcvr_status=OK) 0 = Local Receiver not OK (loc_rcvr_status=NOT_OK) Defined by the value of loc_rcvr_status as per 40.4.5.1.	RO
10	10.12	Remote Receiver Status	1 = Remote Receiver OK (rem_rcvr_status=OK) 0 = Remote Receiver not OK (rem_rcvr_status=NOT_OK) Defined by the value of rem_rcvr_status as per 40.4.5.1.	RO
10	10.11	LP 1000T FD	1 = Link Partner is capable of 1000BASE-T full duplex 0 = Link Partner is not capable of 1000BASE-T full duplex This bit is guaranteed to be valid only when the Page received bit (6.1) has been set to 1.	RO
10	10.10	LP 1000T HD	1 = Link Partner is capable of 1000BASE-T half duplex 0 = Link Partner is not capable of 1000BASE-T half duplex This bit is guaranteed to be valid only when the Page received bit (6.1) has been set to 1.	RO
10	10.9:8	Reserved	Reserved	RO
10	10.7:0	Idle Error Count	Bits 10.7:0 indicate the Idle Error count, where 10.7 is the most significant bit. These bits contain a cumulative count of the errors detected when the receiver is receiving idles and PMA_TXMODE.indicate is equal to SEND_N (indicating that both local and remote receiver status have been detected to be OK). The counter is incremented every symbol period that rxerror_status is equal to ERROR. These bits are reset to all zeros when the error count is read by the management function or upon execution of the PCS Reset function and are to be held at all ones in case of overflow (see 30.5.1.1.11).	RO/SC
15	15.15:12	Extended status register	See 22.2.4.4	RO

[a] R/W = Read/Write, RO = Read Only, SC = Self Clearing, LH = Latch High

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40.5.1.2 1000BASE-T Auto-Negotiation page use

1000BASE-T PHYs shall exchange one Auto-Negotiation Base Page, a 1000BASE-T formatted Next Page, and two 1000BASE-T unformatted Next Pages in sequence, without interruption, as specified in Table 40–4. Additional Next Pages can be exchanged as described in Annex 40C.

Note that the Acknowledge 2 bit is not utilized and has no meaning when used for the 1000BASE-T message page exchange.

Table 40–4—1000BASE-T Base and Next Pages bit assignments

Bit	Bit definition	Register location
BASE PAGE		
D15	1 (to indicate that Next Pages follow)	
D14:D1	As specified in 28.2.1.2	Management register 4
PAGE 0 (Message Next Page)		
M10:M0	8	
PAGE 1 (Unformatted Next Page)		
U10:U5	Reserved transmit as 0	
U4	1000BASE-T half duplex (1 = half duplex and 0 = no half duplex)	GMII register 9.8 (MASTER-SLAVE Control register)
U3	1000BASE-T full duplex (1 = full duplex and 0 = no full duplex)	GMII register 9.9 (MASTER-SLAVE Control register)
U2	1000BASE-T port type bit (1 = multiport device and 0 = single-port device)	GMII register 9.10 (MASTER-SLAVE Control register)
U1	1000BASE-T MASTER-SLAVE Manual Configuration value (1 = MASTER and 0 = SLAVE.) This bit is ignored if 9.12 = 0.	GMII register 9.11 (MASTER-SLAVE Control register)
U0	1000BASE-T MASTER-SLAVE Manual Configuration Enable (1 = Manual Configuration Enable.) This bit is intended to be used for manual selection in a particular MASTER-SLAVE mode and is to be used in conjunction with bit 9.11.	GMII register 9.12 (MASTER-SLAVE Control register)
PAGE 2 (Unformatted Next Page)		
U10	1000BASE-T MASTER-SLAVE Seed Bit 10 (SB10) (MSB)	MASTER-SLAVE Seed Value (10:0)
U9	1000BASE-T MASTER-SLAVE Seed Bit 9 (SB9)	
U8	1000BASE-T MASTER-SLAVE Seed Bit 8 (SB8)	
U7	1000BASE-T MASTER-SLAVE Seed Bit 7 (SB7)	
U6	1000BASE-T MASTER-SLAVE Seed Bit 6 (SB6)	
U5	1000BASE-T MASTER-SLAVE Seed Bit 5 (SB5)	
U4	1000BASE-T MASTER-SLAVE Seed Bit 4 (SB4)	
U3	1000BASE-T MASTER-SLAVE Seed Bit 3 (SB3)	
U2	1000BASE-T MASTER-SLAVE Seed Bit 2 (SB2)	
U1	1000BASE-T MASTER-SLAVE Seed Bit 1 (SB1)	
U0	1000BASE-T MASTER-SLAVE Seed Bit 0 (SB0)	

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40.5.1.3 Sending Next Pages

Implementors who do not wish to send additional Next Pages (i.e., Next Pages in addition to those required to perform PHY configuration as defined in this clause) can use Auto-Negotiation as defined in Clause 28 and the Next Pages defined in 40.5.1.2. Implementors who wish to send additional Next Pages are advised to consult Annex 40C.

40.5.2 MASTER-SLAVE configuration resolution

Since both PHYs that share a link segment are capable of being MASTER or SLAVE, a prioritization scheme exists to ensure that the correct mode is chosen. The MASTER-SLAVE relationship shall be determined during Auto-Negotiation using Table 40–5 with the 1000BASE-T Technology Ability Next Page bit values specified in Table 40–4 and information received from the link partner. This process is conducted at the entrance to the FLP LINK GOOD CHECK state shown in the Arbitration state diagram (Figure 28–13.)

The following four equations are used to determine these relationships:

manual_MASTER = U0 * U1
manual_SLAVE = U0 * !U1
single-port device = !U0 * !U2,
multiport device = !U0 * U2

where

U0 is bit 0 of unformatted page 1,
U1 is bit 1 of unformatted page 1, and
U2 is bit 2 of unformatted page 1 (see Table 40–4).

A 1000BASE-T PHY is capable of operating either as the MASTER or SLAVE. In the scenario of a link between a single-port device and a multiport device, the preferred relationship is for the multiport device to be the MASTER PHY and the single-port device to be the SLAVE. However, other topologies may result in contention. The resolution function of Table 40–5 is defined to handle any relationship conflicts.

Table 40–5—1000BASE-T MASTER-SLAVE configuration resolution table

Local device type	Remote device type	Local device resolution	Remote device resolution
single-port device	multiport device	SLAVE	MASTER
single-port device	manual_MASTER	SLAVE	MASTER
manual_SLAVE	manual_MASTER	SLAVE	MASTER
manual_SLAVE	multiport device	SLAVE	MASTER
multiport device	manual_MASTER	SLAVE	MASTER
manual_SLAVE	single-port device	SLAVE	MASTER
multiport device	single-port device	MASTER	SLAVE
multiport device	manual_SLAVE	MASTER	SLAVE

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Table 40–5—1000BASE-T MASTER-SLAVE configuration resolution table *(continued)*

Local device type	Remote device type	Local device resolution	Remote device resolution
manual_MASTER	manual_SLAVE	MASTER	SLAVE
manual_MASTER	single-port device	MASTER	SLAVE
single-port device	manual_SLAVE	MASTER	SLAVE
manual_MASTER	multiport device	MASTER	SLAVE
multiport device	multiport device	The device with the higher SEED value is configured as MASTER, otherwise SLAVE.	The device with the higher SEED value is configured as MASTER, otherwise SLAVE.
single-port device	single-port device	The device with the higher SEED value is configured as MASTER, otherwise SLAVE	The device with the higher SEED value is configured as MASTER, otherwise SLAVE.
manual_SLAVE	manual_SLAVE	MASTER-SLAVE configuration fault	MASTER-SLAVE configuration fault
manual_MASTER	manual_MASTER	MASTER-SLAVE configuration fault	MASTER-SLAVE configuration fault

The rationale for the hierarchy illustrated in Table 40–5 is straightforward. A 1000BASE-T multiport device has higher priority than a single-port device to become the MASTER. In the case where both devices are of the same type, e.g., both devices are multiport devices, the device with the higher MASTER-SLAVE seed bits (SB0...SB10), where SB10 is the MSB, shall become the MASTER and the device with the lower seed value shall become the SLAVE. In case both devices have the same seed value, both should assert link_status_1GigT=FAIL (as defined in 28.3.1) to force a new cycle through Auto-Negotiation. Successful completion of the MASTER-SLAVE resolution shall be treated as MASTER-SLAVE configuration resolution complete.

The method of generating a random or pseudorandom seed is left to the implementor. The generated random seeds should belong to a sequence of independent, identically distributed integer numbers with a uniform distribution in the range of 0 to $2^{11}-2$. The algorithm used to generate the integer should be designed to minimize the correlation between the number generated by any two devices at any given time. A seed counter shall be provided to track the number of seed attempts. The seed counter shall be set to zero at start-up and shall be incremented each time a seed is generated. When MASTER-SLAVE resolution is complete, the seed counter shall be reset to 0 and bit 10.15 shall be set to logical zero. A MASTER-SLAVE resolution fault shall be declared if resolution is not reached after the generation of seven seeds.

The MASTER-SLAVE Manual Configuration Enable bit (control register bit 9.12) and the MASTER-SLAVE Config Value bit (control register bit 9.11) are used to manually set a device to become the MASTER or the SLAVE. In case both devices are manually set to become the MASTER or the SLAVE, this condition shall be flagged as a MASTER-SLAVE Configuration fault condition, thus the MASTER-SLAVE Configuration fault bit (status register bit 10.15) shall be set to logical one. The MASTER-SLAVE Configuration fault condition shall be treated as MASTER-SLAVE configuration resolution complete and link_status_1GigT shall be set to FAIL, because the MASTER-SLAVE relationship was not resolved. This will force a new cycle through Auto-Negotiation after the link_fail_inhibit_timer has expired. Determination of MASTER-SLAVE values occur on the entrance to the FLP LINK GOOD CHECK state (Figure 28–16) when the highest common denominator (HCD) technology is 1000BASE-T. The resulting MASTER-SLAVE value is used by the 1000BASE-T PHY control (40.4.2.4).

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If MASTER-SLAVE Manual Configuration is disabled (bit 9.12 is set to 0) and the local device detects that both the local device and the remote device are of the same type (either multiport device or single-port device) and that both have generated the same random seed, it generates and transmits a new random seed for MASTER-SLAVE negotiation by setting link_status to FAIL and cycling through the Auto-Negotiation process again.

The MASTER-SLAVE configuration process returns one of the three following outcomes:

a) *Successful:* Bit 10.15 of the 1000BASE-T Status Register is set to logical zero and bit 10.14 is set to logical one for MASTER resolution or for logical zero for SLAVE resolution. 1000BASE-T returns control to Auto_Negotiation (at the entrance to the FLP LINK GOOD CHECK state in Figure 28–16) and passes the value MASTER or SLAVE to PMA_CONFIG.indicate (see 40.2.4.)
b) *Unsuccessful:* link_status_1GigT is set to FAIL and Auto-Negotiation restarts (see Figure 28–16.)
c) *Fault detected:* (This happens when both end stations are set for manual configuration and both are set to MASTER or both are set to SLAVE.) Bit 10.15 of the 1000BASE-T Status Register is set to logical one to indicate that a configuration fault has been detected. This bit also is set when seven attempts to configure the MASTER SLAVE relationship via the seed method have failed. When a fault is detected, link_status_1GigT is set to FAIL, causing Auto-Negotiation to cycle through again.

NOTE—MASTER-SLAVE arbitration only occurs if 1000BASE-T is selected as the highest common denominator; otherwise, it is assumed to have passed this condition.

40.6 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA.

Common-mode tests use the common-mode return point as a reference.

40.6.1 PMA-to-MDI interface tests

40.6.1.1 Isolation requirement

The PHY shall provide electrical isolation between the port device circuits, including frame ground (if any) and all MDI leads. This electrical separation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC 60950: 1991.
b) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC 60950: 1991.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time or half value), as defined in IEC 60060.

There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC 60950: 1991, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 Vdc.

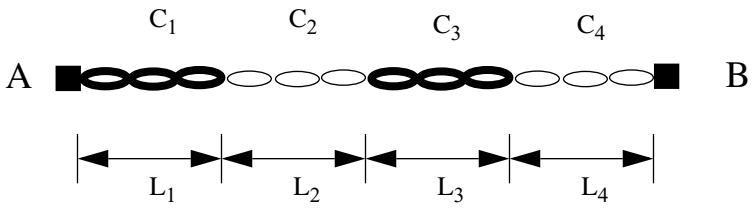
40.6.1.1.1 Test channel

To perform the transmitter MASTER-SLAVE timing jitter tests described in this clause, a test channel is required to ensure that jitter is measured under conditions of poor signal to echo ratio. This test channel shall be constructed by combining 100 and 120 Ω cable segments that both meet or exceed ISO/IEC 11801 Category 5 specifications for each pair, as shown in Figure 40–18, with the lengths and additional restrictions on parameters described in Table 40–6. The ends of the test channel shall be terminated with connectors meeting or exceeding ANSI/TIA/EIA-568-A:1995 or ISO/IEC 11801:1995 Category 5 specifications. The

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return loss of the resulting test channel shall meet the return loss requirements of 40.7.2.3 and the crosstalk requirements of 40.7.3.



Identical for each of the four pairs.

Figure 40–18—Test channel topology for each cable pair

Table 40–6—Test channel cable segment specifications

Cable segment	Length (meters)	Characteristic impedance (at frequencies > 1 MHz)	Attenuation (per 100 meters at 31.25 MHz)
1	L_1=1.20	120 ± 5Ω	7.8 to 8.8 dB
2	L_2=x	100 ± 5Ω	10.8 to 11.8 dB
3	L_3=1.48	120 ± 5Ω	7.8 to 8.8 dB
4	L_4=y	100 ± 5Ω	10.8 to 11.8 dB

NOTE—x is chosen so that the total delay of segments C1, C2, and C3, averaged across all pairs, is equal to 570 ns at 31.25 MHz; however, if this would cause the total attenuation of segments C1, C2, and C3, averaged across all pairs, to exceed the worst case insertion loss specified in 40.7.2.1 then x is chosen so that the total attenuation of segments C1, C2, and C3, averaged across all pairs, does not violate 40.7.2.1 at any frequencies. The value of y is chosen so that the total attenuation of segments C1, C2, C3, and C4, averaged across all pairs, does not violate 40.7.2.1 at any frequency (y may be 0).

40.6.1.1.2 Test modes

The test modes described below shall be provided to allow for testing of the transmitter waveform, transmitter distortion, and transmitted jitter.

For a PHY with a GMII interface, these modes shall be enabled by setting bits 9.13:15 (1000BASE-T Control Register) of the GMII Management register set as shown in Table 40–7. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation. PHYs without a GMII shall provide a means to enable these modes for conformance testing.

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Table 40–7—GMII management register settings for test modes

Bit 1 (9.15)	Bit 2 (9.14)	Bit 3 (9.13)	Mode
0	0	0	Normal operation
0	0	1	Test mode 1—Transmit waveform test
0	1	0	Test mode 2—Transmit jitter test in MASTER mode
0	1	1	Test mode 3—Transmit jitter test in SLAVE mode
1	0	0	Test mode 4—Transmitter distortion test
1	0	1	Reserved, operations not identified.
1	1	0	Reserved, operations not identified.
1	1	1	Reserved, operations not identified.

When test mode 1 is enabled, the PHY shall transmit the following sequence of data symbols A_n, B_n, C_n, D_n, of 40.3.1.3.6 continually from all four transmitters:

{{+2 followed by 127 0 symbols}, {–2 followed by 127 0 symbols},{+1 followed by 127 0 symbols}, {–1 followed by 127 0 symbols}, {128 +2 symbols, 128 –2 symbols, 128 +2 symbols, 128 –2 symbols}, {1024 0 symbols}}

This sequence is repeated continually without breaks between the repetitions when the test mode is enabled. A typical transmitter output is shown in Figure 40–19. The transmitter shall time the transmitted symbols from a 125.00 MHz ± 0.01% clock in the MASTER timing mode.

When test mode 2 is enabled, the PHY shall transmit the data symbol sequence {+2, –2} repeatedly on all channels. The transmitter shall time the transmitted symbols from a 125.00 MHz ± 0.01% clock in the MASTER timing mode.

When test mode 3 is enabled, the PHY shall transmit the data symbol sequence {+2, –2} repeatedly on all channels. The transmitter shall time the transmitted symbols from a 125.00 MHz ± 0.01% clock in the SLAVE timing mode. A typical transmitter output for transmitter test modes 2 and 3 is shown in Figure 40–20.

When test mode 4 is enabled, the PHY shall transmit the sequence of symbols generated by the following scrambler generator polynomial, bit generation, and level mappings:

$$g_{s1} = 1 + x^9 + x^{11}$$

The maximum-length shift register used to generate the sequences defined by this polynomial shall be updated once per symbol interval (8 ns). The bits stored in the shift register delay line at a particular time n are denoted by $Scr_n[10:0]$. At each symbol period the shift register is advanced by one bit and one new bit represented by $Scr_n[0]$ is generated. Bits $Scr_n[8]$ and $Scr_n[10]$ are exclusive OR'd together to generate the next $Scr_n[0]$ bit. The bit sequences, $x0_n$, $x1_n$, and $x2_n$, generated from combinations of the scrambler bits as shown in the following equations, shall be used to generate the quinary symbols, s_n, as shown in Table 40–8. The quinary symbol sequence shall be presented simultaneously to all transmitters. The transmitter shall time the transmitted symbols from a 125.00 MHz ± 0.01% clock in the MASTER timing mode. A typical transmitter output for transmitter test mode 4 is shown in Figure 40–21.

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$$x0_n = Scr_n[0]$$

$$x1_n = Scr_n[1] \wedge Scr_n[4]$$

$$x2_n = Scr_n[2] \wedge Scr_n[4]$$

Table 40–8—Transmitter test mode 4 symbol mapping

x2n	x1n	x0n	quinary symbol, s_n
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	–1
1	0	0	0
1	0	1	1
1	1	0	–2
1	1	1	–1

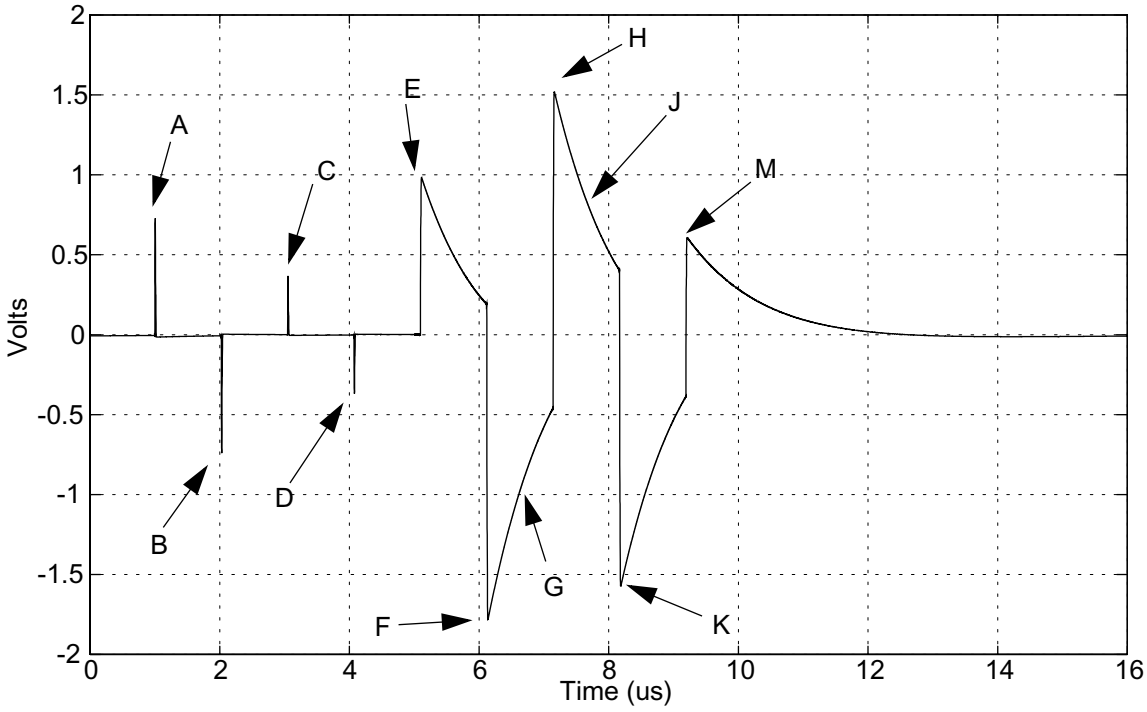


Figure 40–19—Example of transmitter test mode 1 waveform (1 cycle)

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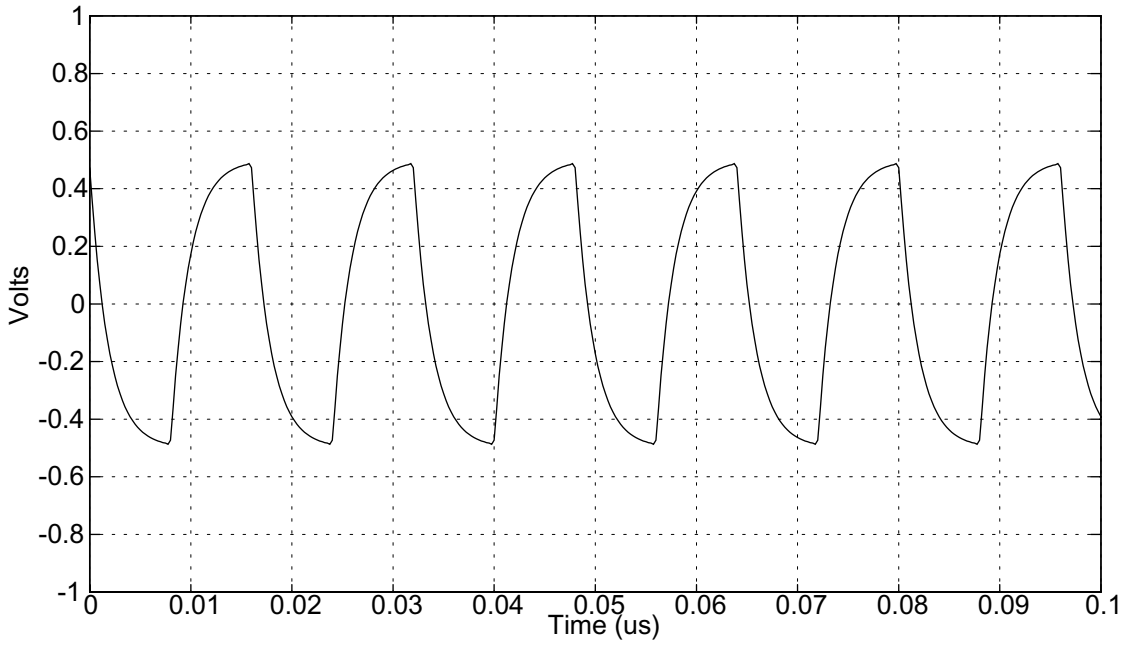


Figure 40–20—Example of transmitter test modes 2 and 3 waveform

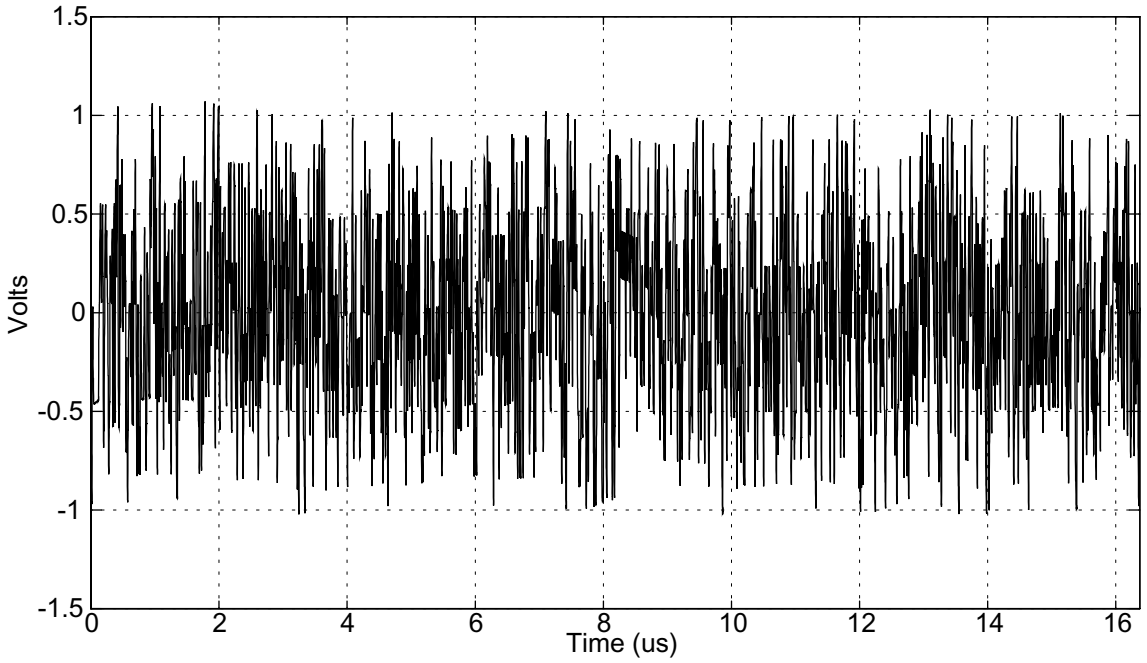


Figure 40–21—Example of Transmitter Test Mode 4 waveform (1 cycle)

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40.6.1.1.3 Test Fixtures

The following fixtures (illustrated by Figure 40–22, Figure 40–23, Figure 40–24, and Figure 40–25), or their functional equivalents, shall be used for measuring the transmitter specifications described in 40.6.1.2.

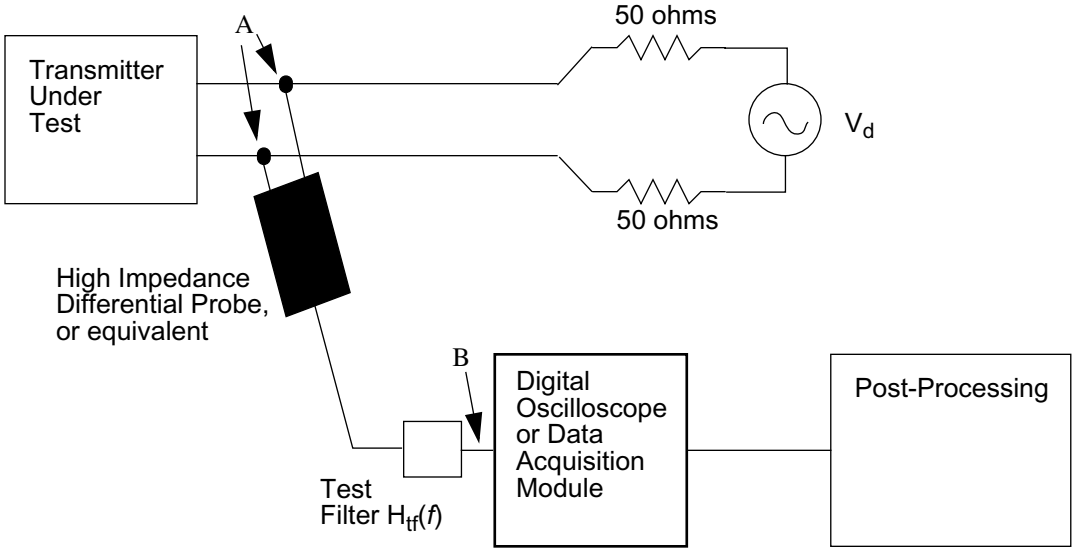


Figure 40–22—Transmitter test fixture 1 for template measurement

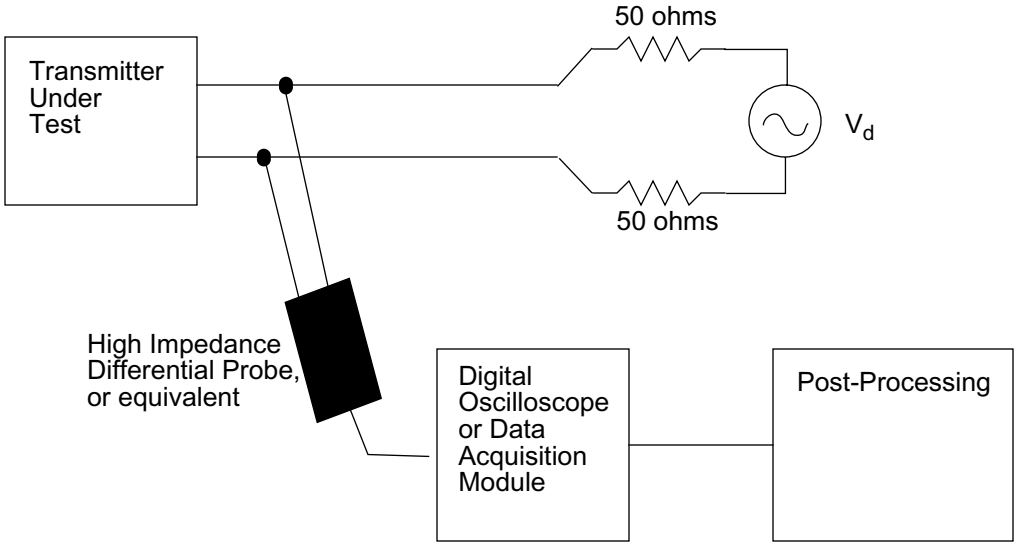


Figure 40–23—Transmitter test fixture 2 for droop measurement

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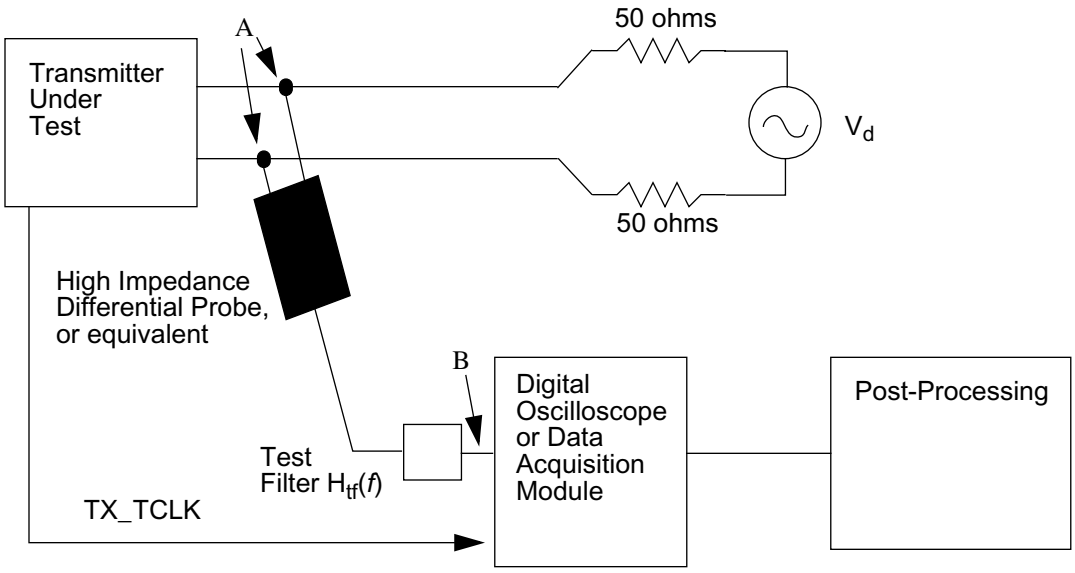


Figure 40–24—Transmitter test fixture 3 for distortion measurement

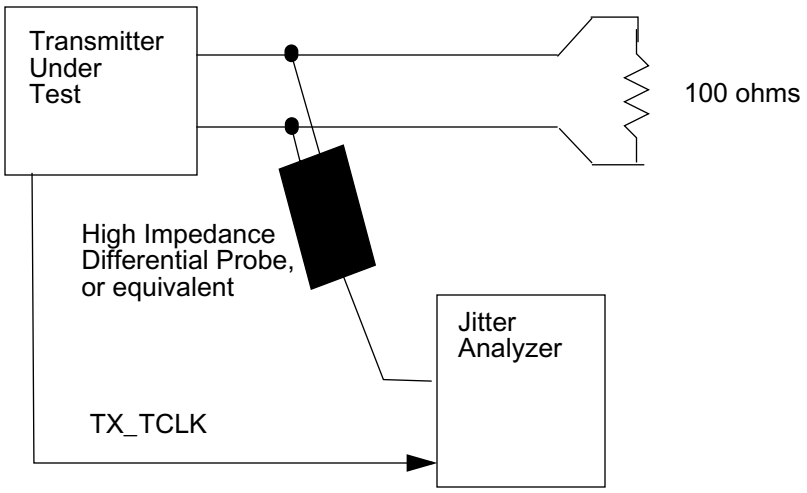


Figure 40–25—Transmitter test fixture 4 for transmitter jitter measurement

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The test filter, $H_{tf}(f)$, used in transmitter test fixtures 1 and 3 may be located between the points A and B as long as the test filter does not significantly alter the impedance seen by the transmitter. The test filter may instead be implemented as a digital filter in the post processing block. The test filter shall have the following continuous time transfer function or its discrete time equivalent:

$$H_{tf}(f) = \frac{jf}{jf + 2\times10^{6}} \qquad f \text{ in Hz}$$

NOTE—j denotes the square root of –1.

The disturbing signal, V_d, shall have the characteristics listed in Table 40–9.

Table 40–9—V_d Characteristics

Characteristic	Transmit test fixture 1	Transmit test fixture 2	Transmit test fixture 3
Waveform	Sine wave		
Amplitude	2.8 volts peak-to-peak	2.8 volts peak-to-peak	5.4 volts peak-to-peak
Frequency	31.25 MHz	31.25 MHz	20.833 MHz (125/6 MHz)
Purity	All harmonics >40 dB below fundamental		

The post-processing block has two roles. The first is to remove the disturbing signal from the measurement. A method of removing the disturbing signal is to take a single shot acquisition of the transmitted signal plus test pattern, then remove the best fit of a sine wave at the fundamental frequency of the disturbing signal from the measurement. It will be necessary to allow the fitting algorithm to adjust the frequency, phase, and amplitude parameters of the sine wave to achieve the best fit.

The second role of the post-processing block is to compare the measured data with the templates, droop specification, or distortion specification.

Trigger averaging of the transmitter output to remove measurement noise and increase measurement resolution is acceptable provided it is done in a manner that does not average out possible distortions caused by the interaction of the transmitter and the disturbing voltage. For transmitter template and droop measurements, averaging can be done by ensuring the disturbing signal is exactly synchronous to the test pattern so that the phase of the disturbing signal at any particular point in the test pattern remains constant. Trigger averaging also requires a triggering event that is synchronous to the test pattern. A trigger pulse generated by the PHY would be ideal for this purpose; however, in practice, triggering off the waveform generated by one of the other transmitter outputs that does not have the disturbing signal present may be possible.

NOTE—The disturbing signal may be made synchronous to the test pattern by creating the disturbing signal using a source of the transmit clock for the PHY under test, dividing it down to the proper frequency for the disturbing signal, passing the result through a high Q bandpass filter to eliminate harmonics and then amplifying the result to the proper amplitude.

The generator of the disturbing signal must have sufficient linearity and range so it does not introduce any appreciable distortion when connected to the transmitter output (see Table 40–9). This may be verified by replacing the transmitter under test with another identical disturbing signal generator having a different frequency output and verifying that the resulting waveform's spectrum does not show significant distortion products.

Additionally, to allow for measurement of transmitted jitter in master and slave modes, the PHY shall provide access to the 125 MHz symbol clock, TX_TCLK, that times the transmitted symbols (see 40.4.2.2). The PHY shall provide a means to enable this clock output if it is not normally enabled.

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40.6.1.2 Transmitter electrical specifications

The PMA shall provide the Transmit function specified in 40.4.2.2 in accordance with the electrical specifications of this clause.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output.

The tolerance on the poles of the test filters used in this subclause shall be ±1%.

Practical considerations prevent measurement of the local transmitter performance in the presence of the remotely driven signal in this standard; however, the design of the transmitter to tolerate the presence of the remotely driven signal with acceptable distortion or other changes in performance is a critical issue and must be addressed by the implementor. To this end, a disturbing sine wave is used to simulate the presence of a remote transmitter for a number of the transmitter tests described in the following subordinate subclauses.

40.6.1.2.1 Peak differential output voltage and level accuracy

The absolute value of the peak of the waveform at points A and B, as defined in Figure 40–19, shall fall within the range of 0.67 V to 0.82 V (0.75 V ± 0.83 dB). These measurements are to be made for each pair while operating in test mode 1 and observing the differential signal output at the MDI using transmitter test fixture 1 with no intervening cable.

The absolute value of the peak of the waveforms at points A and B shall differ by less than 1%.

The absolute value of the peak of the waveform at points C and D as defined in Figure 40–19 shall differ by less than 2% from 0.5 times the average of the absolute values of the peaks of the waveform at points A and B.

40.6.1.2.2 Maximum output droop

The magnitude of the negative peak value of the waveform at point G, as defined in Figure 40–19, shall be greater than 73.1% of the magnitude of the negative peak value of the waveform at point F. These measurements are to be made for each pair while in test mode 1 and observing the differential signal output at the MDI using transmit test fixture 2 with no intervening cable. Point G is defined as the point exactly 500 ns after point F. Point F is defined as the point where the waveform reaches its minimum value at the location indicated in Figure 40–19. Additionally, the magnitude of the peak value of the waveform at point J as defined in Figure 40–19 shall be greater than 73.1% of the magnitude of the peak value of the waveform at point H. Point J is defined as the point exactly 500 ns after point H. Point H is defined as the point where the waveform reaches its maximum value at the location indicated in Figure 40–19.

40.6.1.2.3 Differential output templates

The voltage waveforms around points A, B, C, D defined in Figure 40–19, after the normalization described herein, shall lie within the time domain template 1 defined in Figure 40–26 and the piecewise linear interpolation between the points in Table 40–10. These measurements are to be made for each pair while in test mode 1 and while observing the differential signal output at the MDI using transmitter test fixture 1 with no intervening cable. The waveforms may be shifted in time as appropriate to fit within the template.

The waveform around point A is normalized by dividing by the peak value of the waveform at A.

The waveform around point B is normalized by dividing by the negative of the peak value of the waveform at A.

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The waveform around point C is normalized by dividing by 1/2 the peak value of the waveform at A.

The waveform around point D is normalized by dividing by the negative of 1/2 the peak value of the waveform at A.

The voltage waveforms around points F and H defined in Figure 40–19, after the normalization described herein, shall lie within the time domain template 2 defined in Figure 40–26 and the piecewise linear interpolation between the points in Table 40–11. These measurements are to be made for each pair while in test mode 1 and while observing the differential signal output at the MDI using transmitter test fixture 1 with no intervening cable. The waveforms may be shifted in time as appropriate to fit within the template.

The waveform around point F is normalized by dividing by the peak value of the waveform at F.

The waveform around point H is normalized by dividing by the peak value of the waveform at H.

NOTE—The templates were created with the following assumptions about the elements in the transmit path:

1) Digital Filter: $0.75 + 0.25\ z^{-1}$
2) Ideal DAC
3) Single pole continuous time low pass filter with pole varying from 70.8 MHz to 117 MHz or linear rise/fall time of 5 ns.
4) Single pole continuous time high-pass filter (transformer high pass) with pole varying from 1 Hz to 100 kHz.
5) Single pole continuous time high-pass filter (test filter) with pole varying from 1.8 MHz to 2.2 MHz.
6) Additionally, +0.025 was added to the upper template and –0.025 was added to the lower template to allow for noise and measurement error.

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NOTE—The transmit templates are not intended to address electromagnetic radiation limits.

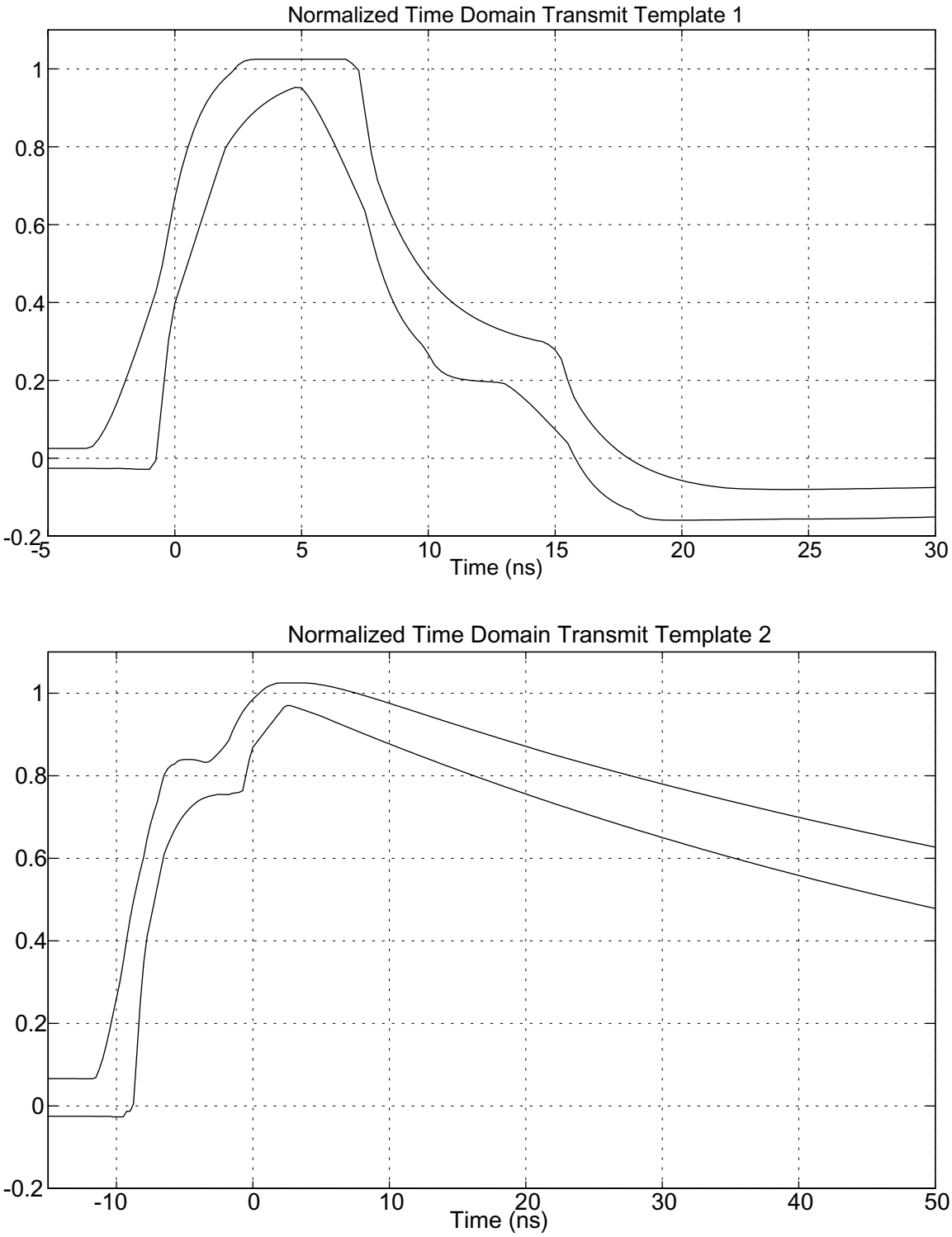


Figure 40–26—Normalized transmit templates as measured at MDI using transmit test fixture 1

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NOTE—The ASCII for Tables 40–10 and 40–11 is available from http://www.ieee802.org/3/publication/index.html.[9]

Table 40–10—Normalized time domain voltage template 1

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
–5.00	0.025	–0.026	12.75	0.332	0.195
–4.75	0.025	–0.026	13.00	0.326	0.192
–4.50	0.025	–0.026	13.25	0.320	0.181
–4.25	0.025	–0.026	13.50	0.315	0.169
–4.00	0.025	–0.026	13.75	0.311	0.155
–3.75	0.025	–0.026	14.00	0.307	0.140
–3.50	0.025	–0.026	14.25	0.303	0.124
–3.25	0.031	–0.026	14.50	0.300	0.108
–3.00	0.050	–0.026	14.75	0.292	0.091
–2.75	0.077	–0.026	15.00	0.278	0.074
–2.50	0.110	–0.026	15.25	0.254	0.056
–2.25	0.148	–0.026	15.50	0.200	0.039
–2.00	0.190	–0.027	15.75	0.157	0.006
–1.75	0.235	–0.027	16.00	0.128	–0.023
–1.50	0.281	–0.028	16.25	0.104	–0.048
–1.25	0.329	–0.028	16.50	0.083	–0.068
–1.00	0.378	–0.028	16.75	0.064	–0.084
–0.75	0.427	–0.006	17.00	0.047	–0.098
–0.50	0.496	0.152	17.25	0.032	–0.110
–0.25	0.584	0.304	17.50	0.019	–0.119
0.00	0.669	0.398	17.75	0.007	–0.127
0.25	0.739	0.448	18.00	–0.004	–0.133
0.50	0.796	0.499	18.25	–0.014	–0.145
0.75	0.844	0.550	18.50	–0.022	–0.152
1.00	0.882	0.601	18.75	–0.030	–0.156
1.25	0.914	0.651	19.00	–0.037	–0.158
1.50	0.940	0.701	19.25	–0.043	–0.159

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Table 40–10—Normalized time domain voltage template 1 *(continued)*

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
1.75	0.960	0.751	19.50	–0.048	–0.159
2.00	0.977	0.797	19.75	–0.053	–0.159
2.25	0.992	0.822	20.00	–0.057	–0.159
2.50	1.010	0.845	20.25	–0.061	–0.159
2.75	1.020	0.864	20.50	–0.064	–0.159
3.00	1.024	0.881	20.75	–0.067	–0.159
3.25	1.025	0.896	21.00	–0.070	–0.159
3.50	1.025	0.909	21.25	–0.072	–0.159
3.75	1.025	0.921	21.50	–0.074	–0.158
4.00	1.025	0.931	21.75	–0.076	–0.158
4.25	1.025	0.939	22.00	–0.077	–0.158
4.50	1.025	0.946	22.25	–0.078	–0.158
4.75	1.025	0.953	22.50	–0.079	–0.158
5.00	1.025	0.951	22.75	–0.079	–0.157
5.25	1.025	0.931	23.00	–0.079	–0.157
5.50	1.025	0.905	23.25	–0.080	–0.157
5.75	1.025	0.877	23.50	–0.080	–0.157
6.00	1.025	0.846	23.75	–0.080	–0.156
6.25	1.025	0.813	24.00	–0.080	–0.156
6.50	1.025	0.779	24.25	–0.080	–0.156
6.75	1.025	0.743	24.50	–0.080	–0.156
7.00	1.014	0.707	24.75	–0.080	–0.156
7.25	0.996	0.671	25.00	–0.080	–0.156
7.50	0.888	0.634	25.25	–0.080	–0.156
7.75	0.784	0.570	25.50	–0.080	–0.156
8.00	0.714	0.510	25.75	–0.079	–0.156
8.25	0.669	0.460	26.00	–0.079	–0.156
8.50	0.629	0.418	26.25	–0.079	–0.156
8.75	0.593	0.383	26.50	–0.079	–0.155

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Table 40–10—Normalized time domain voltage template 1 *(continued)*

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
9.00	0.561	0.354	26.75	–0.079	–0.155
9.25	0.533	0.330	27.00	–0.078	–0.155
9.50	0.507	0.309	27.25	–0.078	–0.155
9.75	0.483	0.292	27.50	–0.078	–0.154
10.00	0.462	0.268	27.75	–0.078	–0.154
10.25	0.443	0.239	28.00	–0.077	–0.154
10.50	0.427	0.223	28.25	–0.077	–0.153
10.75	0.411	0.213	28.50	–0.077	–0.153
11.00	0.398	0.208	28.75	–0.076	–0.153
11.25	0.385	0.204	29.00	–0.076	–0.152
11.50	0.374	0.201	29.25	–0.076	–0.152
11.75	0.364	0.199	29.50	–0.076	–0.152
12.00	0.355	0.198	29.75	–0.075	–0.151
12.25	0.346	0.197	30.00	–0.075	–0.151
12.50	0.339	0.196			

Table 40–11—Normalized time domain voltage template 2

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
–15.00	0.066	–0.025	18.00	0.891	0.779
–14.50	0.066	–0.025	18.50	0.886	0.773
–14.00	0.066	–0.025	19.00	0.881	0.767
–13.50	0.066	–0.025	19.50	0.876	0.762
–13.00	0.066	–0.025	20.00	0.871	0.756
–12.50	0.066	–0.025	20.50	0.866	0.750
–12.00	0.066	–0.025	21.00	0.861	0.745
–11.50	0.069	–0.025	21.50	0.856	0.739
–11.00	0.116	–0.025	22.00	0.852	0.734
–10.50	0.183	–0.025	22.50	0.847	0.728

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Table 40–11—Normalized time domain voltage template 2 *(continued)*

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
–10.00	0.261	–0.027	23.00	0.842	0.723
–9.50	0.348	–0.027	23.50	0.838	0.717
–9.00	0.452	–0.013	24.00	0.833	0.712
–8.50	0.535	0.130	24.50	0.828	0.707
–8.00	0.604	0.347	25.00	0.824	0.701
–7.50	0.683	0.451	25.50	0.819	0.696
–7.00	0.737	0.531	26.00	0.815	0.691
–6.50	0.802	0.610	26.50	0.811	0.686
–6.00	0.825	0.651	27.00	0.806	0.680
–5.50	0.836	0.683	27.50	0.802	0.675
–5.00	0.839	0.707	28.00	0.797	0.670
–4.50	0.839	0.725	28.50	0.793	0.665
–4.00	0.837	0.739	29.00	0.789	0.660
–3.50	0.832	0.747	29.50	0.784	0.655
–3.00	0.839	0.752	30.00	0.780	0.650
–2.50	0.856	0.755	30.50	0.776	0.645
–2.00	0.875	0.755	31.00	0.772	0.641
–1.50	0.907	0.758	31.50	0.767	0.636
–1.00	0.941	0.760	32.00	0.763	0.631
–0.50	0.966	0.803	32.50	0.759	0.626
0.00	0.986	0.869	33.00	0.755	0.621
0.50	1.001	0.890	33.50	0.751	0.617
1.00	1.014	0.912	34.00	0.747	0.612
1.50	1.022	0.933	34.50	0.743	0.607
2.00	1.025	0.954	35.00	0.739	0.603
2.50	1.025	0.970	35.50	0.734	0.598
3.00	1.025	0.967	36.00	0.730	0.594
3.50	1.025	0.962	36.50	0.727	0.589
4.00	1.025	0.956	37.00	0.723	0.585

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Table 40–11—Normalized time domain voltage template 2 *(continued)*

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
4.50	1.023	0.950	37.50	0.719	0.580
5.00	1.020	0.944	38.00	0.715	0.576
5.50	1.017	0.937	38.50	0.711	0.571
6.00	1.014	0.931	39.00	0.707	0.567
6.50	1.010	0.924	39.50	0.703	0.563
7.00	1.005	0.917	40.00	0.699	0.558
7.50	1.001	0.910	40.50	0.695	0.554
8.00	0.996	0.903	41.00	0.692	0.550
8.50	0.991	0.897	41.50	0.688	0.546
9.00	0.986	0.890	42.00	0.684	0.541
9.50	0.981	0.884	42.50	0.680	0.537
10.00	0.976	0.877	43.00	0.677	0.533
10.50	0.970	0.871	43.50	0.673	0.529
11.00	0.965	0.864	44.00	0.669	0.525
11.50	0.960	0.858	44.50	0.666	0.521
12.00	0.954	0.852	45.00	0.662	0.517
12.50	0.949	0.845	45.50	0.659	0.513
13.00	0.944	0.839	46.00	0.655	0.509
13.50	0.938	0.833	46.50	0.651	0.505
14.00	0.933	0.827	47.00	0.648	0.501
14.50	0.928	0.820	47.50	0.644	0.497
15.00	0.923	0.814	48.00	0.641	0.493
15.50	0.917	0.808	48.50	0.637	0.490
16.00	0.912	0.802	49.00	0.634	0.486
16.50	0.907	0.796	49.50	0.631	0.482
17.00	0.902	0.791	50.00	0.627	0.478
17.50	0.897	0.785			

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40.6.1.2.4 Transmitter distortion

When in test mode 4 and observing the differential signal output at the MDI using transmitter test fixture 3, for each pair, with no intervening cable, the peak distortion as defined below shall be less than 10 mV.

The peak distortion is determined by sampling the differential signal output with the symbol rate TX_TCLK at an arbitrary phase and processing a block of any 2047 consecutive samples with the MATLAB (see 1.3) code listed below or equivalent. Note that this code assumes that the differential signal has already been filtered by the test filter.

NOTE—The ASCII for the following MATLAB code is available from http://www.ieee802.org/3/publication/index.html.[10]

MATLAB code for Distortion Post Processing is as follows:

```
%
% Distortion Specification Post Processing
%

% Initialize Variables
clear
symbolRate=125e6;                                % symbol rate
dataFile=input('Data file name: ','s')

% Generate test pattern symbol sequence

scramblerSequence=ones(1,2047);
for i=12:2047
  scramblerSequence(i)=mod(scramblerSequence(i-11) + scramblerSequence(i-9),2);
end

for i=1:2047
  temp=scramblerSequence(mod(i-1,2047)+1) + ...
       2*mod(scramblerSequence(mod(i-2,2047)+1) + scramblerSequence(mod(i-5,2047)+1),2)
+ ...
      4*mod(scramblerSequence(mod(i-3,2047)+1) + scramblerSequence(mod(i-5,2047)+1),2);
  switch temp
    case 0,
      testPattern(i)=0;
    case 1,
      testPattern(i)=1;
    case 2,
      testPattern(i)=2;
    case 3,
      testPattern(i)=-1;
    case 4,
      testPattern(i)=0;
    case 5,
      testPattern(i)=1;
    case 6,
      testPattern(i)=-2;
    case 7,
      testPattern(i)=-1;
  end
end



% Input data file
fid=fopen(dataFile,'r');
sampledData=fscanf(fid,'%f');
```

[10]*Copyright release for MATLAB code*: Users of this standard may freely reproduce the MATLAB code in this subclause so it can be used for its intended purpose.

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```
fclose(fid);
sampledData=sampledData.';


if (length(sampledData) < 2047)
  error('Must have 2047 consecutive samples for processing');
elseif (length(sampledData) > 2047)
  fprintf(1,'\n Warning - only using first 2047 samples in data file');
  sampledData=sampledData(1:2047);
end


% Fit a sine wave to the data and temporarily remove it to yield processed data

options=foptions;
options(1)=0;
options(2)=1e-8;
options(3)=1e-8;
options(14)=2000;
gradfun=zeros(0);
P=fmins('sinefit',[2.0 0 125/6.],options,gradfun,sampledData,symbolRate);

P

processedData=sampledData - ...
    P(1)*sin(2*pi*(P(3)*1e6*[0:2046]/symbolRate + P(2)*1e-9*symbolRate));



% LMS Canceller

numberCoeff=70;  % Number of coefficients in canceller
coefficients=zeros(1,numberCoeff);
delayLine=testPattern;

% Align data in delayLine to sampled data pattern
temp=xcorr(processedData,delayLine);
index=find(abs(temp)==max(abs(temp)));
index=mod(mod(length(processedData) - index(1),2047)+numberCoeff-10,2047);
delayLine=[delayLine((end-index):end) delayLine(1:(end-index-1))];


% Compute coefficients that minimize squared error in cyclic block

for i=1:2047
  X(i,:)=delayLine(mod([0:(numberCoeff-1)]+i-1,2047)+1);
end
coefficients=(inv(X.' * X)*(processedData*X).').';



% Canceller
for i=1:2047
   err(i)=processedData(i)  -  sum(delayLine(1+mod((i-1):(i+numberCoeff-2),2047)).*coef-
ficients);
end

% Add back temporarily removed sine wave

err=err+P(1)*sin(2*pi*(P(3)*1e6*[0:2046]./symbolRate + P(2)*1e-9*symbolRate));


% Re-fit sine wave and do a final removal
```

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```
options=foptions;
options(1)=0;
options(2)=1e-12;
options(3)=1e-12;
options(14)=10000;
gradfun=zeros(0);
P=fmins('sinefit',[2.0 0 125/6.],options,gradfun,err,symbolRate);

P

processedData=sampledData - ...
    P(1)*sin(2*pi*(P(3)*1e6*[0:2046]/symbolRate + P(2)*1e-9*symbolRate));


% Compute coefficients that minimize squared error in cyclic block

coefficients=(inv(X.' * X)*(processedData*X).').';



% Canceller
for i=1:2047
   err(i)=processedData(i) - sum(delayLine(1+mod((i-1):(i+numberCoeff-2),2047)).*coef-
ficients);
end

% SNR Calculation
signal=0.5;
noise=mean(err.^2);

SNR=10*log10(signal./noise);

% Output Peak Distortion

peakDistortion=max(abs(err))


% Function for fitting sine wave
function err=sinefit(parameters,data,symbolRate)
err=sum((data- ...
    parameters(1)*sin(2*pi*(parameters(3)*1e6*[0:(length(data)-1)]/symbolRate + param-
eters(2)*1e-9*symbolRate))).^2);
```

40.6.1.2.5 Transmitter timing jitter

When in test mode 2 or test mode 3, the peak-to-peak jitter J_{txout} of the zero crossings of the differential signal output at the MDI relative to the corresponding edge of TX_TCLK is measured. The corresponding edge of TX_TCLK is the edge of the transmit test clock, in polarity and time, that generates the zero-crossing transition being measured.

When in the normal mode of operation as the MASTER, the peak-to-peak value of the MASTER TX_TCLK jitter relative to an unjittered reference shall be less than 1.4 ns. When the jitter waveform on TX_TCLK is filtered by a high-pass filter, $H_{jf1}(f)$, having the transfer function below, the peak-to-peak value of the resulting filtered timing jitter plus J_{txout} shall be less than 0.3 ns.

$$H_{jf1}(f) = \frac{jf}{jf + 5000} \qquad f \text{ in Hz}$$

When in the normal mode of operation as the SLAVE, receiving valid signals from a compliant PHY operating as the MASTER using the test channel defined in 40.6.1.1.1, with test channel port A connected to the SLAVE, the peak-to-peak value of the SLAVE TX_TCLK jitter relative to the MASTER TX_TCLK shall be less than 1.4 ns after the receiver is properly receiving the data and has set bit 10.13 of the GMII management register set to 1. When the jitter waveform on TX_TCLK is filtered by a high-pass filter, $H_{jf2}(f)$, having

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the transfer function below, the peak-to-peak value of the resulting filtered timing jitter plus J_{txout} shall be no more than 0.4 ns greater than the simultaneously measured peak-to-peak value of the MASTER jitter filtered by $H_{jf1}(f)$.

$$H_{jf2}(f) = \frac{jf}{jf + 32000} \qquad f \text{ in Hz}$$

NOTE—j denotes the square root of –1.

For all high-pass filtered jitter measurements, the peak-to-peak value shall be measured over an unbiased sample of at least 10^5 clock edges. For all unfiltered jitter measurements, the peak-to-peak value shall be measured over an interval of not less than 100 ms and not more than 1 second.

40.6.1.2.6 Transmit clock frequency

The quinary symbol transmission rate on each pair of the master PHY shall be 125.00 MHz ± 0.01%.

40.6.1.3 Receiver electrical specifications

The PMA shall provide the Receive function specified in 40.4.2.3 in accordance with the electrical specifications of this clause. The patch cabling and interconnecting hardware used in test configurations shall be within the limits specified in 40.7.

40.6.1.3.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 40.6.1.2 and have passed through a link specified in 40.7 are translated into one of the PMA_UNITDATA.indicate messages with a 4-D symbol error rate less than 10^{-10} and sent to the PCS after link reset completion. Since the 4-D symbols are not accessible, this specification shall be satisfied by a frame error rate less than 10^{-7} for 125 octet frames.

40.6.1.3.2 Receiver frequency tolerance

The receive feature shall properly receive incoming data with a 5-level symbol rate within the range 125.00 MHz ± 0.01%.

40.6.1.3.3 Common-mode noise rejection

This specification is provided to limit the sensitivity of the PMA receiver to common-mode noise from the cabling system. Common-mode noise generally results when the cabling system is subjected to electromagnetic fields. Figure 40–27 shows the test configuration, which uses a capacitive cable clamp, that injects common-mode signals into a cabling system.

A 100-meter, 4-pair Category 5 cable that meets the specification of 40.7 is connected between two 1000BASE-T PHYs and inserted into the cable clamp. The cable should be terminated on each end with an MDI connector plug specified in 40.8.1. The clamp should be located a distance of ~20 cm from the receiver. It is recommended that the cable between the transmitter and the cable clamp be installed either in a linear run or wrapped randomly on a cable rack. The cable rack should be at least 3 m from the cable clamp. In addition, the cable clamp and 1000BASE-T receiver should be placed on a common copper ground plane and the ground of the receiver should be in contact with the ground plane. The chassis grounds of all test equipment used should be connected to the copper ground plane. No connection is required between the copper ground plane and an external reference. A description of the cable clamp, as well as the validation procedure, can be found in Annex 40B.

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A signal generator with a 50 Ω impedance is connected to one end of the clamp and an oscilloscope with a 50 Ω input is connected to the other end of the clamp. The signal generator shall be capable of providing a sine wave signal of 1 MHz to 250 MHz. The output of the signal generator is adjusted for a voltage of 1.0 Vrms (1.414 Vpeak) on the oscilloscope.

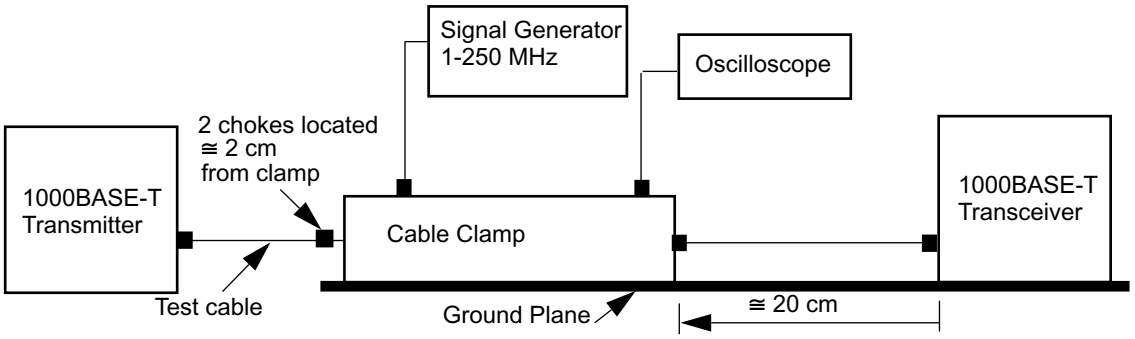


Figure 40–27—Receiver common-mode noise rejection test

While sending data from the transmitter, the receiver shall send the proper PMA_UNITDATA.indicate messages to the PCS as the signal generator frequency is varied from 1 MHz to 250 MHz.

NOTE—Although the signal specification is constrained within the 1–100 MHz band, this test is performed up to 250 MHz to ensure the receiver under test can tolerate out-of-band (100–250 MHz) noise.

40.6.1.3.4 Alien Crosstalk noise rejection

While receiving data from a transmitter specified in 40.6.1.2 through a link segment specified in 40.7 connected to all MDI duplex channels, a receiver shall send the proper PMA_UNITDATA.indicate message to the PCS when any one of the four pairs is connected to a noise source as described in Figure 40–28. Because symbol encoding is employed, this specification shall be satisfied by a frame error rate of less than 10^{-7} for 125 octet frames. The level of the noise signal at the MDI is nominally 25 mV peak-to-peak. (Measurements are to be made on each of the four pairs.) The noise source shall be connected to one of the MDI inputs using Category 5 balanced cable of a maximum length of 0.5 m.

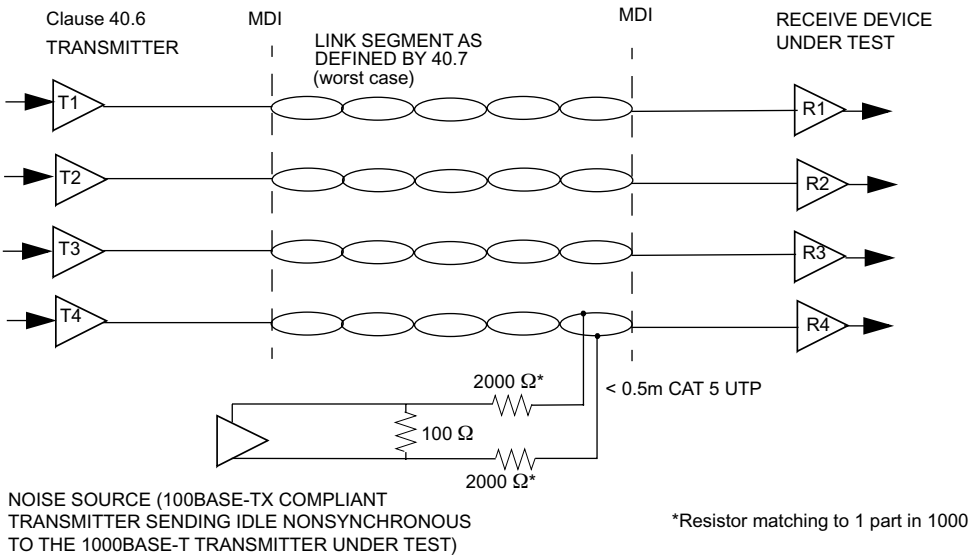


Figure 40–28—Differential mode noise rejection test

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40.7 Link segment characteristics

1000BASE-T is designed to operate over a 4-pair Category 5 balanced cabling system. Each of the four pairs supports an effective data rate of 250 Mbps in each direction simultaneously. The term “link segment” used in this clause refers to four duplex channels. The term “duplex channel” will be used to refer to a single channel with full duplex capability. Specifications for a link segment apply equally to each of the four duplex channels. All implementations of the balanced cabling link shall be compatible at the MDI.

40.7.1 Cabling system characteristics

The cabling system used to support 1000BASE-T requires 4 pairs of Category 5 balanced cabling with a nominal impedance of 100 Ω. The cabling system components (cables, cords, and connectors) used to provide the link segment shall consist of Category 5 components as specified in ANSI/TIA/EIA-568-A:1995 and ISO/IEC 11801:1995. Additionally:

a) 1000BASE-T uses a star topology with Category 5 balanced cabling used to connect PHY entities.
b) 1000BASE-T is an ISO/IEC 11801 Class D application, with additional installation requirements and transmission parameters specified in Annex 40A.
c) The width of the PMD transmit signal spectrum is approximately 80 MHz.
d) The use of shielding is outside the scope of this standard.

40.7.2 Link transmission parameters

The transmission parameters contained in this subclause are specified to ensure that a Category 5 link segment of up to at least 100 m will provide a reliable medium. The transmission parameters of the link segment include insertion loss, delay parameters, characteristic impedance, NEXT loss, ELFEXT loss, and return loss.

Link segment testing shall be conducted using source and load impedances of 100 Ω. The tolerance on the poles of the test filter used in this subclause shall be no worse than 1%.

40.7.2.1 Insertion loss

The insertion loss of each duplex channel shall be less than

$$\text{Insertion\_Loss}(f) < 2.1\ f^{0.529} + 0.4/f \quad \text{(dB)}$$

at all frequencies from 1 MHz to 100 MHz. This includes the attenuation of the balanced cabling pairs, including work area and equipment cables plus connector losses within each duplex channel. The insertion loss specification shall be met when the duplex channel is terminated in 100 Ω.

NOTE—The above equation approximates the insertion loss specification at discrete frequencies for Category 5 100-meter links specified in ANSI/TIA/EIA-568-A Annex E and in TIA/EIA TSB 67.

40.7.2.2 Differential characteristic impedance

The nominal differential characteristic impedance of each link segment duplex channel, which includes cable cords and connecting hardware, is 100 Ω for all frequencies between 1 MHz and 100 MHz.

40.7.2.3 Return loss

Each link segment duplex channel shall meet or exceed the return loss specified in the following equation at all frequencies from 1 MHz to 100 MHz

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$$\text{Return\_Loss}(f) \begin{cases} 15 & (1 - 20\ \text{MHz}) \\ 15 - 10\log_{10}(f/20) & (20 - 100\ \text{MHz}) \end{cases} \text{(dB)}$$

where f is the frequency in MHz. The reference impedance shall be 100 Ω.

40.7.3 Coupling parameters

In order to limit the noise coupled into a duplex channel from adjacent duplex channels, Near-End Crosstalk (NEXT) loss and Equal Level Far-End Crosstalk (ELFEXT) loss are specified for each link segment. Each duplex channel can be disturbed by more than one duplex channel. Requirements for Multiple Disturber Near-End Crosstalk (MDNEXT) are satisfied even when worst case conditions of differential pair-to-pair NEXT as specified under 40.7.3.1.1 occur. Therefore, there are no separate requirements for MDNEXT. Requirements for Multiple Disturber Equal-Level Far-End Crosstalk (MDELFEXT) loss are specified in 40.7.3.2.2.

40.7.3.1 Near-End Crosstalk (NEXT)

40.7.3.1.1 Differential Near-End Crosstalk

In order to limit the crosstalk at the near end of a link segment, the differential pair-to-pair Near-End Crosstalk (NEXT) loss between a duplex channel and the other three duplex channels is specified to meet the symbol error rate objective specified in 40.1. The NEXT loss between any two duplex channels of a link segment shall be at least

$$27.1 - 16.8\log_{10}(f/100)$$

where f is the frequency over the range of 1 MHz to 100 MHz.

NOTE—The above equation approximates the NEXT loss specification at discrete frequencies for Category 5 100-meter links specified in ANSI/TIA/EIA-568-A Annex E and in TSB-67.

40.7.3.2 Far-End Crosstalk (FEXT)

40.7.3.2.1 Equal Level Far-End Crosstalk (ELFEXT) loss

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk at the far end of each link segment duplex channel and meet the BER objective specified in 40.6.1.3.1. Far-End Crosstalk (FEXT) is crosstalk that appears at the far end of a duplex channel (disturbed channel), which is coupled from another duplex channel (disturbing channel) with the noise source (transmitters) at the near end. FEXT loss is defined as

$$\text{FEXT\_Loss}(f) = 20\log_{10}[V\text{pds}(f)/V\text{pcn}(f)]$$

and ELFEXT_Loss is defined as

$$\text{ELFEXT\_Loss}(f) = 20\log_{10}[V\text{pds}(f)/V\text{pcn}(f)] - \text{SLS\_Loss}(f)$$

where

*V*pds	is the peak voltage of disturbing signal (near-end transmitter)
*V*pcn	is the peak crosstalk noise at far end of disturbed channel
SLS_Loss	is the insertion loss of disturbed channel in dB

The worst pair ELFEXT loss between any two duplex channels shall be greater than $17 - 20\log_{10}(f/100)$ dB where f is the frequency over the range of 1 MHz to 100 MHz.

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40.7.3.2.2 Multiple Disturber Equal Level Far-End Crosstalk (MDELFEXT) loss

Since four duplex channels are used to transfer data between PMDs, the FEXT that is coupled into a data carrying channel will be from the three adjacent disturbing duplex channels. This specification is consistent with three channel-to-channel disturbers—one with a ELFEXT loss of at least $17 - 20\log_{10}(f/100)$ dB, one with a ELFEXT loss of at least $19.5 - 20\log_{10}(f/100)$ dB, and one with a ELFEXT loss of at least $23 - 20\log_{10}(f/100)$ dB. To ensure the total FEXT coupled into a duplex channel is limited, multiple disturber ELFEXT loss is specified as the power sum of the individual ELFEXT losses.

The Power Sum loss between a duplex channel and the three adjacent disturbers shall be

$$\text{PSELFEXT loss} > 14.4 - 20\log_{10}(f/100)\ \text{dB}$$

where f is the frequency over the range of 1 MHz to 100 MHz.

40.7.3.2.3 Multiple-Disturber Power Sum Equal Level Far-End Crosstalk (PSELFEXT) loss

PSELFEXT loss is determined by summing the magnitude of the three individual pair-to-pair differential ELFEXT loss values over the frequency range 1 to 100 MHz as follows:

$$\text{PSELFEXT\_Loss(f)} = -10\log_{10}\sum_{i=1}^{i=3} 10^{-(NL(f)i)/10}$$

where

NL(f)i is the magnitude of ELFEXT loss at frequency f of pair combination i
i is the 1, 2, or 3 (pair-to-pair combination)

40.7.4 Delay

In order to simultaneously send data over four duplex channels in parallel, the propagation delay of each duplex channel as well as the difference in delay between any two of the four channels are specified. This ensures the 1000 Mbps data that is divided across four channels can be properly reassembled at the far-end receiver. This also ensures the round-trip delay requirement for effective collision detection is met.

40.7.4.1 Maximum link delay

The propagation delay of a link segment shall not exceed 570 ns at all frequencies between 2 MHz and 100 MHz.

40.7.4.2 Link delay skew

The difference in propagation delay, or skew, between all duplex channel pair combinations of a link segment, under all conditions, shall not exceed 50 ns at all frequencies from 2 MHz to 100 MHz. It is a further functional requirement that, once installed, the skew between any two of the four duplex channels due to environmental conditions shall not vary more than 10 ns within the above requirement.

40.7.5 Noise environment

The 1000BASE-T noise environment consists of noise from many sources. The primary noise sources that impact the objective BER are NEXT and echo interference, which are reduced to a small residual noise using cancelers. The remaining noise sources, which are secondary sources, are discussed in the following list.

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The 1000BASE-T noise environment consists of the following:

a) Echo from the local transmitter on the same duplex channel (cable pair). Echo is caused by the hybrid function used to achieve simultaneous bi-directional transmission of data and by impedance discontinuities in the link segment. It is impractical to achieve the objective BER without using echo cancellation. Since the symbols transmitted by the local disturbing transmitter are available to the cancellation processor, echo interference can be reduced to a small residual noise using echo cancellation methods.

b) Near-End Crosstalk (NEXT) interference from the local transmitters on the duplex channels (cable pairs) of the link segment. Each receiver will experience NEXT interference from three adjacent transmitters. NEXT cancelers are used to reduce the interference from each of the three disturbing transmitters to a small residual noise. NEXT cancellation is possible since the symbols transmitted by the three disturbing local transmitters are available to the cancellation processor. NEXT cancelers can reduce NEXT interference by at least 20 dB.

c) Far-End Crosstalk (FEXT) noise at a receiver is from three disturbing transmitters at the far end of the duplex channel (cable pairs) of the link segment. FEXT noise can be cancelled in the same way as echo and NEXT interference although the symbols from the remote transmitters are not immediately available. However, FEXT noise is much smaller than NEXT interference and can generally be tolerated.

d) Inter-Symbol Interference (ISI) noise. ISI is the extraneous energy from one signaling symbol that interferes with the reception of another symbol on the same channel.

e) Noise from non-idealities in the duplex channel, transmitters, and receivers; for example, DAC/ADC non-linearity, electrical noise (shot and thermal), and non-linear channel characteristics.

f) Noise from sources outside the cabling that couple into the link segment via electric and magnetic fields.

g) Noise from signals in adjacent cables. This noise is referred to as alien NEXT noise and is generally present when cables are bound tightly together. Since the transmitted symbols from the alien NEXT noise source are not available to the cancellation processor (they are in another cable), it is not possible to cancel the alien NEXT noise. To ensure robust operation the alien NEXT noise must meet the specification of 40.7.5.1.

40.7.6 External coupled noise

The noise coupled from external sources that is measured at the output of a filter connected to the output of the near end of a disturbed duplex channel should not exceed 40 mV peak-to-peak. The filter for this measurement is a fifth order Butterworth filter with a 3 dB cutoff at 100MHz.

40.8 MDI specification

This subclause defines the MDI. The link topology requires a crossover function in a DTE-to-DTE connection. See 40.4.4 for a description of the automatic MDI/MDI-X configuration.

40.8.1 MDI connectors

Eight-pin connectors meeting the requirements of subclause 3 and Figures 1 through 4 of IEC 60603-7: 1990 shall be used as the mechanical interface to the balanced cabling. The plug connector shall be used on the balanced cabling and the jack on the PHY. These connectors are depicted (for informational use only) in Figure 40–29 and Figure 40–30. The assignment of PMA signals to connector contacts for PHYs is shown in Table 40-12.

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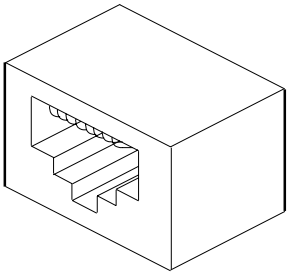


Figure 40–29—MDI connector

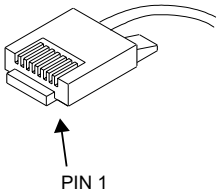


Figure 40–30—Balanced cabling connector

Table 40–12—Assignment of PMA signal to MDI and MDI-X pin-outs

Contact	MDI	MDI-X
1	BI_DA+	BI_DB+
2	BI_DA–	BI_DB–
3	BI_DB+	BI_DA+
4	BI_DC+	BI_DD+
5	BI_DC–	BI_DD–
6	BI_DB–	BI_DA–
7	BI_DD+	BI_DC+
8	BI_DD–	BI_DC–

40.8.2 Crossover function

Although the automatic MDI/MDI-X configuration (see 40.4.4) is not required for successful operation of 1000BASE-T, it is a functional requirement that a crossover function be implemented in every link segment to support the operation of Auto-Negotiation. The crossover function connects the transmitters of one PHY to the receivers of the PHY at the other end of the link segment. Crossover functions may be implemented internally to a PHY or else-where in the link segment. For a PHY that does not implement the crossover function, the MDI labels in the middle column of Table 40–12 refer to its own internal circuits. For PHYs that do implement the internal crossover, the MDI labels in the last column of Table 40–12 refer to the internal circuits of the remote PHY of the link segment. Additionally, the MDI connector for a PHY that implements the crossover function shall be marked with the graphical symbol X. The crossover function specified here is not compatible with the crossover function specified in 14.5.2 for pairs TD and RD.

When a link segment connects a single-port device to a multiport device, it is recommended that the crossover be implemented in the PHY local to the multiport device. If neither or both PHYs of a link segment contain internal crossover functions, an additional external crossover is necessary. It is recommended that the crossover be visible to an installer from one of the PHYs. When both PHYs contain internal crossovers,

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it is further recommended that, in networks in which the topology identifies either a central backbone segment or a central device, the PHY furthest from the central element be assigned the external crossover to maintain consistency.

Implicit implementation of the crossover function within a twisted-pair cable or at a wiring panel, while not expressly forbidden, is beyond the scope of this standard.

40.8.3 MDI electrical specifications

The MDI connector (jack) when mated with a specified balanced cabling connector (plug) shall meet the electrical requirements for Category 5 connecting hardware for use with 100-ohm Category 5 cable as specified in ANSI/TIA/EIA-568-A:1995 and ISO/IEC 11801:1995.

The mated MDI/balanced cabling connector pair shall have a FEXT loss not less than $40 - 20\log_{10}(f/100)$ (where f is the frequency over the range 1 MHz to 100 MHz) between all contact pair combinations shown in Table 40–12.

No spurious signals shall be emitted onto the MDI when the PHY is held in power-down mode (as defined in 22.2.4.1.5) independent of the value of TX_EN, when released from power-down mode, or when external power is first applied to the PHY.

40.8.3.1 MDI return loss

The differential impedance at the MDI for each transmit/receive channel shall be such that any reflection due to differential signals incident upon the MDI from a balanced cabling having an impedance of 100 Ω ± 15% is attenuated, relative to the incident signal, at least 16 dB over the frequency range of 1.0 MHz to 40 MHz and at least $10 - 20\log_{10}(f/80)$ dB over the frequency range 40 MHz to 100 MHz (f in MHz). This return loss shall be maintained at all times when the PHY is transmitting data or control symbols.

40.8.3.2 MDI impedance balance

Impedance balance is a measurement of the impedance-to-ground difference between the two MDI contacts used by a duplex link channel and is referred to as common-mode-to-differential-mode impedance balance. Over the frequency range 1.0 MHz to 100.0 MHz, the common-mode-to-differential-mode impedance balance of each channel of the MDI shall exceed

$$34 - 19.2\log_{10}\left(\frac{f}{50}\right) \quad \text{dB}$$

where f is the frequency in MHz when the transmitter is transmitting random or pseudo random data. Test-mode 4 may be used to generate an appropriate transmitter output.

The balance is defined as

$$20\log_{10}\left(\frac{E_{cm}}{E_{dif}}\right)$$

where E_{cm} is an externally applied sine wave voltage as shown in Figure 40–31 and E_{dif} is the resulting waveform due only to the applied sine wave and not the transmitted data.

NOTES

1—Triggered averaging can be used to separate the component due to the applied common-mode sine wave from the transmitted data component.

2—The imbalance of the test equipment (such as the matching of the test resistors) must be insignificant relative to the balance requirements.

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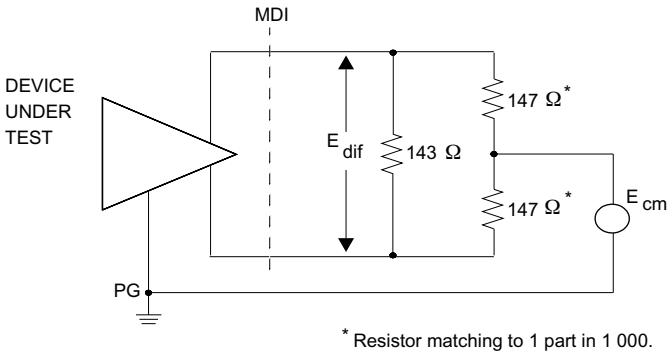


Figure 40–31—MDI impedance balance test circuit

40.8.3.3 MDI common-mode output voltage

The magnitude of the total common-mode output voltage, E_{cm_out}, on any transmit circuit, when measured as shown in Figure 40–32, shall be less than 50 mV peak-to-peak when transmitting data.

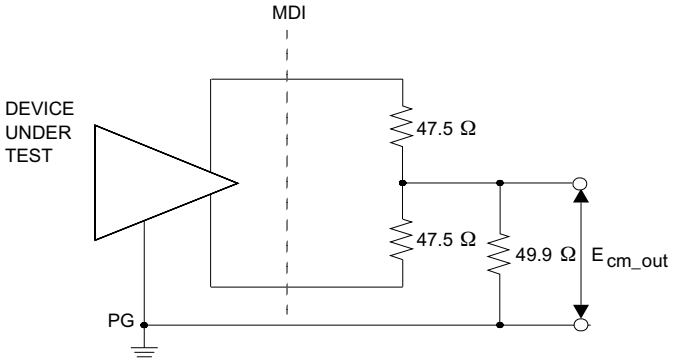


Figure 40–32—Common-mode output voltage test circuit

NOTE—The imbalance of the test equipment (such as the matching of the test resistors) must be insignificant relative to the balance requirements.

40.8.3.4 MDI fault tolerance

Each wire pair of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of any wire to any other wire within the 4-pair cable for an indefinite period of time and shall resume normal operation after the short circuit(s) are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

Each wire pair shall withstand without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity (as indicated in Figure 40–33). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

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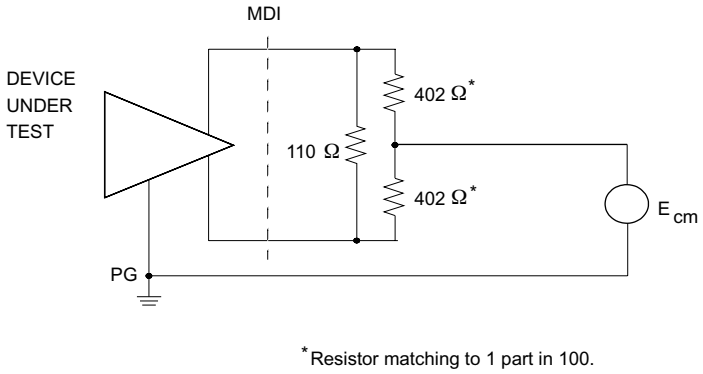


Figure 40–33—MDI fault tolerance test circuit

40.9 Environmental specifications

40.9.1 General safety

All equipment meeting this standard shall conform to IEC 60950: 1991.

40.9.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cabling systems described in this subclause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cabling and components.
c) High-energy transients coupled onto the LAN cabling system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network.

40.9.2.1 Installation

It is a mandatory requirement that sound installation practice, as defined by applicable local codes and regulations, is followed in every instance in which such practice is applicable.

40.9.2.2 Installation and maintenance guidelines

It is a mandatory requirement that, during installation and maintenance of the cabling plant, care is taken to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

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40.9.2.3 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 1000BASE-T equipment. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply:

Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400 Ω source impedance.

Ringing voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 Ω source resistance. The dc component is 56 Vdc with a 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 1000BASE-T equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE—Wiring errors may impose telephony voltages differentially across 1000BASE-T transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, receivers will generally appear to the telephone system as off-hook telephones. Therefore, full-ring voltages will be applied for only short periods. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to the low resistance of the transformer coil.

40.9.3 Environment

40.9.3.1 Electromagnetic emission

A system integrating the 1000BASE-T PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.

40.9.3.2 Temperature and humidity

A system integrating the 1000BASE-T PHY is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

40.10 PHY labeling

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Data rate capability in Mb/s
b) Power level in terms of maximum current drain (for external PHYs)
c) Port type (i.e., 1000BASE-T)
d) Any applicable safety warnings

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40.11 Delay constraints

In half duplex mode, proper operation of a CSMA/CD LAN demands that there be an upper bound on the propagation delays through the network. This implies that MAC, PHY, and repeater implementors must conform to certain delay minima and maxima, and that network planners and administrators conform to constraints regarding the cabling topology and concatenation of devices. MAC constraints are specified in 35.2.4. Topological constraints are contained in Clause 42.

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementors must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The reference point for all MDI measurements is the peak point of the mid-cell transition corresponding to the reference code-bit, as measured at the MDI.

40.11.1 MDI to GMII delay constraints

Every 1000BASE-T PHY associated with a GMII shall comply with the bit delay constraints specified in Table 40–13 for half duplex operation and Table 40–14 for full duplex operation. These constraints apply for all 1000BASE-T PHYs. For any given implementation, the assertion and de-assertion delays on CRS shall be equal.

Table 40–13—MDI to GMII delay constraints (half duplex mode)

Sublayer measurement points	Event	Min (bit times)	Max (bit times)	Input timing reference	Output timing reference
GMII ⇔ MDI	TX_EN Sampled to MDI Output	—	84	GTX_CLK rising	1st symbol of SSD/CSReset/ CSExtend/ CSExtend_Err
	MDI input to CRS assert	—	244	1st symbol of SSD/CSReset	—
	MDI input to CRS de-assert	—	244	1st symbol of SSD/CSReset	—
	MDI input to COL assert	—	244	1st symbol of SSD/CSReset	—
	MDI input to COL de-assert	—	244	1st symbol of SSD/CSReset	—
	TX_EN sampled to CRS assert	—	16	GTX_CLK rising	—
	TX_EN sampled to CRS de-assert	—	16	GTX_CLK rising	—

40.11.2 DTE delay constraints (half duplex only)

Every DTE with a 1000BASE-T PHY shall comply with the bit delay constraints specified in Table 40–15 for half duplex operation.

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Table 40–14—MDI to GMII delay constraints (full duplex mode)

Sublayer measurement points	Event	Min (bit times)	Max (bit times)	Input timing reference	Output timing reference
GMII ⇔ MDI	TX_EN Sampled to MDI Output	—	84	GTX_CLK rising	1st symbol of SSD/CSReset/ CSExtend/ CSExtend_Err
	MDI input to RX_DV de-assert	—	244	1st symbol of CSReset	—

Table 40–15— DTE delay constraints (half duplex mode)

Sublayer measurement points	Event	Min (bit times)	Max (bit times)	Input timing reference	Output timing reference
MAC ⇔ MDI	MAC transmit start to MDI output	—	132	—	1st symbol of SSD
	MDI input to collision detect	—	292	1st symbol of SSD	—
	MDI input to MDI output (nondeferred or Jam)	—	440	1st symbol of SSD	1st symbol of SSD
	MDI Input to MDI output (worse-case non-deferred transmit)	—	440	1st symbol of SSD	1st symbol of SSD

40.11.3 Carrier de-assertion/assertion constraint (half duplex mode)

To ensure fair access to the network, each DTE operating in half duplex mode shall, additionally, satisfy the following: (MAX MDI to MAC Carrier De-assert Detect) – (MIN MDI to MAC Carrier Assert Detect) < 16 Bit Times.

40.12 Protocol implementation conformance statement (PICS) proforma for Clause 40—Physical coding sublayer (PCS), physical medium attachment (PMA) sublayer and baseband medium, type 1000BASE-T[11]

The supplier of a protocol implementation that is claimed to conform to this clause shall complete the Protocol Implementation Conformance Statement (PICS) proforma listed in the following subclauses.

Instructions for interpreting and filling out the PICS proforma may be found in Clause 21.

[11]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so it can be used for its intended purpose and may further publish the completed PICS.

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40.12.1 Identification

40.12.1.1 Implementation identification

Supplier	
Contact point for queries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTES 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

40.12.1.2 Protocol summary

Identification of protocol specification	IEEE Std 802.3-2002, Clause 40, Physical coding sublayer (PCS), physical medium attachment (PMA) sublayer, and baseband medium, type 1000BASE-T
Identification of amendments and corrigenda to this PICS proforma which have been completed as part of this PICS	
Have any Exceptions items been required? No [ ] Yes [ ] (See Clause 21—The answer Yes means that the implementation does not conform to the standard)	
Date of Statement	

40.12.2 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*GMII	PHY associated with GMII	40.1	O	Yes [ ] No [ ]	
*DTE	DTE with PHY not associated with GMII	40.1	O	Yes [ ] No [ ]	
AN	Support for Auto-Negotiation (Clause 28)	40.5.1	M	Yes [ ]	Required
OMS	Operation as MASTER or SLAVE	40.5.1	M	Yes [ ]	Required
*FDX	PHY supports full duplex mode	40.1	O	Yes [ ] No [ ]	
*HDX	PHY support half duplex mode	40.1	O	Yes [ ] No [ ]	
*INS	Installation / cabling	40.7	O	Yes [ ] No [ ]	Items marked with INS include installation practices and cabling specifications not applicable to a PHY manufacturer.
*AXO	Auto-Crossover	40.4.4	O	Yes [ ] No [ ]	PHY supports auto-crossover

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40.12.3 Clause conventions

Item	Feature	Subclause	Status	Support	Value/Comment
CCO1	The values of all components in test circuits shall be	40.1.6	M	Yes [ ]	Accurate to within ±1% unless otherwise stated.

40.12.4 Physical Coding Sublayer (PCS)

Item	Feature	Subclause	Status	Support	Value/Comment
PCT1	The PCS shall	40.3.1.2	M	Yes [ ]	Implement the Data Transmission Enabling process as depicted in Figure 40–8 including compliance with the associated state variables specified in 40.3.3.
PCT2	PCS Transmit function shall	40.3.1.3	M	Yes [ ]	Conform to the PCS Transmit state diagram in Figure 40–9.
PCT3	PCS Transmit shall	40.4.5.1	M	Yes [ ]	Send code-groups according to the value assumed by the tx_mode variable.
PCT4	If the parameter config provided to the PCS by the PHY Control function via the PMA_CONFIG.indicate message assumes the value MASTER, PCS Transmit shall	40.3.1.3.1	M	Yes [ ]	Employ the transmitter side-stream scrambler generator polynomial specified for use with MASTER in 40.3.1.3.1.
PCT5	If the parameter config provided to the PCS by the PHY Control function via the PMA_CONFIG.indicate message assumes the value SLAVE, PCS Transmit shall	40.3.1.3.1	M	Yes [ ]	Employ the transmitter side-stream scrambler generator polynomial specified for use with SLAVE in 40.3.1.3.1.
PCT6	In no case shall	40.3.1.3.1	M	Yes [ ]	The scrambler state be initialized to all zeros.
PCT7	If tx_error_n=1 when the condition (tx_enable_n * tx_enable_{n-2}) = 1, error indication is signaled by means of symbol substitution, wherein the values of $Sd_n[5:0]$ are ignored during mapping and the symbols corresponding to the row denoted as “xmt_err” in Table 40–1 and Table 40–2 shall be used.	40.3.1.3.5	M	Yes [ ]	

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Item	Feature	Subclause	Status	Support	Value/Comment
PCT8	If tx_error_n=0 when the variable $csreset_n$ = 1, the convolutional encoder reset condition is normal. This condition is indicated by means of symbol substitution, where the values of Sd_n[5:0] are ignored during mapping and the symbols corresponding to the row denoted as “CSReset” in Table 40–1 and Table 40–2 shall be used.	40.3.1.3.5	M	Yes [ ]	
PCT9	If tx_error_n=1 is asserted when the variable $csreset_n$ = 1, the convolutional encoder reset indicates carrier extension. In this condition, the values of Sd_n[5:0] are ignored during mapping and the symbols corresponding to the row denoted as “CSExtend” in Table 40–1 and Table 40–2 shall be used when TXD_n = 0x’0F, and the row denoted as “CSExtend_Err” in Table 40–1 and Table 40–2 shall be used when $TXD_n \neq$ 0x’0F.	40.3.1.3.5	M	Yes [ ]	
PCT10	In case carrier extension with error is indicated during the first octet of CSReset, the error condition shall be encoded during the second octet of CSReset, and during the subsequent two octets of the End-of-Stream delimiter.	40.3.1.3.5	M	Yes [ ]	
PCT11	The symbols corresponding to the SSD1 row in Table 40–1 shall be used when the condition (tx_enable_n) * (!tx_enable_{n-1}) = 1.	40.3.1.3.5	M	Yes [ ]	
PCT12	The symbols corresponding to the SSD2 row in Table 40–1 shall be used when the condition (tx_enable_{n-1})* (!tx_enable_{n-2}) = 1.	40.3.1.3.5	M	Yes [ ]	
PCT13	If carrier extend error is indicated during ESD, the symbols corresponding to the ESD_Ext_Err row in Table 40–1 shall be used.	40.3.1.3.5	M	Yes [ ]	
PCT14	The symbols corresponding to the ESD1 row in Table 40–1 shall be used when the condition (!tx_enable_{n-2}) * (tx_enable_{n-3}) = 1, in the absence of carrier extend error indication at time n.	40.3.1.3.5	M	Yes [ ]	

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Item	Feature	Subclause	Status	Support	Value/Comment
PCT15	The symbols corresponding to the ESD2_Ext_0 row in shall be used when the condition (!tx_enable_{n-3}) * (tx_enable_{n-4}) * (!tx_error_{n}) * (!tx_error_{n-1}) = 1.	40.3.1.3.5	M	Yes [ ]	
PCT16	The symbols corresponding to the ESD2_Ext_1 row in Table 40–1 shall be used when the condition (!tx_enable_{n-3}) * (tx_enable_{n-4}) * (!tx_error_{n}) * (tx_error_{n-1}) * (tx_error_{n-2}) * (tx_error_{n-3})= 1.	40.3.1.3.5	M	Yes [ ]	
PCT17	The symbols corresponding to the ESD2_Ext_2 row in Table 40–1 shall be used when the condition (!tx_enable_{n-3}) * (tx_enable_{n-4}) * (tx_error_{n}) * (tx_error_{n-1}) * (tx_error_{n-2}) * (tx_error_{n-3}) * (TXD_{n}=0x0F)= 1, in the absence of carrier extend error indication.	40.3.1.3.5	M	Yes [ ]	

40.12.4.1 PCS receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCR1	PCS Receive function shall	40.3.1.4	M	Yes [ ]	Conform to the PCS Receive state diagram shown in Figure 40–10a including compliance with the associated state variables as specified in 40.3.3.
PCR2	The PHY shall	40.3.1.4.2	M	Yes [ ]	Descramble the data stream and return the proper sequence of data bits RXD<7:0> to the GMII.
PCR3	For side-stream descrambling, the MASTER PHY shall employ	40.3.1.4.2	M	Yes [ ]	The receiver scrambler generator polynomial specified for MASTER operation in 40.3.1.4.2.
PCR4	For side-stream descrambling, the SLAVE PHY shall employ	40.3.1.4.2	M	Yes [ ]	The receiver scrambler generator polynomial specified for SLAVE operation in 40.3.1.4.2.

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40.12.4.2 Other PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCO1	The PCS Reset function shall	40.3.1.1	M	Yes [ ]	Be executed any time “power on” or receipt of a request for reset from the management entity occurs, including compliance with the associated state variables as specified in 40.3.3.
PCO2	The PCS shall	40.3.1.5	M	Yes [ ]	Implement the Carrier Sense process as depicted in Figure 40–11, including compliance with the associated state variables as specified in 40.3.3.
PCO3	Symb-timer shall be generated	40.3.3.3	M	Yes [ ]	Synchronously with TX_TCLK.

40.12.5 Physical Medium Attachment (PMA)

Item	Feature	Subclause	Status	Support	Value/Comment
PMF1	PMA Reset function shall be executed	40.4.2.1	M	Yes [ ]	At power on and upon receipt of a reset request from the management entity or from PHY Control.
PMF2	PMA Transmit shall	40.4.2.2	M	Yes [ ]	Continuously transmit onto the MDI pulses modulated by the quinary symbols given by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD], respectively.
PMF3	The four transmitters shall be driven by the same transmit clock, TX_TCLK	40.4.2.2	M	Yes [ ]	
PMF4	PMA Transmit shall	40.4.2.2	M	Yes [ ]	Follow the mathematical description given in 40.4.3.1.
PMF5	PMA Transmit shall comply with	40.4.2.2	M	Yes [ ]	The electrical specifications given in 40.6.
PMF6	When the PMA_CONFIG.indicate parameter config is MASTER, the PMA Transmit function shall	40.4.2.2	M	Yes [ ]	Source the transmit clock TX_TCLK from a local clock source while meeting the transmit jitter requirements of 40.6.1.2.5.

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Item	Feature	Subclause	Status	Support	Value/Comment
PMF7	When the PMA_CONFIG.indicate parameter config is SLAVE, the PMA Transmit function shall	40.4.2.2	M	Yes [ ]	Source the transmit clock TX_TCLK from the recovered clock of 40.4.2.5 while meeting the jitter requirements of 40.6.1.2.5.
PMF8	PMA Receive function shall	40.4.2.3	M	Yes [ ]	Translate the signals received on pairs BI_DA BI_DB, BI_DC and BI_DD into the PMA_UNITDATA.indicate parameter rx_symb_vector with a symbol error rate of less than one part in 10^{10}.
PMF9	PHY Control function shall	40.4.2.4	M	Yes [ ]	Comply with the state diagram descriptions given in Figure 40–15.
PMF10	The Link Monitor function shall	40.4.2.5	M	Yes [ ]	Comply with the state diagram shown in Figure 40–16.
PMF11	Clock Recovery function shall provide	40.4.2.6	M	Yes [ ]	Provide clocks suitable for signal sampling on each line so that the symbol-error rate indicated in 40.4.2.3 is achieved.
PMF12	The symbol response shall comply with	40.4.3.1	M	Yes [ ]	The electrical specifications given in 40.6.
PMF13	The four signals received on pairs BI_DA, BI_DB, BI_DC, and BI_DD shall be processed within the PMA Receive function to yield	40.4.3.2	M	Yes [ ]	The quinary received symbols rx_symb_vector[BI_DA], rx_symb_vector[BI_DB], rx_symb_vector[BI_DC], and rx_symb_vector[BI_DD].
PMF14	If an automatic configuration method is used, it shall	40.4.4	M	Yes [ ]	Comply with the specifications of 40.4.4.
PMF15	The PMA shall	40.4.5.1	M	Yes [ ]	Generate the config variable continuously and pass it to the PCS via the PMA_CONFIG.indicate primitive.
PMF16	The variable link_det shall take the value	40.4.5.1	AXO:M	N/A [ ] Yes [ ]	TRUE or FALSE as per 40.4.4.1.
PMF17	The variable MDI_status shall take the value	40.4.5.1	AXO:M	N/A [ ] Yes [ ]	MDI or MDI-X as per Table 40–12.
PMF18	PCS Transmit shall	40.4.5.1	M	Yes [ ]	Send code-groups according to the value assumed by tx_mode.
PMF19	The A_timer shall have a period of	40.4.5.2	AXO:M	N/A [ ] Yes [ ]	1.3s ± 25%.
PMF20	The maxwait_timer timer shall expire	40.4.5.2	M	Yes [ ]	750 ± 10 ms if config = MASTER or 350 ± 5ms if config = SLAVE

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Item	Feature	Subclause	Status	Support	Value/Comment
PMF21	The minwait_timer timer shall expire	40.4.5.2	M	Yes [ ]	1 ±0.1μs after being started.
PMF22	The sample_timer shall have a period of	40.4.5.2	AXO:M	N/A [ ] Yes [ ]	62 ± 2ms.
PMF23	The stabilize_timer shall expire	40.4.5.2	M	Yes [ ]	1 ± 0.1 μs after being started.

40.12.6 Management interface

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	All 1000BASE-T PHYs shall provide support for Auto-Negotiation (Clause 28) and shall be capable of operating as MASTER or SLAVE.	40.5.1	M	Yes [ ]	
MF2	A 100BASE-T PHY shall	40.5.1.1	M	Yes [ ]	Use the management register definitions and values specified in Table 40–3.

40.12.6.1 1000BASE-T Specific Auto-Negotiation Requirements

Item	Feature	Subclause	Status	Support	Value/Comment
AN1	1000BASE-T PHYs shall	40.5.1.2	M	Yes [ ]	Exchange one Auto-Negotiation Base Page, a 1000BASE-T formatted Next Page, and two 1000BASE-T unformatted Next Pages in sequence, without interruption, as specified in Table 40–4.
AN2	The MASTER-SLAVE relationship shall be determined during Auto-Negotiation	40.5.2	M	Yes [ ]	Using Table 40–5 with the 1000BASE-T Technology Ability Next Page bit values specified in Table 40–4 and information received from the link partner.
AN3	Successful completion of the MASTER-SLAVE resolution shall	40.5.2	M	Yes [ ]	Be treated as MASTER-SLAVE configuration resolution complete.
AN4	A seed counter shall be provided to	40.5.2	M	Yes [ ]	Track the number of seed attempts.
AN5	At start-up, the seed counter shall be set to	40.5.2	M	Yes [ ]	Zero.
AN6	The seed counter shall be incremented	40.5.2	M	Yes [ ]	Every time a new random seed is sent.

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Item	Feature	Subclause	Status	Support	Value/Comment
AN7	When MASTER-SLAVE resolution is complete, the seed counter shall be reset to 0 and bit 10.15 shall be set to logical zero.	40.5.2	M	Yes [ ]	
AN8	Maximum seed attempts before declaring a MASTER_SLAVE configuration Resolution Fault	40.5.2	M	Yes [ ]	Seven.
AN9	During MASTER_SLAVE configuration, the device with the higher seed value shall	40.5.2	M	Yes [ ]	Become the MASTER.
AN10	During MASTER_SLAVE configuration, the device with the lower seed value shall	40.5.2	M	Yes [ ]	Become the SLAVE.
AN11	Both PHYs set in manual mode to be either MASTER or SLAVE shall be treated as	40.5.2	M	Yes [ ]	MASTER-SLAVE resolution fault (failure) condition.
AN12	MASTER-SLAVE resolution fault (failure) condition shall result in	40.5.2	M	Yes [ ]	MASTER-SLAVE Configuration Resolution Fault bit (10.15) to be set to logical one.
AN13	MASTER-SLAVE Configuration resolution fault condition shall be treated as	40.5.2	M	Yes [ ]	MASTER-SLAVE Configuration Resolution complete.
AN14	MASTER-SLAVE Configuration resolution fault condition shall	40.5.2	M	Yes [ ]	Cause link_status_1000BASE-T to be set to FAIL.

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40.12.7 PMA Electrical Specifications

Item	Feature	Subclause	Status	Support	Value/Comment
PME15	The PHY shall provide electrical isolation between	40.6.1.1	M	Yes [ ]	The port device circuits including frame ground, and all MDI leads.
PME16	PHY-provided electrical separation shall withstand at least one of three electrical strength tests	40.6.1.1	M	Yes [ ]	a) 1500 V rms at 50Hz to 60Hz for 60 s, applied as specified in Section 5.3.2 of IEC 60950:1991. b) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC 60950: 1991. c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs. (1.2 μs virtual front time, 50 μs virtual time or half value), as defined in IEC 60060.
PME17	There shall be no insulation breakdown as defined in Section 5.3.2 of IEC 60950, during the test.	40.6.1.1	M	Yes [ ]	
PME18	The resistance after the test shall be at least	40.6.1.1	M	Yes [ ]	2 MΩ, measured at 500 Vdc.
PME19	The transmitter MASTER-SLAVE timing jitter test channel shall	40.6.1.1.1	M	Yes [ ]	Be constructed by combining 100 Ω and 120 Ω cable segments that meet or exceed ISO.IEC 11801 Category 5 specifications for each pair as shown in Figure 40–18 with the lengths and additional restrictions on parameters described in Table 40–6.
PME20	The ends of the MASTER-SLAVE timing jitter test channel shall	40.6.1.1.1	M	Yes [ ]	Be connectorized with connectors meeting or exceeding ANSI/TIA/EIA-568-A:1995 or ISO/IEC 11801:1995 Category 5 specifications.
PME21	The return loss of the MASTER-SLAVE timing jitter test channel shall	40.6.1.1.1	M	Yes [ ]	Meet the return loss requirements of 40.7.2.3.
PME22	The return loss of the MASTER-SLAVE timing jitter test channel shall	40.6.1.1.1	M	Yes [ ]	Meet the crosstalk requirements of 40.7.3 on each pair.
PME23	The test modes described in 40.6.1.1.2 shall be provided for testing of the transmitted waveform, transmitter distortion and transmitted jitter.	40.6.1.1.2	M	Yes [ ]	

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Item	Feature	Subclause	Status	Support	Value/Comment
PME24	For a PHY with a GMII interface the test modes shall be enabled by	40.6.1.1.2	M	Yes [ ]	Setting bits 9:13-15 (1000BASE-T Control Register) of the GMII Management register set as shown in Table 40–7.
PME25	The test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal operation.	40.6.1.1.2	M	Yes [ ]	
PME26	A PHY without a GMII shall provide a means to enable the test modes for conformance testing.	40.6.1.1.2	M	Yes [ ]	
PME27	When transmit test mode 1 is enabled, the PHY shall transmit	40.6.1.1.2	M	Yes [ ]	The sequence of data symbols specified in 40.6.1.1.2 continuously from all four transmitters.
PME28	When in test mode 1, the transmitter shall time the transmitted symbols	40.6.1.1.2	M	Yes [ ]	From a 125.00 MHz ± 0.01% clock in the MASTER timing mode.
PME29	When test mode 2 is enabled, the PHY shall transmit	40.6.1.1.2	M	Yes [ ]	The data symbol sequence {+2,–2} repeatedly on all four channels.
PME30	When in test mode 2, the transmitter shall time the transmitted symbols	40.6.1.1.2	M	Yes [ ]	From a 125.00 MHz ± 0.01% clock in the MASTER timing mode.
PME31	When transmit test mode 3 is enabled, the PHY shall transmit	40.6.1.1.2	M	Yes [ ]	The data symbol sequence {+2,–2} repeatedly on all four channels.
PME32	When in test mode 3, the transmitter shall time the transmitted symbols	40.6.1.1.2	M	Yes [ ]	From a 125 MHz ± 1% clock in the SLAVE timing mode.
PME33	When test mode 4 is enabled, the PHY shall transmit	40.6.1.1.2	M	Yes [ ]	The data symbols generated by the scrambler polynomial specified in 40.6.1.1.2.
PME34	When test mode 4 is enabled, the PHY shall	40.6.1.1.2	M	Yes [ ]	Use the bit sequences generated by the scrambler bits shown in 40.6.1.1.2 to generate the quinary symbols, s_n, as shown in Table 40–8.
PME35	When test mode 4 is enabled, the maximum-length shift register used to generate the sequences defined by this polynomial shall be	40.6.1.1.2	M	Yes [ ]	Updated once per symbol interval (8 ns).

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Item	Feature	Subclause	Status	Support	Value/Comment
PME36	When test mode 4 is enabled, the bit sequences, $x0_n$, $x1_n$, and $x2_n$, generated from combinations of the scrambler bits shown in 40.6.1.1.2 shall be	40.6.1.1.2	M	Yes [ ]	Used to generate the quinary symbols, s_n, as shown in Table 40–8.
PME37	When test mode 4 is enabled, the quinary symbol sequence shall be	40.6.1.1.2	M	Yes [ ]	Presented simultaneously to all transmitters.
PME38	When in test mode 4, the transmitter shall time the transmitted symbols	40.6.1.1.2	M	Yes [ ]	From a 125.00 MHz ± 0.01% clock in the MASTER timing mode.
PME39	The test fixtures defined in Figure 40–22, Figure 40–23, Figure 40–24, and Figure 40–25 or their functional equivalents shall be used for measuring transmitter specifications.	40.6.1.1.3	M	Yes [ ]	
PME40	The test filter used in transmitter test fixtures 1 and 3 shall	40.6.1.1.3	M	Yes [ ]	Have the continuous time transfer function specified in 40.6.1.1.3 or its discrete time equivalent.
PME41	The disturbing signal V_d shall	40.6.1.1.3	M	Yes [ ]	Have the characteristics listed in Table 40–9.
PME42	To allow for measurement of transmitted jitter in MASTER and SLAVE modes the PHY shall provide access to the 125 MHz symbol clock, TX_TCLK that times the transmitted symbols.	40.6.1.1.3	M	Yes [ ]	
PME43	To allow for measurement of transmitted jitter in MASTER and SLAVE modes the PHY shall provide a means to enable the TX_TCLK output if it is not normally enabled.	40.6.1.1.3	M	Yes [ ]	
PME44	The PMA shall	40.6.1.2	M	Yes [ ]	Provide the Transmit function specified in 40.4.2.2 in accordance with the electrical specifications of this clause.
PME45	Where a load is not specified, the transmitter shall	40.6.1.2	M	Yes [ ]	Meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output.
PME46	The tolerance on the poles of the test filters used in 40.6 shall be ± 1%.	40.6.1.2	M	Yes [ ]	

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Item	Feature	Subclause	Status	Support	Value/Comment
PME47	When in transmit test mode 1 and observing the differential signal output at the MDI using test fixture 1, for each pair, with no intervening cable, the absolute value of the peak of the waveform at points A and B as defined in Figure 40–19 shall fall within	40.6.1.2.1	M	Yes [ ]	The range of 0.67 V to 0.82 V (0.75 V ± 0.83 dB).
PME48	The absolute value of the peak of the waveforms at points A and B shall	40.6.1.2.1	M	Yes [ ]	Differ by less than 1%.
PME49	The absolute value of the peak of the waveform at points C and D as defined in Figure 40–19 shall differ	40.6.1.2.1	M	Yes [ ]	From 0.5 times the average of the absolute values of the peaks of the waveform at points A and B by less than 2%.
PME50	When in transmit test mode 1 and observing the differential transmitted output at the MDI, for either pair, with no intervening cabling, the peak value of the waveform at point F as defined in Figure 40–19 shall be	40.6.1.2.2	M	Yes [ ]	Greater than 73.1% of the magnitude of the negative peak value of the waveform at point F. Point G is defined as the point exactly 500 ns after point F. Point F is defined as the point where the waveform reaches it's minimum value at the location indicated in Figure 40–19.
PME51	When in transmit test mode 1 and observing the differential transmitted output at the MDI, for either pair, with no intervening cabling, the peak value of the waveform at point J as defined in Figure 40–19 shall be	40.6.1.2.2	M	Yes [ ]	Greater than 73.1% of the magnitude of the peak value of the waveform at point H. Point J is defined as the point exactly 500 ns after point H. Point H is defined as the point where the waveform reaches it's maximum value at the location indicated in Figure 40–19.
PME52	When in test mode 1 and observing the differential signal output at the MDI using transmitter test fixture 1, for each pair, with no intervening cable, the voltage waveforms at points A, B, C, D defined in Figure 40–19, after the normalization described within the referenced subclause, shall	40.6.1.2.3	M	Yes [ ]	Lie within the time domain template 1 defined in Figure 40–26 and the piecewise linear interpolation between the points in Table 40–10. The waveforms may be shifted in time as appropriate to fit within the template.
PME53	When in test mode 1 and observing the differential signal output at the MDI using transmitter test fixture 1, for each pair, with no intervening cable, the voltage waveforms at points F and H defined in Figure 40–19, after the normalization described within the referenced subclause, shall	40.6.1.2.3	M	Yes [ ]	Lie within the time domain template 2 defined in Figure 40–26 and the piecewise linear interpolation between the points in Table 40–11. The waveforms may be shifted in time as appropriate to fit within the template.

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Item	Feature	Subclause	Status	Support	Value/Comment
PME54	When in test mode 4 and observing the differential signal output at the MDI using transmitter test fixture 3, for each pair, with no intervening cable, the peak distortion as defined below shall be	40.6.1.2.4	M	Yes [ ]	Less than 10 mV.
PME55	When in the normal mode of operation as the MASTER, the peak-to-peak value of the MASTER TX_TCLK jitter relative to an unjittered reference shall be	40.6.1.2.5	M	Yes [ ]	Less than 1.4 ns.
PME56	When the jitter waveform on TX_TCLK is filtered by a high-pass filter, $H_{jf1}(f)$ having the transfer function specified in 40.6.1.2.5, the peak-to-peak value of the resulting filtered timing jitter plus J_{txout}, shall be	40.6.1.2.5	M	Yes [ ]	Less than 0.3 ns.
PME57	When in the normal mode of operation as the SLAVE, receiving valid signals from a compliant PHY operating as the MASTER using the test channel defined in 40.6.1.1.1, with test channel port A connected to the SLAVE, the peak-to-peak value of the SLAVE TX_TCLK jitter relative to the MASTER TX_TCLK shall be	40.6.1.2.5	M	Yes [ ]	Less than 1.4 ns after the receiver is properly receiving the data and has set bit 10.13 of the GMII management register set to 1.
PME58	When the jitter waveform on TX_TCLK is filtered by a high-pass filter, $H_{jf2}(f)$, having the transfer function specified in 40.6.1.2.5, the peak-to-peak value of the resulting filtered timing jitter plus J_{txout} shall be	40.6.1.2.5	M	Yes [ ]	No more than 0.4 ns greater than the simultaneously measured peak-to-peak value of the MASTER jitter filtered by $H_{jf1}(f)$
PME59	For all jitter measurements the peak-to-peak value shall be	40.6.1.2.5	M	Yes [ ]	Measured over an unbiased sample of at least 10^5 clock edges.
PME60	For all unfiltered jitter measurements the peak-to-peak value shall be	40.6.1.2.5	M	Yes [ ]	Measured over an interval of not less than 100 ms and not more than 1 second.
PME61	The quinary symbol transmission rate on each pair of the MASTER PHY shall be	40.6.1.2.6	M	Yes [ ]	125.00 MHz ± 0.01%
PME62	The PMA shall provide the Receive function specified in 40.3.1.4 in accordance with the electrical specifications of this clause.	40.6.1.3	M	Yes [ ]	

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Item	Feature	Subclause	Status	Support	Value/Comment
PME63	The patch cabling and interconnecting hardware used in test configurations shall be	40.6.1.3	M	Yes [ ]	Within the limits specified in 40.7.
PME64	Differential signals received on the receive inputs that were transmitted within the specifications given in 40.6.1.2 and have then passed through a link compatible with 40.7, shall be translated into	40.6.1.3.1	M	Yes [ ]	One of the PMA_UNITDATA.indicate messages with a 4-D symbol rate error less than 10^{-10} and sent to the PCS after link bring-up. Since the 4-D symbols are not accessible, this specification shall be satisfied by a frame error rate less than 10^{-7} for 125 octet frames.
PME65	The receive feature shall	40.6.1.3.2	M	Yes [ ]	Properly receive incoming data with a 5-level symbol rate within the range 125.00 MHz ± 0.01%.
PME66	The signal generator for the common-mode test shall be	40.6.1.3.3	M	Yes [ ]	Capable of providing a sine wave signal of 1 MHz to 250 MHz.
PME67	While sending data from the transmitter the receiver shall	40.6.1.3.3	M	Yes [ ]	Send the proper PMA_UNITDATA.indicate messages to the PCS as the signal generator frequency is varied from 1 MHz to 250 MHz.
PME68	While receiving data from a transmitter specified in 40.6.1.2 through a link segment specified in 40.7 connected to all MDI duplex channels, a receiver shall	40.6.1.3.4	M	Yes [ ]	Send the proper PMA_UNITDATA.indicate message to the PCS when any one of the four pairs is connected to a noise source as described in Figure 40–28.
PME69	The alien crosstalk test specified in 40.6.1.3.4 shall be satisfied by	40.6.1.3.4	M	Yes [ ]	A frame error rate of less than 10^{-7} for 125 octet frames
PME70	The noise source shall be	40.6.1.3.4	M	Yes [ ]	Connected to one of the MDI inputs using Category 5 balanced cable of a maximum length of 0.5 m.

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40.12.8 Characteristics of the link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LKS1	All implementations of the balanced cabling link shall	40.7.1	M	Yes [ ]	Be compatible at the MDI.
LKS2	1000BASE-T links shall	40.7.1	M	Yes [ ]	Consist of Category 5 components as specified in ANSI/TIA/EIA-568-A:1995 and ISO/IEC 11801:1995.
LKS3	Link segment testing shall be conducted using	40.7.2	M	Yes [ ]	Source and load impedances of 100 Ω.
LKS4	The tolerance on the poles of the test filter used in this section shall be	40.7.2		Yes [ ]	± 1%.
LKS5	The insertion loss of each duplex channel shall be	40.7.2.1	M	Yes [ ]	Less than $2.1 f^{0.529} + 0.4/f$ (dB) at all frequencies from 1 MHz to 100 MHz. This includes the attenuation of the balanced cabling pairs, connector losses, and patch cord losses of the duplex channel.
LKS6	The insertion loss specification shall be met when	40.7.2.1	M	Yes [ ]	The duplex channel is terminated in 100 Ω.
LKS7	The return loss of each duplex channel shall be	40.7.2.3	M	Yes [ ]	As specified in 40.7.2.3 at all frequencies from 1 MHz to 100 MHz.
LKS8	The reference impedance for return loss measurement shall be	40.7.2.3	M	Yes [ ]	100 Ω.
LKS9	The NEXT loss between duplex channel pairs of a link segment shall be	40.7.3.1.1	M	Yes [ ]	At least $27.1 - 16.8\log_{10}(f/100)$ (where f is the frequency in MHz over the frequency range 1 MHz to 100 MHz.)
LKS10	The worst case ELFEXT loss between duplex channel pairs of a link segment shall be	40.7.3.2	M	Yes [ ]	Greater than $17 - 20\log_{10}(f/100)$ dB (where f is the frequency in MHz) over the frequency range 1 MHz to 100 MHz.
LKS11	The Power Sum loss between a duplex channel and the three adjacent disturbers shall be	40.7.3.2.2	M	Yes [ ]	Greater than $14.4 - 20\log_{10}(f/100)$ dB where f is the frequency in MHz over the frequency range of 1 MHz to 100 MHz.

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Item	Feature	Subclause	Status	Support	Value/Comment
LKS12	The propagation delay of a link segment shall	40.7.4.1	M	Yes [ ]	Not exceed 570 ns at all frequencies from 2 MHz to 100 MHz.
LKS13	The difference in propagation delay, or skew, between all duplex channel pair combinations of a link segment under all conditions shall not exceed	40.7.4.2	M	Yes [ ]	50 ns at all frequencies between 2 MHz and 100 MHz.
LKS14	Once installed, the skew between pairs due to environmental conditions shall not vary	40.7.4.2	M	Yes [ ]	More than ± 10 ns.

40.12.9 MDI requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MDI1	MDI connector	40.8.1	M	Yes [ ]	8-Way connector as per IEC 60603-7: 1990.
MDI2	Connector used on cabling	40.8.1	M	Yes [ ]	Plug.
MDI3	Connector used on PHY	40.8.1	M	Yes [ ]	Jack (as opposed to plug).
MDI4	MDI connector	40.8.2	M	Yes [ ]	A PHY that implements the crossover function shall be marked with the graphical symbol X.
MDI5	The MDI connector (jack) when mated with a balanced cabling connector (plug) shall	40.8.3	M	Yes [ ]	Meet the electrical requirements for Category 5 connecting hardware for use with 100 Ω Category 5 cable as specified in ANSI/TIA/EIA-568-A:1995 and ISO/IEC 11801:1995.
MDI6	The mated MDI connector and balanced cabling connector shall	40.8.3	M	Yes [ ]	Not have a FEXT loss greater than $40 - 20\log_{10}(f/100)$ over the frequency range 1 MHz to 100 MHz between all contact pair combinations shown in Table 40–12.
MDI7	No spurious signals shall be emitted onto the MDI when the PHY is held in power down mode as defined in 22.2.4.1.5, independent of the value of TX_EN, when released from power down mode, or when external power is first applied to the PHY.	40.8.3	M	Yes [ ]	

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Item	Feature	Subclause	Status	Support	Value/Comment
MDI8	The differential impedance as measured at the MDI for each transmit/receive channel shall be such that	40.8.3.1	M	Yes [ ]	Any reflection due to differential signals incident upon the MDI from a balanced cabling having an impedance of 100 Ω ± 15% is at least 16 dB over the frequency range of 2.0 MHz to 40 MHz and at least $10 - 20\log_{10}(f/80)$ dB over the frequency range 40 MHz to 100 MHz (f in MHz).
MDI9	This return loss shall be maintained	40.8.3.1	M	Yes [ ]	At all times when the PHY is transmitting data or control symbols.
MDI10	The common-mode to differential-mode impedance balance of each transmit output shall exceed	40.8.3.2	M	Yes [ ]	The value specified by the equations specified in 40.8.3.2. Test mode 4 may be used to generate an appropriate transmitter output.
MDI11	The magnitude of the total common-mode output voltage, E_{cm_out}, on any transmit circuit, when measured as shown in Figure 40–32, shall be	40.8.3.3	M	Yes [ ]	Less than 50 mv peak-to-peak when transmitting data.
MDI12	Each wire pair of the MDI shall	40.8.3.4	M	Yes [ ]	Withstand without damage the application of short circuits across the MDI port for an indefinite period of time without damage.
MDI13	Each wire pair of the MDI shall resume	40.8.3.4	M	Yes [ ]	Normal operation after such faults are removed.
MDI14	The magnitude of the current through the short circuit specified in PME64 shall not exceed	40.8.3.4	M	Yes [ ]	300 mA.
MDI15	Each wire pair shall withstand without damage	40.8.3.4	M	Yes [ ]	A 1000 V common-mode impulse of either polarity (E_{cm} as indicated in Figure 40–33).
MDI16	The shape of the impulse shall be	40.8.3.4	M	Yes [ ]	0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

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40.12.10 General safety and environmental requirements

Item	Feature	Subclause	Status	Support	Value/Comment
ENV1	Conformance to safety specifications	40.9.1	M	Yes [ ]	IEC 60950.
ENV2	Installation practice	40.9.2.1	INS:M	N/A [ ] Yes [ ]	Sound practice, as defined by applicable local codes.
ENV3	Care taken during installation to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.	40.9.2.2	INS:M	N/A [ ] Yes [ ]	
ENV4	1000BASE-T equipment shall be capable of withstanding a telephone battery supply from the outlet as described in 40.9.2.3.	40.9.2.3	M	Yes [ ]	
ENV5	A system integrating the 1000BASE-T PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.	40.9.3.1	INS:M	N/A [ ] Yes [ ]	

40.12.11 Timing requirements

Item	Feature	Subclause	Status	Support	Value/Comment
TR1	Every 1000BASE-T PHY associated with a GMII shall	40.11.1	M	Yes [ ]	Comply with the bit delay constraints specified in Table 40–13 for half duplex operation and Table 40–14 for full duplex operation. These constraints apply for all 1000BASE-T PHYs.
TR2	For any given implementation, the assertion delays on CRS shall	40.11.1	M	Yes [ ]	Be equal.
TR3	Every DTE with a 1000BASE-T PHY shall	40.11.2	M	Yes [ ]	Comply with the bit delay constraints specified in Table 40–15.
TR4	To ensure fair access to the network, each DTE operating in half duplex mode shall, additionally, satisfy the following:	40.11.3	M	Yes [ ]	(MAX MDI to MAC Carrier De-assert Detect) – (MIN MDI to MAC Carrier Assert Detect) < 16 Bit Times.

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41. Repeater for 1000 Mb/s baseband networks

41.1 Overview

41.1.1 Scope

Clause 41 defines the functional and electrical characteristics of a repeater for use with ISO/IEC 8802-3 1000 Mb/s baseband networks. A repeater for any other ISO/IEC 8802-3 network type is beyond the scope of this clause. The relationship of this standard to the entire ISO/IEC 8802-3 CSMA/CD LAN standard is shown in Figure 41–1. The purpose of the repeater is to provide a simple, inexpensive, and flexible means of coupling two or more segments.

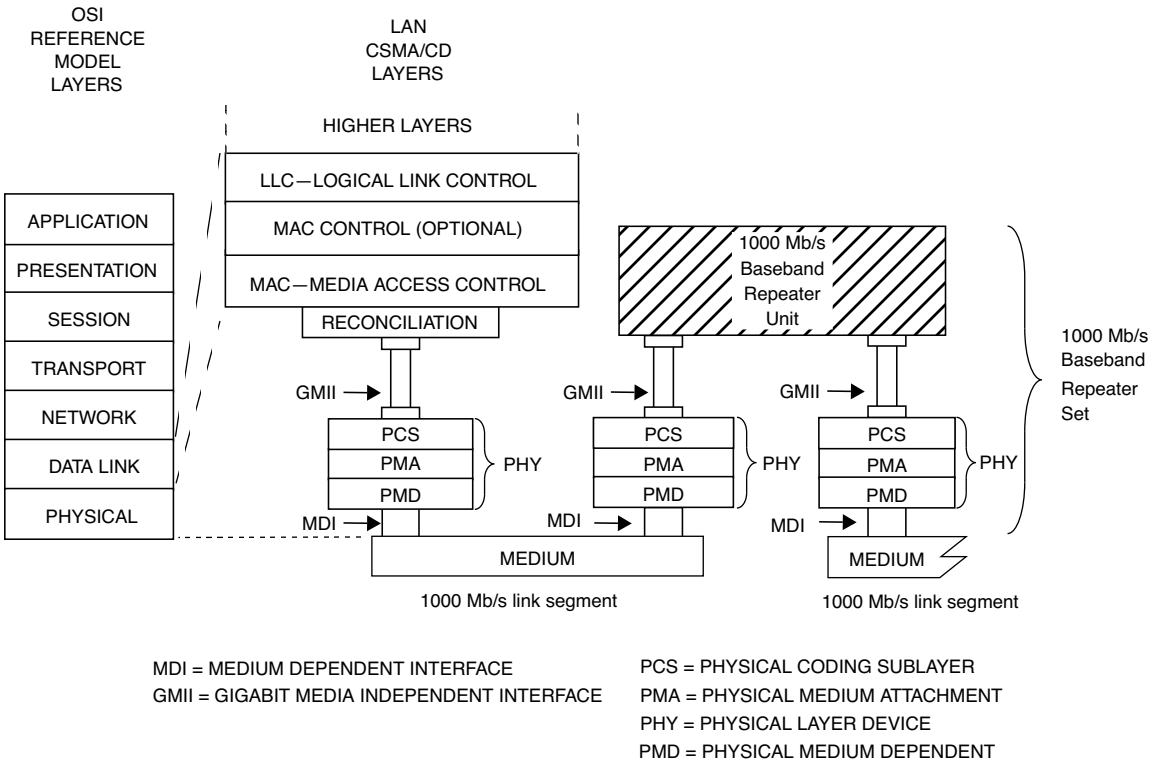


Figure 41–1—1000 Mb/s repeater set relationship to the ISO/IEC OSI reference model

41.1.1.1 Repeater set

Repeater sets are an integral part of all 1000 Mb/s baseband networks with more than two DTEs and are used to extend the physical system topology by providing a means of coupling two or more segments. A single repeater set is permitted within a single collision domain to provide the maximum connection path length. Allowable topologies contain only one operative signal path between any two points on the network. A repeater set is not a station and does not count toward the overall limit of 1024 stations on a network.

A repeater set can receive and decode data from any segment under worst-case noise, timing, and signal amplitude conditions. It retransmits the data to all other segments attached to it with timing, amplitude, and coding restored. The retransmission of data occurs simultaneously with reception. If a collision occurs, the repeater set propagates the collision event throughout the network by transmitting a Jam signal. A repeater set also provides a degree of protection to a network by isolating a faulty segment's carrier activity from propagating through the network.

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41.1.1.2 Repeater unit

A repeater unit is a subset of a repeater set containing all the repeater-specific components and functions, exclusive of PHY components and functions. A repeater unit connects to the PHYs using the Gigabit Media Independent Interface (GMII) defined in Clause 35.

41.1.2 Application perspective

This subclause states the broad objectives and assumptions underlying the specification defined through Clause 41.

41.1.2.1 Objectives

a) Provide physical means for coupling two or more LAN segments at the Physical Layer.
b) Support interoperability of independently developed physical, electrical, and optical interfaces.
c) Provide a communication channel with a mean bit error rate, at the physical service interface equivalent to that for the attached PHY.
d) Provide for ease of installation and service.
e) Ensure that fairness of DTE access is not compromised.
f) Provide for low-cost networks, as related to both equipment and cabling.

41.1.2.2 Compatibility considerations

All implementations of the repeater set shall be compatible at the MDI. The repeater set is defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the repeater set in an application-dependent manner provided the appropriate PHY specifications are met.

41.1.2.2.1 Internal segment compatibility

Implementations of the repeater set that contain a MAC layer for network management or other purposes, irrespective of whether they are connected through an exposed repeater port or are internally ported, shall conform to the requirements of Clause 30 on that port if repeater management is implemented.

41.1.3 Relationship to PHY

A close relationship exists between Clause 41 and the GMII clause (Clause 35) and the PHY clauses (Clauses 36–39 for 1000BASE-X PHYs and Clause 40 for 1000BASE-T PHYs). The PHY's PMA, PCS, and MDI specification provide the actual medium attachment, including drivers, receivers, and Medium Interface Connectors for the various supported media. The repeater clause does not define a new PHY; it utilizes the existing PHYs complete and without modification. The repeater_mode variable in each PHY is set, so that the CRS signal of the GMII is asserted only in response to receive activity (see 36.2.5.1.3).

41.2 Repeater functional specifications

A repeater set provides the means whereby data from any segment can be received under worst-case noise, timing, and amplitude conditions and then retransmitted with timing and amplitude restored to all other attached segments. Retransmission of data occurs simultaneously with reception. If a collision occurs, the repeater set propagates the collision event throughout the network by transmitting a Jam signal. If an error is received by the repeater set, no attempt is made to correct it and it is propagated throughout the network by transmitting an explicit error code.

The repeater set provides the following functional capability to handle data flow between ports:

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a) *Signal restoration*. Provides the ability to restore the timing and amplitude of the received signal prior to retransmission.
b) *Transmit function*. Provides the ability to output signals on the appropriate port and encoded appropriately for that port. Details of signal processing are described in the specifications for the PHYs.
c) *Receive function*. Provides the ability to receive input signals presented to the ports. Details of signal processing are described in the specifications for the PHYs.
d) *Data-Handling function*. Provides the ability to transfer code-elements between ports in the absence of a collision.
e) *Received Event-Handling requirement*. Provides the ability to derive a carrier signal from the input signals presented to the ports.
f) *Collision-Handling function*. Provides the ability to detect the simultaneous reception of frames at two or more ports and then to propagate a Jam message to all connected ports.
g) *Error-Handling function*. Provides the ability to prevent substandard links from generating streams of false carrier and interfering with other links.
h) *Partition function*. Provides the ability to prevent a malfunctioning port from generating an excessive number of consecutive collisions and indefinitely disrupting data transmission on the network.
i) *Receive Jabber function*. Provides the ability to interrupt the reception of abnormally long streams of input data.

41.2.1 Repeater functions

The repeater set shall provide the Signal Restoration, Transmit, Receive, Data Handling, Received Event Handling, Collision Handling, Error Handling, Partition, and Receive Jabber functions. The repeater is transparent to all network acquisition activity and to all DTEs. The repeater will not alter the basic fairness criterion for all DTEs to access the network or weigh it toward any DTE or group of DTEs regardless of network location.

The Transmit and Receive functional requirements are specified by the PHY clauses, Clause 40 for 1000BASE-T and Clauses 36 to 39 for 1000BASE-X.

41.2.1.1 Signal restoration functional requirements

41.2.1.1.1 Signal amplification

The repeater set (including its integral PHYs) shall ensure that the amplitude characteristics of the signals at the MDI outputs of the repeater set are within the tolerances of the specification for the appropriate PHY type. Therefore, any loss of signal-to-noise ratio due to cable loss and noise pickup is regained at the output of the repeater set as long as the incoming data is within system specification.

41.2.1.1.2 Signal wave-shape restoration

The repeater set (including its integral PHYs) shall ensure that the wave-shape characteristics of the signals at the MDI outputs of a repeater set are within the specified tolerance for the appropriate PHY type. Therefore, any loss of wave-shape due to PHYs and media distortion is restored at the output of the repeater set.

41.2.1.1.3 Signal retiming

The repeater set (including its integral PHYs) shall ensure that the timing of the encoded data output at the MDI outputs of a repeater set are within the specified tolerance for the appropriate PHY type. Therefore, any receive jitter from the media is removed at the output of the repeater set.

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41.2.1.2 Data-handling functional requirements

41.2.1.2.1 Data frame forwarding

The repeater set shall ensure that the data frame received on a single input port is distributed to all other output ports in a manner appropriate for the PHY type of that port. The data frame is that portion of the packet after the SFD and before the end-of-frame delimiter. The only exceptions to this rule are when contention exists among any of the ports, when the receive port is partitioned as defined in 41.2.1.6, when the receive port is in the Jabber state as defined in 41.2.1.7, or when the receive port is in the Link Unstable state as defined in 41.2.1.5.1. Between unpartitioned ports, the rules for collision handling (see 41.2.1.4) take precedence.

41.2.1.2.2 Received code violations

The repeater set shall ensure that any code violations received while forwarding a packet are propagated to all outgoing segments. These code violations shall be replaced by a code-group that provide an explicit indication that an error was received, as appropriate for the outgoing PHY type. Once a received code violation has been replaced by a code-group indicating a receive error, this substitution shall continue for the remainder of the received event regardless of its content. The only exception to this rule is when contention exists among any of the ports, where the rules for collision handling (see 41.2.1.4) then take precedence.

41.2.1.3 Received event-handling functional requirements

41.2.1.3.1 Received event handling

For all its ports, the repeater set shall detect received events by monitoring the port for any assertion of the GMII CRS signal that is the result of receive activity. The repeater_mode variable in the PHY shall be set to ensure that the CRS signal is not asserted in response to transmit activity. Received events include both the data frame and any encapsulation of the data frame such as Preamble, SFD, start and end of packet delimiters, carrier extension symbols, and error propagation symbols. A received event is exclusive of the IDLE pattern. Upon detection of a received event from one port, the repeater set shall repeat all received signals in the data frame from that port to the other ports as described in Figure 41–2.

41.2.1.3.2 Preamble regeneration

The repeater set shall output preamble as appropriate for the outgoing PHY type followed by the SFD. The duration of the output preamble shall not vary more than 8 bit times from the duration of the received preamble.

41.2.1.3.3 Start-of-packet propagation delay

The start-of-packet propagation delay for a repeater set is the time delay between the start of a received event on a repeated-from (input) port to the start of transmit on the repeated-to (output) port (or ports). This parameter is referred to as the SOP delay, and is measured at the MDI of the repeater ports. The maximum value of this delay is constrained such that the sum of the SOP delay and SOJ delay shall not exceed the value specified in 41.2.1.4.3.

41.2.1.3.4 Start-of-packet variability

The start-of-packet variability for a repeater set is defined as the total worst-case difference between start-of-packet propagation delays for successive received events separated by 112 bit times or less at the same input port. The variability shall be less than or equal to 16 bit times.

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41.2.1.4 Collision-handling functional requirements

41.2.1.4.1 Collision detection

The repeater performs collision detection by monitoring all its enabled input ports for received events. When the repeater detects received events on more than one input port, it shall enter a collision state and transmit the Jam message to all of its output ports.

41.2.1.4.2 Jam generation

While a collision is occurring between any of its ports, the repeater unit shall transmit the Jam message to all of the ports. The Jam message shall be transmitted in accordance with the repeater state diagram in Figure 41–2. The Jam message is signalled across the GMII using the Transmit Error Propagation encoding if the collision is detected during Normal Data Transmission, or using the Carrier Extend Error encoding if the collision is detected during Carrier Extension.

41.2.1.4.3 Start-of-collision-jam propagation delay

The start-of-collision Jam propagation delay for a repeater set is the time delay between the start of the second received event (that results in a collision) to arrive at its port and the start of Jam out on all ports. This parameter is referred to as the SOJ delay, and is measured at the MDI of the repeater ports. The sum of the SOP delay and SOJ delay shall not exceed 976 bit times (BT).

41.2.1.4.4 Cessation-of-collision Jam propagation delay

The cessation-of-collision Jam propagation delay for a repeater set is the time delay between the end of the received event that creates a state such that Jam should end at a port and the end of Jam at that port. The states of the input signals that should cause Jam to end are covered in detail in the repeater state diagram in Figure 41–2. This parameter is referred to as the EOJ delay. This delay shall not exceed the SOP delay.

41.2.1.5 Error-handling functional requirements

41.2.1.5.1 Carrier integrity functional requirements

It is desirable that the repeater set protect the network from some transient fault conditions that would disrupt network communications. Potential likely causes of such conditions are DTE and repeater power-up and power-down transients, cable disconnects, and faulty wiring.

The repeater unit shall provide a self-interrupt capability at each port, as described in Figure 41–5, to prevent a segment's spurious carrier activity from propagating through the network.

At each port the repeater shall count consecutive false carrier events signalled across the GMII. The count shall be incremented on each false carrier event and shall be reset on reception of a valid carrier event. In addition, each port shall have a false carrier timer, which is enabled at the beginning of a false carrier event and reset at the conclusion of such an event. A repeater unit shall transmit the Jam signals to all ports for the duration of the false carrier event or until the duration of the event exceeds the time specified by the false_carrier_timer (see 41.2.2.1.4), whichever is shorter. The Jam message shall be transmitted in accordance with the repeater state diagram in Figure 41–2. The LINK UNSTABLE condition shall be detected when the False Carrier Event Count equals the value FCELimit (see 41.2.2.1.1) or the duration of a false carrier event exceeds the time specified by the false_carrier_timer. In addition, the LINK UNSTABLE condition shall be detected upon power-up reset.

Upon detection of LINK UNSTABLE at a port, the repeater unit shall perform the following:

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a) Inhibit sending further messages from that port to the repeater unit.
b) Inhibit sending further output messages to that port from the repeater unit.
c) Continue to monitor activity on that port.

The repeater unit shall exit the LINK UNSTABLE condition at the port when one of the following is met:

a) The repeater has detected no activity (Idle) for more than the time specified by ipg_timer plus idle_timer (see 41.2.2.1.4) on port X.
b) A valid carrier event with a duration greater than the time specified by valid_carrier_timer (see 41.2.2.1.4) has been received, preceded by no activity (Idle) for more than the time specified by ipg_timer (see 41.2.2.1.4) on port X.

The false_carrier_timer duration is longer than the maximum round-trip latency from a repeater to a DTE, but less than a slot time. This allows a properly functioning DTE to respond to the Jam message by detecting collision and terminating the transmission prior to the expiration of the timer. The upper limit on the false_carrier_timer prevents the Jam message from exceeding the maximum fragment size.

The combination of the ipg_timer, idle_timer, and valid_carrier_timer filter transient activity that can occur on a link during power cycles or mechanical connection. The duration of the ipg_timer is greater than two-thirds of the minimum IPG, and less than the minimum IPG less some shrinkage. The idle_timer is specified as approximately 320 μs based upon empirical data on such transients. The valid_carrier_timer duration is less than the duration of a minimum valid carrier event, but long enough to filter most spurious carrier events (note that there can be no valid collision fragments on an isolated link in a single repeater topology). The range of the valid_carrier_timer is specified to be the same as the false_carrier_timer range for the convenience of implementations.

41.2.1.5.2 Speed handling

If the PHY has the capability of detecting speeds other than 1000 Mb/s, then the repeater set shall have the capability of blocking the flow of non-1000 Mb/s signals. The incorporation of 1000 Mb/s and 100 Mb/s or 10 Mb/s repeater functionality within a single repeater set is beyond the scope of this standard.

41.2.1.6 Partition functional requirements

It is desirable that the repeater set protect the network from some fault conditions that would disrupt network communications. A potentially likely cause of this condition could be due to a cable fault.

The repeater unit shall provide a self-interrupt capability at each port, as described in Figure 41–4, to prevent a faulty segment's carrier activity from propagating through the network. The repeater unit shall count consecutive collision events at each port. The count shall be incremented on each transmission that suffers a collision and shall be reset on a successful transmission or reception. If this count equals or exceeds the value CELimit (see 41.2.2.1.1), the Partition condition shall be detected. In addition, the partition condition shall be detected due to a carrier event of duration in excess of jabber_timer in which a collision has occurred.

Upon detection of Partition at a port, the repeater unit shall perform the following:

a) Inhibit sending further input messages from that port to the repeater unit.
b) Continue to output messages to that port from the repeater unit.
c) Continue to monitor activity on that port.

The repeater unit shall reset the Partition function at the port when one of the following conditions is met:

— On power-up reset.

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— The repeater has detected activity on the port for more than the number of bits specified for no_collision_timer (see 41.2.2.1.4) without incurring a collision.
— The repeater has transmitted on the port for more than the number of bits specified for no_collision_timer (see 41.2.2.1.4) without incurring a collision.

The no_collision_timer duration is longer than the maximum round-trip latency from a repeater to a DTE (maximum time required for a repeater to detect a collision), and less than the minimum valid carrier event duration (slot time plus header_size minus preamble shrinkage).

41.2.1.7 Receive jabber functional requirements

The repeater unit shall provide a self-interrupt capability at each port, as described in Figure 41–3, to prevent an illegally long reception of data from propagating through the network. The repeater unit shall provide a window of duration jabber_timer bit times (see 41.2.2.1.4) during which the input messages from a port may be passed on to other repeater unit functions. If a reception exceeds this duration, the jabber condition shall be detected.

Upon detection of the jabber condition at a port, the repeater unit shall perform the following:

a) Inhibit sending further input messages from that port to the repeater unit.
b) Inhibit sending further output messages to that port from the repeater unit.

The repeater shall reset the Jabber function at the port, and re-enable data transmission and reception, when either one of the following conditions is met:

— On power-up reset.
— When carrier is no longer detected at that port.

The lower bound of the jabber_timer is longer than the carrier event of a maximum length burst. The upper bound is large enough to permit a wide variety of implementations.

41.2.2 Detailed repeater functions and state diagrams

A precise algorithmic definition is given in this subclause, providing a complete procedural model for the operation of a repeater, in the form of state diagrams. Note that whenever there is any apparent ambiguity concerning the definition of repeater operation, the state diagrams should be consulted for the definitive statement.

The model presented in this subclause is intended as a primary specification of the functions to be provided by any repeater unit. It is important to distinguish, however, between the model and a real implementation. The model is optimized for simplicity and clarity of presentation, while any realistic implementation should place heavier emphasis on such constraints as efficiency and suitability to a particular implementation technology.

It is the functional behavior of any repeater set implementation that is expected to match the standard, not the internal structure. The internal details of the procedural model are useful only to the extent that they help specify the external behavior clearly and precisely. For example, the model uses a separate Receive Port Jabber state diagram for each port. However, in actual implementation, the hardware may be shared.

The notation used in the state diagram follows the conventions of 1.2.1. Note that transitions shown without source states are evaluated at the completion of every state and take precedence over other transition conditions.

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41.2.2.1 State diagram variables

41.2.2.1.1 Constants

CELimit

The number of consecutive Collision Events that must occur before a segment is partitioned.

Values: Positive integer greater than 60.

FCELimit

The number of consecutive False Carrier Events that must occur before a segment is isolated.

Value: 2.

41.2.2.1.2 Variables

begin

The Interprocess flag controlling state diagram initialization values.

Values: true
false

CRS(X), RXD(X), RX_DV(X), RX_ER(X), TXD(X), TX_EN(X), TX_ER(X)

GMII signals received from or sent to the PHY at port X (see Clause 35). The repeater_mode variable in the PHY is set to ensure that the CRS(X) signal is asserted in response to receive activity only.

RXERROR(X)

A combination of the GMII signal encodings indicating that the PHY has detected a Data Error, Carrier Extend Error, or False Carrier Error.

Value: RXERROR(X) ⇐ ((RX_ER(X) = true) *
((RX_DV(X) = true) + (RXD(X) = FalseCarrier) + (RXD(X) = CarrierExtendError)))

TX(X)

A combination of the GMII signal encodings indicating that port X is transmitting a frame.

Value: TX(X) ⇐ ((TX_EN(X) = true) + (TX_ER(X) = true))

isolate(X)

Flag from Carrier Integrity state diagram for port X, which determines whether a port should be enabled or disabled.

Values: true; the Carrier Integrity Monitor has determined the port should be disabled.
false; the Carrier Integrity Monitor has determined the port should be enabled.

force_jam(X)

Flag from Carrier Integrity state diagram for port X, which causes the Repeater Unit to enter the Jam state.

Values: true; the port is in the False Carrier state.
false; the port is not in the False Carrier state.

jabber(X)

Flag from Receive Timer state diagram for port X which indicates that the port has received excessive length activity.

Values: true; port has exceeded the continuous activity limit.
false; port has not exceeded the continuous activity limit.

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link_status(X)

Indication from the Auto-Negotiation process (Clauses 28 and 37) that Auto-Negotiation has completed and the priority resolution function has determined that the link will be operated in half duplex mode.

Values: OK; the link is operational in half duplex mode.
FAIL; the link is not operational in half duplex mode.

partition(X)

Flag from Partition state diagram for port X, which determines whether a port receive path should be enabled or disabled.

Values: true; port has exceeded the consecutive collision limit.
false; port has not exceeded the consecutive collision limit.

41.2.2.1.3 Functions

port(Test)

A function that returns the designation of a port passing the test condition. For example, port(CRS = true) returns the designation: X for a port for which CRS is asserted. If multiple ports meet the test condition, the Port function will be assigned one and only one of the acceptable values.

41.2.2.1.4 Timers

All timers operate in the same fashion. A timer is reset and starts timing upon entering a state where "start x_timer" is asserted. At time "x" after the timer has been started, "x_timer_done" is asserted and remains asserted until the timer is reset. At all other times, "x_timer_not_done" is asserted.

When entering a state where "start x_timer" is asserted, the timer is reset and restarted even if the entered state is the same as the exited state.

The timers used in the repeater state diagrams are defined as follows:

false_carrier_timer

Timer for length of false carrier (41.2.1.5.1) that must be present to set isolate(X) to true. The timer is done when it reaches 3600–4000 BT.

idle_timer

Timer for length of time without carrier activity that must be present to set isolate(X) to false. The timer is done when it reaches 240 000–400 000 BT.

ipg_timer

Timer for length of time without carrier activity that must be present before carrier integrity tests (41.2.1.5.1) are re-enabled. The timer is done when it reaches 64–86 BT.

jabber_timer

Timer for length of carrier which must be present before the Jabber state is entered (41.2.1.7). The timer is done when it reaches 80 000–150 000 BT.

no_collision_timer

Timer for length of packet without collision before partition(X) is set to false (41.2.1.6). The timer is done when it reaches 3600–4144 BT.

valid_carrier_timer

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Timer for length of valid carrier that must be present to cause isolate(X) to be set to false at the end of the carrier event. The timer is done when it reaches 3600–4000 BT.

41.2.2.1.5 Counters

CE(X)

Consecutive port Collision Event count for port X. Partitioning occurs on a terminal count of CELimit being reached.

Values: Non-negative integers up to a terminal count of CELimit.

FCE(X)

False Carrier Event count for port X. Isolation occurs on a terminal count of FCELimit being reached.

Values: Non-negative integers up to a terminal count of FCELimit.

41.2.2.1.6 Port designation

Ports are referred to by number. Port information is obtained by replacing the X in the desired function with the number of the port of interest. Ports are referred to in general as follows:

X

Generic port designator. When X is used in a state diagram, its value is local to that diagram and not global to the set of state diagrams.

N

Identifies the port that caused the exit from the IDLE or JAM states of Figure 41–2. The value is assigned in the term assignment statement on the transition out of these states (see 1.2.1 for State Diagram Conventions).

ALL

Indicates all repeater ports are to be considered. The test passes when all ports meet the test conditions.

ALLXJIPN

The test passes when all ports, excluding those indicated by J, I, P, or N, meet the test conditions. One or more of the J, I, P, or N indications are used to exclude from the test ports with Jabber = true, Isolate = true, Partition = true, or port N, respectively.

ANY

Indicates all ports are to be considered. The test passes when one or more ports meet the test conditions.

ANYXJIPN

The test passes when one or more ports, excluding those indicated by J, I, P, or N, meet the test conditions. One or more of the J, I, P, or N indications are used to exclude from the test ports with Jabber = true, Isolate = true, Partition = true, or port N, respectively.

ONLY1

Indicates all ports except those with Jabber = true, Isolate = true, or Partition = true are to be considered. The test passes when one and only one port meet the test conditions.

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41.2.2.2 State diagrams

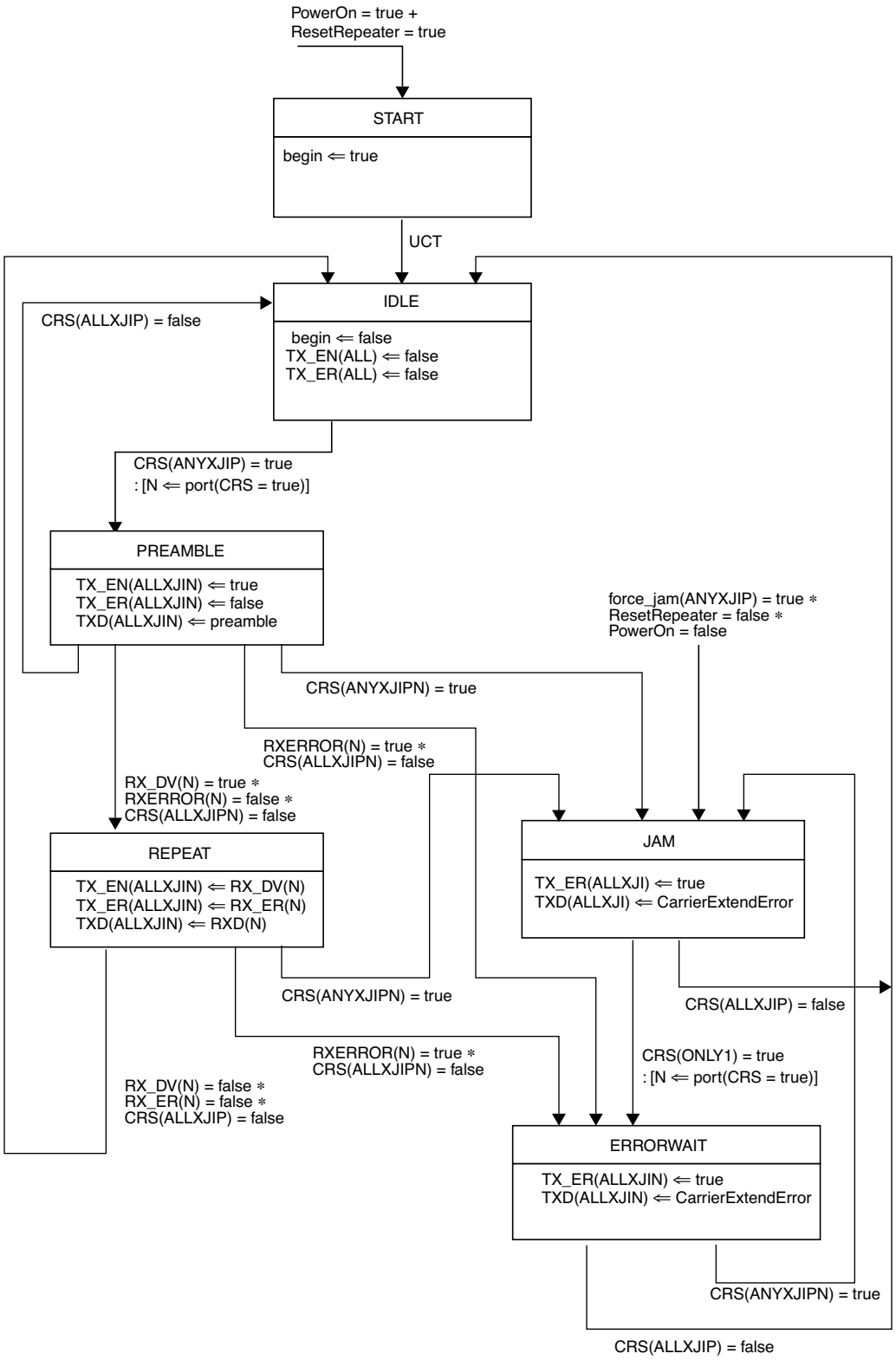


Figure 41–2—Repeater unit state diagram

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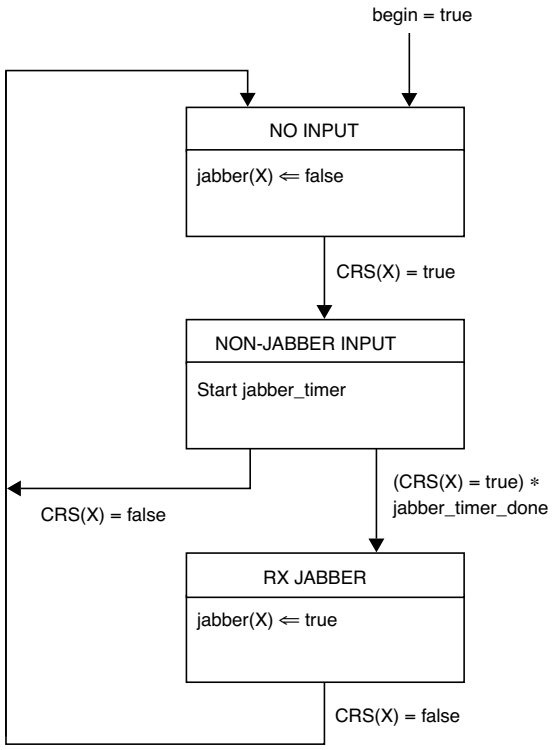


Figure 41–3—Receive timer state diagram for port X

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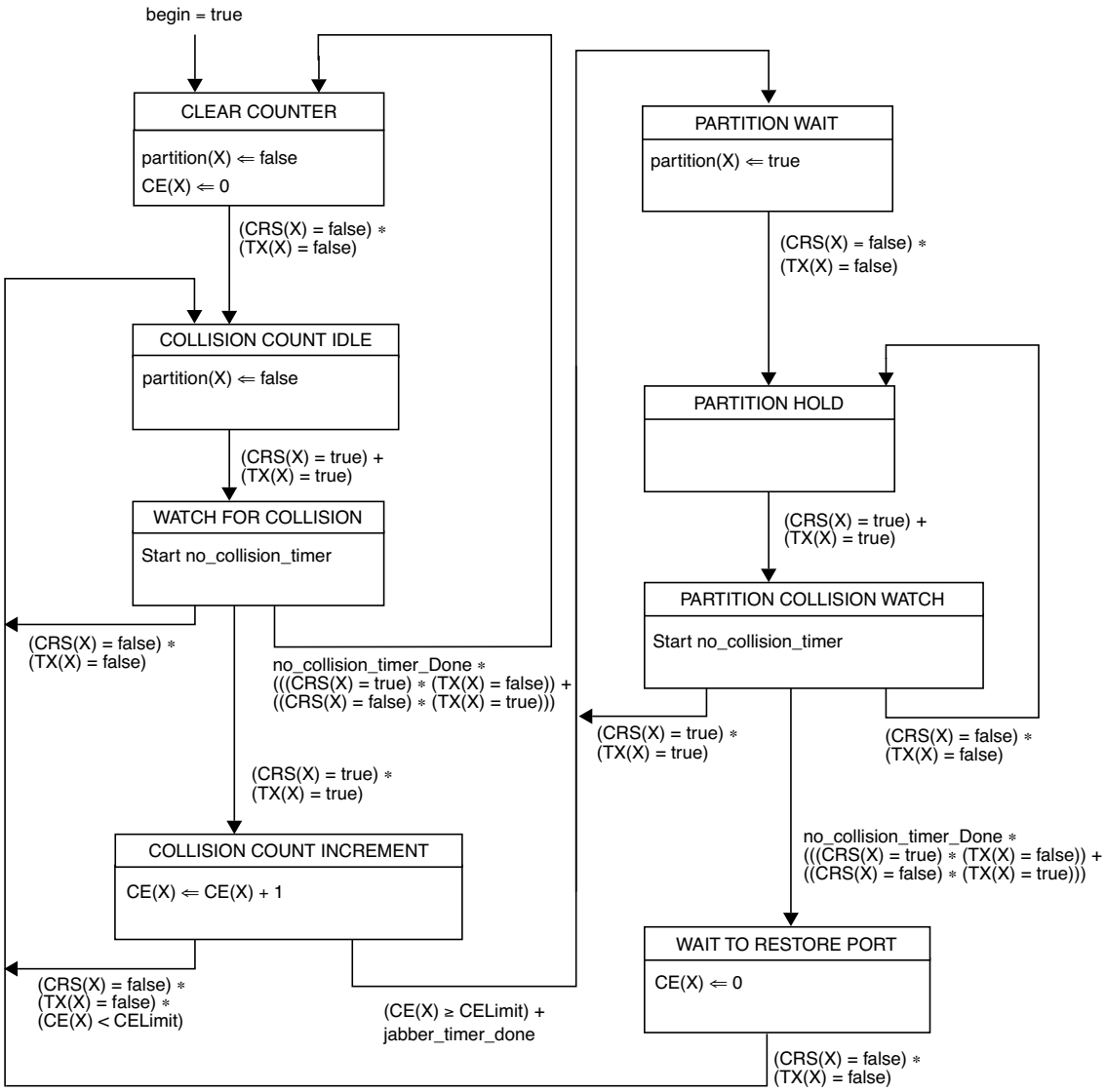


Figure 41–4—Partition state diagram for port X

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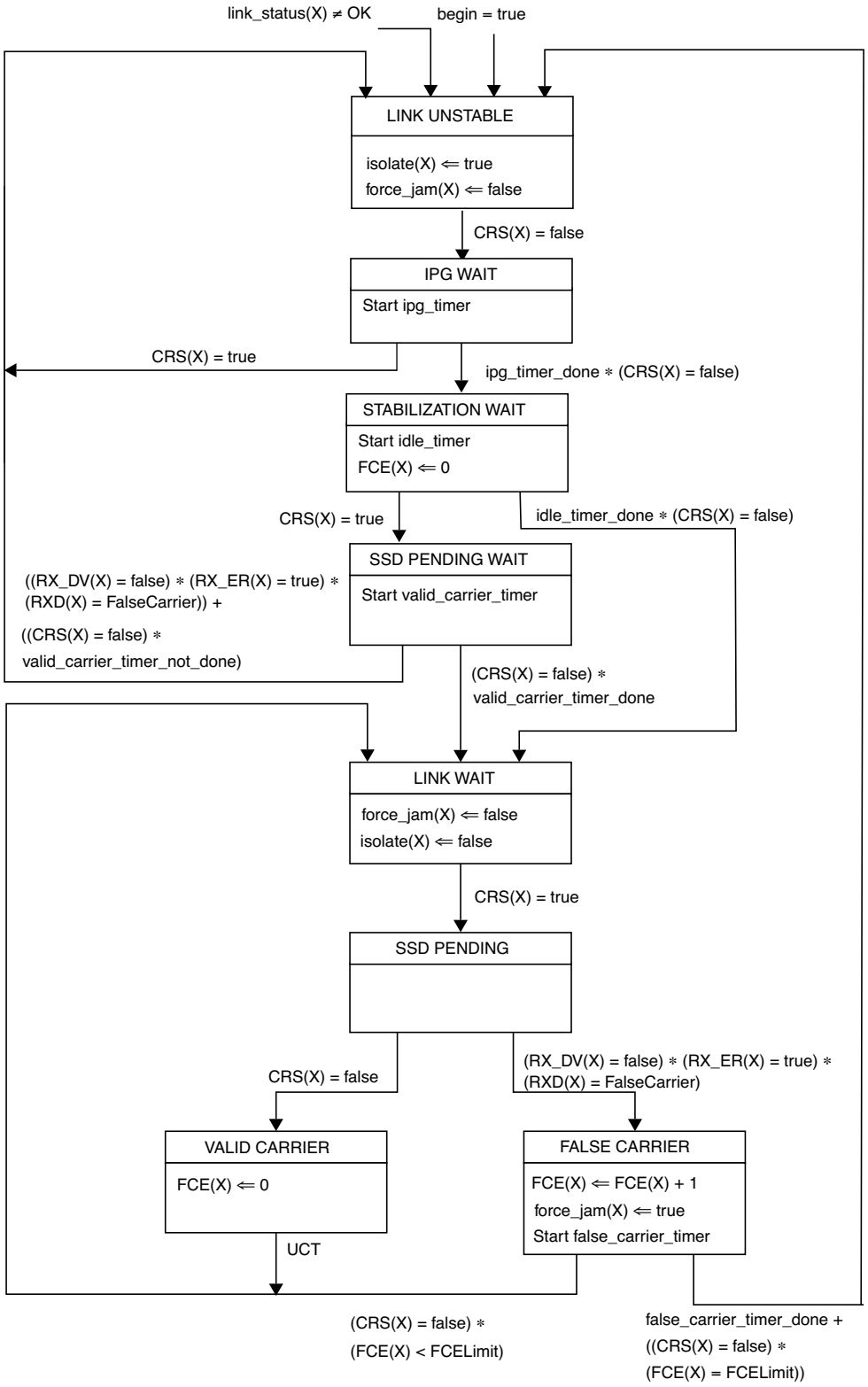


Figure 41–5—Carrier integrity monitor state diagram for port X

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41.3 Repeater electrical specifications

41.3.1 Electrical isolation

Network segments that have different isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of the repeater set.

41.4 Environmental specifications

41.4.1 General safety

All equipment meeting this standard shall conform to IEC 60950: 1991.

41.4.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cable systems described in this subclause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cables and components.
c) High-energy transients coupled onto the LAN cable system.
d) Voltage potential differences between safety grounds to which the various LAN components are connected.

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network. Isolation requirements are defined in 41.4.3.

41.4.2.1 Installation

Sound installation practice, as defined by applicable local codes and regulations, shall be followed in every instance in which such practice is applicable.

41.4.2.2 Grounding

The safety ground, or chassis ground for the repeater set, shall be provided through the main ac power cord via the third wire ground as defined by applicable local codes and regulations.

If the MDI connector should provide a shield connection, the shield may be connected to the repeater safety ground. A network segment connected to the repeater set through the MDI may use a shield. If both ends of the network segment have a shielded MDI connector available, then the shield may be grounded at both ends according to local regulations and ISO/IEC 11801: 1995, and as long as the ground potential difference between both ends of the network segment is less than 1 V rms.

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WARNING

It is assumed that the equipment to which the repeater is attached is properly grounded and not left floating nor serviced by a "doubly insulated ac power distribution system." The use of floating or insulated equipment, and the consequent implications for safety, are beyond the scope of this standard.

41.4.2.3 Installation and maintenance guidelines

During installation and maintenance of the cable plant, care should be taken to ensure that uninsulated network cable connectors do not make electrical contact with unintended conductors or ground.

41.4.3 Electrical isolation

There are two electrical power distribution environments to be considered that require different electrical isolation properties:

a) *Environment A*. When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.
b) *Environment B*. When a LAN crosses the boundary between separate power distribution systems or the boundary of a single building.

41.4.3.1 Environment A requirements

Attachment of network segments via repeater sets requires electrical isolation of 500 V rms, one-minute withstand, between the segment and the protective ground of the repeater unit.

41.4.3.2 Environment B requirements

The attachment of network segments that cross environment B boundaries requires electrical isolation of 1500 Vrms, one-minute withstand, between each segment and all other attached segments and also the protective ground of the repeater unit.

The requirements for interconnected electrically conducting LAN segments that are partially or fully external to a single building environment may require additional protection against lightning strike hazards. Such requirements are beyond the scope of this standard. It is recommended that the above situation be handled by the use of nonelectrically conducting segments (e.g., fiber optic).

It is assumed that any nonelectrically conducting segments will provide sufficient isolation within that media to satisfy the isolation requirements of environment B.

41.4.4 Reliability

A two-port repeater set shall be designed to provide a mean time between failure (MTBF) of at least 50 000 hours of continuous operation without causing a communications failure among stations attached to the network medium. Repeater sets with more than two ports shall add no more than 3.46×10^{-6} failures per hour for each additional port.

The repeater set electronics should be designed to minimize the probability of component failures within the repeater electronics that prevent communications among other PHYs on the individual segments. Connectors and other passive components comprising the means of connecting the repeater to the cable should be designed to minimize the probability of total network failure.

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41.4.5 Environment

41.4.5.1 Electromagnetic emission

The repeater shall comply with applicable local and national codes for the limitation of electromagnetic interference.

41.4.5.2 Temperature and humidity

The repeater is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the repeater the operating environmental conditions to facilitate selection, installation, and maintenance.

41.5 Repeater labeling

It is required that each repeater (and supporting documentation) shall be labeled in a manner visible to the user with these parameters:

a) Crossover ports appropriate to the respective PHY shall be marked with an X.

Additionally it is recommended that each repeater (and supporting documentation) also be labeled in a manner visible to the user with at least these parameters:

b) Data rate capability in Mb/s
c) Any applicable safety warnings
d) Port type, i.e., 1000BASE-CX, 1000BASE-SX, 1000BASE-LX, and 1000BASE-T
e) Worst-case bit time delays between any two ports appropriate for
    1) Start-of-packet propagation delay
    2) Start-of-collision Jam propagation delay
    3) Cessation-of-collision Jam propagation delay

41.6 Protocol Implementation Conformance Statement (PICS) proforma for Clause 41, Repeater for 1000 Mb/s baseband networks[12]

41.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 41, Repeater for 1000 Mb/s baseband networks, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

[12]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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41.6.2 Identification

41.6.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

41.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2002, Clause 41, Repeater for 1000 Mb/s baseband networks
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002.)	

Date of Statement	

41.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*SXP	Repeater supports 1000BASE-SX connections	41.1.2.2		O	Yes [ ] No [ ]
*LXP	Repeater supports 1000BASE-LX connections	41.1.2.2		O	Yes [ ] No [ ]
*CXP	Repeater supports 1000BASE-CX connections	41.1.2.2		O	Yes [ ] No [ ]
*TP	Repeater supports 1000BASE-T connections	41.1.2.2		O	Yes [ ] No [ ]
*PHYS	PHYs capable of detecting non 1000 Mb/s signals	41.2.1.5.2		O	Yes [ ] No [ ]

In addition, the following predicate name is defined for use when different implementations from the set above have common parameters:

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*XP:SXP or LXP or CXP

41.6.4 PICS proforma tables for the Repeater for 1000 Mb/s baseband networks

41.6.4.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	1000BASE-SX port compatible at the MDI	41.1.2.2		SXP:M	Yes [ ] N/A [ ]
CC2	1000BASE-LX port compatible at the MDI	41.1.2.2		LXP:M	Yes [ ] N/A [ ]
CC3	1000BASE-CX port compatible at the MDI	41.1.2.2		CXP:M	Yes [ ] N/A [ ]
CC4	1000BASE-T port compatible at the MDI	41.1.2.2		TP:M	Yes [ ] N/A [ ]
CC5	Internal segment compatibility	41.1.2.2.1	Internal port meets Clause 30 when repeater management implemented	M	Yes [ ]

41.6.4.2 Repeater functions

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Signal Restoration	41.2.1		M	Yes [ ]
RF2	Data Handling	41.2.1		M	Yes [ ]
RF3	Received Event Handling	41.2.1		M	Yes [ ]
RF4	Collision Handling	41.2.1		M	Yes [ ]
RF5	Error Handling	41.2.1		M	Yes [ ]
RF6	Partition	41.2.1		M	Yes [ ]
RF7	Received Jabber	41.2.1		M	Yes [ ]
RF8	Transmit	41.2.1		M	Yes [ ]
RF9	Receive	41.2.1		M	Yes [ ]

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41.6.4.3 Signal restoration function

Item	Feature	Subclause	Value/Comment	Status	Support
SR1	Output amplitude as required by 1000BASE-SX	41.2.1.1.1		SXP:M	Yes [ ] N/A [ ]
SR2	Output amplitude as required by 1000BASE-LX	41.2.1.1.1		LXP:M	Yes [ ] N/A [ ]
SR3	Output amplitude as required by 1000BASE-CX	41.2.1.1.1		CXP:M	Yes [ ] N/A [ ]
SR4	Output amplitude as required by 1000BASE-T	41.2.1.1.1		TP:M	Yes [ ] N/A [ ]
SR5	Output signal wave-shape as required by 1000BASE-SX	41.2.1.1.2		SXP:M	Yes [ ] N/A [ ]
SR6	Output signal wave-shape as required by 1000BASE-LX	41.2.1.1.2		LXP:M	Yes [ ] N/A [ ]
SR7	Output signal wave-shape as required by 1000BASE-CX	41.2.1.1.2		CXP:M	Yes [ ] N/A [ ]
SR8	Output signal wave-shape as required by 1000BASE-T	41.2.1.1.2		TP:M	Yes [ ] N/A [ ]
SR9	Output data timing as required by 1000BASE-SX	41.2.1.1.3		SXP:M	Yes [ ] N/A [ ]
SR10	Output data timing as required by 1000BASE-LX	41.2.1.1.3		LXP:M	Yes [ ] N/A [ ]
SR11	Output data timing as required by 1000BASE-CX	41.2.1.1.3		CXP:M	Yes [ ] N/A [ ]
SR12	Output data timing as required by 1000BASE-T	41.2.1.1.3		TP:M	Yes [ ] N/A [ ]

41.6.4.4 Data-Handling function

Item	Feature	Subclause	Value/Comment	Status	Support
DH1	Data frames forwarded to all ports except receiving port	41.2.1.2.1		M	Yes [ ]
DH2	Code Violations forwarded to all transmitting ports	41.2.1.2.2		M	Yes [ ]
DH3	Received Code Violation forwarded as code-group explicitly indicating received error	41.2.1.2.2		M	Yes [ ]
DH4	Code element substitution for remainder of packet after received Code Violation	41.2.1.2.2		M	Yes [ ]

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41.6.4.5 Receive Event-Handling function

Item	Feature	Subclause	Value/Comment	Status	Support
RE1	Detect all received events	41.2.1.3.1		M	Yes [ ]
RE2	Repeat all received signals	41.2.1.3.1		M	Yes [ ]
RE3	Preamble repeated as required	41.2.1.3.2		M	Yes [ ]
RE4	Start-of-packet propagation delay	41.2.1.3.3	SOP + SOJ ≤ 976 BT	M	Yes [ ]
RE5	Start-of-packet variability	41.2.1.3.4	SOP variation ≤ 16 BT	M	Yes [ ]
RE6	PHY repeater_mode variable	41.2.1.3.1	Shall be set to ensure CRS signal not asserted in response to transmit activity	M	Yes [ ]
RE7	Output preamble variation	41.2.1.3.2	Variation between received and transmitted preamble ≤ 8 BT	M	Yes [ ]

41.6.4.6 Collision-Handling function

Item	Feature	Subclause	Value/Comment	Status	Support
CO1	Collision Detection	41.2.1.4.1	Receive event on more than one port	M	Yes [ ]
CO2	Jam Generation	41.2.1.4.2	Transmit Jam message while collision is detected	M	Yes [ ]
CO3	Collision-Jam Propagation delay	41.2.1.4.3	SOP + SOJ ≤ 976 BT	M	Yes [ ]
CO4	Cessation of Collision Propagation delay	41.2.1.4.4	EOJ ≤ SOP	M	Yes [ ]

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41.6.4.7 Error-Handling function

Item	Feature	Subclause	Value/Comment	Status	Support
EH1	Carrier Integrity function implementation	41.2.1.5.1	Self-interrupt of data reception	M	Yes [ ]
EH2	False Carrier Event count for Link Unstable detection	41.2.1.5.1	False Carrier Event count equals FCELimit	M	Yes [ ]
EH3	False carrier count reset	41.2.1.5.1	Count reset on valid carrier	M	Yes [ ]
EH4	False carrier timer for Link Unstable detection	41.2.1.5.1	False carrier of length in excess of false_carrier_timer	M	Yes [ ]
EH5	Jam message duration	41.2.1.5.1	Equals duration of false carrier event, but not greater than duration of false_carrier_timer	M	Yes [ ]
EH6	Link Unstable detection	41.2.1.5.1	False Carrier Event count equals FCELimit or False carrier exceeds the false_carrier_timer or power-up reset	M	Yes [ ]
EH7	Messages sent to repeater unit in Link Unstable state	41.2.1.5.1	Inhibited sending messages to repeater unit	M	Yes [ ]
EH8	Messages sent from repeater unit in Link Unstable state	41.2.1.5.1	Inhibited sending output messages	M	Yes [ ]
EH9	Monitoring activity on a port in Link Unstable state	41.2.1.5.1	Continue monitoring activity at that port	M	Yes [ ]
EH10	Reset of Link Unstable state	41.2.1.5.1	No activity for more than ipg_timer plus idle_timer or Valid carrier event of duration greater than valid_carrier_timer preceded by Idle of duration greater than ipg_timer	M	Yes [ ]
EH11	Block flow of non-1000 Mb/s signals	41.2.1.5.2		M	Yes [ ]

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41.6.4.8 Partition function

Item	Feature	Subclause	Value/Comment	Status	Support
PA1	Partition function implementation	41.2.1.6	Self-interrupt of data reception	M	Yes [ ]
PA2	Consecutive Collision Event count for entry into partition state	41.2.1.6	Consecutive Collision Event count equals or exceeds CELimit	M	Yes [ ]
PA3	Excessive receive duration with collision for entry into partition state.	41.2.1.6	Reception duration in excess of jabber_timer with collision	M	Yes [ ]
PA4	Consecutive Collision Event counter incrementing	41.2.1.6	Count incremented on each transmission that suffers a collision	M	Yes [ ]
PA5	Consecutive Collision Event counter reset	41.2.1.6	Count reset on successful transmission or reception	M	Yes [ ]
PA6	Messages sent to repeater unit in Partition state	41.2.1.6	Inhibited sending messages to repeater unit	M	Yes [ ]
PA7	Messages sent from repeater unit in Partition state	41.2.1.6	Continue sending output messages	M	Yes [ ]
PA8	Monitoring activity on a port in Partition state	41.2.1.6	Continue monitoring activity at that port	M	Yes [ ]
PA9	Reset of Partition state	41.2.1.6	Power-up reset or transmitting or detecting activity for greater than duration no_collision_timer without a collision	M	Yes [ ]

41.6.4.9 Receive Jabber function

Item	Feature	Subclause	Value/Comment	Status	Support
RJ1	Receive Jabber function implementation	41.2.1.7	Self-interrupt of data reception	M	Yes [ ]
RJ2	Excessive receive duration timer for Receive Jabber detection	41.2.1.7	Reception duration in excess of jabber_timer	M	Yes [ ]
RJ3	Messages sent to repeater unit in Receive Jabber state	41.2.1.7	Inhibit sending input messages to repeater unit	M	Yes [ ]
RJ4	Messages sent from repeater unit in Receive Jabber state	41.2.1.7	Inhibit sending output messages	M	Yes [ ]
RJ5	Reset of Receive Jabber state	41.2.1.7	Power-up reset or Carrier no longer detected	M	Yes [ ]

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41.6.4.10 Repeater state diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	Repeater unit state diagram	41.2.2.2	Meets the requirements of Figure 41–2	M	Yes [ ]
SD2	Receive timer for port X state diagram	41.2.2.2	Meets the requirements of Figure 41–3	M	Yes [ ]
SD3	Repeater partition state diagram for port X	41.2.2.2	Meets the requirements of Figure 41–4	M	Yes [ ]
SD4	Carrier integrity monitor for port X state diagram	41.2.2.2	Meets the requirements of Figure 41–5	M	Yes [ ]

41.6.4.11 Repeater electrical

Item	Feature	Subclause	Value/Comment	Status	Support
EL1	Port-to-port isolation	41.3.1	Satisfies isolation and grounding requirements for attached network segments	M	Yes [ ]
EL2	Safety	41.4.1	IEC 60950: 1991	M	Yes [ ]
EL3	Installation practices	41.4.2.1	Sound, as defined by local code and regulations	M	Yes [ ]
EL4	Grounding	41.4.2.2	Chassis ground provided through ac mains cord	M	Yes [ ]
EL5	Two-port repeater set MTBF	41.4.4	At least 50 000 hours	M	Yes [ ]
EL6	Additional port effect on MTBF	41.4.4	No more than 3.46×10^{-6} increase in failures per hour	M	Yes [ ]
EL7	Electromagnetic interference	41.4.5.1	Comply with local or national codes	M	Yes [ ]

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41.6.4.12 Repeater labeling

Item	Feature	Subclause	Value/Comment	Status	Support
LB1	Crossover ports	41.5	Marked with an X	M	Yes [ ]
LB2	Data Rate	41.5	1000 Mb/s	O	Yes [ ] No [ ]
LB3	Safety warnings	41.5	Any applicable	O	Yes [ ] No [ ]
LB4	Port Types	41.5	1000BASE-SX, 1000BASE-LX, 1000BASE-CX, or 1000BASE-T	O	Yes [ ] No [ ]
LB5	Worse-case start-of-packet propagation delay	41.5	Value in bit times (BT)	O	Yes [ ] No [ ]
LB6	Worse-case start-of-collision-Jam propagation delay	41.5	Value in BT	O	Yes [ ] No [ ]
LB7	Worse-case Cessation-of-Collision Jam propagation delay	41.5	Value in BT	O	Yes [ ] No [ ]

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42. System considerations for multisegment 1000 Mb/s networks

42.1 Overview

This clause provides information on building 1000 Mb/s networks. The 1000 Mb/s technology is designed to be deployed in both homogenous 1000 Mb/s networks and 10/100/1000 Mb/s mixed networks using bridges and/or routers. Network topologies can be developed within a single 1000 Mb/s collision domain, but maximum flexibility is achieved by designing multiple collision domain networks that are joined by bridges and/or routers configured to provide a range of service levels to DTEs. For example, a combined 1000BASE-T/100BASE-T/10BASE-T system built with repeaters and bridges can deliver dedicated or shared service to DTEs at 1000 Mb/s, 100 Mb/s, or 10 Mb/s.

Linking multiple collision domains with bridges maximizes flexibility. Bridged topology designs can provide single data rate (Figure 42–1) or multiple data rate (Figure 42–2) services.

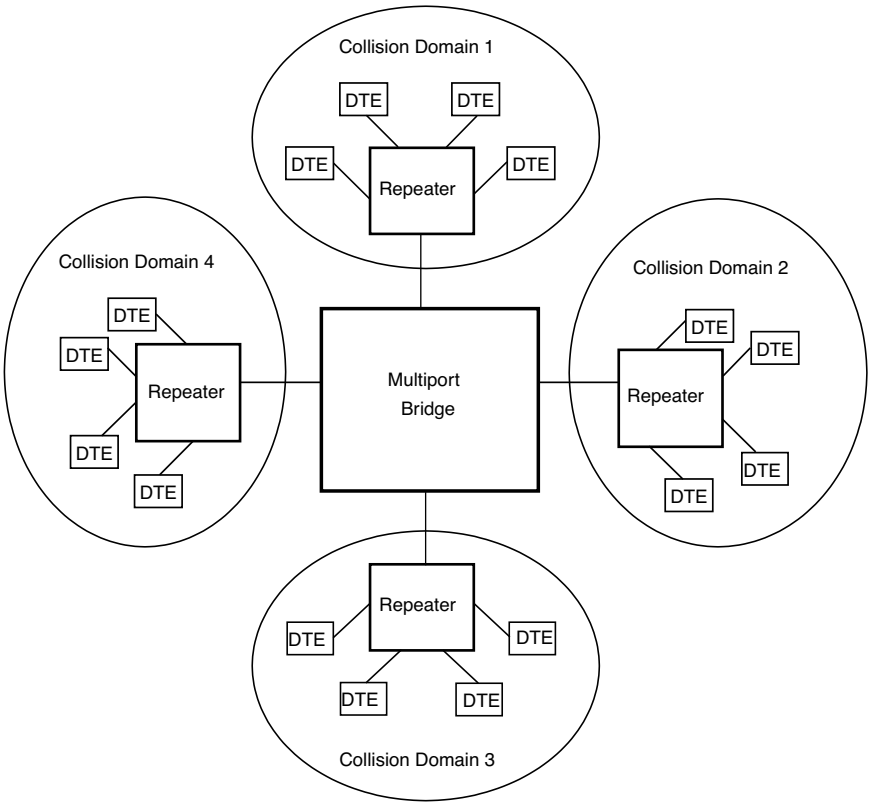


Figure 42–1—1000 Mb/s multiple collision domain topology using multiport bridge

Individual collision domains can be linked by single devices (as shown in Figure 42–1 and Figure 42–2) or by multiple devices from any of several transmission systems. The design of multiple-collision-domain networks is governed by the rules defining each of the transmission systems incorporated into the design.

The design of shared bandwidth 10 Mb/s collision domains is defined in Clause 13; the design of shared bandwidth 100 Mb/s CSMA/CD collision domains is defined in Clause 29; the design of shared bandwidth 1000 Mb/s CSMA/CD collision domains is defined in the following subclauses.

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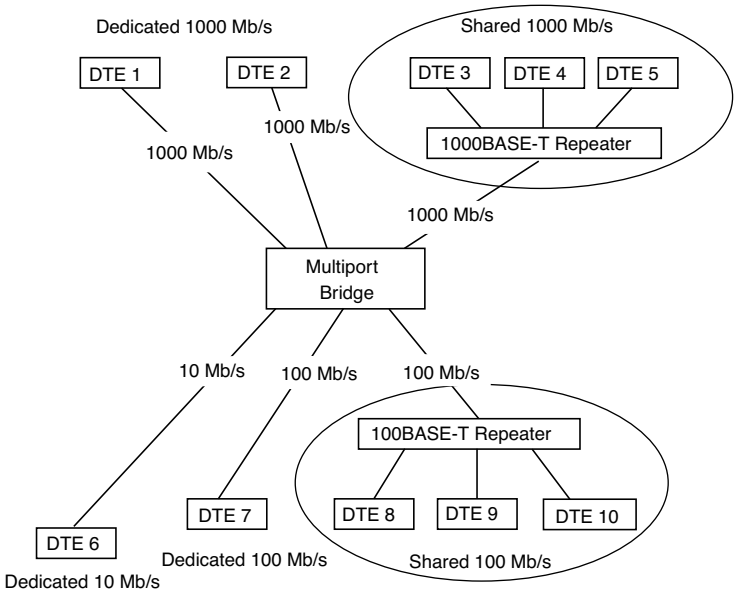


Figure 42–2—Multiple data rate, multiple collision domain topology using multiport bridge

42.1.1 Single collision domain multisegment networks

This clause provides information on building 1000 Mb/s CSMA/CD multisegment networks within a single collision domain. The proper operation of a CSMA/CD network requires the physical size of the collision domain to be limited in order to meet the round-trip propagation delay requirements of 4.2.3.2.3 and 4.4.2.1, and requires the number of repeaters to be limited to one so as not to exceed the InterFrameGap shrinkage noted in 4.4.2.4.

This clause provides two network models. Transmission System Model 1 is a set of configurations that have been validated under conservative rules and have been qualified as meeting the requirements set forth above. Transmission System Model 2 is a set of calculation aids that allow those configuring a network to test a proposed configuration against a simple set of criteria that allows it to be qualified. Transmission System Model 2 validates an additional broad set of topologies that are fully functional and do not fit within the simpler, but more restrictive rules of Model 1.

The physical size of a CSMA/CD network is limited by the characteristics of individual network components. These characteristics include the following:

a) Media lengths and their associated propagation time delay.
b) Delay of repeater units (start-up, steady-state, and end of event).
c) Delay of MAUs and PHYs (start-up, steady-state, and end of event).
d) Interpacket gap shrinkage due to repeater units.
e) Delays within the DTE associated with the CSMA/CD access method.
f) Collision detect and deassertion times associated with the MAUs and PHYs.

Table 42–1 summarizes the delays, measured in Bit Times (BTs), for 1000 Mb/s media segments.

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Table 42–1—Delays for network media segments Model 1

Media type	Maximum number of PHYs per segment	Maximum segment length (m)	Maximum medium round-trip delay per segment (BT)
Category 5 UTP Link Segment (1000BASE-T)	2	100	1112
Shielded Jumper Cable Link Segment (1000BASE-CX)	2	25	253
Optical Fiber Link Segment (1000BASE-SX, 1000BASE-LX)	2	316[a]	3192

[a]May be limited by the maximum transmission distance of the link.

42.1.2 Repeater usage

Repeaters are the means used to connect segments of a network medium together into a single collision domain. Different physical signaling systems (e.g., 1000BASE-CX, 1000BASE-SX, 1000BASE-LX, 1000BASE-T) can be joined into a common collision domain using a repeater. Bridges can also be used to connect different signaling systems; however, if a bridge is so used, each LAN connected to the bridge will comprise a separate collision domain.

42.2 Transmission System Model 1

The following network topology constraints apply to networks using Transmission System Model 1.

a) Single repeater topology maximum.
b) Link distances not to exceed the lesser of 316 m or the segment lengths as shown in Table 42–1.

42.3 Transmission System Model 2

Transmission System Model 2 is a single repeater topology with the physical size limited primarily by round-trip collision delay. A network configuration must be validated against collision delay using a network model for a 1000 Mb/s collision domain. The modeling process is quite straightforward and can easily be done either manually or with a spreadsheet.

The model proposed here is derived from the one presented in 13.4. Modifications have been made to accommodate adjustments for DTE, repeater, and cable speeds.

For a network consisting of two 1000BASE-T DTEs as shown in Figure 42–3, a crossover connection may be required if the auto-crossover function is not implemented. See 40.4 and 40.8.

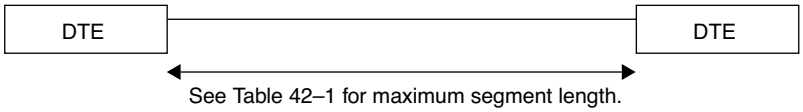


Figure 42–3—Model 1: Two DTEs, no repeater

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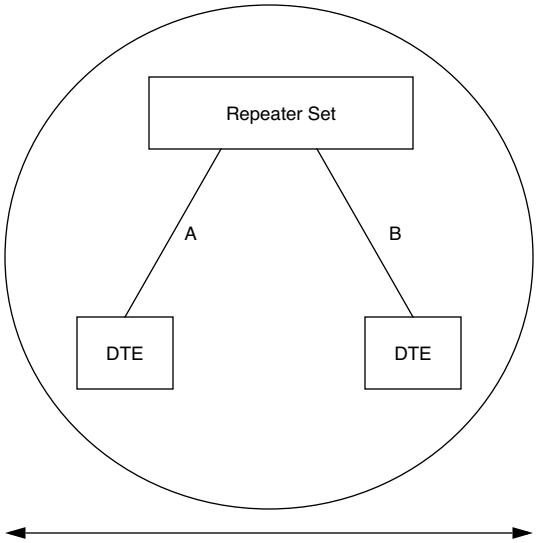


Figure 42–4—Model 1: Single repeater

Table 42–2—Maximum Model 1 collision domain diameter[a]

Configuration	Category 5 UTP (T)	Shielded Jumper Cable (CX)	Optical Fiber (SX/LX)	Mixed Category 5 and Fiber (T and SX/LX)	Mixed Shielded Jumper and Fiber (CX and SX/LX)
DTE-DTE (see Figure 42–3)	100	25	316[b]	NA	NA
One repeater (see Figure 42–4)	200	50	220	210[c]	220[d]

[a]In meters.
[b]May be limited by the maximum transmission distance of the link.
[c]Assumes 100 m of Category 5 UTP and one Optical Fiber link of 110 m.
[d]Assumes 25 m of Shielded Jumper Cable and one Optical Fiber link of 195 m.

42.3.1 Round-trip collision delay

For a network configuration to be valid, it must be possible for any two DTEs on the network to properly arbitrate for the network. When two or more stations attempt to transmit within a slot time interval, each station must be notified of the contention by the returned "collision" signal within the "collision window" (see 4.1.2.2). Additionally, the maximum length fragment created on a 1000 Mb/s network must contain less than 512 bytes after the Start Frame Delimiter (SFD). These requirements limit the physical diameter (maximum distance between DTEs) of a network. The maximum round-trip delay must be qualified between all pairs of DTEs in the network. In practice this means that the qualification must be done between those that, by inspection of the topology, are candidates for the longest delay. The following network modeling methodology is provided to assist that calculation.

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42.3.1.1 Worst-case path delay value (PDV) selection

The worst-case path through a network to be validated is identified by examination of aggregate DTE delays, cable delays, and repeater delay. The worst case consists of the path between the two DTEs at opposite ends of the network that have the longest round-trip time. Figure 42–5 shows a schematic representation of a one-repeater path.

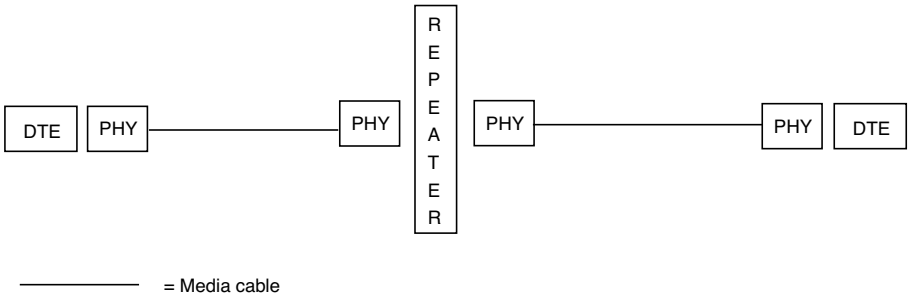


Figure 42–5——System Model 2: Single repeater

42.3.1.2 Worst-case PDV calculation

Once a set of paths is chosen for calculation, each is checked for validity against the following formula:

PDV = ∑link delays (LSDV) + repeater delay + DTE delays + safety margin

Values for the formula variables are determined by the following method:

a) Determine the delay for each link segment (Link Segment Delay Value, or LSDV), using the formula

LSDV=2 (for round-trip delay) × segment length × cable delay for this segment

NOTE 1—Length is the sum of the cable lengths between the PHY interfaces at the repeater and PHY interfaces at the farthest DTE. All measurements are in meters.

NOTE 2—Cable delay is the delay specified by the manufacturer or the maximum value for the type of cable used as shown in Table 42–3. For this calculation, cable delay must be specified in bit times per meter (BT/m). Table 42–4 can be used to convert values specified relative to the speed of light (%c) or nanoseconds per meter (ns/m).

NOTE 3—When actual cable lengths or propagation delays are not known, use the Max delay in bit times as specified in Table 42–3 for copper cables. Delays for fiber should be calculated, as the value found in Table 42–3 will be too large for most applications.

NOTE 4—The value found in Table 42–3 for Shielded Jumper Cable is the maximum delay for cable with solid dielectric. Cables with foam dielectric may have a significantly smaller delay.

b) Sum together the LSDVs for all segments in the path.

c) Determine the delay for the repeater. If model-specific data is not available from the manufacturer, enter the appropriate default value from Table 42–3.

d) Use the DTE delay value shown in Table 42–3 unless your equipment manufacturer defines a different value. If the manufacturer's supplied values are used, the DTE delays of both ends of the worst-case path should be summed together.

e) Decide on appropriate safety margin—0 to 40 bit times—for the PDV calculation. Safety margin is used to provide additional margin to accommodate unanticipated delay elements, such as extra-long connecting cable runs between wall jacks and DTEs. (A safety margin of 32 BT is recommended.)

f) Insert the values obtained through the calculations above into the following formula to calculate the PDV. (Some configurations may not use all the elements of the formula.)

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PDV = ∑link delays (LSDV) + repeater delay + DTE delay + safety margin

g) If the PDV is less than 4096, the path is qualified in terms of worst-case delay.
h) Late collisions and/or CRC errors may be indications that path delays exceed 4096 BT.

Table 42–3—Network component delays, Transmission System Model 2

Component	Round-trip delay in bit times per meter (BT/m)	Maximum round-trip delay in bit times (BT)
Two DTEs		864
Category 5 UTP Cable segment	11.12	1112 (100 m)
Shielded Jumper Cable segment	10.10	253 (25 m)
Optical Fiber Cable segment	10.10	1111 (110 m)
Repeater		976

Table 42–4—Conversion table for cable delays

Speed relative to c	ns/m	BT/m
0.4	8.34	8.34
0.5	6.67	6.67
0.51	6.54	6.54
0.52	6.41	6.41
0.53	6.29	6.29
0.54	6.18	6.18
0.55	6.06	6.06
0.56	5.96	5.96
0.57	5.85	5.85
0.58	5.75	5.75
0.5852	5.70	5.70
0.59	5.65	5.65
0.6	5.56	5.56
0.61	5.47	5.47
0.62	5.38	5.38
0.63	5.29	5.29

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Table 42–4—Conversion table for cable delays *(continued)*

Speed relative to c	ns/m	BT/m
0.64	5.21	5.21
0.65	5.13	5.13
0.654	5.10	5.10
0.66	5.05	5.05
0.666	5.01	5.01
0.67	4.98	4.98
0.68	4.91	4.91
0.69	4.83	4.83
0.7	4.77	4.77
0.8	4.17	4.17
0.9	3.71	3.71

42.4 Full duplex 1000 Mb/s topology limitations

Unlike half duplex CSMA/CD networks, the physical size of full duplex 1000 Mb/s networks is not limited by the round-trip collision propagation delay. Instead, the maximum link length between DTEs is limited only by the signal transmission characteristics of the specific link.

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43. Link Aggregation

43.1 Overview

This clause defines an optional Link Aggregation sublayer for use with CSMA/CD MACs. Link Aggregation allows one or more links to be aggregated together to form a Link Aggregation Group, such that a MAC Client can treat the Link Aggregation Group as if it were a single link. To this end, it specifies the establishment of DTE to DTE logical links, consisting of N parallel instances of full duplex point-to-point links operating at the same data rate.

43.1.1 Terminology

In this clause, unless otherwise noted, the term *link* refers to an *Aggregation Link* and the term *port* refers to *Aggregation Port,* as defined in 1.4. This allows for better readability of this clause while avoiding conflicting use of these terms in other clauses of this standard. Similarly, the term *Key* when used in this clause is synonymous with *Aggregation Key,* and the term *System* is synonymous with *Aggregation System*.

43.1.2 Goals and objectives

Link Aggregation, as specified in this clause, provides the following:

a) **Increased bandwidth**—The capacity of multiple links is combined into one logical link.
b) **Linearly incremental bandwidth**—Bandwidth can be increased in unit multiples as opposed to the order-of-magnitude increase available through Physical Layer technology options (10 Mb/s, 100 Mb/s, 1000 Mb/s, etc.).
c) **Increased availability**—The failure or replacement of a single link within a Link Aggregation Group need not cause failure from the perspective of a MAC Client.
d) **Load sharing**—MAC Client traffic may be distributed across multiple links.
e) **Automatic configuration**—In the absence of manual overrides, an appropriate set of Link Aggregation Groups is automatically configured, and individual links are allocated to those groups. If a set of links can aggregate, they will aggregate.
f) **Rapid configuration and reconfiguration**—In the event of changes in physical connectivity, Link Aggregation will quickly converge to a new configuration, typically on the order of 1 second or less.
g) **Deterministic behavior**—Depending on the selection algorithm chosen, the configuration can be made to resolve deterministically; i.e., the resulting aggregation can be made independent of the order in which events occur, and be completely determined by the capabilities of the individual links and their physical connectivity.
h) **Low risk of duplication or mis-ordering**—During both steady-state operation and link (re)configuration, there is a high probability that frames are neither duplicated nor mis-ordered.
i) **Support of existing IEEE 802.3 MAC Clients**—No change is required to existing higher-layer protocols or applications to use Link Aggregation.
j) **Backwards compatibility with aggregation-unaware devices**—Links that cannot take part in Link Aggregation—either because of their inherent capabilities, management configuration, or the capabilities of the devices to which they attach—operate as normal, individual IEEE 802.3 links.
k) **Accommodation of differing capabilities and constraints**—Devices with differing hardware and software constraints on Link Aggregation are, to the extent possible, accommodated.
l) **No change to the IEEE 802.3 frame format**—Link aggregation neither adds to, nor changes the contents of frames exchanged between MAC Clients.
m) **Network management support**—The standard specifies appropriate management objects for configuration, monitoring, and control of Link Aggregation.

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Link Aggregation, as specified in this clause, does not support the following:

n) **Multipoint Aggregations**—The mechanisms specified in this clause do not support aggregations among more than two Systems.
o) **Dissimilar MACs**—Link Aggregation is supported only on links using the IEEE 802.3 MAC.
p) **Half-duplex operation**—Link Aggregation is supported only on point-to-point links with MACs operating in full duplex mode.
q) **Operation across multiple data rates**—All links in a Link Aggregation Group operate at the same data rate (e.g., 10 Mb/s, 100 Mb/s, or 1000 Mb/s).

43.1.3 Positioning of Link Aggregation within the IEEE 802.3 architecture

Link Aggregation comprises an optional sublayer between a MAC Client and the MAC (or optional MAC Control sublayer). Figure 43–1 depicts the positioning of the Link Aggregation sublayer in the CSMA/CD layer architecture, and the relationship of that architecture to the Data Link and Physical Layers of the OSI Reference Model. The figure also shows the ability of the Link Aggregation sublayer to combine a number of individual links in order to present a single MAC interface to the MAC Client.

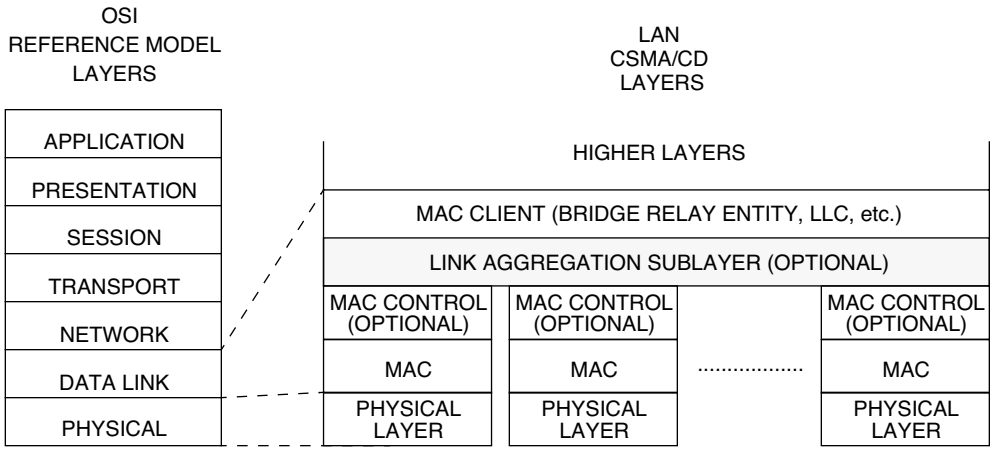


Figure 43–1—Architectural positioning of Link Aggregation sublayer

Figure 43–2 depicts the major blocks that form the Link Aggregation sublayer, and their interrelationships.

It is possible to implement the optional Link Aggregation sublayer for some ports within a System while not implementing it for other ports; i.e., it is not necessary for all ports in a System to be subject to Link Aggregation. A conformant implementation is not required to be able to apply the Link Aggregation sublayer to every port.

43.1.4 State diagram conventions

Many of the functions specified in this clause are presented in state diagram notation. All state diagrams contained in this clause use the notation and conventions defined in 21.5. In the event of a discrepancy between the text description and the state diagram formalization of a function, the state diagrams take precedence.

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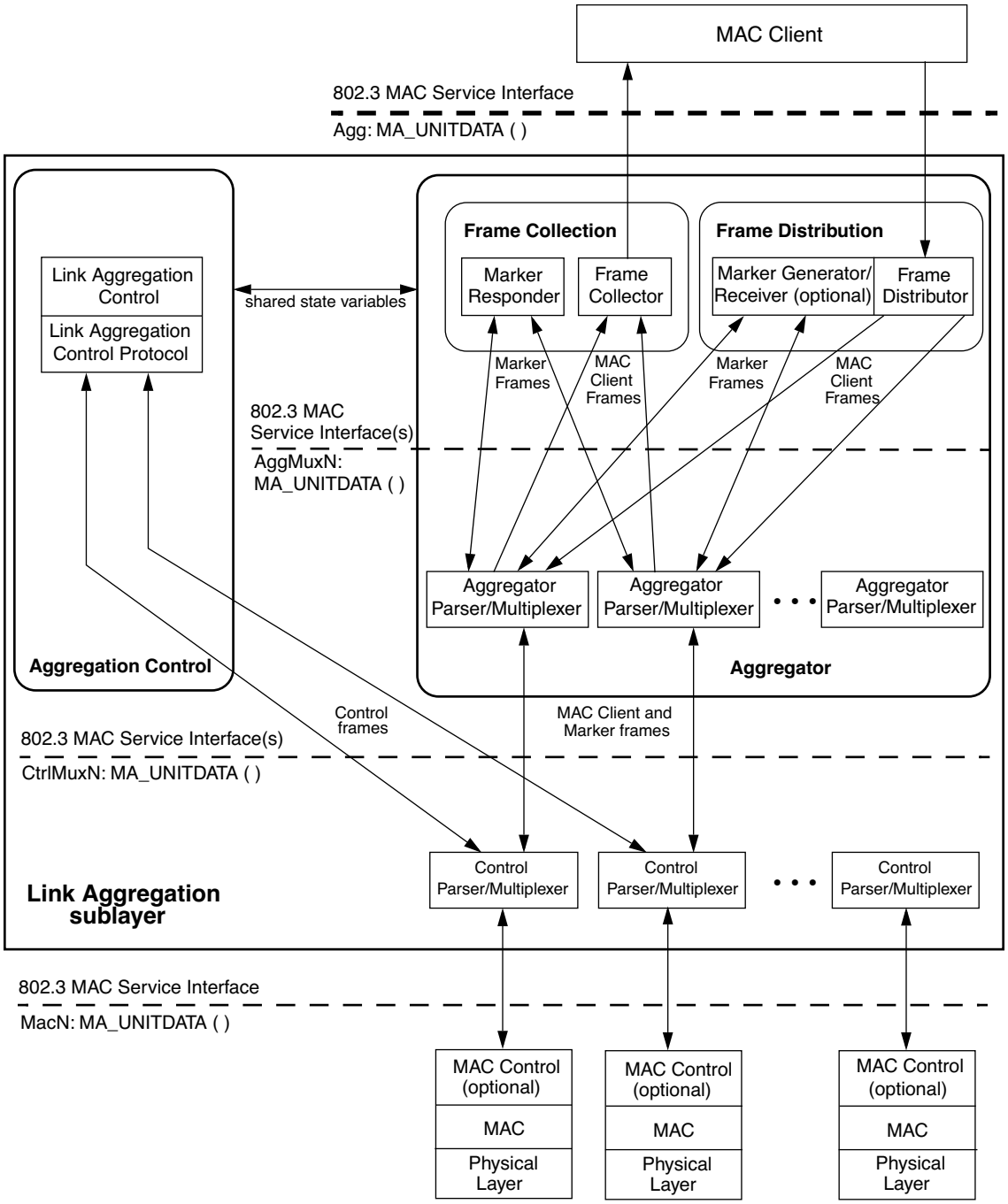


Figure 43–2—Link Aggregation sublayer block diagram

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43.2 Link Aggregation operation

As depicted in Figure 43–2, the Link Aggregation sublayer comprises the following functions:

a) *Frame Distribution*. This block is responsible for taking frames submitted by the MAC Client and submitting them for transmission on the appropriate port, based on a frame distribution algorithm employed by the Frame Distributor. Frame Distribution also includes an optional *Marker Generator/Receiver* used for the Marker protocol. (See 43.2.4, 43.2.5, and 43.5.)

b) *Frame Collection*. This block is responsible for passing frames received from the various ports to the MAC Client. Frame Collection also includes a *Marker Responder,* used for the Marker protocol. (See 43.2.3 and 43.5.)

c) *Aggregator Parser/Multiplexers*. On transmit, these blocks simply pass frame transmission requests from the Distributor, Marker Generator, and/or Marker Responder to the appropriate port. On receive, these blocks distinguish among Marker Request, Marker Response, and MAC Client PDUs, and pass each to the appropriate entity (Marker Responder, Marker Receiver, and Collector, respectively).

d) *Aggregator.* The combination of Frame Distribution and Collection, along with the Aggregator Parser/Multiplexers, is referred to as the Aggregator.

e) *Aggregation Control*. This block is responsible for the configuration and control of Link Aggregation. It incorporates a *Link Aggregation Control Protocol* (LACP) that can be used for automatic communication of aggregation capabilities between Systems and automatic configuration of Link Aggregation.

f) *Control Parser/Multiplexers*. On transmit, these blocks simply pass frame transmission requests from the Aggregator and Control entities to the appropriate port. On receive, these blocks distinguish Link Aggregation Control PDUs from other frames, passing the LACPDUs to the appropriate sublayer entity, and all other frames to the Aggregator.

43.2.1 Principles of Link Aggregation

Link Aggregation allows a MAC Client to treat a set of one or more ports as if it were a single port. In doing so, it employs the following principles and concepts:

a) A MAC Client communicates with a set of ports through an Aggregator, which presents a standard IEEE 802.3 service interface to the MAC Client. The Aggregator binds to one or more ports within a System.

b) It is the responsibility of the Aggregator to distribute frame transmissions from the MAC Client to the various ports, and to collect received frames from the ports and pass them to the MAC Client transparently.

c) A System may contain multiple Aggregators, serving multiple MAC Clients. A given port will bind to (at most) a single Aggregator at any time. A MAC Client is served by a single Aggregator at a time.

d) The binding of ports to Aggregators within a System is managed by the Link Aggregation Control function for that System, which is responsible for determining which links may be aggregated, aggregating them, binding the ports within the System to an appropriate Aggregator, and monitoring conditions to determine when a change in aggregation is needed.

e) Such determination and binding may be under manual control through direct manipulation of the state variables of Link Aggregation (e.g., Keys) by a network manager. In addition, automatic determination, configuration, binding, and monitoring may occur through the use of a Link Aggregation Control Protocol (LACP). The LACP uses peer exchanges across the links to determine, on an ongoing basis, the aggregation capability of the various links, and continuously provides the maximum level of aggregation capability achievable between a given pair of Systems.

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f) Frame ordering must be maintained for certain sequences of frame exchanges between MAC Clients (known as conversations, see 1.4). The Distributor ensures that all frames of a given conversation are passed to a single port. For any given port, the Collector is required to pass frames to the MAC Client in the order that they are received from that port. The Collector is otherwise free to select frames received from the aggregated ports in any order. Since there are no means for frames to be misordered on a single link, this guarantees that frame ordering is maintained for any conversation.

g) Conversations may be moved among ports within an aggregation, both for load balancing and to maintain availability in the event of link failures.

h) This standard does not impose any particular distribution algorithm on the Distributor. Whatever algorithm is used should be appropriate for the MAC Client being supported.

i) Each port is assigned a unique, globally administered MAC address. This MAC address is used as the source address for frame exchanges that are initiated by entities within the Link Aggregation sublayer itself (i.e., LACP and Marker protocol exchanges).

NOTE—The LACP and Marker protocols use a multicast destination address for all exchanges, and do not impose any requirement for a port to recognize more than one unicast address on received frames.

j) Each Aggregator is assigned a unique, globally administered MAC address; this address is used as the MAC address of the aggregation from the perspective of the MAC Client, both as a source address for transmitted frames and as the destination address for received frames. The MAC address of the Aggregator may be one of the MAC addresses of a port in the associated Link Aggregation Group (see 43.2.10).

43.2.2 Service interfaces

The MAC Client communicates with the Aggregator using the standard service interface specified in Clause 2. Similarly, Link Aggregation communicates internally (between Frame Collection/Distribution, the Aggregator Parser/Multiplexers, the Control Parser/Multiplexers, and Link Aggregation Control) and with its bound ports using the same, standard service interface. No new interlayer service interfaces are defined for Link Aggregation.

Since Link Aggregation uses four instances of the MAC Service Interface, it is necessary to introduce a notation convention so that the reader can be clear as to which interface is being referred to at any given time. A prefix is therefore assigned to each service primitive, indicating which of the four interfaces is being invoked, as depicted in Figure 43–2. The prefixes are as follows:

a) *Agg:,* for primitives issued on the interface between the MAC Client and the Link Aggregation sublayer.

b) *AggMuxN:,* for primitives issued on the interface between Aggregator Parser/Multiplexer N and its internal clients (where N is the port number associated with the Aggregator Parser/Multiplexer).

c) *CtrlMuxN:,* for primitives issued on the interface between Control Parser/Multiplexer N and its internal clients (where N is the port number associated with the Control Parser/Multiplexer).

d) *MacN:,* for primitives issued on the interface between underlying MAC N and its Control Parser/Multiplexer (where N is the port number associated with the underlying MAC).

MAC Clients may generate Agg:MA_DATA.request primitives for transmission on an aggregated link. These are passed by the Frame Distributor to a port selected by the distribution algorithm. MacN:MA_DATA.indication primitives signifying received frames are passed unchanged from a port to the MAC Client by the Frame Collector.

MAC Clients that generate MA_CONTROL.request primitives (and which expect MA_CONTROL.indication primitives in response) cannot communicate through a Link Aggregation sublayer. They must communicate directly with the MAC Control entity through which these control primitives are to be sent and received.

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The multiplexing of such MAC Control clients with a Link Aggregation sublayer for simultaneous use of a single port is outside the scope of this standard.

The multiplexing of MAC Clients with a Link Aggregation sublayer for simultaneous use of an individual MAC that is also part of a Link Aggregation Group is outside the scope of this standard.

43.2.3 Frame Collector

A Frame Collector is responsible for receiving incoming frames (i.e., AggMuxN:MA_DATA.indications) from the set of individual links that form the Link Aggregation Group (through each link's associated Aggregator Parser/Multiplexer) and delivering them to the MAC Client. Frames received from a given port are delivered to the MAC Client in the order that they are received by the Frame Collector. Since the Frame Distributor is responsible for maintaining any frame ordering constraints, there is no requirement for the Frame Collector to perform any reordering of frames received from multiple links.

The Frame Collector shall implement the function specified in the state diagram shown in Figure 43–3 and the associated definitions contained in 43.2.3.1.

43.2.3.1 Frame Collector state diagram

43.2.3.1.1 Constants

CollectorMaxDelay
: In tens of microseconds, the maximum time that the Frame Collector may delay the delivery of a frame received from an Aggregator Parser to its MAC Client. Value is assigned by management or administration policy.
Value: Integer

43.2.3.1.2 Variables

DA
SA
m_sdu
status
: The parameters of the MA_DATA.indication primitive, as defined in Clause 2.

BEGIN
: A Boolean variable that is set to TRUE when the System is initialized or reinitialized, and is set to FALSE when (re-)initialization has completed.
Value: Boolean

43.2.3.1.3 Messages

Agg:MA_DATA.indication
AggMuxN:MA_DATA.indication
: The service primitives used to pass a received frame to a client with the specified parameters.

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43.2.3.1.4 State diagram

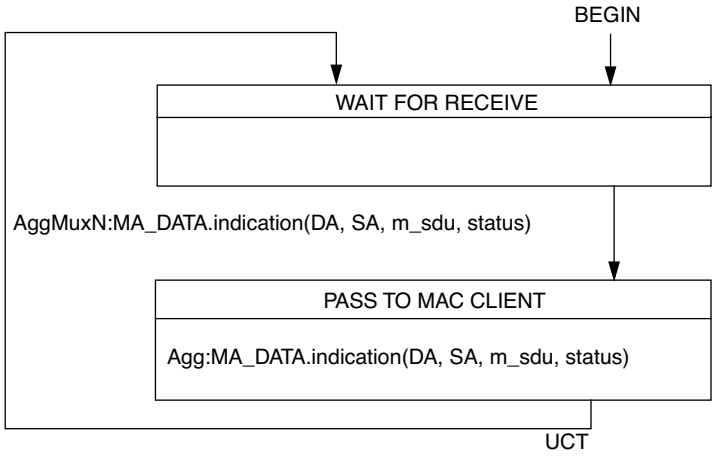


Figure 43–3—Frame Collector state diagram

The architectural models of the IEEE 802.3 MAC and Link Aggregation do not make any provision for queueing of frames between the link and the MAC Client. Furthermore, the state machine conventions used in this standard assume that actions within a state occur instantaneously (see 21.5). However, practical implementations of Link Aggregation will typically incur both queueing and delay in the Frame Collector. In order to ensure that frame delivery is not delayed indefinitely (which could cause a frame ordering problem when moving conversations from one link to another), the Frame Collector shall, upon receiving a frame from an Aggregator Parser, either deliver the frame to its MAC Client, or discard the frame within a CollectorMaxDelay time. The Frame Distributor (within the Partner System at the other end of the link) can assume that all frames transmitted on a given link have been either received by its Partner's MAC Client or discarded after a CollectorMaxDelay plus the propagation delay of the link. The use of CollectorMaxDelay is further discussed in 43A.3.

43.2.4 Frame Distributor

The Frame Distributor is responsible for taking outgoing frames from the MAC Client and transmitting them through the set of links that form the Link Aggregation Group. The Frame Distributor implements a distribution function (algorithm) responsible for choosing the link to be used for the transmission of any given frame or set of frames.

This standard does not mandate any particular distribution algorithm(s); however, any distribution algorithm shall ensure that, when frames are received by a Frame Collector as specified in 43.2.3, the algorithm shall not cause

a) Mis-ordering of frames that are part of any given conversation, or
b) Duplication of frames.

The above requirement to maintain frame ordering is met by ensuring that all frames that compose a given conversation are transmitted on a single link in the order that they are generated by the MAC Client; hence, this requirement does not involve the addition (or modification) of any information to the MAC frame, nor any buffering or processing on the part of the corresponding Frame Collector in order to re-order frames. This approach to the operation of the distribution function permits a wide variety of distribution and load balancing algorithms to be used, while also ensuring interoperability between devices that adopt differing algorithms.

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NOTE—The subject of distribution algorithms and maintenance of frame ordering is discussed in Annex 43A.

The Frame Distributor shall implement the function specified in the state diagram shown in Figure 43–4 and the associated definitions contained in 43.2.4.1.

43.2.4.1 Frame Distributor state diagram

43.2.4.1.1 Variables

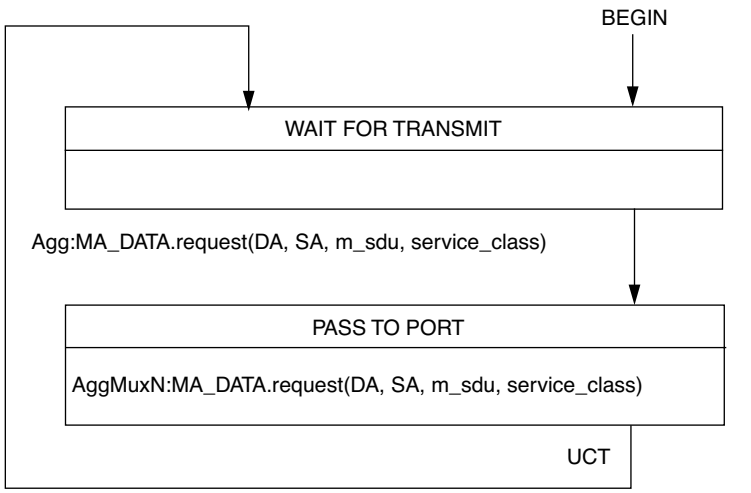
DA
SA
m_sdu
service_class
: The parameters of the MA_DATA.request primitive, as defined in Clause 2.

BEGIN
: A Boolean variable that is set to TRUE when the System is initialized or reinitialized, and is set to FALSE when (re-)initialization has completed.
Value: Boolean

43.2.4.1.2 Messages

Agg:MA_DATA.request
AggMuxN:MA_DATA.request
: The service primitives used to transmit a frame with the specified parameters.

43.2.4.1.3 State diagram



If a client issues an Agg:MA_DATA.request primitive that contains no SA parameter, the AggMuxN:MA_DATA.request primitive generated shall use the Aggregator's MAC address for the SA.

NOTE—The algorithm that the Frame Distributor uses to select the value of N in AggMuxN:MA_DATA.request for a given frame is unspecified.

Figure 43–4—Frame Distributor state diagram

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43.2.5 Marker Generator/Receiver (optional)

The optional Marker Generator is used by the Marker protocol, as specified in 43.5. When implemented and so requested by the Distribution algorithm, the Marker Generator shall issue an AggMuxN:MA_DATA.request primitive, with an m_sdu containing a Marker PDU as defined in 43.5.3, to the port associated with the conversation being marked, subject to the timing restrictions for Slow Protocols specified in Annex 43B.

The optional Marker Receiver is used by the Marker protocol, as specified in 43.5. It receives Marker Response PDUs from the Aggregator Parser.

43.2.6 Marker Responder

The Marker Responder is used by the Marker protocol, as specified in 43.5. The Marker Responder receives Marker PDUs (generated by a Partner System's Marker Generator), and transmits a Marker Response PDU through the same port from which the Marker PDU was received. While implementation of the Marker Generator/Receiver is optional, the ability to respond to a Marker PDU (the Marker Responder) is mandatory. An implementation conformant to this clause shall implement the Marker Responder as specified in 43.5.4.2, thus ensuring that implementations that need to make use of the protocol can do so.

43.2.7 Aggregator Parser/Multiplexer

On transmission, the Aggregator Multiplexer shall provide transparent pass-through of frames submitted by the Marker Responder and optional Marker Generator to the port specified in the transmission request. The Aggregator Multiplexer shall provide transparent pass-through of frames submitted by the Frame Distributor to the port specified in the transmission request only when the port state is Distributing (see 43.4.15); otherwise, such frames shall be discarded.

On receipt, the Aggregator Parser decodes frames received from the Control Parser, passes those frames destined for the Marker Responder or Marker Receiver to the selected entity, and discards frames with invalid Slow Protocol subtype values (see Table 43B–2). The Aggregator Parser shall pass all other frames to the Frame Collector for passage to the MAC Client only when the port state is Collecting (see 43.4.15); otherwise, such frames shall be discarded. The Aggregator Parser shall implement the function specified in the state diagram shown in Figure 43–5 and the associated definitions contained in 43.2.7.1.

43.2.7.1 Aggregator Parser state diagram

43.2.7.1.1 Constants

Slow_Protocols_Multicast
: The value of the Slow Protocols Multicast address. (See Table 43B–1.)

Slow_Protocols_Type
: The value of the Slow Protocols Length/Type field. (See Annex 43B.)

Marker_subtype
: The value of the Subtype field for the Marker protocol. (See 43.5.3.)
Value: Integer
2

Marker_Information
: The encoding of the Marker Information TLV_type field. (See 43.5.3.)
Value: Integer
1

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Marker_Response_Information
The encoding of the Marker Response Information TLV_type field. (See 43.5.3.)
Value: Integer
2

43.2.7.1.2 Variables

DA
SA
m_sdu
status
The parameters of the MA_DATA.indication primitive as defined in Clause 2.

Length/Type
The value of the Length/Type field in a received frame.
Value: Integer

Subtype
The value of the octet following the Length/Type field in a Slow Protocol frame. (See Annex 43B.)
Value: Integer

TLV_type
The value contained in the octet following the Version Number in a received Marker or Marker Response frame. This identifies the "type" for the Type/Length/Value (TLV) tuple. (See 43.5.3.)
Value: Integer

BEGIN
A Boolean variable that is set to TRUE when the System is initialized or reinitialized, and is set to FALSE when (re-)initialization has completed.
Value: Boolean

43.2.7.1.3 Messages

CtrlMuxN:MA_DATA.indication
AggMuxN:MA_DATA.indication
The service primitives used to pass a received frame to a client with the specified parameters.

43.2.8 Aggregator

An *Aggregator* comprises an instance of a Frame Collection function, an instance of a Frame Distribution function and one or more instances of the Aggregator Parser/Multiplexer function for a Link Aggregation Group. A single Aggregator is associated with each Link Aggregation Group. An Aggregator offers a standard IEEE 802.3 MAC service interface to its associated MAC Client; access to the MAC service by a MAC Client is always achieved via an Aggregator. An Aggregator can therefore be considered to be a *logical MAC*, bound to one or more ports, through which the MAC client is provided access to the MAC service.

A single, individual MAC address is associated with each Aggregator (see 43.2.10).

An Aggregator is available for use by the MAC Client if the following are all true:

a) It has one or more attached ports.
b) The Aggregator has not been set to a disabled state by administrative action (see 30.7.1.1.13).

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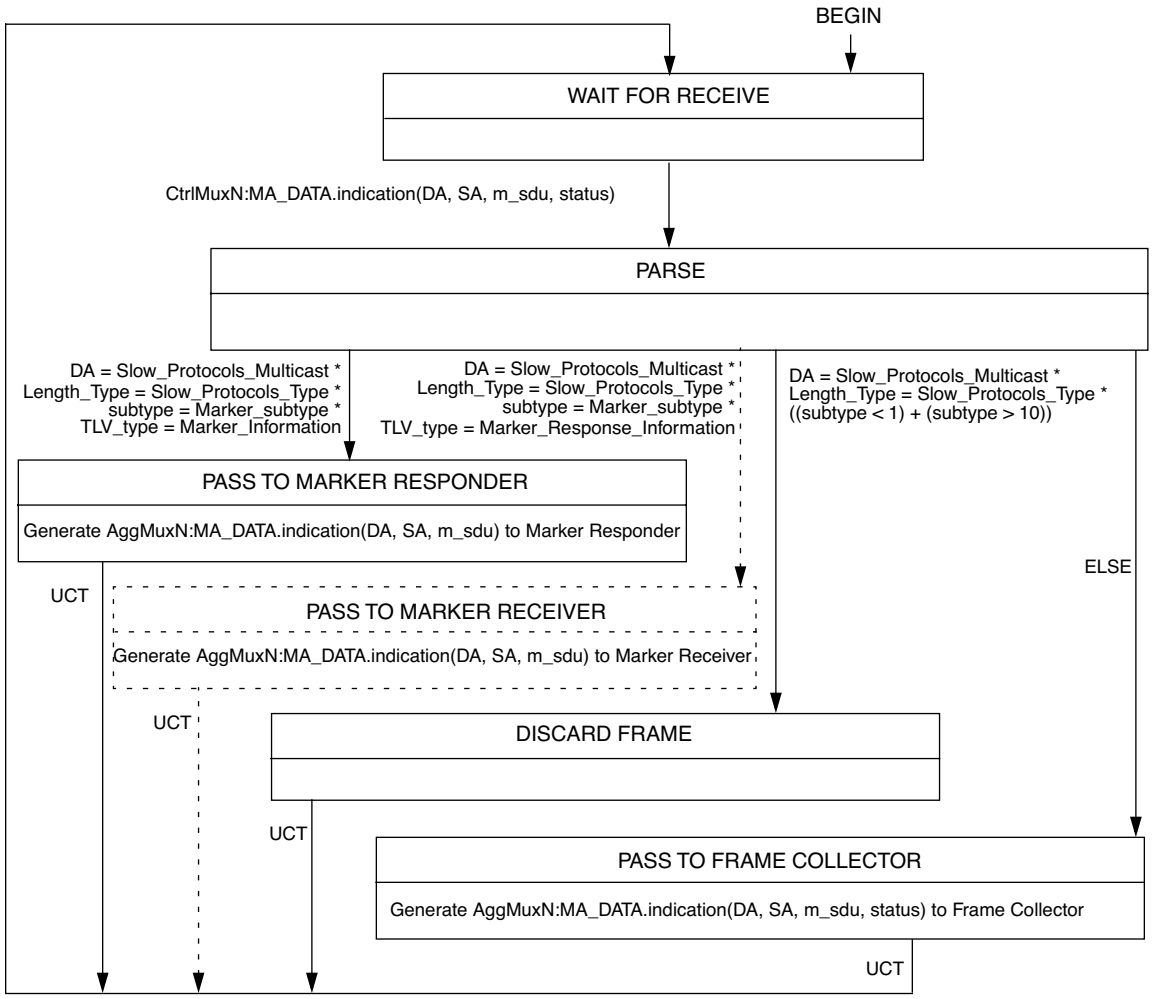
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c) The collection and/or distribution function associated with one or more of the attached ports is enabled (see 30.7.1.1.14).

NOTE—To simplify the modeling and description of the operation of Link Aggregation, it is assumed that there are as many Aggregators as there are ports in a given System; however, this is not a requirement of this standard. Aggregation of two or more ports consists of changing the bindings between ports and Aggregators such that more than one port is bound to a single Aggregator. The creation of any aggregations of two or more links will therefore result in one or more Aggregators that are bound to more than one port, and one or more Aggregators that are not bound to any port. An Aggregator that is not bound to any port appears to a MAC Client as a MAC interface to an inactive port. During times when the bindings between ports and Aggregators are changing, or as a consequence of particular configuration choices, there may be occasions when one or more ports are not bound to any Aggregator.

43.2.8.1 State diagram



If the optional Marker Receiver is not implemented, Marker Responses shall be passed to the Frame Collector. If the port state is not Collecting, all frames that would have been passed to the MAC Client through the Collector will be discarded.

Figure 43–5—Aggregator Parser state diagram

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43.2.9 Control Parser/Multiplexer

On transmission, the Control Multiplexer shall provide transparent pass-through of frames submitted by the Aggregator and Link Aggregation Control Protocol to the port specified in the transmission request.

On receipt, the Control Parser decodes frames received from the various ports in the Link Aggregation Group, passes those frames destined for the Link Aggregation Control Protocol to the appropriate entity, and passes all other frames to the Aggregator Parser. The Control Parser shall implement the function specified by the state diagram shown in Figure 43–6 and the associated definitions contained in 43.2.9.1.

43.2.9.1 Control Parser state diagram

43.2.9.1.1 Constants

Slow_Protocols_Multicast
: The value of the Slow Protocols Multicast address. (See Table 43B–1.)

Slow_Protocols_Type
: The value of the Slow Protocols Length/Type field. (See Table 43B–2.)

LACP_subtype
: The value of the Subtype field for the Link Aggregation Control Protocol. (See Table 43B–3.)
Value: Integer
1

43.2.9.1.2 Variables

DA
SA
m_sdu
status
: The parameters of the MA_DATA.indication primitive, as defined in Clause 2.

Length/Type
: The value of the Length/Type field in a received frame.
Value: Integer

Subtype
: The value of the octet following the Length/Type field in a Slow Protocol frame.
(See Annex 43B.)
Value: Integer

BEGIN
: A Boolean variable that is set to TRUE when the System is initialized or reinitialized, and is set to FALSE when (re-)initialization has completed.
Value: Boolean

43.2.9.1.3 Messages

MacN:MA_DATA.indication
CtrlMuxN:MA_DATA.indication
: The service primitives used to pass a received frame to a client with the specified parameters.

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43.2.9.1.4 State diagram

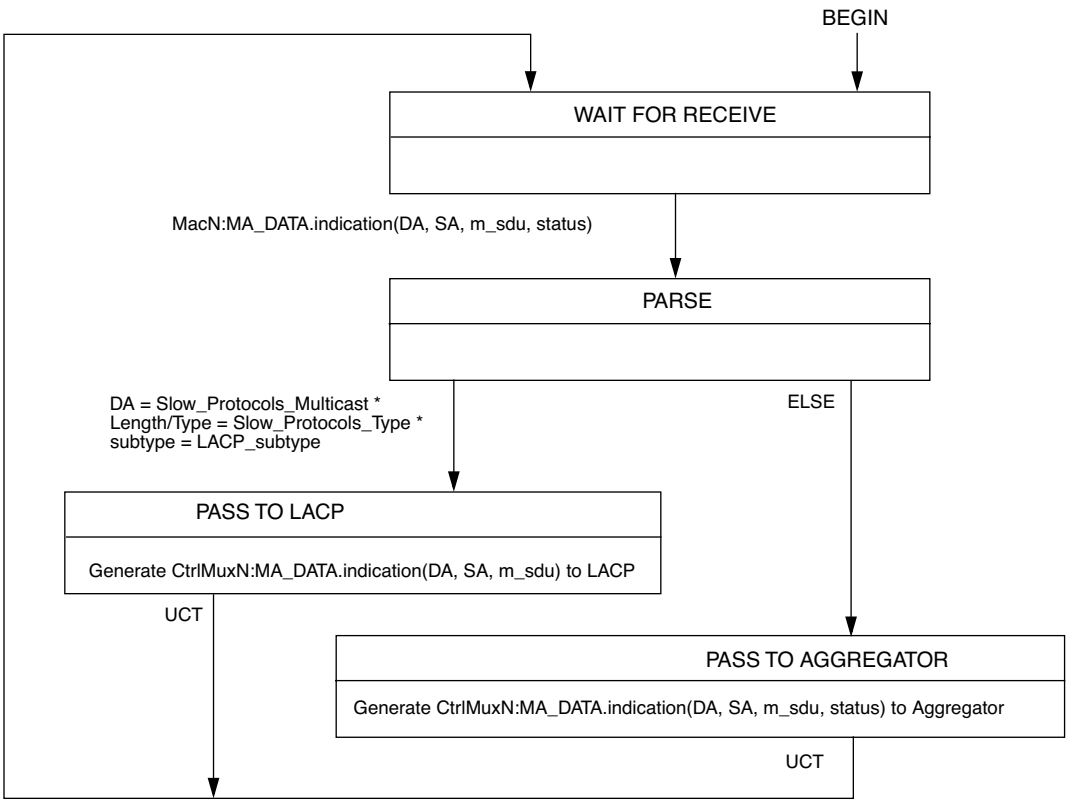


Figure 43–6—Control Parser state diagram

43.2.10 Addressing

Each IEEE 802.3 MAC has an associated globally-unique individual MAC address, whether that MAC is used for Link Aggregation or not (see Clause 4).

Each Aggregator to which one or more ports are attached has an associated globally-unique individual MAC address (see 43.3.3). The MAC address of the Aggregator may be the globally-unique individual MAC addresses of one of the MACs in the associated Link Aggregation Group, or it may be a distinct MAC address. The manner in which such addresses are chosen is not otherwise constrained by this standard.

Protocol entities sourcing frames from within the Link Aggregation sublayer (e.g., LACP and the Marker protocol) use the MAC address of the MAC within an underlying port as the source address in frames transmitted through that port. The MAC Client sees only the Aggregator and not the underlying MACs, and therefore uses the Aggregator's MAC address as the source address in transmitted frames. If a MAC Client submits a frame to the Aggregator for transmission without specifying a source address, the Aggregator inserts its own MAC address as the source address for transmitted frames.

NOTE—This behavior causes the Aggregator to behave the same way as a standard MAC with regard to frames submitted by its client.

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43.3 Link Aggregation Control

Link Aggregation Control configures and controls the Link Aggregation sublayer using static information local to the control function and dynamic information exchanged by means of the Link Aggregation Control Protocol.

For each aggregatable port in the System, Link Aggregation Control

a) Maintains configuration information (reflecting the inherent properties of the individual links as well as those established by management) to control aggregation.

b) Exchanges configuration information with other Systems to allocate the link to a Link Aggregation Group.

NOTE—A given link is allocated to, at most, one Link Aggregation Group at a time. The allocation mechanism attempts to maximize aggregation, subject to management controls.

c) Attaches the port to the Aggregator used by the Link Aggregation Group, and detaches the port from the Aggregator when it is no longer used by the Group.

d) Uses information from the Partner System's Link Aggregation Control entity to enable or disable the Aggregator's Collector and Distributor.

The operation of Link Aggregation Control involves the following activities, which are described in detail in the subclauses that follow:

e) Checking that candidate links can actually be aggregated.

f) Controlling the addition of a link to a Link Aggregation Group, and the creation of the group if necessary.

g) Monitoring the status of aggregated links to ensure that the aggregation is still valid.

h) Removing a link from a Link Aggregation Group if its membership is no longer valid, and removing the group if it no longer has any member links.

In order to allow Link Aggregation Control to determine whether a set of links connect to the same System, and to determine whether those links are compatible from the point of view of aggregation, it is necessary to be able to establish

i) A globally unique identifier for each System that participates in Link Aggregation (see 43.3.2).

j) A means of identifying the set of capabilities associated with each port and with each Aggregator, as understood by a given System.

k) A means of identifying a Link Aggregation Group and its associated Aggregator.

System identification allows the detection of links that are connected in a loopback configuration (i.e., both ends of the same link are connected to the same System).

43.3.1 Characteristics of Link Aggregation Control

Link Aggregation Control provides a configuration capability that is

a) **Automatic.** In the absence of manual override controls, an appropriate set of Link Aggregation Groups is automatically configured, and individual links are allocated to those groups. If a set of links can aggregate, they do aggregate.

b) **Continuous.** Manual intervention or initialization events are not a requirement for correct operation. The configuration mechanism continuously monitors for changes in state that require reconfiguration. The configuration functions detect and correct misconfigurations by performing reconfiguration and/or by taking misconfigured links out of service.

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c) **Deterministic.** The configuration can resolve deterministically; i.e., the configuration achieved can be made independent of the order in which events occur, and be completely determined by the combination of the capabilities of the individual links and their physical connectivity.
d) **Controllable.** The configuration capabilities accommodate devices with differing hardware and software constraints on Link Aggregation.
e) **Compatible.** Links that cannot take part in Link Aggregation, either because of their inherent capabilities or of the capabilities of the devices to which they attach, operate as normal IEEE 802.3 links. The introduction of Link Aggregation capability at one or both ends of a link should not result in a degradation of the perceived performance of the link.
f) **Rapid.** The configuration resolves rapidly to a stable configuration. Convergence can be achieved by the exchange of three LACPDUs, without dependence on timer values.

with

g) **Low risk of misdelivery.** The operation of the (re-)configuration functions minimizes the risk of frames being delivered to the wrong Aggregator.
h) **Low risk of duplication or mis-ordering.** The operation of the (re-)configuration functions minimizes the risk of frame duplication and frame mis-ordering.
i) **Low protocol overhead.** The overhead involved in external communication of configuration information between devices is small.

43.3.2 System identification

The globally unique identifier used to identify a System shall be the concatenation of a globally administered individual MAC address and the System Priority. The MAC address chosen may be the individual MAC address associated with one of the ports of the System.

Where it is necessary to perform numerical comparisons between System Identifiers, each System Identifier is considered to be an eight octet unsigned binary number, constructed as follows:

a) The two most significant octets of the System Identifier comprise the System Priority. The System Priority value is taken to be an unsigned binary number; the most significant octet of the System Priority forms the most significant octet of the System Identifier.
b) The third most significant octet of the System Identifier is derived from the initial octet of the MAC address; the least significant bit of the octet is assigned the value of the first bit of the MAC address, the next most significant bit of the octet is assigned the value of the next bit of the MAC address, and so on. The fourth through eighth octets are similarly assigned the second through sixth octets of the MAC address.

43.3.3 Aggregator identification

Each Aggregator to which one or more ports are attached shall be assigned a unique, globally administered individual MAC address. The MAC address assigned to the Aggregator may be the same as the MAC address assigned to one of its bound ports. No Aggregator shall be assigned a MAC address that is the same as that of a port bound to a different Aggregator within the System. When receiving frames, a port is never required to recognize more than one unicast address, i.e., the Aggregator's MAC address.

NOTE—This ensures that Aggregators can be uniquely addressed, and allows (but does not require) the unique address to be allocated from the same set of addresses as are assigned to the ports. It also acknowledges the fact that locally administered addresses may be used in particular implementations or environments. The stated restriction on the allocation of MAC addresses to Aggregators may have implications with regard to the choice of selection algorithm.

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An aggregator also shall be assigned an integer identifier that is used by Link Aggregation Control to uniquely identify the aggregator within the System. This value will typically be the same as the interface identifier (ifIndex) used for management purposes.

43.3.4 Port identification

Link Aggregation Control uses a Port Identifier, comprising the concatenation of a Port Priority and a Port Number, to identify the port. Port Numbers (and hence, Port Identifiers) shall be uniquely assigned within a System. Port Number 0 shall not be assigned to any port.

When it is necessary to perform numerical comparisons between Port Identifiers, each Port Identifier is considered to be a four octet unsigned binary number constructed as follows:

a) The most significant and second most significant octets are the first and second most significant octets of the Port Priority, respectively.
b) The third and fourth most significant octets are the first and second most significant octets of the Port Number, respectively.

43.3.5 Capability identification

The ability of one port to aggregate with another is summarized by a simple integer parameter, known as a Key. This facilitates communication and comparison of aggregation capabilities, which may be determined by a number of factors, including

a) The port's physical characteristics, such as data rate, duplexity, point-to-point or shared medium.
b) Configuration constraints established by the network administrator.
c) Use of the port by higher layer protocols (e.g. assignment of Network Layer addresses).
d) Characteristics or limitations of the port implementation itself.

Two Keys shall be associated with each port: an operational Key and an administrative Key. The operational Key is the Key that is currently in active use for the purposes of forming aggregations. The administrative Key allows manipulation of Key values by management. The administrative and operational Keys assigned to a port may differ

e) If the operation of the implementation is such that an administrative change to a Key value cannot be immediately reflected in the operational state of the port.
f) If the System supports the dynamic manipulation of Keys, as discussed in 43.6.2, either to accurately reflect changes in operational capabilities of the port (for example, as a result of Auto-Negotiation), or to provide a means of handling constraints on aggregation capability.

A given Key value is meaningful only in the context of the System that allocates it; there is no global significance to Key values. Similarly, the relationship between administrative and operational Key values is meaningful only in the context of the System that allocates it. When a System assigns an administrative Key value to a set of ports, it signifies that the set of ports have the potential to aggregate together, subject to the considerations discussed in 43.6.2. When a System assigns an operational Key value to a set of ports, it signifies that, in the absence of other constraints, the current operational state of the set of ports allows any subset of that set of ports (including the entire set) to be aggregated together from the perspective of the System making the assignment. The set of such ports that will actually be aggregated will be those that terminate at a common Partner System, and for which that Partner System has assigned a common operational Key value, local to that Partner. The set of ports in a given System that share the same operational Key value are said to be members of the same Key Group.

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A System may determine that a given link is not able to be aggregated with other links. Such links are referred to as Individual links (as opposed to Aggregatable links). A System may declare a link to be Individual if the inherent properties of the link allow its use as part of an aggregation, but the system is aware of no other links that are capable of aggregating with this link (e.g., the System has allocated a unique operational Key value to the link).

The capability information communicated between Systems, therefore, includes this local knowledge of the aggregation capability of the link in addition to the operational Key value; i.e., whether the System considers the link to be Aggregatable or Individual.

An administrative Key value and an operational Key value shall also be associated with each Aggregator. The operational Key is the Key that is currently in active use for the purposes of forming aggregations. The administrative Key allows manipulation of Key values by management. The values of administrative and operational Key for an Aggregator may differ in the same manner as that of port Keys, per item e) and item f), in this subclause. Ports that are members of a given Key Group can only be bound to Aggregators that share the same operational Key value.

All Keys are 16-bit identifiers. All values except the null value (all zeroes) are available for local use.

NOTE—This model allows for two convenient initial configurations. The first is achieved by assigning each port an initial administrative and operational Key value identical to its port number, and assigning the same port numbers as Keys to the corresponding Aggregators for each port. A device with this initial configuration will bring up all links as individual, non-aggregated links. The second is achieved by assigning the same administrative and operational Key values to all ports with a common set of capabilities, and also to all Aggregators. A device with this initial configuration will attempt to aggregate together any set of links that have the same Partner System ID and operational Key, and for which both Systems are prepared to allow aggregation.

43.3.6 Link Aggregation Group identification

A Link Aggregation Group consists of either

a) One or more Aggregatable links that terminate in the same pair of Systems and whose ports belong to the same Key Group in each System, or
b) An Individual link.

43.3.6.1 Construction of the Link Aggregation Group Identifier

A unique Link Aggregation Group Identifier (LAG ID) is constructed from the following parameters for each of the communicating Systems:

a) The System Identifier
b) The operational Key assigned to the ports in the LAG
c) The Port Identifier, if the link is identified as an Individual link

The local System's values for these parameters shall be non-zero. In cases where the local System is unable to determine the remote System's values for these parameters by exchange of protocol information, administrative values are used in the construction of the LAG ID. The value of these administrative parameters for the remote System may be configured as zero, provided that the port(s) concerned are also configured to be Individual.

A compound identifier formed from the System Identifiers and Key values alone is sufficient to identify a LAG comprising Aggregatable links. However, such an identifier is not sufficient for a LAG comprising a single Individual link where the Partner System Identifier and operational Key may be zero. Even if these are non-zero there may be multiple Individual Links with the same System Identifier and operational Key combinations, and it becomes necessary to include Port Identifiers to provide unique LAG IDs.

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Given

d) S and T are System Identifiers,
e) K and L are the operational Keys assigned to a LAG by S and T respectively, and
f) P and Q are the Port Identifiers of the ports being attached if the LAG comprises a single Individual Link and zero if the LAG comprises one or more Aggregatable links,

then the general form of the unique LAG ID is [(SKP), (TLQ)].

To simplify comparison of LAG IDs it is conventional to order these such that S is the numerically smaller of S and T.

43.3.6.2 Representation of the Link Aggregation Group Identifier

In order to allow for convenient transcription and interpretation by human network personnel, this standard provides a convention for representing compound LAG IDs. Using this format

a) All fields are written as hexadecimal numbers, 2 digits per octet, in canonical format.
b) Octets are presented in order, from left to right. Within fields carrying numerical significance (e.g., priority values), the most significant octet is presented first, and the least significant octet last.
c) Within fields that carry MAC addresses, successive octets are separated by dashes (-), in accordance with the hexadecimal representation for MAC addresses defined in IEEE Std 802-1990.
d) Parameters of the LAG ID are separated by commas.

For example, consider the parameters for the two Partners in a Link Aggregation Group shown in Table 43–1.

Table 43–1—Example Partner Parameters

	Partner SKP	Partner TLQ
System Parameters (S, T)	System Priority = 0x8000 (see 43.4.2.2) System Identifier = AC-DE-48-03-67-80	System Priority = 0x8000 (see 43.4.2.2) System Identifier = AC-DE-48-03-FF-FF
Key Parameter (K, L)	Key = 0x0001	Key = 0x00AA
Port Parameters (P, Q)	Port Priority = 0x80 (see 43.4.2.2) Port Number = 0x0002	Port Priority = 0x80 (see 43.4.2.2) Port Number = 0x0002

The complete LAG ID derived from this information is represented as follows, for an Individual link:

[(SKP), (TLQ)] = [(8000,AC-DE-48-03-67-80,0001,80,0002), (8000,AC-DE-48-03-FF-FF,00AA,80,0002)]

The corresponding LAG ID for a set of Aggregatable links is represented as follows:

[(SKP), (TLQ)] = [(8000,AC-DE-48-03-67-80,0001,00,0000), (8000,AC-DE-48-03-FF-FF,00AA,00,0000)]

NOTE—The difference between the two representations is that, for an Aggregatable link, the port identifier components are zero.

It is recommended that this format be used whenever displaying LAG ID information for use by network personnel.

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43.3.7 Selecting a Link Aggregation Group

Each port is selected for membership in the Link Aggregation Group uniquely identified by the LAG ID (composed of operational information, both derived from local administrative parameters and received through the Link Aggregation Control Protocol). Initial determination of the LAG ID is delayed to allow receipt of such information from a peer Link Aggregation Control entity; in the event such information is not received, locally configured administrative defaults are assumed for the remote port's operational parameters.

Where a particular link is known to be Individual, the complete LAG ID is not required to select the Link Aggregation Group since the link will not be aggregated with any other.

43.3.8 Agreeing on a Link Aggregation Group

Before frames are distributed and collected from a link, both the local Link Aggregation Control entity and its remote peer (if present) need to agree on the Link Aggregation Group. The Link Aggregation Control Protocol allows each of the communicating entities to check their peer's current understanding of the LAG ID, and facilitates rapid exchange of operational parameters while that understanding differs from their own. The protocol entities monitor their operation and, if agreement is not reached (perhaps due to an implementation failure), management is alerted.

The ability of LACP to signal that a particular link is Individual can accelerate the use of the link since, if both Link Aggregation Control entities know that the link is Individual, full agreement on the LAG ID is not necessary.

43.3.9 Attaching a link to an Aggregator

Once a link has selected a Link Aggregation Group, Link Aggregation Control can attach that link to a compatible Aggregator. An Aggregator is compatible if

a) The Aggregator's operational Key matches the port's operational Key, and
b) All other links currently attached to the Aggregator have selected the same Link Aggregation Group.

If several compatible Aggregators exist, Link Aggregation Control may employ a locally determined algorithm, either to ensure deterministic behavior (i.e., independence from the order in which Aggregators become available) or to maximize availability of the aggregation to a MAC Client. If no compatible Aggregator exists, then it is not possible to enable the link until such a time as a compatible Aggregator becomes available.

NOTE—In a properly configured System, there should always be a suitable Aggregator available with the proper Key assigned to serve a newly created Link Aggregation Group, so the unavailability of a compatible Aggregator is normally a temporary state encountered while links are moved between Aggregators. However, given the flexibility of the Key scheme, and given that in some implementations there may not be enough Aggregators to service a given configuration of links, it is possible to create configurations in which there is no Aggregator available to serve a newly identified LAG, in which case the links that are members of that LAG cannot become active until such a time as the configuration is changed to free up an appropriate Aggregator.

Links that are not successful candidates for aggregation (e.g., links that are attached to other devices that cannot perform aggregation or links that have been manually configured to be non-aggregatable) are enabled to operate as individual IEEE 802.3 links. For consistency of modeling, such a link is regarded as being attached to a compatible Aggregator that can only be associated with a single link. That is, from the perspective of Link Aggregation, non-aggregated links are not a special case; they compose an aggregation with a maximum membership of one link.

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More than one link can select the same Link Aggregation Group within a short period of time and, as these links detach from their prior Aggregators, additional compatible Aggregators can become available. In order to avoid such events causing repeated configuration changes, Link Aggregation Control applies hysteresis to the attachment process and allows multiple links to be attached to an Aggregator at the same time.

43.3.10 Signaling readiness to transfer user data

Once a link has been attached to an Aggregator (43.3.9) compatible with the agreed-upon Link Aggregation Group (43.3.8), each Link Aggregation Control entity signals to its peer its readiness to transfer user data to and from the Aggregator's MAC Client. In addition to allowing time for the organization of local Aggregator resources, including the possibility that a compatible Aggregator may not exist, explicit signaling of readiness to transfer user data can be delayed to ensure preservation of frame ordering and prevention of frame duplication. Link Aggregation Control will not signal readiness until it is certain that there are no frames in transit on the link that were transmitted while the link was a member of a previous Link Aggregation Group. This may involve the use of an explicit Marker protocol that ensures that no frames remain to be received at either end of the link before reconfiguration takes place. The operation of the Marker protocol is described in 43.5. The decision as to when, or if, the Marker protocol is used is entirely dependent upon the nature of the distribution algorithm that is employed.

43.3.11 Enabling Collection and Distribution

Every Aggregator can enable or disable Collection and Distribution of frames for each port that is attached to the Aggregator. Initially, both Collection and Distribution are disabled. Once the Link Aggregation Control entity is ready to transfer user data using the link and its peer entity has also signaled readiness, the process of enabling the link can proceed. The Collector is enabled (thus preparing it to receive frames sent over the link by the remote Aggregator's Distributor) and that fact is communicated to the Partner. Once the received information indicates that the remote Aggregator's Collector is enabled, the Distributor is also enabled.

NOTE—This description assumes that the implementation is capable of controlling the state of the transmit and receive functions of the MAC independently. In an implementation where this is not possible, the transmit and receive functions are enabled or disabled together. The manner in which this is achieved is detailed in the description of the Mux machine (see 43.4.15).

If at least one port's Mux in the Link Aggregation Group is Collecting, then the Receive state of the corresponding Aggregator will be Enabled. If at least one port's Mux in the Link Aggregation Group is Distributing, then the Transmit state of the corresponding Aggregator will be Enabled.

43.3.12 Monitoring the membership of a Link Aggregation Group

Each link is monitored in order to confirm that the Link Aggregation Control functions at each end of the link still agree on the configuration information for that link. If the monitoring process detects a change in configuration that materially affects the link's membership in its current LAG, then it may be necessary to remove the link from its current LAG and to move it to a new LAG.

43.3.13 Detaching a link from an Aggregator

A port may be detached from the Aggregator used by its Link Aggregation Group as a result of protocol (e.g., Key) changes, or because of System constraints (e.g., exceeding a maximum allowable number of aggregated links, or device failures) at either end of the link. Both classes of events will cause the LAG ID information for the link to change, and it will be necessary for Link Aggregation Control to detach the link from its current Aggregator and move it to a new LAG (if possible). At the point where the change is detected, the Collecting and Distributing states for the port are set to FALSE. The Frame Distribution function is informed that the link is no longer part of the group, the changed configuration information is

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communicated to the corresponding Link Aggregation Partner, then the Frame Collection function is informed that the link is no longer part of the group.

Once a link has been removed from its Aggregator, the link can select its new Link Aggregation Group and then attach to a compatible Aggregator, as described in 43.3.7 and 43.3.9.

Any conversation that is reallocated to a different link as a result of detaching a link from an Aggregator shall have its frame ordering preserved. This may involve the use of the Marker protocol to ensure that no frames that form part of that conversation remain to be received at either end of the old link before the conversation can proceed on the new link.

43.3.14 Configuration and administrative control of Link Aggregation

Administrative configuration facilities allow a degree of control to be exerted over the way that links may be aggregated. In particular, administrative configuration allows

a) The Key values associated with a port to be identified or modified.
b) The Key values associated with an Aggregator to be identified or modified.
c) Links to be identified as being incapable of aggregation.
d) Link Aggregation Control Protocol parameters to be identified or modified.

43.3.15 Link Aggregation Control state information

The Link Aggregation Control function maintains the following information with respect to each link:

a) The identifier of the Link Aggregation Group to which it currently belongs.
b) The identifier of the Aggregator associated with that Link Aggregation Group.
c) The status of interaction between the Frame Collection function of the Aggregator and the link (Collecting TRUE or Collecting FALSE). Collecting TRUE indicates that the receive function of this link is enabled with respect to its participation in an aggregation; i.e., received frames will be passed up to the Aggregator for collection.
d) The status of interaction between the Frame Distribution function of the Aggregator and the link (Distributing TRUE or Distributing FALSE). Distributing TRUE indicates that the transmit function of this link is enabled with respect to its participation in an aggregation; i.e., frames may be passed down from the Aggregator's distribution function for transmission.

This state information is communicated directly between Link Aggregation Control and the Aggregator through shared state variables without the use of a formal service interface.

The Link Aggregation Control function maintains the following information with respect to each Aggregator:

e) The status of the Frame Collection function (Receive Enabled or Receive Disabled).
f) The status of the Frame Distribution function (Transmit Enabled or Transmit Disabled).

These status values are exactly the logical OR of the Collection and Distribution status of the individual links associated with that Aggregator; i.e., if one or more links in the Link Aggregation Group are Collecting, then the Aggregator is Receive Enabled, and if one or more links are Distributing, then the Aggregator is Transmit Enabled.

The Transmit and Receive status of the Aggregator effectively govern the point at which the Aggregator becomes available for use by the MAC Client, or conversely, the point at which it ceases to be available.

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43.4 Link Aggregation Control Protocol (LACP)

The Link Aggregation Control Protocol (LACP) provides a standardized means for exchanging information between Partner Systems on a link to allow their Link Aggregation Control instances to reach agreement on the identity of the Link Aggregation Group to which the link belongs, move the link to that Link Aggregation Group, and enable its transmission and reception functions in an orderly manner.

43.4.1 LACP design elements

The following considerations were taken into account during the development of the protocol described in this subclause:

a) The protocol depends upon the transmission of information and state, rather than the transmission of commands. LACPDUs sent by the first party (the Actor) convey to the second party (the Actor's protocol Partner) what the Actor knows, both about its own state and that of the Partner.
b) The information conveyed in the protocol is sufficient to allow the Partner to determine what action to take next.
c) Active or passive participation in LACP is controlled by LACP_Activity, an administrative control associated with each port, that can take the value Active LACP or Passive LACP. Passive LACP indicates the port's preference for not transmitting LACPDUs unless its Partner's control value is Active LACP (i.e., a preference not to speak unless spoken to). Active LACP indicates the port's preference to participate in the protocol regardless of the Partner's control value (i.e., a preference to speak regardless).
d) Periodic transmission of LACPDUs occurs if the LACP_Activity control of either the Actor or the Partner is Active LACP. These periodic transmissions will occur at either a slow or fast transmission rate depending upon the expressed LACP_Timeout preference (Long Timeout or Short Timeout) of the Partner System.
e) In addition to periodic LACPDU transmissions, the protocol transmits LACPDUs when there is a Need To Transmit (NTT) something to the Partner; i.e., when the Actor's state changes or when it is apparent from the Partner's LACPDUs that the Partner does not know the Actor's current state.
f) The protocol assumes that the rate of LACPDU loss is very low.

There is no explicit frame loss detection/retry mechanism employed by the LACP; however, if information is received from the Partner indicating that it does not have up-to-date information on the Actor's state, or if the next periodic transmission is due, then the Actor will transmit a LACPDU that will correctly update the Partner.

43.4.2 LACPDU structure and encoding

43.4.2.1 Transmission and representation of octets

All LACPDUs comprise an integral number of octets. The bits in each octet are numbered from 0 to 7, where 0 is the low-order bit. When consecutive octets are used to represent a numerical value, the most significant octet is transmitted first, followed by successively less significant octets.

When the encoding of (an element of) a LACPDU is depicted in a diagram

a) Octets are transmitted from top to bottom.
b) Within an octet, bits are shown with bit 0 to the left and bit 7 to the right, and are transmitted from left to right.
c) When consecutive octets are used to represent a binary number, the octet transmitted first has the more significant value.

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d) When consecutive octets are used to represent a MAC address, the least significant bit of the first octet is assigned the value of the first bit of the MAC address, the next most significant bit the value of the second bit of the MAC address, and so on through the eighth bit. Similarly the least significant through most significant bits of the second octet are assigned the value of the ninth through seventeenth bits of the MAC address, and so on for all the octets of the MAC address.

43.4.2.2 LACPDU structure

LACPDUs are basic IEEE 802.3 frames; they shall not be tagged (See Clause 3). The LACPDU structure shall be as shown in Figure 43–7 and as further described in the following field definitions:

a) *Destination Address (DA)*. The DA in LACPDUs is the Slow_Protocols_Multicast address. Its use and encoding are specified in Annex 43B.

b) *Source Address (SA)*. The SA in LACPDUs carries the individual MAC address associated with the port through which the LACPDU is transmitted.

c) *Length/Type*. LACPDUs are always Type encoded, and carry the Slow_Protocols_Type field value. The use and encoding of this type is specified in Annex 43B.

d) *Subtype*. The Subtype field identifies the specific Slow Protocol being encapsulated. LACPDUs carry the Subtype value 0x01.

e) *Version Number.* This identifies the LACP version; implementations conformant to this version of the standard carry the value 0x01.

f) *TLV_type = Actor Information*. This field indicates the nature of the information carried in this TLV-tuple. Actor information is identified by the value 0x01.

g) *Actor_Information_Length*. This field indicates the length (in octets) of this TLV-tuple, Actor information uses a length value of 20 (0x14).

h) *Actor_System_Priority*. The priority assigned to this System (by management or administration policy), encoded as an unsigned integer.

i) *Actor_System*. The Actor's System ID, encoded as a MAC address.

j) *Actor_Key*. The operational Key value assigned to the port by the Actor, encoded as an unsigned integer.

k) *Actor_Port_Priority*. The priority assigned to this port by the Actor (the System sending the PDU; assigned by management or administration policy), encoded as an unsigned integer.

l) *Actor_Port*. The port number assigned to the port by the Actor (the System sending the PDU), encoded as an unsigned integer.

m) *Actor_State*. The Actor's state variables for the port, encoded as individual bits within a single octet, as follows and as illustrated in Figure 43–8:

   1) *LACP_Activity* is encoded in bit 0. This flag indicates the Activity control value with regard to this link. Active LACP is encoded as a 1; Passive LACP is encoded as a 0.
   2) *LACP_Timeout* is encoded in bit 1. This flag indicates the Timeout control value with regard to this link. Short Timeout is encoded as a 1; Long Timeout is encoded as a 0.
   3) *Aggregation* is encoded in bit 2. If TRUE (encoded as a 1), this flag indicates that the System considers this link to be *Aggregatable*; i.e., a potential candidate for aggregation. If FALSE (encoded as a 0), the link is considered to be *Individual*; i.e., this link can be operated only as an individual link.
   4) *Synchronization* is encoded in bit 3. If TRUE (encoded as a 1), the System considers this link to be *IN_SYNC*; i.e., it has been allocated to the correct Link Aggregation Group, the group has been associated with a compatible Aggregator, and the identity of the Link Aggregation Group is consistent with the System ID and operational Key information transmitted. If FALSE (encoded as a 0), then this link is currently *OUT_OF_SYNC;* i.e., it is not in the right Aggregation.

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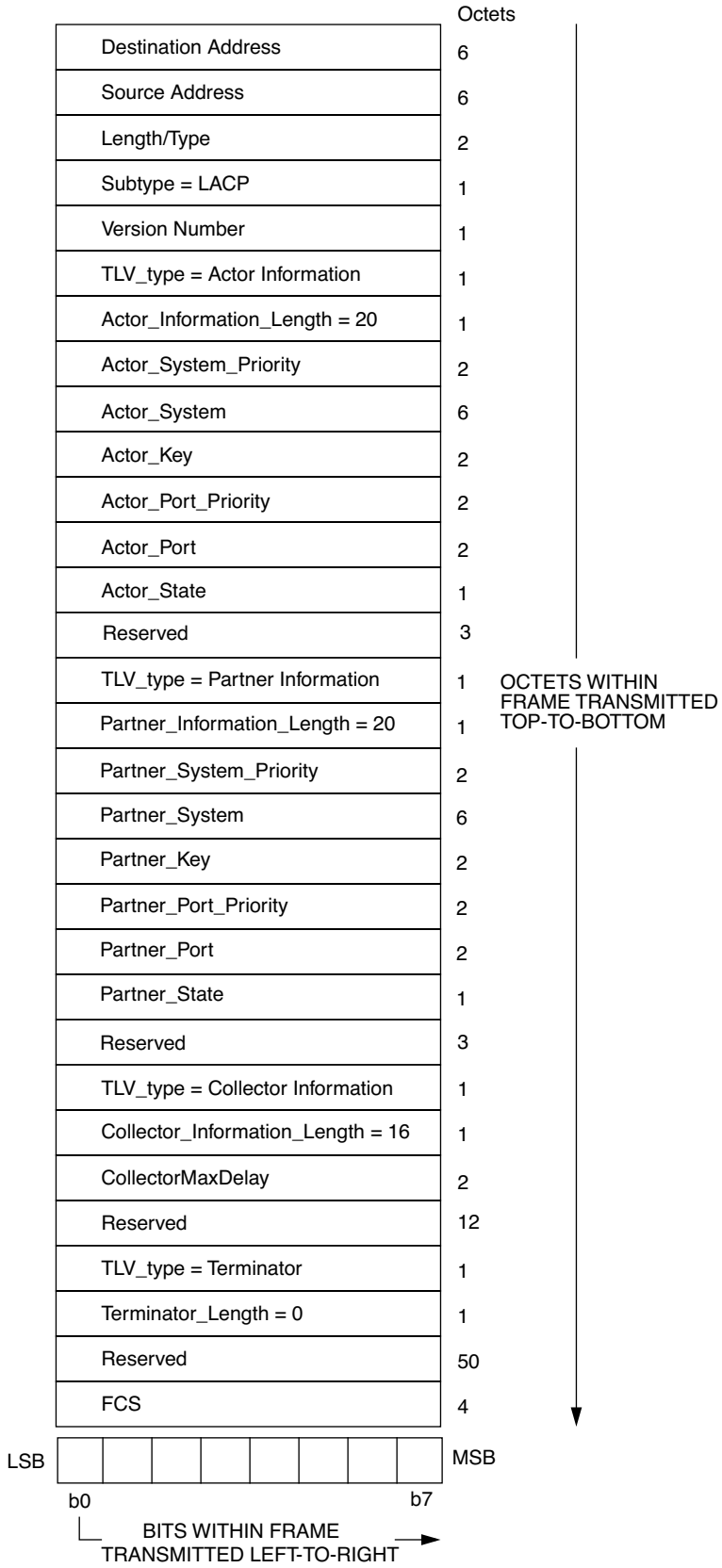


Figure 43–7—LACPDU structure

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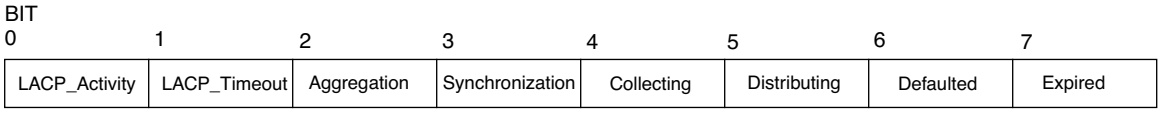
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5) *Collecting* is encoded in bit 4. TRUE (encoded as a 1) means collection of incoming frames on this link is definitely enabled; i.e., collection is currently enabled and is not expected to be disabled in the absence of administrative changes or changes in received protocol information. Its value is otherwise FALSE (encoded as a 0);
6) *Distributing* is encoded in bit 5. FALSE (encoded as a 0) means distribution of outgoing frames on this link is definitely disabled; i.e., distribution is currently disabled and is not expected to be enabled in the absence of administrative changes or changes in received protocol information. Its value is otherwise TRUE (encoded as a 1);
7) *Defaulted* is encoded in bit 6. If TRUE (encoded as a 1), this flag indicates that the Actor's Receive machine is using Defaulted operational Partner information, administratively configured for the Partner. If FALSE (encoded as a 0), the operational Partner information in use has been received in a LACPDU;
8) *Expired* is encoded in bit 7. If TRUE (encoded as a 1), this flag indicates that the Actor's Receive machine is in the EXPIRED state; if FALSE (encoded as a 0), this flag indicates that the Actor's Receive machine is not in the EXPIRED state.

NOTE—The received values of Defaulted and Expired state are not used by LACP; however, knowing their values can be useful when diagnosing protocol problems.



NOTE—Bit ordering within this field is as specified in 43.4.2.1.

Figure 43–8—Bit encoding of the Actor_State and Partner_State fields

n) *Reserved*. These 3 octets are reserved for use in future extensions to the protocol. They shall be ignored on receipt and shall be transmitted as zeroes to claim compliance with Version 1 of this protocol.
o) *TLV_type = Partner Information*. This field indicates the nature of the information carried in this TLV-tuple. Partner information is identified by the integer value 0x02.
p) *Partner_Information_Length*. This field indicates the length (in octets) of this TLV-tuple, Partner information uses a length value of 20 (0x14).
q) *Partner_System_Priority*. The priority assigned to the Partner System (by management or administration policy), encoded as an unsigned integer.
r) *Partner_System*. The Partner's System ID, encoded as a MAC address.
s) *Partner_Key*. The operational Key value assigned to the port associated with this link by the Partner, encoded as an unsigned integer.
t) *Partner_Port_Priority*. The priority assigned to this port by the Partner (by management or administration policy), encoded as an unsigned integer.
u) *Partner_Port*. The port number associated with this link assigned to the port by the Partner, encoded as an unsigned integer.
v) *Partner_State*. The Actor's view of the Partner's state variables, depicted in Figure 43–8 and encoded as individual bits within a single octet, as defined for Actor_State.
w) *Reserved*. These 3 octets are reserved for use in future extensions to the protocol. They shall be ignored on receipt and shall be transmitted as zeroes to claim compliance with Version 1 of this protocol.
x) *TLV_type = Collector Information*. This field indicates the nature of the information carried in this TLV-tuple. Collector information is identified by the integer value 0x03.

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y) *Collector_Information_Length*. This field indicates the length (in octets) of this TLV-tuple. Collector information uses a length value of 16 (0x10).

z) *CollectorMaxDelay*. This field contains the value of CollectorMaxDelay (43.2.3.1.1) of the station transmitting the LACPDU, encoded as an unsigned integer number of tens of microseconds. The range of values for this parameter is 0 to 65 535 tens of microseconds (0.65535 seconds).

aa) *Reserved*. These 12 octets are reserved for use in future extensions to the protocol. They shall be ignored on receipt and shall be transmitted as zeroes to claim compliance with Version 1 of this protocol.

ab) *TLV_type = Terminator*. This field indicates the nature of the information carried in this TLV-tuple. Terminator (end of message) information is identified by the integer value 0x00.

ac) *Terminator_Length*. This field indicates the length (in octets) of this TLV-tuple. Terminator information uses a length value of 0 (0x00).

NOTE—The use of a Terminator_Length of 0 is intentional. In TLV encoding schemes it is common practice for the terminator encoding to be 0 both for the type and the length.

ad) *Reserved*. These 50 octets are reserved for use in future extensions to the protocol. They are ignored on receipt and are transmitted as zeroes to claim compliance with Version 1 of this protocol.

NOTE—The Reserved octets are included in all valid LACPDUs in order to force the TLV lengths to multiples of 4 octets, and to force a fixed PDU size of 128 octets, regardless of the version of the protocol. Hence, a Version 1 implementation is guaranteed to be able to receive version N PDUs successfully, although version N PDUs may contain additional information that cannot be interpreted (and will be ignored) by the Version 1 implementation. A crucial factor in ensuring backwards compatibility is that any future version of the protocol is required not to re-define the structure or semantics of information defined for the previous version; it may only add new information elements to the previous set. Hence, in a version N PDU, a Version 1 implementation can expect to find the Version 1 information in exactly the same places as in a Version 1 PDU, and can expect to interpret that information as defined for Version 1. Future versions of this protocol expect to have the Reserved octets available for their use.

ae) *FCS*. This field is the Frame Check Sequence, typically generated by the underlying MAC.

43.4.3 LACP state machine overview

The operation of the protocol is controlled by a number of state machines, each of which performs a distinct function. These state machines are for the most part described on a per-port basis; any deviations from per-port description are highlighted in the text. Events (such as expiration of a timer or received LACPDUs) may cause state transitions and also cause actions to be taken; those actions may include the need for transmission of a LACPDU containing repeated or new information. Periodic and event-driven transmissions are controlled by the state of a Need-To-Transmit (NTT) variable (see 43.4.7), generated by the state machines as necessary.

The state machines are as follows:

a) *Receive machine (RX—43.4.12)*. This state machine receives LACPDUs from the Partner, records the information contained, and times it out using either Short Timeouts or Long Timeouts, according to the setting of LACP_Timeout. It evaluates the incoming information from the Partner to determine whether the Actor and Partner have both agreed upon the protocol information exchanged to the extent that the port can now be safely used, either in an aggregation with other ports or as an individual port; if not, it asserts NTT in order to transmit fresh protocol information to the Partner. If the protocol information from the Partner times out, the Receive machine installs default parameter values for use by the other state machines.

b) *Periodic Transmission machine (43.4.13)*. This state machine determines whether the Actor and its Partner will exchange LACPDUs periodically in order to maintain an aggregation (periodic LACPDU exchanges occur if either or both are configured for Active LACP).

c) *Selection Logic (43.4.14)*. The Selection Logic is responsible for selecting the Aggregator to be associated with this port.

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d) *Mux machine (MUX—43.4.15)*. This state machine is responsible for attaching the port to a selected Aggregator, detaching the port from a de-selected Aggregator, and for turning collecting and distributing at the port on or off as required by the current protocol information.

e) *Transmit machine (TX—43.4.16)*. This state machine handles the transmission of LACPDUs, both on demand from the other state machines, and on a periodic basis.

Figure 43–9 illustrates the relationships among these state machines and the flow of information between them. The set of arrows labelled Partner State Information represents new Partner information, contained in an incoming LACPDU or supplied by administrative default values, being fed to each state machine by the Receive machine. The set of arrows labelled Actor State Information represents the flow of updated Actor state information between the state machines. Transmission of LACPDUs occurs either as a result of the Periodic machine determining the need to transmit a periodic LACPDU, or as a result of changes to the Actor's state information that need to be communicated to the Partner. The need to transmit a LACPDU is signalled to the Transmit machine by asserting NTT. The remaining arrows represent shared variables in the state machine description that allow a state machine to cause events to occur in another state machine.

NOTE—The arrows marked Ready_N show that information derived from the operation of another port or ports can affect the operation of a port's state machine. See the definition of the Ready and Ready_N variables in 43.4.8.

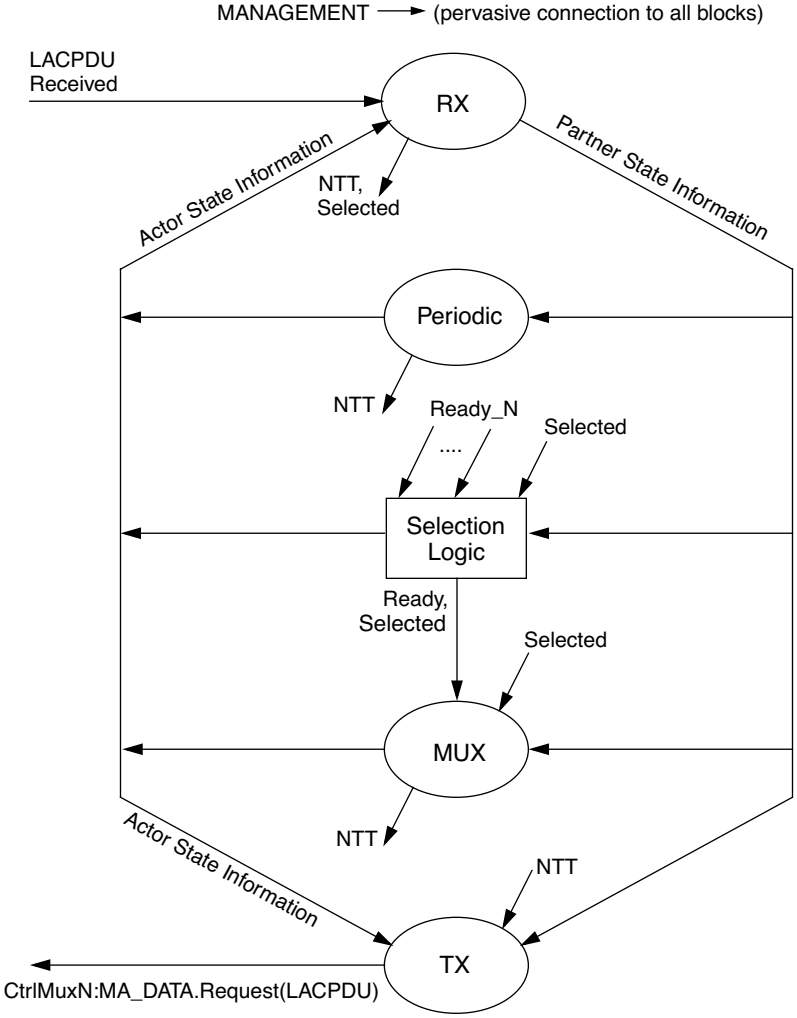


Figure 43–9—Interrelationships among state machines

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Two further state machines are defined for diagnostic purposes. They are as follows:

f) *Actor and Partner Churn Detection machines (43.4.17)*. These state machines make use of the IN_SYNC and OUT_OF_SYNC states generated by the Actor and Partner Mux machines in order to detect the situation where the state machines are unable to resolve the state of a given link; e.g., because the Partner System repeatedly sends conflicting information in its LACPDUs. As this situation can occur in a normally functioning link, particularly where either or both participating Systems have constrained aggregation capability (see 43.6), these state machines simply detect the presence of such a condition and signal its existence to management.

43.4.4 Constants

All timers specified in this subclause have an implementation tolerance of ± 250 ms.

Fast_Periodic_Time
The number of seconds between periodic transmissions using Short Timeouts.
Value: Integer
1

Slow_Periodic_Time
The number of seconds between periodic transmissions using Long Timeouts.
Value: Integer
30

Short_Timeout_Time
The number of seconds before invalidating received LACPDU information when using Short Timeouts (3 x Fast_Periodic_Time).
Value: Integer
3

Long_Timeout_Time
The number of seconds before invalidating received LACPDU information when using Long Timeouts (3 x Slow_Periodic_Time).
Value: Integer
90

Churn_Detection_Time
The number of seconds that the Actor and Partner Churn state machines wait for the Actor or Partner Sync state to stabilize.
Value: Integer
60

Aggregate_Wait_Time
The number of seconds to delay aggregation, to allow multiple links to aggregate simultaneously.
Value: Integer
2

43.4.5 Variables associated with the System

Actor_System
The MAC address component of the System Identifier of the System.
Value: 48 bits
Assigned by administrator or System policy.

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Actor_System_Priority
The System Priority of the System.
Value: Integer
Assigned by administrator or System policy.

43.4.6 Variables associated with each Aggregator

Aggregator_MAC_address
The MAC address assigned to the Aggregator.
Value: 48 bits
Assigned by administrator or System policy.

Aggregator_Identifier
Used to uniquely identify an Aggregator within a System.
Value: Integer
Assigned by administrator or System policy.

Individual_Aggregator
The aggregation capability of the Aggregator.
Value: Boolean
TRUE if the port attached to this Aggregator is not capable of aggregation with any other port.
FALSE if the port(s) attached to this Aggregator are capable of aggregation with other ports.

Actor_Admin_Aggregator_Key
The administrative Key value associated with the Aggregator.
Value: Integer
Assigned by administrator or System policy.

Actor_Oper_Aggregator_Key
The operational Key value associated with the Aggregator.
Value: Integer
Assigned by the Actor.

Partner_System
The MAC address component of the System Identifier of the remote System to which the Aggregator is connected. If the Aggregator has no attached ports, this variable is set to 0x00-00-00-00-00-00.
Value: 48 bits

Partner_System_Priority
The System Priority of the remote System to which the Aggregator is connected. If the Aggregator has no attached ports, this variable is set to zero.
Value: Integer

Partner_Oper_Aggregator_Key
The operational Key assigned to an aggregation by the remote System to which this Aggregator is connected. If the Aggregator has no attached ports, this variable is set to zero.
Value: Integer

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Receive_State
The Receive_State of the Aggregator will be Enabled if one or more ports attached to the Aggregator are Collecting (i.e., Actor_Oper_Port_State.Collecting is TRUE for any port). Otherwise, Receive_State is Disabled.
Values: Enabled or Disabled

Transmit_State
The Transmit_State of the Aggregator will be Enabled if one or more ports attached to the Aggregator are Distributing (i.e., Actor_Oper_Port_State.Distributing is TRUE for any port). Otherwise, Transmit_State is Disabled.
Values: Enabled or Disabled

LAG_Ports
The set of ports that belong to the Link Aggregation Group.
Value: Integer Array

43.4.7 Variables associated with each port

Actor_Port_Number
The port number assigned to the port.
Value: Integer
Assigned by administrator or System policy.

Actor_Port_Priority
The priority value assigned to the port, used to converge dynamic Key changes.
Value: Integer
Assigned by administrator or System policy.

Actor_Port_Aggregator_Identifier
The identifier of the Aggregator that this port is attached to.
Value: Integer

NTT
Need To Transmit flag.
Value: Boolean
TRUE indicates that there is new protocol information that should be transmitted on the link, or that the Partner needs to be reminded of the old information.
FALSE otherwise.

Actor_Admin_Port_Key
The administrative value of Key assigned to this port by administrator or System policy.
Value: Integer

Actor_Oper_Port_Key
The operational value of Key assigned to this port by the Actor.
Value: Integer

Actor_Admin_Port_State
The administrative values of the Actor's state parameters. This consists of the following set of variables, as described in 43.4.2.2:
LACP_Activity
LACP_Timeout
Aggregation
Synchronization

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Collecting
Distributing
Defaulted
Expired
Value: 8 bits

Actor_Oper_Port_State
The operational values of the Actor's state parameters. This consists of the following set of variables, as described in 43.4.2.2:
LACP_Activity
LACP_Timeout
Aggregation
Synchronization
Collecting
Distributing
Defaulted
Expired
Value: 8 bits

Partner_Admin_System
Default value for the MAC address component of the System Identifier of the Partner, assigned by administrator or System policy for use when the Partner's information is unknown or expired.
Value: 48 bits

Partner_Oper_System
The operational value of the MAC address component of the System Identifier of the Partner. The Actor sets this variable either to the value received from the Partner in an LACPDU, or to the value of Partner_Admin_System.
Value: 48 bits

Partner_Admin_System_Priority
Default value for the System Priority component of the System Identifier of the Partner, assigned by administrator or System policy for use when the Partner's information is unknown or expired.
Value: Integer

Partner_Oper_System_Priority
The operational value of the System Priority of the Partner. The Actor sets this variable either to the value received from the Partner in an LACPDU, or to the value of Partner_Admin_System_Priority.
Value: Integer

Partner_Admin_Key
Default value for the Partner's Key, assigned by administrator or System policy for use when the Partner's information is unknown or expired.
Value: Integer

Partner_Oper_Key
The operational value of the Key value assigned to this link by the Partner. The Actor sets this variable either to the value received from the Partner in an LACPDU, or to the value of Partner_Admin_Key.
Value: Integer

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Partner_Admin_Port_Number

Default value for the Port Number component of the Partner's Port Identifier, assigned by administrator or System policy for use when the Partner's information is unknown or expired.
Value: Integer

Partner_Oper_Port_Number

The operational value of the port number assigned to this link by the Partner. The Actor sets this variable either to the value received from the Partner in an LACPDU, or to the value of Partner_Admin_Port_Number.
Value: Integer

Partner_Admin_Port_Priority

Default value for the Port Priority component of the Partner's Port Identifier, assigned by administrator or System policy for use when the Partner's information is unknown or expired.
Value: Integer

Partner_Oper_Port_Priority

The operational value of the priority value assigned to this link by the Partner, used to converge dynamic Key changes. The Actor sets this variable either to the value received from the Partner in an LACPDU, or to the value of Partner_Admin_Port_Priority.
Value: Integer

Partner_Admin_Port_State

Default value for the Partner's state parameters, assigned by administrator or System policy for use when the Partner's information is unknown or expired. The value consists of the following set of variables, as described in 43.4.2.2:

LACP_Activity
LACP_Timeout
Aggregation
Synchronization
Collecting
Distributing
Defaulted
Expired

The value of Collecting shall be set the same as the value of Synchronization.
Value: 8 bits

Partner_Oper_Port_State

The operational value of the Actor's view of the current values of the Partner's state parameters. The Actor sets this variable either to the value received from the Partner in an LACPDU, or to the value of Partner_Admin_Port_State. The value consists of the following set of variables, as described in 43.4.2.2:

LACP_Activity
LACP_Timeout
Aggregation
Synchronization
Collecting
Distributing
Defaulted
Expired

Value: 8 bits

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port_enabled

A variable indicating that the physical layer has indicated that the link has been established and the port is operable.

Value: Boolean

TRUE if the physical layer has indicated that the port is operable.

FALSE otherwise.

NOTE—The means by which the value of the port_enabled variable is generated by the underlying MAC and/or PHY is implementation-dependent.

43.4.8 Variables used for managing the operation of the state machines

BEGIN

This variable indicates the initialization (or reinitialization) of the LACP protocol entity. It is set to TRUE when the System is initialized or reinitialized, and is set to FALSE when (re-)initialization has completed.

Value: Boolean

LACP_Enabled

This variable indicates that the port is operating the LACP. If the port is operating in half duplex, the value of LACP_Enabled shall be FALSE. Otherwise, the value of LACP_Enabled shall be TRUE.

Value: Boolean

actor_churn

This variable indicates that the Actor Churn Detection machine has detected that a local port configuration has failed to converge within a specified time, and that management intervention is required.

Value: Boolean

partner_churn

This variable indicates that the Partner Churn Detection machine has detected that a remote port configuration has failed to converge within a specified time, and that management intervention is required.

Value: Boolean

Ready_N

The port asserts Ready_N TRUE to indicate to the Selection Logic that the wait_while_timer has expired and it is waiting (i.e., the port is in the WAITING state) to attach to an Aggregator. Otherwise, its value is FALSE. There is one Ready_N value for each port.

Value: Boolean

Ready

The Selection Logic asserts Ready TRUE when the values of Ready_N for all ports that are waiting to attach to a given Aggregator are TRUE. If any of the values of Ready_N for the ports that are waiting to attach to that Aggregator are FALSE, or if there are no ports waiting to attach to that Aggregator, then the value of Ready is FALSE.

Value: Boolean

Selected

A value of SELECTED indicates that the Selection Logic has selected an appropriate Aggregator. A value of UNSELECTED indicates that no aggregator is currently selected. A value of STANDBY indicates that although the Selection Logic has selected an appropriate Aggregator, aggregation restrictions currently prevent the port from being enabled as part of the aggrega-

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tion, and so the port is being held in a standby condition. This variable can only be set to SELECTED or STANDBY by the operation of the port's Selection Logic. It can be set to UNSELECTED by the operation of the port's Receive machine, or by the operation of the Selection Logic associated with another port.

NOTE—Setting Selected UNSELECTED in the Selection Logic associated with another port occurs if the Selection Logic determines that the other port has a stronger claim to attach to this port's current Aggregator.

Value: SELECTED, UNSELECTED, or STANDBY

port_moved
This variable is set to TRUE if the Receive machine for a port is in the PORT_DISABLED state, and the combination of Partner_Oper_System and Partner_Oper_Port_Number in use by that port has been received in an incoming LACPDU on a different port. This variable is set to FALSE once the INITIALIZE state of the Receive machine has set the Partner information for the port to administrative default values.
Value: Boolean

43.4.9 Functions

recordPDU
This function records the parameter values for the Actor carried in a received LACPDU (Actor_Port, Actor_Port_Priority, Actor_System, Actor_System_Priority, Actor_Key, and Actor_State variables) as the current Partner operational parameter values (Partner_Oper_Port_Number, Partner_Oper_Port_Priority, Partner_Oper_System, Partner_Oper_System_Priority, Partner_Oper_Key, and Partner_Oper_Port_State variables with the exception of Synchronization) and sets Actor_Oper_Port_State.Defaulted to FALSE.

This function also updates the value of the Partner_Oper_Port_State.Synchronization using the parameter values carried in received LACPDUs. Parameter values for the Partner carried in the received PDU (Partner_Port, Partner_Port_Priority, Partner_System, Partner_System_Priority, Partner_Key, and Partner_State.Aggregation) are compared to the corresponding operational parameter values for the Actor (Actor_Port_Number, Actor_Port_Priority, Actor_System, Actor_System_Priority, Actor_Oper_Port_Key, and Actor_Oper_Port_State.Aggregation). Partner_Oper_Port_State.Synchronization is set to TRUE if all of these parameters match, Actor_State.Synchronization in the received PDU is set to TRUE, and LACP will actively maintain the link in the aggregation.

Partner_Oper_Port_State.Synchronization is also set to TRUE if the value of Actor_State.Aggregation in the received PDU is set to FALSE (i.e., indicates an Individual link), Actor_State.Synchronization in the received PDU is set to TRUE, and LACP will actively maintain the link.

Otherwise, Partner_Oper_Port_State.Synchronization is set to FALSE.

LACP is considered to be actively maintaining the link if either the PDU's Actor_State.LACP_Activity variable is TRUE or both the Actor's Actor_Oper_Port_State.LACP_Activity and the PDU's Partner_State.LACP_Activity variables are TRUE.

recordDefault
This function records the default parameter values for the Partner carried in the Partner Admin parameters (Partner_Admin_Port_Number, Partner_Admin_Port_Priority, Partner_Admin_System, Partner_Admin_System_Priority, Partner_Admin_Key, and

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Partner_Admin_Port_State) as the current Partner operational parameter values (Partner_Oper_Port_Number, Partner_Oper_Port_Priority, Partner_Oper_System, Partner_Oper_System_Priority, Partner_Oper_Key, and Partner_Oper_Port_State) and sets Actor_Oper_Port_State.Defaulted to TRUE.

update_Selected

This function updates the value of the Selected variable, using parameter values from a newly received LACPDU. The parameter values for the Actor carried in the received PDU (Actor_Port, Actor_Port_Priority, Actor_System, Actor_System_Priority, Actor_Key, and Actor_State.Aggregation) are compared with the corresponding operational parameter values for the port's Partner (Partner_Oper_Port_Number, Partner_Oper_Port_Priority, Partner_Oper_System, Partner_Oper_System_Priority, Partner_Oper_Key, and Partner_Oper_Port_State.Aggregation). If one or more of the comparisons show that the value(s) received in the PDU differ from the current operational values, then Selected is set to UNSELECTED. Otherwise, Selected remains unchanged.

update_Default_Selected

This function updates the value of the Selected variable, using the Partner administrative parameter values. The administrative values (Partner_Admin_Port_Number, Partner_Admin_Port_Priority, Partner_Admin_System, Partner_Admin_System_Priority, Partner_Admin_Key, and Partner_Admin_Port_State.Aggregation) are compared with the corresponding operational parameter values for the Partner (Partner_Oper_Port_Number, Partner_Oper_Port_Priority, Partner_Oper_System, Partner_Oper_System_Priority, Partner_Oper_Key, and Partner_Oper_Port_State.Aggregation). If one or more of the comparisons shows that the administrative value(s) differ from the current operational values, then Selected is set to UNSELECTED. Otherwise, Selected remains unchanged.

update_NTT

This function updates the value of the NTT variable, using parameter values from a newly received LACPDU. The parameter values for the Partner carried in the received PDU (Partner_Port, Partner_Port_Priority, Partner_System, Partner_System_Priority, Partner_Key, Partner_State.LACP_Activity, Partner_State.LACP_Timeout, Partner_State.Synchronization, and Partner_State.Aggregation) are compared with the corresponding operational parameter values for the Actor (Actor_Port_Number, Actor_Port_Priority, Actor_System, Actor_System_Priority, Actor_Oper_Port_Key, Actor_Oper_Port_State.LACP_Activity, Actor_Oper_Port_State.LACP_Timeout, Actor_Oper_Port_State.Synchronization, and Actor_Oper_Port_State.Aggregation). If one or more of the comparisons show that the value(s) received in the PDU differ from the current operational values, then NTT is set to TRUE. Otherwise, NTT remains unchanged.

Attach_Mux_To_Aggregator

This function causes the port's Control Parser/Multiplexer to be attached to the Aggregator Parser/Multiplexer of the selected Aggregator, in preparation for collecting and distributing frames.

Detach_Mux_From_Aggregator

This function causes the port's Control Parser/Multiplexer to be detached from the Aggregator Parser/Multiplexer of the Aggregator to which the port is currently attached.

Enable_Collecting

This function causes the Aggregator Parser of the Aggregator to which the port is attached to start collecting frames from the port.

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Disable_Collecting
: This function causes the Aggregator Parser of the Aggregator to which the port is attached to stop collecting frames from the port.

Enable_Distributing
: This function causes the Aggregator Multiplexer of the Aggregator to which the port is attached to start distributing frames to the port.

Disable_Distributing
: This function causes the Aggregator Multiplexer of the Aggregator to which the port is attached to stop distributing frames to the port.

Enable_Collecting_Distributing
: This function causes the Aggregator Parser of the Aggregator to which the port is attached to start collecting frames from the port, and the Aggregator Multiplexer to start distributing frames to the port.

Disable_Collecting_Distributing
: This function causes the Aggregator Parser of the Aggregator to which the port is attached to stop collecting frames from the port, and the Aggregator Multiplexer to stop distributing frames to the port.

43.4.10 Timers

current_while_timer
: This timer is used to detect whether received protocol information has expired. If Actor_Oper_State.LACP_Timeout is set to Short Timeout, the timer is started with the value Short_Timeout_Time. Otherwise, it is started with the value Long_Timeout_Time (see 43.4.4).

actor_churn_timer
: This timer is used to detect Actor churn states. It is started using the value Churn_Detection_Time (see 43.4.4).

periodic_timer (time_value)
: This timer is used to generate periodic transmissions. It is started using the value Slow_Periodic_Time or Fast_Periodic_Time (see 43.4.4), as specified in the Periodic Transmission state machine.

partner_churn_timer
: This timer is used to detect Partner churn states. It is started using the value Churn_Detection_Time (see 43.4.4).

wait_while_timer
: This timer provides hysteresis before performing an aggregation change, to allow all links that will join this Aggregation to do so. It is started using the value Aggregate_Wait_Time (see 43.4.4).

43.4.11 Messages

CtrlMuxN:MA_DATA.indicate(LACPDU)
: This message is generated by the Control Parser as a result of the reception of a LACPDU, formatted as defined in 43.4.2.

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43.4.12 Receive machine

The Receive machine shall implement the function specified in Figure 43–10 with its associated parameters (43.4.4 through 43.4.11).

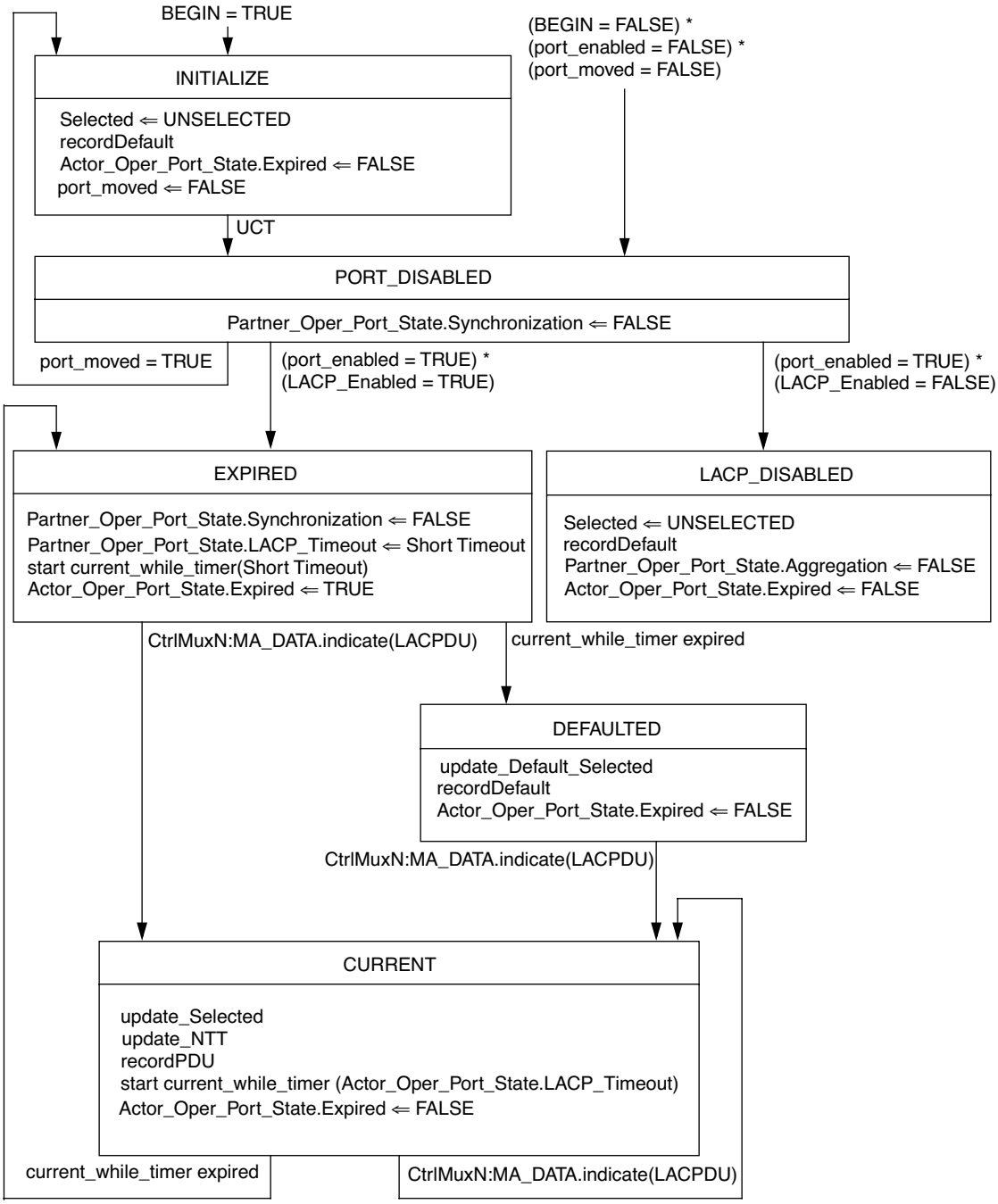


Figure 43–10—Receive machine state diagram

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On receipt of a LACPDU, the state machine enters the CURRENT state. The update_Selected function sets the Selected variable UNSELECTED if the Link Aggregation Group identified by the combination of the protocol Partner's own information and the Actor's own information has changed. The Selected variable is used by the Mux machine (43.4.15).

NOTE—The Receive machine may set the Selected variable to UNSELECTED; however, setting this variable to SELECTED or STANDBY is the responsibility of the Selection Logic.

The update_NTT function is used to determine whether further protocol transmissions are required; NTT is set to TRUE if the Partner's view of the Actor's operational parameters is not up to date. The recordPDU function records the information contained in the LACPDU in the Partner operational variables, and the current_while timer is started. The value used to start the timer is either Short_Timeout_Time or Long_Timeout_Time, depending upon the Actor's operational value of LACP_Timeout.

In the process of executing the recordPDU function, a Receive machine compliant to this standard shall not validate the Version Number, TLV_type, or Reserved fields in received LACPDUs. The same actions are taken regardless of the values received in these fields. A Receive machine may validate the Actor_Information_Length, Partner_Information_Length, Collector_Information_Length, or Terminator_Length fields. These behaviors, together with the constraint on future protocol enhancements, are discussed in 43.4.2.2.

NOTE—The rules expressed above allow Version 1 devices to be compatible with future revisions of the protocol.

If no LACPDU is received before the current_while timer expires, the state machine transits to the EXPIRED state. The Partner_Oper_Port_State.Synchronization variable is set to FALSE, the current operational value of the Partner's LACP_Timeout variable is set to Short Timeout, and the current_while timer is started with a value of Short_Timeout_Time. This is a transient state; the LACP_Timeout settings allow the Actor to transmit LACPDUs rapidly in an attempt to re-establish communication with the Partner.

If no LACPDU is received before the current_while timer expires again, the state machine transits to the DEFAULTED state. The recordDefault function overwrites the current operational parameters for the Partner with administratively configured values. This allows configuration of aggregations and individual links when no protocol Partner is present, while still permitting an active Partner to override default settings. The update_Default_Selected function sets the Selected variable UNSELECTED if the Link Aggregation Group has changed. Since all operational parameters are now set to locally administered values, there can be no disagreement as to the Link Aggregation Group, so the Partner_Oper_Port_State.Synchronization variable is set to TRUE.

If the port becomes inoperable and a BEGIN event has not occurred, the state machine enters the PORT_DISABLED state. Partner_Oper_Port_State.Synchronization is set to FALSE. This state allows the current Selection state to remain undisturbed, so that, in the event that the port is still connected to the same Partner and Partner port when it becomes operable again, there will be no disturbance caused to higher layers by unneccessary re-configuration. If the same Actor System ID and Port are seen in a LACPDU received on a different Port (port_moved is set to TRUE), this indicates that the physical connectivity has changed, and causes the state machine to enter the INITIALIZE state. This state is also entered if a BEGIN event occurs.

The INITIALIZE state causes the administrative values of the Partner parameters to be used as the current operational values, and sets Selected to UNSELECTED. These actions force the Mux machine to detach the port from its current Aggregator. The variable port_moved is set to FALSE; if the entry to INITIALIZE occurred as a result of port_moved being set to TRUE, then the state machine will immediately transition back to the PORT_DISABLED state.

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If the port is operating in half duplex, the operation of LACP is disabled on the port (LACP_Enabled is FALSE) and the LACP_DISABLED state is entered. This state is entered following a BEGIN or Port Enabled event. This state is similar to the DEFAULTED state, except that the port is forced to operate as an Individual port, as the value of Partner_Oper_Port_State.Aggregation is forced to Individual. Exit from this state occurs on a BEGIN or Port Disabled event.

43.4.13 Periodic Transmission machine

The Periodic Transmission machine shall implement the function specified in Figure 43–11 with its associated parameters (43.4.4 through 43.4.11).

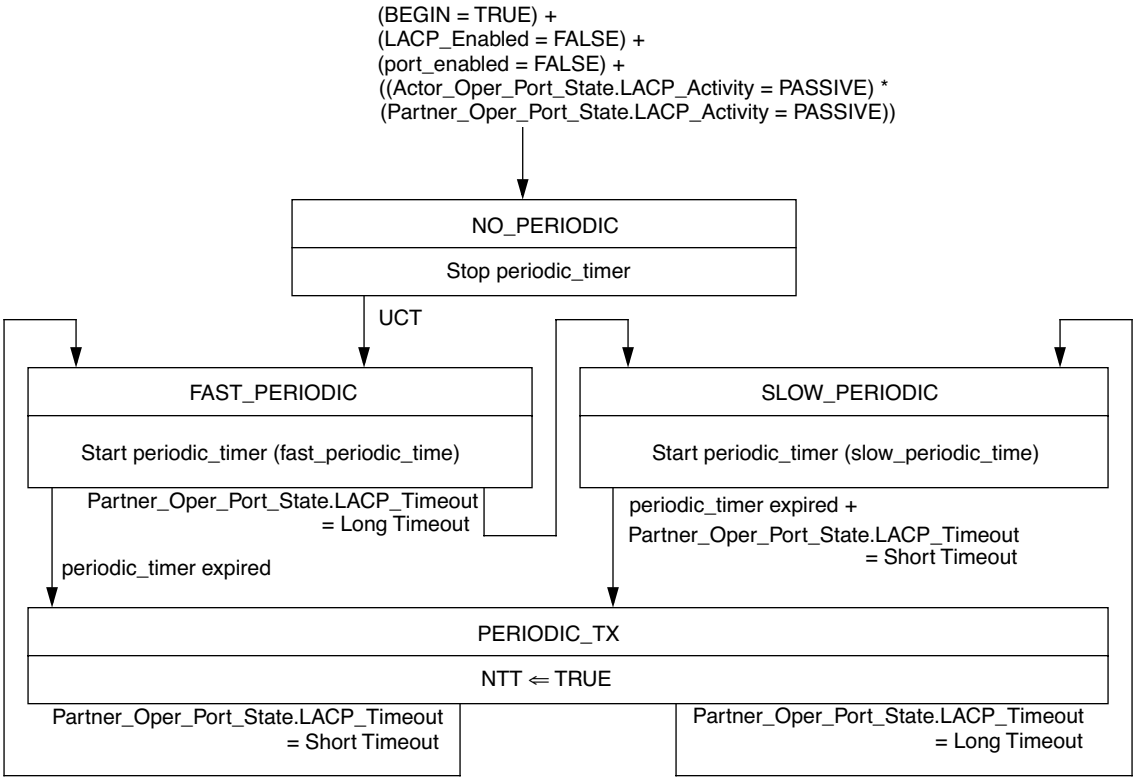


Figure 43–11—Periodic Transmission machine state diagram

The Periodic Transmission machine establishes the desire of the Actor and Partner to exchange periodic LACPDUs on the link in order to maintain an aggregation, and establishes how often those periodic transmissions should occur. Periodic transmissions will take place if either participant so wishes. Transmissions occur at a rate determined by the Partner; this rate is linked to the speed at which the Partner will time out received information.

The state machine has four states. They are as follows:

a) *NO_PERIODIC*. While in this state, periodic transmissions are disabled.
b) *FAST_PERIODIC*. While in this state, periodic transmissions are enabled at a fast transmission rate.
c) *SLOW_PERIODIC*. While in this state, periodic transmissions are enabled at a slow transmission rate.
d) *PERIODIC_TX*. This is a transitory state entered on periodic_timer expiry, that asserts NTT and then exits to FAST_PERIODIC or SLOW_PERIODIC depending upon the Partner's LACP_Timeout setting.

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The values of Partner_Oper_Port_State.LACP_Activity and Actor_Oper_Port_State.LACP_Activity determine whether periodic transmissions take place. If either or both parameters are set to Active LACP, then periodic transmissions occur; if both are set to Passive LACP, then periodic transmissions do not occur. Similarly, if either of the LACP_Enabled or port_enabled variables is set to FALSE, indicating that LACP has been disabled on the port or that the port is non-operational, then no periodic transmissions take place.

If periodic transmissions are enabled, the rate at which they take place is determined by the value of the Partner_Oper_Port_State.LACP_Timeout variable. If this variable is set to Short Timeout, then the value fast_periodic_time is used to determine the time interval between periodic transmissions. Otherwise, slow_periodic_time is used to determine the time interval.

43.4.14 Selection Logic

The Selection Logic selects a compatible Aggregator for a port, using the port's LAG ID. The Selection Logic may determine that the link should be operated as a standby link if there are constraints on the simultaneous attachment of ports that have selected the same Aggregator.

NOTE—There will never be more than one Aggregator with the same LAG ID, but there may be none. Normally, the latter will be a temporary state, caused by the fact that it takes a finite time for ports to be moved to the correct aggregators during reconfiguration.

The Mux machine controls the process of attaching the port to a selected Aggregator, after first detaching the port from any prior Aggregator if the port's LAG ID has changed.

NOTE—A port is always detached from its prior Aggregator when the LAG ID changes, even if the same Aggregator is selected later; to do otherwise would be to risk misdelivery of frames. Selection of a new Aggregator cannot take place until the port is detached from any prior Aggregator; other Aggregators may become free while the port is detaching, and other ports may attach to some of the available Aggregators during this time interval.

The operation of the Selection Logic is separated into the following two subclauses:

a) The requirements for the correct operation of the Selection Logic are defined in 43.4.14.1.
b) The recommended default operation of the Selection Logic is described in 43.4.14.2.

This separation reflects the fact that a wide choice of selection rules is possible within the proper operation of the protocol. An implementation that claims conformance to this standard may support selection rules other than the recommended default; however, any such rules shall meet the requirements stated in 43.4.14.1.

43.4.14.1 Selection Logic—Requirements

Aggregation is represented by a port selecting an appropriate Aggregator, and then attaching to that Aggregator. The following are required for correct operation of the selection and attachment logic:

a) The implementation shall support at least one Aggregator per System.
b) Each port shall be assigned an operational Key (43.3.5). Ports that can aggregate together are assigned the same operational Key as the other ports with which they can aggregate; ports that cannot aggregate with any other port are allocated unique operational Keys.
c) Each Aggregator shall be assigned an operational Key.
d) Each Aggregator shall be assigned an identifier that distinguishes it among the set of Aggregators in the System.
e) A port shall only select an Aggregator that has the same operational Key assignment as its own operational Key.

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f) Subject to the exception stated in item g), ports that are members of the same Link Aggregation Group (i.e., two or more ports that have the same Actor System ID, Actor Key, Partner System ID, and Partner Key, and that are not required to be Individual) shall select the same Aggregator.

g) Any pair of ports that are members of the same Link Aggregation Group, but are connected together by the same link, shall not select the same Aggregator (i.e., if a loopback condition exists between two ports, they shall not be aggregated together. For both ports, the Actor System ID is the same as the Partner System ID; also, for port A, the Partner's port identifier is port B, and for port B, the Partner's port identifier is port A).

NOTE—This exception condition prevents the formation of an aggregated link, comprising two ends of the same physical link aggregated together, in which all frames transmitted through an Aggregator are immediately received through the same Aggregator. However, it permits the aggregation of multiple links that are in loopback; for example, if port A is looped back to port C and port B is looped back to port D, then it is permissible for A and B (or A and D) to aggregate together, and for C and D (or B and C) to aggregate together.

h) Any port that is required to be Individual (i.e., the operational state for the Actor or the Partner indicates that the port is Individual) shall not select the same Aggregator as any other port.

i) Any port that is Aggregatable shall not select an Aggregator to which an Individual port is already attached.

j) If the above conditions result in a given port being unable to select an Aggregator, then that port shall not be attached to any Aggregator.

k) If there are further constraints on the attachment of ports that have selected an Aggregator, those ports may be selected as standby in accordance with the rules specified in 43.6.1. Selection or deselection of that Aggregator can cause the Selection Logic to re-evaluate the ports to be selected as standby.

l) The Selection Logic operates upon the operational information recorded by the Receive state machine, along with knowledge of the Actor's own operational configuration and state. The Selection Logic uses the LAG ID for the port, determined from these operational parameters, to locate the correct Aggregator to attach the port to.

m) The Selection Logic is invoked whenever a port is not attached to and has not selected an Aggregator, and executes continuously until it has determined the correct Aggregator for the port.

NOTE—The Selection Logic may take a significant time to complete its determination of the correct Aggregator, as a suitable Aggregator may not be immediately available, due to configuration restrictions or the time taken to re-allocate ports to other Aggregators.

n) Once the correct Aggregator has been determined, the variable Selected shall be set to SELECTED or to STANDBY (43.4.8, 43.6.1).

NOTE—If Selected is SELECTED, the Mux machine will start the process of attaching the port to the selected Aggregator. If Selected is STANDBY, the Mux machine holds the port in the WAITING state, ready to be attached to its Aggregator once its Selected state changes to SELECTED.

o) The Selection Logic is responsible for computing the value of the Ready variable from the values of the Ready_N variable(s) associated with the set of ports that are waiting to attach to the same Aggregator (see 43.4.8).

p) Where the selection of a new Aggregator by a port, as a result of changes to the selection parameters, results in other ports in the System being required to re-select their Aggregators in turn, this is achieved by setting Selected to UNSELECTED for those other ports that are required to re-select their Aggregators.

NOTE—The value of Selected is set to UNSELECTED by the Receive machine for the port when a change of LAG ID is detected.

q) A port shall not be enabled for use by the MAC Client until it has both selected and attached to an Aggregator.

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43.4.14.2 Selection Logic—Recommended default operation

The recommended default behavior provides an element of determinism (i.e., history independence) in the assignment of ports to Aggregators. It also has the characteristic that no additional MAC addresses are needed, over and above those already assigned to the set of underlying MACs.

NOTE—This standard does not specify any alternative selection rules beyond the recommended set. A wide variety of selection rules are possible within the scope of the requirements stated in 43.4.14.1. In particular, it is possible within these requirements to support implementations that provide fewer Aggregators than ports, as well as implementations designed to minimize configuration changes at the expense of less deterministic behavior.

Each port has an Aggregator associated with it, (i.e., the number of Aggregators in the System equals the number of ports supported). Each port/Aggregator pair is assigned the same operational Key and port number. When there are multiple ports in an aggregation, the Aggregator that the set of ports selects is the Aggregator with the same port number as the lowest-numbered port in the aggregation. Note that this lowest numbered port may not be in a state that allows data transfer across the link; however, it has selected the Aggregator in question. This is illustrated in Figure 43–12.

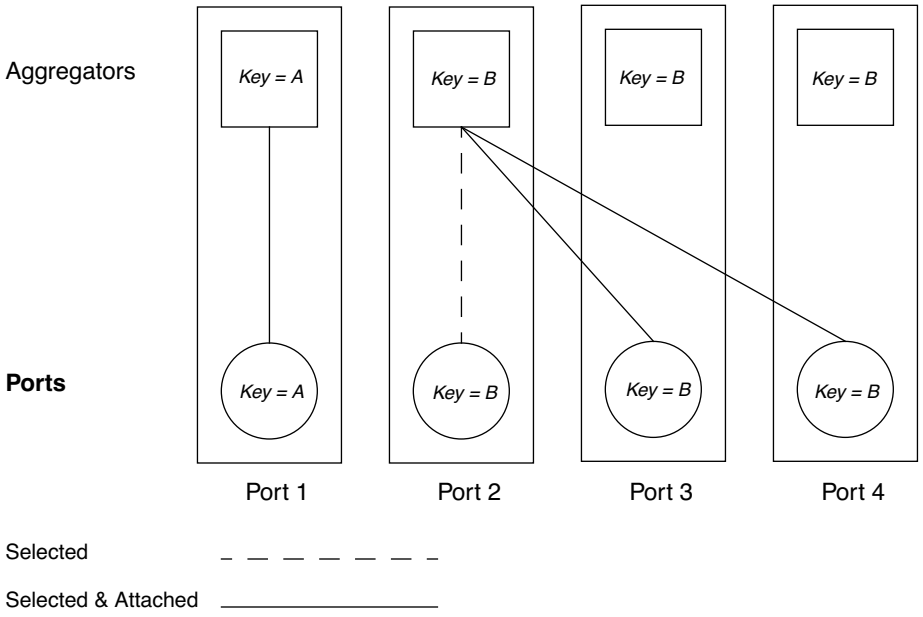


Figure 43–12—Selection of Aggregators

If the port is Individual, then the Aggregator selected is always the port's own Aggregator. Otherwise, an Aggregator is selected from the set of Aggregators corresponding to the set of ports that will form the aggregation. The Aggregator selected is the lowest numbered Aggregator with the same selection parameters as those of the port. These selection parameters are

a) The Actor's System ID
b) The Actor's operational Key
c) The Partner's System ID
d) The Partner's operational Key
e) The Individual_Aggregator state (which must be FALSE)

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43.4.15 Mux machine

The Mux machine shall implement the function specified in either of the Mux machine state diagrams, Figure 43–13 and Figure 43–14, with their associated parameters (43.4.4 through 43.4.11).

The state machine conventions in 21.5 assert that all in-state actions are instantaneous, are performed in sequence, and are performed prior to evaluating any exit conditions. While the Mux machine will operate correctly if all actions can be performed instantaneously, this will not be realistic in many implementations. Correct operation is maintained even if actions are not completed instantaneously, as long as each action completes prior to initiating the next sequential action, and all actions complete prior to evaluating any exit conditions.

The independent control state diagram (Figure 43–13) is suitable for use implementations in which it is possible to control enabling and disabling of frame collection from a port, and frame distribution to a port, independently. The coupled control state diagram (Figure 43–14) is suitable for use implementations where collecting and distributing cannot be controlled independently with respect to a port. It is recommended that the independent control state diagram be implemented in preference to the coupled control state diagram.

The value of the Selected variable may be changed by the following:

a) *The Receive machine*. The Receive machine can set Selected to UNSELECTED at any time if any of the following change: The Partner System ID, the Partner Priority, the Partner Key, the Partner_State.Aggregation, the Actor System ID, the Actor Priority, the Actor Key, or the Actor_State.Aggregation.
b) *The Selection Logic, in the process of selecting an Aggregator.* The Selection Logic will select an Aggregator when the Mux machine is in the DETACHED state and the value of the Selected variable is UNSELECTED.
c) *The Selection Logic, in the process of selecting or de-selecting standby links*. If the value of the Selected variable is SELECTED or STANDBY, the Selection Logic can change the value to STANDBY or SELECTED.

The Mux machine enters the WAITING state from the DETACHED state if the Selection Logic determines that Selected is either SELECTED or STANDBY. The WAITING state provides a holding state for the following two purposes:

d) If Selected is SELECTED, the wait_while_timer forces a delay to allow for the possibility that other ports may be reconfiguring at the same time. Once the wait_while_timer expires, and once the wait_while_timers of all other ports that are ready to attach to the same Aggregator have expired, the process of attaching the port to the Aggregator can proceed, and the state machine enters the ATTACHED state. During the waiting time, changes in selection parameters can occur that will result in a re-evaluation of Selected. If Selected becomes UNSELECTED, then the state machine re-enters the DETACHED state. If Selected becomes STANDBY, the operation is as described in item e).

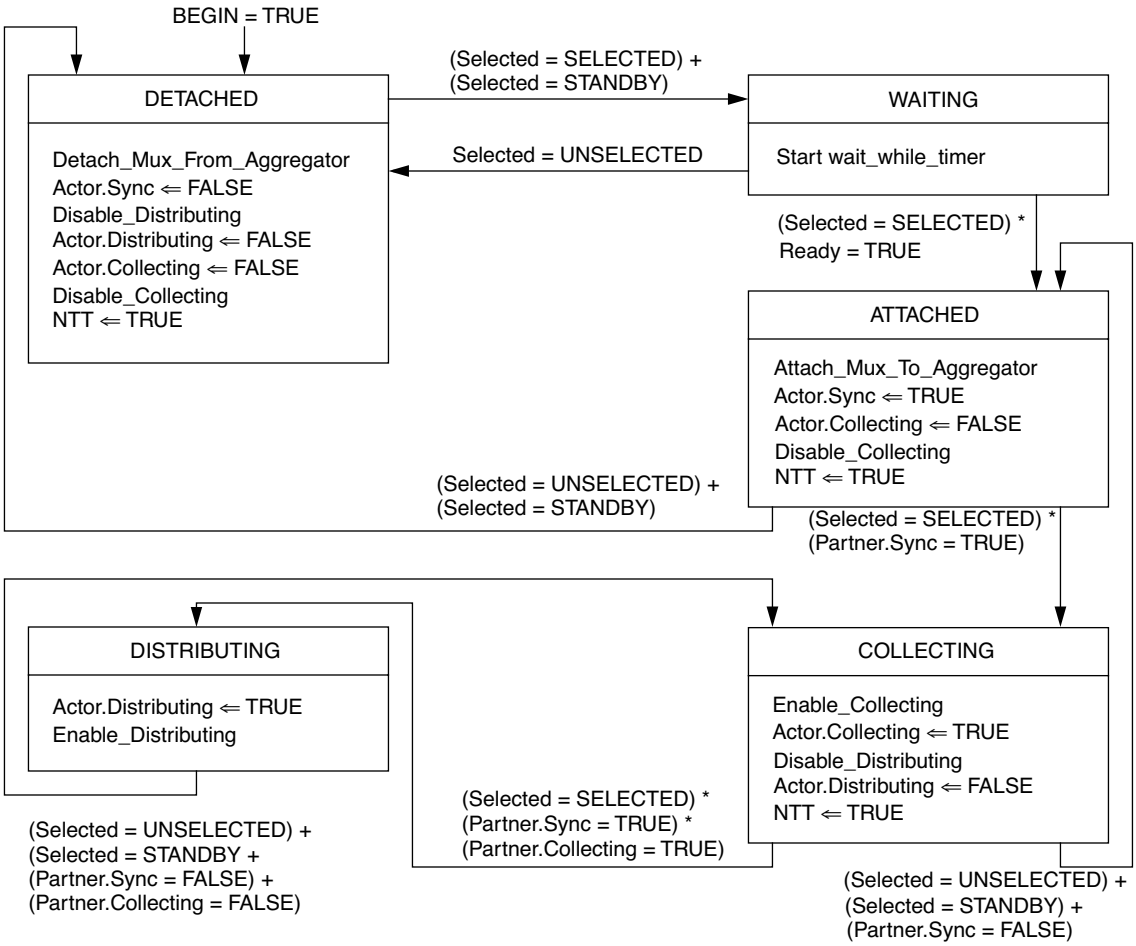
   NOTE—This waiting period reduces the disturbance that will be visible to higher layers; for example, on start-up events. However, the selection need not wait for the entire waiting period in cases where it is known that no other ports will attach; for example, where all other ports with the same operational Key are already attached to the Aggregator.

e) If Selected is STANDBY, the port is held in the WAITING state until such a time as the selection parameters change, resulting in a re-evaluation of the Selected variable. If Selected becomes UNSELECTED, the state machine re-enters the DETACHED state. If SELECTED becomes SELECTED, then the operation is as described in item d). The latter case allows a port to be brought into operation from STANDBY with minimum delay once Selected becomes SELECTED.

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The following abbreviations are used in this diagram:
Actor.Sync: Actor_Oper_Port_State.Synchronization
Actor.Collecting: Actor_Oper_Port_State.Collecting
Actor.Distributing: Actor_Oper_Port_State.Distributing
Partner.Sync: Partner_Oper_Port_State.Synchronization
Partner.Collecting: Partner_Oper_Port_State.Collecting

Figure 43–13—Mux machine state diagram (independent control)

On entry to the ATTACHED state, the Mux machine initiates the process of attaching the port to the selected Aggregator. Once the attachment process has completed, the value of Actor_Oper_Port_State.Synchronization is set to TRUE indicating that the Actor considers the port to be IN_SYNC, and Actor_Oper_Port_State.Collecting is set to FALSE. Collection of frames from the port is disabled. In the coupled control state machine, Distribution of frames to the port is also disabled, and Actor_Oper_Port_State.Distributing is set to FALSE.

A change in the Selected variable to UNSELECTED or to STANDBY causes the state machine to enter the DETACHED state. The process of detaching the port from the Aggregator is started. Once the detachment process is completed, Actor_Oper_Port_State.Synchronization is set to FALSE indicating that the Actor considers the port to be OUT_OF_SYNC, distribution of frames to the port is disabled, Actor_Oper_Port_State.Distributing and Actor_Oper_Port_State.Collecting are set to FALSE, and collection of frames from the port is disabled. The state machine remains in the DISABLED state until such time as the Selection logic is able to select an appropriate Aggregator.

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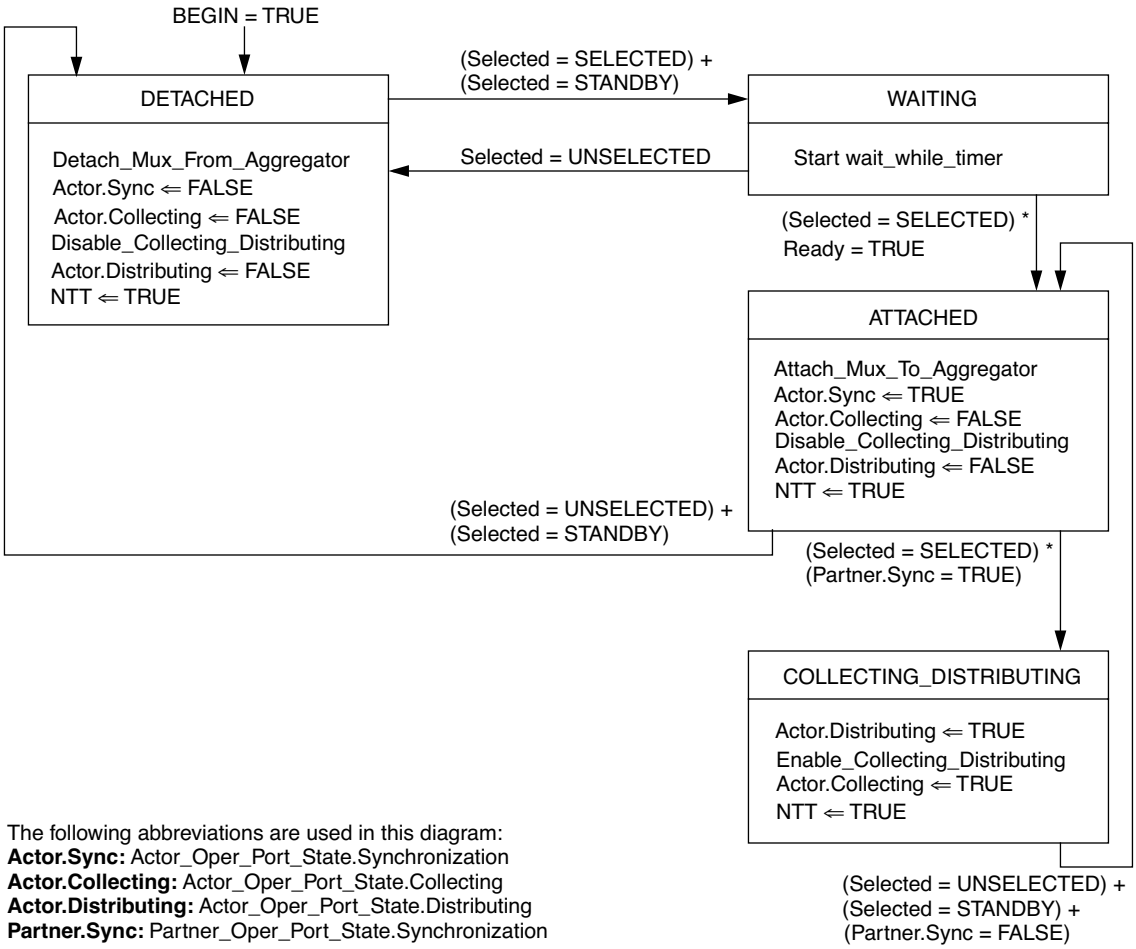


Figure 43–14—Mux machine state diagram (coupled control)

While in the ATTACHED state, a TRUE value for Partner_Oper_Port_State.Synchronization causes the state machine to transition to the COLLECTING state (independent control) or the COLLECTING_DISTRIBUTING state (coupled control).

In the COLLECTING state, collection of frames from the port is enabled, then Actor_Oper_Port_State.Collecting is set to TRUE, then distribution of frames to the port is disabled and Actor_Port_Oper_State.Distributing is set to FALSE. The state machine will return to the ATTACHED state if Selected changes to UNSELECTED or STANDBY, or if the Partner's synchronization state becomes FALSE. Once the Partner has signalled that collecting has been enabled (Partner_Oper_Port_State.Collecting is TRUE), the state machine transitions to the DISTRIBUTING state. The value of Actor_Oper_Port_State.Distributing is set to TRUE, and then distribution of frames to the port is enabled. From DISTRIBUTING, a return to the COLLECTING state occurs if the value of Selected becomes UNSELECTED or STANDBY, if the Partner's synchronization state becomes FALSE, or if the Partner signals that collection has been disabled (Partner_Oper_Port_State.Collecting is FALSE).

In the COLLECTING_DISTRIBUTING state, the value of Actor_Oper_Port_State.Distributing is set to TRUE, distribution of frames to the port and collection of frames from the port are both enabled, and then Actor_Oper_Port_State.Collecting is set to TRUE. The state machine will return to the ATTACHED state if Selected changes to UNSELECTED or STANDBY, or if the Partner's synchronization state becomes FALSE.

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The sequence of operations and transitions defined for the COLLECTING and DISTRIBUTING states in the independent control version of this state machine ensures that frames are not distributed to a port until the Partner has enabled collection, and that distribution is stopped as soon as the Partner's state indicates that collection has been disabled. This sequence minimizes the possibility that frames will be misdelivered during the process of bringing the port into operation or taking the port out of operation. In the coupled control version of the state machine, the COLLECTING and DISTRIBUTING states merge together to form the combined state, COLLECTING_DISTRIBUTING. As independent control is not possible, the coupled control state machine does not wait for the Partner to signal that collection has started before enabling both collection and distribution.

The NTT variable is set to TRUE in the DETACHED, ATTACHED, COLLECTING, and COLLECTING_DISTRIBUTING states in order to ensure that the Partner is made aware of the changes in the Actor's state variables that are caused by the operations performed in those states.

43.4.16 Transmit machine

When the Transmit machine creates a LACPDU for transmission, it shall fill in the following fields with the corresponding operational values for this port:

a) Actor_Port and Actor_Port_Priority
b) Actor_System and Actor_System_Priority
c) Actor_Key
d) Actor_State
e) Partner_Port and Partner_Port_Priority
f) Partner_System and Partner_System_Priority
g) Partner_Key
h) Partner_State
i) CollectorMaxDelay

When the Periodic machine is in the NO_PERIODIC state, the Transmit machine shall

— Not transmit any LACPDUs, and
— Set the value of NTT to FALSE.

When the LACP_Enabled variable is TRUE and the NTT (43.4.7) variable is TRUE, the Transmit machine shall ensure that a properly formatted LACPDU (43.4.2) is transmitted (i.e., issue a CtrlMuxN:MA_DATA.Request(LACPDU) service primitive), subject to the restriction that no more than three LACPDUs may be transmitted in any Fast_Periodic_Time interval. If NTT is set to TRUE when this limit is in force, the transmission shall be delayed until such a time as the restriction is no longer in force. The NTT variable shall be set to FALSE when the Transmit machine has transmitted a LACPDU.

If the transmission of a LACPDU is delayed due to the above restriction, the information sent in the LACPDU corresponds to the operational values for the port at the time of transmission, not at the time when NTT was first set to TRUE. In other words, the LACPDU transmission model is based upon the transmission of state information that is current at the time an opportunity to transmit occurs, as opposed to queuing messages for transmission.

When the LACP_Enabled variable is FALSE, the Transmit machine shall not transmit any LACPDUs and shall set the value of NTT to FALSE.

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43.4.17 Churn Detection machines

If implemented, the Churn Detection machines shall implement the functions specified in Figure 43–15 and Figure 43–16 with their associated parameters (43.4.4 through 43.4.11). Implementation of the Churn Detection machines is mandatory if the associated management functionality (the Aggregation Port Debug Information package) is implemented; otherwise, implementation of the Churn Detection machines is optional.

The Churn Detection machines detect the situation where a port is operable, but the Actor and Partner have not attached the link to an Aggregator and brought the link into operation within a bounded time period. Under normal operation of the LACP, agreement between Actor and Partner should be reached very rapidly. Continued failure to reach agreement can be symptomatic of device failure, of the presence of non-standard devices, or of misconfiguration; it can also be the result of normal operation in cases where either or both Systems are restricted in their ability to aggregate. Detection of this condition is signalled by the Churn Detection machines to management in order to prompt administrative action to further diagnose and correct the fault.

NOTE—One of the classes of problems that will be detected by this machine is the one where the implementation has been designed to support a limited number of Aggregators (fewer than the number of ports—see 43.6.4.2) and the physical topology is such that one or more ports end up with no Aggregator to attach to. This may be the result of a wiring error or an error in the allocation of operational Key values to the ports and Aggregators. Alternatively, failure of a link to aggregate may be the result of a link being placed in standby mode by a System that has hardware limitations placed on its aggregation ability, leading it to make use of the techniques described in 43.6 to find the ideal configuration. Given that the time taken by an aggregation-constrained System to stabilize its configuration may be relatively large, the churn detection timers allow 60 seconds to elapse before a Churn condition is signalled.

The symptoms that the Actor Churn Detection state machine detects is that the Actor's Mux has determined that it is OUT_OF_SYNC, and that condition has not resolved itself within a period of time equal to Short_Timeout_Time (43.4.4). Under normal conditions, this is ample time for convergence to take place. Similarly, the Partner Churn Detection state machine detects a failure of the Partner's Mux to synchronize.

The Actor Churn Detection state machine is depicted in Figure 43–15. The Partner Churn Detection state machine is depicted in Figure 43–16.

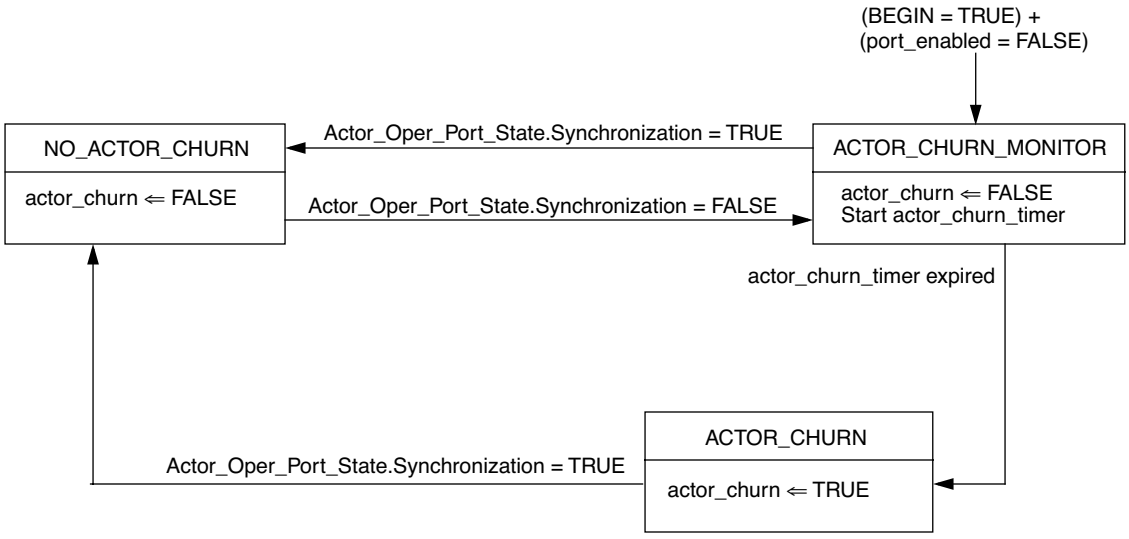


Figure 43–15—Actor Churn Detection machine state diagram

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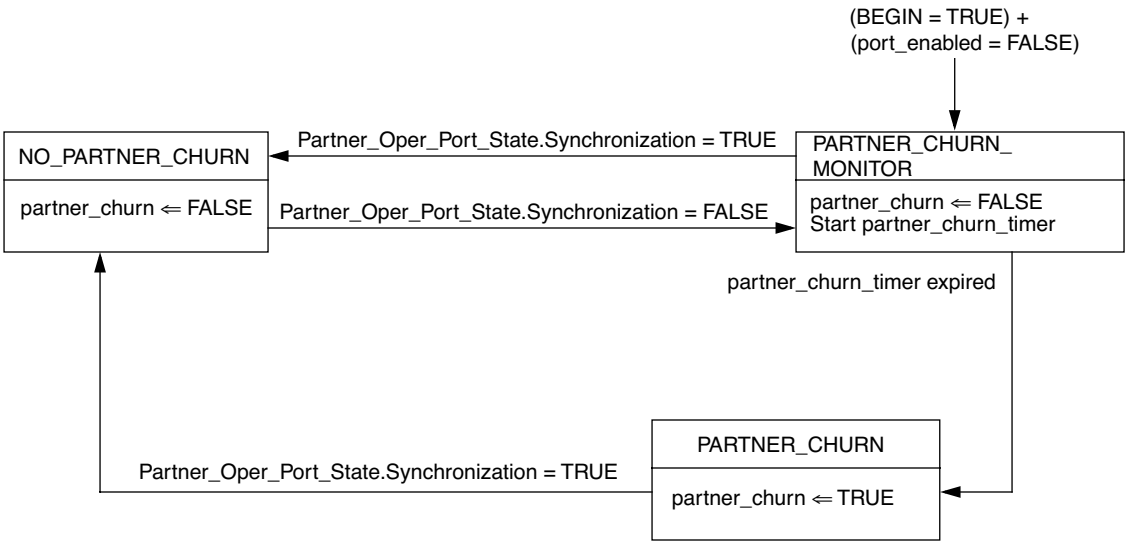


Figure 43–16—Partner Churn Detection machine state diagram

43.5 Marker protocol

43.5.1 Introduction

The Marker protocol allows the distribution function of an Actor's Link Aggregation sublayer to request the transmission of a Marker PDU on a given link. The Marker PDU is received by the Partner's collection function and a Marker Response PDU is returned on the same link to the initiating Actor's distribution function. Marker and Marker Response PDUs are treated by the underlying MACs at each end of the link as normal MAC Client PDUs; i.e., there is no prioritization or special treatment of Marker or Marker Response PDUs relative to other frames. Marker/Marker Response PDUs are subject to the operation of flow control, where supported on the link. Hence, if the distribution function requests transmission of a Marker PDU on a given link and does not transmit any further MAC Client PDUs that relate to a given set of conversations until the corresponding Marker Response PDU is received from that link, then it can be certain that there are no MAC Client PDUs related to those conversations still to be received by the Partner's collection function. The use of the Marker protocol can therefore allow the Distribution function a means of determining the point at which a given set of conversations can safely be reallocated from one link to another without the danger of causing frames in those conversations to be mis-ordered at the collector.

NOTE—The use of the Marker protocol is further discussed in Annex 43A.

The operation of the Marker protocol is unaffected by any changes in the Collecting and Distributing states associated with the port. Therefore, Marker and Marker Response PDUs can be sent on a port whose distribution function is disabled; similarly, such PDUs can be received and passed to the relevant Aggregator's collection or distribution function on a port whose collection function is disabled.

The use of the Marker protocol is optional; however, the ability to respond to Marker PDUs, as defined for the operation of the Marker Responder (see 43.5.4.1 and 43.5.4.2), is mandatory. Some distribution algorithms may not require the use of a marker; other mechanisms (such as timeouts) may be used as an alternative. As the specification of distribution algorithms is outside the scope of this standard, no attempt is made to specify how, when, or if the Marker protocol is used. (See Annex 43A for an informative discussion of distribution algorithms.).

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The Marker protocol does not provide a guarantee of a response from the Partner; no provision is made for the consequences of frame loss or for the failure of the Partner System to respond correctly. Implementations that make use of this protocol must therefore make their own provision for handling such cases.

43.5.2 Sequence of operations

Figure 43–17 illustrates the sequence of marker operations between an initiating and responding System. Time is assumed to flow from the top of the diagram to the bottom.

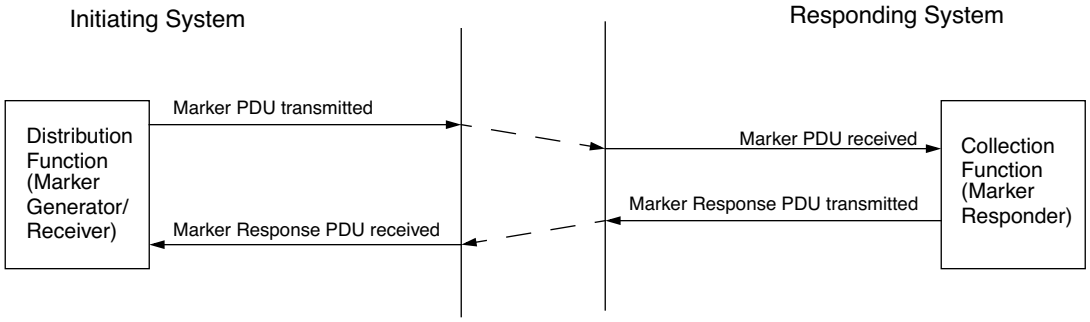


Figure 43–17—Marker protocol time sequence diagram

43.5.3 Marker and Marker Response PDU structure and encoding

43.5.3.1 Transmission and representation of octets

All Marker and Marker Response PDUs comprise an integral number of octets. The bits in each octet are numbered from 0 to 7, where 0 is the low-order bit. When consecutive octets are used to represent a numerical value, the most significant octet is transmitted first, followed by successively less significant octets.

When the encoding of (an element of) a Marker or Marker Response PDU is depicted in a diagram, then

a) Octets are transmitted from top to bottom.
b) Within an octet, bits are shown with bit 0 to the left and bit 7 to the right, and are transmitted from left to right.
c) Numerical values are encoded as binary numbers.

43.5.3.2 Marker and Marker Response PDU structure

Marker PDUs and Marker Response PDUs are basic IEEE 802.3 frames; they shall not be tagged (see Clause 3). The Marker PDU and Marker Response PDU structure shall be as shown in Figure 43–18 and as further described in the following field definitions:

a) *Destination Address*. The DA in all Marker and Marker Response PDUs is the Slow_Protocols_Multicast address. Its use and encoding are specified in Annex 43B.
b) *Source Address*. The SA in Marker and Marker Response PDUs is the individual MAC address associated with the port from which the PDU is transmitted.
c) *Length/Type*. Marker and Marker Response PDUs are always Type encoded, and carry the Slow Protocol type field. The use and encoding of this type field is specified in Annex 43B.
d) *Subtype*. The Subtype field identifies the specific Slow Protocol being encapsulated. Both Marker and Marker Response PDUs carry the Marker_subtype value 0x02.

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e) *Version number*. This identifies the Marker protocol version; implementations conformant to this version of the standard carry the value 0x01.

f) *TLV_type = Marker Information/Marker Response Information*. This indicates the nature of the information carried in this TLV-tuple. Marker Information is encoded as the integer value 0x01; Marker Response Information is encoded as the integer value 0x02.

g) *Marker_Information_Length/Marker_Response_Information_Length*. This field indicates the length (in octets) of this TLV-tuple. Both Marker and Marker Response information use a length value of 16 (0x10).

h) *Requester_Port*. The port number assigned to the port by the Requester (the System sending the initial Marker PDU), encoded as an unsigned integer.

Marker PDU	Octets	Marker Response PDU
Destination Address	6	Destination Address
Source Address	6	Source Address
Length/Type	2	Length/Type
Subtype = Marker	1	Subtype = Marker
Version Number	1	Version Number
TLV_type = Marker Information	1	TLV_type = Marker Response Information
Marker_Information_Length= 16	1	Marker_Response_Information_Length = 16
Requester_Port	2	Requester_Port
Requester_System	6	Requester_System
Requester_Transaction_ID	4	Requester_Transaction_ID
Pad = 0	2	Pad = 0
TLV_type = Terminator	1	TLV_type = Terminator
Terminator_Length = 0	1	Terminator_Length = 0
Reserved	90	Reserved
FCS	4	FCS

Figure 43–18—Marker PDU and Marker Response PDU structure

i) *Requester_System*. The Requester's System ID, encoded as a MAC address.

j) *Requester_Transaction_ID*. The transaction ID allocated to this request by the requester, encoded as an integer.

k) *Pad*. This field is used to align TLV-tuples on 16-byte memory boundaries. It is transmitted as zeroes in Marker PDUs; in Marker Response PDUs, this field may be transmitted as zeroes, or with the contents of this field from the Marker PDU triggering the response. The field is ignored on receipt in all cases.

NOTE—The difference in handling of the Pad field in Marker Response PDUs allows an implementation to reflect the contents of the received Marker PDU in its response, without enforcing the requirement to transmit the field as zeroes.

l) *TLV_type = Terminator*. This field indicates the nature of the information carried in this TLV-tuple. Terminator (end of message) information carries the integer value 0x00.

m) *Terminator_Length*. This field indicates the length (in octets) of this TLV-tuple. Terminator information uses a length value of 0 (0x00).

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n) *Reserved*. These 90 octets are reserved for use in future extensions to the protocol. It is transmitted as zeroes in Marker PDUs; in Marker Response PDUs, this field may be either transmitted as zeroes, or with the contents of this field from the Marker PDU triggering the response. The field is ignored on receipt in all cases.

NOTE—These trailing reserved octets are included in all Marker and Marker Response PDUs in order to force a fixed PDU size, regardless of the version of the protocol. Hence, a Version 1 implementation is guaranteed to be able to receive version N PDUs successfully, although version N PDUs may contain additional information that cannot be interpreted (and will be ignored) by the Version 1 implementation. A crucial factor in ensuring backwards compatibility is that any future version of the protocol is required not to re-define the structure or semantics of information defined for the previous version; it may only add new information elements to the previous set. Hence, in a version N PDU, a Version 1 implementation can expect to find the Version 1 information in exactly the same places as in a Version 1 PDU, and can expect to interpret that information as defined for Version 1.

o) *FCS*. This field is the Frame Check Sequence, typically generated by the underlying MAC.

43.5.4 Protocol definition

43.5.4.1 Operation of the marker protocol

Marker PDUs may be generated by the Frame Distribution function to provide a sequence marker in the stream of frames constituting a conversation or set of conversations. Received Marker PDUs are delivered to the Marker Responder within the Frame Collection function of the Partner System.

On receipt of a valid Marker PDU, the Frame Collection function issues a Marker Response PDU, in the format specified in Figure 43–18, to the same port from which the Marker PDU was received. The **Requester_Port, Requester_System,** and **Requester_Transaction_ID** parameter in the Marker Response PDU carry the same values as those received in the corresponding Marker PDU.

Received Marker Response PDUs are passed to the Marker Receiver within the Frame Distribution function. Implementation of the Marker Generator and Receiver is optional.

The Marker Generator, if implemented, shall comply with the frame rate limitation constraint for Slow Protocols, as specified in Annex 43B.3. A Marker Responder may (but is not required to) control its Marker Response transmissions to conform to this Slow Protocols timing constraint when faced with Marker messages not in compliance with this constraint (i.e., to send fewer Marker Response PDUs than Marker PDUs received). If the Marker Responder is controlling its responses in this manner, Marker Response PDUs corresponding to Marker PDUs received in excess of the Slow Protocols timing constraint shall not be sent.

NOTE—It is important that Marker Response PDUs not be queued indefinitely, and sent long after the corresponding Marker PDU that triggered the response.

Frames generated by the Marker Responder do not count towards the rate limitation constraint for Slow Protocols, as specified in Annex 43B.3.

43.5.4.2 Marker Responder state diagram

The Marker Responder shall implement the function specified in Figure 43–19, with its associated parameters (43.5.4.2.1 through 43.5.4.2.3).

43.5.4.2.1 Constants

Slow_Protocols_Multicast
The value of the Slow Protocols reserved multicast address. (See Table 43B–1.)

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43.5.4.2.2 Variables

DA
SA
m_sdu
service_class
status
: The parameters of the MA_DATA.request and MA_DATA.indication primitives, as defined in Clause 2.

43.5.4.2.3 Messages

AggMuxN:MA_DATA.request
: The service primitive used to transmit a frame with the specified parameters.

AggMuxN:MA_DATA.indication
: The service primitive used to pass a received frame to a client with the specified parameters.

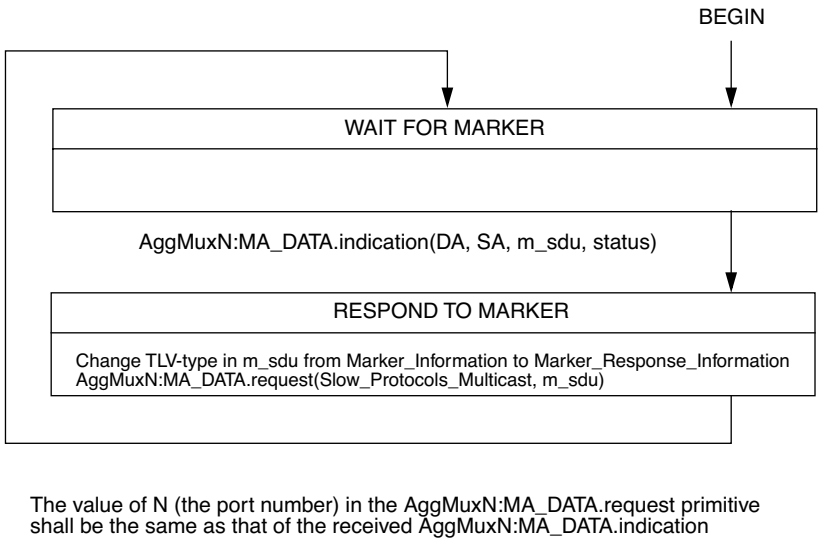


Figure 43–19—Marker Responder state diagram

Upon receipt of an AggMuxN:MA_DATA.indication primitive, the Marker Responder shall not validate the Version Number, Pad, or Reserved fields in the contained Marker Request PDU. The same actions are taken regardless of the values received in these fields. A Marker Responder may validate the Marker_Information_Length field. These behaviors, together with the constraint on future protocol enhancements discussed in the Note in 43.5.3.2, allow Version 1 devices to be compatible with future revisions of the protocol.

43.6 Configuration capabilities and restrictions

43.6.1 Use of system and port priorities

The formulation chosen for the Link Aggregation Group identifier (43.3.6) has the consequence that it is not possible to represent two or more Link Aggregation Groups, comprising aggregatable links, that share the same combination of {SK, TL}. Hence, placing configuration restrictions on the size of an aggregation (e.g.,

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for a Key Group containing 6 members, restricting the size of any aggregation to 4 members or fewer) is only possible if it is also acceptable that only one Link Aggregation Group can be constructed from that Key Group for a given {SK, TL}. In practice, this restriction can be somewhat alleviated by subdividing Key Groups and allocating different operational Keys to each subdivision; however, this is, in general, only useful if the form of the size restriction is closely bound to physical subdivisions in the implementation (e.g., it might be possible to aggregate only those links that are on the same interface card).

In Systems that have limited aggregation capability of this form, the following algorithm shall be used to determine the subset of ports that will be aggregated together:

a) The System Aggregation Priority of each System is an eight octet binary number, formed by using the Actor_System_Priority as the two most significant octets and the Actor's System ID as the least significant six octets. For a given Actor and Partner, the System with the numerically lower value of System Aggregation Priority has the higher priority.

b) The Port Aggregation Priority of each port is a four octet binary number, formed by using the Actor_Port_Priority as the two most significant octets and the port number as the two least significant octets. For any given set of ports, the port with the numerically lower value of Port Aggregation Priority has the higher priority.

c) Ports shall be selected for aggregation by each System based upon the Port Aggregation Priority assigned by the System with the higher System Aggregation Priority, starting with the highest priority port of the System with the higher priority, and working downward through the ordered list of Port Aggregation Priority values for the N ports, applying the particular constraints imposed on the System concerned.

d) For each link that a given System cannot include in the aggregation, the Selection Logic identifies the Selection state of the corresponding port as STANDBY, preventing the link from becoming active. The synchronization state signalled in transmitted LACPDUs for such links will be OUT_OF_SYNC.

e) The selection algorithm is reapplied upon changes in the membership of the Link Aggregation Group (for example, if a link fails, or if a new link joins the group) and any consequent changes to the set of active links are made accordingly.

A port that is selected as standby as a result of limitations on aggregation capability can be viewed as providing a "hot standby" facility, as it will be able to take part in the aggregation upon failure of one of the active links in the aggregation. The ability to hold links in a standby mode in this way provides the possibility of using LACP even where the System is incapable of supporting distribution and collection with more than one port. Parallel links could be automatically configured as standby links, and deployed to mask link failures without any disruption to higher layer protocols.

43.6.2 Dynamic allocation of operational Keys

In some circumstances, the use of System and port priorities may prove to be insufficient to generate the optimum aggregation among the set of links connecting a pair of Systems. A System may have a limited aggregation capability that cannot be simply expressed as a limit on the total number of links in the aggregation. The full description of its restrictions may be that it can only aggregate together particular subsets of links, and the sizes of the subsets need not all be the same.

NOTE—An example would be an implementation organized such that, for a set of four links A through D, it would be possible to operate with {A+B+C+D} as a single aggregation, or operate with {A+B} and {C+D} as two separate aggregations, or operate as four individual links; however, all other aggregation possibilities (such as {A+C} and {B+D}) would not be achievable by the implementation.

In such circumstances, it is permissible for the System with the higher System Aggregation Priority (i.e., the numerically lower value) to dynamically modify the operational Key value associated with one or more of

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the ports; the System with the lower priority shall not attempt to modify operational Key values for this purpose. Operational Key changes made by the higher priority System should be consistent with maintaining its highest priority port in the aggregate as an active link (i.e., in the IN_SYNC state). Successive operational Key changes, if they occur, should progressively reduce the number of ports in the aggregation. The original operational Key value should be maintained for the highest priority port thought to be aggregatable.

NOTE—Restricting operational Key changes in the manner described prevents the case where both Partner Systems involved have limited capability and both attempt to make operational Key changes; this could be a non-converging process, as a change by one participant can cause the other participant to make a change, which in turn causes the first participant to make a change—and so on, ad infinitum.

This approach effectively gives the higher priority System permission to search the set of possible configurations, in order to find the best combination of links given its own and its Partner's configuration constraints. The reaction of the Partner System to these changes can be determined by observing the changes in the synchronization state of each link. A System performing operational Key changes should allow at least 4 seconds for the Partner System to change an OUT_OF_SYNC state to an IN_SYNC state.

In the course of normal operation a port can dynamically change its operating characteristics (e.g., data rate, full or half duplex operation). It is permissible (and appropriate) for the operational Key value associated with such a port to change with the corresponding changes in the operating characteristics of the link, so that the operational Key value always correctly reflects the aggregation capability of the link. Operational Key changes that reflect such dynamic changes in the operating characteristics of a link may be made by either System without restriction.

43.6.3 Link Aggregation on shared-medium links

The Link Aggregation Control Protocol cannot detect the presence of multiple Aggregation-aware devices on the same link. Hence, shared-medium links shall be treated as Individual, with transmission/reception of LACPDUs disabled on such ports.

43.6.4 Selection Logic variants

Two variants of the Selection Logic rules are described as follows:

a) The first accommodates implementations that may wish to operate in a manner that minimizes disturbance of existing aggregates, at the expense of the deterministic characteristics of the logic described in 43.4.14.2.
b) The second accommodates implementations that may wish to limit the number of Aggregators that are available for use to fewer than the number of ports supported.

43.6.4.1 Reduced reconfiguration

By removing the constraint that the Aggregator chosen is always the lowest numbered Aggregator associated with the set of ports in an aggregation, an implementation can minimize the degree to which changes in the membership of a given aggregation result in changes of connectivity at higher layers. As there would still be the same number of Aggregators and ports with a given operational Key value, any port will still always be able to find an appropriate Aggregator to attach to, however the configuration achieved over time (i.e., after a series of link disconnections, reconnections, or reconfigurations) with this relaxed set of rules would not necessarily be the same as the configuration achieved if all Systems involved were reset, given the rules stated in 43.4.15.

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43.6.4.2 Limited Aggregator availability

By removing the constraint that there are always as many Aggregators as ports, an implementation can limit the number of MAC Client interfaces available to higher layers while maintaining the ability for each Aggregator to serve multiple ports. This has the same effect as removing the assumption that Aggregators and their associated ports have the same operational Key value; Aggregators can be effectively disabled (and therefore ignored) by configuring their Keys to be different from any operational Key value allocated to any of the ports.

In this scenario, any port(s) that cannot find a suitable Aggregator to attach to will simply wait in the DETACHED state until an Aggregator becomes available, with a synchronization state of OUT_OF_SYNC.

43.7 Protocol Implementation Conformance Statement (PICS) proforma for Clause 43, Aggregation of Multiple Link Segments[13]

43.7.1 Introduction

The supplier of an implementation that is claimed to conform to Clause 43, Link Aggregation, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

43.7.2 Identification

43.7.2.1 Implementation identification

Supplier (Note 1)	
Contact point for queries about the PICS (Note 1)	
Implementation Name(s) and Version(s) (Notes 1 and 3)	
Other information necessary for full identification—e.g., name(s) and version(s) of machines and/or operating system names (Note 2)	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

[13] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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43.7.2.2 Protocol summary

Identification of protocol specification	IEEE Std 802.3-2002, Clause 43, Link Aggregation.
Identification of amendments and corrigenda to the PICS proforma which have been completed as part of the PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21: the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002, Clause 43, Link Aggregation.)	

Date of Statement	

43.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*MG	Marker Generator/Receiver	43.2.5		O	Yes [ ] No [ ]
*AM	Aggregation Port Debug Information package support	30.7		O	Yes [ ] No [ ]
*CM	Churn Detection machine	43.4.17	Required if Aggregation Port Debug Information package supported	AM: M !AM: O	N/A [ ] M:Yes [ ] Yes [ ] No [ ]

43.7.4 Frame Collector

Item	Feature	Subclause	Value/Comment	Status	Support
FC1	Frame Collector function	43.2.3	As specified in the state diagram shown in Figure 43–3 and associated definitions in 43.2.3.1	M	Yes [ ]
FC2	Frame Collector function—CollectorMaxDelay	43.2.3.1.4	Deliver or discard frames within CollectorMaxDelay	M	Yes [ ]

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43.7.5 Frame Distributor

Item	Feature	Subclause	Value/Comment	Status	Support
	Distribution algorithm ensures the following, when frames received by Frame Collector:	43.2.4			
FD1	Frame mis-ordering		None	M	Yes [ ]
FD2	Frame duplication		None	M	Yes [ ]
FD3	Frame Distributor function	43.2.4	Function as specified in the state diagram shown in Figure 43–4 and associated definitions in 43.2.4.1	M	Yes [ ]

43.7.6 Marker protocol

Item	Feature	Subclause	Value/Comment	Status	Support
MGR1	Marker Generator/Receiver	43.2.5		MG:M	N/A [ ] M:Yes [ ]
MGR2	Marker Responder	43.2.6	Function specified in 43.5.4.2	M	Yes [ ]

43.7.7 Aggregator Parser/Multiplexer

Item	Feature	Subclause	Value/Comment	Status	Support
APM1	Aggregator Multiplexer	43.2.7	Transparent pass-through of frames	M	Yes [ ]
APM2	Aggregator Multiplexer	43.2.7	Discard of TX frames when port not Distributing	M	Yes [ ]
APM3	Aggregator Parser	43.2.7	Function specified by state diagram shown in Figure 43–5 and associated definitions in 43.2.7.1.	M	Yes [ ]
APM4	Aggregator Parser	43.2.7	Discard of RX frames when port not Collecting	M	Yes [ ]

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43.7.8 Control Parser/Multiplexer

Item	Feature	Subclause	Value/Comment	Status	Support
CPM1	Control Multiplexer	43.2.9	Transparent pass-through of frames	M	Yes [ ]
CPM2	Control Parser	43.2.9	Function specified by state diagram shown in Figure 43–6 and associated definitions in 43.2.9.1.	M	Yes [ ]

43.7.9 System identification

Item	Feature	Subclause	Value/Comment	Status	Support
SID1	Globally unique identifier	43.3.2	Globally administered individual MAC address plus System Priority	M	Yes [ ]
SID2	MAC address chosen	43.3.2	MAC address associated with one of the ports	O	Yes [ ] No [ ]

43.7.10 Aggregator identification

Item	Feature	Subclause	Value/Comment	Status	Support
AID1	Globally unique identifier	43.3.3	Globally administered individual MAC address	M	Yes [ ]
AID2	Integer identifier	43.3.3	Uniquely identifies the Aggregator within the System	M	Yes [ ]
*AID3	Unique identifier allocated	43.3.3	Unique identifier assigned to one of its bound ports	O	Yes [ ] No [ ]
AID4			Unique identifier not assigned to any other Aggregator	!AID3 :M	N/A [ ] M:Yes [ ]

43.7.11 Port identification

Item	Feature	Subclause	Value/Comment	Status	Support
PID1	Port identifiers	43.3.4	Unique within a System; port number 0 not used for any port	M	Yes [ ]

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43.7.12 Capability identification

Item	Feature	Subclause	Value/Comment	Status	Support
CID1	Administrative and operational Key values associated with each port	43.3.5		M	Yes [ ]
CID2	Administrative and operational Key values associated with each Aggregator	43.3.5		M	Yes [ ]

43.7.13 Link Aggregation Group identification

Item	Feature	Subclause	Value/Comment	Status	Support
LAG1	LAG ID component values	43.3.6.1	Actor's values non-zero. Partner's admin values only zero for Individual ports	M	Yes [ ]

43.7.14 Detaching a link from an Aggregator

Item	Feature	Subclause	Value/Comment	Status	Support
DLA1	Effect on conversation reallocated to a different link	43.3.13	Frame ordering preserved	M	Yes [ ]

43.7.15 LACPDU structure

Item	Feature	Subclause	Value/Comment	Status	Support
LPS1	LACPDU Frame format	43.4.2.2	Not Tagged	M	Yes [ ]
LPS2	LACPDU structure	43.4.2.2	As shown in Figure 43–7 and as described	M	Yes [ ]
LPS3	LACPDU structure	43.4.2	All Reserved octets ignored on receipt and transmitted as zero	M	Yes [ ]

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43.7.16 State machine variables

Item	Feature	Subclause	Value/Comment	Status	Support
SMV1	Partner_Admin_Port_State	43.4.7	Collecting set to the same value as Synchronization	M	Yes [ ]
SMV2	LACP_Enabled	43.4.8	FALSE for half duplex ports, otherwise TRUE	M	Yes [ ]

43.7.17 Receive machine

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	Receive machine	43.4.12	As defined in Figure 43–10 and associated parameters	M	Yes [ ]
RM2	Validation of LACPDUs		No validation of Version Number, TLV_type, or Reserved fields	M	Yes [ ]

43.7.18 Periodic Transmission machine

Item	Feature	Subclause	Value/Comment	Status	Support
PM1	Periodic Transmission machine	43.4.13	As defined in Figure 43–11 and associated parameters	M	Yes [ ]

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43.7.19 Selection Logic

Item	Feature	Subclause	Value/Comment	Status	Support
	Selection logic requirements	43.4.14.1			
SLM1	Aggregator support		At least one Aggregator per System	M	Yes [ ]
SLM2	Port Keys		Each port assigned an operational Key	M	Yes [ ]
SLM3	Aggregator Keys		Each Aggregator assigned an operational Key	M	Yes [ ]
SLM4	Aggregator Identifiers		Each Aggregator assigned an identifier	M	Yes [ ]
SLM5	Aggregator selection		If same Key assignment as port	M	Yes [ ]
SLM6	Ports that are members of the same Link Aggregation Group		Ports select same Aggregator	M	Yes [ ]
SLM7	Pair of ports connected in loopback		Not select same Aggregator as each other	M	Yes [ ]
SLM8	Port required to be Individual		Not select same Aggregator as any other port	M	Yes [ ]
SLM9	Port is Aggregatable		Not select same Aggregator as any Individual port	M	Yes [ ]
SLM10	Port unable to select an Aggregator		Port not attached to any Aggregator	M	Yes [ ]
SLM11	Further aggregation constraints		Ports may be selected as standby	O	Yes [ ] No [ ]
SLM12	Selected variable		Set to SELECTED or STANDBY once Aggregator is determined	M	Yes [ ]
SLM13	Port enabled		Only when selected and attached to an Aggregator	M	Yes [ ]
SLM14	Recommended default operation of Selection Logic	43.4.14.2	Meets requirements of 43.4.14.2	O	Yes [ ] No [ ]

43.7.20 Mux machine

Item	Feature	Subclause	Value/Comment	Status	Support
XM1	Mux machine	43.4.15	As defined in Figure 43–13 or Figure 43–14, and associated parameters	M	Yes [ ]

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43.7.21 Transmit machine

Item	Feature	Subclause	Value/Comment	Status	Support
	Transmitted in outgoing LACP-DUs	43.4.16			
TM1	Actor_Port and Actor_Port_Priority			M	Yes [ ]
TM2	Actor_System and Actor_System_Priority			M	Yes [ ]
TM3	Actor_Key			M	Yes [ ]
TM4	Actor_State			M	Yes [ ]
TM5	Partner_Port and Partner_Port_Priority			M	Yes [ ]
TM6	Partner_System and Partner_System_Priority			M	Yes [ ]
TM7	Partner_Key			M	Yes [ ]
TM8	Partner_State			M	Yes [ ]
TM9	CollectorMaxDelay			M	Yes [ ]
TM10	Action when Periodic machine is in the NO_PERIODIC state	43.4.16	Set NTT to FALSE, do not transmit	M	Yes [ ]
TM11	Action when LACP_Enabled is TRUE, NTT is TRUE, and not rate limited	43.4.16	Properly formatted LACPDU transmitted	M	Yes [ ]
TM12	Action when LACP_Enabled is TRUE and NTT is TRUE, when rate limit is in force	43.4.16	Transmission delayed until limit is no longer in force	M	Yes [ ]
TM13	Action when LACPDU has been transmitted	43.4.16	Set NTT to FALSE	M	Yes [ ]
TM14	Action when LACP_Enabled is FALSE	43.4.16	Set NTT to FALSE, do not transmit	M	Yes [ ]

43.7.22 Churn Detection machines

Item	Feature	Subclause	Value/Comment	Status	Support
CM1	Churn Detection machines	43.4.17	As defined in Figure 43–15 and Figure 43–16	CM:M	N/A [ ] Yes [ ]

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43.7.23 Marker protocol

Item	Feature	Subclause	Value/Comment	Status	Support
FP1	Respond to all received Marker PDUs	43.5.1	As specified by 43.5.4	M	Yes [ ]
FP2	Use of the Marker protocol	43.5.1	As specified by 43.5.4	O	Yes [ ] No [ ]
FP3	MARKER.request service primitives request rate	43.5.4.1	Maximum of five during any one-second period	MG:M	N/A [ ] Yes [ ]
FP4	Marker PDU Frame format	43.5.3.2	Not Tagged	MG:M	N/A [ ] Yes [ ]
FP5	Marker Response PDU Frame format	43.5.3.2	Not Tagged	M	Yes [ ]
FP6	Marker PDU structure	43.5.3.2	As shown in Figure 43–18 and as described	MG:M	N/A [ ] Yes [ ]
FP7	Marker Response PDU structure	43.5.3.2	As shown in Figure 43–18 and as described	M	Yes [ ]
FP8	Marker Responder State Diagram	43.5.4.2	As specified in Figure 43–19 and 43.5.4.2.1 through 43.5.4.2.3	M	Yes [ ]
FP9	Validation of Marker Request PDUs	43.5.4.2.3	Marker Responder shall not validate the Version Number, Pad, or Reserved fields	M	Yes [ ]

43.7.24 Configuration capabilities and restrictions

Item	Feature	Subclause	Value/Comment	Status	Support
CCR1	Algorithm used to determine subset of ports that will be aggregated in Systems that have limited aggregation capability	43.6.1	As specified in items a) to e) of 43.6.1	M	Yes[ ]
CCR2	Key value modification to generate optimum aggregation	43.6.2		O	Yes [ ] No [ ]
CCR3	Key value modification when System has higher System Aggregation Priority			CCR2:M	N/A [ ] M:Yes [ ]
CCR4	Key value modification when System has lower System Aggregation Priority			CCR2:X	N/A [ ] X:Yes [ ]

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43.7.25 Link Aggregation on shared-medium links

Item	Feature	Subclause	Value/Comment	Status	Support
LSM1	Shared-medium links—Configuration	43.6.3	Configured as Individual links	M	Yes [ ]
LSM2	Shared-medium links—Operation of LACP	43.6.3	LACP is disabled	M	Yes [ ]

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Annex 36A

(informative)

Jitter test patterns

This annex defines test patterns that allow 1000BASE-X PMDs to be tested for compliance while in a system environment. The patterns may be implemented at a bit, code-group, or frame level and may be used for transmitter testing. The receiver may not have the capability to accept these diagnostic sequences; however, system debug can be improved if a receiver is able to test for one or more of these patterns and report bit errors (e.g. 8B/10B decoder errors) back to the user.

36A.1 High-frequency test pattern

The intent of this test pattern is to test random jitter (RJ) at a BER of 10^{-12}, and also to test the asymmetry of transition times. This high-frequency test pattern generates a one, or light on, for a duration of 1 bit time, followed by a zero, or light off, for a duration of 1 bit time. This pattern repeats continuously for the duration of the test. For example: 10101010101010101010101010101010101010...

NOTE—This pattern can be generated by the repeated transmission of the D21.5 code-group. Disparity rules are followed.

36A.2 Low-frequency test pattern

The intent of this test pattern is to test low-frequency RJ and also to test PLL tracking error. This low frequency test pattern generates a one, or light on, for a duration of 5 bit times, followed by a zero, or light off, for a duration of 5 bit times. This pattern repeats continuously for the duration of the test. For example: 11111000001111100000111110000011111100000...

NOTE—This pattern can be generated by the repeated transmission of the K28.7 code-group. Disparity rules are followed.

36A.3 Mixed frequency test pattern

The intent of this test pattern is to test the combination of RJ and deterministic jitter (DJ). This mixed frequency test pattern generates a one, or light on, for a duration of 5 bit times, followed by a zero, or light off, for a duration of 1 bit times, followed by a one for 1 bit time followed by a zero for 1 bit time followed by a one for 2 bit times followed by a zero for 5 bit times followed by a one for 1 bit time followed by a zero for 1 bit time followed by a one for 1 bit time followed by a zero for 2 bit times. This pattern repeats continuously for the duration of the test. For example: 11111010110000010100111110101100000101100...

NOTE—This pattern can be generated by the repeated transmission of the K28.5 code-group. Disparity rules are followed.

36A.4 Long continuous random test pattern

The long continuous random test pattern is a random test pattern intended to provide broad spectral content and minimal peaking that can be used for the measurement of jitter at either a component or system level.

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NOTE—The derivation of this pattern may be found in *Fibre Channel Jitter Working Group Technical Report* [B36]. This technical report modified the original RPAT as defined by Fibre Channel so that it would maintain its intended qualities but fit into a Fibre Channel frame. This annex uses similar modifications to fit the same RPAT into an 802.3 frame.

The long continuous random test pattern consists of a continuous stream of identical packets, separated by a minimum IPG. Each packet is encapsulated within SPD and EPD delimiters as specified in Clause 36 in the ordinary way. The contents of each packet is composed of the following octet sequences, as observed at the GMII, before 8B/10B coding.

Each packet in the long continuous random test pattern consists of 8 octets of PREAMBLE/SFD, followed by 1512 data octets (126 repetitions of the 12-octet modified RPAT sequence), plus 4 CRC octets, followed by a minimum IPG of 12 octets of IDLE.

PREAMBLE/SFD:

55 55 55 55 55 55 55 D5

MODIFIED RPAT SEQUENCE (LOOP 126 TIMES)

BE D7 23 47 6B 8F B3 14 5E FB 35 59

CRC

94 D2 54 AC

IPG (TX_EN and TX_ER low)

00 00 00 00 00 00 00 00 00 00 00 00

END

36A.5 Short continuous random test pattern

The short continuous random test pattern is a random test pattern intended to provide broad spectral content and minimal peaking that can be used for the measurement of jitter at either a component or system level.

NOTE—The derivation of this pattern may be found in *Fibre Channel Jitter Working Group Technical Report* [B36]. This technical report modified the original RPAT as defined by Fibre Channel so that it would maintain its intended qualities but fit into a Fibre Channel frame. This annex uses similar modifications to fit the same RPAT into an 802.3 frame.

The short continuous random test pattern consists of a continuous stream of identical packets, separated by a minimum IPG. Each packet is encapsulated within SPD and EPD delimiters as specified in Clause 36 in the ordinary way. The contents of each packet is composed of the following octet sequences, as observed at the GMII, before 8B/10B coding.

Each packet in the short continuous random test pattern consists of 8 octets of PREAMBLE/SFD, followed by 348 data octets (29 repetitions of the 12-octet modified RPAT sequence), plus 4 CRC octets, followed by a minimum IPG of 12 octets of IDLE.

The format of this packet is such that the PCS will generate the following ordered sets for the IPG: /T/ /R/ /I1/ /I2/ /I2/ /I2/ /I2/

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PREAMBLE/SFD:

55 55 55 55 55 55 55 D5

MODIFIED RPAT SEQUENCE (LOOP 29 TIMES)

BE D7 23 47 6B 8F B3 14 5E FB 35 59

CRC

2F E0 AA EF

IPG (TX_EN and TX_ER low)

00 00 00 00 00 00 00 00 00 00 00 00

END

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Annex 36B

(informative)

8B/10B transmission code running disparity calculation examples

Detection of a invalid code-group in the 8B/10B transmission code does not necessarily indicate that the code-group in which the error was detected was the one in which the error occurred. Invalid code-groups may result from a prior error that altered the running disparity of the bit stream but that did not result in a detectable error at the code-group in which the error occurred. The examples shown in Tables 36B–1 and 36B–2 exhibit this behavior. The example shown in Table 36B–3 exhibits the case where a bit error in a received code-group is detected in that code-group, affects the next code group, and error propagation is halted upon detection of the running disparity error.

Table 36B–1—RD error detected two code-groups following error

Stream	Code-group			Code-group			Code-group		
	RD		RD		RD			RD	
Transmitted code-group	–	D21.1	–		D10.2	–		D23.5	+
Transmitted bit stream	–	101010 - 1001	–	010101	– 0101	–	111010	+ 1010	+
Received bit stream	–	101010 - 10**1**1[a]	+	010101	+ 0101	+	111010	+[b] 1010	+
Received code-group	–	D21.0	+		D10.2	+	invalid code-group[b]		+[c]

[a]Bit error introduced (1001 ⇒ 10**1**1)
[b]Nonzero disparity blocks must alternate in polarity (+ ⇒ –). In this case, RD does not alternate (+ ⇒ **+**), the received code group is not found in the Current RD+ column in either Table 36–1a or Table 36–2, and an invalid code-group is recognized.
[c]Running disparity is calculated on the received code-group regardless of the validity of the received code-group. Nonzero disparity blocks prevent the propagation of errors and normalize running disparity to the transmitted bit stream (i.e., equivalent to the received bit stream had an error not occurred).

Table 36B–2—RD error detected in next code-group following error

Stream	Code-group			Code-group			Code-group		
	RD		RD		RD			RD	
Transmitted code-group	–	D21.1	–		D23.4	–		D23.5	+
Transmitted bit stream	–	101010 – 1001	–	111010	+ 0010	–	111010	+ 1010	+
Received bit stream	–	101010 – 10**1**1[a]	+	111010	+[b] 0010	–	111010	+ 1010	+
Received code-group	–	D21.0	+	invalid code-group[b]		–		D23.5	+

[a]Bit error introduced (1001 ⇒ 10**1**1)
[b]Nonzero disparity blocks must alternate in polarity (+ ⇒ –).

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Table 36B–3—A single bit error affects two received code-groups

Stream	Code-group RD		Code-group RD		Code-group RD		Code-group RD	
Transmitted code-group	–	D3.6 (FCS3)	–	K29.7 (/T/)	–	K23.7 (/R/)	–	
Transmitted bit stream	–	110001 - 0110	–	101110 + 1000	–	111010 + 1000	–	
Received bit stream	–	110001 - 011**1**[a]	+[b]	101110 +[c] 1000	–	111010 + 1000	–	
Received code-group	–	invalid code-group[d]	+	invalid code-group[e]	–	K23.7 (/R/)	–	

[a]Bit error introduced (0110 ⇒ 011**1**).
[b]Nonzero disparity blocks must alternate in polarity (– ⇒ +). Received RD differs from transmitted RD.
[c]Nonzero disparity blocks must alternate in polarity (+ ⇒ –). Invalid code-group due to RD error since RD remains at +.
[d]Received code-group is not found in either Table 36–1a or Table 36–2.
[e]Nonzero disparity blocks prevent the propagation of errors and normalize running disparity to the transmitted bit stream (i.e. equivalent to the received bit stream had an error not occurred). All code-groups contained in PCS End_of_Packet delimiters (/T/R/R or /T/R/K28.5/) include nonzero disparity blocks.

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Annex 38A

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Fiber launch conditions

38A.1 Overfilled Launch

Overfilled Launch (OFL), as described in IEC 60793-1-4 [B24], is the standard launch used to define optical fiber bandwidth. This launch uniformly overfills the fiber both angularly and spatially. It excites both radial and azimuthal modes of the fiber equally, thus providing a reproducible bandwidth which is insensitive to small misalignments of the input fiber. It is also relatively insensitive to microbending and macrobending when they are not sufficient to affect power distribution carried by the fiber. A restricted launch gives a less reproducible bandwidth number and is dependent on an exact definition of the launch. Overfilled launch is commonly used to measure the bandwidth of LED-based links.

38A.2 Radial Overfilled Launch (ROFL)

A Radial Overfilled Launch is created when a multimode optical fiber is illuminated by the coherent optical output of a source operating in its lowest order transverse mode in a manner that excites predominantly the radial modes of the multimode fiber. This contrasts with the OFL, which is intended to excite both radial and azimuthal modes of the fiber equally. In practice an ROFL is obtained when

a) A spot of laser light is projected onto the core of the multimode fiber,
b) The laser spot is approximately symmetrical about the optical center of the multimode fiber,
c) The optical axis of both the fiber and the laser beam are approximately aligned,
d) The angle of divergence of the laser beam is less than the numerical aperture of the multimode fiber,
e) The laser spot is larger than the core of the multimode fiber.

An ROFL cannot be created using a multi-transverse mode laser or by simply projecting a speckle pattern through an aperture.

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Annex 40A

(informative)

Additional cabling design guidelines

This annex provides additional cabling guidelines when installing a new Category 5 balanced cabling system or using an existing Category 5 balanced cabling system. These guidelines are intended to supplement those in Clause 40. 1000BASE-T is designed to operate over 4-pair unshielded twisted-pair cabling systems that meet both the Category 5 requirements described in ANSI/TIA/EIA-568A (1995) and ISO/IEC 11801:1995, and the additional transmission parameters of return loss, ELFEXT loss, and MDELFEXT loss specified in 40.7. There are additional steps that may be taken by network designers that provide additional operating margins and ensure the objective BER of 10^{-10} is achieved. Cabling systems that meet or exceed the specifications in 40.7 for a worst case 4-connector topology are recommended for new installations. Whether installing a new Category 5 balanced cabling system or reusing one that is already installed, it is *highly recommended* that the cabling system be measured/certified before connecting 1000BASE-T equipment following the guidelines in (proposed) ANSI/TIA/EIA TSB95.

40A.1 Alien crosstalk

40A.1.1 Multipair cabling (i.e., greater than 4-pair)

Multiple Gigabit Ethernet links [(n*4-Pair) with n greater than 1] should not share a common sheath as in a 25-pair binder group in a multipair cable. When the multipair cable is terminated into compliant connecting hardware (TIA does not specify 25 position connecting hardware), the NEXT loss contributions between the adjacent 4-pair gigabit ethernet link, from connecting hardware and the cable combined, cannot be completely cancelled.

40A.1.2 Bundled or hybrid cable configurations

Another source of alien crosstalk can occur in a bundled or hybrid cable configuration where two or more 4-pair cables are assembled together.

In order to limit the noise coupled between adjacent 1000BASE-T link segments in a bundled or hybrid cable configuration, the PSNEXT loss between a 1000BASE-T duplex channel in a link segment and all duplex channels in adjacent 1000BASE-T link segments should be greater than 35 – 15*log(*f*/100) (dB) at all frequencies from 1 MHz to 100 MHz.

40A.2 Cabling configurations

The primary application for the Clause 40 specification is expected to be between a workstation and the local telecommunications closet. In commercial buildings this application is generally referred to as the horizontal cabling subsystem. As specified in ANSI/TIA/EIA-568-A and ISO/IEC 11801: 1995 the maximum length of a horizontal subsystem building wiring channel is 100 m. The channel consists of cords, cables, and connecting hardware. The maximum configuration for this channel is shown in Figure 40A–1.

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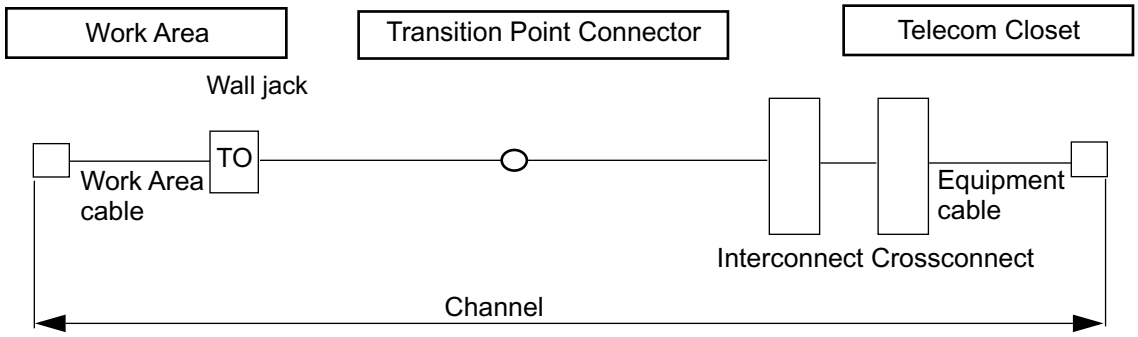


Figure 40A–1—Maximum horizontal subsystem configuration

On the other hand, a minimum configuration can be achieved by removing the patch cord and transition point, which is shown in Figure 40A–2.

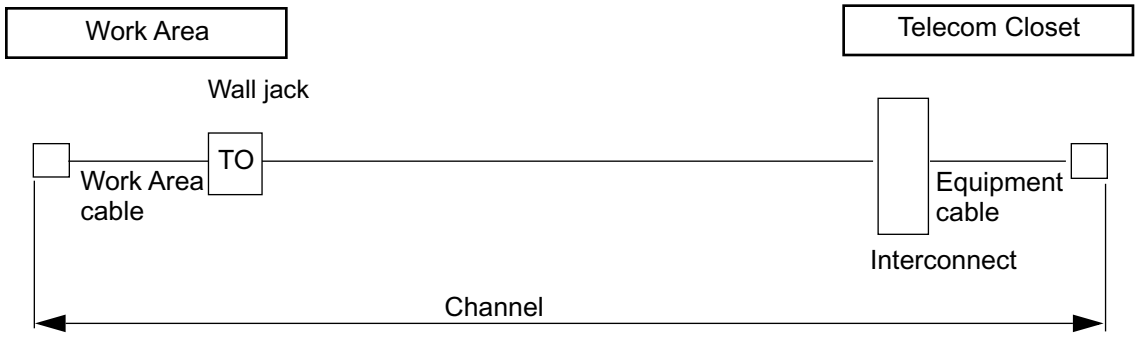


Figure 40A–2—Minimum horizontal subsystem configuration

1000BASE-T is designed to operate over a channel that meets the specifications of 40.7 and the channel configuration shown in Figure 40A–1. However, if the channel specifications of 40.8 cannot be met when using the channel configuration shown in Figure 40A–1, the configuration shown in Figure 40A–2 is recommended. This optimized channel for a 1000BASE-T link segment deletes the transition point and runs an equipment patch cord directly between the LAN equipment and the connector termination of the permanent link. This reduces the number of connectors and their associated crosstalk in the link. The minimum link configuration:

a) Minimizes crosstalk, both near-end and far-end, which maximizes the BER margin; and
b) Minimizes link insertion loss.

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Annex 40B

(informative)

Description of cable clamp

This annex describes the cable clamp used in the common-mode noise rejection test of 40.6.1.3.3, which is used to determine the sensitivity of the 1000BASE-T receiver to common-mode noise from the link segment. As shown in Figure 40B–1, the clamp is 300 mm long, 58 mm wide, 54 mm high with a center opening of 6.35 mm (0.25 in). The clamp consists of two halves that permit the insertion of a cable into the clamp.

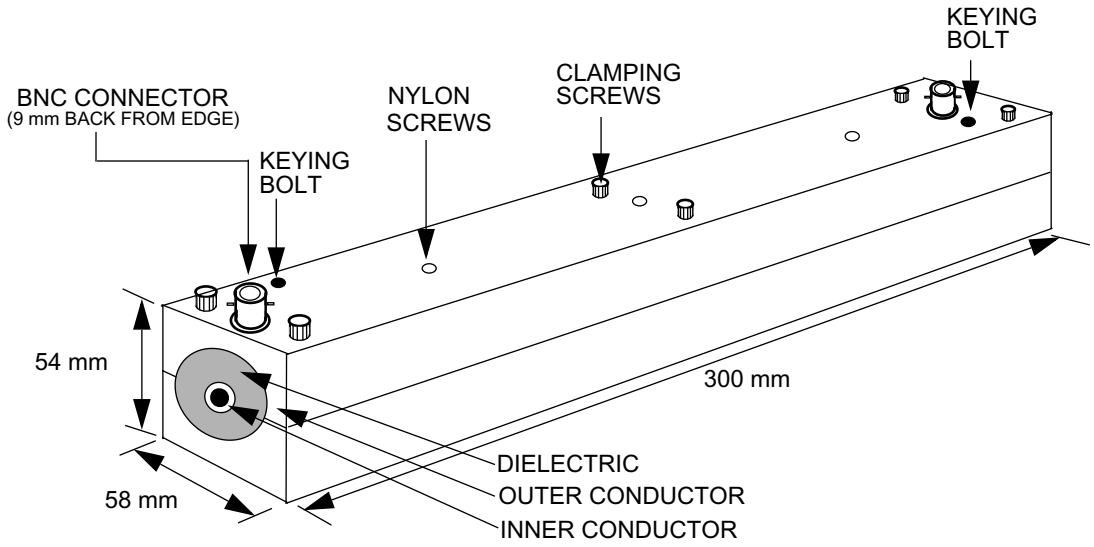


Figure 40B–1—Cable clamp

The clamp has a copper center conductor and an aluminum outer conductor with a high density polyethylene dielectric. The following is a review of the construction and materials of the clamp:

a) *Inner conductor*—Copper tubing with an inner diameter of 6.35 mm (0.25 in) and an outer diameter of 9.4 mm (0.37 in).
b) *Outer conductor*—Aluminum bar that is 300 mm long and approximately 54 mm by 58 mm. The bar is milled to accept the outer diameter of the dielectric material.
c) *Dielectric*—High Density Polyethylene (Residual, TypeF) with dielectric constant of 2.32. An outside diameter of 33.5 mm and an inner diameter that accepts the outside diameter of the copper inner conductor.
d) *Connectors*—BNC connectors are located 9 mm (0.39 in) from each end of the clamp and are recessed into the outer conductor. The center conductor of the connector is connected to the inter conductor as shown in Figure 40B–2.
e) *Clamping screws*—Six screws are used to connect the two halves of the clamp together after the cable has been inserted. Although clamping screws are shown in Figure 40B–1, any clamping method may be used that ensures the two halves are connected electrically and permits quick assembly and disassembly.
f) *Nylon screws*—Used to align and secure the inner conductor and dielectric to the outer conductor. The use and location of the screws is left to the manufacturer.
g) *Keying bolts*—Two studs used to align the two halves of the clamp.

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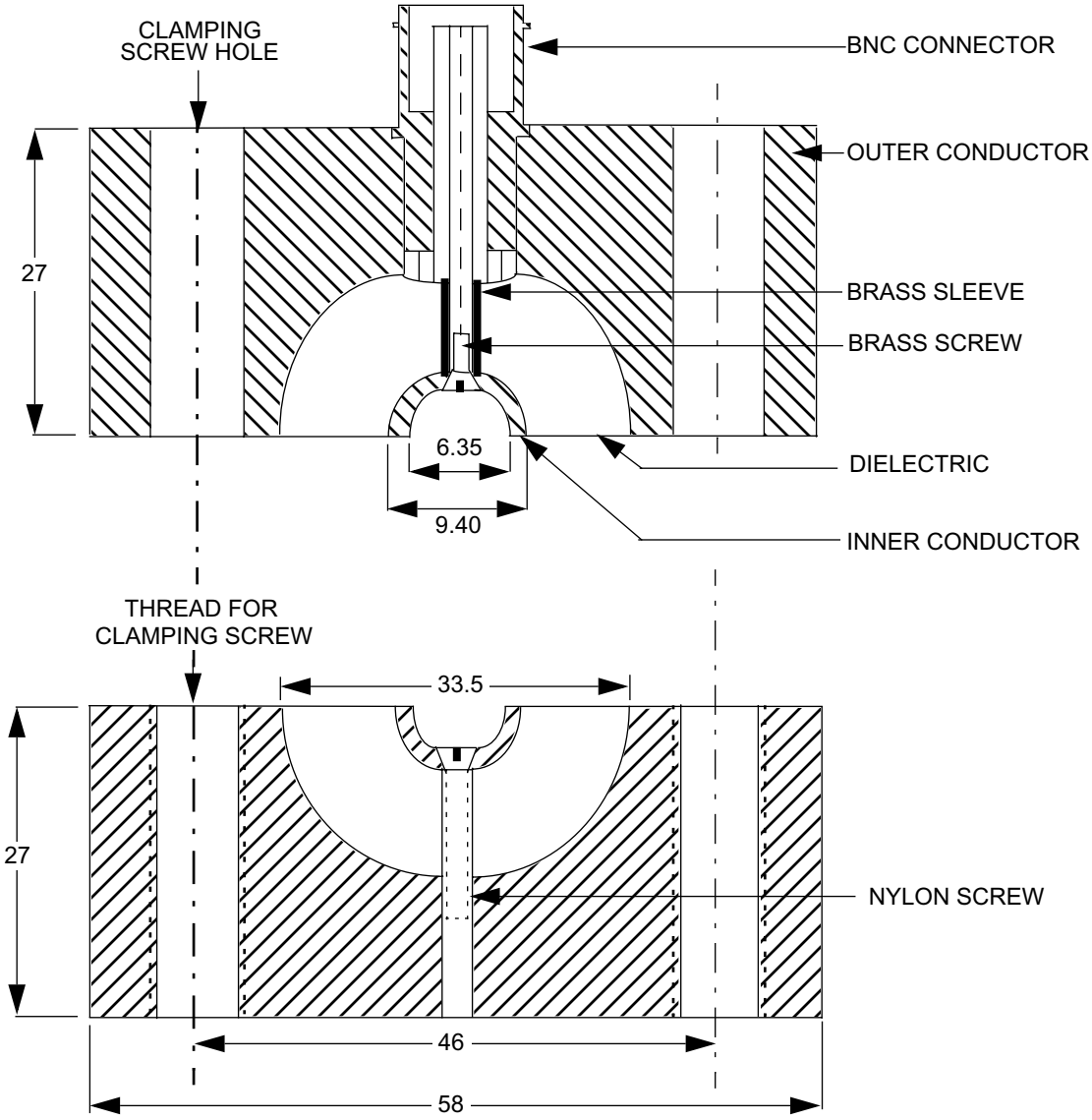


Figure 40B–2—Cross-section of cable clamp

As shown in Figure 40B–2 the inner conductor on the bottom half of the clamp extends slightly (~ 0.1mm) above the dielectric to ensure there is good electrical connection with the inner conductor of the top half of the clamp along the full length of the conductor when the two halves are clamped together.

The electrical parameters of the clamp between 1MHz and 250 MHz are as follows:

a) Insertion loss: < 0.2 dB
b) Return loss: > 20.0 dB

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40B.1 Cable clamp validation

In order to ensure the cable clamp described above is operating correctly, the following test procedure is provided. Prior to conducting the following test shown in Figure 40B–3, the clamp should be tested to ensure the insertion loss and return loss are as specified above. The cable clamp validation test procedure uses a well-balanced 4-pair Category 5 unshielded test cable or better that meets the specifications of 40.7. The test hardware consists of the following:

a) *Resistor network*—Network consists of three 50 ±0.1% Ω resistors; two resistors are connected in series as a differential termination for cable pairs and the other resistor is connected between the two and the ground plane as a common-mode termination.

b) *Balun*—3 ports, laboratory quality with a 100 Ω differential input, 50 Ω differential output, and a 50 Ω common-mode output:

Insertion Loss (100 Ω balanced <->50 Ω unbalanced): <1.2 dB (1-350MHz)

Return Loss: >20 dB (1-350 MHz)

Longitudinal Balance: >50 dB (1-350 MHz)

c) *Test cable*—4-pair 100 Ω UTP category 5 balanced cable at least 30 m long.

d) *Chokes (2)*—Wideband Ferrite Material:

Inter-diameter: 6.35 to 6.86 mm

Impedance: 250 Ω @ 100 MHz

e) *Ground plane*—Copper sheet or equivalent.

f) *Signal generator*

g) *Oscilloscope*

h) *Receiver*

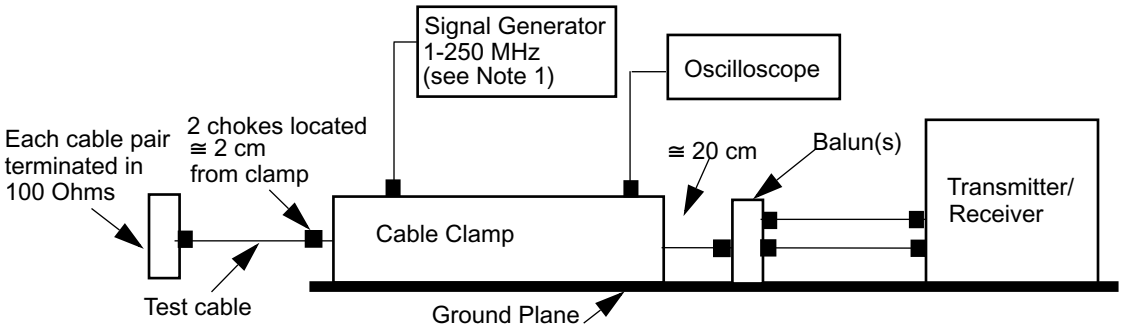


Figure 40B–3—Cable clamp validation test configuration

With the test cable inserted in the cable clamp, a signal generator with a 50 Ω output impedance is connected to one end of the cable clamp and an oscilloscope with a 50 Ω input impedance is connected to the other end. The signal generator shall be capable of providing a sine wave signal of 1 MHz to 250 MHz. The output of the signal generator is adjusted for a voltage of 1.0 Vrms (2.83 Vpp) at 20 MHz on the oscilloscope. The remainder of the test is conducted without changing the signal generator voltage. The cable pairs not connected to the balun are terminated in a resistor network, although when possible it is recommended that each cable pair be terminated in a balun. It very important that the cable clamp, balun, receiver, and resistor networks have good contact with the ground plane. The two chokes, which are located next to each other, are located approximately 2.0 cm from the clamp. The cable between the clamp and the balun should be straight and not in contact with the ground plane.

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The differential-mode and common-mode voltage outputs of the balun should meet the limits shown in Table 40B–1 over the frequency range 1 MHz to 250 MHz for each cable pair. The differential mode voltage at the output of the balun must be increased by 3 dB to take into account the 100-to-50 impedance matching loss of the balun.

Table 40B–1—Common- and differential-mode output voltages

Frequency (*f*)	Common-mode voltage	Differential-mode voltage
1-30 MHz	<0.1+0.97(f/30) Vpp	<2.4 + 19.68 (f/30) mVpp
30-80 MHz	<1.07 Vpp	<22 mVpp
80-250 MHz	<1.07 – 0.6 (f-80)/170 Vpp	<22 mVpp

NOTE—Prior to conducting the validation test the cable clamp should be tested without the cable inserted to determine the variation of the signal generator voltage with frequency at the output of the clamp. The signal generator voltage should be adjusted to 1 Vrms (2.83 Vpp) at 20 MHz on the oscilloscope. When the frequency is varied from 20 MHz to 250 MHz, the voltage on the oscilloscope should not vary more than ±7.5%. If the voltage varies more than ±7.5%, then a correction factor must be applied at each measurement frequency.

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Annex 40C

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Add-on interface for additional Next Pages

This annex describes a technique for implementing Auto-Negotiation for 1000BASE-T when the implementor wishes to send additional Next Pages (other than those required to configure for 1000BASE-T operation). To accomplish this mode of Auto-Negotiation, the implementor must ensure that the three Next Pages required for 1000BASE-T configuration are sent first.

The add-on interface described in this annex shows one technique for supporting the transmission of additional Next Pages. This mechanism utilizes the existing Clause 28 Auto-Negotiation mechanism and variables defined in Clause 28. Its purpose is merely to provide optional NEXT PAGE WAIT responses to the Auto-Negotiation Arbitration state diagram (see Figure 28–16).

The add-on interface for Auto-Negotiation is intended to interface directly between the defined registers and the Auto-Negotiation mechanism defined in Clause 28. The mechanism described includes five main blocks (see Figure 40C–1).

The first three blocks are used by the MASTER-SLAVE resolution function. They are used to generate and store random seeds and to resolve the status of the MASTER-SLAVE relationship. Their operation is described later in this annex. The final two blocks, the transmit state machine for the 1000BASE-T Next Page exchange and the receive state machine for the 1000BASE-T Next Page exchange, are described in this annex.

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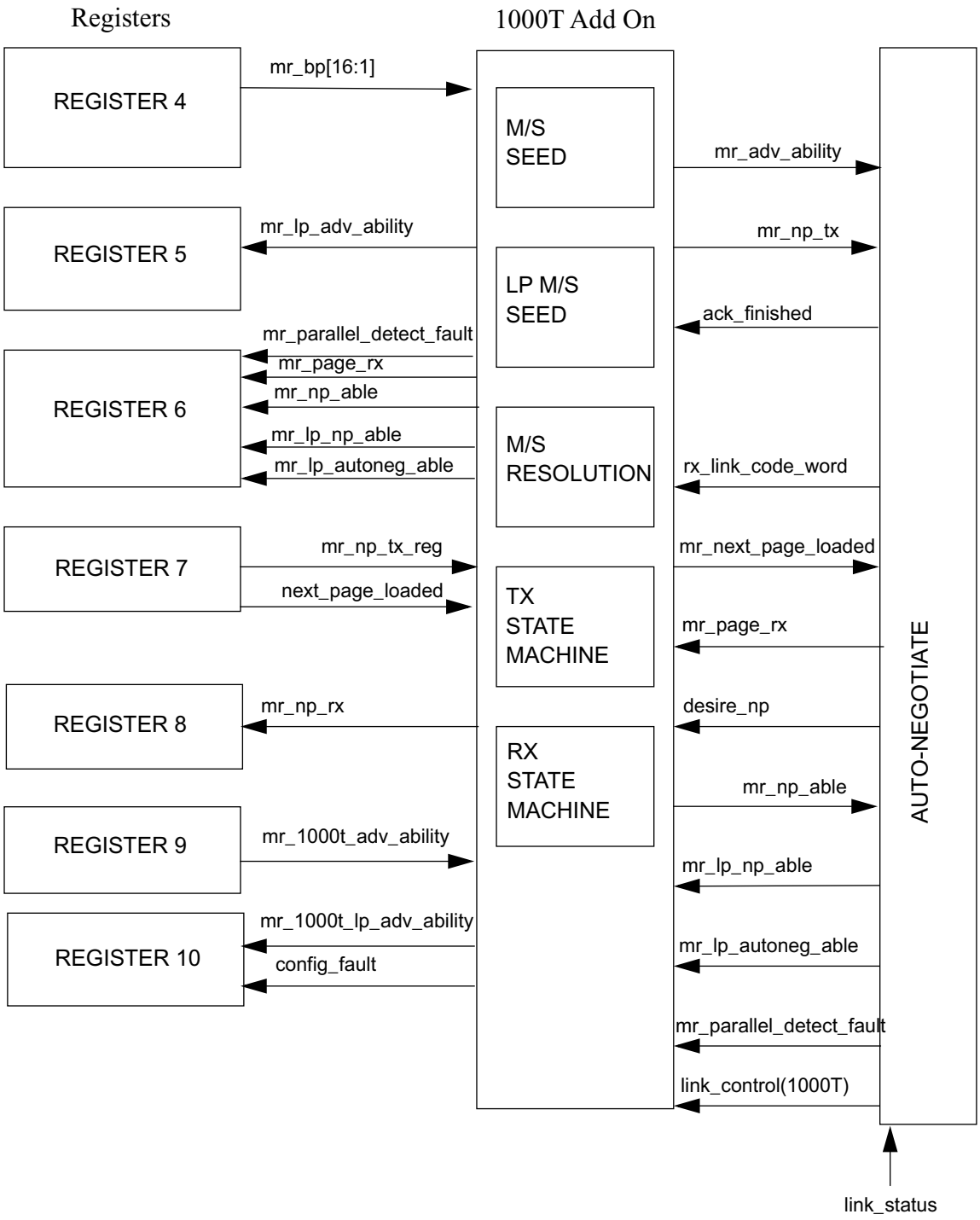


Figure 40C–1—Auto-negotiate add-on diagram for 1000BASE-T

NOTE—When the exchange of Next Pages is complete, the MASTER-SLAVE relationship can be determined using Table 40–5 with the 1000BASE-T Technology Ability Next Page bit values specified in Table 40–4 and information received from the link partner. This process is conducted at the entrance to the FLP LINK GOOD CHECK state shown in the Auto-Negotiation Arbitration State Diagram (Figure 28–16).

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40C.1 State variables

mr_bp
: This variable is used as an intermediate signal from register 4. Normally register 4 would directly source the mr_adv_ability information. This information is now sourced from the transmit state machine.

mr_1000t_adv_ability
: A 16-bit array used to store and indicate the contents of register 9.

mr_1000t_lp_adv_ability
: A 16-bit array used to write information to register 10.

mr_np_tx_reg
: This variable is an intermediate signal from register 7. Normally register 7 would directly source the information to the Auto-Negotiation function via mr_np_tx. This information is now sourced from the transmit state machine.

mr_np_rx
: A 16-bit array used to write information to register 8.
Values: Zeros; data bit is logical zero.
One; data bit is logical one.

config_fault
: This variable indicates the result of the MASTER-SLAVE resolution function.

next_page_loaded
: This variable is an intermediate signal from register 7. Normally register 7 would directly source the information to the Auto-Negotiation function via mr_next_page_loaded. This information is now sourced from the transmit state machine.

reg_random
: An 11-bit array used to store the received random seed from the link partner. It is used by the MASTER-SLAVE resolution function.

1000T_capable
: This variable is used merely to show the local device is 1000Base-T capable. It is shown to illustrate the path that a non-1000Base-T device would take within the auto negotiation mechanism.

ATMP_CNT
: This variable is used to count the number of failed MASTER-SLAVE resolutions. It has a maximum value of 7.

All other signals are defined in Clause 28.

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40C.2 State diagrams

40C.2.1 Auto-Negotiation Transmit state machine add-on for 1000BASE-T

The Auto-Negotiation transmit state machine add-on (see Figure 40C–2) is responsible for sending the Base Page, 1000BASE-T Next Pages, as well as additional Next Pages as specified by the management interface. 1000BASE-T Next Pages will automatically be sent by the PHY whenever there are no additional Next Pages to be sent. If the user desires to send additional Next Pages, then the user must first send three pages of any format. Management will automatically replace these three pages with the appropriate 1000BASE-T Message Page and the two following unformatted pages and then will send the additional Next Pages as specified by the user. All other steps are performed by the management interface. The management interface is now required to complete the Next Page exchange by sourcing its own NULL page. This is shown in Figure 40C–2 for illustration only.

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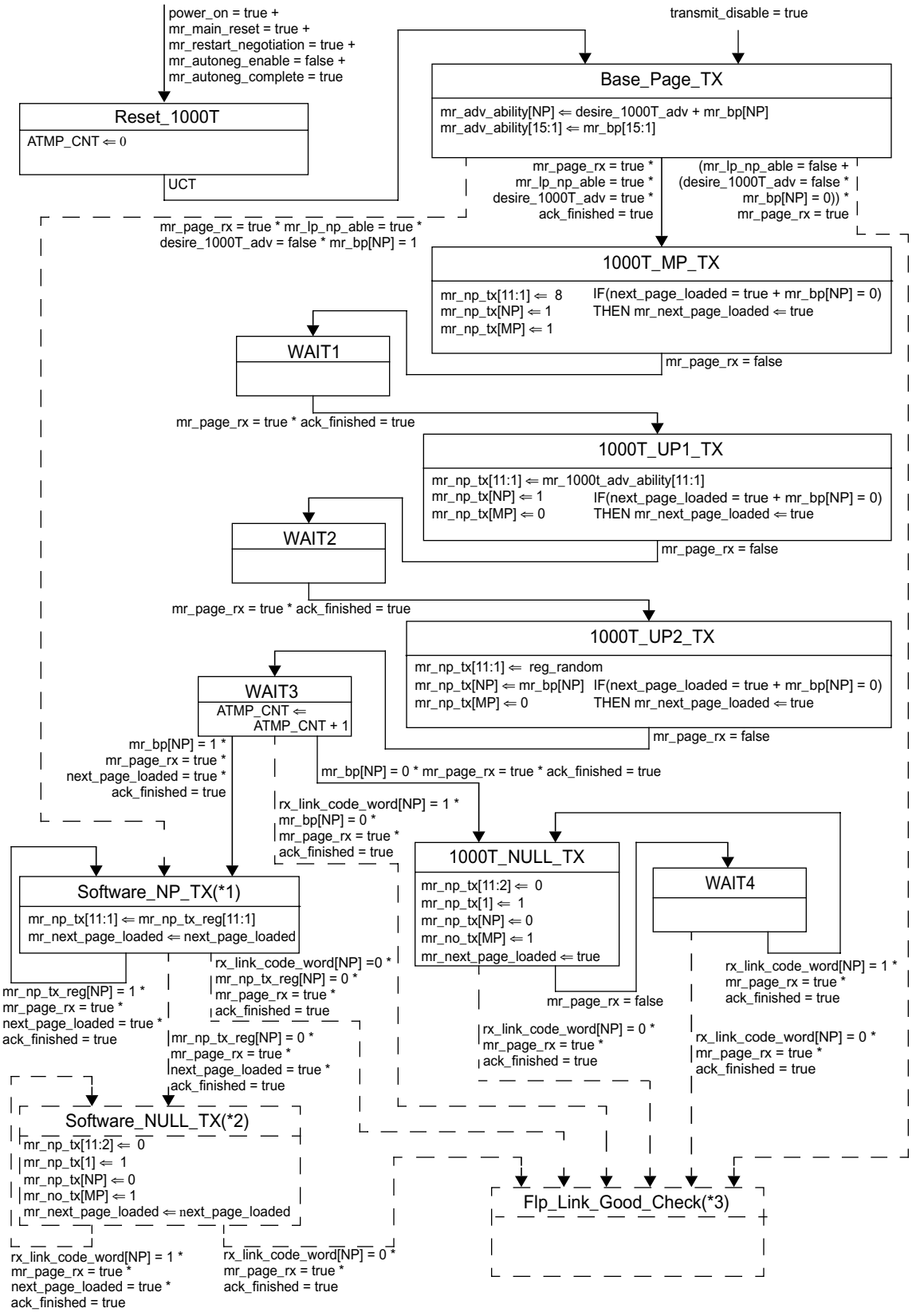


Figure 40C–2—Auto-Negotiation Transmit state diagram add-on for 1000BASE-T

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NOTES for Figure 40C–2

1—(Software_NP_TX) If the user desires to send additional Next Pages, then the contents of the first three Next Pages will be overwritten by the three 1000BASE-T Next Pages. In this case, the user is responsible for stepping through the Next Page sequence (by creating the initial three Next Pages to be overwritten by the three 1000BASE-T Next Pages); otherwise the process is automatic. (next_page_loaded signals clear operation as per Clause 28.)

2—(Software_NULL_TX) This is shown for illustration only. This is done in software and is required.

3—(Flp_Link_Good_Check) This is shown for illustration only. This state is from the Auto-Negotiation arbitration state diagram and indicates the conclusion of pages being sent. (The transition 1000T_capable = false is to show sequence for non 1000BASE-T implementations.)

40C.2.2 Auto-Negotiation receive state diagram add-on for 1000BASE-T

The Auto-Negotiation receive state machine add-on for 1000BASE-T Next Pages (see Figure 40C–3) is responsible for receiving the Base Page, 1000BASE-T Next Pages, and any additional Next Pages received. 1000BASE-T Next Pages will automatically be received whenever the user does not wish to participate in Next Page exchanges. In this case, the appropriate 1000BASE-T message page and its two unformatted pages will automatically be received and stored in their appropriate registers. Any additional Next Pages received will still be placed in register 8, but will be overwritten automatically when a new page is received. The net result is that the management interface does not need to poll registers 6 and 8. The information in register 8 will be meaningless in this case. If the user desires to participate in additional Next Page exchanges via setting the appropriate bit in register 4, the user now becomes responsible (as was previously the case) for defining how this will be accomplished. In this situation, the first three Next Pages received may be 1000BASE-T and should be discarded. This information will automatically be stored internally in the appropriate register 10 and reg_random. The management interface/user can ignore the information received for the 1000BASE-T Next Pages.

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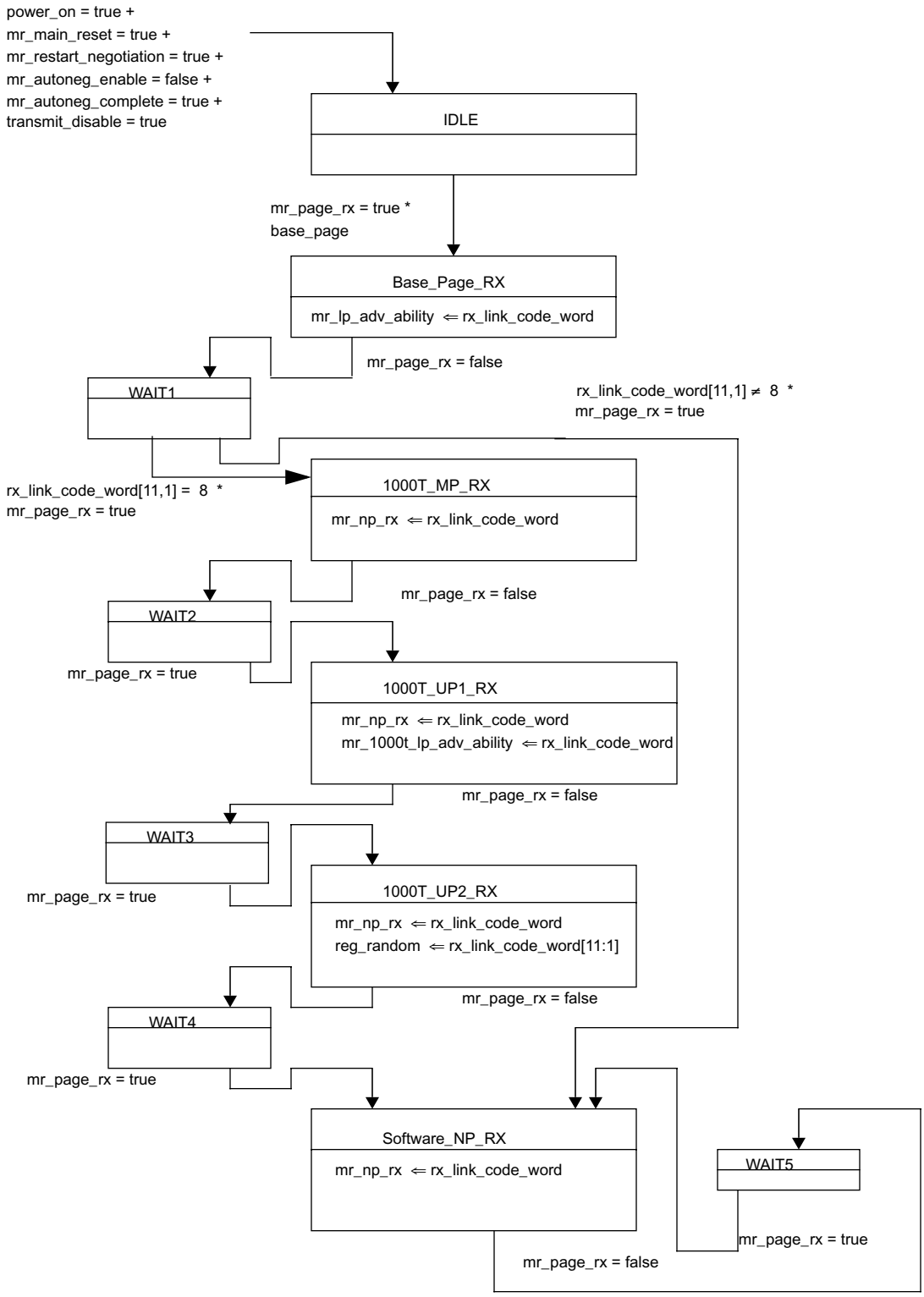


Figure 40C–3—Auto-Negotiation Receive state diagram add-on for 1000BASE-T

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Annex 43A

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Collection and Distribution functions

43A.1 Introduction

The specification of the Collection and Distribution functions was defined with the following considerations in mind:

a) Frame duplication is not permitted.
b) Frame ordering must be preserved in aggregated links. Strictly, the MAC service specification (ISO/IEC 15802-1) states that order must be preserved for frames with a given SA, DA, and priority; however, this is a tighter constraint than is absolutely necessary. There may be multiple, logically independent conversations in progress between a given SA-DA pair at a given priority; the real requirement is to maintain ordering within a conversation, though not necessarily between conversations.
c) A single algorithm can be defined for the collection function that is independent of the distribution function(s) employed by the Partner System.
d) In the interests of simplicity and scalability, the collection function should not perform re-assembly functions, re-order received frames, or modify received frames. Distribution functions, therefore, do not make use of segmentation techniques, do not label or otherwise modify transmitted frames in any way, and must operate in a manner that will inherently ensure proper ordering of received frames with the specified collector.
e) The distribution and collection functions need to be capable of handling dynamic changes in aggregation membership.
f) There are expected to be many different topologies and many different types of devices in which Link Aggregation will be employed. It is therefore unlikely that a single distribution function will be applicable in all cases.

A simple collection function has been specified. The Collector preserves the order of frames received on a given link, but does not preserve frame ordering amongst links. The distribution function maintains frame ordering by

— Transmitting frames of a given conversation on a single link at any time.
— Before changing the link on which frames of a given conversation are transmitted, ensuring that all previously transmitted frames of that conversation have been received to a point such that any subsequently transmitted frames received on a different links will be delivered to the MAC Client at a later time.

Given the wide variety of potential distribution algorithms, the normative text in Clause 43 specifies only the requirements that such algorithms must meet, and not the details of the algorithms themselves. To clarify the intent, this informative annex gives examples of distribution algorithms, when they might be used, and the role of the Marker protocol (43.5) in their operation. The examples are not intended to be either exhaustive or prescriptive; implementors may make use of any distribution algorithms as long as the requirements of Clause 43 are met.

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43A.2 Port selection

A distribution algorithm selects the port used to transmit a given frame, such that the same port will be chosen for subsequent frames that form part of the same conversation. The algorithm may make use of information carried in the frame in order to make its decision, in combination with other information associated with the frame, such as its reception port in the case of a MAC Bridge.

The algorithm may assign one or more conversations to the same port, however, it must not allocate some of the frames of a given conversation to one port and the remainder to different ports. The information used to assign conversations to ports could include the following:

a) Source MAC address
b) Destination MAC address
c) The reception port
d) The type of destination address (individual or group MAC address)
e) Ethernet Length/Type value (i.e., protocol identification)
f) Higher layer protocol information (e.g., addressing and protocol identification information from the LLC sublayer or above)
g) Combinations of the above

One simple approach applies a hash function to the selected information to generate a port number. This produces a deterministic (i.e., history independent) port selection across a given number of ports in an aggregation. However, as it is difficult to select a hash function that will generate a uniform distribution of load across the set of ports for all traffic models, it might be appropriate to weight the port selection in favor of ports that are carrying lower traffic levels. In more sophisticated approaches, load balancing is dynamic; i.e., the port selected for a given set of conversations changes over time, independent of any changes that take place in the membership of the aggregation.

43A.3 Dynamic reallocation of conversations to different ports

It may be necessary for a given conversation or set of conversations to be moved from one port to one or more others, as a result of

a) An existing port being removed from the aggregation,
b) A new port being added to the aggregation, or
c) A decision on the part of the Distributor to re-distribute the traffic across the set of ports.

Before moving conversation(s) to a new port, it is necessary to ensure that all frames already transmitted that are part of those conversations have been successfully received. The following procedure shows how the Marker protocol (43.5) can be used to ensure that no mis-ordering of frames occurs:

1) Stop transmitting frames for the set of conversations affected. If the MAC Client requests transmission of further frames that are part of this set of conversations, these frames are discarded.
2) Start a timer, choosing the timeout period such that, if the timer expires, the destination System can be assumed either to have received or discarded all frames transmitted prior to starting the timer.
3) Use the Marker protocol to send a Marker PDU on the port previously used for this set of conversations.
4) Wait until either the corresponding Marker Response PDU is received or the timer expires.
5) Restart frame transmission for the set of conversations on the newly selected port.

The appropriate timeout value depends on the connected devices. For example, the recommended maximum Bridge Transit Delay is 1 second; if the receiving device is a MAC Bridge, it may be expected to have

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forwarded or discarded all frames received more than 1 second ago. The appropriate timeout value for other circumstances could be smaller or larger than this by several orders of magnitude. For example, if the two Systems concerned are high-performance end stations connected via Gigabit Ethernet links, then timeout periods measured in milliseconds might be more appropriate. In order to allow an appropriate timeout value to be determined, the Frame Collector parameter CollectorMaxDelay (see 43.2.3) defines the maximum delay that the collector can introduce between receiving a frame from a port and either delivering it to the MAC Client or discarding it. This value will be dependent upon the particular implementation choices that have been made in a System. As far as the operation of the Collector state machine is concerned, CollectorMaxDelay is a constant; however, a management attribute, aAggCollectorMaxDelay (30.7.1.1.32), is provided that allows interrogation and administative control of its value. Hence, if a System knows the value of CollectorMaxDelay that is in use by a Partner System, it can set the value of timeout used when flushing a link to be equal to that value of CollectorMaxDelay, plus sufficient additional time to allow for the propagation delay experienced by frames between the two Systems. A value of zero for the CollectorMaxDelay parameter indicates that the delay imposed by the Collector is less than the resolution of the parameter (10 microseconds). In this case, the delay that must be considered is the physical propagation delay of the channel. Allowing management manipulation of CollectorMaxDelay permits fine-tuning of the value used in those cases where it may be difficult for the equipment to pre-configure a piece of equipment with a realistic value for the physical propagation delay of the channel.

The Marker protocol provides an optimization that can result in faster reallocation of conversations than would otherwise be possible—without the use of markers, the full timeout period would always have to be used in order to be sure that no frames remained in transit between the local Distributor and the remote Collector. The timeout described recovers from loss of Marker or Marker Response PDUs that can occur.

43A.4 Topology considerations in the choice of distribution algorithm

Figure 43A–1 gives some examples of different aggregated link scenarios. In some cases, it is possible to use distribution algorithms that use MAC frame information to allocate conversations to links; in others, it is necessary to make use of higher-layer information.

In example A, there is a many-to-many relationship between end stations communicating over the aggregated link. It would be possible for each switch to allocate conversations to links simply on the basis of source or destination MAC addresses.

In examples B and C, a number of end stations communicate with a single server via the aggregated link. In these cases, the distribution algorithm employed in the server or in Switch 2 can allocate traffic from the server on the basis of destination MAC address; however, as one end of all conversations constitutes a single server with a single MAC address, traffic from the end stations to the server would have to be allocated on the basis of source MAC address. These examples illustrate the fact that different distribution algorithms can be used in different devices, as appropriate to the circumstances. The collection function is independent of the distribution function(s) that are employed.

In examples D and E, assuming that the servers are using a single MAC address for all of their traffic, the only appropriate option is for the distribution algorithm used in the servers and switches to make use of higher-layer information (e.g., Transport Layer socket identifiers) in order to allocate conversations to links. Alternatively, in example E, if the servers were able to make use of multiple MAC addresses and allocate conversations to them, then the switches could revert to MAC Address-based allocation.

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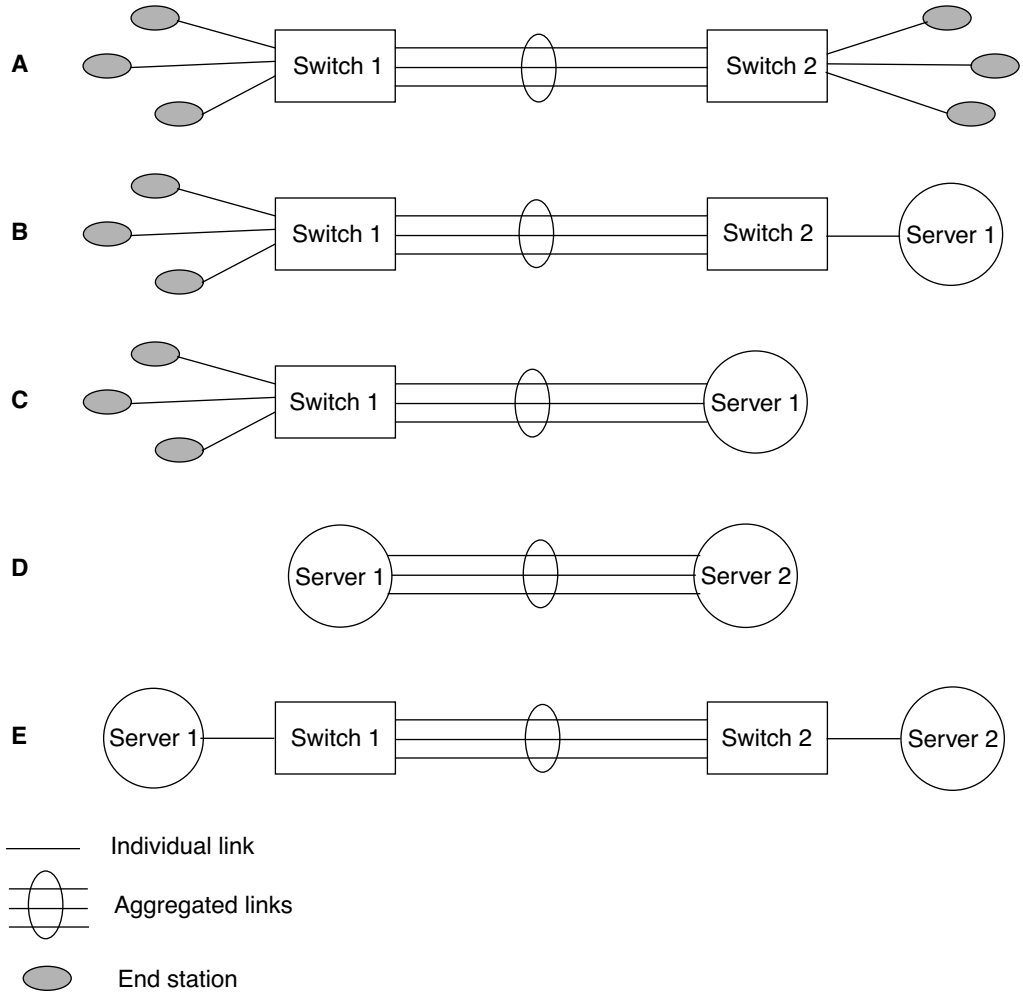


Figure 43A–1—Link aggregation topology examples

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Annex 43B

(normative)

Requirements for support of Slow Protocols

43B.1 Introduction and rationale

There are two distinct classes of protocols used to control various aspects of the operation of IEEE 802.3 devices. They are as follows:

a) Protocols such as the MAC Control PAUSE operation (Annex 31B) that need to process and respond to PDUs rapidly in order to avoid performance degradation. These are likely to be implemented as embedded hardware functions, making it relatively unlikely that existing equipment could be easily upgraded to support additional such protocols.

   NOTE—This consideration was one of the contributing factors in the decision to use a separate group MAC address to support LACP and the Marker protocol, rather than re-using the group MAC address currently used for PAUSE frames.

b) Protocols such as LACP, with less stringent frequency and latency requirements. These may be implemented in software, with a reasonable expectation that existing equipment be upgradeable to support additional such protocols, depending upon the approach taken in the original implementation.

In order to place some realistic bounds upon the demands that might be placed upon such a protocol implementation, this annex defines the characteristics of this class of protocols and identifies some of the behaviors that an extensible implementation needs to exhibit.

43B.2 Slow Protocol transmission characteristics

Protocols that make use of the addressing and protocol identification mechanisms identified in this annex are subject to the following constraints:

a) No more than 5 frames shall be transmitted in any one-second period.
b) The maximum number of Slow Protocols is 10.

   NOTE—This is the maximum number of Slow Protocols that use the specified protocol type defined here. That is, there may be more than 10 slow protocols in the universe, but no more than 10 may map to the same Ethernet Length/Type field.

c) The MAC Client data generated by any of these protocols shall be in the normal length range for an IEEE 802.3 MAC frame, as specified in 4.4.2. It is recommended that the maximum length for a Slow Protocol frame be limited to 128 octets.

   NOTE—The Slow Protocols specified in Clause 43 (i.e., LACP and Marker) conform to this recommended maximum.

d) PDUs generated by these protocols shall use the Basic and not the Tagged frame format (see Clause 3).

The effect of these restrictions is to restrict the bandwidth consumed and performance demanded by this set of protocols; the absolute maximum traffic loading that would result is 50 maximum length frames per second per link.

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43B.3 Addressing

The Slow_Protocols_Multicast address has been allocated exclusively for use by Slow Protocols PDUs; its value is identified in Table 43B–1.

Table 43B–1—Slow_Protocols_Multicast address

Name	Value
Slow_Protocols_Multicast address	01-80-C2-00-00-02

NOTES

1—This address is within the range reserved by ISO/IEC 15802-3 (MAC Bridges) for link-constrained protocols. As such, frames sent to this address will not be forwarded by conformant MAC Bridges; its use is restricted to a single link.

2—Although the two currently existing Slow Protocols (i.e., LACP and the Marker protocol) always use this MAC address as the destination address in transmitted PDUs, this may not be true for all Slow Protocols. In some yet-to-be-defined protocol, unicast addressing may be appropriate and necessary. Rather, the requirement is that this address not be used by any protocols that are not Slow Protocols.

43B.4 Protocol identification

All Slow Protocols use Type-field encoding of the Length/Type field, and use the Slow_Protocols_Type value as the primary means of protocol identification; its value is shown in Table 43B–2.

Table 43B–2—Slow_Protocols_Type field

Name	Value
Slow_Protocols_Type field	88-09

The first octet of the MAC Client data following the Length/Type field is a protocol subtype identifier that distinguishes between different Slow Protocols. Table 43B–3 identifies the semantics of this subtype.

NOTE—Although this mechanism is defined as part of an IEEE 802.3 standard, it is the intent that the reserved code points in this table will be made available to protocols defined by other working groups within IEEE 802, should this mechanism be appropriate for their use.

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Table 43B–3—Slow Protocols subtypes

Protocol Subtype value	Protocol name
0	Unused—Illegal value
1	Link Aggregation Control Protocol (LACP)
2	Link Aggregation—Marker Protocol
3	Reserved for future use
4	Reserved for future use
5	Reserved for future use
6	Reserved for future use
7	Reserved for future use
8	Reserved for future use
9	Reserved for future use
10	Reserved for future use
11–255	Unused—Illegal values

43B.5 Handling of Slow Protocol frames

Any received MAC frame that carries the Slow_Protocols_Type field value is assumed to be a Slow Protocol frame. An implementation that claims conformance to this standard shall handle all Slow Protocol frames as follows:

a) Discard any Slow Protocol frame that carries an illegal value of Protocol Subtype (see Table 43B–3). Such frames shall not be passed to the MAC Client.

b) Pass any Slow Protocol frames that carry Protocol Subtype values that identify supported Slow Protocols to the protocol entity for the identified Slow Protocol.

c) Pass any Slow Protocol frames that carry Protocol Subtype values that identify unsupported Slow Protocols to the MAC Client.

NOTE—The intent of these rules is twofold. First, they rigidly enforce the maximum number of Slow Protocols, ensuring that early implementations of this mechanism do not become invalidated as a result of "scope creep." Second, they make it clear that the appropriate thing to do in any embedded frame parsing mechanism is to pass frames destined for unsupported protocols up to the MAC Client rather than discarding them, thus allowing for the possibility that, in soft configurable systems, the MAC Client might be enhanced in the future in order to support protocols that were not implemented in the hardware.

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43B.6 Protocol Implementation Conformance Statement (PICS) proforma for Annex 43B, Requirements for support of Slow Protocols[14]

43B.6.1 Introduction

The supplier of an implementation that is claimed to conform to Annex 43B shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

43B.6.2 Identification

43B.6.2.1 Implementation identification

Supplier (Note 1)	
Contact point for queries about the PICS (Note 1)	
Implementation Name(s) and Version(s) (Notes 1 and 3)	
Other information necessary for full identification—e.g., name(s) and version(s) of machines and/or operating system names (Note 2)	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

43B.6.2.2 Protocol summary

Identification of protocol specification	IEEE Std 802.3-2002, Annex 43B, Requirements for support of Slow Protocols.
Identification of amendments and corrigenda to the PICS proforma which have been completed as part of the PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21: the answer Yes means that the implementation does not conform to IEEE Std 802.3-2002, Annex 43B, Requirements for support of Slow Protocols.)	

Date of Statement	

[14]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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43B.6.2.3 Transmission characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
SP1	Transmission rate	43B.2	Max 5 frames in any one-second period	M	Yes [ ]
SP2	Frame size	43B.2	Normal IEEE 802.3 frame size range (see 4.4.2)	M	Yes [ ]
SP3	Frame format	43B.2	Basic (not Tagged) frame format	M	Yes [ ]

43B.6.2.4 Frame handling

Item	Feature	Subclause	Value/Comment	Status	Support
FH1	Handling of Slow Protocol frames	43B.5	As specified in 43B.5	M	Yes [ ]

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Annex 43C

(informative)

LACP standby link selection and dynamic Key management

43C.1 Introduction

While any two ports on a given system that have been assigned the same administrative Key may be capable of aggregation, it is not necessarily the case that an arbitrary selection of such ports can be aggregated. (Keys may have been deliberately assigned to allow one link to be operated specifically as a hot standby for another). A system may reasonably limit the number of ports attached to a single Aggregator, or the particular way more than two ports can be combined.

In cases where both communicating systems have constraints on aggregation, it is necessary for them both to agree to some extent on the links to be selected for aggregation and on which not to use. Otherwise it might be possible for the two systems to make different selections, possibly resulting in no communication at all.

When one or more links have to be selected as standby, it is possible that they could be used as part of a different Link Aggregation Group. For this to happen, one or another of the communicating systems has to change the operational Key values used for the ports attached to those links.

If the operational Key values were to be changed independently by each system, the resulting set of aggregations could be unpredictable. It is possible that numerous aggregations, each containing a single link, may result. Worse, with no constraint on changes, the process of both systems independently searching for the best combination of operational Key values may never end.

This annex describes protocol rules for standby link selection and dynamic Key management. It provides examples of a dynamic Key management algorithm applied to connections between systems with various aggregation constraints.

43C.2 Goals

The protocol rules presented

a) Enable coordinated, predictable, and reproducible standby link selections.
b) Permit predictable and reproducible partitioning of links into aggregations by dynamic Key management.

They do not require

c) A LACP system to understand all the constraints on aggregations of multiple ports that might be imposed by other systems.
d) Correct configuration of parameters, i.e., they retain the plug and play attributes of LACP.

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43C.3 Standby link selection

Every link between systems operating LACP is assigned a unique priority. This priority comprises (in priority order) the System Priority, System ID, Port Priority, and Port Number of the higher-priority system. In priority comparisons, numerically lower values have higher priority.

Ports are considered for active use in an aggregation in link priority order, starting with the port attached to the highest priority link. Each port is selected for active use if preceding higher priority selections can also be maintained, otherwise the port is selected as standby.

43C.4 Dynamic Key management

Dynamic Key management changes the Key values used for links that either system has selected as a standby to allow use of more links. Whether this is desirable depends on their use. For example, if a single spanning tree is being used throughout the network, separating standby links into a separate aggregation serves little purpose. In contrast, if equal cost load sharing is being provided by routing, making additional bandwidth available in a separate Link Aggregation Group may be preferable to holding links in standby to provide link resilience.

The communicating system with the higher priority (as determined by System Priority and unique System ID) controls dynamic Key changes. Dynamic Key changes may only be made by this controlling system.

NOTE—The controlling system can observe the port priorities assigned by the Partner system, if it wishes to take these into account.

This rule prevents the confusion that could arise if both systems change Keys simultaneously. In principle the controlling system might search all possible Key combinations for the best way to partition the links into groups. In practice the number of times that Keys may have to be changed to yield acceptable results is small.

After each Key change, the controlling system assesses which links are being held in standby by its Partner. Although there is no direct indication of this decision, standby links will be held OUT_OF_SYNC. After matched information is received from the protocol Partner, and before acting on this information, a “settling time” allows for the Partner’s aggregate wait delay, and for the selected links to be aggregated. Twice the Aggregate Wait Time (the expiry period for the wait_while_timer), i.e., 4 seconds, should be ample. If matched Partner information indicates that all the links that the Actor can make active have been brought IN_SYNC, it can proceed to change Keys on other links without further delay.

43C.5 A dynamic Key management algorithm

The following algorithm is simple but effective.

After the “settling time” (see 43C.4) has elapsed, the controlling system scans its ports in the Link Aggregation Group (i.e., all those ports with a specific operational Key value that have the same Partner System Priority, System ID, and Key) in descending priority order.

For each port, it may wish to know

a) Is the port (i.e., the Actor) *capable* of being aggregated with the ports already selected for aggregation with the current Key? Alternatively is the Actor *not capable* of this aggregation?
b) Is the port’s Partner IN_SYNC or is the Partner OUT_OF_SYNC?

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And as it inspects each port it may

c) *Select* the port to be part of the aggregation with the current Key.
d) *Retain* the current Key for a further iteration of the algorithm, without selecting the port to be part of the current aggregation.
e) *Change* the operational Key to a new value. Once a new value is chosen, all the ports in the current Link Aggregation Group that have their Keys changed will be changed to this new value.

As the ports are scanned for the first time

1) The highest priority port is always selected.

   If it is capable and IN_SYNC, move to step 2).

   Otherwise, **change** the operational Key of all other ports (if any) in this Link Aggregation Group, and apply this dynamic Key algorithm to those ports, beginning with step 1), after the settling time.

2) Move to the next port.

   IF there is a next port, continue at step 3).

   Otherwise, dynamic Key changes for ports with this operational Key are complete.

   Note that ports that were once in the same aggregation may have had their operational Keys changed to (further) new values. If so, apply the dynamic Key management algorithms to those ports, beginning with step 1), after the settling time.

3) If this port is capable and IN_SYNC:

      select it, and repeat from step 2).

   If this port is OUT_OF_SYNC:

      change the operational Key, and repeat from step 2).

   If this port is not capable but IN_SYNC:

      change the operational Key, move to step 4).

4) Move to the next port.

   If there is a next port, continue at step 5).

   Otherwise If there are still ports in the current Link Aggregation Group (which will have the current operational Key), wait for the settling time and appy the dynamic Key management algorithm, beginning with the first such port, at step 3).

   Otherwise, dynamic Key changes for ports with this operational Key are complete.

5) **If** this port is capable:

      retain the current Key and repeat from step 2).

   Otherwise, **change** the operational Key and repeat from step 2).

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This procedure is repeated until no OUT_OF_SYNC links remain, or a limit on the number of steps has been reached.

If the Partner's System ID changes on any link at any time, the Actor's operational Key for that link should revert to the administrative Key value, and the dynamic Key procedure should be rerun. This may involve changing the operational Key values for all the links that were assigned Key values subsequent to the change in Key for the link with the new Partner.

43C.6 Example 1

Two systems, A and B, are connected by four parallel links. Each system can support a maximum of two links in an aggregation. They are connected as shown in Figure 43C–1. System A is the higher priority system.

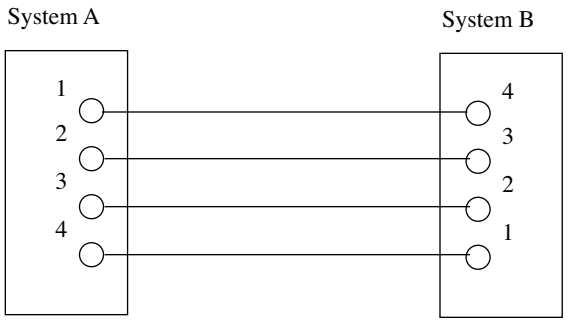


Figure 43C–1—Example 1

The administrative Key for all of System A and System B's ports is 1. Neither system knows before the configuration is chosen that all its ports would attach to links of the same Partner system. Equally, if the links were attached to two different systems, it is not known which pair of links (e.g., 1 and 2, or 1 and 4) would be attached to the same Partner. So choosing the administrative Keys values to be identical for four ports, even though only two could be actively aggregated, is very reasonable.

If there was no rule for selecting standby links, System A and System B might have both selected their own ports 1 and 2 as the active links, and there would be no communication. With the rule, the links A1-B4 and A2-B3 will become active, while A3-B2 and A4-B1 will be standby.

Since System A is the higher-priority system, System B's operational Key values will remain 1 while System A may dynamically change Keys, though it may choose to retain the standby links. Following the Key management algorithm suggested, System A would be able to change the Keys for A3 and A4 in a little over 2 seconds (depending on how fast System B completes the process of attaching its ports to the selected Aggregator) after the connections were first made, and both aggregations could be operating within 5 seconds.

If System A's aggregations were to be constrained to a maximum of three links, rather than two, while System B's are still constrained to two, the suggested algorithm would delay for 4 seconds before changing Keys. Both aggregations could be operating within 7 seconds.

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43C.7 Example 2

A system has the odd design constraint that each of its four ports may be aggregated with one other as follows:

a) Port 1 with port 2, or port 4.
b) Port 2 with port 3, or port 1.
c) Port 3 with port 4, or port 2.
d) Port 4 with port 1, or port 3.

This is equivalent to each port being able to aggregate with either neighbor, understanding the ports to be arranged in a circle.

Two such systems are connected with four parallel links as shown in Figure 43C–2.

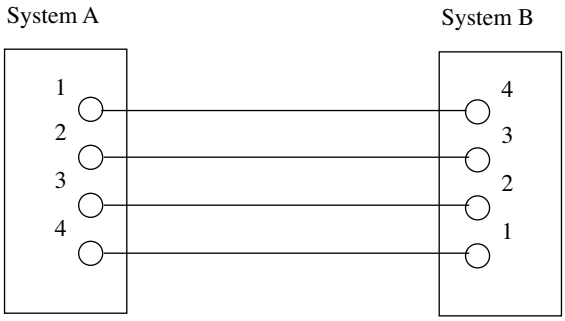


Figure 43C–2—Example 2a

Just as for Example 1, links A1-B4 and A2-B3 become active without changing the operational Key from its original administrative value. The Key for A3 and A4 is changed as soon as they become active, and a few seconds later A3-B2 and A4-B1 become active in a separate aggregation.

If the two systems had been connected as shown in Figure 43C–3:

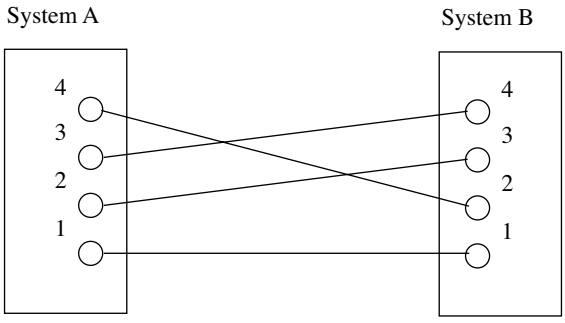


Figure 43C–3—Example 2b

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the following would occur, assuming that System A operates the simple algorithm already described.

Initially System A advertises an operational Key equal to the administrative Key value of 1 on all ports. System B first selects B1 as active; since the link connects to A1 it has the highest priority. The next highest priority link is B3-A2, but System B cannot aggregate B3 with B1, so System B makes this port standby. System B can aggregate B4-A3, so the port is made active. Finally if B4 is aggregated with B1, B2 cannot be aggregated, so B2 is made standby.

System A, observing the resulting synchronization status from System B, assigns a Key value of 2 to ports 2 and 3, retaining the initial Key of 1 for ports 1 and 4. System B will remove B4 from the aggregation with B1, and substitute B2. B3 and B4 will be aggregated. In the final configuration A1-B1 and A4-B2 are aggregated, as are A2-B3 and A3-B4.

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