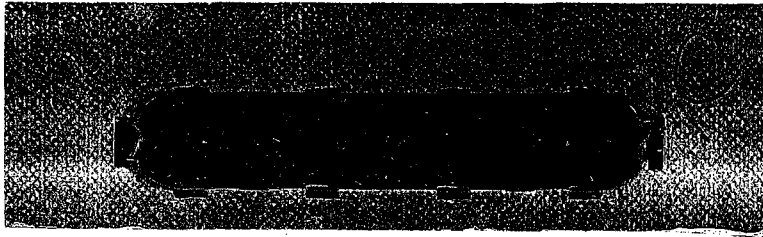


JC688 U.S. PTO
09/11/76
11/17/99

257	Class	447	Subclass
ISSUE CLASSIFICATION			



PATENT NUMBER
6169319
6169319

U.S. UTILITY PATENT APPLICATION

O.I.P.E. <u>SD</u>	PATENT DATE
SCANNED <u>AS</u> Q.A. <u>CT</u>	JAN 02 2001

SECTOR	CLASS <u>257</u> <u>438</u>	SUBCLASS <u>447</u> <u>225</u>	ART UNIT <u>2823</u> <u>2811</u>	EXAMINER <u>MUNSON</u>
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MALINOVICH

div 9/372,863 8/12/99

FILED WITH: ☐ DISK (CRF) ☐ FICHE
(Attached in pocket on right inside flap)

PREPARED AND APPROVED FOR ISSUE

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)					
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	447	257	292	228			
INTERNATIONAL CLASSIFICATION							
H 01 L	27/146						
H 01 L	31/0232						

☐ Continued on Issue Slip Inside File Jacket

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. <u>8</u>	Figs. Drwg. <u>24</u>	Print Fig. <u>5</u>	Total Claims <u>6</u>	Print Claim for O.G. <u>1</u>
☐ a) The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED <u>8/29/00</u>	
☐ b) The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____	GENE M. MUNSON EXAMINER GROUP ART UNIT 2831 <u>Gene M. Munson</u> 8/25/00 (Primary Examiner) (Date)			ISSUE FEE Amount Due <u>1210.00</u> Date Paid <u>11-14-00</u>	
☐ c) The terminal _____ months of this patent have been disclaimed.	<u>Keith Grader</u> (Legal Instruments Examiner) (Date)			ISSUE BATCH NUMBER <u>1244</u>	

WARNING:

The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

Form PTO-436A
(Rev. 10/97)

Issue Fee In File

(LABEL AREA)

Normal Drawings (____ sheets) set _____

(FACE)

PATENT APPLICATION SERIAL NO.

09444, Kdo

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

12/02/1999 DTHOMAS 00000034 09441766

01 FC:101

750.00 OP

PTO-1556
(5/87)

*U.S. GPO: 1998-433-214/80404

Please type a plus sign (+) inside this box → ☐

PTO/SB/05 (4/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**UTILITY
PATENT APPLICATION
TRANSMITTAL**

Only for new nonprovisional applications under 37 C.F.R. § 1.53(b)

Attorney Docket No. TSL-008-1D
First Inventor or Application Identifier Yacov Malinovich
Title "Backside Illuminated Image Sensor"
Express Mail Label No. EL188845492US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ * Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☒ Specification [Total Pages 28]
(preferred arrangement set forth below)
- Descriptive title of the Invention
 - Cross References to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to Microfiche Appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
3. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 8]
4. Oath or Declaration [Total Pages 3]
- a. ☐ Newly executed (original or copy)
- b. ☒ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
- i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting
inventor(s) named in the prior application,
see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

5. ☐ Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
- a. ☐ Computer Readable Copy
- b. ☐ Paper Copy (identical to computer copy)
- c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☐ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement ☐ Power of
(when there is an assignee) ☐ Attorney
9. ☐ English Translation Document (if applicable)
10. ☒ Information Disclosure ☒ Copies of IDS
Statement (IDS)/PTO-1449 ☒ Citations
11. ☒ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
- * Small Entity ☐ Statement filed in prior application
Statement(s) ☐ Status still proper and desired
(PTO/SB/09-12)
13. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
14. ☐ Other: Copy of Recorded Assignment
from parent case
15. ☒ Other: Copy of Recorded Assignment
from parent case

* NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY
FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT
IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28)

16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No: 09/372,863
Prior application Information: Examiner L. Pham Group & Art Unit: 2823

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

☐ Customer Number or Bar Code Label (Insert Customer No. or Attach bar code label here) or ☒ Correspondence address below

Name	Patrick T. Bever				
	BEVER & HOFFMAN, LLP				
Address	2099 Gateway Place, Suite 320				
City	San Jose	State	CA	Zip Code	95110-1017
Country		Telephone	(408) 451-5902	Fax	(408) 451-5908

Name (Print/Type)	Patrick T. Bever	Registration No. (Attorney/Agent)	33,834
Signature	<i>Patrick T. Bever</i>	Date	11/17/99

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

FEE TRANSMITTAL for FY 1999 Patent fees are subject to annual revision. Small Entity payments <u>must</u> be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.	Complete if Known	
	Application Number	Filed herewith
	Filing Date	November 17, 1999
	First Named Inventor	Yacov Malinovich
	Examiner Name	unknown
	Group / Art Unit	unknown
TOTAL AMOUNT OF PAYMENT	(\$)760.00	
Attorney Docket No.		TSL-008-1D

METHOD OF PAYMENT (check one)	FEE CALCULATION (continued)																																																																																																																																																																																				
1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to: Deposit Account Number <u>50-0574</u> Deposit Account Name <u>50-0574</u> ☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17	3. ADDITIONAL FEES <table border="1"><thead><tr><th>Large Fee Code</th><th>Entity Fee (\$)</th><th>Small Fee Code</th><th>Entity Fee (\$)</th><th>Fee Description</th><th>Fee Paid</th></tr></thead><tbody><tr><td>105</td><td>130</td><td>205</td><td>65</td><td>Surcharge - late filing fee or oath</td><td>0.00</td></tr><tr><td>127</td><td>50</td><td>227</td><td>25</td><td>Surcharge - late provisional filing fee or cover sheet.</td><td>0.00</td></tr><tr><td>139</td><td>130</td><td>139</td><td>130</td><td>Non-English specification</td><td>0.00</td></tr><tr><td>147</td><td>2,520</td><td>147</td><td>2,520</td><td>For filing a request for reexamination</td><td>0.00</td></tr><tr><td>112</td><td>920*</td><td>112</td><td>920*</td><td>Requesting publication of SIR prior to Examiner action</td><td>0.00</td></tr><tr><td>113</td><td>1,840*</td><td>113</td><td>1,840*</td><td>Requesting publication of SIR after Examiner action</td><td>0.00</td></tr><tr><td>115</td><td>110</td><td>215</td><td>55</td><td>Extension for reply within first month</td><td>0.00</td></tr><tr><td>116</td><td>380</td><td>216</td><td>190</td><td>Extension for reply within second month</td><td>0.00</td></tr><tr><td>117</td><td>870</td><td>217</td><td>435</td><td>Extension for reply within third month</td><td>0.00</td></tr><tr><td>118</td><td>1,360</td><td>218</td><td>680</td><td>Extension for reply within fourth month</td><td>0.00</td></tr><tr><td>128</td><td>1,850</td><td>228</td><td>925</td><td>Extension for reply within fifth month</td><td>0.00</td></tr><tr><td>119</td><td>300</td><td>219</td><td>150</td><td>Notice of Appeal</td><td>0.00</td></tr><tr><td>120</td><td>300</td><td>220</td><td>150</td><td>Filing a brief in support of an appeal</td><td>0.00</td></tr><tr><td>121</td><td>260</td><td>221</td><td>130</td><td>Request for oral hearing</td><td>0.00</td></tr><tr><td>138</td><td>1,510</td><td>138</td><td>1,510</td><td>Petition to institute a public use proceeding</td><td>0.00</td></tr><tr><td>140</td><td>110</td><td>240</td><td>55</td><td>Petition to revive - unavoidable</td><td>0.00</td></tr><tr><td>141</td><td>1,210</td><td>241</td><td>605</td><td>Petition to revive - unintentional</td><td>0.00</td></tr><tr><td>142</td><td>1,210</td><td>242</td><td>605</td><td>Utility issue fee (or reissue)</td><td>0.00</td></tr><tr><td>143</td><td>430</td><td>243</td><td>215</td><td>Design issue fee</td><td>0.00</td></tr><tr><td>144</td><td>580</td><td>244</td><td>290</td><td>Plant issue fee</td><td>0.00</td></tr><tr><td>122</td><td>130</td><td>122</td><td>130</td><td>Petitions to the Commissioner</td><td>0.00</td></tr><tr><td>123</td><td>50</td><td>123</td><td>50</td><td>Petitions related to provisional applications</td><td>0.00</td></tr><tr><td>126</td><td>240</td><td>126</td><td>240</td><td>Submission of Information Disclosure Stmt</td><td>0.00</td></tr><tr><td>581</td><td>40</td><td>581</td><td>40</td><td>Recording each patent assignment per property (times number of properties)</td><td>0.00</td></tr><tr><td>146</td><td>760</td><td>246</td><td>380</td><td>Filing a submission after final rejection (37 CFR 1.129(a))</td><td>0.00</td></tr><tr><td>149</td><td>760</td><td>249</td><td>380</td><td>For each additional invention to be examined (37 CFR 1.129(b))</td><td>0.00</td></tr><tr><td colspan="5">Other fee (specify) _____</td><td>0.00</td></tr><tr><td colspan="5">Other fee (specify) _____</td><td>0.00</td></tr><tr><td colspan="5">* Reduced by Basic Filing Fee Paid</td><td></td></tr></tbody></table>	Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description	Fee Paid	105	130	205	65	Surcharge - late filing fee or oath	0.00	127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	0.00	139	130	139	130	Non-English specification	0.00	147	2,520	147	2,520	For filing a request for reexamination	0.00	112	920*	112	920*	Requesting publication of SIR prior to Examiner action	0.00	113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	0.00	115	110	215	55	Extension for reply within first month	0.00	116	380	216	190	Extension for reply within second month	0.00	117	870	217	435	Extension for reply within third month	0.00	118	1,360	218	680	Extension for reply within fourth month	0.00	128	1,850	228	925	Extension for reply within fifth month	0.00	119	300	219	150	Notice of Appeal	0.00	120	300	220	150	Filing a brief in support of an appeal	0.00	121	260	221	130	Request for oral hearing	0.00	138	1,510	138	1,510	Petition to institute a public use proceeding	0.00	140	110	240	55	Petition to revive - unavoidable	0.00	141	1,210	241	605	Petition to revive - unintentional	0.00	142	1,210	242	605	Utility issue fee (or reissue)	0.00	143	430	243	215	Design issue fee	0.00	144	580	244	290	Plant issue fee	0.00	122	130	122	130	Petitions to the Commissioner	0.00	123	50	123	50	Petitions related to provisional applications	0.00	126	240	126	240	Submission of Information Disclosure Stmt	0.00	581	40	581	40	Recording each patent assignment per property (times number of properties)	0.00	146	760	246	380	Filing a submission after final rejection (37 CFR 1.129(a))	0.00	149	760	249	380	For each additional invention to be examined (37 CFR 1.129(b))	0.00	Other fee (specify) _____					0.00	Other fee (specify) _____					0.00	* Reduced by Basic Filing Fee Paid					
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SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	Patrick J. Bever			Reg. Number	33,834
Signature				Deposit Account User ID	
Date	11/17/99				

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FEE TRANSMITTAL for FY 1999

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Small Entity payments must be supported by a small entity statement,
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TOTAL AMOUNT OF PAYMENT (\$760.00)

Complete if Known

Application Number Filed herewith
Filing Date November 17, 1999
First Named Inventor Yacov Malinovich
Examiner Name unknown
Group / Art Unit unknown
Attorney Docket No. TSL-008-1D

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit
Account
Number
Deposit
Account
Name

50-0574

- ☒ Charge Any Additional
Fee Required Under
37 CFR 1.16 and 1.17

2. ☒ Payment Enclosed:
☒ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description	Fee Paid
101	760	201	380	Utility filing fee	760.00
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	760	208	380	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) (\$760.00)

2. EXTRA CLAIM FEES

Total Claims	Extra Claims	Fee from below	Fee Paid
6	-20** = 0	18.00	0.00
1	-3** = 0	78.00	0.00
Multiple Dependent			0.00

**or number previously paid, if greater; For Reissues, see below

Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) (\$0.00)

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	0.00
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	0.00
139	130	139	130	Non-English specification	0.00
147	2,520	147	2,520	For filing a request for reexamination	0.00
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	0.00
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	0.00
115	110	215	55	Extension for reply within first month	0.00
116	380	216	190	Extension for reply within second month	0.00
117	870	217	435	Extension for reply within third month	0.00
118	1,360	218	680	Extension for reply within fourth month	0.00
128	1,850	228	925	Extension for reply within fifth month	0.00
119	300	219	150	Notice of Appeal	0.00
120	300	220	150	Filing a brief in support of an appeal	0.00
121	260	221	130	Request for oral hearing	0.00
138	1,510	138	1,510	Petition to institute a public use proceeding	0.00
140	110	240	55	Petition to revive - unavoidable	0.00
141	1,210	241	605	Petition to revive - unintentional	0.00
142	1,210	242	605	Utility issue fee (or reissue)	0.00
143	430	243	215	Design issue fee	0.00
144	580	244	290	Plant issue fee	0.00
122	130	122	130	Petitions to the Commissioner	0.00
123	50	123	50	Petitions related to provisional applications	0.00
126	240	126	240	Submission of Information Disclosure Stmt	0.00
581	40	581	40	Recording each patent assignment per property (times number of properties)	0.00
146	760	246	380	Filing a submission after final rejection (37 CFR 1.129(a))	0.00
149	760	249	380	For each additional invention to be examined (37 CFR 1.129(b))	0.00
Other fee (specify)					0.00
Other fee (specify)					0.00

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$0.00)

SUBMITTED BY

Typed or
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1 BACKSIDE ILLUMINATED IMAGE SENSOR

2
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4 Ephie Koltin

5 *This App'n is a Div of Ser. No. 09/372,863 filed Aug. 12, 1999.*

6 FIELD OF THE INVENTION

7 The present invention relates to solid state image
8 sensors. More specifically, the present invention relates
9 to a method for fabricating backside illuminated image
10 sensors and to a backside illuminated image sensor
11 fabricated by the method.

12
13 RELATED ART

14 Solid state image sensors are used in, for example,
15 video cameras, and are presently realized in a number of
16 forms including charge coupled devices (CCDs) and CMOS image
17 sensors. These image sensors are based on a two dimensional
18 array of pixels. Each pixel includes a sensing element that
19 is capable of converting a portion of an optical image into
20 an electronic signal. These electronic signals are then
21 used to regenerate the optical image on, for example, a
22 display.

23 CMOS image sensors first appeared in 1967. However,
24 CCDs have prevailed since their invention in 1970. Both
25 solid-state imaging sensors depend on the photovoltaic
26 response that results when silicon is exposed to light.
27 Photons in the visible and near-IR regions of the spectrum
28 have sufficient energy to break covalent bonds in silicon.
29 The number of electrons released is proportional to the
30 light intensity. Even though both technologies use the same
31 physical properties, all-analog CCDs dominate vision

1 applications because of their superior dynamic range, low
2 fixed-pattern noise (FPN), and high sensitivity to light.

3 More recently, however, CMOS image sensors have gained
4 in popularity. Pure CMOS image sensors have benefited from
5 advances in CMOS technology for microprocessors and ASICs
6 and provide several advantages over CCD imagers. Shrinking
7 lithography, coupled with advanced signal-processing
8 algorithms, sets the stage for sensor array, array control,
9 and image processing on one chip produced using these well-
10 established CMOS techniques. Shrinking lithography should
11 also decrease image-array cost due to smaller pixels.
12 However, pixels cannot shrink too much, or they have an
13 insufficient light-sensitive area. Nonetheless, shrinking
14 lithography provides reduced metal-line widths that connect
15 transistors and buses in the array. As discussed below, in
16 frontside illuminated image sensors, this reduction of
17 metal-line width exposes more silicon to light, thereby
18 increasing light sensitivity. CMOS image sensors also
19 provide greater power savings, because they require fewer
20 power-supply voltages than do CCD imagers. In addition, due
21 to modifications to CMOS pixels, newly developed CMOS image
22 sensors provide high-resolution, low-noise images that
23 compare with CCD imager quality.

24 CMOS pixel arrays are at the heart of the newly
25 developed CMOS image sensors. CMOS pixel-array construction
26 uses active or passive pixels. Active-pixel sensors (APSSs)
27 include amplification circuitry in each pixel. Passive
28 pixels use photodiodes to collect the photocharge, whereas
29 active pixels can include either photodiode or photogate
30 light sensitive regions. The first image-sensor devices
31 used in the 1960s were passive pixel arrays, but read noise
32 for passive pixels has been found to be high, and it is

1 difficult to increase the passive pixel array's size without
2 exacerbating the noise. CMOS active-pixel sensors (APSS)
3 overcome passive-pixel deficiencies by including active
4 circuits (transistors) in each pixel.

5 Fig. 1 shows a CMOS APS image sensor circuit 100 that
6 includes a pixel array 110 and control circuitry 120.

7 Pixel array 110 includes a closely-spaced matrix of APS
8 cells (pixels) 140 that are arranged in rows and columns.
9 Pixel array 110 is depicted as a ten-by-ten array for
10 illustrative purposes only. Pixel arrays typically consist
11 of a much larger number of pixels (e.g., 804-by-1016
12 arrays). Moreover, the pixels may be arranged in patterns
13 other than rows and columns. Each APS cell 140 of pixel
14 array 110 includes a light sensing element that is capable
15 of converting a detected quantity of light into a
16 corresponding electrical signal at an output terminal 150.
17 The pixels in each row are connected to a common reset
18 control line 123 and a common row select control line 127.
19 The pixels in each column are connected through respective
20 output terminals 150 to an associated common column data
21 line 130.

22 Control circuitry 120 includes a row decoder 123 and
23 sense amplifiers/registers 127. A timing controller (not
24 shown) provides timing signals to row decoder 120 that
25 sequentially activates each row of APS cells 140 via reset
26 control lines 124 and row select control lines 125 to detect
27 light intensity and to generate corresponding output voltage
28 signals during each frame interval. A frame, as used
29 herein, refers to a single complete cycle of activating and
30 sensing the output from each APS cell 140 in the array a
31 single time over a predetermined frame time period. The
32 timing of the imaging system is controlled to achieve a

4 3

1 desired frame rate, such as 30 frames per second in video
2 applications. The detailed circuitry of the row decoder
3 123, sense amplifiers/registers 127 and timing controller is
4 well known to one ordinarily skilled in the art. When
5 detecting a particular frame, each row of pixels may be
6 activated to detect light intensity over a substantial
7 portion of the frame interval. In the time remaining after
8 the row of APS cells 140 has detected the light intensity
9 for the frame, each of the respective pixels simultaneously
10 generates output voltage signals corresponding to the amount
11 of light detected by that APS cell 140. If an image is
12 focused on the array 110 by, for example, a conventional
13 camera lens, then each APS cell 140 generates an output
14 voltage signal corresponding to the light intensity for a
15 portion of the image focused on that APS cell 140. The
16 output voltage signals generated by the activated row are
17 simultaneously provided to column output lines 130 via
18 output terminals 150. Column output lines 130 transmit
19 these output voltage signals to sense amplifiers/registers
20 127.

21 Figs. 2(A) and 2(B) are simplified schematic and cross-
22 sectional views showing a conventional frontside illuminated
23 APS (image sensor) cell 140(1). APS cell 140(1) includes a
24 photodiode 210, a reset transistor 220, an amplifier formed
25 by a source-follower transistor 230, and a select transistor
26 240. Reset transistor 220 includes a gate connected to
27 reset control line 124(1), a first terminal connected to a
28 voltage source V_{DD} (e.g., 5 volts) that is transmitted on a
29 voltage source line 223, and a second terminal connected to
30 a terminal of photodiode 210 and to the gate of source-
31 follower transistor 230 via metal line 224. Reset
32 transistor 220 controls integration time and, therefore,

5 4

1 provides for electronic shutter control. Source-follower
2 transistor 230 has a first terminal connected to voltage
3 source line 223, a second terminal connected to a first
4 terminal of select transistor 240. Source-follower
5 transistor 230 buffers the charge transferred to column
6 output lines 130 from photodiode 210, and provides current
7 to charge and discharge capacitance on column output lines
8 130 more quickly. The faster charging and discharging allow
9 the length of column output lines 130 to increase. This
10 increased length, in turn, allows an increase in array size.
11 Select transistor 240 has a gate connected to row select
12 control line 125(1) and a second terminal connected to
13 column data line 130(1) via output terminal 150(1). Select
14 transistor 240 gives half the coordinate-readout capability
15 to the array. Although reset transistor 220, source-
16 follower transistor 230 and select transistor 240 would
17 appear to increase the power consumption of APS cell 140(1)
18 over passive pixel cells, little difference exists between
19 an active and a passive pixel's power consumption.

20 Fig. 2(B) shows a simplified cross-section of
21 conventional APS cell 140(1). APS cell 140(1) is formed in
22 a P-type substrate 250 using known CMOS techniques.
23 Photodiode 210 is formed in a first n-type diffusion (light
24 sensitive) region 215. Voltage source V_{DD} is applied via
25 voltage source line 223 to a second n-type diffusion region
26 225 that is spaced from photodiode region 215. A first
27 polysilicon gate structure 227 is provided over the space
28 between diffusion region 225 and photodiode region 215 and
29 connected to reset control line 124(1) to collectively form
30 reset transistor 220. A third n-type diffusion region 235
31 is spaced from second region 225, and a second polysilicon
32 gate structure 237 is formed over this space. Photodiode

1 210 is connected to second polysilicon gate 237 by metal
2 line 224 to form source-follower transistor 230. A fourth
3 n-type diffusion region 245 is spaced from third region 235,
4 and a third polysilicon gate structure 247 is formed over
5 this space and connected to row select control line 125(1)
6 to form select transistor 240. Fourth diffusion region 245
7 is connected to output terminal 150(1), which in turn is
8 connected to column data line 130(1). APS cell 140(1) is
9 depicted as an n-channel device with electrons as the photo-
10 generated charge carriers. In alternative embodiments (not
11 shown), APS cells may be formed as a p-channel device with
12 holes as the photo-generated charge carriers.

13 APS cell 140(1) operates in an integration and readout
14 phase that is controlled by signals received on reset
15 control line 124(1) and row select control line 125(1).
16 Reset transistor 220 is pulsed on and off during the
17 integration phase. This reset process causes the potential
18 of photodiode region 215 to float at a reset level
19 approximately equal to V_{DD} less the threshold voltage of
20 reset transistor 220. Photodiode 210 inherently includes
21 capacitance to store an amount of charge proportional to the
22 light intensity reflected from an object. The
23 photogenerated current discharges the pixel capacitance and
24 causes the potential of the photodiode 210 to decrease from
25 its value of approximately V_{DD} to another value, the signal
26 value, which is dictated by the amount of photogenerated
27 current. The difference between the reset and signal levels
28 is proportional to the incident light and constitutes the
29 video signal. Photodiode 210 is buffered from the output
30 terminal 50 by source-follower transistor 230. Select
31 transistor 240 is used to select the pixel for read-out.

1 A problem associated with frontside illuminated CMOS APS
2 cell 140(1) is that the active circuits, and in
3 particular, the metal lines associated with the active
4 circuits, reduce the fill factor (i.e., the ratio of light
5 sensing area to total pixel area) of CMOS APS pixel arrays.
6 In particular, as shown in Fig. 2(B), reset control lines
7 124, row select control lines 125, voltage source lines 223,
8 metal lines 224 and column output lines 130 are all formed
9 in an silicon-dioxide insulation layer located over P-
10 substrate 250. Light, in the form of photons, passes
11 through the insulation layer to light sensitive diffusion
12 region 215, thereby producing a photovoltaic reaction. The
13 presence of the metal and polysilicon lines associated with
14 the active circuits reduces the amount of light that reaches
15 the photodiode diffusion region 215, thereby producing a
16 non-optimal fill factor. As mentioned above, the reduction
17 of metal-line width associated with cutting edge CMOS
18 fabrication processes exposes more silicon to light.
19 However, even very thin metal lines produce some light
20 blockage, thereby preventing frontside illuminated image
21 sensors from achieving a 100% fill factor.

22 Backside illuminated image sensors are alternative image
23 sensor structures that address the fill factor problems
24 associated with front illumination. Backside illuminated
25 image sensors receive light through a backside (lower)
26 surface of the substrate supporting the CMOS image sensor
27 circuitry. To detect light from the backside, the substrate
28 must be extremely thin (i.e., in the range of 15 to 20
29 microns).

30 While backside illuminated image sensors eliminate the
31 fill factor problems associated with frontside illuminated
32 sensors, conventional methods for fabricating backside

8

7

1 illuminated image sensors are expensive. Most notably, many
2 conventional methods require non-standard fabrication
3 process steps, such as a boron doping step and diffusion of
4 special metal films that differ from standard CMOS processes
5 and are performed to control the potential on the backside
6 of the wafer during fabrication. In addition, packaging of
7 conventional backside illuminated image sensors is performed
8 after image sensor fabrication is completed (e.g., device
9 fabrication on a semiconductor substrate, backside treatment
10 of the semiconductor substrate, mounting the semiconductor
11 substrate onto a permanent substrate, and thinning the
12 semiconductor substrate to facilitate backside
13 illumination). This post-production packaging of backside
14 illuminated image sensors is logistically complex and
15 produces high production costs.

16 What is needed is a method for fabricating back
17 illuminated image sensors that minimizes the fabrication and
18 production costs associated with conventional methods.

19
20 SUMMARY

21 The present invention is directed to a method for
22 producing a back-illuminated CMOS image sensor in which the
23 semiconductor wafer upon which pixels are fabricated is
24 mounted onto a protective substrate, and then subjected to a
25 material erosion process to thin the semiconductor substrate
26 until the semiconductor substrate has a thickness that
27 allows effective exposure of the pixels through the backside
28 surface of the semiconductor substrate. Because the
29 material erosion process takes place after the semiconductor
30 substrate is mounted on the protective substrate, the CMOS
31 image sensor can be fabricated using well-established
32 processing parameters, thereby making the fabrication

1 process less expensive to perform. In addition, because the
2 method utilizes a protective substrate to support the
3 semiconductor substrate, the thinning process is less
4 expensive to perform. Further, the production method
5 incorporates package formation using standard CMOS process
6 steps, thereby reducing logistical complexity and production
7 costs.

8 In accordance with one embodiment, the method begins by
9 fabricating an image sensor circuit, including a matrix of
10 pixels (e.g., CMOS APS cells), on the semiconductor
11 substrate. The semiconductor substrate is then secured to
12 the protective substrate using an adhesive such that the
13 processed (frontside) surface of the semiconductor substrate
14 (i.e., the surface upon which the image sensor circuit is
15 formed) faces the protective substrate. The exposed
16 backside surface of the semiconductor substrate is then
17 subjected to the material erosion process (i.e., grinding
18 and chemical etching, followed by an optional backside
19 stripping technique such as chemical/mechanical polishing)
20 to thin the semiconductor substrate until the semiconductor
21 substrate is transparent to visible light, thereby
22 effectively exposing the light-sensitive pixel diffusion
23 regions of the image sensor circuit through the backside
24 surface. In one embodiment, the semiconductor substrate is
25 eroded until its thickness is in the range of 10 to 15
26 microns. The backside surface is then treated using known
27 techniques (i.e., doping or backside metal film formation)
28 to remove the backside depletion region and to drive
29 electrons toward the frontside surface of the semiconductor
30 substrate. A transparent substrate (e.g., glass) is then
31 secured to the backside surface of the semiconductor
32 substrate, thereby sandwiching the semiconductor substrate

10⁹

1 between the transparent substrate and the protective
2 substrate. Openings are then formed in either the
3 protective substrate or the transparent substrate, and metal
4 leads are then formed to contact metal pads of the image
5 sensor.

6 In accordance with another embodiment of the present
7 invention, a back-illuminated CMOS image sensor includes a
8 matrix of CMOS APS cells (light-sensitive pixel regions)
9 that are produced on a semiconductor substrate. In contrast
10 to prior art APS cells, the novel CMOS APS cell is formed on
11 a frontside surface of the semiconductor substrate that is
12 facing away from the image source. In particular, the novel
13 CMOS APS cells include a photodiode diffusion region that
14 extends into the substrate from the frontside surface, and
15 several metal lines are formed in an insulator material that
16 is formed on the frontside surface. A protective substrate
17 is secured to the semiconductor substrate such that the
18 metal lines are located behind the photodiode diffusion
19 region (i.e., between the protective substrate and the
20 semiconductor substrate). Finally, a transparent substrate
21 (e.g., glass) is secured to the backside surface of the
22 semiconductor substrate, thereby sandwiching the
23 semiconductor substrate between the transparent substrate
24 and the protective substrate.

25 The novel aspects of the present invention will be more
26 fully understood in view of the following description and
27 drawings.

28

29 BRIEF DESCRIPTION OF THE DRAWINGS

30 Fig. 1 is a schematic diagram of an active pixel sensor
31 array;

1 Figs. 2(A) and 2(B) are simplified schematic and cross-
2 sectional views showing a conventional front-illuminated
3 CMOS APS cell;

4 Figs. 3(A) and 3(B) are simplified plan and partial
5 cross-sectional views showing a semiconductor wafer that
6 includes a plurality of image sensor circuits;

7 Figs. 4(A) through 4(I) are cross-sectional views
8 showing process steps associated with the production of
9 backside illuminated image sensors in accordance with a
10 first embodiment of the present invention; and

11 Fig. 5 is a cross-sectional view showing a backside
12 illuminated CMOS APS cell that is fabricated in accordance
13 with the present invention; and

14 Figs. 6(A) through 6(I) are cross-sectional views
15 showing process steps associated with the production of
16 backside illuminated image sensors in accordance with a
17 second embodiment of the present invention.

18
19 DETAILED DESCRIPTION

20 The present invention is described below with reference
21 to CMOS active-pixel sensors (APSS), and in particular to
22 CMOS APSS utilizing photodiode light sensitive regions.
23 However, the methods and structures described below may also
24 be used to produce passive CMOS image sensors and CMOS APSS
25 utilizing photogate light sensitive regions. In addition,
26 the present inventors believe the methods and structures of
27 the present invention may also be used to produce MOS pixel
28 arrays and charge-coupled devices (CCDs).

29 Figs. 3(A) and 3(B) are plan and partial cross-
30 sectional views showing a wafer 300 upon which is formed a
31 plurality of image sensor circuits 100. Wafer 300 is, e.g.,
32 a silicon wafer having a thickness in the range of 600 to

1 650 μm , and includes a first (frontside) surface 310 and a
2 second (backside) surface 320. Each image sensor circuit
3 100 is formed on first surface 310, and includes a matrix of
4 light-sensitive pixel regions 110 (see Fig. 1) extending
5 into wafer 300 from first surface 310. Each image sensor
6 circuit 100 also includes control circuitry 120 (see Fig. 1)
7 and a plurality of metal contact pads 330 extending onto
8 first surface 310 of wafer 300. Insulation and metal lines
9 (not shown) are formed on wafer 300 and provide connections
10 between metal contact pads 330 and the matrix of light-
11 sensitive pixel regions 110 and control circuitry 120.
12 After the fabrication process is completed and wafer 300 is
13 diced, each image sensor 100 is a fully packaged device with
14 metal contact pads 330 providing contact points for external
15 access to light-sensitive pixel regions 110 and control
16 circuitry 120.

17 Figs. 4(A) through 4(I) illustrate a method of
18 producing backside illuminated image sensors 100 in
19 accordance with a first embodiment of the present invention.

20 Fig. 4(A) is a cross-sectional view showing a step of
21 securing wafer 300 onto a protective substrate 410 with
22 first surface 310 facing protective substrate 410.
23 Specifically, as described above with reference to Figs.
24 3(A) and 3(B), wafer 300 is pre-fabricated with image
25 sensors 100 formed on first surface 310. Because
26 fabrication of image sensors 100 is performed before
27 mounting onto protective substrate 410, standard processes
28 and equipment are used during the fabrication process. As
29 mentioned above, wafer 300 has a beginning thickness T_0 of
30 600 to 650 μm . A first adhesive layer 420 is deposited onto
31 protective substrate 410, and then wafer 300 is placed onto
32 protective substrate 410 such that first surface 310

1 contacts the deposited adhesive layer 410. In one
2 embodiment, protective substrate 410 is formed from glass
3 having a thickness of approximately 100 μm . Adhesive layer
4 420 is composed of, e.g., epoxy, and has a thickness in the
5 range of 80 to 100 μm .

6 Figs. 4(B) and 4(C) are cross-sectional views showing
7 subsequent steps of removing material from second surface
8 320 of the wafer 300 until the light-sensitive pixel regions
9 of image sensor circuits 100 are effectively exposed through
10 the second surface 320. The term "effectively exposed" is
11 used herein to indicate that the pixel of each light-
12 sensitive pixel region generates electron flow in response
13 to light (photons) passing through second surface 320. As
14 such, the term "effectively exposed" is intended to cover
15 the actual exposure of the diffused (n+) pixel regions on
16 second surface 320, by may also cover the case where a thin,
17 mostly transparent layer of p-type wafer material is located
18 between each diffused pixel region and second surface 320.

19 Referring to Fig. 4(B), the process of removing
20 material from second surface 320(A) of wafer 300 begins with
21 a planar erosion process 433 whereby the thickness of wafer
22 300 is reduced to a thickness T_1 , which is in the range of
23 120 to 140 μm . In one embodiment, planar erosion process
24 433 includes coarse and fine grinding operations on second
25 surface 320 using known techniques until wafer 300 is within
26 the specified range. Subsequent to the grinding process,
27 second surface 320(A) will have a certain amount of stress
28 and defects that are removed in subsequent thinning steps
29 (discussed below).

30 Turning now to Fig. 4(C), after planar erosion is
31 completed, a chemical etchant 435 is applied to second
32 surface 320(B) to further erode second surface 320(B) until

1 wafer 300 has a thickness T2 in the range of 10 to 15 μm .
2 Chemical etchant 435 is applied using equipment specially
3 designed to perform chemical etching at high etch rates
4 while maintaining a high level of uniformity. Such
5 equipment is produced, for example, by SEZ AG of Villach,
6 Austria. Chemical etchant 435 is, for example, HF (50%) and
7 HNO_3 (70%) mixed with a ratio of 1:25 and applied at room
8 temperature. Another suitable chemical etchant 435, which
9 is also sold by SEZ AG, includes HF, HNO_3 , H_3PO_4 and H_2SO_4 .
10 After the chemical etching process, it is important that all
11 organic and grinding residues be removed from lower surface
12 320(B) using known methods. Further, if the roughness of
13 lower surface 320(B) is a concern, an optional
14 chemical/mechanical polishing process may be performed using
15 known techniques to prepare lower surface 320(B) for further
16 processing.

17 Fig. 4(D) illustrates a subsequent step of separating
18 image sensor circuits 100 from each other using techniques
19 disclosed in U.S. Patent No. 5,455,455. In particular,
20 second surface 320 is scribed along predetermined dice lines
21 and then etched using an etchant 437 to separate the
22 individual image sensor circuits 100. A resist coating 436
23 is patterned on wafer 300 over image sensor circuits 100
24 during this separation process, thereby maintaining the
25 thickness T2 of wafer 300 in these regions. Etchant 437 is
26 a conventional semiconductor substrate etching solution,
27 which for silicon may be a combination of 24% potassium
28 hydroxide (KOH), 63% water and 13% isopropanol, so as to
29 etch the silicon down to metal contact pads 330 (i.e., to
30 adhesive layer 420), as shown in Fig. 4(D). The result of
31 wafer etching is a plurality of separated dies 300-1 through
32 300-4 arranged on substrate 410, each of which includes on

1 image sensor circuit 100 and has a thickness (including
2 image sensor circuit 100) in the range of 10 to 15 microns.

3 As mentioned in the background section (above), it is
4 necessary to negatively charge backside surface 320 of each
5 image sensor circuit 100 during operation as a backside
6 illuminated image sensor device. In one optional process
7 step, a metal film is formed over exposed backside surface
8 320 using known techniques that allows the application of
9 the negative bias to control the depletion region during
10 operation. According to another optional process, during
11 fabrication of image sensor circuits 100, a special implant
12 step is performed that is introduced before the source/drain
13 implant activation. This special implant is, for example,
14 As or Sb implanted at 150-400KeV.. While this second
15 optional process adds a step to the fabrication process, it
16 is relatively simple to implement.

17 Figs. 4(E) through 4(I) illustrate process steps
18 associated with the formation of a chip-size package (CSP)
19 for dies 300-1 through 300-4 in accordance with the first
20 embodiment. An alternative packaging process is disclosed
21 below with reference to Figs. 6(A) through 6(H).

22 Fig. 4(E) is a cross-sectional view showing a process
23 of securing a transparent (e.g., glass) substrate 440 onto
24 the second surface 320 of the wafer 300, thereby producing a
25 waferwise sandwich. In particular, transparent substrate
26 440 is bonded over dies 300-1 through 300-4 on the side
27 thereof opposite to protective substrate 410. A layer 430
28 of epoxy is applied on dies 300-1 through 300-4, and then
29 transparent substrate 440 is placed onto epoxy 430. Note
30 that epoxy 430 also fills the interstices between dies 300-1
31 through 300-4, thereby protecting each of the image sensor
32 circuits 100. Accordingly, each die 300-1 through 300-4 is

1 completely surrounded by epoxy layers 420 and 430, and is
2 sandwiched between protective substrate 410 and transparent
3 substrate 440.

4 Figs. 4(F) through 4(I) show process steps associated
5 with the formation of metal leads that are connected to
6 metal contact pads 330 of each image sensor circuit 100 to
7 facilitate signal transmission between each image sensor
8 circuit 100 and an external system (not shown). These metal
9 leads are formed on protective substrate 410, thereby
10 allowing the packaged image sensor circuits 100 to be
11 mounted on, for example, a printed circuit board with
12 transparent substrate 440 facing upward.

13 Note that the structures shown in Figs. 4(F) through
14 4(I) are upside-down relative to Figs. 4(A) through 4(E)
15 (i.e., with transparent layer 440 below dies 300-1 through
16 300-4).

17 Fig. 4(F) is a cross-sectional view showing the
18 formation of compliant layer portions 450, and the
19 subsequent formation of grooves 455 through protective
20 substrate 410 and adhesive layer 420 to expose metal contact
21 pads 330 of that are located along the edges of dies 300-1
22 through 300-4. Grooves 455 separate protective substrate
23 410 into die-sized sections 410-1 through 410-4 that are
24 respectively attached to dies 300-1 through 300-4 via
25 adhesive regions 420-1 through 420-4. Note that dies 300-1
26 through 300-4 remain connected by transparent substrate 440
27 and epoxy 430.

28 Referring to Fig. 4(G), after grooves 455 are formed,
29 metal leads 460 are formed over die-sized sections 410-1
30 through 410-4. Each metal lead 460 extends from an
31 associated compliant layer portion 450 to an associated
32 metal contact pad 330. After the formation of metal leads

17 16

1 460, a solder mask (BCB) 470 is patterned such that a
2 portion of each metal lead 460 located over its associated
3 compliant layer portion 450 is exposed through an opening in
4 solder mask 470.

5 Fig. 4(H) shows the formation of solder bumps 480 using
6 known ball-grid array (BGA) technology. Each solder bump
7 480 is formed on the exposed portion of an associated metal
8 lead 460.

9 Finally, Fig. 4(I) is a cross-sectional view
10 illustrating a dicing process during which the waferwise
11 sandwich is sliced along lines 490 that extend into grooves
12 455, thereby separating die-sized sections 410-1 through
13 410-4 into separate backside-illuminated image sensor
14 devices. The dicing process is performed using known
15 mechanical sawing techniques.

16 A benefit provided by the fabrication process
17 illustrated in Figs. 4(A) through 4(I) is that each of the
18 disclosed process steps is performed using standard wafer
19 processing techniques and equipment. In particular, the
20 disclosed thinning and separating steps can be incorporated
21 into a fabrication process without the need for special
22 bonding technologies, thinning techniques and packaging
23 steps. Therefore, the disclosed fabrication process reduces
24 the complexity, direct cost, cycle time, handling and
25 shipping of back-illuminated CMOS APS devices, thereby
26 providing such devices at a lower cost than conventional
27 back-illuminated CMOS APS devices.

28 Fig. 5 is a simplified cross-section showing a portion
29 of a back-illuminated CMOS image sensor that is produced,
30 for example, in accordance with the method shown in Figs.
31 4(A) through 4(I). In particular, the back-illuminated CMOS
32 image sensor includes a matrix of CMOS APS cells (light-

18 17

1 sensitive pixel regions), including CMOS APS cell 500, that
2 are produced on semiconductor substrate 505. In contrast to
3 prior art APS cell 40(1), APS cell 500 is formed with front
4 surface 310 facing down, and backside surface 320 facing
5 upward (i.e. toward the source of photons). CMOS APS cell
6 500 is formed on first surface 310 of the substrate 505, and
7 includes a photodiode 510 formed by a diffusion region 515
8 extending into substrate 505 from first surface 310.
9 Several metal lines (e.g., metal line 524 connected between
10 diffusion region 515 and polysilicon gate structure 537) are
11 formed in an insulator material (e.g., silicon dioxide) that
12 is located adjacent first surface 310 of substrate 505. A
13 protective substrate 410-1 is secured to semiconductor
14 substrate 505 such that the metal lines are located behind
15 diffusion region 515 (i.e., between protective substrate
16 410-1 and substrate 505). Finally, a transparent substrate
17 440 is secured to second surface 320 of substrate 505 such
18 that substrate 505 is sandwiched between transparent
19 substrate 440 and protective substrate 410-1.

20 In accordance with an aspect of the present invention,
21 substrate 505 is processed by grinding, chemical etching and
22 an optional chemical/mechanical polishing process to have a
23 thickness defined such that light-sensitive pixel region 500
24 is effectively exposed through second surface 320. As
25 discussed above, this effective exposure is achieved by
26 reducing the thickness of substrate 505 to the range of 10
27 to 15 microns.

28 In accordance with another aspect of the present
29 invention, backside illuminated image sensor 500 further
30 comprises a first adhesive layer 420, such as epoxy, that is
31 located between protective substrate 410 and substrate 505,
32 and a second adhesive layer 430 (also epoxy) that is located

1 between transparent substrate 440 and semiconductor
2 substrate 505. By selecting an epoxy with, for example,
3 good optical qualities and a 98% transparency, there is
4 virtually no degradation in the optical performance of image
5 sensor circuits 100.

6 Referring again to Fig. 5, in accordance with another
7 aspect of the present invention, each CMOS APS cell 500 is
8 similar to conventional frontside illuminated CMOS APS cell
9 140(1) (see Fig. 2(B)), in that each CMOS APS cell 500 also
10 includes active circuitry for controlling diffusion 515 of
11 photodiode 510. Diffusion (light sensitive) region 515 is
12 formed as an n-type in p-type substrate 505. Voltage source
13 V_{DD} is applied via voltage source line 523 to a second n-type
14 diffusion region 525 that is spaced from photodiode region
15 515. A first polysilicon gate structure 527 is provided
16 between diffusion region 525 and photodiode region 515 and
17 connected to reset control line 526 to collectively form
18 reset transistor 520. A third n-type diffusion region 535
19 is spaced from second region 525, and second polysilicon
20 gate structure 537 is formed over this space. Photodiode
21 510 is connected to second polysilicon gate 537 by metal
22 line 524 to form source-follower transistor 530. A fourth
23 n-type diffusion region 545 is spaced from third region 535,
24 and a third polysilicon gate structure 547 is formed over
25 this space and connected to row select control line 549 to
26 form select transistor 540. Fourth diffusion region 545 is
27 connected to output terminal 550, which in turn is connected
28 to column data line 555. APS cell 500 is depicted as an n-
29 channel device with electrons as the photo-generated charge
30 carriers. In alternative embodiments (not shown), APS cells
31 may be formed as a p-channel device with holes as the photo-
32 generated charge carriers.

20¹⁹

1 Other than the backside arrangement, discussed above
2 with reference to CMOS APS cell 500, the backside
3 illuminated CMOS image sensor of Fig. 5 is arranged in a
4 manner similar to that of conventional image sensor 100
5 shown in Fig. 1 and includes similar control circuitry (not
6 shown in Fig. 5) and a matrix of CMOS APS cells 500. As
7 such, CMOS APS cell 500 operates substantially in the manner
8 described above with reference to Fig. 2(B), with the
9 exception that the image sensed by APS cell 500 is located
10 on the backside of substrate 505 (i.e., facing second
11 surface ³²⁰~~310~~).

12 Figs. 6(A) through 6(I) illustrate a method of
13 producing backside illuminated image sensors 100 in
14 accordance with a second embodiment of the present
15 invention.

16 Fig. 6(A) is a cross-sectional view showing wafer 300
17 that is pre-fabricated with image sensors 100 formed on
18 first surface 310, and includes metal contact pads 330
19 exposed on first surface 310. As mentioned above, wafer 300
20 has a beginning thickness T0 of 600 to 650 μm .

21 Fig. 6(B) shows the formation of a passivation layer
22 610 on upper surface 310 using known methods. In one
23 embodiment, passivation layer 610 has a thickness in the
24 range of 8500 and 9500 angstroms.

25 Fig. 6(C) illustrates the formation of holes 620 in
26 passivation layer 610 through which metal contact pads 330
27 are exposed. Holes 620 are formed using known techniques.

28 Fig. 6(D) shows the step of attaching a substrate 640
29 to wafer 300 such that passivation layer 610 is sandwiched
30 therebetween. In one embodiment, substrate 640 is glass and
31 has a thickness T61 in the range of 150 to 250 μm .

21²⁰

1 Referring to Fig. 6(E), the process of removing
2 material from second surface 320(A) of wafer 300 begins with
3 a planar erosion process 653 whereby the thickness of wafer
4 300 is reduced to thickness T1, which is in the range of 120
5 to 140 μm . In one embodiment, planar erosion process 633
6 includes coarse and fine grinding operations on second
7 surface 320 using known grinding technologies until wafer
8 300 is within the specified range. In another embodiment,
9 all planar erosion steps may be performed using chemical
10 etching, although this embodiment may not be economical with
11 current technologies.

12 Turning now to Fig. 6(F), after planar erosion is
13 completed, a chemical etchant 655 is then applied to second
14 surface 320(B) to further erode second surface 320(B) until
15 wafer 300 has the thickness T3 in the range of 10 to 15 μm .
16 Suitable chemical etchants 635 are described above with
17 reference to Fig. 4(C), as is equipment suitable for
18 performing the chemical etching process. Unlike the
19 embodiment shown in Figs. 4(A) through 4(I), the present
20 embodiment does not require the scribing and etching step
21 (see description related to Fig. 4(D)).

22 Fig. 6(G) illustrates a step of attaching a glass
23 substrate 660 to second surface 320(B). Glass substrate 660
24 has a thickness of approximately 100 μm , and is attached
25 using substantially transparent epoxy (not shown).

26 Fig. 6(H) illustrates a subsequent step of grinding
27 substrate 640 to a thickness T62 of approximately 50 μm
28 using known grinding technologies. This secondary grinding
29 process provides an extremely thin overall device thickness
30 in the range of 350 to 500 μm .

31 Fig. 6(I) shows the formation of openings through
32 thinned substrate 640, and the formation of solder bumps 670

21
22

1 using known ball-grid array (BGA) technology. The openings
2 formed in substrate 640 are aligned with openings 620
3 through passivation layer 610. Finally, Fig. 6(I) shows a
4 dicing process during which the waferwise sandwich is sliced
5 along lines 680, thereby separating the waferwise sandwich
6 into die-sized sections, each section forming a separate
7 backside-illuminated image sensor device.

8 As with the embodiment shown in Figs. 4(A) through
9 4(I), the second embodiment described above provides a
10 benefit in that the disclosed process steps are performed
11 using standard wafer processing techniques and equipment.

12 Although the invention has been described in connection
13 with several embodiments, it is understood that this
14 invention is not limited to the embodiments disclosed, but
15 is capable of various modifications which would be apparent
16 to a person skilled in the art. For example, in addition to
17 fabricating CMOS APS devices, the disclosed methods may be
18 beneficially utilized to produce backside illuminated CCD
19 image sensors, as well as passive pixel CMOS sensors and
20 other MOS image sensors. Further, the particular parameters
21 set forth in the above examples are exemplary, and may be
22 altered to meet the requirements of particular fabrication
23 processes. Thus, the invention is limited only by the
24 following claims.

23²²

1 **CLAIMS**

2 What Is Claimed Is:

3
4 1. A method of producing backside illuminated image
5 sensors comprising the steps of:

6 producing a plurality of image sensor circuits on a
7 wafer having first and second surfaces each of the image
8 sensor circuits being formed on the first surface and
9 including a matrix of light-sensitive pixel regions
10 extending into the wafer from the first surface;

11 securing the wafer onto a protective substrate such
12 that the first surface faces the protective substrate;

13 removing material from the second surface of the wafer
14 until the light-sensitive pixel regions of each image sensor
15 circuit are effectively exposed through the second surface;

16 securing a transparent substrate onto the second
17 surface of the wafer, thereby producing a waferwise
18 sandwich; and

19 slicing the waferwise sandwich, thereby defining a
20 plurality of backside illuminated image sensors.

21
22 2. The method according to Claim 1, wherein the step
23 of securing the protective layer onto the first surface
24 comprises depositing an adhesive onto the protective
25 substrate, and then placing the wafer onto the protective
26 substrate such that the first surface contacts the deposited
27 adhesive.

28
29
30 3. The method according to Claim 1, wherein the step
31 of removing material from the wafer comprises:

32 grinding the second surface until a thickness of each

24²³

1 image sensor circuit is in the range of 120 to 140 microns;
2 and

3 etching the second surface until a thickness of each
4 image sensor circuit is in the range of 10 to 15 microns.

5

6 4. The method according to Claim 3, wherein the step
7 of etching comprises:

8 scribing the second surface along predetermined dice
9 lines located between the plurality of image sensor
10 circuits; and

11 applying an etching solution to the second surface to
12 expose metal contact pads located on the first surface of
13 the wafer.

14

15 5. The method according to Claim 1, wherein the step
16 of removing material from the wafer comprises:

17 performing a first etching process on the second planar
18 surface, and

19 performing a second etching process on the second
20 surface to separate the image sensor circuits from each
21 other so as to define edges thereof.

22

23 6. The method according to Claim 5, wherein the step
24 of performing the second etching process comprises:

25 scribing the second surface along predetermined dice
26 lines located between the plurality of image sensor
27 circuits; and

28 applying an etching solution to the second surface to
29 expose metal contact pads located on the first surface of
30 the wafer.

31

32 7. The method according to Claim 1, wherein the step

1 of securing a transparent substrate onto the second surface
2 comprises depositing an adhesive onto the second surface,
3 and then placing the transparent substrate onto the
4 deposited adhesive.

5
6 8. The method according to Claim 7,
7 wherein the step of removing material includes
8 separating each of the plurality of image sensor circuits;
9 and

10 wherein the step of depositing the adhesive onto the
11 second surface further comprises depositing adhesive into
12 interstices located between the plurality of image sensor
13 circuits, thereby protecting the image sensor circuits.

14
15 9. The method according to Claim 1, further
16 comprising the step of forming metal leads on the protective
17 substrate after the step of securing the transparent
18 substrate, wherein the metal leads are connected to metal
19 contact pads located on the first surface of the wafer.

20
21 10. The method according to Claim 1, wherein the step
22 of securing the wafer onto a protective substrate further
23 comprises:
24 forming a passivation layer on the first surface of the
25 wafer;
26 forming openings in the passivation layer; and
27 securing the protective substrate onto the passivation
28 layer.

29
30 11. The method according to Claim 1, further
31 comprising, after the step of securing the transparent
32 substrate, grinding the protective substrate until the

1 ~~protective substrate has a thickness of 50 microns.~~

2

3 1. A backside illuminated image sensor comprising:
4 a semiconductor substrate having a first surface and a
5 second surface;

6 a plurality of light-sensitive pixel regions formed on
7 the first surface of the semiconductor substrate and
8 including a photodiode diffusion region extending into the
9 semiconductor substrate from the first surface;

10 a metal line formed adjacent the first surface of the
11 semiconductor substrate;

12 a protective substrate secured to the semiconductor
13 substrate such that the metal line is located between the
14 protective substrate and the semiconductor substrate; and

15 a transparent substrate secured to the second surface
16 of the semiconductor substrate such that the semiconductor
17 substrate is sandwiched between the transparent substrate
18 and the protective substrate;

19 wherein the semiconductor substrate has a thickness
20 defined such that the light-sensitive pixel region is
21 effectively exposed through the second surface.

22

23 2. The backside illuminated image sensor according to
24 Claim 1, further comprising a first adhesive layer located
25 between the protective substrate and the semiconductor
26 substrate, and a second adhesive layer located between the
27 transparent substrate and the semiconductor substrate.

28

29 3. The back-illuminated image sensor according to
30 Claim 2, wherein each of the plurality of light-sensitive
31 pixel regions further comprises:

1 a second diffusion region that is formed in the
2 semiconductor substrate and spaced from the photodiode
3 diffusion region;

4 a first polysilicon gate structure provided between the
5 second diffusion region and the photodiode diffusion region;

6 a third diffusion region that is formed in the
7 semiconductor substrate and spaced from the second diffusion
8 region;

9 a second polysilicon gate structure that is provided
10 between the second diffusion region and the third diffusion
11 region;

12 a fourth diffusion region that is formed in the
13 semiconductor substrate and spaced from third diffusion
14 region;

15 a third polysilicon gate structure that is provided
16 between the third diffusion region and the fourth diffusion
17 region; wherein the photodiode region is connected to the
18 second polysilicon gate by a first metal line to form a
19 source-follower transistor, and wherein the first metal line
20 is located between the semiconductor substrate and the
21 protective substrate.

22 ^{4.}
23 ^{15.} The backside illuminated image sensor according to
24 Claim 12, wherein the thickness of the semiconductor
25 substrate is in the range of 10 to 15 microns.

26 ^{5.}
27 ^{16.} The backside illuminated image sensor according to
28 Claim 12, wherein the transparent substrate is glass.

29 ^{6.}
30 ^{17.} The backside illuminated image sensor according to
31 Claim 12, further comprising a plurality of metal leads
32 formed on the protective layer.

1 BACKSIDE ILLUMINATED IMAGE SENSOR

2
3 Yacov Malinovich

4 Ephie Koltin

5
6
7 ABSTRACT OF THE DISCLOSURE

8 A method for producing a back-illuminated CMOS image
9 sensor including a matrix of pixels (e.g., CMOS APS cells)
10 that are fabricated on a semiconductor substrate. The
11 semiconductor substrate is secured to a protective substrate
12 by an adhesive such that the processed (frontside) surface
13 of the semiconductor substrate faces the protective
14 substrate. With the protective substrate providing
15 structural support, the exposed backside surface of the
16 semiconductor substrate is then subjected to grinding and/or
17 chemical etching, followed by optional chemical/mechanical
18 processing, to thin the semiconductor substrate to a range
19 of 10 to 15 microns. A transparent substrate (e.g., glass)
20 is then secured to the backside surface of the semiconductor
21 substrate, thereby sandwiching the semiconductor substrate
22 between the transparent substrate and the protective
23 substrate.

COMBINED DECLARATION AND POWER OF ATTORNEY

(ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL, DIVISIONAL,
CONTINUATION, OR C-I-P)

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is for an original application.

INVENTORSHIP IDENTIFICATION

My residence, post office address and citizenship are as stated below, next to my name. I believe that I am the original, first and sole inventor (*if only one name is listed below*) or an original, first and joint inventor (*if plural names are listed below*) of the subject matter that is claimed, and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

"Backside Illuminated Image Sensor"

SPECIFICATION IDENTIFICATION

The specification is attached hereto.

ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in 37, Code of Federal Regulations, § 1.56, and which is material to the examination of this application, namely, information where there is a substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent, and in compliance with this duty, there is attached an information disclosure statement, in accordance with 37 CFR 1.98.

(Declaration and Power of Attorney—page 1 of 3)

Practitioner's Docket No. TSL-008

PATENT

POWER OF ATTORNEY

I hereby appoint the following practitioner(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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(Declaration and Power of Attorney—page 2 of 3)

Practitioner's Docket No. TSL-008

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ASSIGNMENT OF INVENTION

In consideration of the payment by ASSIGNEE to ASSIGNOR of the sum of One Dollar (\$1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration,

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(Assignment of Invention—page 1 of 2)

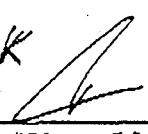
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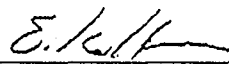

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TOWER, MIGDAL HAEMEK

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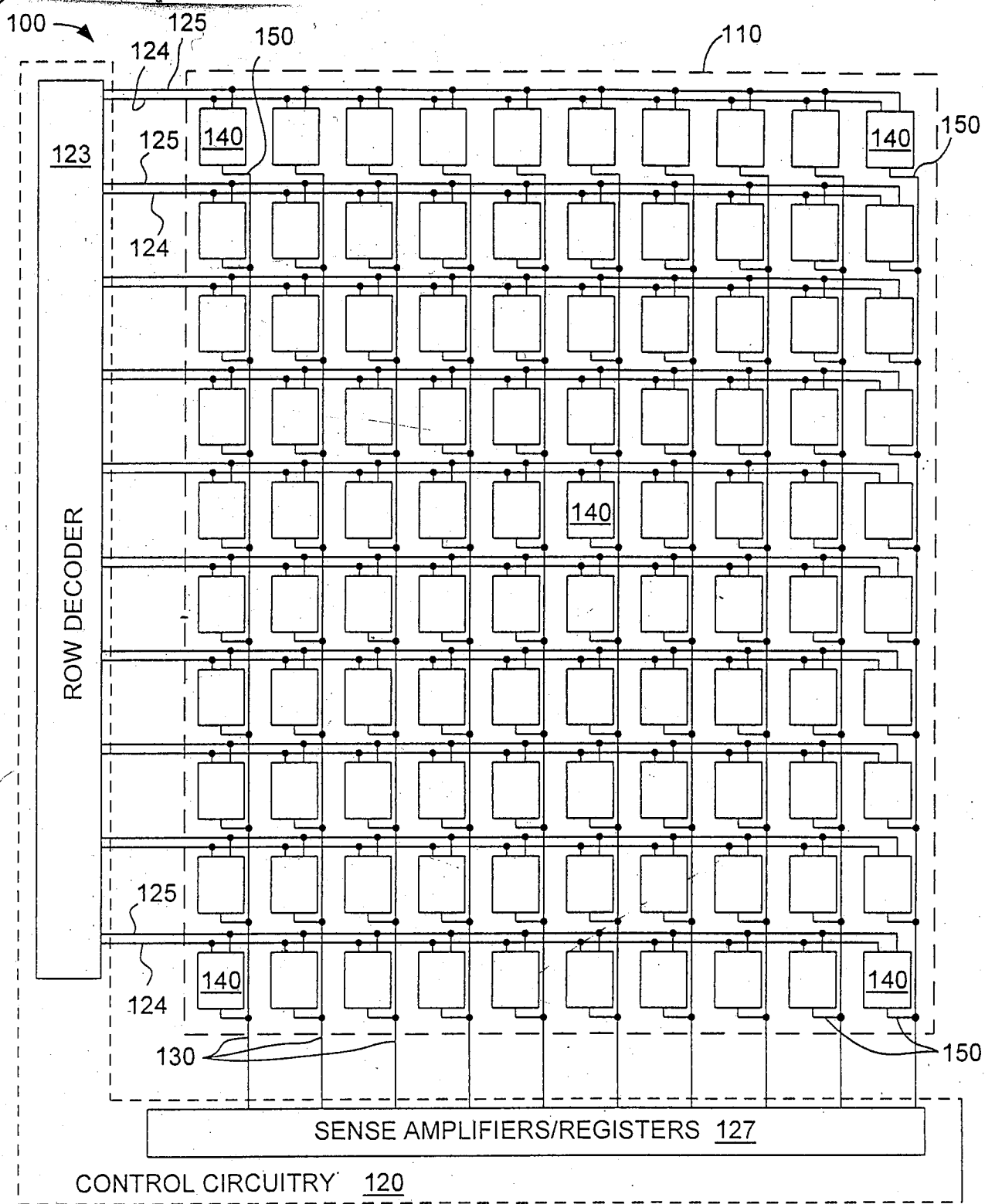


FIG. 1

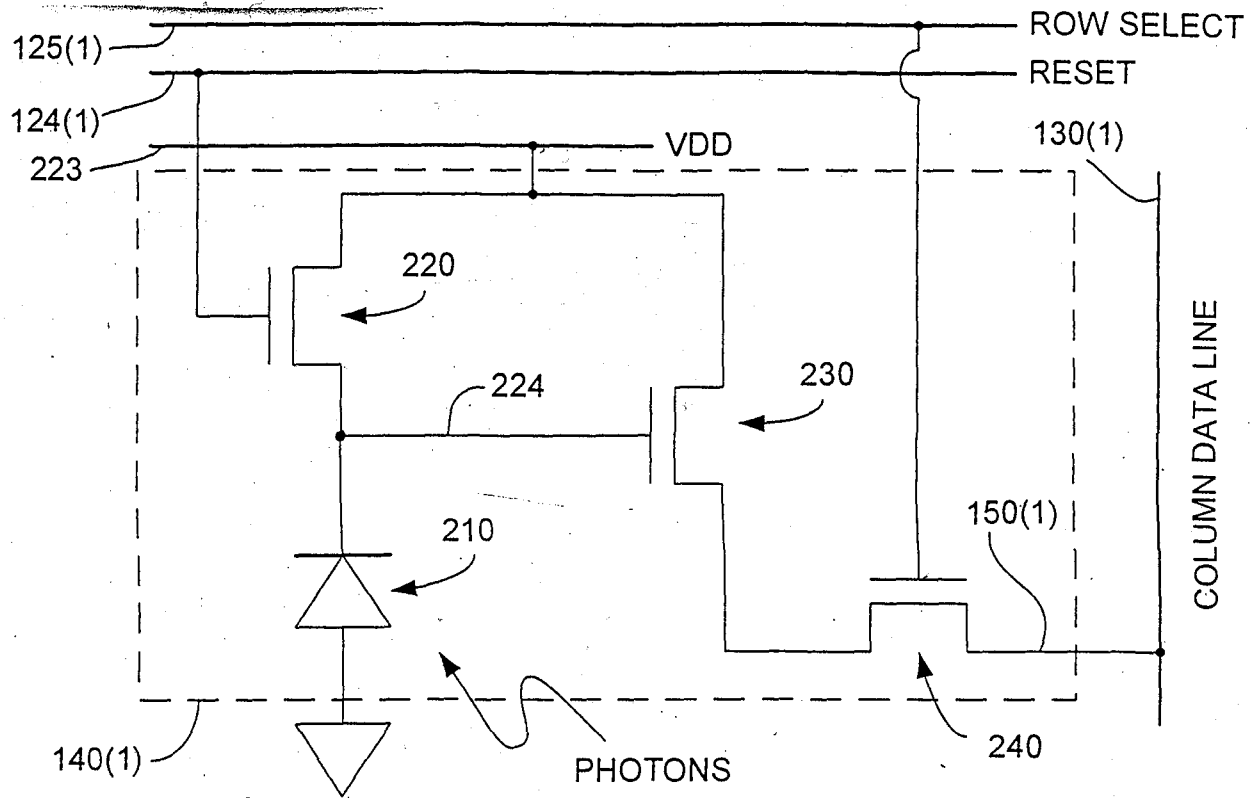


FIG. 2(A) (PRIOR ART)

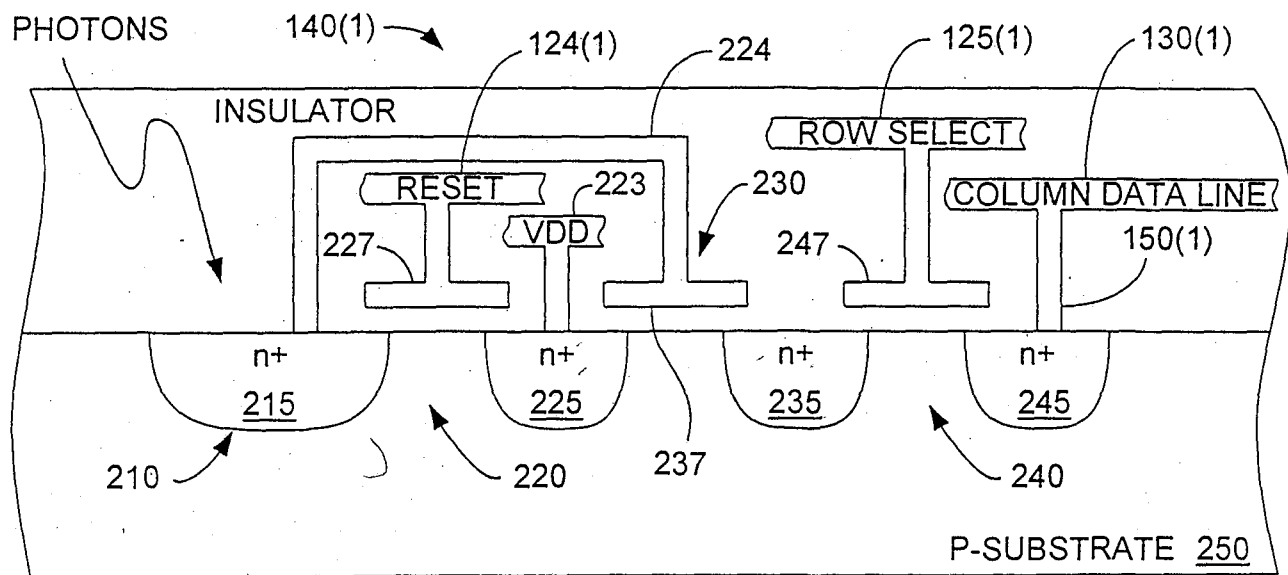


FIG. 2(B) (PRIOR ART)

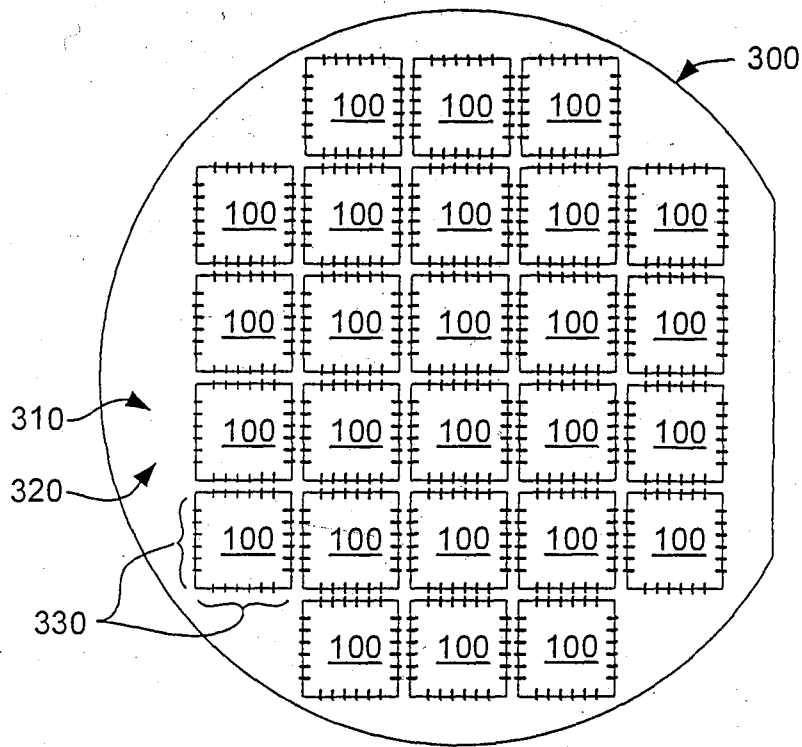


FIG. 3(A)

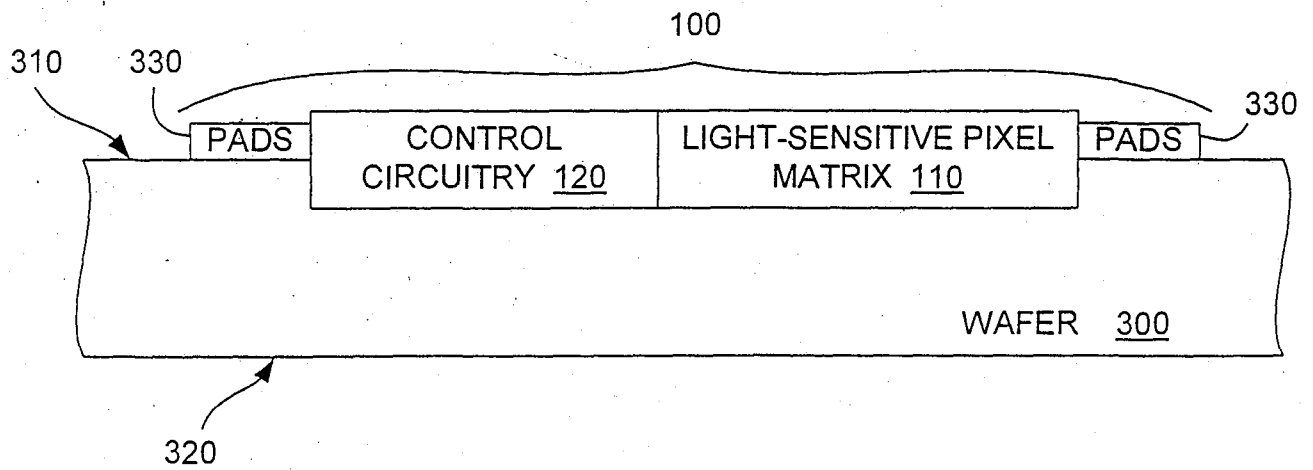


FIG. 3(B)

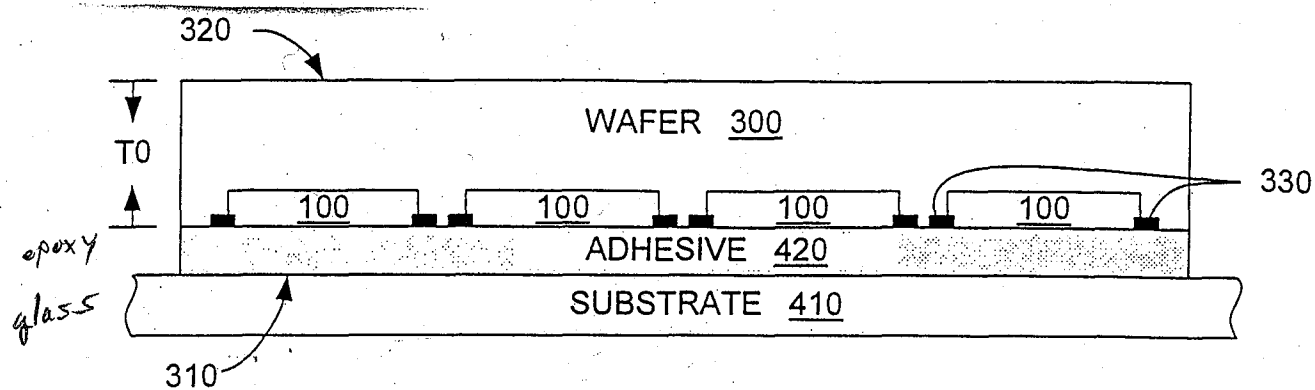


FIG. 4(A)

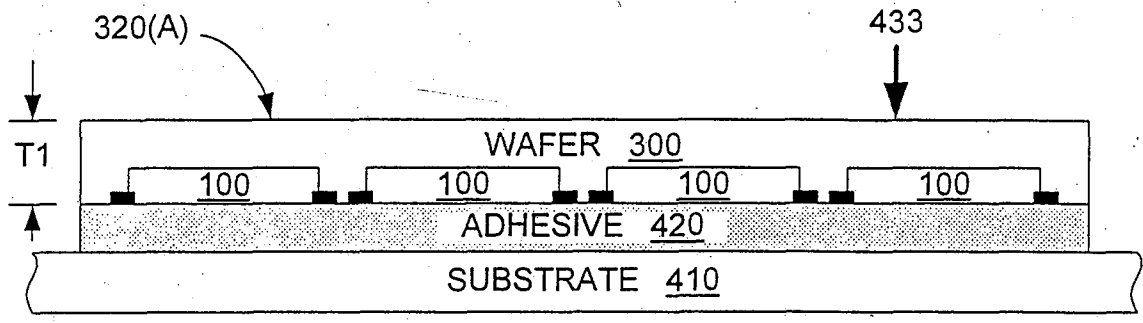


FIG. 4(B)

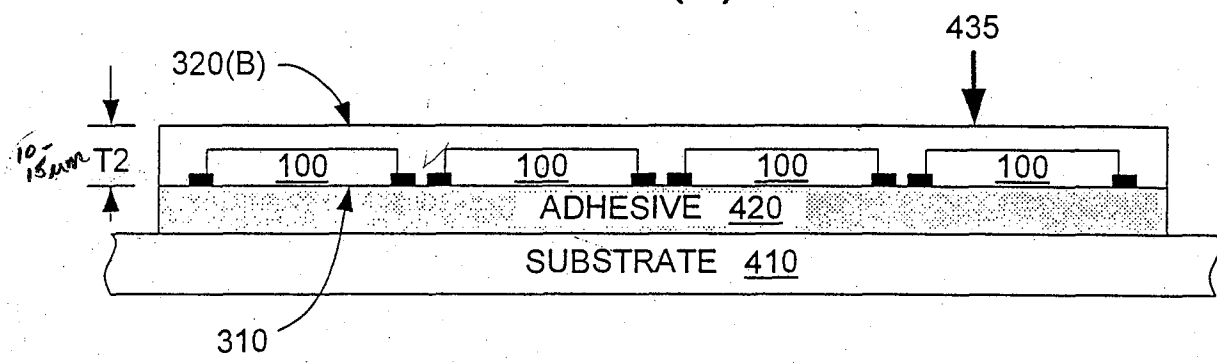


FIG. 4(C)

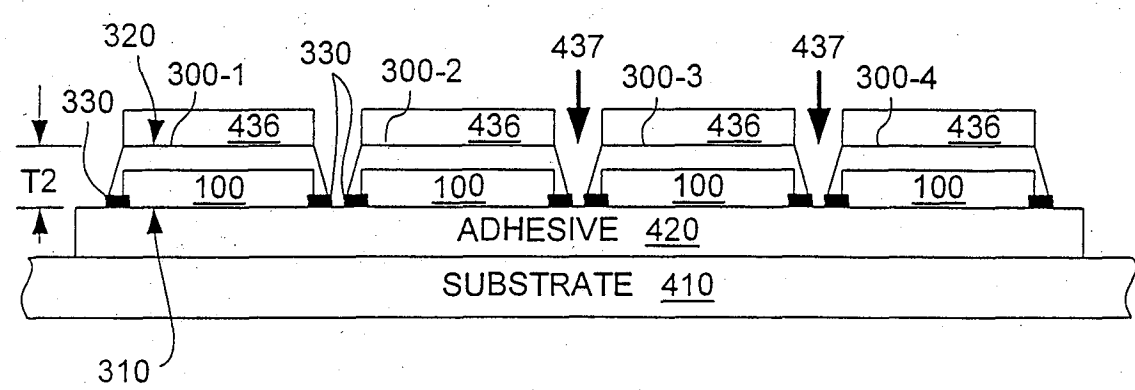


FIG. 4(D)

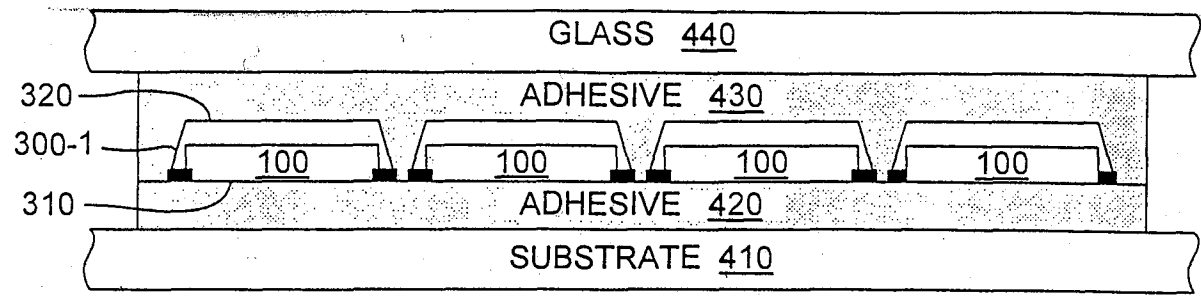


FIG. 4(E)

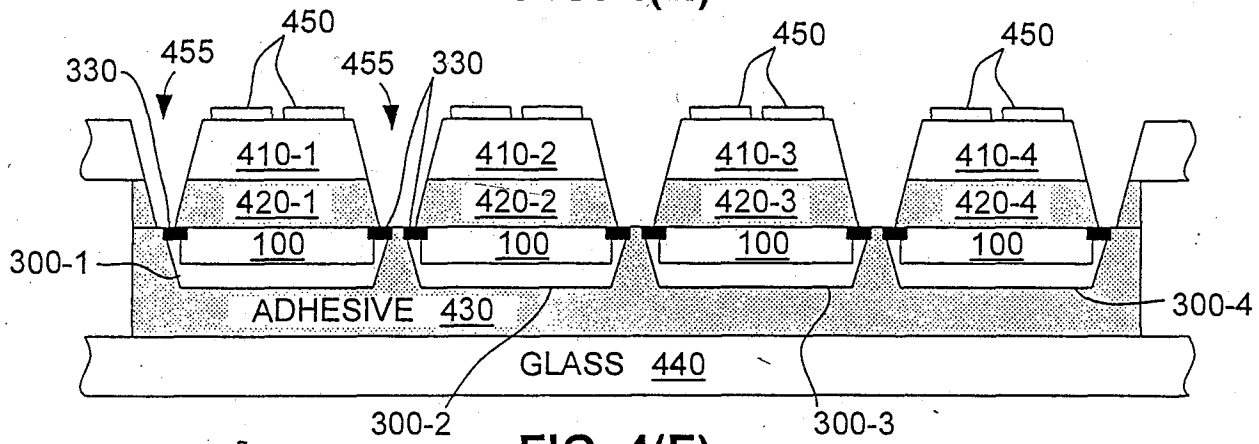


FIG. 4(F)

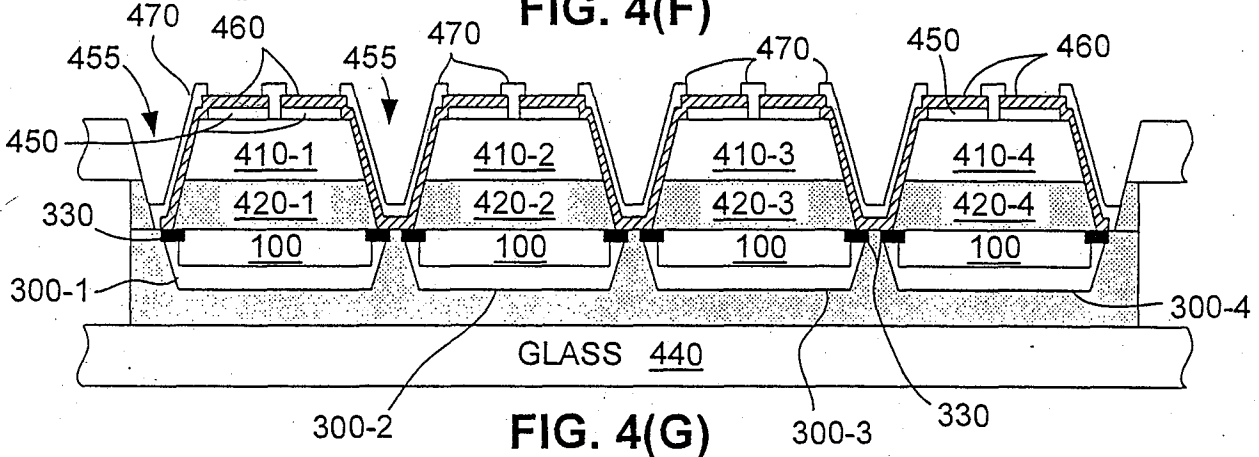


FIG. 4(G)

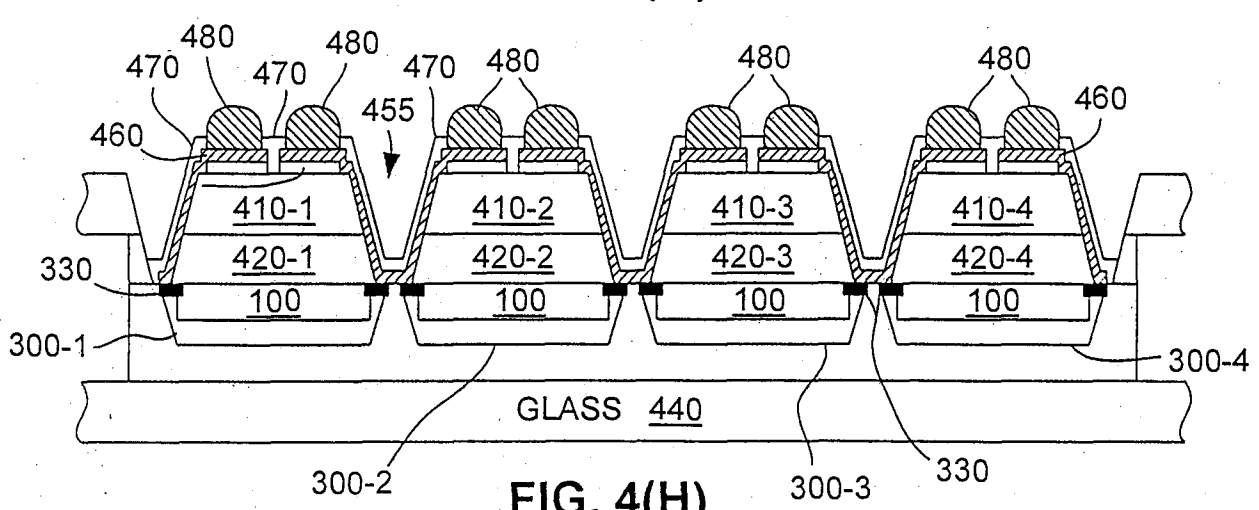


FIG. 4(H)

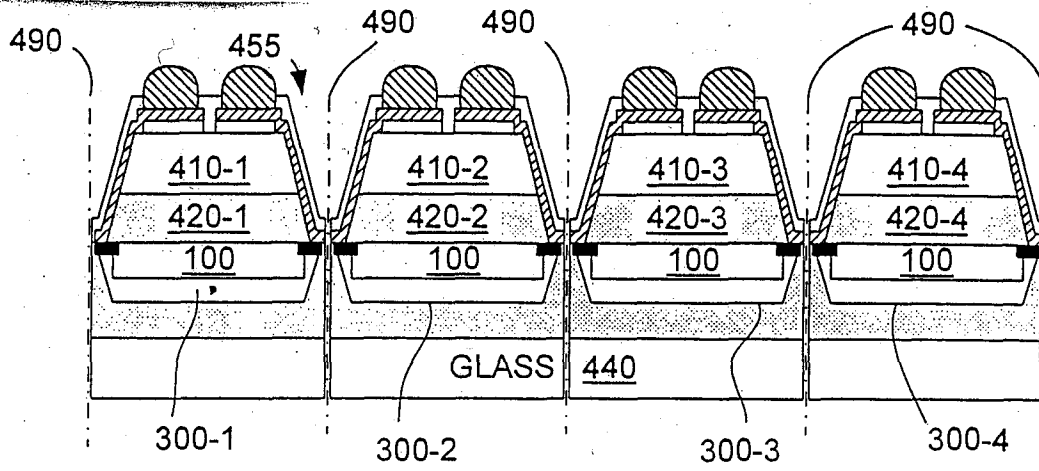


FIG. 4(I)

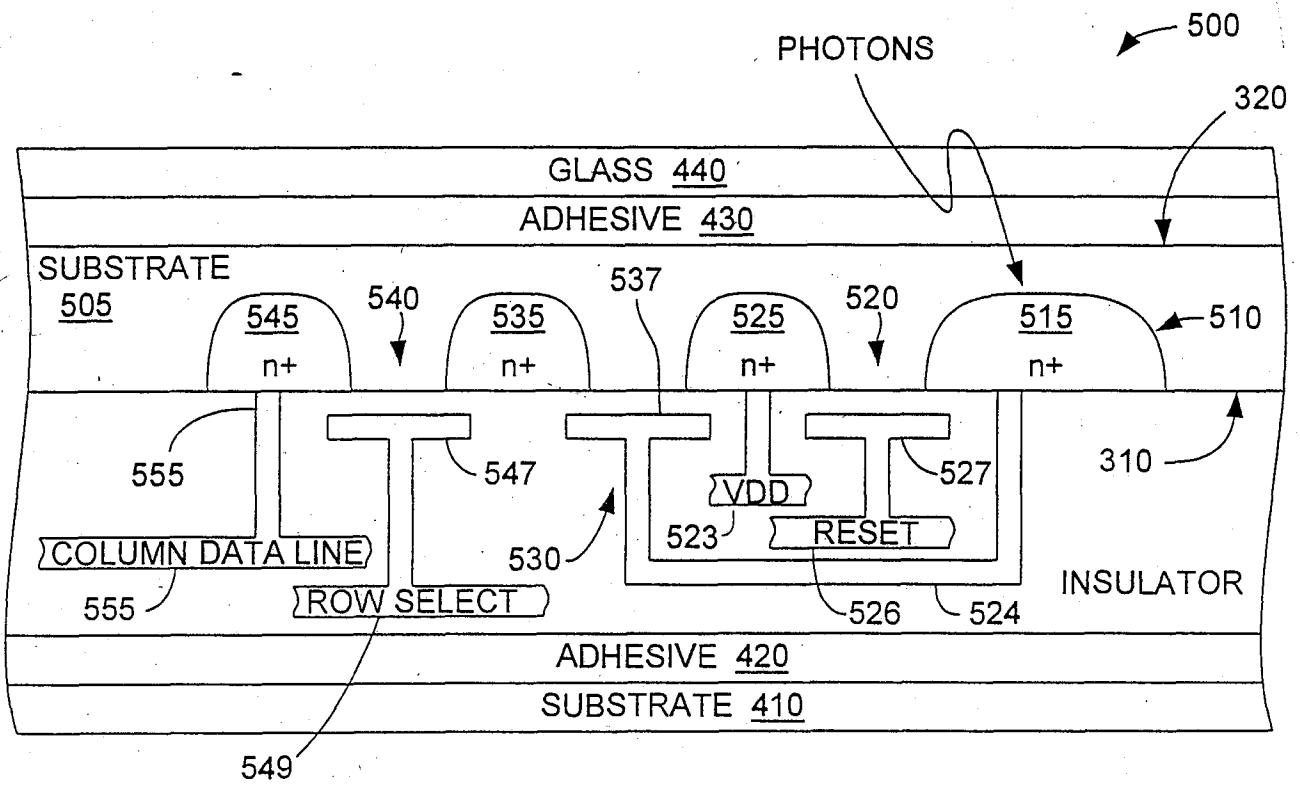


FIG. 5

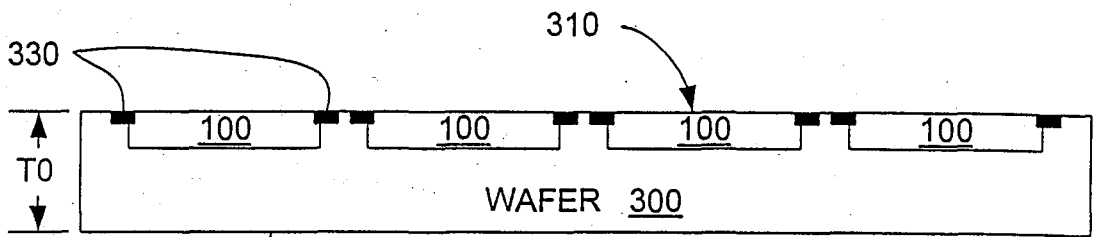


FIG. 6(A)

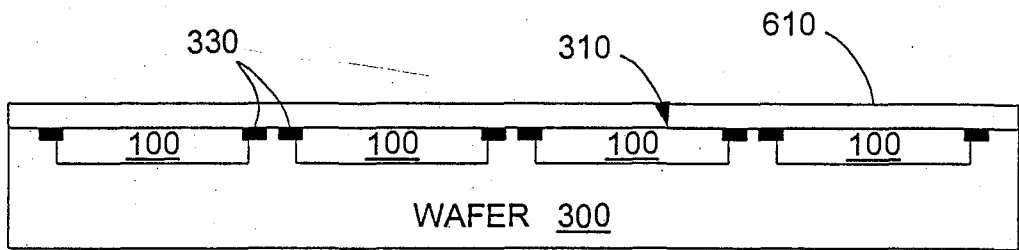


FIG. 6(B)

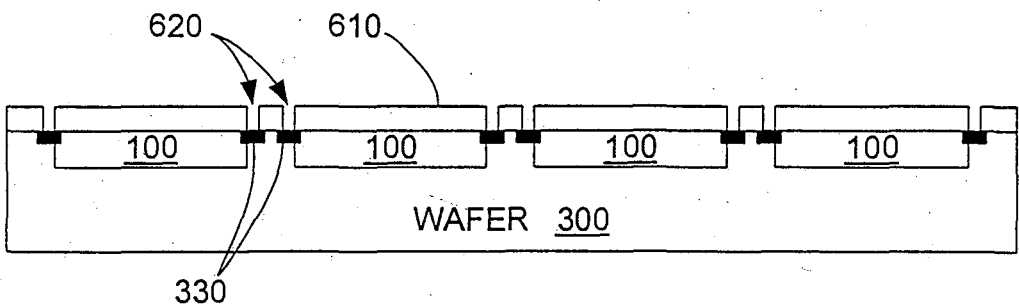


FIG. 6(C)

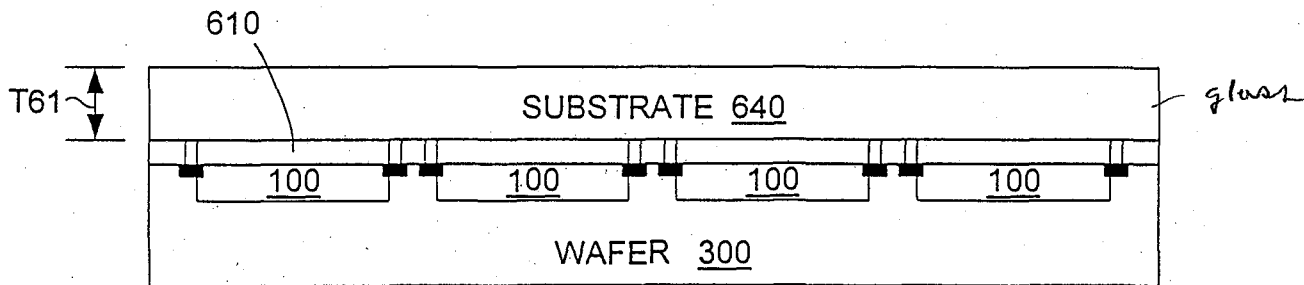


FIG. 6(D)

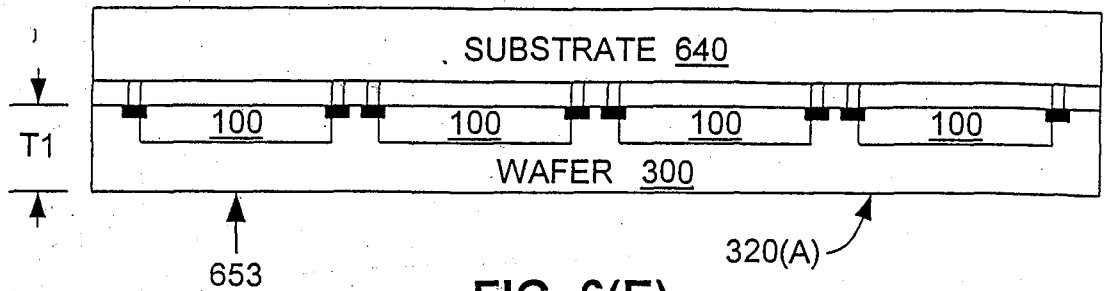


FIG. 6(E)

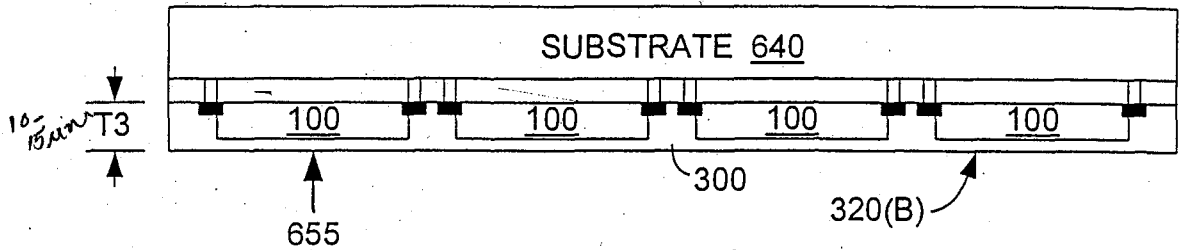


FIG. 6(F)

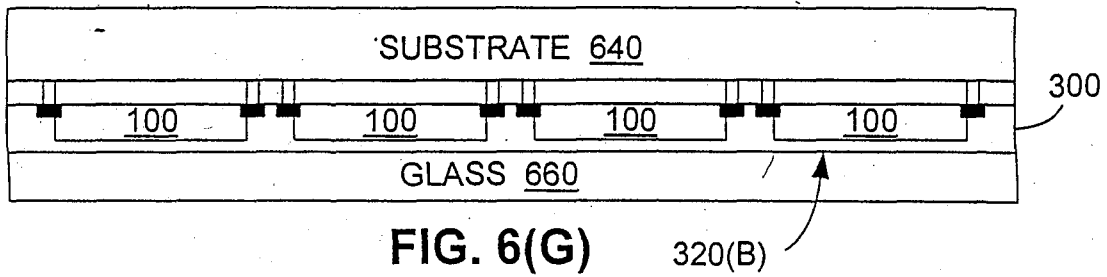


FIG. 6(G)

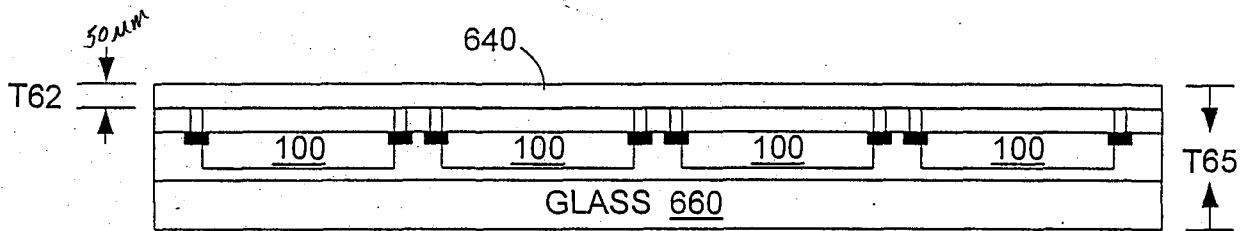


FIG. 6(H)

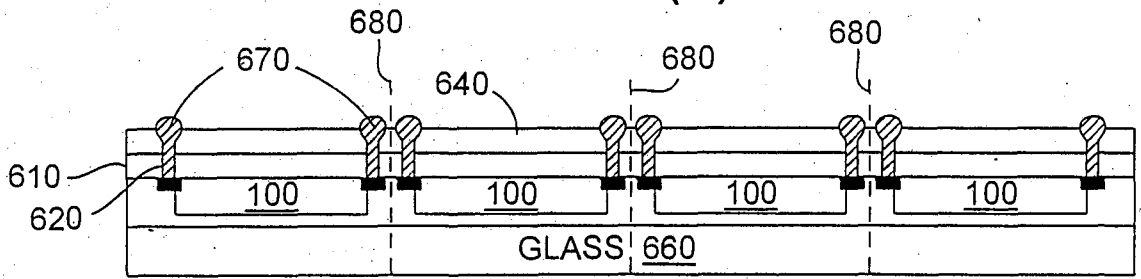


FIG. 6(I)

TSL-008 US
09/372,863

3 2 72-00
PB
PATENT
PRE. Anst. A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Yacov Malinovich, Ephie Koltin
Assignee: Tower Semiconductor, Ltd.
Title: "Backside Illuminated Image Sensor"
Serial No.: Not Yet Assigned Filed: Herewith
Attorney Docket No.: TSL-008-1D US

San Jose, California

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

PRELIMINARY AMENDMENT

Sir:

IN THE CLAIMS

Please delete Claims 1-11.

REMARKS

The present divisional application is filed in response to a Restriction Requirement filed in parent U.S. application serial no. 09/372,863. Claims 1-11 are hereby canceled from the above-identified divisional application, thereby leaving Claims 12-17 pending.

Should the Examiner have any questions regarding this application, the Examiner is invited to contact the undersigned attorney.

Respectfully submitted,



Patrick T. Bever
Attorney for Applicants
Reg. No. 33,834
408-451-5902

PTO - 1449 CHECKLIST

Serial No.

09/441766

Examiner:

Pho my

Date to Examiner:

2-18-00

For each considered document, both the month and year **MUST** be provided - no exceptions. Class and subclass data **MUST** either be provided or the space lined through. The Examiners name and the date the disclosure citation was considered **MUST** be provided at the bottom of the PTO 1449.

CHECK OFF THE FOLLOWING ITEMS AS COMPLETED

For each citation considered:

1. ☐ Initials inserted in left-hand column for each citation considered

2. ☐ Month ☐ Year - inserted in appropriate box (if unavailable, citation is incomplete - go to item 4)

3. ☐ Class ☐ Subclass - inserted in appropriate box (if unavailable, citation is still proper, but you **MUST** draw a line through each blank space)

For each citation not considered or incomplete:

4. ☐ Citation lined through if not considered or incomplete

At bottom of PTO 1449:

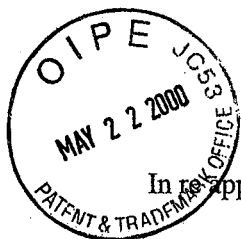
5. ☐ Examiner's name in appropriate place

6. ☐ Enter the date citations were considered in the appropriate place

2877

Practitioner's Docket No. TSL-008-1D

PATENT



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Yacov Malinovich et al.

Application No.: 09/441,766

Group No.: 2877

Filed: 11/17/1999

Examiner: unknown

For: "Backside Illuminated Image Sensor"

Date: May 12, 2000

Assistant Commissioner for Patents
Washington, D.C. 20231

**TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT
WITHIN THREE MONTHS OF FILING OR
BEFORE MAILING OF FIRST OFFICE ACTION (37 C.F.R. 1.97(b))**

**IDENTIFICATION OF TIME OF FILING THE ACCOMPANYING
INFORMATION DISCLOSURE STATEMENT**

The information disclosure statement submitted herewith is being filed within three months of the filing date of the application or date of entry into the national stage of an international application or before the mailing date of a first Office action on the merits, whichever event occurs last. 37 C.F.R. 1.97(b).

SIGNATURE OF PRACTITIONER

Reg. No. 33,834
Tel. No.: (408) 451-5902

Patrick T. Bever
BEVER, HOFFMAN & HARMS, LLP
2099 Gateway Place, Suite 320
San Jose, CA 95110-1017

Customer No.: 022888

I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231-0001, on May 12, 2000.

Date: May 12, 2000 Signature: Patrick T. Bever

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TC 2800 MAIL ROOM

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**UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231 TSL-008-1D

441,766 09/441,766

11/17/99

MALINOVICH

APPLICATION NUMBER

FILING DATE

FIRST NAMED APPLICANT

ATTORNEY DOCKET NO.

022888

MMC1/0829

BEVER HOFFMAN & HARMS, LLP
2099 GATEWAY PLACE
SUITE 320
SAN JOSE CA 95110-1017

MUNSON, G

EXAMINER

2811

ART UNIT

PAPER NUMBER

08/25/00
5/8

DATE MAILED:

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to preliminary amendment filed 17 November 1999

☒ The allowed claim(s) is/are 12-17

☐ The drawings filed on _____ are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR REPLY to comply with the requirements noted below is set to EXPIRE **THREE MONTHS** FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☒ Applicant MUST submit NEW FORMAL DRAWINGS

☐ because the originally filed drawings were declared by applicant to be informal.

☒ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any reply to this notice should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 2, 4

☒ Notice of Draftperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☒ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☐ Examiner's Statement of Reasons for Allowance

Gene M. Munson
GENE M. MUNSON
EXAMINER

09/44/766

NOTICE OF DRAFTSPERSON'S
PATENT DRAWING REVIEWThe drawing(s) filed (insert date) 11/17/99 are:A. ☐ approved by the Draftsperson under 37 CFR 1.84 or 1.152.B. ☒ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be submitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a). Acceptable categories of drawings:
Black ink. Color drawings are not acceptable until petition is granted.
Fig(s)
Pencil and non-black ink not permitted. Fig(s)
2. PHOTOGRAPHS. 37 CFR 1.84(b)
1 full-tone set is required. Fig(s)
Photographs not properly mounted (must use bristol board or photographic double-weight paper). Fig(s)
Poor quality (half-tone). Fig(s)
3. TYPE OF PAPER. 37 CFR 1.84(e)
Paper not flexible, strong, white, and durable. Fig(s)
Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s)
Mylar, velum paper is not acceptable (too thin). Fig(s)
4. SIZE OF PAPER. 37 CFR 1.84(f). Acceptable sizes:
21.0 cm by 29.7 cm (DIN size A4)
21.6 cm by 27.9 cm (8 1/2 x 11 inches)
All drawing sheets not the same size.
Sheet(s)
Drawings sheets not an acceptable size. Fig(s)
5. MARGINS. 37 CFR 1.84(g). Acceptable margins:
Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
SIZE: A4 Size
Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
SIZE: 8 1/2 x 11
Margins not acceptable. Fig(s)
Top (T) Left (L)
Right (R) Bottom (B)
6. VIEWS. 37 CFR 1.84(h)
REMINDER: Specification may require revision to correspond to drawing changes.
Partial views. 37 CFR 1.84(h)(2)
Brackets needed to show figure as one entity. Fig(s)
Views not labeled separately or properly. Fig(s)
Enlarged view not labeled separately or properly. Fig(s)
7. SECTIONAL VIEWS. 37 CFR 1.84(h)(3)
Hatching not indicated for sectional portions of an object. Fig(s)
Sectional designation should be noted with Arabic or Roman numbers. Fig(s)
8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(f)
Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s)
9. SCALE. 37 CFR 1.84(k)
Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s)
10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(i)
Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality). Fig(s)
Solid black areas pale. Fig(s)
Solid black shading not permitted. Fig(s)
Shade tints, pale, rough and blurred. Fig(s)
11. SHADING. 37 CFR 1.84(m)
Shade tints, pale, rough and blurred. Fig(s)
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)
Numbers and reference characters not plain and legible. Fig(s)
Figure legends are poor. Fig(s)
Numbers and reference characters not oriented in the same direction as the view. Fig(s)
English alphabet not used. 37 CFR 1.84(p)(2) Fig(s)
Numbers, letters and reference characters must be at least 32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig(s)
13. LEAD LINES. 37 CFR 1.84(q)
Lead lines cross each other. Fig(s)
Lead lines missing. Fig(s)
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s)
15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s)
16. CORRECTIONS. 37 CFR 1.84(w)
Corrections not made from prior PTO-948 dated
17. DESIGN DRAWINGS. 37 CFR 1.152
Surface shading shown not appropriate. Fig(s)
Solid black shading not used for color contrast. Fig(s)

COMMENTS

REVIEWER DATE 12/28/99TELEPHONE NO. 308-0011ATTACHMENT TO PAPER NO. 5

Y. MALINOVICH ET AL

257/228, 291, 292, 447, 460

G. MUNSON

2817

Page 1 of 1

*	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
✓ A	5,134,274	7/92	POOLE ET AL	257	447
✓ B	5,598,016	1/97	TANABE ET AL	257	228
C					
D					
E					
F					
G					
H					
I					
J					
K					
L					
M					

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
	N						
	O						
	P						
	Q						
	R						
	S						
	T						

*		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	U		
	V		
	W		
	X		

Part of Paper No.

TSMC EX. 1002 Page 59 of 77



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

022888
BEVER HOFFMAN & HARMS, LLP
2099 GATEWAY PLACE
SUITE 320
SAN JOSE CA 95110-1017

MMC1/0829

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/441,766	11/17/99	006	MUNSON, G	2811 08/29/00
First Named Applicant	MALINOVICH,	35 USC 154(b) term ext. = 0 Days.		

TITLE OF INVENTION BACKSIDE ILLUMINATED IMAGE SENSOR

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
3 TSL-008-1D	257-447.000	R44	UTILITY	NO	\$1210.00	11/29/00

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

- Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:
 - If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
 - If the status is the same, pay the FEE DUE shown above.
- If the SMALL ENTITY is shown as NO:
 - Pay FEE DUE shown above, or
 - File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.
- Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.
- All communications regarding this application must give application number and batch number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

PTOL-85 (REV. 10-96) Approved for use through 06/30/99. (0651-0033)



Practitioner's Docket No.: TSL-008-1D

#667

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of (1st Inventor): Yacov Malinovich
Assignee: Tower Semiconductor Ltd.
Serial No.: 09/441,766 Group No.: 2811
Filed: 11/17/1999 Examiner: G. Munson
For: "Backside Illuminated Image Sensor"

Date: November 10, 2000

Assistant Commissioner for Patents
Box Issue Fee
Washington, D.C. 20231-0001

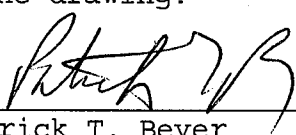
TRANSMITTAL OF FORMAL DRAWINGS

In response to the Notice of Allowance mailed on August 29, 2000,
attached please find:

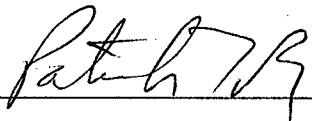
(a) corrected formal drawings for this application - Number of Sheets: 3

Each sheet of drawing indicates the identifying indicia suggested
in Section 1.84(c) on the reverse side of the drawing.

BEVER, HOFFMAN & HARMS, LLP
2099 Gateway Place, Suite 320
San Jose, CA 95110-1017
Tel.: (408) 451-5902
Fax: (408) 451-5908


Patrick T. Bever
Reg. No. 33,834

I hereby certify that this correspondence is being deposited with the United States
Postal Service as FIRST CLASS MAIL in an envelope addressed to: Assistant Commissioner
of Patents, Box Issue Fee, Washington, D.C. 20231-0001, on November 10, 2000.

Date: 11-10-2000 Signature: 

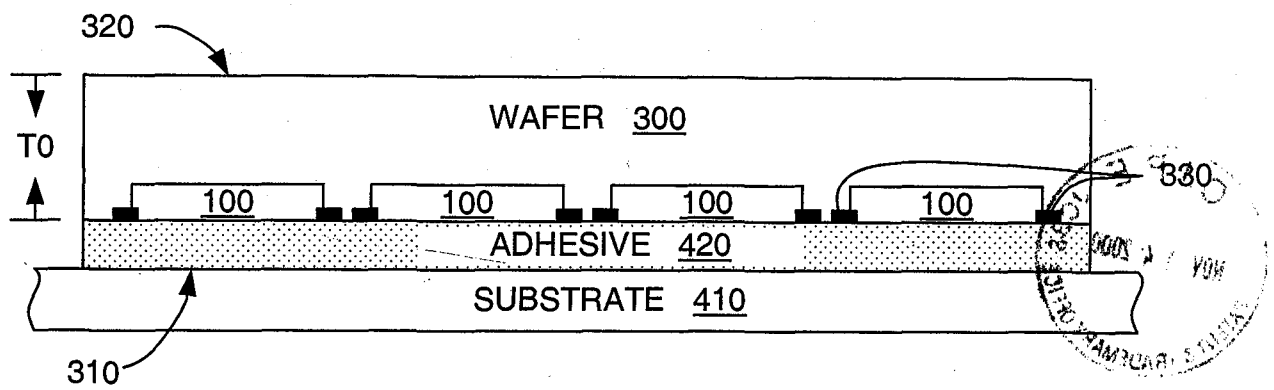


FIG. 4(A)

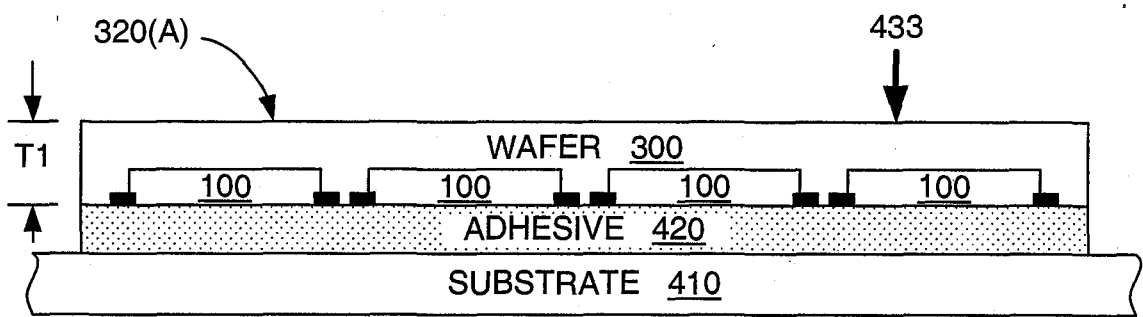


FIG. 4(B)

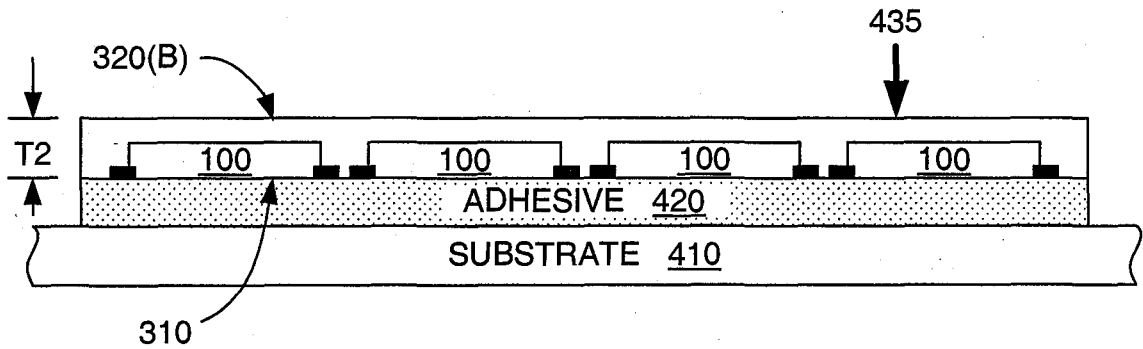


FIG. 4(C)

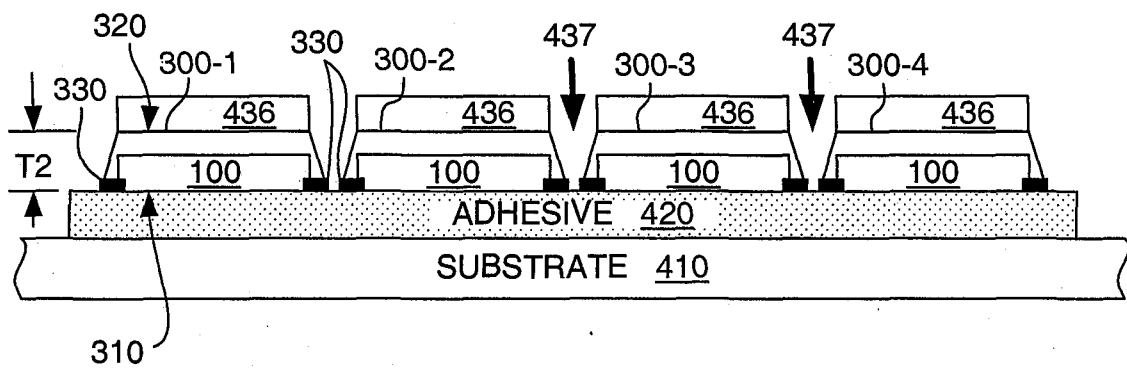


FIG. 4(D)

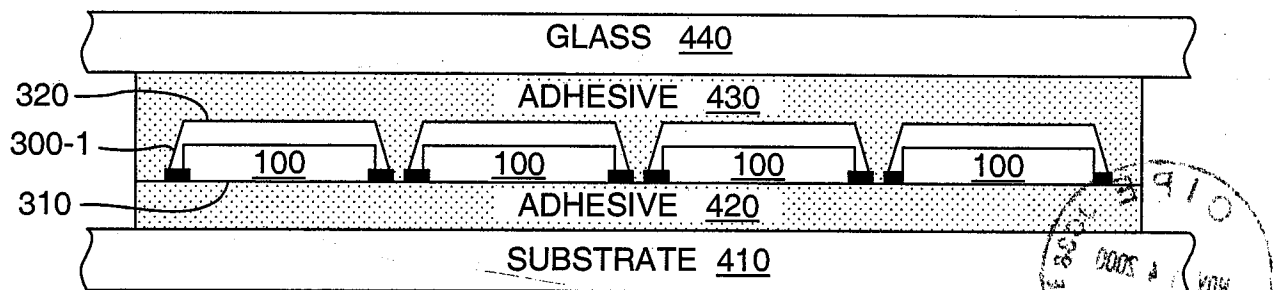


FIG. 4(E)

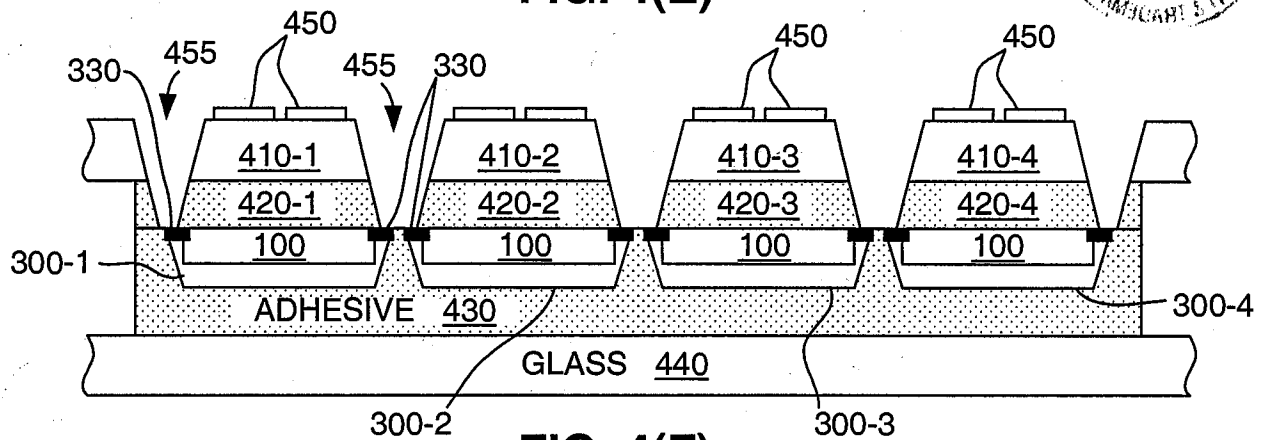


FIG. 4(F)

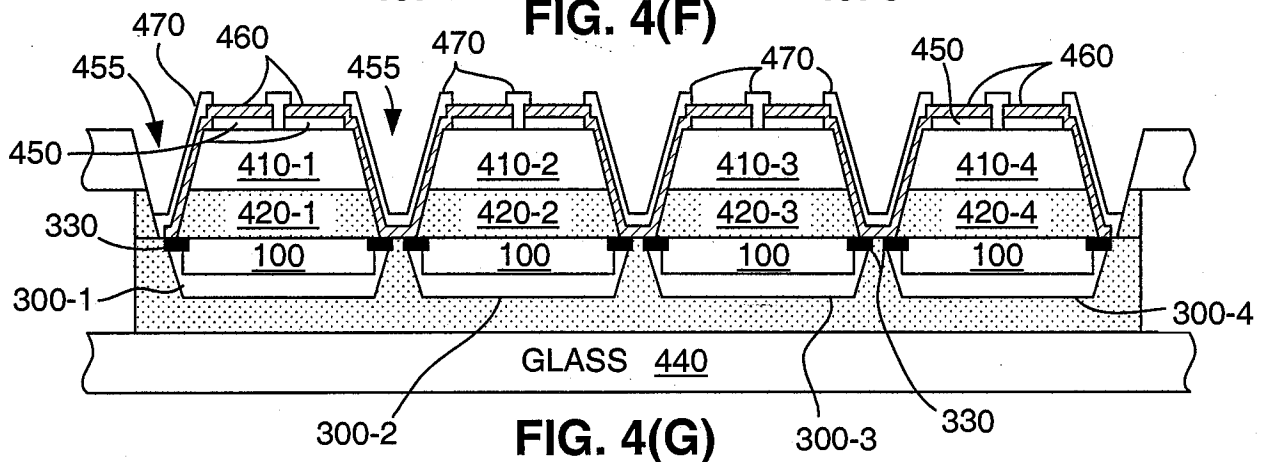


FIG. 4(G)

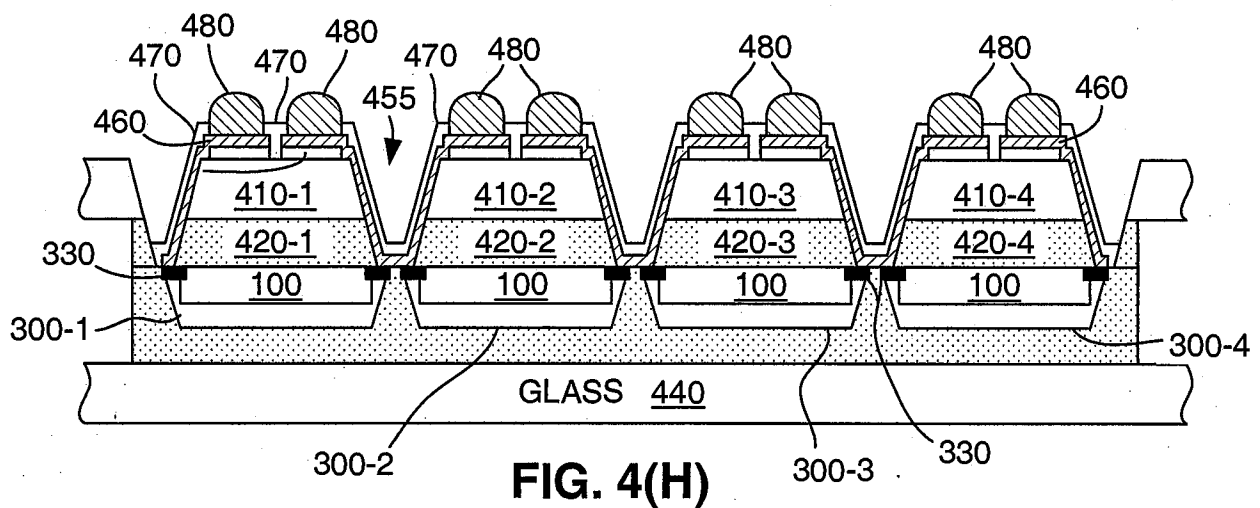


FIG. 4(H)

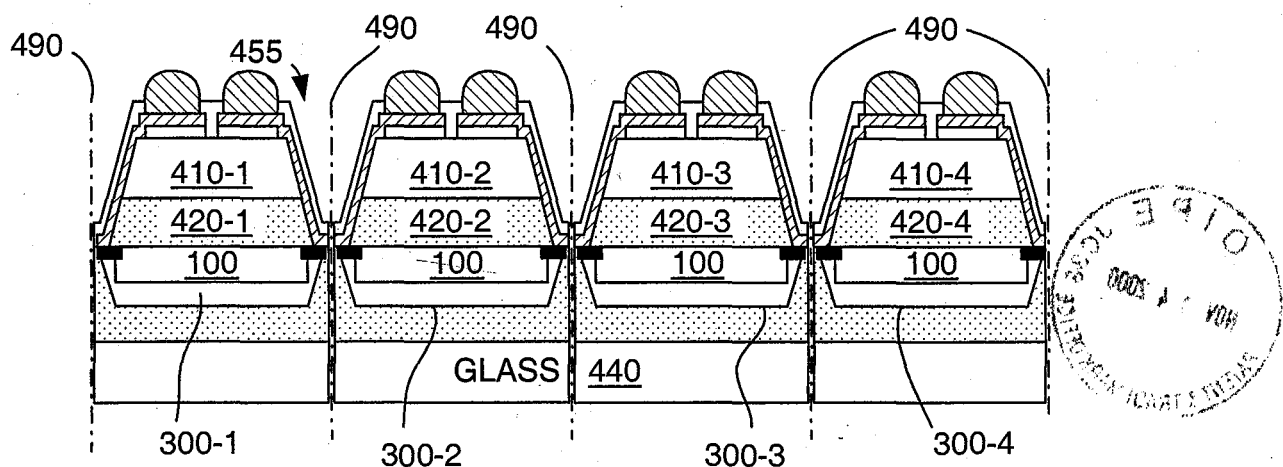


FIG. 4(I)

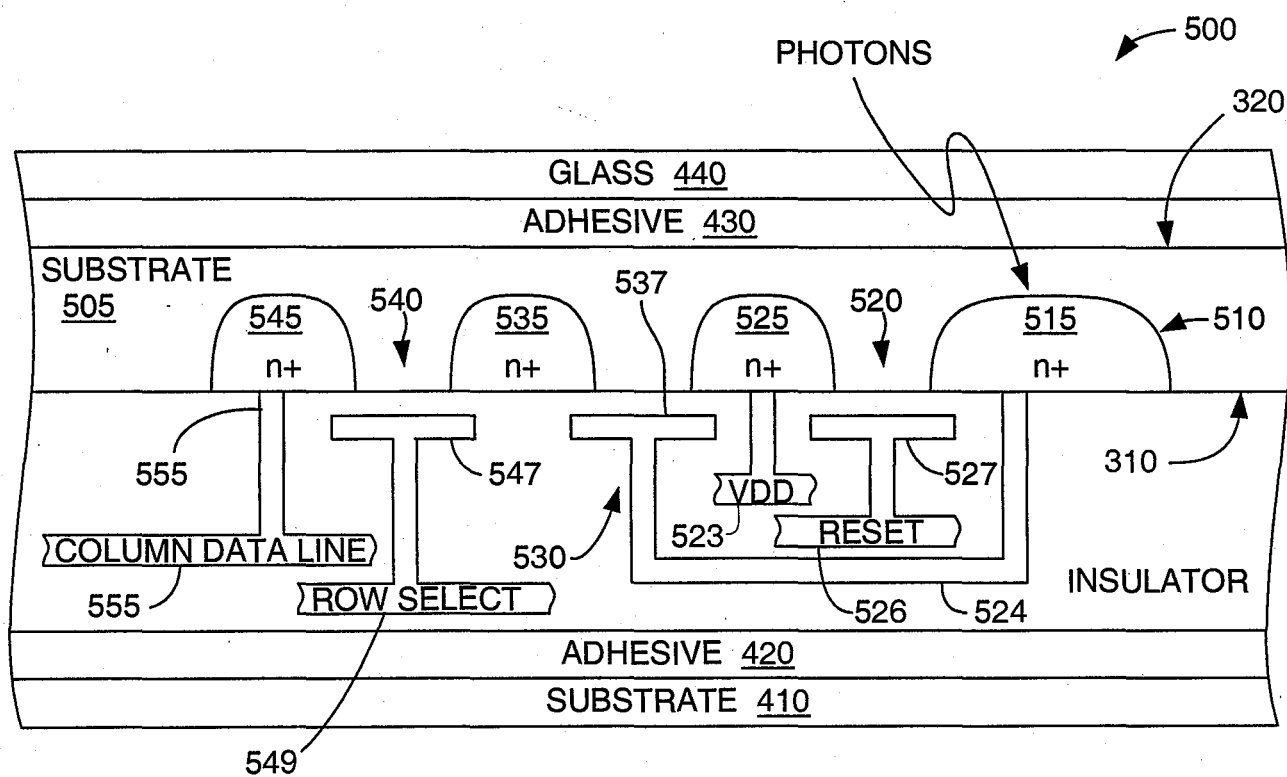


FIG. 5

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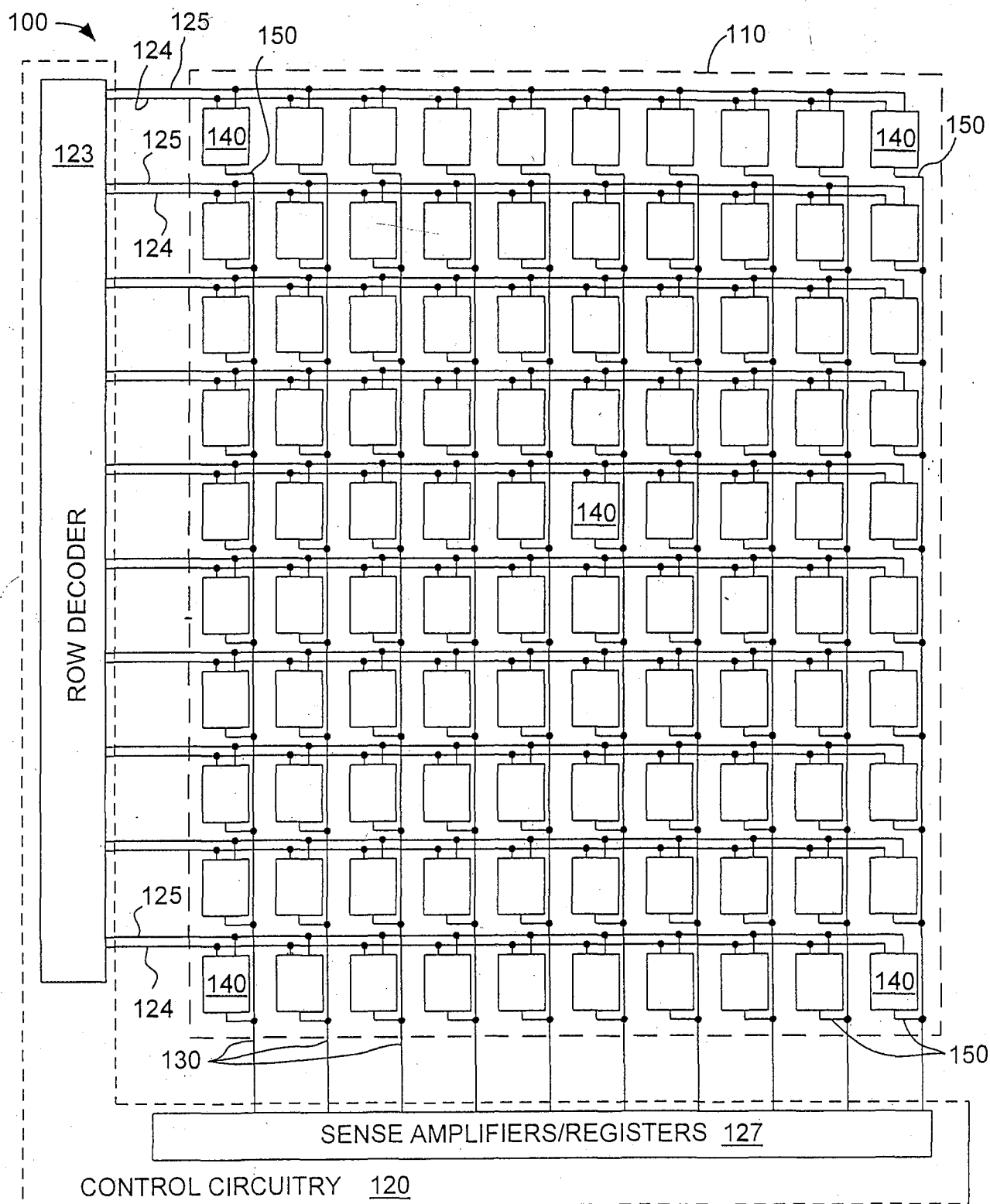


FIG. 1

Fig. 24

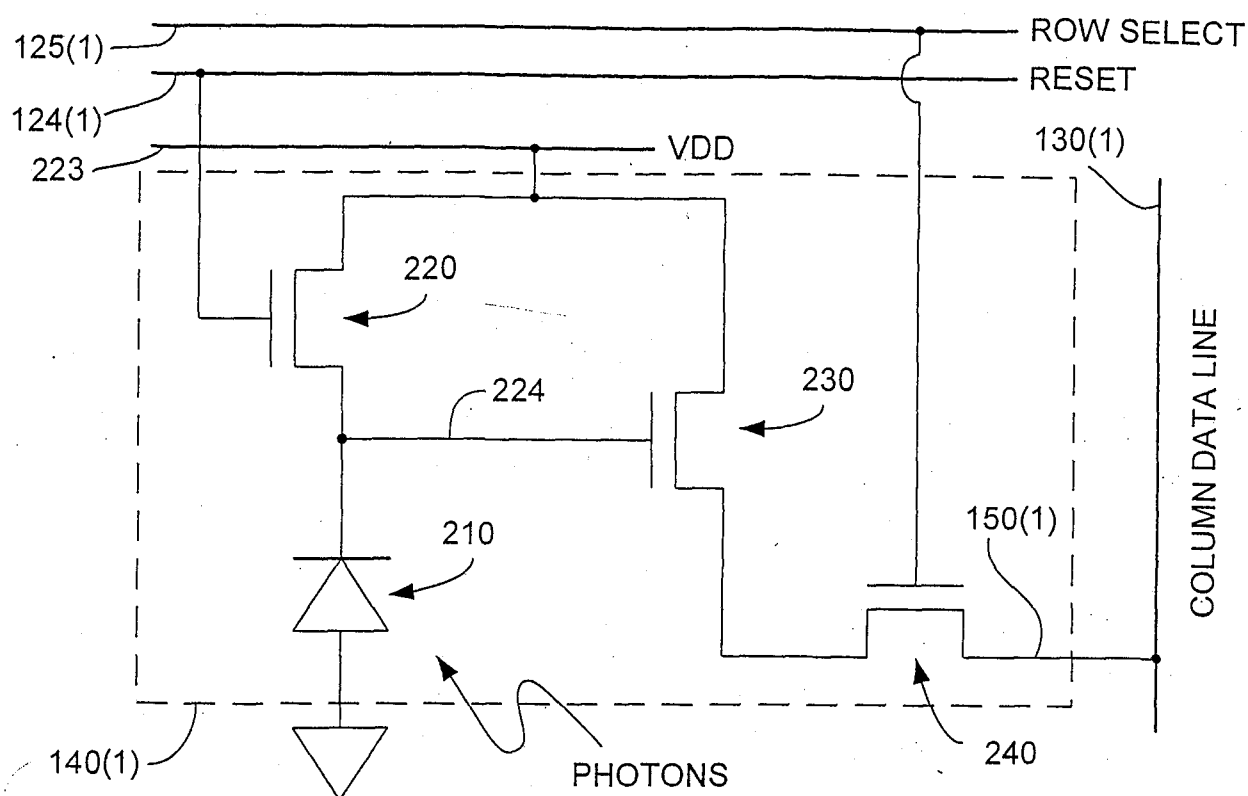


FIG. 2(A) (PRIOR ART)

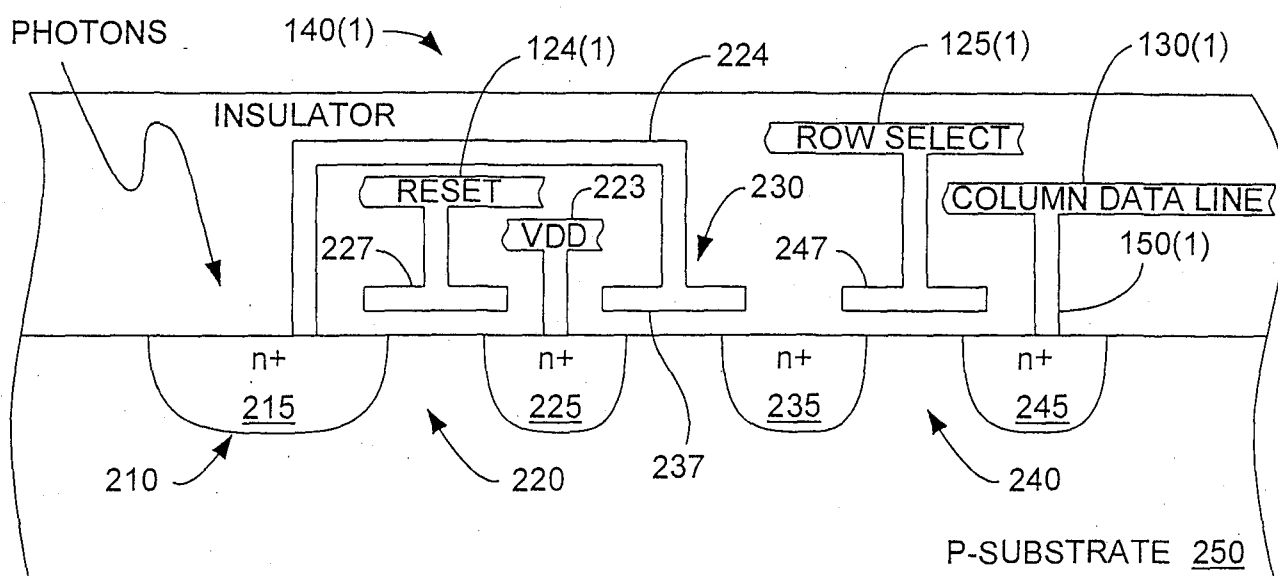


FIG. 2(B) (PRIOR ART)

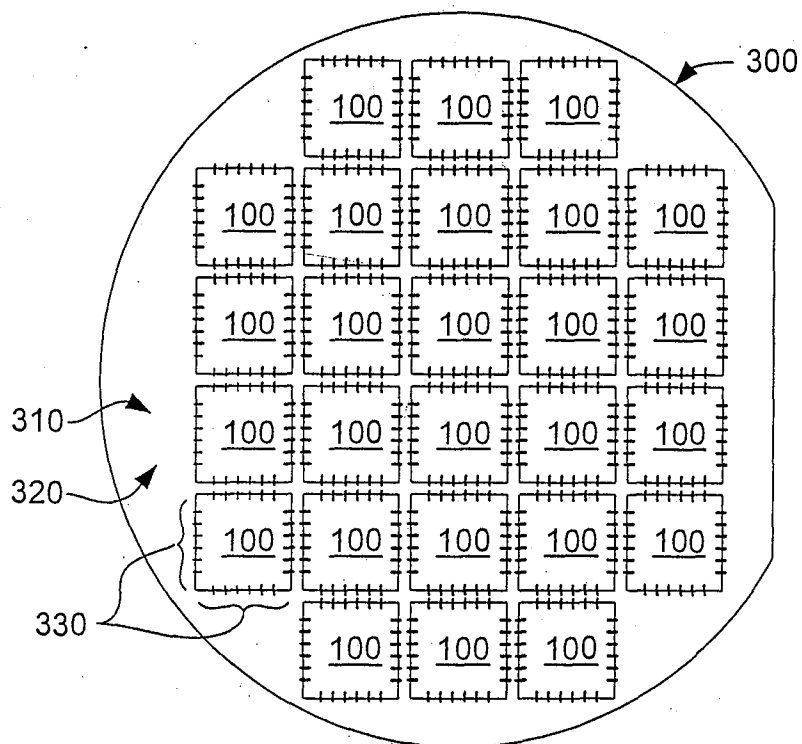


FIG. 3(A)

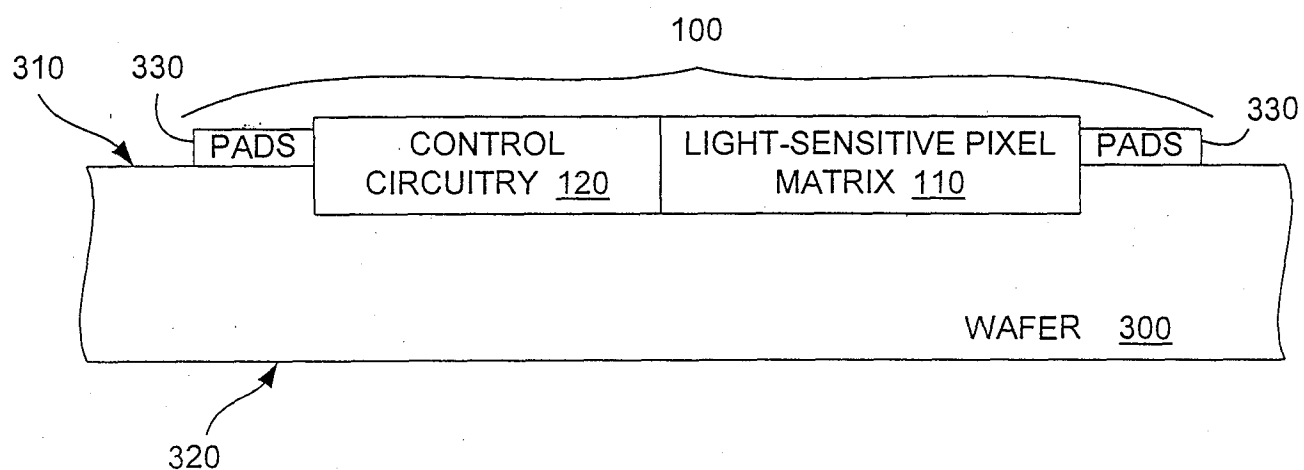


FIG. 3(B)

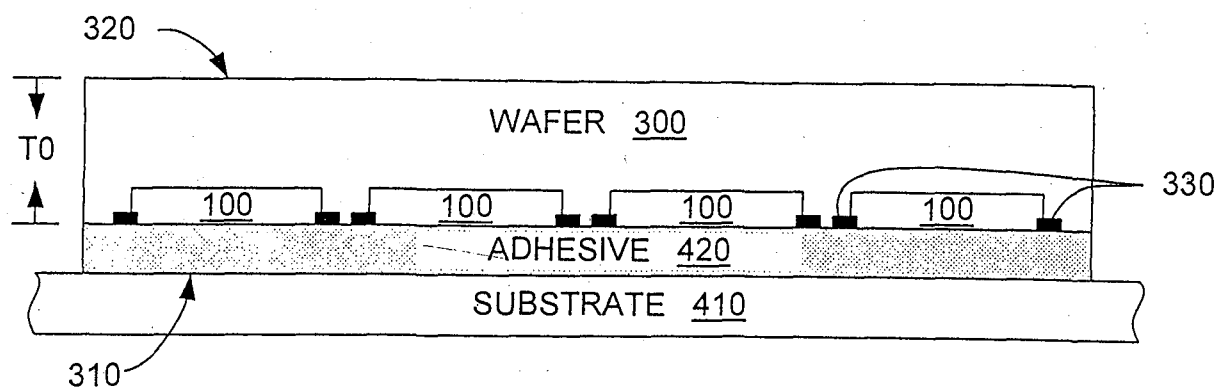


FIG. 4(A)

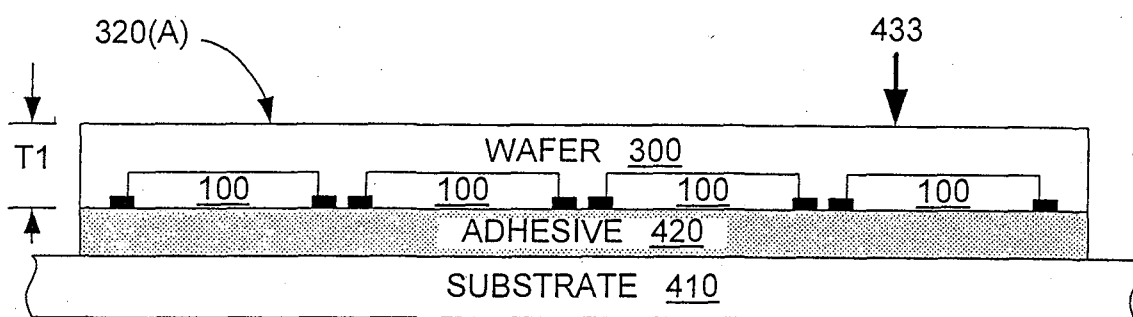


FIG. 4(B)

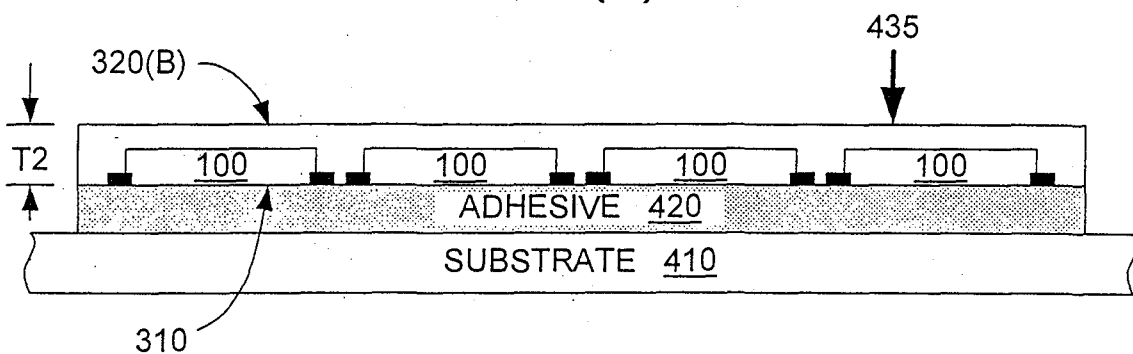


FIG. 4(C)

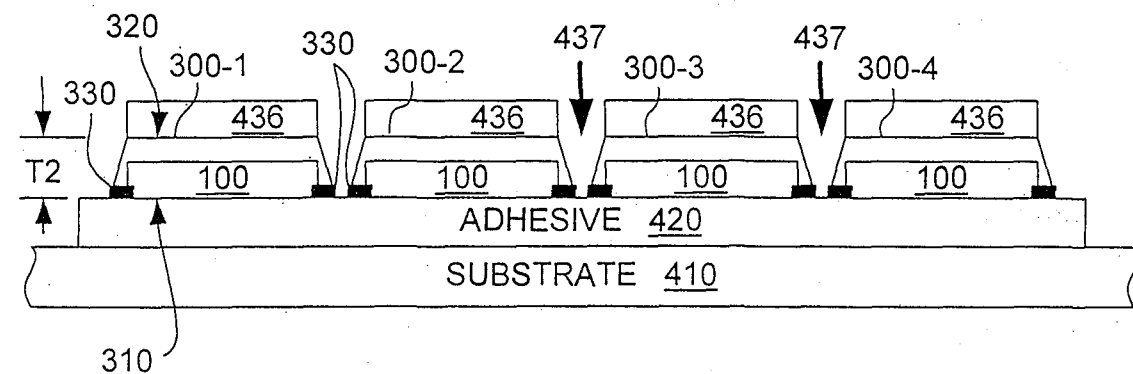


FIG. 4(D)

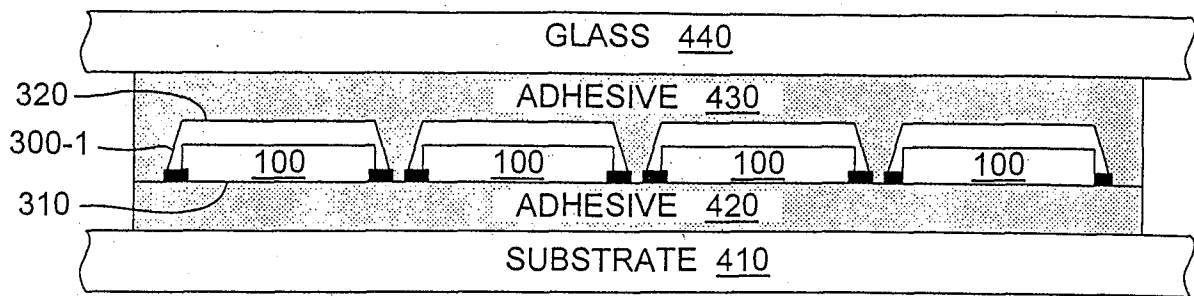


FIG. 4(E)

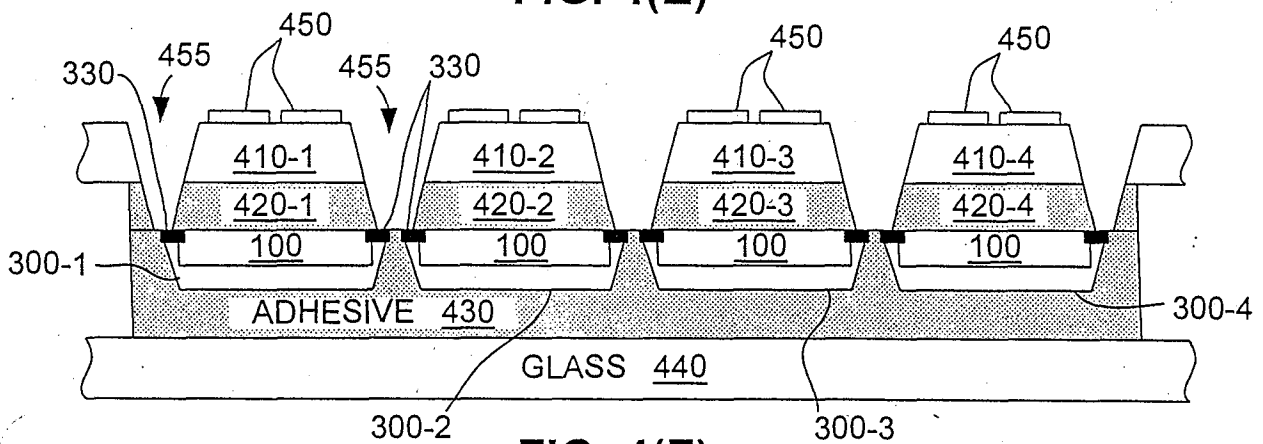


FIG. 4(F)

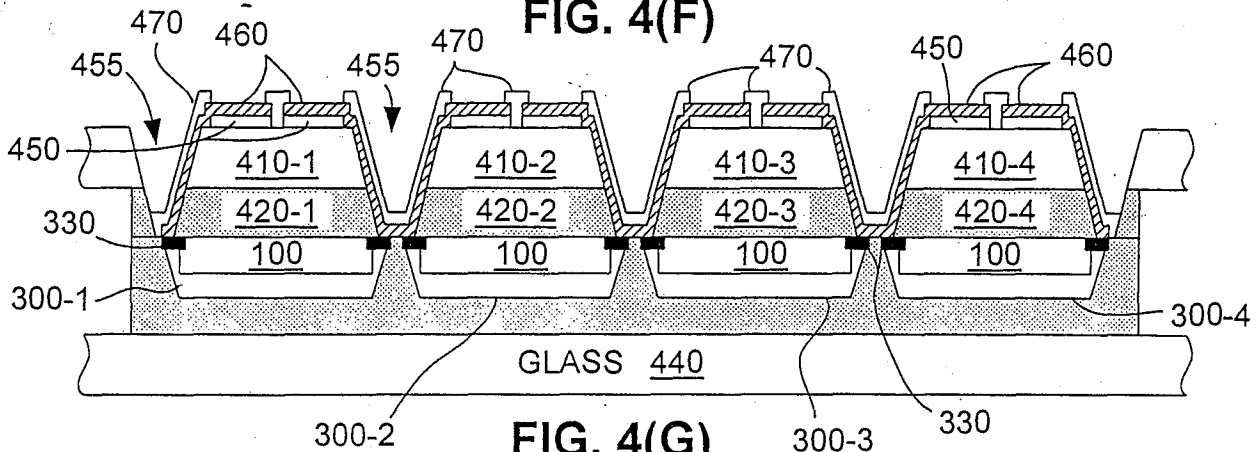


FIG. 4(G)

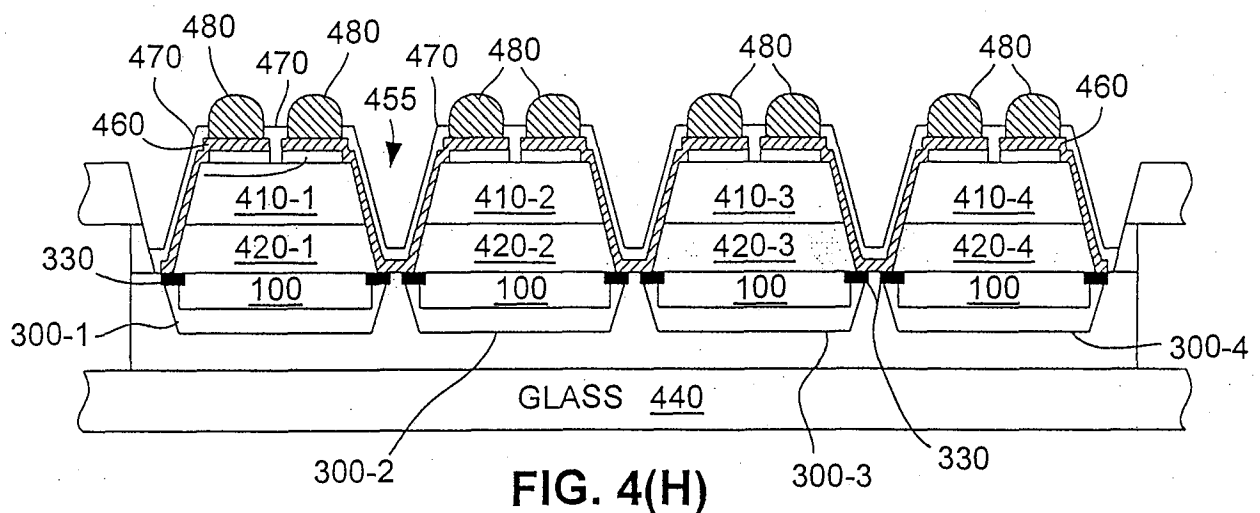
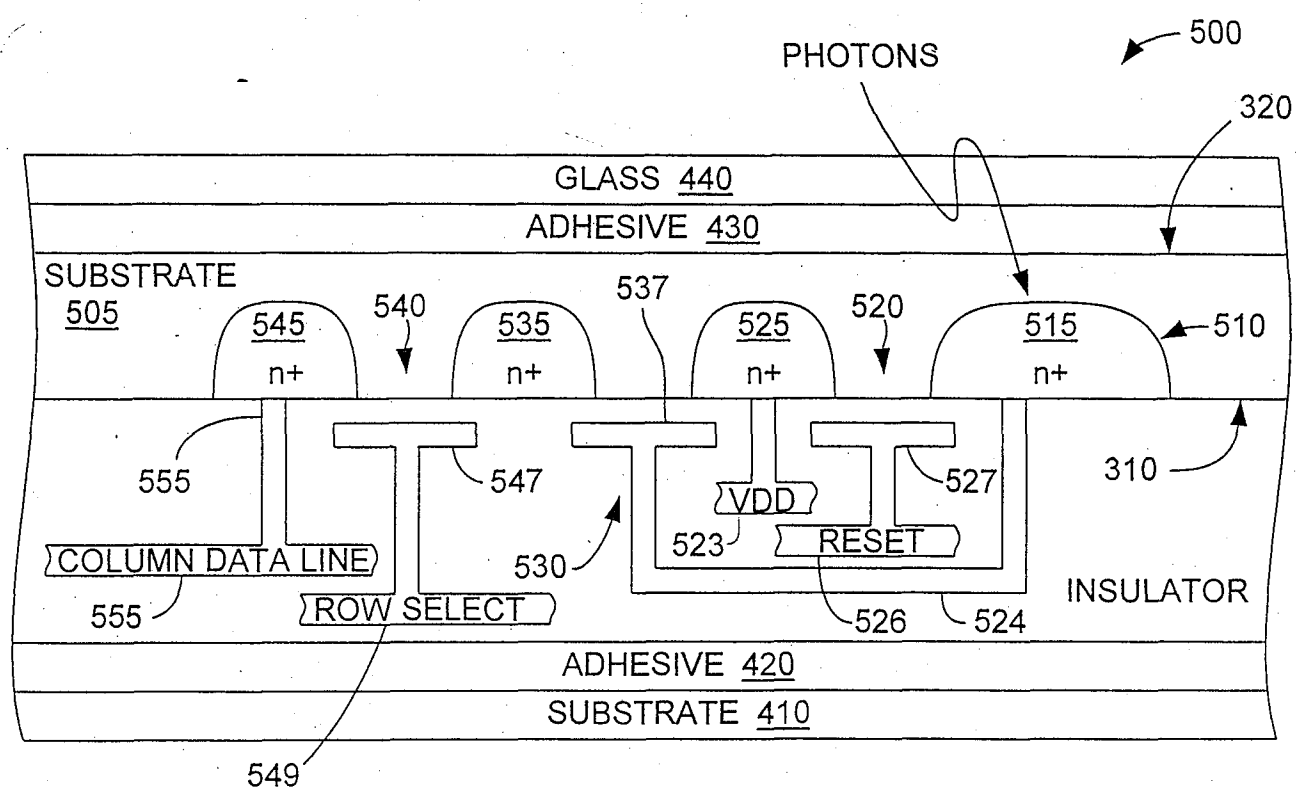
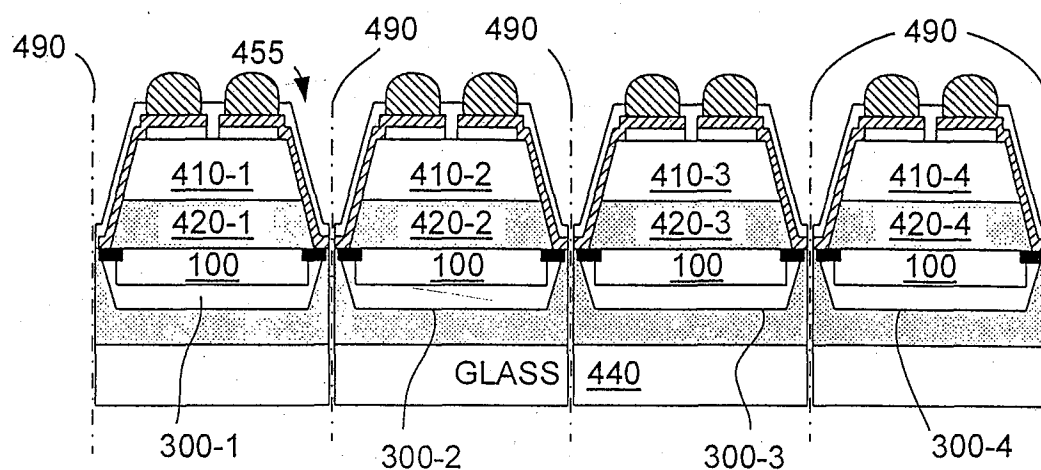
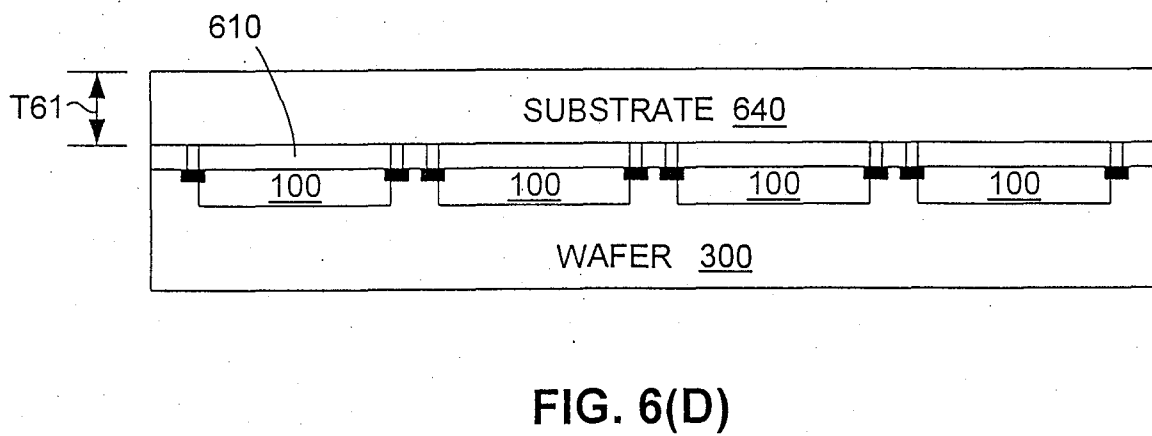
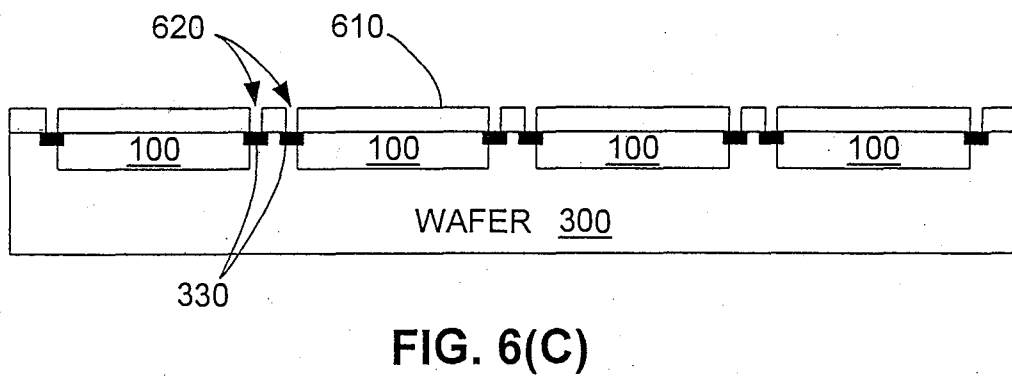
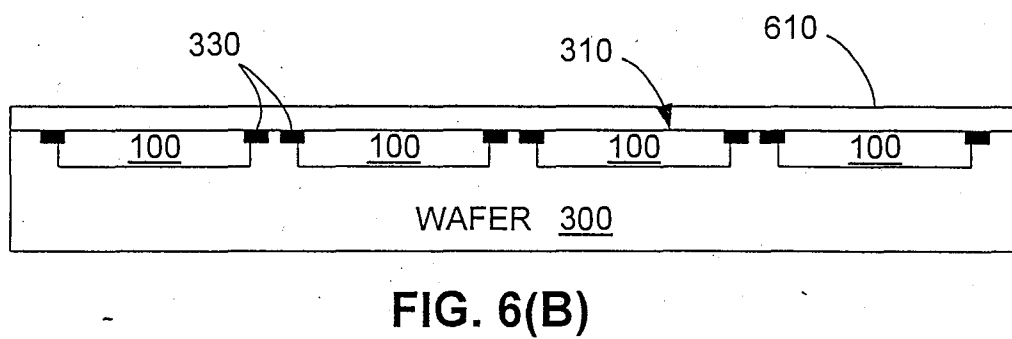
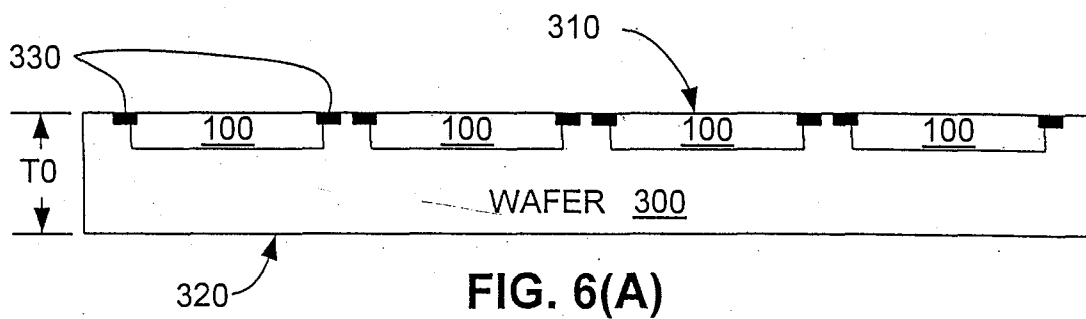


FIG. 4(H)





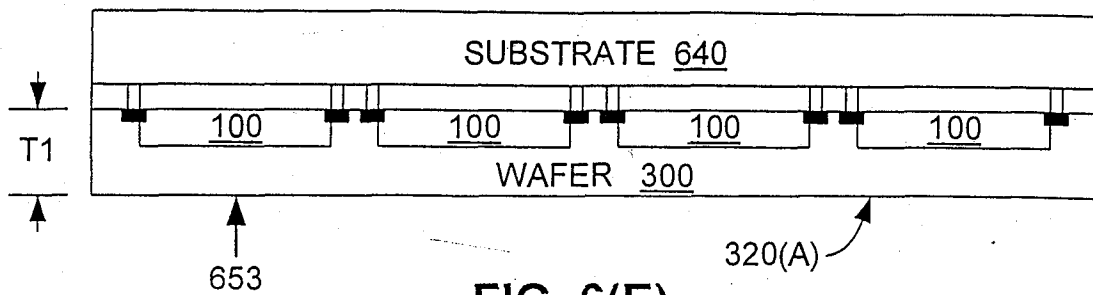


FIG. 6(E)

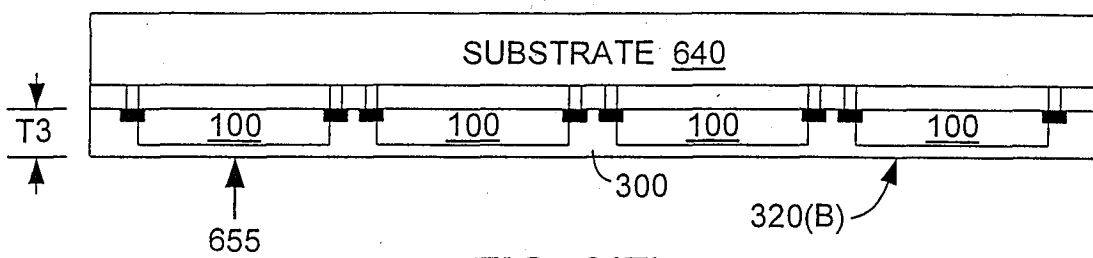


FIG. 6(F)

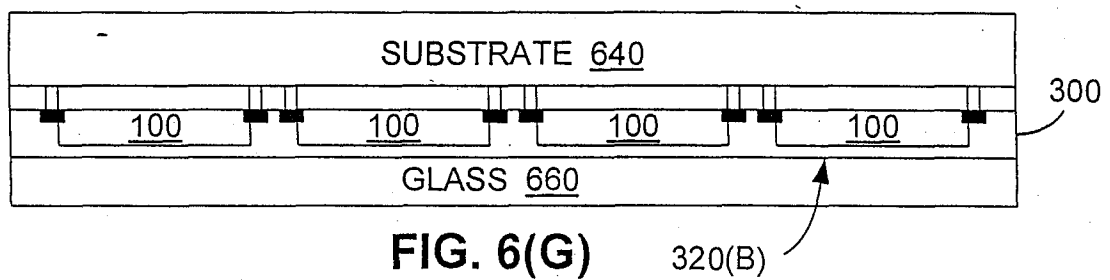


FIG. 6(G)

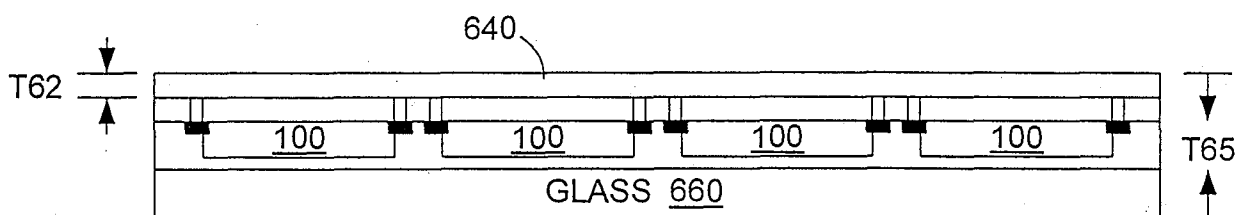


FIG. 6(H)

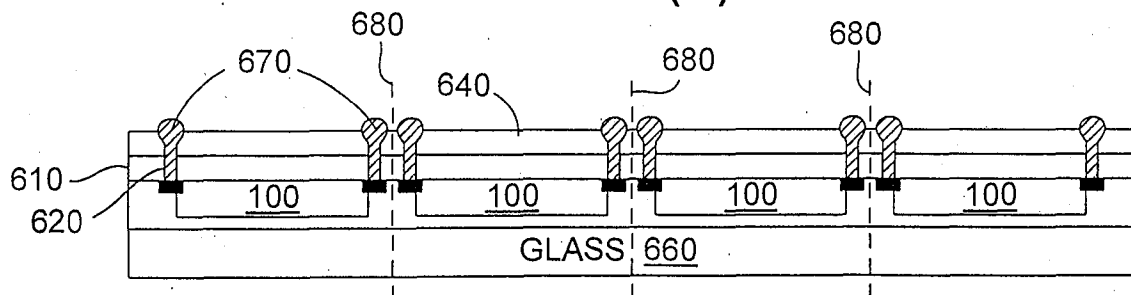
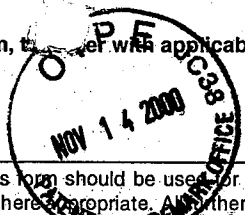


FIG. 6(I)

PART B—ISSUE FEE TRANSMITTAL

Complete and mail this form, together with applicable fees, to:

Box ISSUE FEE
Assistant Commissioner for Patents
Washington, D.C. 20231B \$
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MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All other correspondence including the Issue Fee Receipt, the Patent, advance orders and ~~MAINTENANCE~~ maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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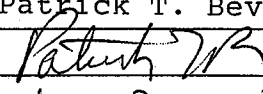
022888 MMC1/0829
BEVER HOFFMAN & HARMS, LLP
2099 GATEWAY PLACE
SUITE 320
SAN JOSE CA 95110-1017

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Patrick T. Bever (Depositor's name)

 (Signature)

11-10-2000 (Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/441,766	11/17/99	006	MUNSON, G	2811 08/29/00
First Named Applicant	MALINOVICH,	35 USC 154(b) term ext. =	0 Days.	

TITLE OF INVENTION BACKSIDE ILLUMINATED IMAGE SENSOR

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
3 TSL-008-1D	257-447.000	R44	UTILITY	NO	~~\$1210.00~~ 1,240.00	11/29/00

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

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1 BEVER, HOFFMAN &
2 HARMS, LLP
3 Patrick T. Bever

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PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE Tower Semiconductor Ltd.

(B) RESIDENCE: (CITY & STATE OR COUNTRY) Migdal Haemek, Israel

Please check the appropriate assignee category indicated below (will not be printed on the patent)

☐ Individual ☒ Corporation or other private group entity ☐ government

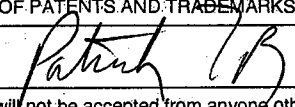
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Effective November 10, 1998

09/441766

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(Column 2)

(Column 3)

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(Column 1)

(Column 2)

(Column 3)

FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM

(Column 1)

(Column 2)

(Column 3)

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OR

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SEARCHED

Class	Sub.	Date	Exmr.
257	228, 291, 292, 447, 460	25 Aug 2000	REH/

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
257	228, 291, 292, 447, 460	25 Aug 2000	REH/

SEARCH NOTES
(INCLUDING SEARCH STRATEGY)

	Date	Exmr.
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ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	DT		12-11-99
O.I.P.E. CLASSIFIER		12	
FORMALITY REVIEW	CM	711632	12/21/99

INDEX OF CLAIMS

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Appeal
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If more than 150 claims or 10 actions
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PATENT APPLICATION



09441766

JC688 U.S. PTO

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11/17/99

INITIALS



CONTENTS

DEC 08 994

Date received
(Incl. C. of M.)
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Date Mailed

Date received
(Incl. C. of M.)
or
Date Mailed

1. Application 8 papers.

2. IDS 11-17-99

3. Pre-Amdt A 11-17-99

4. IDS 5-22-00

5. Allow POL-37/Ex Amdt B 8-28-00

6. 11/22/00 L8 after set 11/14/00

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