

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED,

Petitioner,

v.

ALIDDOUBLE, INC.

Patent Owner.

U.S. Patent No. 6,169,319

DECLARATION OF DR. KONSTANTINOS P. GIAPIS

TABLE OF CONTENTS

I.	BACKGROUND AND QUALIFICATIONS.....	1
II.	MATERIALS REVIEWED AND CONSIDERED	3
III.	MY UNDERSTANDING OF PATENT LAW	7
	A. Claim Construction.....	7
	B. Anticipation.....	8
	C. Obviousness.....	8
IV.	OVERVIEW OF THE '319 PATENT	11
	A. Claims.....	18
V.	OVERVIEW OF THE TECHNOLOGY	19
	A. CCD and CMOS Image Sensors	19
	1. CCDs.....	20
	2. CMOS Image Sensor (CIS).....	21
	3. Frontside Illumination (“FSI”) v. Backside Illumination (“BSI”) CCD.....	22
	B. Pixel	24
	1. Photodiode-Type Passive Pixel.....	24
	2. Photodiode-Type Active Pixel / Photogate-Type Active Pixel	25
	3. Photogate-Type Active Pixel.....	25
	C. Removal of Material from Backside of Wafer.....	26
	D. Wafer-Level Packaging	27
VI.	LEVEL OF ORDINARY SKILL IN THE ART	28

VII. CLAIM CONSTRUCTION.....	29
VIII. OVERVIEW OF THE PRIOR ART	29
A. Nixon.....	29
1. Overview of Nixon	36
B. Badihi	38
C. Merrill.....	39
D. Watanabe.....	41
IX. SPECIFIC GROUNDS FOR PETITION.....	42
X. GROUND 1: NIXON RENDERS OBVIOUS CLAIMS 1, 2, 5, AND 6.....	43
1. Claim 1	43
2. Claim 2	53
3. Claim 5	54
4. Claim 6	54
XI. GROUND 2: NIXON IN VIEW OF MERRILL RENDERS OBVIOUS CLAIM 3.....	55
1. Reasons to Combine Nixon with Merrill	56
2. Claim 3	58
XII. GROUND 3: NIXON IN VIEW OF WATANABE RENDERS OBVIOUS CLAIM 4.....	67
1. Reasons to Combine Nixon with Watanabe	68
2. Claim 4	70
XIII. GROUND 4: BADIHI RENDERS OBVIOUS CLAIMS 1, 2, 5, AND 6.....	72
1. Claim 1	72

2.	Claim 2	81
3.	Claim 5	83
4.	Claim 6	84
XIV. GROUND 5: BADIHI IN VIEW OF WATANABE RENDERs OBVIOUS CLAIM 4.....		85
1.	Reasons to Combine Badihi with Watanabe	85
2.	Claim 4	87
XV. GROUND 6: MERRILL IN VIEW OF BADIHI RENDERs OBVIOUS CLAIMS 1, 2, 3, 5, AND 6.....		88
1.	Reasons to Combine Merrill with Badihi.....	88
2.	Claim 1	90
3.	Claim 2	99
4.	Claim 3	101
5.	Claim 5	103
6.	Claim 6	104
XVI. GROUND 7: MERRILL IN VIEW OF BADIHI AND WATANABE RENDERs OBVIOUS CLAIM 4		105
1.	Reasons to Combine Merrill and Badihi with Watanabe.....	105
2.	Claim 4	107
XVII.CONCLUSION.....		108

I, Dr. Konstantinos P. Giapis, declare as follows:

1. I have been retained as an expert witness on behalf of Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) for the above captioned Petition for *Inter Partes* Review (“IPR”) of U.S. Patent No. 6,169,319 (“the ’319 patent”) (Ex. 1001).

2. I am being compensated for my time in connection with this IPR at my standard consulting rate of \$700 per hour. My compensation is not affected by the outcome of this matter.

3. I have been asked to provide my opinions regarding whether claims 1-6 of the ’319 patent (the “Challenged Claims”) are invalid as being anticipated by or obvious over the prior art to a person having ordinary skill in the art at the time of the alleged invention.

4. I am not currently, and have not at any time in the past been, an employee of TSMC. I have no financial interest in TSMC.

I. BACKGROUND AND QUALIFICATIONS

5. I am a professor of chemical engineering at the California Institute of Technology (“Caltech”). I have held that position since 1992.

6. My research relates to processing of semiconductors, dielectrics, and metals, as performed in the fabrication of semiconductor devices, including microprocessors and digital memories. In particular, my work has focused upon

patterning layers of electronic materials to fabricate sub-micron features such as transistor gates, vias, and metal lines found in VLSI circuits. I have also conducted modeling and simulations of the evolution of poly-silicon and metal gate profiles subjected to plasma etching and studied their charging interactions with plasmas. Since the start of my graduate career in 1985, I have accumulated over 35 years of experience on semiconductor materials, devices, and their processing.

7. In my professorial duties at Caltech, I have developed and taught new undergraduate and graduate level courses on semiconductor device physics and their processing. These innovative courses combined solid state physics and electronic materials processing technologies with the more traditional chemical engineering subjects of transport phenomena and chemical thermodynamics. The courses have prepared several generations of students for successful careers in the semiconductor industry.

8. During my research career, I have authored or co-authored 98 peer-reviewed papers, 12 refereed conferences proceedings, two book chapters. Most of my publications relate to semiconductor device processing. My papers on charging damage of high-density integrated devices such as microprocessors, and digital memories are highly cited. I have also been granted 13 patents.

9. My curriculum vitae is provided as Exhibit 1053.

II. MATERIALS REVIEWED AND CONSIDERED

10. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art, and have considered the viewpoint of a person having ordinary skill in the art (POSITA) at the time of the alleged invention.

11. In forming my opinions, I have reviewed and considered the following documents:

Exhibit No.	Description
1001	U.S. Patent No. 6,169,319 (“the ’319 Patent”)
1002	Prosecution File History for the ’319 Patent
1003	Declaration of Dr. Konstantinos P. Giapis
1004	U.S. Patent No. 6,429,036 (“Nixon”)
1005	U.S. Provisional Patent Application No. 60/116144 (“’144 Nixon Provisional”)
1006	Intentionally omitted
1007	Certified translation of JP H06-268183 (“Watanabe”)
1008	Intentionally omitted
1009	Certified translation of JP H10-116977 (“Muramatsu”)
1010	Certified translation of Sakai, H., <i>CSP Development of Shell Case Type</i> , in THE J. OF JAPAN INST. OF INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS, vol. 12, no. 3, pp. 144-147 (1997) (“Sakai”)
1011	Intentionally omitted

Exhibit No.	Description
1012	Intentionally omitted
1013	Fossum, E., <i>Active Pixel Sensors: Are CCDs Dinosaurs?</i> , in CHARGE-COUPLED DEVICES AND SOLID STATE OPTICAL SENSORS III, SPIE, vol. 1900, pp. 2-14 (1993) (“Fossum I”)
1014	Intentionally omitted
1015	Barbe, F., <i>A Tradeoff Analysis for CCD Area Imagers: Frontside Illuminated Interline Transfer vs. Backside Illuminated Frame Transfer</i> , in PROCS., CCD APPLICATIONS CONF., pp. 13-20 (1973) (“Barbe”)
1016	Fossum, E., <i>Ultra-low power imaging systems using CMOS image sensor technology</i> , in ADV. MICRODEVICES AND SPACE SCIENCE SENSORS, SPIE, vol. 2267, pp. 107-111 (Sept. 23, 1994) (“Fossum II”)
1017	Brissot, L., et al., <i>High-definition CCDs for enhanced definition television</i> , in HIGH-RESOLUTION SENSORS AND HYBRID SYSTEMS, SPIE, vol. 1656, pp. 427-436 (Aug. 12, 1992) (“Brissot”)
1018	<i>Introduction to Quantum Efficiency</i> , TELEDYNE, available at https://www.photometrics.com/learn/imaging-topics/quantum-efficiency (“Quantum Efficiency”)
1019	U.S. Patent No. 5,244,817 (“Hawkins”)
1020	U.S. Patent No. 5,270,221 (“Garcia”)
1021	U.S. Patent No. 5,494,833 (“Martin”)
1022	WO1999/040624 (“Badehi I”)
1023	<i>CMOS Fundamentals</i> , SILICON IMAGING, available at http://www.siliconimaging.com/cmoss_fundamentals.htm#:~:text=Passive%2Dpixel%20sensors%20(PPS),the%20photosites%20and%20their%20connections (“CMOS Fundamentals”)
1024	U.S. Patent No. 8,063,963 (“Dierickx”)

Exhibit No.	Description
1025	Intentionally omitted
1026	Intentionally omitted
1027	Intentionally omitted
1028	Intentionally omitted
1029	U.S. Patent No. 6,960,795 (“Rhodes”)
1030	“Digital camera,” <i>Encyclopedia Britannica</i> (https://www.britannica.com/technology/webcamming) (“Digital camera”)
1031	Sorrell, C., <i>Inside the Nobel Prize: How a CCD Works</i> , WIRED (Oct. 7, 2009), available at https://www.wired.com/2009/10/ccd-inventors-awarded-nobel-prize-40-years-on/ (“How a CCD Works”)
1032	CCD vs. CMOS, TELEDYNE DALSA, available at https://www.teledynedalsa.com/en/learn/knowledge-center/ccd-vs-cmos/ (“CCD vs. CMOS”)
1033	<i>Introduction to Charge-Coupled Devices (CCDs)</i> , NIKON, available at https://www.microscopyu.com/digital-imaging/introduction-to-charge-coupled-devices-ccds (“Intro to CCDs”)
1034	<i>What Is a CMOS Image Sensor?</i> , NANOTEC MUSEUM, available at https://www.tel.com/museum/exhibition/principle/cmos.html (“What is a CMOS Image Sensor”)
1035	Fowler, B., et al., <i>CMOS image sensors – past, present and future</i> , Proceedings ICIS 2006 – International Congress of Imaging Science (2006) (“Fowler”)
1036	L. J. Kozlowski, et al, <i>Comparison of passive and active pixel schemes for CMOS visible imagers</i> , Proc. SPIE 3360, Infrared Readout Electronics IV (September, 1998) (“Kozlowski”)

Exhibit No.	Description
1037	Intentionally omitted
1038	U.S. Patent No. 9,257,479 (“Koizumi”)
1039	Intentionally omitted
1040	Intentionally omitted
1041	Intentionally omitted
1042	Fossum and Hondongwa, <i>A Review of the Pinned Photodiode for CCD and CMOS Image Sensors</i> , IEEE Journal of the Electron Devices Society (May, 2014) (“Fossum III”)
1043	<i>Back-illuminated sensor</i> , WIKIPEDIA, available at https://en.wikipedia.org/wiki/Back-illuminated_sensor
1044	Intentionally omitted
1045	Fossum, Eric R., <i>CMOS Image Sensors: Electronic Camera-On-A-Chip</i> , 44 IEEE TRANSACTIONS ON ELECTRON DEVICES, no. 10, pp. 1689-98 (Oct. 1997) (“Fossum IV”)
1046	U.S. Pat. No. 6,084,259 (“Kwon”)
1047	Fossum, Eric R., <i>Image capture circuits in CMOS</i> , IEEE INT’L SYMPOSIUM ON VLSI TECH. SYS. AND APPLICATIONS, 52-57 (June 3, 1997) (“Fossum V”)
1048	<i>Introduction to CMOS Image Sensors</i> , OLYMPUS LS, available at https://www.olympus-lifescience.com/en/microscope-resource/primer/digitalimaging/cmosimagesensors/ (“Olympus article”)
1049	U.S. Patent No. 5,789,774 (“Merrill”)
1050	Photodiodes, LEARN ABOUT Electronics, available at https://learnabout-electronics.org/Semiconductors/diodes_27.php (“LEB article”)

Exhibit No.	Description
1051	<i>Photobit PB-159: Digital Camera On A Chip</i> , PHOTOBIT (“PB-159 datasheet”)
1052	U.S. Pat. No. 3,676,715 (“Brojdo”)
1053	Curriculum Vitae of Dr. Konstantinos P. Giapis
1054	Declaration of Dr. Sylvia Hall-Ellis
1055	Affidavit of Nathaniel E Frank-White
1101	Badihi, A., <i>ShellCase Ultrathin Chip Size Package</i> , in PROCS. INT’L SYMPOSIUM ON ADV. PACKING MATERIALS, PROCESSES, PROPERTIES AND INTERFACES (IEEE CAT. NO. 99TH8405), IEEE, pp. 236-40 (Mar. 1999) (“Badihi”), attached as Exhibit 1101 to Declaration of Dr. Sylvia Hall-Ellis
1102	Intentionally omitted
1103	Sakai, attached as Exhibit 1103 to Declaration of Dr. Sylvia Hall-Ellis
1104	Intentionally omitted

III. MY UNDERSTANDING OF PATENT LAW

12. I am not an attorney. For purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as listed below.

A. Claim Construction

13. I understand that in an IPR petition filed after November 13, 2018, a claim must be construed under the Phillips standard. Under that standard, words of

a claim are given their plain and ordinary meaning as understood by a POSITA at the time of invention, in light of the specification and prosecution history, unless those sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent.

B. Anticipation

14. I understand that a claim is invalid if it is anticipated. Anticipation of a claim requires that every element of a claim be disclosed expressly or inherently in a single prior-art reference, arranged in the prior-art reference the same way it is arranged in the claim, so that the disclosure effectively puts the public in possession of the invention. For the claim to be anticipated implicitly, I understand that the reference must make clear that the missing descriptive matter in the claim of the patent is necessarily or implicitly present in the allegedly anticipating reference, and that it would be so recognized by one of ordinary skill in the art.

C. Obviousness

15. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed.

16. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

17. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- whether a POSITA could implement a predictable variation, and would see the benefit of doing so;

- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

18. I understand that a POSITA has ordinary creativity, and is not an automaton.

19. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

20. I understand that prior art to the '319 patent includes patents and printed publications in the relevant art that predate the Priority Date of the '319 patent.

21. I understand that certain factors—often called “secondary considerations”—may support or rebut an assertion of obviousness of a claim. I

understand that such secondary considerations include, among other things, commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I further understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

IV. OVERVIEW OF THE '319 PATENT

22. The '319 patent is entitled “Backside illuminated image sensor.” The named inventors are Yacov Malinovich and Ephie Koltin. The named assignee of the '319 patent is Alidouble Inc (“Alidouble”).

23. The '319 patent was filed on November 17, 1999, claiming priority to Application No. 09/372,865 filed on August 12, 1999.

24. My opinion analyzes the invalidity of the '319 patent assuming that the Priority Date of the '319 patent is August 12, 1999.

25. The '319 patent discloses conventional backside illuminated image (BSI) image sensors are expensive because (1) they are made using nonstandard

complementary metal-oxide-semiconductor (CMOS) processes and (2) packaging the BSI image sensors is complex. Ex. 1001, 4:14-31. To address these problems, the '319 patent discloses a method for making and packaging BSI image sensors using standard wafer processing techniques and equipment. *Id.*, 8:52-55.

26. The '319 patent discloses “a back-illuminated [complementary metal–oxide–semiconductor] CMOS image sensor including a matrix of pixels (e.g., CMOS [active-pixel sensors] APS cells) that are fabricated on a semiconductor substrate.” *Id.*, Abstract. Each APS “includes a light sensing element that is capable of converting a detected quantity of light into a corresponding electrical signal.” *Id.*, 2:9-12. The method starts with a wafer having image sensor circuits formed on the wafer’s frontside, also known as the active side since that is where all the microelectronics of the image sensor circuits are located. *Id.*, 5:21-28, 6:13-16. The frontside of the wafer is secured to a protective substrate and then the backside of the wafer is thinned until the pixels in the image sensor circuits can detect light passing through the backside of the wafer. *Id.*, 6:30-60. The thinning process include a grinding process, such as planar erosion, and a chemical etching process. *Id.*, 6:61-7:41. After thinning, a transparent substrate is secured to the backside of the wafer, forming a waferwise sandwich. *Id.*, 7:62-8:8. The waferwise sandwich is sliced to produce individually packaged image sensors. *Id.*, 8:45-51.

27. Figures 4(A)-4(I) are cross-sectional views illustrating the process steps of one such method in accordance with one embodiment of the '319 patent. *Id.*, 6:27-8:63. Figure 4(A) shows the method starts with a **wafer 300** having **image sensor circuits 100** extending into the **wafer 300**'s first (frontside) surface 310,¹ which is secured by an **adhesive layer 420** onto a **protective substrate 410**:

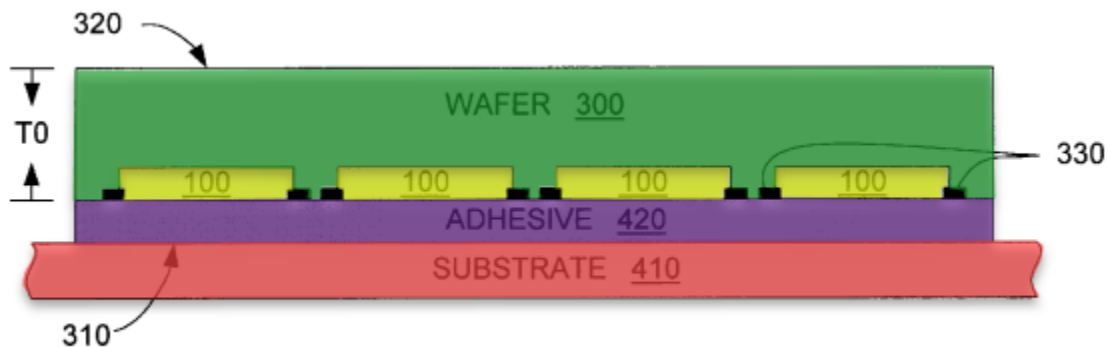


FIG. 4(A)

Id., Fig. 4(A) (annotated). “Each image sensor circuit 100 also includes ... metal contact pads 330 extending [i]nto first surface 310 of wafer 300” and “metal lines

¹ The first (frontside) surface 310 is mislabeled in Figure 4(A) and should actually point to where the “image sensors 100 [are] formed,” not in between the adhesive 420 and protective substrate 410. *Ex. 1001*, 6:30-36; *see also id.*, 9:6-9 (“CMOS APS cell 500 is formed on first surface 310 of the substrate 505, and includes a photodiode 510 formed by a diffusion region 515 extending into substrate 505 from first surface 310.”). The location of the first (frontside) surface 310 is correctly identified in Figures 3(B) and 4(C)-4(E). *Id.*, Figs. 3(B), 4(C)-4(E).

(not shown) are formed on wafer 300 and provide connection between metal contact pads 330 and the matrix of light sensitive pixel regions 110” *Id.*, 6:13-22.

28. Figures 4(B) and 4(C) illustrate the removal material from the second (backside) surface 320 of **wafer 300** with a planar erosion process 433 and a chemical etchant 435 “until the light-sensitive pixel region of image sensor circuits 100 are effectively exposed through the second surface 320 [so] that the pixel of each light-sensitive pixel region generates electron flow in response to light (photons) passing through the second surface 320”:

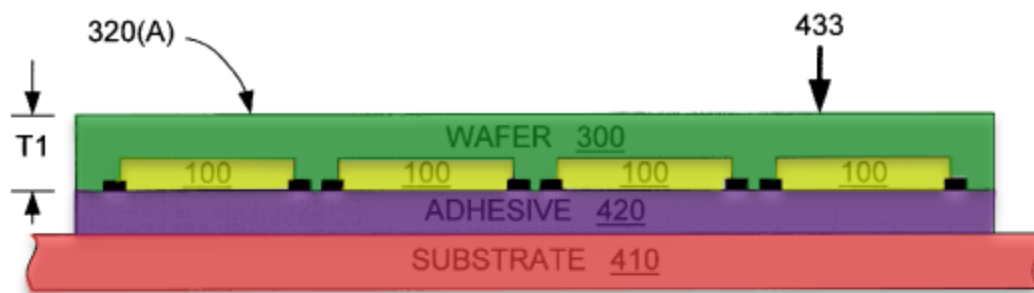


FIG. 4(B)

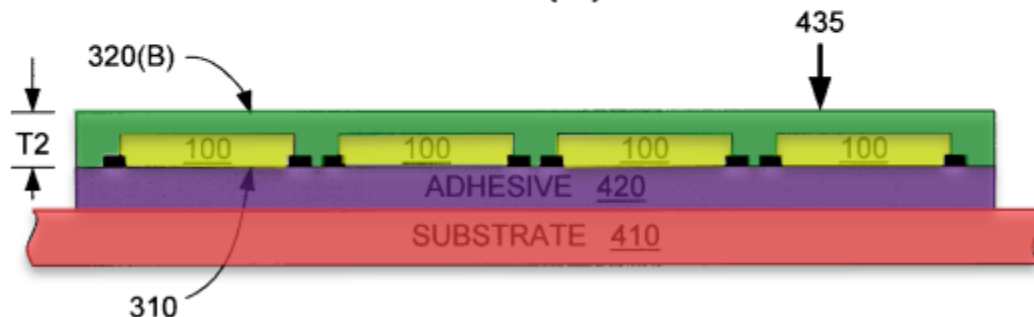


FIG. 4(C)

Id., 6:48-7:23, Figs. 4(B) (annotated) -(C) (annotated).

29. Figure 4(D) illustrates the separation of individual image sensor circuits 100 from each other to form dies 300-1 to 300-4 on **protective substrate 410**:
410:

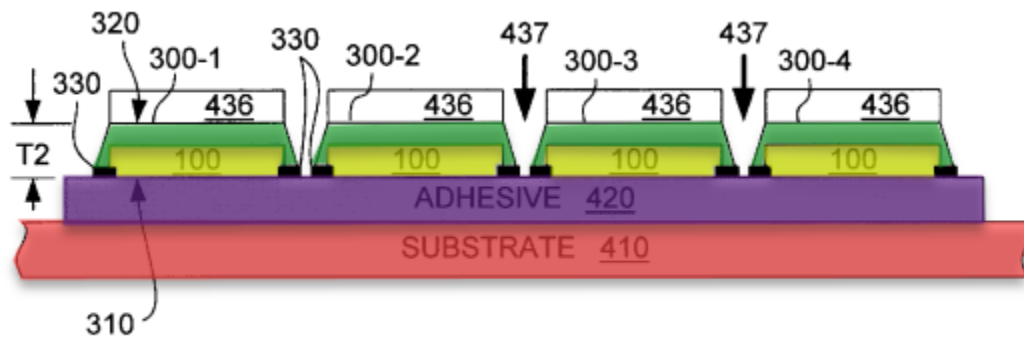


FIG. 4(D)

Id., Fig. 4(D) (annotated), 7:25-42 (“[S]econd surface 320 is scribed along predetermined dice lines and then etched using an etchant 437 to separate the individual image sensor circuits 100.”).

30. Figure 4(E) illustrates the securing of a **transparent (glass) substrate 440** onto the backside surface 320 of **wafer 300** using a **layer 430** of epoxy, producing a waferwise sandwich:

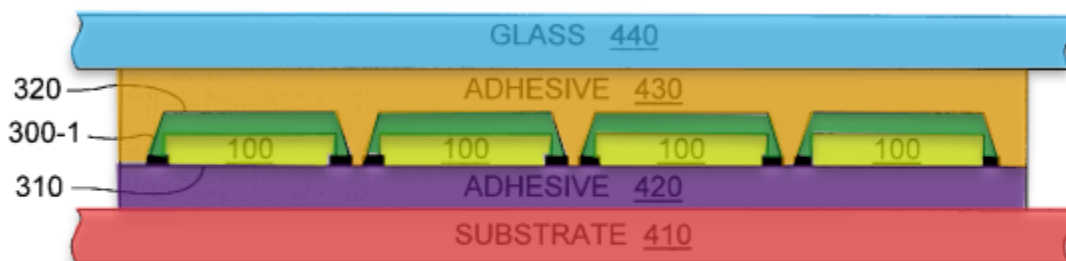
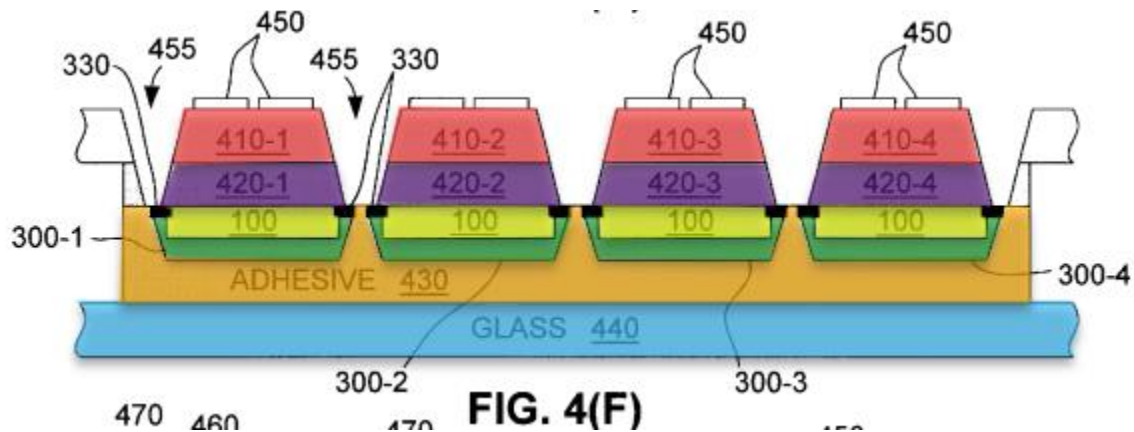


FIG. 4(E)

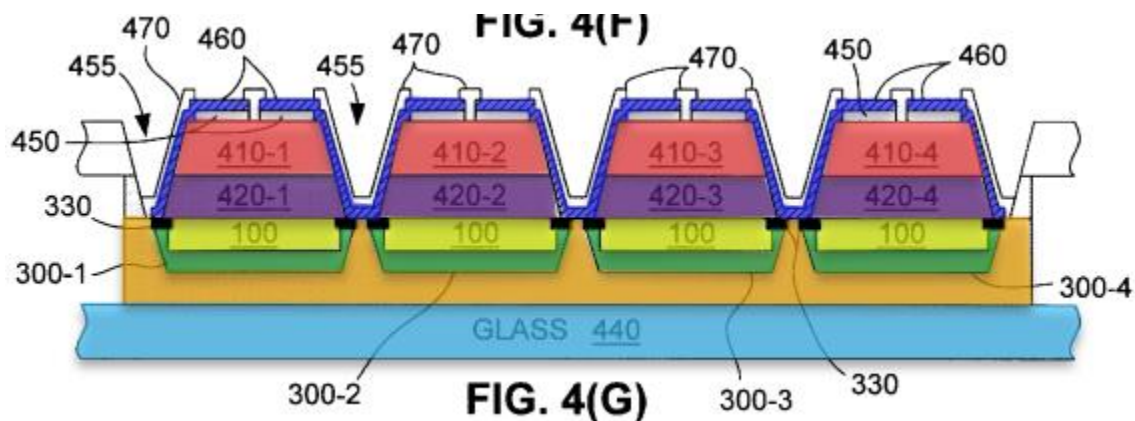
Id., Fig. 4(E) (annotated), 7:56-8:8.

31. Figure 4(F) illustrates the “form[ing of] grooves 455 through **protective substrate 410** and **adhesive layer 420** to expose metal contact pads 330”:



Id., Fig. 4(F) (annotated), 8:9-31.

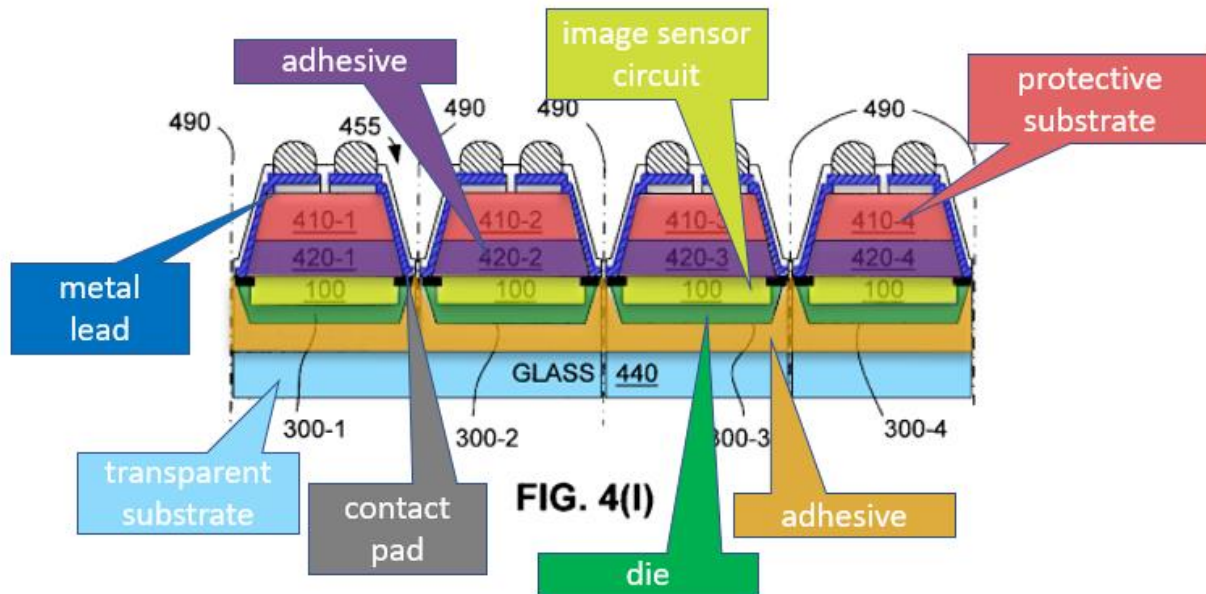
32. Figure 4(G) illustrates the forming of **metal leads 460** in grooves 455 to contact the exposed metal contact pads 330:



Id., Fig. 4(G) (annotated), 8:32-40.

33. Figure 4(H) illustrates the “form[ing of] solder bumps 480 using known ball-grid array (BGA) technology” on the “exposed portion of an associated

metal lead 460,” resulting in the CMOS image sensor illustrated in Figure 4(I), which illustrates BSI image sensors in a waferwise sandwich about to be diced.



Id., Figs. 4(H), (I) (annotated), 8:41-51. There, each BSI image sensor has a **die 300-1** with an **image sensor circuit 100** and **metal contact pads 330**, which provide access to a matrix of light-sensitive pixel regions 110 and control circuitry 120 in image sensor circuit 100. *Id.*, 7:37-41, 6:13-19, Fig. 3(B). “Insulation and metal lines (not shown) ... provide connections between metal contact pads 330 and the matrix of light-sensitive pixel regions 110 and control circuitry 120.” *Id.*, 6:19-22.

34. Each BSI image sensor further has a die-sized section 410-1 of a **protective substrate 410** secured to the frontside surface of **die 300-1** by an **adhesive region 420-1**, a die-sized section of a **transparent substrate 440**

secured to the backside surface of **die 300-1** by an **adhesive region**, and **metal leads 460** formed over die-sized section 410-1 and “connected to **metal contact pads 330** of each image sensor circuit 100 to facilitate signal between each image sensor circuit 100 and an external system (not shown).” *Id.*, Figs. 4(H), (I), 8:26-29, 8:31-33, 8:10-13.

35. As explained below, a BSI CMOS image sensor with the above structures and components was already known and used in the art.

A. Claims

36. The '319 patent has 6 claims. I understand that claims 1-6 are the Challenged Claims, with claim 1 the only independent claim.

37. For convenience, I have reproduced independent claim 1 below and have annotated it with the element numbering that is used in the claim mapping below.

- Preamble: “A backside illuminated image sensor comprising:”
- Element [1a]: “a semiconductor substrate having a first surface and a second surface;”
- Element [1b]: “a plurality of light-sensitive pixel regions formed on the first surface of the semiconductor substrate and including a photodiode diffusion region extending into the semiconductor substrate from the first surface;”

- Element [1c]: “a metal line formed adjacent the first surface of the semiconductor substrate;”
- Element [1d]: “a protective substrate secured to the semiconductor substrate such that the metal line is located between the protective substrate and the semiconductor substrate; and”
- Element [1e]: “a transparent substrate secured to the second surface of the semiconductor substrate such that the semiconductor substrate is sandwiched between the transparent substrate and the protective substrate;”
- Element [1f]: “wherein the semiconductor substrate has a thickness defined such that the light-sensitive pixel region is effectively exposed through the second surface.”

V. OVERVIEW OF THE TECHNOLOGY

A. CCD and CMOS Image Sensors

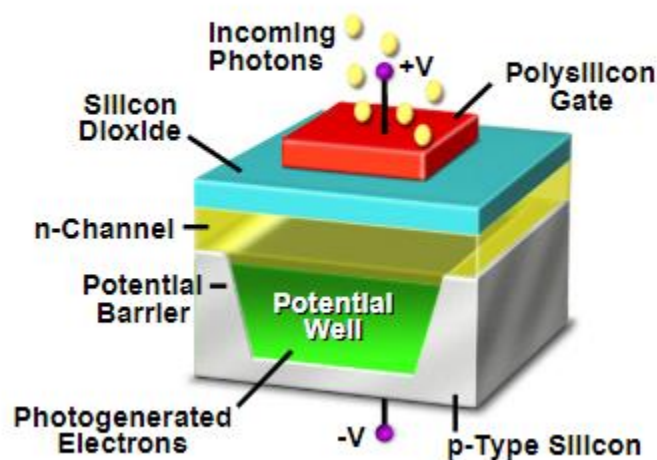
38. Charge-coupled devices (“CCD”) and complementary metal-oxide semiconductor (“CMOS”) image sensors are ubiquitous and typically used in devices that output digital recordings of images. One category of such devices is digital cameras. “At the core of a digital camera is a semiconductor device (CCD) or ... CMOS[], which measures light intensity and colour (using different filters) transmitted through the camera’s lenses. When light strikes the individual light

receptors, or pixels, on the semiconductor, an electric current is induced and is translated into binary digits for storage within another digital medium, such as flash memory” Ex. 1030. It was common knowledge that such image sensors would have “a matrix of pixels comprising light sensitive elements [that] constitute[] an image sensor.” Ex. 1024, 1:34-41; Ex. 1038, Abstract.

1. CCDs

39. CCDs were developed in the late 1960s and were the first practical way to let a light-sensitive silicon chip store an image and then digitize it.” Ex. 1031. A CCD sensor is “made up of pixels, each of which is a MOS (metal-oxide semiconductor) capacitor.” *Id.* An illustrative MOS capacitor is shown below:

Figure 2 - Metal Oxide Semiconductor (MOS) Capacitor



Ex. 1033.

40. “As the light falls on each pixel, the photons become electrons ... when photons of light hit the silicon of the pixel and knock electrons out of place.”

Ex. 1031. The electrons are stored in a MOS capacitor or “bucket,” where the charge, or amount of electrons in the bucket, corresponds to the amount of light that has hit that pixel. *Id.* Then, the charge in each row is shifted or transferred from one MOS capacitor to the next down the line until they reach an amplifier and other readout circuitry that convert the analog measurement into a digital value, resulting in a digital grid that describes the image. *Id.*

41. CCDs “were attractive because only three electrodes were required per pixel to make them operate.” Ex. 1013, 6. Initially, “CCD became dominant [to CMOS], primarily because they gave far superior images with the fabrication technology available.” Ex. 1032.

2. CMOS Image Sensor (CIS)

42. CIS were developed around the same time as CCDs but did not become dominant until the 1990s. Ex. 1013, 6; Ex. 1035, 136-137. A CIS may be comprised of “a photodiode and a CMOS transistor switch for each pixel, allowing the pixel signals to be amplified individually. By operating the matrix of switches, the pixel signals can be accessed directly and sequentially.” Ex. 1034; Ex. 1016, 2; Ex. 1029, 2:9-41; Ex. 1037; Ex. 1045, 35; Ex. 1046, 2:58-3:4; Ex. 1047, B1.1.

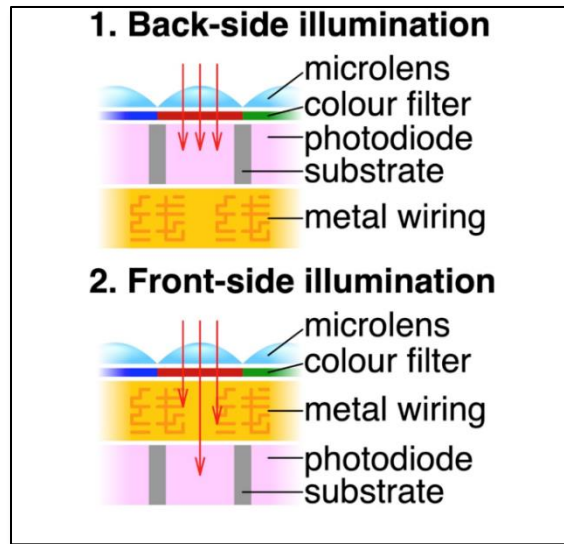
While CIS offered certain advantages over CCDs, such as “smaller size, faster frame rate, lower power consumption, and lower production cost,” they “required more uniformity and smaller features than silicon wafer foundries could deliver at

the time.” Ex. 1032; Ex. 1023. Only when microlithography techniques advanced to the point where “pixel size is determined more by scientific imaging optics in the 1990’s than by microlithography constraints” did CIS start becoming more mainstream. Ex. 1013, 6. Indeed, since “[t]he technology push of the semiconductor industry has driven microlithography to the sub-micron regime, and 1.25 micron CMOS is practically an industry standard,” “the fundamental advantage CCDs had over any other imaging technology has been eclipsed.” *Id.*

43. Similarly, the ’319 patent also describes that “CMOS image sensors first appeared in 1967,” but that charge coupled devices (CCDs) “have prevailed since their invention in 1970” due to “their superior dynamic range, low fixed-pattern noise (FPN), and high sensitivity to light.” Ex. 1001, 1:22-32. CMOS image sensors only “[m]ore recently ... gained in popularity” due to “advances in CMOS technology. *Id.*, 1:33-54.

3. Frontside Illumination (“FSI”) v. Backside Illumination (“BSI”) CCD

44. There are two fundamental design choices for image sensors: frontside illuminated (FSI) and backside illuminated (BSI). Ex. 1015, 13; Ex. 1017, 428. The difference between a BSI image sensor and a front-side illuminated (FSI) image sensor is the arrangement of imaging elements in the sensor with respect to incident light to the pixel, as shown in the image below:



Ex. 1043 (colors and annotations in original).

45. One important metric for image sensors is quantum efficiency, i.e., “the measure of the effectiveness of an imaging device to convert incident photons into electrons.” Ex. 1018. BSI, as opposed to FSI, allows the image sensors to achieve high quantum efficiency, which is a “desirable feature[.]” Ex. 1019, 1:10-17; Ex. 1020, 4:7-11 (“[O]ne objective of the present invention is to provide a method for fabricating thinned, back-illuminated, solid state image sensors that have an inherently high quantum efficiency over a broad spectral range.”); *see also* Ex. 1021, 2:26-30 (disclosing an “improved Metal Semiconductor Metal (MSM) photodiode device” where “frontside electrodes and backside illumination [is employed] to avoid active area shadowing in the device.”); Ex. 1037. Similarly, the ’319 patent also discloses that BSI CMOS image sensors “are alternative image sensor structures that address the fill factor problems associated with front

illumination.” Ex. 1001, 4:7-9, 3:53-58 (describing “fill factor” as “the ratio of light sensing area to total pixel areas”).

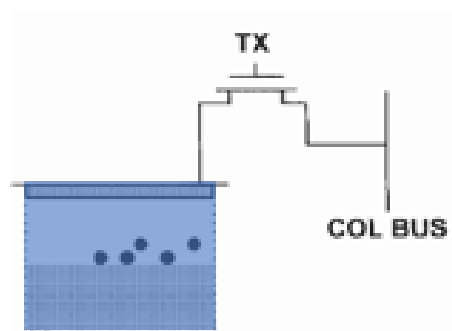
B. Pixel

46. There are three well-known CIS pixel implementations: photodiode-type passive pixel, photodiode-type active pixel, and photogate-type active pixel.

Ex. 1045, 1691. These are described below.

1. Photodiode-Type Passive Pixel

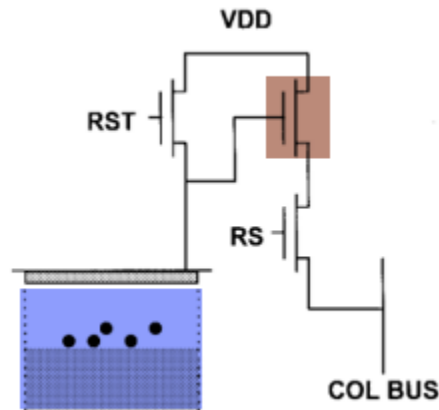
47. A photodiode-type passive pixel consists of a photodiode and a transistor. *Id.* A diagram of the photodiode-type passive pixel is shown below:



Id., Fig. 2 (annotated). The transfer (TX) transistor is activated to connect the **photodiode**, which is comprised of a photodiode diffusion region, to the column bus to sense photogenerated charge collected by the photodiode. *Id.*; Ex. 1046, 2:58-3:4; Ex. 1050. Photogenerated charge is read out without pixel-based amplification. Ex. 1036, 2.

2. Photodiode-Type Active Pixel / Photogate-Type Active Pixel

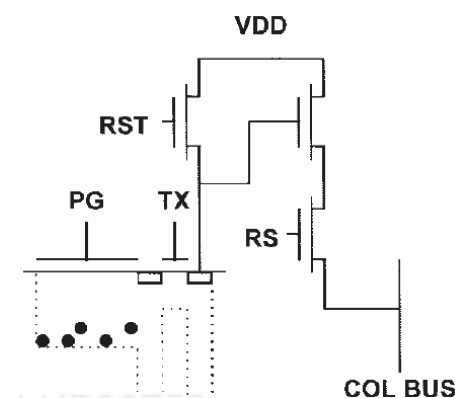
48. A photodiode-type active pixel consists of a photodiode and several transistors. Ex. 1036, 3. A diagram of the photodiode-type active pixel is shown below:



Ex. 1045, Fig. 4 (annotated). The voltage at the **photodiode** is buffered by the **source-follower transistor** to the column bus, which is selected by row select (RS) transistor, and the voltage at the **photodiode** is reset by the reset (RST) transistor. *Id.*; Ex. 1029, 2:9-41; Ex. 1037; Ex. 1048. This type of APS pixel is commonly referred to as a “3T pixel” because it uses three transistors to read out the voltage signal from the photodiode. *See also* Ex. 1001, 1:55-67, 3:11-15; Ex. 1042, 35.

3. Photogate-Type Active Pixel

49. A photogate-type active pixel consists of a photogate, a floating diffusion, and several transistors. Ex. 1045, Fig. 5. A diagram of the photogate-type passive pixel is shown below:



Id., Fig. 5. Photogenerated charge is collected under the photogate and then transferred to the floating diffusion. *Id.*, 4. The voltage at the floating diffusion is buffered by the source-follower transistor to the column bus, which is selected by row select (RS) transistor, and the voltage at the floating node is reset by the reset (RST) transistor. *Id.* Photodiodes provide high quantum efficiency. *Id.* Photogates, on the other hand, have less noise at low light but a lower fill factor and poorer blue light response and quantum efficiency. *Id.*

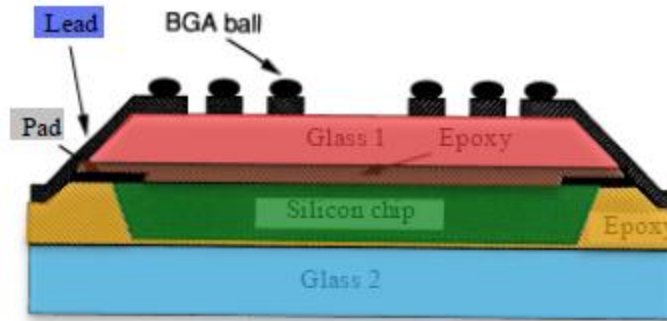
C. Removal of Material from Backside of Wafer

50. Removal of material from the backside of the wafer was well known before the priority date of the '319 patent. Namely, it was well-known that “[t]o overcome the attenuation problems of front-illuminated solid state image sensors, it has become *common practice to uniformly thin the silicon base layer* to a thickness on the order of 10 μm using conventional chemical etching techniques.” Ex. 1020, 2:10-22, 6:10-42; *see also* Ex. 1022, 14 (describing the wafer being “thinned at its non-active surface” using commercially available

grinding apparatus and/or etched using a conventional, commercially available Chemical-Mechanical Planarization (CMP) equipment); Ex. 1010, 144; Ex. 1009, ¶109, Fig. 6(b). Similarly, the '319 patent confirms that removing material from the backside of the wafer is a conventional technique. Ex. 1001, 4:45-50 (describing fabrication according to “well-established processing parameters”); see *also id.*, 6:61-7:4 (describing “coarse and fine grinding operations” “using known techniques”).

D. Wafer-Level Packaging

51. Wafer-level packaging of BSI image sensors based on conventional semiconductor process and standard semiconductor manufacturing equipment was well known. Ex. 1010, 144-146, Figs. 3, 5. For example, it was well-known to package a die with a protective shell comprised of glass plates at the top and bottom of the die. *Id.*, 144-146, Figs. 3, 5. It was also well-known to provide metal contact pads in between the top glass plate covering the top or active surface of the silicon die and the silicon die itself and to provide metal leads on the glass plate covering the active surface and that are connected the contact pads as part of this conventional packaging process. *Id.*, 144, 146, Figs. 3, 5. Sakai's Figure 3 illustrates the resulting packaged die, with the **silicon chip** sandwiched by **glass 1** and **glass 2** and the **pads** connected to the **electrical leads**:



Id., Fig. 3 (annotated).

VI. LEVEL OF ORDINARY SKILL IN THE ART

52. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the technology, the type of problems encountered in the art, and the prior art solutions to those problems.

53. In determining the characteristics of a hypothetical person of ordinary skill in the art of the '319 patent at the time of the alleged invention, I considered several things, including the type of problems encountered in this field, and the rapidity with which innovations were made. I also considered the sophistication of the technology involved, and the educational background and experience of those actively working in the field, and the level of education that would be necessary to understand the '319 patent. Finally, I placed myself back in the relevant periods of time, and considered the state of the art and the level of skill of the engineers working in this field in those times.

54. Based on the materials I have considered and my own experiences, it is my opinion that a person of ordinary skill in the art (“POSITA”) at the time of the alleged invention would have been a person having a bachelor’s degree in electrical engineering, material science, physics, or other related disciplines with at least three years of industry experience in integrated circuit design, layout, packaging or fabrication. A greater level of experience may compensate for less education and vice versa.

55. I also note that my opinions provided in this Declaration would not change in view of any minor modifications to this level of skill.

VII. CLAIM CONSTRUCTION

56. For purposes of this proceeding, the claim terms do not need to be construed to resolve the prior art issues presented in this Petition. This is because, as detailed below, each of the prior art grounds teaches, in relevant part, the exact same combination of features found in the ’319 patent.

VIII. OVERVIEW OF THE PRIOR ART

A. Nixon

57. I understand that Nixon claims priority to the ’144 Nixon Provisional, which includes an Invention Disclosure Technical Description (“IDTD”) and an article entitled “A CSP Optoelectronic Package for Imaging and Light Detection Applications” by Shweky et al. (“Shweky”). Shweky is incorporated in the ’144 Nixon Provisional as a prior art reference, upon which the IDTD claims an

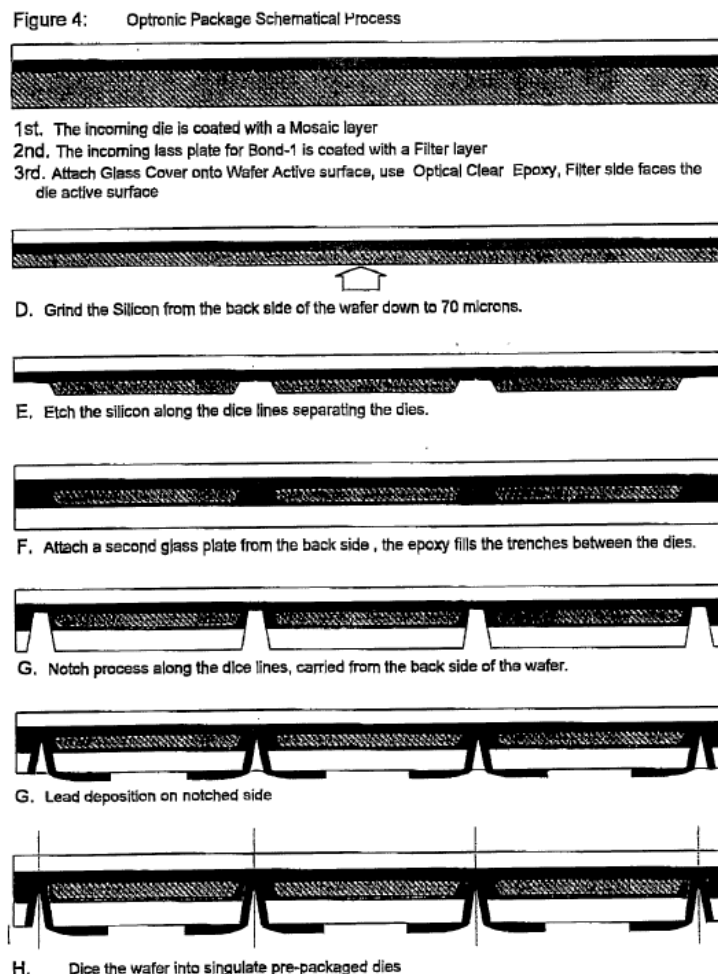
improvement using wafer level processing and packaging techniques for CMOS imaging, including its backside.

58. I was asked to analyze whether the '144 Nixon Provisional supports all aspects of the disclosures of the Nixon reference in this petition. It does. For example, claim 1 of Nixon is supported by the following portions of the '144 Nixon Provisional:

Nixon (Ex. 1004) Claim 1	Exemplary Support (Ex. 1006) '114 Prov.
1. A method...comprising:	IDTD, PDF pages 4-5, Figs. 1-2 Shweky, PDF pages 7-9, Fig. 4
attaching a first cover layer...a silicon wafer	IDTD, PDF pages 4-5, Figs. 1-2 Shweky, PDF pages 7-9, Fig. 4
attaching a second cover layer...the silicon wafer	IDTD, PDF pages 4-5, Figs. 1-2 Shweky, PDF pages 7-9, Fig. 4
notching...the second cover layer; and	IDTD, PDF pages 4-5, Fig. 1 Shweky, PDF pages 7-9, Fig 4
forming...the silicon wafer;	IDTD, PDF pages 4-5, Fig. 1 Shweky, PDF pages 7-9, Fig 4
wherein....from a back side.	IDTD, PDF pages 4-5, Fig. 1 Shweky, PDF pages 7-9, Fig 4

59. I am of the opinion that the '144 Nixon Provisional discloses this claim element of Nixon.

60. Specifically, the '144 Nixon Provisional discloses that the “essence of this disclosure,” among other things, is the “[b]ackside imaging using wafer level processing techniques to obtain thinning and integrated packaging of the image sensor.” Ex. 1005, IDTD, 4. Shweky’s Figure 4 also provides support for this limitation, as it illustrates a manufacturing process for image sensors:



Id., Shweky, Fig. 4.

Nixon [1a] attaching a first cover layer to an active surface of a silicon wafer;

61. I am of the opinion that the '144 Nixon Provisional discloses this claim element of Nixon.

62. Shweky discloses a process step of attaching a **(first) glass cover** to the active surface of a **wafer** in Figure 4:

Figure 4: Optronic Package Schematical Process



1st. The incoming die is coated with a Mosaic layer
2nd. The incoming lass plate for Bond-1 is coated with a Filter layer
3rd. Attach Glass Cover onto Wafer Active surface, use Optical Clear Epoxy, Filter side faces the die active surface

Ex. 1005, Shweky, 8, Fig. 4 (annotated). At the end of the manufacturing process, Shweky discloses dicing the wafer into packaged image sensors. *Id.*, 8, Fig. 4.

63. Relatedly, IDTD discloses each packaged image sensor has a **glass plate (first cover layer)** attached to the active surface (where **pixels** are located) of a **silicon die** in Figure 1:

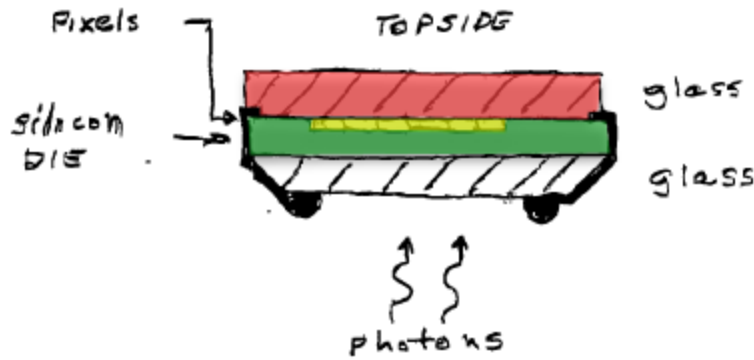


Figure 1.

Id., IDTD, 4-5, Fig. 1 (annotated).

Nixon [1b] attaching a second cover layer to an opposite surface of the silicon wafer;

64. I am of the opinion that the '144 Nixon Provisional discloses this claim element of Nixon.

65. Shweky discloses a process step of attaching a **second glass plate (second glass cover)** to the backside of the **wafer** in Figure 4:



F. Attach a second glass plate from the back side, the epoxy fills the trenches between the dies.

Ex. 1005, Shweky, 8, Fig. 4 (annotated).

66. Relatedly, IDTD discloses the resulting packaged image sensor has **another glass plate (second glass cover)** attached to the backside of the **silicon die** in Figure 1:

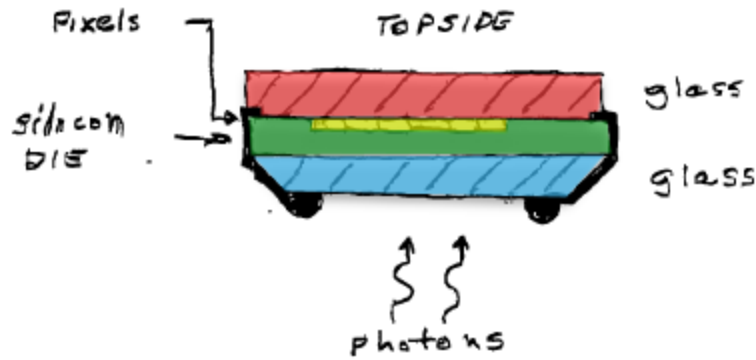


Figure 1.

Id., IDTD, 4-5, Fig. 1 (annotated).

Nixon [1c] notching the silicon wafer along the second cover layer; and

67. I am of the opinion that the '144 Nixon Provisional discloses this claim element of Nixon.

68. Shweky discloses that “[d]eep notches are drawn between the dice, so as to reveal the pads cross section.” Ex. 1005, Shweky, 8. Shweky further discloses the process step of forming **notches** along the backside of the **wafer** through the **second glass plate (second glass cover)** in Figure 4:



G. Notch process along the dice lines, carried from the back side of the wafer.

Id., Fig. 4 (annotated).

Nixon [1d] forming electrical interconnections on the notched surface of the silicon wafer;

69. I am of the opinion that the '144 Nixon Provisional discloses this claim element of Nixon.

70. IDTD discloses that conventionally, the bump contacts and interconnect lines are located on the backside of the wafer for FSI image sensors. Ex. 1005, IDTD, 4, Fig. 1. Shweky discloses a process step of depositing a metal layer “to contact the metal pads at their cross sections.” Ex. 1005, Shweky, 8. Figure 4 shows that **leads** are deposited on the notched sides of the **wafer**:



Id., Fig. 4 (annotated).

Nixon [1e] wherein the image sensor is light sensitive from a back side.

71. I am of the opinion that the '144 Nixon Provisional discloses this claim element of Nixon.

72. IDTD discloses the resulting packaged image sensor has “the ability to do backside imaging ... by 1) thinning the silicon ... and 2) relocating the ... bump contacts and interconnect lines away from the image area of the die and covering with optically transparent material to give support.” Ex. 1005, IDTD, 4-

5. IDTD's Figure 1 illustrates the packaged image sensor receiving photons from the backside:

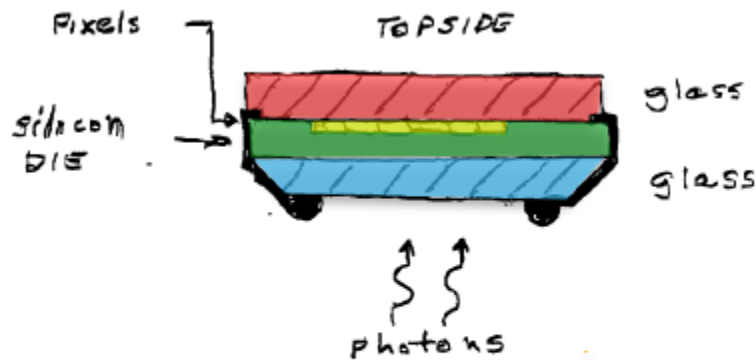


Figure 1.

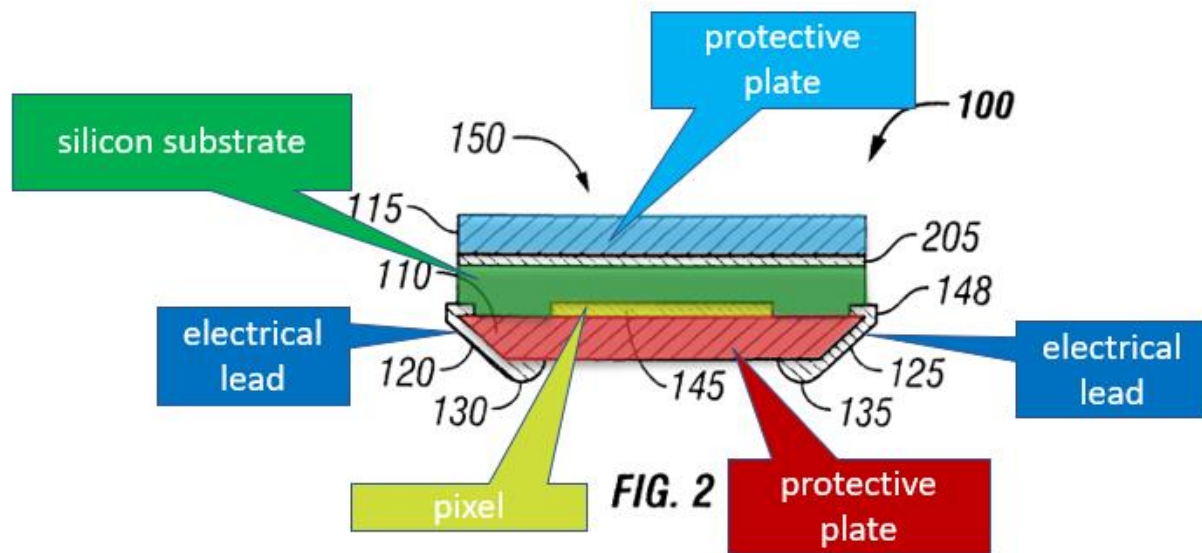
Id., Fig. 1 (annotated).

1. Overview of Nixon

73. Nixon discloses “the manufacturing of CMOS image sensors capable of backside illumination.” Ex. 1004, 1:8-10; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 7-8, Fig. 4. “[U]sing semiconductor manufacturing processes,” Nixon’s BSI CMOS image sensors are “packaged at the wafer level,” and “[t]he manufacturing process ... results in lower cost, particularly for smaller dies.” *Id.*, 1:65-2:1, 3:16-17. Nixon’s Figures 4A to 4G “illustrate[] the image sensor in various stages of formation.” *Id.*, 1:61-62. Nixon’s Figure 1 and 2 illustrate two embodiments of a BSI CMOS image sensor 100 and Nixon’s Figure 4 illustrates the manufacturing process for the image sensor 100 of Figures 1 and 2. *Id.*, 1:56-57, Figs. 1, 2, 4.

Both embodiments have a **silicon substrate 105** sandwiched between a **protective**

plate 110 and a **protective plate 115**. *Id.*, 2:1-3, Figs. 1, 2. **Pixels 145** are formed on the active surface of **silicon substrate 105** facing **protective plate 110**. *Id.*, 2:8-10, Figs. 1, 2. Protective plates **110** and **115** are made from glass plates. *Id.*, 2:26-28, 2:49-52. The embodiment in Figure 2 has **electrical leads 120, 125** and pads 130, 135 formed on **protective plate 110** at the frontside of image sensor 100 so light can enter unobstructed through **protective plate 115** at the backside of image sensor 100:



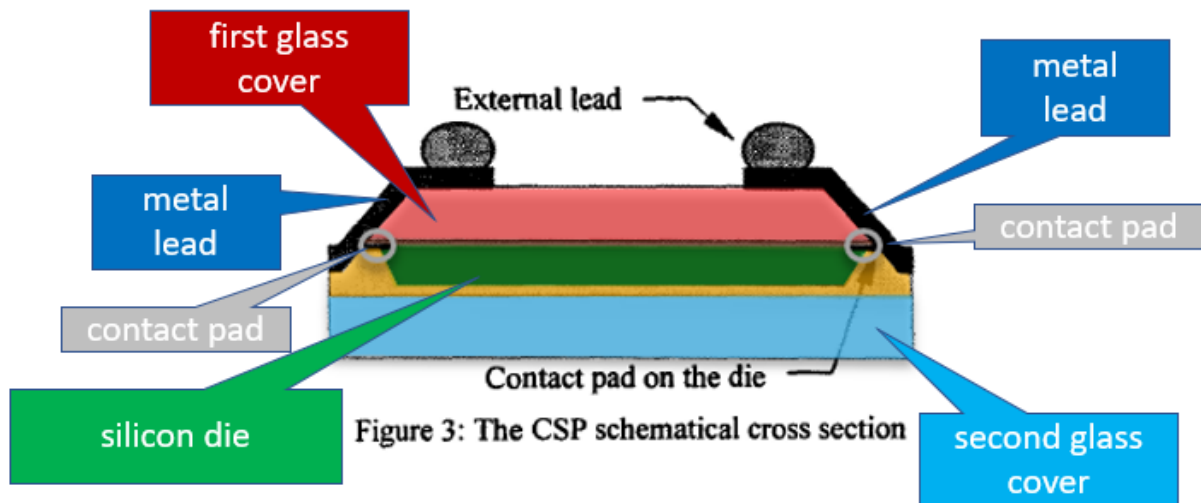
Id., Fig. 2 (annotated), 2:16-22. Both embodiments disclose notching in order to expose the metal pads 130, 135 to be connected with the electrical leads 120, 125, with Figure 1 illustrating notching from the protective plate 115 and Figure 2 illustrating notching from the protective plate 110. *Id.*, Figs. 1, 2, 1:65-2:10, 2:15-22.

B. Badihi

74. Badihi was published in the *Proceedings International Symposium on Advanced Packaging Materials, Processes, Properties and Interfaces*, which I am aware of. In my experience, Badihi, along with the other papers presented at that conference (and published in its proceedings), would have been available as of the publication of those proceedings.

75. Badihi discloses a ShellCase Chip Size Package (CSP) for, inter alia, BSI CMOS image sensors. Ex. 1101, 236, 239. Badihi's ShellCase CSPs are made with a "wafer-level packaging process ... can be accomplished with commercial [s]emiconductor wafer processing equipment" and be "based on [s]emiconductor processes." *Id.*, 236, 240. In particular, Badihi discloses bonding a first glass cover to the active side of a silicon wafer using epoxy adhesive, etching the backside of the silicon wafer to form grooves between the dies, and filling the grooves with inert material to bond a second glass layer to the backside of the silicon dies with adhesive. *Id.*, 237, Fig. 2. Then, deep notches are "drawn" (i.e., made) between the dies to reveal contact pads of the dies, and a metal layer is deposited in the notches and patterned by lithography to form individual leads connected to the contact pads. *Id.*, 237, Fig. 2. Finally, the wafer is diced, yielding individual packaged dies. *Id.*, 237, Fig. 2. The resulting "glass transparent package encases the Imager Die in a solid protecting optically clear enclosure." *Id.*, 239.

Badihi's Figure 3 illustrates the ShellCase CSP has a **silicon die** (e.g., an **imager die**) sandwiched between a **first glass cover** and a **second glass cover**, with the active side of the **silicon die** facing the **first glass cover**, **contact pads** formed on the active side of the **silicon die**, and **individuals metal leads** formed on the **first glass cover** to contact the **contact pads**:

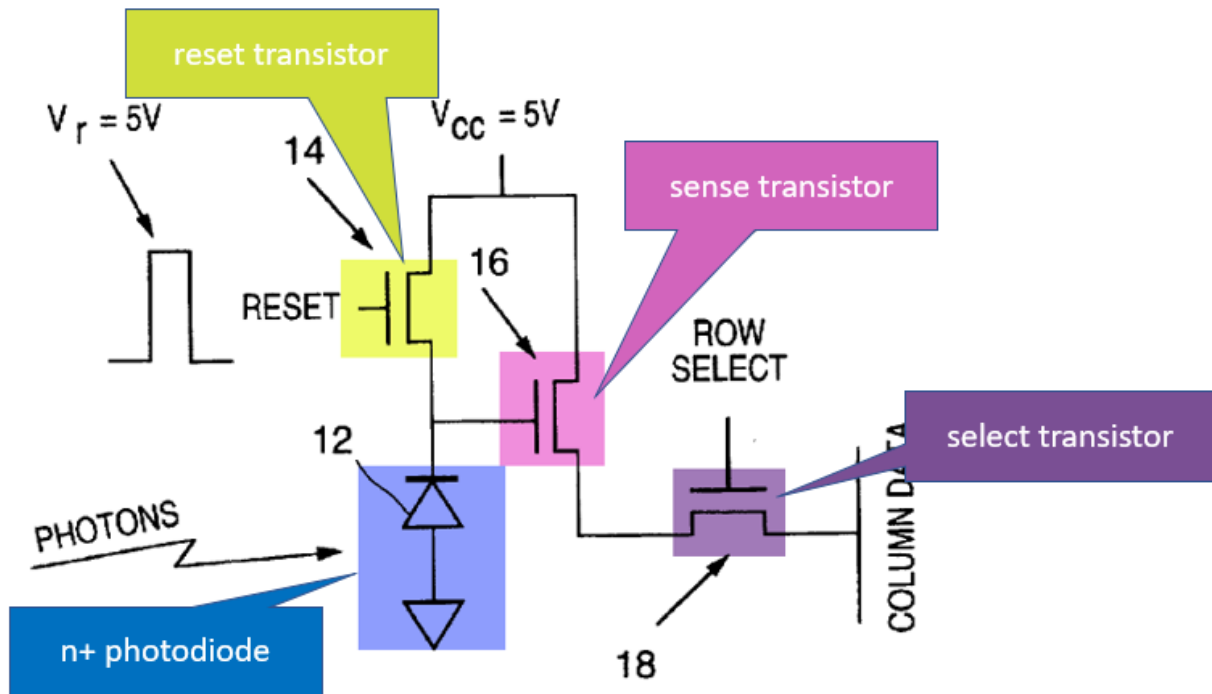


Id., Fig. 3; *see also id.*, 237, Fig. 2 (annotated). Badihi further discloses that the above ShellCase CSP package is a “glass transparent package [that] encases the [i]mager [d]ie in a solid protecting optically clear enclosure,” including, for example, packaged CMOS APS shown in Badihi's Figure 4. *Id.*, 239, Fig. 4.

C. Merrill

76. Merrill teaches a prior art “conventional CMOS active pixel sensor cell 10” shown in Figure 1. Ex. 1049, 1:42-43. Merrill's Figure 1 discloses a CMOS APS cell 10 that “includes a photodiode 12, a **reset transistor 14**, whose

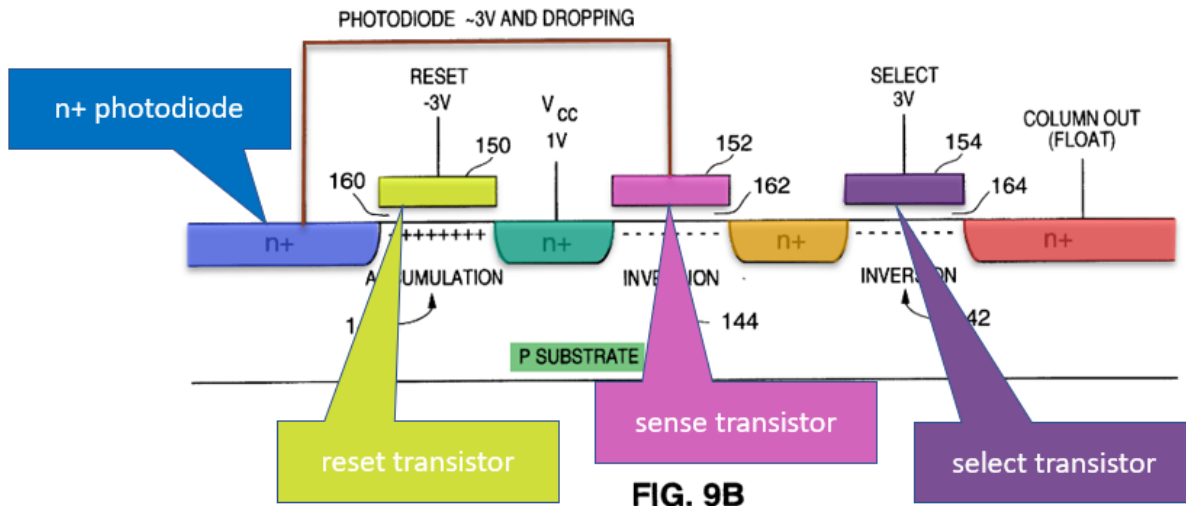
source is connected to photodiode 12, a **sense transistor 16**; whose gate is connected to photodiode 12, and a **select transistor 18**, whose drain is connected in series to the source of **sense transistor 16**”:



Ex. 1049, 1:38-44, Fig. 1 (annotated). A POSITA would understand that CMOS APS cell 10 is a 3T pixel because it uses three transistors to read out the voltage signal from photodiode 12.

77. Merrill’s Figure 9B illustrates a cross-sectional view of CMOS APS cell 100, which “implements the schematic representation of cell 10,” with an **n+ photodiode 140** and a **reset transistor 14** for which “**reset line 150** functions as the lead-in and gate,” a **sense transistor 16** for which “**local interconnect line 152** forms the gate,” and a **select transistor 18** for which “**select line 154** functions as

the lead-in and gate,” with n+ regions for **photodiode 140** and sources and drains for the transistors:



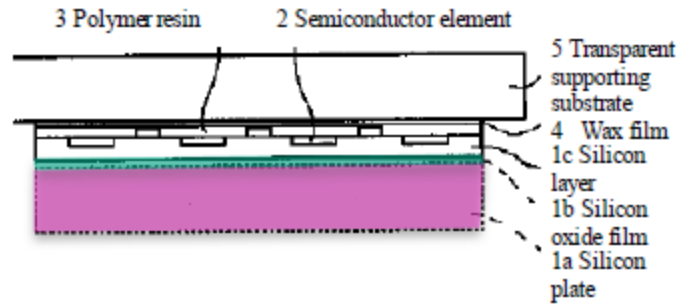
Ex. 1049, 1:39-44, 3:43-45, 5:13-17, 5:56-68, 6:6-8, 6:25-27, Figs. 1, 9B

(annotated).

D. Watanabe

78. Watanabe discloses a manufacturing method for thinning a CMOS infrared detector (*i.e.*, image sensor), where the substrate 1 is initially comprised of silicon plate 1a, silicon oxide film 1b, and silicon layer 1c. Ex. 1007, Abstract, ¶17. First, an insulator (SOI) substrate 1 with a **silicon plate 1a**, **silicon oxide film 1b**, and a silicon layer 1c is provided, and semiconductor elements 2 are formed on silicon layer 1c. *Id.*, Fig. 2(c), ¶17. SOI substrate 1 is bonded to a transparent supporting substrate 5, and then **silicon oxide film 1b** and silicon layer 1c are removed from the backside of SOI substrate 1:

(c) Polishing the silicon plate (1a) and etching the silicon oxide film (1b)



Id., Fig. 2(c) (annotated), Abstract, ¶¶18, 19.

IX. SPECIFIC GROUNDS FOR PETITION

79. I am of the opinion that the Challenged Claims of the '319 patent are invalid on the following grounds:

Grounds	Claims	Statutory Basis	Prior Art
1	1, 2, 5, and 6	§103	Nixon
2	3	§103	Nixon and Merrill
3	4	§103	Nixon and Watanabe
4	1, 2, 5, and 6	§103	Badihi
5	4	§103	Badihi and Watanabe
6	1, 2, 3, 5, and 6	§103	Merrill and Badihi
7	4	§103	Merrill, Badihi, and Watanabe

80. None of these references relied upon were before or considered by the Examiner during prosecution of the '319 patent. Further, none of the Grounds above relies on prior art reference combinations that were evaluated during prosecution of the '319 patent.

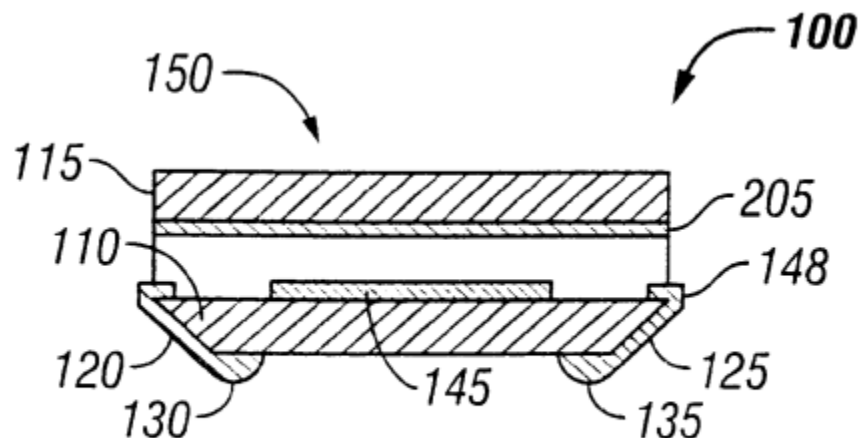
81. I am of the opinion that Nixon renders obvious claims 1, 2, 5, and 6 of the '319 patent.

1. Claim 1

[1pre] A backside illuminated image sensor comprising:

82. To the extent the preamble is considered to be a limitation, I am of the opinion that Nixon discloses this claim element.

83. Nixon discloses that “[t]his invention related to image sensors, and more particularly to the manufacturing of CMOS image sensors capable of backside illumination,” such as BSI CMOS image sensors 100 (*i.e.*, ***a backside illuminated image sensor***). Ex. 1004, 1:8-10, Abstract, Figs. 1, 2, 4A-4G; Ex. 1005, IDTD, 4-5, Fig. 1, Shweky, 7-9, Fig. 4. Figure 2 of Nixon illustrates image sensor 100:



Ex. 1004, Fig. 2; Ex. 1005, IDTD, Fig. 2.

[1a] a semiconductor substrate having a first surface and a second surface;

84. I am of the opinion that Nixon discloses this claim element.

85. Nixon's silicon substrate 105 corresponds to the claimed "semiconductor substrate." Nixon discloses "image sensor [100] includes a thin silicon substrate 105 which is sandwiched ... on the top and bottom sides" (*i.e.*, **semiconductor substrate having a first surface and a second surface**). Ex. 1004, 1:65-2:10; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8-9, Figs. 3, 4. Nixon's Fig. 2 illustrates **silicon substrate 105** with a **protective plate 110** facing **top surface 148** and a **protective plate 115** facing the bottom surface:

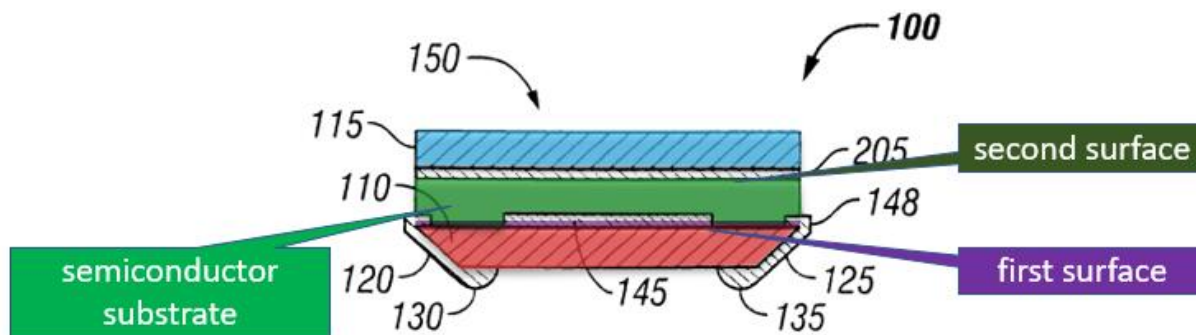


FIG. 2

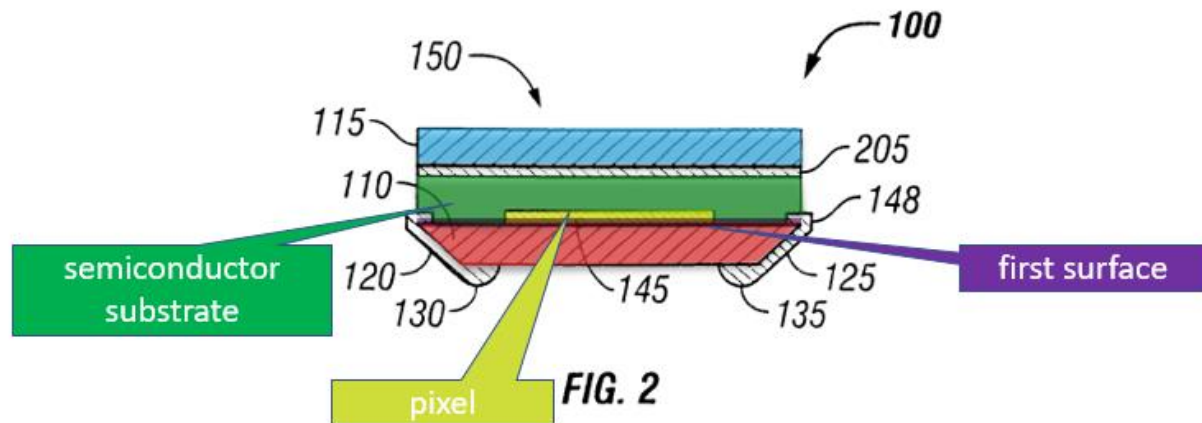
Ex. 1004, Fig. 2 (annotated); Ex. 1005, IDTD, Fig. 2.

[1b] a plurality of light-sensitive pixel regions formed on the first surface of the semiconductor substrate and including a photodiode diffusion region extending into the semiconductor substrate from the first surface;

86. I am of the opinion that Nixon discloses or renders obvious this claim element.

87. I am of the opinion that Nixon discloses or renders obvious “a plurality of light-sensitive pixel regions formed on the first surface of the semiconductor substrate.” Nixon discloses silicon substrate 105 and top surface 148 that correspond to the claimed “semiconductor substrate” and “first surface,” respectively. *See supra*, claim 1a. Nixon discloses that image sensor 100 has “[p]ixels 145 ... positioned at the top surface 148 of the silicon substrate 105” (*i.e.*, ***a plurality of light-sensitive pixel regions formed on the first surface of the semiconductor substrate***). Ex. 1004, 2:8-9; Ex. 1005, IDTD 4, Fig. 2, Shweky, 8, Figs. 3-4; *see supra*, §V.A.

88. Nixon also discloses or renders obvious “a plurality of light-sensitive pixel regions ... including a photodiode diffusion region extending into the semiconductor substrate from the first surface.” Nixon’s Figure 2 illustrates **pixels 145** extending into **silicon substrate 105** from **top surface 148** (*i.e.*, ***first surface***):



Ex. 1004, Fig. 2 (annotated); Ex. 1005, IDTD, Fig. 2.² Pixels 145 are CMOS pixels because they are part of CMOS image sensor 100 made with CMOS process. A POSITA at the time of the invention would readily understand CMOS pixels would have been implemented as one of three known and available options: (1) passive pixels with photodiodes; (2) active pixels with photodiodes; or (3) active pixels with photogates. *See supra*, §V.B.

89. Using any one of the three well-known and available CIS pixel implementations would have been a simple design choice for a POSITA. Moreover, using any of these three CIS pixel implementations would not change

² Nixon's Figures 4A to 4G "illustrate[] the image sensor in various stages of formation." Ex. 1004, 1:61-62. Nixon's Figure 2, described as "an image sensor including a color filter array according to the present invention," illustrates an embodiment created using the process depicted in Figures 4A to 4G. *Id.*, 1:56-57.

the nature of claimed invention, which would remain a BSI image sensor. In fact, the '319 patent recognizes its invention is applicable to passive pixels and active pixels with photodiode or photogates. Ex. 1001, 6:1-3. (“[T]he methods and structures described below may also be used to produce passive CMOS image sensors and CMOS APS utilizing photogate light sensitive regions.”). It is simply a matter of common sense and well within the capabilities of a POSITA to include APS with photodiodes in a CMOS image sensor given the known problem of fill factor. *See supra*, §§V.A-B. Thus, it would have been a matter of routine, design choice to implement Nixon’s pixels 145 as ***active pixels with photodiodes***, which includes ***photodiode diffusion regions***. *See supra*, §§V.A-B. A POSITA would also readily understand that Nixon’s pixels 145 are in the silicon substrate, and therefore their photodiode diffusion regions would also extend into the silicon substrate (*i.e.*, ***photodiode diffusion region extending into the semiconductor substrate from the first surface***). *See supra*, §§V.A-C.

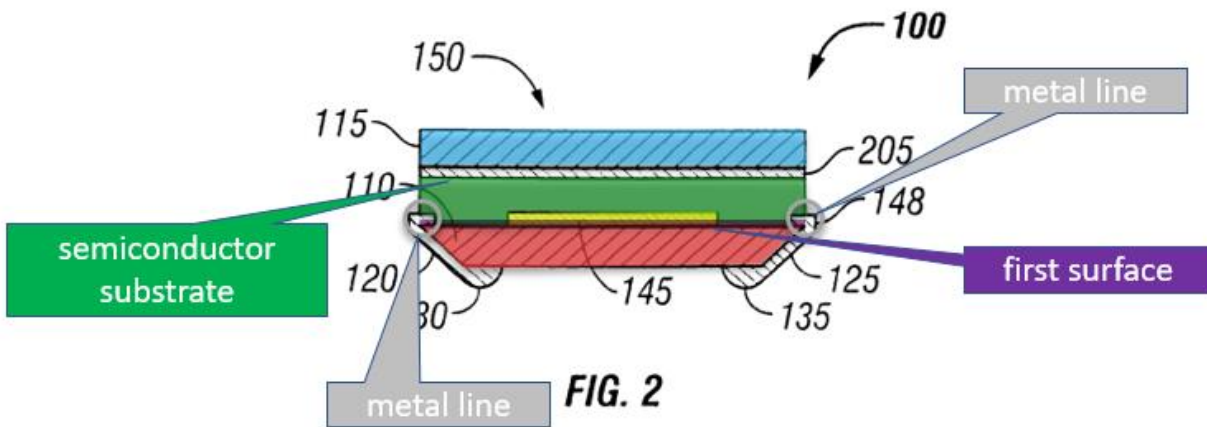
[1c] a metal line formed adjacent the first surface of the semiconductor substrate;

90. I am of the opinion that Nixon discloses or renders obvious this claim element.

91. Nixon’s metal pads correspond to the claimed “metal line.” Ex. 1004, 2:6-8, 2:20-22; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8, Fig. 4. Nixon discloses

drawing deep notches between the dies to expose the cross-sections of each of the metal pads. Ex. 1004, 2:58-61; Ex. 1005, IDTD 4-5, Fig. 2, Shweky, 8, Fig. 4.

Nixon's Figure 2 illustrates the **metal pads** that are formed adjacent to **top surface 148** of **silicon substrate 105** (i.e., *a metal line formed adjacent the first surface of the semiconductor substrate*):



Ex. 1004, Fig. 2 (annotated); Ex. 1005, IDTD, Fig. 2.

92. To the extent the Patent Owner argues that a metal line is not expressly disclosed in Nixon, a POSITA would readily understand that Nixon's CMOS image sensor 100 includes the claimed "metal line." This is because pixels 145 extend into top surface 148 of silicon substrate 105 and the electrical signals generated by the collected charges must be transmitted from pixels 145 to the outside world. Ex. 1004, 2:8-9; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8. A POSITA would have understood that the only way to transmit these charges is via

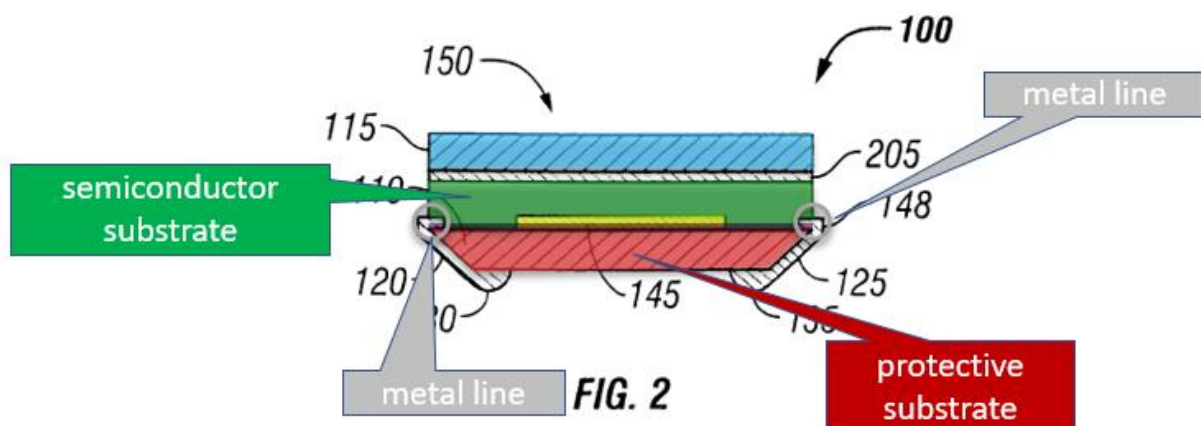
metal lines formed where pixels 145 are located, which are adjacent to top surface 148 of silicon substrate 105. *See supra*, §V.D; *see also* Ex. 1010, 146, Fig. 3.

[1d] a protective substrate secured to the semiconductor substrate such that the metal line is located between the protective substrate and the semiconductor substrate; and

93. I am of the opinion that Nixon discloses this claim element.

94. Nixon’s protective plate 110 corresponds to the claimed “protective substrate.” Ex. 1004, 2:1-6; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8, Fig. 4.

Nixon discloses that image sensor 100 has an epoxy adhesive layer attaching the silicon substrate 105 to the protective plate 110 (*i.e.*, **a protective substrate secured to the semiconductor substrate**). Ex. 1004, 2:1-6; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8, Fig. 4. Nixon further discloses metal pads (*i.e.*, **metal line**). *See supra*, claim 1c. The **metal pads** are located between **protective plate 110** and **silicon substrate 105** as shown in Nixon’s Figure 2:



Ex. 1004, Fig. 2 (annotated); Ex. 1005, IDTD, Fig. 2. Furthermore, it was conventional at the time of invention to place the metal line in between the semiconductor substrate and protective substrate. *See supra*, §V.D.

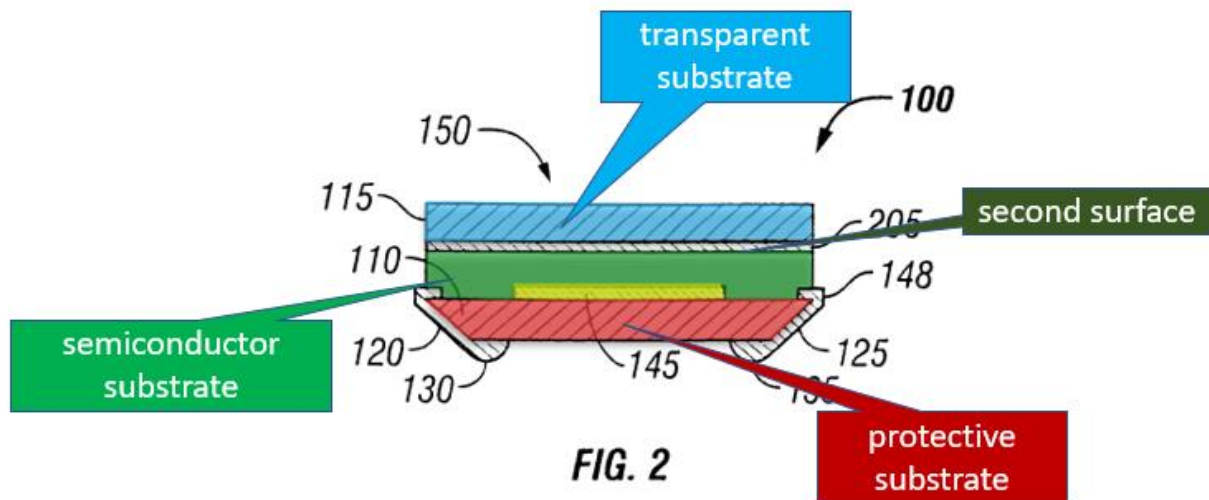
[1e] a transparent substrate secured to the second surface of the semiconductor substrate such that the semiconductor substrate is sandwiched between the transparent substrate and the protective substrate;

95. I am of the opinion that Nixon discloses this claim element.

96. Nixon’s protective plate 115 and glass plate 440 correspond to the claimed “transparent substrate.” Ex. 1004, 1:65-2:10, Abstract; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8, Fig. 4. Indeed, Nixon discloses fabricating and packaging a CMOS image sensor can be illuminated from the backside, where the “die is covered with an optically transparent material.” Ex. 1004, 1:37-47; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 7-8, Fig. 4 (expressly disclosing “[a]ttach[ing] a second glass plate from the back side”). Protective plate 115 is the resulting die-sized section of Nixon’s second glass plate 440, after it is diced to separate the dies. Ex. 1004, 1:37-47, 2:49-57; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 7-8, Fig. 4.

97. Nixon discloses “[a]n epoxy adhesive layer ... attaches the protective plates 110, 115 to the silicon substrate 105 and surrounds and protects the edges of the silicon 105” (*i.e.*, ***a transparent substrate secured to the second surface of the***

semiconductor substrate) and “a thin silicon substrate 105 ... is sandwiched between two thin protective plates 110, 115 on the top and bottom sides” (i.e., *the semiconductor substrate is sandwiched between the transparent substrate and the protective substrate*). Ex. 1004, 1:65-2:10; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8, Fig. 4. Nixon’s Figure 2 illustrates **silicon substrate 105** being sandwiched between **protective plate 110** and **protective plate 115**:



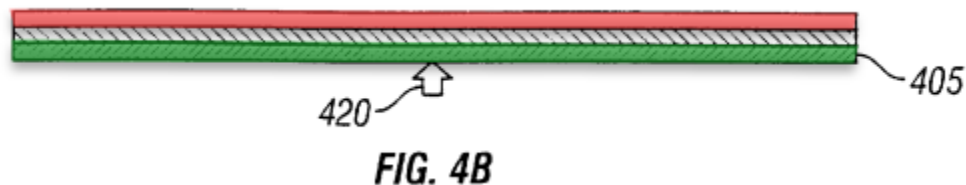
Ex. 1004, Fig. 2 (annotated); Ex. 1005, IDTD, Fig. 2.

[1f] wherein the semiconductor substrate has a thickness defined such that the light-sensitive pixel region is effectively exposed through the second surface

98. I am of the opinion that Nixon discloses this claim element.

99. Nixon discloses “grinding the silicon wafer from the opposite surface of the silicon wafer” to a “predetermined thickness” that “allows for the light sensitive area of the die 430 to be illuminated from . . . the back side” (i.e.,

*wherein the semiconductor substrate has a thickness defined such that the light-sensitive pixel region is effectively exposed through the second surface).*³ Ex. 1004, 2:36-41, 3:7-17, 1:37-39, 1:65-2:10; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8, Fig. 4. As an example, Nixon discloses an embodiment where “the silicon wafer 405 is ground to a thickness of approximately 70 microns” from its backside. Ex. 1004, 2:36-41; Ex. 1005, IDTD, 4-5, Shweky, 8 Fig. 4. Nixon’s Figures 4A-4G illustrate the process by which die 430 is formed from silicon wafer 405. Ex. 1004, Figs. 4A-4G; Ex. 1005, IDTD, Shweky, Fig. 4. Nixon’s Figure 4B illustrates grinding (indicated by arrow 420) of the back side of **silicon wafer 405** to achieve a thickness that would expose the light sensitive area of the **die 430** from the back side:



³ The '319 patent describes that “effectively exposing the light-sensitive pixel diffusions regions of the image sensor circuit through the backside surface” is achieved when the semiconductor substrate is thinned “until [it] is transparent to visible light.” Ex. 1001, 4:63-5:7. Nixon discloses what is described in the '319 patent.

Ex. 1004, Fig. 4B (annotated); Ex. 1005, Shweky, Fig. 4.

2. Claim 2

[2pre]. The backside illuminated image sensor according to claim 1, further comprising

100. I am of the opinion that Nixon discloses claim 2pre for the same reasons as claim 1 above.

[2a] a first adhesive layer located between the protective substrate and the semiconductor substrate, and

101. I am of the opinion that Nixon discloses this claim element.

102. Nixon's epoxy adhesive layer corresponds to the claimed "first adhesive layer." Ex. 1004, 2:3-6; Ex. 1005, Shweky, 7-8, Fig. 4. Nixon discloses that "[a]n epoxy adhesive layer ... [that] attaches the protective plates 110, 115 to the silicon substrate 105" and therefore is in between the silicon substrate 105 and protective plate 110 (*i.e.*, ***a first adhesive layer located between the protective substrate and the semiconductor substrate***). Ex. 1004, 2:3-6, Fig. 2; Ex. 1005, Shweky, 7-8, Fig. 4.

[2b] a second adhesive layer located between the transparent substrate and the semiconductor substrate.

103. I am of the opinion that Nixon discloses this claim element.

104. Nixon's epoxy adhesive layer corresponds to the claimed "second adhesive layer." Ex. 1004, 2:3-6; Ex. 1005, Shweky, 7-8, Fig. 4. Nixon discloses

that “[a]n epoxy adhesive layer ... [that] attaches the protective plates 110, 115 to the silicon substrate 105” and therefore is in between the silicon substrate 105 and protective plate 115 (*i.e.*, ***a second adhesive layer located between the transparent substrate and the semiconductor substrate***). Ex. 1004, 2:3-6, Fig. 2; Ex. 1005, Shweky, 7-8, Fig. 4.

3. Claim 5

[5pre] The backside illuminated image sensor according to claim 1,

105. I am of the opinion that Nixon discloses claim 5pre for the same reasons as claim 1 above.

[5a] wherein the transparent substrate is glass.

106. I am of the opinion that Nixon discloses this claim element.

107. Nixon discloses the transparent substrate is glass for the same reasons discussed above in connection with claim 1e. *See supra*, claim 1e.

4. Claim 6

[6pre]. The backside illuminated image sensor according to claim 1, further comprising

108. I am of the opinion that Nixon discloses claim 6pre for the same reasons as claim 1 above.

[6a] a plurality of metal leads formed on the protective layer.

109. I am of the opinion that Nixon discloses this claim element.

1. Reasons to Combine Nixon with Merrill

112. A POSITA would have been motivated to modify Nixon's manufacturing process for a BSI CMOS image sensor to include the CMOS APS employing photodiodes as taught by Merrill. Nixon discloses a BSI CMOS image sensor with pixels 145 on the active surface of the silicon die. Ex. 1004, 2:8-9; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8. Nixon, however, does not disclose the specific circuitry and structure of pixel 145 to read out the potential from the collected photons. By the priority date of the '319 patent, there were three well-known options for designing a CMOS image sensor to collect and read out the potential from the collected photons: passive pixel with photodiode, active pixel with photodiode, and active pixel with photogate. *See supra*, §V.B. The use of APS with photodiodes in such pixels was one of those well-known, conventional choices, and as such would have simply been a design choice for a POSITA to implement. *Id.*

113. Merrill discloses a CMOS APS image sensor cell and teaches the arrangement of the various elements in a CMOS APS. Ex. 1049, 6:13-18. Further, Merrill's CMOS APS performs three steps, all of which were conventional by the time of the '319 patent: "a reset step, where cell 100 is reset from the previous integration cycle; an image integration step, where the light energy is collected and converted into an electrical signal; and a signal readout step, where the signal is

read out.” Ex. 1049, 6:13-18. A POSITA would have naturally looked to Merrill’s CMOS APS with “a conventional photodiode ... typically combined with a number of active transistors” to modify Nixon’s manufacturing process for a BSI CMOS image sensor. *Id.*, 1:31-45; *see supra*, §§V.A-B, D. Accordingly, it would have been obvious to a POSITA to utilize a CMOS APS structure, such as the one taught by Merrill, because it would be a mere routine design choice that a POSITA would readily understand how to implement using conventional CMOS manufacturing techniques. *See supra*, §§V.A-B, D.

114. Merrill’s CMOS APS is readily applicable to Nixon’s manufacturing process, and a POSITA could have modified Nixon’s manufacturing process to include fabrication of a CMOS APS such as taught in Merrill with a reasonable expectation of success. *See supra*, §§V.A-B, D. The CMOS APS sensor of Merrill would be simply fabricated on a separate silicon wafer, which would replace one-for-one Nixon’s substrate 105. Such a modification to Nixon’s manufacturing process would have merely required using one of the three well-known options for designing CMOS image sensors at the time. *See supra*, §V.B. A POSITA would have also been further motivated to combine the low fill factor CMOS APS of Merrill with Nixon’s BSI scheme and substrate thinning, because the unobstructed illumination of the photodiode region would improve sensitivity and prevent noise from scattered light. *See supra*, §§V.A-C.

2. Claim 3

[3pre] The back-illuminated image sensor according to claim 2, wherein each of the plurality of light-sensitive pixel regions further comprises:

115. I am of the opinion that Nixon discloses claim 3pre for the same reasons as claim 2 above.

[3a] a second diffusion region that is formed in the semiconductor substrate and spaced from the photodiode diffusion region;

116. I am of the opinion that Nixon combined with Merrill renders obvious this claim element.

117. Nixon discloses a fabrication and packaging process for a CMOS image sensor with a silicon substrate 105 corresponding to the claimed “semiconductor substrate.” Ex. 1004, 1:37-47, 1:65-2:10; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8, Fig. 4.

118. Merrill’s n+ photodiode 140 corresponds to the claimed “photodiode diffusion region” and the n+ active region that “functions as the drains for reset transistor 14 and sense transistor 16” corresponds to the claimed “second diffusion region. Ex. 1049, 5:9-23, 5:56-68, 6:41-43. Merrill further discloses that the APS cell 100 “is formed on a substrate 110 ... that encloses a plurality of active regions within substrate 100.” *Id.*, 2:63-3:1. Merrill’s Figure 9B illustrates that **n+ active region** is formed in **substrate 110** and spaced from **n+ photodiode 140** (*i.e.*, a

second diffusion region that is formed in the semiconductor substrate and spaced from the photodiode diffusion region):

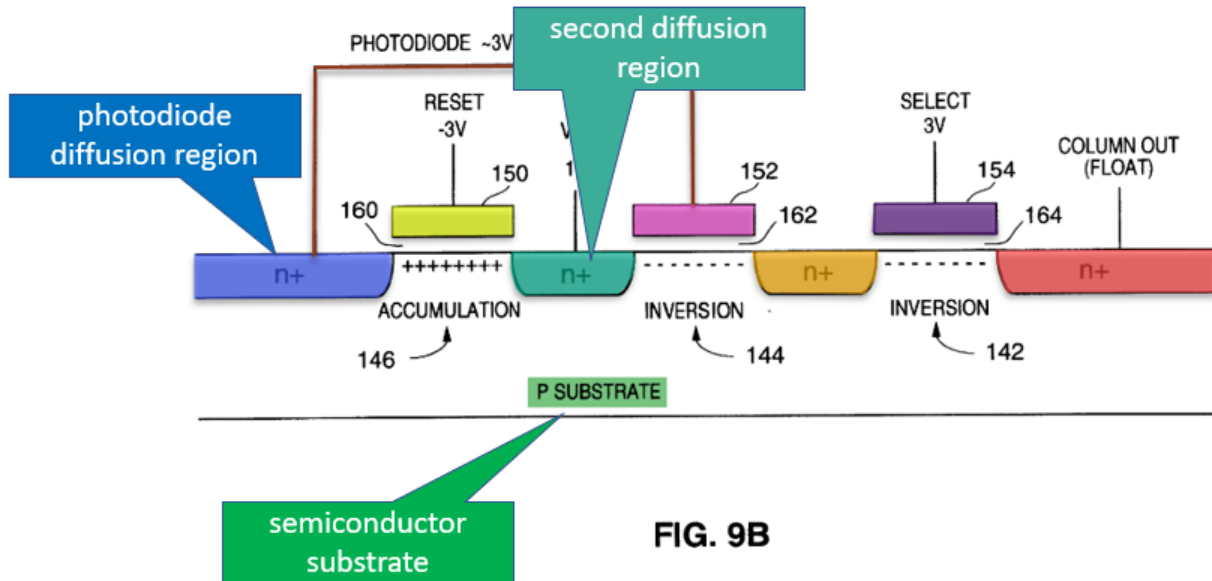


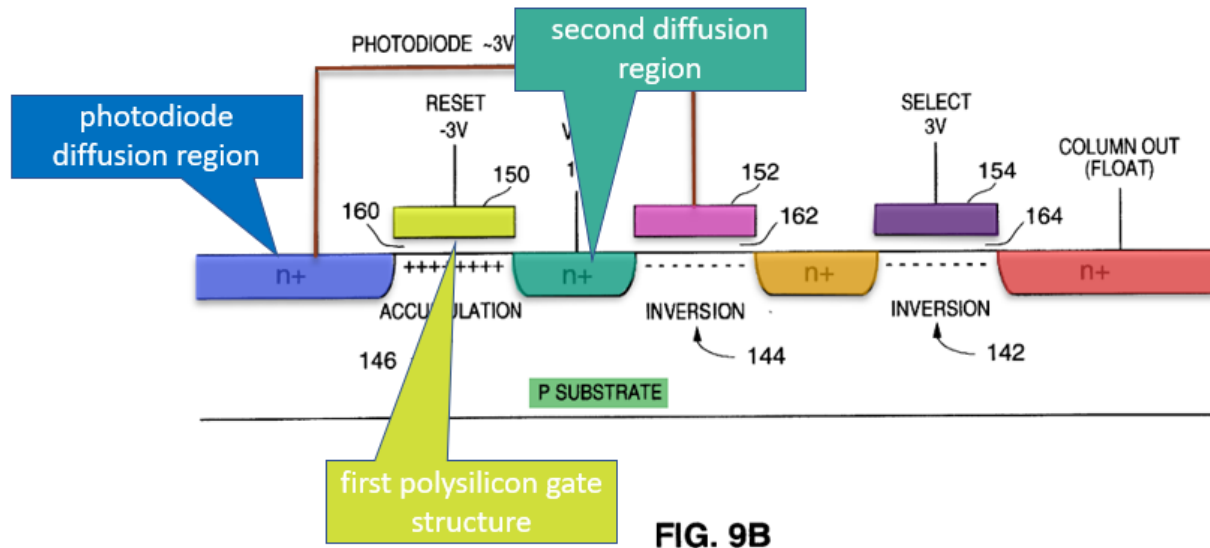
FIG. 9B

Id., Fig. 9B (annotated).

[3b] a first polysilicon gate structure provided between the second diffusion region and the photodiode diffusion region;

119. I am of the opinion that Merrill renders obvious this claim element.

120. Merrill's reset line 150, which is polysilicon, and reset transistor 14 correspond to the claimed "first polysilicon gate structure." Ex. 1049, 5:47-58. Merrill's Figure 9B illustrates that the **reset line 150**, serving as the gate of **reset transistor 14** (not labeled), is provided between the **n+ active region** and **n+ photodiode 140** (i.e., *a first polysilicon gate structure provided between the second diffusion region and the photodiode diffusion region*):

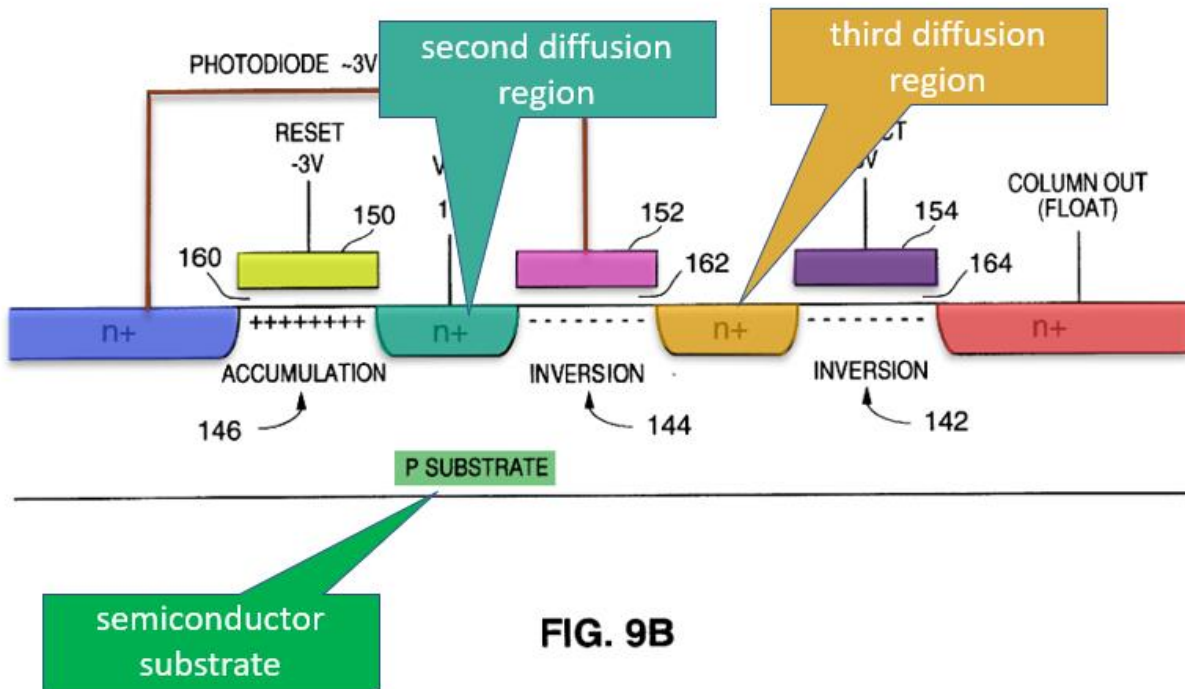


Id., Fig. 9B (annotated).

[3c] a third diffusion region that is formed in the semiconductor substrate and spaced from the second diffusion region;

121. I am of the opinion that Merrill renders obvious this claim element.

122. Merrill's other n⁺ active region that "functions as the source of sense transistor 16 and the drain of select transistor 18" corresponds to the claimed "third diffusion region." Ex. 1049, 5:18-23. Merrill's Figure 9B illustrates the **other n⁺ active region** that is formed in **substrate 110** and spaced from the **n⁺ active region** (i.e., *a third diffusion region that is formed in the semiconductor substrate and spaced from the second diffusion region*):



Id., Fig. 9B (annotated).

[3d] a second polysilicon gate structure that is provided between the second diffusion region and the third diffusion region;

123. I am of the opinion that Merrill renders obvious this claim element.

124. Merrill's local interconnect line 152, which is polysilicon, and sense transistor 16 correspond to the claimed "second polysilicon gate structure." Ex. 1049, 5:59-67. Merrill's Figure 9B illustrates that **local interconnect line 152**, serving as the gate of **sense transistor 16** (not labeled), is provided between the **n+ active region** and **other n+ active region** (i.e., *a second polysilicon gate structure that is provided between the second diffusion region and the third diffusion region*):

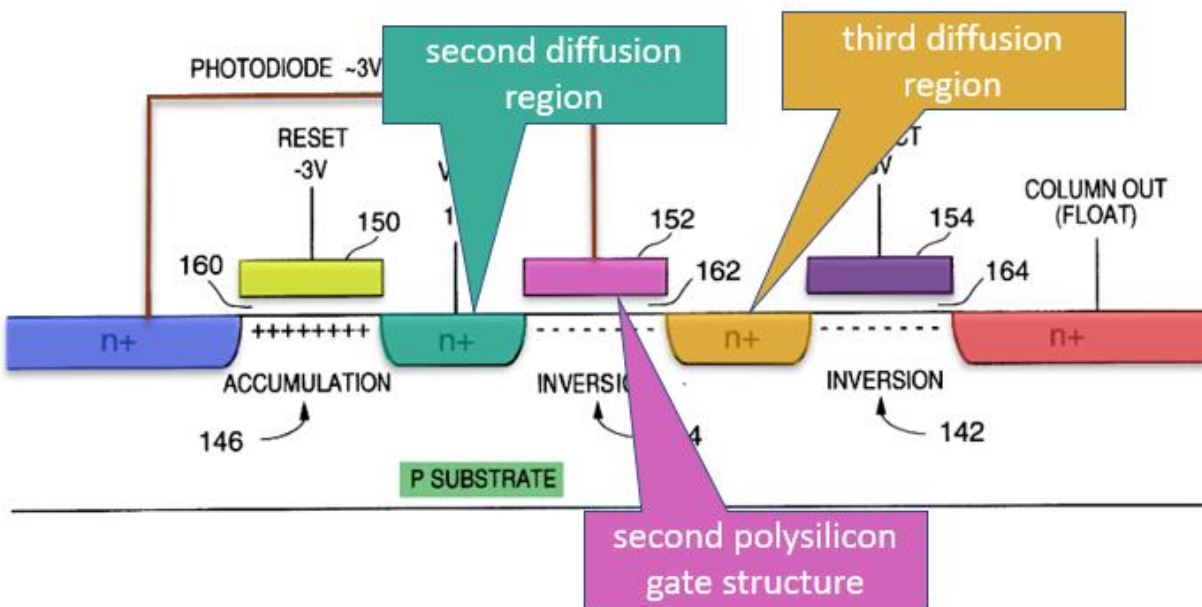


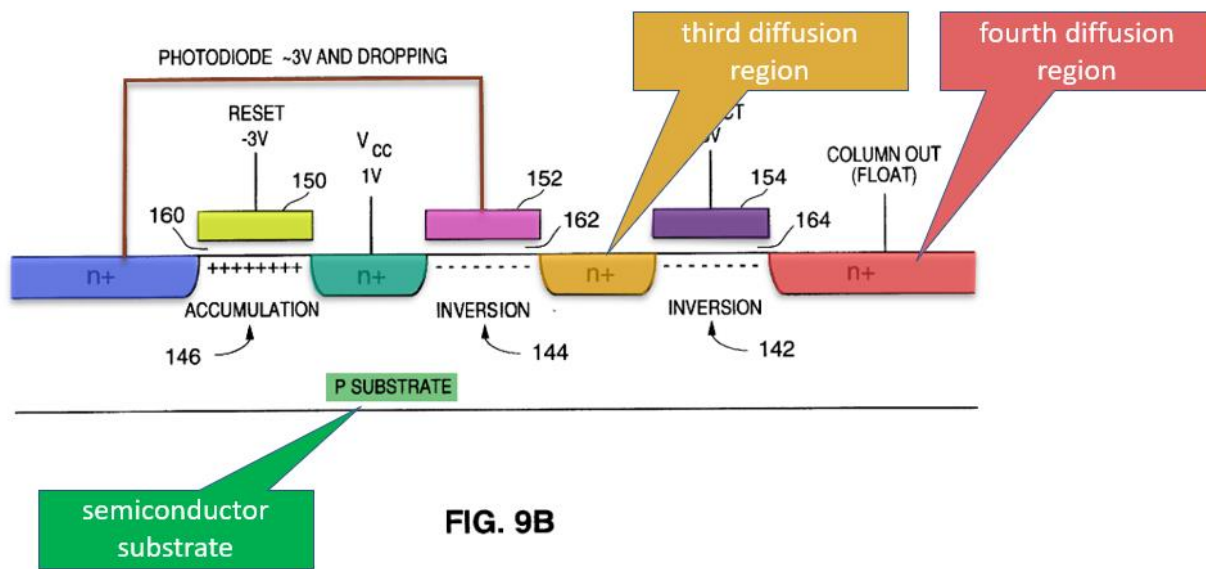
FIG. 9B

Id., Fig. 9B (annotated).

[3e] a fourth diffusion region that is formed in the semiconductor substrate and spaced from third diffusion region;

125. I am of the opinion that Merrill renders obvious this claim element.

126. Merrill's another n+ active region (on the far right) that "functions as the source of select transistor 18" corresponds to the claimed "fourth diffusion region." Ex. 1049, 5:9-23. Merrill's Figure 9B illustrates **another n+ active region** that is **formed** in **substrate 110** and spaced from the **other n+ active region** (i.e., **a fourth diffusion region that is formed in the semiconductor substrate and spaced from third diffusion region**):



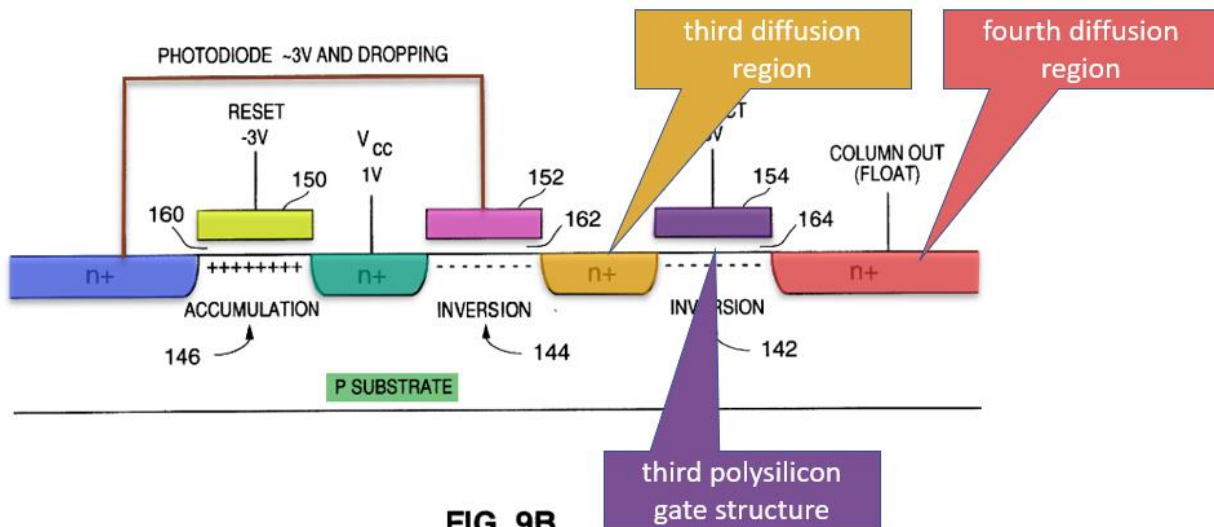
Id., Fig. 9B (annotated).

[3f] a third polysilicon gate structure that is provided between the third diffusion region and the fourth diffusion region;

127. I am of the opinion that Merrill renders obvious this claim element.

128. Merrill’s select line 154, which is polysilicon, and select transistor 18 correspond to the claimed “third polysilicon gate structure.” Ex. 1049, 6:1-8.

Merrill’s Figure 9B illustrates that the **select line 154**, serving as the gate for **select transistor 18** (not labeled), is provided between the **other n+ active region** and **another n+ active region** (*i.e.*, *a third polysilicon gate structure that is provided between the third diffusion region and the fourth diffusion region*):

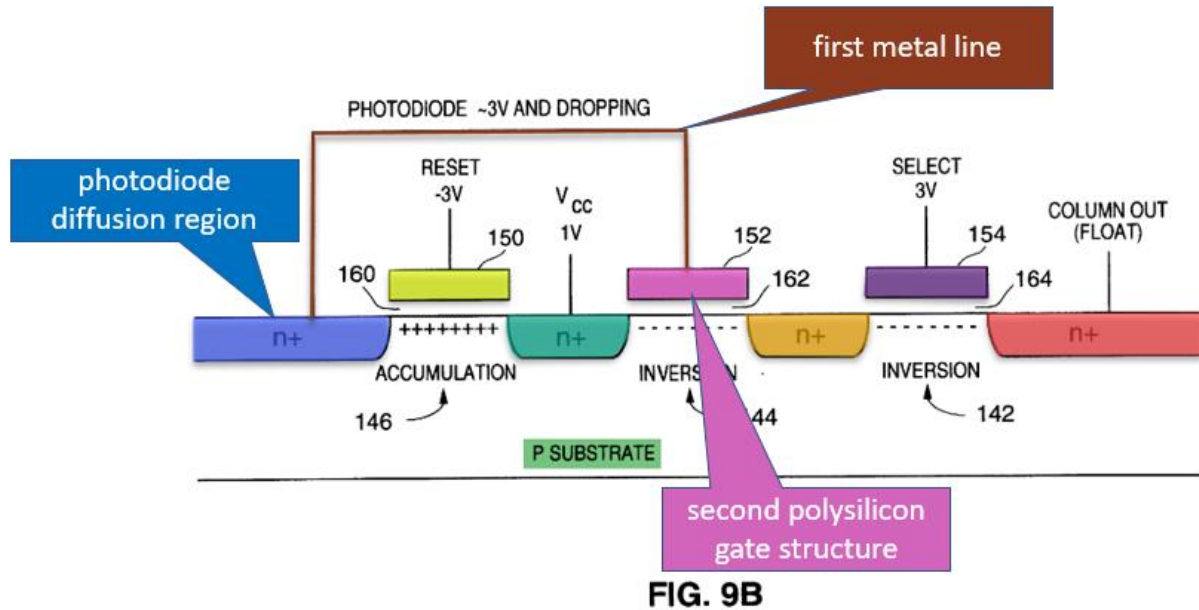


Id., Fig. 9B (annotated).

[3g] wherein the photodiode region is connected to the second polysilicon gate by a first metal line to form a source-follower transistor, and

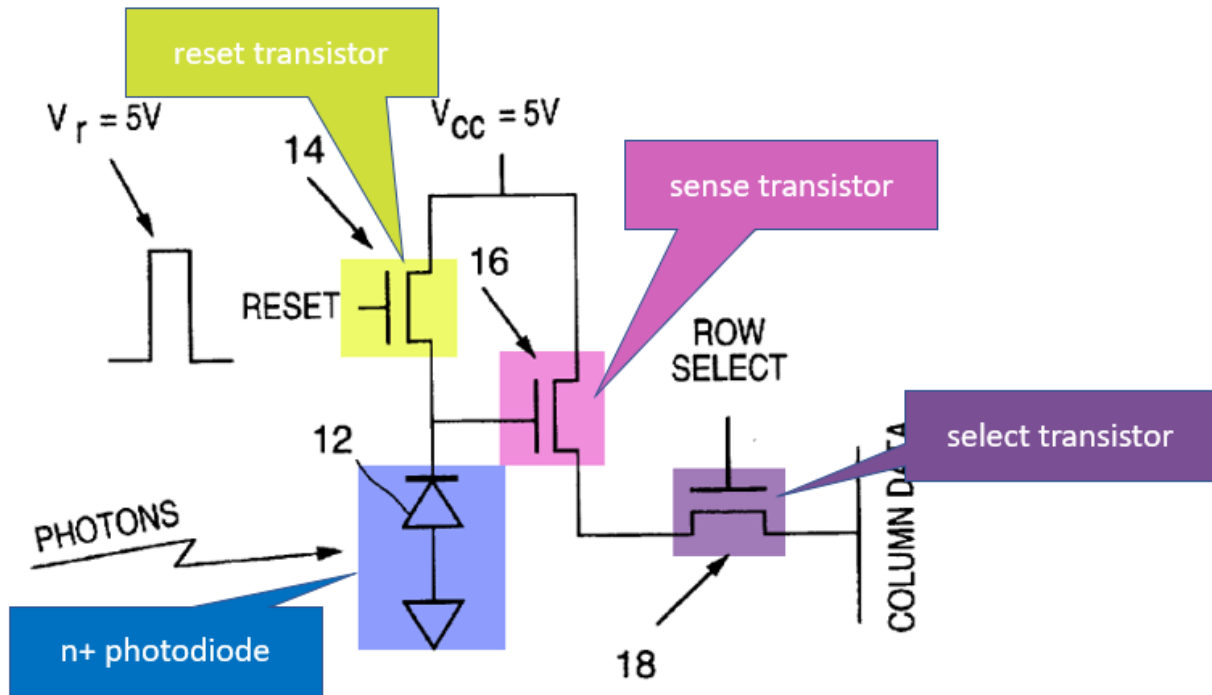
129. I am of the opinion that Merrill renders obvious this claim element.

130. Merrill's local interconnect line 152 corresponds to the claimed "first metal line." Ex. 1049, 5:59-67. Merrill discloses that the "local interconnect line 152 forms the gate of sense transistor 16 (see FIG. 1), and connects the first active area 130 [*i.e.*, **the photodiode region**] to the gate of sense transistor 16 [*i.e.*, **second polysilicon gate**]." *Id.*, 5:59-67. Merrill's Figure 9 illustrates the **n+ photodiode 140** connected to **sense transistor 16** (not labeled) by **local interconnect line 152** (*i.e.*, **wherein the photodiode region is connected to the second polysilicon gate by a first metal line to form a source-follower transistor**):



Id., Fig. 9B (annotated).

131. Merrill's Fig. 1 illustrates that sense transistor 16 is a source-follower transistor because its gate is connected to photodiode 12, its drain is connected to supply voltage V_{cc} , and its source is connected by select transistor 18 to a column bus:

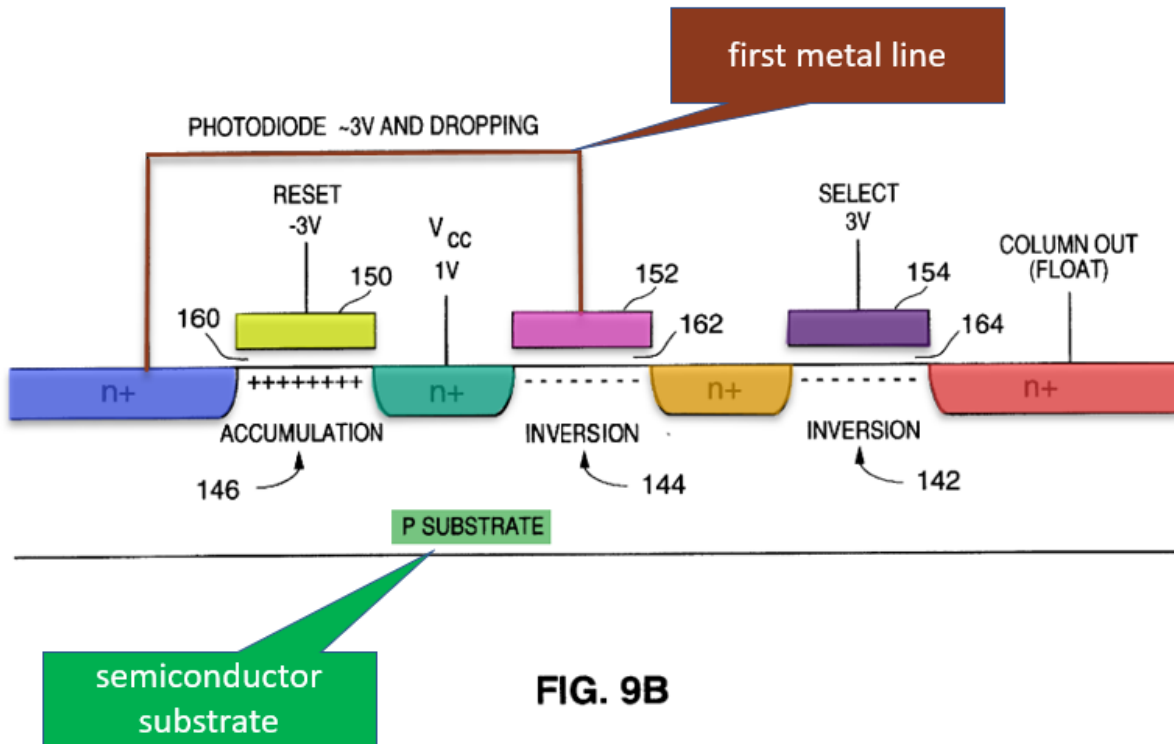


Ex. 1049, Fig. 1 (annotated).

[3h] wherein the first metal line is located between the semiconductor substrate and the protective substrate.

132. I am of the opinion that Merrill renders obvious this claim element.

133. Merrill's local interconnect line 152 corresponds to the claimed "first metal line." Ex. 1049, 5:59-67. As illustrated in Merrill's Figure 9B, Merrill's **local interconnect line 152** is formed on the top (frontside) surface of the image sensor (*i.e., wherein the first metal line is located between the semiconductor substrate and the protective substrate*):



Id., Fig. 9B (annotated).

134. In the combination of Nixon and Merrill, a POSITA would readily understand that Merrill's **local interconnect line 152** would be sandwiched between Nixon's **substrate 11** on one side and Nixon's **protective substrate** on the other side. *See supra*, §V.D.

XII. GROUND 3: NIXON IN VIEW OF WATANABE RENDERS OBVIOUS CLAIM 4

135. I am of the opinion that Nixon in view of Watanabe renders obvious claim 4.

1. Reasons to Combine Nixon with Watanabe

136. A POSITA would have been motivated to modify Nixon's manufacturing process for a BSI CMOS image sensor to thin the silicon layer to a thickness of 5 to 15 μm as taught by Watanabe. During semiconductor fabrication, including image sensor fabrication, the beginning thickness of a typical raw silicon wafer is on the order of 500 μm . Ex. 1010, 145. BSI CMOS image sensors must be much thinner than this 500 μm starting thickness so that photons may be absorbed by the remaining substrate and photogenerated electrons may be captured by the photodiode and not be recombined with holes within the substrate. *See supra*, §V.C.

137. Similarly, Nixon also discloses that the semiconductor wafer needs to be "thinned considerably" "to absorb the photons in the sensitive area" and describes in one embodiment thinning the substrate to 70 microns. Ex. 1004, 1:22-33, 2:36-41; Ex. 1005, IDTD, 4, Shweky, 8, Fig. 4. It was therefore commonplace at the time of the '319 patent for the substrate to be thinned to a fraction of their starting thickness during manufacturing of BSI sensors. Watanabe is an example of a substrate thinning technique applicable to BSI image sensors like Nixon's.⁴

⁴ Watanabe, like Nixon, teaches thinning a silicon substrate to a desired thickness during fabrication.

138. A POSITA would have understood that Nixon's substrate must have been thinned using a technique such as that taught in Watanabe. Accordingly, applying the teachings of Watanabe to BSI CMOS image sensor manufacturing process of Nixon would lead to a suitably thin substrate that ensures photons are absorbed by the remaining substrate and electrons are generated closer to the photodiode for better response. *See supra*, §§V.A-D. Indeed, it was common knowledge that a silicon layer in a photodiode-based image sensor must be thick enough to absorb visible light, but not so thick that diffusing electrons would be likely to recombine before reaching the p/n junction. Ex. 1052, 5:8-31; *see supra*, §V.C. This thickness depends on many factors, but is typically on the order of 10's of microns. Ex. 1052, 5:8-31; *see supra*, §V.C.

139. Watanabe's substrate thinning to a thickness of 5 to 15 microns is readily applicable to Nixon's manufacturing process, and a POSITA could have modified Nixon's manufacturing process to include Watanabe's substrate thinning to a thickness of 5 to 15 microns with a reasonable expectation of success. *See supra*, §§V.A, C. As disclosed in Nixon, "[p]ixels 145 are positioned at the top surface 148 of the silicon substrate 105." Ex. 1004, 2:8-10; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 7-8, Fig. 4. And because the pixels are positioned on the top surface of the substrate, the substrate must be thinned to a certain thickness, which

as taught in Watanabe is 5 to 15 microns, to minimize unwanted photon absorption. *See supra*, §V.C.

2. Claim 4

[4pre] The backside illuminated image sensor according to claim 1,

140. I am of the opinion that Nixon discloses claim 4pre for the same reasons as claim 1 above.

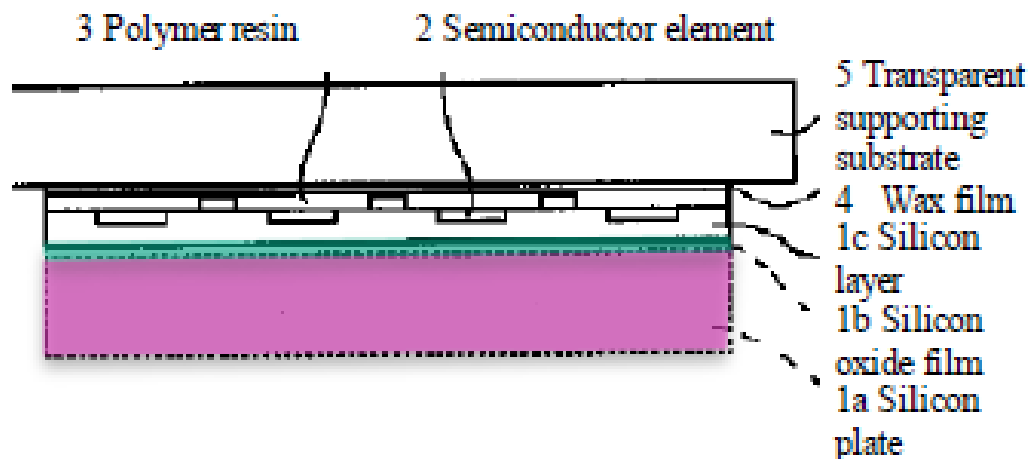
[4a] the thickness of the semiconductor substrate is in the range of 10 to 15 microns.

141. I am of the opinion that Nixon combined with Watanabe renders obvious this claim element.

142. Nixon's Figures 4A-4G illustrate the process to form silicon substrate 105, which is represented by die 430 from silicon wafer 405. *See supra*, claim 1f. Nixon discloses that "the silicon wafer 405 is ground to a thickness of approximately 70 microns." Ex. 1004, 2:36-42; Ex. 1005, IDTD, 5, Shweky, 8, Fig. 4. Watanabe discloses a substrate 1 which is comprised of silicon plate 1a with a thickness of 400 μm , silicon oxide film 1b with a thickness of 1 μm , and silicon layer 1c with a thickness of 5 to 15 μm . Ex. 1007, ¶17. Watanabe further discloses that the silicon plate 1a is subjected to a polishing process until it has a thickness of about 360 μm and is not entirely etched away. *Id.*, ¶19. Watanabe also discloses that the remaining **silicon plate 1a** can be removed by an "etchant

made of caustic potash until reaching the interface with the silicon oxide film 1b” or “by dry etching.” *Id.* Then, from the backside of substrate 1, “the **silicon oxide film 1b** is removed using buffered hydrofluoric acid composed of ammonium fluoride (NH₄F) and hydrofluoric acid (HF),” as illustrated in Watanabe’s Figure 2c:

(c) Polishing the silicon plate (1a) and etching the silicon oxide film (1b)



Id., ¶19, Fig. 2c (annotated). As a result, for substrate 1, only silicon layer 1c with its 5 to 15 µm thickness remains, which includes a thickness in the range of “10 to 15 microns” (*i.e.*, ***the thickness of the semiconductor substrate is in the range of 10 to 15 microns***). *Id.*, ¶17.

143. In the combination of Nixon and Watanabe, silicon layer 1c, with a 10 to 15 micron thickness, is used in place of Nixon’s silicon substrate 105. A POSITA would have been motivated to make this modification for the reasons discussed above. *See supra*, §V.C.

XIII. GROUND 4: BADIHI RENDERS OBVIOUS CLAIMS 1, 2, 5, AND 6

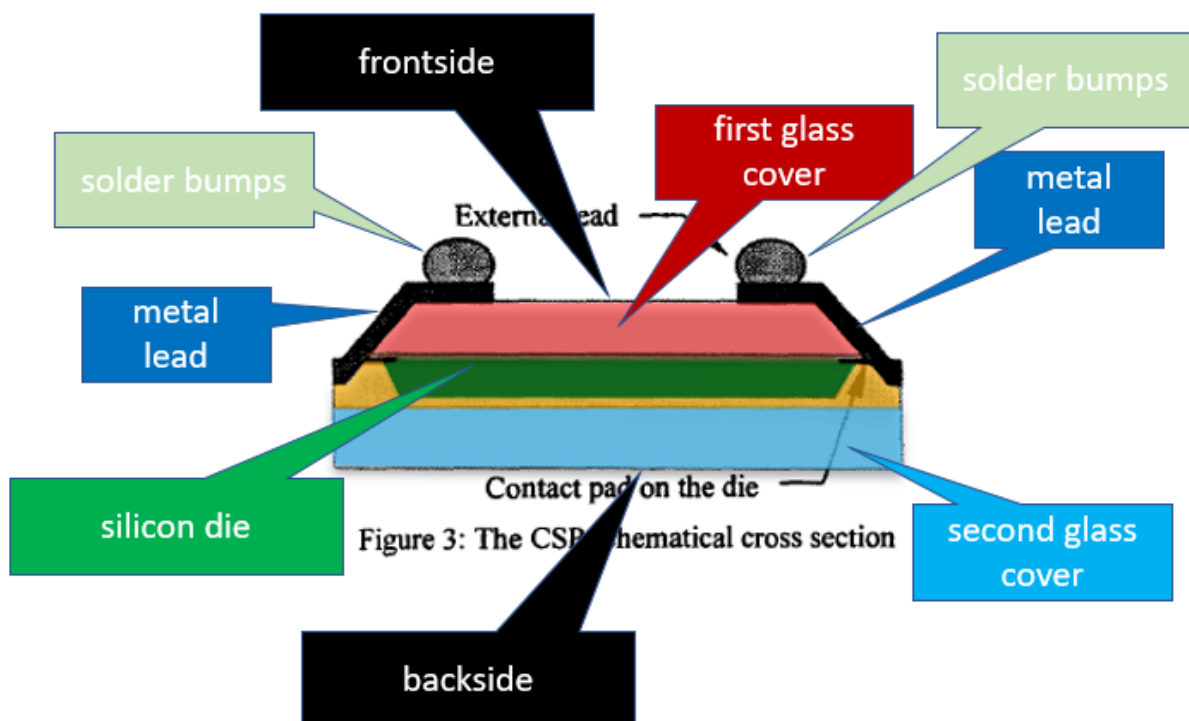
144. I am of the opinion that Badihi renders obvious claims 1, 2, 5, and 6 of the '319 patent.

1. Claim 1

[1pre] A backside illuminated image sensor comprising:

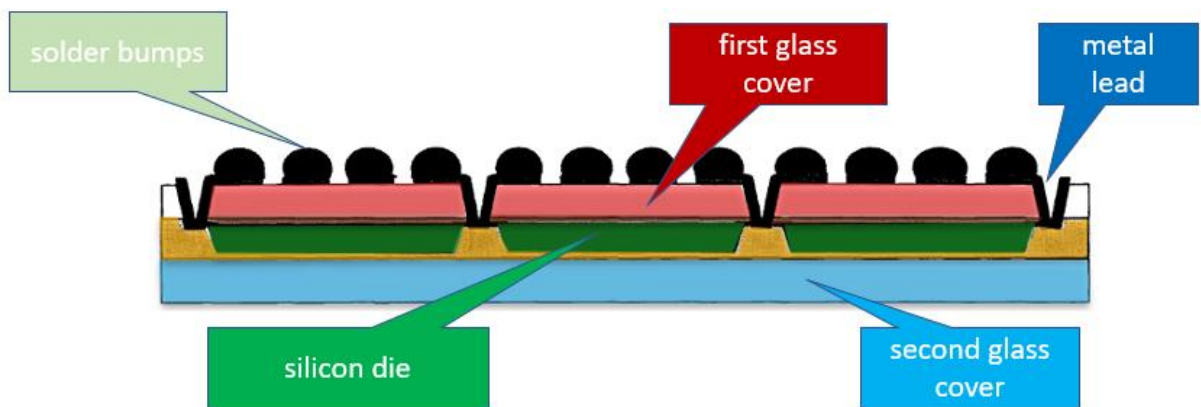
145. To the extent the preamble is considered to be a limitation, I am of the opinion that Badihi renders obvious this claim element.

146. Badihi's Figure 3 illustrates the resulting packaged semiconductor where a **first glass cover** is bonded to the frontside of a **silicon die**, **metal leads** and solder bumps are formed on the **first glass cover**, and a **second glass cover** is bonded to the backside of the **silicon die**:



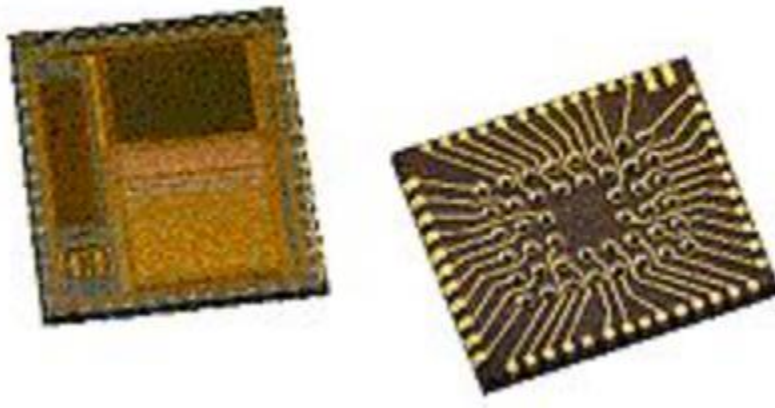
Ex. 1101, 237, Fig. 3 (annotated). Badihi's disclosures are not specific to image sensors; however, Badihi discloses that its packaging process can be readily applied to silicon light detectors, CMOS image sensors, and CCD devices. *Id.*, 239.

147. Badihi's Figure 2 illustrates the resulting packaged semiconductor with metal leads and solder bumps covering top of the frontside (active) surface, indicating that the wafer as packaged would be back-illuminated (*i.e.*, ***a backside illuminated image sensor***):

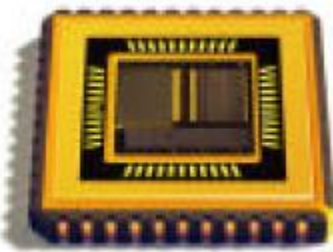


Id., Fig. 2 (annotated), 237.

148. Figure 4 provides an example of a BSI image sensor created using the ShellPack wafer-level packaging process. *Id.*, Fig. 4. Figure 4 shows photographs of a CMOS APS image sensor, the Photobit PB0159, with an “optically clear enclosure” made with Badihi's process:



Ex. 1055, Ex. A, Fig. 4, 239. The photo on the right is the frontside of the packaged image sensor, because Badihi specifically teaches metal leads and solder bumps are formed on the glass cover at the frontside of the packaged image sensor (facing the active surface of the imager die), and the photo on the left is therefore the backside of the packaged image sensor. Ex. 1101, 237. A diagram of the Photobit PB-159 in a contemporaneous datasheet confirms that the photo on the left in Badihi is comprised of an array of 512x384 pixels:



Ex. 1051, 1.

149. A POSITA would recognize the packaged image sensor is a BSI image sensor because light would enter through its unobstructed backside since its frontside is covered by metal leads and solder bumps.

[1a] a semiconductor substrate having a first surface and a second surface;

150. I am of the opinion that Badihi discloses this claim element.

151. Badihi's silicon die corresponds to the claimed "semiconductor substrate." Ex. 1101, 237. Badihi discloses "[a] thin protective glass layer is bonded to the active side of a silicon wafer with epoxy adhesive" (*i.e.*, **a semiconductor substrate having a first surface**) and "a second thin glass cover is bonded onto the silicon dies **back side**" (*i.e.*, **a semiconductor substrate having ... a second surface**). *Id.* Badihi's Figure 3 illustrates the **silicon die** with its active side facing the **protective glass layer (first glass cover)** and its backside facing the **second glass cover**:

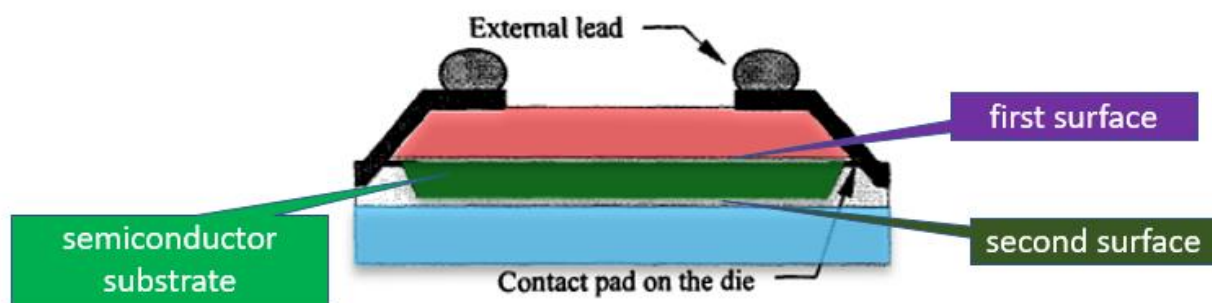


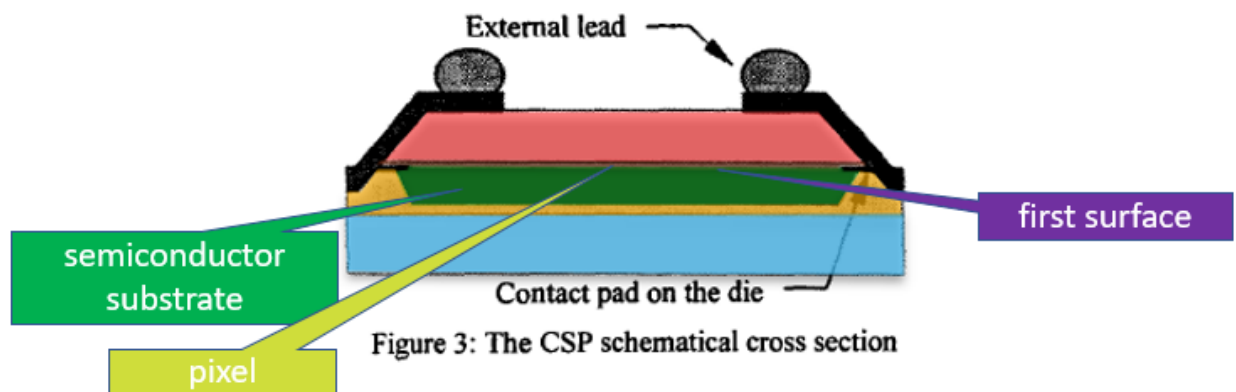
Figure 3: The CSP schematical cross section

Id., Fig. 3.

[1b] a plurality of light-sensitive pixel regions formed on the first surface of the semiconductor substrate and including a photodiode diffusion region extending into the semiconductor substrate from the first surface;

152. I am of the opinion that Badihi discloses or renders obvious this claim element.

153. Badihi's **silicon die** corresponds to the claimed "semiconductor substrate" and its active side facing the **protective glass layer (first glass cover)** corresponds to the claimed "first surface," which is illustrated in Badihi's Figure 3:



Id., Fig. 3 (annotated).

154. When Badihi's manufacturing method is applied to a CMOS image sensor such as the CMOS APS product called Photobit PB0159 containing an array of pixels as disclosed, it was well-known that the pixels, and therefore many light-sensitive pixel regions, would have been on the active side of the die (*i.e.*, **a plurality of light-sensitive pixel regions formed on the first surface of the semiconductor substrate**). Ex. 1101, Fig. 4; see *supra*, §V.A. Pixels in a CMOS

APS image sensor (like Photobit PB0159) are no different. *See supra*, §V.A. It is also well known that APS pixels in APS image sensors have light-sensitive pixel regions built into the die. *See supra*, §§V.A-B.

155. Badihi also discloses “including a photodiode diffusion region extending into the semiconductor substrate from the first surface.” Using any one of the three well-known CIS pixel implementations would have been a simple design choice that was a matter of common sense to a POSITA at the time of invention and would not have changed the nature of the claimed invention. *See supra*, §V.B. Thus, it would have been a matter of routine, design choice to incorporate active pixels with photodiodes, which include photodiode diffusion regions, into Badihi’s wafer-level semiconductor processing (*i.e.*, ***including a photodiode diffusion region extending into the semiconductor substrate from the first surface***). *See supra*, §§V.A-B, D.

[1c] a metal line formed adjacent the first surface of the semiconductor substrate;
--

156. I am of the opinion that Badihi discloses this claim element.

157. Badihi’s bond pads corresponds to the claimed “metal line.” Ex. 1101, 237, Fig. 3. Badihi further discloses that “[d]eep notches are drawn between the dies, revealing the cross-section of the bond pads.” *Id.*, 237. Badihi’s Figure 3 illustrates the resulting packaged image sensor where the **bond pads** are formed

adjacent to the active side of the **silicon die** (*i.e., a metal line formed adjacent the first surface of the semiconductor substrate*):

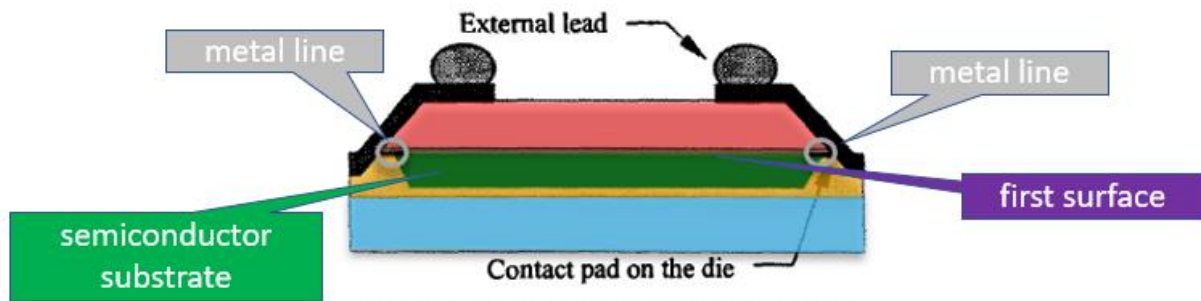


Figure 3: The CSP schematical cross section

Id., Fig. 3 (annotated). Indeed, the annotation in Figure 3 itself describes the “[c]ontact pad on the die.” *Id.*

[1d] a protective substrate secured to the semiconductor substrate such that the metal line is located between the protective substrate and the semiconductor substrate; and

158. I am of the opinion that Badihi discloses this claim element.

159. Badihi’s protective glass layer (first glass cover) corresponds to the claimed “protective substrate.” Ex. 1101, 237. Badihi discloses the “protective glass layer is bonded to the active side of a silicon wafer with epoxy adhesive” (*i.e., a protective substrate secured to the semiconductor substrate*). *Id.* Badihi’s Figure 3 discloses the resulting packaged image sensor where the **protective glass layer (first glass cover)** is **bonded** to the **silicon die** with the **bond pads** in between (*i.e., a protective substrate secured to the semiconductor substrate such*

that the metal line is located between the protective substrate and the semiconductor substrate):

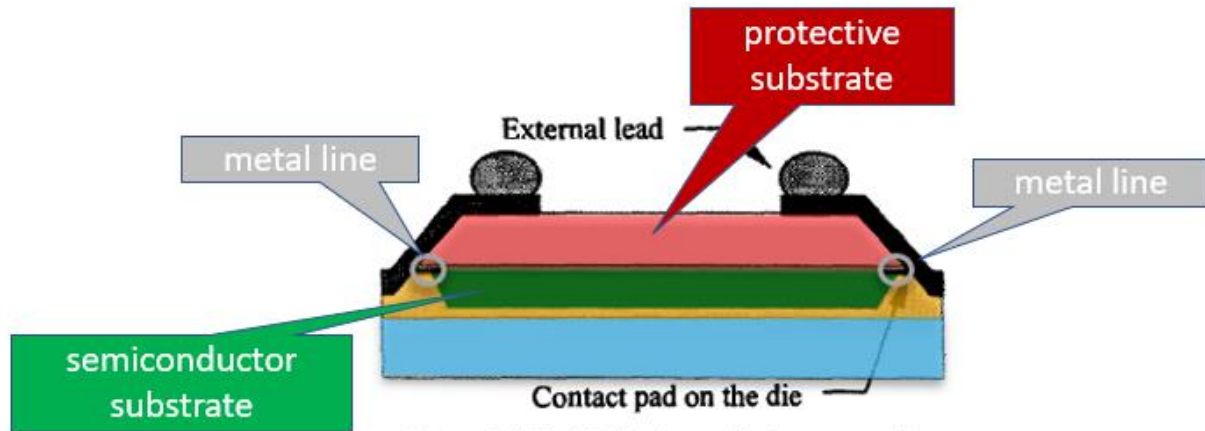


Figure 3: The CSP schematical cross section

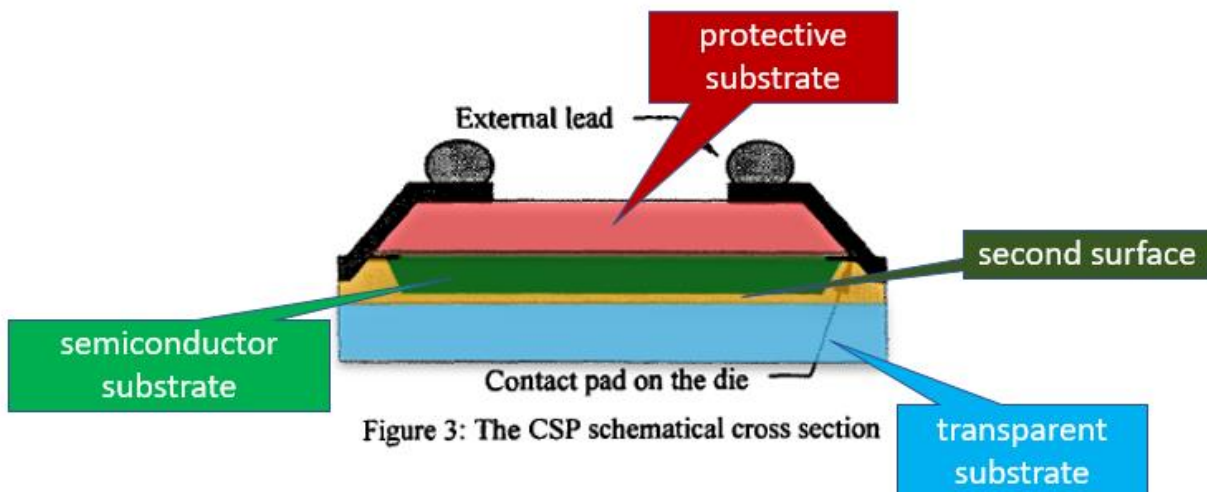
Id., Fig. 3 (annotated). Indeed, the annotation in Figure 3 itself describes the “[c]ontact pad on the die” and illustrates that the contact pad is located between the silicon die and protective glass layer (first glass cover). *Id.*

[1e] a transparent substrate secured to the second surface of the semiconductor substrate such that the semiconductor substrate is sandwiched between the transparent substrate and the protective substrate;

160. I am of the opinion that Badihi discloses this claim element.

161. Badihi’s second glass cover corresponds to the claimed “transparent substrate.” Ex. 1101, 237, Fig. 3. Badihi discloses the “second thin glass cover is bonded onto the silicon dies back side to achieve a complete protective enclosure for each die,” resulting in “dies [that] are packaged and encapsulated in separate enclosures” (*i.e.*, ***a transparent substrate secured to the second surface of the***

semiconductor substrate) *Id.*, 237, Fig. 3. Badihi further discloses that “[t]he glass transparent package encases the [i]mager [d]ie in a solid protecting optically clear enclosure.” *Id.*, 239. Badihi’s Figure 3 illustrates the resulting packaged image sensor where the **second glass cover** is **bonded** to the **silicon die** and the **protective glass layer (first glass cover)** and the **second glass cover** sandwich the **silicon die** (*i.e.*, *a transparent substrate secured to the second surface of the semiconductor substrate such that the semiconductor substrate is sandwiched between the transparent substrate and the protective substrate*):



Id., Fig. 3 (annotated).

[1f]	wherein the semiconductor substrate has a thickness defined such that the light-sensitive pixel region is effectively exposed through the second surface
------	--

162. I am of the opinion that Badihi discloses this claim element.

163. Badihi's Figure 2 illustrates the process step where the **silicon wafer** is grinded from its backside until 100 microns is left (*i.e.*, ***second surface***):



B. The silicon wafer is Back - Grinded to 100 microns

Id., Fig. 2 (annotated).

164. A POSITA would readily understand that the purpose of grinding the silicon wafer from its backside before enclosing it in a glass transparent package is so that the photons absorbed by the remaining semiconductor substrate are closer to the photodiode for a better response (*i.e.*, ***wherein the semiconductor substrate has a thickness defined such that the light-sensitive pixel regions are exposed from the backside of the silicon die***).⁵ See *supra*, §V.C.

2. Claim 2

[2pre]. The backside illuminated image sensor according to claim 1, further comprising

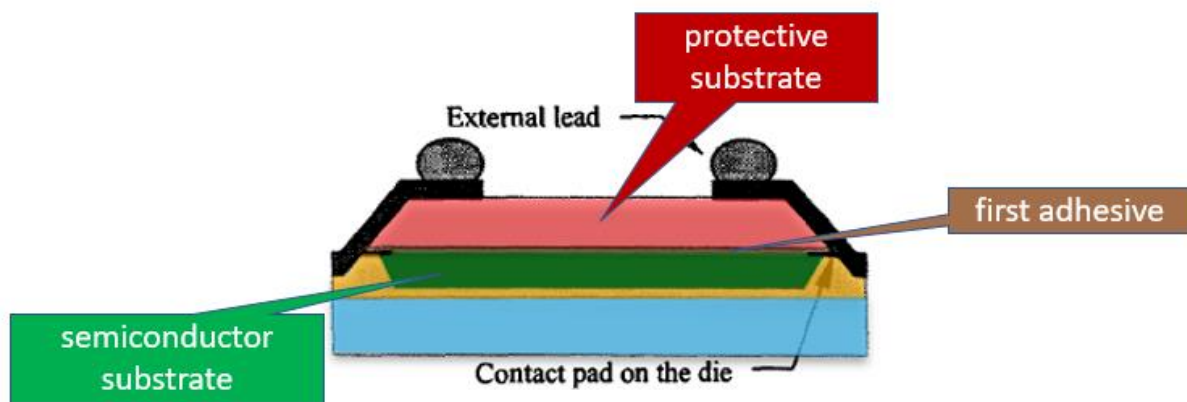
165. I am of the opinion that Badihi discloses claim 2pre for the same reasons as claim 1 above.

⁵ See *supra*, §X, Ground 1, 1f. A POSITA would readily understand that Badihi discloses what is described in the '319 patent.

[2a] a first adhesive layer located between the protective substrate and the semiconductor substrate, and

166. I am of the opinion that Badihi discloses this claim element.

167. Badihi's epoxy adhesive corresponds to the claimed "first adhesive layer." Ex. 1101, 237, Fig. 3. Badihi discloses the "thin protective glass layer is bonded to the active side of a silicon wafer with epoxy adhesive" (*i.e., a first adhesive layer located between the protective substrate and the semiconductor substrate*). See *supra*, claim 1d. Badihi's Figure 3 illustrates the resulting packaged image sensor where the **protective glass layer (first glass cover)** is **bonded using epoxy adhesive** to the **silicon die** (*i.e., a first adhesive layer located between the protective substrate and the semiconductor substrate*):

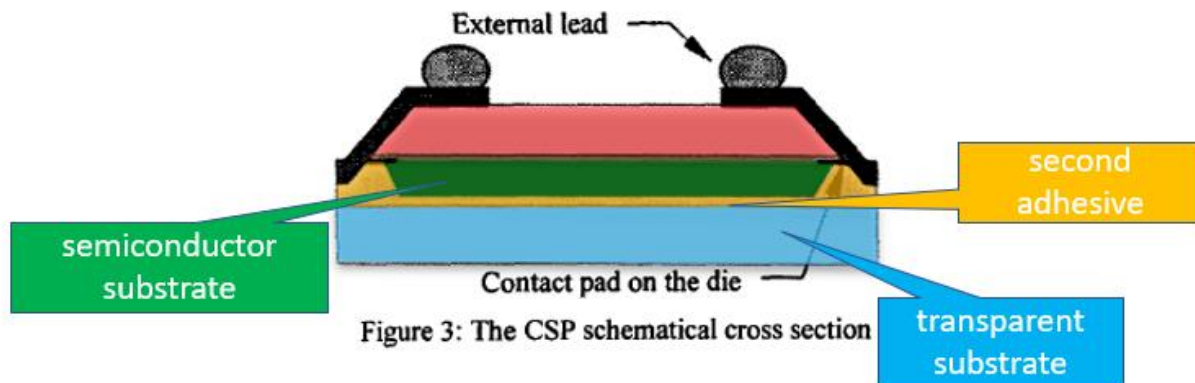


Id., Fig. 3 (annotated).

[2b] a second adhesive layer located between the transparent substrate and the semiconductor substrate.

168. I am of the opinion that Badihi discloses this claim element.

169. Badihi's epoxy adhesive corresponds to the claimed "second adhesive layer." Ex. 1101, 237, Fig. 3. Badihi discloses a process step where "second thin glass cover is bonded onto the silicon dies back side to achieve a complete protective enclosure for each die." *Id.*, 237, Fig. 3. Badihi's Figure 3 illustrates the resulting packaged image sensor where the **epoxy adhesive** is deposited on the backside of the **silicon dies** (*i.e.*, *a second adhesive layer located between the transparent substrate and the semiconductor substrate*):



Id., Fig. 3 (annotated).

3. Claim 5

[5pre] The backside illuminated image sensor according to claim 1,

170. I am of the opinion that Badihi discloses claim 5pre for the same reasons as claim 1 above.

[5a] wherein the transparent substrate is glass.

171. I am of the opinion that Badihi discloses this claim element.

172. Badihi discloses the transparent substrate is glass for the same reasons as discussed above in connection with claim 1e. *See supra*, claim 1e.

4. Claim 6

[6pre]. The backside illuminated image sensor according to claim 1, further comprising

173. I am of the opinion that Badihi discloses claim 6pre for the same reasons as claim 1 above.

[6a] a plurality of metal leads formed on the protective layer.

174. I am of the opinion that Badihi discloses this claim element.

175. Badihi's individual leads corresponds to the claimed "metal leads." Ex. 1101, 237, Fig. 3. Badihi discloses that "[d]eep notches are drawn between the dies, revealing the cross-section of the bond pads" and that "[a] metal layer, patterned by lithography to individual leads, is deposited to contact the bond pads at their cross sections" (*i.e.*, ***a plurality of metal leads formed***). *Id.*, 237. Badihi's Figure 3 illustrates the resulting packaged image sensor where the **individual leads** are formed on the **protective glass layer (first glass cover)** (*i.e.*, ***a plurality of metal leads formed on the protective layer***):

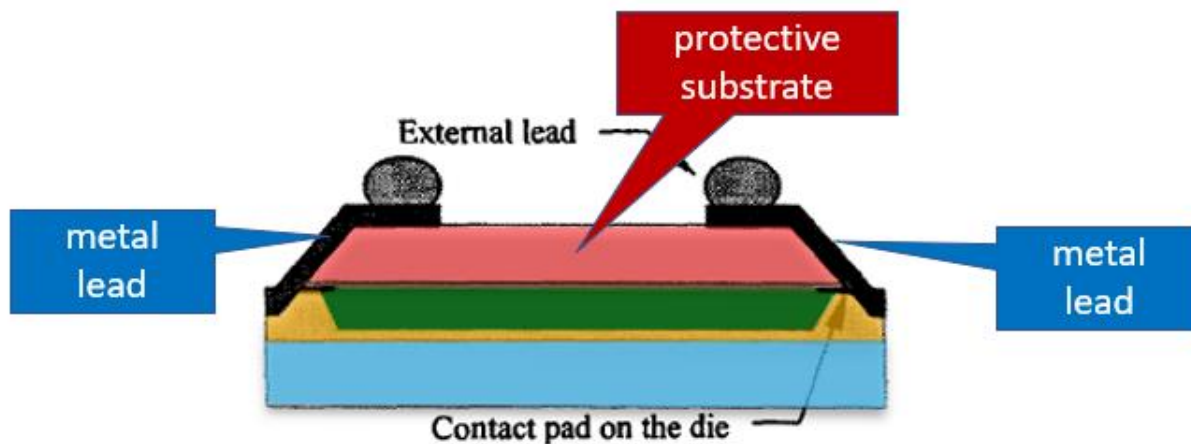


Figure 3: The CSP schematical cross section

Id., Fig. 3 (annotated).

XIV. GROUND 5: BADIHI IN VIEW OF WATANABE RENDERS OBVIOUS CLAIM 4

176. I am of the opinion that Badihi in view of Watanabe renders obvious claim 4.

1. Reasons to Combine Badihi with Watanabe

177. A POSITA would have been motivated to modify Badihi's manufacturing process for BSI CMOS image sensors to thin the silicon substrate to a thickness of 5 to 15 μm as taught by Watanabe. During semiconductor fabrication, including image sensor fabrication, the beginning thickness of a typical raw silicon wafer is on the order of 500 μm . Ex. 1010, 145. BSI CMOS image sensors must be much thinner than this 500 μm starting thickness so that photons may be absorbed by the remaining substrate and photogenerated electrons may be

captured by the photodiode and not be recombined with holes within the substrate. *See supra*, §V.C.

178. Similarly, Badihi discloses grinding the silicon wafer from the back to 100 microns. Ex. 1101, Fig. 2. It was therefore commonplace at the time of the '319 patent for the substrate to be thinned to a fraction of their starting thickness during manufacturing of BSI sensors. *Id.* Watanabe is an example of a substrate thinning technique applicable to BSI image sensors like the CMOS image sensor depicted in Badihi's Figure 4.⁶ *Id.* A POSITA would have understood that Badihi's substrate must have been thinned using a technique such as that taught in Watanabe. Accordingly, applying the teachings of Watanabe to the image sensor manufacturing process of Badihi would lead to a suitably thin substrate that ensures photons are absorbed by the remaining substrate and electrons are generated closer to the photodiode for better response. Ex. 1101, Fig. 2; *see supra*, §§V.A-D. Indeed, it was common knowledge that a silicon layer in a photodiode-based image sensor must be thick enough to absorb visible light, but not so thick that diffusing electrons would be likely to recombine before reaching the p/n junction. Ex. 1052, 5:8-31; *see supra*, §V.C. This thickness depends on many

⁶ Watanabe, like Badihi, teaches thinning a silicon substrate to a desired thickness during fabrication.

factors, but is typically on the order of 10's of microns. Ex. 1052, 5:8-31; *see supra*, §V.C.

179. Watanabe's substrate thinning to a thickness of 5 to 15 microns is readily applicable to Badihi's manufacturing process, and a POSITA could have modified Badihi's manufacturing process to include Watanabe's substrate thinning to a thickness of 5 to 15 microns with a reasonable expectation of success. *See supra*, §§V.A, C-D. In Badihi's design, the substrate must be thinned to minimize unwanted absorption of backside-incident photons. *See supra*, §V.C.

2. Claim 4

[4pre] The backside illuminated image sensor according to claim 1,

180. I am of the opinion that Badihi discloses claim 4pre for the same reasons as claim 1 above.

[4a] the thickness of the semiconductor substrate is in the range of 10 to 15 microns.

181. I am of the opinion that Badihi combined with Watanabe renders obvious this claim element.

182. Badihi discloses a process step where the silicon wafer is grinded from its backside to 100 microns. Ex. 1101, Fig. 2. Watanabe discloses from the backside of the substrate 1, first polishing the silicon plate 1a then etching the remaining silicon plate 1a and silicon oxide film 1b, leaving only the silicon layer

1c with its 5 to 15 μm thickness, which overlaps with the claimed “10 to 15 microns” (*i.e.*, ***the thickness of the semiconductor substrate is in the range of 10 to 15 microns***). Ex. 1007, ¶¶17, 19, Fig. 2c; *see supra*, §V.C.

183. In the combination of Badihi and Watanabe, silicon layer 1c, with a 10 to 15 micron thickness, is used in place of Badihi’s silicon die. A POSITA would have been motivated to make this modification for the reasons discussed above. *See supra*, §V.C. A POSITA would have been motivated to make this modification for the reasons discussed above. Ex. 1052, 5:8-31; *see supra*, §V.C.

XV. GROUND 6: MERRILL IN VIEW OF BADIHI RENDERS OBVIOUS CLAIMS 1, 2, 3, 5, AND 6

184. I am of the opinion that Badihi in view of Merrill renders obvious claims 1, 2, 3, 5, and 6 of the ’319 patent.

1. Reasons to Combine Merrill with Badihi

185. A POSITA would have been motivated to modify Merrill’s CMOS APS cells to include the wafer-level semiconductor packaging process as taught by Badihi. Merrill discloses that a CMOS APS cell employs a photodiode and teaches the arrangement of the various elements in the CMOS APS cell, as it includes a “conventional photodiode ... typically combined with a number of active transistors”. Ex. 1049, 1:31-45, 6:13-18. Further, Merrill’s CMOS APS cell performs three steps, all of which were conventional by the time of the ’319 patent: “a reset step, where cell 100 is reset from the previous integration cycle; an

image integration step, where the light energy is collected and converted into an electrical signal; and a signal readout step, where the signal is read out.” Ex. 1049, 6:13-18. Badihi teaches a generalized process for manufacturing semiconductor devices, including BSI image sensors. Indeed, Badihi’s Figure 4 depicts Photobit PB-159 CMOS Active Pixel Image Sensor and illustrates a packaged image sensor has a frontside blanketed with metal leads and solder bumps and an unobstructed backside to allow light to enter. Ex. 1101, Fig. 4; *see supra*, §V.D. A POSITA would have naturally looked to Badihi’s wafer-level semiconductor packaging process to be used on Merrill’s CMOS APS cell to produce thin CMOS APS die packages that are backside illuminated. *See supra*, §§V.B-D.

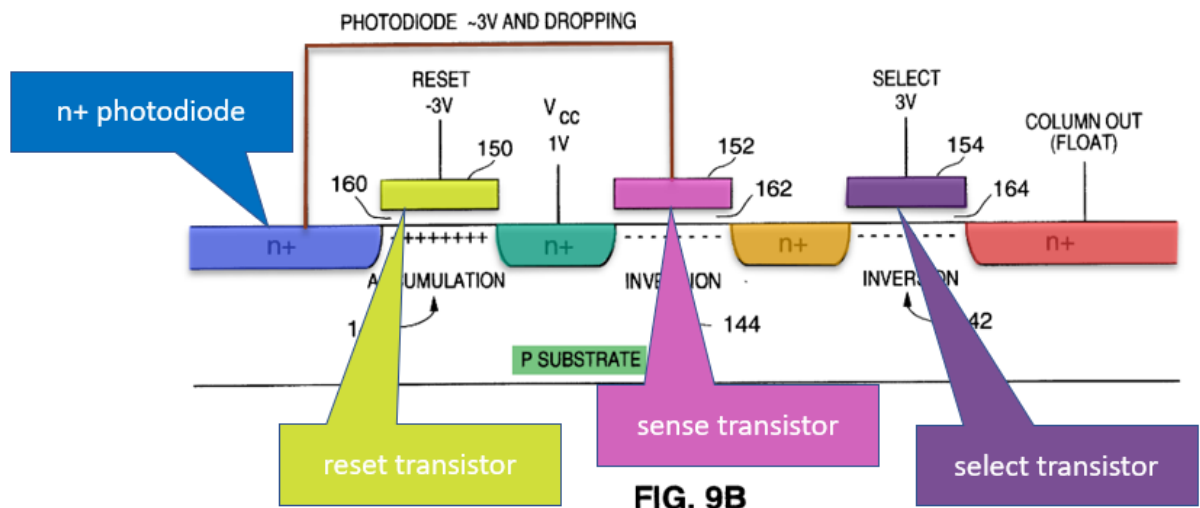
186. Badihi’s wafer-level semiconductor packaging process is readily applicable to Merrill’s CMOS APS cell, as a POSITA could have used Badihi’s wafer-level semiconductor packaging process to package the CMOS APS cell as taught in Merrill with a reasonable expectation of success since it is a conventional process readily understood by a POSITA at the time of invention. *See supra*, §§V.A-B, D. A POSITA would have also been further motivated to combine Badihi’s wafer-level semiconductor packaging process with Merrill’s CMOS APS cell due to the resulting low fill factor, enabling backside illumination of the photodiode region for improved sensitivity and reduced noise from scattered light. *See supra*, §§V.A-C.

2. Claim 1

[1pre] A backside illuminated image sensor comprising:

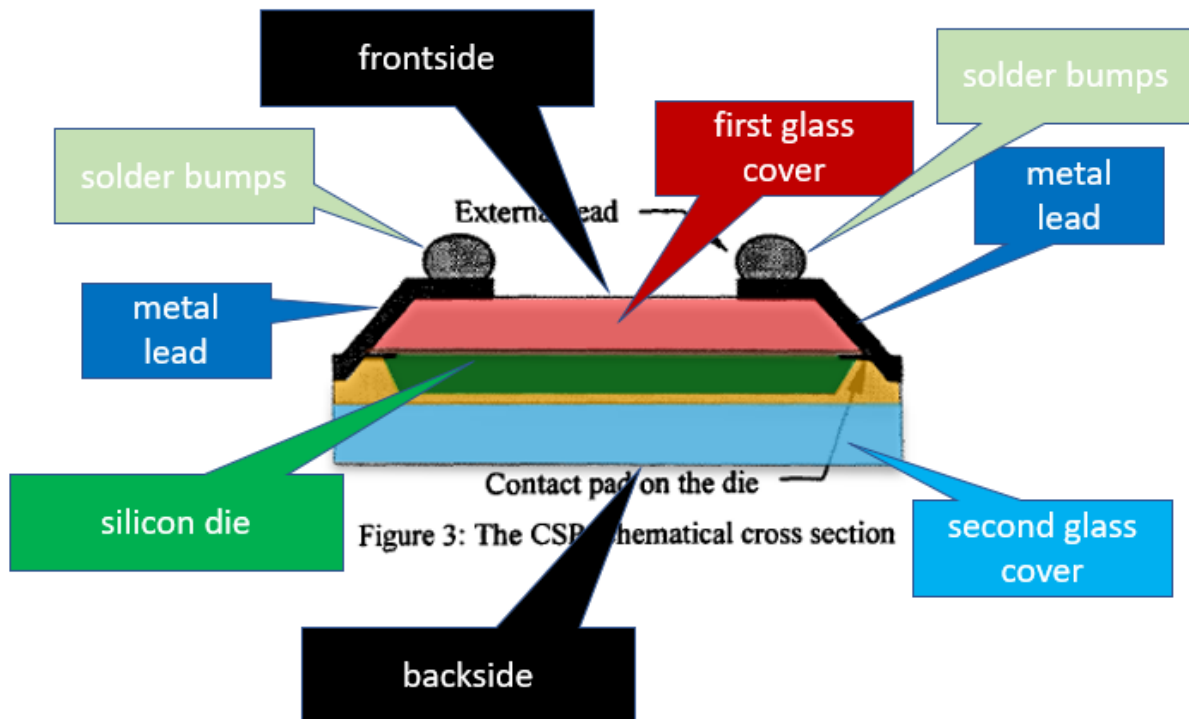
187. To the extent the preamble is considered to be a limitation, I am of the opinion that Merrill combined with Badihi renders obvious this claim element.

188. Merrill's Figure 9B illustrates a cross-sectional view of CMOS APS cell 100 (*i.e.*, *image sensor*):



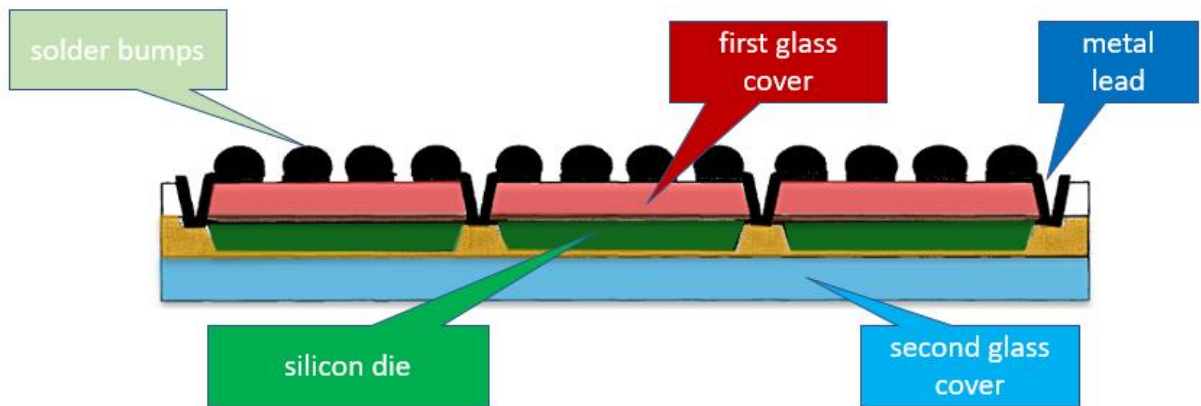
Ex. 1049, Fig. 9B (annotated).

189. Badihi's Figure 3 illustrates the resulting packaged semiconductor where a **first glass cover** is bonded to the frontside of a **silicon die**, with the active side of the **silicon die** facing the **first glass cover**, **metal leads** and solder bumps are formed on the **first glass cover**, and a **second glass cover** is bonded to the backside of the **silicon die**:



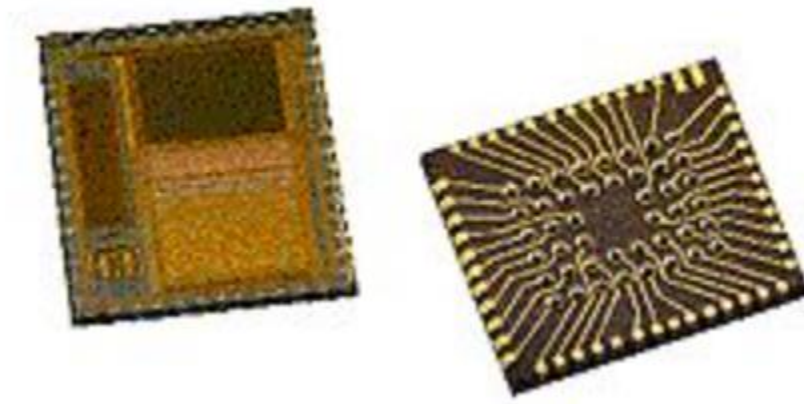
Ex. 1101, 237, Fig. 3 (annotated). Badihi's disclosures are not specific to image sensors; however, Badihi discloses that its packaging process can be readily applied to silicon light detectors, CMOS image sensors, and CCD devices. *Id.*, 239. A POSITA would understand that CMOS image sensors include BSI CMOS image sensors and would further understand that the packaging taught by Badihi could be used for BSI CMOS image sensors.

190. Badihi's Figure 2 illustrates the resulting packaged semiconductor with metal leads and solder bumps covering top of the frontside (active) surface, indicating that the wafer as packaged would be back-illuminated (*i.e.*, ***a backside illuminated image sensor***):



Id., Fig. 2 (annotated), 237.

191. Badihi’s Figure 4 provides an example of a BSI image sensor created using the ShellPack wafer-level packaging process. *Id.*, Fig. 4. Figure 4 shows photographs of a CMOS APS image sensor, the Photobit PB0159, with an “optically clear enclosure” made with Badihi’s process:



Ex. 1055, Ex. A, Fig. 4, 239. The photo on the right is the frontside of the packaged image sensor, because Badihi specifically teaches metal leads and solder bumps are formed on the glass cover at the frontside of the packaged image sensor (facing the

active surface of the imager die), and the photo on the left is therefore the backside of the packaged image sensor. Ex. 1101, 237.

[1a] a semiconductor substrate having a first surface and a second surface;

192. I am of the opinion that Merrill combined with Badihi renders obvious this claim element.

193. Merrill's substrate 110 and Badihi's silicon die corresponds to the claimed "semiconductor substrate." Ex. 1049, 5:4-17; Ex. 1101, 237. Badihi discloses "[a] thin protective glass layer is bonded to the active side of a silicon wafer with epoxy adhesive" (i.e., *a semiconductor substrate having a first surface*) and "a second thin glass cover is bonded onto the silicon dies *back side*" (i.e., *a semiconductor substrate having ... a second surface*). *Id.* Badihi's Figure 3 illustrates the **silicon die** with its active side facing the **protective glass layer (first glass cover)** and its backside facing the **second glass cover**:

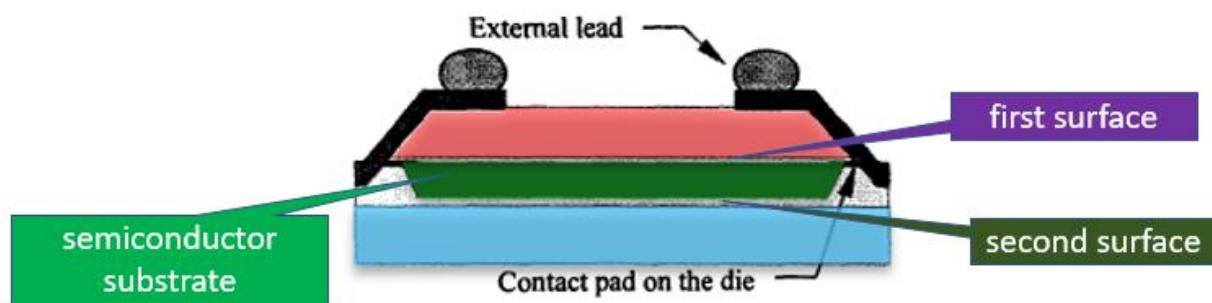


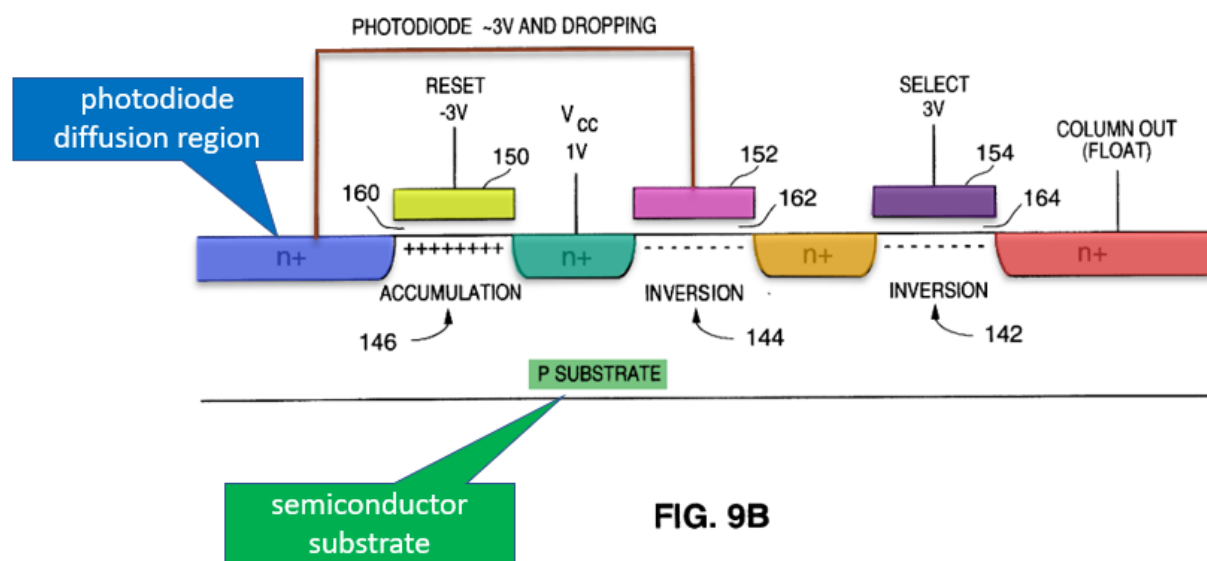
Figure 3: The CSP schematical cross section

Id., Fig. 3 (annotated).

[1b] a plurality of light-sensitive pixel regions formed on the first surface of the semiconductor substrate and including a photodiode diffusion region extending into the semiconductor substrate from the first surface;

194. I am of the opinion that Merrill discloses this claim element.

195. Merrill's CMOS APS 100 corresponds to the claimed "light-sensitive pixel region" and n+ photodiode 140 corresponds to the claimed "photodiode diffusion region." Ex. 1049, 1:31-45, 5:9-17. Merrill discloses "a plurality of active regions within substrate 110" (*i.e., a plurality of light-sensitive pixel regions; extending into the semiconductor substrate*). *Id.* 5:4-8. Merrill's Figure 9B illustrates a cross-sectional view of CMOS APS cell 100 with an n+ photodiode 140 extending into the substrate 110 (*i.e., light-sensitive pixel region; formed on the first surface of the semiconductor substrate; a photodiode diffusion region extending into the semiconductor substrate*):



Ex. 1049, 1:39-44, Fig. 9B (annotated).

[1c] a metal line formed adjacent the first surface of the semiconductor substrate;

196. I am of the opinion that Badihi renders obvious this claim element.

197. Badihi's bond pads corresponds to the claimed "metal line." Ex. 1101, 237, Fig. 3. Badihi further discloses that "[d]eep notches are drawn between the dies, revealing the cross-section of the bond pads." *Id.*, 237. Badihi's Figure 3 illustrates the resulting packaged image sensor where the **bond pads** are formed adjacent to the active side of the **silicon die** (*i.e.*, *a metal line formed adjacent the first surface of the semiconductor substrate*):

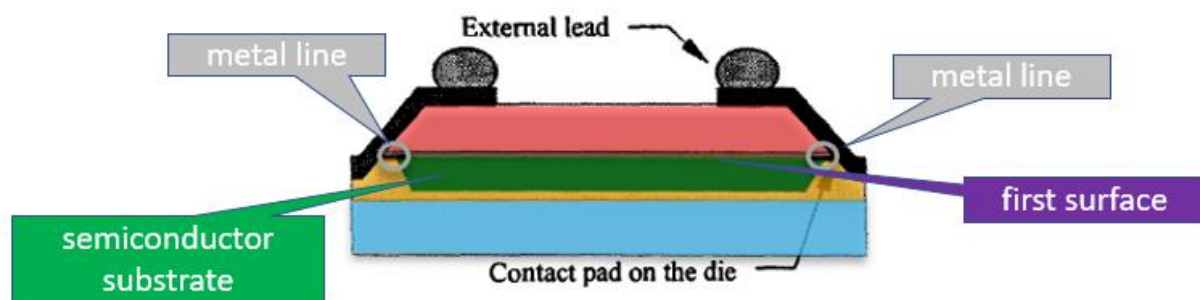


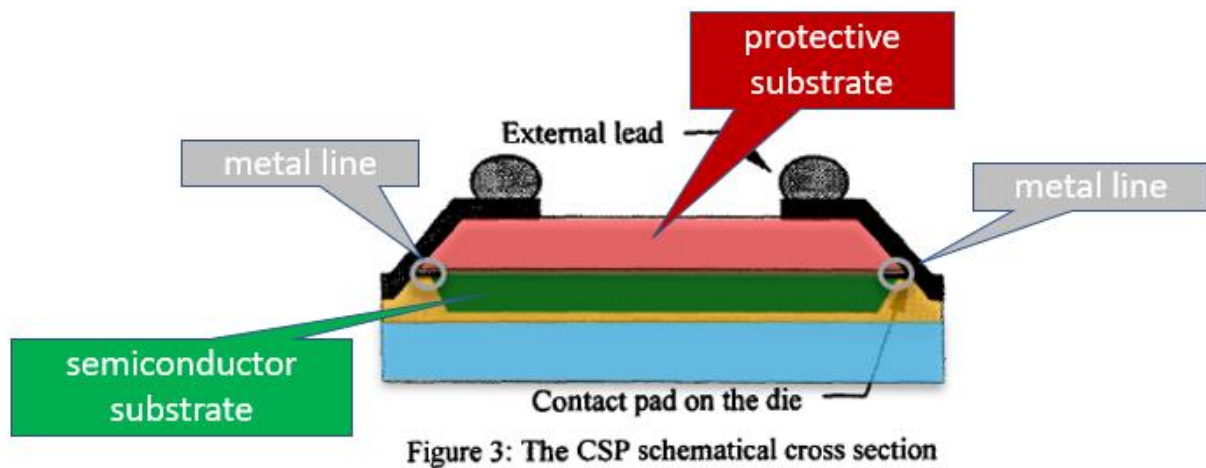
Figure 3: The CSP schematical cross section

Id., Fig. 3 (annotated). Indeed, the annotation in Figure 3 itself describes the "[c]ontact pad on the die." *Id.*

[1d] a protective substrate secured to the semiconductor substrate such that the metal line is located between the protective substrate and the semiconductor substrate; and

198. I am of the opinion that Badihi renders obvious this claim element.

199. Badihi's protective glass layer (first glass cover) corresponds to the claimed "protective substrate." Ex. 1101, 237. Badihi discloses the "protective glass layer is bonded to the active side of a silicon wafer with epoxy adhesive" (*i.e., a protective substrate secured to the semiconductor substrate*). *Id.* Badihi's Figure 3 discloses the resulting packaged image sensor where the **protective glass layer (first glass cover)** is **bonded** to the **silicon die** with the **bond pads** in between (*i.e., a protective substrate secured to the semiconductor substrate such that the metal line is located between the protective substrate and the semiconductor substrate*):

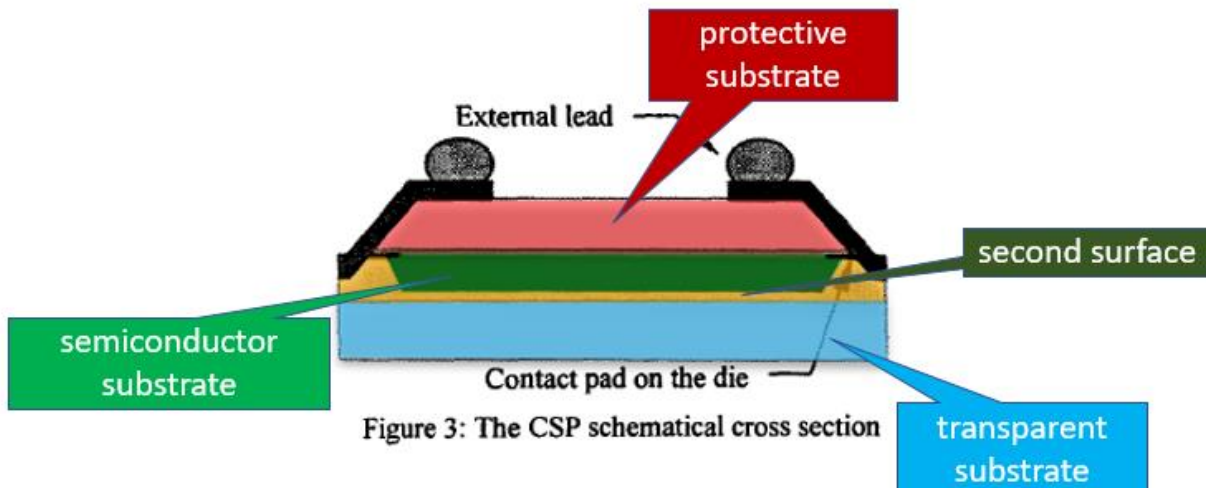


Id., Fig. 3 (annotated). Indeed, the annotation in Figure 3 itself describes the "[c]ontact pad on the die" and illustrates that it is between the silicon die and the protective glass layer (first glass cover). *Id.*

[1e] a transparent substrate secured to the second surface of the semiconductor substrate such that the semiconductor substrate is sandwiched between the transparent substrate and the protective substrate;

200. I am of the opinion that Badihi renders obvious this claim element.

201. Badihi's second glass cover corresponds to the claimed "transparent substrate." Ex. 1101, 237, Fig. 3. Badihi discloses the "second thin glass cover is bonded onto the silicon dies back side to achieve a complete protective enclosure for each die," resulting in "dies [that] are packaged and encapsulated in separate enclosures" (*i.e., a transparent substrate secured to the second surface of the semiconductor substrate*) *Id.*, 237, Fig. 3. Badihi further discloses that "[t]he glass transparent package encases the [i]mager [d]ie in a solid protecting optically clear enclosure." *Id.*, 239. Badihi's Figure 3 illustrates the resulting packaged image sensor where the **second glass cover** is **bonded** to the **silicon die** and the **protective glass layer (first glass cover)** and the **second glass cover** sandwich the **silicon die** (*i.e., a transparent substrate secured to the second surface of the semiconductor substrate such that the semiconductor substrate is sandwiched between the transparent substrate and the protective substrate*):



Id., Fig. 3 (annotated).

[1f] wherein the semiconductor substrate has a thickness defined such that the light-sensitive pixel region is effectively exposed through the second surface

202. I am of the opinion that Badihi renders obvious this claim element.

203. Badihi's Figure 2 illustrates the process step where the **silicon wafer** is grinded from its backside until 100 microns is left (*i.e.*, **second surface**):



Id., Fig. 2 (annotated).

204. A POSITA would readily understand that the purpose of grinding the silicon wafer from its backside before enclosing it in a glass transparent package is so that the photons absorbed by the remaining semiconductor substrate are closer to the photodiode for a better response (*i.e.*, **wherein the semiconductor substrate**

has a thickness defined such that the light-sensitive pixel regions are exposed from the backside of the silicon die).⁷ See *supra*, §V.C. Accordingly, Badihi at a minimum renders this claim limitation obvious.

3. Claim 2

[2pre]. The backside illuminated image sensor according to claim 1, further comprising

205. I am of the opinion that Merrill combined with Badihi renders obvious claim 2pre for the same reasons as claim 1 above.

[2a] a first adhesive layer located between the protective substrate and the semiconductor substrate, and

206. I am of the opinion that Badihi renders obvious this claim element.

207. Badihi's epoxy adhesive corresponds to the claimed "first adhesive layer." Ex. 1101, 237, Fig. 3. Badihi discloses the "thin protective glass layer is bonded to the active side of a silicon wafer with epoxy adhesive" (*i.e.*, ***a first adhesive layer located between the protective substrate and the semiconductor substrate***). See *supra*, claim 1d. Badihi's Figure 3 illustrates the resulting packaged image sensor where the **protective glass layer (first glass cover)** is

⁷ See *supra*, §X, Ground 1, 1f. A POSITA would readily understand that Badihi discloses what is described in the '319 patent.

bonded using epoxy adhesive to the **silicon die** (i.e., a first adhesive layer located between the protective substrate and the semiconductor substrate):

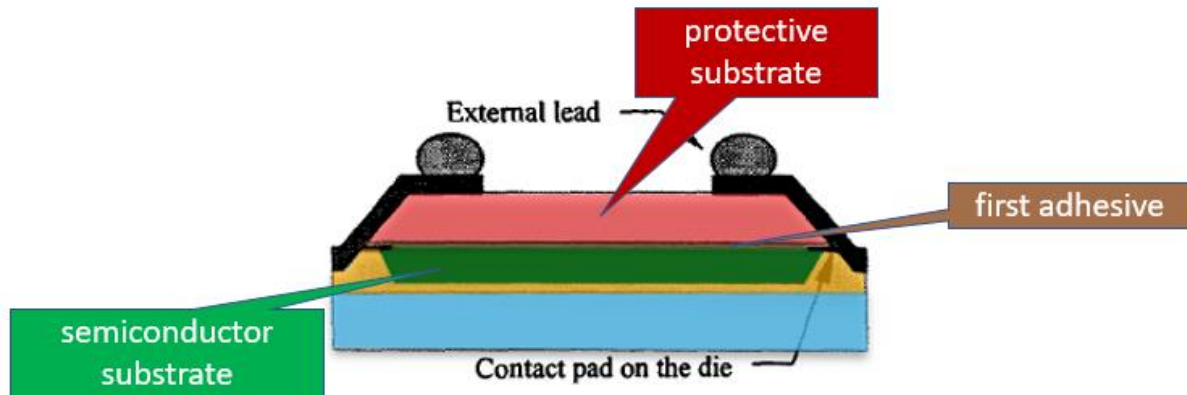


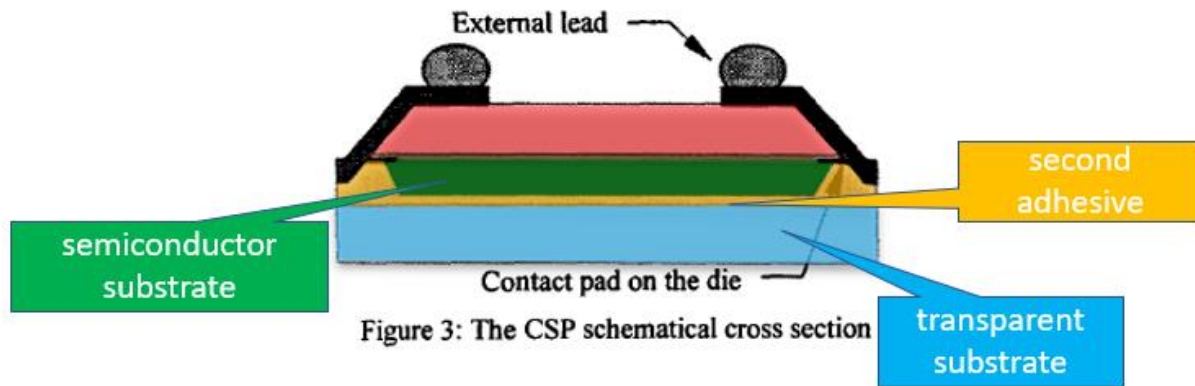
Figure 3: The CSP schematical cross section

Id., Fig. 3 (annotated).

[2b] a second adhesive layer located between the transparent substrate and the semiconductor substrate.

208. I am of the opinion that Badihi renders obvious this claim element.

209. Badihi's epoxy adhesive corresponds to the claimed "second adhesive layer." Ex. 1101, 237, Fig. 3. Badihi discloses a process step where "second thin glass cover is bonded onto the silicon dies back side to achieve a complete protective enclosure for each die." *Id.*, 237, Fig. 3. Badihi's Figure 3 illustrates the resulting packaged image sensor where the **epoxy adhesive** is applied on the backside of the **silicon dies** (i.e., a second adhesive layer located between the transparent substrate and the semiconductor substrate):



Id., Fig. 3 (annotated).

4. Claim 3

[3pre] The back-illuminated image sensor according to claim 2, wherein each of the plurality of light-sensitive pixel regions further comprises:

210. I am of the opinion that Merrill combined with Badihi renders obvious claim 3pre for the same reasons as claim 2 above.

[3a] a second diffusion region that is formed in the semiconductor substrate and spaced from the photodiode diffusion region;

211. I am of the opinion that Merrill discloses this claim element. *See supra*, §XI, Ground 2, claim 3a.

[3b] a first polysilicon gate structure provided between the second diffusion region and the photodiode diffusion region;

212. I am of the opinion that Merrill discloses this claim element. *See supra*, §XI, Ground 2, claim 3b.

[3c] a third diffusion region that is formed in the semiconductor substrate and spaced from the second diffusion region;

213. I am of the opinion that Merrill discloses this claim element. *See supra*, §XI, Ground 2, claim 3c.

[3d] a second polysilicon gate structure that is provided between the second diffusion region and the third diffusion region;

214. I am of the opinion that Merrill discloses this claim element. *See supra*, §XI, Ground 2, claim 3d.

[3e] a fourth diffusion region that is formed in the semiconductor substrate and spaced from third diffusion region;

215. I am of the opinion that Merrill discloses this claim element. *See supra*, §XI, Ground 2, claim 3e.

[3f] a third polysilicon gate structure that is provided between the third diffusion region and the fourth diffusion region;

216. I am of the opinion that Merrill discloses this claim element. *See supra*, §XI, Ground 2, claim 3f.

[3g] wherein the photodiode region is connected to the second polysilicon gate by a first metal line to form a source-follower transistor, and

217. I am of the opinion that Merrill discloses this claim element, as Merrill's local interconnect line 152 corresponds to the claimed "first metal line." *See supra*, §XI, Ground 2, claim 3g.

[3h] wherein the first metal line is located between the semiconductor substrate and the protective substrate.

218. I am of the opinion that Merrill discloses this claim element. *See supra*, §XI, Ground 2, claim 3h.

219. The “first metal line” is Merrill’s local interconnect line 152. *See supra*, claim 9a. A POSITA would readily understand that Merrill’s local interconnect line 152 is would be sandwiched between the substrate 110 on one side and a protective substrate on the other side (*i.e., wherein the first metal line is located between the semiconductor substrate and the protective substrate*). *See supra*, §V.D.

5. Claim 5

[5pre] The backside illuminated image sensor according to claim 1,

220. I am of the opinion that Merrill combined with Badihi renders obvious claim 5pre for the same reasons as claim 1 above.

[5a] wherein the transparent substrate is glass.

221. I am of the opinion that Badihi renders obvious this claim element for the same reasons discussed above in connection with claim 1e. *See supra*, claim 1e.

6. Claim 6

[6pre]. The backside illuminated image sensor according to claim 1, further comprising

222. I am of the opinion that Merrill combined with Badihi renders obvious claim 6pre for the same reasons as claim 1 above.

[6a] a plurality of metal leads formed on the protective layer.

223. I am of the opinion that Badihi renders obvious this claim element.

224. Badihi's individual leads corresponds to the claimed "metal leads." Ex. 1101, 237, Fig. 3. Badihi discloses that "[d]eep notches are drawn between the dies, revealing the cross-section of the bond pads" and that "[a] metal layer, patterned by lithography to individual leads, is deposited to contact the bond pads at their cross sections" (*i.e., a plurality of metal leads formed*). *Id.*, 237. Badihi's Figure 3 illustrates the resulting packaged image sensor where the **individual leads** are formed on the **protective glass layer (first glass cover)** (*i.e., a plurality of metal leads formed on the protective layer*):

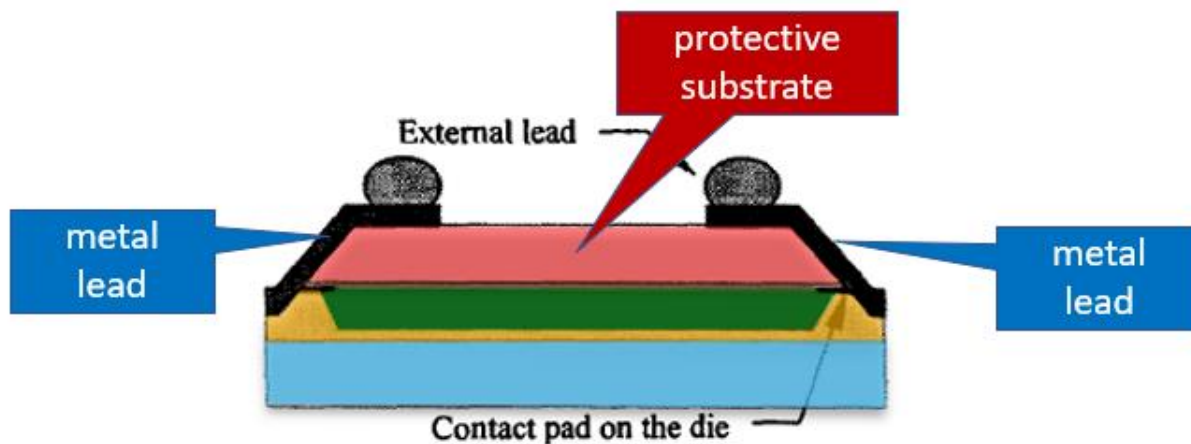


Figure 3: The CSP schematical cross section

Id., Fig. 3 (annotated).

XVI. GROUND 7: MERRILL IN VIEW OF BADIHI AND WATANABE RENDERS OBVIOUS CLAIM 4

225. I am of the opinion that Merrill in view of Badihi and Watanabe renders obvious claim 4 of the '319 patent.

1. Reasons to Combine Merrill and Badihi with Watanabe

226. A POSITA would have been motivated to modify Merrill's CMOS APS cell and Badihi's manufacturing process for BSI CMOS image sensors to thin the silicon substrate to a thickness of 5 to 15 μm as taught by Watanabe. During semiconductor fabrication, including image sensor fabrication, the beginning thickness of a typical raw silicon wafer is on the order of 500 μm . Ex. 1010, 145. BSI CMOS image sensors must be much thinner than this 500 μm starting thickness so that photons may be absorbed by the remaining substrate and

photogenerated electrons may be captured by the photodiode and not be recombined with holes within the substrate. *See supra*, §V.C.

227. Similarly, Badihi discloses grinding the silicon wafer from back to 100 microns. Ex. 1101, Fig. 2. It was therefore commonplace at the time of the '319 patent for the substrate to be thinned to a fraction of their starting thickness during manufacturing of BSI sensors. *Id.* Watanabe is an example of a substrate thinning technique applicable to BSI image sensors like the CMOS image sensor depicted in Badihi's Figure 4. *Id.* A POSITA would have understood that Badihi's substrate must have been thinned using a technique such as that taught in Watanabe. *See supra*, §V.C. Accordingly, applying the teachings of Watanabe to the CMOS APS with photodiodes in Merrill and image sensor manufacturing process of Badihi would lead to a suitably thin substrate that ensures photons are absorbed by the remaining substrate and electrons are generated closer to the photodiode for better response. *See supra*, §§V.A-D. Indeed, it was common knowledge that a silicon layer in a photodiode-based image sensor must be thick enough to absorb visible light, but not so thick that diffusing electrons would be likely to recombine before reaching the p/n junction. Ex. 1052, 5:8-31; *see supra*, §V.C. This thickness depends on many factors, but is typically on the order of 10's of microns. Ex. 1052, 5:8-31; *see supra*, §V.C.

228. Watanabe's substrate thinning to a thickness of 5 to 15 microns is readily applicable to Merrill's CMOS APS with photodiodes and Badihi's manufacturing process, and a POSITA could have modified Merrill's CMOS APS with photodiodes and Badihi's manufacturing process to include Watanabe's substrate thinning to a thickness of 5 to 15 microns with a reasonable expectation of success. *See supra*, §§V.A-C. Indeed, in Badihi's design, the substrate must be thinned to minimize unwanted absorption of backside-incident photons. *See supra*, §V.C.

2. Claim 4

[4pre] The backside illuminated image sensor according to claim 1,

229. I am of the opinion that Merrill combined with Badihi and Watanabe renders obvious claim 4pre for the same reasons as claim 1 above.

[4a] the thickness of the semiconductor substrate is in the range of 10 to 15 microns.

230. I am of the opinion that Merrill combined with Badihi and Watanabe renders obvious claim this claim element.

231. Badihi discloses a process step where the silicon wafer is grinded from its backside to 100 microns. Ex. 1101, Fig. 2. Watanabe discloses from the backside of the substrate 1, first polishing the silicon plate 1a then etching the remaining silicon plate 1a and silicon oxide film 1b, leaving only the silicon layer

1c with its 5 to 15 μm thickness, which overlaps with the claimed “10 to 15 microns” (*i.e.*, ***the thickness of the semiconductor substrate is in the range of 10 to 15 microns***). Ex. 1007, ¶¶17, 19, Fig. 2c; *see supra*, §V.C.

232. In the combination of Badihi and Watanabe, silicon layer 1c, with a 10 to 15 micron thickness, is used in place of Badihi’s silicon die. A POSITA would have been motivated to make this modification for the reasons discussed above. *See supra*, §V.C. A POSITA would have been motivated to make this modification for the reasons discussed above. *See supra*, §V.C.

XVII. CONCLUSION

233. For the aforementioned reasons, in my opinion, to a person of ordinary skill in the art, the Challenged Claims of the ’319 patent are invalid in view of the prior art.

234. I understand that the Patent Owner has not asserted secondary considerations of non-obviousness. I reserve the right to respond to any such assertions.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on the information and belief are believed to be true; I declare under penalty of perjury that the foregoing is true and correct, and understand that willful false statements and the like are punishable by fine or imprisonment, or both pursuant to 18 U.S.C. 1001.

Date: December 16, 2022

Respectfully Submitted

A handwritten signature in black ink, appearing to read 'Konstantinos P. Giapis', with a long horizontal flourish extending to the right.

Dr. Konstantinos P. Giapis