

PROVISIONAL APPLICATION FOR PATENT COVER SHEET

Request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53 (b)(2).

A/PROV

01/14/99
 Jc541 U.S. PTO

Docket Number	08305/063001 99-01	Type a plus sign (+) inside this box →	+
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Jc541 U.S. PTO
 60/116144
 01/14/99

INVENTOR(s)/APPLICANT(s)			
LAST NAME	FIRST NAME	MIDDLE INITIAL	RESIDENCE (CITY AND EITHER STATE OR FOREIGN COUNTRY)
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Fossum	Eric		La Crescenta, CA
Doudoumopoulos	Nick		Pasadena, CA

TITLE OF THE INVENTION (250 characters max)	
BACKSIDE ILLUMINATION OF CMOS IMAGE SENSOR	

"EXPRESS MAIL" Mailing Label Number EM32746-107US
 Date of Deposit January 14, 1999

I hereby certify under 37 CFR 1.10 that this correspondence is being deposited with the United States Postal Service as "Express Mail Post Office To Addressee" with sufficient postage on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

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ENCLOSED APPLICATION PARTS (check all that apply)				
☒ Specification	Number of Pages	9	☒ Small Entity Statement	
☐ Drawing(s)	Number of Sheets		☐ Other (specify)	

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT (check one)		
☒ A check or money order is enclosed to cover the filing fees		
☒ The Commissioner is hereby authorized to charge filing fees and credit Deposit Account Number: 06-1050	FILING FEE AMOUNT (\$)	\$75.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

- ☒ No.
☐ Yes, the name of the U.S. Government agency and the Government contract number are:

Respectfully submitted,

SIGNATURE Scott C. Harris

Date 1/14/99

TYPED or PRINTED NAME Scott C. Harris

REGISTRATION NO.
(if appropriate)

32,030

☐ Additional inventors are being named on separately numbered sheets attached hereto

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

Burden Hour Statement: This form is estimated to take 2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Box Provisional Application, Assistant Commissioner for Patents, Washington, DC 20231.

Applicant or Patentee: Robert Nixon et al.
Serial or Patent No.:
Filed or Issued: 1/14/99
For: BACKSIDE ILLUMINATION OF CMOS IMAGE SENSORS

**VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) and 1.27(c)) - SMALL BUSINESS CONCERN**

I hereby declare that I am

- ☐ the owner of the small business concern identified below:
☒ an official of the small business concern empowered to act on behalf of the concern identified below:

Name of Small Business Concern: Photobit Corporation

Address of Small Business Concern: 135 North Los Robles Avenue, 7th Floor, Pasadena, CA 91101

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled BACKSIDE ILLUMINATION OF CMOS IMAGE SENSORS by inventor(s) ROBERT NIXON; ERIC FOSSUM AND NIKK DOUDOUNPOULOS described in

- ☒ the specification filed herewith.
☐ application serial no., filed .
☐ patent no., issued .

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(a). NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Full Name: _____

Address: _____

☐ INDIVIDUAL ☒ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status when any new rule 53 application is filed or prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent on which this verified statement is directed.

Name: Claudine Antonino

Title: New Technology Manager

Address: 135 N. Los Robles Ave 7th Fl Pasadena CA 91101

Signature: Claudine Antonino

Date: _____

PROVISIONAL APPLICATION

UNDER 37 CFR 1.53(b)(2)

TITLE: BACKSIDE ILLUMINATION OF CMOS IMAGE SENSORS

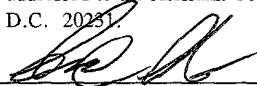
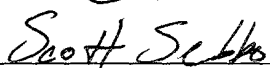
APPLICANT: ROBERT NIXON; ERIC FOSSUM AND NICK
DOUDOUMOPOULOS

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Date of Deposit 1-14-99

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Invention Disclosure Technical Description**BACKSIDE ILLUMINATION OF CMOS IMAGE SENSORS**

A CMOS image sensor die is fabricated and packaged to allow the light sensitive area of the die to be illuminated from either the front side (present state-of-the-art) or from the backside, or simultaneously from both front and back. The implementation is achieved using wafer level processing that facilitates photon collection at both surfaces. Further, this approach permits processing at the wafer level to allow the deposition of color filter arrays (CFA) on either surface.

In prior art, a CMOS imager sensor is illuminated from the front (or top side) of the silicon die. Because of processing features (metalization, polysilicon, diffusions, etc.) the pixel area is partially obscured, resulting in a loss of photons reaching the sensitive area and a reduction in the area in which photons are effectively collected. The consequence of this, is a reduction in the overall sensitivity of the sensor. If photons were to be collected from the back side of the pixel area, these obstacles would be overcome, resulting in a significant improvement in sensitivity. The problem in backside illumination has been the thickness of the bulk silicon and the packaging technology to allow the backside to be exposed to the illuminating source. The thickness of a typical silicon wafer needs to be thinned considerably in order to absorb the photons in the sensitive area. Prior approaches have primarily utilized methods for thinning die after they have been scribed from a wafer and then packaging them in specialized packages which give support to the thin die while providing unobstructed ports for illumination from the back side. This approach is costly and time consuming and does not lend itself well to a cost driven consumer market.

These problems can be solved with wafer level processing techniques that lead to packaged die at the wafer level. The attached paper describes such a packaging technique that can be utilized for CMOS imaging from the front side of the silicon die. With suitable modification of the approach, these die can be made to image effectively from either the front side or the back side or from both simultaneously (see figures 1 and 2). The essence of this disclosure is:

1. Backside imaging using wafer level processing techniques to obtain thinning and integrated packaging of the image sensor.
2. Simultaneous imaging from both the front and backside of the sensor.
3. Wafer level CFA on the back side of the wafer.
4. Wafer level process modifications to accommodate the above.

In the process flow described in the attached paper, the ability to do backside imaging without CFA can be accommodated by modifying the described process by 1) thinning the silicon to approximately _____ microns and 2) relocating the the bump

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Invention Disclosure Technical Description

BACKSIDE ILLUMINATION OF CMOS IMAGE SENSORS

contacts and interconnect lines away from the image area of the die and covering with optically transparent material to give support. The resulting packaged die would be capable of imaging from either side.

To achieve color imaging, the CFA will be processed at the wafer level and deposited on the thinned backside of the silicon. In order to do this, the bump contacts and related interconnect need to be moved to the top surface. After deposition of the CFA, optically transparent material would be added to the backside to provide protection and give added mechanical rigidity to the package. To do color imaging from both sides, the CFA would be applied to the front side during normal processing and the bump contacts would be placed outside of the imaging area.

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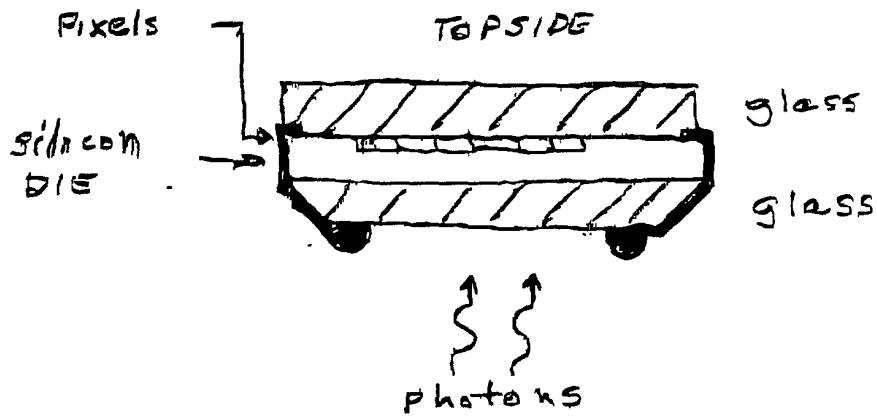


Figure 1.

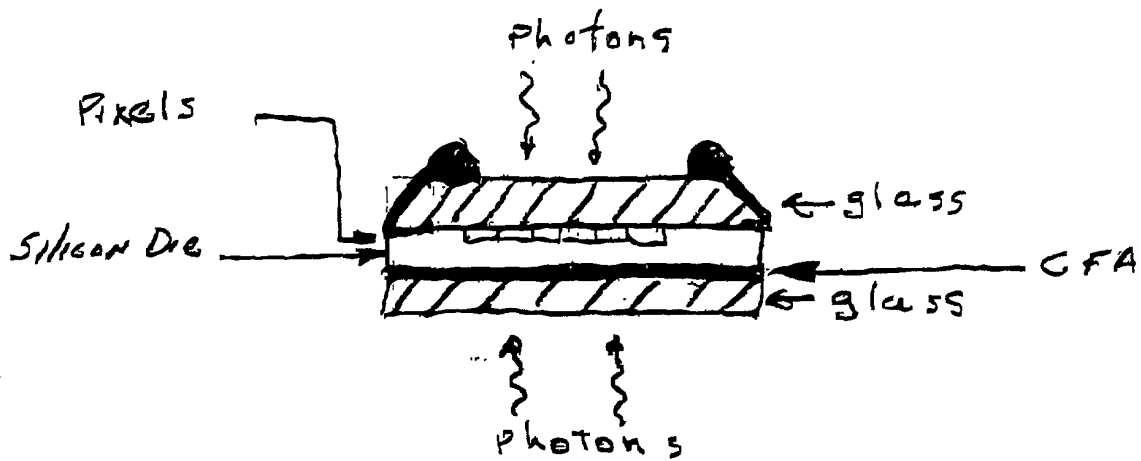


Figure 2

PHOTOBIT CONFIDENTIAL

A CSP Optoelectronic Package For Imaging And Light Detection Applications

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Key Words: ShellCase, UTP, CSP, CCD, CMOS Camera, Imaging, Light Detection, Optoelectronic, SMT process, Dichroic filter, Reliability.

INTRODUCTION:

Portability and miniaturization are key factors in the electronic product market.

A fast growing market is Digital Photography, with a variety of small size and low weight electronic products, for professional and personal photography, medical and video conferencing.

The development of low cost imaging devices drives the market for low cost Packages for Opto-Electronic imaging dice.

A recent packaging technology development (1,2) offers a substantial reduction of both costs and physical dimension of the Opto-electronic package.

The Digital Imaging Market:

The popular use of consumer digital camera is fast becoming common place. It's two major drivers and contributors are: the Web, and computer based digital photography.

The use of digital cameras is compelling. The elimination of consumables (films, paper) and the immediate imaging capability of digital photography seems to be a strong attraction for the product. Recent introduction of low cost yet high quality color printers that produce "photo quality" images is serving to further inspire the market.

The recent evolution of CMOS imaging devices has fueled a new wave of optronic imaging devices. This trend is dominated by the US semiconductor companies, identifying a new market opportunity, well fit to their core technology.

Price and Technology Trends

Diverse competitors, ranging from traditional camera manufacturers and consumer electronics manufacturers,

to PC peripheral manufacturers, are battling to define the future of digital imaging. This results in significant price

reductions while digital image resolutions continue to soar to new levels.

Furthermore, the use of digital CMOS makes it possible to integrate signal-conditioning elements DSP's, analog signal conditioners and communications interface—on the same substrate with the light-sensing elements, further reducing the electronics cost.

As has been typical in the consumer electronics markets, consumer market growth will drive aggressive cost reduction to expand the market even farther. For the optronic imaging devices, a major element in that cost reduction will be in the packaging of the imager die.

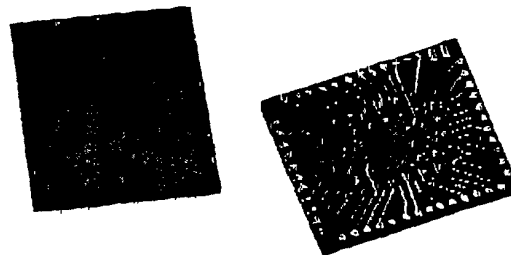


Figure 1: Shell-OP the Optronic CSP

The Opto-Electronic CSP:

A Die Size, Ultra Thin Opto-Electronic Package was developed. The Assembly process extends the semiconductor processing to the packaging of Integrated Circuits (Figure 1).

The glass transparent package encases the Imager Die. The assembly is held using a clear epoxy. A selective spectral filter can be embedded within the package close to the active layer of the die

The package has special features both in relation to conventional Opto-Electronic packaging and Chip Size Packaging.

- True Die Size package.
- Configurable Spectral transparency.
- Ability to integrate Absorption or interference (dichroic) optical filters into the package
- Ability to integrate Color Filter Array (CFA) into the package.
- Extremely low thickness: 0.6 to 2.0 mm.
- Peripheral or area array configuration.
- The package, even as thin as 0.6 mm, offers a complete mechanical enclosure to the die. It does not leave any exposed Silicon, and seals the Silicon from the outside world, providing mechanical and environmental protection.
- Low cost -- particularly for small dies.

The packaging is implemented at the wafer level, where an optronic device is completely packaged using semiconductor manufacturing processes. The very small form factor, in comparison to the conventional optronic package, (see Figure 2).

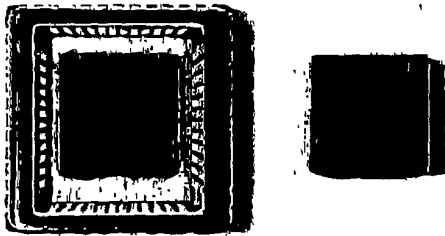


Figure 2: A comparative view, a regular Optronic Package LCC type, and a die size Optronic CSP

The schematical cross sectional view of the package (Figure 3) shows a thin silicon substrate, which is sandwiched between two thin protective plates on the top and bottom sides. An epoxy adhesive layer attaches the glass plates to the Silicon and surrounds and protects the edges of the Silicon die. Electrical leads connect to the pads of the die by a non-bonding technique.

The package is available with either perimeter or area array leaded configurations. Solderable leads have

itches down to 0.5 mm in the peripheral configuration and 0.8 mm in the area array configurations.

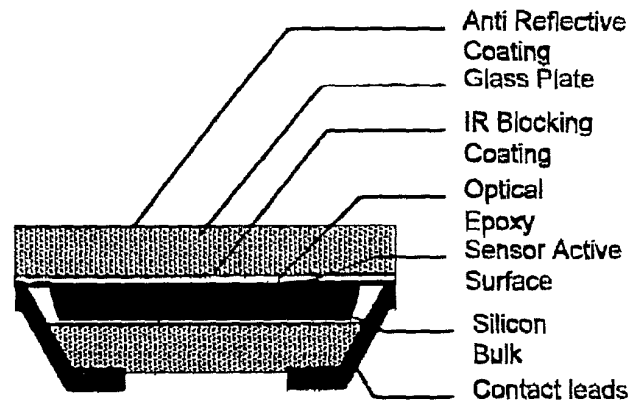


Figure 3: The Optronic CSP-Schematic

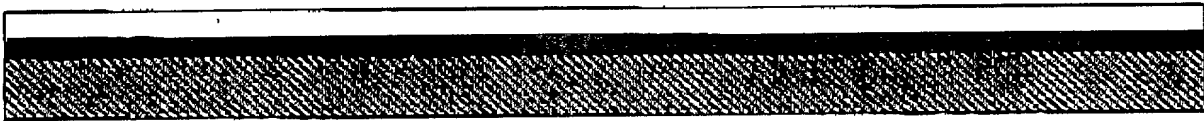
The Manufacturing Process:

The package manufacturing uses thin film and related processes that are commonly in use to manufacture Semiconductors. The Optronic CSP is thus an extension of the IC manufacturing processes. The dies are packaged and encapsulated into separate enclosures while still in wafer form.

The basic steps in the manufacturing process are as follows (Figure 4):

- A thin protective layer is bonded on to a silicon wafer bearing active devices while the active surface of the IC is facing up into the encapsulate.
- The silicon material between the dies is etched away (back side), yielding individual IC's attached to the supporting cover.
- The grooves between the dies are filled with an inert material, and a second thin cover is bonded onto the silicon dies back side to achieve a complete protective enclosure for each die.
- Deep notches are drawn between the dice, so as to reveal the pads cross section.
- A metal layer is deposited so as to contact the metal pads at their cross sections. The metal layer is patterned by a lithography process to individual leads, contacting the pads and forming a soldering pad on the upper surface of the package. Finally, contacts are plated by either gold or lead-tin.
- Wafer dicing yields individual packaged dies.

Figure 4: Optron Package Schematical Process



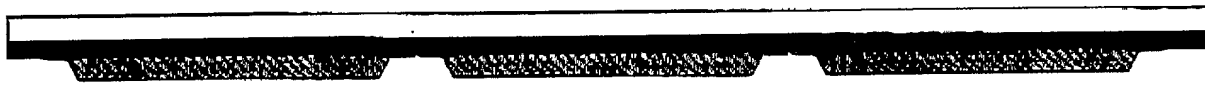
1st. The incoming die is coated with a Mosaic layer

2nd. The incoming lass plate for Bond-1 is coated with a Filter layer

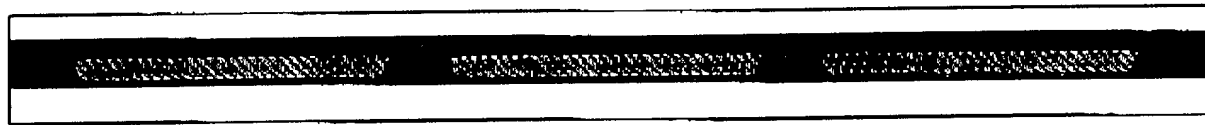
3rd. Attach Glass Cover onto Wafer Active surface, use Optical Clear Epoxy, Filter side faces the die active surface



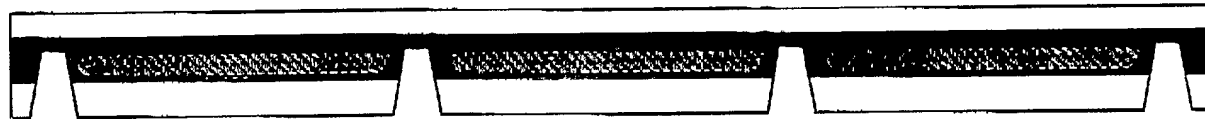
D. Grind the Silicon from the back side of the wafer down to 70 microns.



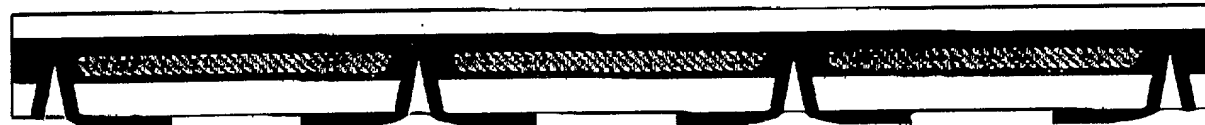
E. Etch the silicon along the dice lines separating the dies.



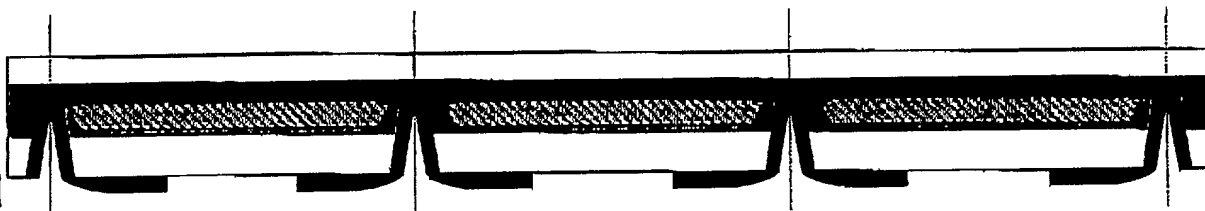
F. Attach a second glass plate from the back side, the epoxy fills the trenches between the dies.



G. Notch process along the dice lines, carried from the back side of the wafer.



G. Lead deposition on notched side



H. Dice the wafer into singulate pre-packaged dies

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Optical characteristics of the Package Components:

Refraction indexes for the glass and epoxy are shown on the following table.

Material	Index of Refraction
Glass	1.5275
Epoxy	1.5400

Figures 5 and 6 show the absorption spectra of the glass and the epoxy.

The figures indicate little absorption throughout the visible range (see APPENDIX 1).

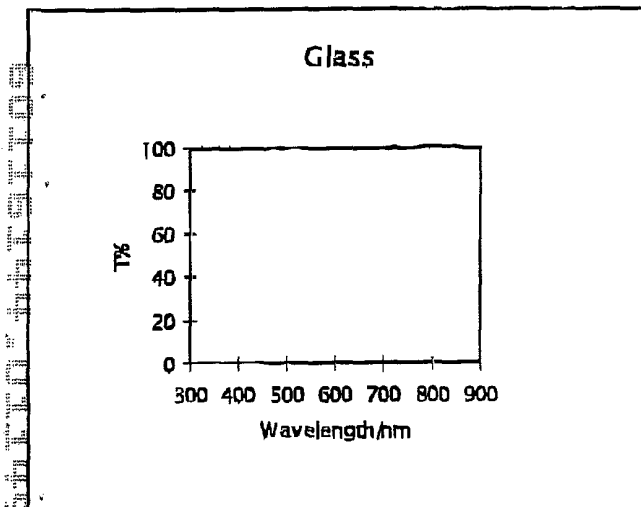


Figure 5: Transmission characteristics of the glass plate used.

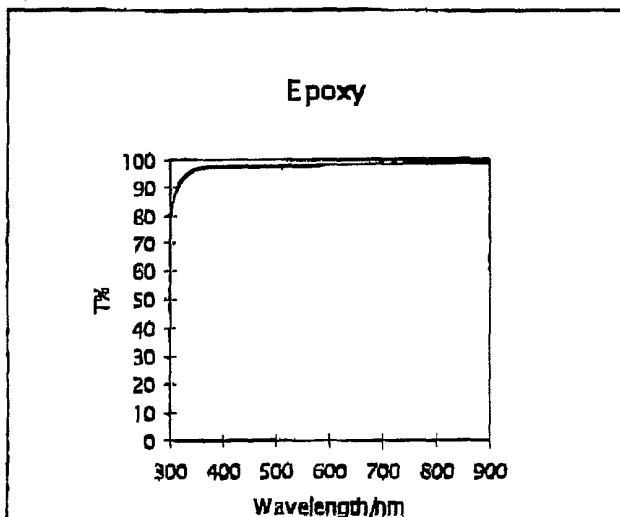


Figure 6: Transmission characteristics of the optically clear epoxy.

The optronic dimensional accuracies and tolerances.

The dimensional and assembly tolerances and accuracies of the Electro-Optical imager die assembly in the package is a major issue, far more sensitive than for ordinary IC packaging.

Accurate optical assembly of the device package at the system level depends on the assembly process accuracy, and reproducibility.

These mechanical tolerances, translation of the imager, rotation and tilt of the imager die in relation to the reference plan, are all critical for the effective implementation of the imager in the next level system.

Table 1, compares the mechanical accuracies between the Wafer Level Optical Package, and two regular, mechanically assembled, optical packages.

Note the excellent accuracies of the wafer level process, in comparison to mechanical assembly.

Table 1: Mechanical features and Dimensional tolerance comparison for different Packages.

Mechanical Feature	Package A	Package B	Opto CSP
Center Translation of effective image area (X, Y)	$\pm 150\mu$	$0 \pm 85\mu$	$\pm 35\mu$
Rotation angle of effective image area (in focal plane)	$< \pm 1^\circ$	$< \pm 0.25^\circ$	$< \pm 0.01^\circ$
Tilt of effective Image area (Z-axis)	$< 60\mu$	$< \pm 25\mu$	$< 10\mu$
Thickness of cover glass & refractive index	0.75 mm $n = 1.5$	0.55 mm ± 0.05	> 0.4 to 1 mm $n = 1.53$
Self Centering	No	No	Yes

Self Centering.

One of the main advantage of Bump Solder Array interconnects is the "self centering" phenomenon that occurs during solder reflow.

The solder bumped Optical CSP (see Figure 7) is placed on the pad with solder paste. Exact placement is not required, in fact, a placement of only 50% of the sphere on the soldering pad will still allow the self adjustment action.

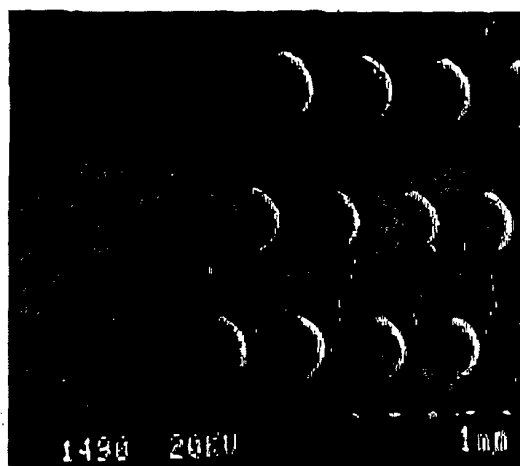


Figure 7: Solder Bump Array on the Optical CSP.

For many optical assemblies, the accurate alignment of the optical components is critical, and thus requires special care as well as specialized assembly tools.

With the "self centering" process, the device even loosely placed on the board, will align itself to exact placement in relation to the pads and trace patterns on the board. The surface tension of the molten solder drives the self alignment.

Alignment in the lateral dimensions is not the only "self centering" action that occurs. There is vertical alignment as well, that occurs as apart of the setting of the component, balanced with the surface tension of the molten solder.

This vertical alignment can compensate for some of the warpage and irregularities that might be seen in the board, again improving and simplifying the accurate assembly of the Optical system (3).

The integrated filter:

The Optronic CSP allows the integration of a filter or color layer in the package.

Two alternatives for the filter integration are available:

1. Coated filter for IR Blocking (Figure 3)
2. Absorption filter for IR Blocking (Figure 8)

The purpose of integrating the Infra - Red blocking filter in the package is to compensate for the different spectral response of the Silicon detector and the human retina. Not only does the silicon detect in the Ultra Violet and Infra Red range beyond the visual range, but the spectral response in the visible spectra is different for the eye and the silicon detector.

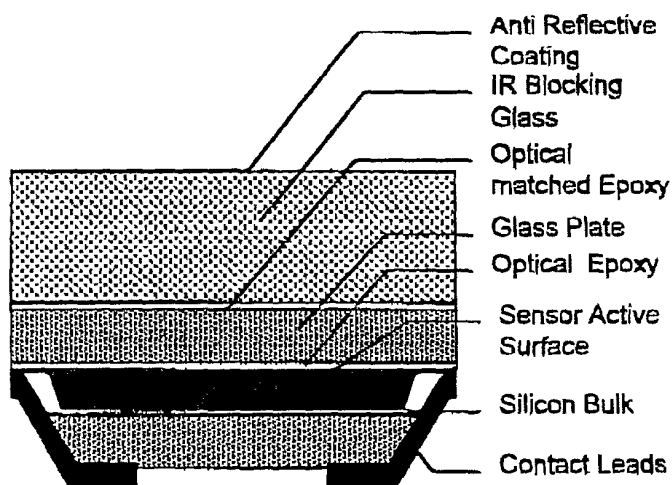


Figure 8: Optronic CSP - with IR Blocking Glass Filter

Correcting Filters such as the one shown on Figure 9, correct the Silicon detection response to match the eye response.

These filters are commercially available as either interference, thin film type or absorption type, and are an essential part of every Solid state imaging element.

The integration of the filter into the package allows the use of the minimal filter plate area (silicon detector size). Thus saving costs, by reducing the number of optical components required. Furthermore, filter integration saves costs, by reducing the filter size required.

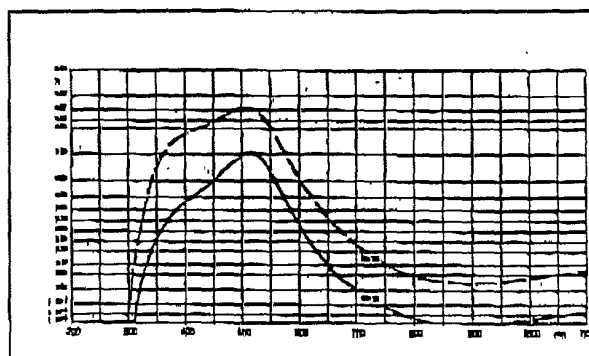


Figure 9: IR Blocking Glass Filter type BG 18 and BG 38 (source SCHOTT GLAS, Optics Div.)

Reliability and environmental Testing:

The Shell-OP package is undergoing reliability tests, using custom test dies. Tests are performed with the packaged die SMT mounted to a Printed Circuit Board. Table 2 details the test program.

Test	Conditions
THB	85°C; 85% RH; 5V Bias
Endurance	125°C, 50 mA/Lead, $J = 3.3 \times 10^4 \text{ A/cm}^2$
Thermal Cycling	-40°C to +85°C, air to air, 1000 cycles
Popcorn	JEDEC A112, level 2

Summary:

An Optronic CSP package has been developed, achieving a reduction of size as well as a reduction in the manufacturing costs. The manufacturing process is carried out at the wafer level, and extends IC manufacturing processes into device packaging. CMOS Imager dice have already been packaged with the optical CSP, and are currently undergoing both optical qualification and reliability tests.

REFERENCES:

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2. Badihi & al. , ShellBGA a Thin Chip Size Integrated Circuit Package, ISHM Workshop on CSP, August 1996.
3. Y.C. Lee, "studies on Solder Self Alignment", LEOS 94 conference proceedings, Vol. 1, pp. 73 - 74