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(54) [TITLE OF THE INVENTION] MANUFACTURE OF SEMICONDUCTOR DEVICE

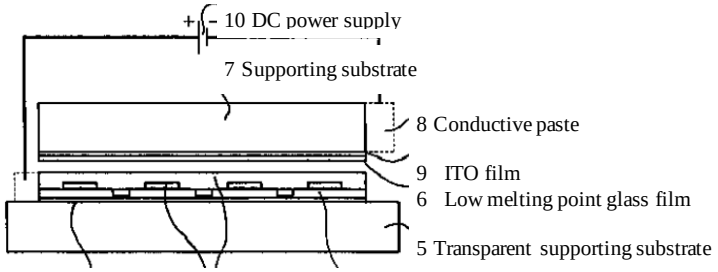
(57) Abstract

PURPOSE: To provide a manufacturing method of a semiconductor device, wherein a thinned substrate can be bonded to an insulating supporting substrate firmly without generating bubbles, etc., in an insulating supporting substrate regarding a manufacturing method of a semiconductor device wherein the thinned substrate is transferred to another supporting substrate by forming a semiconductor device.

CONSTITUTION: In a manufacturing process of a back-thinned infrared detector, wherein after forming a semiconductor element 2 on the surface of a silicon layer 1c of an SOI substrate, a polymer resin 3 is buried and flattened in the forming region of the semiconductor element 2, the polymer resin 3 is bonded to a transparent supporting substrate 5, and the insulator side of the SOI substrate at an opposite side of the forming region of the semiconductor element 2 is polished, thinning the silicon layer 1c, it also includes a step of bonding this thinned silicon layer 1c to a supporting substrate 7, which has insulation property and through which infrared rays pass, at a normal temperature while applying a DC voltage through a low melting point glass film 6, and a step of peeling off this transparent supporting substrate 5 from the polymer resin 3 and removing the polymer resin 3.

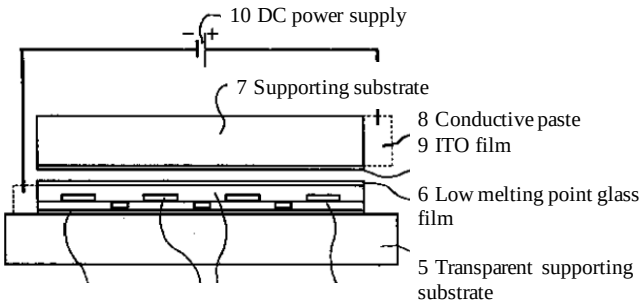
A diagram showing an embodiment of the present invention

(a) A schematic diagram of an embodiment in the state of anodic bonding



4 Wax film 2 Semiconductor element 1c Silicon layer 3 Polymer resin

(b) A schematic diagram of another embodiment in the state of anodic bonding



4 Wax film 2 Semiconductor element 1c Silicon layer 3 Polymer resin

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[Scope of Patent Claims]
[Claim 1] A method of manufacturing a semiconductor device, characterized in that,
in a manufacturing process of a back-thinned infrared detector, wherein after forming a semiconductor element (2) on the surface of a silicon substrate, or on the surface of a silicon layer (1c) of the SOI substrate (1) in which the silicon layer (1c) is provided on the insulator (1a), a resin (3) is buried in the forming region of the semiconductor element (2) to planarize the forming region of the semiconductor element (2), the flattened resin (3) after embedding the forming region of the semiconductor element (2) is bonded together to the transparent supporting substrate (5), thinning the silicon layer (1c) by polishing the silicon substrate, or the insulator (1a) side of the SOI substrate (1) on the side facing the forming region of the semiconductor element (2);
the method also includes
a step of bonding this thinned silicon substrate, or silicon layer (1c) to a supporting substrate (7), which has an insulation property and through which infrared rays pass, at a normal temperature while applying a DC voltage through a low melting point glass film (6), and
a step of peeling off this transparent supporting substrate (5) from the resin (3) in which the semiconductor element (2) has been embedded, and removing the embedded resin (3).
[Detailed Description of the Invention]
[0001]
[Industrial Field of Application] The present invention relates to a semiconductor device, micromachines, etc., in which micromechanical parts such as gears are formed of polysilicon, etc. and more particularly, to a method of manufacturing a semiconductor device in which a substrate thinned after forming a semiconductor device is transferred to another supporting substrate.
[0002]
[Prior art] Conventionally, in the case of forming a CMOS-type semiconductor element on a semiconductor substrate made of silicon, or the like, to manufacture an infrared detecting element; the surface of the silicon substrate is formed with a silicon oxide film, electrodes, a wiring layer, or the like. When infrared rays are incident on the surface side of the silicon substrate on which the semiconductor element is formed, the infrared ray is shielded by the wiring layer and electrodes and does not enter into the forming region of the semiconductor element, so in order to manufacture a highly sensitive infrared imaging element, a back-thinned infrared detector is manufactured in which infrared rays are incident from the back side of the silicon substrate on which the semiconductor element is not formed.
[0003] However, if the thickness of the silicon substrate is large, infrared rays incident from the back side are likely to be absorbed by the silicon substrate, the thickness of the silicon substrate must be reduced to 10 μm or less, and if the silicon substrate is made of a thin plate having a thickness of 10 μm or less, it is fragile and difficult to handle.
[0004] For this reason, conventionally adopted, as shown in FIG. 5, is a method of bonding, using an epoxy resin 36, a thin semiconductor substrate 31 on which a semiconductor element 32 is formed to an insulating supporting substrate 37 made of sapphire, or the like, through which infrared rays pass.
[0005]
[Problem to be Solved by the Invention] With the conventional method for manufacturing a semiconductor device described above, as described above, an adhesive is used to bond the semiconductor substrate to an insulating supporting substrate made of sapphire, or the like, through which infrared rays pass. However, it is technically very difficult to stretch the adhesive evenly and thinly. Also, air bubbles are likely to form inside the adhesive. When the infrared imaging device manufactured by bonding a semiconductor substrate to a supporting substrate in this way is exposed to room temperature when not operating from the temperature of liquid nitrogen at operating temperature, the air in the air bubbles expands due to the difference in temperature, and cracks occur in the adhesive, which is a problem.
[0006] In view of the above circumstances, it is an object of the present invention to provide a method of manufacturing a semiconductor device with which a thinned semiconductor substrate after forming a semiconductor element can be firmly bonded to an insulating supporting substrate without generating bubbles, or the like.
[0007]
[Means for Solving the Problem] In the method for manufacturing a semiconductor device, in a manufacturing process of a back-thinned infrared detector, wherein after forming a semiconductor element on the surface of a silicon substrate, or on the surface of the silicon layer of the SOI substrate in which the silicon layer is provided on the insulator, a resin is buried in the forming region of the semiconductor element to planarize the forming region of the semiconductor element, the resin flattened after embedding the forming region of the semiconductor element and the transparent supporting substrate are bonded together, thinning the silicon layer by polishing the silicon substrate, or the insulator side of the SOI substrate on the side facing the forming region of the semiconductor element; the method also includes a step of bonding this thinned silicon substrate, or silicon layer to a supporting substrate, which has insulation property and through which infrared rays pass, at a normal temperature while applying a DC voltage through a low melting point glass film, and a step of peeling off this transparent supporting substrate from the resin in which the semiconductor element is embedded, and removing the embedded resin.
[0008]
[Action of the Invention] In other words, in the present invention, after a semiconductor element is formed on one surface of a semiconductor layer, a thin semiconductor layer and a supporting substrate having a thermal expansion coefficient similar to that of the semiconductor layer and through which infrared rays pass and having an insulating property are bonded by room-temperature anodic bonding, so that the semiconductor device can be firmly bonded. Even when the semiconductor device is exposed from 77°K of the liquid nitrogen temperature of the operating temperature of the operating temperature to room temperature of the non-operating temperature, it is possible to prevent the semiconductor layer from separating from the supporting substrate.
[0009] This cold anodic bonding is disclosed in the literature (Sensors and Actuators, A-21-A23 (1990) 931-934), “Low temperature Silicon-to-silicon Anodic Bonding with Intermediate Low Melting Point Glass, by MASAYOSHI

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ESASHI, AKIRA NAKANO, SHUICHI SHOJI, and HIROYUKI HEBIGUCHI".

[0010] According to this document, as shown in FIG. 4, when one silicon wafer 11 is coated with a glass layer 16 by a sputtering method, and the other silicon wafer 21 to be bonded is placed facing the other, and a DC power supply 20 applies a negative DC voltage to the silicon wafer 11 on which the glass layer 16 is sputtered, negative ions gather in a part of the glass layer 16 sputtered by the electric field of the applied DC voltage to form a polarized region 16a, and the negative ions in the polarized region are attracted to the other silicon wafer 21 to which a positive voltage is applied, and the silicon wafers are bonded together.

[0011] In the present invention, this principle is used, as shown in FIG. 1(a), to ensure that the voltage is applied, a film of conductive and transparent indium-tin-oxide (ITO) is coated on the surface of the supporting substrate 7 so that the supporting substrate 7 side becomes a conductor, and a low-melting glass film 6 made of low-melting glass (PbO-ZnO-B_2O_3) is deposited on the surface of the ITO film 9.

[0012] Then, a conductive paste 8 is applied on each side surface of the supporting substrate 7 and the silicon layer 1c, and a voltage is applied so that a negative DC voltage is applied to the supporting substrate 7 side on which the low melting point glass film 6 is deposited, so that the low melting point glass film 6 and the silicon layer 1c can be bonded to each other. This allows the supporting substrate 7 and the silicon layer 1c to be bonded together.

[0013] Also, as shown in FIG. 1(b), when a low melting point glass film 6 is formed on the surface of the silicon layer 1c, a DC voltage was applied so that a negative DC voltage was applied to the silicon layer 1c, contrary to the case of FIG. 1(a), pressure-bonding the low melting point glass film 6 and the ITO film 9. This allows the supporting substrate 7 and the silicon layer 1c to bond together.

[0014] The thickness of the low melting point glass (PbO-ZnO-B_2O_3) film used for this bonding is as follows: When bonding is performed with a resin layer, it is possible to bond with a layer having a thickness of 1 μm or less, which [previously] cannot be realized, and since no bubbles remain as in the case, when it is bonded with a resin, peeling off does not occur, even if the semiconductor device is exposed to room temperature, which is a non-operating temperatures from 77°K, which is the operating temperature of liquid nitrogen.

[0015]

[Embodiments] Embodiments using an SOI substrate in which a silicon layer is formed on a silicon plate according to the present invention will be described in detail below with reference to FIGS. 1 to 3 below.

[0016] FIG. 1 is a diagram showing an embodiment of room-temperature anodic bonding of the present invention; FIG. 2 is a side cross-sectional view (1) showing a method of manufacturing a semiconductor device according to an embodiment of the present invention in order of steps; and FIG. 3 is a side cross-sectional view (2) showing the manufacturing method of a semiconductor device according to one embodiment of the present invention in order of steps.

[0017] First, as shown in FIG. 2(a), after forming the semiconductor element 2, by the CMOS process, on the silicon layer 1c side of the SOI substrate 1 having a silicon oxide film 1b with a thickness of 1 μm and a silicon layer 1c with a thickness of 5 to 15 μm formed on a silicon plate 1a with a thickness of 400 μm, a polymer resin 3 made of polyimide resin (manufactured by Hitachi Chemical Co., Ltd., product name: PIQ) is applied to the entire surface of the forming region of the semiconductor element 2 thus formed to flatten the forming region of the semiconductor element 2.

[0018] Next, as shown in FIG. 2(b), the flat surface of the polymer resin 3 covering the forming region of the semiconductor element 2, and a transparent supporting substrate 5 made of quartz are heated and bonded with melted wax. The reason why the transparent supporting substrate 5 is used here is to find and remove air bubbles in the wax film 4 to ensure bonding.

[0019] Then, as shown in FIG. 2(c), the silicon plate 1a of the SOI substrate 1 on the side opposite to the side on which the semiconductor element 2 is formed is polished by about 360 μm, and the polishing is stopped just before reaching the silicon oxide film 1b, and etching is performed using an etchant made of caustic potash until reaching the interface with the silicon oxide film 1b of the SOI substrate 1, or alternatively, the remaining silicon plate 1a is removed by dry etching, and the silicon oxide film 1b is removed using buffered hydrofluoric acid composed of ammonium fluoride (NH_4F) and hydrofluoric acid (HF).

[0020] Then, as shown in FIG. 3(a), in order to give electrical conductivity to the supporting substrate 7 made of sapphire and having a thermal expansion coefficient matching that of the silicon layer 1c on which the semiconductor chip 2 is formed, an ITO layer 9 made of indium-tin-oxide (hereinafter abbreviated as ITO) and having a thickness of 0.3 μm is formed by sputtering, and after forming a low melting point glass (PbO-ZnO-B_2O_3) film 6 with a thickness of 0.5 μm on the surface of the ITO layer 9 by sputtering, as shown in FIG. 1(a), the side surface of the silicon layer 1c and the side surface of the supporting substrate 7 are coated with a conductive paste 8.

[0021] When DC power supply 10 applies a DC voltage of several tens of volts to apply a voltage, so that a negative DC voltage is applied to the supporting substrate 7 coated with the low melting point glass (PbO-ZnO-B_2O_3) film 6, and a positive DC voltage is applied to the silicon layer 1c side, the ITO film 9 on the surface of the supporting substrate 7 and the silicon layer 1c can be firmly bonded via the low melting point glass film 6. At this time, applying pressure by placing a weight on the substrate can lower the applied voltage.

[0022] After that, the wax film 4 is softened by immersing it in boiled pure water, as shown in FIG. 3(b), the transparent supporting substrate 5 is separated from the thinned silicon layer 1c, as shown in FIG. 3(c), the remaining wax film 4 is removed using an organic solvent such as xylene, and the polymer resin 3 is removed using a PIQ etchant to complete the fabrication of the semiconductor device.

[0023] In this embodiment, although the low melting point glass film 6 was formed on the surface of the ITO film 9 formed on the surface of the supporting substrate 7 in the step of bonding the supporting substrate 7 in FIG. 3(a), it is also possible to apply only the ITO layer 9 to the supporting substrate 7 and form the low melting point glass film 6 on the surface of the silicon layer 1c. In this case, as shown in FIG. 1(b), contrary to FIG. 1(a), the negative terminal of the DC power supply 10 must be connected to the conductive paste 8 formed on the side of the silicon layer 1c.

[0024]

[Effect of the Invention] As is clear from the above description, using the room temperature anodic bonding method of the

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present invention will not allow air bubbles to be mixed in the adhesion layer, when bonding a thinned silicon layer after forming a semiconductor element to a supporting substrate, and it becomes possible to bond in a state where the bonding strength is increased. The semiconductor element formed on the thinned silicon substrate has the advantage of the thinned silicon substrate not peeling off from the supporting substrate, even when exposed from a low operating temperature to non-operating room temperature, so it is possible to provide a manufacturing method of semiconductor devices that can be expected to have significant economic and reliability improvement effects.

[Brief Description of the Drawings]

[FIG. 1] a diagram showing an embodiment of the present invention

[FIG. 2] a side sectional view (1) showing a method of manufacturing a semiconductor device according to an embodiment of the present invention in order of steps

[FIG. 3] a side sectional view (2) showing a method of manufacturing a semiconductor device according to an embodiment of the present invention in order of steps

[FIG. 4] a diagram explaining room temperature anodic bonding

[FIG. 5] a sectional side elevation showing the configuration of the conventional semiconductor device

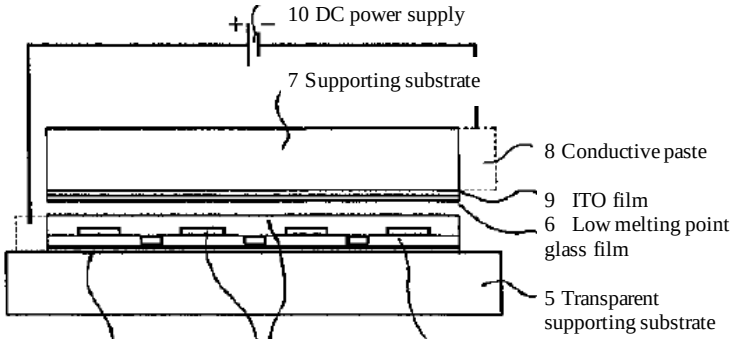
[Explanation of References]

1 SOI substrate
1a Silicon plate
1b Silicon oxide film
1c Silicon layer
2 Semiconductor element
3 Polymer resin
4 Wax film
5 Transparent supporting substrate
6 Low melting point glass film
7 Supporting substrate
8 Conductive paste
9 ITO film

(FIG. 1)

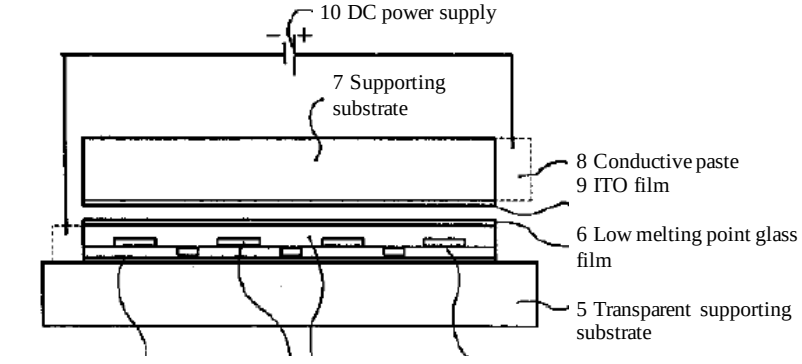
A diagram showing an embodiment of the present invention

(a) A schematic diagram of an embodiment in the state of anodic bonding



4 Wax film 2 Semiconductor element 1c Silicon layer 3 Polymer resin

(b) A schematic diagram of another embodiment in the state of anodic bonding

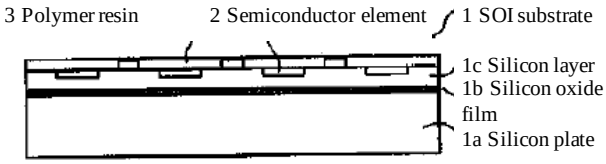


4 Wax film 2 Semiconductor element 1c Silicon layer 3 Polymer resin

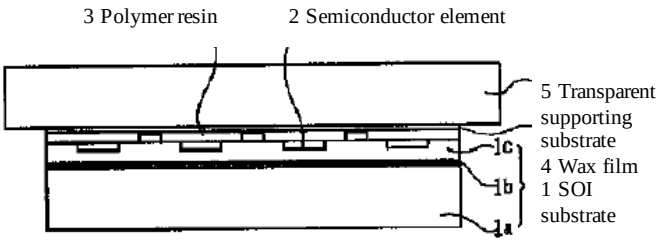
(FIG. 2)

A side sectional view (1) showing a method of manufacturing a semiconductor device according to an embodiment of the present invention in order of steps

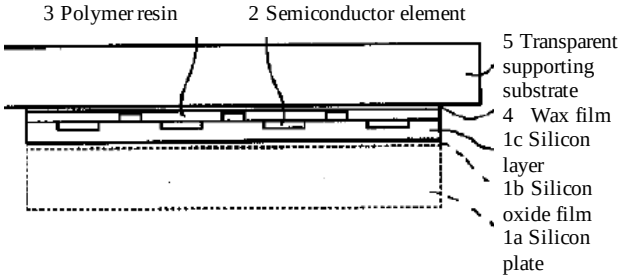
(a) The shape of semiconductor element (2) and coating of polymer resin (3)



(b) Coating to transparent supporting substrate (5)



(c) Polishing the silicon plate (1a) and etching the silicon oxide film (1b)



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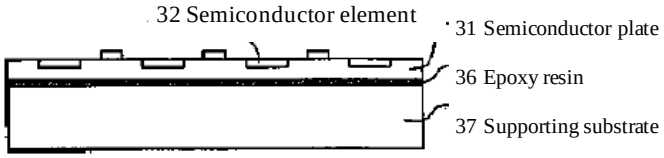
(FIG. 5)

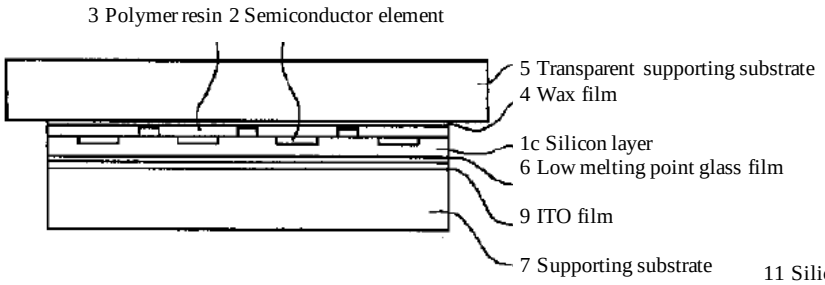
A sectional side elevation showing the configuration of the conventional semiconductor device



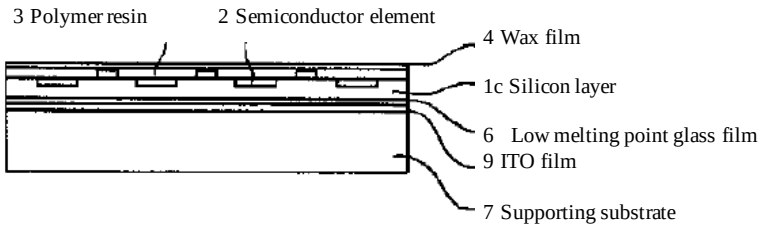
(FIG. 3)

A side sectional view (2) showing a method of manufac
device according to an embodiment of the present invention in order of steps

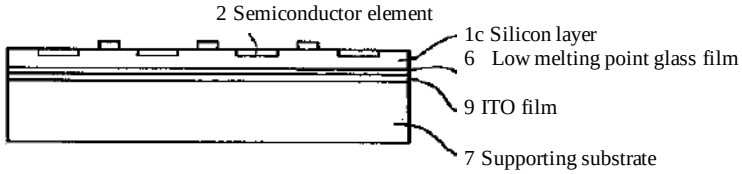
(a) Bonding of supporting substrate (7)



(b) Peeling off of transparent supporting substrate (5)

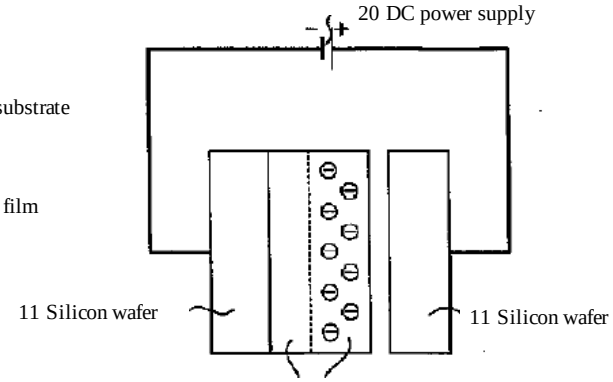


(c) Removal of wax film (4) and polymer resin (3)



(FIG. 4)

A diagram explaining room temperature anodic bonding



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27/14				
		7210－4Ｍ	Ｈ０１Ｌ　27/ 14	Ｋ

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(54)【発明の名称】　半導体装置の製造方法

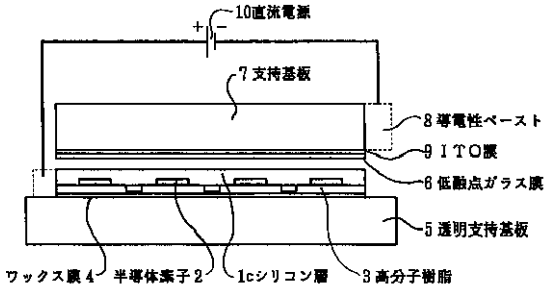
(57)【要約】

【目的】　半導体装置を形成して薄層化した基板を他の支持基板に転写する半導体装置の製造方法に関し、この薄層化した基板を絶縁性の支持基板に気泡などを発生させないで、強固に接着できる半導体装置の製造方法の提供を目的とする。

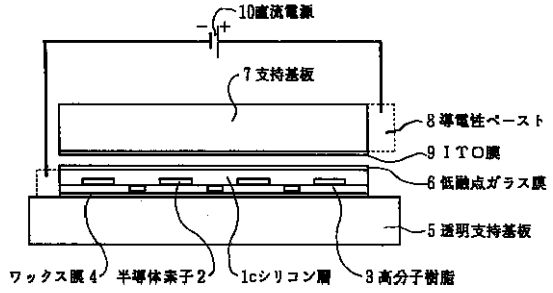
【構成】　ＳＯＩ基板のシリコン層1cの表面に半導体素子２を形成した後、この半導体素子２形成領域に高分子樹脂３を埋設して平坦化し、この高分子樹脂３と透明支持基板５とを接着し、この半導体素子２形成領域と対向する側のこのＳＯＩ基板のこの絶縁体側を研磨してシリコン層1cを薄層化する裏面入射型の赤外線検知素子の製造工程において、薄層化したこのシリコン層1cを、絶縁性を有し且つ赤外線を透過する支持基板７に、低融点ガラス膜６を介して、直流電圧を印加しながら、常温において接合する工程と、この高分子樹脂３からこの透明支持基板５を剥離し、この高分子樹脂３を除去する工程とを含むように構成する。

本発明の常温陽極接合の実施例を示す図

(a) 陽極接合状態の一例の構成図



(b) 陽極接合状態の他の例の構成図



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【特許請求の範囲】
【請求項１】　シリコン基板、或いは絶縁体(1a)上にシリコン層(1c)を設けたＳＯＩ基板(1) の前記シリコン層(1c)の表面に半導体素子(2) を形成した後、該半導体素子(2)形成領域に樹脂(3)を埋設して該半導体素子(2) 形成領域を平坦化し、該半導体素子(2)形成領域を埋設して平坦化した前記樹脂(3)と透明支持基板(5) とを接着し、前記半導体素子(2) 形成領域と対向する側の前記シリコン基板、或いは前記ＳＯＩ基板(1) の前記絶縁体(1a)側を研磨してシリコン層(1c)を薄層化する裏面入射型の赤外線検知素子の製造工程において、
薄層化した前記シリコン基板、或いは前記シリコン層(1c)を、絶縁性を有し且つ赤外線を透過する支持基板(7) に、低融点ガラス膜(6) を介して、直流電圧を印加しながら、常温において接合する工程と、
前記半導体素子(2) を埋設した前記樹脂(3) から前記透明支持基板(5) を剥離し、埋設した前記樹脂(3) を除去する工程と、
を含むことを特徴とする半導体装置の製造方法。

【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は半導体撮像素子や、ポリシリコン等で歯車等の微小機械部品を形成したマイクロマシン等に係り、特に半導体装置を形成して薄層化した基板を他の支持基板に転写する半導体装置の製造方法に関するものである。
【０００２】
【従来の技術】従来はシリコン等の半導体基板にＣＭＯＳ型の半導体素子を形成して赤外線検知素子を製造する場合には、このシリコン基板表面にはシリコン酸化膜や、電極や配線層等が形成されており、このシリコン基板の半導体素子を形成した面側から赤外線を入射すると、上記の配線層や電極で赤外線が遮蔽されて半導体素子形成領域に入射しないので、高感度の赤外線撮像素子を製造するには、シリコン基板の半導体素子を形成していない裏面側より赤外線を入射する裏面入射型の赤外線検知素子が製造されている。
【０００３】しかし、シリコン基板の板厚が厚い場合には、裏面側より入射した赤外線がシリコン基板に吸収され易いので、シリコン基板の板厚は10μｍ 以下に薄くしなければならないが、このようにシリコン基板を10μｍ以下の薄板にすると、割れやすくなり取扱が困難であるという問題が生じている。
【０００４】このため従来は、図５に示すように半導体素子32を形成した板厚が薄い半導体基板31を、赤外線を透過するサファイア等からなる絶縁性の支持基板37にエポキシ樹脂36を用いて接着する方法を採用している。
【０００５】
【発明が解決しようとする課題】以上説明した従来の半導体装置の製造方法においては、上記のように接着剤を用いて半導体基板を赤外線を透過するサファイア等からなる絶縁性の支持基板に接着しているが、接着剤を均一に薄く引き伸ばして接着することは技術的に非常に困難であり、また接着剤の内部に気泡が形成され易く、このように半導体基板を支持基板に接着して製造した赤外線撮像素子を、動作温度の液体窒素の温度から動作させていない場合の室内の温度に曝すと、気泡内の空気が温度差によって膨張し、接着剤にひび割れが発生するという問題点があった。
【０００６】本発明は以上のような状況から、半導体素子を形成して薄層化した半導体基板を絶縁性の支持基板に接着する際に、気泡などを発生させないで、強固に接着することが可能となる半導体装置の製造方法の提供を目的としたものである。
【０００７】
【課題を解決するための手段】本発明の半導体装置の製造方法は、シリコン基板、或いは絶縁体上にシリコン層を設けたＳＯＩ基板のこのシリコン層の表面に半導体素子を形成した後、この半導体素子形成領域に樹脂を埋設してこの半導体素子形成領域を平坦化し、この半導体素子形成領域を埋設して平坦化したこの樹脂と透明支持基板とを接着し、この半導体素子形成領域と対向する側のこのシリコン基板、或いはこのＳＯＩ基板の前記絶縁体側を研磨してシリコン層を薄層化する裏面入射型の赤外線検知素子の製造工程において、薄層化した前記シリコン基板、或いは前記シリコン層を、絶縁性を有し且つ赤外線を透過する支持基板に、低融点ガラス膜を介して、直流電圧を印加しながら、常温において接合する工程と、この半導体素子を埋設したこの樹脂からこの透明支持基板を剥離し、埋設したこの樹脂を除去する工程とを含むように構成する。
【０００８】
【作用】即ち本発明においては、半導体層の一方の面に半導体素子を形成した後、薄層化した半導体層と、この半導体層と同様な熱膨張係数を有し、赤外線を透過して絶縁性を有する支持基板とを常温陽極接合により接着するので強固に接着することが可能となり、半導体装置を動作温度の液体窒素温度の77° Ｋから非動作温度の室温に曝す場合においても、この半導体層が支持基板から剥離するのを防止することが可能となる。
【０００９】この常温陽極接合は文献（Sensors and Actuators,A-21-A23(1990)931-934)の"LoW-temperature Silicon-to-silicon Anodic Bonding with Intermediate LowMelting Point Glass,by MASAYOSHI ESASHI,AKIRA NAKANO,SHUICHI SHOJI andHIROYUKI HEBIGUCHI"において開示されている。
【００１０】この文献によれば、この方法は図４に示すように一方のシリコンウエーハ11にガラス層16をスパッタ法で被着し、他方の接着すべきシリコンウエーハ21と対向させて配置し、直流電源20によりガラス層16をスパ

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ッタしたシリコンウエーハ11に負の直流電圧が印加されるように電圧を印加すると、印加された直流電圧の電界によってスパッタされているガラス層16の一部に負のイオンが集合して分極領域16a が形成され、正の電圧が印加されている他方のシリコンウエーハ21にこの分極領域内の負のイオンが引きつけられてシリコンウエーハ同士が接着される方法である。

【００１１】本発明においては、この原理を利用し、図１(a) に示すように電圧が確実に印加されるように、支持基板７側が導体になるように支持基板７の表面に導電性で透明なインジウム・錫・酸化物（ＩＴＯ）の膜を被着し、このＩＴＯ膜９の表面に低融点ガラス（$PbO-ZnO-B_2O_3$）からなる低融点ガラス膜６を被着する。

【００１２】そして支持基板７およびシリコン層1cのそれぞれの側面に導電性ペースト８を塗布し、低融点ガラス膜６を被着した支持基板７側に負の直流電圧が印加されるように電圧を印加して低融点ガラス膜６とシリコン層1cとを圧着すると、支持基板７とシリコン層1cとを接着することが可能である。

【００１３】また図１(b) に示すようにシリコン層1cの表面に低融点ガラス膜６を形成した場合には、直流電圧を図１(a) の場合とは反対にシリコン層1cに負の直流電圧が印加されるように電圧を印加して低融点ガラス膜６とＩＴＯ膜９とを圧着すると、支持基板７とシリコン層1cとを接着することが可能である。

【００１４】この接着に用いる低融点ガラス（$PbO-ZnO-B_2O_3$）膜の厚さは、樹脂層で接着する場合には実現不可能な１μm 以下の厚さの層で接着することが可能であり、樹脂で接着した場合のように気泡が残留しないので、半導体装置を動作温度の液体窒素温度の77°Ｋから室温の非動作温度に曝しても剥離することはない。

【００１５】

【実施例】以下図１～図３により本発明のシリコン板上にシリコン層を形成したＳＯＩ基板を用いる一実施例について詳細に説明する。

【００１６】図１は本発明の常温陽極接合の実施例を示す図、図２は本発明による一実施例の半導体装置の製造方法を工程順に示す側断面図(1) 、図３は本発明による一実施例の半導体装置の製造方法を工程順に示す側断面図(2) である。

【００１７】まず図２(a) に示すように、板厚 400μm のシリコン板1a上に膜厚１μm のシリコン酸化膜1bと膜厚５～15μm のシリコン層1cを形成したＳＯＩ基板１の、シリコン層1c側にＣＭＯＳプロセスで半導体素子２を形成した後、この形成した半導体素子２の形成領域の全面にポリイミド樹脂(日立化成社製、商品名：ＰＩＱ)からなる高分子樹脂３を塗布してこの半導体素子２の形成領域側を平坦にする。

【００１８】つぎに、図２(b) に示すように、この半導体素子２の形成領域を被覆している高分子樹脂３の平坦な表面と、石英からなる透明支持基板５とを加熱し溶融したワックスを用いて接着する。ここで透明支持基板５を用いるのは、ワックス膜４の気泡を見つけて除去し、接着を確実にするためである。

【００１９】ついで図２(c) に示すように、半導体素子２を形成した側の反対側のＳＯＩ基板１のシリコン板1aを約 360μm 研磨してシリコン酸化膜1bに到達する直前で研磨を停止し、ＳＯＩ基板１のシリコン酸化膜1bとの界面に到達するまで苛性カリからなるエッチング液を用いるエッチングか、或いはドライエッチングにより残余のシリコン板1aを除去し、弗化アンモン(NH_4F) と弗酸（ＨＦ）とからなるバッファード弗酸を用いてシリコン酸化膜1bを除去する。

【００２０】ついで図３(a) に示すように、この半導体素子２を形成したシリコン層1cと熱膨張率が合致した、サファイヤからなる支持基板７に導電性を持たせるために、インジウム・錫・酸化物（以下、ＩＴＯと略称する。）からなる膜厚 0.3μm のＩＴＯ層９をスパッタ法により形成し、このＩＴＯ層９の表面に膜厚 0.5μm の低融点ガラス（$PbO-ZnO-B_2O_3$）膜６をスパッタ法により形成した後、図１(a) に示すようにシリコン層1cの側面と支持基板７の側面に導電性ペースト８を被着させて形成する。

【００２１】前記の低融点ガラス（$PbO-ZnO-B_2O_3$）膜６を被着した支持基板７に負の直流電圧が印加されるように電圧を印加し、シリコン層1c側に正の直流電圧が印加されるように電圧を印加した状態で直流電源10により数10Ｖの直流電圧を印加すると、支持基板７の表面のＩＴＯ膜９とシリコン層1cとを低融点ガラス膜６を介して強固に接着することが可能となる。この際、基板上に錘を載せて加圧すると、印加電圧を低くすることが可能となる。

【００２２】その後、煮沸した純水中に浸漬してワックス膜４を軟化させ、図３(b) に示すように薄層化したシリコン層1cから透明支持基板５を剥離し、図３(c) に示すようにキシレン等の有機溶剤を用いて残留しているワックス膜４を除去し、ＰＩＱエッチャント液を用いて高分子樹脂３を除去して半導体装置の製造が完了する。

【００２３】本実施例では、図３(a) の支持基板７の接着工程において低融点ガラス膜６を支持基板７の表面に形成したＩＴＯ膜９の表面に形成したが、支持基板７にはＩＴＯ層９のみを被着し、シリコン層1cの表面に低融点ガラス膜６を形成する方法も可能であり、この場合には図１(b) に示すように図１(a) とは逆に、直流電源10の負の端子をシリコン層1cの側面に形成した導電性ペースト８に接続しなければならない。

【００２４】

【発明の効果】以上の説明から明らかなように、本発明の常温陽極接合法を用いると、半導体素子を形成して薄層化したシリコン層を支持基板に接着する際に接着層に

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気泡を混入させず、且つ接着強度を高めた状態で接着することが可能となり、この薄層化したシリコン基板に形成した半導体素子を動作温度の低温から、非動作温度の室温に曝した場合においても、支持基板から薄層化したシリコン基板が剥離しない等の利点があり、著しい経済的及び、信頼性向上の効果が期待できる半導体装置の製造方法の提供が可能である。

【図面の簡単な説明】

【図１】　本発明の常温陽極接合の実施例を示す図

【図２】　本発明による一実施例の半導体装置の製造方法を工程順に示す側断面図(1)

【図３】　本発明による一実施例の半導体装置の製造方法を工程順に示す側断面図(2)

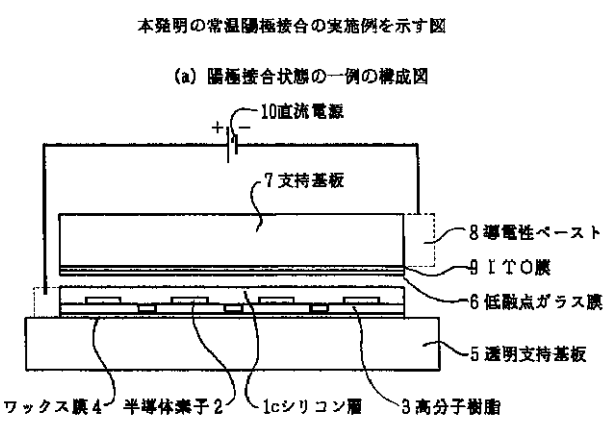
【図４】　常温陽極接合を説明する図

【図５】　従来の半導体装置の構成を示す側断面図

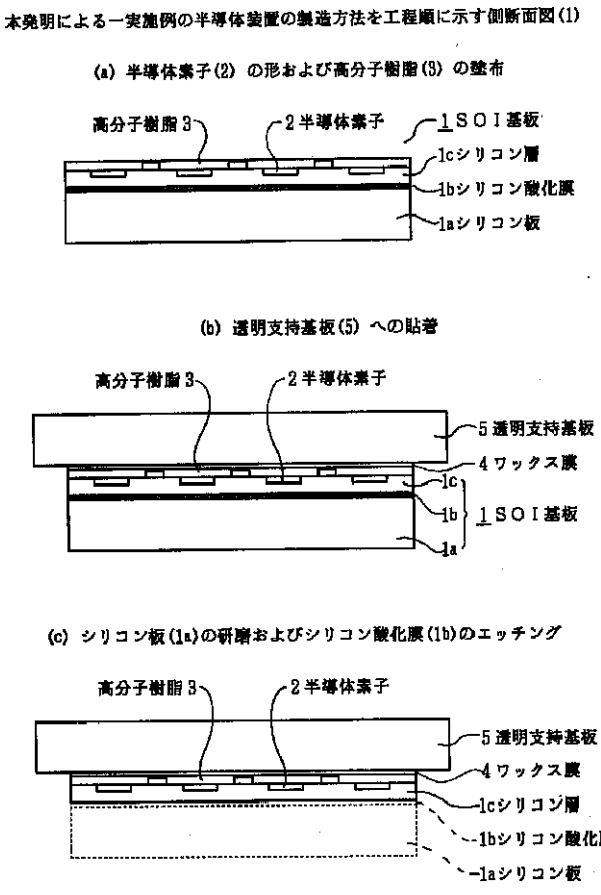
【符号の説明】

１　ＳＯＩ基板
1a　シリコン板
1b　シリコン酸化膜
1c　シリコン層
２　半導体素子
３　高分子樹脂
４　ワックス膜
５　透明支持基板
６　低融点ガラス膜
７　支持基板
８　導電性ペースト
９　ＩＴＯ膜

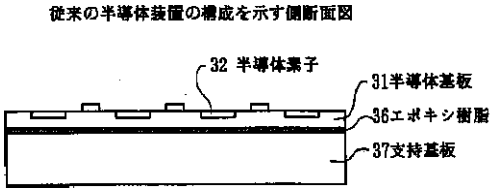
【図１】



【図２】



【図５】



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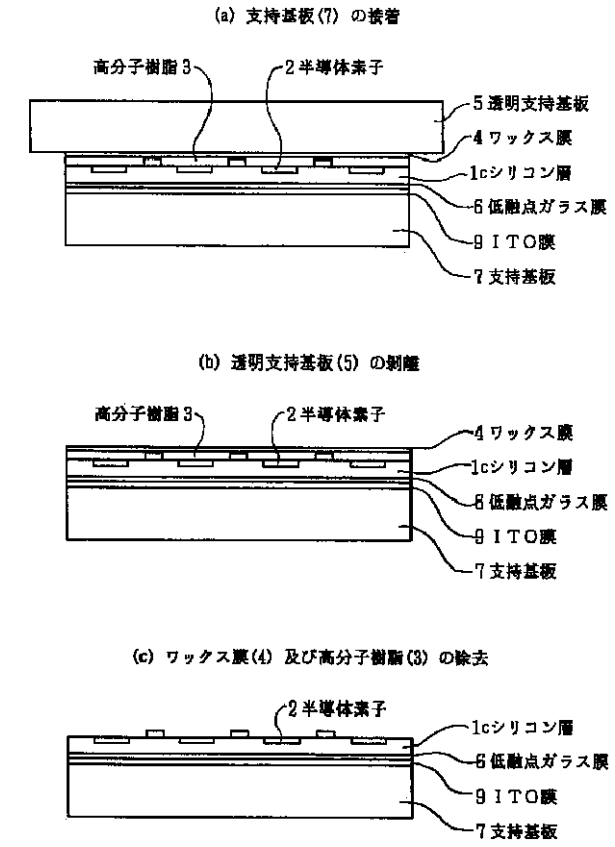
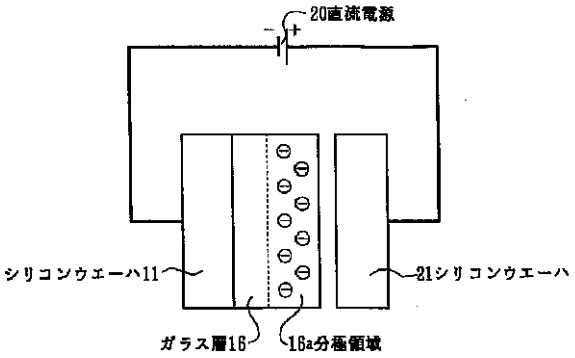
【図３】

本発明による一実施例の半導体装置の製造方法を工程順に示す側断面図(2)



【図４】

常温陽極接合を説明する図



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TRANSPERFECT

I, **Peter Gold,** declare as follows:

1. I am over eighteen years of age and fully competent to make this affidavit. I have personal knowledge of the information contained in this affidavit, and it is true and accurate to the best of my knowledge.

2. I am a translator fluent in the Japanese and English languages. I provide this affidavit on behalf of TransPerfect.

3. I translated "JPH06-268183" from Japanese to English and attest that it is a true and accurate translation.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on the information and belief are believed to be true; I declare under penalty of perjury that the foregoing is true and correct, and understand that willful false statements and the like are punishable by fine or imprisonment, or both pursuant to 18 U.S.C. 1001.

Peter L. Gold

LINGUIST NAME

Signature of Linguist